Fast Offset Compensation for a 10Gbps Limit Amplifier

by

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Bachelor of Science in Electrical Engineering and Computer Science,
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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

A novel offset voltage compensation method is presented that significantly modifies the existing tradeoff between control loop bandwidth, and therefore total compensation time, and total output jitter. The proposed system achieves comparable output jitter performance to traditional approaches while significantly reducing the total compensation time by nearly three orders of magnitude.

Traditional offset compensation methods are based on simple offset measurement techniques that generally rely on passive compensation blocks and exhibit a direct inverse relationship between total compensation time and resulting output jitter. Therefore, current high-speed data-link systems suffer from extremely long offset compensation loop settling times in order to satisfy the strict protocol jitter specifications. In the proposed system, the new CMOS peak detector design is the enabling component that allows us break this relationship and achieve extremely fast settling behavior while preventing data dependence of the control signal.

Simulated results show that the implemented system can achieve output jitter performance similar to existing methods while dramatically improving the compensation time. Specifically, the proposed system can achieve less than 2pS of peak-to-peak jitter, or less than 700fS of RMS jitter, while reducing the total compensation time from roughly 500μS to less than 1μS. The system was implemented in National Semiconductor's CMOS9 0.18μm CMOS process. Packaged parts will be tested to verify agreement with simulated performance.

Thesis Supervisor: Michael H. Perrott
Title: Assistant Professor

"It is not the critic who counts: not the man who points out how the strong man stumbles or where the doer of deeds could have done better. The credit belongs to the man who is actually in the arena, whose face is marred by dust and sweat and blood, who strives valiantly, who errs and comes up short again and again, because there is no effort without error or shortcoming, but who knows the great enthusiasms, the great devotions, who spends himself for a worthy cause; who, at the best, knows, in the end, the triumph of high achievement, and who, at the worst, if he fails, at least he fails while daring greatly, so that his place shall never be with those cold and timid souls who knew neither victory nor defeat."

Theodore Roosevelt
University of Paris, Sorbonne
April 23, 1910

Acknowledgments

It was a significant decision to leave the work force, uproot my entire family from their home and friends and return to academia after an eight year hiatus. The path has not been without its trials and and I was tempted to give in on more than one occasion. That is why I feel extremely lucky to have an incredible group of friends, family, lab partners and mentors that helped me along the way. I owe a debt of gratitude to several people who made it possible for me to complete my Masters of Engineering thesis and dare to continue with my PhD.

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Contents

1 Introduction **19**

1.1 Background 20

1.2 Motivation 22

1.2.1 Review of Offset Voltage 22

1.2.2 Impact of Offset Voltage on Amplifiers 23

1.3 Prior Offset Compensation Approaches 23

1.3.1 Sampled Offset Compensation 23

1.3.2 Low-Pass Filter Compensation 24

1.3.3 Other Approaches 25

1.4 Proposed Approach and Contribution 26

1.5 Thesis Organization 26

2 Proposed Approach **29**

2.1 Measuring Offset Voltage 29

2.1.1 Extracting the Offset Voltage with Min/Max Detectors 29

2.1.2 Issues with Sensing Offset with Min/Max Detectors 30

2.1.3 Extracting Offset with Simple Max Detectors 31

2.1.4 Issues with Sensing Output Referred Offset with Max Detectors 32

2.1.5 Final Peak Detector Design 33

2.2 Summary 34

3 System Modeling **37**

3.1 System Level Implementation 37

3.2 Linear System Modeling 39

3.2.1 Modeling System Response with PLL Design Assistant 42

3.2.2 Modeling the Impact of System Parameter Variation on Stability and Compensation Time 44

3.3 Summary 44

4 Numerical Design of High Speed Differential Amplifiers **47**

4.1 Methodology 47

4.2 Proposed Approach 49

4.2.1 Derivation of Gain/Swing Constraint Formulation 50

4.2.2 Derivation of Gain-Bandwidth Tradeoff 50

4.3 Intuitive Insights from Method 51

4.4 Results 52

4.5 Application to SCL Digital Circuits 53

4.6 Summary 54

5 Circuit Design of Systems Blocks **55**

5.1 High Speed Limit Amplifier 55

5.1.1 Determining Optimal Number of Stages 56

5.1.2 Bandwidth Extension Techniques 62

5.1.3 Final Amplifier Design 63

5.2 Peak Detector 64

5.3 Integrator 67

5.4 Output Buffer 74

5.5 Comparator and Logic 75

5.6 ESD 78

5.7 Summary 78

6 Results **79**

6.1 CppSim Modeling and Simulation Results 79

6.1.1 Limit Amplifier 79

6.1.2 Peak Detector 80

6.1.3 Integrator 80

6.1.4 Control Logic 81

6.2 CppSim Simulation Results 81

6.3 Hspice Simulation Results 81

6.4 Summary 82

7 Layout **87**

7.1 Peak Detector 87

7.2 Integrator 87

7.3 High Speed Limit Amplifier 88

7.4 Output Buffer 89

7.5 Top Level 90

7.6 Summary 91

8 Conclusions and Future Work **93**

8.1 Contributions 93

8.2 Future Work 94

A Derivation of Input Referred Offset Voltage **95**

A.0.1 Square-Law Operation 96

A.0.2 Velocity Saturation 97

B Circuit Design Details **99**

B.1 ESD Design 99

C CppSim Code 101

C.1 Limit Amplifier Code 101

C.2 Peak Detector Code 102

C.3 Integrator Code 102

D Optimal Gain/Stage for Maximum Bandwidth 103

D.0.1 Determining Optimal Number of Stages 103

E Matlab Amplifier Script 107

E.1 Script for Fixed Bandwidth 107

E.2 Script for Fixed Power Dissipation 112

List of Figures

1-1 Block Diagram of High-Speed Data Link System 20
1-2 High-Speed, Multi-Stage Limit Amplifier 21
1-3 Implementation of Each Stage in Limit Amplifier 21
1-4 LPF to Extract Output Referred Offset in High-Speed Data Link Systems 24

2-1 Measuring Output Referred Offset Voltage Using Minimum and Maximum Detectors 30
2-2 Traditional Implementations for Minimum and Maximum Detectors . 30
2-3 Influence of Symbol Period on Droop of Simple Peak Detector 32
2-4 Measuring Output Referred Offset Voltage Using Maximum Detectors Only 32
2-5 Schematic of Typical CMOS Maximum Detector 33
2-6 Schematic of Proposed Peak Detector with Reduced Droop 34
2-7 Comparison of Influence of Symbol Period on Droop of Simple Peak Detector vs Proposed Peak Detector Design 34

3-1 System Level of Limit Amplifier with Offset Compensation 38
3-2 Typical Transfer Function for Limit Amplifier Cell 38
3-3 Complete System Showing Multiple Control Loops and Logic 39
3-4 Linear Model of Limit Amplifier with Offset Compensation 41
3-5 Bode Plot Showing Stability Degradation with Increasing Gain 42

3-6 Root Locus Plot of G(s) Showing Necessary Condition for Stability . 43
3-7 PLL Design Assistant Graphical Interface 43
3-8 Step Response of System Designed with PLL Design Assistant 44
3-9 PLL Design Assistant Graphical Interface 45
3-10 Impact of ±20% Variation in Loop Gain and Dominant Pole Location on the Step Response of the System 45

4-1 Differential amplifier used in calculations. 48
4-2 Small signal model for amplifier. 49
4-3 Calculated Gain-Bandwidth product vs I_{den}. 52
4-4 Current density settings versus gain/swing. 53
4-5 Digital high speed circuits. 54

5-1 High-Speed, Multi-Stage Limit Amplifier 55
5-2 Number of Stages vs Total Bandwidth: Normalized Total Bandwidth vs Number of Stages for $G^{1/n} = A = 1.65$, 2.0 and 3.0 and Total Gains, G, of 10, 100 and 1000 57
5-3 Total Power Dissipation of Limit Amplifier for a Total Gain of 100 and Bandwidths/Stage from 2-10GHz 59
5-4 (a) Full Resistive-Loaded Differential Amplifier (b) Half-Circuit with Noise Sources Added (c) Half-Circuit with Noise Source Referred to Input 60
5-5 Total Input Referred Voltage Noise Versus Number of Amplifier Stages for a Fixed Total Gain 61
5-6 Minimum Input Voltage Versus Number of Amplifier Stages for a Fixed Total Gain 62
5-7 Limit Amplifier Stage with Neutralization Capacitors 63

5-8 Eye Diagrams for the Limit Amplifier at Data Rates of 5Gbps and 10Gbps and input amplitudes of 2mV, 20mV and 200mV peak-to-peak 65

5-9 Simplified Schematic of Fully Differential Peak Detector 66

5-10 Basic Differential RC Integrator 67

5-11 Simplified Schematic of Differential g_mC Integrator 68

5-12 Bode Plot of Modified Open-Loop Parameter A(s) 70

5-13 Schematic showing how integrator array is configured 71

5-14 Bode Plot of integrator demonstrate how transfer function varies with n, the number of parallel integrator cells 72

5-15 (a) CMFB with Resistive Output Common-Mode Level Sensing, (b) CMFB Using Differential Amplifier to Sense Output Common-Mode Level 73

5-16 Simplified Schematic of Integrator Showing Biasing and CMFB . . . 73

5-17 Differential Package Model Showing the Bond Pad and Package Capacitance and the Bond Wire Inductance 74

5-18 Final Output Buffer Design 75

5-19 Eye Diagram at Output of Output Buffer (a) 5Gbps, (b) 10Gbps . . . 75

5-20 Typical Implementation of Clocked Comparator 76

5-21 Implementation of Comparator in Windowing Block 77

6-1 3rd Order Polynomial Fit to Limit Amplifier Transfer Function Measured in Hspice 80

6-2 Control voltage of offset compensation loop during compensation from CppSim: (A) 1MHz bandwidth, (B) 5MHz bandwidth, (C) 10 MHz Bandwidth 82

6-3 Eye diagram of limit amplifier output after compensation from CppSim 83

6-4 Control voltage of offset compensation loop during compensation from Hspice: (A) 1MHz bandwidth, (B) 5MHz bandwidth, (C) 10 MHz Bandwidth 84
6-5 Eye diagram of limit amplifier output after compensation from Hspice 85

7-1 Detail of Peak Detector Cell Showing Common-Centroid Layout and Dummy Devices 88
7-2 Layout of Base Integrator Cell 89
7-3 Layout of Integrator Array 89
7-4 Layout of Limit Amplifier Stage 90
7-5 Layout of Limit Amplifier Top Level 90
7-6 Layout of Output Buffer Stage 91
7-7 Layout of Output Buffer Top Level 91
7-8 Layout of Chip Top Level 92

A-1 Implementation of Each Stage in Limit Amplifier 95

B-1 Simplified schematic of ESD circuitry used on all pads 99
B-2 Layouts for the two pads with ESD structures 100

D-1 High-Speed, Multi-Stage Limit Amplifier 103

List of Tables

1.1 Typical vs Goal Performance Specifications for Offset Compensation . 26

4.1 Calculated vs simulated amplifier performance. 52

5.1 Simulated Hysteresis vs Process and Temperature Corner 77

Chapter 1

Introduction

In today's information age there is an ever increasing demand for products that deliver higher performance, lower power dissipation and smaller form factor than existing designs. New products that improve in these three areas will enable the continued exponential growth of the worldwide communication infrastructure. Ultimately, a combination of novel architectural and circuit techniques need to be developed to achieve this end.

Offset compensation is important for aggressive high speed design to achieve high input sensitivity and low DC offset. In traditional offset compensation implementations the data dependence of the control signal is proportional to the compensation loop bandwidth. As a result of this limitation, current approaches suffer from long compensation times and require expensive off-chip components to minimize data-dependent jitter and to meet protocol (i.e. SONET/SDH) jitter specifications. Manipulation of fundamental characteristics of the differential architecture allow us to modify this relationship in the proposed approach. The goal of this thesis is to develop a broadband limit amplifier with dynamic, fully integrated, continuous-time DC offset cancellation that achieves sub-$1\mu S$ compensation times while providing a low jitter, constant amplitude output. The limit amplifier will be used as the main amplifier in an optical network receiver. The chip has been implemented in National Semiconductor's CMOS9 $0.18\mu m$ CMOS process.

Additionally, a simple numerical procedure is introduced that enables straightforward design of high speed, resistor loaded, differential amplifiers in modern CMOS processes. The design procedure is beneficial because the device characteristics of modern CMOS processes dramatically depart from traditional square law characteristics. The analytical form of the procedure allows for an intuitive perspective of the varying gain-bandwidth product for such amplifiers. Calculations based on the method are compared to Hspice simulated results based on a National Semiconductor's 0.18u CMOS process. Application of the design methodology to the design of high speed, source-coupled logic (SCL) gates and latches is also discussed.

1.1 Background

One well established industry standard for broadband optical fiber networks known as SONET, or Synchronous Optical NETwork, is defined for various data speeds. Operating at a data rate of 10Gbps, the OC-192 SONET standard allows for very high data transfer rates on optical fiber cable over long distances. One obstacle to achieving the desired performance is DC offset in the data link. The offset can be introduced by the transmitter, the transmit path or the circuit components in the front-end receiver. The desire to reduce the cost structure and improve the efficiency of these networks will increase the demand for quick power-up and switching between multiple incoming links. This demand will drive the need for fast DC offset compensation.

Figure 1-1 exhibits a block diagram of a modern optical-link system. At the transmit end of the fiber cable, a laser driver feeds a synchronous, Non-Return to Zero (NRZ) data stream into the cable, which can range in length from tens to thousands of kilometers. Sending distinct clock and data signals would require separate, dedicated cables and would be prohibitively expensive. Therefore, a single serial data stream is transmitted with the clock encoded in the data transitions. At the receiver end of the cable an avalanche photo-diode drives a Transimpedance Amplifier (TIA) that translates the current signal to a voltage signal. The output of the TIA then feeds the main amplifier, which is the focus of this thesis. The main amplifier must amplify this small voltage signal to a large enough level so that the clock and data recovery (CDR) circuitry can operate reliably. The purpose of the CDR is to extract the clock signal from the data stream and re-time the data to the new, synchronized clock signal.

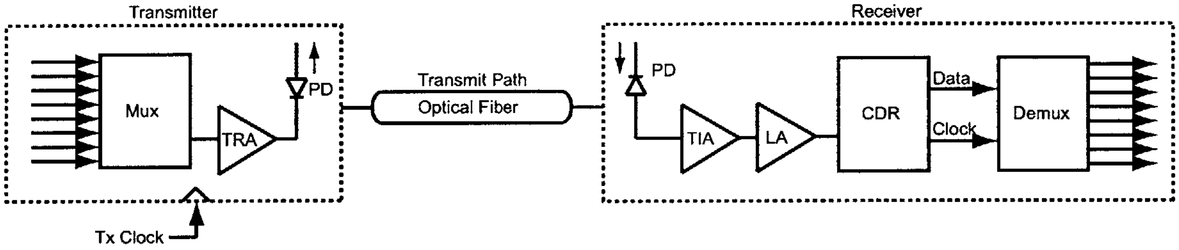


Figure 1-1: Block Diagram of High-Speed Data Link System

The overall design goal of the main amplifier is to increase the signal strength without degrading the SNR achieved by the system front-end. Additionally, the amplifier must provide a low jitter, constant amplitude input to the CDR. There are two main architectures that can be used to implement the amplifier, namely an Automatic Gain Control (AGC) amplifier or a Limit Amplifier (LA). As the name suggests, the AGC amplifier dynamically adjusts its gain depending on the input amplitude to achieve a constant amplitude output signal. In contrast, the limit amplifier achieves the same effect by forcing the output to saturate at a known amplitude for input signals greater than some predetermined minimum amplitude. The limit amplifier design was selected for this work because it is more amenable to high-speed operation.

The key advantages of the limiting amplifier over the AGC are higher operating speed and lower implementation complexity. AGCs will exhibit inferior high-frequency characteristics compared to limit amplifiers because of the increased capacitive loading of the sense and feedback circuitry. Also, the added feedback network, for gain control, increases the design complexity. Therefore, the limiting amplifier topology was used in this thesis. A limit amplifier can be implemented as a cascade of resistively loaded differential pair amplifiers, as shown in Figure 1-2. Each of the amplifier blocks is implemented as differential pairs, as shown in Figure 1-3.

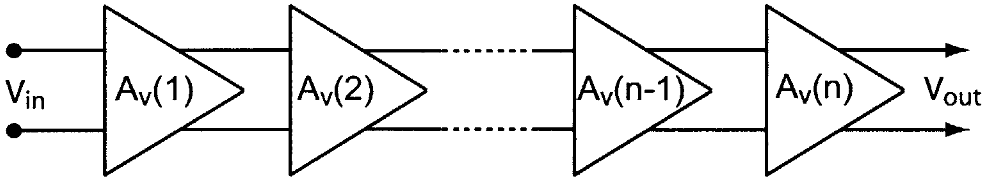


Figure 1-2: High-Speed, Multi-Stage Limit Amplifier

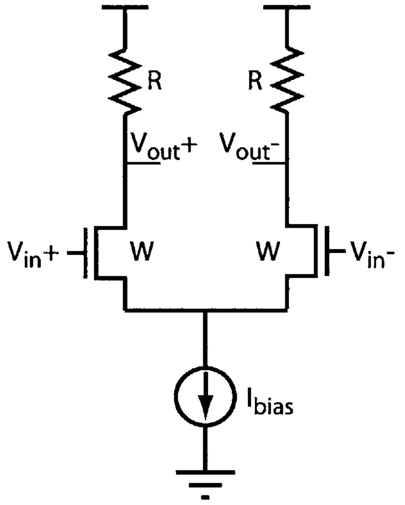


Figure 1-3: Implementation of Each Stage in Limit Amplifier

Cost is the fundamental driving force behind process selection for modern day integrated circuits. CMOS has become the process of choice compared to more specialized III-IV processes like SiGe, GaAs and InP due to the immense inertia behind process development in the PC market. However, this economic advantage does not come without added design challenges. CMOS presents its own unique problems for high speed design due to its lower f_t and higher 1/f noise corner compared to the afore mentioned processes. Despite these challenges, CMOS is the preferred technology due to its low cost, high integration density and fast paced technology development driven by Moore's Law.

1.2 Motivation

1.2.1 Review of Offset Voltage

As mentioned earlier, the data-link network suffers from two main sources of DC offset. The first source of offset is the received signal. The circuit components of the receiver are the other source of offset. The following section will examine the origin of these two sources of offset and the impact of the offset on the system.

The offset introduced by the incoming signal originates at the transmitter and is due to the power of the incoming signal. When the receiver initially powers up, the received signal power may introduce a DC offset in the receiver. Additionally, the magnitude of the offset can change when switching from one transmit path to another. Different power levels between the two transmit paths, caused by different output powers of the two transmitters or different losses in the transmit paths, will result in a change in the DC voltage offset of the receiver.

The main amplifier itself may also introduce a finite DC offset component due to mismatches in the differential paths. To understand the origin of the offset voltage, consider the resistively loaded differential pair shown in Figure 1-3. Assuming $V_{in} = 0$ and perfect symmetry, $V_{out} = 0$. However, this assumption is violated in practice due to device mismatches in transistor physical dimensions, threshold voltages and resistor values so that $V_{out} \neq 0$. The output referred offset voltage is defined as the voltage that exists at the output with $V_{in} = 0$. By convention, this voltage is referred to the input and the offset voltage is therefore the voltage that must be applied to the input to force $V_{out} = 0$. The input referred offset is related to the output referred offset voltage by $\mid V_{os,in} \mid = \mid \frac{V_{os,out}}{A_v} \mid$, where A_v is the gain of the amplifier.

It is beneficial to develop an expression for the offset voltage in terms of the circuit parameters to determine how we, as the designer, can minimize it. Assuming that the input devices operate in velocity saturation, the final expression for the input referred offset voltage is:

$$V_{os,in}^2 = (V_{GS} - V_{TH})^2 \cdot \left[\left(\frac{\Delta W}{W} \right)^2 + \left(\frac{\Delta R}{R} \right)^2 \right] + \Delta V_{TH}^2 \qquad (1.1)$$

where $(\Delta W/W)$, $(\Delta R/R)$ and $(\Delta V_{TH}/V_{TH})$ are the normalized variation in the transistor width, load resistance and transistor threshold voltage, respectively, of the amplifier. The reader is invited to refer to Appendix A for the full development. The resulting equation is similar to the result found in [1], where square-law operation was assumed. The exception is that a scaling in the magnitude of the over-drive term and no direct dependence on device length, L. The offset is indirectly dependent on L through the V_{TH}^2 term.

By examining this result some useful insights can be obtained. First, the offset voltage is dependent on transistor length mismatches through the dependence on threshold mismatches. Second, this analysis shows that threshold voltage mismatches are directly referred to the input and that mismatches in transistor width and load resistance are scaled by the transistor over-drive. Therefore, to minimize offset voltage, the transistor over-drives should be minimized by either reducing the bias current or by increasing the device widths. Reducing the bias current is only appropriate in low power (i.e. low-speed) designs. As will be shown in Chapter 4, the transistor widths and load resistance are not free variables when designing resistively loaded, differential amplifiers. The device dimensions and bias conditions are uniquely determined when the gain, output swing and either bandwidth or power are specified. Additionally, appropriate layout matching techniques such as common-centroid layout and using dummy devices/stripes to minimize device mismatch should be incorporated where appropriate. Unfortunately, as shown in Equation 1.1, the offset voltage of the amplifier can not be reduced to zero even if the utmost care is taken in the design and layout. In the next section we will explore the impact of DC offsets on the performance of the amplifier.

1.2.2 Impact of Offset Voltage on Amplifiers

Both the undesired input-referred offset and the desired input signal experience the large gain of the limit amplifier, which is usually on the order of 40dB to 60dB. Typical values of input-referred offset voltage can range from 1mV to 10mV since the high-speed amplifier stages are designed for maximum bandwidth at the expense of matching and offset issues. The input-referred offset can be comparable in magnitude to the input signal levels for high-speed optical receivers. For this reason, the offset voltage can decrease sensitivity to incoming signals or, even worse, drive the later stages into nonlinear operation and cause the outputs to saturate. In extreme cases, the offset can be large enough to block the desired signal. For these reasons, some form of offset compensation is required in modern, high-speed data-link systems.

1.3 Prior Offset Compensation Approaches

Several existing offset compensation techniques can be found in the literature. The existing approaches generally fall into one of two categories: active sampled systems or passive continuous time systems. We will explore the most significant methods in this section. Two important characteristics of each design are the compensation time and the data dependent output jitter. Long compensation times lead to loss of data and decrease system efficiency. One source of jitter in the output signal is data dependence of the offset compensation control signal. Unless the measured offset is sufficiently filtered in this method, the proportional control signal will lead to increased output jitter. All of the system discussed below exhibit a direct relationship between compensation time and output jitter.

1.3.1 Sampled Offset Compensation

The three most common offset compensation techniques that fall into the sampled system classification are auto-zeroing, correlated double sampling and chopper stabilization [2]. The basic principle behind auto-zeroing and correlated double sampling is to sample the undesired offset that exists in the system on one clock phase and to subtract it from the desired signal on the following clock phase. By design, both of these techniques require a clock and a sampling phase to measure the offset in the system, fundamentally limiting the maximum input data rate to half the sampling rate. Additionally, each of these techniques require sampling capacitors in the data path which can be quite large if designed for minimal noise. On the other hand, chopper stabilization achieves the same result by operating in the frequency domain. Compensation is performed by modulating the desired signal to a higher frequency, where the undesired offset and noise signals do not exist, performing the amplification on the modulated signal and finally demodulating the amplified signal back to baseband. Chopper-stabilization methods are fundamentally limited to low-speed applications because the residual offset, or the offset remaining after compensation, is proportional to the sampling rate. If the sampling rate is set too high, the residual offset will increase. Also, the forward path gain can be attenuated and the noise floor will increase due to the aliasing of the wide-band noise into the frequency band of interest. Ultimately, none of these techniques are amenable to high-speed, continuous-time systems.

1.3.2 Low-Pass Filter Compensation

By far, the most common technique for offset compensation in continuous time, high-speed, broadband systems is to use a low-pass filter in a feedback configuration [3, 4, 5], as shown in Figure 1-4. The bandwidth of the filter must be set sufficiently low to ensure stability of the overall system and to ensure that there is minimal data dependence of the control loop.

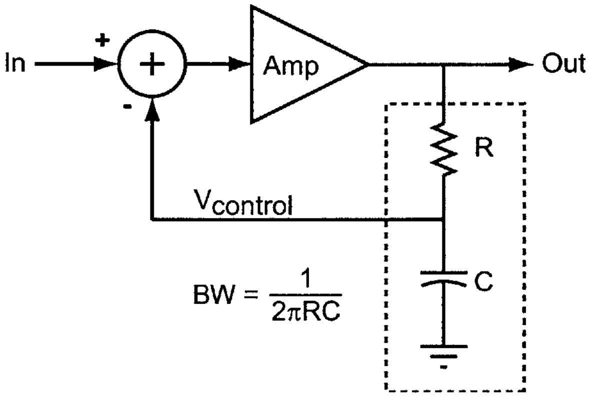


Figure 1-4: LPF to Extract Output Referred Offset in High-Speed Data Link Systems

Due to the requirement for such a low loop bandwidth, this design has two significant disadvantages. First, the very small loop bandwidth translates to a very large time constant for the loop dynamics which results in very long compensation times [6, 7]. Long compensation times will become a significant issue as emerging standards such as Optical Time-Division Multiplexing (OTDM) [8] and Dense-Wave

Division Multiplexing (DWDM) [9] take hold in commercial applications. Second, from the viewpoint of cost and ease of integration, the small bandwidth requirement results in large component values that are not economically feasible to implement on chip. Specifically capacitor values on the order of 10's of μF are required which would consume considerable silicon area if implemented on chip. The result is the need for expensive off-chip components.

1.3.3 Other Approaches

One of the earliest forms of offset compensation in the literature uses Minimum Mean-Square Estimation (MMSE) [10, 11]. Similar to Chopper Stabilization, MMSE performs the offset compensation in the frequency domain using adaptive equalizers. The equalizers, which are slowly time-varying linear filters, will insert a null in the transfer function at DC to compensate for DC offsets. One issue with this approach is that the magnitude of residual offset is proportional to both the number of filter taps and the magnitude of the uncompensated offset of the system. Therefore, low residual DC offset requires high equalizer complexity and a small input referred offset. As CMOS processes continue to scale the increased digital complexity required to implement the higher order filters will become less of an issue and this approach may become more feasible.

Another solution, implemented in a silicon bipolar process, uses peak detectors to measure the output referred DC offset (drift) of the main amplifier [11]. The output of the peak detector is low-pass filtered to reduce the data dependence of the control signal. Finally, the output of the low-pass filter feeds the input stage to perform the compensation. Similar to the low-pass filter approach, the data dependence of the control signal is proportional to the control loop bandwidth. To minimize the output jitter this design also suffers from very long compensation times.

An alternative solution, that also uses maximum detectors in the feedback loop to extract the output referred offset voltage, was proposed by Tanabe et al [12]. However, this design was implemented in a CMOS process. Compensation is performed by feeding the difference between the instantaneous maximum value of the two differential data signals to the input stage. Assuming a 50% duty cycle between high and low data transitions (i.e. the average value of the data is zero) and that the bandwidth of the maximum detector is sufficiently low, this implementation works as intended. However, this design suffers from the same limitations as previous approaches. Specifically, the data dependence of the control signal is directly related to the bandwidth of the compensation loop. When the data has extended periods with a non-zero mean value the control signal is data dependent. To minimize the data dependence of the control signal, the bandwidth of the maximum detector must be very low which leads to long compensation times.

All of the offset compensation designs considered above suffer from the same limitation. Namely, the magnitude of the output jitter is directly coupled to the offset compensation time. To reduce the output jitter in these designs the compensation loop bandwidth must be very low. This restriction results in long compensation times. The following section introduces the proposed approach which dramatically reduces the dependence of the output jitter on compensation time.

1.4 Proposed Approach and Contribution

There are two significant obstacles to designing a fast offset compensation network in CMOS. First accurately measuring the offset voltage of the system is difficult. The biggest reason for this is that CMOS transistors used to perform diode functions (i.e. source follower) have limited high frequency capability. Additionally, mismatches between the minimum (min) and maximum (max) detectors introduce error into the measurement. Second, it is difficult to simultaneously generate a control signal that is independent of the data while achieving fast settling performance. The reason for the difficulty is that the amount of droop at the output of the peak detector is proportional to the loop bandwidth in typical min/max detector designs.

The key contribution of this thesis is the development of a peak detector that enables the design of a fast offset compensation loop in CMOS processes that also meets strict jitter specifications. In traditional CMOS peak detectors the bandwidth is proportional to the bias current when the input is high. Similarly, when the input is low the amount of droop at the output is also proportional to I_{bias}. In the proposed peak detector this restriction has been practically eliminated. The bandwidth is still proportional to the bias current. However, the amount of droop at the output is now proportional to an NMOS transistor off-state leakage current. Since the off-state leakage current of modern CMOS devices is typically orders of magnitude less than the peak detector bias current, the amount of droop is also reduced by several orders of magnitude. This thesis focuses on the peak detector design and system implementation details.

Output jitter and settling time performance for typical offset compensation designs are compared to the targeted performance of the proposed approach in Table 1.1. Although the output jitter targets are identical, the settling time goal in the proposed solution is almost 3 orders of magnitude shorter than the typical design goals. The peak detector allows the proposed system to meet both the jitter and the aggressive settling time performance goals.

Specification	Typical Design	Proposed Design
Output Jitter	$< 2pS_{p-p}$	$< 2pS_{p-p}$
Settling Time	$\approx 500\mu S$	$< 1\mu S$

Table 1.1: Typical vs Goal Performance Specifications for Offset Compensation

1.5 Thesis Organization

This thesis is organized as follows. Chapter 2 introduces the proposed architecture to achieve the sub-$1\mu S$ offset compensation time while still satisfying the output jitter requirement of the CDR input. Chapter 3 discusses the linear modeling of the proposed system architecture and computes the system parameters required to guarantee stability and the desired dynamic response. Chapter 4 presents a novel, closed-form numerical methodology for designing resistively loaded, high-speed, differential amplifiers that make up the limit amplifier. Circuit design issues and CppSim and Hspice simulation details are discussed in Chapters 5 and 6, respectively. Important layout issues are discussed in Chapter 7. Finally, Chapter 8 presents conclusions and potential extensions for future work.

Chapter 2

Proposed Approach

2.1 Measuring Offset Voltage

The most significant obstacles to designing a fast offset compensation network are accurately measuring the offset voltage of the system and generating a control signal that is independent of the data. This chapter incrementally develops the proposed design of the key enabling component in the offset compensation loop, the peak detector.

2.1.1 Extracting the Offset Voltage with Min/Max Detectors

One possible solution for measuring the offset voltage of the limit amplifier is to take the difference between the common-mode voltages of each output signal [13]. The output common-mode level can be obtained by taking the average of the instantaneous maximum and minimum output values with max and min detectors, respectively, as shown in Figure 2-1. The max and min detectors can be either continuous time or sampled systems. Although high performance peak detectors have been designed in BiCMOS and Bipolar processes [14, 15, 16], it is not trivial to do so in CMOS processes. The fundamental design challenge is the limited high-frequency performance of CMOS transistors used to perform diode functions (i.e. source follower).

Typical maximum and minimum detector implementations are shown in Figure 2-2. The output of the minimum detector will track its input, plus a V_{GS} shift equal to $(V_{TH}+V_{DSAT})_{M1}$. Similarly, the output of the maximum detector will track its input, less a V_{GS} shift equal to $(V_{TH}+V_{DSAT})_{M2}$. In steady-state operation, both M1 and M2 remain on and either sink or source a current equal to I_{bias} such that the charge stored on C_{min} and C_{max} remains unchanged. If the output referred offset voltage increases $I_{D,M1}$ will decrease in order to cancel charge on C_{min}. V_{out} will increase until steady state conditions are met. Likewise, $I_{D,M2}$ will increase to add charge to C_{max} until steady state conditions are met. Conversely, if the output referred offset voltage decreases then $I_{D,M1}$ will increase and $I_{D,M2}$ will decrease until steady-state conditions are once again met.

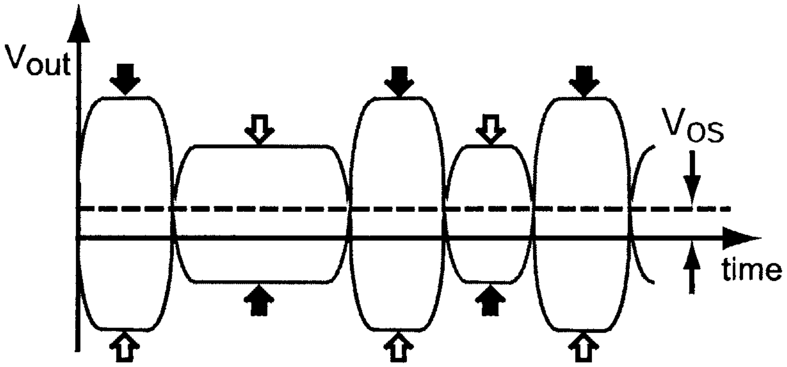


Figure 2-1: Measuring Output Referred Offset Voltage Using Minimum and Maximum Detectors

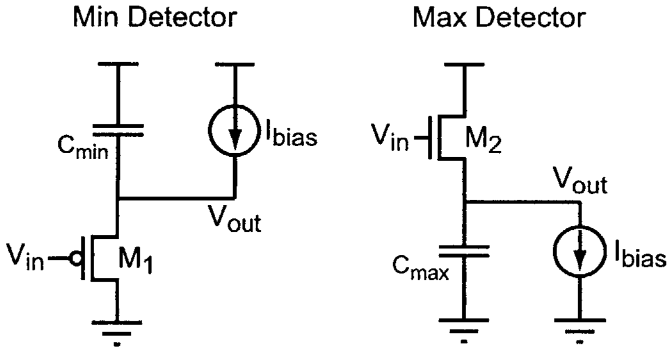


Figure 2-2: Traditional Implementations for Minimum and Maximum Detectors

2.1.2 Issues with Sensing Offset with Min/Max Detectors

There are two main issues with measuring the offset voltage with the different types of detectors, as shown in Figure 2-2. First, since we are attempting to measure the offset with min and max detectors that are based on PMOS and NMOS transistors, respectively, the accuracy of the measured offset is limited to the matching between the two device types. The transistor threshold voltages, transconductance and even physical dimensions will change with process, voltage and temperature variations and these changes will not necessarily track in the two devices. Ultimately, these differences will introduce offsets into the compensation loop and limit the effectiveness of the compensation.

To understand the second issue, we need to examine the max and min detectors' ability to track changes at their inputs. We will only consider the response of the max detector, here to referred to as a peak detector, and infer the min detector operation by extension.

For a unit change at the input, the output will follow by either adding charge to or subtracting charge from C_{max}. Consider first a step increase at the input. The output voltage will increase by M1 sourcing current onto C_{max} and the rate of change at the output will be limited by M1's transconductance. The ratio of the transconductance of M1 to C_{max} corresponds to the bandwidth of the peak detector while the device is on:

$$f_{3dB} = \frac{g_{m,M1}}{2\pi C_{max}} \tag{2.1}$$

Since g_m is proportional to the bias current, the bandwidth is also proportional to the bias current. If the bandwidth of the peak detector is much higher than the data rate then M1 will fully charge C_{max} so that the output will take on the correct value at each successive peak, thus operating as a zero order hold that samples the peaks of the input. If the bandwidth of the peak detector is set much lower than the data rate, the high frequency components of the input will be greatly attenuated and the output will track the lower frequency components of the input.

Alternately, consider a step decrease in the magnitude of the input signal. The output will slew according to the tail current source's ability to strip charge away from C_{max} and the change in the output voltage will be:

$$\delta V = \frac{I_{bias} - I_{M1}}{C_{max}} \cdot \delta t = \Delta \tag{2.2}$$

where δt is the data symbol period. The magnitude of the droop at the output is proportional to the bias current and the number of symbol periods that the input is low.

To understand why the asymmetric response of the peak detector is an issue, consider the case when the input is driven by a constant amplitude, Non-Return to Zero (NRZ), pseudo-random data stream whose amplitude does not change. Let us also assume that the peak detector operates in steady-state (i.e. the offset compensation has been performed), as shown in the top of Figure 2-3. When the input is high, the output of the peak detector will be refreshed to its correct value. However, when the input goes low, $V_{GS,M1}$ will be reduced so $I_{D,M1}$ will be either very low or zero and C_{max} will discharge according to Equation 2.2 as shown in the bottom of Figure 2-3. If the output is low for n symbol periods, then C_{max} will discharge according to:

$$\delta V = \frac{I_{bias}}{C_{max}} \cdot n\delta t = n\,\Delta \tag{2.3}$$

where and n is the number of successive low bits at the input. The total droop is defined as $n \cdot \Delta$. When the input goes high the output will return to the correct, steady-state value. Therefore, the measured offset voltage is data dependent and violates one of our design requirements for the offset compensation.

2.1.3 Extracting Offset with Simple Max Detectors

The offset issue due to the mismatch between the NMOS and PMOS devices in the max and min detectors can be solved by taking advantage of the symmetry of the limit

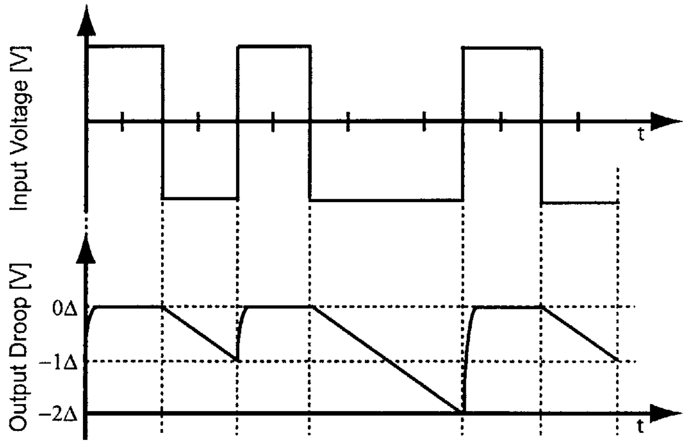


Figure 2-3: Influence of Symbol Period on Droop of Simple Peak Detector

amplifier structure. Since the data paths through the limit amplifier are differential and the amplifier stages are symmetric, the gains through each path are close to being equal, in practice. If the gains through each path are similar then the peak-to-peak values must also be equal. With zero offset in the limit amplifier, the peak values of the two paths must also be equal. However, as shown in Figure 2-4, if the output referred offset is non-zero then the peak values of two outputs will be different. In fact, the difference will equal the output referred offset and the max/min pair can be replaced by a simple peak detector, as shown in Figure 2-5. This observation eliminates the offset issue due to the mismatched min/max detectors [12].

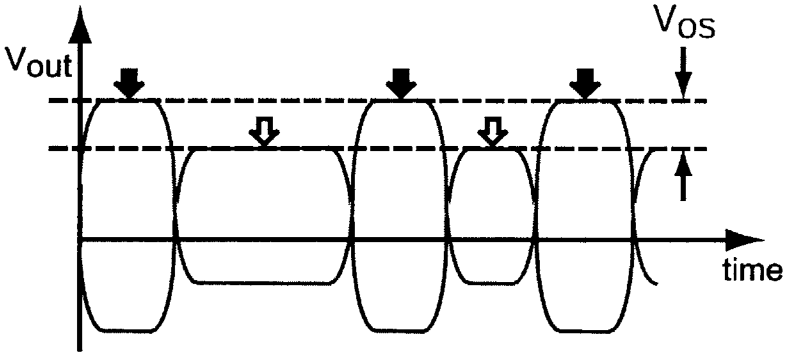


Figure 2-4: Measuring Output Referred Offset Voltage Using Maximum Detectors Only

2.1.4 Issues with Sensing Output Referred Offset with Max Detectors

The offset issue caused by mismatches between different type detectors has been solved by taking advantage of the symmetry of the limit amplifier stages. However, the basic architecture of the peak detector has not changed and it still suffers from

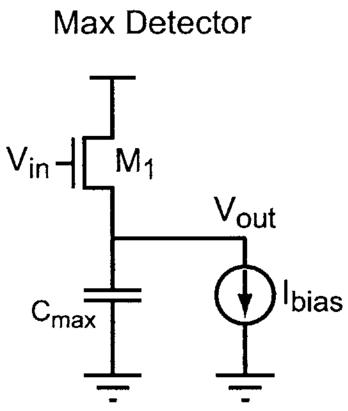


Figure 2-5: Schematic of Typical CMOS Maximum Detector

the same data dependence issue described in Section 2.1.2. To solve fix this issue we need to develop a new peak detector design.

2.1.5 Final Peak Detector Design

The operation of the basic peak detector was described in Section 2.1.2. The remaining issue is related to the droop of the peak detector output when the input voltage goes low. The absolute magnitude of the droop is not specifically the issue, rather the dependence of the degree of droop on the symbol period, and hence the data dependent control signal, is the issue.

The fundamental problem is that both the bandwidth of the peak detector when the input is high and the amount that the sampling capacitor is discharged when the input is low are proportional to I_{bias}. One possible solution is to decrease I_{bias}, effectively reducing the rate that charge is stripped from the storage capacitor and reducing the amount that the output droops each data period. However, since the bandwidth of the peak detector is also proportional to I_{bias} when the input is high, this approach will directly impact the tracking ability of the peak detector. We need to develop a method of measuring the offset that preserves the required slew rate and bandwidth during the tracking phase while reducing the discharge current on the hold phase. Fundamentally, there is no way to reduce the dependence of the amount of droop on the symbol period with the current topology without paying a severe performance penalty.

We propose that the peak detector circuit shown in Figure 2-6 provides a simple solution to this problem. Let's consider the operation of the circuit. Transistors M1 and M2 act as simple source followers, similar to device M1 in the basic peak detector described in Figure 2-5 and transistors M3 and M4 act as switches. When the input is high M3 and M4 are closed so that the peak detector behaves as a traditional peak detector. Alternately, when the input is low the switch devices are open and prevent I_{bias} from discharging C_{max}.

Compared to traditional peak detector designs, the droop in this design is greatly reduced because the switch devices, M3 and M4, dramatically reduce the dependence

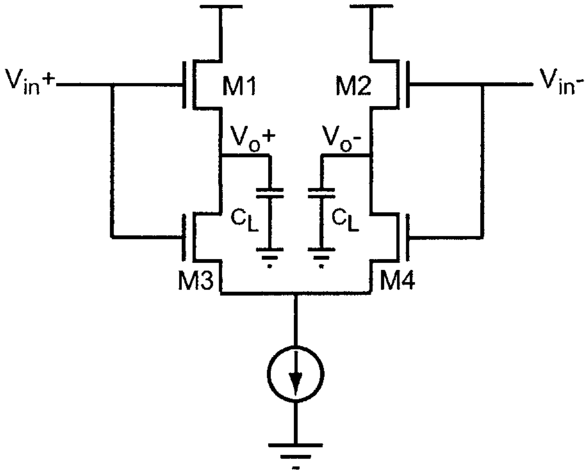


Figure 2-6: Schematic of Proposed Peak Detector with Reduced Droop

of droop on I_{bias}. The amount of droop per data period in the traditional peak detector design is determined by I_{bias} while the amount of droop per data period in the proposed peak detector design is determined by the off-state current of the switch devices. Although the output of the peak detector is still dependent on the symbol length, the magnitude of the variation is greatly attenuated. This point is illustrated in Figure 2-7 by the difference in droop between the response of the traditional peak detector, represented by the solid black line, and the response of the new peak detector design, represented by the dashed line.

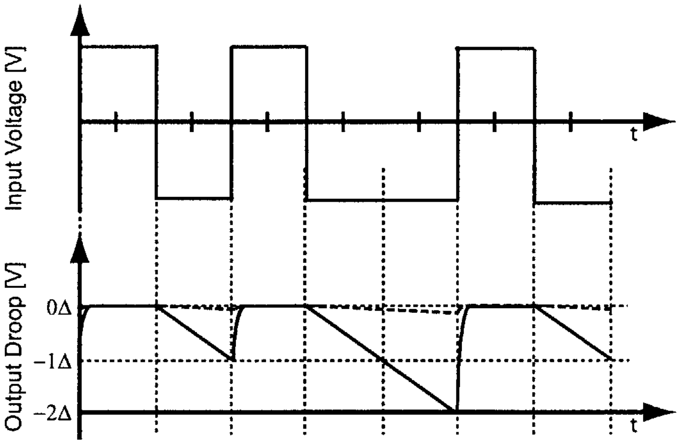


Figure 2-7: Comparison of Influence of Symbol Period on Droop of Simple Peak Detector vs Proposed Peak Detector Design

2.2 Summary

This chapter presented the design of the proposed peak detector implementation. The addition of series switch devices, which are controlled by the input, prevent the peak detector bias current from discharging the sampling capacitor when the peak detector input is low. In traditional peak detector designs both the peak detector bandwidth and droop are determined by the peak detector bias current. In the proposed design the bandwidth of the peak detector is determined by its bias current while the droop is determined by transistor off-state leakage current. By substantially reducing the dependence of the droop on the bias current, this peak detector design enables the system to simultaneously achieve the fast settling time and low output jitter goals. In the next chapter the system modeling issues will be discussed.

Chapter 3

System Modeling

The peak detector design presented in the previous chapter is the corner-stone of the offset compensation loop. The system topology and modeling of each control loop will be presented in this chapter. Additionally, we will determine the system parameters that provide the desired system dynamics in this chapter. There are several performance parameters that must be considered when determining the system parameters:

- Loop bandwidth → compensation time: Determined by compensation time goal and impact on jitter of output signal.
- Forward path gain: Based on input and output signal characteristics
- Output jitter: Need to minimize output jitter for the CDR that follows
- System stability: Unconditional requirement

3.1 System Level Implementation

The next step is to pull all of the pieces together and implement the complete control loop. A fully differential implementation of the system is shown in Figure 3-1. The peak detector is used to measure the offset referred to the output of the limit amplifier. The integrator in the feedback path filters the instantaneous peak detector output. Additionally, the integrator forces the steady-state, output-referred offset voltage to be zero regardless of the loop gain. However, there are a few changes that need to be made to the system based on the assumptions that we made in developing the proposed peak detector design.

As explained in Section 2.1.3, the offset information is contained in the peaks of the outputs (i.e. the output referred offset is equal to the difference in the peak values). Therefore, we need to account for the case when the output of the limit amplifier becomes saturated. A typical DC transfer function between the input voltage and output voltage of the basic limit amplifier stage is shown in Figure 3-2. The output nonlinearly approaches a maximum value, determined by the positive power supply, and ultimately saturates due to either a large input amplitude or a large offset.

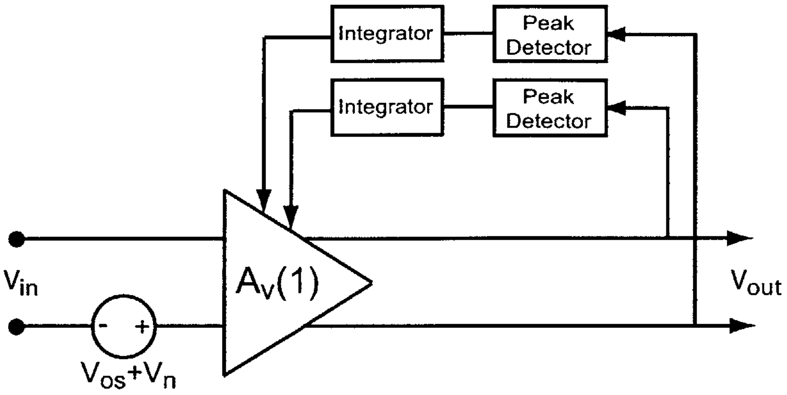


Figure 3-1: System Level of Limit Amplifier with Offset Compensation

Compensation will be ineffective, or at least severely degraded in performance, if we attempt to measure the offset from the saturated output. To solve this problem, multiple control loops are used with taps located at each of the limit amplifier stage outputs, as shown if Figure 3-3. The windowing and select logic determines the first amplifier stage with a non-saturated output and compensates the output referred offset at the selected output. Additionally, the select logic is dynamic and the selected output tap location can change as the system is compensated and outputs later in the amplifier chain become unsaturated.

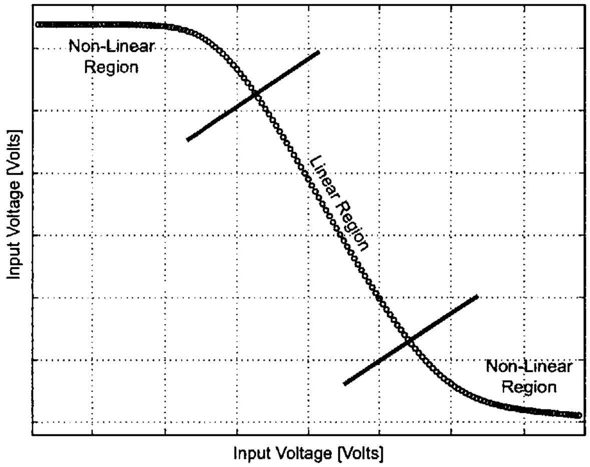


Figure 3-2: Typical Transfer Function for Limit Amplifier Cell

As shown in Figure 3-2, for large amplitude inputs the output nonlinearly approaches the maximum value defined by the positive power supply. This nonlinearity can also reduce the effective gain of the offset compensation loop. To minimize this undesired effect, the switching threshold of the windowing logic can be set lower than the positive supply voltage, say by $50-100mV$, so that the non-linear portion of the amplifier transfer function does not impact the offset compensation. There are two seeming drawbacks to this solution.

First, the maximum amplitude of input referred offset that the system can compen-

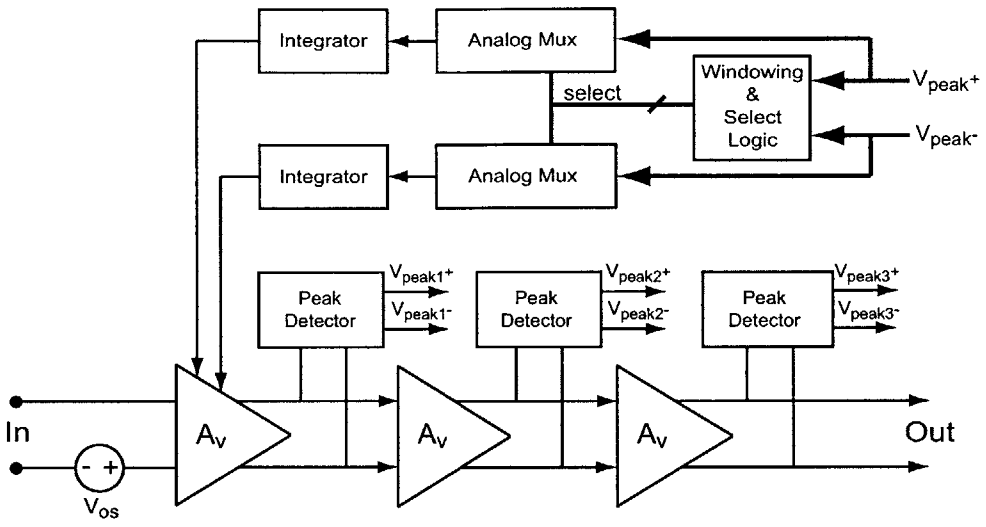


Figure 3-3: Complete System Showing Multiple Control Loops and Logic

sate is reduced because we have limited the range of each loop to avoid the non-linear portion of the amplifier transfer function. However, the input referred offset would have to be large enough to saturate the output of the first stage in the limit amplifier for this to become an issue. In this design, the maximum input referred offset that can be compensated is 450mV. However, it is highly unlikely that the input referred offset would be this large.

The second potential issue is that the amplifier cells situated after the selected compensation tap in the limit amplifier operate open-loop and any offset added by these stages will not be compensated. As mentioned in Chapter 1, the DC offset introduced by each limit amplifier stage, referred to its own input, will be on the order of a few millivolts. Each of these offset components are referred to the output of the limit amplifier through the gain of subsequent stages. The aggregate output referred offset that can not be compensated is the sum of these components. Assuming that the total output referred offset remains on the order of a few 10's of millivolts, which will be true in practice, this condition is acceptable. The goal of the offset compensation is to eliminate the gross offset that causes the output of any stage in the limit amplifier to saturate.

To ensure that the system dynamics are consistent over all possible offset values, the system parameters for each control loop are set equal. Since the gain increases at each subsequent output of the limit amplifier, the gain in each feedback path must be adjusted to satisfy this requirement. Full details of the system modeling will be covered later in this chapter.

3.2 Linear System Modeling

To model the control loop we need to make some simplifying assumptions. First, to eliminate the difficulty of analyzing multiple control loops, we only consider the case when there is one active control loop. In the end, we can extend the analysis to the more general case when there are multiple control loops and test that this assumption is valid in simulation. Further, we can assume that all blocks in the system are linear about a given operating point and make use of LTI modeling techniques. We will now develop models for each of the system blocks.

Each of the amplifiers in the forward amplifier path can be modeled by a DC gain and a single pole, representing the bandwidth of the amplifier. Therefore, the linear model for each amplifier is:

$$H(s) = \frac{A_v}{1 + s/p_1} \tag{3.1}$$

where A_v is the gain and p_1 is the pole at the $3dB$ frequency. If we consider a cascade of n amplifiers, the aggregate transfer function becomes:

$$H(s) = \left(\frac{A_v}{1 + s/p_1}\right)^n \tag{3.2}$$

Additionally, the peak detector can be similarly modeled by its DC gain, K_1, and a single pole, p_2, and has the same form as Equation 3.1. If the bandwidth of the peak detector is low enough the model takes the same form as Equation 2.1 after some simplification. The justification for this abstraction is that the peak detector only needs to measure the average output referred offset of the system, or the DC component of the output signal. To first order, the output of the peak detector is not affected by instantaneous variations at its input. The final form of the peak detector model is:

$$H(s) = \frac{K_1}{1 + s/p_2} = \frac{K_1 \cdot p_2}{s} \tag{3.3}$$

The integrator can be modeled as an ideal integrator:

$$H(s) = \frac{K_2}{s} \tag{3.4}$$

where K_2 is the gain. Putting all of the pieces together, the complete model for the forward amplifier path and the offset compensation is shown in Figure 3-4.

For the following discussion, we assume that $p_1 \gg p_2$. This is valid in this system since p_1 corresponds to the bandwidth of the limit amplifier (10GHz), and p_2 corresponds to the bandwidth of the peak detector ($\approx$ 10MHz). In a similar fashion to the linear model for a PLL, where the state variable is phase and not the data signal itself, the variable of interest in this system is the offset voltage. To characterize the system response, we define the open loop response to be:

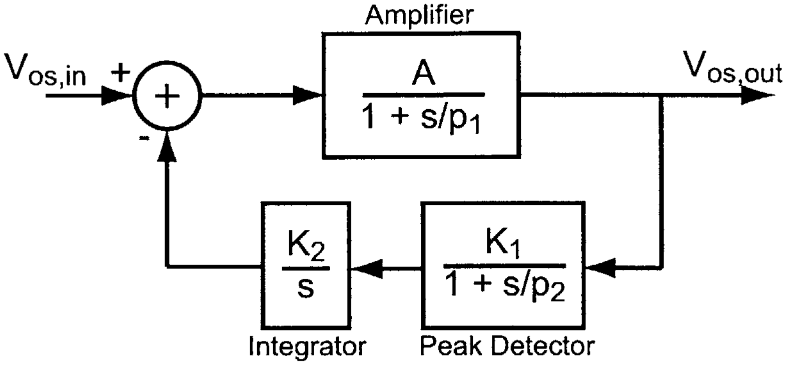


Figure 3-4: Linear Model of Limit Amplifier with Offset Compensation

$$A(s) = \left(\frac{A_v}{1+s/p_1}\right)\left(\frac{K_1}{1+s/p_2}\right)\left(\frac{K_2}{s}\right) \tag{3.5}$$

The necessary criteria for stability can be determined based on traditional feedback heuristics by analyzing the behavior of the open-loop parameter A(s). In this system, p_2 is the peak detector pole location and f_u is the unity-gain frequency. From the Bode plot in Figure 3-5, we can readily see that the integrator in the feedback path reduces the magnitude at $20dB/dec$ at frequencies below the first pole, p_2, and introduces a 90° phase shift. Phase margin is defined as the difference in phase from 180° at unity gain. If we require greater than 45° of phase margin to be stable then a necessary condition is that $p_2 \geq f_u$. Additionally, as the loop gain increases, the unity-gain frequency increases and the phase margin, and therefore stability, degrades. Ultimately, there are optimal values for p_2 and the loop gain, $A_vK_1K_2$, that guarantee stability and provide the desired loop dynamics.

To gain more intuition of the system modeling, we can further define a closed loop response parameterizing function G(s) as:

$$G(s) = \frac{A(s)}{1+A(s)} \tag{3.6}$$

where A(s) is the open loop response defined above. If $AK_1K_2 = 0$ then the loop is open, there is one closed-loop pole, $p_{1,closed-loop}$, located at the origin and there is a pair of closed-loop poles located at:

$$p_{2/3,closed-loop} = -0.5 \cdot \left[(p_1+p_2) \mp \sqrt{(p_1+p_2)^2 - 4p_1p_2}\right] \tag{3.7}$$

The pole locations, $p_{2/3,closed-loop}$, roughly correspond to the open-loop pole locations, p_1 and p_2. To understand how the closed-loop poles vary with increased gain, we construct the root locus plot in Figure 3-6. As the DC loop gain increases, the first

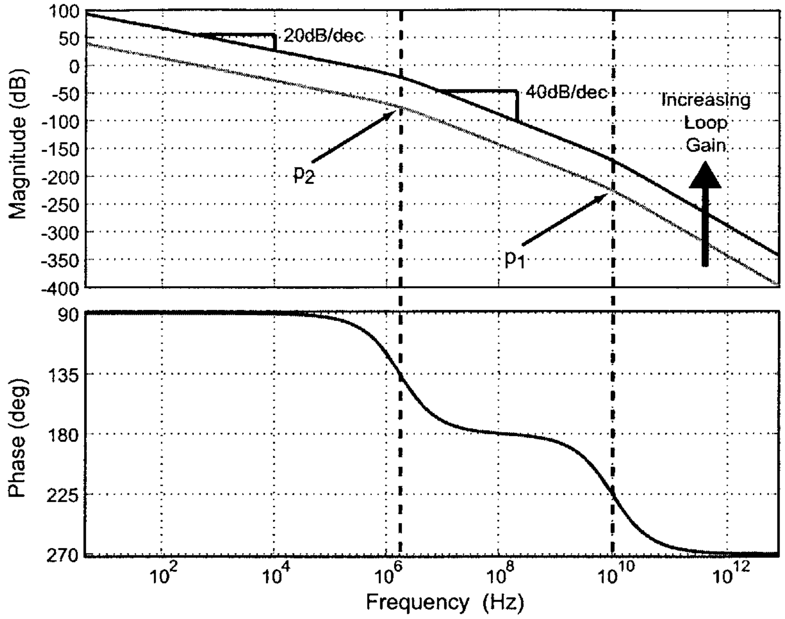


Figure 3-5: Bode Plot Showing Stability Degradation with Increasing Gain

two closed-loop poles, $p_{1,closed-loop}$ and $p_{2,closed-loop}$, approach each other from zero and the first open-loop pole location (p_2) along the negative real axis as shown in Figure 3-6. Additionally, $p_{3,closed-loop}$ moves away from the origin along the negative real axis. When $AK_1K_2 \approx p_2/4$, where p_2 is the second open-loop pole corresponding to the peak detector, a complex conjugate pole pair is formed that diverges at an angle of ± 60° to the real axis. As the open-loop gain increases, the poles will cross into the right-half-plane and the system will become unstable. So, how do we determine the value of gain that not only guarantees stability but also provides the desired settling response? One solution is to use the PLL Design Assistant [17].

3.2.1 Modeling System Response with PLL Design Assistant

The PLL Design Assistant is a useful tool that was developed to aid the design of PLL systems and can be downloaded at http://www-mtl.mit.edu/perrottgroup/tools.html. However, with a little imagination this tool can be used to model nearly any linear system. We can think of the system in Figure 3-4 as a second order, type I PLL with the forward amplifier path corresponding to a high frequency parasitic pole. Let's assume that the open-loop pole p_1 is set to 10GHz, based on the desired data-rate, and that the gain of the peak detector, K_1, is unity. Then, using the PLL Design Assistant we can specify a desired closed-loop bandwidth, based on the desired compensation settling time, and step-response shape to achieve the optimal settling time.

For example, Figure 3-7 illustrates the the GUI of the PLL Design Assistant designing the system loop with a Bessel shape and a bandwidth of 2.5MHz. The resulting gain coefficient, K, corresponds to the product A_vK_2, assuming that the peak detector has a gain of one. The pole frequency, f_p, corresponds to the open-loop

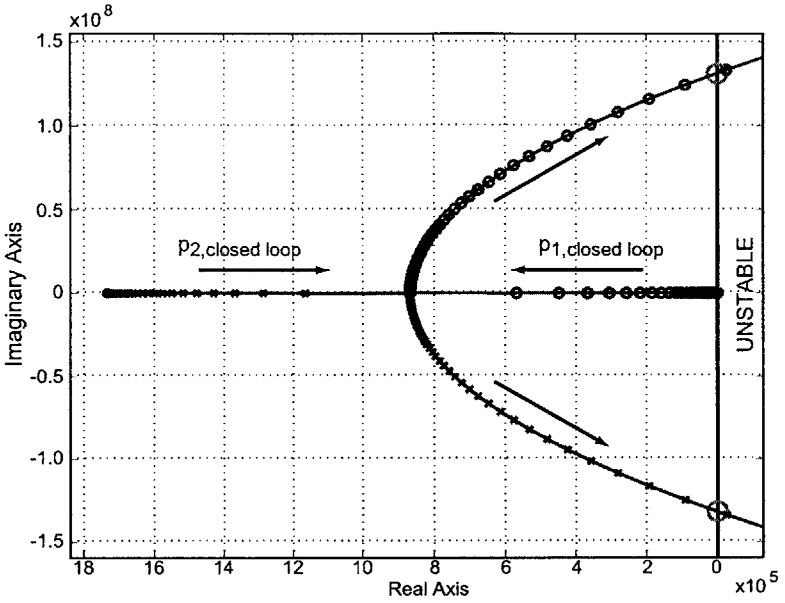


Figure 3-6: Root Locus Plot of G(s) Showing Necessary Condition for Stability

pole of the peak detector, p_2. Note that the closed-loop complex conjugate pole pair follow the trajectory determined in the root locus analysis and that the frequency of the open-loop pole p_2 is higher than the dominant closed-loop pole frequency, as required by our earlier stability analysis. The resulting step-response of the closed-loop system, shown in Figure 3-8, indicates that the total settling time for the offset compensation is roughly 500nS and that the system is stable.

Figure 3-7: PLL Design Assistant Graphical Interface

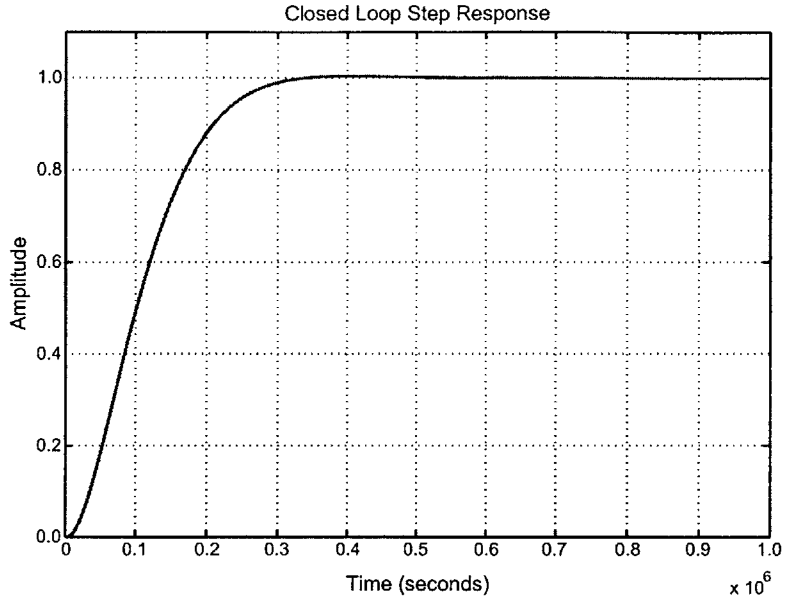


Figure 3-8: Step Response of System Designed with PLL Design Assistant

3.2.2 Modeling the Impact of System Parameter Variation on Stability and Compensation Time

Despite the designers best effort, variations in both process and environmental variables will impact of system parameters and therefore the overall system operation. We want to design the system to be robust to some degree of variation so that it will operate as intended over a wide range of process and environmental conditions. The PLL Design Assistant provides the designer with the ability to investigate the impact system parameter variations on stability and the dynamic response of the system. For example, variations in system parameters can be specified in the PLL Design Assistant GUI as shown in the alter commands in Figure 3-9. In this case we introduce a ±20% variation in both the open-loop gain and dominant open-loop pole location. Figure 3-10 demonstrates the impact on the step response of the system. Even with these large variations in the system parameters, the compensation loop is still stable and the total compensation time remains less than $1\mu S$.

3.3 Summary

This chapter presented the linearized model for the offset compensation system. To simplify the analysis, only a single control loop was considered in this chapter. The system component values required for stability and the desired dynamic behavior were determined. The assumption that the analysis can be extended to multiple loops will be tested in Chapter 6. The next two chapters will present a numerical design procedure for resistor-loaded differential amplifiers and the circuit design of each of the system components.

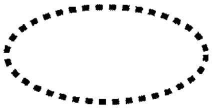


Figure 3-9: PLL Design Assistant Graphical Interface

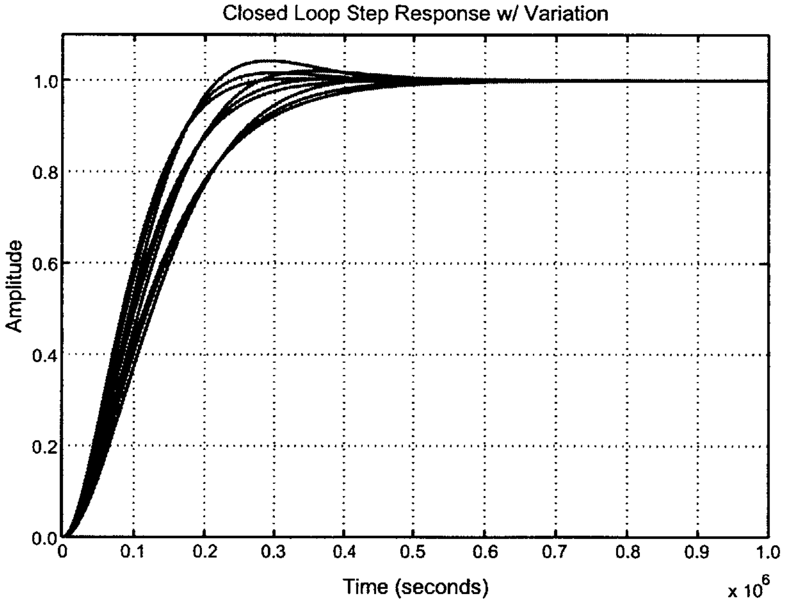


Figure 3-10: Impact of ±20% Variation in Loop Gain and Dominant Pole Location on the Step Response of the System

Chapter 4

Numerical Design of High Speed Differential Amplifiers

A novel numerical design procedure was developed to design the limit amplifier stages [18] that provides quick and accurate results. After specifying the desired performance metrics for the amplifier, the amplifier device parameters and bias conditions are determined using the methodology. Accuracy is achieved by leveraging numerical computation and basing the design on device characteristics extracted from SPICE.

4.1 Methodology

CMOS analog design techniques have traditionally assumed square law characteristics for device I-V curves when calculating the impact of device properties on circuit performance. However, the square law assumption is quickly becoming highly inaccurate with the introduction of finer line width processes due to non-ideal effects such as velocity saturation. As a result, the accuracy of traditional design equations is steadily degrading, and analog designers are in need of alternate approaches to such formulations.

Thus far, there have been two responses to dealing with changing device characteristics in the analog design community. The first has been to assume square law I-V characteristics in calculations, and then rely on a simulator such as SPICE to tweak in final device parameter adjustments. Unfortunately, the square law is rapidly becoming inaccurate to the point that the analytical calculations are practically useless — all design time is then spent on SPICE simulations. Such an approach removes intuition from the designer's grasp, leads to a lengthy design process (since many tweaks are required), and often leads to suboptimal performance. The second approach is to completely automate the analog design process — the user simply specifies performance specifications and some possible topologies, and customized software takes care of the rest [19]. Unfortunately, while very useful for the design of standard analog blocks, such an approach removes creativity from the designer's grasp and offers little intuition for the creation of new circuit topologies.

We propose an alternate approach to this issue — develop numerical procedures for

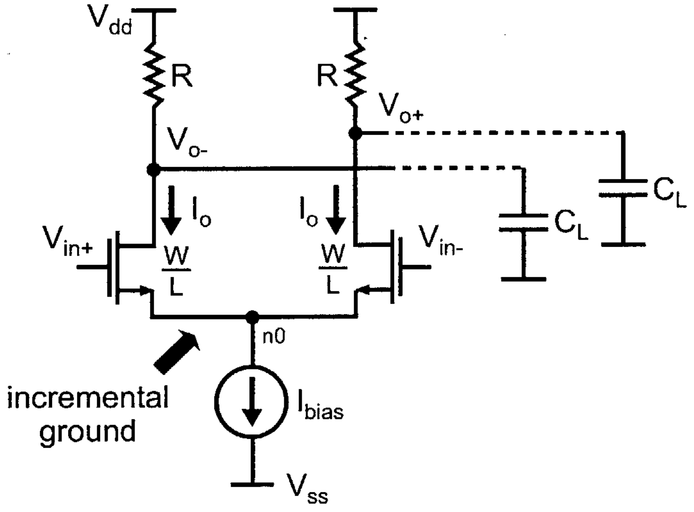


Figure 4-1: Differential amplifier used in calculations.

designing specific classes of circuits which resemble hand analysis, but use simulated device characteristics in place of analytical expressions. By sticking with procedures similar to hand analysis, much intuition can be gained about design tradeoffs. By using simulated device characteristics, the results are made accurate so that little or no tweaking is required in SPICE. This paper applies the above philosophy to the design of high speed, resistor-loaded, differential amplifiers. These structures are tremendously useful in circuit applications whose speed requirements exceed the abilities of full-swing logic circuits. Implications for the design of SCL latches, registers, and gates are also discussed.

Figure 4-1 displays a resistor-loaded, differential amplifier used in high speed applications. The resistors are often realized within a reasonably small area using unsilicided polysilicon, and introduce less capacitance than other loads such as triode PMOS devices or diode-connected NMOS devices. Further increases in bandwidth can be achieved at the expense of chip area by introducing inductors into the loads [20].

Design of resistor-loaded amplifiers entails choosing appropriate device sizes and resistance values given three design specifications:

- Allowable power dissipation: I_{bias}
- Desired voltage swing: V_{sw}
- Desired DC voltage gain: $|A_v|$

An additional specification for the amplifier is its bandwidth — its value is constrained by choice of the above three specifications as well as the load that the amplifier is required to drive (assumed capacitive). We define intrinsic bandwidth (BW) as the amplifier bandwidth that results when the amplifier drives an identical stage without additional wiring capacitance. Since actual circuits contain wiring capacitance, the intrinsic bandwidth offers only an upper bound on achievable performance, but is still a very useful metric. Note that, to achieve the maximum bandwidth, the transistor length, L, will always be assumed to be set to its minimum value for the discussion to follow.

Figure 4-1 allows us to relate the first two design specifications to other circuit parameters. When zero differential input voltage is applied to the amplifier, the bias current through each transistor is observed to be

$$I_o = I_{bias}/2.$$

As the input differential voltage is varied, the current through each resistor ranges between 0 and I_{bias}. Therefore, the maximum single-ended voltage swing at the amplifier output is

$$V_{sw} = I_{bias}R = 2I_oR \tag{4.1}$$

The third design specification, DC gain, is derived about the bias point of zero differential input voltage using the small signal transistor model shown in Figure 4-2. Here we have assumed that node $n0$ in Figure 4-1 is at incremental ground as the differential voltage is varied. Ignoring capacitance for this DC calculation, we write

$$|A_v| = g_m(R||\frac{1}{g_{ds}}) \Rightarrow g_m = |A_v|/R + |A_v|g_{ds} \tag{4.2}$$

Unfortunately, evaluation of the above equation requires calculation of g_m and g_{ds} as a function of the device bias current and size. As pointed out earlier, hand calculations assuming square law I-V characteristics prove inaccurate for this task. Our proposed method of addressing this issue is described in the following section.

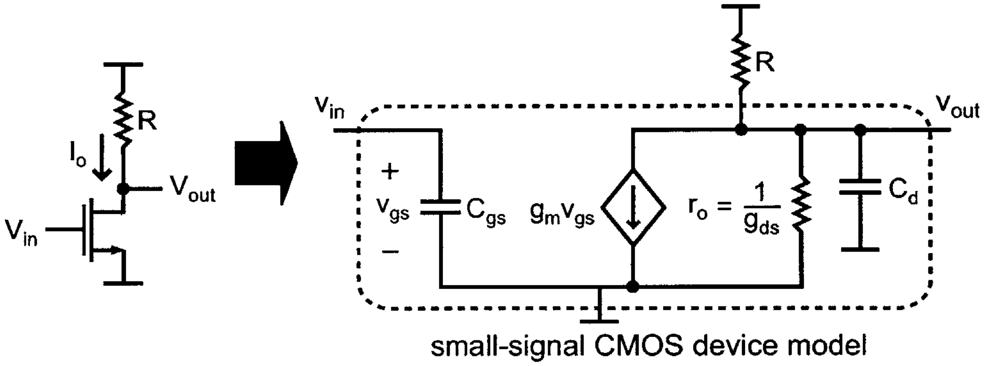


Figure 4-2: Small signal model for amplifier.

4.2 Proposed Approach

We will now show that we can create a design framework in which all design calculations revolve around the solution of just one key variable given the three constraints described earlier. This key variable is current density, and is defined as

$$I_{den} = \frac{I_o}{W},$$

where W is the width of the transistor as indicated in Figure 4-1.

Two key relationships involving current density will now be derived. The first is a gain/swing constraint formulation that will set the value of I_{den}. The second is a gain-bandwidth product expression that incorporates the impact of I_{den}.

4.2.1 Derivation of Gain/Swing Constraint Formulation

Given a fixed transistor length, $L = L_{min}$, both the g_m and g_{ds} values of a CMOS device are dependent primarily on the transistor width, W, and bias current I_o. Given a fixed value for I_o, as set by power dissipation requirements, it is straightforward to sweep W of the device in SPICE to obtain simulated plots of $g_m(I_o, W)$ and $g_{ds}(I_o, W)$. We then define $g_{m0}(I_{den})$ and $g_{ds0}(I_{den})$ as

$$g_{m0}(I_{den}) = g_m(I_o, W)/W, \quad g_{ds0}(I_{den}) = g_{ds}(I_o, W)/W \tag{4.3}$$

Let us now revisit the swing and gain constraints discussed in the Background section. Combining Equation 4.1 and Equation 4.2, we obtain

$$g_m = \frac{2|A_v|}{V_{sw}} I_o + |A_v| g_{ds}.$$

We relate g_m and g_{ds} to the simulated characteristics defined in (4.3) as

$$W g_{m0}(I_{den}) = \frac{2|A_v|}{V_{sw}} I_o + |A_v| W g_{ds0}(I_{den}).$$

Dividing through by W, we obtain the key gain/swing constraint formulation as a function of current density:

$$g_{m0}(I_{den}) = \frac{2|A_v|}{V_{sw}} I_{den} + |A_v| g_{ds0}(I_{den}) \tag{4.4}$$

The above expression states that current density is completely set by the choice of gain, swing, and the simulated g_m, g_{ds} curves.

4.2.2 Derivation of Gain-Bandwidth Tradeoff

To examine the tradeoff between gain and intrinsic bandwidth, we first note that the capacitive load can be approximately related to the amplifier device size as

$$C_L = W C_{L0} = W(C_{gs0} + C_{d0}), \tag{4.5}$$

where C_{L0} is the simulated capacitive load normalized to an effective W equal to one. Justification for the above expression follows from the fact that the amplifier is driving an identical structure for its load and that both C_{gs} and C_d scale linearly with the device width, W.

Calculation of the intrinsic bandwidth is computed as

$$BW(rad/s) = \frac{1}{RC_L} = \frac{2I_{den}}{V_{sw}C_{L0}}. \tag{4.6}$$

The amplifier gain is found through algebraic manipulation of Equation 4.4:

$$|A_v| = \frac{g_{m0}(I_{den})}{(2/V_{sw})I_{den} + g_{ds0}(I_{den})}. \tag{4.7}$$

The gain-bandwidth product is then found by combining the above two expressions:

$$|A_v| \cdot BW = \frac{g_{m0}(I_{den})}{C_{L0}} \frac{1}{1 + V_{sw}g_{ds0}(I_{den})/(2I_{den})}. \tag{4.8}$$

Given g_{ds0} is negligibly small, the above expression reverts to the classic g_m/C expression familiar to analog designers. However, one must note that g_m is a function of current density — the implications of this point will be brought home in the following section.

4.3 Intuitive Insights from Method

The first useful insight of the proposed method is that it provides an intuitive picture of the dependence of gain-bandwidth product on current density. Figure 4-3 displays a gain-bandwidth plot for a 0.18u NMOS device according to Equation 4.8. Each curve utilized a $g_{m0}(I_{den})$ curve and estimate of C_{L0} generated in Hspice from a SPICE model file for the 0.18u CMOS process. The top curve assumes $g_{ds} = 0$, while the bottom one includes its effect based on $g_{ds0}(I_{den})$ generated from Hspice. In either case, we see that gain-bandwidth product is increased as current density is increased, so that high current density is desirable in high speed applications.

The second useful insight of the proposed method is that it reveals that current density is not a free variable — it is determined by the gain and swing requirements of the amplifier as well as the $g_{m0}(I_{den})$ and $g_{ds0}(I_{den})$ characteristics of the device. Figure 4-4 displays a graphical interpretation of Equation 4.4 in setting the current density. Ignoring the influence of $g_{ds0}(I_{den})$, the current density is determined as the intersection of the $g_{m0}(I_{den})$ curve for the CMOS process with a straight line whose slope is $2|A_v|/V_{sw}$. As gain is increased relative to a given voltage swing, the line slope is increased and I_{den} must be reduced. Combining this observation with Figure 4-3, we see that higher gains lead to reduced gain-bandwidth products.

Note that the impact of finite output conductance, $g_{ds0}(I_{den})$, is to add to the straight line whose slope is $2|A_v|/V_{sw}$, which leads to further reduction of the resulting current density setting. Therefore, finite output conductance degrades the achievable

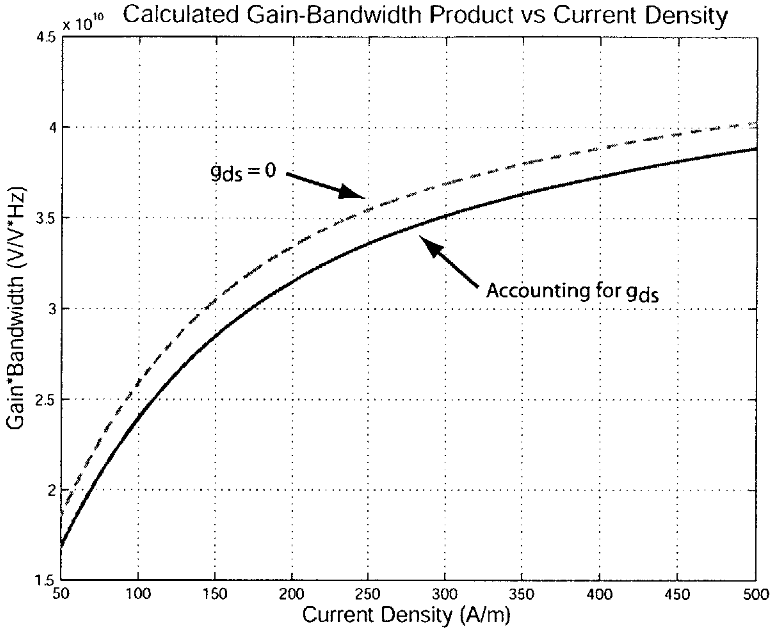


Figure 4-3: Calculated Gain-Bandwidth product vs I_{den}.

gain-bandwidth product of the differential amplifier structure.

4.4 Results

The proposed procedure was used to design several differential amplifiers in a 0.18u CMOS process (only NMOS devices were used) with varying gain values. The swing and power dissipation were held constant at V_{sw} = 1V and I_{bias} = 2mA, respectively, and the bandwidth was calculated based on Equation 4.6. Table 4.1 displays a comparison of the calculated gain and bandwidth values to the Hspice simulation results. In the Hspice simulation, the amplifier has the same topology as shown in Figure 4-1 and is loaded by an identical amplifier stage whose output is set to a constant voltage in order to eliminate Miller effect on the capacitive load it presents.

Target Gain	Calculated BW (GHz)	Simulated Gain	Simulated BW (GHz)
2.00	14.45	2.03	13.74
3.00	8.30	3.02	8.17
4.00	5.18	4.00	5.31
5.00	3.27	4.98	3.48
6.00	1.99	5.97	2.19

Table 4.1: Calculated vs simulated amplifier performance.

Table 4.1 reveals that the proposed design procedure is quite accurate with respect to achieving the desired gain for the amplifier. The calculated versus simulated

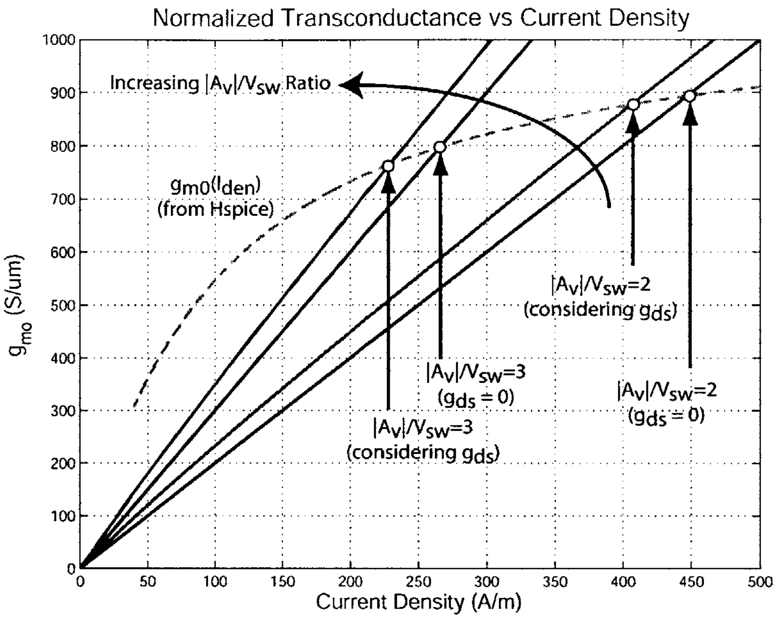


Figure 4-4: Current density settings versus gain/swing.

bandwidth values are not as accurate, but are still within ± 10 % of each other. The discrepancy in bandwidth is likely due to the fact that the capacitive load is not strictly a linear function of W as assumed in Equation 4.5.

4.5 Application to SCL Digital Circuits

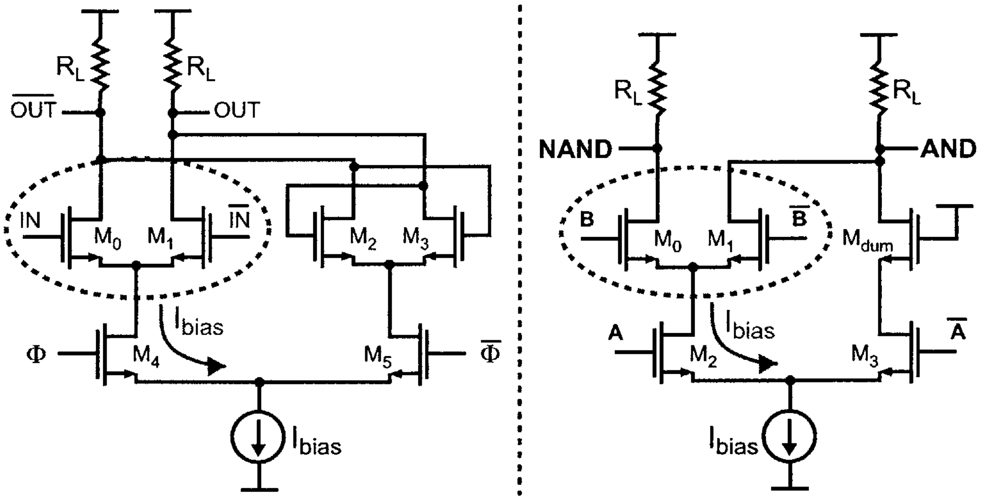
It is interesting to note that high speed digital structures also make use of such differential amplifier structures. Figure 4-5 illustrates a high speed SCL latch and a NAND/AND gate. The differential amplifiers embedded in such structures are turned on or off based on other differential pairs below them. When turned on, their behavior corresponds to that of the basic differential amplifier structure.

We have found that the following heuristic design method works well for such circuit structures:

1. Use the proposed method to design the differential amplifier portion of the structure with given gain, swing, and bias current requirements. We have found that a choice of gain in the range of 1.25 to 1.75 works well (the swing and bias current values depend on the application). In the latch example of Figure 4-5 (a), this step yields sizes for M_0 and M_1.

2. Choose identical sizes for transistors that feed off the same diff pair as the differential amplifier above. In the latch example, this would lead to M_2 and M_3 having the same sizes as M_0 and M_1.

3. Choose sizes that are roughly 20 % larger for the transistors that feed the above differential pairs. In the latch example, the widths of M_4 and M_5 would then



(a) SCL Latch (b) SCL NAND/AND gate

Figure 4-5: Digital high speed circuits.

be set to be 20% higher than the widths of M_0 and M_1 (L should be minimum in all cases). Note that this progressive scaling technique is commonly applied in digital design (see page 298 of [21]) — the value of 20% is not necessarily optimal but has worked well for us in practice.

4.6 Summary

This chapter presented a simple numerical technique to design high speed differential amplifiers with resistor loads without relying on square law assumptions for the CMOS devices. By combining hand analysis with SPICE generated data, intuition of such issues as gain-bandwidth product properties is achieved while still obtaining highly accurate design calculations. Calculations from the method were compared to Hspice simulations, and reveal that the formulations are highly accurate with respect to achieving desired gain, and reasonably accurate for bandwidth estimation. A heuristic extension of the method can be applied to high speed SCL logic gates and latches. The next chapter will discuss the circuit design issues related to each system component.

Chapter 5

Circuit Design of Systems Blocks

This section of the thesis is intended to highlight important design details for each of the critical system blocks. The limit amplifier design will be presented first since the design of the peak detector, integrator and control logic depend on the final limit amplifier design. Next, the peak detector and integrator design will be presented. Finally, the feedback control logic and output buffer will be briefly discussed. Full cell schematics and additional characterization details for each cell can be found in Appendix B.

5.1 High Speed Limit Amplifier

The main amplifier is not the main focus of this thesis, rather it is the system to be compensated. It is necessary to implement the limit amplifier to demonstrate the performance of the proposed offset compensation technique. There are numerous ways to implement the amplifier structure. As explained in Chapter 1, the selected topology is a limit amplifier composed of a cascade of resistively loaded differential amplifiers as shown in Figure 5-1. Following are the design specifications for the limit amplifier:

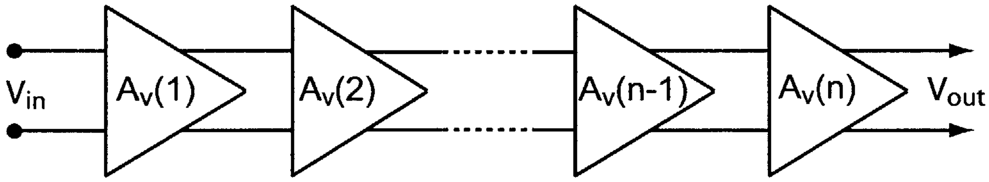


Figure 5-1: High-Speed, Multi-Stage Limit Amplifier

- Total Gain: > 100 ($> 40dB$)
- Total Bandwidth (3dB): $> 6GHz$
- RMS Jitter: $< 1pS$
- Output Swing: 1V

- Input Sensitivity: 3mV

A key question to ask is how are these design constraints determined, specifically, the gain, output swing and bandwidth? The total gain of the limit amplifier is based on the difference between the TIA output amplitude and the clock and data recovery (CDR) input amplitude requirements. The output swing is determined by a combination of the CDR input requirements and its influence on bandwidth and power dissipation. The total bandwidth is set according to the data rate to minimize inter-symbol interference (ISI). The gain per stage is set to balance the trade-off between maximizing the bandwidth and power efficiency and maximizing the input sensitivity. The number of stages is calculated by simply dividing the total gain by the gain per stage. Once the number of stages has been determined, the required bandwidth per stage can then be calculated. Therefore, the gain, output voltage swing and bandwidth are based on trade-offs between signal conditioning, power dissipation and input SNR requirements. Chapter 4 presented the design methodology for determining the appropriate biasing, transistor widths and resistance once the gain, swing and bandwidth are determined.

5.1.1 Determining Optimal Number of Stages

The total gain, bandwidth and output swing for the limit amplifier are fixed and the number of stages must be designed to meet the above specifications. How do we determine the optimal number of stages, or gain per stage? Also, how does the optimal number of stages required to maximize bandwidth compare to the optimal number of stages required to minimize power dissipation or to minimize the input referred noise (i.e. maximize the input sensitivity)? The following discussion will address these issues.

Optimal Number of Stages for Maximum Bandwidth

Following the derivation in Chapter 8 of [20], we can determine the optimal gain per stage, or conversely the optimal number of stages, of the limit amplifier to maximize bandwidth for a given total amplifier gain. As before, if we model each stage of the limit amplifier by a gain and a single pole, the model for the limit amplifier is:

$$\frac{V_{out}}{V_{in}} = \left(\frac{A_v}{1 + w_1/w_o}\right)^n \tag{5.1}$$

A_v is the gain/stage, w_1 is the overall bandwidth of the limit amplifier, w_o is the bandwidth of each stage and n is the number of stages. If we solve for w_1 we can see that as the number of stages, n, increases, the bandwidth decreases much slower than the gain increases:

$$w_1 = w_o\sqrt{2^{1/n} - 1} \tag{5.2}$$

This means that we can increase the gain-bandwidth product as the number of stages increases, to a limit. If the total gain of the limit amplifier is G then the gain per stage is $A_v = G^{1/n}$. After a significant amount of algebra (refer to Appendix D), the optimal gain per stage to maximize the total bandwidth for a specified total gain is found to be:

$$G^{1/n} = e^{1/2} \tag{5.3}$$

Therefore, the optimal gain per stage, neglecting the impact on power dissipation, implementation size and noise, is approximately 1.65.

The following discussion is based on the analysis presented in [22]. The total limit amplifier bandwidth, normalized to $w_t = Aw_o$, is plotted as solid lines in Figure 5-2 versus n for total gains, G, of 10, 100 and 1000. The total normalized bandwidths are also plotted versus n for gain per stage, A_v, of 1.65 (the optimum), 2 and 3 as dashed lines. The intersection of two lines corresponds to a possible design point. The line corresponding to a gain of $A = 1.65$ per stage intersects each of the solid lines at its peak, indicating maximum achievable bandwidth. This agrees with our previous analysis. Each of the solid curves for total normalized bandwidth are quite shallow at their maximum, especially for large total gains. From a designers perspective, this is desirable because it provides flexibility in the design. A gain per stage slightly different from the optimal value can be used with minimal impact on total bandwidth. The advantage is an extra degree of freedom in determining the number of stages.

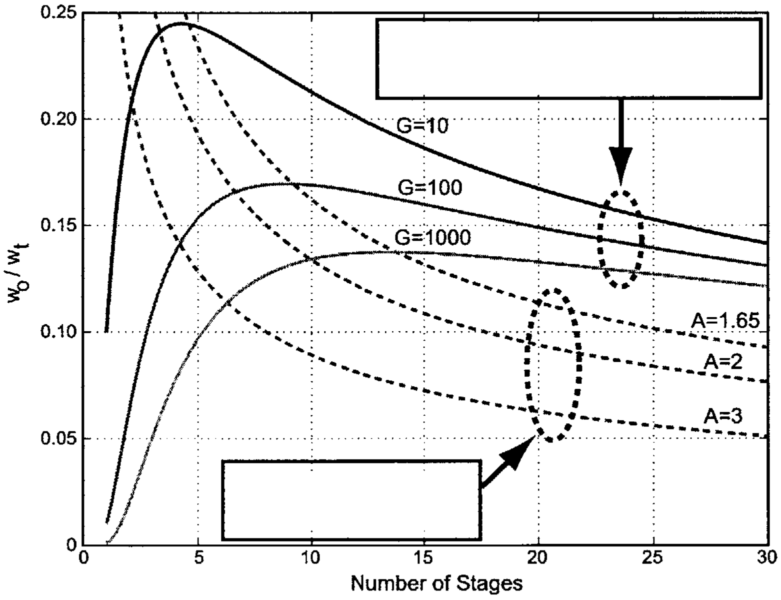


Figure 5-2: Number of Stages vs Total Bandwidth: Normalized Total Bandwidth vs Number of Stages for $G^{1/n} = A = 1.65$, 2.0 and 3.0 and Total Gains, G, of 10, 100 and 1000

Optimal Number of Stages for Minimum Power Dissipation

Power dissipation is an important consideration that must considered in the design. If the power dissipation of the final design is too high then the design will not be practical. As mentioned in the previous section, as n increases to the number required to maximize bandwidth, the total gain-bandwidth product also increases. This occurs because the total gain increases faster than the bandwidth decreases. As n continues to increase past the optimum, the gain-bandwidth product decreases. Therefore, for a fixed total gain and bandwidth, the power per stage should also decrease faster than the total power increases as n increases to the optimum. After n exceeds the optimum, the power per stage continues to decrease but the total power starts to increase. Intuitively, there should be some number of stages that provides the minimum power dissipation.

Making use of the design methodology presented in Chapter 4, a Matlab script was generated that returns the transistor width, resistance and bias current required for a specified bandwidth. The script can be found in Appendix E. Using this information, the total power dissipation for the limit amplifier is plotted in Figure 5-3 as the dashed lines versus the n for a total gain, G, of 100 and bandwidths of 2,4,6,8 and 10GHz. The points at the minimum of each line corresponds to the number of stages required to achieve minimum power dissipation for each bandwidth. Point A, which lies at the minimum power for a bandwidth per stage of 8GHz, corresponds to 9 amplifier stages, or a gain per stage of 1.65. Therefore, *the number of stages required for maximum bandwidth determined in Figure 5-2 equals the number of stages required for minimum power dissipation.* Moving to the minimum of a lower dashed lines results in a lower total bandwidth, but minimum power dissipation for the resulting bandwidth. The simulated results generated with the script match the intuition presented above. This analysis demonstrates the powerful result that *it is possible to simultaneously achieve maximum total bandwidth and minimal total power dissipation for a specified total gain and bandwidth.*

Optimal Number of Stages to Minimize Total Noise

The input sensitivity of the limit amplifier is limited by the total input referred noise from the amplifier. If the input referred noise is too large then the input SNR decreases. Similar to the analysis performed above, we can analyze the impact on the number of stages, or the gain per stage, on the input sensitivity. Figure 5-4a shows a single limit amplifier stage. Figure 5-4b displays the half-circuit for each limit amplifier stage with the noise sources for each of the devices included. The current noise source for the resistor thermal noise is:

$$\overline{i_{n,r}^2} = 4KT\frac{1}{R}\Delta f \tag{5.4}$$

where K is Boltzmann's constant ($K = 1.38\text{x}10^{-}23$ J/K), R is the resistance value and Δf is the bandwidth of interest. Both of the input devices, M1 and M2, and

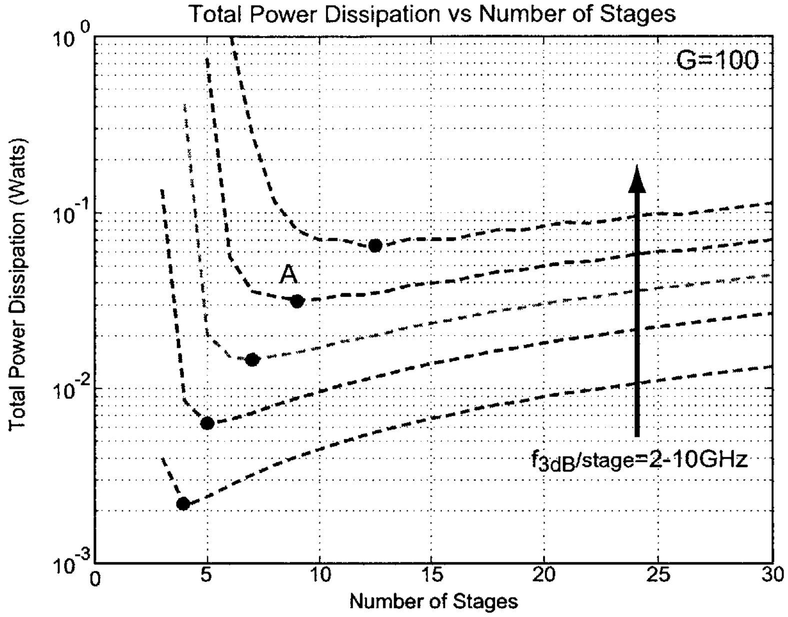


Figure 5-3: Total Power Dissipation of Limit Amplifier for a Total Gain of 100 and Bandwidths/Stage from 2-10GHz

the tail current source, M3, have flicker noise, thermal noise and gate noise. The cross-over frequency, f_c, is defined as the frequency where the flicker noise and the thermal noise of the transistor are equal and depends on process and circuit variables. Since f_c is on the order of 10's of MHz and the limit amplifier is broadband, with a bandwidth of 10GHz, we can ignore flicker noise to first order. Gate noise is a high frequency, narrow-band noise phenomenon that can also be ignored to first order. Therefore, in the half-circuit model the channel induced drain noise current for M1 and M3 can be expressed as:

$$\overline{i_{nd,M1}^2} = 4KT\gamma g_{do,M1}\Delta f \tag{5.5}$$

$$\overline{i_{nd,M3}^2} = 4KT\gamma g_{do,M3}\Delta f \tag{5.6}$$

In the above equations, γ is the the excess noise factor, which is a process dependent, and is roughly 2-3 in short channel devices. g_{do} is the output conductance of the transistors at a zero V_{ds}. Input referring all of these noise sources to a voltage noise source, as shown in Figure 5-4c, yields:

$$\overline{v_{in}^2} = \frac{4KT}{g_{m,M1}^2} \cdot \left[\frac{1}{R} + \gamma g_{do,M1} + 0.5 \cdot \gamma g_{do,M3}\right] \Delta f \tag{5.7}$$

Finally, to determine the total input referred noise voltage of the limit amplifier, refer each of the individual input referred noise sources in each stage to the input of

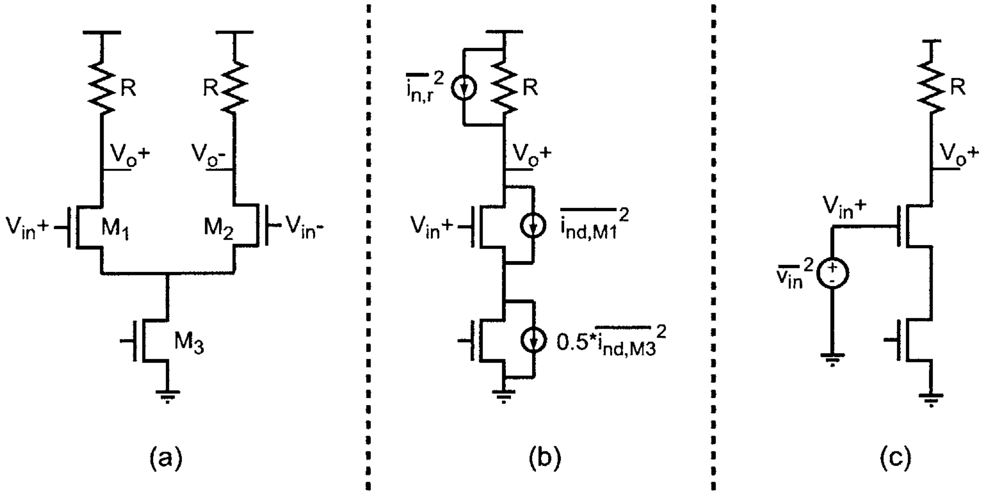


Figure 5-4: (a) Full Resistive-Loaded Differential Amplifier (b) Half-Circuit with Noise Sources Added (c) Half-Circuit with Noise Source Referred to Input

the limit amplifier. Each noise source will simply be inversely scaled by the gain of the preceding stages. Therefore, the total input referred noise voltage of the limit amplifier is:

$$\overline{v_{in,tot}^2} = \sum_{i=1}^{n} \frac{1}{A^{(i-1)}} \cdot \overline{v_{in,i}^2} \tag{5.8}$$

where n is the number of stages and A is gain per stage. To understand how the number of stages in the limit amplifier impacts the total noise, we need to make a few assumptions. First, we can assume that the tail current source adds negligible to the total input referred noise. Next, if we assume that $g_m = \alpha g_{do}$, where α is a scaling factor, then we can simplify Equation 5.7 to:

$$\begin{aligned} \overline{v_{in}^2} &\approx \frac{4KT}{g_{m,M1}^2} \cdot \left[\frac{1}{R} + \gamma g_{do,M1}\right] \Delta f & (5.9) \\ &= \frac{4KT}{g_{m,M1}^2} \cdot \left[\frac{1}{R} + \frac{\gamma}{\alpha} g_{m,M1}\right] \Delta f & (5.10) \\ &= \frac{4KT}{g_{m,M1}} \cdot \left[\frac{1}{A_v} + \frac{\gamma}{\alpha}\right] \Delta f & (5.11) \\ &= \frac{4KTR}{A_v} \cdot \left[\frac{1}{A_v} + \frac{\gamma}{\alpha}\right] \Delta f & (5.12) \end{aligned}$$

To be conservative, we assume that the excess noise factor $\gamma = 3$ and that $\alpha = 0.5$.

Finally, using the amplifier script in Appendix E, the total input referred voltage noise is plotted versus n for 3 different amplifier stage bandwidths and a total gain of 100 in Figure 5-5. The lines marked with diamonds are the total input referred noise voltage of the limit amplifier. The lines without the diamonds are the total input referred noise voltage due only to the input devices of each amplifier stage. It is evident that the channel noise of the input devices dominates the total noise and that the total input referred noise increases nearly linearly with the number of stages. Interestingly, the total noise spectral density decreases as the bandwidth of the limit amplifier increases. This is expected since, for a fixed gain, the current density increases as the bandwidth requirement increases. As the current density increases the resistance decreases and the transistor transconductance increases to maintain a constant $g_m R_o$ product. However, the improved noise performance is achieved at the expense of higher power dissipation. This trade-off between noise and power dissipation is well documented [13, 23, 1]. From Equation 5.10 the total noise is inversely proportional to g_m, to first order, so it will decrease as the bandwidth increases. Therefore, to minimize the total noise, and maximize the input SNR, it is desirable to minimize the total number of stages in the limit amplifier.

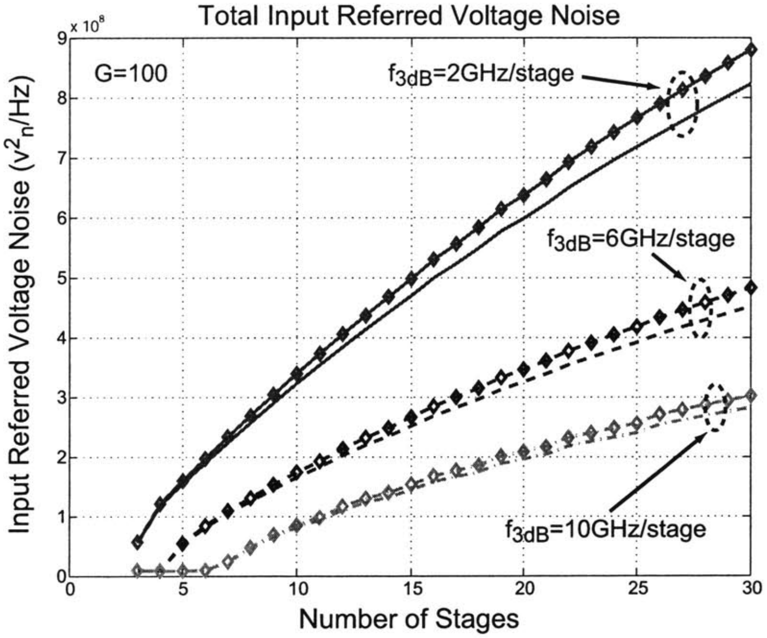


Figure 5-5: Total Input Referred Voltage Noise Versus Number of Amplifier Stages for a Fixed Total Gain

Finally, we can translate the noise performance to input sensitivity. The input sensitivity can be determined using the following expression[4]:

$$V_{in,min} = 12 \cdot \overline{v_{in,tot}} \sqrt{BW} \tag{5.13}$$

where BW is the total bandwidth of the limit amplifier. The minimum input voltage is plotted in Figure 5-6 for the same conditions as in Figure 5-5.

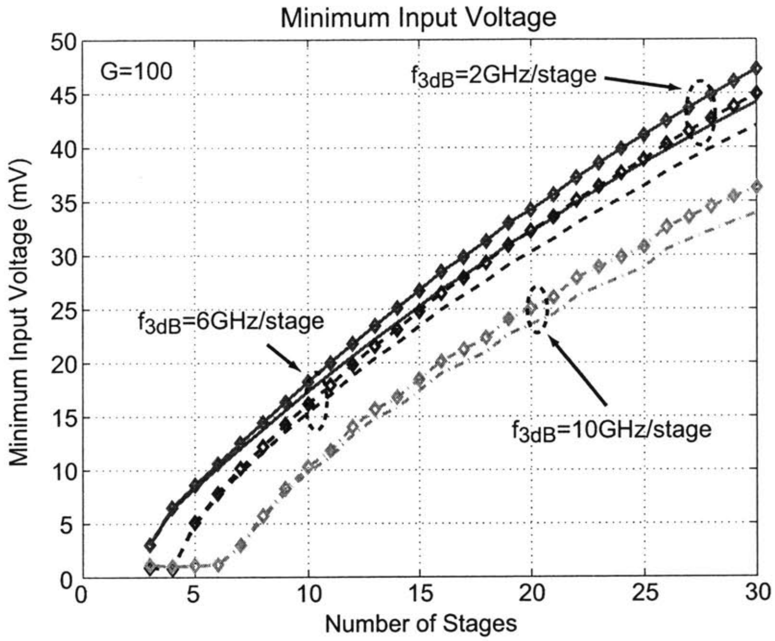


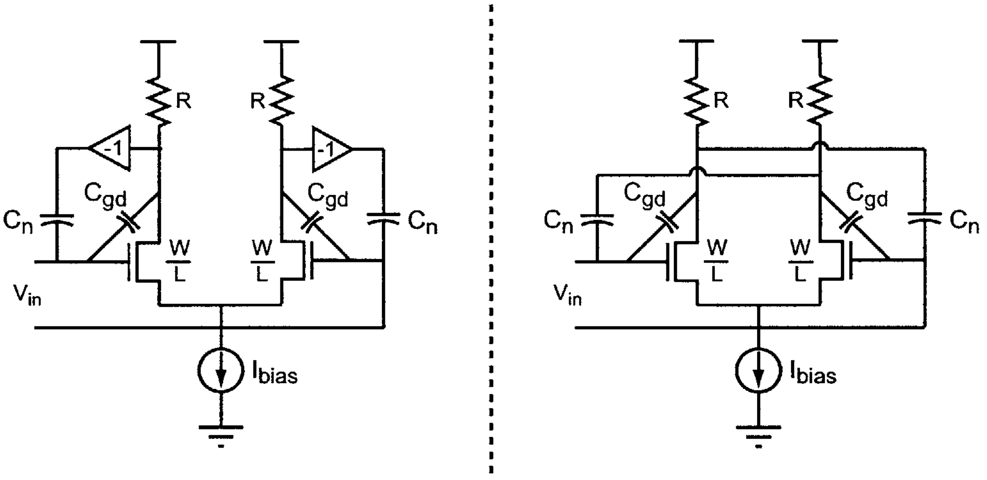
Figure 5-6: Minimum Input Voltage Versus Number of Amplifier Stages for a Fixed Total Gain

5.1.2 Bandwidth Extension Techniques

The analysis in the previous sections assumed that the amplifier stages could be modeled by a gain and single pole which provides a first-order response. However, there are several design techniques that can be used to provide a higher order response and, therefore, enhance the bandwidth of the amplifier. The most common technique for enhancing the bandwidth of resistively loaded, differential amplifiers is shunt peaking with inductors [20, 24]. However, a significant disadvantage of using inductors in integrated designs is their large area. For this reason, this design will not use inductors or shunt peaking.

A simple trick known as neutralization [20] utilizes negative capacitors to cancel the gate to drain capacitance, C_{gd}, as shown in Figure 5-7. Although not as effective as shunt peaking, neutralization can provide significant bandwidth enhancement while occupying much less die area. The neutralization capacitors, C_n, are connected in parallel with C_{gd} between each input and output with a gain of -1 as shown in Figure 5-7a. When the input goes high the charge is supplied to C_{gd} by C_n rather than the driving stage effectively increasing the bandwidth of the limit amplifier. Similarly, when the input goes low the charge on C_{gd} simply transfers to C_n rather than discharging to ground.

A severe obstacle to using the neutralization technique is implementing the inverting buffers at each output. Recognizing that the differential outputs are 180° out of phase, the neutralization capacitors can simply be connected between each input



(a) (b)

Figure 5-7: Limit Amplifier Stage with Neutralization Capacitors

and the opposite output, as shown if Figure 5-7b. If C_n is smaller than C_{gd}, there will be a residual Miller Effect. If C_n is the same size as C_{gd} the Miller effect will be eliminated. Following this train of thought, if C_n is larger than C_{gd} there will be a net negative capacitance, or an equivalent inductive effect over a narrow frequency band. Over a broad frequency range, the magnitude of the impedance of an inductor is proportional to frequency. However, the magnitude of the impedance of the negative capacitance is inversely proportional to frequency. The final size of C_n was determined by inspecting eye diagrams of limit amplifier output.

Other bandwidth enhancement techniques such as inverse scaling of the limit amplifier stages were investigated but not employed in this design. Inverse scaling would have significantly increased the layout burden and the amplifier design was not the focus of this thesis.

5.1.3 Final Amplifier Design

To review the design goals, the limit amplifier is designed for a total gain of 40dB, bandwidth of 6GHz, output swing of 1V and input sensitivity of 3mV. Based on the analysis above, the final amplifier design was performed using the Matlab script included in Appendix E. The gain-bandwidth requirement of the limit amplifier tests the upper performance limits of this process. Therefore, the gain per stage was selected near the optimal number of stages to maximum the bandwidth for the desired gain. There is some flexibility in the choice of n since the curves of total bandwidth versus number of stages in Figure 5-2 are very shallow. Considering the impact of large n on power and noise, the amplifier was designed with 7 stages, rather than the optimum of 9. The impact of this choice is a 1.2% reduction in total bandwidth and a 25% increase in power dissipation. However, the total input referred noise is reduced from approximately $6.9nV/\sqrt{Hz}$ to just under $2.5nV/\sqrt{Hz}$, resulting in an improvement in input sensitivity from 8.3mV to 3.0mV. To keep the power of the chip manageable, the total power dissipation for the limit amplifier was limited to 100mW, or 55.5mA from a 1.8V supply. This power budget translates to 7.9mA bias current per stage with 7 amplifier stages. Based on the total gain goal and number of stages, each amplifier stage was designed for a gain of 2. The output swing was set to 1V. Based on these design choices and the script in Appendix E, each limit amplifier stage has a bandwidth of 9.0GHz, neglecting the enhancement techniques. The total bandwidth of the limit amplifier neglecting enhancement techniques is 2.9GHz. With the neutralization technique described in Section 5.1.2 the final bandwidth is roughly 4.0GHz, less than the desired bandwidth of 6.0GHz.

The total bandwidth predicted by the linear model in Section 5.1.1 for a cascaded amplifier design may be a conservative estimate [24]. In the analysis for optimal gain per stage we assumed that each of the amplifier stages operates in the small-signal region. We also assumed that the bandwidth of each stage is related to a single time constant determined by the output resistance of the driving stage in parallel with the total capacitance at the output. However, the later amplifier cells experience a larger amplitude input than the first several stages, completely switching the bias current, and exhibit large-signal behavior. The large transconductance of the input devices of the later stages quickly switch the bias current and sharpen the edge rates of the signals. When the delayed current flows to the output it only has to charge the capacitance of the load resistor and input capacitance of the loading stage. The capacitance due to the input stage has effectively been eliminated and the speed is therefore determined by a single stage.

Ultimately, the performance of the limit amplifier must be judged by the quality of the opening of the eye diagram. Figure 5-8 exhibits Hspice eye diagrams at the output of the limit amplifier, loaded by the output buffer, for data rates of 5Gbps and 10Gbps and for input amplitudes of 2mV, 20mV and 200mV (peak-to-peak). The 5Gbps eye diagrams exhibit almost no ISI and all three eyes are very open. The peak-to-peak jitter due to the offset compensation and ISI is less than 1.5pS for all three eyes. The 10Gbps eye diagrams suffer from significant ISI and the eye for $V_{in} = 2mV_{pp}$ exhibits closure. Due to the limited limit amplifier bandwidth, the outputs do not reach the minimum and maximum values for successive high-low bits that transition at the maximum transition rate. The peak-to-peak jitter due to the offset compensation and the limited bandwidth of the limit amplifier for the three eyes are 4.5pS, 3.5ps and 2.3ps. All three eyes exhibit jitter which is greater than the goal of 2ps.

5.2 Peak Detector

The peak detector topology, shown in Figure 5-9, and its operation was discussed in detail in Chapter 2. In this chapter we will review the basic operation of the peak detector and analyze the two most significant design issues for the peak detector. The first issue is that variations in the peak detector pole location directly impact the system dynamics. Techniques for minimizing this undesired effect are discussed. Also, the size of the peak detector input devices represents a trade-off between limit

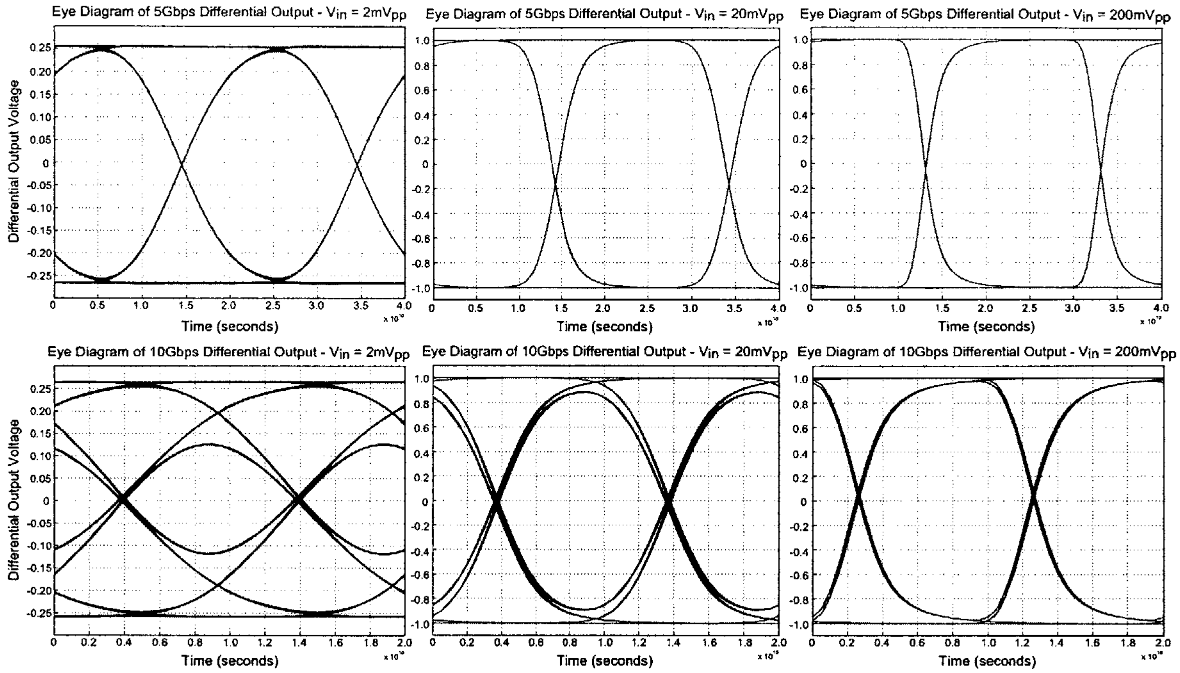


Figure 5-8: Eye Diagrams for the Limit Amplifier at Data Rates of 5Gbps and 10Gbps and input amplitudes of 2mV, 20mV and 200mV peak-to-peak

amplifier bandwidth and offset introduced by the peak detector input devices. This trade-off will be explored. We will also explore how the peak detector was designed to allow its bandwidth to be programmed.

As discussed in Chapter 2, when the input is high, the switch devices M3 and M4 are on and the peak detector behaves as a traditional peak detector (source follower). With the input high, the bandwidth of the peak detector can be expressed as:

$$f_{3dB} = \frac{g_{m,M1/2}}{2\pi C_L} \tag{5.14}$$

Alternately, when the input is low the switch devices are open and the output will retain its current value minus any droop. The amount of droop is determined by the off-state leakage of the switch devices, M3 and M4, rather than the bias current. In contrast to traditional peak detector designs, the bandwidth of the proposed peak detector (when then input is high) can be set independently from the droop (when the input is low).

In Chapter 3 we determined that the dominant open-loop pole of the offset compensation corresponded to the pole of the peak detector. To minimize variation in the system dynamics we would like to define the pole location to minimize its sensitivity to process and temperature variations. Biasing devices M1 and M2 in the peak detector in subthreshold causes $g_{m,M1/2}$ to be a linear, rather than quadratic, function of the bias current and independent of device dimensions to first order. Therefore, variations in the bias current and physical device dimensions will have a minimal im-

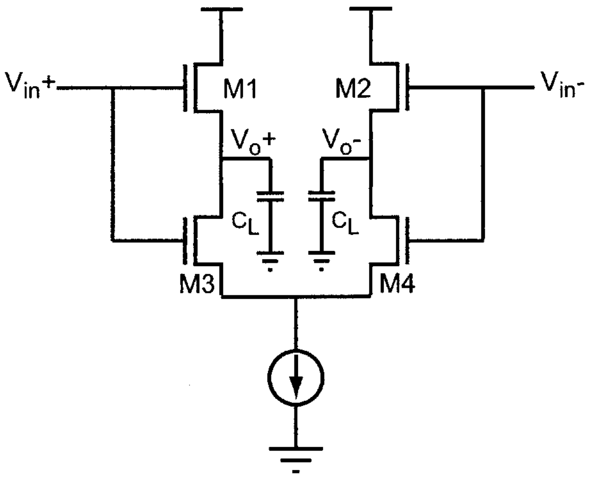


Figure 5-9: Simplified Schematic of Fully Differential Peak Detector

pact on the dominant open-loop pole location. Additionally, it is trivial to reprogram the bandwidth for different system dynamics if the bandwidth is a linear function of the bias current.

The most significant design issue for the peak detector is the trade-off between the offset due to device mismatch, introduced by the peak detector input devices, and the limit amplifier bandwidth. As we know from the development in Appendix A, the total offset due to device mismatch is inversely proportional to the square-root of the peak detector input device gate area. Additionally, this offset will be directly referred to the output of the limit amplifier through a low-pass filter transfer function. However, the gate capacitance, and hence the loading on the limit amplifier output due to the peak detector input, increases linearly with the gate area of the input devices. The gate oxide density is approximately $8.5fF/\mu m^2$ so large peak detector input devices can not be tolerated. To limit the impact on the limit amplifier bandwidth, the total gate capacitance of the peak detector input devices was limited to 10fF. This results in input device dimensions of $4.0\mu m \times 0.35\mu m$ (WxL).

One potential downside to biasing the input devices in subthreshold is that, by definition, they operate at low current densities (amps/width). For a desired bandwidth the peak detector must satisfy some g_m/C ratio, which is linearly proportional to I_{bias}/C. Due to the upper bound placed on total gate capacitance of the input devices, the peak detector has a maximum achievable bandwidth. In this process, the current density for the peak detector must remain below $1\mu A/\mu m$ to stay in subthreshold. Equivalently, the total bias current must be less than $4\mu A$ since the width of the input devices is $4\mu m$. With a load capacitance of 1pF, the maximum bandwidth of the peak detector at room temperature is:

$$BW_{max} = \frac{g_m}{2\pi C_L} = \frac{qI_{bias}}{2\pi C_L nKT} \approx 20MHz \tag{5.15}$$

where n is a fitting constant approximately equal to 1.5 and T is 294° K. The bandwidth was simulated using Hspice across process variations and a temperature range from 0° C to 70° C. The maximum bandwidth of the peak detector varies between 16.3MHz (slow/70° C) and 19.5MHz (fast/0° C) with values between 17.9MHz and 18.4MHz at 27° C across process variation. Peak detector bandwidths between 1.7MHz and 17MHz are required to achieve loop bandwidths between 1MHz and 10MHz so this design satisfies the design goals. In case the measured results dramatically differ from the simulated results, the peak detector bias current and load capacitance can be independently adjusted to compensate the design.

5.3 Integrator

There were several challenges with designing the integrator. Each of the issues will be discussed and the final integrator design, which addresses each of the issues, will be presented. Figure 5-10 shows a typical implementation of a differential active integrator. The transfer function is:

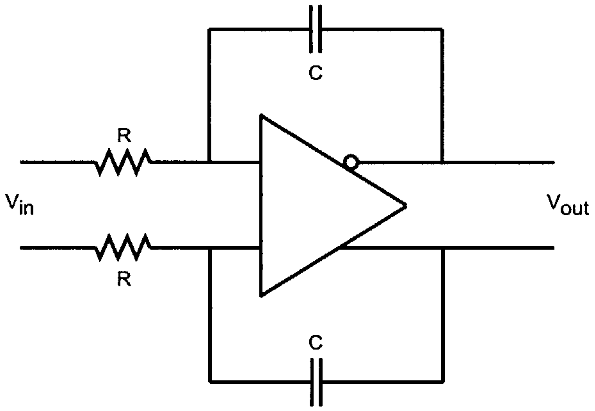


Figure 5-10: Basic Differential RC Integrator

$$\frac{V_{out}}{V_{in}} = \frac{1}{RC} \cdot \frac{1}{s} \tag{5.16}$$

and corresponds to a gain of 1/(RC) cascaded with an ideal integrator. The undesirable characteristic of this design for integrated CMOS designs is that it presents a resistive load and can significantly attenuate the gain of the driving stage. Ideally, the integrator should have a purely capacitive input impedance. Therefore, the g_mC filter shown in Figure 5-11, which satisfies the input impedance requirement, was used as the integrator. Unfortunately, the filter's frequency response, shown here, does not match the desired response from Equation 5.16:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m,M1} \cdot (R_{o,M1} \parallel R_{o,M4})}{1 + (R_{o,M1} \parallel R_{o,M4}) \cdot C} = \frac{K_2}{1 + s/p_3} \tag{5.17}$$

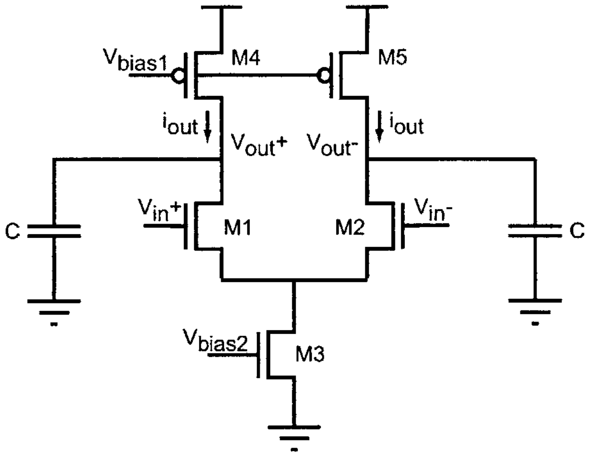


Figure 5-11: Simplified Schematic of Differential g_mC Integrator

where $R_{o,M1}$ and $R_{o,M4}$ are the output impedances of M1 and M4. Specifically, the g_mC filter, as designed, has a finite DC gain:

$$\frac{V_{out}}{V_{in}} = g_{m,M1} \cdot (R_{o,M1} \parallel R_{o,M4}) = K_2 \tag{5.18}$$

and a dominant low-frequency pole:

$$p_3 = \frac{1}{(R_{o,M1} \parallel R_{o,M4}) \cdot C} \tag{5.19}$$

Since the gain is proportional to the output resistance and the pole location is inversely proportional to the output resistance, the filter will approximate an ideal integrator for large output resistance. There are two main design techniques that can be used to increase the output resistance: cascode the output devices M1-M2 and M4-M5 and/or use long length devices. Unfortunately, it was not feasible to use cascoded devices in this design due to head-room issues. The gate lengths of M1-M2 and M4-M5 were set to $1\mu m$ to achieve the desired high output impedance. To determine if this restriction is an issue, we need to investigate the impact of the new design on the overall compensation performance.

To understand the impact of the non-ideal characteristics of the proposed implementation on the system operation, we will refer back to Chapter 3 where the linear system model was developed and compare the impact of the two integrator models on the system transfer function. First, expanding Equation 3.6 and solving for V_{out}/V_{in} yields:

$$G(s) = \frac{A(s)}{1 + A(s)} \tag{5.20}$$

$$= \frac{A_v K_1 K_2}{s \cdot (1 + s/p_1) \cdot (1 + s/p_2) + A_v K_1 K_2} \tag{5.21}$$

$$\frac{V_{out}}{V_{in}}(s) = G(s) \cdot \left(\frac{1 + s/p_2}{K_1}\right)\left(\frac{s}{K_2}\right) \tag{5.22}$$

$$= \frac{A_v \cdot (1 + s/p_2) \cdot s}{s \cdot (1 + s/p_1) \cdot (1 + s/p_2) + A_v K_1 K_2} \tag{5.23}$$

$$\frac{V_{out}}{V_{in}}(s = 0) = 0 \tag{5.24}$$

For the ideal model we can see that the offset compensation drives the steady-state output-referred offset voltage to zero because of the infinite DC gain of the integrator. Alternatively, consider that in steady-state the input to the integrator, which corresponds to the output referred offset voltage, must be equal to zero. If the input to the integrator were non-zero then the integrator output would ramp and the system would not be in steady state.

Now, consider substituting the model for the proposed integrator into Equation 5.20 and solve for V_{out}/V_{in}:

$$G(s) = \frac{A_v K_1 K_2}{((1 + s/p_1) \cdot (1 + s/p_2) \cdot (1 + s/p_3) + A_v K_1 K_2} \tag{5.25}$$

$$\frac{V_{out}}{V_{in}}(s) = G(s) \cdot \left(\frac{1 + s/p_2}{K_1}\right)\left(\frac{1 + s/p_3}{K_2}\right) \tag{5.26}$$

$$= \frac{A_v \cdot (1 + s/p_2) \cdot (1 + s/p_3)}{(1 + s/p_1) \cdot (1 + s/p_2) \cdot (1 + s/p_3) + A_v K_1 K_2} \tag{5.27}$$

$$\frac{V_{out}}{V_{in}}(s = 0) \approx \frac{1}{K_1 K_2} \tag{5.28}$$

As expected, the proposed integrator causes a non-zero steady-state output referred offset voltage that is inversely proportional to the DC gain of the feedback path. To minimize the steady-state error (i.e. output referred offset voltage) we need to maximize the DC gain of the feedback path, $K_1 K_2$. Since the gain of the peak detector, K_1, is roughly unity, the gain of the feedback path is dominated by the integrator gain term, K_2.

The impact of the finite DC gain can also be seen if we plug Equation 5.28 into our system model and inspect the Bode plot of the open-loop parameter A(s) in Figure 5-12. The additional pole in the integrator transfer function changes the low frequency characteristics of A(s), as explained above, and forces us to lower the open loop gain to ensure stability. The impact of the new pole, p_3, and the finite DC gain on stability can be seen more clearly if we create a Root Locus plot of the new G(s) term in Equation 5.26. The root locus has the same shape as the root locus plot shown in Figure 3-6 located in Section 3.2. However, the loop gain where $p_{1,closed-loop}$ and $p_{2,closed-loop}$ cross into the right-half plane is reduced by approximately the magnitude of p_3, the pole location in the modified integrator transfer function. Therefore, there is a tradeoff between system stability and the magnitude of the residual offset.

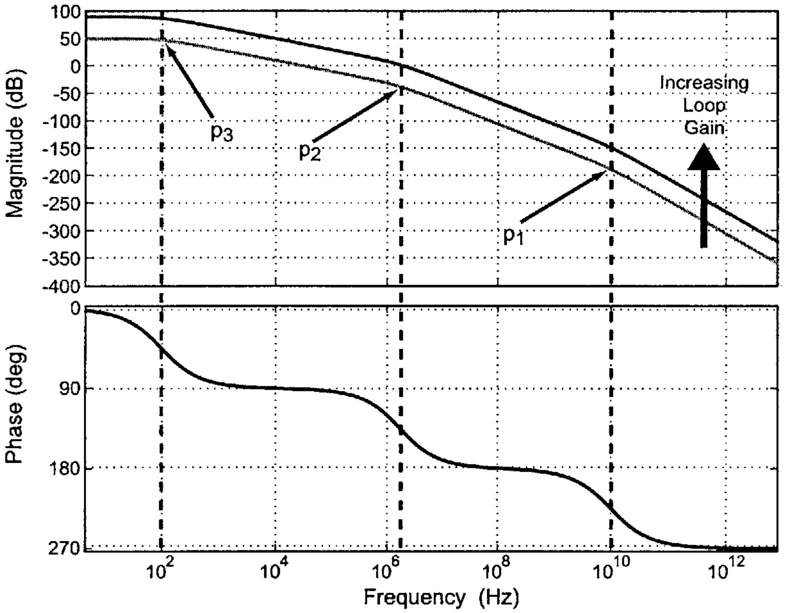


Figure 5-12: Bode Plot of Modified Open-Loop Parameter A(s)

Another issue in the design of the integrator cells relates to the overall system implementation. In Chapter 2 we determined that multiple control loops are required to account for the outputs of the limit amplifiers saturating. Also, to keep the dynamics of each of the control loops equal, both the loop gain and bandwidth of all loops must be equal. The loop bandwidth is determined by the peak detectors, which are identical in all loops. However, there are different numbers of limit amplifier stages in each control loop resulting in different gains in each of the control loops. To keep the total loop gains equal, the integrator gain, K_2, must be different for each loop. The easiest way to implement the gain variation is to create 2^{n-1} unit integrator cells, where n is the number of taps (or the number of stages in the limit amplifier in this case), and select the required number depending on which control loop is active. Since there are 7 stages in the limit amplifier, the integrator was designed as an array of 64 identical unit integrator cells with a single common load capacitance. The outputs are connected through pass-gates to control which integrators are active as shown in Figure 5-13. By superposition, the transfer function of n integrators in parallel is:

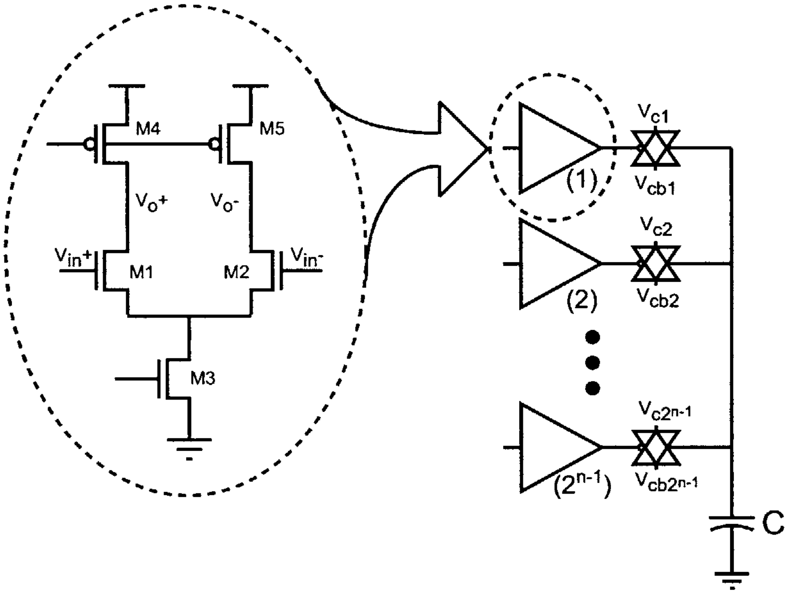


Figure 5-13: Schematic showing how integrator array is configured

$$\begin{aligned}
\frac{V_{out}}{V_{in}} &= \frac{ng_{m,M1} \cdot \frac{(R_{out,M1} \| R_{out,M4})}{n}}{1 + (R_{out,M1} \parallel R_{out,M4}) \cdot \frac{C}{n}} \qquad (5.29) \\
&= \frac{g_{m,M1} \cdot (R_{out,M1} \parallel R_{out,M4})}{1 + (R_{out,M1} \parallel R_{out,M4}) \cdot \frac{C}{n}} \qquad (5.30)
\end{aligned}$$

The DC gain of the integrator versus n is:

$$\begin{aligned}
\frac{V_{out}}{V_{in}} &= n \cdot g_{m,M1} \cdot \frac{(R_{o,M1} \parallel R_{o,M4})}{n} \qquad (5.31) \\
&= g_{m,M1} \cdot (R_{o,M1} \parallel R_{o,M4}) \qquad (5.32) \\
&= K_2 \qquad (5.33)
\end{aligned}$$

and the dominant low-frequency pole becomes:

$$p_3 = \frac{n}{(R_{o,M1} \parallel R_{o,M4}) \cdot C} \qquad (5.34)$$

This is demonstrated in Figure 5-14. As n increases, the DC gain remains constant, the dominant pole frequency increases and the effective integrator gain, or gain in the frequency range when the integrator acts as an ideal integrator, increases. Therefore, although the DC gain remains constant, the effective integrator gain is scaled linearly by the number of active integrator cells, as desired. A DC gain of 40dB was achieved by using long length devices (length= $1\mu m$) and, as will be shown in Section 6, this is large enough gain to achieve acceptably low residual output referred offset voltage.

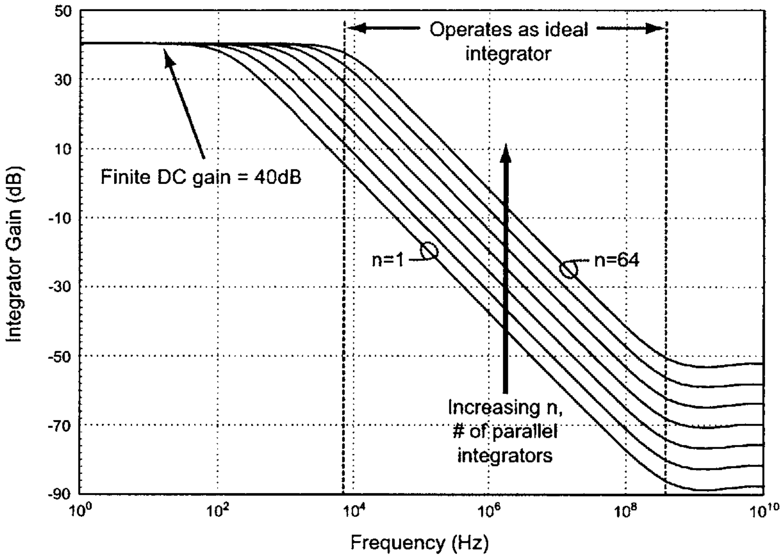


Figure 5-14: Bode Plot of integrator demonstrate how transfer function varies with n, the number of parallel integrator cells

The final two issues for the integrator design are the biasing and common-mode feedback (CMFB) implementation. Since the integrator was implemented as an array of 64 unit integrator cells, it was important to keep the biasing and, more importantly, the CMFB circuitry compact. It is especially important to keep the CMFB circuitry compact because it is repeated in each unit integrator cell. The design of both the integrator biasing network and CMFB are discussed here.

There are two typical CMFB implementations in CMOS processes. The first design requires extremely large sensing resistors to extract the output common-mode level to prevent the CMFB circuitry from loading the output of the integrator and degrading the gain and bandwidth. A simplified schematic of this approach is shown in Figure 5-15a. The second design uses a differential amplifier cell to extract the output common-mode level. The CMFB amplifier can be comparable in size to the unit integrator cell. A schematic for this approach is shown in Figure 5-15b. Neither of these CMFB approaches were acceptable because they consumed too much area.

The solution was to use the CMFB scheme shown in Figure 5-16. The the desired common-mode level is applied to the gate of M4R and device M4 (a and b) form the feedback control loop in each integrator cell [1]. The output common-mode level is defined as $(V_{out+} + V_{out-})/2$ in Figure 5-16. If the output common-mode level is at the desired level then $I_{cm} = 2I_1$, assuming that the biasing stage and the integrator

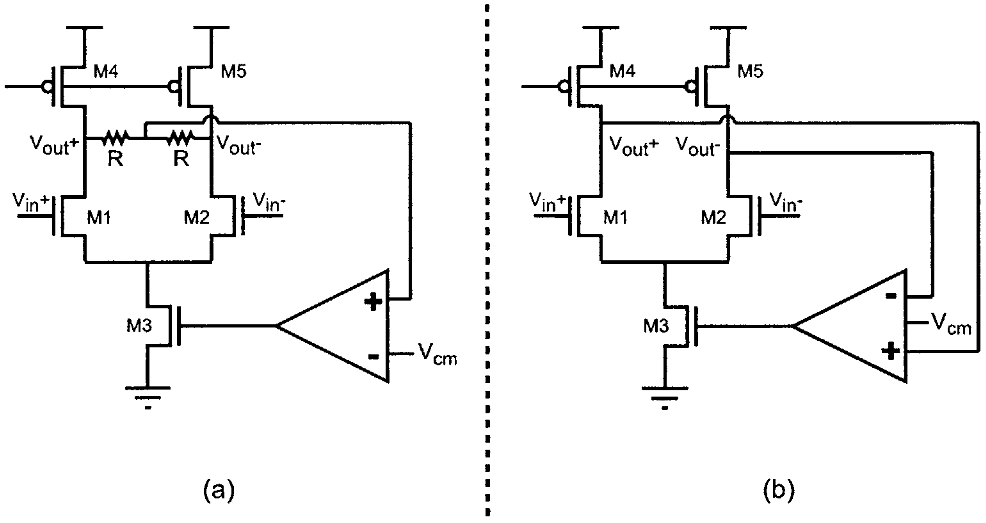

M4
M5
Vout+
Vout-
R
R
Vin+
M1
M2
Vin-
M3
+
-
Vcm
(a)
M4
M5
Vout+
Vout-
Vin+
M1
M2
Vin-
M3
-
+
Vcm
(b)

Figure 5-15: (a) CMFB with Resistive Output Common-Mode Level Sensing, (b) CMFB Using Differential Amplifier to Sense Output Common-Mode Level

cell have a 1:1 sizing ratio. However, if the output common-mode level increases, $V_{GS,M4}$ will increase causing I_{cm} to increase. I_1, the drain current of M6 and M7, will increase forcing $V_{DS,M6/7}$ to increase. The output common-mode level is then lowered back to the desired value. If the output common-mode level decreases, the operation is similar whereby I_{cm} and I_1 both decrease forcing $V_{DS,M6/7}$ to decrease. The output common-mode level will then increase to the desired value. The circuit is ideal because it operates as intended and consumes negligible die area.

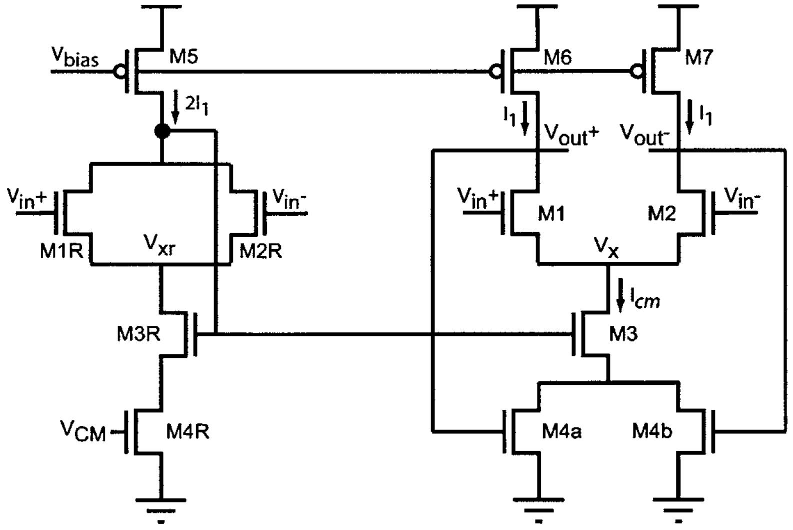

Vbias
M5
2I1
Vin+
M1R
Vxr
M2R
Vin-
M3R
VCM
M4R
M6
M7
I1
Vout+
Vout-
I1
Vin+
M1
M2
Vin-
Vx
Icm
M3
M4a
M4b

Figure 5-16: Simplified Schematic of Integrator Showing Biasing and CMFB

Figure 5-16 also shows the replica biasing, composed of transistors M1R-M4R and M6, used in the integrator. The design is based on [25]. The replica biasing stage is common to all integrator cells.

5.4 Output Buffer

The output buffer is subject to most of the same constraints as the limit amplifier. However, the output buffer must also satisfy fairly harsh output drive requirements dictated by the package parasitics and the medium that the output buffer is driving into. Luckily, the output buffer does not have to provide appreciable gain. The gain per stage only needs to be large enough to guarantee that the total output buffer gain remains greater than unity over all process, voltage and temperature corners. The model for the output bond pad, bond wire inductor package capacitance is shown in Figure 5-17. The pad capacitance, due to both the bond pad and ESD, was extracted with StarRC and found to be approximately 185fF. Based in the chip size and available packages, the bond wire inductance was assumed to be 2nH and the package capacitance was conservatively assumed to be 500fF. Finally, the transmission line at the output was assumed to be 50Ω.

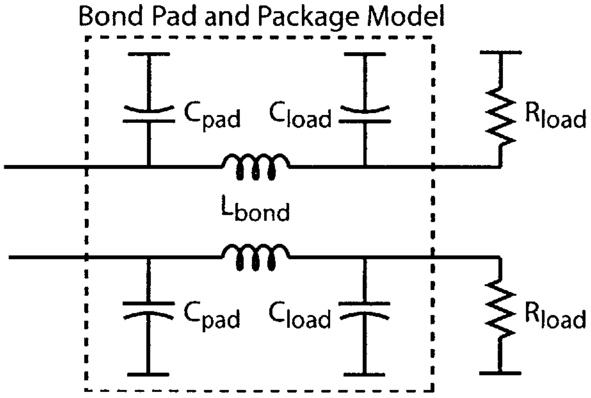


Figure 5-17: Differential Package Model Showing the Bond Pad and Package Capacitance and the Bond Wire Inductance

To drive the large load in the package model, the output buffer was designed as a cascade of 3 stages. Each successive stage has twice the output drive as the preceding stage, resulting in a total scaling of 8 [26]. Following the same design methodology used for the limit amplifier, each of the 3 stages was designed with a gain of 1.3, output swing of 750mV and bandwidth per stage of 12.5GHz. To avoid laying out 3 different high-speed amplifier stages a different approach was used. Instead of using 3 scaled stages the output drive scaling was achieved by cascading parallel configurations of a single output buffer to achieve the correct drive scaling. The conceptual schematic is shown in Figure 5-18. The final power dissipation of the output buffer is 225mW, or 125mA from a 1.8V supply, and the bias current per buffer cell is 17.9mA. The effective total bandwidth of the output buffer is 6.4GHz. Neutralization was used on the first two stages to increase the bandwidth to approximately 8.5GHz.

As with the limit amplifier, the best judge of the output buffer performance is an eye diagram. Eye diagrams of the output buffer output generated with Hspice, driving the package model, are shown in Figure 5-19 for 5Gbps and 10Gbps data. Both eye diagrams are satisfactory, although the 10Gbps output visibly has more ISI.

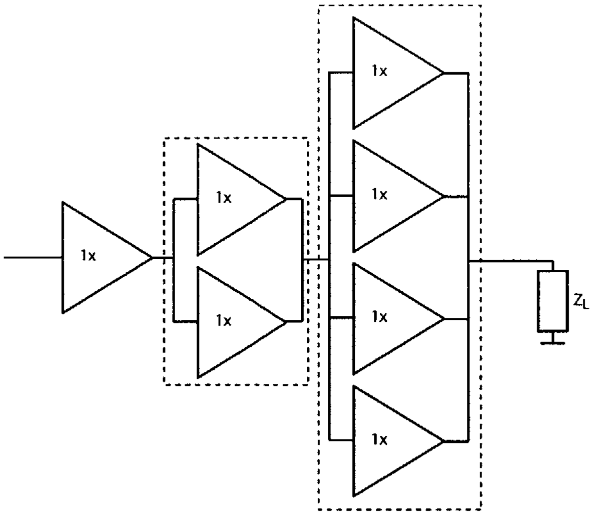


Figure 5-18: Final Output Buffer Design

The measured jitter for the two data rates due to ISI alone are $800fS_{p-p}$, or 280fS RMS, for the 5Gbps data and $1.0pS_{p-p}$, or 350fS RMS, for the 10Gbps data.

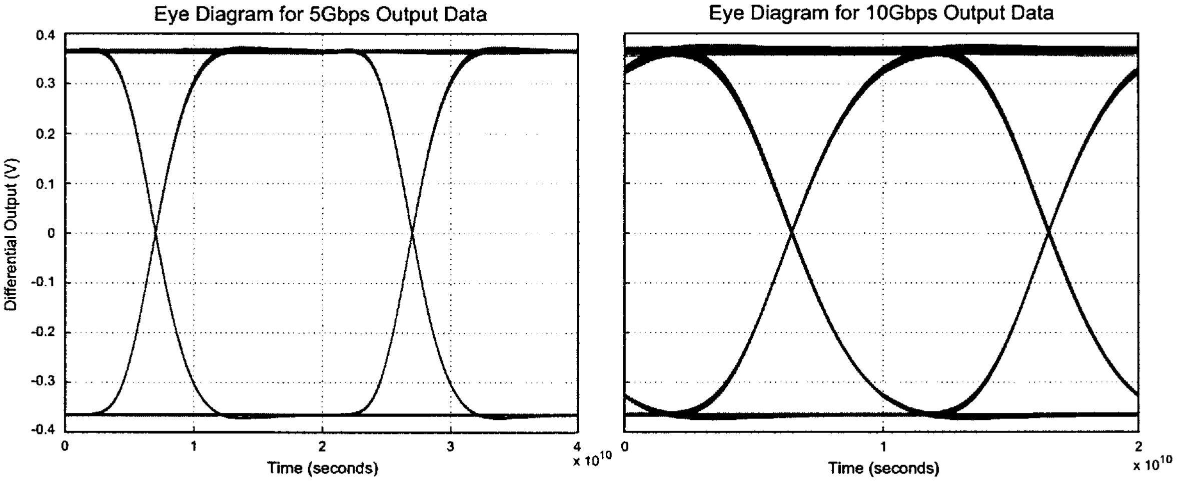


Figure 5-19: Eye Diagram at Output of Output Buffer (a) 5Gbps, (b) 10Gbps

5.5 Comparator and Logic

Comparators fall into one of two classes, clocked or unclocked, with each type having its associated strengths and weaknesses. There are several factors to consider when designing a comparator:

- Implementation complexity
- Robustness

- Power dissipation
- Speed

Each of these issues will be addressed in the design of the comparator in the feedback windowing circuitry.

The most significant advantages of clocked comparators is their inherent robustness to noise and high input sensitivity. These advantages occur because the comparison is done in a discrete-time fashion and the decision circuitry is reset prior to each comparison. In Figure 5-20, when the clk signal goes high the decision circuitry is reset to prepare for the comparison phase on the falling clock edge. The gates of M3 and $M6 - M8$ are pulled high, cutting off current flow through the output stage and forcing V_O+ and V_O- low. Nodes A and B, at the drains of M9 and M10, see a high impedance path through M7 and M8. Therefore, any charge stored at this node can not be discharged, but M11 ensures that this charge is evenly distributed between the two nodes. When the clock goes low, $M7 - M8$ turn on and M3, M6 and M11 turn off. M1 and M2 sense the input signal and mirror a current to the output stage through the PMOS current mirrors to charge nodes A and B accordingly. The decision circuitry is composed of the cross-coupled NMOS devices, $M4 - M5$, and PMOS devices, $M9 - M10$. The positive feedback of the cross-coupled devices forces the outputs to be either high or low. Since the latches are reset between each decision phase, the output does not have to over-drive the positive feedback when the input changes sign. As a result, the design can be very low power. One undesirable aspect of this design is that it requires a clock signal. One of the design goals for the offset compensation was to avoid clock signals so this design was undesirable.

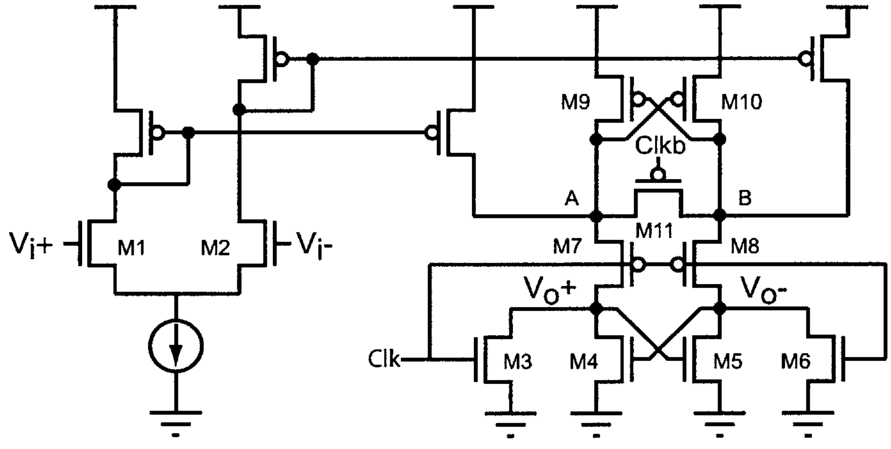


Figure 5-20: Typical Implementation of Clocked Comparator

Consider the simplified schematic of the continuous time comparator in Figure 5-21. The input stage is identical to the clocked comparator case in that it mirrors a current proportional to the input voltage through the PMOS current source devices to the output. This is where the similarities end. The mirrored current feeds diode connected NMOS devices M3 and M4. In turn, M3 and M4 generate an input voltage for M5 and M6, the input devices to the decision circuitry. The significant difference from the clocked implementation is that the decision circuitry does not have separate sample/reset and decision phases. As a result, M5 and M6 must over drive the cross-coupled PMOS devices M7 and M8 if the output is to change sign. If the comparator is designed for low power operation, $M7 - M8$ must be made small so that $M5 - M6$ can over drive their positive feedback. The problem with this approach is that the circuit will become vulnerable to noise from the rest of the system. To improve the robustness of the circuit, the power must be increased to ensure that $M7 - M8$ will reliably latch and that $M5 - M6$ can over drive the positive feedback. Therefore, there is a trade-off between power and robustness. Finally, the final comparator design has a differential to full-swing converter in the output stage so that it can drive the windowing control logic.

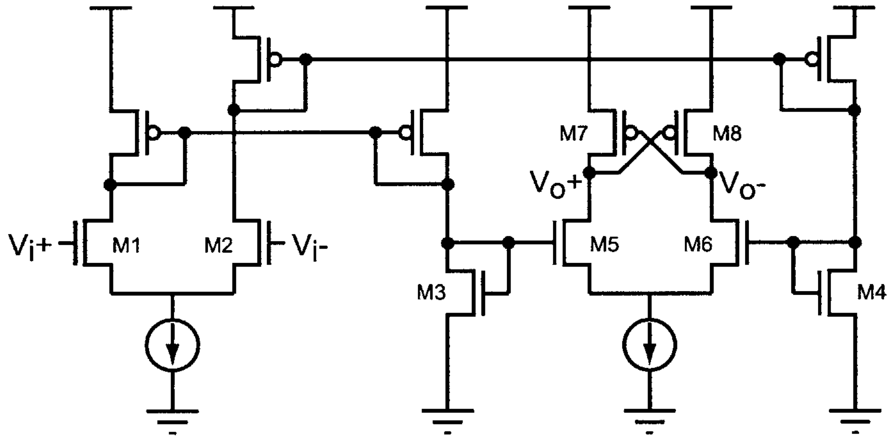


Figure 5-21: Implementation of Comparator in Windowing Block

The comparator was designed for minimum power dissipation while guaranteeing greater than 20mV of hysteresis over all process and temperature corners. The final power dissipation for each comparator is 165μW with a 1.8V supply. Additionally, the comparator operates up to a maximum frequency of 80MHz over all process and temperature corners. This performance is much greater than the targeted 10MHz bandwidth for the feedback loop. Table 5.1 summarizes the simulated hysteresis for the critical process and temperature corners.

Process Corner	Temperature	Hysteresis
Slow	70° C	19mV
Typical	25° C	36mV
Fast	0° C	43mV

Table 5.1: Simulated Hysteresis vs Process and Temperature Corner

5.6 ESD

Refer to Appendix B for the discussion of the ESD circuitry.

5.7 Summary

The design details of each of the system blocks was presented in this chapter. In the limit amplifier analysis we investigated the impact of the number of stages on total bandwidth, power dissipation and input sensitivity. It was shown that for a chain of resistively loaded, differential amplifiers it is possible to simultaneously achieve maximum bandwidth and minimum power dissipation for a given total gain and bandwidth. The final design parameters for the limit amplifier were determined based on the trade-off between bandwidth, power dissipation and input sensitivity. The peak detector was biased in subthreshold to allow for bandwidth adjustment and the impact of mismatch in the peak detector was explored. The integrator was implemented as a g_mC filter with a high DC gain and low-frequency dominant pole. The impact of the non-ideal transfer function on the system performance was determined to be acceptable. The gain of each loop is adjusted by using the appropriate number of parallel integrator base cells. Finally, the details of the output buffer, which parallel limit amplifier discussion, were presented. The next chapter will discuss behavioral and SPICE simulation results.

Chapter 6

Results

The linear modeling analysis presented in Chapter 3 is useful for evaluating stability issues of an individual control loop. However, we made several simplifying assumptions that allowed us to develop analytic expression to describe the system behavior. We now need to validate these assumptions with both behavioral and SPICE simulations of the entire system. We will explore the effect of non-idealities in the modeling of each of the system blocks such as the nonlinear transfer function of the limit amplifier and the modeling of the peak detector as a gain and simple pole. Also, we will explore the impact of multiple control loops and how transitioning between them affects the overall system response.

6.1 CppSim Modeling and Simulation Results

Performing behavioral simulations with CppSim allows the designer to quickly gain intuition about system issues and to iterate the design at a fast pace. CppSim is not intended as a replacement for SPICE simulations. Rather, CppSim is an enhancement to the tool set. Performing simulations as compiled C++ programs enhances the user's ability to design innovative solutions by dramatically shortening the design cycle. Specifics about working with CppSim can be found in the CppSim Manual, located at http://www-mtl.mit.edu/perrottgroup/tools.html.

The following sections describe how each of the system components were modeled in CppSim. The code for each block can be found in Appendix C. Following the modeling discussion, CppSim simulation results are presented.

6.1.1 Limit Amplifier

In Section 3.2 the limit amplifier was simply modeled as a gain and a single pole to enable us to get intuition about basic system issues. In reality there are several non-idealities that limit the accuracy of this basic model that should be accounted for in the behavioral model. First, the limit amplifier generally does not have a perfectly linear relationship between the input and the output. In fact, as shown in Figure 6-1, the transfer function can be modeled by a 3rd order polynomial over most of the input range. Outside of the valid input range the transfer function can be modeled by a simple limiting action. In other words, the output will be constant for inputs larger than some input amplitude determined by the limit amplifier output swing, gain and linearity.

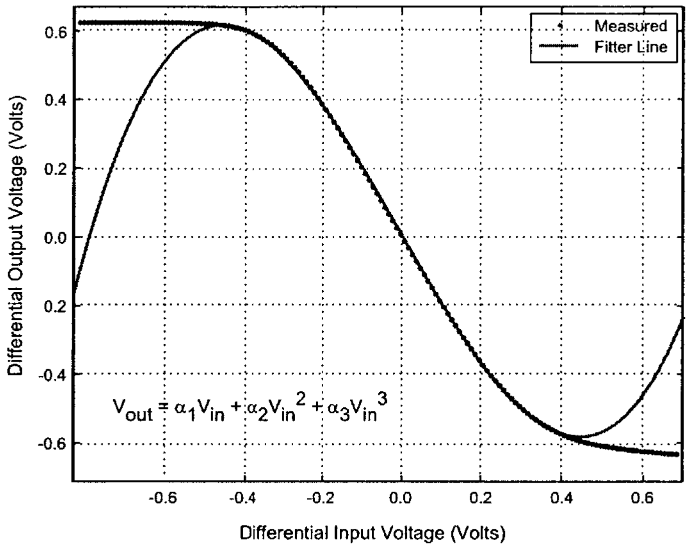


Figure 6-1: 3rd Order Polynomial Fit to Limit Amplifier Transfer Function Measured in Hspice

The approximation of modeling the frequency response of the amplifier with a single pole is valid and provides excellent results. Additional modifications to the model can be made to account for bandwidth extension techniques.

6.1.2 Peak Detector

The linear model that was developed for the peak detector simply consisted of a gain and single pole, similar to the model for the limit amplifier. As discussed in Section 2, the peak detector has asymmetric large signal tracking behavior due to the difference between the pull-up and pull-down ability of the source follower. However, based on the system modeling we know that the bandwidth of the peak detector, which roughly corresponds to the loop bandwidth, is much lower than the data rate. The peak detector simply filters the high-frequency components of the limit amplifier output and extracts the DC component and the large signal changes in the limit amplifier output are rejected by the peak detector. Changes in the instantaneous DC component of each limit amplifier output are small in amplitude and occur at a rate determined by the loop bandwidth. Therefore modeling the peak detector as a simple low-pass filter is accurate for this specific system.

6.1.3 Integrator

The integrator model needs to account for the non-ideal, low-pass transfer function of the design discussed in Section 5. The model for the integrator is a simple low-pass filter and is very similar to the model for the peak detector.

6.1.4 Control Logic

Specifics of the models for each of the CppSim modules can be found in Appendix C.

6.2 CppSim Simulation Results

The two metrics that we are interested in measuring with CppSim are compensation settling time and output jitter versus loop bandwidth. In CppSim, simulations were performed with the loop bandwidth ranging from 1MHz to 10MHz, a data rate of 5Gbps and input amplitude of $5mV_{p-p}$. The system settling time can be measured from the settling of the control voltage and the output jitter can be measured from an eye diagram of the differential output signals. Figure 6-2 shows three plots of the control voltage that correspond to loop bandwidths of (A) 1MHz, (B) 5MHz and (C) 10MHz. Approximate settling times for the 3 cases are $1\mu S$, 200nS and 100nS, respectively. All three designs meet the settling time goal of $1\mu S$ and agree well with the behavior predicted by the linear modeling in Chapter 3. Figure 6-3 exhibits corresponding eye diagrams for the same 3 loop bandwidths. The impact of the bandwidth on the output jitter is readily apparent. Interestingly, the measured peak-to-peak jitter for the three bandwidths are 1pS, 5pS and 10pS.

To meet the specified jitter target of the design there is a maximum loop bandwidth for a given data rate. There is also a lower bound on settling time, based on the jitter performance, which is dependent on the data rate. The dominant cause of jitter in these simulations is the data dependence of the compensation control voltage. As explained in Chapter 2, the data dependence is caused by the droop at the output of the peak detector, which is proportional to the symbol period of the data. Therefore, higher data rates result in lower absolute jitter. However, most jitter specifications are relative and are expressed as a percentage of the minimum symbol period. Since both the absolute jitter and the minimum symbol period decrease as the data rate increase, the minimum settling for a given design should remain roughly constant for a given relative jitter goal, independent of data rate.

6.3 Hspice Simulation Results

This section will discuss the Hspice simulation results and compare them to the CppSim simulation results. The circuit design details were discussed in Chapter 5. Similar to the CppSim simulations, the SPICE design was simulated with the loop bandwidth ranging from 1MHz to 10MHz, a data rate of 5Gbps and input amplitude of $5mV_{p-p}$. Figure 6-4 shows three plots of the control voltage that correspond to loop bandwidths of (A) 1MHz, (B) 5MHz and (C) 10MHz. Approximate settling times for the 3 cases are 800ns, 400nS and 200nS, respectively. The settling time performance for the three cases are in good agreement with the CppSim results. Figure 6-5 exhibits corresponding eye diagrams for the same 3 loop bandwidths. Both the shape of the

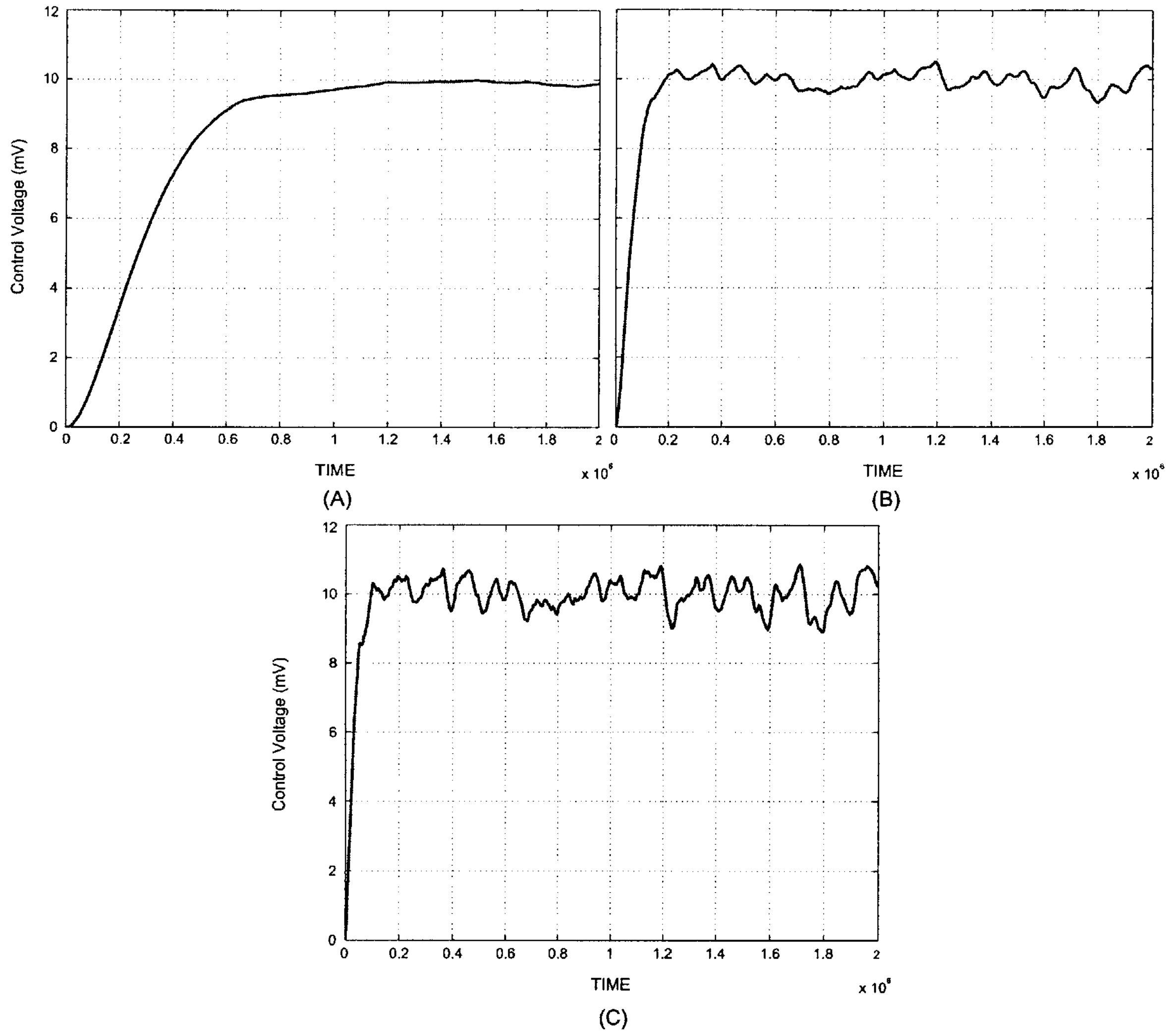


Figure 6-2: Control voltage of offset compensation loop during compensation from CppSim: (A) 1MHz bandwidth, (B) 5MHz bandwidth, (C) 10 MHz Bandwidth

eye and the jitter behavior are in excellent agreement with the CppSim result. The close match is due to the modeling of the non-linearities of the limit amplifier.

6.4 Summary

The simulations results presented show that the offset compensation loop operates as intended. More extensive simulation result will be conducted to verify the full set of design specifications. Noise simulations, extracted simulations with StarRC and Monte Carlo simulations. Additionally, the trade-off between loop bandwidth and output jitter will be characterized in Hspice and compared to the results from CppSim. Finally, the Hspice results will be compared to measure results from packaged parts.

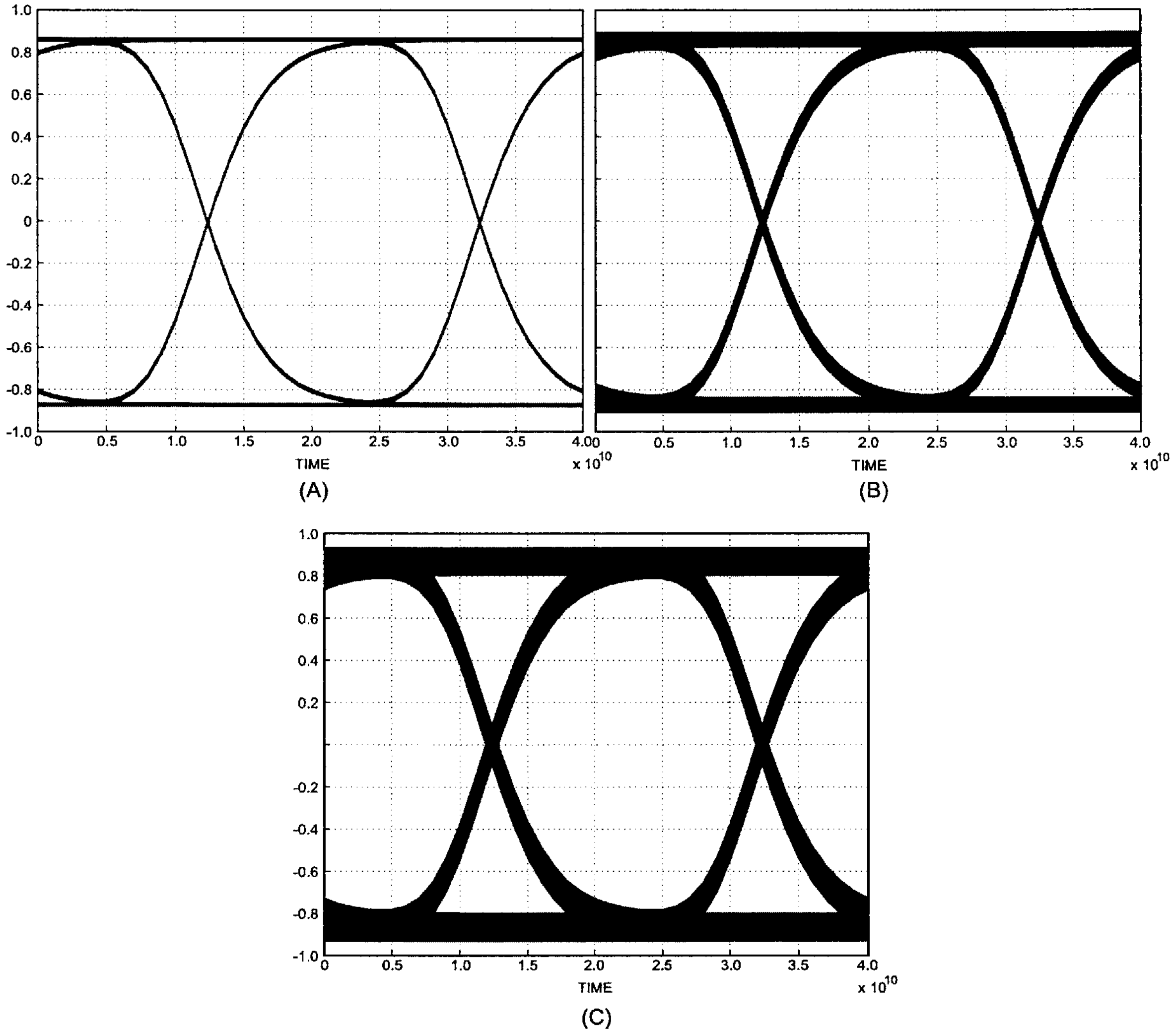


Figure 6-3: Eye diagram of limit amplifier output after compensation from CppSim

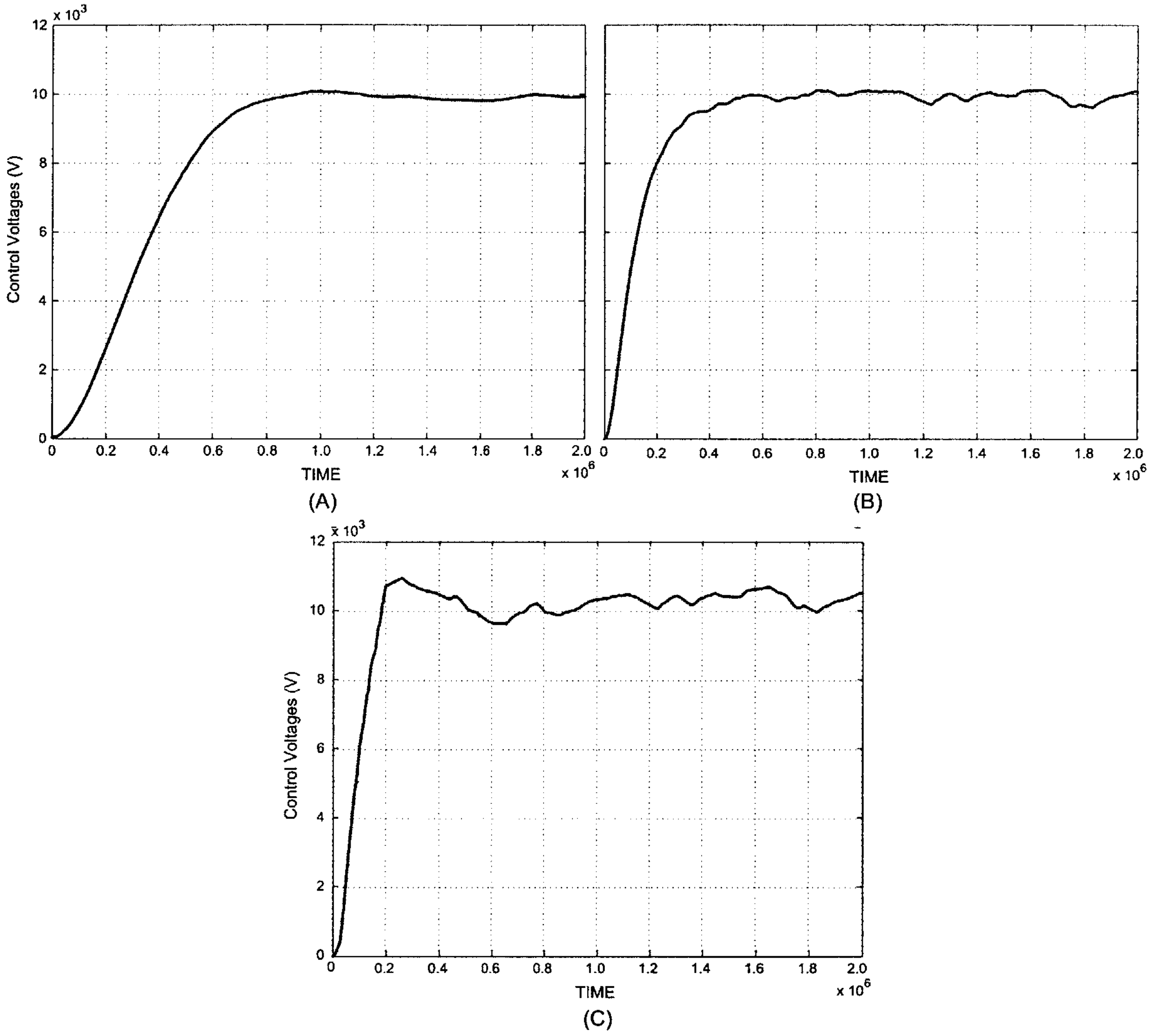
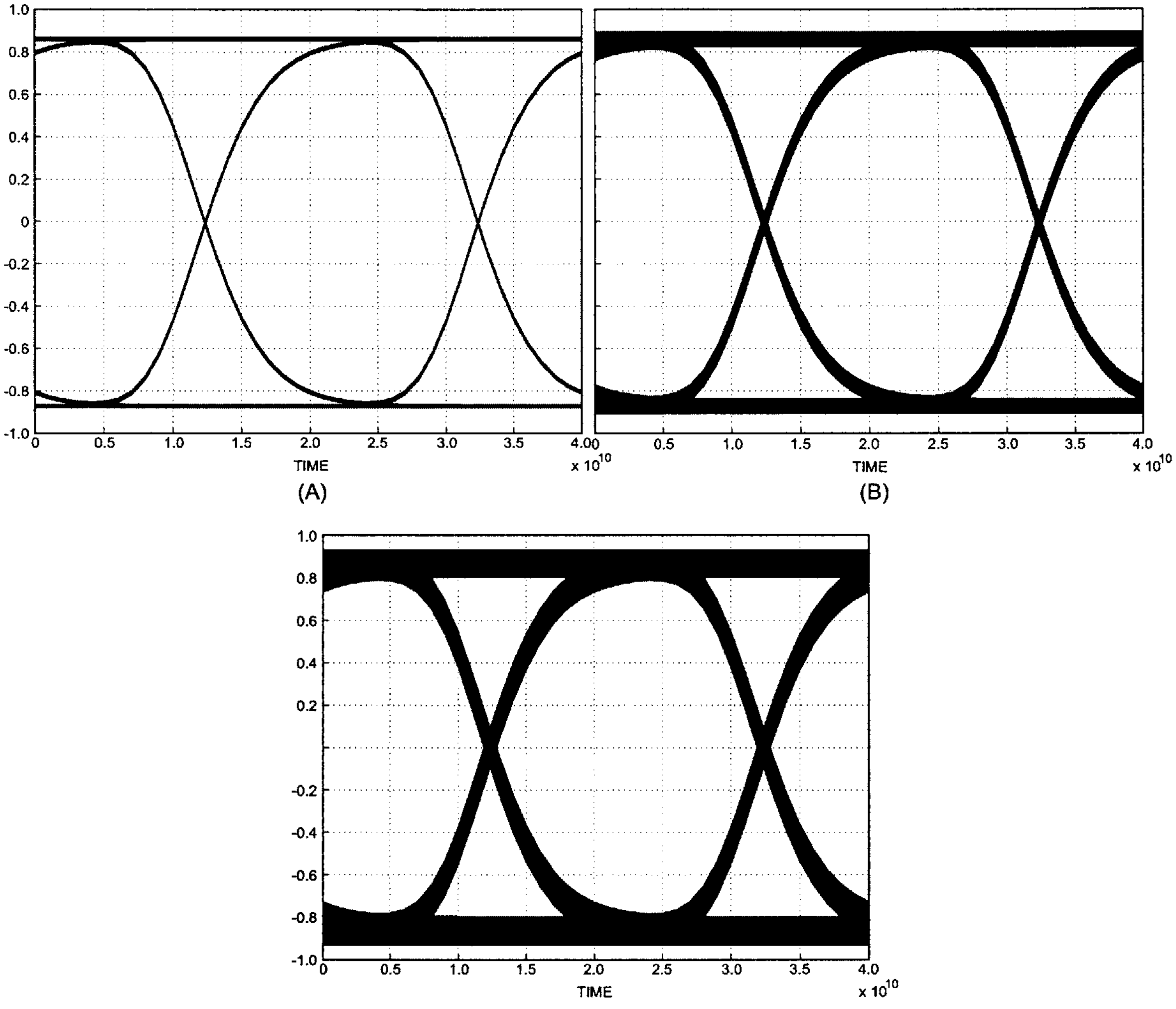


Figure 6-4: Control voltage of offset compensation loop during compensation from Hspice: (A) 1MHz bandwidth, (B) 5MHz bandwidth, (C) 10 MHz Bandwidth



(A)

(B)

(C)

Figure 6-5: Eye diagram of limit amplifier output after compensation from Hspice

Chapter 7

Layout

In this chapter key layout details that impact the performance of the forward amplifier path and the offset compensation are discussed. Since both the forward data path and the feedback compensation path are differential, inevitable mismatches between the devices in the two paths will add offset to the loop. Mismatches in the forward path will be compensated for by the feedback loop, but offset introduced by the feedback path will be simply low pass filtered and appear directly at the output. The layout of the limit amplifier cells is optimized for high-speed operation at the expense of matching issues. Techniques such as common-centroid layout and the addition of dummy devices must be used in the feedback cells in addition to sizing and biasing devices for acceptable matching. The layout for cells in the feedback path will be discussed in the context of matching and the layout of the limit amplifier will be discussed in the context of achieving maximum bandwidth and an acceptable level of matching.

7.1 Peak Detector

As mentioned in Chapter 5, the input devices of the peak detector are sized to achieve an acceptable trade-off between matching of the devices in the differential paths and the impact on the limit amplifier bandwidth. To enhance the matching between the two input devices in the peak detector, a common centroid layout and dummy devices were used as shown in Figure 7-1. The maximum bandwidth of the peak detector is less than 20MHz so the added capacitance from the dummy devices could be tolerated. Additionally, a guard-ring completely surrounds the peak detector and isolates the sensitive input devices from substrate noise. Finally, no metal interconnect overlaps the sensitive poly gates of the input devices.

7.2 Integrator

Similar to the peak detector, offset between the differential input devices of the integrator are directly referred to the output through a low-pass filter transfer function. Therefore, the devices were laid out with dummy loading devices to either side, as

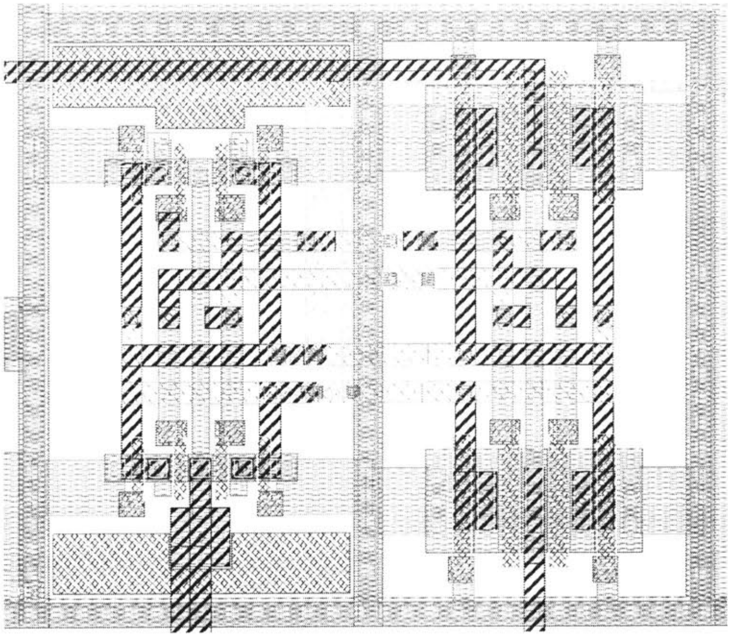


Figure 7-1: Detail of Peak Detector Cell Showing Common-Centroid Layout and Dummy Devices

shown in the top of Figure 7-2. The tail current-source devices are located at the bottom of the cell and arranged as an array of parallel gates with dummy loading devices on either end. The interconnect for biasing and data signals are located in the center and form buses that connect adjacent cells in the array. Also similar to the layout for the peak detector, substrate guard-rings surround all sensitive circuitry. The top level layout of the integrator cell, an array of 64 integrator base cells, is shown in Figure 7-3.

7.3 High Speed Limit Amplifier

Unlike the peak detector and integrator layouts where matching was the biggest concern, the focus in the layout of the limit amplifier, Figure 7-4, is to minimize parasitic capacitance. To this end, the aspect ratio of the limit amplifier cell, or the ratio between the width and height of the cell, is quite small to minimize the length of the interconnect. To balance the impact of the RC time-constant of the interconnect and the coupling capacitance to ground, the signal lines are $2\mu m$ wide. Also, to minimize the coupling capacitance between the differential signal lines, a ground shield is place between the lines and all interconnect lines are separated by $3\mu m$. Also, no dummy stripes or devices were used.

Due to the large bias currents in the limit amplifier, required by the input transistors for high-speed operation, special care was used in sizing all of the metal interconnect. The tail current source device, located at the bottom of the cell, is large to achieve a low over-drive with the large bias current levels. Substrate taps are located to either side of the bias current device to ensure that the local substrate remains

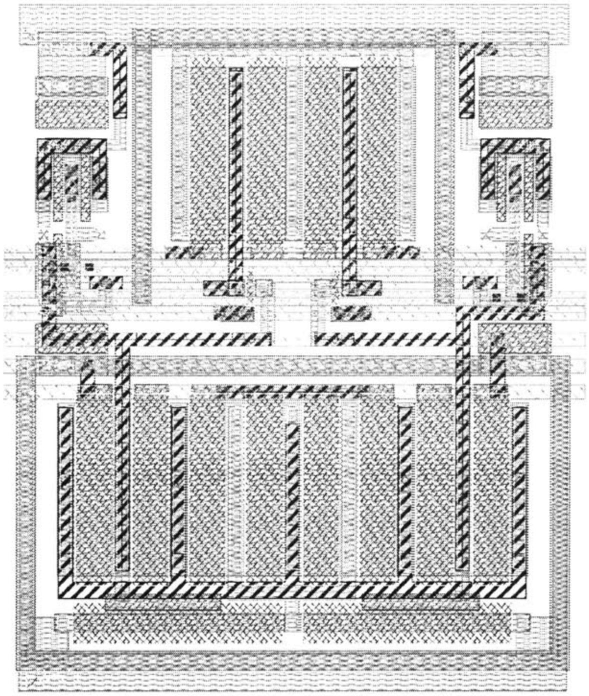


Figure 7-2: Layout of Base Integrator Cell

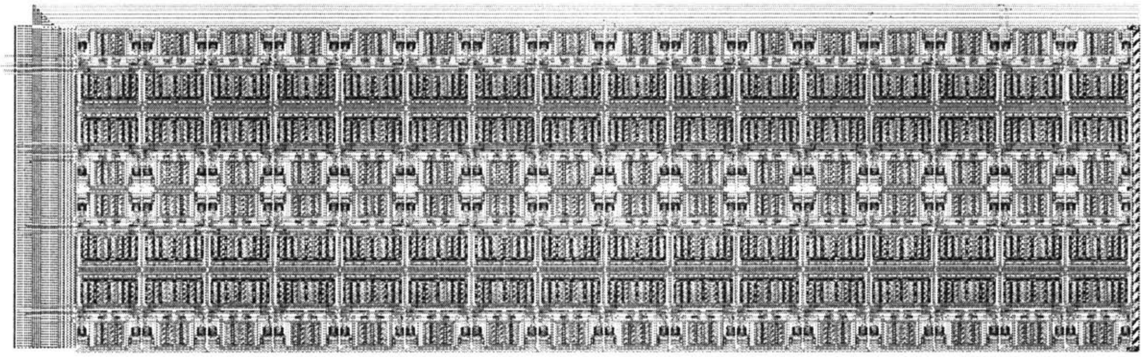


Figure 7-3: Layout of Integrator Array

grounded.

The complete limit amplifier layout, shown in Figure 7-5, consists of 7 base cells in parallel sharing a common power and ground bus. The total signal path length in the limit amplifier is less than $200\mu m$ and the resulting bandwidth is greater than 50GHz.

7.4 Output Buffer

The layout concerns for the output buffer are similar to those in the limit amplifier, but perhaps more severe. The current levels in the output buffer are approximately three times larger than in the limit amplifier so the current carrying metal lines are exceptionally large. Also, since the tail current source is proportionally larger than

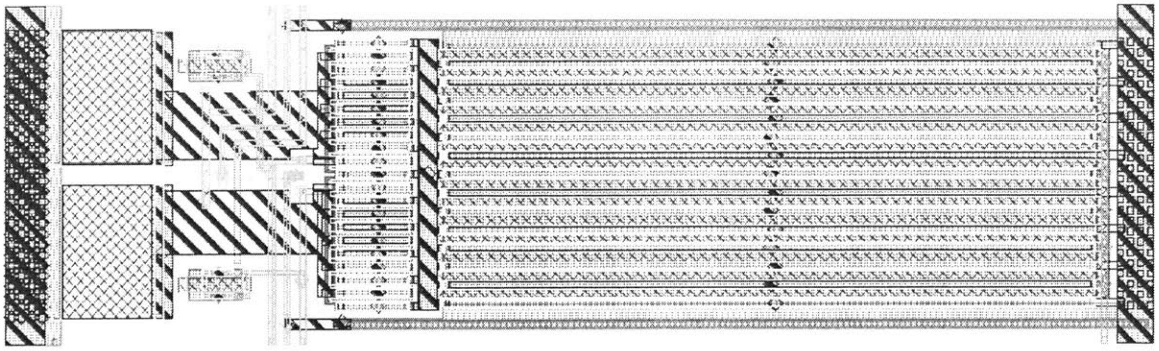


Figure 7-4: Layout of Limit Amplifier Stage

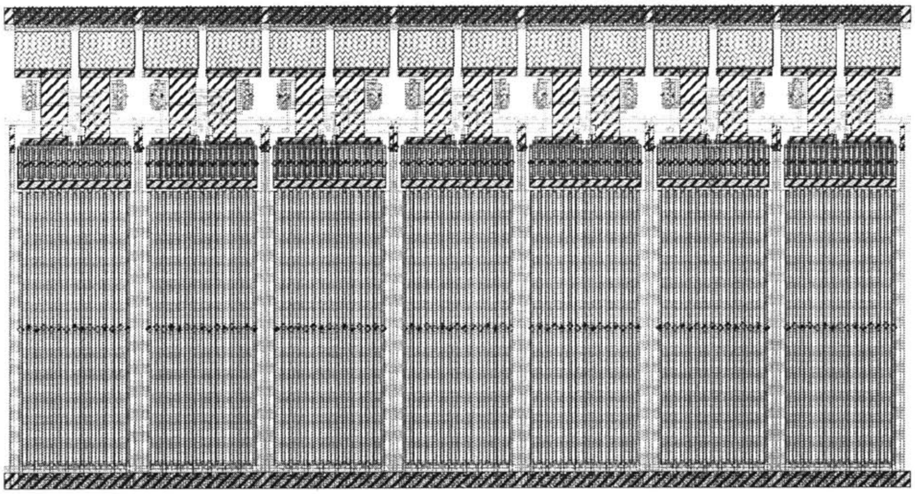


Figure 7-5: Layout of Limit Amplifier Top Level

the tail-current device in the limit amplifier cell, additional substrate taps must be placed at its center. The output buffer layout is shown in Figure 7-6.

7.5 Top Level

The top level layout view is shown in Figure 7-8. The final die size, after shrink, is just over $1mm \times 1mm$. The system component cells were laid out to minimize interconnect length, to ensure that there is sufficient power and ground bussing to all cells and to satisfy the strict density rules for poly, composite and each of the metal layers.

Both the limit amplifier and the output buffer are located close to bond pads, in the center of the left side and bottom, respectively, to minimize the on-chip interconnect length. Also, the interconnect between the bond pads and the limit amplifier and output buffer cells is laid out symmetrically (i.e. the two differential paths are the same length and have the same bends).

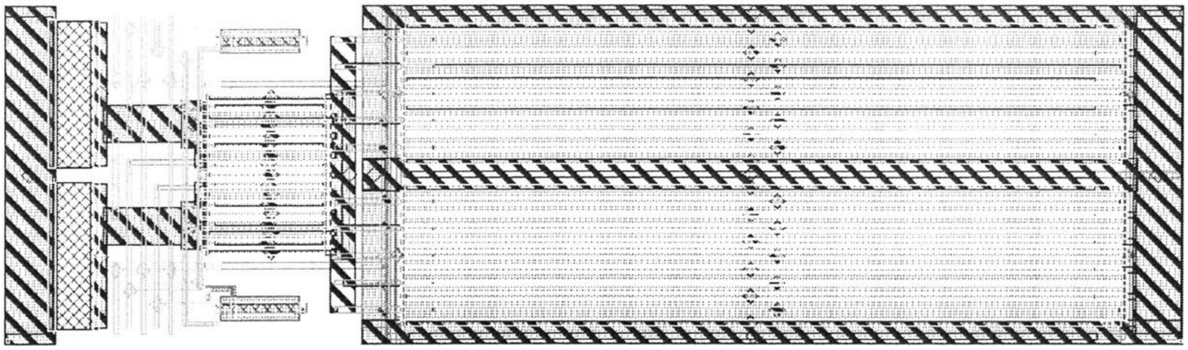


Figure 7-6: Layout of Output Buffer Stage

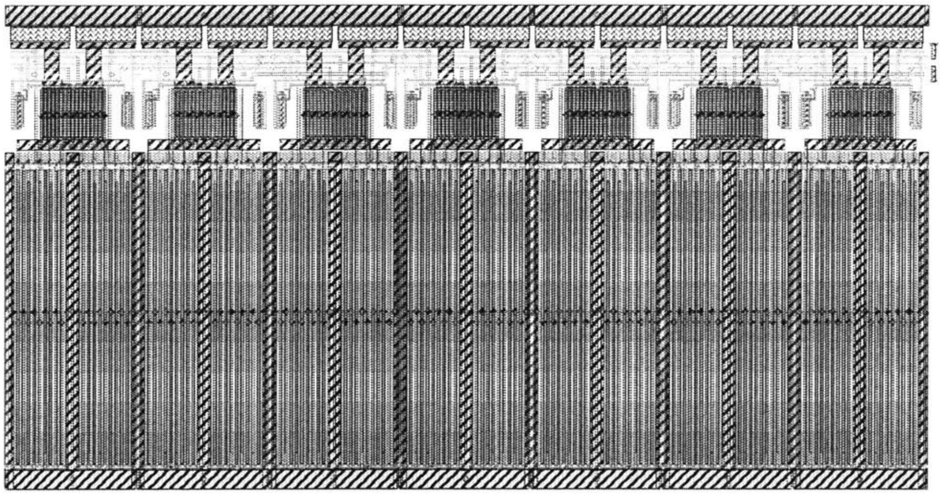


Figure 7-7: Layout of Output Buffer Top Level

7.6 Summary

In this chapter the critical layout issues for each of the cells was discussed. Matching issues are paramount for both the peak detector and integrator cells so common-centroid layout configurations and dummy loading devices were used. However, speed is the critical issue in the limit amplifier over matching. The layout of the limit amplifier cells is symmetric to improve matching between the differential paths but the layout is optimized to minimize diffusion and interconnect capacitances. The layout of the output buffer parallels the layout of the limit amplifier. The individual cells were arranged in the top-level layout to minimize interconnect length and to spatially isolate the high-speed blocks from the sensitive feedback cells.

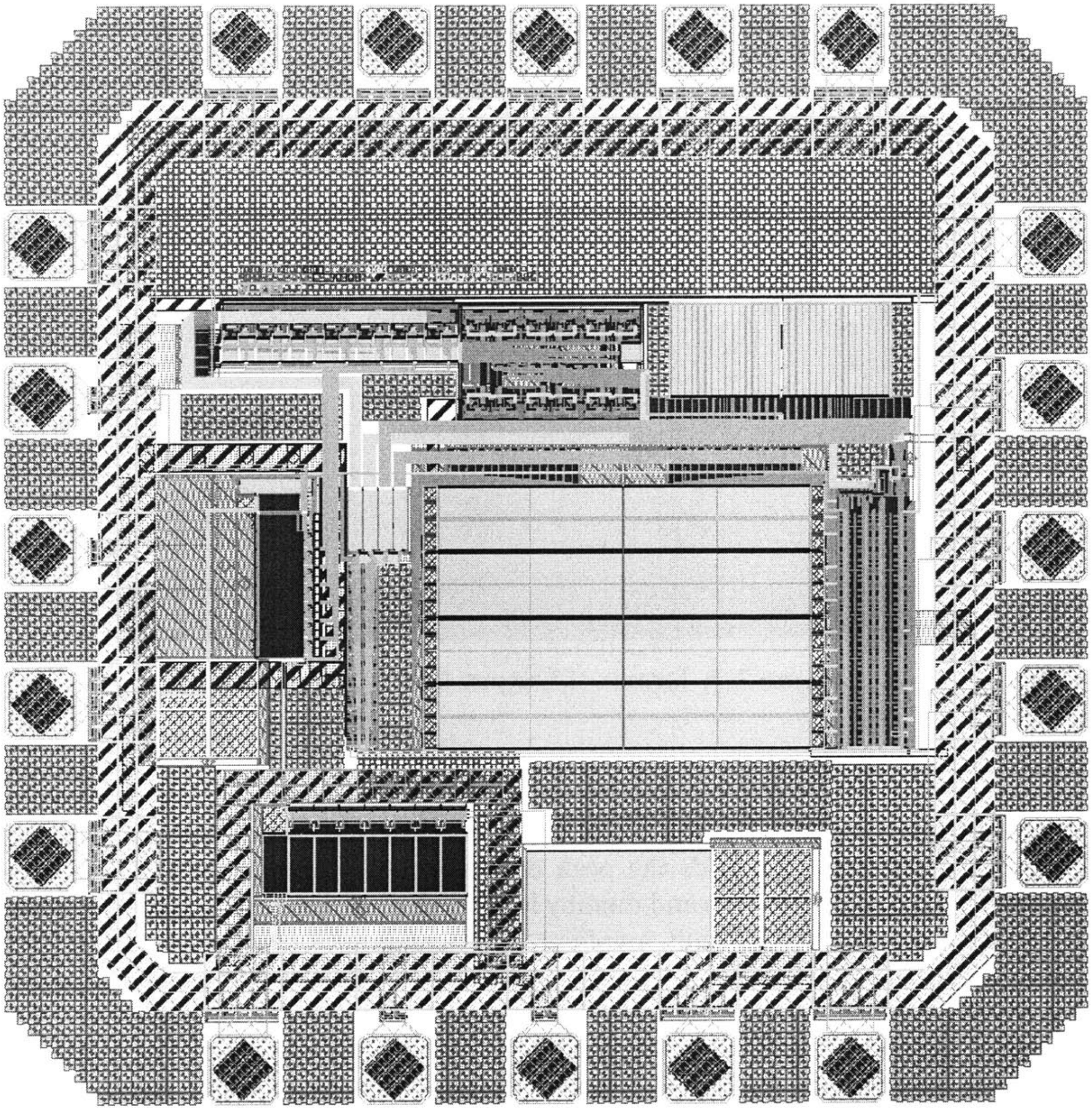


Figure 7-8: Layout of Chip Top Level

Chapter 8

Conclusions and Future Work

The design of a low power, fully integrated, fast offset compensation system for high-speed data-links was described in this thesis. The system meets all of the performance goals of total compensation time, output jitter and residual offset voltage. The key enabling system component, the peak detector, allows this design to achieve similar jitter and residual offset performance to current compensation techniques while achieving superior settling time performance. Additionally, the design eliminates the need for expensive off-chip components, which is attractive in the drive to reduce component count and system costs.

The initial system architecture and performance were proven in CppSim, a fast and accurate behavioral simulator, and verified in SPICE. The system was implemented in National Semiconductor's $0.18\mu m$ CMOS9 process and is currently in the process of fabrication. Measured results will be compared to simulated results when parts are available.

8.1 Contributions

The key contribution of this thesis is the introduction of a new offset compensation implementation for CMOS limit amplifier that significantly reduces the dependence of output jitter on loop bandwidth, or settling time. In all current offset compensation designs that we are aware of the output jitter is proportional to the loop bandwidth. As a result, all of these systems suffer from long compensation time to meet strict jitter specifications. By taking advantage of the symmetry of the limit amplifier design, a novel peak detector design was developed that allows the designed system to modify this relationship. Both the bandwidth and droop of traditional peak detectors are proportional to the bias current. However, only the bandwidth is dependent on the bias current in the proposed design. The droop is determined by NMOS off-state leakage current. The designed offset compensation loop achieves both fast settling time and low output jitter.

Additionally, a novel numerical design procedure was developed for high-speed, resistor loaded, differential, CMOS amplifiers. Extremely accurate designs are realized because inaccurate square-law models are replaced with simulated device characteristics from SPICE. The design procedure was implemented in a Matlab script and is available from http://www-mtl.mit.edu/perrottgroup/tools.html.

8.2 Future Work

A possible enhancement to the proposed approach would allow us to further alleviate the trade-off between settling time and jitter. We want to achieve very fast settling time but also have low output jitter. The compensation time of the system is proportional to the loop bandwidth. However, even with the proposed design there is a trade-off between settling time and output jitter - faster settling times result in higher jitter. We could slightly modify the existing design so that the loop bandwidth adapts based on the required operation. The loop bandwidth could be increased to provide fast settling performance during initial compensation and then decreased to provide low jitter performance during steady-state operation. This could be accomplished simply by controlling the peak detector bias current and would provide further performance enhancements.

A possible extension of the work completed in this thesis is to investigate the application of the proposed peak detector to AGCs. AGCs are prevalent in bipolar processes but see limited application in CMOS designs because it is difficult to perform the amplitude detection. Current CMOS AGC designs use complex peak detector circuitry in the gain control loop. The proposed design offers a simple alternate means of performing the peak detection.

The system described in this thesis was specifically designed to be used in wireline applications with NRZ data. However, the issue of offset compensation is not restricted to broadband systems. Offset is also a significant issue in direct conversion wireless systems and it would be interesting to investigate the application of this compensation technique to direct conversion receiver designs.

A full characterization of the relationship between the loop bandwidth and the resulting jitter performance was not completed in this thesis. However, the circuitry required to adjust the loop bandwidth, and the required loop gain, were included in the system design. When final packaged parts are available, this analysis will be performed and measured results will be compared to the simulated results.

Appendix A

Derivation of Input Referred Offset Voltage

Following are the derivations for offset voltage assuming both square-law operation and velocity saturation. As will be shown, the results have similar forms. In fact, the results are only different by a fixed scale factor and, as expected, the result assuming velocity saturation is dependent on L through the V_{TH} term. In reality, the offset voltage will be somewhere in between these two results. For the following discussion refer to Figure A-1.

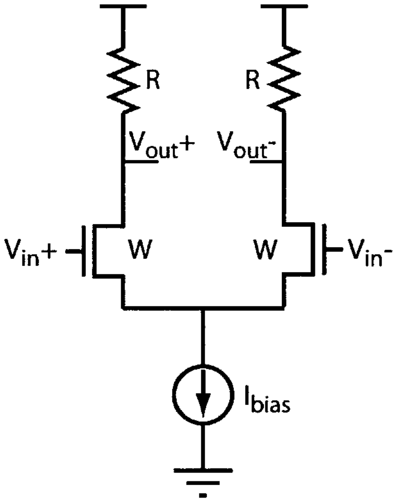


Figure A-1: Implementation of Each Stage in Limit Amplifier

In order to quantify the offset voltage as a function of circuit parameters, consider, as mentioned in Chapter 1, mismatches in the transistor physical dimensions, where $(W/L)_1 = W/L$ and $(W/L)_2 = W/L + \Delta(W/L)$, transistor threshold voltages, where $V_{TH1} = V_{TH}$ and $V_{TH2} = V_{TH} + \Delta V_{TH}$, and the load resistor values, where $R_1 = R$ and $R_2 = R + \Delta R$. In order for $V_{out} = 0$, $I_1 R_1 = I_2 R_2$, which means $I_1 \neq I_2$, since $R_1 \neq R_2$[1]. Similar to the previous parameterizations, $I_1 = I$ and $I_2 = I + \Delta I$.

A.0.1 Square-Law Operation

Following is the development assuming square-law operation. We can quantify the currents in M_1 and M_2 as:

$$I_1 = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \tag{A.1}$$

Solving for V_{GS} :

$$V_{GS} = \sqrt{\frac{2I}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{TH} \tag{A.2}$$

With $V_{os,in} = V_{GS1} - V_{GS2}$, substituting for the appropriate parameters yields:

$$V_{os,in} = \sqrt{\frac{2I_1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{TH1} - \sqrt{\frac{2I_2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_2}} - V_{TH2} \tag{A.3}$$

$$= \sqrt{\frac{2}{\mu_n C_{ox}}} \cdot \left[\sqrt{\frac{I}{(W/L)}} - \sqrt{\frac{I + \Delta I}{(W/L) + \Delta(W/L)}}\right] \tag{A.4}$$

$$= \sqrt{\frac{2}{\mu_n C_{ox}}} \cdot \sqrt{\frac{I}{(W/L)}} \cdot \left[1 - \sqrt{\frac{1 + (\frac{\Delta I}{I})}{1 + \frac{\Delta(W/L)}{(W/L)}}}\right] \tag{A.5}$$

To recast the above expression in terms of the transistor and resistor physical parameters, we need to solve for $\Delta I/I$ in terms of $\Delta R/R$. From before, $R_1 = R$, $R_2 = R + \Delta R$, $I_1 = I$ and $I_2 = I + \Delta I$. To satisfy the condition that $V_{out} = 0$, $I_1 R_1 = I_2 R_2$:

$$IR = (R + \Delta R) \cdot (I + \Delta I) \tag{A.6}$$

$$= IR + \Delta I R + I \Delta R + \Delta I \Delta R \tag{A.7}$$

$$\approx IR + \Delta I R + I \Delta R \tag{A.8}$$

After solving for $\Delta I/I$, assuming that the product of two small quantities approaches zero and recognizing that $\frac{2I}{\mu_n C_{ox}(W/L)} = (V_{GS} - V_{TH})^2$, the following equation results:

$$V_{os,in} = \frac{(V_{GS} - V_{TH})}{2} \cdot \left[\frac{\Delta(W/L)}{(W/L)} + \frac{\Delta R}{R}\right] - \Delta V_{TH} \tag{A.9}$$

Finally, recognizing that offset voltage is a statistical value, similar to noise, we can square each side of the last equation to find the standard deviation of the input referred offset voltage.

$$V_{os,in}^2 = \left(\frac{V_{GS} - V_{TH}}{2}\right)^2 \cdot \left\{\left[\frac{\Delta(W/L)}{(W/L)}\right]^2 + \left[\frac{\Delta R}{R}\right]^2\right\} + \Delta V_{TH}^2 \tag{A.10}$$

A.0.2 Velocity Saturation

Following is the development assuming velocity saturation. We can quantify the currents in M_1 and M_2 as:

$$I_1 = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) \cdot V_{DSAT} \tag{A.11}$$

$$= \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) \cdot L E_{SAT} \tag{A.12}$$

Solving for V_{GS} :

$$V_{GS} = \frac{2}{\mu_n C_{ox} E_{SAT}} \cdot \left(\frac{I}{W}\right) + V_{TH}$$

With $V_{os,in} = V_{GS1} - V_{GS2}$, substituting for the appropriate parameters yields:

$$V_{os,in} = \frac{2}{\mu_n C_{ox} E_{SAT}} \cdot \left(\frac{I_1}{W_1}\right) + V_{TH1} - \frac{2}{\mu_n C_{ox} E_{SAT}} \cdot \left(\frac{I_2}{W_2}\right) + V_{TH2} \tag{A.13}$$

$$= \frac{2}{\mu_n C_{ox} E_{SAT}} \cdot \left(\frac{I}{W} - \frac{I + \Delta I}{W + \Delta W}\right) - \Delta V_{TH} \tag{A.14}$$

$$= \frac{2I}{\mu_n C_{ox} E_{SAT} W} \cdot \left(1 - \frac{1 + \frac{\Delta I}{I}}{1 + \frac{\Delta W}{W}}\right) - \Delta V_{TH} \tag{A.15}$$

To recast the above expression in terms of the transistor and resistor physical parameters, we need to solve for $\Delta I/I$ in terms of $\Delta R/R$. From before, $R_1 = R$, $R_2 = R + \Delta R$, $I_1 = I$ and $I_2 = I + \Delta I$. To satisfy the condition that $V_{out} = 0$, $I_1 R_1 = I_2 R_2$:

$$IR = (R + \Delta R) \cdot (I + \Delta I) \tag{A.16}$$

$$= IR + \Delta IR + I\Delta R + \Delta I\Delta R \tag{A.17}$$

$$\approx IR + \Delta IR + I\Delta R \tag{A.18}$$

After solving for $\Delta I/I$, assuming that the product of two small quantities approaches zero and recognizing that $\frac{2I}{\mu_n C_{ox} E_{SAT} W} = (V_{GS} - V_{TH})$, the following equation results:

$$V_{os,in} = (V_{GS} - V_{TH}) \cdot \left[\frac{\Delta W}{W} + \frac{\Delta R}{R}\right] - \Delta V_{TH} \tag{A.19}$$

Finally, recognizing that offset voltage is a statistical value, similar to noise, we can square each side of the last equation to find the standard deviation of the input referred offset voltage.

$$V_{os,in}^2 = (V_{GS} - V_{TH})^2 \cdot \left[\left(\frac{\Delta W}{W}\right)^2 + \left(\frac{\Delta R}{R}\right)^2\right] + \Delta V_{TH}^2 \tag{A.20}$$

Appendix B

Circuit Design Details

B.1 ESD Design

It is essential to add ESD protection to all pins that interact with the outside world. Static charge during the manufacturing, packaging and testing of the parts can destroy sensitive circuitry at the outputs of the chip if ESD is not added. However, the ESD circuitry adds capacitance that is directly proportional to the level of protection it provides. Therefore, there is a direct conflict between high-speed operation and the necessary ESD protection.

To achieve the greatest flexibility in the chip design, custom ESD cells were created. A simplified schematic of the basic ESD structure used is shown in Figure B-1. The ESD protection essentially forms a high-pass filter with a very high cut-off frequency formed by the gate resistance and the capacitances at the drain of the NMOS device. The transfer function can be approximated by:

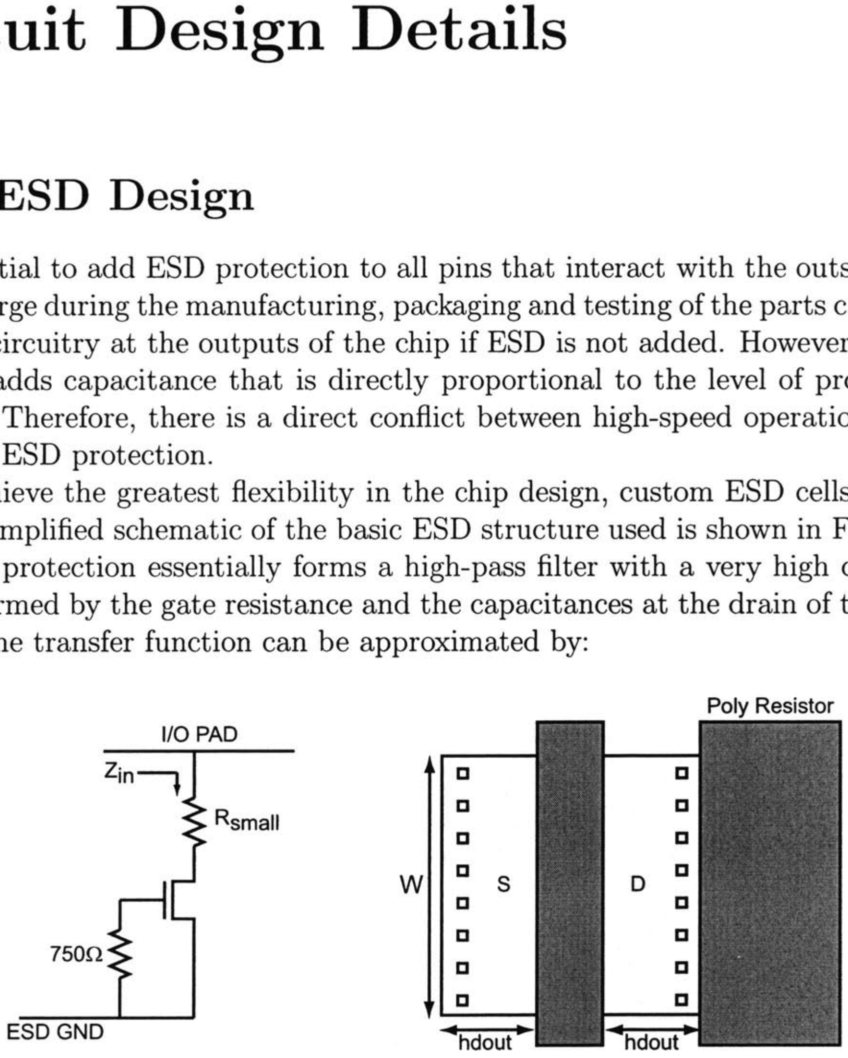


Figure B-1: Simplified schematic of ESD circuitry used on all pads

$$Z_{in}(s) = \frac{1}{sC_{gd}} \cdot \left[\frac{1 + R_g(C_{gd} + C_{gs})s}{1 + g_m R_g + R_g C_{gd} s}\right] \simeq \frac{1}{sC_{gd}} \qquad \text{(B.1)}$$

The level of ESD protection is controlled primarily by the device width, W. The gate resistance, Rg, has limited impact based on analytical analysis and Hspice simulations. As a rough rule of thumb, the structure provides 10V of protection per μm of gate width. Additionally, the gate resistance should be sized somewhere between 300Ω and $1k\Omega$ to achieve the desired level of protection. The small series resistor at the drain of NMOS is used in lieu of an unsilicided region and acts as a current limiter to protect the NMOS device. Data signals are not affected by the ESD circuitry, other than by the added capacitive load. Since ESD events are characterized by very short pulses of charge injection most of the energy in the pulse is at very high frequencies and will be filtered by the ESD circuitry.

We can tolerate a significant amount of additional capacitance from the ESD structures on all of the programming pins, the bias pins and the supply pins. Therefore, the ESD for the control pins, bias pins and the supply pins was designed for 1kV of protection. The total gate widths for these structures is $100\mu m$ and R_g was set to 750Ω based on Hspice simulations and R_{small} is just 20Ω. The total capacitive load due to the ESD and bond pad was extracted using StarRC is 198fF. Specialized, low capacitance ESD structures are required on both the RF input pads and the RF output pads. The ESD for the RF I/O pads was designed for 200V of protection. The total gate widths for these structures is $40\mu m$, R_g is 750Ω and R_{small} is 20Ω. The bond pads measure $75\mu m \times 75\mu m$ and are constructed of metal layers 3, 4 and 5. The total capacitive load due to ESD and the bond pad on the RF I/O's was also extracted using StarRC and is just 185fF. The final pad and ESD layouts for the two levels of protection are shown in Figure B-2.

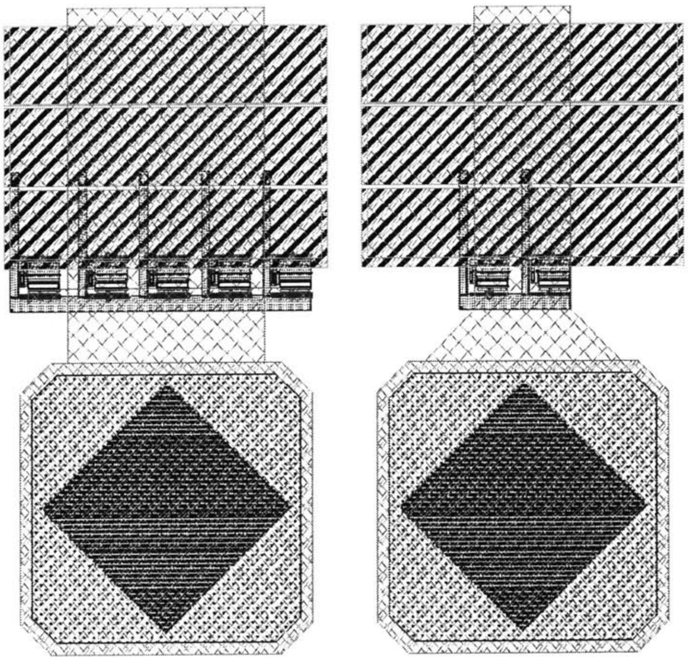


Figure B-2: Layouts for the two pads with ESD structures

Appendix C

CppSim Code

C.1 Limit Amplifier Code

The CppSim code to implement the limit amplifier is shown below. The transfer function for the amplifier is separated into several stages. The two amplifier class definitions, *amp1* and *amp2*, are used to implement the non-linear transfer function and limiting action. To model the amplifier stages without the neutralization capacitors, *filt1* and *filt2* are used to model the bandwidth of the amplifier stages. Alternately, *filt3-filt6* are used to model the amplifier frequency characteristics with the neutralization capacitors. The two differential paths of each stage of the limit amplifier are implemented as a cascade of each of these classes.

```
module: amp1
parameters: double off double gain double min double max
inputs: double a double b
outputs: double y double z
classes:
 Amp amp1("off/2+gain*a+A1*a^2+A2*a^3","off,gain,min,max,A1,A2",off,
          gain,min,max,0.6,-3.3);
 Amp amp2("-off/2+gain*b+B1*b^2+B2*b^3","off,gain,min,max,B1,B2",off,
          gain,min,max,0.6,-3.3);
 Filter filt1("1","1 + 1/(2*pi*fp)*s","fp,Ts,Min,Max",10e9,Ts,min,max);
 Filter filt2("1","1 + 1/(2*pi*fp)*s","fp,Ts,Min,Max",10e9,Ts,min,max);
 Filter filt3("1 + 1/(2*pi*fz)*s","1","fz,Ts",100e9,Ts);
 Filter filt4("1 + 1/(2*pi*fz)*s","1","fz,Ts",100e9,Ts);
 Filter filt5("1","1 + 1/(2*pi*fp)*s + 1/(fp*fz*(2*pi)^2)*s^2","fp,fz,
              Ts,Min,Max",10e9,60e9,Ts,min,max);
 Filter filt6("1","1 + 1/(2*pi*fp)*s + 1/(fp*fz*(2*pi)^2)*s^2","fp,fz,
              Ts,Min,Max",10e9,60e9,Ts,min,max);
static_variables:
init:
code:
 amp1.inp(a);
 amp2.inp(b);
 filt3.inp(amp1.out);
 filt4.inp(amp2.out);
 filt5.inp(filt3.out);
 filt6.inp(filt4.out);
 y = filt5.out;
 z = filt6.out;
```

C.2 Peak Detector Code

The CppSim code used to implement the peak detector is shown below. Initially, the code modeled the peak detector as a low pass filter when the input was high and as a constant droop when the input was low. However, the final code models the peak detector as a simple low-pass filter with unity gain. The entire peak detector operation is performed by the *filt1* and *filt2* class definitions.

```
module: peakdetect
parameters: double fp
inputs: double in double inb
outputs: double out double outb
static_variables:
classes:
Filter filt1("K","1 + 1/(2*pi*fp)*s","K,fp,Ts",1,fp,Ts);
Filter filt2("K","1 + 1/(2*pi*fp)*s","K,fp,Ts",1,fp,Ts);
init:
 out = 0.0;
 outb = 0.0;
code:
 filt1.inp(in);
 out = filt1.out;
 filt2.inp(inb);
 outb = filt2.out;
```

C.3 Integrator Code

Similar to the CppSim code for the peak detector, the integrator CppSim code is omitted because it merely implements a low-pass filter with a gain term and closely resembles the peak detector code.

Appendix D

Optimal Gain/Stage for Maximum Bandwidth

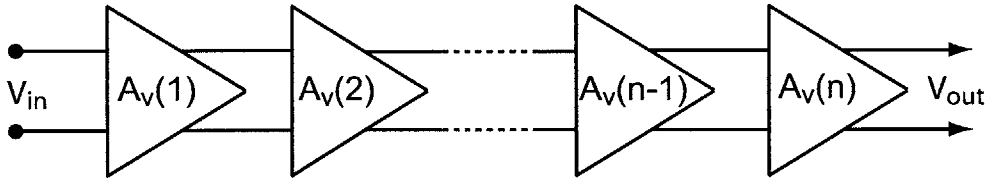


Figure D-1: High-Speed, Multi-Stage Limit Amplifier

D.0.1 Determining Optimal Number of Stages

Following the derivation in Chapter 8 of [20], we can determine the optimal gain per stage, or conversely, the optimal number of stages, of the limit amplifier to maximize bandwidth for a given total amplifier gain. As before, if we model each stage of the limit amplifier by a gain and a single pole, the model for the limit amplifier is:

$$\frac{V_{out}}{V_{in}} = \left(\frac{A}{1 + w_1/w_o}\right)^n \tag{D.1}$$

where A is the gain/stage, w_1 is the overall bandwidth of the limit amplifier, w_o is the bandwidth of each stage and n is the number of stages. The overall 3dB bandwidth of the amplifier is:

$$\begin{aligned} \left|\frac{V_{out}}{V_{in}}\right| &= \left|\frac{A}{1 + s/p_o}\right|^n = \frac{A^n}{\sqrt{2}} && \text{(D.2)} \\ &= \left(\frac{A}{\sqrt{1 + (w_1/w_o)^2}}\right)^n = \frac{A^n}{\sqrt{2}} && \text{(D.3)} \end{aligned}$$

If we solve for w_1 we can see that as the number of stages, n, increases the bandwidth decreases much slower than the gain increases:

$$(1 + (w_1/w_o)^2)^n = 2 \tag{D.4}$$

$$w_1 = w_o\sqrt{2^{1/n} - 1} \tag{D.5}$$

This means that we can increase the gain-bandwidth product as the number of stages increases, to a limit. To determine what this limit is, let's assume that to first order each individual stage has a constant gain-bandwidth product of:

$$Aw_o = w_t \Rightarrow w_o = \frac{w_t}{A} \tag{D.6}$$

Substituting Equation D.6 into Equation D.5 yields the following result:

$$w_1 = \frac{w_t}{A}\sqrt{2^{1/n} - 1} \tag{D.7}$$

If we want to achieve a total gain G with n stages, where $A = G^{1/n}$, then Equation D.7 becomes:

$$w_1 = \frac{w_t}{G^{1/n}}\sqrt{2^{1/n} - 1} \tag{D.8}$$

To determine the optimal gain per stage, recognize that:

$$2^{1/n} = exp\left(\frac{1}{n}ln2\right) \tag{D.9}$$

which, for large n, can be rewritten as:

$$exp\left(\frac{1}{n}ln2\right) = 1 + \frac{1}{n}ln2 \tag{D.10}$$

Substituting Equation D.10 into Equation D.8 and simplifying terms yields:

$$w_1 = \frac{w_t}{G^{1/n}}\sqrt{\frac{1}{n}ln2} \tag{D.11}$$

$$\approx \frac{w_t}{G^{1/n}} \frac{\sqrt{ln2}}{\sqrt{n}} \tag{D.12}$$

$$\frac{1}{w_1} = \frac{G^{1/n}}{w_t} \frac{\sqrt{n}}{\sqrt{ln2}} \tag{D.13}$$

$$= \sqrt{n} \cdot G^{1/n} \left(\frac{1}{w_t \sqrt{ln2}} \right) \tag{D.14}$$

Finally, determine the number of stages, n, to achieve the maximum total bandwidth for a total gain by taking the derivative of Equation D.14, and setting the result equal to zero to find the minimum.

$$\frac{d}{dn} = (\sqrt{n} G^{1/n}) = 0 \tag{D.15}$$

$$ln(G^{1/n}) = \frac{1}{2} \Rightarrow G^{1/n} = e^{1/2} \tag{D.16}$$

Therefore, the optimal gain per stage, for maximum bandwidth, is approximately 1.65.

Appendix E

Matlab Amplifier Script

Following are two Matlab scripts based on the design methodology presented in Chapter 4. The first version of the script accepts output voltage swing (Vsw), gain (Av), desired bandwidth (BW), scaling ratio of loading stage to driving stage (scale) and process and temperature corner (corner) as input arguments and returns device width (W), resistance (R) and bias current (I) for the design. The second version of the script accepts output voltage swing, gain, desired power dissipation, scaling ratio of loading stage to driving stage and process and temperature corner as input arguments and returns device width (W), resistance (R) and 3dB bandwidth (F) for the resulting design.

E.1 Script for Fixed Bandwidth

This is the Matlab script for calculating transistor width, load resistance and amplifier bias current for a given output voltage swing, gain and bandwidth.

```
% Script for generating device size and biasing for resistively
% loaded differential pair with National Semiconductor CMOS9
% 0.18um process.  Inputs are  output voltage swing (Vsw), DC
% gain (Av), power (Ibias), scaling factor (Scale) which represents
% the ratio of widths for the loading stage and the stage under test,
% model corner and the simulation characterization file name (file).
% Script returns the input pair width (assuming l=0.18um), bias current,
% load resistance (RlE), bandwidth (FbwoE) and calculated gain (AvoeE).
%
% Format for specifying corner:  <model corner><temp>
%       choices: s-40, s25, s85, t-40, t25, t85, f-40, f25, f85
%
% [WnE,RlE,IbiasE]=diffampnscsBW(Vsw,Av,BW,Scale,corner)
% Alternatively...
% [WnE,RlE,IbiasE,FbwoE,VswoE,AvoE]=diffampnscBW(Vsw,Av,BW,Scale,corner)
```

```
function [WnE,RlE,IbiasE,FbwoE,VswoE,AvoE]=diffampnscBW(Vsw,Av,BW,
         Scale,corner)

% Process constants: NSC CMOS9 0.18um
% format is [t s f]

switch corner
    case 't-40'
        c = 1;
        file1 = 'spicefiles/test.sw4';
        file2 = 'spicefiles/test.ac4';
    case 't25'
        c = 1;
        file1 = 'spicefiles/test.sw5';
        file2 = 'spicefiles/test.ac5';
    case 't85'
        c = 1;
        file1 = 'spicefiles/test.sw6';
        file2 = 'spicefiles/test.ac6';
    case 's-40'
        c = 2;
        file1 = 'spicefiles/test.sw1';
        file2 = 'spicefiles/test.ac1';
    case 's25'
        c = 2;
        file1 = 'spicefiles/test.sw2';
        file2 = 'spicefiles/test.ac2';
    case 's85'
        c = 2;
        file1 = 'spicefiles/test.sw3';
        file2 = 'spicefiles/test.ac3';
    case 'f-40'
        c = 3;
        file1 = 'spicefiles/test.sw7';
        file2 = 'spicefiles/test.ac7';
    case 'f25'
        c = 3;
        file1 = 'spicefiles/test.sw8';
        file2 = 'spicefiles/test.ac8';
    case 'f85'
        c = 3;
        file1 = 'spicefiles/test.sw9';
        file2 = 'spicefiles/test.ac9';
end;
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Design variables - NEED TO UPDATE PROCESS & CIRCUIT PARAMETERS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%rrrrr%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Hdin = 0.56e-6;              % minimum s/d extension w/ sharing (m)
Hdout = 0.52e-6;             % minimum s/d extension w/out sharing (m)
Rsh = 185;                   % sheet rho of pp-poly resistor (ohms/sq)
Lmin = 0.40e-6;              % use minimum L devices (m)
CRp = 0.5*98.6e-6;           % 1/2 of capacitance of np-poly (F/um^2)
Idenmax = 0.5e3;             % maximum current den for poly res (A/m)
MinSq = 5;                   % Minimum # of squares for poly res
Cfix = 15e-15;               % Assume fixed wiring cap. (F)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Empirical solution for device width - need to call Hspice
% and extract typical gm/W value for the given Av and Vsw
% Alternately, load characterization file

%hspsim                                 % file is test.par
x = loadsig(file1);                     % load Hspice dc data
gmSIM = 1.1*evalsig(x,'lx7_m0');        % simulated gm
gdsSIM = evalsig(x,'lx8_m0');           % simulated gds
IdSIM = evalsig(x,'i_m0');              % simulated Id
wSIM = 2*evalsig(x,'w');                % width from char
y = loadsig(file2);                     % load Hspice ac data
cgSIM = 2/1.1*evalsig(y,'lx18_m0');     % cg for load device
cgdSIM = -2/1.1*evalsig(y,'lx19_m0');   % cgd for load device
cgsSIM = -2/1.1*evalsig(y,'lx20_m0');   % cgs for load device
cgbSIM = -2/1.1*evalsig(y,'lx21_m0');   % cgb for load device
cdbSIM = -2/1.1*evalsig(y,'lx22_m0');   % cdb for driving device

% Determine the appropriate current density and
% transconductance density from characterization
% data based on desired gain and voltage swing.

k = length(wSIM);
while (gmSIM(k)/wSIM(k))>
      (2*Av/Vsw*(IdSIM(k)/wSIM(k))+Av*gdsSIM(k)/wSIM(k))
   k=k-1;
end;

gmDen = gmSIM(k+1)/wSIM(k+1);           % empirical gm/w
gdsDen = gdsSIM(k+1)/wSIM(k+1);         % empirical gds/w
iDen = IdSIM(k+1)/wSIM(k+1);            % empirical ibias/w
cgDen = cgSIM(k+1)/wSIM(k+1);           % empirical cg/w
cgdDen = cgdSIM(k+1)/wSIM(k+1);         % empirical cgd/w
```

```
cgsDen = cgsSIM(k+1)/wSIM(k+1);        % empirical cgs/w
cgbDen = cgbSIM(k+1)/wSIM(k+1);        % empirical cgb/w
cdbDen = cdbSIM(k+1)/wSIM(k+1);        % empirical cds/w

% Determine the circuit parameters based on the process
% characterization data, design specifications and the script

% These equations are for inputs - Vsw, Av, Ibias
WnE = 0.28e-6;
IbiasE = 2*iDen*WnE;
RlE = Vsw/IbiasE;
AvoE = gmDen*WnE*RlE/(1+gdsDen*WnE*RlE);
VswoE = IbiasE*RlE;
%% To ignore Miller effect use this calculation for load device
%% capacitance for some strange reason NSC models have Cg = Cgs+Cgb
%% (no Cgd)
%Cvar = WnE*(cdbDen+Scale*(cgsDen+cgbDen+cgdDen));
%% To account for Miller effect, use this calculation
Cvar = WnE*(cdbDen+Scale*(cgsDen+cgbDen+(1+AvoE)*cgdDen));

% Need to guarantee that Nsq >= MinSq

% This code calculates resistor size based on satisfying
% minimum number of squares (Nsq) and current density
% requirements based on design rule recommendations for
% device matching.

% Nsq = VswoE/(IbiasE*Rsh);
% Width = 2e-6;
% if ((Nsq >= MinSq)&&(IbiasE/Width <= Idenmax))
%     Length = Width*Nsq;
% else if ((Nsq >= MinSq)&&(IbiasE/Width > Idenmax))
%         Width = IbiasE/Idenmax;
%         Length = Nsq*Width;
%     else if ((Nsq < MinSq)&&(IbiasE/Width <= Idenmax))
%                Width = ceil(MinSq/Nsq)*2e-6;
%                Length = Nsq*Width*ceil(MinSq/Nsq);
%         else if ((Nsq < MinSq)&&(IbiasE/Width > Idenmax))
%                 Width = max(ceil(MinSq/Nsq)*2e-6, IbiasE/Idenmax);
%                 Length = Nsq*Width*ceil(MinSq/Nsq);
%             end
%         end
%     end
% end
% This code calculates resistor size based on satisfying
% current density rules only and optimizes the size for
% speed.  The total area is kept larger than 10um^2.

Nsq = VswoE/(IbiasE*Rsh);
Width = max(2e-6,IbiasE/Idenmax);
Length = Nsq*Width;
if (Width*Length < 10e-12)
    ratio = sqrt(10e-12/Width/Length);
    Width = Width*ratio;
    Length = Length*ratio;
end

FbwoE = (2*pi*RlE/(1+gdsDen*WnE*RlE)*(Cfix+Cvar+CRp*Length*Width))^-1;

if (FbwoE<BW)
   while (FbwoE<BW)
      WnE = WnE+0.01e-6;
      IbiasE = 2*iDen*WnE;
      RlE = Vsw/IbiasE;
      AvoE = gmDen*WnE*RlE/(1+gdsDen*WnE*RlE);
      VswoE = IbiasE*RlE;
      %% To ignore Miller effect use this calculation for load
      %%device capacitance
      %% for some strange reason NSC models have Cg = Cgs+Cgb (no Cgd)
      %Cvar = WnE*(cdbDen+Scale*(cgsDen+cgbDen+cgdDen));
      %% To account for Miller effect, use this calculation
      Cvar = WnE*(cdbDen+Scale*(cgsDen+cgbDen+(1+AvoE)*cgdDen));
      Nsq = VswoE/(IbiasE*Rsh);
      Width = max(2e-6,IbiasE/Idenmax);
      Length = Nsq*Width;
      if (Width*Length < 10e-12)
          ratio = sqrt(10e-12/Width/Length);
          Width = Width*ratio;
          Length = Length*ratio;
      end
      FbwoE = (2*pi*RlE/(1+gdsDen*WnE*RlE)*
              (Cfix+Cvar+CRp*Length*Width))^-1;
      if WnE>700e-6
         FbwoE = 1e20;
         WnE = 0.01e-6;
      end;
    end;
    WnE = WnE-0.01e-6;
else
```

```
  FbwoE = 1e20;
  WnE = 0.01e-6;
end;
```

E.2 Script for Fixed Power Dissipation

This is the Matlab script for calculating transistor width, load resistance and amplifier bias current for a given output voltage swing, gain and power dissipation.

```
% Script for generating device size and biasing for resistively
% loaded differential pair with National Semiconductor CMOS9
% 0.18um process.  Inputs are  output voltage swing (Vsw), DC
% gain (Av), power (Ibias), scaling factor (Scale) which represents
% the ratio of widths for the loading stage and the stage under test,
% model corner and the simulation characterization file name (file).
% Script returns the input pair width (assuming l=0.18um), bias current,
% load resistance (RlE), bandwidth (FbwoE) and calculated gain (AvoeE).
%
% Format for specifying corner:  <model corner><temp>
%       choices: s-40, s25, s85, t-40, t25, t85, f-40, f25, f85
%
% [WnE,RlE,FbwoE,IbiasE]=diffampnscPWR(Vsw,Av,Ibias,Scale,corner)
% Alternatively...
% [WnE,RlE,FbwoE,IbiasE,VswoE,AvoE]=
%                          diffampnscPWR(Vsw,Av,Ibias,Scale,corner)

function [WnE,RlE,FbwoE,IbiasE,VswoE,AvoE]=
         diffampnscPWR(Vsw,Av,Ibias,Scale,corner)

% Process constants: NSC CMOS9 0.18um
% format is [t s f]

switch corner
    case 't-40'
        c = 1;
        file1 = 'spicefiles/test.sw4';
        file2 = 'spicefiles/test.ac4';
    case 't25'
        c = 1;
        file1 = 'spicefiles/test.sw5';
        file2 = 'spicefiles/test.ac5';
    case 't85'
```

```
        c = 1;
        file1 = 'spicefiles/test.sw6';
        file2 = 'spicefiles/test.ac6';
    case 's-40'
        c = 2;
        file1 = 'spicefiles/test.sw1';
        file2 = 'spicefiles/test.ac1';
    case 's25'
        c = 2;
        file1 = 'spicefiles/test.sw2';
        file2 = 'spicefiles/test.ac2';
    case 's85'
        c = 2;
        file1 = 'spicefiles/test.sw3';
        file2 = 'spicefiles/test.ac3';
    case 'f-40'
        c = 3;
        file1 = 'spicefiles/test.sw7';
        file2 = 'spicefiles/test.ac7';
    case 'f25'
        c = 3;
        file1 = 'spicefiles/test.sw8';
        file2 = 'spicefiles/test.ac8';
    case 'f85'
        c = 3;
        file1 = 'spicefiles/test.sw9';
        file2 = 'spicefiles/test.ac9';
end;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Design variables - NEED TO UPDATE PROCESS & CIRCUIT PARAMETERS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%rrrrr%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Hdin = 0.56e-6;               % minimum s/d extension w/ sharing (m)
Hdout = 0.48e-6;              % minimum s/d extension w/out sharing (m)
Rsh = 185;                    % sheet rho of pp-poly resistor (ohms/sq)
Lmin = 0.40e-6;               % use minimum L devices (m)
CRp = 0.5*98.6e-6;            % 1/2 of capacitance of np-poly (F/um^2)
Idenmax = 0.5e3;              % maximum current den for poly res (A/m)
MinSq = 5;                    % Minimum # of squares for poly res
Cfix = 15e-15;                % Assume fixed wiring cap. (F)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Empirical solution for device width - need to call Hspice
% and extract typical gm/W value for the given Av and Vsw
% Alternately, load characterization file
```

```
%hspsim                                        % file is test.par
x = loadsig(file1);                            % load Hspice dc data
gmSIM = 1.1*evalsig(x,'lx7_m0');               % simulated gm
gdsSIM = evalsig(x,'lx8_m0');                  % simulated gds
IdSIM = evalsig(x,'i_m0');                     % simulated Id
wSIM = 2*evalsig(x,'w');                       % width from char
y = loadsig(file2);                            % load Hspice ac data
cgSIM = 2/1.1*evalsig(y,'lx18_m0');            % cg for load device
cgdSIM = -2/1.1*evalsig(y,'lx19_m0');          % cgd for load device
cgsSIM = -2/1.1*evalsig(y,'lx20_m0');          % cgs for load device
cgbSIM = -2/1.1*evalsig(y,'lx21_m0');          % cgb for load device
cdbSIM = -2/1.1*evalsig(y,'lx22_m0');          % cdb for driving device

% Determine the appropriate current density and
% transconductance density from characterization
% data based on desired gain and voltage swing.

k = length(wSIM);
while (gmSIM(k)/wSIM(k))>
      (2*Av/Vsw*(IdSIM(k)/wSIM(k))+Av*gdsSIM(k)/wSIM(k))
   k=k-1;
end;

gmDen = gmSIM(k+1)/wSIM(k+1);                  % empirical gm/w
gdsDen = gdsSIM(k+1)/wSIM(k+1);                % empirical gds/w
iDen = IdSIM(k+1)/wSIM(k+1);                   % empirical ibias/w
cgDen = cgSIM(k+1)/wSIM(k+1);                  % empirical cg/w
cgdDen = cgdSIM(k+1)/wSIM(k+1);                % empirical cgd/w
cgsDen = cgsSIM(k+1)/wSIM(k+1);                % empirical cgs/w
cgbDen = cgbSIM(k+1)/wSIM(k+1);                % empirical cgb/w
cdbDen = cdbSIM(k+1)/wSIM(k+1);                % empirical cds/w

% Determine the circuit parameters based on the process
% characterization data, design specifications and the script

% These equations are for inputs - Vsw, Av, Ibias
IbiasE = Ibias;
RlE = Vsw/IbiasE;
VswoE = IbiasE*RlE;
WnE = 0.5*IbiasE/iDen;
AvoE = gmDen*WnE*RlE/(1+gdsDen*WnE*RlE);
%% To ignore Miller effect use this calculation for load device
%% capacitance
%% for some strange reason NSC models have Cg = Cgs+Cgb (no Cgd)
```

```
%Cvar = WnE*(cdbDen+Scale*(cgsDen+cgbDen+cgdDen));
%% To account for Miller effect, use this calculation
Cvar = WnE*(cdbDen+Scale*(cgsDen+cgbDen+(1+AvoE)*cgdDen));

% Need to guarantee that Nsq >= MinSq

% This code calculates resistor size based on satisfying
% minimum number of squares (Nsq) and current density
% requirements based on design rule recommendations for
% device matching.

% Nsq = VswoE/(IbiasE*Rsh);
% Width = 2e-6;
% if ((Nsq >= MinSq)&&(IbiasE/Width <= Idenmax))
%     Length = Width*Nsq;
% else if ((Nsq >= MinSq)&&(IbiasE/Width > Idenmax))
%         Width = IbiasE/Idenmax;
%         Length = Nsq*Width;
%     else if ((Nsq < MinSq)&&(IbiasE/Width <= Idenmax))
%                Width = ceil(MinSq/Nsq)*2e-6;
%                Length = Nsq*Width*ceil(MinSq/Nsq);
%         else if ((Nsq < MinSq)&&(IbiasE/Width > Idenmax))
%                 Width = max(ceil(MinSq/Nsq)*2e-6, IbiasE/Idenmax);
%                 Length = Nsq*Width*ceil(MinSq/Nsq);
%             end
%         end
%     end
% end

% This code calculates resistor size based on satisfying
% current density rules only and optimizes the size for
% speed.  The total area is kept larger than 10um^2.

Nsq = VswoE/(IbiasE*Rsh);
Width = max(2e-6,IbiasE/Idenmax);
Length = Nsq*Width;
if (Width*Length < 10e-12)
    ratio = sqrt(10e-12/Width/Length);
    Width = Width*ratio;
    Length = Length*ratio;
end

FbwoE = (2*pi*RlE/(1+gdsDen*WnE*RlE)*
        (Cfix+Cvar+CRp*Length*Width))^-1;
```

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5823-3