Characterization of Schottky Barrier Carbon Nanotube Transistors and their Applications to Digital Circuit Design

by

Julia Van Meter Cline

B.Sc., Brown University (2002)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

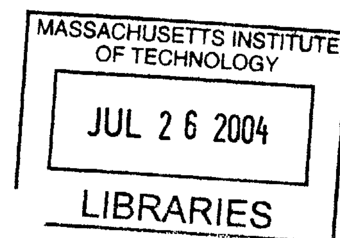
Masters of Science in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2004

© Massachusetts Institute of Technology 2004



Signature of Author ....
Department of Electrical Engineering and Computer Science
May 24, 2004

Certified by ....
Anantha Chandrakasan
Professor, EECS
Thesis Supervisor

Certified by ....
Dimitri Antoniadis
Professor, EECS
Thesis Supervisor

Accepted by ....
Arthur C. Smith
Chairman, EECS Department Committee on Graduate Students

BARKER

Characterization of Schottky Barrier Carbon Nanotube Transistors and their Applications to Digital Circuit Design

by

Julia Van Meter Cline

Submitted to the Department of Electrical Engineering and Computer Science
on May 21, 2004, in partial fulfillment of the
requirements for the degree of
Masters of Science in Electrical Engineering and Computer Science

Abstract

The difficulty in shrinking silicon transistors past a certain feature size has been acknowledged for years. Carbon nanotubes (CNTs) offer a technology with an exciting solution to the scaling issues of transistors and interconnects and with the possibility of coexistence in the present silicon technology. The goal of the present work is to propose circuit models for carbon nanotube field effect transistors (CNTFETs) and apply them to aspects of digital circuit design.

This research models the current voltage characteristics of CNTFETs below and above threshold. The current characteristics are similar to MOSFETs, but with a few caveats. Under standard conditions, the devices do not enter saturation. Also, it is shown that CNTFETs are ambipolar devices, with a minimum current at $V_{ds}/2$. Despite this distinction from MOSFETs, CNTFETs show impressive voltage transfer characteristics (VTC), even at low voltages. The large noise margin and notable output voltage swing can be traded-off for higher on-current, depending on the nanotube diameter, as shown in this work. Thus, digital designers have an ability to control both performance and power by changing the nanotube diameters.

Carbon nanotubes FETs can become prominent in the arena of array devices, which are a technical front runner for the integration of wires and transistors. This work shows that carbon nanotube field effect transistors have strong potential in read only memory (ROM) arrays. Many CNTFETs can be placed along the length of a nanotube to create intermolecular devices and small array applications. The present process variations within carbon nanotubes lead to possible metallic CNTs and added redundancy. The necessary redundancy is illustrated in detail in this thesis along with the corresponding trade-offs for redundancy, area, and performance.

In conclusion, the striking properties of carbon nanotubes give CNTFET noteworthy IV characteristics and offer many opportunities for digital circuit designers in the near future. This thesis research models and characterizes the future opportunities of CNTFETs within digital designs.

Thesis Supervisor: Anantha Chandrakasan
Title: Professor, EECS

Thesis Supervisor: Dimitri Antoniadis
Title: Professor, EECS

Acknowledgements

I would like to thank Anantha Chandrakasan for giving me the opportunity to work on this project and in his group for two years; his advice, comments, support, and contacts have been invaluable. These past two years have been a struggle for me at times; however, I have learned an enormous amount.

Without a background, this field was difficult to enter and hard to find a focused project; Professor Antoniadis's discussions and advice on the topic were very helpful. Also, his comments on my thesis were especially enlightening.

I would like to thank Joerg Appenzeller and Phillip Wong at IBM. My phone call discussions with Joerg were incredibly helpful. It was wonderful to have the perspective and knowledge of someone working first hand within the nanotube field.

The Semiconducting Research Corporation (SRC) gave me the opportunity to research this interesting future topic. My SRC Master's Fellowship opened up many possibilities for me. And, I would also like to thank the SRC for introducing me to an amazing community.

I would not have been at this place in my career without the help and support from the following people. Kerry Bernstein at IBM gave me an endless amount of thought provoking comments, contacts, and confidence. Also, Professor Friedman, at the University of Rochester, gave me the opportunity to start exploring the field of digital circuit design and Professor Beresford gave me continual support and advice throughout my Brown University career.

Thank you to Johnna Powell for being my proofreader, outlet, and friend. And, I would also like to thank Anantha-group past and present. Alex, Frank, Ben, Alice, Nathan, Rex, Puneet, Dave, Brian, Naveen, Fred, Raul, Daniel, Payam, and Denis gave me help, comments, questions, and friendships. It was a pleasure working in the same lab with them.

I would also like to thank Kate Martin. As I figure out my career path, I hope to make both of our paths cross again soon; I do not know how I will manage without her. I'm leaving my exercise partner, my every-night-date, my study partner, and most importantly my best friend. I would have never made it through without her. I would also like to thank Steve Kelly for giving me his love, support, confidence, jokes, and stories. I look forward to our time together. Thank you also to Betsy More. It is unbelievable how our lives are so opposite, but take us to the same places. I hope that continues.

Thank you to April, Taylor, Nancy, Kathy, Chrissy, Alison, and Angela for their friendship on and off the field. Also, it was a true honor to play with sMITe through any condition and any opponent.

I would like to thank Jackie; it is because of our endless discussions that I have found my own path through MIT and into the future.

And last but not at all least, I would like to thank my family. My dad and mom have gotten me through everything, good and bad. I do not know how to thank them enough. It seems the more I grow up, the more help and advice I ask for. No distance will ever be great enough to keep me from calling home everyday and sometimes even a few times a day. Once a parent, always a parent! Thank you also to my brother Geoffrey, who has shown me how to follow what I really want and keep me calm through any storm.

Contents

1 Carbon Nanotubes Structure, Properties, and Growth **15**

1.1 Background 15

1.2 Structure of Carbon Nanotubes 16

1.2.1 Chirality 16

1.2.2 Single Walled versus Multi Walled Carbon Nanotubes 17

1.3 Growth Processes 19

1.3.1 Arc-Discharge 20

1.3.2 Chemical Vapor Deposition 20

1.3.3 Laser Ablation 20

1.3.4 Growth Processes Variation 23

1.4 Electron Mobility Characteristics in Carbon Nanotubes 23

1.5 Conclusion 24

2 Carbon Nanotubes as Transistors **25**

2.1 Schottky Barrier Field Effect Transistors: Fabrication 25

2.2 Schottky Barrier Field Effect Transistors: Operation 27

2.3 Carbon Nanotube Transistor Width 32

2.4 P-Channel versus N-Channel Schottky barrier CNTFETs 33

2.4.1 Annealing 34

2.4.2 Doping with Alkali Metals 34

2.4.3 Conclusion 36

2.5 CNTFET Scaling 36

2.6 Conclusion . . . 38

3 Subthreshold Carbon Nanotube Field Effect Transistors **39**

3.1 Subthreshold CNTFET Current . . . 40

3.1.1 Current versus $V_{Gate-Source}$ Characteristics . . . 41

3.2 Matlab Model . . . 44

3.2.1 I_{drain} versus $V_{gate-source}$ Model . . . 44

3.2.2 Current versus $V_{Drain-Source}$ Model . . . 49

3.3 Inverter . . . 51

3.3.1 Voltage Transfer Characteristics of an Inverter . . . 51

3.4 Process Variations . . . 59

3.4.1 Varying Nanotube Diameter . . . 59

3.4.2 Changing Drain Control versus Gate Control (h_n) . . . 61

4 Capacitance, Energy, and Delay of Subthreshold CNTFETs **64**

4.0.3 Capacitance . . . 64

4.0.4 Delay . . . 75

4.0.5 Conclusion . . . 76

5 Above Threshold Model **78**

5.0.6 Linear Regime . . . 78

5.0.7 Saturation Point . . . 81

5.0.8 Saturation Regime . . . 83

5.0.9 MOSFETs compared to CNTFETs . . . 84

5.0.10 Process Variations . . . 85

6 ROM Research **87**

6.1 Schottky Barrier ROM Array Structures . . . 88

6.1.1 NOR ROMs . . . 88

6.1.2 Programing ROM Arrays . . . 88

6.1.3 ROM Redundancy . . . 93

6.1.4 ROM Area . . . 95

6.1.5 ROM Capacitance 98
6.1.6 ROM Resistance 100
6.1.7 Conclusion 100

7 Conclusions **103**

A Appendix **110**

A.1 Matlab Code for I_d versus V_{gs} and V_{ds} including Voltage Transfer Characteristics 110
A.2 Matlab Code for ROM Capacitance Model 117

List of Figures

1-1 Carbon nanotube cylinders with varying chiralities. (From [1]) 16

1-2 A multi walled carbon nanotube. (From [2]) 18

1-3 Multi walled carbon nanotubes are shown at the top and single walled carbon nanotubes are bundled in the second picture. (From [3]) 19

1-4 A diagram illustrating SWCNT growth by chemical vapor deposition. (From [4]) 21

1-5 Picture of CVD growth from [4]. The bottom bar is a scale of 10 nm in length. . 22

2-1 Diagram of a top gated CNT transistor structure. 26

2-2 Illustration of band diagrams for a Schottky barrier CNT transistor in the 'off' and 'on' states, respectively. (From [5].) 28

2-3 Subthreshold band diagrams for Schottky barrier transistors related to the I_d versus V_{gs} graph. 28

2-4 I_d versus V_{gs} subthreshold characteristics for a p-type transitor, with a channel length of 300nm and a gate oxide thickness (t_{ox}), HfO_2, of 20nm. The subthreshold characteristics do not vary largely with V_{ds} and the subthreshold slope, S, remains relatively constant with temperature. (From [5]) 29

2-5 Conductance changes as the work function of the drain and source metals are varied to the band gap of the semiconducting CNT. Also, these graphs note how current increases if an opposite gate voltage is applied. (From [6]) 30

2-6 Band diagrams for a Schottky barrier transistor in the triode regime and at the saturation point. 31

2-7 This figure follows the drain voltages shown in Figure 2-6. Drain-1 & 2: Linear Regime, Drain-3: Saturation point 31

2-8 Energy band bending of a CNTFET is larger with a thinner gate oxide. (From [7]) 32

2-9 CNTFET IV characteristics, depending on oxidation of the CNT to metal interface. (From [7]) 35

2-10 Shifting of I_d versus V_{gs} curves, with a varying amounts of potassium. (From [6]) 36

2-11 Conversion between P and N type CNTFETs, using an annealing process in vacuum. (From [8]) 37

3-1 Picture A represents the band modulation of a transistor with the least current; the V_{ds} voltage is split evenly between the source to channel and drain to channel and thus the Schottky barriers are thickest and the current is at a minimum. In picture B, the band diagrams illustrate a transistor that is 'on', with a larger negative gate voltage. The hole tunneling current from the source is orders of magnitude larger than the electron tunneling current from the drain. In both A and B, the arrows represent the hole and electron tunneling currents. The relative size of these arrows represents the relative size of the tunneling currents. 42

3-2 Subthreshold IV characteristics. Graph A: CNT Diameter (D_t) =1.3nm. Graph B: D_t=2.5nm. Both FET devices have a mid-band gap line up and an oxide thickness of 2nm (t_{oxide}=2nm) and titanium source, drain and gate contacts. Data obtained from Joerg Appenzeller at IBM. 43

3-3 Matlab model's I_d versus V_{gs} graphs for diameters of 1.3nm and 2.5nm. Details illustrate the threshold votlages and the δV_{sub} values. 46

3-4 Matlab model of I_d versus V_{gs} on a linear-linear plot. The threshold voltage of the larger diameter tubes is visible in the bottom graph. V_{dd}=0.4V 47

3-5 Matlab model's absolute value of I_d versus V_{ds} graph for a p-channel transistor with a CNT diameter of 1.9nm. The current is equal to an identically sized n-channel transistor with a negated V_{ds} value. 48

3-6 The subthreshold model (bold lines) overlayed over the original data. 49

3-7 Illustration from Matlab model of I_d versus V_{gs} graphs with changing drain control (h_n) values. CNT diameter is 1.9nm. 50

3-8 Current versus drain to source voltage for a CNTFET with a CNT diameter of 1.3nm and a changing drain control versus gate control level, h_n. Low h_n in the top graph, gives little slope to the high V_{gs} lines. With a higher h_n in the second graph, the lines have a much larger slope. 52
3-9 I_d versus V_{ds} characteristics for a 2.5nm diameter CNT, in a Matlab modeled CNTFET. The h_n level changes from the top to the bottom graphs: original, $h_n = 14.6$, to high, $h_n = 20.0$, levels respectively. 53
3-10 Inverter structure composed of both an NFET and a PFET transistor. 54
3-11 The voltage transfer characteristics for various diameter CNT transistors. (D_t= 1.3nm, 1.9nm, and 2.5nm) The shaded area represents less than 10%V_{dd} and more than 90% V_{dd}. 54
3-12 High and low limits for the output votlage swing of an inverter versus the CNT diameter, for Vdd=0.4V. 56
3-13 Model VTC curves at varying supply voltage levels V_{dd}=[0.6V, 0.4V, 0.2V] As the supply voltage is lowered, CNTFETs continue to keep similar and large voltage swing for various diameter tubes. The dotten circles illustrate the output voltage swing away from the V_{dd} and ground rails with large diameter nanotubes. 57
3-14 The band diagrams in A represent the maximum output voltage state. The NFET current is at a minimum and, therefore, the output voltage is at a maximum. B represents the output voltage when V_{in}=0V; thus, V_{out} is high, but less than V_{out} for case A. 58
3-15 V_{out} versus V_{in}, for an inverter structure, can be concluded using the load lines (I_d versus V_{out} curves). Here, V_{out} is found for V_{in}=0V and V_{in}=0.1V. 59
3-16 When the CNT diameter changes between the two transistors in an inverter, the inverter will not function properly. Here, the VTC curve illustrates the inability of an inverter to pull the output node high. 60
3-17 With the addition of large h_n values, the output voltage swing will not be more than 10% to 90% of the supply voltage. The larger the tube diameter, the more effect h_n has on the output swing. 62

3-18 The output voltage swing varying by drain-control and carbon nanotube diameter. The more drain-control, the less voltage swing is possible on an inverter's output voltage. 62
3-19 A VTC curve, illustrating the potential effect of different h_n levels between the NFET and PFET transistors within an inverter. 63

4-1 The capacitance of a CNTFET is modeled as a cylinder with an oxide and cylindrical gate. However, when a CNT is placed on a thick bulk oxide, the capacitance model must change. B contains fringe capacitance. 66
4-2 An illustration of a carbon nanotube arrays with varying pitch. This research assumes that the nanotubes are more than 2*(R+t_{oxide}) apart, to eliminate capacitance coupling between devices. From [9] 67
4-3 The C_{gate} (for a nanotube in the middle of an array of parrallel tubes) versus the pitch. The solid symbols represent r=0.7nm and the open symbols are for r=1.5nm, where r is the CNT radius and t is the oxide thickness.[9] 68
4-4 To model the capacitance of a CNTFET, that is partially covered by a metallic top gate, the percentage of the nanotube circumference covered by the gate must be found. 68
4-5 The table above illustrates the modeled capacitance measurements for this research compared to those given in citation [9]. 69
4-6 A CNTFET channel length is dictated by the gate via contact dimensions. The drain and source vias are dictated by the same constraints. The $C_{drain-bulk}$, $C_{gate-backgate}$, $C_{gate-nanotube}$, C_{miller}, and $C_{source-bulk}$ are shown in the diagram. 69
4-7 The gate capacitance consists of both the metal gate to backgate and the metal gate to nanotube capacitances. The gate to nanotube capacitance depends on the nanotube diameter. Here the two types of gate capacitances are graphed versus the future lithographic generations for multiple nanotube diameters (D_t). The backgate oxide thickness is 100nm, compared to the gate oxide thickness of [1.1, 0.8, 0.65, 0.55, 0.5] for years [2007, 2010, 2013, 2016, 2018] respectively. The channel lengths are dependent on the ITRS Roadmap's lithographic specifications. 70

4-8 The load capacitance of an inverter chain depends on the Miller capacitance, the wire capacitance, the drain to bulk capacitance of the driving transistors (Transistors: 1 & 2), and the gate capacitances of the driven transistors (Transistors: 3 & 4). 71
4-9 As the years increase, the lithographic dimensions are decreasing according to the 2003 ITRS roadmap [10]. The Miller capacitance scales dramatically with lithography because it depends on both the width and the length of the contacts and the gate overlap. The gate capacitance mainly depends on the channel length. The drain to bulk capacitance depends on the metal via scaling. 72
4-10 The gate capacitance is smaller than the load capacitance of a CNTFET, especially with small diameter CNTs. However, the gate capacitance doubles if the number of carbon nanotubes per metal gate doubles; yet, the parasitic load capacitance remains constant; independent of the number of nanotubes. 73
4-11 The partial capacitance is an underestimate of the total gate capacitance because the fringe capacitance was neglected, however, the solid lines represent a coaxial formation that is an overestimate. The same results occur in the overestimate as in 4-10. 74
4-12 The parasitic load capacitance of a driving inverter is much larger than the extrinsic fanout capacitance in near term generations. This can lead to self loading if multiple nanotubes per gate are not used. However, as lithography scales down, the parasitic capacitance is dropping dramatically and self loading will become less of a problem. 75
4-13 Average current versus changing PFET diameter and h_n level. 76
4-14 Model of time delay for a PFET, with the original h_n value, versus the CNT diameter and the lithographic scaling by year (determined from [10]) 77

5-1 Graph of a PFET's measured I_d versus V_{ds} for varying V_{gs}[-0.5V: 0.5V]. Data courtisy of [11]. 79
5-2 Graph of I_d versus V_{ds} for a CNTFET's linear regime, data curtisy of IBM. Placed atop the data are trend lines to show the linearity of the data. 80

5-3 The slope of the triode regime depends linearly on the gate to source voltage, due to the control of the Schottky Barrier at the source. 81
5-4 Illustration dipicting the votlage that leads to saturation for a p-type carbon nanotube FET. Saturation occurs when no Schottky barrier exists at the drain. 82
5-5 The saturation voltage occurs linearly with a changing gate voltage. 82
5-6 CNTFETs with thinner gate oxides have more control over the energy band diagrams and, thus, tighter control over the irIV characteristics. Thin oxide data from [12] 83
5-7 Table depicting the characteristics of CNTFETs in comparison to future MOSFETs. 85
5-8 CNTFET IV characteristics for one nanotube measured in one dirction. The CNT was then flipped around and the current was measured again. The varying current levels prove that the intrinsic nanotube does not control the current voltage characteristics. [5] 86

6-1 NOR ROM arrays are created out of parallel NFET transistors from either MOSFET or CNTFET technology, sharing a ground contact to save area. The V_{bias} is an input to p-channel transistors that act as pull-up resistors. 89
6-2 If a CNTFET ROM is programmed with drain vias, the ground contacts can be shared, however, each transistor must have a seperate output, drain, contact. This can be used for a PFET or NFET NOR array, depending on the doping or annealing of the CNTFETs. 90
6-3 Extra contacts are needed if a NMOS NOR ROM is programmed by the addition of drain vias from the output bit line to a present transistor. The extra contacts add area and output capacitance. 91
6-4 The size of transistors is dictated by the metallic pitch for the gate, drain, and source contacts. This figure shows the values used in this research to predict the size of future ROM technologies. These sizes are based off of the predictions made by [10]. 92

6-5 An overlap is needed by the gate to source and gate to drain–without an overlap, a transistor will not work properly. A CNTFET ROM, programmed by the extended channel method, eliminates the need for extra drain contacts by selectively adding gate/drain and gate/souce overlaps to present transistors. . . . 93
6-6 To increase the current drive of transistors, CNTs can be added in parrallel. To save area and contact capactiance, 4 nanotubes can be placed under the same contact. Other layouts include 2 CNTs placed under 2 seperate contacts and the contacts wired together or, each CNT placed under a seperate contact. The contact number and dimensions dictates the area of the array. 94
6-7 The area savings associated with multiple nanotubes per contact can be outweighed by the redundancy associated with metallic nanotubes as shown in the scenario above. Here 4 CNTs per transistor are needed; in this case, it is beneficial in terms of area to have few CNTs per contact (Option 2) rather than Option 1 with 4 CNTs per contact. 96
6-8 The total number of contacts for a 128bit wide ROM, with 16 parallel CNTs per transistor. The number of CNTs per metal gate is varied on the x-axis and the percent of metallic CNTs is also varied. 97
6-9 The parasitic capacitance per bit line drops as the number of output contacts decrease, or the number of CNTs per contact increases. This graph shows the capacitance for a 128x128 ROM, with 16 CNTs per transistor, programmed by drain vias. 99
6-10 A ROM programmed with an extended gate will have a relatively large capacitance when few FET devices are present per bit line. This is because of the connection to all output contacts. However, as the number of FET devices increases per bitline, the shared contacts, used in the extended gate programming method, begin to become advantageous. 101

Chapter 1

Carbon Nanotubes Structure, Properties, and Growth

1.1 Background

The electronics industry continues to push the limits of Moore's Law. However, the physical restrictions of scaling metal oxide semiconductor field effect transistors (MOSFET) are becoming more prevalent; as these limitations arise, alternative technologies must replace the standard silicon technology. Completely disruptive technologies are being researched and among them carbon nanotubes offer a technology with a unique solution to scaling transistors and interconnects and with the possibility of integration into the well established, current Silicon technology, in the near future.

Since the discovery of carbon nanotubes in 1991, by Sumio Iijima [13], their many extraordinary properties and applications have been researched closely. Carbon nanotubes (CNT) can grow up to millimeters in length; however, their diameters are around 1nm to 40nm. These long thin nanotubes can withstand incredibly high current rates and can be used as both metal wires and channels of field effect transistors (FET). With these impressive properties, CNTs can aid the problem of shrinking electronics.

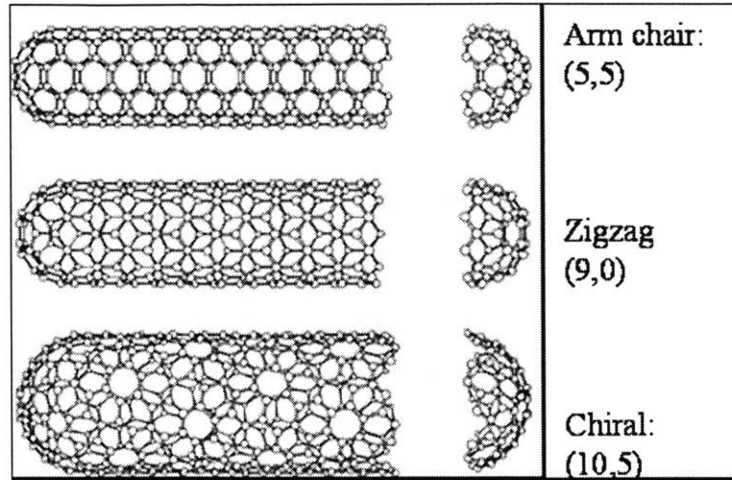


Figure 1-1: Carbon nanotube cylinders with varying chiralities. (From [1])

1.2 Structure of Carbon Nanotubes

Carbon nanotubes have extraordinary properties and applications on account of their unique structure. Carbon nanotubes are quantum wires with diameters ranging from approximately 1nm to 40nm and lengths reaching the millimeter range. [14] Such long thin nanotubes are formed out of flat sheets of hexagonal carbon lattices, called graphene sheets. To lower the large dangling bond energy of these flat graphene sheets, the sheets roll into cylindrical nanotubes. Such nanotubes are energetically favorable; the savings in dangling bond energy outweighs the increased strain energy of the tight cylinders. [15] To eliminate all dangling bonds within the nanotubes, the ends are usually capped with half a fullerene molecule.

1.2.1 Chirality

The particular roll orientation of a carbon nanotube (CNT) is called the chirality, see Figure 1-1 for examples. The chirality determines both the structure and the properties of a nanotube and is described by the chiral vector, $C_h = n\ \hat{a}_1 + m\ \hat{a}_2$, where n and m are integers in a two dimensional lattice space described by $\hat{a}_1$ and $\hat{a}_2$. [1]

There are three types of rolls: armchair, zigzag, and chiral as shown in Figure 1-1. Armchair nanotubes are formed when n=m, and thus, the angle between the chiral vectors is 30 degrees.

These nanotubes display metal characteristics. Zigzag nanotubes are formed when either n or m is equal to zero, and chiral nanotubes are created from all other angles. If $n+m=3j$, where j is an integer, the CNT forms a small band gap semiconductor and displays semi-metallic characteristics. The other angles, including zigzag and chiral, form semiconducting CNTs.

The single sheet of graphene, forming a carbon nanotube, limits the number of atomic standing wave vectors and confines electrons to travel along the nanotube axis. The number of possible wave vectors for conduction depends on the diameter of the nanotube. With a larger diameter, there is an increase in carbon atoms around the CNT perimeter and therefore, more atomic wave vectors exist. These extra wave vectors create additional band states, lowering the semiconducting band gap energy. Consequently, the diameter of the nanotube is proportional to $\frac{1}{Bandgap\ Energy}$. [1] [15] A nanotube with a lattice vector of (n,m)=(10,10) has a band gap of 0.5-0.65 eV and a diameter of 1.4 nm. With a diameter of approximately 3 nm, the bandgap energy is approximately equal to $\frac{kT}{q}$ at room temperature.

Theoretically, if the chirality could be controlled during CNT formation, it would be possible to change the properties of a nanotube within the growth process. A metal to semiconducting junction or a junction between two semiconductors of different bandgaps could be made within the same nanotube. In this way, Schottky barriers could be created within a nanotube. This change in band structure along a CNT's length can happen if a carbon pentagon-heptagonal pair is theoretically added as a defect to a nanotube, the addition would change the chirality from (n,m) to (n-1, m+1) or (n+1, m-1). The defect would case a permutation on the nanotube infinitely far away. If this control is available in future electronics, wires, diodes, and FET structures can be created and attached within a carbon nanotube structure, without the need for separate metal contacts. Presently, such control is impossible and only theoretical; this CNT characteristics will not be considered in this thesis.

This research and thesis will compare the characteristics of a nanotube's chirality and diameter to specific electronic applications.

1.2.2 Single Walled versus Multi Walled Carbon Nanotubes

The cylindrical carbon nanotubes described above can grow in two forms: multi walled or single walled. Multi walled carbon nanotubes (MWCNT) consist of concentric CNT cylinders held

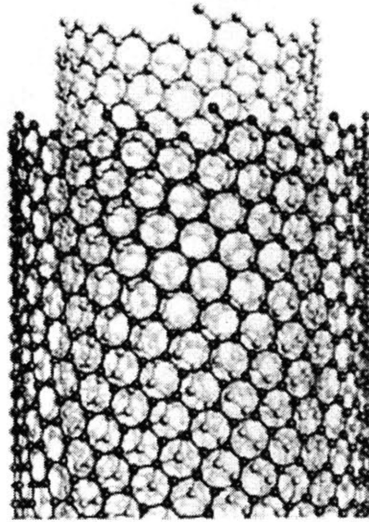


Figure 1-2: A multi walled carbon nanotube. (From [2])

within each other by van der Waals forces. The distance between shells is approximately 3.4Å, which is the van der Waals distance for two graphite carbon lattices. [15] An example of a MWCNT is shown in Figure 1-2.

The concentric shells of MWCNTs can differ in their chirality and can consist of both semiconducting and metallic nanotubes. If a MWCNT consists of both semiconducting and metallic cylinders, the metallic shells can negate the possible semiconducting properties. As a consequence, these multi walled carbon nanotubes have limited use in electronics. There is a process by which MWCNT shells can be eliminated, however, the outer shells are eliminated first. The elimination process involves large currents being placed on a MWCNT; a large percentage of the current is transferred down the outermost shell because of its direct contact with the electrode. Shells can withstand approximately 10^9 A/cm^2; however, with a larger current on a MWCNT, there will be a shell by shell failure due to current induced electrical breakdown. This breakdown of the outer shells can be seen in Figure 1-3.

Single walled carbon nanotubes (SWCNT) consist of one graphene cylinder of either a metallic or a semiconducting nature. Because of the single shell, these nanotubes can be classified by their properties related to their tube structure. For the rest of this research and

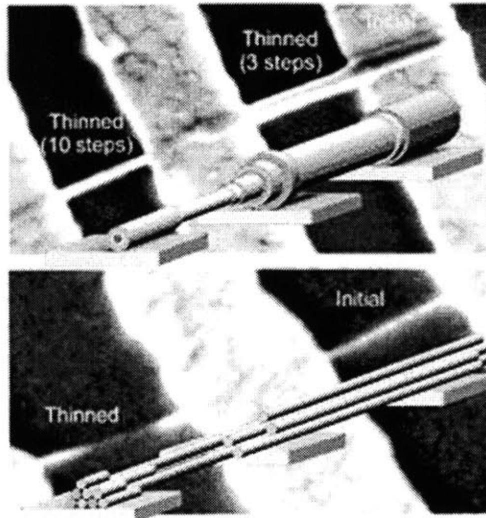


Figure 1-3: Multi walled carbon nanotubes are shown at the top and single walled carbon nanotubes are bundled in the second picture. (From [3])

thesis, only SWCNTs will be described, since they are a possible basis for future electronics; unless otherwise specified, CNT will mean SWCNT.

1.3 Growth Processes

Presently, much of the research involving carbon nanotubes is related to CNT growth and characterization. SWCNTs are difficult to grow. Currently, there are three methods by which to produce mass quantities of single walled nanotubes with a reasonably high yield: arc-discharge, chemical vapor deposition (CVD), and laser ablation. All three processes require a transition metal catalyst, such as Fe, Co, Ni, or Ti, for growth; the size and type of the catalyst, to some extent, controls the properties of a nanotube. However, none of these three processes can completely control the nanotube properties; all produce mixtures of metallic and semiconducting nanotubes with a wide range in CNT lengths and diameters. None of the three methods are ideal for the electronic industry. Below is a short description of the three processes that create carbon nanotubes, with micro to millimeter length scales.

1.3.1 Arc-Discharge

The process of arc-discharge can create large amounts of macroscopic CNTs. [16] In this process, two graphite rods are placed millimeters apart and are attached to a power supply. At the moment the power supply is turned on, a spark vaporizes the carbon into a plasma; when the plasma re-condenses, approximately 30% of it forms nanotubes at catalyst sites. [15] [17] This process creates very defect free structures; however, the process forms large amounts of by-products and the CNTs tend to be both multi walled and single walled, placed randomly in all directions, and the nanotubes are relatively short ($\leq 50\mu m$).

1.3.2 Chemical Vapor Deposition

Endo and Kroto [18] first created CNTs via chemical vapor deposition (CVD); Dai's group has continued to look closely at the CVD process. [19] [20] [21] To create CNTs via CVD, a substrate made of a powder-based transition metal catalyst [20] is placed in a heating chamber at approximately 600°C and hydrocarbon gas, such as methane, is added to the heating chamber. The gas decomposes and frees carbon atoms; these free carbon atoms can recombine at either a catalyst site or at the end of a carbon nanotube to increase the length of the nanotubes, see Figures 1-4 and 1-5.

Dai's group employs this CVD method to control the placement and direction of growth. The gas flow direction and the catalyst placement, by e-beam lithography, are closely monitored to help align nanotubes carefully on the substrate. The CVD method can theoretically produce large quantities of nanotubes at site specific locations. [22] However, this process does have limitations. CVD introduces more defects into the CNTs than arc-discharge. [17] Also, the alignment process still has large placement concerns, and chirality is not fully controlled.

1.3.3 Laser Ablation

CVD and laser ablation are the two main processes used to create CNTs for electronics. Laser ablation was discovered by Smalley's group. [23] A laser pulse is fired at graphite rods that contain a small amount of Co or Ni to help the carbon condense into SWCNTs. This process produces a hot carbon gas which condenses into bundles of 70%-90% single walled carbon nanotubes. [15] By using a particular catalyst, SWCNT can be created with a large percentage

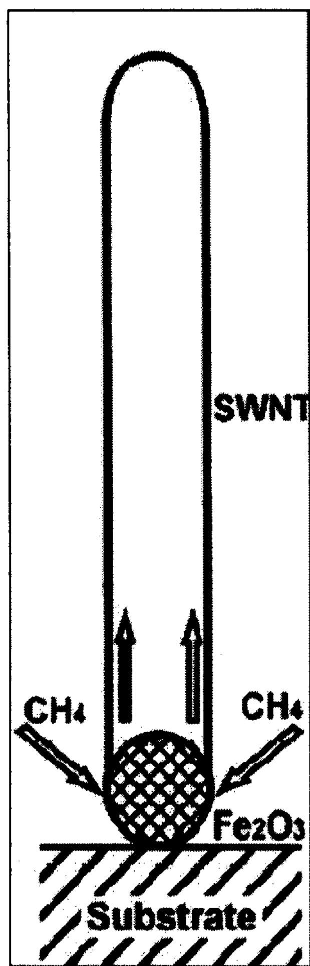


Figure 1-4: A diagram illustrating SWCNT growth by chemical vapor deposition. (From [4])

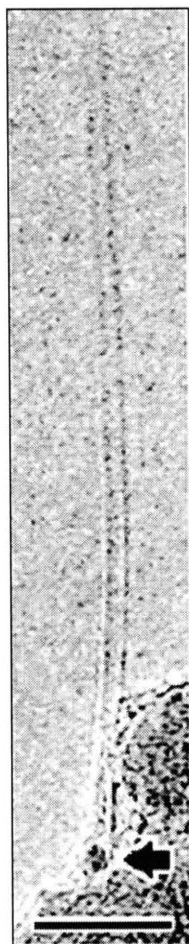


Figure 1-5: Picture of CVD growth from [4]. The bottom bar is a scale of 10 nm in length.

of similar diameter nanotubes. The diameters can be controlled by changing the reaction temperature and the catalyst. Typically the yield of carbon CNTs to total carbon processed is around 70%; however, it is the most expensive of the three processes.

Both the arc-discharge process and the laser ablation process necessitate solid-state carbon precursors and temperatures reaching up to thousands of degrees Celsius.

1.3.4 Growth Processes Variation

Presently, it is very difficult to achieve uniform diameters among nanotubes. Thus, the properties of each nanotube must be discovered after fabrication. The uncertainty of whether a nanotube is metallic or semiconducting creates large problems for circuit application of CNTs and will be considered in the read only memory chapter of this thesis. This research assumes some of these problems will be curtailed in the near future, or at least, the process variations must be controlled before carbon nanotubes can become truly integrated into circuit design applications.

1.4 Electron Mobility Characteristics in Carbon Nanotubes

Single walled carbon nanotubes have large potential for applications in electronics because of both their metallic and semiconducting properties and their capability for high current rates. Electrons and holes have a high current density along the length of a CNT due to the low scattering rates along the CNT axis. This type of structure is similar to an ideal waveguide.

When an electron or hole moves along the axis of a metallic or semiconducting CNT, the scattering rates are negligible. The scattering lengths for a carbon nanotube are on the micro meter length scale, while the relevant electronic distances are in the nanometer range. This is because of the limited number of impurities and defects in a carbon nanotube structure, and the lack of interface problems because of the saturated and stable chemical bonds forming the CNT. Atomic wave vectors create circular standing waves around the core and confine electrons and holes to travel solely in the axial direction. [15] The stable and saturated carbon-carbon bonds also limit electro migration in nanotubes; CNTs can carry current around 10 $\mu A/nm^2$, while standard metal wires have a current carrying capability around 10 nA/nm^2. Thus, carbon

nanotubes have the ideal current carrying capacity: a quintessential mobility and high electro migration thresholds. [15]

1.5 Conclusion

Carbon nanotubes offer an intriguing solution to the scaling of silicon electronics. Single walled carbon nanotubes, with their high carrier mobility and their possible metallic or semiconducting properties can be used in many electronic applications, such as the channel of transistors and metal interconnects. This thesis is centered around carbon nanotube applications to field effect transistors (FET). There continue to be many research groups studying CNT current, growth, and structure; however, little at this time has been done related to circuit characteristics and models.

This thesis strives to model semiconducting carbon nanotube FETs to illustrate their potential applications within the electronics industry. Chapter 2 of this thesis models the current voltage (IV) characteristics of a carbon nanotube transistor in the subthreshold or low voltage regime. The current in carbon nanotube FETs (CNTFET) is carefully described because it is due to a completely different physical process than the current within standard silicon devices. To create a full circuit model for these CNTFET devices, the above threshold IV model is described along with the capacitive model used in this research to characterize the energy and delay of CNTFET transistors.

The current models created in this research for CNTFETs are used in circuit structures, such as a voltage inverter and a read only memory (ROM). The trade-offs associated with different diameter carbon nanotubes is discussed in terms of voltage inverters. And, the potential benefits and trade-offs of CNT ROMs are discussed in relation to future generations of lithography and the possibility of metallic CNTs within the ROM. In general, this thesis models, and characterizes semiconducting CNT field effect transistors within digital circuit designs.

Chapter 2

Carbon Nanotubes as Transistors

The transport of electrons and holes in carbon nanotubes (CNT) has been described in Chapter 1: Carbon Nanotubes Structure, Properties, and Growth. Semiconducting single walled CNT current can be modulated with a voltage and can have similar IV characteristics to a metal oxide semiconducting field effect transistor (MOSFET). Therefore, these s-CNTs can be used in FET devices, but with higher current rates and a possibility for better scaling characteristics compared to Silicon devices.

There are two main types of carbon nanotube FETs differing by their current injection methods: Schottky barrier FETs [5] [6] [8] [24] [25] [26], and doped CNTFETs, [14] [19]. This research only models Schottky Barrier (SB) carbon nanotube FETs.

2.1 Schottky Barrier Field Effect Transistors: Fabrication

It has been shown that semiconducting carbon nanotubes can be used as the conducting channel in Schottky barrier carbon nanotube FETs (CNTFET). [5] [6] [8] [24] [25] [26] [27] [28] To create such devices, nanotubes are grown on top of a thick silicon dioxide, which is itself on a silicon wafer. Metal contacts, commonly made of Titanium or Cobalt, are placed over the nanotube to create source and drain contacts. To form a strong interaction between the metal and the nanotube, the metal is annealed at 850°C for approximately 100 seconds to form metal carbides. [29] These high annealing temperatures are acceptable because the carbon nanotube structure can withstand temperatures up to its melting point of around 3,000°C. [15] When multiple

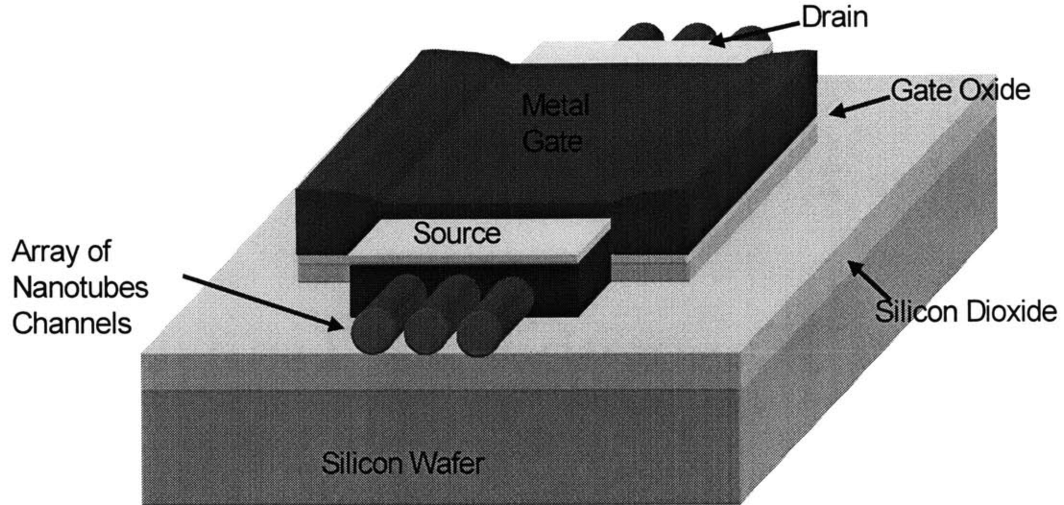


Figure 2-1: Diagram of a top gated CNT transistor structure.

metal contacts are laid along the length of a nanotube, many transistors are formed along the CNT. The length of the nanotube, between two contacts, acts as the channel of a transistor with metal source and drain. Because of the fixed CNT diameter once a nanotube is grown, the width of the nanotube cannot be changed to increase the current drive; instead, a transistor's width and current drive can be increased by adding nanotubes in parallel.

A metal gate, in contrast to a MOSFET's poly Silicon gate, is used to modulate the electronic band structure of the source, drain, and carbon nanotube through a thin gate oxide. The metal gate and oxide must overlap slightly with the source and drain contacts. This overlap limits the area savings of CNTFETs because of the lithographic pitch requirements between the metal gate and the metal source and drain contacts and vias. The current is regulated by the gate to source and gate to drain interactions. Figure 2-1 is a theoretical illustration of a carbon nanotube FET structure. The structure resembles that of a MOSFET, but the nanotube is the channel for conduction. The structure and operation of CNTFETs will be given below.

2.2 Schottky Barrier Field Effect Transistors: Operation

Background

To understand the operation of a Schottky barrier CNTFET, the energy band diagram for the structure should be studied. At the intersection between the metal carbide contacts and the semiconducting carbon nanotube, Schottky barriers are created. The energy band diagrams in Figure 2-2 illustrate this situation. The current in CNTFETs is from the tunneling of carriers through the Schottky barriers. The type of metal for the contacts is chosen so that its work function forces the metal Fermi Level to lie between the valance and conduction band of the CNT, hopefully lining up approximately in the center of the s-CNT's energy band. The work function for Al is 4.2eV and Ti is 3.9eV; these are similar to the work function of a CNT with a diameter of 1.4nm (≈4.5 eV). [12] Titanium is used most frequently because of its stable carbide. [15] For the strongest nanotube to contact interactions, the contact is best placed at the end of a nanotube, because of possible loose carbon-carbon bonds within the tube structure. However, if many transistors are placed along the length of a nanotube, tube-end contacts are not always possible.

At sufficiently short channel lights, the CNT channel can become ballistic and hence, the metal contact resistance and the Schottky barriers at the source and drain ends limit the current drive through the nanotube. Thus, a low contact resistance, such as that of Titanium, is desirable. Presently, the control of the metal contacts to carbon nanotubes is not consistent and the tunneling current levels between transistors can vary greatly, even on the order of magnitude. This problem must be addressed before mass numbers of CNT circuits can be realized.

Operation

Typically, CNTFETs are pFETs. When a negative voltage is applied between the drain and source, the band structure, of the CNT, is modulated to account for the drain to source voltage (V_{ds}) as shown in Figure 2-2.

When a small negative gate to source voltage is applied, a CNTFET is in the subthreshold regime. With a negative gate voltage applied, the Schottky barrier width at the source is

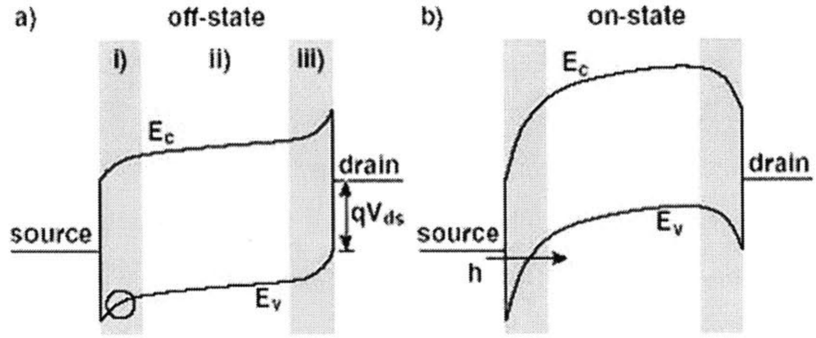


Figure 2-2: Illustration of band diagrams for a Schottky barrier CNT transistor in the 'off' and 'on' states, respectively. (From [5].)

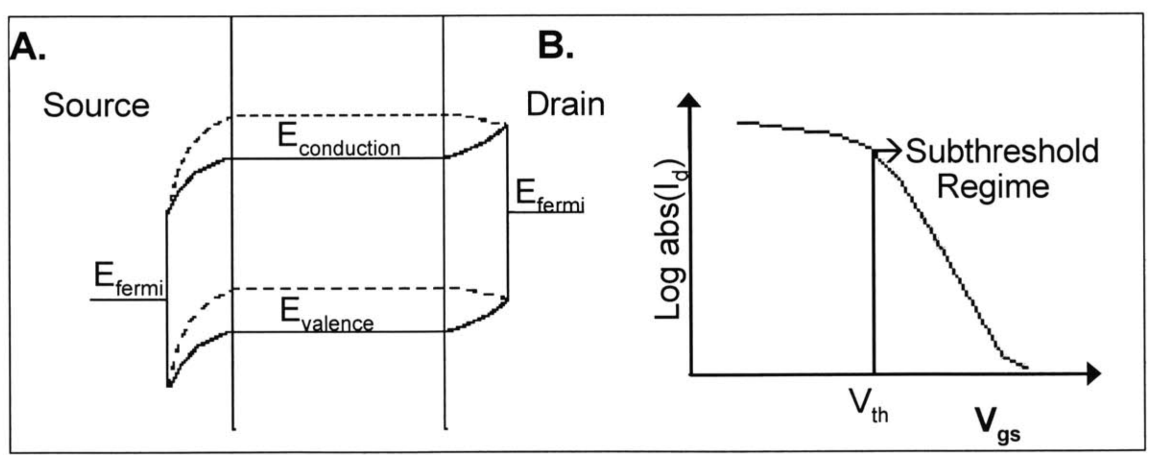


Figure 2-3: Subthreshold band diagrams for Schottky barrier transistors related to the I_d versus V_{gs} graph.

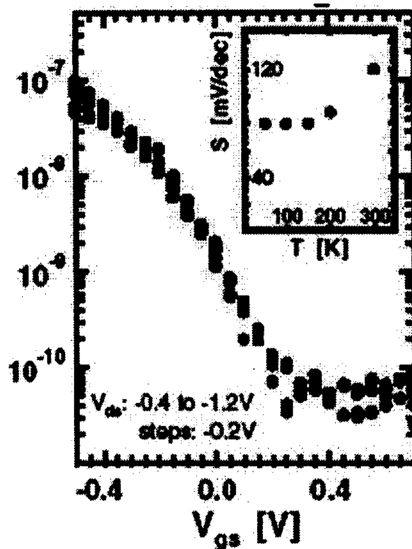


Figure 2-4: I_d versus V_{gs} subthreshold characteristics for a p-type transitor, with a channel length of 300nm and a gate oxide thickness (t_{ox}), HfO_2, of 20nm. The subthreshold characteristics do not vary largely with V_{ds} and the subthreshold slope, S, remains relatively constant with temperature. (From [5])

modulated, allowing for holes to tunnel through the valence band and pass unimpeded to the drain. This state is illustrated in of Figure 2-2 b. The thickness of the source Schottky barrier at the metal Fermi level decreases exponentially with an increasing gate to source voltage. Thus, the tunneling current through the Schottky barrier increases exponentially, inversely to the barrier thickness. See Figure 2-3 for the exponential current-voltage (IV) characteristics of the subthreshold regime. The I_d versus V_{gs} graphs do not differ greatly with a changing V_{ds} because the drain voltage does not significantly control the source Schottky barrier. This exponential current relation can be seen in the Figure 2-4.

If the gate voltage increases in the opposite direction, with a positive V_{gs}, the same effect will occur due to the Schottky Barrier on the opposite side of the s-CNT energy band; however, since the metal Fermi level is further away from the conduction band, a larger gate voltage is needed to achieve similar current levels. See Figure 2-5 to explain how a CNTFET can act as an ambipolar device–both an n-channel and a p-channel transistor depending on the FET voltages. Also, to note about CNTFET devices is, if the metal work function is varied, the

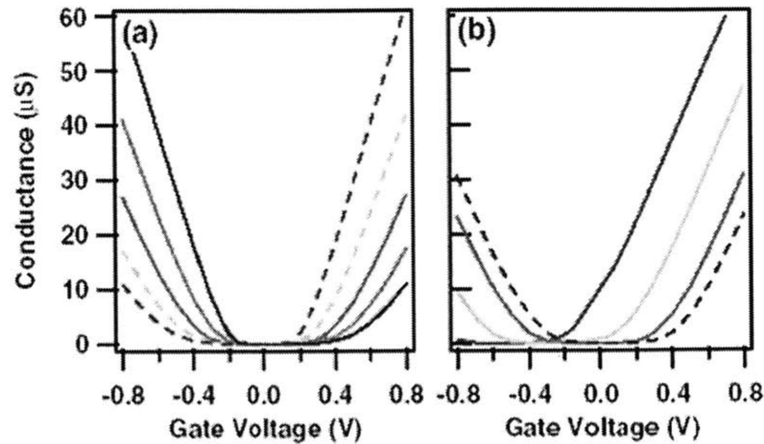


Figure 2-5: Conductance changes as the work function of the drain and source metals are varied to the band gap of the semiconducting CNT. Also, these graphs note how current increases if an opposite gate voltage is applied. (From [6])

graph of the I_{ds} versus V_{gs} curves are shifted horizontally on the voltage axis as shown in Figure 2-5.

The transistor threshold voltage, where the device acts similarly to an 'on' MOSFET, is reached when the metal source Fermi level is approximately even with the valence or conduction band of the s-CNT, in a p-channel or n-channel respectively. If the gate voltage continues to increase above this threshold, the Schottky barrier thickness at the source will remain constant and the current will not continue to increase exponentially. Above the threshold voltage, the current will only increase linearly with V_{ds}. See Figure 2-6 along with Figure 2-7 to show this effect.

Above the CNTFET threshold voltage, the current voltage characteristics look very similar to a MOSFET's IV characteristics; the current increases linearly with V_{ds}; and, when the barrier at the drain is completely eliminated, the FET current saturates. A saturated SB-CNTFETs has very little slope on the I_d versus V_{ds} graph, unlike short channel MOSFETs.

The start of the saturation regime is dependent on the gate to source and the drain to source voltages. By studying the energy bands shown in Figure 2-6, it can be seen that the band modulation from V_{ds} has to be greater or equal to the band modulation due to V_{gs} for CNTFETs that use Titanium for the source, drain, and gate. In most electronic applications,

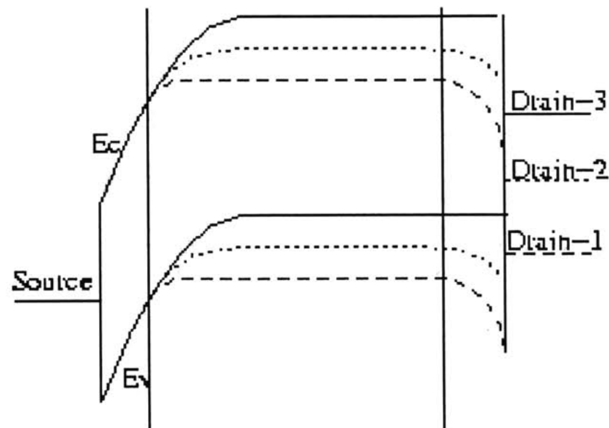


Figure 2-6: Band diagrams for a Schottky barrier transistor in the triode regime and at the saturation point.

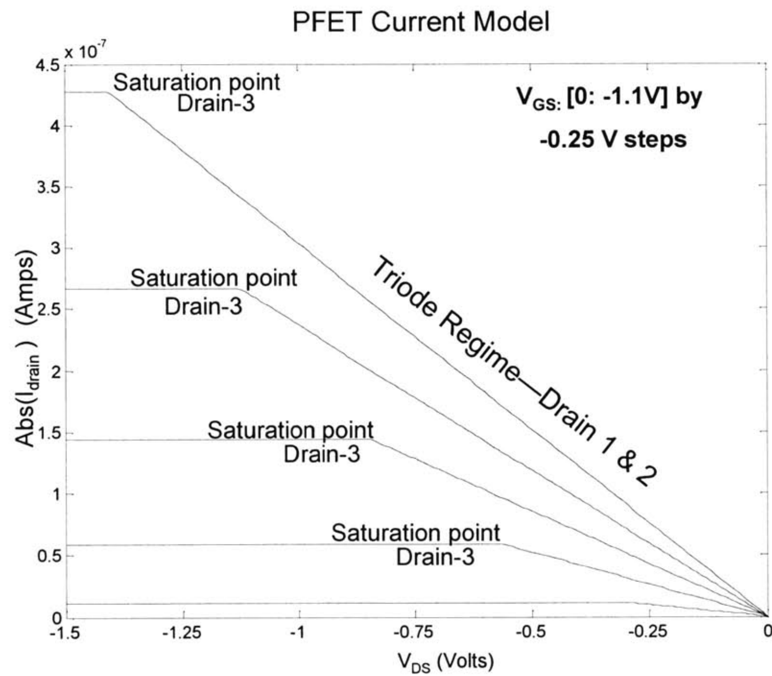


Figure 2-7: This figure follows the drain voltages shown in Figure 2-6. Drain-1 & 2: Linear Regime, Drain-3: Saturation point

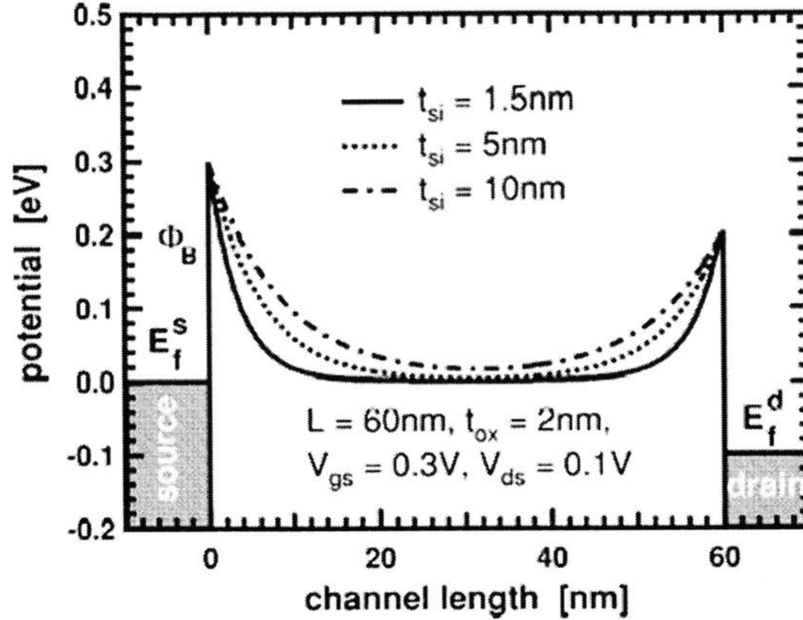


Figure 2-8: Energy band bending of a CNTFET is larger with a thinner gate oxide. (From [7])

the gate to source voltage does not surpass the drain to source voltage. Thus, CNTFETs will be in the linear (triode) or the subthreshold regime and will not enter saturation.

In Schottky barrier devices, it is beneficial to have the gate voltage modulate the tunneling barrier at the source end as strongly as possible. To achieve this, the gate-channel capacitance must be very high (at the moment SiO_2 oxides range in thickness around 1-10nm and high κ dielectrics, such as ZrO_2, have been used to lower this capacitance [21]), see Figure 2-8. Many types of dielectrics can be used in carbon nanotube FETs. All carbon-carbon bonds are satisfied in carbon nanotubes and as a consequence, they have no interface states associated with oxides.

In this research, IBM data is used to model the current in CNTFETs. The model will be described in the following chapters of this thesis.

2.3 Carbon Nanotube Transistor Width

If large current rates are needed in CNTFETs, the nanotube diameters cannot be increased. To increase the transistor width, nanotubes can be added in parallel under a shared metallic

gate, see Figure 2-1. Thus, the width of a CNTFET can not be increased linearly, but rather the width is quantized by the number of nanotubes in parallel.

Multiple nanotubes can be placed in close proximity, sharing the same metallic gate; however, the nanotubes cannot be placed directly next to or on top of each other. The gate capacitance limits the proximity of these parallel nanotubes. If carbon nanotubes are placed too close to each other, capacitive screening of the gate, from neighboring CNTs, will become a problem. [26] More capacitance related issues will be discussed in Chapter 4: Capacitance, Energy, and Delay of Subthreshold CNTFETs.

2.4 P-Channel versus N-Channel Schottky barrier CNTFETs

It was mentioned previously that CNTFET current is a result of hole or electron tunneling through the source and drain contact Schottky barriers, depending on the gate and drain voltages. In all of the band diagrams previously described, the current is the product of holes tunneling through the Schottky barrier on the valance band. However, if the gate and source are given large positive voltages, electrons will begin to tunnel through the Schottky barrier at the conduction band edge, to create an n-channel transistor. Thus, a CNTFET can act as both an n-channel and a p-channel transistor depending on the voltages; this type of device is called an ambipolar transistor.

Theoretically, if the work function of the source metal were aligned directly with the middle of the s-CNT, the current would be perfectly symmetrical for holes and electrons around a certain gate to source and gate to drain voltage. As the voltages increase, in either direction, the FET will act as either a p-channel transistor or an n-channel transistor with equal, but opposite characteristics. This is because short CNTs have ballistic current and therefore, the mobility for holes and electrons is essentially the same. This fact must be taken into consideration when sizing transistors: the standard MOSFET assumption, that PMOS transistors must be 2-3 times as wide in as NMOS transistors, is not applicable in this case. CNT n-channel and p-channel transistors will be sized symmetrically. This fact will help in complementary logic style circuit designs.

If the source Fermi level lines-up closer to the CNT valence band, a carbon nanotube

transistor will have better p-type characteristics. Changing the relation of the metal E_{fermi} to the s-CNT band gap effects the thickness of the Schottky barrier and therefore, influences the tunneling rate of holes or electrons and changes the current characteristics. At first glance, if the work function of the metal were changed to line-up with the valence band of the CNT, one would assume a perfect ohmic contact and an ideal p-channel transistor. However, a Schottky barrier is created at the junction independent of the metal work function. [7]

The CNTFETs created by IBM have better p-channel characteristics because of the work function of Ti in relation to the CNT energy band. However, better n-channel characteristics can be achieved by shifting the line-up of the source Fermi level with the CNT band gap. This shifting can happen through either an annealing or a doping process. Below is a short description of these two processes.

2.4.1 Annealing

If CNT transistors, with better PFET characteristics (p-channel transistors), are vacuum annealed, they can be converted to better n-channel CNTFETs. In the annealing process, absorbed oxygen is driven out of the contact region; this process shifts the metal Fermi level up in relation to the CNT band gap and thus, lowers the Schottky barrier at the conduction band edge. In turn, the electron tunneling current increases and the device has better n-channel characteristics. Graphically, the annealing process moves the I_{ds}-V_{gs} curve toward more negative gate voltages; however, it does not change the shape of the curve; see Figure 2-9. Physically, annealing removes the oxygen from the contact, which changes the surface potential of the metal contacts to the CNT band gap. This process is reversible; if the CNT is exposed to air, the original IV characteristics will return.

2.4.2 Doping with Alkali Metals

Doping nanotubes with an alkali metal, such as potassium, has the same result as the annealing process; transistors can be made to have better p- or n-channel properties by graphically shifting the IV characteristics of a Schottky barrier transistor. Physically, potassium can be used to adjust the s-CNT bandgap in relation to the source and drain metal Fermi levels. Doping does not lead to intrinsic CNTs, instead doping shifts the current versus gate voltage curves, as can

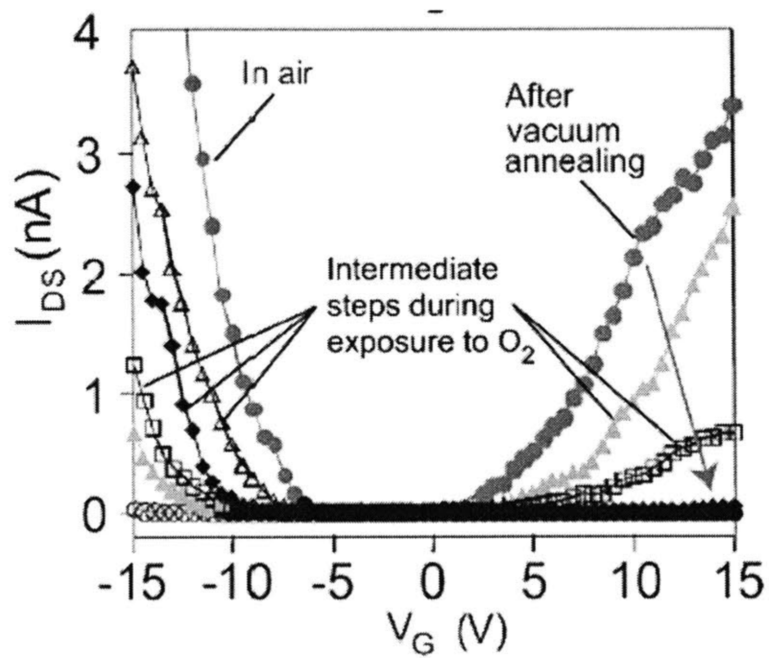


Figure 2-9: CNTFET IV characteristics, depending on oxidation of the CNT to metal interface. (From [7])

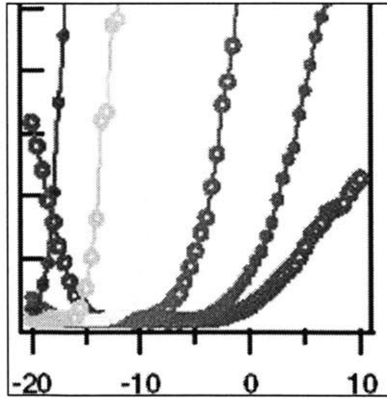


Figure 2-10: Shifting of I_d versus V_{gs} curves, with a varying amounts of potassium. (From [6])

be seen from the graphs in Figures 2-10 and 2-11.

2.4.3 Conclusion

Ambipolar Schottky barrier CNTFETs can be used as both p-channel and n-channel FETs depending on the relative drain, gate and source voltages. If the transistors are doped or annealed, their IV characteristics can be shifted towards better p-type or n-type transistors. This shift can be used to the advantage of a circuit designer if there are precise process controls.

2.5 CNTFET Scaling

The carbon nanotube transistor devices described in this chapter are similar in structure and IV characteristics to MOSFETs, however, they have certain properties that make them viable candidates for future technologies. CNTFETs have ballistic transport, ambipolar voltage characteristics, and increased scaling ability. MOSFETs scale in dimension to increase speed and density and to lower power. However, fundamental scaling limits are going to constrain future Silicon devices. Currently increased device performance and lower power are achieved by scaling all dimensions and characteristics by $\alpha>1$. The following describes the generalized scaling methodology for MOSFETs.

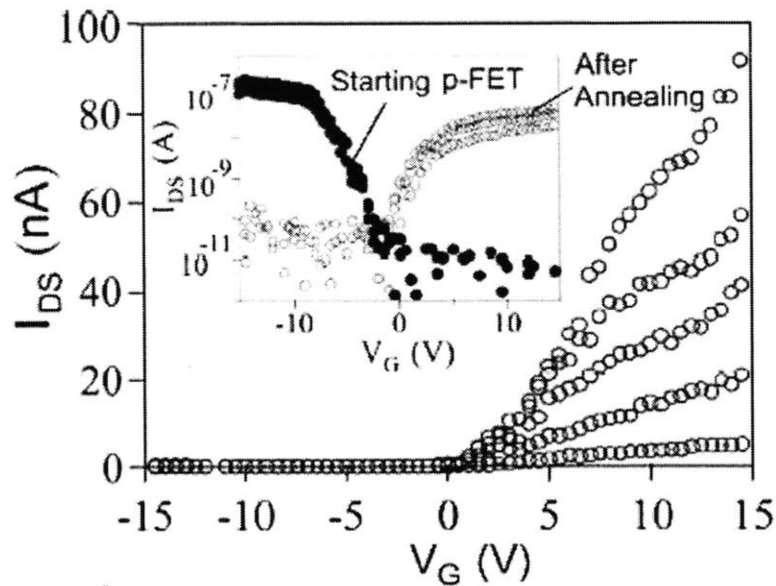


Figure 2-11: Conversion between P and N type CNTFETs, using an annealing process in vacuum. (From [8])

Dimensions	$\frac{t_{oxide}}{\alpha}$, $\frac{Channel_Length}{\alpha}$, $\frac{Vertical_Dimensions}{\alpha}$, $\frac{Width}{\alpha}$
Substrate Doping	$\alpha * N_A$
Lower Voltage	$Vdd \Downarrow$
Higher Density	α^2
Higher Speed	α
Power Density	*constant*

MOSFET scaling is causing more severe problems with each future generation. Carbon nanotube transistors are immune from some of the same scaling constraints. The current levels in a CNTFET do not depend on the channel length. Thus, in comparison to MOSFETs, there is no channel length minimization or subsequent substrate doping problems. Also, in MOSFETs, the gate oxide thickness has already entered the nanometer range; channel scattering from the rough oxide interface and tunneling through the thin oxide are becoming prevalent problems. Carbon nanotube transistors do not have these difficulties; all chemical bonds are satisfied in a CNT and thus, there are fewer oxide to channel interface problems. A multitude of oxides can be placed on the nanotubes and thus, many high-κ dielectrics can be incorporated into CNTFETs

to reduce the tunneling currents. And, the nanotube, in essence, protects the conducting channel form any interface problems; ballistic transport can continue in a CNT independent of the oxide.

2.6 Conclusion

In conclusion, complementary transistors can be created along the length of a carbon nanotube. And thus, intermolecular devices are possible. Certain aspects of these CNTFETs make them strong candidates for future electronics. Carbon nanotube FET devices do not have problems with short channel effects, there is no electro migration, the breakdown is very high. And, the NFET and PFET devices are symmetrical, which is ideal for CMOS structures. These characteristics leave CNTFETs as a viable option for future technology generations.

Chapter 3

Subthreshold Carbon Nanotube Field Effect Transistors

The portable electronics industry has expanded dramatically in the recent years. With this increase, there has been a focus on lower power applications. Future technologies, such as carbon nanotube transistors must accommodate and follow these low power trends.

Scaling down the supply voltage of electronics decreases the power quadratically. Weak inversion or subthreshold circuit operation allows the ultimate in voltage supply scaling; the supply voltage is lower than the threshold voltage of a transistor; thus, the transistor 'on' to 'off' current ratio is small. Such logic MOSFET subthreshold circuits have been tested functional down to approximately 180mV. [30] The threshold voltage of carbon nanotube transistors will scale down when the gate oxide and the gate work function decrease or the CNT diameter is increased. The CNT diameter is not linked with technology scaling. Therefore, the threshold voltage will probably not scale as fast as the supply voltages and CNTFETs will have to operate in the low voltage, subthreshold regime. It is also important to research CNTFETs in the subthreshold regime because of their future operation at low voltages and the disparity in CNTFET low voltage characteristics from MOSFET subthreshold IV characteristics. Because of this difference, this chapter will look closely at the subthreshold characteristics of CNTFETs.

An important metric in subthreshold design is the ratio of on-current to off-current (I_{on}:I_{off}). This ratio characterizes the difference in current between a closed and open switch, or a transis-

tor with an 'on' voltage versus 'off' voltage on the control gate. A large ratio of leakage currents, I_{on}:I_{off}, will give functionality in digital logic design. Carbon nanotubes have a varying I_{on}:I_{off} ratio, depending on the nanotube structure and properties.

Many low power applications, such as hearing aids, trade performance for power savings; the 'off' current is a crucial factor in lowering the power. The 'on' or high current is still an important metric in subthreshold design. Carbon nanotubes have very high current because of their ballistic transport and their limited electron and hole scattering. Therefore, CNTs have the ability to increase performance while adhering to lower power requirements in subthreshold circuits.

The I_{on} in MOSFETs decreases exponentially as the supply voltage is lowered; the same is true in carbon nanotube transistors. However, compared to MOSFETs, the off-current in CNTFETs continues to decrease as the voltage across the FET from drain to source decreases. Thus, as the supply voltage is lowered in CNTFETs, the ratio of I_{on}:I_{off} can remain large for certain circuits.

This research will model, using Matlab, CNT Schottky barrier (SB) transistors in the low voltage, subthreshold regime from data given by Appenzeller at TJ Watson Research Center, IBM. The Matlab model will be used to determine the functionality of future subthreshold CNTFETs in digital design, accounting for changing nanotube properties and process variations.

3.1 Subthreshold CNTFET Current

CNTFETs can act as ambipolar transistors, however, the IBM data given are for CNTFETs acting as n-channel transistors. In this research, an assumption is made that a carbon nanotube transistor has symmetric current drives for holes and electrons around a minimum current. Also, as was previously described, the source and drain Fermi levels can be moved in relation to the CNT band gap. With this fact, n-channel and p-channel IV characteristics can be equal for the absolute value of the applied voltages, $|V_{drain-source}|$ ($|V_{ds}|$) and $|V_{gate-source}|$ ($|V_{gs}|$). This result is based on the physical understanding that carbon nanotube channels conduct ballistically at the length ranges in question and, as a result, both electrons and holes have the same velocity. This means that p-channel or n-channel transistors can have the same current

levels when their widths and process variations are equal and the V_{gs} and V_{ds} are equal and of opposite sign.

3.1.1 Current versus $V_{Gate-Source}$ Characteristics

It was described in Chapter 2 that the subthreshold current of a CNTFET increases exponentially as the thickness of the Schottky barrier at the source decreases. In this section, the I_d versus $V_{gate-source}$ characteristics will be discussed and modeled.

Minimum Current

The exponential current-voltage (I_d versus V_{gs}) relationship of subthreshold CNTFETs is also seen in MOS transistors. However, there is a large difference in the IV characteristics between CNT and MOS transistors; the minimum current of a CNTFET does not occur at V_{gs}=0 Volts, as it does for MOSFETs; instead, the minimum current occurs at $V_{gs}=\frac{V_{ds}}{2}$. This is true for all Schottky barrier CNTFETs that have the same metal used for the gate, drain, and source and transistors that are not doped. The minimum voltage will remain at $V_{gs}=\frac{V_{ds}}{2}$, independent of the metal work function; however, a work function or metal change will greatly effect the current level at the minimum voltage.

The total current in a carbon nanotube transistor depends on the tunneling currents of both holes and electrons through the source and the drain SBs. The minimum current occurs when the energy band bending at the SBs is minimum and therefore, when both the hole and electron currents are minimized. To minimize the CNT band bending at the SBs, the voltage drop from V_{ds} is split between the source and drain Schottky barriers. As can be seen in Figure 3-1, when one of the Schottky barriers becomes thinner, by a change in V_{gs}, the electron or hole tunneling current starts to increase exponentially through the respective Schottky Barrier.

This minimum CNT transistor current and the exponential subthreshold characteristics can be noted in the subthreshold current data in Figure 3-2, courtesy of Joerg Appenzeller at IBM TJ Watson. The data, in Figure 3-2, illustrate the current-voltage characteristics for two n-channel devices made with different diameter (D_t) carbon nanotubes, 1.3nm and 2.5nm. The gate oxide, in both devices, is 2nm thick (t_{ox}=2nm) and the metal source and drain Fermi levels match with the mid-band of the carbon nanotube.

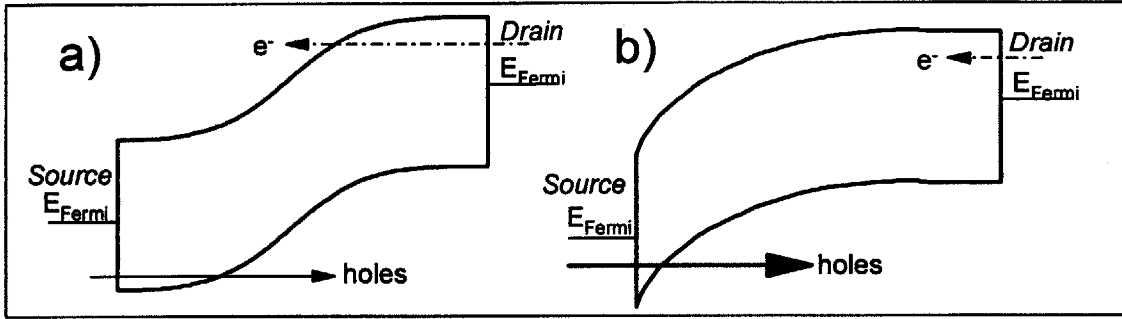


Figure 3-1: Picture A represents the band modulation of a transistor with the least current; the V_{ds} voltage is split evenly between the source to channel and drain to channel and thus the Schottky barriers are thickest and the current is at a minimum. In picture B, the band diagrams illustrate a transistor that is 'on', with a larger negative gate voltage. The hole tunneling current from the source is orders of magnitude larger than the electron tunneling current from the drain. In both A and B, the arrows represent the hole and electron tunneling currents. The relative size of these arrows represents the relative size of the tunneling currents.

The model created in this research models the minimum current for devices with t_{ox}=2nm and $E_{Fermi-metal} = E_{CNT_midband_gap}$ by the following equations:

$D_n = 6.96 * 10^{-20} \exp\{9.17 * \ D_t(nm)\}$, where D_t is the CNT diameter is nanometers.

$I_{d-\min imum} = D_n \exp(h_n \, |V_{ds}|)$, where h_n is a constant dependent on the drain control level, that will be explained in a later section of this chapter.

No Potential Difference across a CNTFET

The graphs in Figure 3-2 do not illustrate the current for when the drain to source voltage falls to zero volts (V_{ds}=0V). Assuming a large gate to source voltage (V_{gs}) and a nonzero V_{ds}, a current will flow; however, with no voltage difference from the source to the drain, no potential difference will exists across the structure and the current will fall suddenly to zero amps. Conversely, with even a slight source to drain voltage, the current will jump to the values illustrated by the data. This jump occurs suddenly because holes and electrons will tunnel between the source and drain, until there is no potential difference across the transistor. Thus, the hole and electron tunneling currents will continue until no potential exists and V_{ds}=0V.

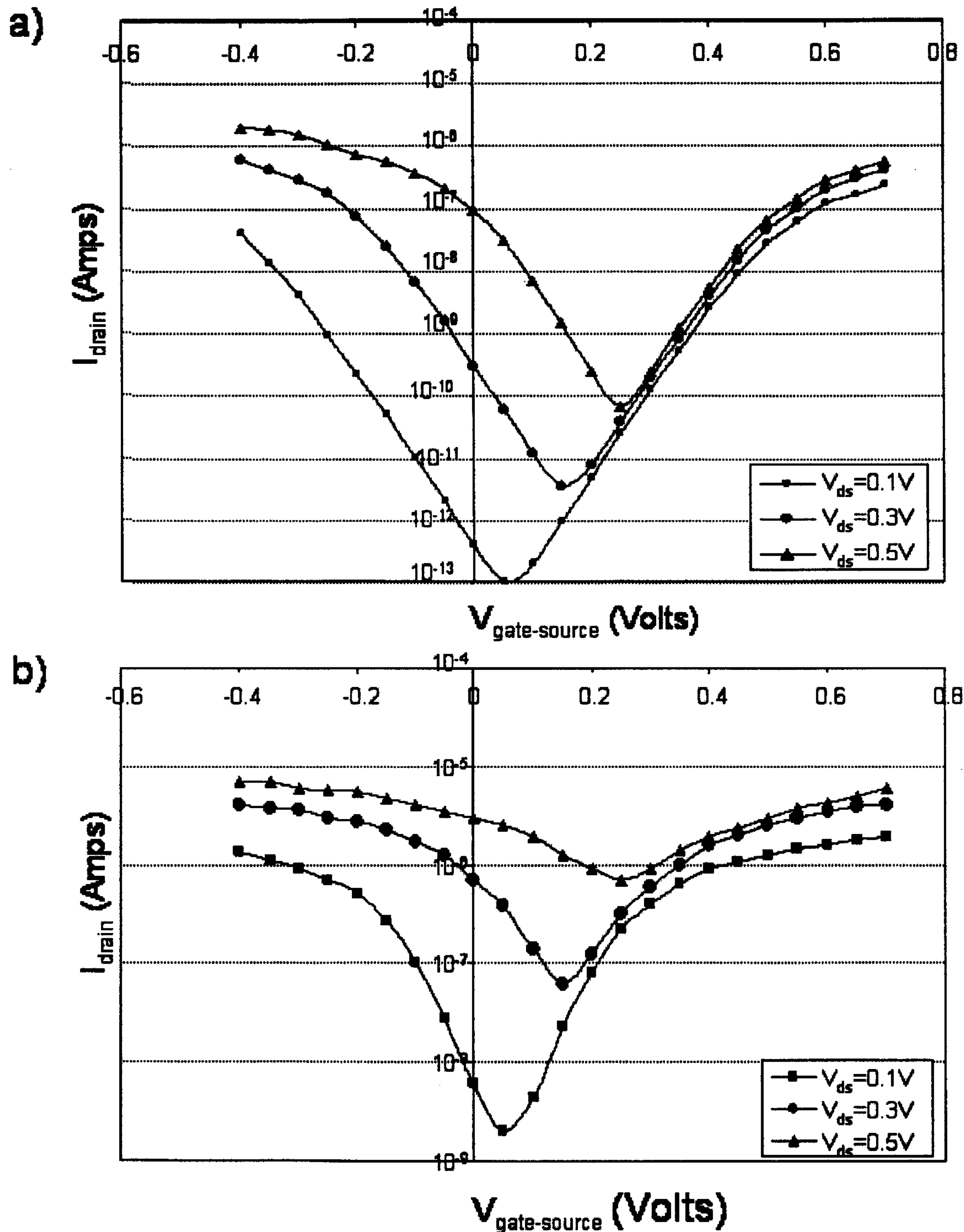


Figure 3-2: Subthreshold IV characteristics. Graph A: CNT Diameter (D_t) =1.3nm. Graph B: D_t=2.5nm. Both FET devices have a mid-band gap line up and an oxide thickness of 2nm (t_{oxide}=2nm) and titanium source, drain and gate contacts. Data obtained from Joerg Appenzeller at IBM.

Changing Diameters

It can be observed from the graphs in Figure 3-2 that the current changes dramatically with a change in nanotube diameter. It was described in Chapter 1: Carbon Nanotubes Structure, Properties, and Growth that the energy bandgap of a CNT is inversely proportional to the nanotube diameter ($E_{gap} \alpha \frac{1}{Diameter}$). With a smaller CNT energy bandgap (larger diameter), the Schottky barrier (SB) formed at the metal contact will be smaller if the metal Fermi level is equal to the mid bandgap of the CNT. The smaller SB, will lead to an exponentially larger tunneling current. However, this fact also means that the off-current will be much larger because the Schottky barriers for both electrons and holes will be smaller. This creates a trade-off between the performance and the on- to off-current ratio.

Another aspect of the CNT E_{gap} being inversely proportional to the diameter is that the threshold voltage varies. The threshold voltage of a CNTFET occurs when the CNT valence or conduction band is equal to the Fermi energy at the metal source, for a PFET or NFET respectively. Because the band gap is smaller for a large diameter nanotube, the threshold voltage will be reached sooner and be smaller in magnitude. Figure 3-2 illustrates the difference in IV characteristics for different diameter nanotubes.

3.2 Matlab Model

3.2.1 I_{drain} versus $V_{gate-source}$ Model

A Matlab model is created in this research to simulate the IV characteristics of a CNTFET. The overall CNTFET model is formed with a theoretical understanding of CNTFETs and with the IBM IV measurements given in Figure 3-2. Graphs of I_d versus V_{gs} characteristics from the Matlab model, are shown in Figures 3-3 and 3-4 for n-channel transistors and in Figure 3-5 for a p-channel transistor. Because $E_{Fermi-metal} = E_{CNT_midband_gap}$ is an assumption in this model, the p-channel current characteristics are equal to the n-channel IV data, except the voltages are negated. These figures also illustrate the differences between CNTFETs of varying nanotube diameter.

The model is characterized by the minimum current at $\frac{V_{ds}}{2}$, the threshold voltage, and the exponential subthreshold current. The following expressions illustrate the current for an

n-channel transistor.

$V_{Threshold} = \{-0.125 * (D_t/2)\} + 0.6625$

$V_{\min} = \frac{V_{ds}}{2}$

$D_n = 6.96 * 10^{-20} \exp(9.17 * D_t)$

$I_{d-\min} = D_n \exp(h_n |V_{ds}|)$, where h_n is a constant depending on the process variations

$I_{d_nchannel} = I_{d-\min} \exp(a_n |V_{gs} - V_{\min}|)$, where a_n is a function of t_{oxide} and the CNT diameter.

The model fit to the original data is shown in Figure 3-6.

The p-channel transistor follows the same expressions except the voltages are negated.

The CNTFET subthreshold regime occurs between the two threshold voltage points occurring because of the CNTFET ambipolar characteristics. The threshold voltage points are equal distance from the minimum voltage. The distance from the minimum to the threshold is $\delta V_{sub}(V_{ds}) = (V_{Threshold} - V_{\min})$. In Figure 3-3, the two threshold points can only be see for $V_{ds} = 0.5V$ because δV_{sub} is smallest and $\{V_{\min} - \delta V_{sub}(V_{ds} = 0.5V)\} > \{V_{gs} = 0V\}$.

Non Idealities in Model

In an ideal subthreshold CNT transistor, the gate fully controls the source to channel tunneling barrier and thus, the total IV characteristics of the subthreshold FET. However, the gate does not have an ideal control over the source; instead, the drain to source voltage has some control over the source Schottky barrier and therefore, the IV characteristics of the device. The strength of the gate control over the source Schottky barrier (SB) depends on the CNTFET channel length and contact process variations. More carbon-carbon bonds broken during the contact annealing process will ensure a better nanotube to contact control. There is a large spread between the drain control versus gate control of different devices within and between research groups; this research considers the spread in terms of the IV model and the circuit structures presented. The drain control versus gate control is accounted for in the h_n value. The h_n value extrapolated from the data is considered the original h_n value. When h_n is larger than the original, the gate has a weaker control and the drain has a stronger control over the source SB; when h_n is small or nonexistent, the drain has no control over the source tunneling current and the gate voltage completely controls the subthreshold FET IV characteristics. Figure 3-7

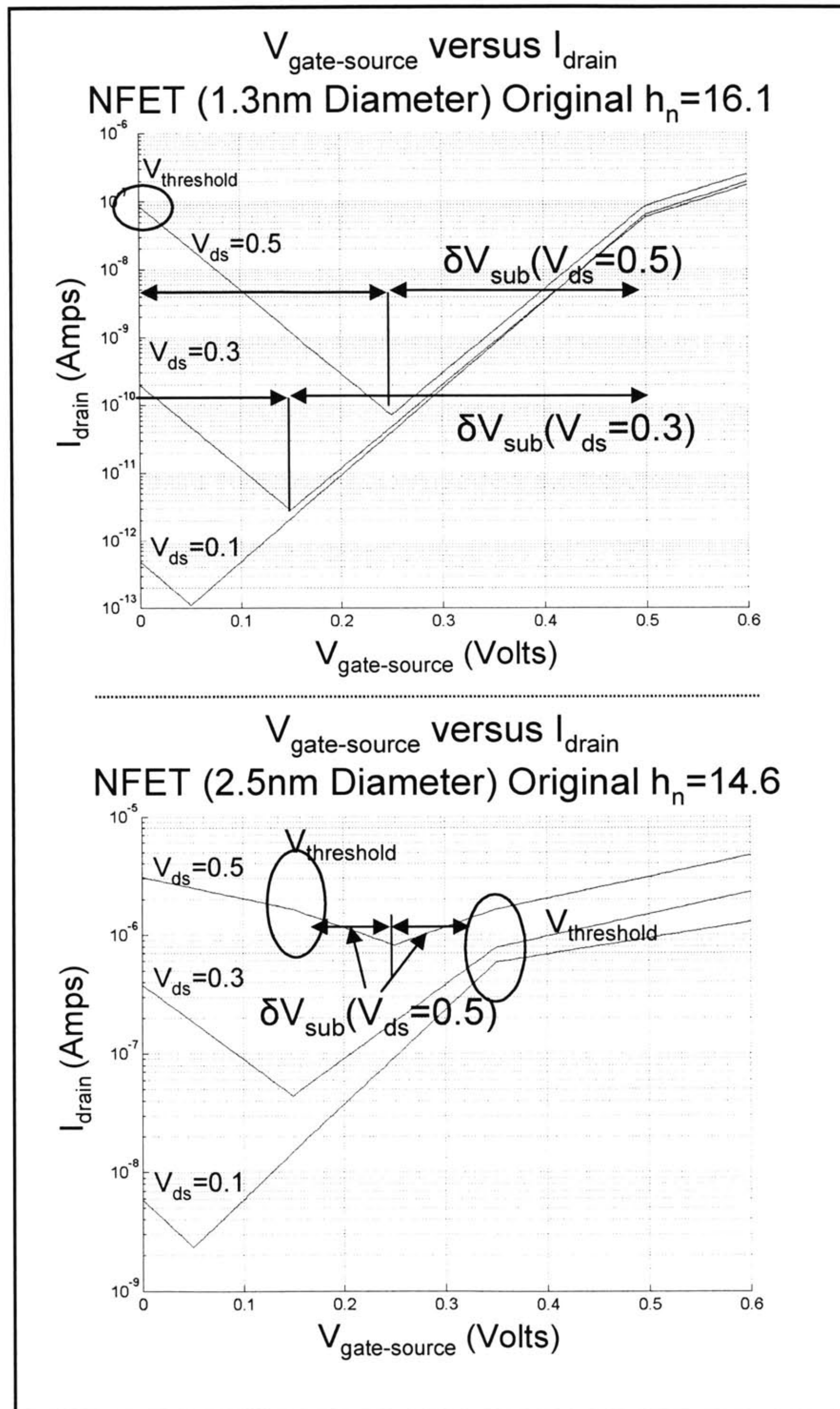


Figure 3-3: Matlab model's I_d versus V_{gs} graphs for diameters of 1.3nm and 2.5nm. Details illustrate the threshold votlages and the δV_{sub} values.

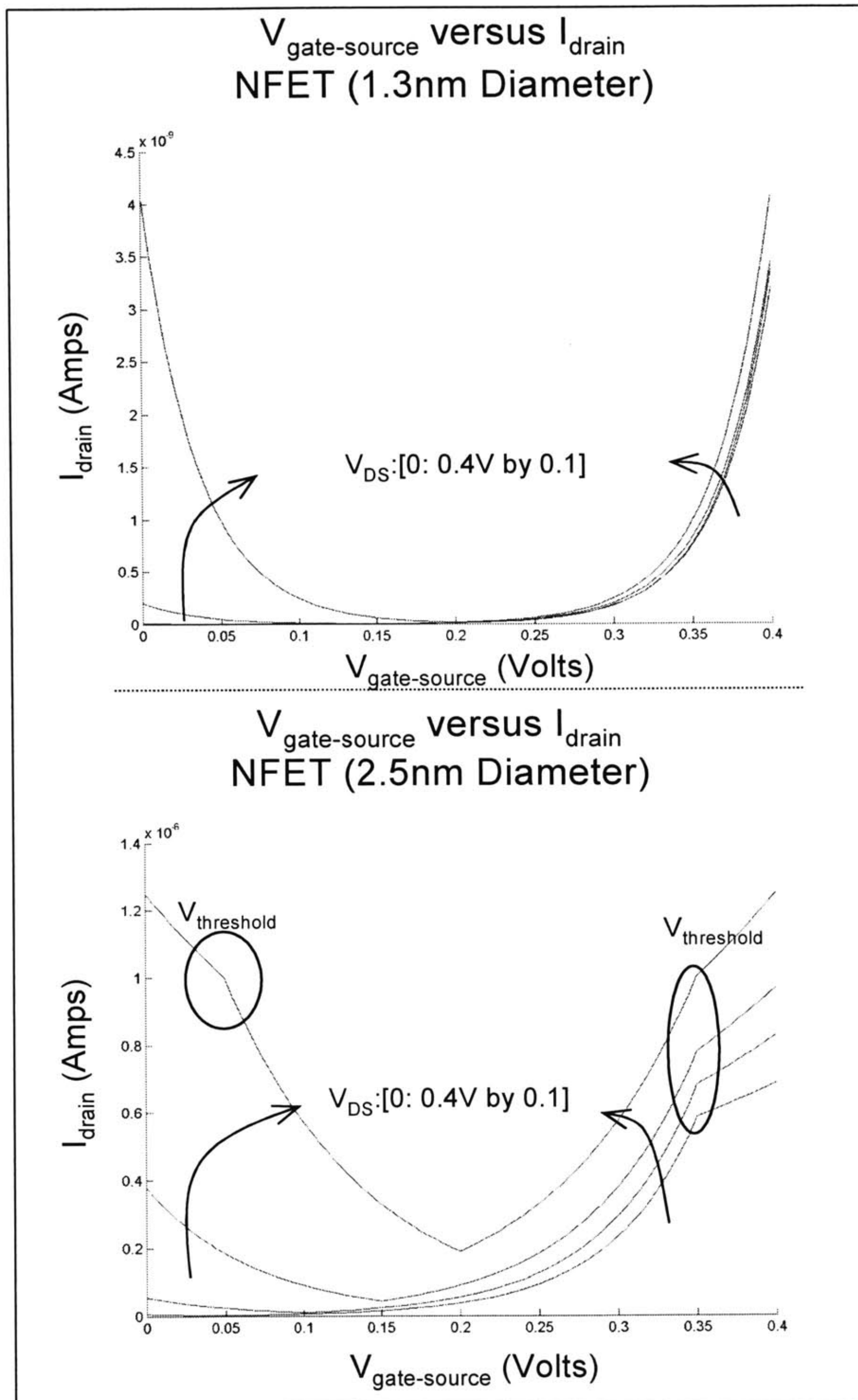


Figure 3-4: Matlab model of I_d versus V_{gs} on a linear-linear plot. The threshold voltage of the larger diameter tubes is visible in the bottom graph. V_{dd}=0.4V

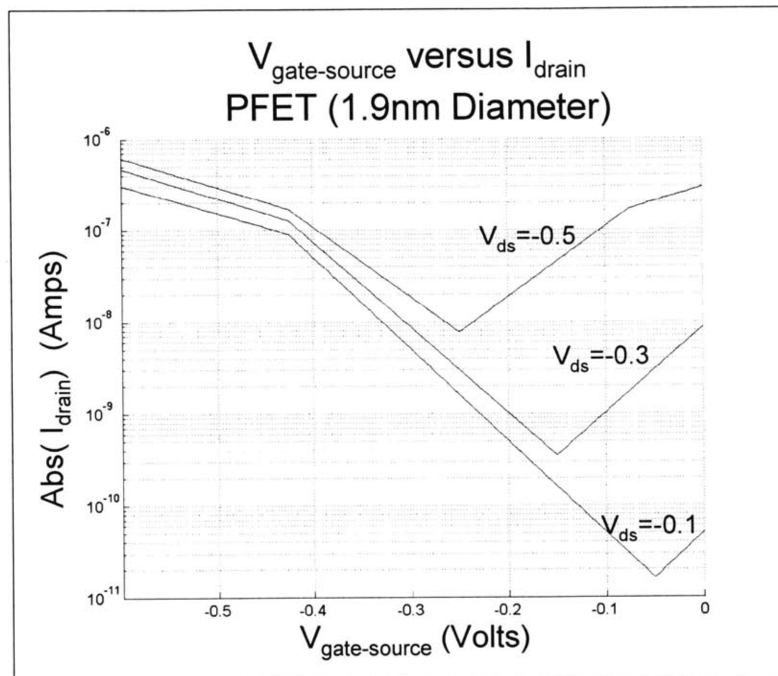


Figure 3-5: Matlab model's absolute value of I_d versus V_{ds} graph for a p-channel transistor with a CNT diameter of 1.9nm. The current is equal to an identically sized n-channel transistor with a negated V_{ds} value.

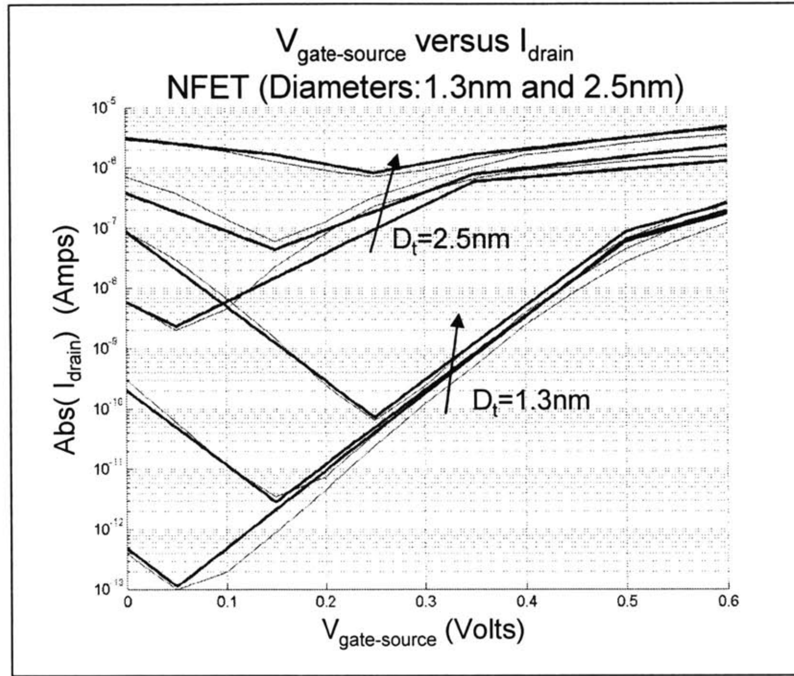


Figure 3-6: The subthreshold model (bold lines) overlayed over the original data.

shows the difference between the original h_n level (given from the IBM data) and a high h_n level for a CNT with a diameter of 1.9nm.

Using the Matlab model, this research will illustrate the circuit differences associated with changing diameter and h_n levels within CNT devices. This research will look at devices around and below the threshold voltage, focusing on subthreshold devices.

3.2.2 Current versus $V_{Drain-Source}$ Model

Using the Matlab model created for this research and shown in the section above, the current versus drain to source voltage can be studied. As was described above, at V_{ds}=0V, the current will suddenly drop to zero. This is not seen in the graphs because, the current model equations do not account for the discontinuity at V_{ds}=0V. However, this discontinuity can easily be accounted for in this research, as described in section 3.3.1. In section 3.3.1, it is stated that if an inverter's NFET and PFET I-V_{out} graphs cross at V_{out} equals V_{dd} or ground, the output voltage for an inverter will be just below or above the power supply rails, respectively.

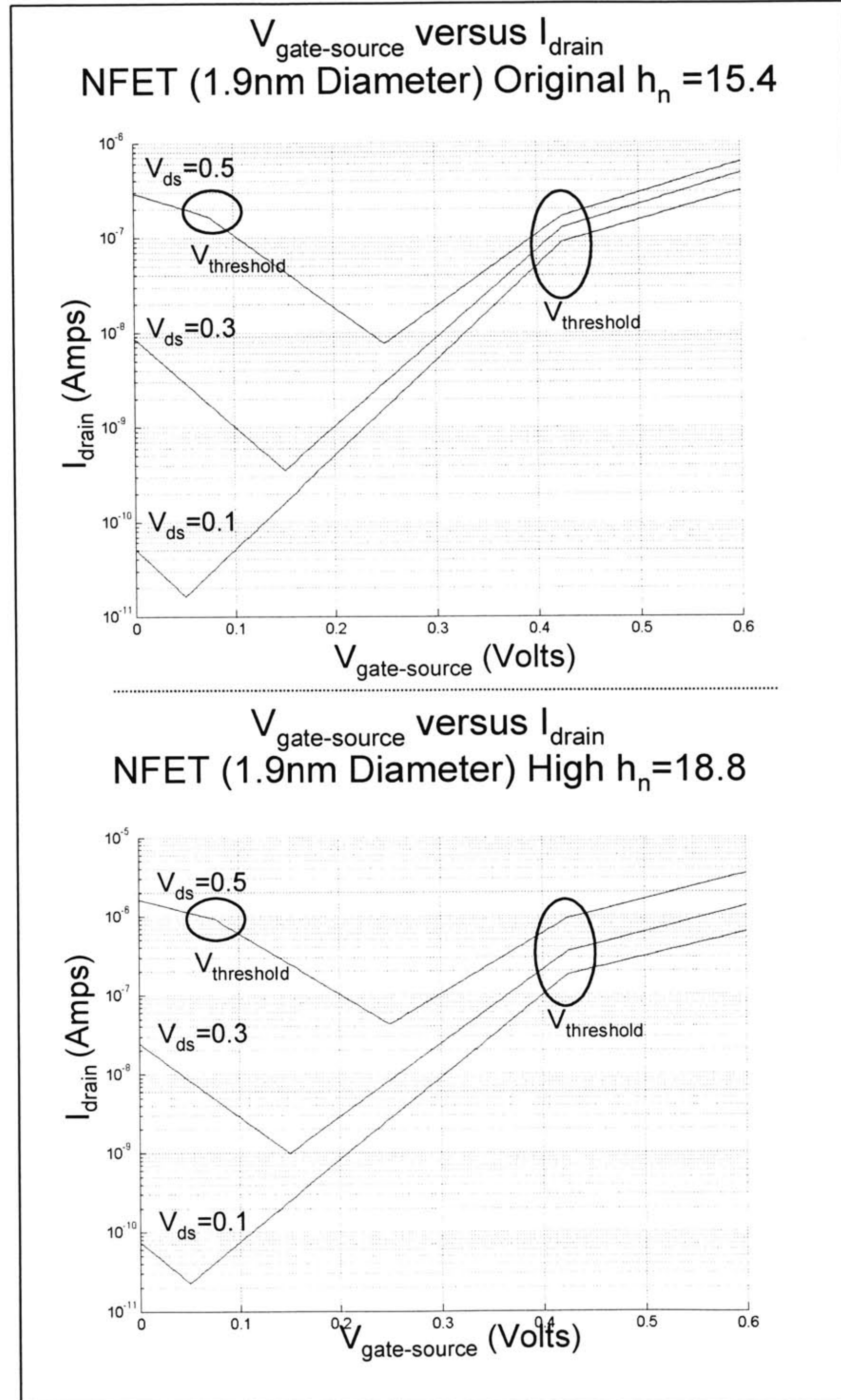


Figure 3-7: Illustration from Matlab model of I_d versus V_{gs} graphs with changing drain control (h_n) values. CNT diameter is 1.9nm.

The I_d versus V_{ds} curves have an interesting crossover illustrated in Figure 3-8. This can be explained by relating the I_d-V_{ds} curves to the I_d-V_{gs} curves. In Figure 3-3, at V_{gs} =0 Volts, there is a large difference between the current for differing V_{ds} curves; this leads to a large I versus V_{ds} slope. If V_{gs}=0.1V is studied on the I_d versus V_{gs} graph, any graph with a $V_{ds} \leq 0.1$V, will have a very little change in current from V_{gs}=0.1V and thus, the slope of the I_d versus V_{ds} graph will be relatively flat; however, once V_{ds}>0.1V, the current increases dramatically with varying V_{ds}. With $V_{ds} \geq \frac{V_{dd}}{2}$, the current levels do not change as drastically and the I_d-V_{ds} graph is relatively flat. In these I_d versus V_{ds} graphs, a changing drain control (h_n) parameter will create a change in the slope for the I_d-V_{ds} curve, as shown in Figures 3-8 and 3-9.

3.3 Inverter

To illustrate and quantify the operation of a subthreshold SB CNTFET in digital circuit design, theoretical inverter structures are simulated out of the Matlab transistor models shown above. Figure 3-10 displays the inverter structure for a complementary CNTFET inverter.

3.3.1 Voltage Transfer Characteristics of an Inverter

To study quantitatively an inverter structure, both transistor's IV characteristics must be closely studied, in terms of the inverter's input and output voltages. If I_d versus V_{out} simulated data, for both inverter transistors, are graphs on the same axis, the output versus input voltage characteristics of the inverter can be obtained. The output voltage is found from the intersection of the PFET and NFET curves with a common V_{in}. If the curves cross near the edge of the supply voltage range, where the current dramatically falls to zero, the model assumes the output voltage to be just below the supply voltage or above the ground voltage; this follows the assumption that the current drops to zero directly at V_{ds}=0. Voltage transfer characteristic (VTC) Curves give a quantitative illustration of the robustness of a digital inverter. Figure 3-11 gives examples of VTC curves for various diameter CNTFETs at V_{dd}= 0.2V, which is below threshold for all devices modeled in this research.

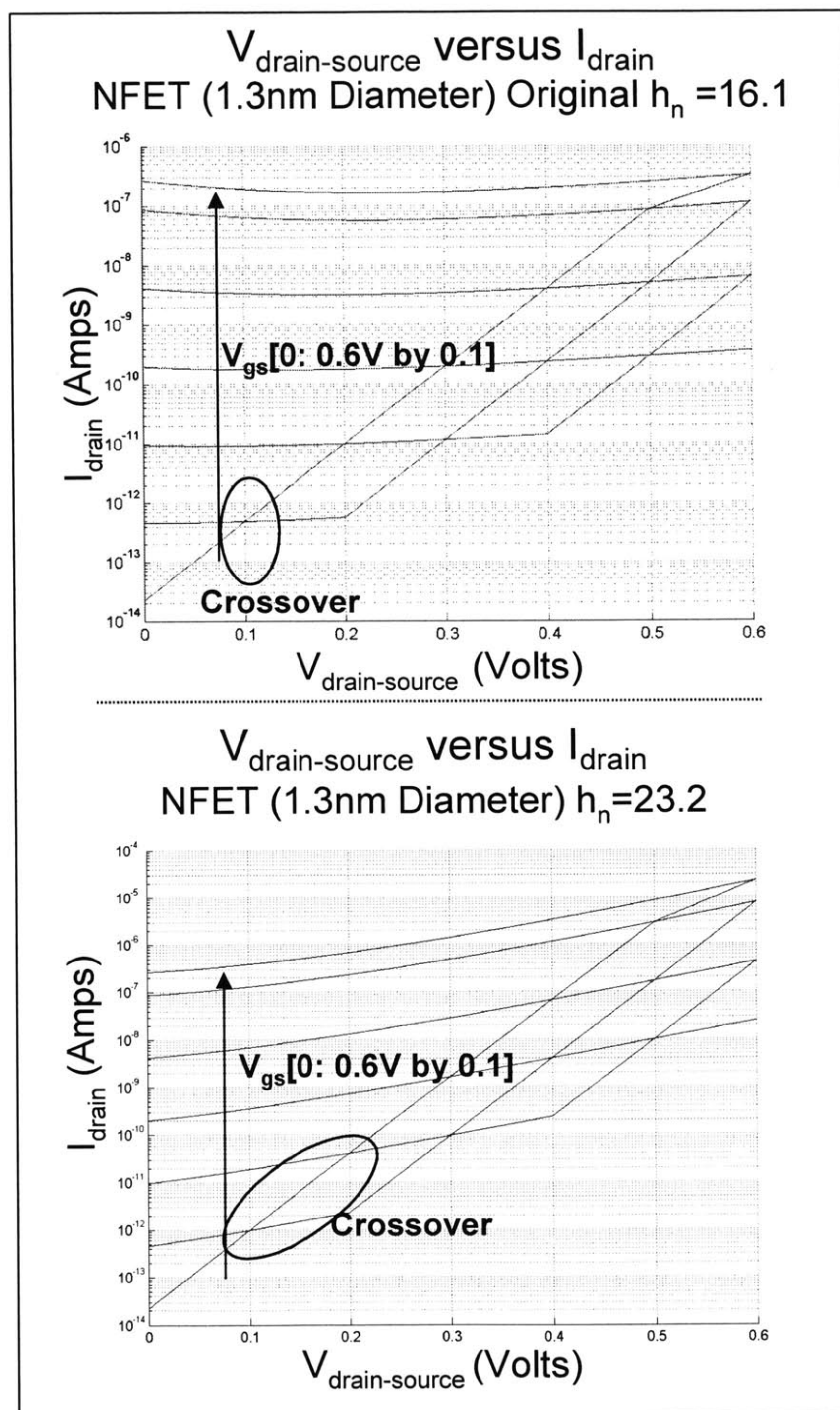


Figure 3-8: Current versus drain to source voltage for a CNTFET with a CNT diameter of 1.3nm and a changing drain control versus gate control level, h_n. Low h_n in the top graph, gives little slope to the high V_{gs} lines. With a higher h_n in the second graph, the lines have a much larger slope.

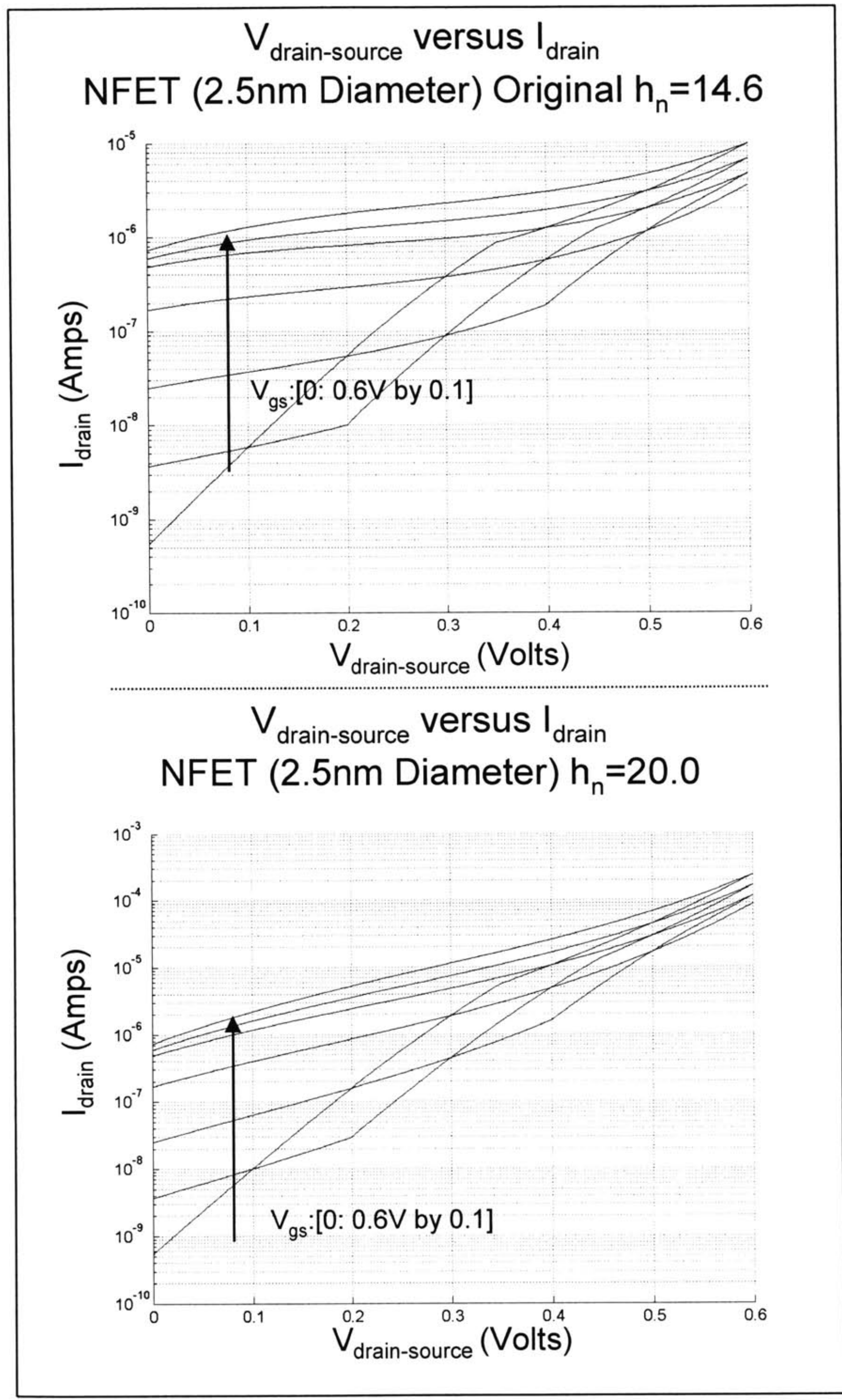


Figure 3-9: I_d versus V_{ds} characteristics for a 2.5nm diameter CNT, in a Matlab modeled CNTFET. The h_n level changes from the top to the bottom graphs: original, $h_n = 14.6$, to high, $h_n = 20.0$, levels respectively.

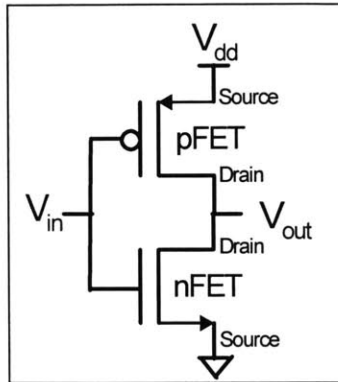


Figure 3-10: Inverter structure composed of both an NFET and a PFET transistor.

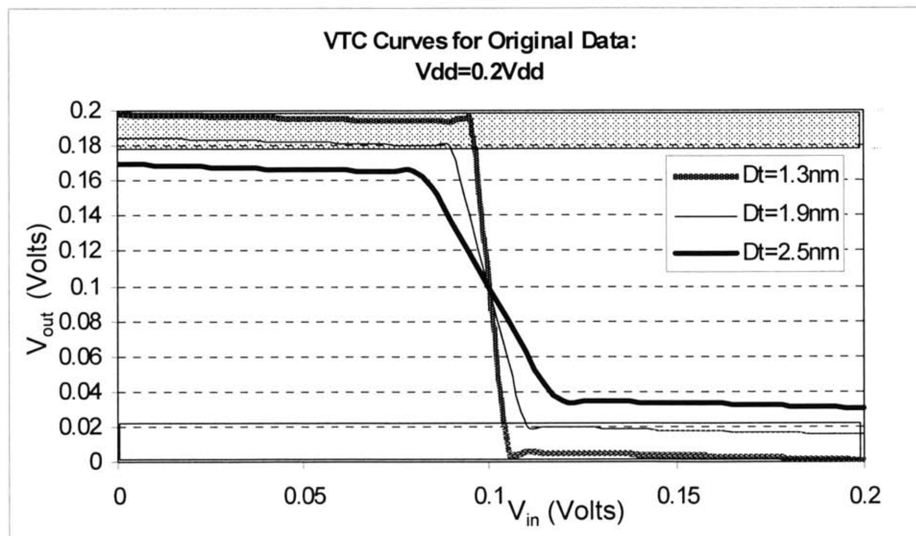


Figure 3-11: The voltage transfer characteristics for various diameter CNT transistors. (D_t= 1.3nm, 1.9nm, and 2.5nm) The shaded area represents less than 10%V_{dd} and more than 90% V_{dd}.

Changing CNTFET Diameter

An inverter's VTC curves change in relation to the diameter of the carbon nanotube channel. It can be noted from Figure 3-11 that as the CNT diameter increases in a CNTFET inverter, the noise margin and voltage swing shrink. This is because of the small E_{gap} and I_{on}:I_{off} in large diameter nanotubes.

In a physical sense, the I_{off} of a large diameter NFET will become more substantial in proportion to the PFET's I_{on}; this will bring down an inverter's 'high' output voltage. For smaller diameter CNTFETs, the same effect occurs, however, the I_{on}:I_{off} ratio is so large, that the increase in NFET off-current does not substantially effect the VTC characteristics. Thus, as the nanotube diameter increases, the I_{on}:I_{off} ratio drops and the voltage swing decreases. Figure 3-12 illustrates an example of high to low output voltage swing for changing CNT diameters.

In Figure 3-11, the CNTFETs with diameters equal to 1.3nm and 1.9nm have impressive voltage transfer characteristics. The noise margins are large and the high and low voltages are above 90% and below 10% of the supply voltage, respectively. For optimum digital circuit implementation of any transistors, an inverter's output voltage should swing at least lower than 10% of V_{dd} and more than 90% of V_{dd}. The VTC curve for the 2.5nm diameter nanotube does not swing beyond 10% and 90% of V_{dd} and the noise margin is smaller. In this case, the large voltage swing of small diameter nanotubes is a trade-off for high on-current and performance of larger diameter nanotubes.

A circuit designer can use the CNT diameter trade-off to benefit and satisfy the general chip level power and performance requirements.

Changing Supply Voltage

Lowering the supply voltage of circuits has a quadratic power savings. In subthreshold MOSFET transistors, lowering the voltage supply will limit the output voltage swing. This is not always the case for the CNT subthreshold FET's model in this research. This fact makes supply voltage scaling theoretically very possible in subthreshold CNTFETs. Figure 3-13, shows the VTC curves of CNTFETs as the V_{dd} is scaled from 0.6V-0.2V. Below 0.2V, the VTC curves remain similar to the V_{dd}=0.2V characteristics.

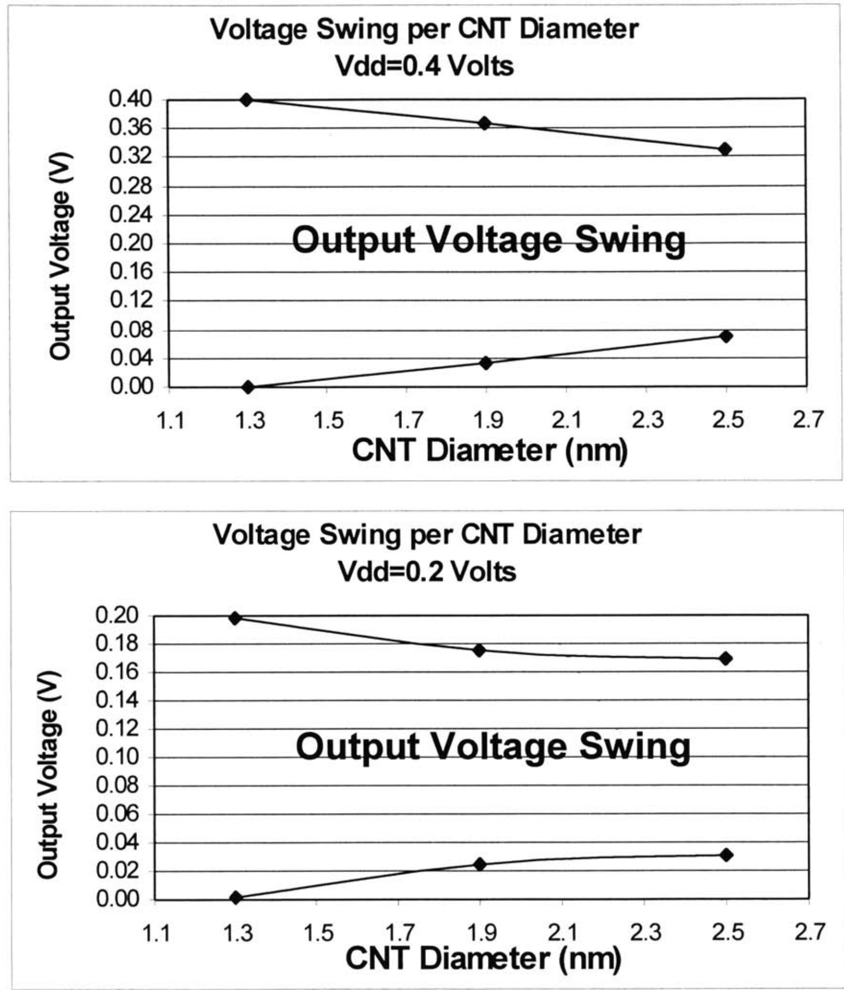


Figure 3-12: High and low limits for the output votlage swing of an inverter versus the CNT diameter, for Vdd=0.4V.

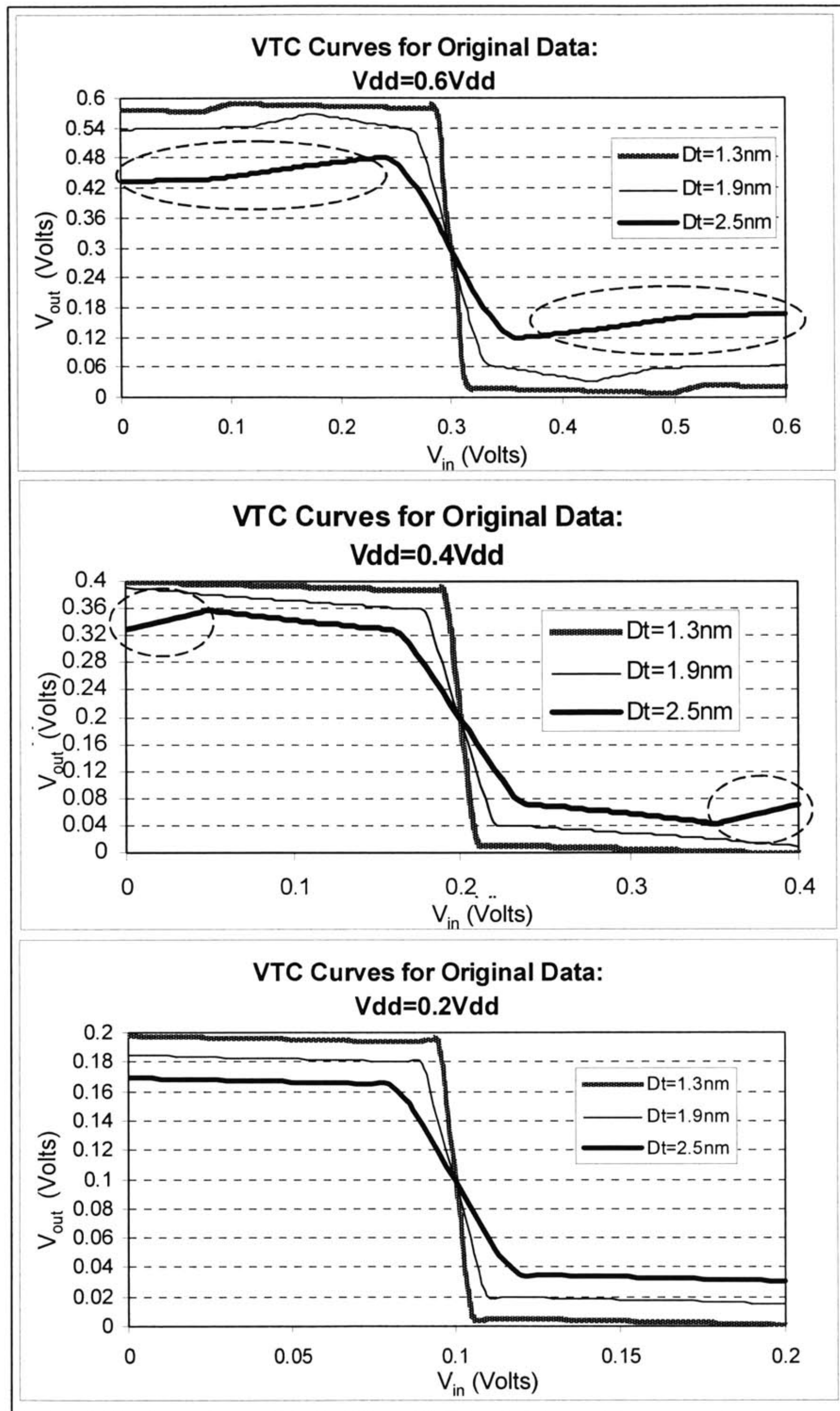


Figure 3-13: Model VTC curves at varying supply voltage levels V_{dd}=[0.6V, 0.4V, 0.2V] As the supply voltage is lowered, CNTFETs continue to keep similar and large voltage swing for various diameter tubes. The dotten circles illustrate the output voltage swing away from the V_{dd} and ground rails with large diameter nanotubes.

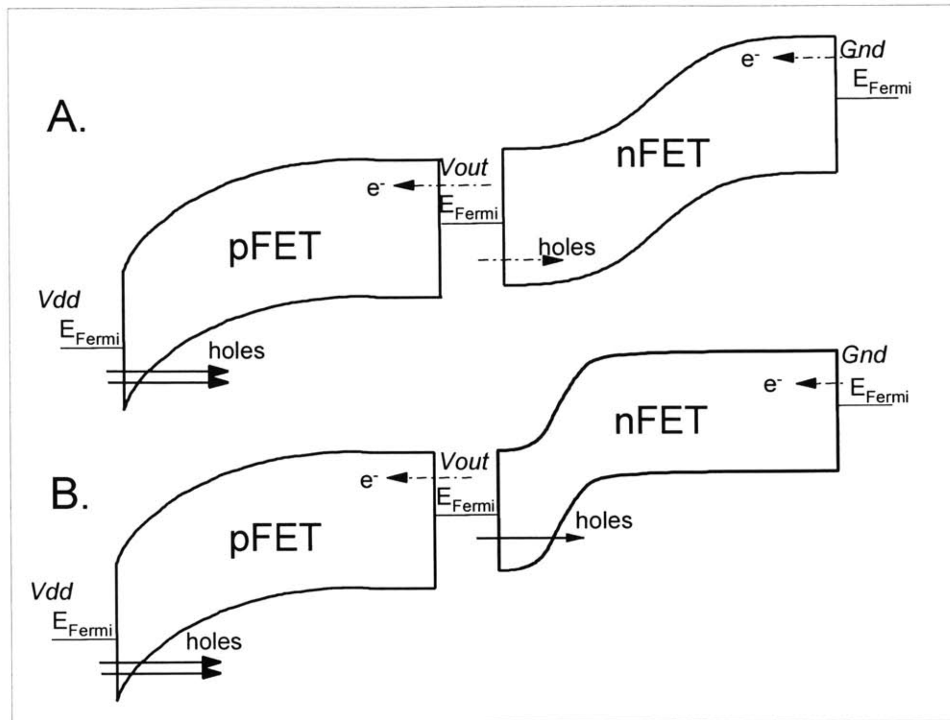


Figure 3-14: The band diagrams in A represent the maximum output voltage state. The NFET current is at a minimum and, therefore, the output voltage is at a maximum. B represents the output voltage when V_{in}=0V; thus, V_{out} is high, but less than V_{out} for case A.

As can be seen from Figure 3-13, for larger diameter CNT devices and with a large V_{dd}, the output voltage swings toward the middle of the supply voltage range, at the edge of the input supply voltage range. This is different from MOSFET devices. This observation is a consequence of the minimum current level existing at $V_{gs}=\frac{V_{ds}}{2}$ and not V_{gs}=0V for CNTFETs. If a zero input voltage is placed on an inverter, the output voltage should rise to approximately the supply voltage (~V_{dd}). The output will be highest when the NFET device has the least current. This minimum current occurs when $V_{gs}=\frac{V_{ds}}{2}$, when the electron and hole currents are minimized and the energy bands are modulated evenly between the source-to-channel and drain-to-channel, as can be seen in Figure 3-14. If the gate voltage is brought to zero volts, the Schottky Barrier for holes decreases in thickness on the NFET and the hole tunneling rate increases, causing an increased current and thus, the output node to drop in voltage.

The effect of a decreasing voltage swing at the end of the input supply range can be shown

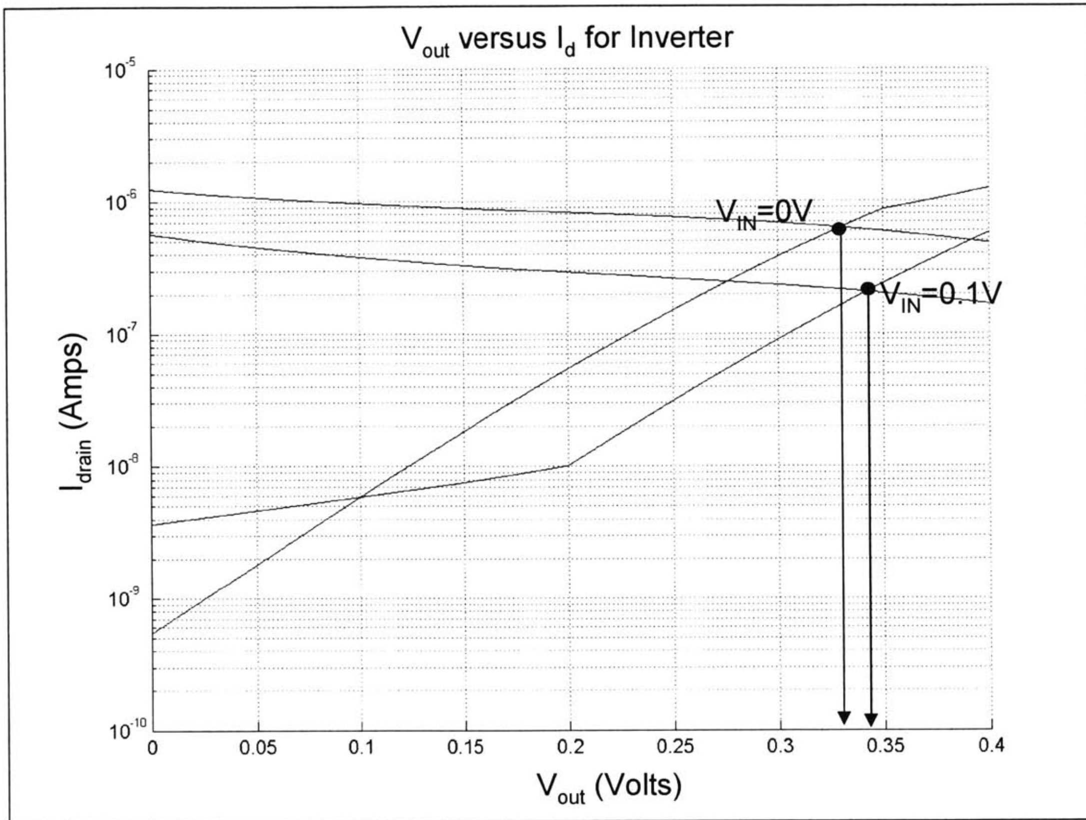


Figure 3-15: V_{out} versus V_{in}, for an inverter structure, can be concluded using the load lines (I_d versus V_{out} curves). Here, V_{out} is found for V_{in}=0V and V_{in}=0.1V.

graphically using the Matlab model. Figure 3-15 illustrates the fact that with a V_{in}=0V, the output voltage is lower than for a larger V_{in}, because of the lower NFET current for a higher V_{in}.

3.4 Process Variations

3.4.1 Varying Nanotube Diameter

Presently, carbon nanotube growth has large process variations. The exact diameter of a nanotube cannot be completely dictated by the growth process. There are even differences in diameters between nanotubes grown within the same batch process. From a circuit designer's perspective, this process variation is hard to account for in design. The difference in nanotube

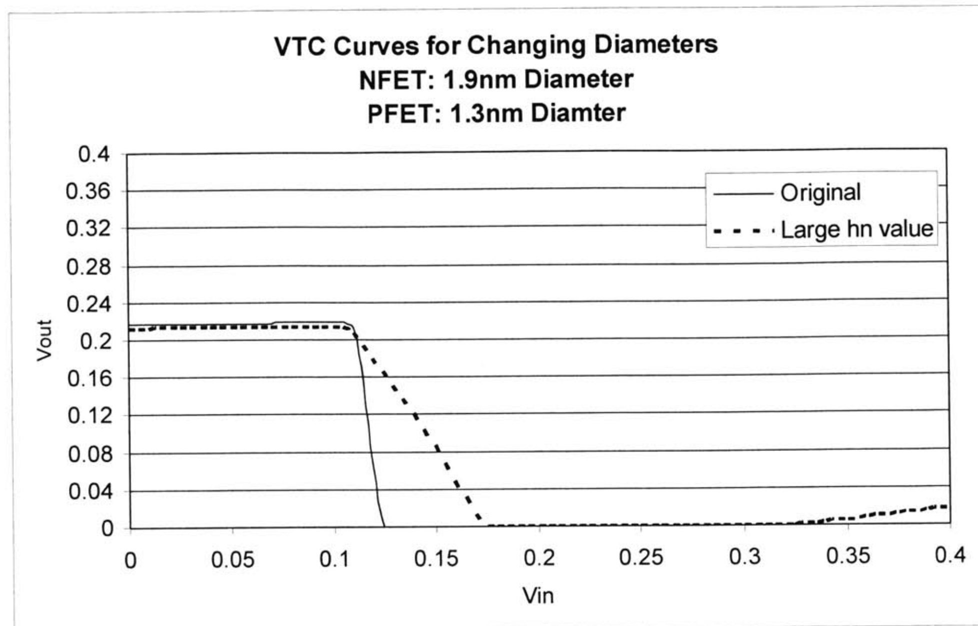


Figure 3-16: When the CNT diameter changes between the two transistors in an inverter, the inverter will not function properly. Here, the VTC curve illustrates the inability of an inverter to pull the output node high.

IV characteristics can change drastically with a small change in diameter as noted previously in this chapter. For example, even metallic nanotubes can be interspersed among semiconducting nanotubes; metallic CNTs cannot be used in CNTFETs. Metallic nanotubes leave a CNTFET ineffective and therefore, they will be neglected in this analysis.

To compare different diameter s-CNTFETs quantitatively, even within the same inverter structure, voltage transfer characteristics (VTC) curves are compared and contrasted. Figure 3-16 shows the VTC curve for an inverter composed of two different diameter transistors, the NFET has a diameter, D_t=1.9nm and the PFET has D_t=1.3nm. The output of the inverter structure never pulls high because the NFETs I_{off} is in the same order of magnitude as the I_{on} for the small diameter PFET. From this result, it is important to realized that, if carbon nanotube circuits are going to be constructed in mass production, the diameter of the nanotubes is going to have to be tightly controlled. If the diameter between nanotubes cannot be completely controlled, it leads to the conclusion that transistors, within a digital circuit structure, should be laid along the length of one nanotube. With all transistors along the same nanotubes, within

a logic circuit, the circuit will have a higher percent of functionality. For example, a complementary NAND gate, should have all 4 transistors along the same nanotubes. The ratio of currents can vary between other NAND gates on other CNTs, however the ratio of currents within a NAND gate will remain relatively the same. If the diameter changes between transistors, in the NAND gate, the off current of the PFETs can exceed the on-current of the NFETs. This design, along one nanotubes, leads to design requirements and large wiring considerations to connect transistors lengthwise.

3.4.2 Changing Drain Control versus Gate Control (h_n)

An increasing drain-control (h_n) level means that the gate to source voltage does not control the subthreshold current completely. A changing h_n level can be a consequence of process variations such as a changing oxide thickness or varying metal contact to nanotube interactions. Both of these variations change the source to gate interaction. The contact to nanotube dictates the current voltage characteristics because, as was described earlier, the intrinsic CNT does not control the current. Presently, the contact to nanotube interactions are variable and change greatly between contacts, even along the length of one CNT. Without control of the h_n level, the output voltage range can vary dramatically between transistors. Compare the VTC Curves in Figure 3-17 to the curves in Figure 3-11. Figure 3-18 compares the changing output voltage ranges for different h_n values as a function of CNT diameter. If there is a difference in h_n within the two transistors of an inverter, the VTC curves can very dramatically. One example is shown in Figure 3-19. Large differences in VTC characteristics and current measurements can be due to small changes in CNT diameter or contacts; these results can affect the circuit design, power, and performance requirements dramatically. Such process variations must be curtailed before mass production can exist for Schottky barrier subthreshold circuits.

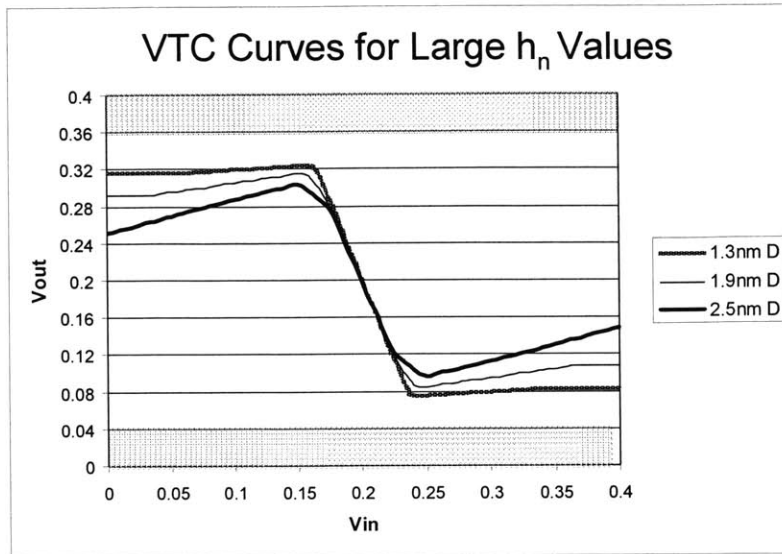


Figure 3-17: With the addition of large h_n values, the output voltage swing will not be more than 10% to 90% of the supply voltage. The larger the tube diameter, the more effect h_n has on the output swing.

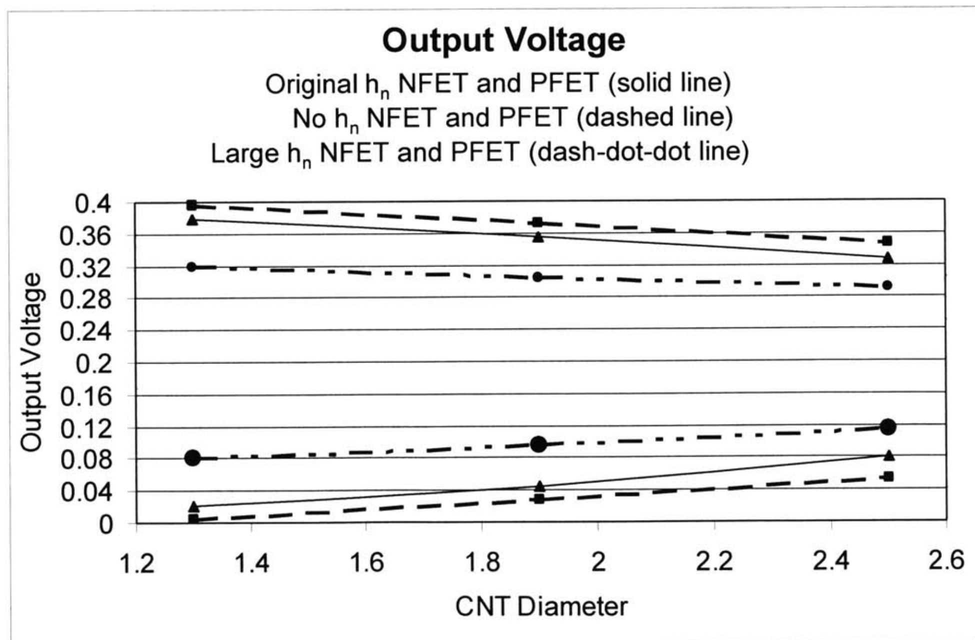


Figure 3-18: The output voltage swing varying by drain-control and carbon nanotube diameter. The more drain-control, the less voltage swing is possible on an inverter's output voltage.

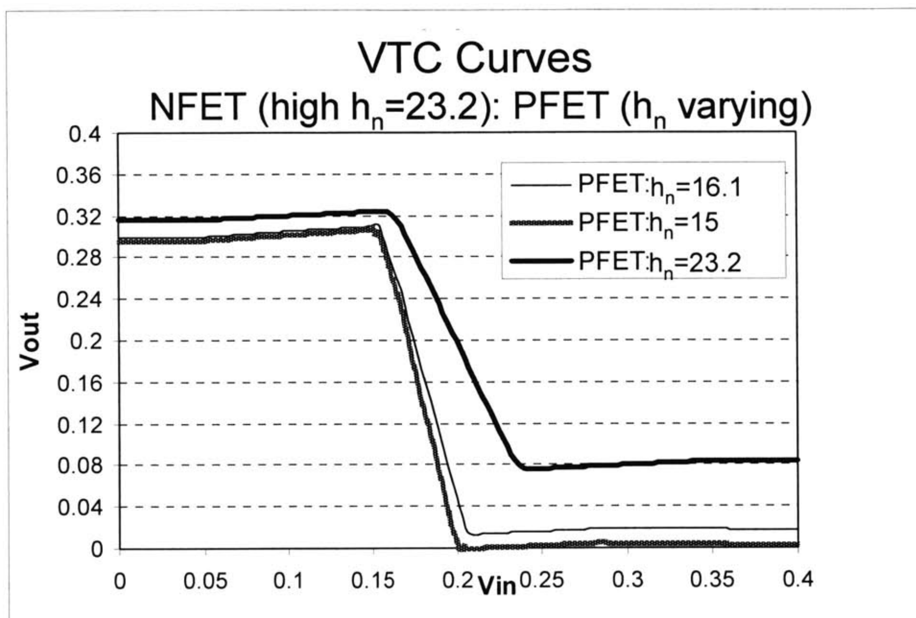


Figure 3-19: A VTC curve, illustrating the potential effect of different h_n levels between the NFET and PFET transistors within an inverter.

Chapter 4

Capacitance, Energy, and Delay of Subthreshold CNTFETs

In this thesis, a model has been created to demonstrate the current and voltage characteristics of subthreshold CNTFETs, along with their applications to inverter structures. This chapter will give a more thorough explanation of carbon nanotube transistors in circuit designs, by studying the capacitance, delay, energy, and power characteristics of subthreshold CNTFETs.

4.0.3 Capacitance

In order to find the delay and energy characteristics of a carbon nanotube FET device, the capacitance of the transistors must be ascertained. The main types of capacitances are the gate capacitance (C_{gate}), the drain to bulk capacitance (C_{db}), the overlap capacitance ($C_{overlap}$), and the Miller capacitance (C_{Miller}). [31]

Gate Capacitance

Looking first at the gate capacitance, a nanotube is grown on a thick silicon dioxide and then surrounded by a thin gate oxide (assumed to be SiO_2 in this research, with $\epsilon_{ox}= 3.9$). A metallic gate rests on the thin oxide, creating a coaxial capacitance structure with the nanotube at the center, shown in A of Figure 4-1; however, because the nanotube lays directly on the bulk oxide, the actual capacitance is described by B in Figure 4-1. Also, the metal gate

extends not just over the nanotube, but over the width of the transistor, which is dictated by the lithographic specifications for minimum metal width and minimum via size. Because of the large metal gate width, the gate to bulk or back-gate capacitance must also be considered.

In the gate capacitance measurements here, the nanotube will be treated as an equipotential metal. The gate capacitance of a MOSFET depends on the existence and size of the conducting channel; therefore, the capacitance depends on the region of operation for the transistor. This is not the case in a CNTFET. The conducting channel of a CNTFET, is the carbon nanotube itself and thus, the channel exists independently of the FET operation. If no current is flowing, which only happens when there is no potential different across the transistor, the channel will be considered an insulator and the gate capacitance will only consist of the parallel plate capacitance from the gate metal to the back gate. However, in any active regime, there will be either off- or on-currents flowing through the carbon nanotube and it can be modeled as a equipotential metal cylinder; in this case, the gate capacitance is composed of both a gate to nanotube and gate to bulk capacitances.

To model the gate capacitance over one nanotube accurately, the quantum capacitance must be taken into account because the nanotube is a not an equipotential cylinder, according to reference [9]. However, as a simplification for this model, the CNT will be considered classically. Treating the CNT classically will give an overestimate for the capacitance In a classical coaxial formation, such as A of Figure 4-1, the capacitance per channel length is $\frac{C_{gate}}{L} = \frac{2\pi * \epsilon_{ox}}{\log(\frac{t_{ox}}{R}+1)}$, if the nanotube is treated as an equipotential. In the case given by B, the gate capacitance is less, however, it is not just described by the percentage of the CNT covered by the gate. As shown in B, of Figure 4-1, the gate has influence on the lower section of the nanotube, not covered by the gate, due to fringe capacitance. However, the fringe capacitance will not be considered in this model. Therefore, the model has an overestimate from treating the nanotube classically and an underestimate from neglecting fringe capacitance. The CNT to bottom silicon plate must also be considered for the gate capacitance measurements, however, is neglected here due to the thick bulk oxide, $T_{ox-bulk}$, and narrow carbon nanotube.

Reference [9] describes the gate to nanotube capacitance in terms of arrays of CNT devices. If nanotubes are placed below a certain pitch, where pitch is defined as the distance between the center of two nanotubes, screening between nanotubes will become important for capacitance

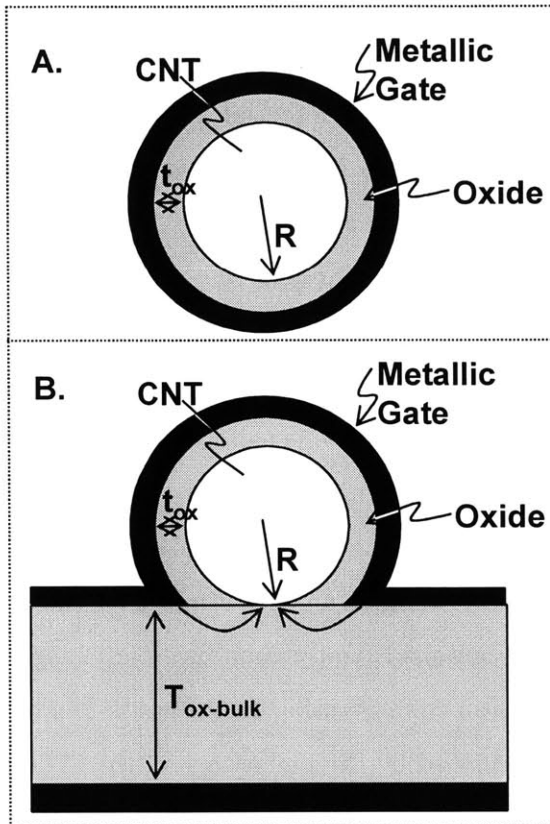


Figure 4-1: The capacitance of a CNTFET is modeled as a cylinder with an oxide and cylindrical gate. However, when a CNT is placed on a thick bulk oxide, the capacitance model must change. B contains fringe capacitance.

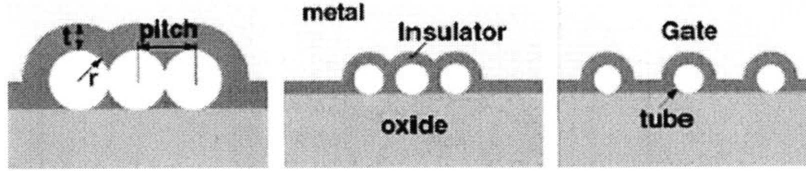


Figure 4-2: An illustration of a carbon nanotube arrays with varying pitch. This research assumes that the nanotubes are more than 2*(R+t_{oxide}) apart, to eliminate capacitance coupling between devices. From [9]

measurements. The point where screening becomes an issue is at a pitch of $2(t_{ox} + R)$, where R is the CNT radius and t_{ox} is the thickness of the SiO_2 gate oxide; see Figure 4-2 for an explanation. The gate to CNT coupling capacitance is stronger for the edge nanotubes, so the general capacitance in [9] is given for the middle nanotubes within an array. In this research, the pitch between nanotubes will be greater than $2(t_{ox} + R)$.

Figure 4-3 gives data for the gate to nanotube capacitance per channel length for one nanotube in the middle of an array, versus the pitch between the array of nanotubes. To simplify the capacitive calculations in this research, the capacitance of B in Figure 4-1 is used, which is less than the actual capacitance due to the extra fringe capacitance. $(\frac{C_{gate-partial}}{L} = \frac{2\theta+\pi}{2\pi} * \frac{C_{gate-channel}}{L})\}$ where $2\theta + \pi$ represents the angle of the CNT cylinder covered by the metallic gate $(\theta = \arcsin(\frac{1}{1+\frac{t_{ox}}{R}}))$. See Figure 4-4. The difference between the capacitance model in this research and the IBM data found by FIELDAY [9] is given in Figure 4-5. The partially covered cylindrical capacitance will be used in this research, however, this is an underestimate of the capacitance. The model assumes that screening between nanotubes is not a true consideration because the $pitch \geq 2(R + T_{ox})$.

The gate capacitance per channel length for one nanotube has been described above. The actual value of the capacitance differs depending on the channel length. The channel length and metal gate width are considered to be controlled by the metal pitch needed for the gate, source, and drain contacts in future generations, according to the 2003 ITRS Roadmap.[10] An illustration of a transistor is in Figure 4-6. All future gate capacitance calculations will include the gate to nanotube capacitance for one nanotube, unless otherwise specified, and the gate to bulk capacitance. The two gate capacitances are shown in Figure 4-7 for a variety of diameter

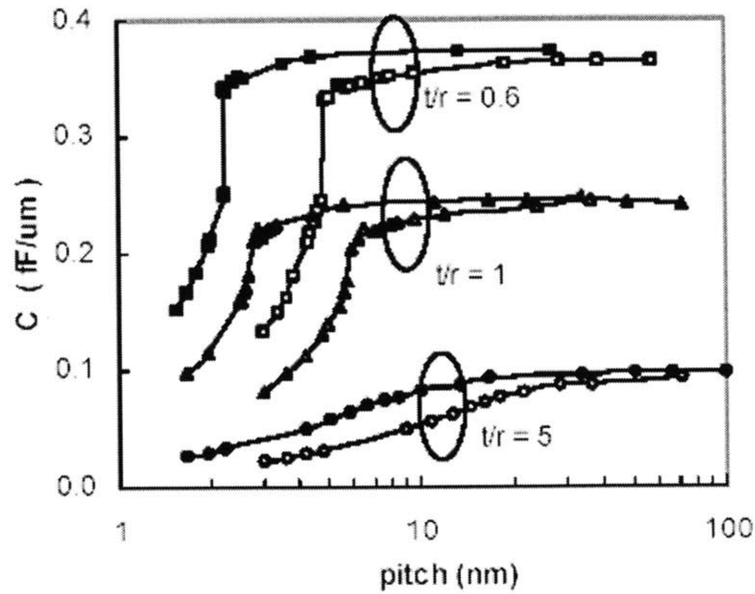


Figure 4-3: The C_{gate} (for a nanotube in the middle of an array of parrallel tubes) versus the pitch. The solid symbols represent r=0.7nm and the open symbols are for r=1.5nm, where r is the CNT radius and t is the oxide thickness.[9]

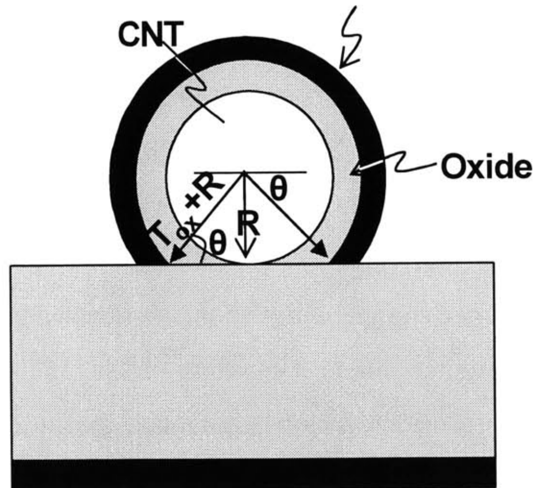


Figure 4-4: To model the capacitance of a CNTFET, that is partially covered by a metallic top gate, the percentage of the nanotube circumference covered by the gate must be found.

T_{ox}/R	C_{gate}/Length from IBM Data		Modeled C_{gate}/Length	
	R=1.5nm	**R=0.7nm**	**A: coaxial cylinder**	**B: partial covered cylinder**
5	0.094 fF/um	0.1 fF/um	0.121 fF/um	0.067 fF/um
1	0.244 fF/um	0.25 fF/um	0.313 fF/um	0.209 fF/um
0.6	0.363 fF/um	0.375 fF/um	0.462 fF/um	0.330 fF/um

Figure 4-5: The table above illustrates the modeled capacitance measurements for this research compared to those given in citation [9].

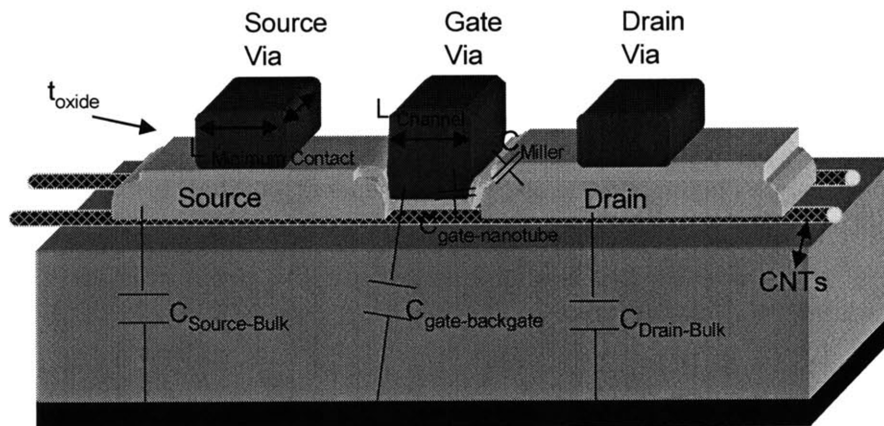


Figure 4-6: A CNTFET channel length is dictated by the gate via contact dimensions. The drain and source vias are dictated by the same constraints. The $C_{drain-bulk}$, $C_{gate-backgate}$, $C_{gate-nanotube}$, C_{miller}, and $C_{source-bulk}$ are shown in the diagram.

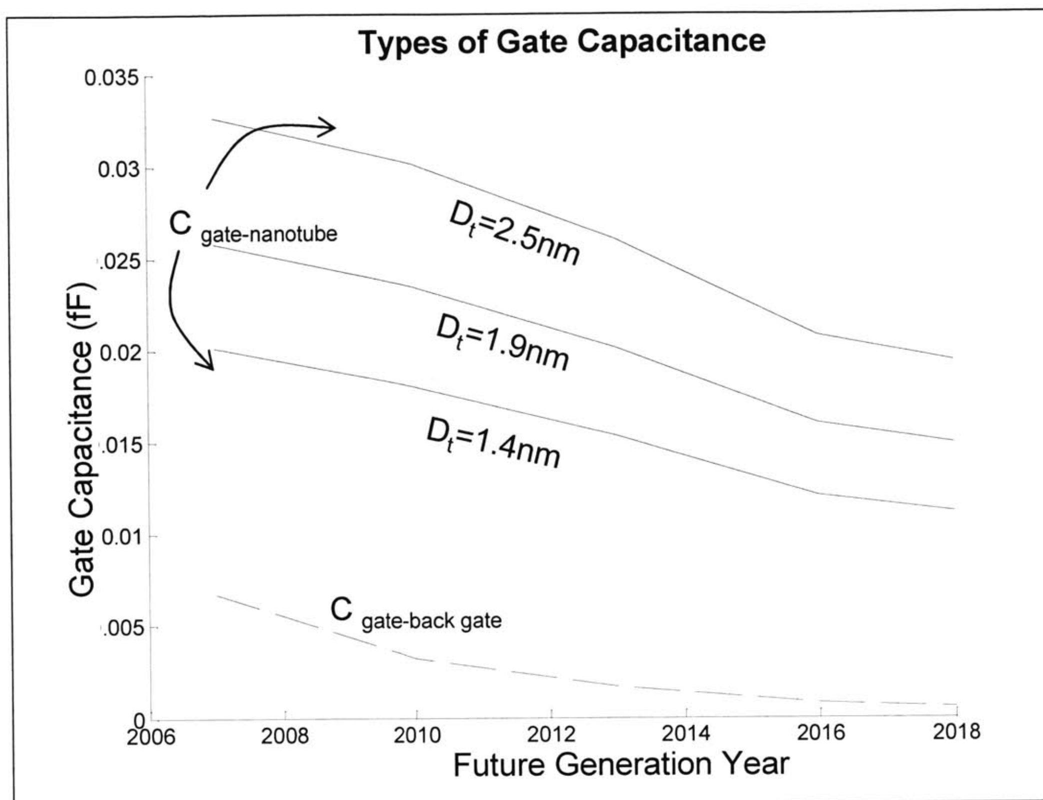


Figure 4-7: The gate capacitance consists of both the metal gate to backgate and the metal gate to nanotube capacitances. The gate to nanotube capacitance depends on the nanotube diameter. Here the two types of gate capacitances are graphed versus the future lithographic generations for multiple nanotube diameters (D_t). The backgate oxide thickness is 100nm, compared to the gate oxide thickness of [1.1, 0.8, 0.65, 0.55, 0.5] for years [2007, 2010, 2013, 2016, 2018] respectively. The channel lengths are dependent on the ITRS Roadmap's lithographic specifications.

nanotubes.

Parasitic Drain Capacitances

The total gate capacitance is dependent on the number of tubes in an array under one metallic gate and the lithographic dimensions of the gate to the back gate. In contrast, the parasitic drain capacitance is not dependent on the number of nanotubes, but only on the metal lithographic dimensions. The overlap capacitance between the drain and gate ($C_{overlap}$) depends on the width of the metal gate and drain, along with the length of the gate/drain overlap.

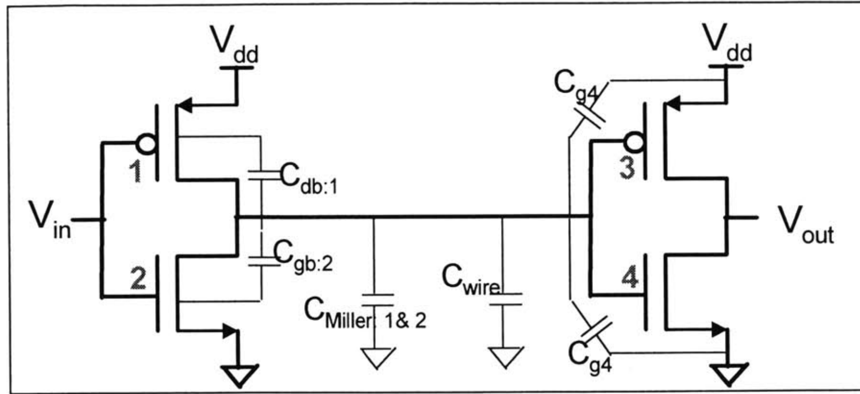


Figure 4-8: The load capacitance of an inverter chain depends on the Miller capacitance, the wire capacitance, the drain to bulk capacitance of the driving transistors (Transistors: 1 & 2), and the gate capacitances of the driven transistors (Transistors: 3 & 4).

Looking into an inverter from the output node, the overlap capacitance can be replaced by a Miller capacitance from the output node to ground. Considering the Miller effect, the Miller capacitance is double the $C_{overlap}$ ($C_{Miller} = 2*C_{overlap}$). [31]

Along with the Miller capacitance associated with the drain, there is a drain to bulk capacitance (C_{db}) that exists between the metal drain contact and the bulk back gate. Though the bulk oxide is thick, and thus, limits the capacitance per area, the area of the metal contacts is dictated entirely by the lithographic dimensions and is relatively large.

The load capacitance (C_L) of an inverter structure, associated with the drain contact, is therefore made from the combination of C_{db}, C_{Miller}, and C_{wire}, plus the input gate capacitances (C_g) of the driven gates. See Figure 4-8 for a diagram of the capacitances.

Capacitance in Relation to Lithography

The capacitance is greatly effected by the lithograph dimensions. The dimensions of metal contacts are much larger than the radii of a carbon nanotubes and the t_{ox} of a gate. The minimum metal dimensions will control the contact sizes, the necessary gate overlap, and the width between the metallic gate, and the metal source/drain contacts. Contrary to CMOS poly gates, a metallic gate has much less resistance, however, the scaling relies on metal dimensions. Thus, many parallel nanotubes can be placed under a metallic gate, source, and drain contact

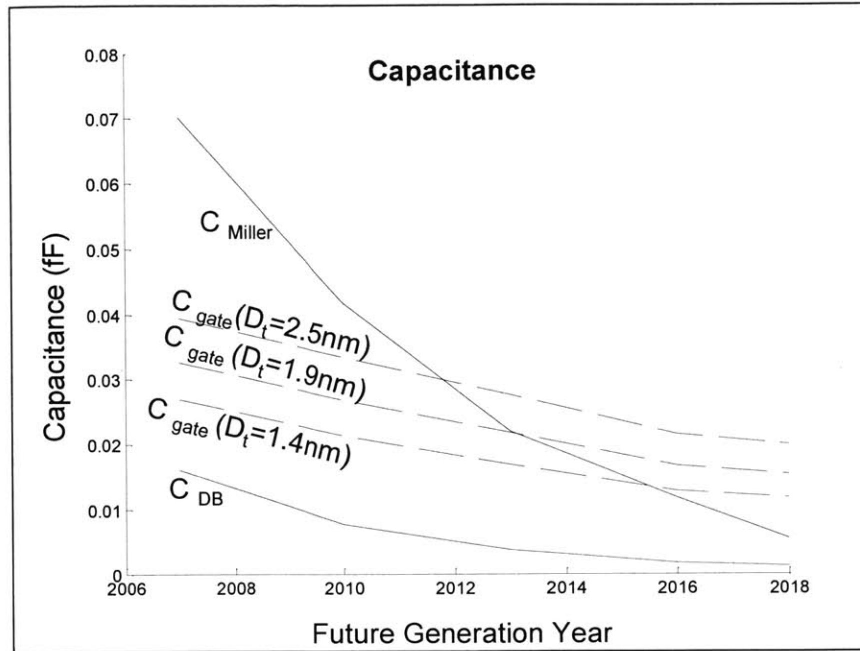


Figure 4-9: As the years increase, the lithographic dimensions are decreasing according to the 2003 ITRS roadmap [10]. The Miller capacitance scales dramatically with lithography because it depends on both the width and the length of the contacts and the gate overlap. The gate capacitance mainly depends on the channel length. The drain to bulk capacitance depends on the metal via scaling.

without increasing the minimum metal contact or gate sizes. Also, the channel length of a CNTFET will not be limited by the carbon nanotube, but instead by the metal minimum lithographic pitch between the source, drain, and gate vias and contacts.

The lithographic dimensions effect the capacitance by the following: the gate capacitance depends on the number and the diameter of the CNTs and to a lesser extent, the width and length of the channel in comparison to the back gate. The overlap capacitance depends on both the width and the length of the overlap and thus, scales quadratically as the generation scales. Figure 4-9 illustrates the scaling of the various capacitances depending on generation year according to the ITRS 2003 Roadmap. [10]

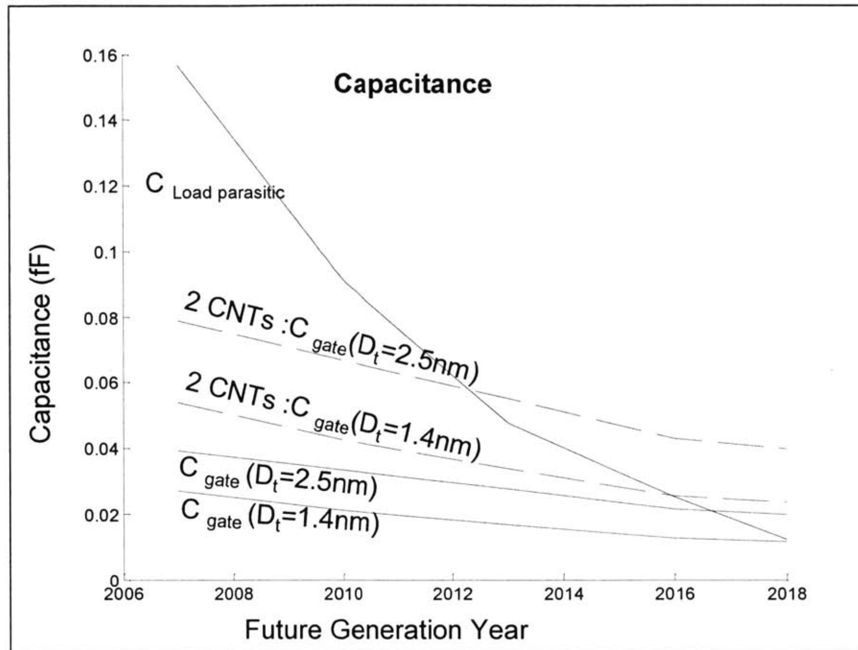


Figure 4-10: The gate capacitance is smaller than the load capacitance of a CNTFET, especially with small diameter CNTs. However, the gate capacitance doubles if the number of carbon nanotubes per metal gate doubles; yet, the parasitic load capacitance remains constant; independent of the number of nanotubes.

Self Loading

It can be seen from Figures 4-9 and 4-10 that when the lithographic dimensions are large, the drain parasitic capacitance will out weigh the gate capacitance in an FET; this gate capacitance is an underestimate, but if we take an overestimate by using a coaxial cable such as A in Figure 4-1, the relative capacitance will be similar, see Figure 4-11. This will lead to self loading problems in circuit design, unless multiple nanotubes per metallic gate are used. Self loading becomes a problem when the parasitic capacitance dominates over extrinsic fanout capacitance. If two CNTFETs, with different contacts, are placed in parallel; because the time delay is equal to $\tau = RC$, the resistance would drop by 2, however, the capacitance would increase by two, thus, keeping τ constant, see Figure 4-10 for the ratio of parasitic and extrinsic capacitances. The gate capacitance will increase greatly if multiple nanotubes per contact are used.

For a set of series inverters, as shown in Figure 4-8, the extrinsic gate capacitance of the

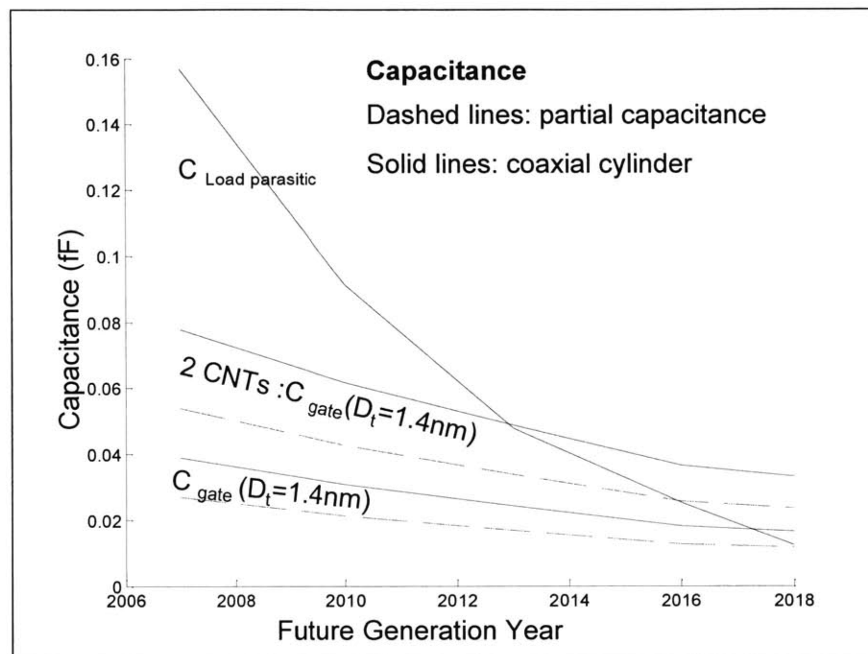


Figure 4-11: The partial capacitance is an underestimate of the total gate capacitance because the fringe capacitance was neglected, however, the solid lines represent a coaxial formation that is an overestimate. The same results occur in the overestimate as in 4-10.

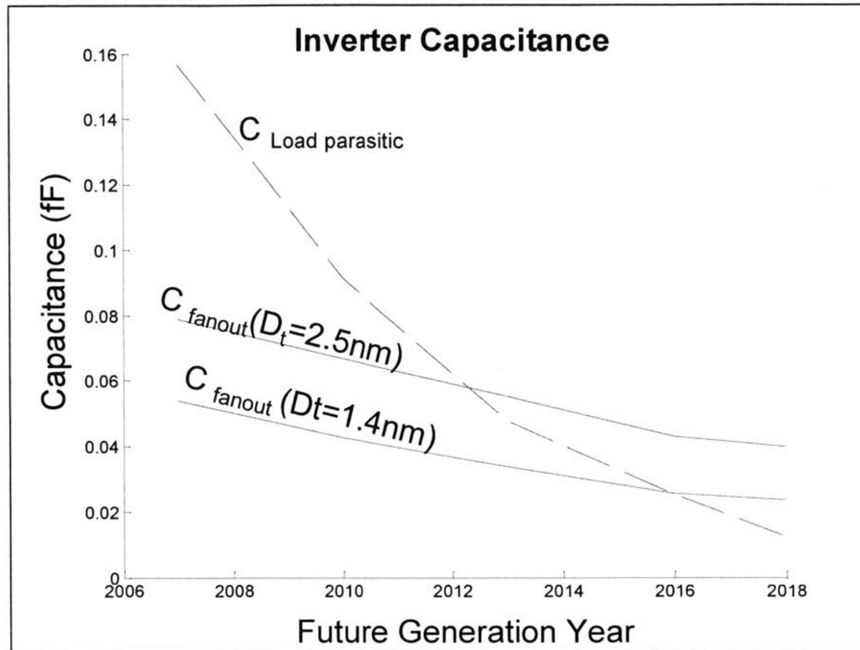


Figure 4-12: The parasitic load capacitance of a driving inverter is much larger than the extrinsic fanout capacitance in near term generations. This can lead to self loading if multiple nanotubes per gate are not used. However, as lithography scales down, the parasitic capacitance is dropping dramatically and self loading will become less of a problem.

driven inverter and the intrinsic capacitance of the driving inverter are shown relative to each other in the graph in Figure 4-12.

4.0.4 Delay

With the capacitance of inverter structures known, the time delay (T_{delay}) of an inverter can be found from $T_{delay} = C_L * \frac{\Delta V}{Iaverage}$, where $\Delta V = \frac{V_{dd}}{2}$.[31] It was shown above that the capacitance in the near term relies heavily on the parasitic drain and Miller capacitances, which are independent of the number of CNTs per gate or the nanotube diameter. Thus, a transistors time delay is dependent on the transistors average current ($I_{average}$). When considering an inverter, if the V_{in}=0V, then the PFET will pull the output node high. $I_{average}$ for this case is the average between $I(V_{ds}=V_{dd})$ and $I(V_{ds}=\frac{V_{dd}}{2})$. Graph in Figure 4-13 illustrates the $I_{average}$ for the PFET transistors considering a changing diameter and changing h_n level. As previously described, the average on-current increases with diameter and drain control.

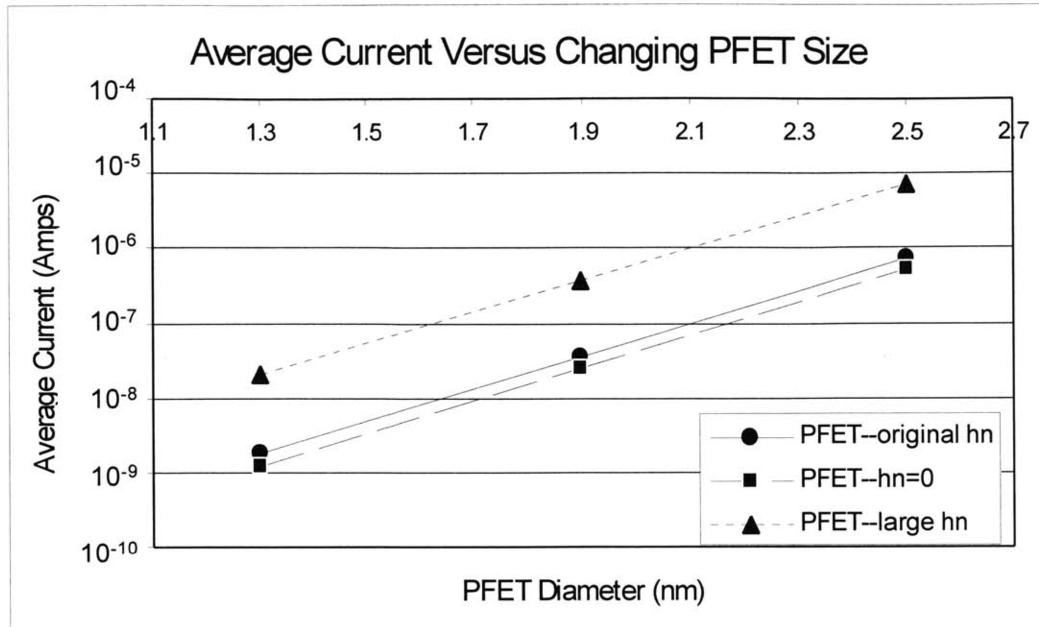


Figure 4-13: Average current versus changing PFET diameter and h_n level.

Therefore, with the average current and capacitance known, the time delay can be found. Figure 4-14 demonstrates the time delay for an inverter circuit pulling up using the original h_n values. Also, the capacitance scales with contact feature size; Figure 4-14 illustrates the time delay decreasing with lithographic and therefore load capacitance scaling. The time delay decreases with increasing nanotube diameter; however, this increase in performance comes as a trade-off to the high/low voltage swing as shown in Figure 3-12.

4.0.5 Conclusion

In conclusion, the diameter of a CNT transistor can be used as a trade-off for performance, energy, and voltage swing. These trade-offs can be used to a circuit designer's advantage. If high performance is required for a circuit structure, larger nanotubes can be implemented with the knowledge and understanding that the noise margin and high/low output voltage swing will be low.

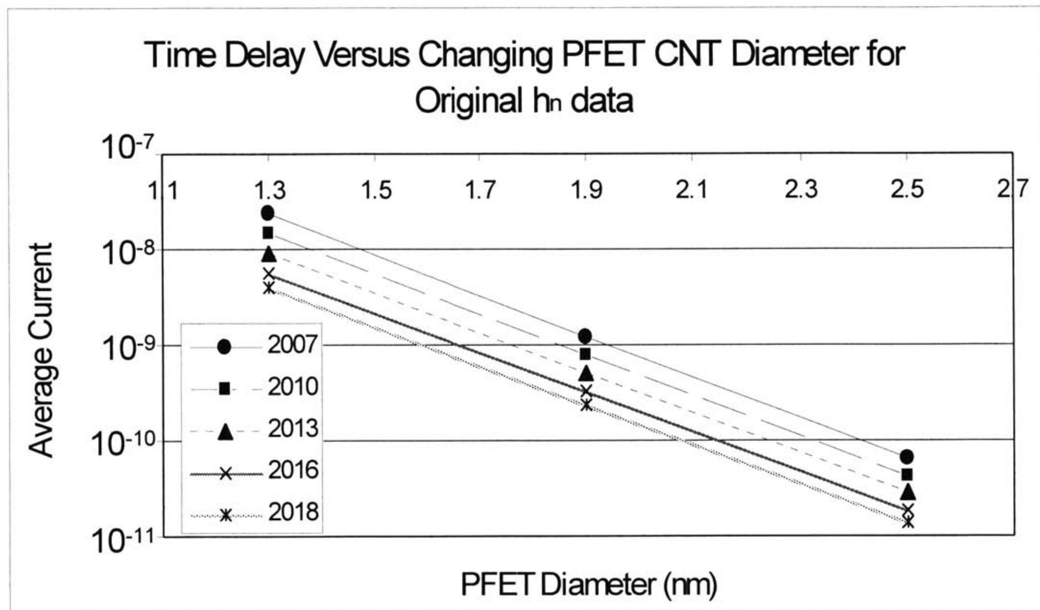


Figure 4-14: Model of time delay for a PFET, with the original h_n value, versus the CNT diameter and the lithographic scaling by year (determined from [10])

Chapter 5

Above Threshold Model

This thesis research has carefully considered carbon nanotube field effect transistors in the subthreshold regime and their applications to an inverter structure. This chapter will model and characterize CNTFET devices above threshold, in both the triode and saturation regimes. IBM has generously given data for a carbon nanotube transistor in these two regime, focusing on the triode regime. [11]

Figure 5-1 shows the IBM data of a CNTFET above threshold. The IBM data here and in the subthreshold chapter are not for the same transistor devices; the device characteristics do not match perfectly. Figure 5-1 is a CNTFET's I_d versus V_{ds} curve; it resembles the IV characteristics for a MOSFET in the triode regime. Just as with MOSFETs, the triode and saturation regions of CNTFETs are dependent on the source voltage in respect to both the drain and gate voltages.

5.0.6 Linear Regime

At the threshold voltage of a transistor, the subthreshold regime ends and the CNTFET enters the linear or triode regime. Here, the Schottky Barrier(SB), at the source end of the transistor does not change in thickness with a varying gate voltage. Instead the tunneling current is controlled by the drain SB barrier. As the drain to source voltage increases, the drain SB shrinks and the current increases linearly.

Data from the linear, or triode, regime is shown in detail in Figure 5-2; trend lines have been added to the IBM data to show the linearity. Within the linear regime, the current increases

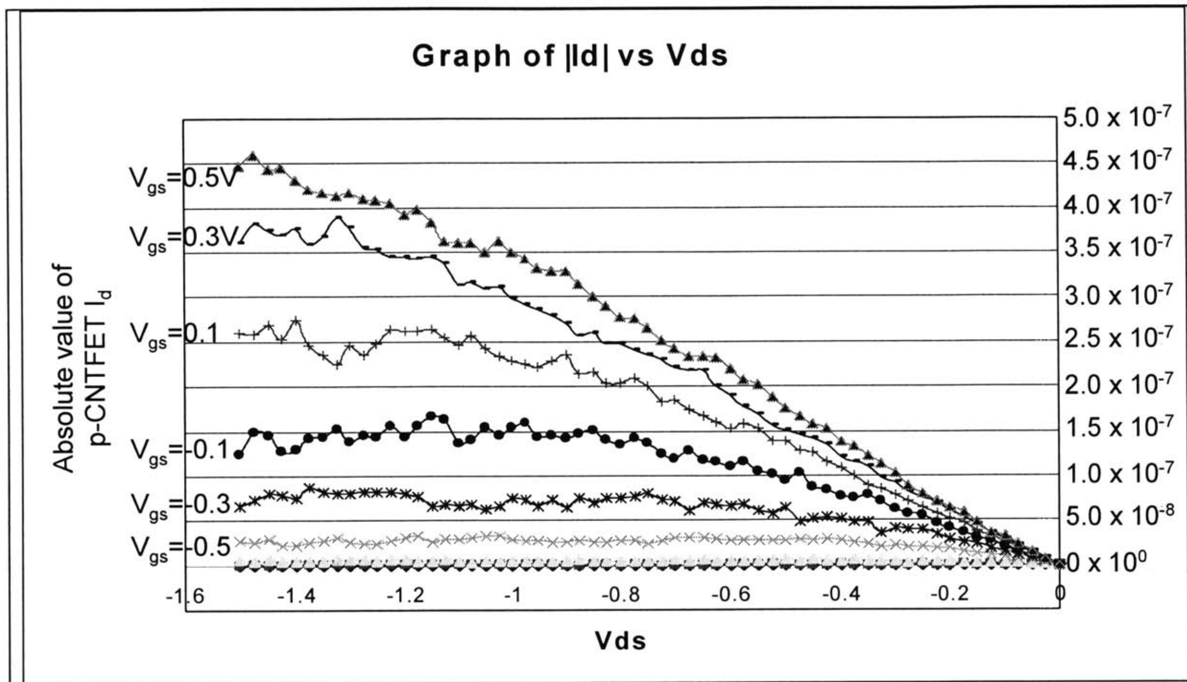


Figure 5-1: Graph of a PFET's measured I_d versus V_{ds} for varying V_{gs}[-0.5V: 0.5V]. Data courtisy of [11].

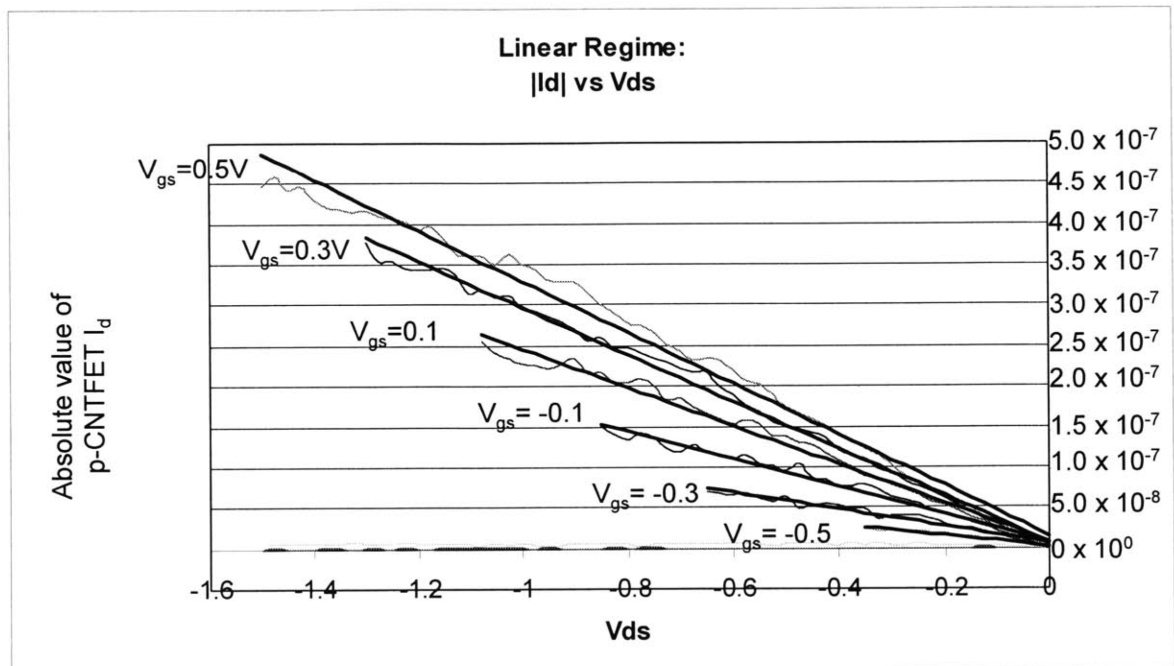


Figure 5-2: Graph of I_d versus V_{ds} for a CNTFET's linear regime, data curtisy of IBM. Placed atop the data are trend lines to show the linearity of the data.

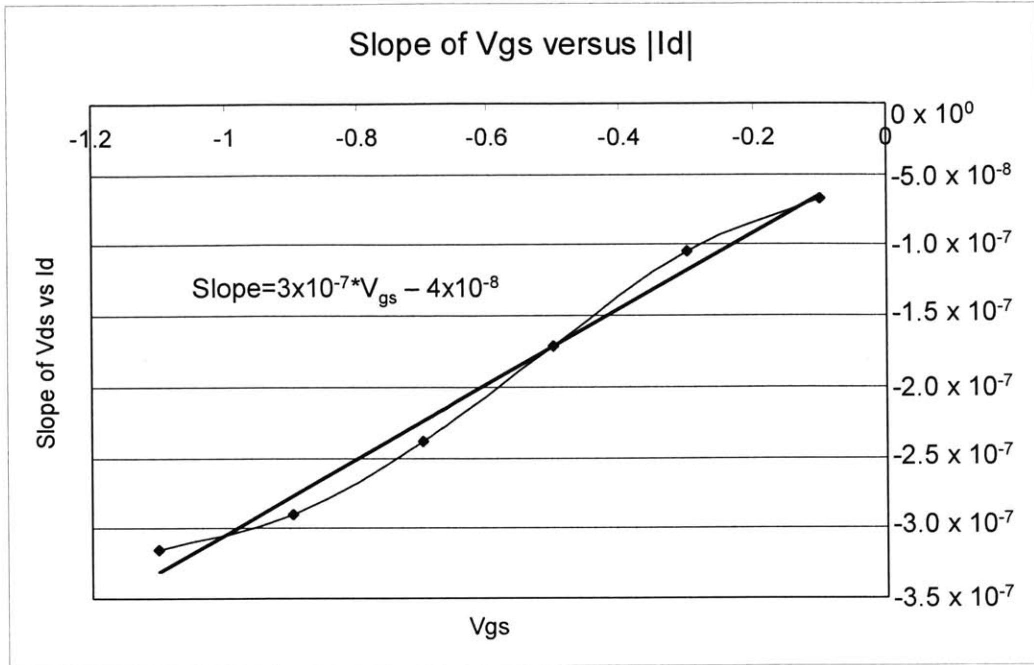


Figure 5-3: The slope of the triode regime depends linearly on the gate to source voltage, due to the control of the Schottky Barrier at the source.

monotonically with drain voltage and gate voltage. As the gate voltage increases, the slopes of the I_d versus V_{ds} curves increase linearly with constant V_{gs}. With an increase in V_{gs}, the Schottky barrier is reduced in thickness at the drain, for a constant V_{ds} voltage. With this decrease in thickness, the current increases linearly. The current changed linearly with the thickness at the drain Schottky barrier. The slope is proportional to the change in current over the change in drain to source voltage. Therefore, as the V_{gs} increase, the slope increase linearly with the current, see Figure 5-3.

5.0.7 Saturation Point

The saturation point occurs when no barrier exists at the drain end of a CNTFET. Figure 5-4 shows a description of the saturation point in terms of the energy band diagrams. The drain to source saturation point commences in a linear fashion with V_{gs}, unlike in MOSFETs where the saturation point increases in a quadratic nature. See Figure 5-5 to illustrate this linear effect.

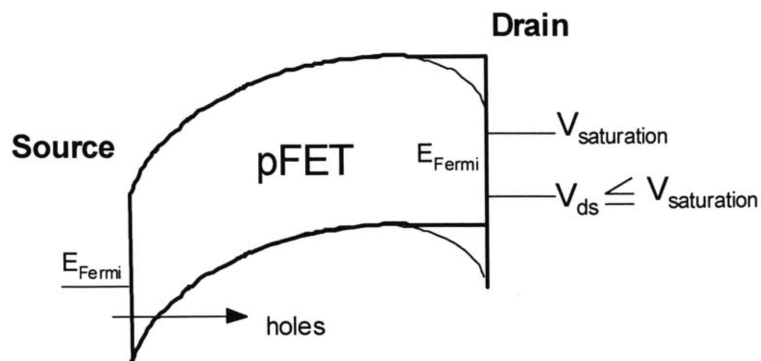


Figure 5-4: Illustration dipicting the votlage that leads to saturation for a p-type carbon nanotube FET. Saturation occurs when no Schottky barrier exists at the drain.

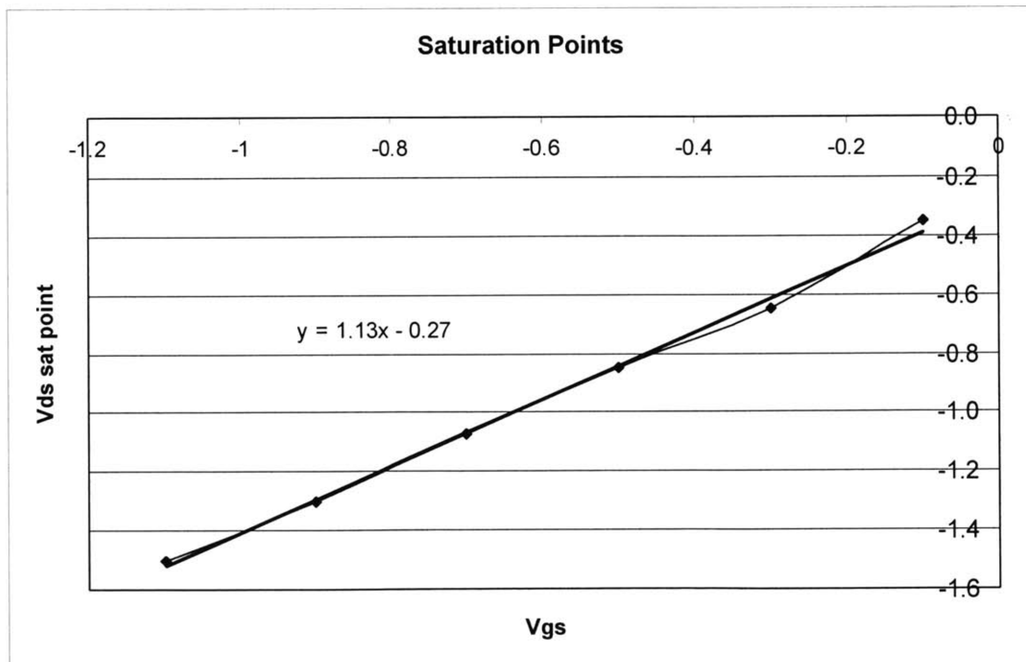


Figure 5-5: The saturation voltage occurs linearly with a changing gate voltage.

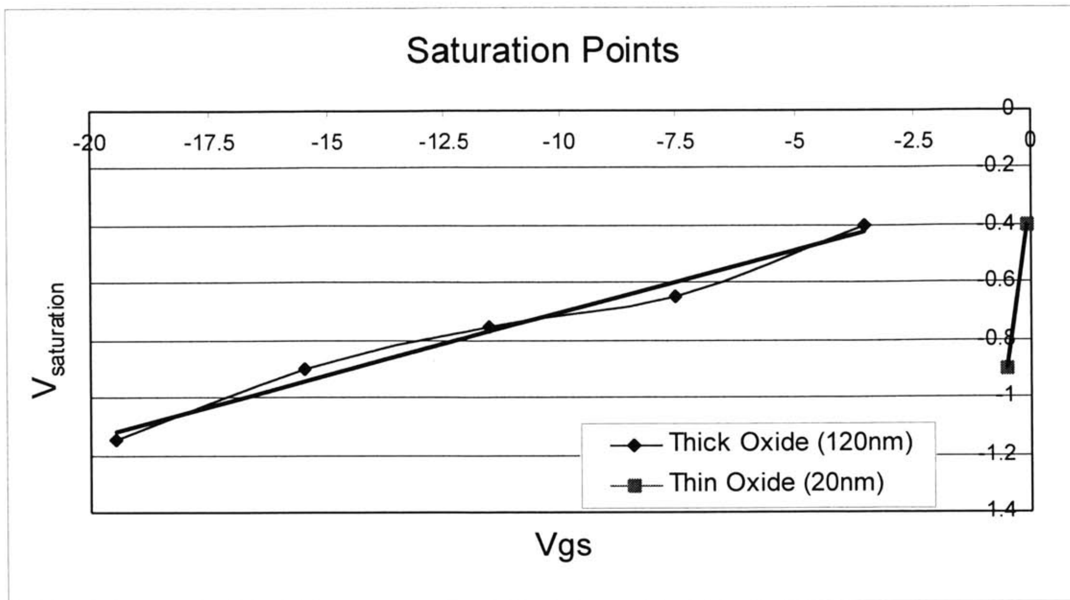


Figure 5-6: CNTFETs with thinner gate oxides have more control over the energy band diagrams and, thus, tighter control over the irIV characteristics. Thin oxide data from [12]

Saturation Point in relation to Oxide Thickness

In the subthreshold chapter of this thesis, the difference in oxide thickness was described in relation to a carbon nanotube FET's current and voltage characteristics. The gate voltage has superior control and thus, better IV characteristics, when a thinner gate oxide is applied. With a thicker oxide, a larger V_{gs} is needed to modulate the energy bands by the same amount. Thus, the saturation voltage will increase as can be seen in Figure 5-6.

5.0.8 Saturation Regime

Once the saturation point has occurred for a particular CNTFET at a V_{ds} and V_{gs}, the current will remain at relatively the same level. The tunneling at the source end will not increase with an increase in the drain to source voltages as a first order effect; also, the drain barrier has been completely eliminated. Thus, no barriers exist for holes or electrons once they pass through the source Schottky Barrier. This steady current is juxtaposed with the current in short-channel MOSFETs, which have a large slope in the saturation regime, on a V_{ds} versus I_d curve. If

second order effects are taken into account for CNTFETs, the source Schottky barrier width could change as the drain voltage increases, thus, creating a smaller slope in the saturation regime.

CNTFETs in the Saturation Regime

An important conclusion of this research and model suggest that many CNTFET devices will not enter the saturation regime. For a particular V_{gs}, the drain to source voltage needed to enter saturation must be larger than the specific gate voltages. In general the drain is attached to the highest supply voltage, so that the output swing can be as large as possible. In this case, the V_{gs} will not be larger than the V_{ds} for a transistor. Thus, CNTs created by IBM, will, most likely, remain in the triode regime. These transistors will be modeled as a voltage variable resistor in this research. The tubes themselves can be thought to be ballistic, but the contacts give the resistive drop of the transistor, with a linear IV relationship.

5.0.9 MOSFETs compared to CNTFETs

Carbon nanotubes can be used in digital circuit design because of their large on-current to off-current ratio. Part of this thesis research is designed to consider and compare the aspects of carbon nanotube FETs to future MOSFETs. Table 5-7 compares future parameters of MOSFETs to carbon nanotube transistors. The details for the MOSFETs were obtained from the 1999 ITRS roadmap. Figure 5-7 illustrates that CNTs have very high current drives in comparison to their diameter; however, if only one tube is placed per metallic contact, the current per width is greatly dissipated and silicon transistors could actually have a higher current drive per transistor width. This can be seen when comparing Rows 2 and 4 in Figure 5-7. If carbon nanotubes can be placed in parallel under one metallic contact, the high current drive of multiple tubes will greatly exceed that of silicon transistors; compare rows 2 and 5 to see the order of magnitude savings. However, with even the slight possibility of metallic tubes, redundancy would need to be added and in general, the area benefit of the CNTs would be reduced.

	1999 ITRS table	2006	2009	2012	2015
		100nm	70nm	50nm	35nm
1	**MOSFET: Max I_{off}:** (for Min L devices) @25 °C (nA/um)	**3**	**10**	**10**	**2**
2	**MOSFET: Nominal I_{on}:** [NMOS/PMOS] (high Perf) @25 °C (μA/um)	**600/280**	**600/280**	**600/280**	**600/280**
3	**CNT: Max I_{off}** for 2.5nm tube/1.3nm tube. One tube per contact. (nA/μm)	**3.0e5/30**	**4.3e5/43**	**6.2e5/61**	**8.4e5/84**
4	**CNT: Nominal I_{on}** for 2.5nm tube/1.3nm tube. One tube per contact (μA/μm)	**37.74/3.74**	**54.0/5.4**	**76.9/7.69**	**105/10.5**
5	**CNT: Nominal I_{on}** per tube diameter for 2.5nm tube/1.3nm tube	**4,000/769**	**4,000/769**	**4,000/769**	**4,000/769**

Figure 5-7: Table depicting the characteristics of CNTFETs in comparison to future MOSFETs.

5.0.10 Process Variations

Carbon nanotubes can have very impressive current characteristics, however, as was mentioned above, and in Chapter 3: Subthreshold Carbon Nanotube FETs, the process variations have to be controlled more closely before the use of CNTFETs will become prolific. It is very difficult to assume a certain current level for a particular CNT device due to large process variations. The contacts dictate the current levels and the metal contacts to carbon nanotubes differ dramatically, even among transistors along the same CNT. The variation can be as large as orders of magnitudes as seen in Figure 5-8. During the contact annealing process, a different number of carbon-carbon bonds are broken within the nanotube structure and thus, there is a different level of connection between the contact and nanotube. This difference leads to a limited ability of modern CNTs to be use in circuits. However, in general, once the process variations are controlled, carbon nanotubes can excel in digital circuit designs because of the large I_{on}:I_{off} ratio and high current drives.

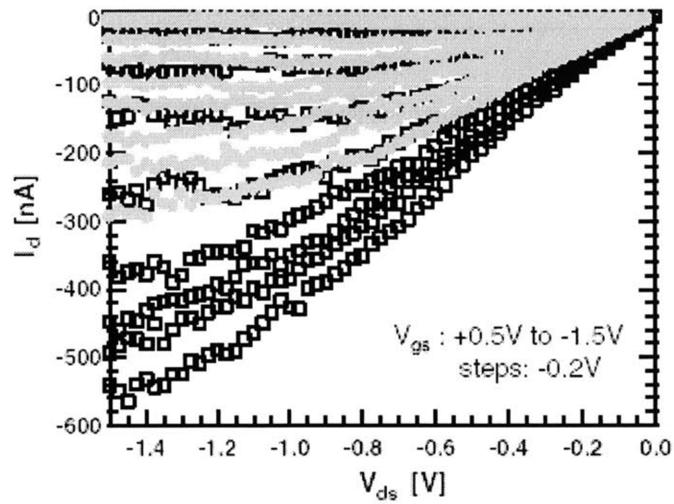


Figure 5-8: CNTFET IV characteristics for one nanotube measured in one dirction. The CNT was then flipped around and the current was measured again. The varying current levels prove that the intrinsic nanotube does not control the current voltage characteristics. [5]

Chapter 6

ROM Research

Carbon nanotubes have characteristics that make them well suited to aid in following Moore's Law when silicon limits arise. Carbon nanotubes are especially useful in read only memory arrays (ROM)—in such circuit devices, multiple transistors can be placed along the length of a CNT. This research aims to describe, characterize, and compare the parameters of CNT ROMs in respect to CMOS ROM arrays.

In CNT ROM arrays, if nanotubes can be closely aligned, there is a large possibility for many nanotubes to be placed under similar gates, along the length of a micro to millimeter long CNT. This research is theoretical—presently there are no growth processes that produce carbon nanotubes in arrays as tightly spaced as a few nanometers apart. However, the possibility for such growth is being closely considered [32] and this thesis research will assume the availability of tightly packed parallel nanotubes.

CNT transistors can help in scaling ROM devices, because they have very large current drives that depend on the source and drain contact, the gate oxide, and the CNT diameter, rather than the channel length. In CMOS ROM's, to increase the current drive, transistor channel lengths are having to become increasingly small; this scaling of channel lengths will cause many problems for future technologies. Because carbon nanotube FET current is dictated by the contacts (the channel is considered to have ballistic transport) the length of the CNTFET channel can vary without changing the current. Also, carbon nanotube FETs have an even current drive for PFETs and NFETs because of the equal mobility of electron and holes in a CNT.

This research will take these CNTFET advantages and look at the previously described Schottky barrier transistors in terms of read only memory arrays.

6.1 Schottky Barrier ROM Array Structures

6.1.1 NOR ROMs

In silicon ROMs, electrons have a much lower mobility than holes and therefore, NMOS transistors have a higher current drive per width than PMOS transistors. Therefore, NMOS transistors are on average 2-3 times smaller than PMOS transistors. Thus, in CMOS ROMs, NMOS transistors are generally used for the array section. NOR ROMs are created in CMOS technology by adding NMOS transistors in parallel. NAND ROMs can be created by placing NMOS devices in series; NAND CMOS arrays are very compact because the devices are stacked without intermediate contacts. However, NAND ROMs loose performance drastically because of the series device and therefore, are generally not used. NAND ROMs have large delays and hence NOR ROMs are generally used unless special conditions require the size scaling of NAND ROMs.

In contrast, carbon nanotube parallel array ROMs have the option of using both PFETs or NFETs without loosing performance. In CNTFETs, PFET devices are not at a disadvantage to NFET transistors in terms of current voltage (I-V) characteristics or area as is the case in CMOS technology. Therefore, NOR arrays can be created easily out of parallel NFET or PFET transistors with bias transistor as shown in Figures 6-1. The bias transistors acts as a small pull-up resistor; it must be large enough to the pull the output high, but small enough to guarantee that one word line transistor could pull the output low. A sample circuit diagram of a NOR ROM is given in Figure 6-1. The area is decreased in the ROM cell because every other device is flipped so that the ground contacts can be shared between word lines.

6.1.2 Programing ROM Arrays

Generally only one mask level is used to program a ROM in CMOS technology. This same one mask method will be assumed for programing CNTFET ROMs. There are two possible methods to program a CMOS ROM; either the Active mask can be altered to selectively add a diffusion layer to the present transistors, or the output contact mask can be changed to only contact

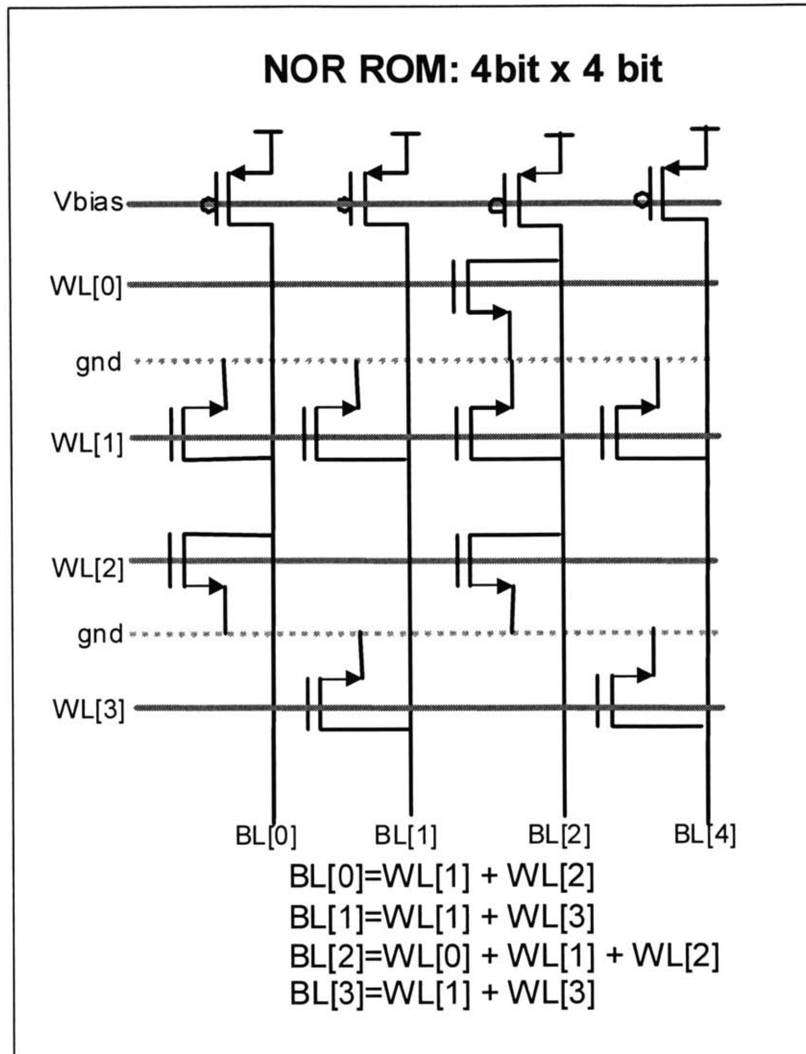


Figure 6-1: NOR ROM arrays are created out of parallel NFET transistors from either MOSFET or CNTFET technology, sharing a ground contact to save area. The V_{bias} is an input to p-channel transistors that act as pull-up resistors.

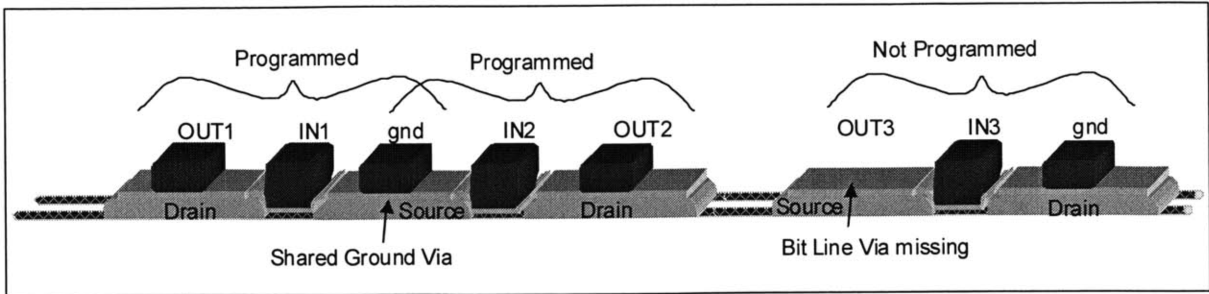


Figure 6-2: If a CNTFET ROM is programmed with drain vias, the ground contacts can be shared, however, each transistor must have a seperate output, drain, contact. This can be used for a PFET or NFET NOR array, depending on the doping or annealing of the CNTFETs.

the drains of present transistors. Since there is no active mask step in CNTFET technology, this programming method cannot be considered. On the other hand, if the bit line via mask is altered, a CNTFET ROM can be programed by contacting the drain of a present transistor to the bitline with a via or not adding a via for an absent transistor. Figure 6-2 illustrates this "drain via" style of programming.

In this programming method, bit line vias and drain contacts cannot be used for multiple transistors. Thus, the contact area greatly dictates the size of the array. The layout can be seen in Figure 6-3. As was described previously, the area of the source and drain contacts are dictated entirely by the metal lithographic dimensions, not by the carbon nanotube dimensions. Figure 6-4 illustrates the metal pitch sizes used in this research, taken from the predictions made by [10]. [10] predicts CMOS scaling; it will be used for CNTFETs because only the metal scaling is considered in this research. Therefore, in a NOR ROM, made of CNTFETs, the channel length and width are dictated by the metal gate and gate vias. The source and drain metal area is dictated by the source and drain wiring vias and the required pitch between the gate to source and gate to drain contacts. Thus, unshared contacts within the array, increase the area and capacitance dramatically. Figure 6-3 diagrams the need for extra contacts within CNTFET ROM for parallel transistors. A more efficient programming method would share output contacts between neighboring CNTFETs.

A theoretically proposed programming method, similar to the CMOS Active mask step, will be considered here just to show the difference between the drain via programming method

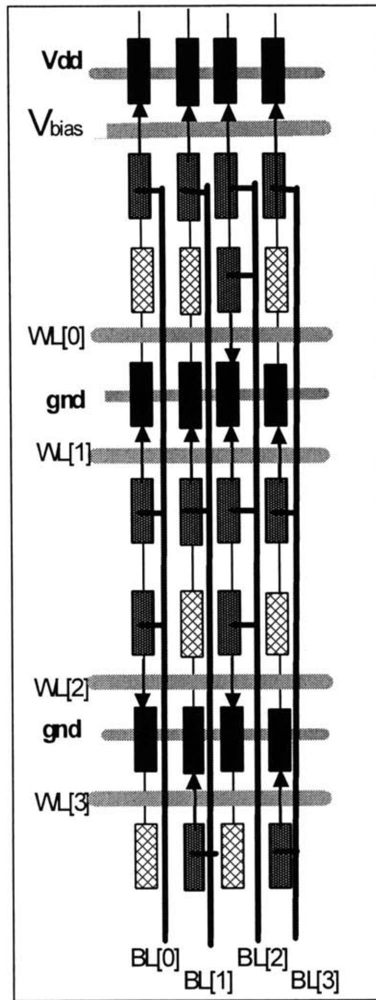
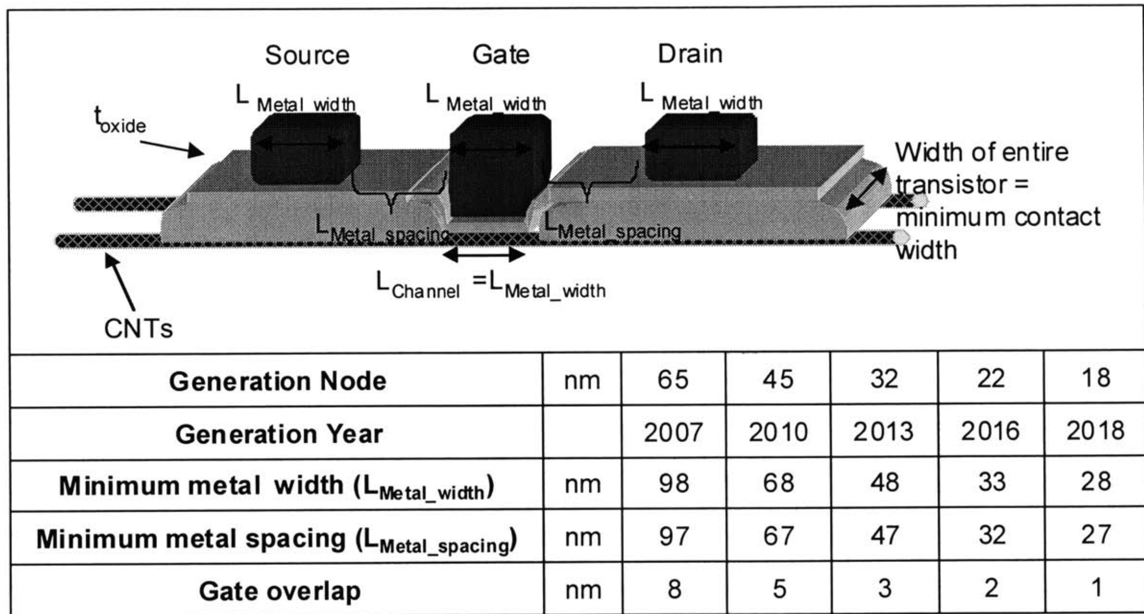


Figure 6-3: Extra contacts are needed if a NMOS NOR ROM is programmed by the addition of drain vias from the output bit line to a present transistor. The extra contacts add area and output capacitance.



Generation Node	nm	65	45	32	22	18
Generation Year		2007	2010	2013	2016	2018
Minimum metal width (L_{Metal_width})	nm	98	68	48	33	28
Minimum metal spacing ($L_{Metal_spacing}$)	nm	97	67	47	32	27
Gate overlap	nm	8	5	3	2	1

Figure 6-4: The size of transistors is dictated by the metallic pitch for the gate, drain, and source contacts. This figure shows the values used in this research to predict the size of future ROM technologies. These sizes are based off of the predictions made by [10].

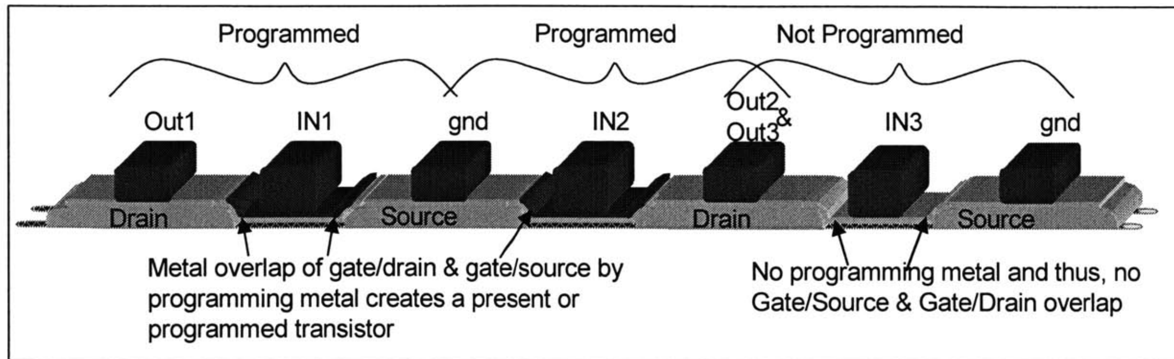


Figure 6-5: An overlap is needed by the gate to source and gate to drain–without an overlap, a transistor will not work properly. A CNTFET ROM, programmed by the extended channel method, eliminates the need for extra drain contacts by selectively adding gate/drain and gate/souce overlaps to present transistors.

above and a method in which output contacts can be shared. In Schottky barrier CNTFETs, the source overlap with the metal gate controls the current flow. A carbon nanotube FET can be eliminated by not placing a gate overlap across the source and drains. In this theoretical proposition, the channel length of the transistors will be increased to account for the spacing of a metal programming gate to overlap the source and drain. The extended channel leaves area for a word line wiring contact separate from the programming metal. This structure can be seen in Figure 6-5 and compared to Figure 6-2. Because the carbon nanotube FET field is relatively young, no ROM arrays have been programming using the programming metal. However, because a gate overlap is needed in a CNTFET transistor, this method is proposed to show a possible programming method that could lower both area and output capacitance. In the coming thesis sections, both types of programmed ROMs will be compared for capacitance, resistance, and area considerations.

6.1.3 ROM Redundancy

If more current drive is needed within transistors, additional carbon nanotubes can be added in parallel to other CNTs, while sharing the same gate, drain, and source or CNTs can be added in parallel under separate gates. Figure 6-6 shows different methods of increasing the current drive of transistors to 4 CNTs per transistor. When multiple CNTs share similar contacts,

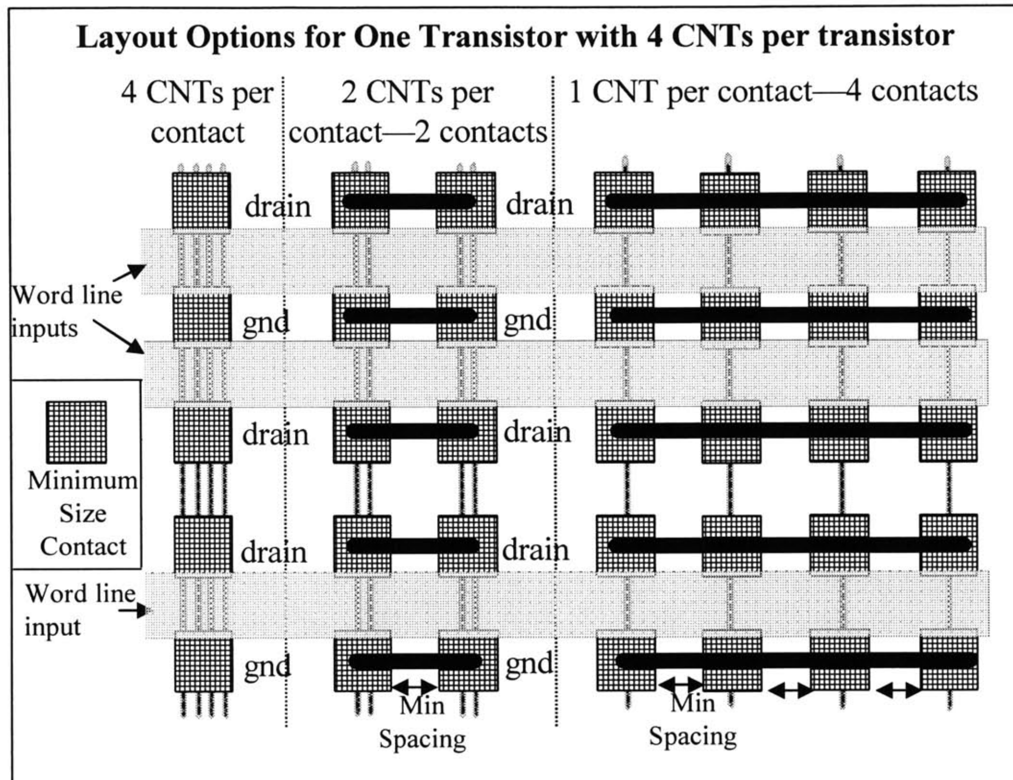


Figure 6-6: To increase the current drive of transistors, CNTs can be added in parrallel. To save area and contact capactiance, 4 nanotubes can be placed under the same contact. Other layouts include 2 CNTs placed under 2 seperate contacts and the contacts wired together or, each CNT placed under a seperate contact. The contact number and dimensions dictates the area of the array.

the additional CNTs will decrease the resistance without adding additional contacts or area. However, a percentage of nanotubes will be created metallic. If metallic nanotubes are placed in a CNTFET, in leu of a semiconducting nanotube, the metallic nanotube will connect the source and drain directly. This will happen along the length of the entire metal carbon nanotube and that row will not be useful. Therefore, it is best to keep one bit line along one nanotube. In this case, if a CNT is metallic, one bit line is destroyed, but redundancy can account for such a case–no other bit lines will be affected.

To account for metallic nanotubes, large amounts of redundancy must be added to the array. In this research, a percentage, ρ, of nanotubes are considered to be metallic. Therefore, (1-ρ) is the probability of a semiconducting nanotube. If n nanotubes are placed per transistor gate, the number of good contacts, q, is $q = (1-\rho)^n$. This research wants to find the total number of contacts needed, L, to create N good contacts (contacts without metallic CNTs), accounting for a certain percentage accuracy, ζ. P($M \geq N$) $= \zeta$, where M is the total number of good contacts. If L is large, $M \approx$Binomial Distribution(μ, σ^2), where the mean (μ) is $L * q$, and the variance is $\sigma^2 = L * q(1-q)$. With the Binomial Distribution, the total number of good contacts, N, can be found for a certain percentage of metallic nanotubes, ρ, out of L number of total contacts. In this research, a Matlab script has been merged into the Matlab CNTFET model and is run to consider ROM area and bit line capacitance. Figure 6-7 shows visually that 4 CNTs per transistor ($n = 4$) can save area in Figure 6-6, however, with a high percentage of metallic nanotubes, the added redundancy might surpass the area of an array with $n = 2$.

6.1.4 ROM Area

The area is going to be least when the number of contacts is at a minimum. Figure 6-8 shows the graph of the total number of contacts, L, versus the number of CNTs per contact, depending on the percentage of metallic nanotubes, ρ. If only 1 CNT per metal source and drain is used, each nanotube will use a separate contact along with added contacts for the redundancy. For example, in Figure 6-8, a 128 bit wide ROM, with 5% of the carbon nanotubes metallic and 16 CNTs per transistor, will use 2048 semiconducting CNTs along with 103 nanotubes for redundancy. Therefore, with only one nanotube per contact, 2151 contacts are needed. However, if many (9-16) CNTs share a common source and drain, there is a large probability that

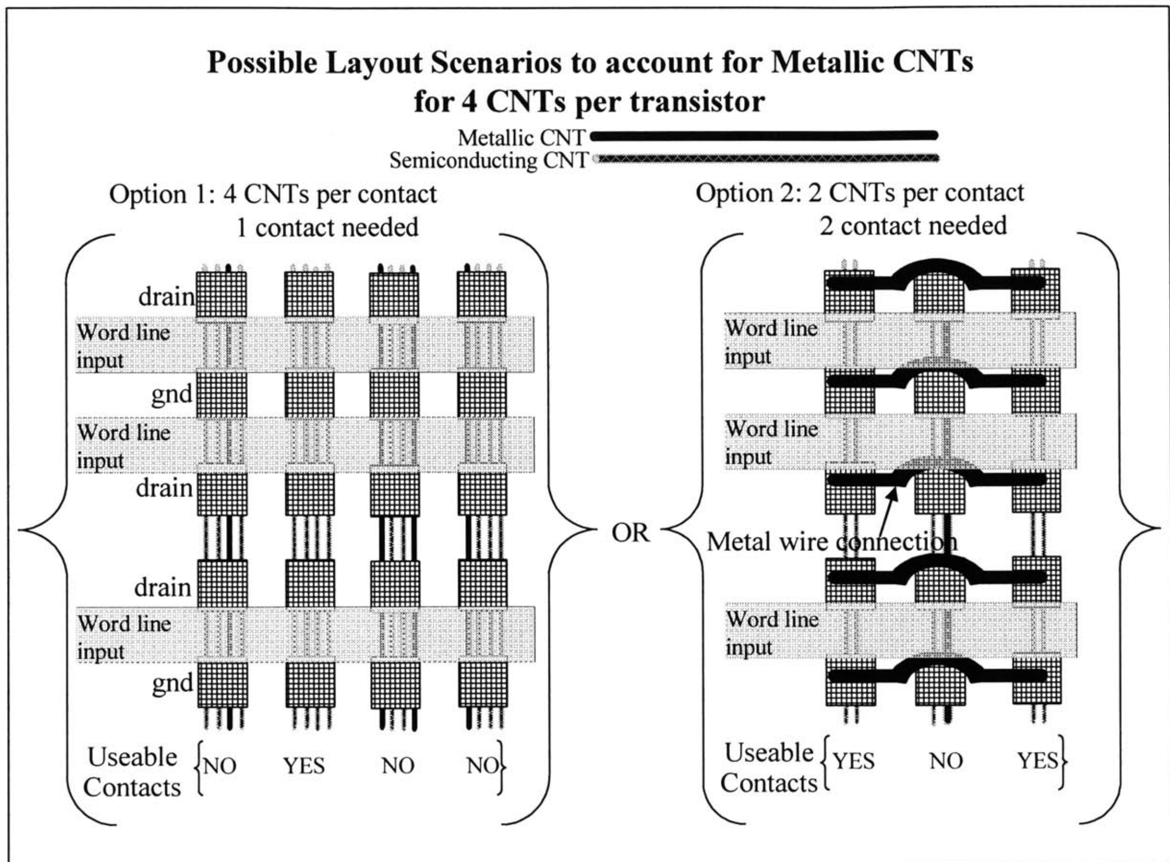


Figure 6-7: The area savings associated with multiple nanotubes per contact can be outweighed by the redundancy associated with metallic nanotubes as shown in the scenario above. Here 4 CNTs per transistor are needed; in this case, it is beneficial in terms of area to have few CNTs per contact (Option 2) rather than Option 1 with 4 CNTs per contact.

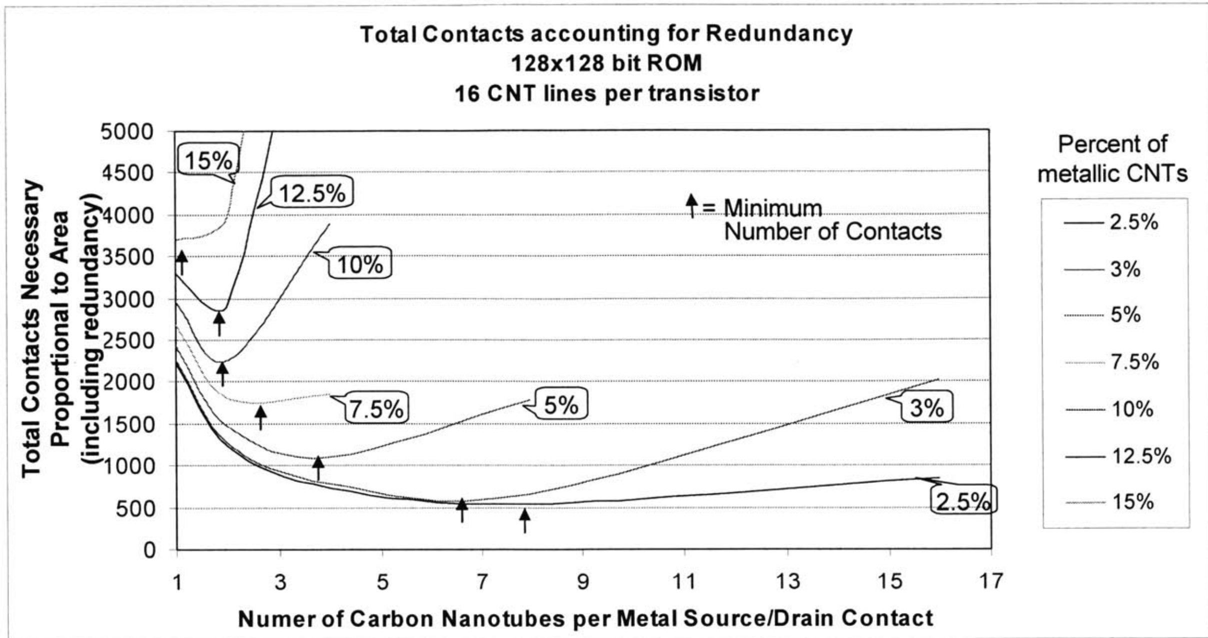


Figure 6-8: The total number of contacts for a 128bit wide ROM, with 16 parallel CNTs per transistor. The number of CNTs per metal gate is varied on the x-axis and the percent of metallic CNTs is also varied.

a metallic nanotube will be placed on almost every contact and render most of the transistors futile. Thus, there is a minimum number of contacts that exist for each percentage of metallic CNTs, ρ. Figure 6-8 also illustrates that as ρ increases, a larger number of CNTs per gate will eliminate many of the rows and it is cost effective in terms of area to reduce the number of CNTs per metallic gate because less redundancy will be necessary. At a certain point, around ρ=15%, in Figure 6-8, the total number of contacts is at a minimum when only one CNT is placed per metal gate. This optimization is at a cost of output capacitance, which varies per output contact.

The width and the area depends on the number of contacts. If the optimal number of contacts from the redundancy stand point are chosen, the area will be at a minimum. Figure ??, illustrates the difference in area between ROM arrays programmed with drain vias and with an extended channel. The later is always smaller because of the shared drain contacts.

6.1.5 ROM Capacitance

The number of contacts and therefore, the width and area of a ROM will dictate the capacitance properties of a ROM. The output or bit line capacitance of a CNTFET ROM depends on the capacitance theory described in Chapter 4: Capacitance, Energy, and Delay of Subthreshold CNTFETs. The bit line capacitance is composed of the drain parasitic capacitance and the drain Miller overlap capacitance. Thus, as the number of output contacts increase, the capacitance also increases. To minimize output capacitance, more carbon nanotubes should be placed under a single metal gate instead of using each with its own contacts. This fact can be see in Figure 6-9, where the capacitance is graphed versus future year and lithography and the number of CNTs sharing a common gate, source, and drain. The capacitance is a trade-off versus the area considerations above that include metallic nanotube redundancy calculations.

There is a difference between the capacitance of the two differently programmed ROMs. ROMs programmed using drain vias to connect the output contacts to the bit line will have the capacitance depend on the number of transistors in the ROM and thus, the number of connected outputs. The capacitance in Figure 6-9 shows the worst case, where all drain contacts are attached. On the contrary, ROMs programmed with lengthened channels and additional gate metal will have all output contacts attached to the bit line, independent of the number of programmed transistors. This means when few transistors are programmed, the capacitance will be large because of the additional drain to bulk capacitance from all drain contacts.

As was shown in Chapter 4: Capacitance, Energy, and Delay of Subthreshold CNTFETs, the Miller capacitance dominates the parasitic drain capacitance. When no device is programmed, the Miller overlap capacitance does not exists; the additional parasitic capacitance will only depend on the small drain to bulk capacitance of the metal drain. This drain to bulk capacitance will only become a problem when very few transistors are programmed along a bit line or when few CNTs are placed per metallic gate–consequently, there are more parallel CNTFETs with additional contacts. It can be seen in Figure 6-10 that if there are very few transistors programmed along a bit line, the ROM programmed with output vias has a smaller capacitance; however, as the number of transistors along the bit line increases, the capacitance of such a ROM will increase faster than a ROM programmed with the extended channel method. Both ROMs increase dramatically in capacitance as the number of CNTs per contact drop and the

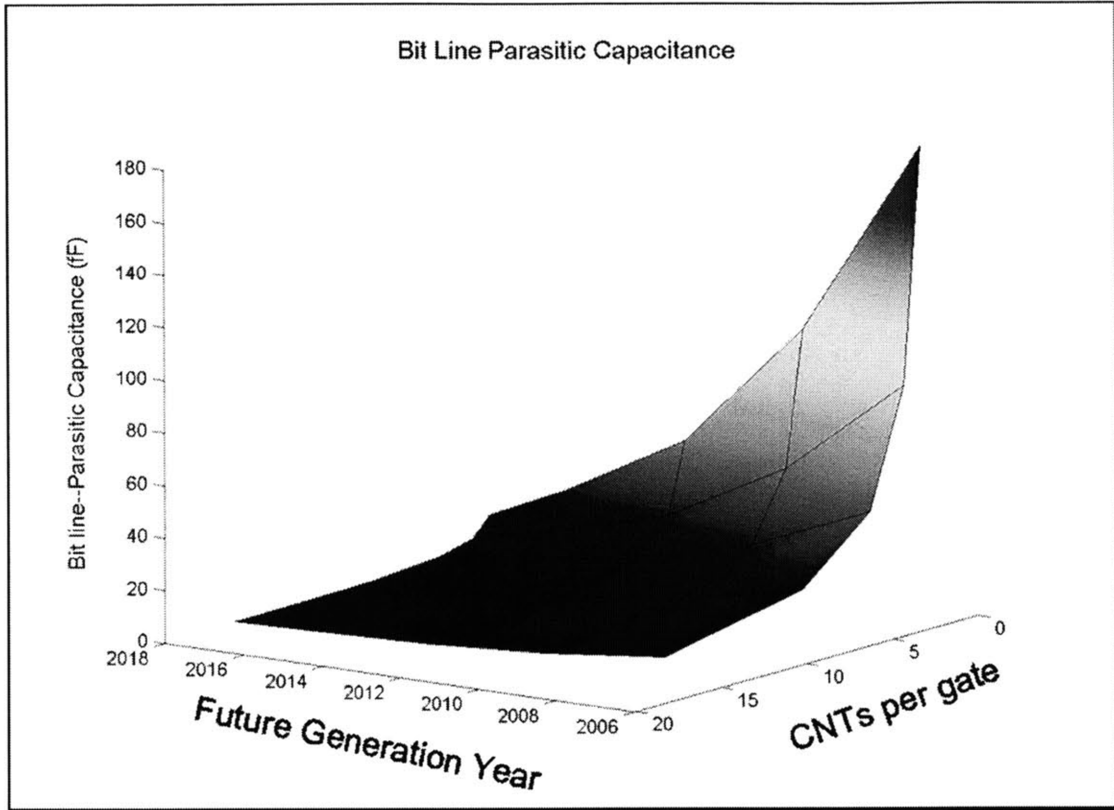


Figure 6-9: The parasitic capacitance per bit line drops as the number of output contacts decrease, or the number of CNTs per contact increases. This graph shows the capacitance for a 128x128 ROM, with 16 CNTs per transistor, programmed by drain vias.

number of parallel transistors and output contacts increase.

In the case, where all transistors are attached to a bit line and there are few CNTs per contact, and consequently many parallel contacts, the capacitance will drastically increase for both types of ROMs, but especially for the drain via programmed ROM, as can be see from Figure 6-10.

It can be seen in this section, the output capacitance of a CNTFET ROM is greatly dictated by the number, size, and type of output contacts. The number of CNTs per gate can be increased to decrease the capacitance, however, this may increase the area for such a ROM. The trade-offs must be considered in the design.

6.1.6 ROM Resistance

The current voltage, I-V, characteristics of CNTFETs have been described in previous chapters. The ROM devices in this chapter are considered variable voltage resistors. The gate voltage is applied directly to a metal word line and not a poly line. This metal gate will decrease the resistance of the word lines. The bit line resistance will depend dramatically on the amount of wiring between contacts. If few CNTs are placed per contact, but wide FETs are needed, the wiring resistance will grow dramatically because of the parallel connection of CNTFETs and the additional contacts. The addition of the extra parallel CNTFETs will not increase the current as dramatically as expected because of the large wiring resistance necessary to connect parallel CNTFET of one bitline. Thus, both the R and C factors in $\tau = RC$, will decrease as the number of CNTs per single metal gate increase.

6.1.7 Conclusion

CNTFETs have a large potential in ROM arrays. There channel lengths do not have to scale in CMOS technologies. Instead, more carbon nanotubes must be added in parallel under one metallic gate. This will decrease the parasitic capacitance and output resistance. However, this comes at a large cost for area. The area is future ROM CNTFET technologies is going to rely on the certainly of fewer metallic CNTs in the growth process. If CNTs are metal upon growth, large amounts of redundancy will have to be added to account for possible metallic nanotubes. The redundancy necessary was given in this chapter along with the trade-offs between the

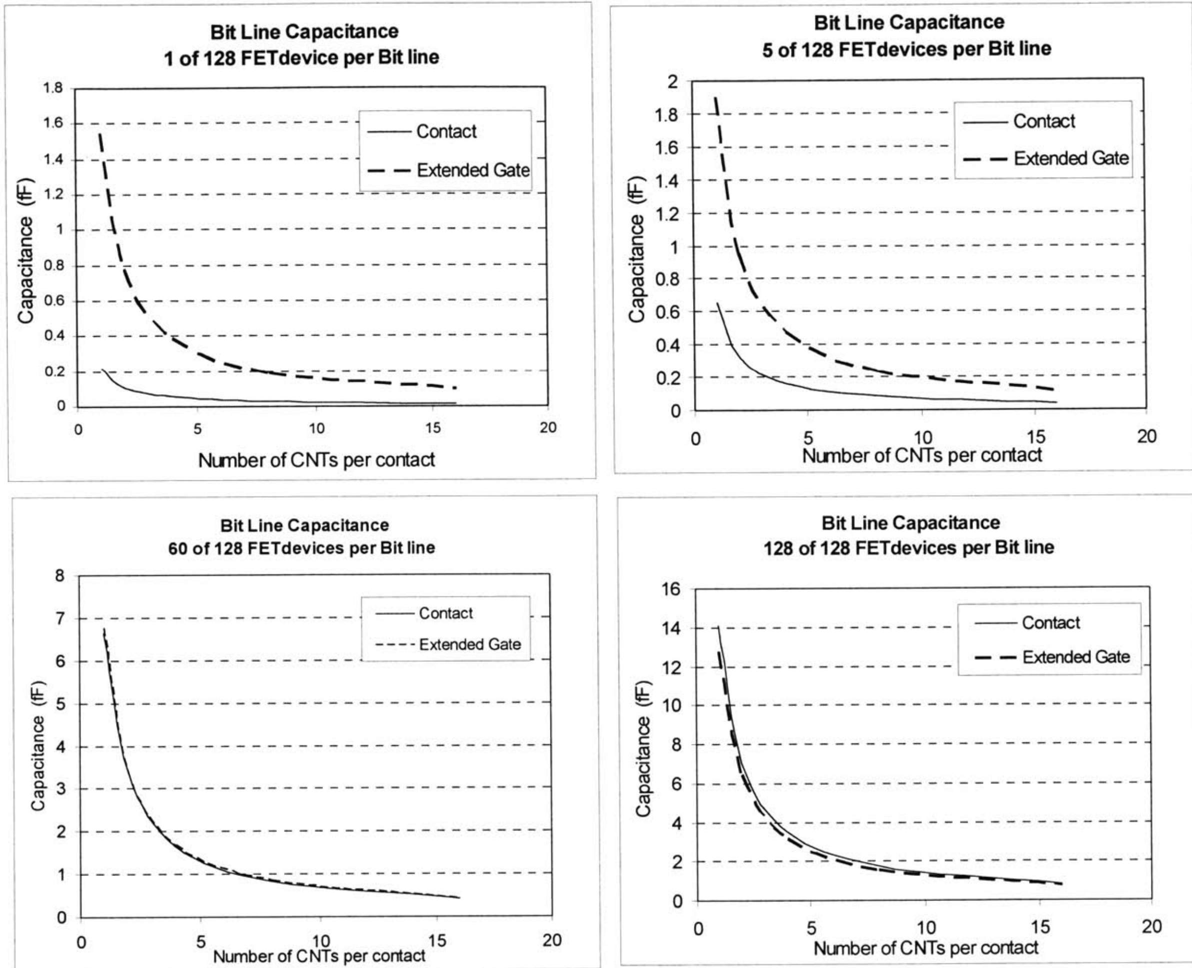


Figure 6-10: A ROM programmed with an extended gate will have a relatively large capacitance when few FET devices are present per bit line. This is because of the connection to all output contacts. However, as the number of FET devices increases per bitline, the shared contacts, used in the extended gate programming method, begin to become advantageous.

output capacitance and resistance.

Chapter 7

Conclusions

The electronics industry continues to scale metal oxide semiconducting transistors (MOSFETs) following the predictions of Moore's Law; with the scaling, i.e. reduction of feature size, physical restrictions are becoming more apparent and difficult to surpass. Many disruptive technologies are being considered to aid in future generations of electronics; carbon nanotubes offer scaling opportunities and the possibility of coexistence with the present silicon technology.

Carbon nanotubes (CNTs) are cylinders that can grow up to millimeters in length with diameters in the nanometer range; these long cylinders can aid in scaling because of their unique properties. CNTs can have a varied energy band gap depending on their chirality and CNT diameter. This variable band gap gives rise to nanotube properties ranging from metallic to semi metallic to semiconducting. Most present CNT research pertains to the growth and properties of nanotubes; the work presented in this thesis displays their potential within digital circuit design by creating a model and then applying that model to low voltage circuits and read only memory arrays.

Metallic carbon nanotubes can be used as wires on circuit boards; semiconducting carbon nanotubes can be used as the channel in transistors. This research studies carbon nanotube's applications to carbon nanotube field effect transistors (CNTFETs). CNTFETs are similar in structure and current voltage characteristics to MOSFETs; the gate, drain, and source voltages control the device in an exponential subthreshold regime, a linear regime, and a saturation regime. Despite the similar properties of CNTFETs to MOSFETs, carbon nanotube transistor current is dictated by an entirely different process. CNTFET Schottky barriers are formed

at the source and drain contacts. These barriers control the tunneling current of the device; the CNT acts as a ballistic channel between the contacts. This ballistic channel gives rise to potentially high current rates per transistor, symmetric hole and electron mobilities, and no current versus channel length dependence; therefore, CNTFETs can skirt some of the scaling requirements of MOSFETs such as channel length minimization and channel doping.

Carbon nanotube field effect transistors have similar linear and saturation current voltage (I-V) characteristics to MOSFETs; the I-V characteristics were studied and modeled closely in this thesis. An interesting property of CNTFETs, shown in this research, is that they will most likely remain in the linear or weak inversion regimes. To enter saturation, the drain to source voltage must be larger than the gate to source voltage; this does not often occur in digital logic designs. Therefore, CNTFETs above threshold were modeled as variable voltage resistors in this research. Also, CNTFETs have an interesting low voltage, weak inversion regime. This regime will be important in future technologies; on-chip voltages continue to scale with future generations. The weak inversion regime shows that CNTFETs are ambipolar transistors; they have an exponential subthreshold regime on either side of a minimum voltage at $V_{\min} = \frac{V_{drain-source}}{2}$ if the gate, source, and drain are made of the same metals. This minimum occurs when the Schottky barriers at both the source and drain are thickest and the tunneling current is smallest for both electrons and holes. These I-V characteristics have been studied closely in the present work to prove the ability of these ambipolar FETs to be placed in digital designs. Also, the application of these CNTFETs to inverters was contrasted for different size diameter nanotubes. This research illustrated the trade-offs between the impressive voltage transfer characteristics of inverters made with small diameter CNTs and inverters composed of larger diameter CNTs with high current drives. These trade-offs give carbon nanotube field effect transistors great potential within digital circuit design.

The large potential of carbon nanotube FETs to read only memory (ROM) arrays is illustrated in this thesis. Unlike CMOS, CNTFETs have even current drives between n-channel and p-channel devices; thus, parallel transistor arrays can be created out of NFET and PFET transistors to create both NOR and NAND ROMs, contrary to NOR only arrays from n-channel MOSFETs. The area of these ROMs is dictated entirely by the metal contact and via lithography specifications. Thus, to minimize the area of these devices, the least number of contacts

should be used. This minimum depends on the total current drive needed, the percentage of metallic versus semiconducting nanotubes, and the number of nanotubes sharing the same gate, drain, and source contacts. In this research, the minimum number of contacts, and thus the minimum area, was found to depend on the percentage of metallic nanotubes. However, this minimized area does not necessarily correspond to the array with the minimized capacitance and, therefore, delay. The output capacitance of CNTFET devices is mostly dependent on the number and dimensions of the contacts. Therefore, it is best to have a minimum number of contacts by placing more CNTs per gate, this may lead to additional redundancy and area. A circuit designer has the ability to trade-off speed and area of ROMs depending on the contact size, redundancy, and number of CNTs per contact.

Thus, carbon nanotubes transistors have the ability to scale the technology into new feature sizes and generations with similar I-V characteristics to MOSFETs. Most current CNTFET research is in the growth and characterization stage. The process variations within the growth processes must be controlled before these devices can reach their full potential and can truly compete with the present silicon technology. These variations are limiting all applications of CNTFETs including the digital logic design and array designs described above. The band energy of carbon nanotubes cannot completely be controlled, therefore, a few nanotubes will be metallic in nature. Also, the current can vary dramatically between transistors, depending on the drain and source contact variations. However, the carbon nanotube field is very young and the technology for reducing the process variations is developing quickly. Once these variations are more tightly controlled, which should happen in the near future, the impressive I-V characteristics of CNTFETs have great promise for future circuit designs and will open many opportunities for digital circuit designers.

Bibliography

[1] M. Dresselhaus, G. Dresselhaus, P. Eklund, and R. Saito, "Carbon nanotubes," *Physics Web Online.*

[2] S. Iijima, "Carbon nanotubes: past, present, and future," *Applied Physics Letters*, vol. 323, pp. 1–5, Oct. 2002.

[3] P. G. Collins, M. S. Arnold, and Ph. Avouris, "Engineering carbon nanotubes and nanotube circuits using electrical breakdown," *Science*, vol. 292, pp. 706–709, Apr. 2001.

[4] H. Dai, "Carbon nanotubes: Synthesis, integration, and properties," *Acc. Chem. Rev*, vol. 35, no. 12, pp. 1035–1044, 2002.

[5] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S. Wind, and Ph. Avouris, "Field-modulated carrier transport in carbon nanotube transistors," *Physical Review Letters*, vol. 89, pp. 126801.1–126801.4, Aug. 2002.

[6] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, "Carbon nanotubes as schottky barrier transitors," *Physical Review Letters*, vol. 89, no. 10, pp. 106801.1–106801.4, Sept. 2002.

[7] J. Appenzeller, J. Knoch, R. Martel, V. Derycke, S. Wind, and Ph. Avouris, "Carbon nanotube electronics," *IEEE Transactions on Nanotechnology*, vol. 1, no. 4, pp. 184–189, Dec. 2002.

[8] Ph. Avouris, R. Martel, V. Derycke, and J. Appenzeller, "Carbon nanotube transistors and logic circuits," *Physica B: Condensed Matter*, vol. 323, pp. 6–14, Oct. 2002.

[9] X. Wang, H-S. P. Wong, P. Oldigs, and R. Miller, "Electrostatic analysis of carbon nanotube arrays," *International Conference on Simulation of Semiconductor Processes and Devices*, pp. 163–166, Sept. 2003.

[10] ITRS, "International technology roadmap for semiconductors," *public.itrs.net*, 2003.

[11] IBM-Joerg Appenzeller, ," *IBM TJ Watson Research Center*, 2003.

[12] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, "Verical scaling of carbon nanotube field-effect transistors using top gate electrodes," *Applied Physics Letters*, vol. 80, pp. 3817–3819, May 2002.

[13] S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 354, pp. 56–58, 1991.

[14] J. Kong, J. Cao, and H. Dai, "Chemical profiling of single nanotubes: Intramolecular p-n-p junctions and on-tube single-electron transitors," *Applied Physics Letters*, vol. 80, no. 1, pp. 73–75, Jan. 2002.

[15] M. S. Dresselhaus, G. Dresselhaus, and Ph. Avouris, *Carbon Nanotubes: Synthesis, Structure, Properties, and Applications*, vol. I, Springer, New York, 2001.

[16] T. W. Ebbesen and P. M. Ajayan, "Large-scale synthesis of carbon nanotubes," *Nature*, vol. 358, pp. 603–605, 1992.

[17] P. G. Collins and Ph. Avouris, "Nanotubes in electronics," *Scientific American*, pp. 62–69, Dec. 2000.

[18] M. Endo and H.W. Kroto, "Formation of carbon nanofibers," *Journal of Physical Chemistry*, vol. 96, no. 17, pp. 6941–6944, 1992.

[19] C. Zhou, J. Kong, E. Yenilmez, and H. Dai, "Modulated chemical doping of individual carbon nanotubes," *Science*, vol. 290, pp. 1552–1555, Nov. 2000.

[20] W. Kim, H.C. Choi, M. Shim, Y. Li, D. Wang, and H. Dai, "Synthesis of ultralong and high percentage of semiconducting single-walled carbon nanotubes," *Nano Letters*, vol. 2, no. 7, pp. 703–708, 2002.

[21] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, and H. Dai, "High-k dielectrics for advanced carbon-nanotube transistors and logic gates," *Nature Materials*, vol. 1, pp. 241–246, Dec. 2002.

[22] A. Javey, Q. Wang, A. Ural, y. Li, and H. Dai, "Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators," *Nano Letter*, vol. 2, no. 9, pp. 929–932, 2002.

[23] A. Thess, R. Lee, P. Nikolaev, H. Dai, P. Petit, J. Robert, C. Xu, Y.H. Lee, S.G. Kim, D.T. Colbert, G. Scuseria, D. Tomanek, J.E. Fischer, and R.E. Smalley, "Crystalline ropes of metallic carbon nanotubes," *Science*, vol. 273, pp. 483–487, July 1996.

[24] J. Appenzeller, J. Knoch, R. Martel, V. Derycke, S. Wind, and Ph. Avouris, "Short-channel like effects in schottky barrier carbon nanotube field-effect transitors," *IEEE International Electron Devices Meeting*, 2002.

[25] Ph. Avouris, J. Appenzeller, V. Derycke, R. Martel, and S. Wind, "Carbon nanotube electronics," *IEEE International Electron Devices Meeting*, 2002.

[26] R. Martel, H-S. P. Wong, K. Chan, and Ph. Avouris, "Carbon nanotube field effect transistors for logic applications," *IEEE International Electron Devices Meeting*, 2001.

[27] R. Martel, V. Derycke, J. Appenzeller, S. Wind, and Ph. Avouris, "Carbon nanotube field effect-transistors and logic circuits," *Design Automation Conference*, 2002.

[28] R. Martel, "High-performance transistors," *Nature Materials*, vol. 1, pp. 203–204, Dec. 2002.

[29] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, "Fabrication and electrical characterization of top gate single-wall carbon nanotube field effect transitors," *Journal of Vacuum Science and Technology B*, vol. 20, no. 6, pp. 2798–2801, Nov. 2002.

[30] A. Wang and A. Chandrakasan, "A 180mv fft processor using subthreshold circuit techniques," *IEEE International Solid-State Circuits Conference*, pp. 292–293, 2004.

[31] J. Rabaey, A. Chandrkasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, vol. 2, Pearson Education, Inc., Upper Saddle River, NJ, 2003.

[32] M. Lay, J. Novak, and E. Snow, "Simple route to large-scale ordered arrays of liquid-deposited carbon nanotubes," *Nano Letters*, vol. 4, no. 4, pp. 604–606, 2004.

Appendix A

Appendix

A.1 Matlab Code for I_d versus V_{gs} and V_{ds} including Voltage Transfer Characteristics

```
% Shows the Id versus Vgs model first.
% Uses the matlab model for the subthreshold data and finds the input
% versus the output voltage for the VTC Curves.
% Variables from Excel spreadsheet–shown here for Diameters of 1.3nm,
% 1.9nm, and 2.5nm that were illustrated carefully in the thesis.
clear all;
close all;
Vdd=0.4;
%Dt=1.3nm: Original hn
% Dn=2.201112e-14; hn=16.19243; an3s=-2.23463; an2s=-6.80715; an1s=30.08726;
an3f=6.03125; an2f=-4.238; an1f=24.51749;
% Dp=Dn; hp=hn; ap3s=an3s; ap2s=an2s; ap1s=an1s; ap3f=an3f; ap2f=an2f; ap1f=an1f;
%Dt=1.3nm: No hn
% Dn=2.201112e-14; hn=15; an3s=-2.23463; an2s=-6.80715; an1s=30.08726;
an3f=6.03125; an2f=-4.238; an1f=24.51749;
% Dp=Dn; hp=hn; ap3s=an3s; ap2s=an2s; ap1s=an1s; ap3f=an3f; ap2f=an2f; ap1f=an1f;
```

```
%Dt=1.3nm: High hn
% Dn=2.201112e-14; hn=23.219; an3s=-2.23463; an2s=-6.80715; an1s=30.08726;
an3f=6.03125; an2f=-4.238; an1f=24.51749;
% Dp=Dn; hp=hn; ap3s=an3s; ap2s=an2s; ap1s=an1s; ap3f=an3f; ap2f=an2f; ap1f=an1f;
%Dt=2.5nm: Original hn
% Dn=5.412219e-10; hn=14.64483; an3s=-47.5701; an2s=-20.5114; an1s= 27.1745;
an3f=-34.96325; an2f=21.0253; an1f=3.13579;
% Dp=Dn; hp=hn; ap3s=an3s; ap2s=an2s; ap1s=an1s; ap3f=an3f; ap2f=an2f; ap1f=an1f;
%Dt=2.5nm: No hn
% Dn=5.412219e-10; hn=13.55; an3s=-47.5701; an2s=-20.5114; an1s= 27.1745;
an3f=-34.96325; an2f=21.0253; an1f=3.13579;
% Dp=Dn; hp=hn; ap3s=an3s; ap2s=an2s; ap1s=an1s; ap3f=an3f; ap2f=an2f; ap1f=an1f;
%Dt=2.5nm: High hn
% Dn=5.412219e-10; hn=21; an3s=-47.5701; an2s=-20.5114; an1s= 27.1745;
an3f=-34.96325; an2f=21.0253; an1f=3.13579;
% Dp=Dn; hp=hn; ap3s=an3s; ap2s=an2s; ap1s=an1s; ap3f=an3f; ap2f=an2f; ap1f=an1f;
%Dt=1.9nm: Original hn
% Dn=3.45151E-12; hn=15.4186; an3s=-24.9024; an2s=-13.6593; an1s=28.6309;
an3f=-14.4660; an2f=8.3936; an1f=13.8266;
% Dp=Dn; hp=hn; ap3s=an3s; ap2s=an2s; ap1s=an1s; ap3f=an3f; ap2f=an2f; ap1f=an1f;
%Dt=1.9nm: No hn
% Dn=3.45151E-12; hn=14.25; an3s=-24.9024; an2s=-13.6593; an1s=28.6309;
an3f=-14.4660; an2f=8.3936; an1f=13.8266;
% Dp=Dn; hp=hn; ap3s=an3s; ap2s=an2s; ap1s=an1s; ap3f=an3f; ap2f=an2f; ap1f=an1f;
%Dt=1.9nm: HIGH hn
% Dn=3.45151E-12; hn=22.10955; an3s=-24.9024; an2s=-13.6593; an1s=28.6309;
an3f=-14.4660; an2f=8.3936; an1f=13.8266;
% Dp=Dn; hp=hn; ap3s=an3s; ap2s=an2s; ap1s=an1s; ap3f=an3f; ap2f=an2f; ap1f=an1f;
%_____________________VGate-S__________________________
%NCHANNEL: Create the Vin versus log Id curve
```

```
zz_An=0;
xx_An=0;
for Vout_An = 0:.1:Vdd,
    zz_An=zz_An+1;
    Vout_array_An(zz_An)=Vout_An;
for Vin_An= 0:0.005:Vdd,
    xx_An=xx_An+1;
    Vin_array_An(xx_An)=Vin_An;
    Vmin_An=Vout_An/2;
    Vmin_array_An(xx_An, zz_An)=Vmin_An;
    saturation_pt_An(zz_An)=0.2 .* Vout_An + 0.2;
    deltaV_An=saturation_pt_An(zz_An)-Vmin_An;
    minus_sat_pt_An=Vmin_An-deltaV_An;
    Vds_An=Vout_An;
    %Finding the An_sat to be able to know Idn_minimum
        an_sat=( an3s .*Vout_An .* Vout_An) + (an2s .* Vout_An) + an1s;
        an_sat_array(zz_An)=an_sat;
        Id_An_sat = Dn.*exp(hn.*(Vds_An)) .* exp(an_sat.*
        abs(saturation_pt_An(zz_An)-Vmin_An));
        Id_An_sat_array(zz_An)=Id_An_sat;
    if Vin_An < minus_sat_pt_An %FLAT LEFT SECTION
        an(xx_An, zz_An)=( an3f .* Vout_An.*Vout_An) + (an2f .* Vout_An) + an1f;
        Id_An_Vin(xx_An, zz_An) = Id_An_sat .* exp(an(xx_An, zz_An).*
        abs(Vin_array_An(xx_An)-minus_sat_pt_An));
    elseif Vin_An > saturation_pt_An(zz_An) %FLAT AN
        an(xx_An, zz_An)=( an3f .* Vout_An.*Vout_An) + (an2f .* Vout_An) + an1f;
        Id_An_Vin(xx_An, zz_An) = Id_An_sat .* exp(an(xx_An, zz_An).*
        abs(Vin_array_An(xx_An)-saturation_pt_An(zz_An)));
    else %STEEP AN
        an(xx_An, zz_An)=( an3s .*Vout_An .* Vout_An) +(an2s .* Vout_An) + an1s;
```

```
        Id_An_Vin(xx_An, zz_An) = Dn .* exp(hn.*Vds_An) .
        * exp(an(xx_An, zz_An).* abs(Vin_array_An(xx_An)-Vmin_An));
    end
end
xx_An=0;
end
plot_var_limit_An=zz_An;
%P CHANNEL: Create the Vin versus log Id curve
zz_Ap=0;
xx_Ap=0;
for Vout_Ap = 0:.1:Vdd,
    zz_Ap=zz_Ap+1;
    Vout_array_Ap(zz_Ap)=Vout_Ap;
for Vin_Ap= 0:0.005:Vdd,
    xx_Ap=xx_Ap+1;
    Vin_array_Ap(xx_Ap)=Vin_Ap;
    Vds_Ap=Vdd-Vout_Ap;
    Vmin_Ap= Vdd-((Vds_Ap)/2);
    Vmin_array_Ap(xx_Ap, zz_Ap)=Vmin_Ap;
    saturation_pt_Ap(zz_Ap)=0.2 .* (Vout_Ap-Vdd) + 0.2;
    deltaV_Ap= Vmin_Ap - saturation_pt_Ap(zz_Ap);
    plus_sat_pt_Ap= Vmin_Ap + deltaV_Ap;
    %Finding the Ap_sat to be able to know Idn_minimum
    ap_sat=( ap3s .*Vds_Ap .* Vds_Ap)+(ap2s.* Vds_Ap) + ap1s;
    Id_Ap_sat= Dp.*exp(hp.*abs(Vds_Ap)) .* exp(ap_sat.*
    abs(saturation_pt_Ap(zz_Ap)-Vmin_Ap));
    Id_Ap_sat_array(zz_Ap)=Id_Ap_sat;
    if Vin_Ap > plus_sat_pt_Ap %FLAT Right SECTION–to right if there
        ap(xx_Ap, zz_Ap)=( ap3f .* Vds_Ap.*Vds_Ap)+(ap2f.* Vds_Ap) + ap1f;
        Id_Ap_Vin(xx_Ap, zz_Ap) = Id_Ap_sat .* exp(ap(xx_Ap, zz_Ap).*
```

```
        abs(Vin_array_Ap(xx_Ap)-plus_sat_pt_Ap));
    elseif Vin_Ap < saturation_pt_Ap(zz_Ap) %FLAT Left Section -always there
        ap(xx_Ap, zz_Ap)=( ap3f .* Vds_Ap.*Vds_Ap)+(ap2f.* Vds_Ap) + ap1f;
        Id_Ap_Vin(xx_Ap, zz_Ap) = Id_Ap_sat .* exp(ap(xx_Ap, zz_Ap).*
        abs(Vin_array_Ap(xx_Ap)-saturation_pt_Ap(zz_Ap)));
    else %STEEP AP
        ap(xx_Ap, zz_Ap)=( ap3s .*Vds_Ap .* Vds_Ap)+(ap2s .* Vds_Ap) + ap1s;
        Id_Ap_Vin(xx_Ap, zz_Ap) = Dp .* exp(hp .* abs(Vds_Ap)) .*
         exp(ap(xx_Ap, zz_Ap) .*  abs(Vin_array_Ap(xx_Ap)-Vmin_Ap));
    end
end
xx_Ap=0;
end
plot_var_limit_Ap=zz_Ap;
%____________________VDrain-S________________________
%NCHANNEL: Create the Vds versus log Id curve
zz_Bn=0;
xx_Bn=0;
for Vin_Bn = 0:0.005:Vdd,
zz_Bn=zz_Bn+1;
Vin_array_Bn(zz_Bn)=Vin_Bn;
for Vout_Bn= 0:0.00025:Vdd,
    xx_Bn=xx_Bn+1;
    Vout_array_Bn(xx_Bn)=Vout_Bn;
    Vmin_Bn=Vout_Bn/2;
    Vmin_array_Bn(xx_Bn, zz_Bn)=Vmin_Bn;
    saturation_pt_Bn(xx_Bn)=0.2 .* Vout_Bn + 0.2;
    deltaV_Bn=saturation_pt_Bn(xx_Bn)-Vmin_Bn;
    minus_sat_pt_Bn=Vmin_Bn-deltaV_Bn;
    Vds_Bn=Vout_Bn;
```

```
    %Finding the Bn_sat to be able to know Idn_minimum
    bn_sat=(an3s .*Vds_Bn .* Vds_Bn) +(an2s .* Vds_Bn) + an1s;
    IdBn_sat = Dn.*exp(hn.*(Vds_Bn)) .* exp(bn_sat.*
    abs(saturation_pt_Bn(xx_Bn)-Vmin_Bn));
    if Vin_Bn < minus_sat_pt_Bn %FLAT LEFT SECTION
        bn(xx_Bn, zz_Bn)=( an3f.* Vout_Bn.*Vout_Bn) +(an2f .* Vout_Bn) + an1f;
        Id_Bn_Vin(xx_Bn, zz_Bn) = IdBn_sat .* exp(bn(xx_Bn, zz_Bn).*
        abs(Vin_array_Bn(zz_Bn)-minus_sat_pt_Bn));
    elseif Vin_Bn > saturation_pt_Bn(xx_Bn) %FLAT An
        bn(xx_Bn, zz_Bn)=( an3f.* Vout_Bn.*Vout_Bn) +(an2f .* Vout_Bn) + an1f;
        Id_Bn_Vin(xx_Bn, zz_Bn) = IdBn_sat .* exp(bn(xx_Bn, zz_Bn).*
        abs(Vin_array_Bn(zz_Bn)-saturation_pt_Bn(xx_Bn)));
    else %STEEP AN
        bn(xx_Bn, zz_Bn)=( an3s .*Vds_Bn .* Vds_Bn) + (an2s .* Vds_Bn) + an1s;
        Id_Bn_Vin(xx_Bn, zz_Bn) = Dn .* exp(hn.*Vds_Bn) .*
    exp(bn(xx_Bn, zz_Bn).* abs(Vin_array_Bn(zz_Bn)-Vmin_Bn));
    end
end
xx_Bn=0;
end
plot_var_limit_Bn=zz_Bn;
%P CHANNEL: Create the Vin versus log Id curve
zz_Bp=0;
xx_Bp=0;
for Vin_Bp =0:0.005:Vdd,
    zz_Bp=zz_Bp+1;
    Vin_array_Bp(zz_Bp)=Vin_Bp;
    for Vout_Bp= 0:0.00025:Vdd,
        xx_Bp=xx_Bp+1;
        Vout_array_Bp(xx_Bp)=Vout_Bp;
```

```
        Vds_Bp=Vdd-Vout_Bp;
        Vmin_Bp= Vdd-((Vds_Bp)/2);
        Vmin_array_Bp(xx_Bp, zz_Bp)=Vmin_Bp;
        saturation_pt_Bp(xx_Bp)=0.2 .* (Vout_Bp-Vdd) + 0.2;
        deltaV_Bp= Vmin_Bp - saturation_pt_Bp(xx_Bp);
        plus_sat_pt_Bp= Vmin_Bp + deltaV_Bp;
        %Finding the Bp_sat to be able to know Idn_minimum
        bp_sat=( ap3s .*Vds_Bp .* Vds_Bp) + (ap2s .* Vds_Bp) + ap1s;
        Id_Bp_sat= Dp.*exp(hp.*abs(Vds_Bp)) .* exp(bp_sat .*
          abs(saturation_pt_Bp(xx_Bp)-Vmin_Bp));
    if Vin_Bp > plus_sat_pt_Bp %FLAT Right SECTION--to right if there
        bp(xx_Bp, zz_Bp)=( ap3f .* Vds_Bp.*Vds_Bp) + (ap2f .* Vds_Bp)+ ap1f;
        Id_Bp_Vin(xx_Bp, zz_Bp) = Id_Bp_sat .* exp(bp(xx_Bp, zz_Bp).*
          abs(Vin_array_Bp(zz_Bp)-plus_sat_pt_Bp));
    elseif Vin_Bp < saturation_pt_Bp(xx_Bp) %FLAT Left Section --always there
        bp(xx_Bp, zz_Bp)=( ap3f .* Vds_Bp.*Vds_Bp) + (ap2f .* Vds_Bp)+ ap1f;
        Id_Bp_Vin(xx_Bp, zz_Bp) = Id_Bp_sat .* exp(bp(xx_Bp, zz_Bp).*
          abs(Vin_array_Bp(zz_Bp)-saturation_pt_Bp(xx_Bp)));
    else %STEEP AP
        bp(xx_Bp, zz_Bp)=( ap3s .*Vds_Bp .* Vds_Bp) + (ap2s .* Vds_Bp)+ap1s ;
        Id_Bp_Vin(xx_Bp, zz_Bp) = Dp .* exp(hp .* abs(Vds_Bp)) .*
          exp(bp(xx_Bp, zz_Bp).* abs(Vin_array_Bp(zz_Bp)-Vmin_Bp));
end
% For the Vin_Vout_array
plot_var_Vout_Bp=xx_Bp;
end
xx_Bp=0;
end
plot_var_limit_Bp=zz_Bp;
%__________VTC Characteristics_____________
```

```
% Plot Vout versus Vin for the VTC characteristics
I_diff_array=log(Id_Bp_Vin)-log(Id_Bn_Vin);
plot_var_Vin_Bp=zz_Bp;
for plot_var_diff_array=1:1:plot_var_Vin_Bp,
    [Ival, index_dif]=min(abs(I_diff_array(:, plot_var_diff_array)));
    Aux_current(plot_var_diff_array) = Id_Bp_Vin(index_dif, plot_var_diff_array);
    Vout_Vin_array(plot_var_diff_array, 1)=Vin_array_Bp(plot_var_diff_array);
    index_dif_array(plot_var_diff_array)=index_dif;
    Vout_Vin_array(plot_var_diff_array, 2)=Vout_array_Bp(index_dif);
end
```

A.2 Matlab Code for ROM Capacitance Model

```
%The Capacitance Model
clear all;
close all;
% This is all done using nanometers!
% Define AREA variables:
    CNT_width=2.5;
    CNT_radius=CNT_width/2;
    metal_lines=128; % This is the number of gates the array–not including the pull up
transistor.
    ROM_width=128;
    CNT_per_tx=16;
    p= 0.025 % percent of CNTs that fail
for dd= 1: 1: CNT_per_tx,
    CNT_per_contact(dd)=dd;
end
    VDD=0.4;
    tox_bulk= 100;
```

```
    epsilon=8.85e-12.* 1e-9; % Farad / nanometer
    Eox_bulk= 3.9 .* epsilon;
    Eox_gate= 3.9 .* epsilon;
%TO CHANGE:
tox_gate=[1.1, .8, .65, .55, .5];
year_array=[2007, 2010, 2013, 2016, 2018];
max_index=length(year_array);
generatio_node=[65, 45, 32, 22, 18];
int_wire_width=[98, 68, 48, 33, 28];
int_wire_space=[97, 67, 47, 32, 27];
met_cont_ratio=7/10;
B_extra_chan_space=int_wire_width/4;
gate_overlap=[8, 5, 3, 2, 1];
%END OF CHANGE
for aa=1:max_index,
    int_contact_size(aa)=round(int_wire_width(aa)/met_cont_ratio);
    contact_length(aa)=round((2.*int_wire_space(aa))+int_contact_size(aa));
     contact_width(aa)=int_contact_size(aa);
    btwn_tx_width(aa)=int_wire_space(aa);
end
% Type A ROM array! this has the whole channel taken up by the contact, but also,
% there has to be extra contacts for the output node.
% Type B ROM array! This has the extra section made specifically for a
% metal gate or no metal gate. That way, we can just add the contact and if
% there is no gate, the cell will not be a transistor.
A_channel_length=int_contact_size;
%this is going to make sure B is going to be bigger than what A is
B_test_space=int_contact_size + 2.*B_extra_chan_space;
B_channel_length = B_test_space;
%_____________________Time Delay__________________________
```

```
for yr_num=1: max_index,
    % Capacitance Model:
    tr_ratio(yr_num)=tox_gate(yr_num)/CNT_radius;
    %tr_ratio=5
    theta_tube(yr_num)=asin(1/(1+tr_ratio(yr_num)));
    Cg_tube_chan_L(yr_num)=(2*pi*Eox_gate)/(log(tr_ratio(yr_num)+1)); % F/nm
    Cg_tube_Length(yr_num)=Cg_tube_part_chan_L(yr_num); % C per L
    Cg_tube_Length_femtoF(yr_num)=Cg_tube_Length(yr_num) .* 1e15; % C per L
%Gate parasitic to bulk per length
    A_Cg_parasitic_length(yr_num)=(Eox_bulk.*(contact_width(yr_num)))./
        tox_bulk;
    A_Cg_parasitic_length_femtoF(yr_num)=A_Cg_parasitic_length(yr_num).*1e15;
    B_Cg_parasitic_length(yr_num)=(Eox_bulk.*(contact_width(yr_num)))./
        tox_bulk;
    B_Cg_parasitic_length_femtoF(yr_num)=B_Cg_parasitic_length(yr_num).*1e15;
%Gate to nanotube capacitance
    A_Cg_chan_nanotube(yr_num)=(Cg_tube_Length(yr_num)).*
        A_channel_length(yr_num);
    A_Cg_chan_nanotube_femtoF(yr_num)=A_Cg_chan_nanotube(yr_num).* 1e15;
    B_Cg_chan_nanotube(yr_num)=(Cg_tube_Length(yr_num)).*
        B_channel_length(yr_num);
    B_Cg_chan_nanotube_femtoF(yr_num)=B_Cg_chan_nanotube(yr_num) .* 1e15;
%Gate to bulk capacitance
    A_Cg_chan_to_bulk(yr_num)=(A_Cg_parasitic_length(yr_num)).*
        A_channel_length(yr_num);
    A_Cg_chan_to_bulk_femtoF(yr_num)=A_Cg_chan_to_bulk(yr_num).*1e15;
    B_Cg_chan_to_bulk(yr_num)=(B_Cg_parasitic_length(yr_num)).*
        B_channel_length(yr_num);
    B_Cg_chan_to_bulk_femtoF(yr_num)=B_Cg_chan_to_bulk(yr_num) .* 1e15;
%Total Gate Capacitance
```

```
A_Cg_chan_tot(yr_num)=(Cg_tube_Length(yr_num)+
    A_Cg_parasitic_length(yr_num)).* A_channel_length(yr_num);
A_Cg_chan_tot_femtoF(yr_num)=A_Cg_chan_tot(yr_num).* 1e15; % fF
B_Cg_chan_tot(yr_num)=(Cg_tube_Length(yr_num)+
    B_Cg_parasitic_length(yr_num)).* B_channel_length(yr_num);
B_Cg_chan_tot_femtoF(yr_num)=B_Cg_chan_tot(yr_num) .* 1e15; % fF
%Cdrain to bulk capacitance
Cds_b(yr_num)=(Eox_bulk*(contact_length(yr_num).*
    contact_width(yr_num)))./tox_bulk;
Cds_b_femtoF(yr_num)= Cds_b(yr_num) .* 1e15;
%Gate to Source overlap capacitance
Cg_overlap(yr_num)=(Eox_gate*(gate_overlap(yr_num) .*
    contact_width(yr_num))) ./ tox_gate(yr_num);
Cg_overlap_miller(yr_num)=Cg_overlap(yr_num) .*2; % Miller effect
Cg_overlap_miller_femtoF(yr_num)=Cg_overlap_miller(yr_num).*1e15;
C_load_parasitic(yr_num)= (2.*Cg_overlap_miller(yr_num)) +
    Cds_b(yr_num);
C_load_parasitic_femtoF(yr_num)= C_load_parasitic(yr_num).* 1e15;
end
```


6075-11