

Germanium on Insulator Fabrication Technology

by

John Hennessy

B.S., Electrical Engineering (2002)

The Cooper Union for the Advancement of Science and Art

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

at the

Massachusetts Institute of Technology

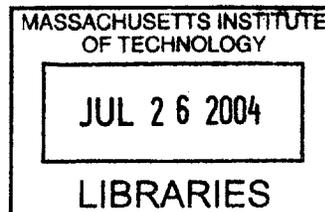
June 2004

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ABSTRACT

As CMOS devices continue to scale to smaller dimensions, it has become clear that new materials and structures are needed to also continue to improve performance. Germanium on insulator is proposed as it combines both a high mobility material (relative to silicon) and a structure with improved scaling characteristics compared to bulk devices. The goal of this work is to develop of procedure for the transfer of a germanium layer to bulk silicon by means of wafer bonding and hydrogen-induced layer transfer.

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Acknowledgments

I would like to thank my advisor, Dimitri Antoniadis, for his support over the course of this project and for giving me the opportunity to work in an interesting and rewarding environment. I would also like to thank Arthur Pitera whose work motivated this thesis, and who was instrumental in introducing me to the theory and fabrication steps needed for this work. I would also like to acknowledge the other members of the Antoniadis research group who aided my work: Andy Ritenour, Isaac Lauer, Osama Nayfeh, Scott Yu, Ali Khakifirooz, and Jae-Kyu Lee. I would like to thank Arthur Pitera and Larry Lee for the TEM preparation, and Ingvar Aberg for some discussions on wafer bonding. I would also like to thank the staff and faculty of the Microsystems Technology Lab for their help.

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Chapter 1

Introduction

As planar bulk Si CMOS devices continue to scale below 100 nm gate lengths, it has become clear that new structures and new materials are needed to continue to improve device performance. In this regard, Ge is a promising material because it possesses higher bulk electron and hole mobility than Si. Similarly, the on-insulator structure is also a good candidate for improved device performance due to the reduction of parasitic capacitances and the ability to use lightly doped channels. This work is a combination of both of these improvements, Ge on insulator (GeOI).

The first chapter presents the issues associated with scaling of bulk CMOS devices. This leads to the motivation for new structures, specifically the on-insulator structure. Silicon on insulator (SOI) devices are described with respect to their scaling properties and related benefits over bulk devices.

The second chapter presents Ge as an alternative to Si as the channel material. Aside from the mobility enhancement gained by switching to Ge, other benefits are also investigated to determine how the material properties of Ge affect the electrostatics of the on-insulator device.

The third chapter introduces some traditional techniques for the fabrication of on-insulator structures. Each procedure is discussed, and its possible application for GeOI fabrication is also considered.

The fourth chapter introduces some problems associated with working with Ge that affect processing decisions. Also, some of the techniques used in this work such as wafer bonding and chemical mechanical processing are discussed in more detail.

The fifth and final chapter proposes a fabrication technique for producing GeOI substrates. The results of this work are presented along with some conclusions and considerations for possible improvements.

1.1 CMOS Scaling

Table 1. 2003 ITRS scaling requirements for high-performance applications. [1]

Production Year	2003	2005	2007	2009	2012	2018
DRAM $\frac{1}{2}$ Pitch (nm)	100	80	65	50	35	18
Physical Gate Length (nm)	45	32	25	20	14	7
Oxide Thickness (nm)	1.3	1.1	0.9	0.8	0.7	0.5
V_{DD} (V)	1.2	1.1	1.1	1.0	0.9	0.7
Source/Drain Resistance (Ohm-μm)	180	180	162	144	116	60

The continued growth of the microelectronics industry has been the result of sustained increases in circuit speed, density, and complexity for each technology generation. These increases have been the result of the downsizing of the physical dimensions of each device, otherwise known as scaling. The benefits of scaling include lower device time constants, which allows for faster operation, and a reduction in area, which allows for a higher density of devices and for additional complexity in the circuit design. The limits of scaling have been predicted for gate sizes as large 1 μm in the 1970's, to as small as 100 nm a decade ago.[2] Fortunately these predictions have all proven to be false, but the fact remains that fundamental physical considerations will limit CMOS scaling sometime in the near future.

Typically scaling implies a reduction in the gate length of the device. However in order to maintain the electrostatic integrity of the transistor, several other parameters must also be modified. Electrostatic integrity is often quantified by two parameters, the subthreshold swing and the amount of drain-induced barrier lowering (DIBL). The subthreshold swing, SS , of a transistor characteristic is a measure of how abruptly a device can turn on and off as the gate voltage changes. DIBL is a measure of how much the threshold voltage, V_{th} , depends on V_{DS} . Ideally SS and V_{th} should not vary with the drain voltage. However as devices get smaller, these variations with changing drain bias get larger as does their negative impact on device performance.

To combat these short channel effects, the thickness of the gate oxide, the depth of the source/drain junctions, and the supply voltage all must also be reduced. Non-uniform doping profiles of high concentrations are also needed to control the threshold

voltage. In other words, the general goal of scaling is to extract a maximum I_{on} for a given amount of DIBL, and a given I_{off} . However, these scaling trends are leading to several key barriers in both performance and manufacturability.

First, the gate oxide has already been scaled to a physical thickness near 1 nm.[1] Not only is this approaching the physical limit of a single monolayer of SiO_2 , but also tunnel leakage currents increase exponentially with shrinking oxide thickness. This leakage will likely limit the application of SiO_2 gate dielectrics in MOSFETs beyond the 45nm technology generation.[3]

Increased channel doping and reduction of the S/D junction depth can help control short channel effects, but both may also limit performance. Increasing the channel doping reduces channel mobility due to increased impurity scattering. Making shallow and abrupt junctions increases source/drain resistances because of doping level limits and introduces manufacturing difficulties.

1.2 Silicon on Insulator (SOI)

For many decades CMOS transistors have been fabricated on bulk Si wafers. Si has dominated the CMOS industry because of the ability to produce high quality single crystal wafers of the material, as well as the inherently good native oxide formed on Si.

Bulk transistors are manufactured on wafers that are nearly one millimeter thick, yet the device region is often confined to only the very top few microns of the substrate. This geometry can often lead to unwanted parasitic effects. Figure 1 illustrates the difference between bulk CMOS and SOI CMOS. In the bulk case, unwanted interactions may occur between the various pn junctions leading to problems like CMOS latch-up and punchthrough. Manufacturing techniques like trench isolation can limit some of these effects, but also take up additional area on the wafer. In the SOI case, each device is dielectrically isolated from the others. Not only does this eliminate parasitic interactions, but it also decreases the required device area and allows devices to be made much closer to each other.

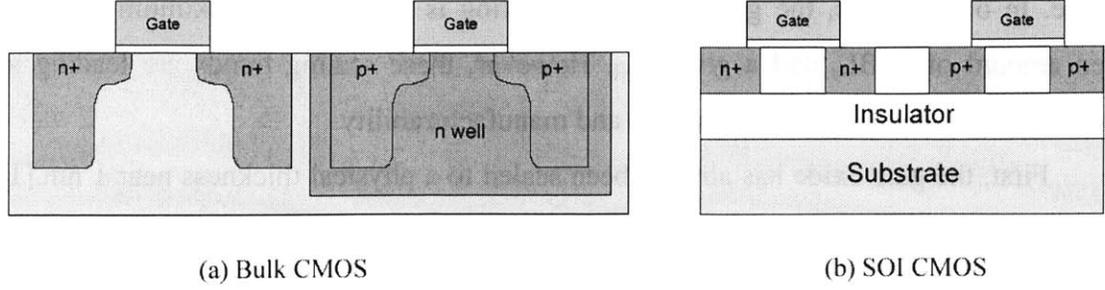


Figure 1. Cross section comparison of bulk CMOS and SOI CMOS.

In a bulk device the source or drain junction capacitance is given by [4]

$$C = \sqrt{\frac{q\epsilon_{Si}N_aN_d}{2(N_a + N_d)(\Phi_{bi} - V_d)}}, \quad (1)$$

where V_d is the junction voltage, Φ_{bi} is the built in junction potential, ϵ_{Si} is the dielectric constant of Si, N_a and N_d are impurity concentration in the drain and substrate regions, and q is the electronic charge. In the on-insulator structure the source/drain to substrate pn junctions are eliminated. The junction capacitance now looks like an MOS capacitor and is given by [4]

$$C = \frac{C_{box}}{\sqrt{1 + \frac{2C_{box}^2 V_d}{qN_a \epsilon_{Si}}}}, \quad (2)$$

where C_{box} is the capacitance of the buried oxide layer, and the same type of doping is assumed for the substrate as for the channel. This represents a reduction in the junction capacitance by roughly one order of magnitude. This reduction means that the time constant associated with charging and discharging this capacitance has also been reduced, allowing for the faster operation of the on-insulator devices.

The introduction of a buried oxide layer may also lead to a reduction in short-channel effects. In general, the subthreshold swing can be given as

$$SS = \frac{dV_{GS}}{d(\log I_D)} \approx \frac{kT}{q} \left(1 + \frac{C_b}{C_{ox}} \right) \ln 10, \quad (3)$$

where C_{ox} is the gate oxide capacitance and C_b is the capacitance between the inversion layer and the back electrode. In bulk devices $C_b \approx C_d$, the capacitance of the depletion region. The same is true for partially depleted SOI because the maximum width of the

depletion region, x_{dmax} , is still less than the thickness of the device layer. For fully depleted devices, $t_{Si} < x_{dmax}$, so $C_b \approx C_{Si} + C_{ox2}$, where C_{Si} is the capacitance the device layer, and C_{ox2} is the capacitance of the buried oxide. This again is a significant reduction in capacitance and allows the subthreshold swing to approach the thermal limit of

$$SS = \frac{kT}{q} \ln 10 = 60 \frac{mV}{decade} . \quad (4)$$

Minimization of the subthreshold slope means that the on/off current ratio has been maximized, and thus would potentially allow for a lower operating voltage to meet the same off current target as the bulk case, or a higher drive current for the same supply voltage.

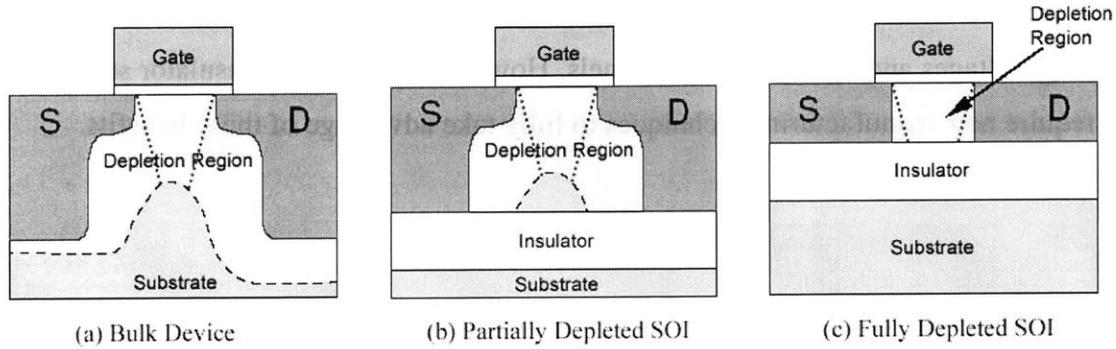


Figure 2. Comparison of depletion effects in bulk devices, PDSOI, and FDSOI.

Ideally the channel depletion charge should be completely controlled by the gate. However, due to encroachment of the source and drain regions, part of this charge is no longer controlled entirely by the gate. For short devices the portion of the charge controlled by the source and drain can become very significant, leading to a reduction in the threshold voltage, otherwise known as V_{th} roll-off. In Figure 2a, the dotted lines represent the portion of the depletion region controlled by the source and drain. In the bulk case, the depletion charge controlled by the source and drain is a significant percentage of the entire depletion charge. When the source and drain has enough influence over the depletion charge, they begin to modulate the threshold voltage. Figure 2c indicates that for the same amount of “control” by the source and drain, and the same

gate length, the influence on the depletion charge is much smaller in an on-insulator structure.

For very thin device layers the gate has very good electrostatic control of the channel. This means there is no longer a need for high channel doping to control the threshold voltage roll-off. Instead lightly doped or undoped channels could be used, which would decrease impurity scattering and increase carrier mobility. However, this would require that the threshold voltage be controlled by the gate workfunction, which increases the manufacturing complexity.

To summarize, fully depleted SOI has several key benefits over bulk technologies. The structure of the SOI substrate allows for smaller device area and increased packing density. A reduction in parasitic capacitances allows for faster operation. And reduced short channel effects could potentially allow for the use of lower operating voltages and lightly doped channels. However ultra-thin on-insulator structures may require new manufacturing techniques to fully take advantage of these benefits.

Chapter 2

Germanium vs. Silicon

Bulk Si MOS devices have been the dominant components of the microelectronics industry for decades. Chapter 1 illustrates how continued device scaling has led to improved performance. Nevertheless, it has become clear that limits of scaling bulk devices will soon be reached. As the benefits of scaling subside, one approach to extract performance gains may be to attempt to improve the carrier transport, mainly through increased mobility.

There are several approaches being taken now to increase mobility relative to bulk Si devices. One approach is the incorporation of strain in the Si channel. This is often accomplished by the epitaxial growth of Si on a material with a different lattice constant.[5] Another method is the use of silicon-based heterostructures where electrons and holes may not be confined to same material.[6] Another choice is to simply replace Si as the channel material with something that possesses a higher electron and hole mobility such as Ge.

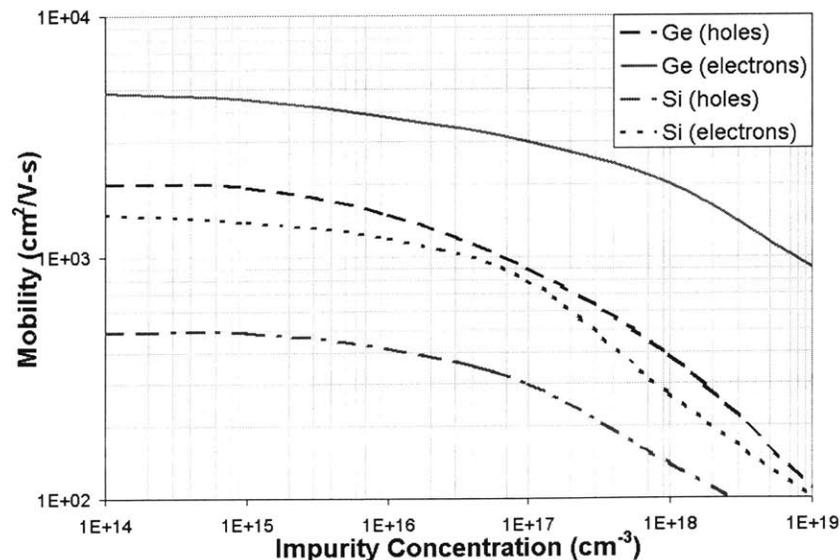


Figure 3. Comparison of bulk drift mobilities for Ge and Si versus impurity concentration. (After Sze [7].)

Figure 3 shows a comparison of the drift mobilities for bulk Si and bulk Ge. Ge possesses roughly a 2x increase in electron mobility and a 4x increase in hole mobility. This is the primary reason for the investigation of Ge as alternative to Si. Recently there has much interest in the characterization of bulk Ge MOSFETs. Hole mobility enhancements up to 2x higher than Si have been observed.[8][9]

It is expected then that a performance benefit can be gained by simply changing materials. However, Ge and Si differ in many more ways than a variation in carrier mobility. Table 2 summarizes some of the key material differences between Ge and Si. How will these differences affect the electrostatics of device operation? Is there an additional benefit from these changes, or do they offset the gains achieved by the increase in carrier mobility. To investigate the electrostatic effect of these parameters, both bulk and thin on-insulator devices were simulated using the DESSIS device simulator.[10]

Ge Bulk devices were simulated using a modification of the 50nm well-tempered Si MOSFET.[11] The ultra-thin on insulator device used a single metal gate and nominally undoped channels. The gate workfunctions were modified for Ge and Si to match I_{off} in the bulk Si case. All devices were simulated using standard drift-diffusion models. Quantum and hydrodynamic effects were not considered as it was expected that their impact on short-channel electrostatic effects would be small.

Table 2. Material differences that have a significant impact on electrostatic integrity.

	Ge	Si
Energy Gap (eV)	0.66	1.12
Dielectric Constant	16.0	11.9
Intrinsic Concentration (cm⁻³)	2.4×10^{13}	1.45×10^{10}

The maximum depletion width can be given by

$$x_{d \max} = \sqrt{\frac{4\epsilon_{Si}\phi_F}{qN_a}}, \quad (5)$$

where ϵ_{Si} is the dielectric constant of the material, ϕ_F is the Fermi potential, and N_a is the channel doping. The Fermi potential is given by

$$\phi_F \approx \frac{2kT}{q} \ln\left(\frac{N_a}{n_i}\right), \quad (6)$$

where n_i is the intrinsic carrier concentration of the material. In Ge, n_i is much larger than in Si, so the Fermi potential is lower. The dielectric constant is higher, but not enough to offset the effect of ϕ_F , so x_{dmax} is also lower in Ge. The capacitance of the depletion region in inversion is

$$C_d = \frac{\epsilon}{x_{dmax}}, \quad (7)$$

so for Ge this value is always larger than for Si. And therefore from Eq. 3, the subthreshold swing is also larger for bulk Ge devices. Figure 4 shows that the simulation predict this trend for short-channel bulk devices.

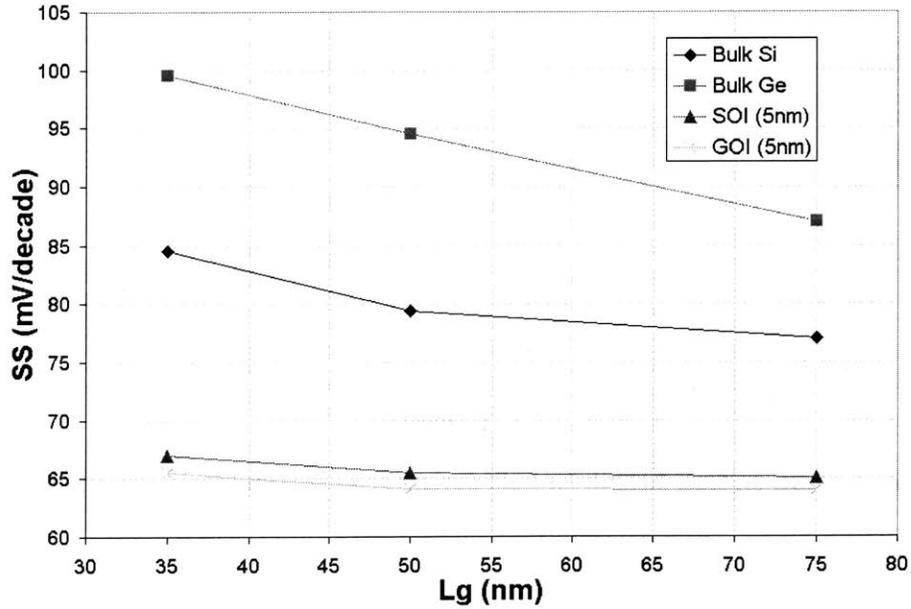


Figure 4. SS vs. gate length for bulk devices and ultra-thin on-insulator devices.

DIBL is harder to quantify analytically, but is strictly defined as the change in threshold voltage per volt of change in the drain bias. Several expressions have been developed to model the change in threshold as a function of V_{DS} , one example is [12]

$$\Delta V_T \approx -[3(\phi_{bi} - 2\phi_F) + V_{DS}]e^{-L/\lambda} \quad (8)$$

where ϕ_{bi} is the built-in potential, and λ is a characteristic length for the channel given by

$$\lambda = \sqrt{\frac{\epsilon t_{ox} x_{dmax}}{\epsilon_{ox}}}. \quad (9)$$

The built in potential for Ge is lower than Si due to the smaller bandgap. However the more important term in the threshold voltage shift is the exponential dependence on λ . Again note that x_{dmax} for Ge is lower, but λ is ultimately higher due to the difference in dielectric constants. This suggests that for small gate lengths the DIBL for Ge is higher than for Si. Figure 5 shows that this is also true.

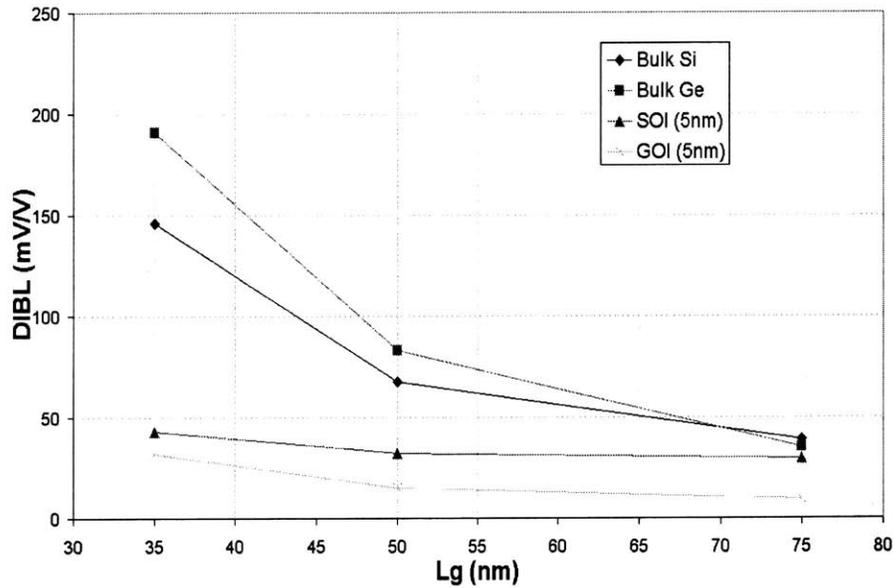


Figure 5. DIBL vs. Gate Length for bulk devices and ultra-thin on-insulator devices.

For the ultra-thin on insulator devices the results are quite different. Now the maximum depth of the depletion region and the depletion capacitance are fixed by the structure. Therefore it is expected that the subthreshold swing will approach 60 mV/decade for both Ge and Si, and Figure 4 indicates that this is approximately true. In the case of DIBL, the characteristic length is now only dependent on the value of ϵ for each material. Again this is higher for Ge, but the value of λ compared to the bulk case has now been lowered because x_{dmax} has been fixed to the thickness of the device layer. Now the benefits of the lower bandgap outweigh the change in λ , so it is expected that Ge

will have less DIBL than Si. The simulations shown in Figure 5 also predict this, but it is also noted that the DIBL benefit for Ge is shrinking for smaller gate lengths.

The change in the short-channel effects in Si and Ge due to material differences can be viewed as a competition between the benefits of Ge's lower bandgap and the disadvantages of Ge's higher dielectric constant. For bulk devices the effect of a large dielectric constant is much more significant due to its impact on the depth of the depletion region and therefore the depletion capacitance. In ultra-thin on insulator devices the impact of ϵ is nullified by ensuring t_{Si} is less than x_{dmax} .

Chapter 3

Fabrication of SOI

Part of the reason Si is such a successful component of the microelectronics industry is the ability to produce high quality, defect free, single crystal wafers. It is considerably more challenging to produce a high quality thin layer of silicon on top of an insulated substrate. Nevertheless, several techniques have been developed for producing on-insulators structures. This section reviews some of these technologies and considers their application in producing GeOI.

3.1 Epitaxy

SOI substrates can be obtained by epitaxial growing a silicon layer on a single-crystal insulator. Silicon on sapphire (SOS) is one example of this type of material. In fact, prior to the 1980's, SOS was the only on-insulator structure to successfully incorporate large-scale integrated circuits.[4]

The starting material is a single crystal, insulating wafer such as sapphire. Then a thin layer of silicon is deposited using silane or dichlorosilane at temperatures near 1000 °C. Due to the lattice mismatch between silicon and sapphire, it is hard to grow high quality thin epitaxial layers. Also, the thermal mismatch between the two materials can result in unwanted stress in the film and additional defects. Both of these defects tend to reduce the mobility of carrier in SOS devices compared to bulk Si.

Although several techniques have been developed to reduce the effect of these issues, this option is still not particularly suitable for deeply scaled CMOS. Due to large concentration of defects at the film/buried oxide interface, this technique is especially unsuitable for ultra-thin on-insulator structures.

3.2 The Recrystallization Method

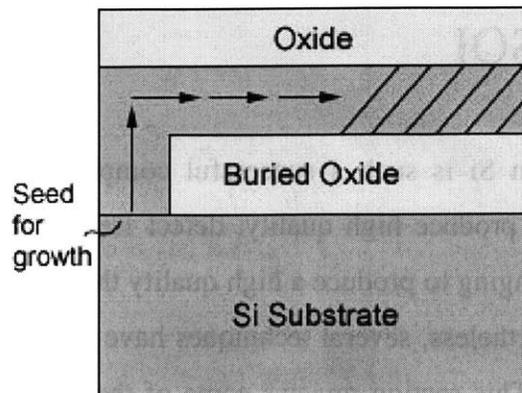


Figure 6. Regrowth of SOI layer by lateral liquid or solid phase epitaxy.

The recrystallization method is based on the crystallization of an amorphous silicon layer that has been deposited on an oxidized handle wafer. It is analogous to liquid or solid phase epitaxy, except that in this case the growth occurs laterally across the wafer surface. The growth is started by contacting the deposited film to a small seeding region on the substrate. Growth is initiated vertically from the seeding region, and then continues laterally over the oxide layer. The crystal orientation of the device layer is determined by the underlying substrate.

The greatest benefit of this method is its potential application in fabricating 3D integrated circuits.[13] Another silicon layer could be deposited on top of the structure shown in Figure 6, and regrowth of that layer could also take place. For this reason solid-phase epitaxy is more attractive from a temperature standpoint, especially in Si processing. The high temperature required for liquid-phase epitaxy would redistribute dopants and otherwise damage underlying layers. Solid-phase epitaxy can limit processing temperature to below 600 °C.

One difficulty with this technique is producing a defect-free device layer over large areas. If the lateral growth is too slow, random nucleations in the device layer disrupt the crystalline growth. Typically, perfect crystal growth is possible over tens of microns. Regrowth over the entire wafer surface is possible using methods like zone-

melting recrystallization.[14] However, this typically requires complex processing tools, and is not suitable for the fabrication of ultra-thin films.

This technique does have potential applications in the fabrication of GeOI. Recently, growth of single-crystal GeOI was reported by means of lateral liquid-phase epitaxy.[23] Section 5.1 presents a more detailed description of this work.

3.3 SIMOX

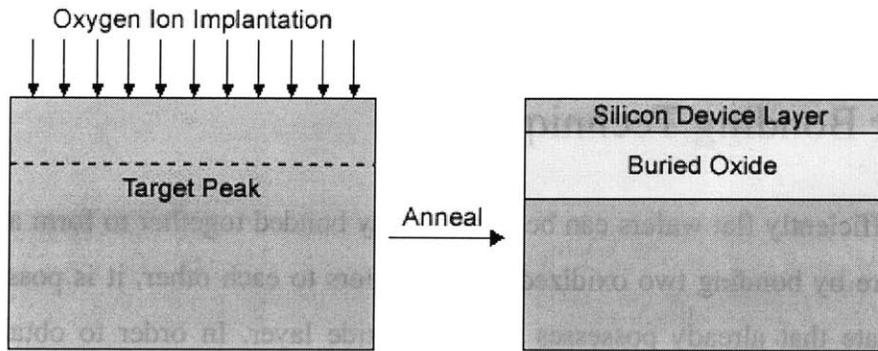


Figure 7. SOI substrate created by oxygen implantation.

SIMOX is an acronym that stands for “separation by implanted oxygen”. A bulk Si wafer is implanted with oxygen ions and a subsequent anneal leads to the formation of a buried oxide layer. This technique has the benefit of using a single wafer, but it does require a high energy, large dose implant. Ion implantation of Si is routinely used for source and drain implants. The same concept is used for SIMOX, but instead of implanting donor or acceptor impurities, ionized oxygen is implanted.

The dose must be high enough to introduce two oxygen atoms for every silicon atom in the region that becomes the buried SiO_2 layer. This typically requires a dose in the 10^{17} to 10^{18} cm^{-2} range, which is several orders of magnitude greater than the normal dose for source/drain implants. Also, source/drain implants are intended to produce a peak implant profile near the surface of the wafer, while a SIMOX implant requires a peak up to several hundred nanometers from the surface. This requires a high-energy implant, which combined with the high dose may result in significant damage to the silicon crystal structure. However, optimization of the implant conditions (e.g.

temperature) and of subsequent annealing parameters can greatly reduce the final number of defects.

This technique is not suitable for the production of GeOI substrates. First, for economic reasons it is not favorable to use an entire bulk Ge wafer as the substrate. Ideally, a thin region of the Ge could be used as the device layer while the substrate (most of the material) would be a cheaper material like Si. This is something that is not straightforward to achieve with the SIMOX technique. Also, even if one were to use a bulk Ge wafer, the implanted oxygen would not likely create a suitable buried oxide. Compared to SiO_2 , GeO_2 is not a stable and electrically robust oxide.

3.4 Wafer Bonding Techniques

Two sufficiently flat wafers can be permanently bonded together to form a single wafer. Therefore by bonding two oxidized silicon wafers to each other, it is possible to create a substrate that already possesses a buried oxide layer. In order to obtain thin channels it is necessary to reduce the thickness of the top wafer, which can be accomplished by two methods described in this section. The specifics of wafer bonding are described in more detail in Section 4.2.

3.4.1 Bond and Etch Back (BESOI)

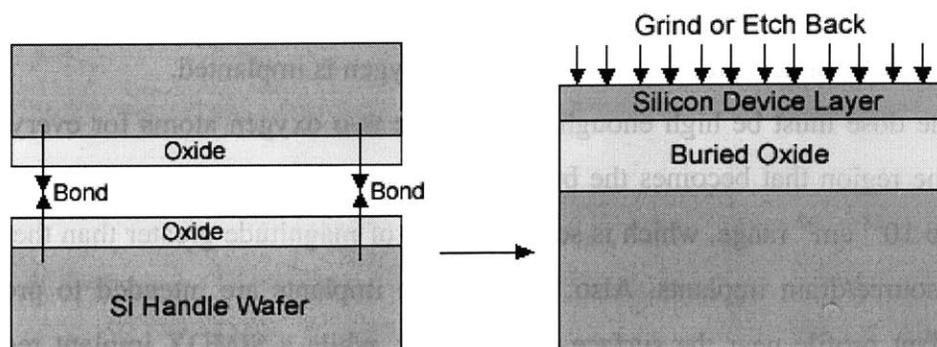


Figure 8. The bond and etch back technique.

Following the bonding of two wafers, the top wafer must be sufficiently thinned down to create a useful SOI substrate. This involves removing what is essentially an entire wafer's worth of material, typically around 600 μm . One approach is to grind the majority of the wafer away, and then polish the remaining silicon to produce a uniform surface. This technique is simple but it is difficult to control the thickness of the device layer, making it even more complicated to produce ultra-thin channels.

A more accurate method involves the use of an etch stop region to control the device layer thickness. The initial silicon wafer incorporates an etch stop region that differs from the device layer in either doping concentration or material. For example, the device wafer may be implanted to create a highly doped layer at the surface. Then, a lightly doped epitaxial silicon layer that eventually becomes the device region is grown on top. After bonding and grinding back the wafer, a chemical etch can be used that stops on the device layer with high selectivity. This allows for the development of almost arbitrarily thin device layers.

The advantage of BESOI over the previous methods is that the final device layer should be identical to the original crystalline silicon. There is no damage associated with a high-energy implant, and no defects should be created at the Si/buried oxide interface. It also allows for the possibility of creating a device layer of a different material than the substrate, something that is not simple to achieve with the SIMOX technique.

One noticeable drawback of BESOI is the requirement of the two entire wafers to produce one substrate. This may affect the economics of using this method in industry, especially if a more expensive material like germanium is substituted for silicon. Another drawback of using this method for the production of GeOI is that two entire wafers are direct bonded together and then annealed. As discussed in Chapter 4, one of the major difficulties of producing GeOI by wafer bonding methods is the mismatch between the thermal coefficients of expansion for Ge and Si. In order to use BESOI to make GeOI it would be necessary to develop a high quality, low temperature bonding procedure. Even then it would require grinding away a large portion of expensive material.

3.4.2 Hydrogen Implantation

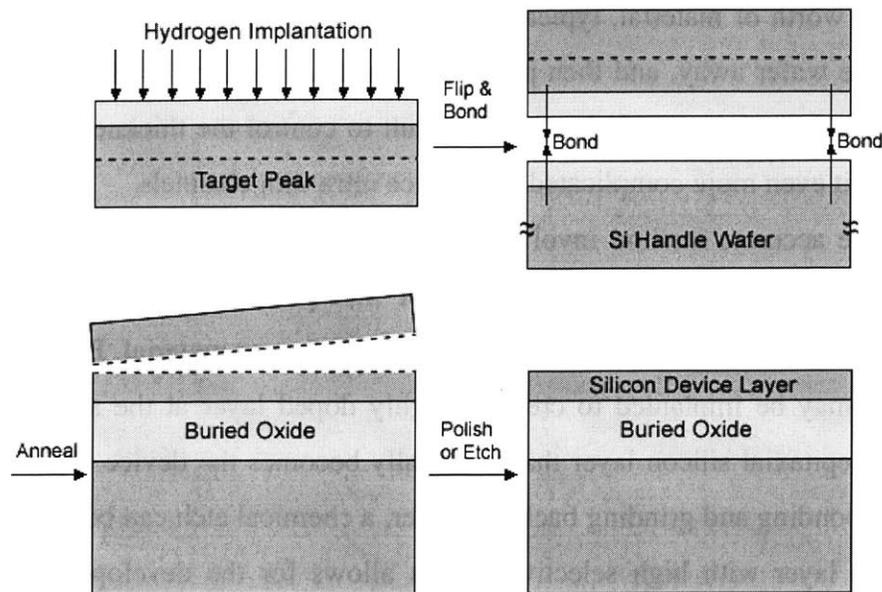


Figure 9. Hydrogen implantation occurs prior to bonding, then a layer is transferred following the anneal.

This method addresses some of the drawbacks associated with BESOI. The procedure is similar, but the top wafer is now removed by activating a hydrogen implant that splits the wafer pair at a predetermined depth. This is known commercially as the SmartCut[®] process.

First the top wafer is implanted with hydrogen ions at a typical dose on the order of $5 \times 10^{16} \text{ cm}^{-2}$. The energy of the implant determines where the peak occurs and therefore where the wafer ultimately splits. The wafers are cleaned and bonded as per the typical procedure. The first thermal treatment splits the implanted wafer, transferring a layer that remains bonded to the handle wafer. The next thermal treatment can then be applied at a higher temperature to strengthen the bonded interface.

The initial implantation damages the crystal structure of the implanted wafer and small platelets of hydrogen gas form around the damaged area. As the temperature is increased after bonding, these platelets begin to grow in size and form microcracks centered around the peak of the implant. Eventually these cracks merge and propagate over the entire wafer area, leading to the separation of the implanted wafer.[15] The dose of the implant controls the time and temperature necessary to split the wafer.

This technique has several benefits over BESOI. First, after the layer is transferred, the top wafer can be polished and reused as the new handle wafer. So while BESOI requires $2N$ wafers for N substrates produced, this technique only requires $N+x$, where x is less than N and depends on the number of times the implanted wafer can be reused. Secondly, because the layer transfer can take place at a relatively low temperature, this technique can be used to transfer a layer of almost any material to a silicon handle. In the case of GeOI fabrication, the top wafer would be Ge and could potentially be reused a number of times.

Chapter 4

GeOI Processing

This chapter is meant to introduce the techniques used in this work for producing germanium on insulator. Some of the difficulties associated with working with Ge are discussed. Wafer bonding and chemical mechanical polishing are described in more detail, with the motivation of producing a high quality bonded interface.

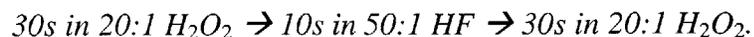
4.1 Germanium Processing

The production of GeOI would be fairly straightforward if the material parameters of Ge were the same as the intended substrate, Si. That way standard Si chemistries could be used in the cleaning steps, and typical annealing temperatures could be used for film densification and bonding. Table 3 indicates some of the material parameters that affect the ability to easily process Ge.

Table 3. Material properties of Ge and Si that affect processing. [7]

	Ge	Si
Melting Point (°C)	937	1415
Lattice Constant (Å)	5.646	5.431
Linear Coeff. Of Thermal Expansion at 300K (1/K)	5.8×10^{-6}	2.6×10^{-6}
Density (g/cm³)	5.33	2.33
Knoop Hardness (kg /mm²)	780	1150
Fracture Toughness (MPa *m^{1/2})	0.66	0.95

First, Ge is rapidly etched in any peroxide solution, making it incompatible with standard RCA or piranha cleans. At present, the best option for cleaning Ge surfaces appears to be a cyclic etch in dilute H₂O₂ and HF. This has been determined to significantly reduce residual impurities on Ge surfaces as long as the last step is an H₂O₂ dip.[19] For this work any cleaning of the Ge surface used the following procedure:



Although this does reduce contamination, it also etches Ge. For ultra-thin applications an alternative clean may be necessary.

The melting point of Ge is significantly lower than that of Si. Typically, deposited oxide densification, or post-bond anneals take place at 1000 °C, which is clearly unacceptable when processing Ge. This may limit the maximum bond energy that can take place when direct bonding bulk Ge, but it can also lead to problems in properly densifying deposited oxides on Ge.

Another bonding issue results from the mismatch in the coefficient of thermal expansion for Ge and Si. During the post-bond anneal, the Ge expands more than twice as much as the Si wafer. This may result in debonding, or more likely will result in wafer breakage. Table 3 also indicates that Ge is significantly easier to break than Si, and also much heavier. This requires delicate handling of Ge wafers to prevent breakage. This also means that as the wafers bow from thermal stress, the germanium wafer is more likely to fracture.

4.2 Wafer Bonding

Clean, flat wafers of almost any material can be bonded together by simply bringing the surfaces into contact with each other. This “bonding” is the result of attractive van der Waals forces that locally pull the materials together.[16] This technique has been used since the eighties in the fabrication of SOI structures.

The measure of the flatness of a bonded surface indicates how much the surface deviates from an ideally flat reference plane. Flatness is a macroscopic quantity that depends on variation in the thickness of a wafer as well as large scale wafer bow. Even if the flatness of the wafer varies several micrometers, successful bonding can still be achieved because the wafer pair deforms in order to achieve a conformal bonded interface. Bonding studies have indicated that flatness variations up to 25 μm do not prevent a successful bond.[17] Attempting to bond wafers with larger variations typically results in unbonded areas.

A more important measure is the microscopic smoothness of a wafer surface. This is often quantified as surface roughness; wafers that exceed a critical surface roughness are no longer bondable. For typical silicon direct bonding, it has been seen that bonding occurs if the root mean square (rms) surface roughness is less than 0.5 nm.[16] Prime polished silicon wafers have an rms roughness that is on the order of 0.1-0.2 nm. This makes room temperature direct bonding of bulk silicon wafers straightforward. Thermal oxidation of these wafers does not appreciably increase the roughness. However, deposition of oxide films by various techniques generally results in a surface roughness greater than 1.5 nm as shown in Figure 10. In order to achieve a high quality bond with these materials, a polishing step is necessary to reduce the surface roughness.

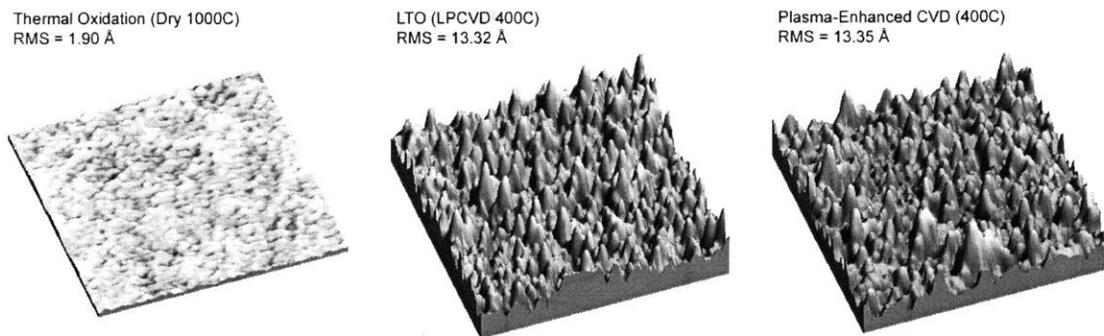
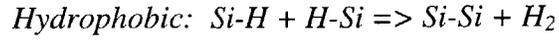
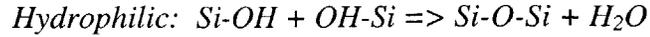


Figure 10. Surface roughness comparison of oxide layers on silicon.

Lastly a high quality bond requires surfaces that are free from chemical or particle contamination. Particles at the bond interface result in trapped bubbles or voids at the interface. For this reason, bonding must be carried out in a clean room environment. Chemical contaminants on the surface may also result in unbonded areas by interfering with the bond reaction. Typically the surface of each wafer is chemically conditioned before bonding. Depending on the conditioning used, the reaction at the interface is usually one of two forms: hydrophilic surfaces which are terminated in OH-groups, or hydrophobic surfaces which are terminated with hydrogen atoms. In the case of silicon direct bonding the following reactions would characterize these surfaces:



The cleaning steps taken immediately prior to the bond determine whether the surface is characterized as hydrophilic or hydrophobic. An RCA clean without an HF dip leads to a thin native oxide on the wafer surfaces, and therefore a hydrophilic bond. If an HF dip is used, the native oxide is removed and the resulting surface is hydrophobic. A bond involving SiO₂ as one of the surfaces is classified as hydrophilic.

The bonding procedure used in this work is classified as a direct bond. First, the wafers are aligned and brought into close proximity to one another in an EV aligner. Contact is initiated in the center of the wafer pair by bowing the top wafer and pressing it against the bottom wafer. A pressure of 0.3 bar is maintained while the top wafer is released, and the bond propagates to the edge of the wafer pair. The pressure is held for two minutes to ensure that bond has completed traveling along the interface.

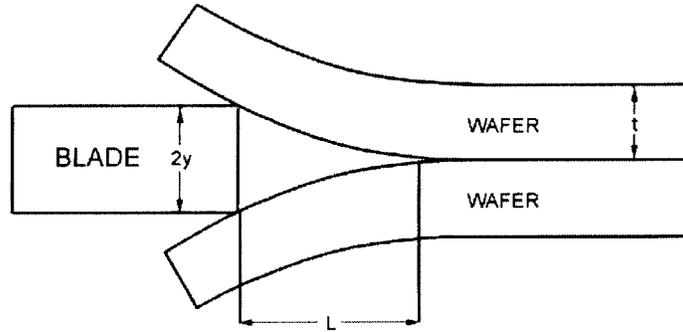


Figure 11. Crack length technique to measure bond energy. (After [18]).

The quantification of a “good bond is typically reported in terms of the bond energy. A simple method can be used to estimate the effective surface energy at the bonded interface. A razor blade is inserted between the bonded wafers in order to initiate a crack along the interface as shown in Figure 11. The bond energy can then be expressed as [18]

$$\gamma = \frac{3 Et^3 y^2}{8 L^4}, \quad (10)$$

where E is the modulus of elasticity, t is the thickness of the wafer, 2y is the thickness of the blade, and L is the measured crack length. Figure 12 shows the results of using the

crack open method to estimate bond energy. The wafer pair of the left is thermally oxidized Si bonded directly to Si. On the right is a wafer with deposited oxide of and a surface roughness of approximately 0.5 nm. The bond energy goes like the inverse of the crack length to the fourth power. Therefore in the case of Figure 12 the wafer pair on the right has a bond energy of slightly less than half that of the wafer pair on the left.

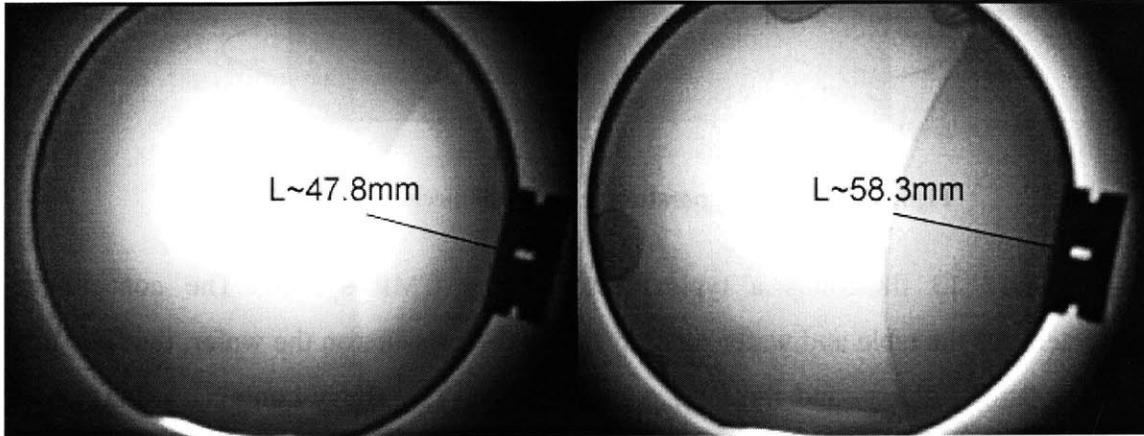


Figure 12. IR spectrograph showing crack length method, and illustrating the relative bond energy for wafers of different surface roughness.

4.3 Chemical Mechanical Polishing (CMP)

The surface roughness of deposited oxide films must be reduced to be of use in direct bonding applications. One method of accomplishing this is called chemical mechanical polishing. Ideally this process should produce a globally flat and smooth wafer surface without contaminating or otherwise damaging the film.

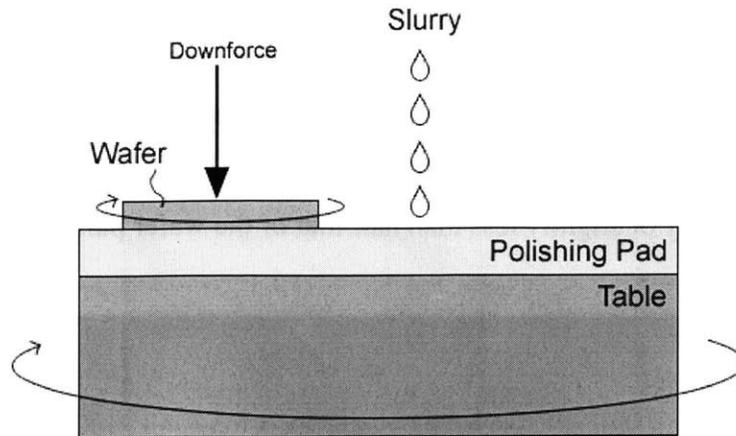


Figure 13. Typical apparatus for chemical mechanical polishing.

Figure 13 illustrates a typical setup for a CMP system. The controllable parameters are the table and wafer rotation speed, the pressure on the wafer, the flow rate of the polishing slurry, and the total polishing time. The slurry contains a mixture of abrasive SiO_2 particles, and a dilute chemical etching agent like HF or KOH. The etching agent reacts with the oxide layer to form a hydrated silicate layer that is then abraded away by the suspended particles and contact with the pad.[20] Because the formation and removal of the silicate layer is dependent on pressure, this process removes higher points on the surface selectively over lower points, ideally resulting in a planar surface. The minimum surface roughness that can be achieved is dependent on the diameter of the abrasive particles, the polishing pressure, and some material properties of the wafer. For a typical system the minimum surface roughness that can be attained with CMP is approximately 0.3 nm. [20]

Table 4. Polishing characteristics for various oxides. Polish conditions were 3.5psi wafer pressure, 1.5 psi table pressure, for 25s and 45s.

	Removal Rate ($\text{\AA}/\text{min}$)	Original Uniformity (%)	Post-polish Uniformity 25s (%)	Post-polish Uniformity 45s (%)
Thermal Oxide (1000°C)	325	0.8	4.2	8.2
LPCVD Oxide (400°C)	445	6.0	8.5	14.6
PECVD Oxide (400°C)	405	1.6	6.0	8.0

The CMP system at MIT’s Microsystems Technology Laboratory (MTL) is composed of a Rodel IC1000[®] polishing pad, and Cabot Semi-Sperse[®] 25 slurry. This is a silica-based slurry that uses a KOH suspension. Table 4 shows the removal rates for various oxide films and different polishing conditions. Figure 14 shows how these conditions affect the surface roughness of a deposited oxide film. Note that although the surface roughness is decreased, the overall film uniformity has worsened. As discussed in the previous section, surface roughness is the more important parameter for wafer bonding applications. However the uniformity of the buried oxide layer may also be important for some applications.

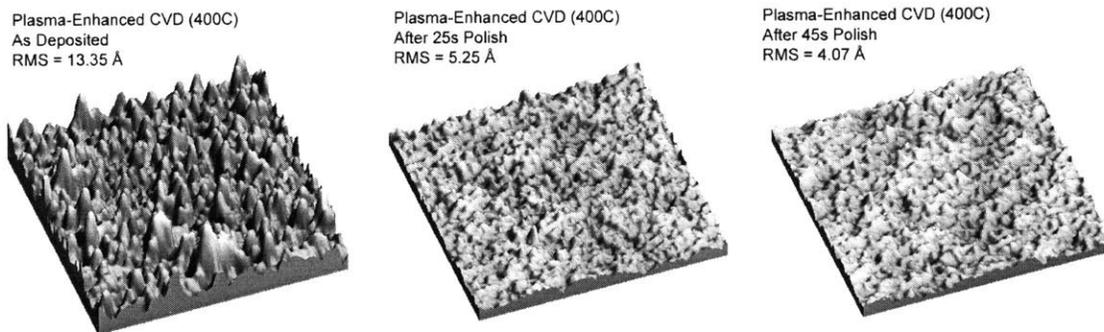


Figure 14. Surface roughness of PECVD oxide for different polishing times.

Chapter 5

GeOI Fabrication

Ideally, GeOI fabrication produces defect-free, and ultra-thin Ge layers on inexpensive and widely available Si substrates. The procedure should be compatible with standard industry techniques for CMOS processing. This chapter introduces some of the prior work involved in the fabrication of GeOI, and addresses some of the limitations and benefits of each method. The approach adopted in this thesis work is presented along with some of the results obtained. Finally, some considerations for improvements and further work are discussed.

5.1 Background

Huang et al. reported the fabrication of GeOI by plasma-assisted wafer bonding and etch back.[21] CVD SiO₂ was deposited on bulk Ge and Si wafers, and both were then treated with O₂ plasma to activate the surface before bonding. After bonding at 500 °C for ten hours, the top Ge wafer was etched back to make a GeOI substrate. This technique is likely not suitable for the fabrication of ultra-thin device for two reasons. First, the layer thickness cannot be precisely controlled during the etch back. Second, it is undesirable to have a Ge/SiO₂ back interface in ultra-thin body devices.

Nakaharai et al. have proposed a fabrication technique using a Ge condensation method.[22] First, an epitaxial SiGe layer is deposited on a thin SOI wafer. Then, the wafer is annealed in O₂ in an attempt to oxidize the SiGe layer. As the oxidization proceeds, Ge atoms are rejected from the newly formed SiO₂ layers. Eventually, all the Ge atoms diffuse to the buried oxide, while all the Si atoms are consumed in the SiO₂. The result is a pure Ge layer that retains the orientation of SOI layer, and some of the compressive strain of the SiGe layer. The benefit of this technique is that ultra-thin GeOI structures can be obtained without the use of wafer bonding. This technique also allows for the possibility of strained Ge channels that could further enhance mobility. One drawback is that the device layer necessarily has some density of dislocations, possibly too high for efficient circuit fabrication.

Liu et al. introduced a method to produce GeOI using liquid-phase epitaxy.[23] As in Figure 6, a Ge layer is deposited on an insulated Si substrate. Contact is made between the Ge film and the Si substrate in a small seeding region. After patterning, LTO is deposited on top of the film to completely enclose the Ge layer. The wafer is rapidly heated just past the melting point of Ge to liquefy the deposited film. As the wafer is cooled, crystallization of the Ge occurs starting at the seeding region and then propagates laterally over the buried insulator. Similarly to Czochralski growth, any dislocations or stacking faults at the interface of the seeding region propagate and eventually terminate at the LTO layer. The resulting device layer is reportedly defect free, and can be designed to be very thin. The major benefits of this method include no bulk wafer bonding, no dislocations in the device layer, and compatibility with standard CMOS processing. The drawback is that it is difficult to achieve large areas of crystal Ge growth with being interrupted by random nucleations. The authors were able to achieve perfect crystal growth of approximately 20 μm from the seed area.

Finally, in the work that served as the motivation for this thesis, Pitera et al. have fabricated GeOI by wafer bonding virtual Ge substrates using hydrogen-induced delamination and the etch-stop technique.[24] First, a SiGe graded buffer is grown on a Si substrate up to pure relaxed Ge. An etch stop layer of $\text{Si}_{0.4}\text{Ge}_{0.6}$ is then grown, followed by a relaxed Ge layer. A passivation layer of Si is deposited, followed by LPCVD of SiO_2 . This SiO_2 layer is then polished and the wafer is implanted with hydrogen and bonded to a Si handle. Subsequent annealing activates the hydrogen implant and transfers the Ge structure to the handle wafer. The damaged Ge can be selectively removed with a chemical etch that stops on the SiGe layer. The etch stop layer can then be selectively removed with a CMP step.

The power of this technique is the ability to transfer a thermally mismatched material using thermal matched substrates. This avoids many of the difficulties associated with the bonding of bulk Ge to Si substrates. Also because bulk Ge wafers are not used, and the Ge device layer is protected by oxide, standard chemical cleans can be used prior to bonding. The drawbacks are the result of the growth on a graded buffer. First, a finite number of dislocations are always present in the device layer. Also a crosshatch

morphology is present in the device layer that limits the application of this technique for the production of ultra-thin Ge layers.

5.2 Fabrication Procedure

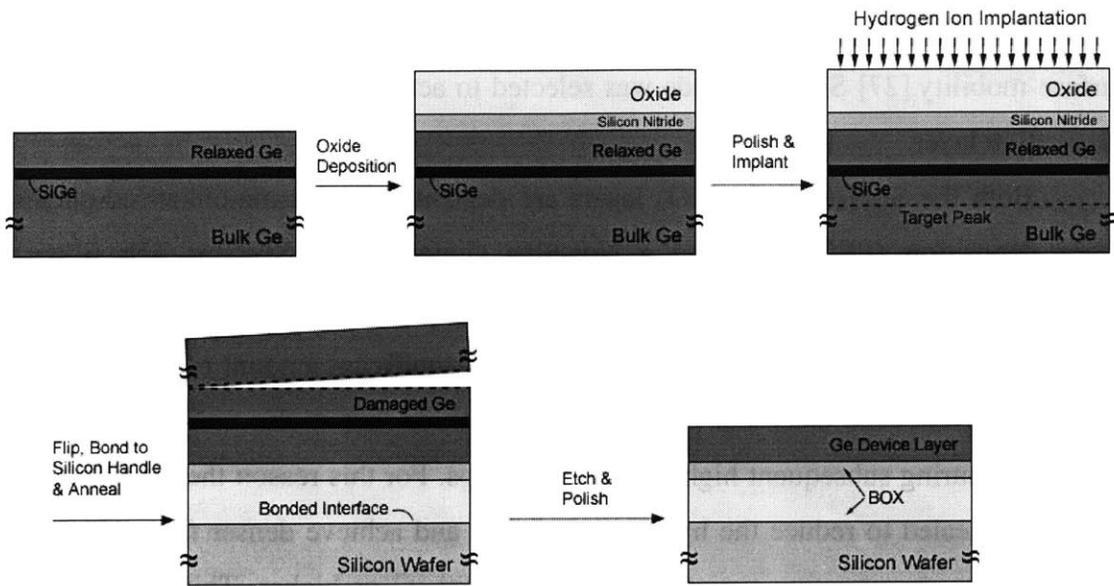


Figure 15. Illustration of the process flow used in this work.

The fabrication procedure used in this work is related to the hydrogen-induced delamination method described in Section 3.4.2. The starting point is a bulk Ge wafer, on which an epitaxial layer of $\text{Si}_{0.4}\text{Ge}_{0.6}$ is deposited by UHVCVD. This eventually serves as the etch stop layer for the removal of the damaged Ge. Sixty percent SiGe was chosen because this is the fraction for which the etch rate in H_2O_2 essentially goes to zero. This layer is less than the critical thickness for the pseudomorphic growth of $\text{Si}_{0.4}\text{Ge}_{0.6}$ on Ge. This allows for the subsequent deposition of a layer of relaxed Ge that ultimately becomes the GeOI device layer. Because the growth occurs epitaxially on a lattice-matched substrate, the device layer should ultimately be free of dislocations.

Next, the buried oxide layer is deposited on top of the bulk Ge. The surface on which this film is deposited eventually becomes the back interface of the GeOI device layer. The back interface in ultra-thin on-insulator structures has a significant impact on

device performance. Therefore, several concerns were addressed when determining the structure of the buried oxide layer. It is preferred that the buried oxide be composed of SiO₂ because this would result in a simpler and higher quality bond to the Si handle. However, it is undesirable to have direct interface between Ge and SiO₂ for several reasons. First, the diffusion of Ge into SiO₂ would lead to an increase in surface roughness scattering and difficulty fabricating ultra-thin films. Second it is well known that the Ge/SiO₂ interface is electrically inferior to other possible dielectrics.[25],[26] It has been characterized as having a rather large density of interface states as well as poor surface mobility.[27] Silicon nitride was selected to act as both a diffusion barrier and a passivation layer.

Both the Si₃N₄ and the SiO₂ layers are deposited by plasma-enhanced chemical vapor deposition (PECVD) using a Novellus ConceptOne[®] System. The films are deposited at 400 °C at pressure of 2400 mT. The total film thickness as deposited is 500 nm. Dielectric films deposited by PECVD contain significant amount of hydrogen. This not only degrades the electrical properties of the oxide, but it also causes problems by outgassing during subsequent high-temperature steps. For this reason the deposited films must be annealed to reduce the hydrogen contents and achieve denser films. On silicon substrates the densification typically occurs at 1000 °C or higher. This temperature is higher than the melting point of Ge, but in this case the limiting thermal constraint is the diffusion of the etch stop layer. Based upon annealing experiments and SIMS data on the diffusion of the etch stop layer, the densification anneal is limited to 650 °C for three hours.[28]

As discussed in Section 4.2, the surface roughness of PECVD films as deposited is too great to ensure good bonding. Therefore the deposited oxide layer is polished in order to reduce the surface roughness (rms) below 0.5 nm. Figure 14 indicates that a 45s polish was sufficient for direct bonding. This polishing time reduces the thickness of the buried oxide to layer to approximately 300 nm.

The next step is the implantation of hydrogen ions (H⁺) in the Ge substrate. The energy of the implant must be high enough to achieve a peak in the bulk Ge region away from the etch stop layer. For an oxide layer approximately 300 nm thick, an implant energy of 120 keV at a dose of $5 \times 10^{16} \text{ cm}^{-2}$ is sufficient to ensure this condition.

Next direct bonding of the Ge wafer to a Si handle takes place. Again, if both wafers were silicon, the post-bond anneal would likely take place at temperatures up to 1000 °C. But again this process is limited by thermal constraints; in this case it is the mismatch between the thermal coefficients of expansion between Ge and Si. As indicated in Table 3, the linear coefficient of thermal expansion for Ge is more than twice that of Si. This means that for a given increase in temperature experienced during the post-bond anneal, the Ge wafer attempts to expand more than twice as much as the Si wafer. This expansion places an enormous amount of stress at the bonded interface. If the bond energy is low, this may simply result in debonding. If the bond is strong enough the wafer pair begins to bow to accommodate the mismatched expansion. When the bow is too great the wafer pair simply breaks.

Therefore it is necessary to develop a procedure to minimize the temperature needed to activate the hydrogen implant and transfer the film. One method may be to pre-anneal the implanted Ge wafer at a temperature below the hydrogen blister point. This is defined as the point where the formation of hydrogen microcavities leads to an apparent bubbling immediately prior to the delamination of the film.[15] Annealing for a thermal treatment less than what is required to reach this point getters hydrogen near the peak of the implant without yet transferring a layer. The wafer can then be bonded, and annealed to activate the remaining hydrogen. Because the wafer has been pre-annealed, the bonded pair will need less time and less temperature to reach the new blister point.

Once the film has been transferred to the handle wafer, the temperature can be increased to further strengthen the bonded interface. As this point the bulk Ge wafer has separated, leaving a damaged Ge region with high surface roughness. In a typical SOI process, this layer may be planarized by CMP, or thinned by successive oxidations. As illustrated in Figure 16, this technique is not suitable for bulk Ge processes due to the lack of good planarization method for Ge. Because the etch stop technique is used here, the damaged Ge can simply be etched away in a dilute solution of H₂O₂ (~20:1). The inability to polish Ge is now beneficial because the etch stop layer can be removed by CMP with high selectivity.

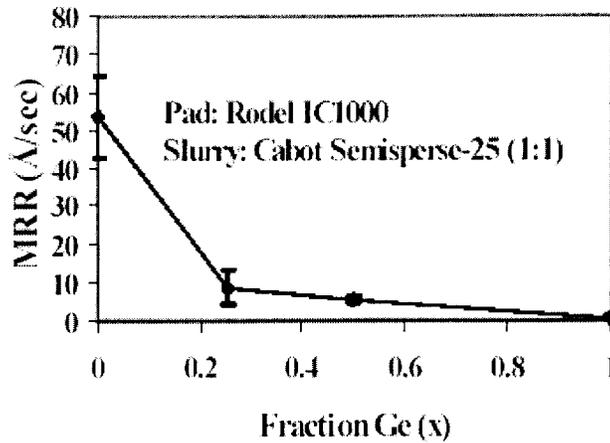


Figure 16. Material removal rate for SiGe for the CMP system at MTL. (From Pitera [29]).

5.3 Results

Figure 17 shows a cross sectional TEM of the GeOI structure immediately following the activation of the hydrogen implant. The top Ge layer shows significant roughness and lattice damage, but this layer can be selectively removed in H_2O_2 . This example is from a direct-bonded pair that was annealed for 15 hours at 250 °C immediately following the bond. The temperature was ramped to 400 °C, to activate the hydrogen implant and layer transfer occurred. The TEM indicates that the etch stop layer is intact, and did not suffer damage from the implant or out-diffusion during the oxide densification.

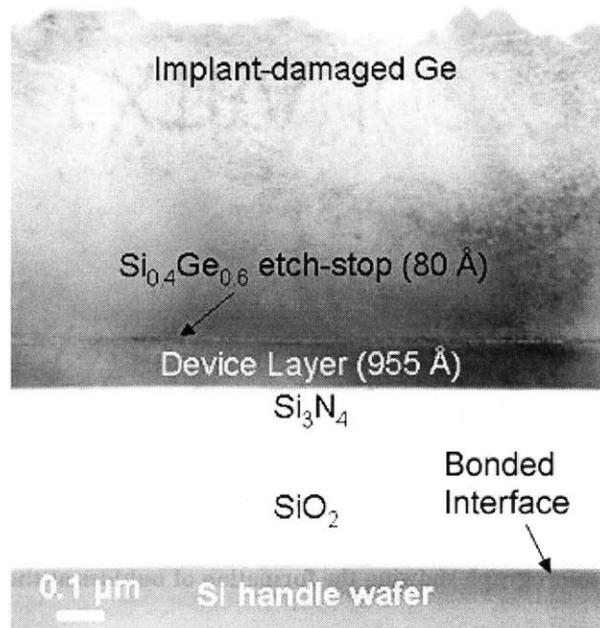


Figure 17. Cross sectional TEM of GeOI immediately after layer transfer.

Figure 18 illustrates the problems associated with using PECVD oxide as the buried layer. This micrograph shows the formation of bubbles at the bonded interface due to the outgassing of hydrogen from the buried oxide layer. Figure 19 shows a section of one of these bubbles, confirming that they have occurred at the bonded interface. The fact the bubbles are consistent across the film indicates that they formed after the layer transferred occurred. If they had formed prior it is likely that the delamination cleave would have propagated all the way to the bonded interface. Also, the fact that the bubbles are small and tightly packed indicates the bond energy is quite good. If the bond had been weak, the bubbles would have been able to propagate further and merge.

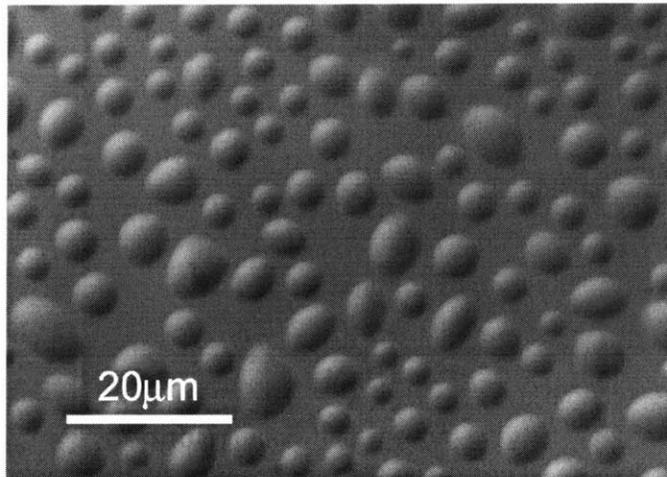


Figure 18. Nomarski micrograph showing the formation of bubbles at the bonded interface.

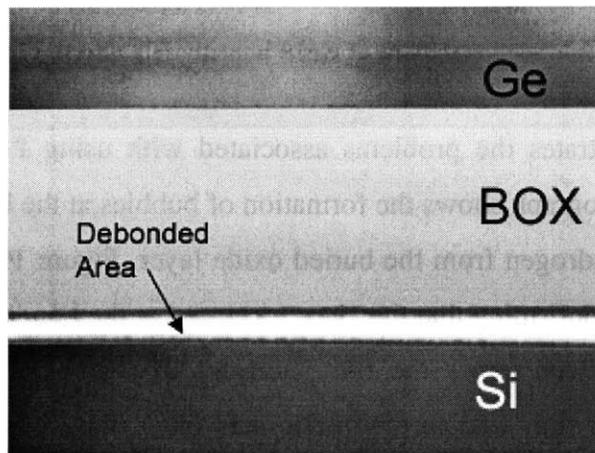


Figure 19. Debanded area due to oxide outgassing.

The solution to this problem is either further densification of the oxide layer prior to bonding or the use of a different oxide. The difficulty with the first solution is the diffusion of the etch stop layer. Although the TEMs shown indicate the etch stop is in good condition, it is not likely that it would survive much higher temperatures or longer annealing times. Using an alternative buried oxide layer is a more likely solution. Various deposited oxides available in MIT's Microsystems Technology Laboratory (MTL) were investigated to gauge their relative hydrogen content. While not a perfect measure of hydrogen content or density, the etch rate of an oxide film is a good indicator. Table 5 shows the etch rate for different deposited oxides films, and indicates the best solution

may be PECVD oxide deposited by an Applied Materials DCVD[®], or TEOS base SiO₂ from a Novellus ConceptOne[®] system. Further studies are needed to determine the best solution.

Table 5. Etch rate in 50:1 HF of deposited oxide films available at MTL (in Å/min).

	As deposited	After Densification (3hrs at 600°C)
Thermal Oxide (dry, 1000 °C)	190	-
Novellus PECVD (silane, 400 °C)	1500	750
Novellus PECVD (TEOS, 350 °C)	800	550
LPCVD (400 °C)	1000	600
Applied PECVD (silane, 400 °C)	800	600

5.4 Conclusions

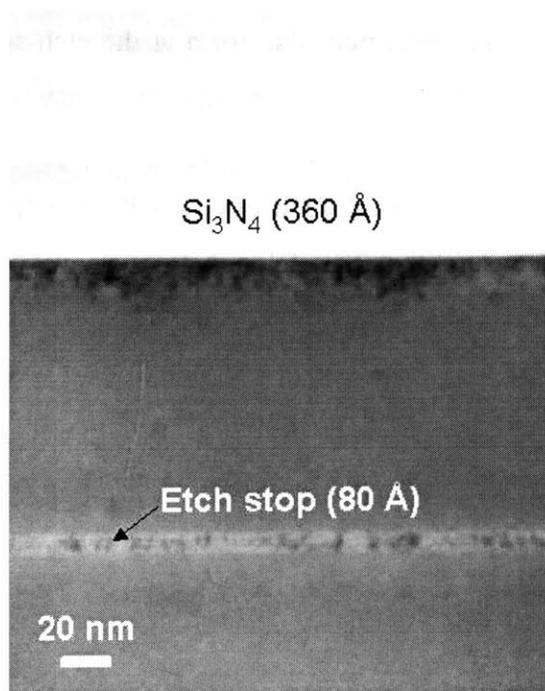


Figure 20. Cross sectional TEM showing detailed view of the device layer.

The greatest obstacle to the fabrication of GeOI using the method described in this work is the thermal mismatch of the bonded wafer pair. In some cases cracking of the Ge wafer was observed as low as 200 °C. This was presumed to be the result of poor

bonding due to surface defects; as the wafer pair bows a crack is more likely to initiate from a poorly bonded site on the wafer or some other defect. However in other cases the bonded wafer did not break at temperatures up to 300 °C. In this work the bonding was performed with bulk six-inch wafers. It is likely that smaller wafers would not break as easily, but conversely larger wafers used in industry may break at even lower temperatures.

By annealing the implanted Ge wafer before bonding, layer transfer was observed at temperatures as low as 250 °C. Further investigation of the blister point for various implant parameters could lead to further optimization of annealing conditions. Increasing the dose of the implant would also allow for shorter, lower temperature anneals, but there is a drawback to that approach. Figure 21 shows the result of a Monte Carlo based simulation for the stopping range of ions in matter (SRIM) for the implantation of hydrogen ions into the Ge substrate.[30] Note that the etch-stop layer gets a significant amount of hydrogen during the implant. As the implanted wafer is annealed and the hydrogen begins to diffuse, platelets may also form at the etch-stop layer if the dose is sufficiently high. As the delamination cleave propagates it may be redirected to the etch stop layer, resulting in damage to the device layer, and preventing the subsequent removal of the damaged Ge layer. The dose must be small enough to minimize damage to the etch stop layer and ensure that the delamination cleave propagates through the intended area of the wafer.

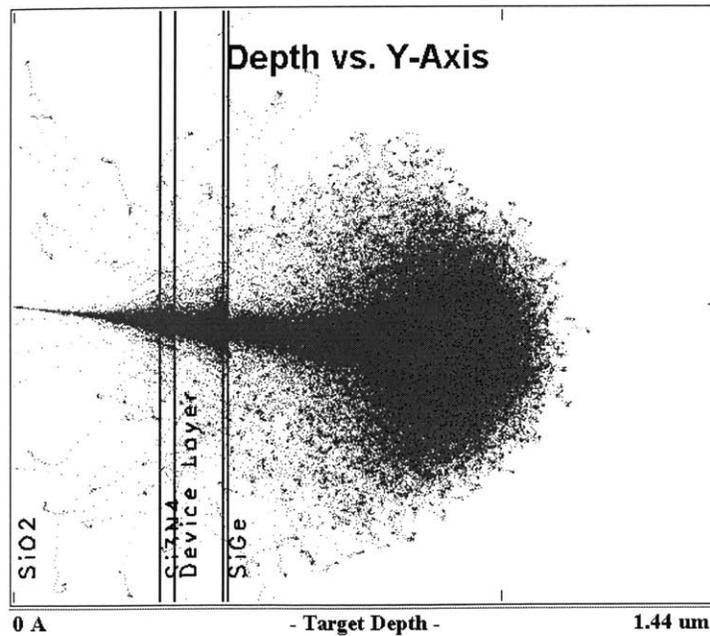


Figure 21. SRIM calculation of hydrogen implantation into the Ge structure.

Another approach may be the so-called “smarter-cut” method.[31] Implanting boron along with hydrogen has been shown to significantly reduce the blistering temperature in Si. However, it is not necessarily clear that this approach works in Ge, and it is also unclear whether further implant damage to the device layer is acceptable.

To summarize, GeOI structures have been fabricated using wafer bonding and layer transfer by hydrogen implantation. This approach can also be easily extended to producing ultra-thin GeOI layers. It also has the benefit of producing a dislocation-free device layer over the entire wafer area. The process does use bulk Ge wafers, but they potentially may be reused several times after layer transfer. Although thermal constraints limit the ease with which this process can be carried out, there are possible solutions to further reducing the thermal budget.

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