Ultra-Low Voltage CMOS Operational Amplifiers

by

Ayman U. Shabra

B.S., King Fahd University of Petroleum and Minerals (1994)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Science Master
[Master of Science]
at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 1997

Author .....
Department of Electrical Engineering and Computer Science
February, 1997

Certified by ..
.....
Hae-Seung Lee
Professor of Electrical Engineering
Thesis Supervisor

Accepted by .....
Arthur C. Smith
Chairman, Departmental Committee on Graduate Students

Ultra-Low Voltage CMOS Operational Amplifiers

by

Ayman U. Shabra

Submitted to the Department of Electrical Engineering and Computer Science
on February, 1997, in partial fulfillment of the
requirements for the degree of
Science Master

Abstract

The trend towards low supply voltages presents new challenges in the design of high performance switched capacitor circuits. This thesis presents the design of 0.9V CMOS switched capacitor operational amplifiers. Two approaches are investigated: the first uses only high threshold voltage (Vt) MOSFETs, and the second utilizes low Vt MOSFETs, both in a 0.8μm multi-threshold BICMOS process. It is shown that the second approach offers great advantage. The settling time of the opamp built using the first approach is 182ns, while it is only 72ns for the second approach. The design of both opamps' bias circuit, common mode feedback circuit and switches is presented. A tail current source design, that provides a constant current and requires less than 10mV for proper operation, will be demonstrated for each opamp.

Thesis Supervisor: Hae-Seung Lee
Title: Professor of Electrical Engineering

Acknowledgments

I wish to thank IBM for providing the device models and technology files used in this work.

I would particularly like to thank my advisor, Prof. Hae-Seung Lee, for his invaluable guidance that has made my experience at MIT very rich and fruitful.

I would also like to thank my office-mate Kush Gulati for the long hours of discussion that helped deepen my understanding of my field and improved my design skills. Special thanks to Jen Lloyd for her valuable help and suggestions throughout the duration of this work. I would like to thank Dr. Paul Yu for his keen observations and insightful comments. Thanks also to Meelan Lee for helping me with Cadence and its seemingly insolvable problems. I would like to thank Iliana Fujimori for her help with Latex, which allowed me to write this thesis. Special thanks to Mathew Varghese for his helpful comments on the first draft of this thesis.

I am particularly grateful to my undergraduate advisor at KFUPM, Prof. Muhammad Tahir Abuelma'atti, for sparking my interest in research. His remarkable personality and genuine care for his students has been a great source of inspiration.

Thanks to Ammar, Fawzi, Gassan, Jalal, Kashif, M.Ali, M.Saeed, Sab'bir and Yassir for an enjoyable time at MIT. Special thanks to Ibrahim, Rayyan and Reda for being such good friends.

Thanks to my nieces and nephews Sarah, Khadeejah, Aziz and Ahmed for moments of unsought for happiness. I would like to thank my sisters Maryam and Sumayyah and my brother Anas, for their continuous and unconditional love. My feelings and sense of gratitude for my parents cannot be encompassed by words and I only hope that I can give them the sort of happiness that they have given to me. Most of all, I would like to express my gratitude to the Almighty for the countless blessings he has bestowed upon me over the years.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The scaling down of transistor dimensions which has continued relentlessly over the past few decades, has pushed down the supply voltages as well[1]. Lower supply voltages pose a very interesting challenge to circuit designers because of the lower drive available for transistors. The design trade-offs for digital design have been well investigated. It has been shown that the lower voltage supplies can be utilized to reach an optimum performance in terms of the energy-delay product[3],[4].

The situation for analog circuits is quite different. Unlike digital circuits, which can be designed to operate very efficiently at low voltages, analog circuits suffer. Low voltage analog circuit design to date has been confined to applications, such as implantable devices and sensors[5],[6], which require circuits that are very reliable and consume very little power, but do not demand high performance circuitry. The demands on low voltage analog circuits will definitely change. The objective of this work is to attempt to build high performance analog circuits at low voltages.

1.1 Thesis Objectives

The focus of this work will be on the design of low voltage CMOS operational amplifiers for switch capacitor circuits powered by a 0.9V supply. The work will investigate circuit solu-

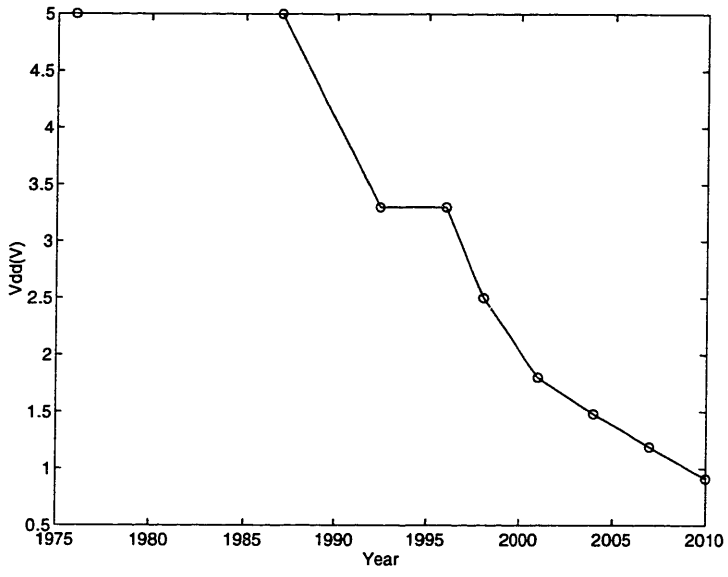

Figure 1-1: Past and projected future voltage supply trends [1]

tions using MOSFETs with high threshold voltages. Furthermore, the utility of MOSFETs with low threshold voltages will be studied. These two approaches will be demonstrated through the design of two opamps, one using only high threshold MOSFETs and other using both high and low threshold MOSFETs. The performance of these opamps will be compared in an attempt to reach a conclusion on which approach is more attractive.

1.2 Thesis Motivation

The trend towards low voltages is strong in the semiconductor industry today. The scaling down of transistor dimensions has produced transistors with very high electric fields. At these high fields effects such as hot carrier degradation, dielectric breakdown and punch through become prominent. These ailments can degrade, and even destroy circuit performance. One way to alleviate these problems is to reduce the electric field by operating at a lower voltage. The plot in figure 1-1 shows how the standard supply voltages have reduced over the years in response to these problems, and shows projections for the future which are just below 1V[1]. This work will therefore cater to the future needs of analog IC design.

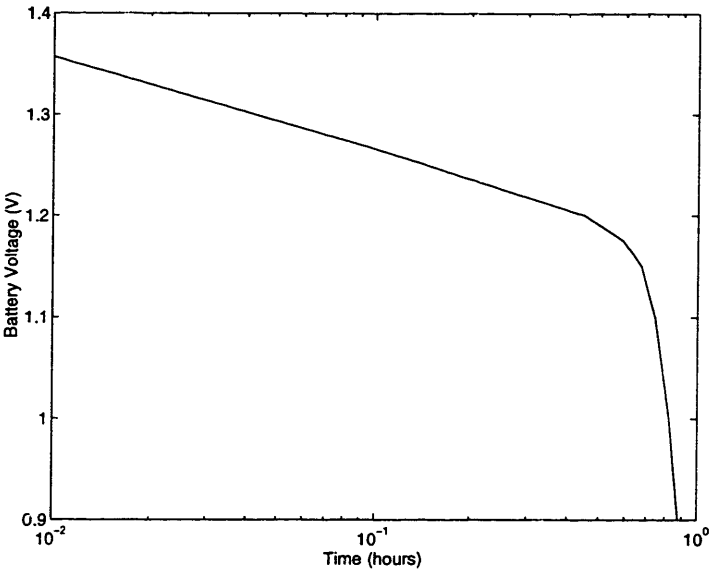

Figure 1-2: A typical discharge curve for a Nickel Cadmium battery with a discharge rate equal to the battery capacity[2].

Another reason we believe this work is interesting is because it falls in the domain of single cell battery operation. The energy density performance of batteries has not improved drastically in the past. Even the advent of lithium ion and nickel-metal hydride batteries does not promise to improve battery performance by anywhere near an order of magnitude over the standard nickel cadmium cells[7]. Therefore, the only way to reduce the size of batteries is to use fewer of them, and to rely on circuit techniques to compensate for the reduction in supply voltage and power. Figure 1-2 show the discharge curve for a single nickel cadmium battery[2], which is similar to the discharge curve of nickel-metal hydride. At the end of the cell life it has a voltage of roughly 0.9V. This voltage represents the worst case voltage at which the circuits must be designed.

For digital circuits lower voltages can be translated into lower power consumption. This is not true in analog circuits. A lower supply voltage reduces the maximum signal swing at the output. To compensate for this the current levels in the circuit must increase to reduce the noise floor, resulting in higher power consumption. Low voltage offers little advantage for most analog circuits. In many applications analog circuits constitute only a

small portion of the overall system. In these situations it may be of great advantage, in terms of the overall power consumption of the system, to operate at the low voltages at which the digital circuits operate.

Switched capacitor circuits are by far the most popular approach to implement a large variety of analog circuits[8],[9],[10],[11]. The performance of switched capacitor circuits is limited, mainly, by the performance of the opamps. Hence, building opamps is the first step toward having complete systems at low voltages. In this work, low voltage design techniques will, therefore, be demonstrated using opamps because they are the most important elements in switched capacitor applications.

One of the aims of this work is to investigate whether low threshold voltage (Vt) MOSFETs (LMOS) offer any particular advantage. For low voltage (Lower) digital circuits LMOSs help reduce circuit delay by increasing the drive to the transistor (Vgs-Vt)[3]. However, LMOSs typically have much larger minimum gate lengths than high threshold voltage MOSFETs (HMOS) within a given process. The speed of analog circuits is fundamentally limited by the transition frequency, which is inversely related to the square of the gate length[12]:

$$f_t \propto \frac{1}{L^2} \tag{1.1}$$

Larger gate lengths imply lower f_t as shown in figure 1-3(a), and hence also imply slower circuits. MOSFETs designed with low Vt suffer more hot carrier degradation, measured in terms of percentage change in the dc drain current, as opposed to MOSFETs designed with high Vt for the same number of hot carriers observed in the substrate current[13]. This demands the usage of large gate lengths for LMOSs to reduce the degradation. However, if the transistors are operated with a supply voltage, such as 0.9V, that is much lower than the maximum allowed voltage within the process, then the electrical field in the channel will not be large and hot carriers will not be generated, enabling the usage of shorter gate lengths. Figure 1-3(b) shows that at a gate length of 0.8μ the transition frequency of the LMOS significantly improves.

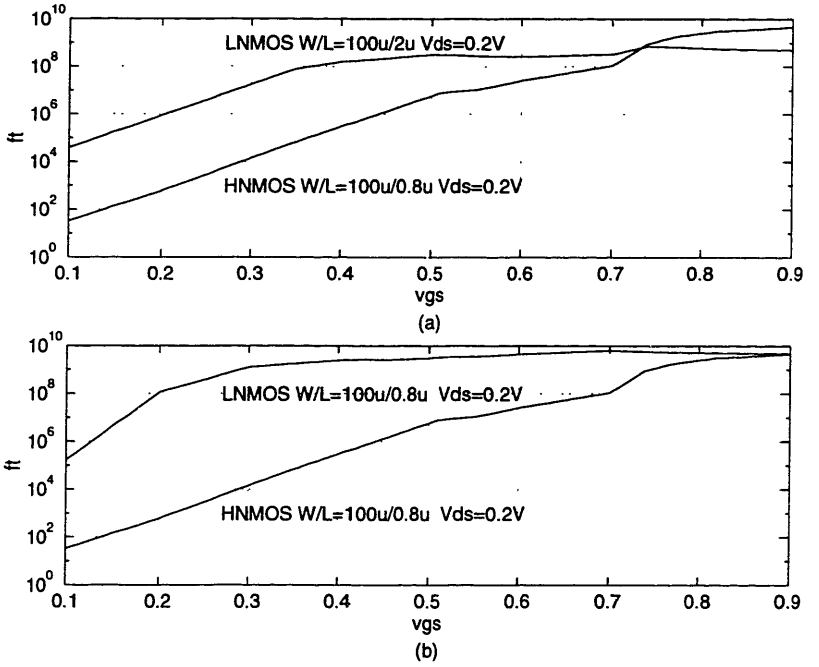

Figure 1-3: The transition frequency versus the gate to source voltage.

The difficulty with using the minimum gate length of 0.8μ for the LMOSs is illustrated in figure 1-4, which shows how the intrinsic gain ($g_m r_o$) of a LMOS changes with the gate length and gate to source voltage. At small gate lengths $g_m r_o$ is very small, and if this device were to be used in an opamp, the overall gain of the opamp will be very low, which is definitely undesirable. Hence, small gate lengths cannot be used in circuits where gain is desired. This implies that the f_t of LMOS transistors will be lower than the f_t of HMOS transistors.

So in the first order analysis, LMOSs do not appear to offer much advantage. HMOSs, on the other hand, can be operated in subthreshold and, therefore, offer a larger gain and better frequency response because of the large transconductance in the subthreshold regime. They also provide a larger swing because of their low saturation voltage.

In spite of the arguments that have been presented, LMOSs are very attractive for low voltage design. As will be shown in subsequent chapters the main drawback of HMOS opamps is the very poor slew rate which severely limits the speed of the opamp.

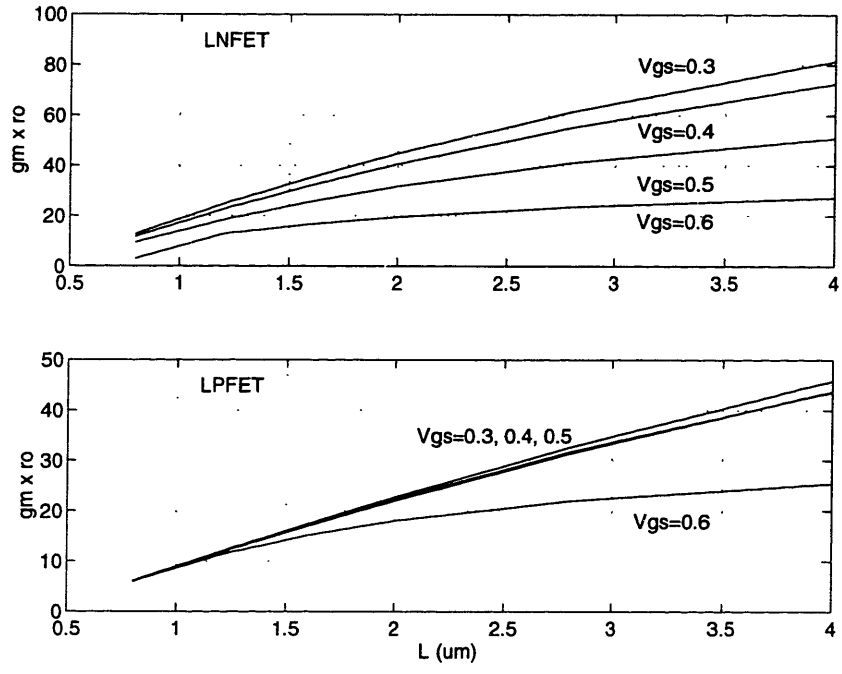

Figure 1-4: The intrinsic transistor gain as a function of the gate length.

1.3 Thesis Organization

The thesis will begin with discussing general design considerations for low voltage switched capacitor opamps in chapter 2. In chapter 3, the design of the first opamp, which uses only HMOSs will be presented. This will be followed, in chapter 4, by the design of the second opamp, which utilizes LMOSs. Simulation results for both designs will be presented in chapter 5. Finally, conclusions on the performance of both opamps will be drawn in chapter 6.

Chapter 2

Low Voltage Operational Amplifier Architecture

The selection of the opamp is a very critical step in the design of switched capacitor circuits, since these circuits are fundamentally limited by the performance of the opamp. Different opamp designs offer varying performance capabilities. The specific application in which the opamp will be used dictates the performance required from the opamp, and which should be used as a guideline in the selection the of the opamp architecture. Some of the important opamp performance metrics that are commonly used in the selection process are the opamp gain, transient settling speed, output swing, noise performance, power consumption, power supply rejection and common mode rejection. Under low voltage operation the dynamic range, gain, and speed of the opamp are severely limited. Any attempt to use the opamp under this operating condition must address these issues if proper operation is to be achieved. This chapter will address these issues in an attempt to reach some general strategies for low voltage opamp design.

A large variety of opamp architectures have been proposed which will not be considered in this discussion. Class A-B opamps and opamps with rail-to-rail output stages[14] will not be considered, because the limited power supply and the large minimum voltage requirements of these circuits prohibits their practical implementation. Opamps with rail-to-rail

input stages offer a large input common mode range[15], a feature that is not needed in switched capacitor applications since the input common mode is fixed. In addition, if a fully differential one-stage architecture is used, the input common mode is essentially fixed because of the opamp external feedback.

2.1 Dynamic Range

The most obvious limitation under low voltage operation is the severely limited dynamic range. The dynamic range is a function of the opamp output voltage swing and the noise appearing at the output. The maximum possible power that the signal at the output of the opamp can have has an upper bound given by the square of the opamp swing. The opamp swing is defined here as the range of opamp output values under which the opamp provides the gain required by the application. Reducing the supply voltage directly results in a reduction in swing and ultimately in the output signal power. To illustrate the effect of a voltage reduction on the opamp swing consider a supply voltage reduction from 5V to 0.9V. This can result in roughly 87% decrease in output swing.

A fully differential opamp architecture can reduce the brunt of the reduction of the power supply. Furthermore, the swing can be controlled through the designing the opamp output stage. The two stage, folded cascode and telescopic opamps shown in figure 2-1 are popular opamp designs[12],[16]. These designs have different output swings which are summarized in table 2.1. From these equations it can be seen that the two stage architecture offers the largest swing while the Telescopic opamp offers the lowest. Furthermore the swing can be enhanced by operating the transistors in weak inversion where $V_{ds,sat}$ is low.

The dynamic range is also effected by electronic noise. In switch capacitor applications there are two main sources that contribute to the noise. The first is the noise due to the switches. During the switch on state the switch has a finite resistance which generates thermal noise. When the switch is turned of the noise due to the switches is stored on the sampling capacitor. This process results in KT/C mean squared value of noise[17]. This noise cannot be reduced by changing the size of the switches, in fact, the noise is

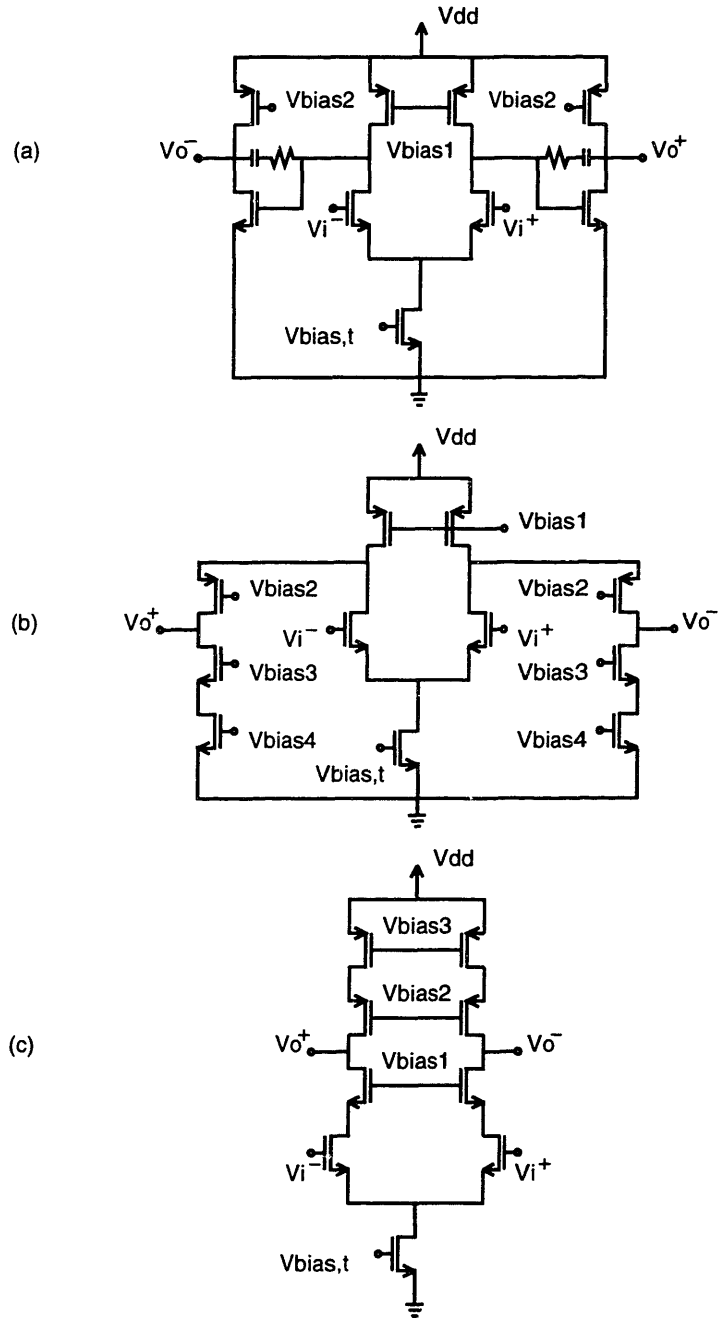

Figure 2-1: a) Two stage opamp b) Folded cascode opamp c) Telescopic opamp

Opamp	Swing
Two stage	$2V_{dd} - 4V_{ds,sat}$
Folded cascode	$2V_{dd} - 8V_{ds,sat} - 4V_{margin}$
Telescopic	$2V_{dd} - 10V_{ds,sat} - 6V_{margin}$

Table 2.1: Output swing of different opamp architectures. V_{dd} is the supply voltage and $V_{ds,sat}$ is the drain to source saturation voltage.

independent of the design of the switches. The only way to reduce this noise is to use larger sampling capacitors. The second factor that contributes to the noise is the operational amplifier. The mean squared value of the opamp noise depends on the opamp architecture and topology of the feedback circuit.

Figure 2-2 shows a switched capacitor circuit that can be used to perform a fixed ratio multiply or divide operation, which are commonly used functions in analog to digital and digital to analog converters. The circuit operates in two phases. At the end of the first phase $\phi 1$, the mean square thermal noise due to the switches is stored on capacitors C_s and C_f as KT/C_s and KT/C_f respectively as shown in figure 2-3. During the second phase $\phi 2$, shown in figure 2-4, the mean square noise stored on the capacitors at the end of $\phi 1$ will appear at the opamp output as KT/C_s and $KT \times C_s/C_d^2$. Furthermore, noise due to the switches that are now closed also appears at the output. This noise is, however, insignificant in typical switched capacitor circuits for two reasons. Firstly, it is suppressed at high frequencies. The transfer function from the switch noise generators in the feedback path to the circuit output is a low pass filter given by:

$$H_f(f) = \frac{C_s \times A(f)}{C_f \times A(f) + C_f + C_s} \tag{2.1}$$

and the transfer function for the input side switches is also a low pass filter and is given by:

$$H_s(f) = \frac{-C_f \times A(f)}{C_f \times A(f) + C_f + C_s} \tag{2.2}$$

where $A(f)$ is the opamp open loop transfer function. The second reason the direct switch

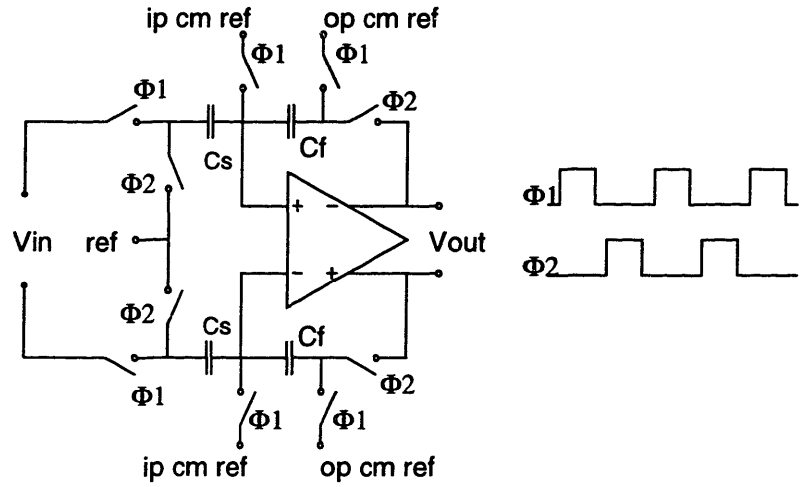

Figure 2-2: Switched capacitor circuit

noise is not important is that the high frequency components of this noise are not significantly aliased down to the baseband when sampled by the next stage, because the noise has been limited to a bandwidth ($\propto \frac{g_m(\text{opamp 1st stage})}{C_{compensation}}$) which is much lower than the bandwidth of the RC sampling circuit of the on switch and the sampling capacitor. The conductance of the on switch ($\frac{1}{R}$) is the drain to source conductance of a MOSFET in the triode regime, and is designed to be larger than the transconductance of the opamp first stage g_m(opamp 1st stage) so the settling time of the switched capacitor stage is not limited by the switches. Control of the switch on resistance can be easily accomplished by changing the width of the transistors.

The noise generated by the opamp constitutes the other important source of noise in this circuit. Opamp noise is due to the noise generated by its constituent transistors. If these transistors are operated in strong inversion the noise will be mainly thermal noise. If, on the other hand, the transistors are operated in subthreshold the noise will be due to shot noise. The effect of the transistor flicker noise is diminished if offset cancelation is used[17]. If the input referred opamp mean square noise is modeled by $\bar{v}_{n,ip}^2$, as shown in figure 2-4,

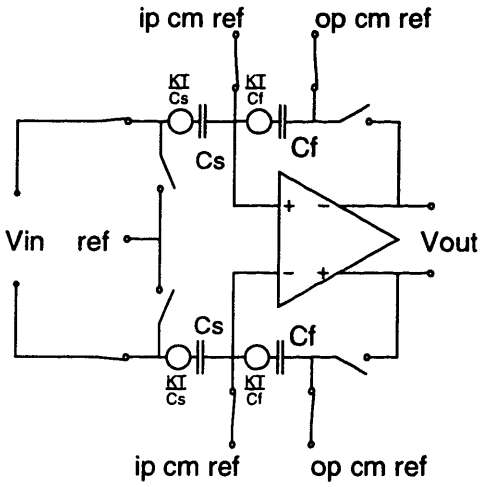

Figure 2-3: Noise sources at the end of $\phi 1$

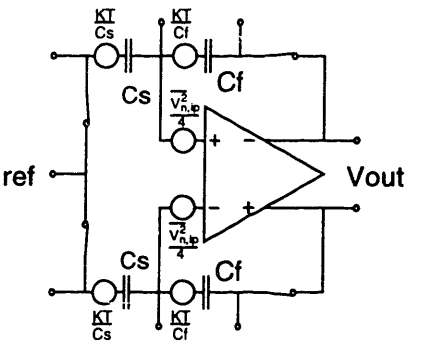

Figure 2-4: Noise sources during $\phi 2$

the mean square noise at the output would be:

$$\bar{v}_{n,op}^2 = \int_{-\infty}^{\infty} H^2(f) S_i(f) df \tag{2.3}$$

where $H(f)$ is the transfer function from the noise source to the output of the opamp and is given by:

$$H(f) = \frac{A(f)}{1 + A(f)\frac{C_f}{C_f + C_s}} = \frac{A(f)}{1 + A(f)\beta} \tag{2.4}$$

where β is the feedback factor. $S_i(f)$ in equation 2.3 is the two sided power spectral density of the input referred opamp noise and has the general form:

$$S_i(f) = \frac{KT}{g_m} \times m \times N \tag{2.5}$$

where g_m is the transconductance of the input devices. N is a factor that depends on whether the transistors are in strong inversion or weak inversion. In strong inversion $N = \frac{16}{3}$, and in weak inversion $N = 2 \times n$, where n is the subthreshold slope ideality factor. Finally, m is the excess noise factor which depends on the opamp architecture. For the two stage opamp or the telescopic opamp in figure 2-1 m is:

$$m = 1 + \frac{g_{ml}}{g_m} \tag{2.6}$$

where g_{ml} is the transconductance of the first stage load devices in the two stage opamp, and it is the transconductance of the load devices for the telescopic opamp. For the folded cascode opamp the excess noise factor is:

$$m = 1 + \frac{g_{ml1}}{g_m} + \frac{g_{ml2}}{g_m} \tag{2.7}$$

here again g_{ml1} and g_{ml2} are the transconductance of the load devices.

If the opamp is assume to have a single pole transfer function $A(f) = \frac{1}{\frac{1}{g_m R} + j2\pi f \frac{C_c}{g_m}}$, where $g_m R$ is the opamp low frequency gain and C_c is the compensation capacitor, then

the mean squared output noise will be:

$$\begin{aligned} \bar{v}_{n,op}^2 &= \int_{-\infty}^{\infty} \left(\frac{A(f)}{1+A(f)\beta}\right)^2 \frac{KTmN}{g_m} df \\ &= \frac{KTmN}{4g_m} \int_{-\infty}^{\infty} \frac{df}{\beta^2 + \pi f C_c/g_m} \\ &= \frac{KTmN}{4\beta C_c} \end{aligned} \tag{2.8}$$

If $\beta = 0.4$ and $m = 2$ then in strong inversion $\bar{v}_{n,op}^2 = 6.67\frac{KT}{C_c}$, while in the subthreshold regime with $n = 1.5$ then $\bar{v}_{n,op}^2 = 3.75\frac{KT}{C_c}$. From this it can be concluded that the opamp noise is the dominant noise source. In addition, equation 2.8 identifies some key parameters that can be used to reduce the noise floor. The feedback factor β can be increased to reduce the noise. This, however, will result in a lower gain from the switched capacitor stage, and may degrade the dynamic range of the system. Equation 2.8 also indicates that operating the transistors in the subthreshold region will result in lower noise because N is smaller. It is interesting to note that the transconductance of the input and load devices appears only as a ratio in the excess noise factor m. The absolute value of the transconductances does not control the noise. However, their ratio can be used to some extent to control the output noise. Since the folded cascode has the largest m, it can have a larger input referred mean squared noise.

2.2 Gain and Speed

The two stage design has the advantage that it has a potentially higher gain than the telescopic and folded cascode opamps. Gain enhancement in the form of cascode devices can be used on both input and output stages. The telescopic and folded cascode opamps could use regulated cascode gain enhancement[18], but if transistors with low threshold voltages are not available this will not be viable, because the output of the gain enhancement amplifier will have to be very near the supply voltage making it difficult to obtain gain from

the enhancement amplifier. Since the improvement in opamp gain is proportional to the gain of the enhancement amplifier, regulated gain enhancement will not be useful.

The disadvantage of the two stage design is that it is generally slower than the other two topologies. It has lower non-dominant poles which degrade its linear settling time. Furthermore, only the first stage current is used to aid in the settling when the opamp is slew rate limited, which is wasteful. The telescopic opamp, on the other hand, uses all of its current to aid in the settling when it is slewing.

At the device level operating in subthreshold regime offer a higher gain for the opamp because of the larger intrinsic gain of the transistors in that regime. On the down side, transistors in the subthreshold regime are much slower since the transition frequency falls exponentially as we move deeper into the subthreshold regime. Operating on the edge of the subthreshold and moderate inversion may be a compromise. Moreover, if the threshold voltage is comparable with the supply voltage this is the only alternative due to the lack of large enough gate drive.

2.3 Conclusions on Opamp Architercture

From the above discussion a few conclusions can be reached. Firstly, a two stage architecture appears to be the best choice for low voltage operation because it has the largest output swing, a small excess noise factor, and a potentially larger gain. The second conclusion is that operating in the subthershold regime is attractive because of the lower transistor saturation voltage, which translates into a larger swing. Furthermore, in the subthershold region the noise is lower compared with strong inversion. Finally, a fully differential configuration is essential to improve the output swing.

Chapter 3

High Vt Operational Amplifier

In this chapter the design of the first opamp, which uses only MOSFETs with high threshold voltages, is presented. The opamp design is analyzed in detail, in particular the effects of the specific circuit design choices on the dynamic behavior of the opamp will be discussed.

When setting out to design this opamp it was not entirely clear what performance could be achieved, because it was anticipated that many circuits, such as current sources and active loads, would not function properly. Furthermore, the reported low voltage CMOS opamps were generally of low performance, with unity gain frequencies in the order of 1MHz or less and with gains of about 1000 or less[19],[20]. The key performance that was to be optimized was the opamp settling time. It was desired that the system be clocked at a frequency of at least 1MHz. This requires the opamp to have a unity gain frequency higher than 7MHz for 0.1% settling accuracy. Practically, the unity gain frequency that was required was found to be larger than the initial estimates because the opamp settling time had a large slewing component. The gain of the opamp should be about 5K for it to be used in switched capacitor filters or in an analog to digital converter with approximately 10 bits resolution. The remaining performance measures would have to be acceptable, but no performance performance objectives were set initially.

3.1 Overview of the Opamp Design

A two stage opamp was used because neither the folded cascode nor the telescopic opamp could be practically implemented. The reason for this is the threshold voltage of PMOS transistors, which is about 0.8V in the process that was used. Since the circuit should operate at 0.9V, PMOS cascode circuits could not be built. The opamp design shown in figure 3-1(design values are given in table 3.1) has some modifications over the conventional 2 stage opamp. NMOS cascode circuits were used in both the input and output stages to improve the gain. This was needed because of the large channel length modulation factor λ which resulted in a low gain for the opamp. Long channel devices were avoided because of their higher threshold voltage and lower transition frequency. The other main modification was to the tail current source Mt at the bottom of the input differential pair[21],[22]. The gate bias of Mt is changed adaptively to compensate for changes in its drain voltage, which are caused by changes in the input common mode of the opamp. The bias voltage is changed in a manner that maintains a constant current through the transistor, and hence provides a nearly ideal current source over a large range of voltages.

A fully differential design was implemented to increase the opamp output swing. To set the output common mode a switched capacitor common mode feedback circuit was used. The opamp has a pole splitting compensation capacitor C_c to stabilize its operation under feedback. A nulling resistor Rc is used to eliminate the feedforward path created by the compensation capacitor.

3.2 Two Stage Opamp

The gain of the amplifier is mainly dominated by the output resistance of the PMOS load transistors (M5, M6, M25 and M26). This is simply because the output resistance of the NMOS cascode structure is much larger than the single PMOS transistor. The gain when all transistors are operated in the subthreshold regime can simply be written as:

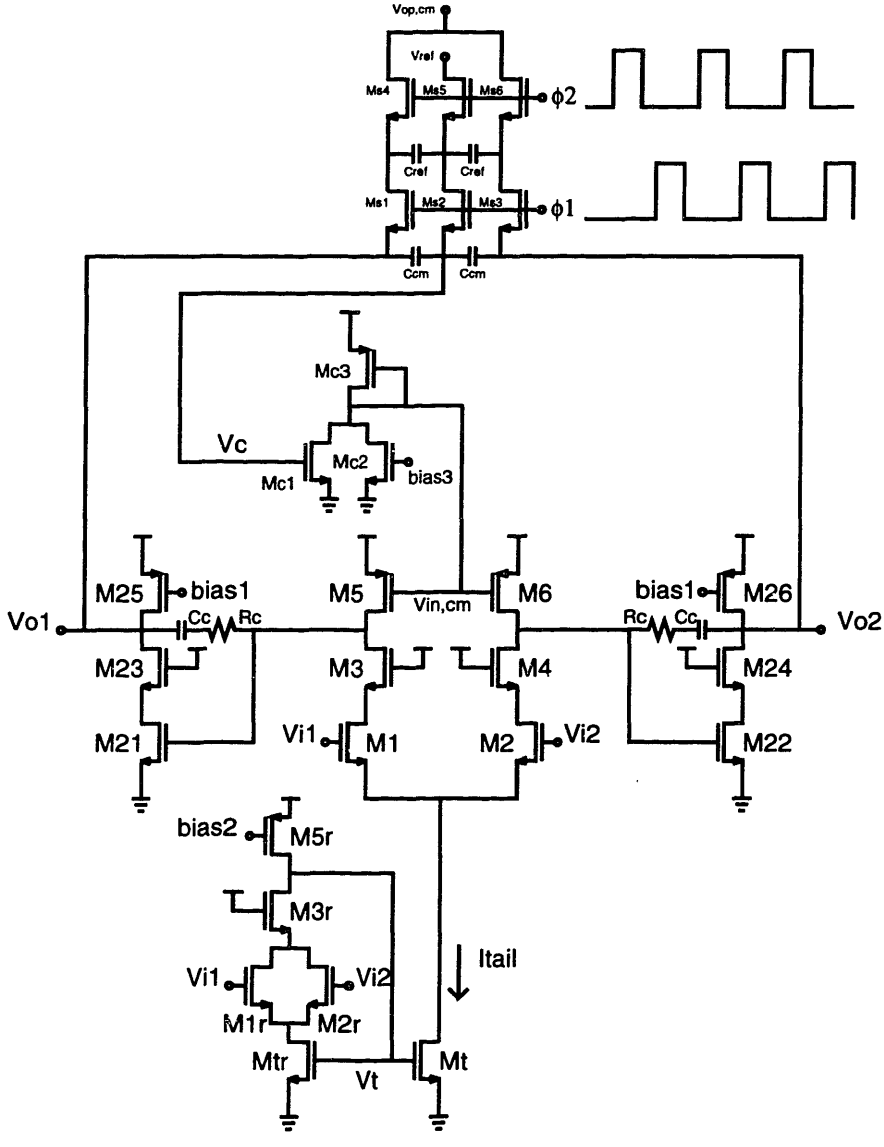

Figure 3-1: High Vt opamp design

Transistor	Length(μm)	Width(μm)
Mt	0.8	250
M1,M2	0.8	133.6
M3,M4	0.8	60
M5,M6	1.4	184.8
M21,M22	0.8	400
M23,M24	0.8	82
M25,M26	1.4	714
Mtr	0.8	125
M1r,M2r	0.8	66.8
M3r	0.8	60
M5r	1.4	184.8
Mc1	0.8	120
Mc2	0.8	80
Mc3	0.8	51
Ms1 to Ms6	0.8	14

Component	design value
Ccm	250fF
Cc	2.5pF
Cload	1.5pF
Rc	1.5kΩ

Table 3.1: High Vt opamp design values.

$$\begin{aligned} A &= g_{m1}r_{o5}g_{m21}r_{o25} \\ &= \frac{1}{(nV_{th})^2\lambda_{o5}\lambda_{o25}} \end{aligned} \tag{3.1}$$

where n is the subthreshold slope ideality factor, V_{th} is the thermal voltage and λ is the channel length modulation factor. From equation 3.1 it can be seen that the only way to improve the opamp gain is to increase the load devices channel length.

The opamp first pole is set by the compensation capacitors C_c, and can be found using the open circuit time constant method:

$$\omega_{p1} = \frac{1}{g_{m21}r_{o25}C_c r_{o5}} \tag{3.2}$$

The unity gain frequency of the opamp can be estimated from the first pole location and the opamp gain assuming a single pole roll off, and is:

$$\omega_u = \omega_{p1} \times A = \frac{g_{m1}}{C_c} \tag{3.3}$$

This is valid if the second pole of the opamp is much higher than the unity gain frequency. The unity gain frequency is strongly related to the time domain behavior of the opamp. Generally, for a given phase margin, the higher the the unity gain frequency the faster is the time domain settling. The settling time constant of the opamp under feedback is:

$$\tau = \frac{1}{\omega_u}\frac{C_f + C_s + C_p}{C_f} \tag{3.4}$$

Where C_f is the feedback capacitor, C_s is the sampling capacitor and C_p is the parasitic capacitor at the input of the opamp. The location of the second pole can be found by using the open circuit time constant method at the output of the opamp when C_c has short circuited:

$$\omega_{p2} = \frac{g_{m21}}{C_l} = \frac{I_{m21}}{nV_{th}C_l} \tag{3.5}$$

where C_l it the opamp load capacitor. The location of the second pole controls the phase margin, and thus influences the time domain behavior of the opamp. Generally, a higher second pole results in a faster settling provided that the system under feedback is not too underdamped. Equation 3.5 shows that the second pole location can be pushed up by increasing the current in the second stage of the opamp. To keep the transistors in the subthreshold region, the output stage transistors must be widened correspondingly.

The compensation capacitor is essential for ensuring a stable system under feedback. Due to the Miller effect, the compensation capacitor appears at the output of the first stage amplified by the gain of the second stage. This creates the dominant pole ω_{p1} at low frequencies. If the second pole of the system is designed to fall above the unity gain frequency, the opamp gain will have a phase margin greater than 45^o.

The compensation capacitor, however, creates a feedforward path, which results in a right hand plane zero that degrades the phase margin and may cause instability. The feedforward path was impeded, in this design, by using the nulling resistor R_c[14]. This moves the zero form the right to the left hand plane. R_c can be also used to cancel the zero, if it chosen to equal $\frac{1}{g_{m21}}$. The nulling resistor is usually implemented using a MOSFET operating in the triode regime. This provides good matching with the $\frac{1}{g_{m21}}$. In this circuit, due to the limited power supply, the transistor would not operate properly, because it would not have sufficient gate to source voltage to turn on. Hence, it would not allow sufficient current flow to charge up the compensation capacitor quickly. To avoid these difficulties, R_z was implemented using an un-silicided polysilicon resistor.

3.3 The Cascode Circuits

The cascode structure provides an enhancement of the opamp gain[12]. This is achieved since the output of both stages is no longer loaded by the NMOS transistors. The small

signal output resistance of the cascode circuit is on the order of $r_o^2 g_m$ which can be 25 times larger than output resistance of a single transistor. The adverse effect of the cascode on the frequency response and the settling time of the opamp is negligible. Even when its output resistance begins to fall due to the effect of different parasitic capacitances including the one at the source of M3 in figure 3-1, the resistance of the load PMOS transistors remains dominant. The cascode, in fact, helps the time domain settling of the opamp as measured by equation 3.4, by reducing the parasitic Miller capacitance at the input of the opamp.

The cascode circuit in the output stage, however, does reduce the output swing of the opamp. The swing is reduced form $2 \times (V_{dd} - 2 \times V_{dsat})$ to $2 \times (V_{dd} - 3 \times V_{dsat} - V_{margin})$, which is a reduction of $2 \times (V_{dsat} + V_{margin}) \approx 300mV$. This large penalty in swing was paid to improve the opamp gain without effecting its time domain response.

3.4 Replica (Adaptive) Bias Circuit for the Tail Current Source

It is crucial to implement a constant tail current source with a very small minimum output voltage, because the limited supply voltage mandates that only a small voltage be dropped across the tail transistor. Furthermore, the source voltage of the input transistors should not be very large to ensure that only a small back bias is applied. A large back bias would result in a large increase in the threshold voltage, which is very undesirable when the threshold voltage is comparable to the supply voltage. Operating the tail transistor with a very small drain voltage pushes the transistor deep into the triode region where it has a small output resistance, and therefore, would adversely effect the common mode rejection ratio (CMRR) and the negative power supply rejection(PSRR-). Even though a fully differential architecture is used, variations in the tail transistor current are not split evenly between the input differential pair transistors, because of the finite mismatch that always exits between the input transistors. This results in a differential output voltage at the output of the opamp.

To achieve a good CMRR and PSRR- a current source with a large output resistance is needed. The approach that is adopted here is to have a circuit adaptively change the bias

voltage of the tail transistor Mt[21],[22], in a manner that ensures that the current in the tail transistor remains constant even when its drain voltage is reduced to a few millivolts. The circuit that realizes this function is shown in figure 3-1 and is made up of transistors Mtr, M1r, M2r, M3r and M5r. These transistors are sized in a manner similar (replica) to the transistors of the first stage of the opamp. The gates of M1r and M2r are connected respectively to the gates of M1 and M2, which are the inputs of the opamp.

Transistor M_{5r} in figure 3-1 is a current source because it is operated in the saturation regime and has a large gate length. The constant current provided by M_{5r} and the feedback action in the replica circuit, fixes the current flowing in transistor M_{tr}. Since the circuit consisting of M_{tr}, M_{1r}, M_{2r}, M_{3r} and M_{5r} is a replica of the the input stage of the opamp, that is:

$$\frac{(W/L)_{Mt}}{(W/L)_{Mtr}} = \frac{(W/L)_{M1}}{(W/L)_{M1r}} = \frac{(W/L)_{M2}}{(W/L)_{M2r}} = \frac{2(W/L)_{M3}}{(W/L)_{M3r}} = \frac{2(W/L)_{M5}}{(W/L)_{M5r}} \tag{3.6}$$

one can, therefore, conclude that $V_{ds,M_t} = V_{ds,M_{tr}}$ and $I_{d,M_t} = I_{d,M_{tr}}$.

To quantitively show the enhancement that the replica bias circuit offers, a small signal analysis of the circuit is carried out. If an incremental input common mode voltage v_i is applied to the input of the opamp, then the incremental voltage v_t at the gate of the tail current source is:

$$v_t = -\frac{\frac{g_{m_{M1r+M2r}} \times r_{o_{M5r}}}{1+g_{m_{M1r+M2r}} \times r_{o_{Mtr}}}}{1 + g_{m_{Mtr}} \times r_{o_{M5r}}} v_i \tag{3.7}$$

where $g_{m_{M1r+M2r}} = g_{m_{M1r}} + g_{m_{M2r}}$. Superposition theorem can be used to calculate the incremental tail transistor current i_{tail} as a function of v_i:

$$\begin{aligned} i_{tail} &= \frac{g_{m_{M1+M2}}}{1 + g_{m_{M1+M2}} \times r_{o_{Mt}}} \times v_i + g_{m_{Mt}} \times v_t \\ &= \left(\frac{g_{m_{M1+M2}}}{1 + g_{m_{M1+M2}} \times r_{o_{Mt}}} - g_{m_{Mt}} \times \frac{g_{m_{M1r+M2r}} \times r_{o_{M5r}}}{(1 + g_{m_{M1r+M2r}} \times r_{o_{Mtr}})(1 + g_{m_{Mtr}} \times r_{o_{M5r}})} \right) \times v_i \end{aligned} \tag{3.8}$$

Here it is assumed that $r_{o_{Mt}}$ is much greater than $1/g_{m_{M1+M2}}$, which is in this case a reasonably accurate approximation, but it does not generally hold. If it is further assumed that the bias circuit is an exact replica of the first stage then:

$$i_{tail} = \frac{g_{m_{M1+M2}}}{1 + g_{m_{M1+M2}} \times r_{o_{Mt}}} \left(\frac{1}{1 + g_{m_{Mtr}} \times r_{o,M5r}} \right) \times v_i \tag{3.9}$$

From this equation some key dependencies can be identified. First of all, as $r_{o_{Mt}}$, the small signal output resistance of Mt, increases the change in the current i_{tail} would reduce. This is to be expected because the better the tail transistor is to begin with, the better would be the performance of the replica circuit. Secondly, as the loop gain of the replica circuit $g_{m_{Mtr}} \times r_{o_{M5r}}$ increases the current regulation will improve. This result is also expected because the higher the loop gain, the smaller would be the error signal that is generated, and a smaller change in the current would be seen.

If the bias circuit is scaled down it can be shown that the same results would apply. At high frequencies, however, the scaled down version of the bias circuit would have an inferior performance. This is due mainly to the fact that the loop gain of the replica circuit would have poles at lower frequencies because the circuit transconductance is reduced while the circuit load, which is the gate capacitance of Mt, remains unchanged. Hence, the loop gain would start to fall at lower frequencies. Scaling down the bias circuit can, however, be used to reduce the power consumption.

Figure 3-2 plots the tail current source current versus the input common mode and the drain voltage of the tail transistor. As can be seen clearly from the plots the current remains constant over a very large range of input common mode values. It can also be noted that the tail transistor provides a constant current up to the point when its drain voltage is just a few millivolts. Figure 3-3 shows the small signal impedance of the tail transistor. At low frequencies the impedance is very high which is due to the current regulation by the bias circuit. At high frequencies the impedance falls because the bias circuit does not function as effectively due to its finite bandwidth. The impedance converges to r_{Mt} at high enough frequencies. The data in these plots are simulation results generated by SPICE.

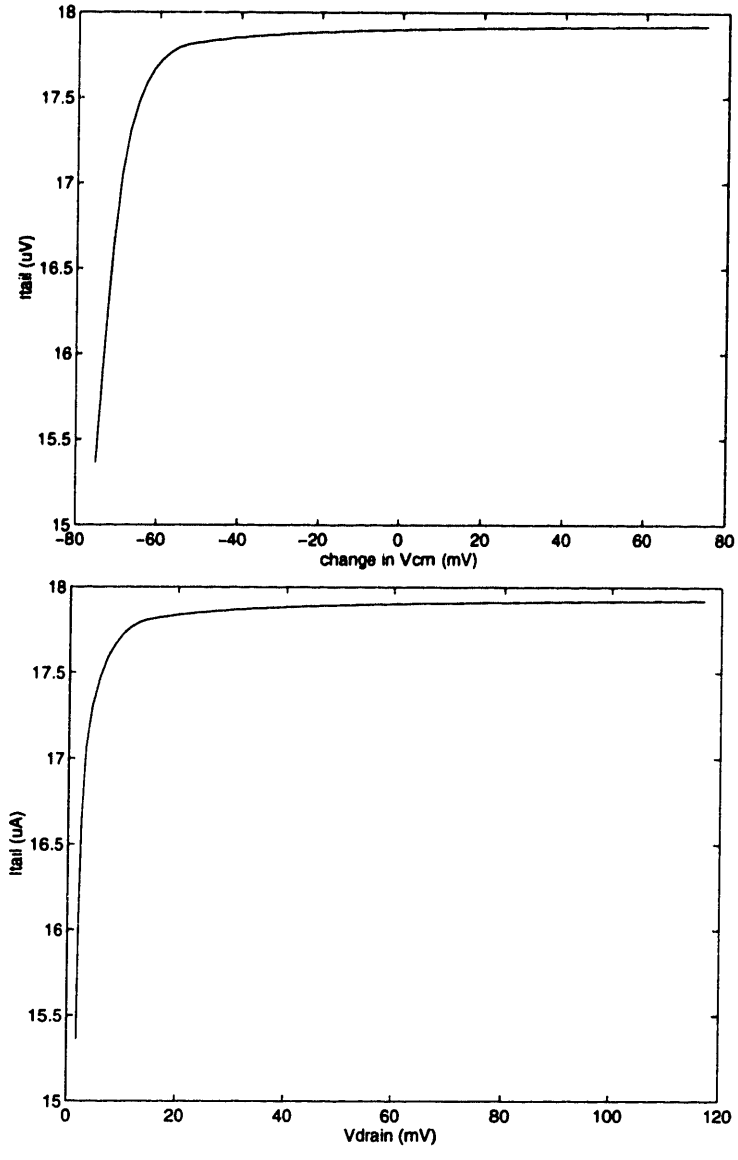

Figure 3-2: The current in the tail transistor current source as a function of the input common mode and the drain voltage.

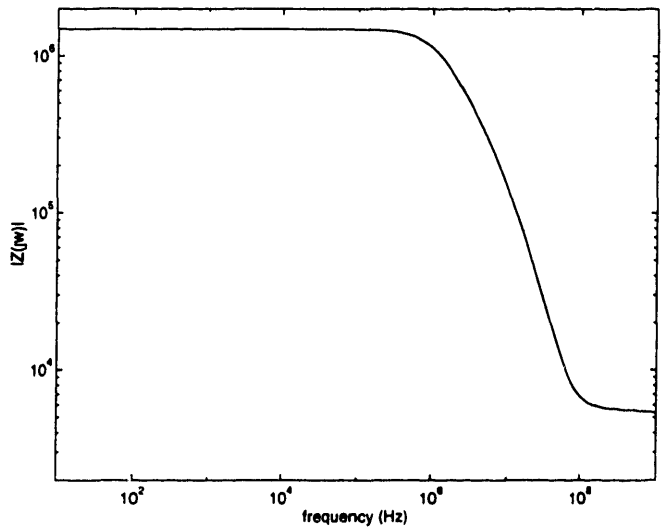

Figure 3-3: Small signal tail current source impedance.

3.5 The Common Mode Feedback Circuit

In a fully differential opamp the output common mode can take on any value depending on the transistor parameters in the circuit. Since the opamp inputs can only control the differential output, a circuit is needed to set the output common mode of the opamp[14]. This can be achieved if the output common mode is sensed and then fed-back to a common mode input. The feedback action sets the output common mode to a value that can be controlled through the design of the feedback circuit. To maximize the output swing of the opamp the output common mode should be set to:

$$V_{out,cm} = 2 \times V_{ds,sat} + V_{margin} + \frac{V_{dd} - 3 \times V_{ds,sat} - V_{margin}}{2} \tag{3.10}$$

A switched capacitor implementation of the feedback circuit [11] was chosen, and is shown at the top of figure 3-1. Capacitors C_{cm} in the common mode feedback circuit (CMFB) circuit senses the output common mode voltage and generate a small signal voltage v_c, which is independent of the small signal differential mode output and is equal to:

$$v_c = \frac{C_{cm}}{2 \times C_{cm} + C_{gate,Mc1}} \times (v_{o1} + v_{o2}) \tag{3.11}$$

where $C_{gate,Mc1}$ is the gate capacitance of transistor Mc1. The voltage v_c is applied to an inverting stage made up of Mc1, Mc2 and Mc3. The output of the inverting stage is connected to the common mode input of the opamp, which is at the gates of M5 and M6. The common mode input passes through both stages of the opamp and is amplified, completing the CMFB loop. The inverting stage was added to ensure that the loop feedback is negative. However, this stage adds high frequency poles and zeros, which degrade the phase margin of the common mode loop. To compensate for this transistor, Mc2 was added to reduce the gain of the stage by reducing the transconductance of Mc1.

The CMFB circuit operates in two phases. During phase $\phi 2$ a voltage $V_{op,cm} - V_{ref}$ is placed across capacitors C_{ref}, where $V_{op,cm}$ is the desired output common mode voltage, and V_{ref} is the bias voltage at the gate of Mc1 that is needed to get the desired output common mode. During $\phi 1$ charge from C_{ref} is transfered to C_{cm}, and after a few clock cycles the dc voltage across C_{cm} will converge to $V_{op,cm} - V_{ref}$. The common mode voltage at the output of the opamp will then be $V_{op,cm}$. After the desired ouput common mode level is established, the charge accross C_{cm} has to be periodically refreshed to compensate for the charge that leaks away through the switches.

Practically, the output common mode does not converge to $V_{op,cm}$, but is offset from it, reducing the opamp swing by four times this offset. For low voltage operation the reduction in swing is important and must be minimized. One source of the output common mode offset is the charge injected from the switches into capacitors C_{cm}. To minimize this offset, the switches and C_{cm} must be sized properly to reduce the injected charge, and to reduce the voltage change that results due to the injected charge.

3.6 Stability of the Common Mode Loops

In the discussion up to this point two mechanisms that control the common mode behavior of the opamp have been identified, namely the common mode feedback circuit and the replica tail transistor bias circuit. Placing the opamp in differential feedback effects the common mode stability. This differential feedback is of the positive feedback nature because the opamp is non-inverting form a common mode point of view. It is important to ensure that the opamp is stable under such conditions. The positive feedback must be overcome by the negative feedback in order to ensure stability. The use of the replica bias circuit for the tail transistor accomplishes this because it significantly reduces the opamp common mode gain, and hence reduces the positive feedback. It is also necessary that these common mode loops have fast and accurate time domain settling to avoid adversely effecting the opamp output swing. A detailed analysis of the common mode settling is rather complicated and is best left for computer simulations.

3.7 The Switches

In the common mode feedback circuit, transistor switches are at the core of the operation of the circuit. In this section the approach that was used to operate these switches is explained. The key limitation in this application is that the threshold voltage is only slightly smaller than the supply voltage. If NMOS switches are used, and the clock is limited by the supply, the switches will only function properly when the signal is near the negative rail (ground in this case). This will require that all signals, which are switched, to be near the negative rail, include the signal at the output of the opamp. This would severely limit the output swing of the opamp which is very undesirable. To circumvent this problem, the clocks were boot strapped [23] to about twice the supply voltage, enabling all switched signals to take on any value within the supply range without turning the switches off.

Two additional considerations were taken into account when designing the switches. The switches must be small enough to reduce charge injection and the parasitic capacitance, and

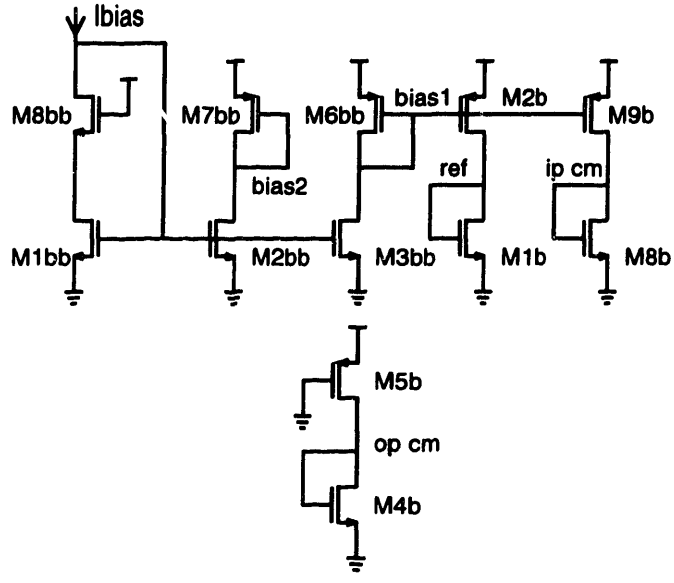

Figure 3-4: Opamp bias circuit.

they must be wide to enough to allow enough current to pass during the switch on state. The appropriate switch size was selected using SPICE simulations.

3.8 The Bias Circuit

The bias circuit for the opamp is shown in figure 3-4, with the transistor sizes summarized in table 3.2. No cascode current sources are used because of the supply voltage limitation. The small output resistance of the uncascoded transistors degraded the power supply rejection, and the bias voltages change significantly as the supply voltage changes[12].

Two interesting problems arise when designing the bias circuit. The first is generating bias voltages that lie near the middle of the supply voltage. The second is generating a

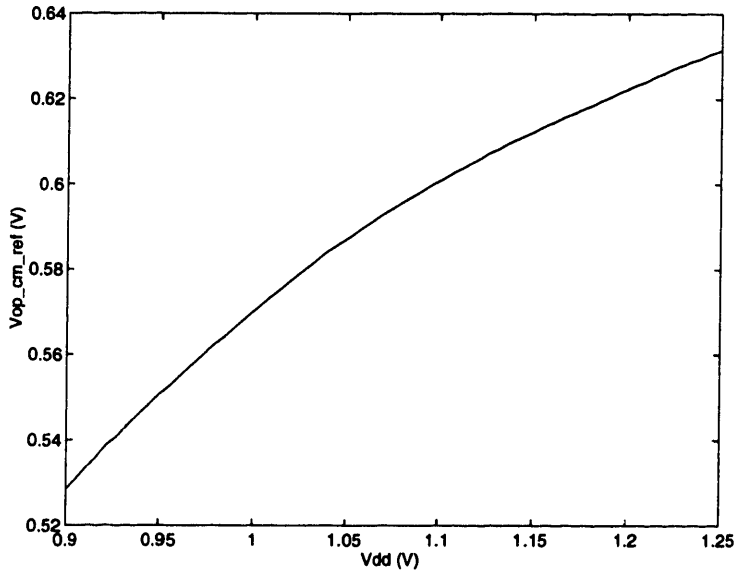

Figure 3-5: The output common mode reference changes with the supply voltage to maximize the opamp swing at 0.9V.

bias very near the supply voltages. In the first case a diode connected transistor was driven deep into weak inversion by using a very large device. The output common mode reference voltage is an example of such a circuit. It is made up of transistors M5b and M4b. The output common mode reference, unlike other bias voltages, must change with the supply voltage as shown in figure 3-5. This is to guarantee the largest possible opamp output swing under the worst case supply voltage of 0.9V.

To generate the bias voltages that are close to the the supply, the transistor that acts as the current source and drives a diode connected transistor, was operated in the subthreshold region. This provides a small drain saturation voltage, and the circuit can be effectively used to generate bias voltages as closes as 100mV to the tail. In figure 3-4 transistors M2bb and M7bb generate a bias voltage of 100mV for the replica tail transistor bias circuit of figure 3-1.

When bias voltages less than 100mV away from the rails were needed the rail voltages were used as the bias. Transistors M3, M4, M23 and M24, in figure 3-1, were biased in this manner. For M3 and M4, which lie in the first stage of the opamp, this is not a problem.

Transistor	Width(μm)	Length(μm)
M1bb	33	0.8
M2bb	44	0.8
M3bb	33	0.8
M7bb	87	0.8
M6bb	64	0.8
M8bb	17	0.8
M1b	33	0.8
M2b	19	0.8
M4b	500	0.8
M5b	90	8
M8b	50	0.8
M9b	100	0.8

Table 3.2: High Vt opamp bias circuit design values.

However, for transistor M32 and M42, which are in the second stage, this impacted the gain and the swing of the opamp. At high supply voltages the source voltage of M32 and M42 is higher than its value at low voltages. This causes M32 and M42 to prematurely go into the triode region, eliminating the benefit of the gain enhancement due the cascode.

Chapter 4

Low Vt Operational Amplifier

In this chapter the design of the second opamp will be presented. This opamp makes use of low threshold voltage MOSFETs and will be called the low Vt opamp. Since this opamp uses basically the same architecture of the two stage opamp of the last chapter, this chapter will emphasize the aspects of the design that are different.

There has been only one report of the usage of low threshold MOSFETs in the design of low voltage analog circuits[24]. That work avoided the use of switched capacitor techniques in the design because of the poor performance of the MOS switches. This work will attempt to circumvent this problem, because discrete time signal processing techniques offer significant advantage over continuous time techniques.

4.1 Overview of the Opamp Design

The opamp circuit is shown in figure 4-1 and the design values are summarized in table 4.1. The opamp uses a fully differential two stage design for the reason discussed in chapter 2. The transistors were not operated in the subthreshold regime, because of the lower transition frequency of the transistors in that regime as compared to the strong inversion regime. The transistors in the output stage of the opamp were, however, driven to the edge of strong inversion in order to maximize the output swing.

From the figure it can be seen that the first stage of the opamp has been modified to a telescopic opamp. This was done to improve the gain of the opamp, which was degraded by the low intrinsic gain of the low Vt MOSFETs. The bias circuit for the tail transistor Mt uses the replica biasing idea presented in the previous chapter[21],[22]. This replica circuit regulates the tail transistor current against variations in the opamp input common mode and variations in the negative supply voltage. The common mode feedback (CMFB) circuit utilizes the replica bias stage as the inverting stage [25] needed to stabilize the common mode loop. The function of the CMFB circuits is to set the output common mode voltage of the opamp. Capacitor C_{os1} and C_{os2} are part of an offset cancelation circuit that measure the opamp offset, stores it on these capacitors, and applies it to the opamp inputs at the gates of M_7 and M_8. Frequency compensation is provided by capacitor Cc and nulling polysilicon resistor Rz.

4.2 The Telescopic Input Stage

The main motivation behind using cascode circuits in the first stage of the opamp was to improve the gain. The first stage makes use of only low threshold MOSFETs, which have a channel length modulation factor λ significantly larger than high Vt MOSFETs as can be seen in the plot of figure 4-2. This results in low output resistance of the transistors and, therefore, a lower gain. Using cascode circuits results in an improvement in gain by a factor of $g_m r_o$[12]. The gain could be further improved by using high Vt PMOS (HPMOS) transistors in place of M_7 and M_8. This would help because the gain is dominated by the PMOS cascode, and HPMOS offer a larger output resistance. This was not done for two reasons. The first reason is that using HPMOS transistors would result in a larger opamp noise. The second reason is the possible degradation that could occur to the time domain response of the opamp.

The noise due to the first stage load devices appears as an excess noise factor in the input referred noise of the opamp. Reducing this noise is one method of improving the dynamic range of the opamp. The noise due to the load devices is shown in figure 4-3 in

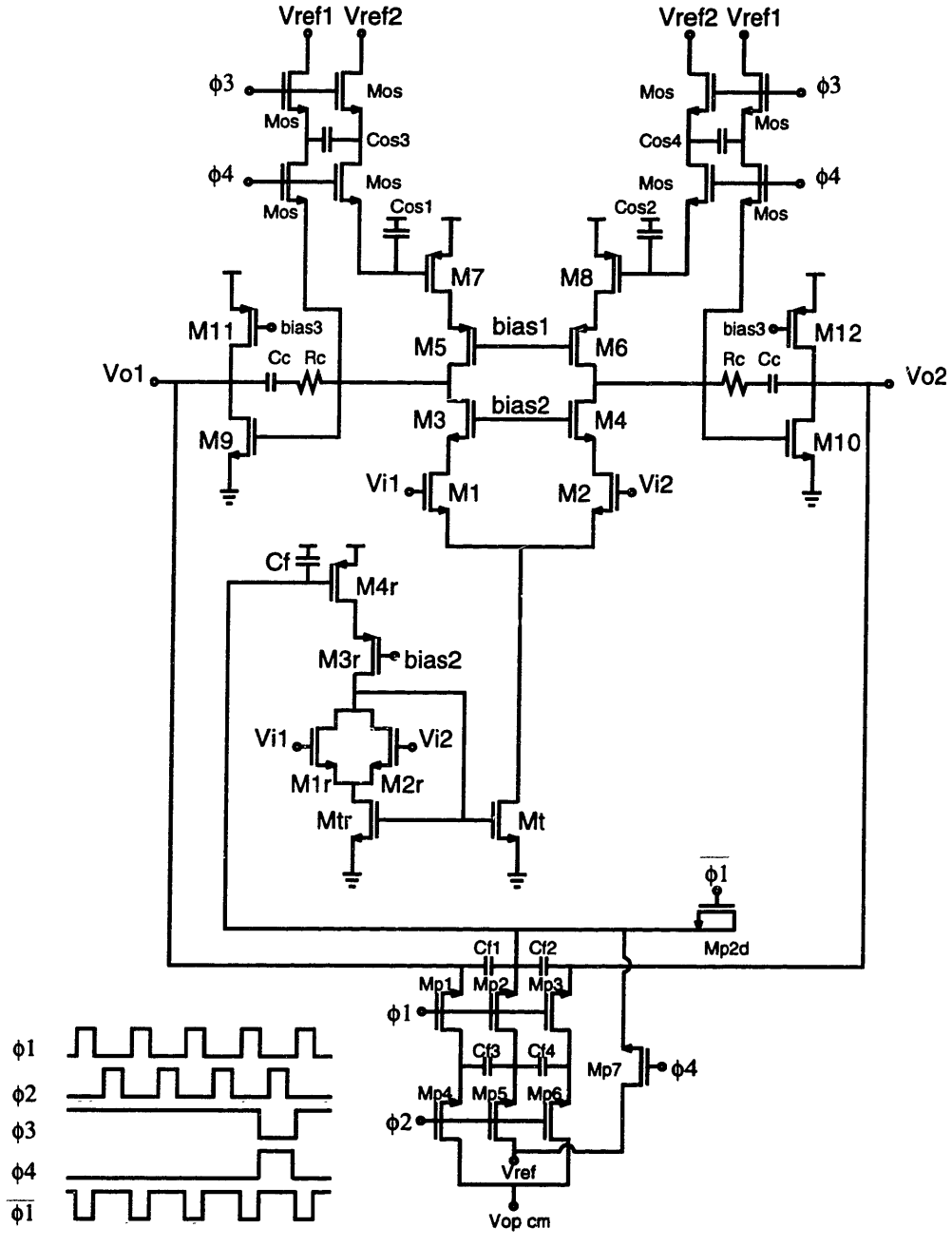

Figure 4-1: Low Vt opamp design

Transistor	Length(μm)	Width(μm)
Mt	1.6	308
M1,M2	2	20.2
M3,M4	1.2	118
M5,M6	2	177.6
M7,M8	2.4	210.4
M9,M10	1.6	221.6
M11,M12	2	408
Mtr	2	108
M1r,M2r	2	5.6
M3r	2	84
M4r	1.2	315.2
Mp1 to Mp6	0.8	14
Mp2d	0.8	14
Mos1 to Mos6	0.8	14
Mos7,Mos8	0.8	7

Component	design value
Cf1,Cf2	200fF
Cf3,Cf4	450fF
Cos,Cos1,Cos2	250fF
Cload	2pF
Cc	1.6pF
Rc	1.6kΩ

Table 4.1: Low Vt opamp design values.

various regions of operation but with a fixed drain current. Sketched in the figure is the spot value of the mean square of the transistor noise normalized by dividing it by the drain current and the product of Boltzmann constant and the temperature (KT). The equations used in drawing these plots are summarized in table 4.2. It can be seen from the plot that as the transistors are pushed deeper into strong inversion, the noise contribution of the transistors decreases. Since HPMOS transistors can only be operated in the subthreshold region, they would increase the excess noise of the opamp.

To understand the effect of the HPMOS load transistors on the opamp time domain response the cascode circuit must be first studied. The discussion that follows is general,

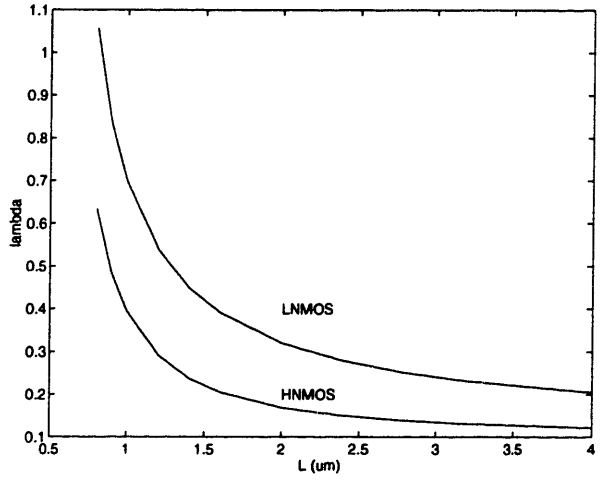

Figure 4-2: Channel length modulation factor λ for low threshold and high threshold MOSFETs.

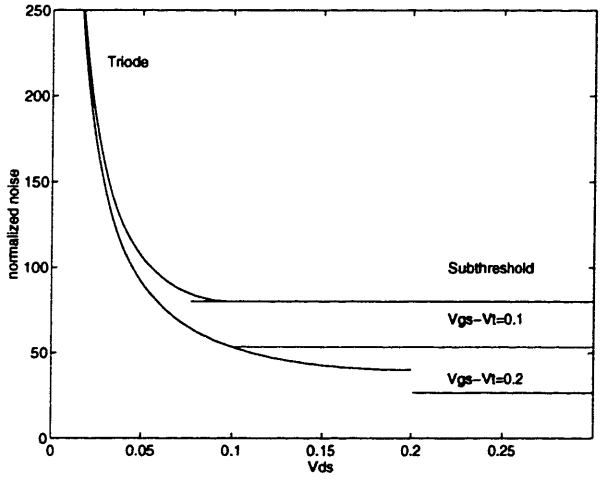

Figure 4-3: The normalized noise due to a PMOS load transistor operating in various regions of operation at a fixed drain current.

Region of operation	$\frac{\bar{i}_{eq}^2}{\Delta f}$
Saturation	$\frac{16KT}{3}\frac{I_D}{V_{gs}-V_t}$
Triode	$4KT\frac{I_D}{V_{ds}}$
Weak inversion	$2KT\frac{I_D}{V_{th}}$

Table 4.2: The spot value of the transistor drain current noise under different operating conditions.

and must be considered even when low threshold PMOS transistors (LPMOS) are used as loads. The impact of HPMOS is however not as pronounce.

The cascode circuit impedance has a high frequency pole and zero due to the parasitic capacitance C_{par} that is shown in figure 4-4. The origin of the pole and zero is shown in figure 4-4, which sketches the output impedance of the cascode structure. The straight line in the figure is the output impedance in the absences of both the load and parasitic capacitances. The dashed line is the output impedance when the parasitic capacitor is taken into account. The output impedance reduces to the value of a single transistor M_1 as the capacitor C_{par} shorts out. The total impedance of the cascode can be found by parallel connecting the dashed line impedance with the impedance of the load capacitor(C_l). This is plotted as the dotted line. As can be seen the shorting out of transistor M_2 results in a pole-zero pair(doublet).

The effect of the cascodes pole-zero doublet on the magnitude and phase response of the opamp is not very significant. However, its effect on the settling behavior can be important[26]. If the pole-zero doublet falls below the the unity gain frequency of the opamp, it will introduce a slow settling component in the dynamic response of the opamp in feedback. This can be seen in the root locus of the opamp under feedback as sketched in figure 4-5. Figure a) sketches the root locus for an opamp which does not have a doublet, where it is assumed that the opamp has only two poles. Figure b) shows the root locus in the presences of a doublet. From these diagrams it can be concluded that, for a given feedback factor, the second opamp will have a lower frequency pole. If the magnitude of

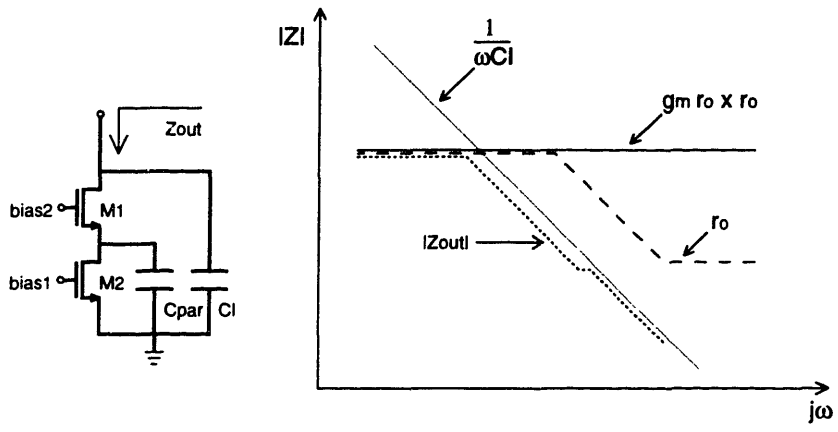

Figure 4-4: Cascode circuit.

the settling due to this pole is comparable to the magnitude scale of interest in the specific application, the opamp will settle to its final value slower.

This problem would occur if the load transistors M_7 and M_8 in figure 3-1 are driven deep into the subthreshold regime. This mode of operation will require the use of large transistors, which would have large parasitic capacitances.

4.3 Replica Tail Bias Circuit and Common Mode Feedback Circuit

The replica tail bias circuit [21],kush and the common mode feedback circuit [11] are shown in figure 4-1. The replica tail bias circuit is made up of transistors M_{tr}, M_{1r}, M_{2r}, M_{3r} and M_{4r}. The CMFB circuit is made up of the capacitors labeled C_f and the LNMOS switches labeled M_p. It uses the voltage $V_{oc,cm}$ as a reference for the desired output common mode voltage, and the voltage V_{ref} as a reference for the desired dc bias at the gate of M_{4r}. The principle of operation of both the replica tail bias circuit and the CMFB circuit is essentially the same as in the high Vt opamp, but a few differences exist. The replica stage was used as the inverting stage of the common mode feedback loop[25]. This reduces the area and power

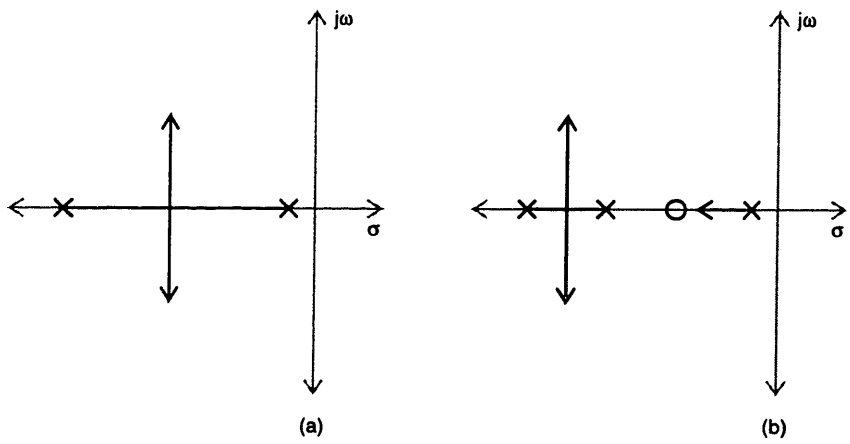

Figure 4-5: Root locus of an opamp a) without a pole-zero doublet b)with a poles zero doublet.

consumption. But, more importantly, the common mode feedback circuit configured this way provides an additional means of regulating the tail transistor current. Figure 4-6 shows how the tail transistor current changes as function of the input common mode and the tail transistor drain voltage. As can be seen form this diagram, the tail transistor maintains a nearly constant current even as the drain voltage falls to a few millivolts.

The charge injected on capacitors Cf1 and Cf2 results in a shift in the output common mode which degrades the output swing of the opamp. The charge injection was reduced by using the minimum switch size required for proper operation of the loop. Furthermore, transistor Mp2d was added and clocked by $\overline{\phi 1}$ the inverse of the clock of Mp2. As Mp2d turns on it draws most of the charge injected by Mp2. The combination of these methods reduced the output common mode offset to an acceptable level.

Capacitor Cf reduces the feedback factor of the common mode loop and, therefore, relaxes the stability requirements of the CMFB loop. The combination of CMFB and replica bias ensured that when the opamp is placed in feedback, the common mode loops are stable in spite of the positive feedback.

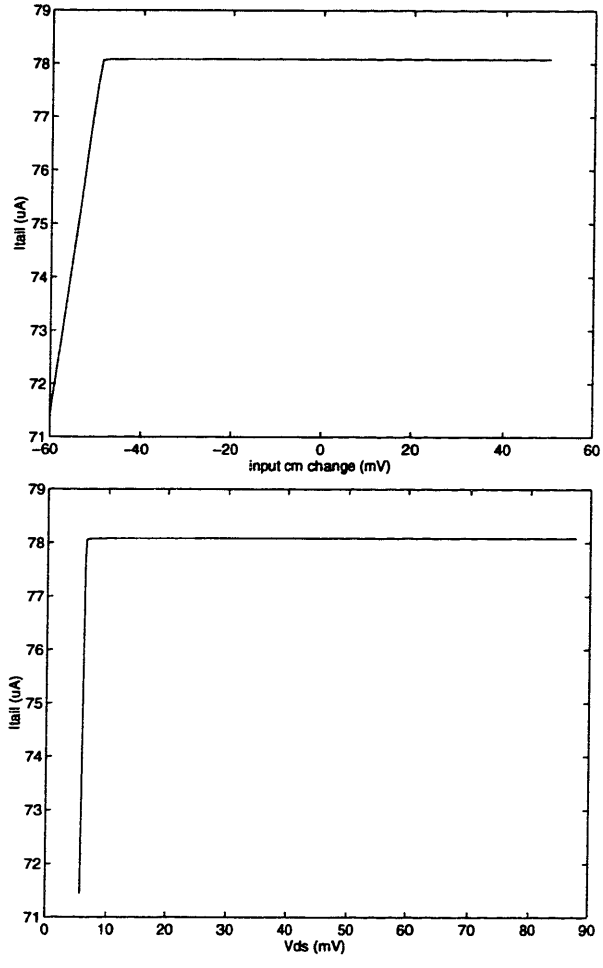

Figure 4-6: The tail transistor current as a function of the input common mode and the tail transistor drain voltage.

4.4 Offset Cancelation

LPMOS transistors were used as load devices for the first stage of the opamp to reduce the load devices noise contribution. The LPMOS devices unfortunately suffer from poor matching even between adjacent devices. For example, in the technology that was used in this work the variation in the threshold voltage can be as high as ± 35mV for devices that are only 50μm apart. This translates into a large opamp offset voltage that can be in the 100mV range, making it necessary to perform offset cancelation.

The offset cancelation circuit is shown at the top of figure 4-1. The circuit is composed of the capacitors label C_{os} and the switches labeled M_{os}. It uses the voltage V_{ref1} as a reference for the desired voltage at the output of the first stage of the opamp, and the voltage V_{ref2} as a reference for the desired dc bias voltage at the gates of M_7 and M_8. The circuit samples the opamp offset voltage and stores it on the capacitors C_{os1} and C_{os2} with a polarity that cancels the opamp input referred offset. This technique is called the auxiliary input offset cancelation because it uses inputs others than the opamp inputs to apply the offset cancelation signal[9].

During phase ϕ_3 a voltage $V_{ref1} - V_{ref2}$ is stored across capacitors C_{os3} and C_{os4}. The offset cancelation circuit operates during phase ϕ_4, in which the opamp is placed in feedback with capacitors C_{os3} and C_{os4} acting as the feedback capacitors. The feedback capacitors also act as level shifters due to the voltage $(V_{ref1} - V_{ref2})$ that is stored on them during ϕ_3. This is needed because of the different dc levels at the output of the first stage and the gates of transistors M_7 and M_8. The feedback is placed across the first stage only, because the gain of the opamp is mainly due to the first stage. In addition, any attempt to include the second stage would require the use of an additional inverting stage to stabilize the feedback from a common mode perspective.

Let us define V_{os} as the offset of the opamp as seen form the inputs of the opamp when no offset cancelation signal is applied. The offset seen from the auxiliary inputs is hence $V_{os}^{'} = V_{os}\frac{g_{m1}}{g_{m7}}$. Further, if we define the gain from the opamp inputs to the output of the first stage to be A_1, then the gain form the auxiliary inputs would be $A_1^{'} = A_1\frac{g_{m7}}{g_{m1}}$. It is

straight forward to show that the new offset, as seen for the auxiliary inputs, after the end of the offset cancelation phase is:

$$\begin{aligned} V'_{os,new} &= V'_{os}\frac{C_{os1}+C_{os3}}{C_{os1}+(1+A'_1)C_{os3}} \\ &\approx V'_{os}\frac{1}{A'_1\beta_{os}} \end{aligned} \tag{4.1}$$

where $\beta_{os} = \frac{C_{os3}}{C_{os1}+C_{os3}}$, and is the feedback factor of the offset cancelation loop. Here it is assumed that $C_{os1} = C_{os2}$ and $C_{os3} = C_{os4}$. The new offset when referred to the input of the opamp is equal to:

$$V_{os,new} = \left(\frac{g_{m7}}{g_{m1}}\right)^3 \frac{V_{os}}{A_1\beta_{os}} \tag{4.2}$$

From this equation it can be seen that the offset voltage is reduced by the gain of the opamp first stage, a reduction in the order of $(g_m r_o)^2$. It can be also concluded that reducing g_{m7} and increasing β_{os} can further reduce the offset voltage. However, reducing g_{m7} will result in a slower convergence of the offset cancelation loop and was avoided here. Furthermore, increasing β_{os} is not a very effective method of improving the offset, because the value of C_{os1} is set by the duration the voltage has to be maintained across it, while C_{os3} weakly controls β_{os}.

If the common mode feedback loop is active during the offset cancelation phase, the current in the first stage of the opamp does not converge to a specific value, because no reference value is defined for the current. Due to this problem, the common mode feedback loop is disabled during the offset cancelation phase, by connecting the gate of M_{4r} to the reference voltage V_{ref} using M_{p7}. Although this perturbs the output common mode of the opamp, the output common mode need not be defined, because the opamp output is not used during offset cancelation.

A final remark on the offset cancelation circuit is concerned with C_{os1} and C_{os2}. These capacitors have their top plate connected to V_{dd}. This significantly improves the positive power supply rejection of the opamp. If the top plates were connected to ground, for exam-

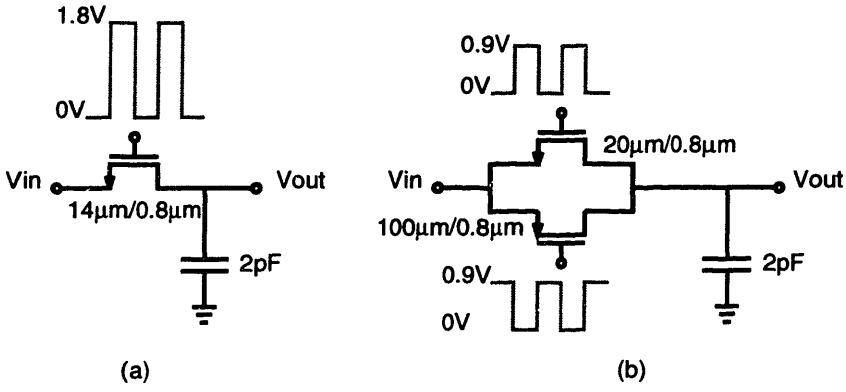

Figure 4-7: Test circuits to measure the performance of the switches.

ple, any variation in V_{dd} will appear at the inputs of M_7 and M_8 and will be transformed, by the mismatch of these devices, into a differential signal at the output of the opamp.

4.5 The Switches

Two approaches were considered for implementing the switches. The first approach involves the use of a single minimum length LNMOS transistor clocked with twice the supply voltage during the clock high state[23]. The second approach involved the use of a LPMOS and a LNMOS both with minimum gate lengths[27]. The clock is connected to gate of the LNMOS and its inverse to the gate of the LPMOS. The clock level is equal to the supply voltage V_{dd} during the high state and ground during the low state.

SPICE simulations were run for both approaches using the test circuit of figure 4-7. The simulation results are shown in figure 4-8. The second approach (shown in the bottom plot) results in a slower capacitor charging time, specially when the input signal is near the middle of the supply voltage, because neither transistor is on strongly enough to support a large current. The first approach, on the other hand, results in a fast charging of the

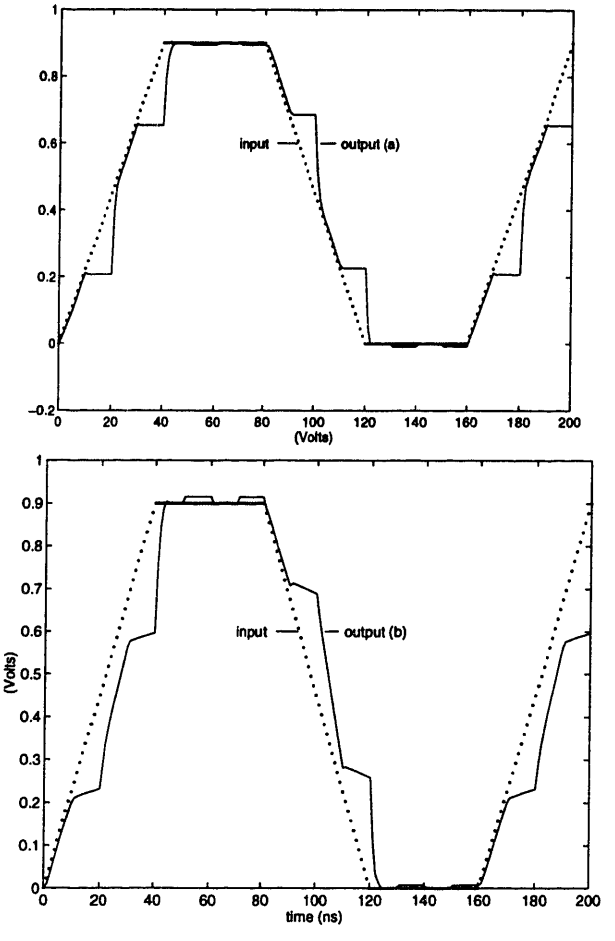

Figure 4-8: SPICE simulation of the test circuits of figure 4-7.

capacitor(shown in the upper plot), and was selected for this reason. The disadvantage of this approach is that it requires the complexity of clock boot strapping.

4.6 The Bias Circuit

The opamp bias circuit is shown in figure 4-9, and table 4.3 gives the transistor design values. The bias circuit makes use of cascode current sources to provide good power supply rejection[12]. The use of LPMOS transistors, however, can result in bias voltages that are off the design values, due to the large variation in the LPMOS transistor threshold voltage.

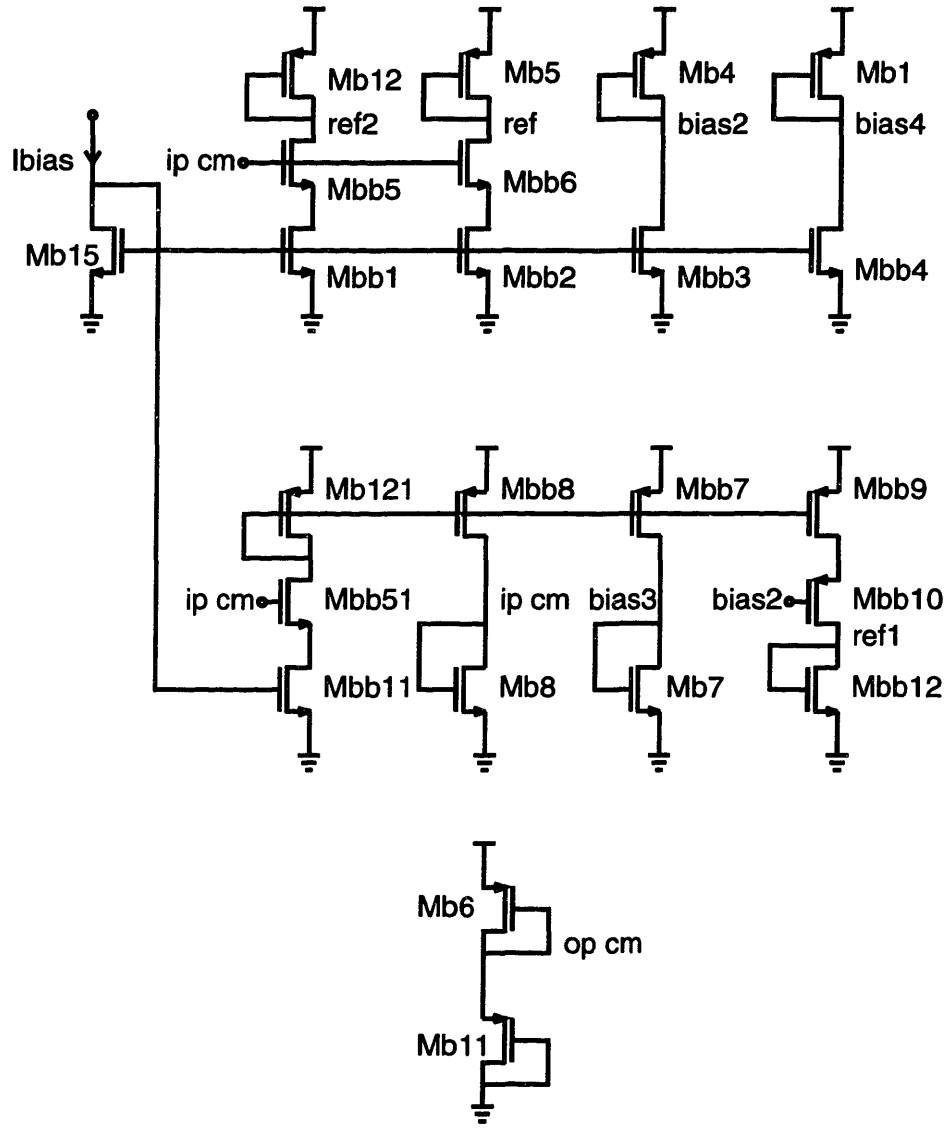

Figure 4-9: Opamp bias circuit.

Transistor	Vt	Width(μm)	Length(μm)
Mbb1	low	61.2	2
Mbb11	low	61.2	2
Mbb2	low	61.2	2
Mbb3	low	62	2
Mbb4	low	60	2
Mbb5	low	32	2
Mbb51	low	32	2
Mbb6	low	30	2
Mbb12	low	57.2	2
Mb7	high	72	2
Mb8	high	133.2	2
Mb15	low	57.2	2
Mb6	low	150	1.6
Mbb7	low	120	2.4
Mbb8	low	114	2.4
Mbb10	low	96	2
Mbb9	low	98	2
Mb1	low	85	2.4
Mb4	low	54.8	6.4
Mb5	low	264	1.2
Mb11	low	150	1.6
Mb12	low	99	2.4
Mb121	low	99	2.4

Table 4.3: Low Vt opamp bias circuit design values.

The effect on the opamp performance is not expected to be significant, because of the use of the common mode feedback circuit.

Generating the opamp output common mode reference for the common mode feedback circuit used two diode connected LPMOS transistors M_{b11} and M_{b6}, shown in figure 4-9. This configuration ensures that the output common mode reference is in the middle of the supply voltage regardless of the actual value of the supply. This provide the maximum opamp swing at all supply voltages. An alternative approach to this design would be to use a resistive voltage divider, but for the resistive divider to be as power efficient, it would have to use resistor values in the tens of kilo-ohms.

Chapter 5

Simulation Results

In this chapter simulation results will be presented for the high and low Vt opamps. HSPICE simulations were an integral part of the design process of the opamps. The simulations were use to validate circuit design ideas and to optimize circuit performance. Simulations were also used to characterize the final design and to test the robustness against variations in the fabrication process. An important concern was the validity of the simulation results. Level 39 models were used to achieve good simulation accuracy. The models were for the IBM BiCMOS-4S+ BiCMOS process.

5.1 High Vt Opamp

Table 5.1 summarizes the simulated performance of the high Vt opamp. The table contains values for the two extremes of the expected operating voltage 0.9V and 1.25V. Most of the performance metrics degrade as the supply voltage is reduced. The most notable reduction is in swing, which reduces by 47%. The power consumption reduces, with decreasing supply voltage, as a direct consequence of the reduction in voltage and the decrease of the second stage current.

The frequency domain magnitude and phase response of the opamp is shown in figure 5-1. The response of the system to a 575mV step input in shown in figure 5-2, where a long

	Units	V_{dd}=0.9V	V_{dd}=1.25V
DC gain	-	4.6K	4.7K
Unity gain frequency	MHz	12.8K	15.1K
Phase margin	degrees	55	58
Output swing	mV	1150	2160
0.1% Settling time (linear)	ns	132	124
0.1% Settling time (step size)	ns(mV)	182(575)	168(575)
Slew rate	V/μs	6.4	7.8
Opamp power	μW	81	129
Total power	μW	156	312
Input referred noise	nV/$\sqrt{Hz}$	17.5	16.2
Offset voltage	mV	35	39
CMRR	dB	27	27.5
PSRR+	dB	42.8	40.3
PSRR-	dB	25.7	25.6

Table 5.1: Summary of the high Vt opamp simulation performance.

slewing component can be clearly seen. The CMRR, PSRR+, and PSRR- as a function of frequency, and with worst case transistor mismatch, are shown in figures 5-3, 5-4 and 5-5 respectively. All these parameters degrade at high frequencies. The low frequency CMRR and PSRR- are good even though the tail transistor is operated in the triode regime. This is a consequence of the use of replica bias circuit. The performance of the high Vt opamp would allow its use in a 10 bit data converter with a maximum clock frequency of 2MHz.

5.2 Low Vt Opamp

The simulated performance of the low Vt opamp are summarized in table 5.2. The performance of the opamp improves as the supply voltage is increased with the exception of the power consumption which increases. The opamp frequency domain magnitude and phase response is shown in figure 5-6. The step response, shown in figure 5-7, is mainly dominated by the linear component of the settling. The CMRR, PSRR+ and PSRR- are shown in figures 5-8, 5-9 and 5-10 respectively all of which degrade at high frequencies. The

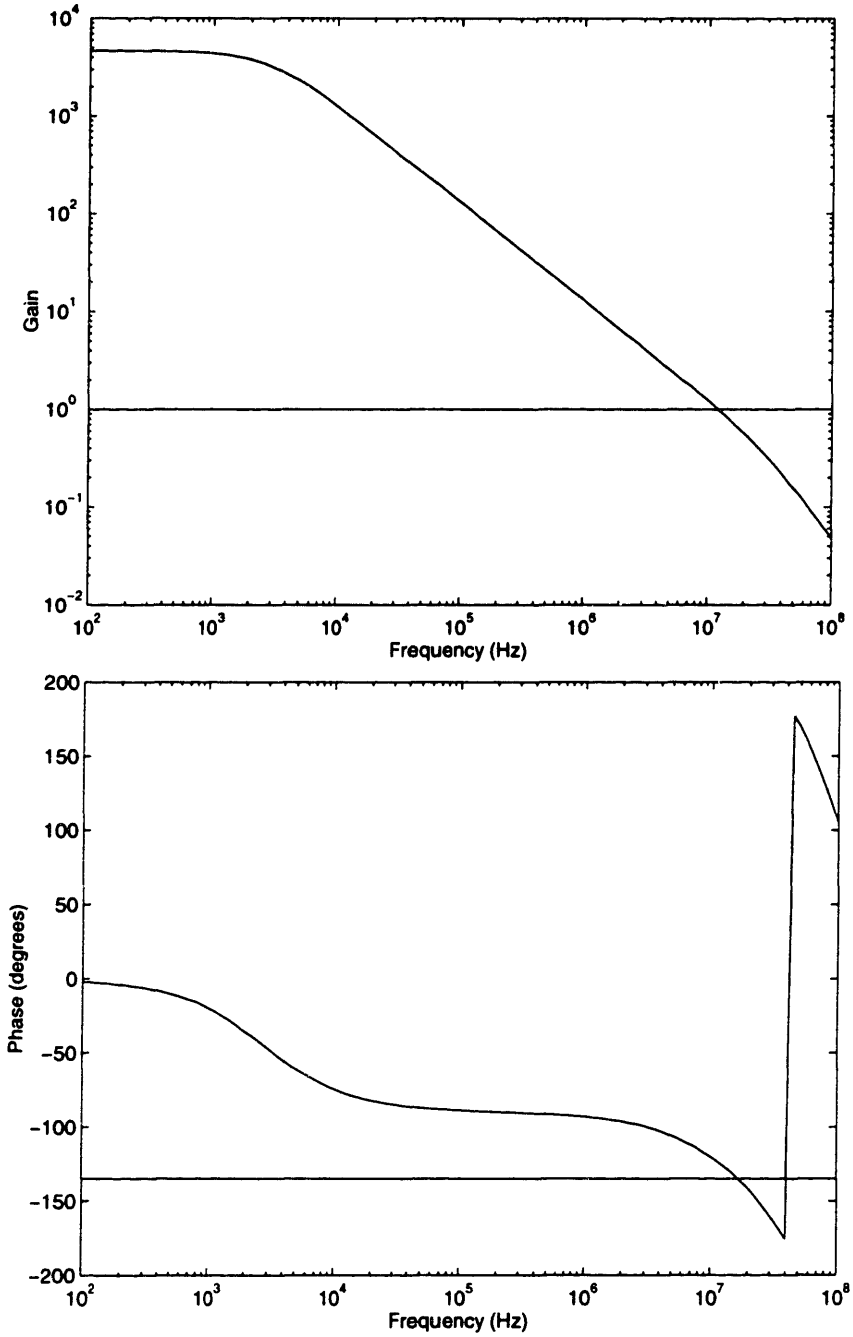

Figure 5-1: High Vt opamp frequency domain magnitude and phase response(V_{dd}=0.9V).

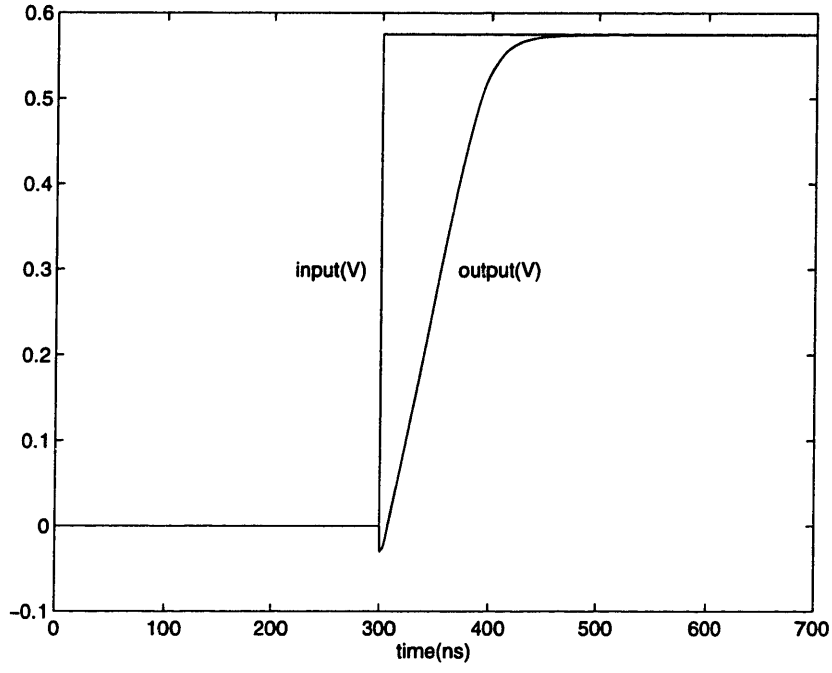

Figure 5-2: High Vt opamp full scale output step response(V_{dd}=0.9V).

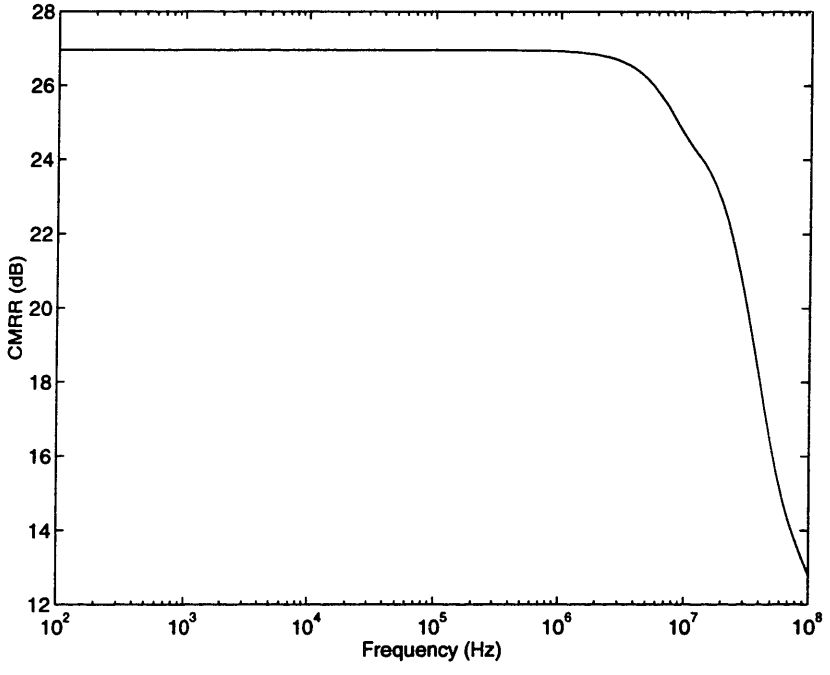

Figure 5-3: High Vt opamp CMRR(V_{dd}=0.9V).

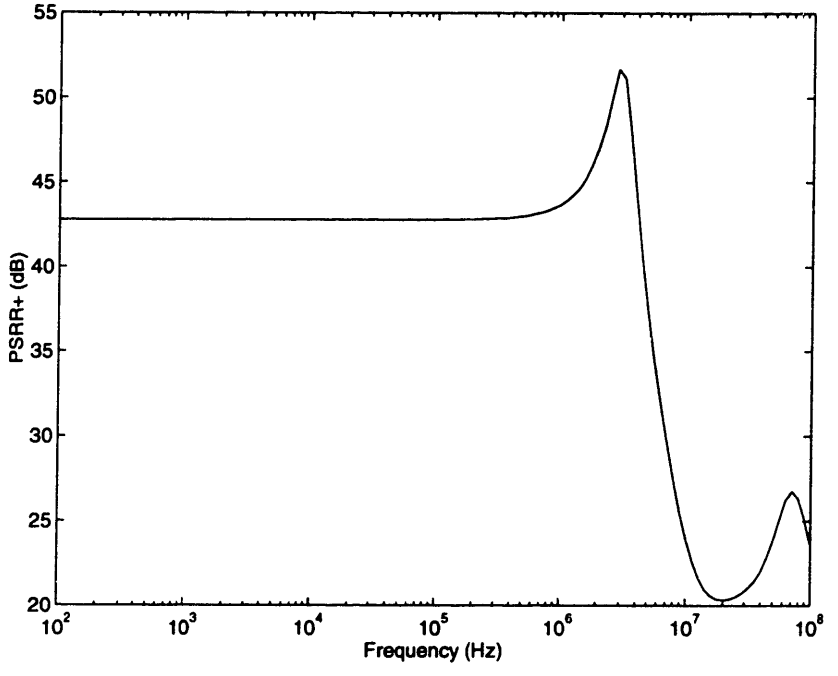

Figure 5-4: High Vt opamp PSRR+(V_{dd}=0.9V).

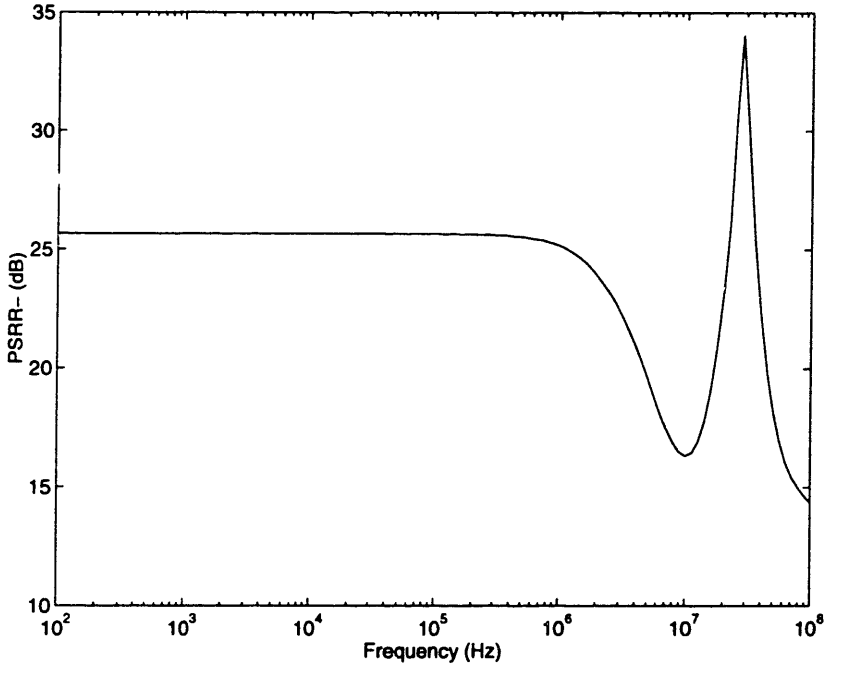

Figure 5-5: High Vt opamp PSRR-(V_{dd}=0.9V).

	Units	V_{dd}=0.9V	V_{dd}=1.25V
DC gain	-	5K	5.3K
Unity gain frequency	MHz	26	27
Phase margin	degrees	55	58
Output swing	mV	1430	2120
0.1% Settling time (linear)	ns	55	44
0.1% Settling time (step size)	ns(V)	72(0.66)	61(0.66)
Slew rate	V/μs	40	40
Opamp power	μW	270	420
Total power	μW	457	756
Input referred noise	nV/$\sqrt{Hz}$	11.6	11.5
Offset voltage	mV	322	100
CMRR	dB	50.3	50.4
PSRR+	dB	60.8	65.7
PSRR-	dB	48.4	49.1

Table 5.2: Summary of the low Vt opamp simulation performance.

performance of the high Vt opamp would allow its use in a 10 bit data converter with a maximum clock frequency of 6.5MHz.

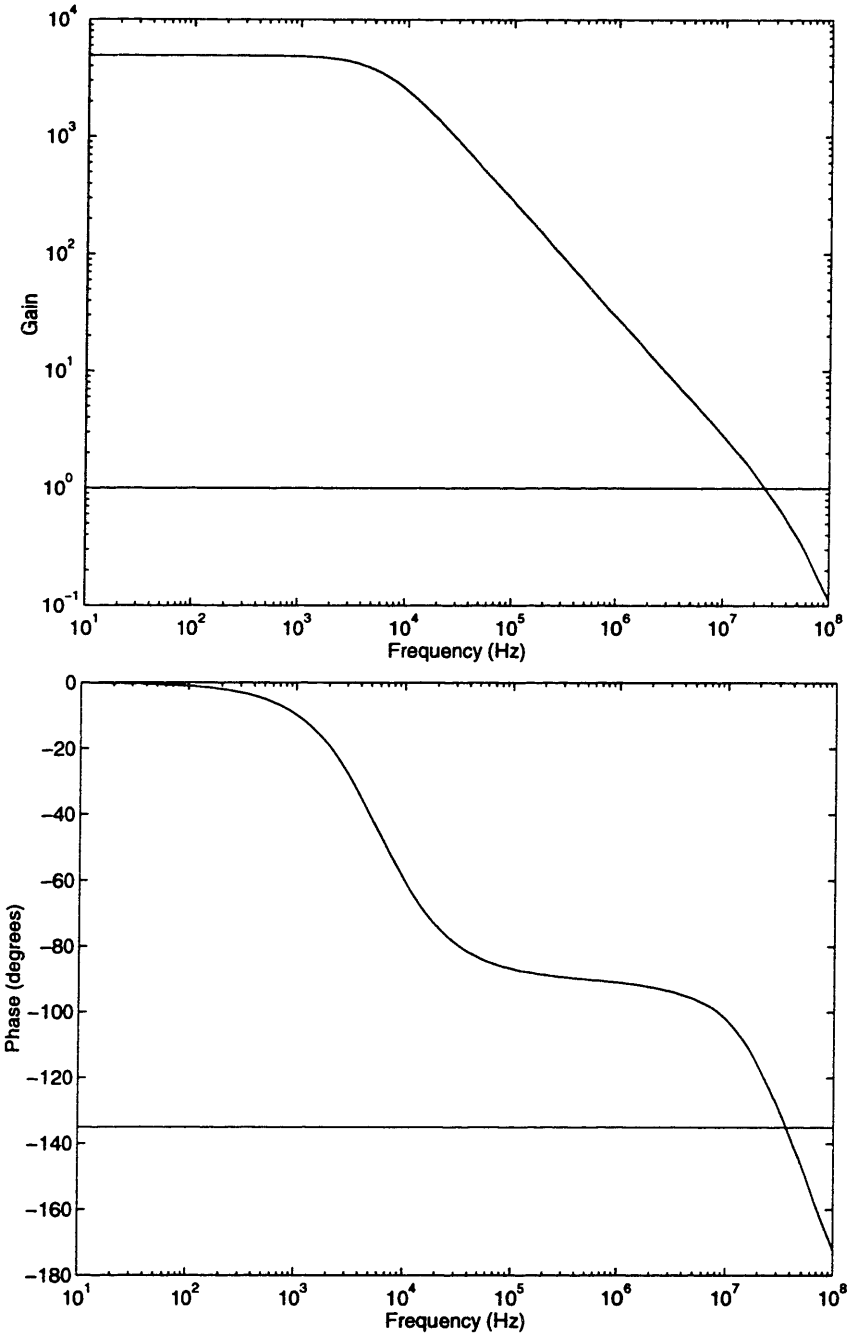

Figure 5-6: Low Vt opamp frequency domain magnitude and phase response(V_{dd}=0.9V).

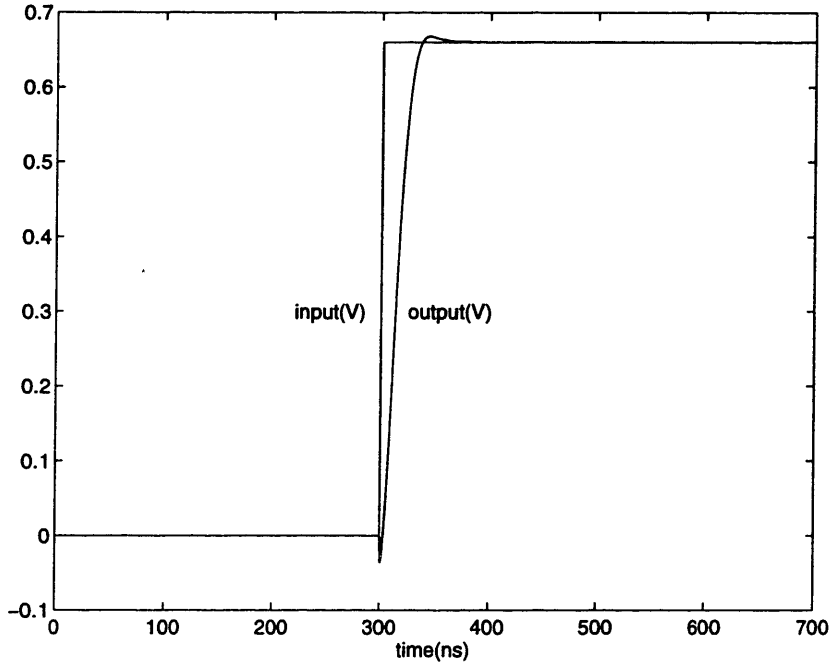

Figure 5-7: Low Vt opamp full scale output step response(V_{dd}=0.9V).

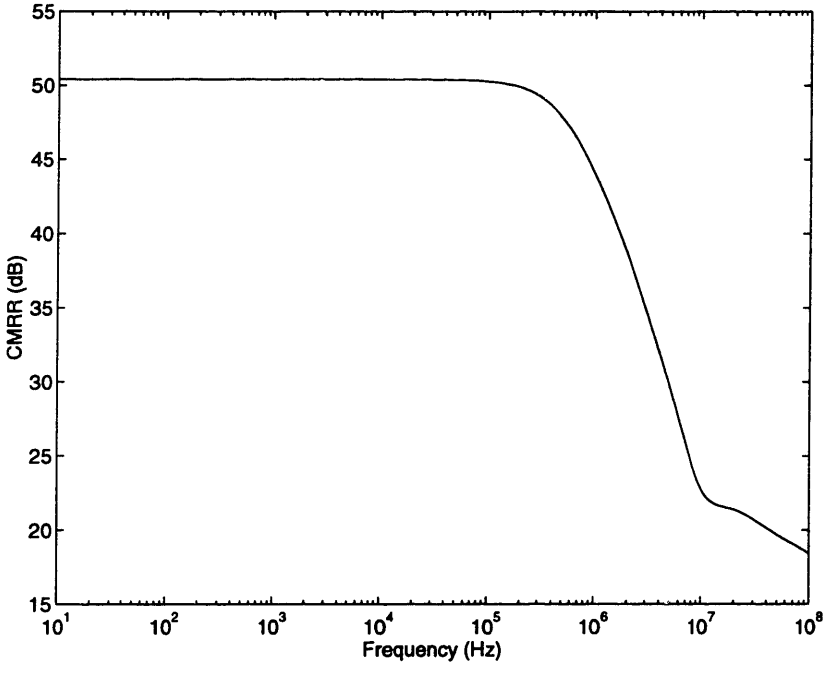

Figure 5-8: Low Vt opamp CMRR(V_{dd}=0.9V).

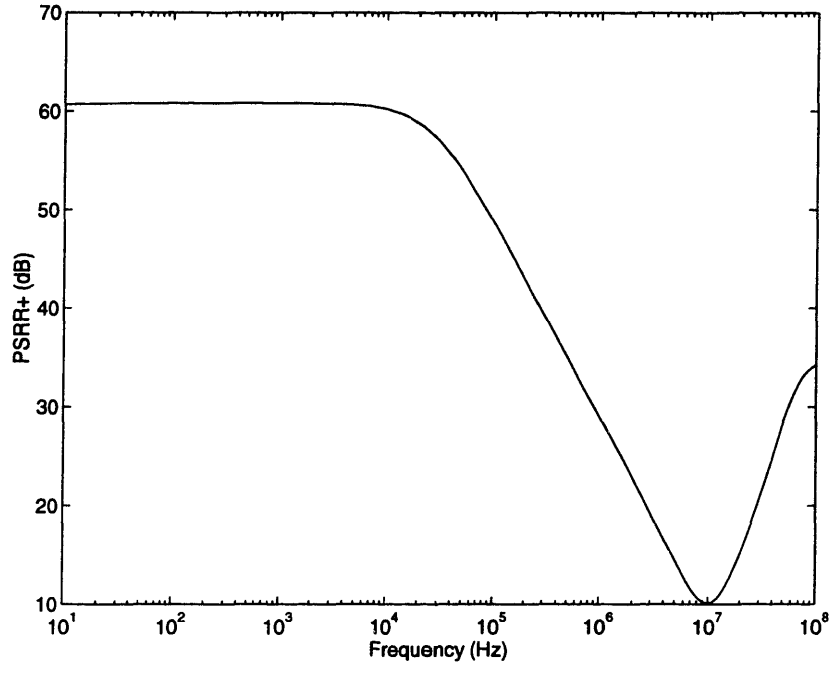

Figure 5-9: Low Vt opamp PSRR+(V_{dd}=0.9V).

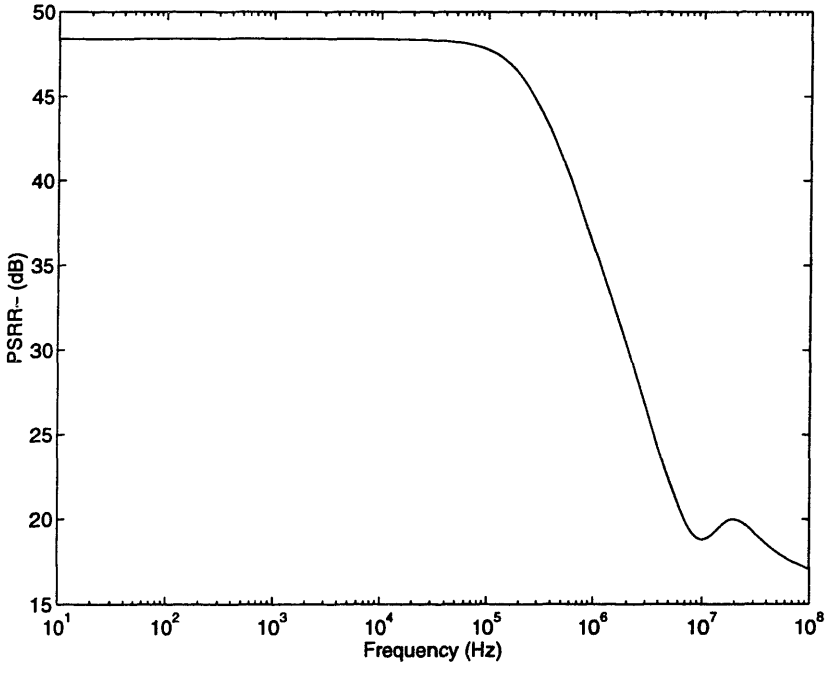

Figure 5-10: Low Vt opamp PSRR-(V_{dd}=0.9V).

Chapter 6

Discussions and Conclusion

6.1 Discussions

Low threshold MOS transistors are very attractive for low voltage CMOS analog circuit design. They allow the construction of high performance and high speed circuits. The performance of the low Vt opamp is far superior to the high Vt opamp. This is in spite of the fact that the low Vt opamp uses transistors with longer channel lengths (around 2μm as opposed to 0.8μm for the high Vt opamp).

The high Vt opamp is slower than the low Vt opamp for a variety of reasons. The most prominent is the low slew rate. Another reason is the large input parasitic capacitance at the input of the opamp which degrades the feedback factor and results in slower settling. The large parasitic capacitance is due to the large input device that were used. To remain in the subthreshold region and to, at the same time, increase the current and the transconductance of the transistors, it is necessary to increase the transistor dimensions, which results in a larger capacitance.

The high Vt opamp has a lower power consumption, which is in part responsible for the slower performance. Increasing the power consumption to improve speed was not found to be effective. Increasing power consumption by scaling up the opamp design also required the scaling up of the compensation capacitor to ensure stability. The improvement in the

slew rate and the linear settling time were not very significant.

The slew rate of the high Vt opamp can be improved without stability problems by scaling up the first stage of the opamp, and degenerating the input transistors. This would increase the current in the first stage but maintain the transconductance of the stage constant. The compensation capacitor, therefore, would not have to be change. The disadvantage is that the voltage gain of the opamp would be reduced because the output resistance of the first stage load devices, which is the dominant resistance, would reduce due to the larger current.

The swing of the low Vt opamp is significantly better due to the simple output stage design. The high Vt opamp could not have used the same output stage without sacrificing the gain, and a cascoded output stage was necessary. Further, the gain could not have been incorporated into the first stage, because PMOS cascode circuits could not be practically built.

The offset cancelation circuit that was used in the low Vt opamp resulted in a significantly lower offset voltage, and a better low frequency CMRR and PSRR. There is no reason that offset cancelation could not be performed for the high Vt opamp, but it is not as badly needed. The threshold voltage mismatch of the low Vt PMOS transistors can be as high as $\pm$35mV, which is significantly higher than that of the high Vt PMOS transistors, made it necessary to implement the offset cancelation.

The use of low threshold transistors provides the designer with great deal of freedom. The circuit can be easily tailored to provide for the desired performance. High Vt transistors on the contrary severely confine the designer, resulting in longer design time and poorer circuit performance.

6.2 Conclusion

This thesis presented the design of two very low voltage switched capacitor operational amplifiers. The design of the first opamp utilized only high threshold voltage (Vt) MOSFETs, while the second opamp made use of low Vt MOSFETs. The opamps function properly for

supply voltages from 0.9V to 1.25V. The worst case settling time for the first opamp was 182ns, and was 72ns for the second opamp. The benefits of using low threshold MOSFETs for low voltage opamp design were demonstrated. A tail current source was designed for each opamp, and was shown to provide a constant current even when the voltage across it was a few millivolts. The design of the bias circuit, common mode feedback circuit and switches was discussed for each opamp.

Bibliography

[1] Semiconductor Industry Association. *The National Technology Roadmap for Semiconductors.* 1994.

[2] I. Sinclair. *Electronic Power Supply Handbook.* PC Publishing, 1995.

[3] A. Chandrakasan, S. Sheng, and R. W. Brodersen. Low power CMOS digital design. *IEEE Journal of Solid-State Circuits*, pages 473–484, April 1992.

[4] J. Rabaey and M. Pedram. *Low Power Design Methodologies.* Kluwer Academic Publishers, 1996.

[5] K. Fernald, J. Paulos, B. Stackhouse, and R. Heaton. A Self-Tuning Digital Telemetry IC for Use in a Microprocessor-Based Implantable Instrument . *IEEE Journal of Solid-State Circuits*, pages 1826–1832, December 1992.

[6] P. Wouters, M. De Cooman, and R. Puers. A Multi-Purpose CMOS Sensor Interface for Low-Power Applications . *IEEE Journal of Solid-State Circuits*, pages 952–956, August 1992.

[7] Better Batteries for Low-Power Job . *Electronic Design*, page 15, July 23 1992.

[8] K. Matsui, T. Matsuura, S. Fukasawa, Y. Izawa, T. Toba, N. Miyake, and K. Nagasawa. CMOS Video Filters Using Switched Capacitor 14-MHz Circuits . *IEEE Journal of Solid-State Circuits*, pages 952–956, August 1992.

[9] M. Degrauwe, E. Vittoz, and I. Verbauwhede. Micropower CMOS-Instrumentation Amplifier . *IEEE Journal of Solid-State Circuits*, pages 805–807, June 1985.

[10] B. Del Signore, N. Sooch D. Kerth, and E. Swanson. A Monolithic 20-b Delta-Sigma A/D Converter . *IEEE Journal of Solid-State Circuits*, pages 1311–1317, June 1990.

[11] D. Senderowicz, S. Dreyer, J. Huggins, C. Rahim, and C. Laber. A Family of Differential NMOS Analog Circuits for a PCM Codec Filter Chip . *IEEE Journal of Solid-State Circuits*, pages 1014–1023, June 1982.

[12] P.R. Gray and R.G. Meyer. *Analysis and Design of Analog Integrated Circuits.* John Wiley & Sons, 1993.

[13] C. Jiang, D. Pramanik, and C. Hu. Hot Carrier Reliability Considerations for Low Vdd CMOS Technology . *1995 4th International Conference on Solid State and Inte grated Circuit Technology*, pages 322–324, 1995.

[14] P. Gray and R. Meyer. MOS Operational Amplifier Design-A Tutorial Overview. *IEEE Journal of Solid-State Circuits*, pages 969–982, December 1984.

[15] J. Huijsing, R. Hogervorst, and K. Langen. Low-Power Low-Voltage VLSI Operational Amplifier Cells. *IEEE Transactions on Circuits and Systems-I*, pages 841–852, November 1995.

[16] G. Nicollini, F. Moretti, and M. Conti. High-frequency fully differential filter using operational amplifiers without common-mode feedback . *IEEE Journal of Solid-State Circuits*, pages 969–982, December 1984.

[17] R. Gregorian and G.C. Temes. *Analog MOS Integrated Circuits for Signal Processing.* John Wiley & Sons, 1986.

[18] K. Bult and G. Geelen. A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain. *IEEE Journal of Solid-State Circuits*, pages 1379–1384, December 1990.

[19] P. Allen, B. Blalock, and G. Rincon. A 1 V CMOS op amp using bulk-driven MOSFETs. *1995 IEEE International Solid-State Circuits Conference*, pages 192–193, 1995.

[20] J. Fonderie, M. Maris, E. Schnitger, and J. Huijsing. 1-V Operation Amplifier with Rail-to-Rail Input and Output Ranges. *IEEE Journal of Solid-State Circuits*, pages 1551–1559, December 1989.

[21] Hae-Seung Lee. Private communication.

[22] Kush Gulati. Private communication.

[23] T. Cho and P. Gray. A 10b, 20 Msample/s, 35mW Piplined A/D Converter. *IEEE Journal of Solid-State Circuits*, pages 166–172, March 1995.

[24] Y. Matsuya and J. Yamada. 1V Power Supply, Low-Power Consumption A/D Conversion Technique with Swing-Suppression Noise Shaping. *IEEE Journal of Solid-State Circuits*, pages 1524–1530, December 1994.

[25] Paul Yu. Private communication.

[26] B. Kamath, R. Meyer, and P. Gray. Relationship Between Frequency Response and Settling Time of Operational Amplifiers. *IEEE Journal of Solid-State Circuits*, pages 347–352, December 1974.

[27] N. Weste and K. Eshraghian. *Principles of CMOS VLSI Design.* Addison Wesley, 1993.

THESIS PROCESSING SLIP

FIXED FIELD: ill _____ name _____

index _____ biblio _____

▶ COPIES (Archives) Aero Dewey (Eng) Hum

Lindgren Music Rotch Science

TITLE VARIES ▶☐ _____

NAME VARIES: ▶☑ in degree book, name is listed as "Ayman M. Umar Shabra"

IMPRINT (COPYRIGHT) _____

▶ COLLATION: 69 l

▶ ADD. DEGREE: _____ ▶ DEPT.: _____

SUPERVISORS: _____

NOTES:

cat'r: date:

page: F42

▶ DEPT: E.E.

▶ YEAR: 1997 ▶ DEGREE: M.S.

▶ NAME: SHABRA, Ayman U.