The Electromigration Drift Velocity and the Reliability of Dual-Damascene Copper Interconnect Trees

by

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ABSTRACT

Cu has replaced Al as the interconnect metal of choice for high performance Si-based integrated circuits. Its electromigration behavior must be quantified and an experimental basis for a circuit-level reliability assessment is needed.

Experiments on straight two-terminal via-to-via Cu dual-damascene segments with different line lengths, both with via-above and via-below geometries, have been carried out. By contrasting the failure characteristics of via-above and via-below structures, the Cu/Si$_3$N$_4$ interface has been identified as the site for void nucleation and the most dominant diffusion path. Consequently, an asymmetry in lifetime exists between via-above and via-below interconnect lines. It has also been found that at short line lengths, true Blech immortality occurs only for very short lines, at best, due to the ease of void nucleation. Immortality due to void growth saturation is also limited, because, in the absence of the conducting refractory-metal current-shunting overlayers characteristic of Al technology, very small voids at vias can cause failures. We find that at long lengths a sub-population of Cu lines is immortal. We propose that this is a result of non-blocking liners at the base of the vias associated with the high stresses developed at the ends of the lines.

In order to quantify the fundamental Cu electromigration kinetics which precedes all failure modes, electromigration drift velocity measurements were carried out using fully processed interconnect structures. It was observed that in a significant fraction of the test population, the resistance of the lines increased steadily over time prior to failure. It is postulated that this gradual resistance increase results from void growth and that the rate of resistance increase correlates with the drift velocity for electromigration. Through drift measurements, we determined the activation energy for electromigration is 0.80±0.06eV. The values of the drift velocities determined in vias-below lines were similar to those measured in vias-above lines. This fact supports the proposal that the
asymmetry in reliability between the two different configurations is associated with the void sizes required for failure.

Reliability characterization of dotted-I and T-shaped Cu interconnect trees was also carried out. Similar to Al, we found that individual interconnect segments cannot serve as fundamental reliability units (FRU). Unlike Al, we found that Cu interconnect trees are not the FRUs either, due to possible non-blocking vias. Furthermore, due to low stress required for void nucleation in Cu- compared to Al-based interconnects, Cu reliability behavior points to the need to develop a via-based reliability assessment methodology. An atomic reservoir effect for Cu was not indicated by the investigation T-shaped trees. This leads to conservative void growth model for circuit-level reliability assessment methodology.

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Chapter 1 INTRODUCTION

In 1960, the introduction of the first planarized and transistorized integrated circuit (IC) by Robert Noyce and Gordon Moore of Fairchild Semiconductor Corp. marked the beginning of the modern microelectronic era. Progress ensuing this technological revolution enabled the births of modern marvels like the microprocessor, the integrated personal computer, and the Internet. Moore’s law [Moo 65] brilliantly captured the rapid evolution of semiconductor electronics. In order to maintain such progress, the monumental advancements of the semiconductor industry have revolved around these common themes: miniaturizing components in the IC’s so that more could be packed onto a single chip, and improving the performance and reliability of the IC components.

As a result of these achievements, inside today’s microprocessor one can find tens of millions of transistors packed in less than one square inch area making up complex logic circuits. The topological challenge of wiring all the transistors together is enormous. Usually, 6 to 8 layers of metal wire connections are required for a typical processor [ITRS 01] (see Figure 1.1). In addition, as the feature sizes become more compact, the resistance-capacitance delay associated with the signal propagation through the metal wire connections also becomes more significant (see Figure 1.2). To minimize this delay, Cu metallization and low-K inter-level dielectric materials must be integrated into Si technology, due to their low resistivity and low capacitance, respectively. Lastly, the total length of metal wire connections and the current density that the wires carry increases with each new generation of semiconductor technology. This trend calls for continuously increasing reliability requirements for these metallic wires (see Figure 1.3).
Over the past four decades, many scientists and engineers have focused on overcoming these issues associated with the metal wire connections. The metallic wires in discussion have a special name – interconnects. This dissertation addresses methods for quantitatively assessing the reliability of dual-damascene Cu interconnects.

Fig 1.1. Cross-sectional view of a hierarchical design of metallization levels. [ITRS 01]
Fig 1.2. Delays related to metal wiring for Al and Cu as metals of choice versus feature size. One can see that the overall delay for Cu technology is lower than that for Al technology. [ITRS 01]

Fig 1.3. FITs (failures in $10^3$/m) of metallic wiring versus total metallic wiring length/cm² chip Area. Also, the projected time to achieve these reliability requirements is indicated in the figure above. [ITRS 01]
1.1 Electromigration

As difficult as fabricating these multi-level interconnects is, characterizing the reliability of interconnects is no trivial task. Under service conditions in a typical IC chip, the current density is about $4 \times 10^5 \text{ Amp/cm}^2$, and the temperature is about $100^\circ\text{C}$. Interconnects are subjected to tremendous mechanical stresses that can lead to failure. The main failure mechanism is electromigration [Ble 67], which is the diffusion of metal atoms due to momentum transfer from conducting electrons in the presence of an electric field.

Similar to other atomic diffussional processes, electromigration is thermally activated, a measure of which is the activation energy, $E_a$. At finite temperatures, a finite amount of vacancies exist in the metal. For simplicity, we consider that when atoms diffuse in a crystal, they first achieve an activated state in between the original lattice site and a neighboring vacancy by acquiring sufficient activation energy. If the diffusion is random, the probability that the activated atom will fall into the vacancy or the original lattice site is the same. However, if the atoms experience an external force, for example, a momentum transfer from conducting electrons, the diffusion process is biased [Bal 01, Hun 75]. Usually, the activation energy is higher for metals with higher melting temperatures because more energy is required to break inter-atomic bonds to achieve the activated state. Consequently, metals with higher melting temperatures are more resistant to electromigration.

The electromigration phenomenon was first discovered in 1861 [Ger 1861]. However, this topic remained of limited interest until the 1960's, when failures of interconnects in IC's due to electromigration were reported. The basic physics behind
electromigration can be understood in the following semi-classical description, which was formulized by H.B. Huntington [Hun 75] and M.A. Korhonen [Kor 93].

1.2 Huntington-Korhonen Model for 1-D Electromigration

1.2.1 The Electron Wind Force

The description for the electron wind force can be derived from ballistic transport theory [Fik 59]. The number of scattering events per unit time between conducting electrons and the activated metal ion, \( n_s \), is given by

\[
    n_s = n_e v_e \sigma_e ,
\]

(1.1)

where \( n_e \) is the electron density, \( v_e \) is the electron velocity, and \( \sigma_e \) is the scattering cross section. The average momentum transfer per scattering event, \( \Delta p \), is given by

\[
    \Delta p = \frac{q E l_e}{v_e} ,
\]

(1.2)

where \( q \) is the fundamental charge, \( E \) is the applied electric field, and \( l_e \) is the mean free path of an electron. The electron wind force is the product of these two quantities

\[
    F_{e-wind} = (\# of events) \cdot \left( \frac{\Delta p}{\text{event}} \right) = -n_e \sigma_e q E l_e .
\]

(1.3)

Conventionally, for convenience, we define a fictitious quantity \( z^* \) – the effective charge for any diffusing species, such that

\[
    F_{e-wind} = q z^* E .
\]

(1.4)

Therefore, \( z^* \) equals to the product of \( -n_e \sigma_e l_e \). In most literature discussions, however, \( z^* \) is equivalent to \( | n_e \sigma_e l_e | \), a positive number.
From this description of the electron wind force, we arrive at an expression for the atomic flux due to electromigration. Einstein's relationship yields the drift velocity for electromigration

$$v = \frac{DF_{e \text{-wind}}}{kT},$$  \hspace{1cm} (1.5)

where $D$ is the diffusivity, $k$ is the Boltzmann's constant, and $T$ is the temperature. Therefore, the atomic flux due to electromigration due to the electron wind force is

$$J_{EM} = v \cdot c_a = \frac{Dc_a}{kT}(\rho_j)(q^*),$$  \hspace{1cm} (1.6)

where $c_a$ is the atomic concentration, and the product of the resistivity and current density, $\rho_j$, represents the electric field, $E$.

### 1.2.2 The Back-Stress

When rigid dielectric materials surround a metal line, such is the case for a segment of interconnect on an IC chip, the motion of atoms leads to mechanical stresses. If there is a flux divergence at the ends of a line, near the cathode end of the line, where atoms are depleted, a tensile stress develops. On the other hand, near the anode end of the line, where atoms accumulate, a compressive stress develops. This gradient in stress results in a gradient in chemical potential and corresponding force often referred to as the back stress. If a condition is reached in which the tensile stress and the compressive stress balance, the difference between the stresses in a straight segment of interconnect is described by [Ble 76]

$$z^* q \rho_j = \frac{\Omega \Delta \sigma}{L},$$  \hspace{1cm} (1.7)
where \( \Delta \sigma \) is the stress difference between the cathode and the anode, \( L \) is the line length, and \( \Omega \) is the activation volume for electromigration. The value for the activation volume is usually approximated as the atomic volume for the electromigrating metal.

If no damage occurs inside the line, i.e., if the stress difference between the cathode and anode is less than that required for void nucleation or extrusions, the stress profile will evolve toward a steady state (see Figure 1.4). At this point, the net atomic flux becomes zero, equation 1.7 applies, and the interconnect segment is considered ‘immortal’. We can rewrite equation 1.7 as an immortality condition [Ble 76]

\[
(jL)_{\text{critical}} = \frac{2\Delta \sigma_{\text{nucleation}} \Omega}{z*q\rho},
\]

where \( \Delta \sigma_{\text{nucleation}} \) denotes the stress difference required for void nucleation.

In order to predict the transient evolution, Korhonen et al. formulated a description for the total atomic flux due to both the electron wind force and back stress force [Ble 76, Kor 93], given by

\[
J = \frac{Dc_a}{kT} \left( qz \cdot \vec{E} + \nabla \mu \right),
\]

where \( \nabla \mu \) corresponds to the chemical potential gradient due to the stress gradient developed in the line. For 1-D considerations, this can be re-written as

\[
J_a = \frac{Dc_a}{kT} \rho | j | z \cdot q - \frac{Dc_a}{kT} B \frac{\partial \mu}{\partial x},
\]

where \( B \) is the effective bulk modulus, which is a function of the mechanical properties of the interconnect material as well as the surrounding dielectric material. In most literature, this is the starting point for a discussion of electromigration. This model served as a basis for the electromigration simulation tool MIT/EmSim, which was
developed for Al-based interconnects by Park et al. and Andleigh et al. [Par 97, Par 99, And 99]. One of the most useful simulations that MIT/EmSim is capable of is to predict the stress evolution in a segment of interconnect over time. This is done in a series of iterative steps, which are outlined in the PhD thesis of S.P. Hau-Riege [Hau 00]. Figure 1.4 depicts the output.

Fig. 1.4. Stress evolution in an interconnect segment based on the Korhonen model. The left side is the cathode end, where a tensile stress develops over time. The right side is the anode end, where a compressive stress develops over time.
1.3 Interconnect Trees

In real circuits, jointed segments of interconnect in the same level of metallization do not have blocking boundaries between them. Therefore, the flux of metal atoms in each segment is dependent upon the fluxes in its neighboring limbs. The reliability behavior for Al-based interconnect trees (interconnect segments jointed on the same level of metallization and terminating at W-filled, electromigration-blocking vias) has been carefully observed by Hau-Riege et al. [Hau 98, Hau 00, Hau 00d, Hau 01b]. As a result of these experiments, S.P. Hau-Riege has argued that an interconnect tree is the fundamental reliability unit for Al-based interconnect trees. Methodologies for evaluating the stresses inside any given tree and a tree-based circuit-level reliability assessment tool have been developed as well. However, for Cu interconnect trees, we lack such knowledge.

1.4 Accelerated Lifetime Testing and Reliability Statistics

Regardless of the material used in interconnects, in order to understand the methods and terminology used to describe the reliability of interconnects, one must review the basics of reliability statistics.

1.4.1 Accelerated Life Testing

The bathtub curve (see Figure 1.5) describes the failure rate for most components or groups of components working together. The bathtub curve has three regions: infant mortality, useful life, and wear out regions. Electromigration is considered a wear out mechanism. Therefore, in order to quickly gain useful information about this failure
mechanism, one must decrease the testing time from the actual lifetime in service. This reduction in test time is accomplished through accelerated life testing. Accelerated tests are conducted under conditions beyond normal operating ranges. In particular, the accelerated tests for electromigration involve elevated temperatures and current densities.

**The Bathtub Curve**

Hypothetical Failure Rate versus Time

- **Unit Life**
  - Infant Mortality
  - Decreasing Failure Rate
  - Normal Life (Useful Life)
    - Low "Constant" Failure Rate
  - End of Life Wear-Out
    - Increasing Failure Rate

**Time**

**Fig. 1.5.** The bathtub curve describing failure rates for most components.
For electromigration accelerated life tests, the in-service lifetime is extrapolated from the accelerated lifetime using the following formula, known as Black’s equation [Bla 67, Bla 69, Llo 91, Llo 91b, Llo 91c, Llo 92]

\[ t_{50} = A j^{-n} \exp\left(\frac{E_a}{kT}\right), \]  

(1.11)

where \( t_{50} \) is the medium time to failure (MTF), \( A \) is a constant, \( E_a \) is the activation energy for electromigration, and \( n \) is a constant of value 1, or 2, or intermediate values for Cu technology. The exact value of \( n \) depends on the particular failure mechanisms. Values of \( E_a \) have been widely reported in the literature: for Al interconnects, \( E_{a,G.B.} = 0.55 \) eV [Ho 74, Ble 76b], \( E_{a,Lamca} = 0.6-0.7 \) eV [Llo 95]; for Cu interconnects, \( E_{a,G.B.} = 1.0-1.2 \) eV [Sim 60, Llo 95], \( E_{a,interface} = 0.7-0.9 \) eV [Par 91, Hu 99].

1.4.2 Reliability Statistics

In discussions about both service lifetimes and accelerated lifetimes, a lifetime distribution is used to describe how failures occur in time. Experimentally determined lifetime distributions are fit to probability density functions (PDF). Common PDFs include the normal (or Gaussian), Weibull, and lognormal distributions. The normal distribution is used for modeling failures that occur randomly at a steady state with significant wear-out or degradation. This model is most suitable for the useful-life period of the bathtub curve. The Weibull distribution corresponds to a ‘weakest-link’ mechanism, in which any potential failure location causes failure of the device. The lognormal distribution is often used to describe wear-out mechanisms, which electromigration is categorized as.

The mathematical form of the lognormal distribution is
\[ f(t) = \frac{1}{\sigma t \sqrt{2\pi}} \exp\left[-\frac{1}{2\sigma^2}(\ln(t) - \mu)^2\right], \quad (1.12) \]

where \( t_{50} = \exp(\mu) \) is the MTF, and \( \sigma \), the shape parameter, corresponds to the standard deviation of the natural log of the failure times (see Figure 1.6). \( \ln(f(t)) \) is normally distributed with mean of \( \mu \) and variance \( \sigma^2 \).

In our experiments, the test population consists of about 20 samples per experiment. In order to obtain \( \mu \) and \( \sigma \) for each test, we perform the following calculations. Let \( F \) be the cumulative probability of failure

\[ F(t) = \int_0^t f(t')dt' = \Phi\left[ \frac{1}{\sigma} \left( \ln \frac{t}{t_{50}} \right) \right], \quad (1.13) \]

where \( t \) is the lifetime of a given sample, and \( \Phi \) is the standard normal cumulative distribution function

\[ \Phi(z) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{z} \exp\left(-\frac{u^2}{2}\right) du. \quad (1.14) \]

The natural log of the given lifetime is generated by

\[ \ln t = \ln t_{50} + \sigma \Phi^{-1}(F). \quad (1.15) \]

Lastly, linear regression fitting of \( \ln t_{50} \) versus \( \Phi^{-1}(F) \) yields \( \ln t_{50} \) and \( \sigma \). When describing multi-modal lifetime distributions, values for \( t_{50} \) and \( \sigma \) are needed for all modes. This is the situation encountered in discussions of Cu interconnect length effects (Chapter 2).
Fig. 1.6. Example lognormal distribution plots. (a) variations with respect to changes in $\mu$; (b) variations with respect to changes in $\sigma$. 
1.5 Al Technology versus Cu Technology: Architectures

Cu replaced Al as the metal of choice for interconnects because of its low value of resistivity and higher resistance to electromigration. However, due to the difference in the chemical properties of Cu, the fabrication technology (commonly referred as the back-end processes) for Cu is drastically different from that of Al [Plu 00]. Figure 1.7 illustrates a comparison of the Al and Cu interconnect architectures.

In Al technology, thick, highly electromigration-resistant refractory metal layers, which are made of TiN, Al,Ti, or both, are usually used as anti-reflection coatings on the top of the lines, and similar layers have been included as under-layers, initially for use as seed layers for via-fill processes. Al chemically reacts with SiO₂ to form alumina, which blocks the diffusion of Al into the surrounding dielectrics. Therefore, no diffusion barriers are needed on the sides of Al interconnects. W-filled vias are used to connect layers of metallization and also serve as fully blocking boundaries for electromigration. One benefit of such an architecture is that electron flow can be shunted around small-volume voids inside Al interconnects through the refractory metal layers.

Since Cu is not very chemically reactive compared to Al, encapsulating diffusion barriers are needed for all sides of the line. Usually, in practice, very thin refractory metal layers consisting of Ta or Ta/TaN are fabricated for the sides and bottom of the Cu line. On the top, the Cu lines are capped with a dielectric diffusion barrier, which is usually made of Si₃N₄. Cu-filled vias are used to connect layers of metallization in the dual-damascene process. Because of the non-conducting capping layer and thin diffusion barrier at the bottom of the vias, the electromigration behavior of Cu interconnects is
much different from that of Al interconnects. The direct consequences of these differences are presented in more detail in Chapter 2.

**Fig. 1.7.** Comparisons of Al and Cu fabrication technologies. The structure on the left corresponds to Al interconnects, with W-filled vias and conducting shunt layers on the top and bottom of the interconnect line. The structure on the right corresponds to dual-damascene Cu interconnects, with Cu vias, thin refractory liners at the side and bottom of the line, and dielectric capping layer on the top of the line.
1.6 Goal of the Thesis

The goal of this thesis is to provide a quantitative characterization of electromigration through measurements of the drift velocity in dual-damascene Cu interconnects, as well as to develop an experimental understanding of the reliability of both via-to-via and multi-limb Cu interconnects. Such investigations are critical to the understanding of the circuit-level reliability of Cu interconnects, and provide the necessary background for development of new reliability assessment methodologies for Cu interconnects.

1.7 Thesis Organization

Arising from the differences in the architecture between Cu and Al technologies, lifetime trends and reliability behaviors are different for these two types of interconnects. The essential distinction is that the dominant diffusion path in Cu interconnects is the Cu/Si$_3$N$_4$ interface [Hau 01, Hau 02, Gan 01, Gan 02, Hu 99, Arn 00, McC 00, Pro 00], compared to grain boundaries in Al interconnects [Hau 00b, Hau 00c, Ho 88, Llo 95]. The direct impact of this different diffusion path on the reliability of Cu interconnect in straight-line segments is discussed in Chapter 2. Also, due to the architectural difference between Cu and Al technology, new experimental methods for physically characterizing electromigration in Cu interconnects are needed. Chapter 3 presents methods that characterize Cu electromigration by measuring the drift velocity in fully processed dual-damascene structures. As one would expect, the behavior of Cu multi-limb trees is different from that of Al as well. Chapter 4 describes experimental studies using multi-limb, dual-damascene Cu tree structures. Lastly, the results of these experimental studies
using Cu interconnects point to the need to develop a new set of methodologies for evaluating circuit-level reliability for Cu interconnects. Chapter 5 outlines further background knowledge and future work necessary to complete such a task.
Chapter 2  Cu ELECTROMIGRATION: THE Cu/Si$_3$N$_4$ INTERFACE

In order to improve the reliability of interconnects, one must first identify the dominant electromigration diffusion path in the material system. In Al interconnects, this path is the grain boundaries [Hau 00b, Hau 00c, Ho 88, Llo 95, Kin 80]. Consequently, a number of ways to restrain electromigration in Al interconnects have been developed. For example, the reliability may be improved by developing a bamboo-like grain structure [Cho 89, Iye 84, Hau 00c], where the grain boundaries are perpendicular to the electron flow. Also alloying Al with Cu [Gan 75, Ble 77, Hu 93] can suppress grain boundary Al self-diffusion. Models incorporating these effects have been included in MIT/EmSim for Al interconnects [And 99, And 01].

In Cu interconnects, the dominant diffusion path is along the Cu/Si$_3$N$_4$ interface [Hau 01, Hau 02, Gan 01, Gan 02, Hu 99, Arn 00, McC 00, Pro 00, Hu 01, Oga 01]. This leads to important differences in the phenomenology of electromigration-induced failure in Cu compared to Al, as will be described in this chapter.

2.1 Experiments

For this study, dual-damascene Cu interconnect structures were fabricated by International Sematech Inc. in the USA and by the Institute of Microelectronics (IME) in Singapore. These structures were produced using 0.18μm minimum feature size fabrication technology on 200-mm diameter wafers. Straight-line test structures terminating at vias were used for this study. Two types of straight-line structures (M1
and M2) were fabricated. In M1 type test structures, the EM test structure lies in the lower level of metallization, and the vias are located above the test line. Much wider (5-10 times wider) connector lines, which lie in the upper level of metallization, connect the vias to the bondpads. Conversely, in M2 type structures, the test lines are in the upper level while the vias are located below the test structures. The connector lines are in the lower metallization level in the M2 type structures. Figure 2.1 shows comparisons of the M1 and M2 test structures.

A conventional process flow for fabricating Cu interconnects is the following: first, a trench is patterned in a dielectric layer, SiO₂, in this case. Second, Ta diffusion barriers and Cu seed layers are sputter deposited into the trenches. Third, the trenches are filled with Cu by electroplating. Forth, excess Ta and Cu between trenches is removed using chemical mechanical polishing. Lastly, layers of SiN and SiO₂ are deposited using plasma-enhanced chemical vapor deposition. For dual-levels of metallization, this process is repeated, except that the trenches for the inter-level vias are incorporated. The bondpads consist of large Cu pads in both M1 and M2 levels. The bondpads are covered with a thin layer of Ta, which acts as a diffusion barrier. The Ta layer is covered with a layer of Al to prevent oxidation. As a result, all the test structures are fully passivated. For the Cu interconnect lines, Ta metal liners bound the sides and bottom, while a Si₃N₄ inter-level dielectric layer caps the top. The final specifications for Sematech and IME structures are listed in Table 2.1.
Fig. 2.1. Schematic top and side views of the M1 and M2-type interconnect structures.

Table 2.1. Process specifications of IME and Sematech fabricated interconnects.

<table>
<thead>
<tr>
<th>Specs</th>
<th>Sematech</th>
<th>IME</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ta Liner – Bottom (Å)</td>
<td>200</td>
<td>250</td>
</tr>
<tr>
<td>Ta Liner – Side (Å)</td>
<td>100</td>
<td>125</td>
</tr>
<tr>
<td>SiN Capping Layer (Å)</td>
<td>1000</td>
<td>14000 [alternating SiN/SiO₂ stack]</td>
</tr>
<tr>
<td>M1 Layer Height (µm)</td>
<td>0.45</td>
<td>0.34</td>
</tr>
<tr>
<td>M2 Layer Height (µm)</td>
<td>0.45</td>
<td>0.24</td>
</tr>
<tr>
<td>Via Aspect Ratio: Width/Height (µm/µm)</td>
<td>0.25/0.45</td>
<td>0.25/0.75</td>
</tr>
</tbody>
</table>
Electromigration stress experiments were conducted at both the wafer- and package-level. The wafer-level tests were performed at MIT. In these tests, each die was tested individually, and probe stations were used as electrical connections to the bondpads (see Figure 2.2 for setup illustration). Our collaborators at Sandia National Labs, AMD Corp., IME, and Intel Corp performed the package-level tests. During package-level testing, 16 to 18 dice were packaged into ceramic packages to be tested simultaneously. Gold wires were used to connect the bondpads to the tester. We carried out the experiments under constant current and constant temperature for a range of currents and temperatures. The failure criterion was a 100% change of the initial resistance, with a tolerance of 1% change of the initial resistance.
2.2 Joule Heating Measurements

At accelerated electromigration testing conditions, electron-phonon scattering in interconnect lines may become significant enough to affect the controlled experimental conditions, through Joule heating. Since diffusivity is highly temperature dependent, Joule heating is not desired during electromigration tests. A common acceptable level is 2 to 4°C.
The temperature coefficient of resistivity, TCR, or $\alpha$, is defined by the following [Sch 94]:

\[ R(T) = R_0 (1 + \alpha \Delta T) , \quad (2.1) \]

where $R_0$ is the resistivity at a reference temperature. Equation (2.1) can be rewritten as

\[ \Delta T = \frac{R - R_0}{\alpha} , \quad (2.2) \]

to predict how much Joule heating, or $\Delta T$, is produced at given conditions. $\alpha$ and Joule heating measurements were completed at wafer-level using an M1 interconnect structure with $L=1000\mu$m and $W=0.3\mu$m fabricated by Sematech. In the first part of the experiment, a nominal current density ($j=1.1\times10^5\,A/cm^2$) is passed through the structure in order to collect the resistance values at temperatures from 25 to 350°C. Using equation (2.1), we obtain $\alpha=3.1\times10^{-3}\,K^{-1}$ (see Figure 2.3). In the second part, while the temperature was fixed at 350°C, the current density was ramped from $1.1\times10^5$ up to $1.0\times10^7\,A/cm^2$ in less than half-hour. The resistance values were recorded at current density increments. As shown in Figure 2.4, the results suggest that at the test temperature of 350°C, for current densities less than $4.0\times10^6\,A/cm^2$, Joule heating is not significant for the Cu interconnects used in this study.
Fig. 2.3. Resistance versus temperature for an M1-type Cu interconnect with $L=1000\mu m$ and $W=0.3\mu m$.

Fig. 2.4. Resistance measurements and predicted Joule heating ($\Delta T$) versus current density for a M1-type Cu interconnect with $L=1000\mu m$ and $W=0.3\mu m$. 

2.3 Stress Voiding and Pre-test Annealing

As the interconnect structures undergo numerous cycles of temperature variations during processing and testing, such as SiN layer deposition, the intrinsic stress inside the line may change. This thermally induced stress comes from mismatching of thermal expansion between the metal layer and Si substrate (see Figure 2.5). Non-zero intrinsic stresses at elevated temperatures can lead to stress-induced voiding.

During the fabrication of the interconnects, the electroplated Cu is assumed to have zero intrinsic stress. The SiN capping layer is deposited at $T=400^\circ\text{C}$, which is usually the first, and the highest temperature annealing step for the Cu lines during processing. This means that the stress in the Cu lines would follow Path1 in Figure 2.5(a). Cu has a higher coefficient of thermal expansion (CTE) than Si does, therefore, as the temperature increases, a compressive stress develops in the Cu. However, because SiN deposition is the first annealing step for Cu, this compressive thermal stress may be relieved through microstructural changes, such as grain growth, or through diffusive creep, or dislocation-mediated plasticity, all of which are thermally activated. Hence, as represented in Path1, the compressive stress build-up is relieved at temperatures close to the SiN deposition temperature. As the entire structure cools after processing, the Cu lines develop tensile stresses due to its mismatch in CTE with Si. If this tensile stress exceeds that required for void nucleation, then stress voiding would occur. Once the void nucleates, the tensile stress is relieved. On the other hand, if the tensile stress does not exceed the void nucleation threshold, the stress can be relaxed upon re-heating the structure. For simplicity, we assume the interconnect lines behave perfectly elastically. Therefore, Path2 and 3 coincide with each other in Figure 2.5(a).
Relieving the intrinsic stress build-up is the thermodynamic driving force for stress voiding to occur. Kinetically, however, the stress-induced void growth rate is also characterized by atomic mobility. The intrinsic stress is highest at the lowest temperature. On the other hand, the Cu atomic diffusivity increases exponentially as the temperature increases. This would yield a maximum stress voiding rate at a temperature that is relatively high compared to room temperature but lower than the SiN deposition temperature (see Figure 2.5(b)).
Fig. 2.5. (a) Illustration of the intrinsic stresses inside a Cu interconnect line assuming perfect elastic behavior. (b) The stress voiding rate.
In order to quantitatively characterize stress voiding, we applied a model for
atomic diffusion in embedded lines by Nix et al. [Sau 92] in our calculations. This model
correlates the activation energy for electromigration and the temperature to the rate of the
void growth. C.L. Gan's calculation shows that the temperature at which fastest stress
induced void growth occurs is near 320°C [Gan 02b], which is close to that of the
electromigration testing temperature (350°C).

Experimentally, direct evidence of stress-induced voiding was seen in an
extrusion monitor plate that was not used during an electromigration stress test at 350°C
for nearly 300 hours. Figure 2.6 shows a cross-sectional SEM image of void formation in
that extrusion monitor plate. The void nucleated at the top Cu/SiN interface of the
extrusion monitor in the upper metallization shown in Figure 2.6. This suggests that the
Cu/SiN interface not only serves as a fast diffusion path for electromigration, but also
provides a site for void nucleation.

In addition, we also observed that the \( t_{50} \)'s for Cu interconnects decreased after
pre-test annealing (see Table 2.2). In this study, all the electromigration experiments
were conducted at 350°C, and 2.0x10^6 A/cm^2. During pre-test annealing, the sample was
continuously heated at 350°C for 300 hours. From the contrasts in the results shown in
Table 2.2, for all the interconnect lengths tested, pre-test annealing appeared to lead to
decreased lifetimes of the Cu interconnects, although the effect was small.
Fig. 2.6. Cross-sectional SEM image of stress-induced void in an unused extrusion monitor. Here, the extrusion monitor plate is the upper metallization of two. The void nucleated at the Cu/SiN interface.

Table 2.2. Results from electromigration experiments using M1 structures.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Pre-test</th>
<th>Length (μm)</th>
<th>Width (μm)</th>
<th>j (MA/cm²)</th>
<th>t₀ (mins)</th>
<th>σ</th>
<th>% Unfailed Lines</th>
<th>% Test Unfailed Lines</th>
<th>Decrease in MTTF (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>No</td>
<td>1000</td>
<td>0.30</td>
<td>2.0</td>
<td>3138</td>
<td>≥1.12</td>
<td>23.1</td>
<td>13659</td>
<td>--</td>
</tr>
<tr>
<td>M1</td>
<td>Yes</td>
<td>1000</td>
<td>0.30</td>
<td>2.0</td>
<td>2430</td>
<td>≥1.22</td>
<td>7.70</td>
<td>16631</td>
<td>22.5</td>
</tr>
<tr>
<td>M1</td>
<td>No</td>
<td>100</td>
<td>0.30</td>
<td>2.0</td>
<td>1158</td>
<td>0.76</td>
<td>0</td>
<td>4851</td>
<td>--</td>
</tr>
<tr>
<td>M1</td>
<td>Yes</td>
<td>100</td>
<td>0.30</td>
<td>2.0</td>
<td>966</td>
<td>0.48</td>
<td>0</td>
<td>2373</td>
<td>14.0</td>
</tr>
<tr>
<td>M1</td>
<td>No</td>
<td>50</td>
<td>0.30</td>
<td>2.0</td>
<td>4854</td>
<td>≥0.49</td>
<td>20.0</td>
<td>8511</td>
<td>--</td>
</tr>
<tr>
<td>M1</td>
<td>Yes</td>
<td>50</td>
<td>0.30</td>
<td>2.0</td>
<td>4356</td>
<td>≥1.01</td>
<td>25.0</td>
<td>9691</td>
<td>10.2</td>
</tr>
</tbody>
</table>
2.4 Current Direction Effects

As previously mentioned, the Cu/SiN interface inside dual-damascene Cu interconnects serves both as the dominant diffusion path and as the likely site for void nucleation. This fact is important in determining the locations and modes for Cu interconnect failures. C.L. Gan carried out a series of comparisons between M1 and M2-type interconnect lines, where the only difference between the two types was the direction of the electron flow [Gan 01, Gan 02]. Gan reported an asymmetry in reliability behavior, where the lifetimes of the M2-type structures were always higher than those of the M1 type structures, provided that both types of interconnects had the same length, width, and the number of vias at each end (see Figure 2.7 and Table 2.3 [Gan 01]). This section explains how the direction of the electron flow affects the interconnect reliability.
Fig. 2.7. Time-to-failure for 800μm-long, 0.28μm-wide single via and 1.0μm-wide 4-via, M1 and M2 test structures stressed at 350°C and 2.5 MA/cm². The data show that M2 structures are more reliable and are more likely not to fail after very long test times. [Gan 01]
Table 2.3. Test results for populations of M1 and M2 test structures with various physical characteristics. The structure label indicates the metallization level of the test line (e.g., level 2 for M2_1) and the number of vias at the end of the test line (e.g., 4 for M2_4).

MTF is the measured median time to failure, including unfailed lines, and σ is the standard deviation of the natural log of the failure times, excluding unfailed lines. [Gan01]

<table>
<thead>
<tr>
<th>Structure</th>
<th>Length (µm)</th>
<th>Width (µm)</th>
<th>J (MA/cm²)</th>
<th>t₅₀ (hours)</th>
<th>σ</th>
<th>% unfailed lines (test time in hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1_1</td>
<td>800</td>
<td>0.28</td>
<td>2.5</td>
<td>28.7</td>
<td>1.07</td>
<td>6.7 (479)</td>
</tr>
<tr>
<td>M2_1</td>
<td>800</td>
<td>0.28</td>
<td>2.5</td>
<td>186.7</td>
<td>1.70</td>
<td>31.3 (479)</td>
</tr>
<tr>
<td>M1_1</td>
<td>800</td>
<td>1.0</td>
<td>2.3</td>
<td>3.4</td>
<td>0.53</td>
<td>0 (169)</td>
</tr>
<tr>
<td>M2_1</td>
<td>800</td>
<td>1.0</td>
<td>3.6</td>
<td>8.0</td>
<td>1.16</td>
<td>0 (169)</td>
</tr>
<tr>
<td>M1_4</td>
<td>800</td>
<td>0.28</td>
<td>2.3</td>
<td>93.4</td>
<td>0.42</td>
<td>0 (317)</td>
</tr>
<tr>
<td>M2_4</td>
<td>800</td>
<td>0.28</td>
<td>3.6</td>
<td>266.7</td>
<td>2.21</td>
<td>50 (317)</td>
</tr>
<tr>
<td>M1_4</td>
<td>800</td>
<td>1.0</td>
<td>2.5</td>
<td>53.3</td>
<td>0.72</td>
<td>0 (191)</td>
</tr>
<tr>
<td>M2_4</td>
<td>800</td>
<td>1.0</td>
<td>2.5</td>
<td>125.3</td>
<td>0.17</td>
<td>0 (191)</td>
</tr>
<tr>
<td>M1_1</td>
<td>100</td>
<td>0.28</td>
<td>2.5</td>
<td>20.5</td>
<td>0.85</td>
<td>6.3 (192)</td>
</tr>
<tr>
<td>M2_1</td>
<td>100</td>
<td>0.28</td>
<td>2.5</td>
<td>122.8</td>
<td>1.54</td>
<td>27.3 (434)</td>
</tr>
<tr>
<td>M1_1</td>
<td>50</td>
<td>0.28</td>
<td>2.3</td>
<td>20.8</td>
<td>1.48</td>
<td>12.5 (166)</td>
</tr>
<tr>
<td>M2_1</td>
<td>50</td>
<td>0.28</td>
<td>3.6</td>
<td>68.7</td>
<td>1.58</td>
<td>31.3 (166)</td>
</tr>
<tr>
<td>M1_1</td>
<td>20</td>
<td>0.28</td>
<td>2.5</td>
<td>163.7</td>
<td>1.74</td>
<td>37.5 (386)</td>
</tr>
<tr>
<td>M2_1</td>
<td>20</td>
<td>0.28</td>
<td>2.5</td>
<td>236.7</td>
<td>1.48</td>
<td>40 (434)</td>
</tr>
</tbody>
</table>

Gan's report points out that the observed asymmetry in the reliability of M1 and M2 structures is related to the ease of nucleation and growth of electromigration-induced voids at the Cu/Si₃N₄ interface. During electromigration in Cu interconnects, a tensile stress develops at the cathode ends of the lines, where the Ta liner forms a blocking boundary to the diffusing Cu atoms [Wan98, Fil95]. If the critical tensile stress for void nucleation is reached, a void forms. In M2 structures, the maximum tensile stress is reached at the base of the vias, where Ta binds the Cu on all sides. However, voids preferentially nucleate at the Cu/Si₃N₄ interface. After nucleation, the void will grow, resulting in a partially spanning void. As a result, the resistance of the test structure will
increase only slightly while there is still a high-conductivity Cu path for conduction (see Figure 2.8). An open-circuit failure will result only when the void grows to span the whole thickness of the metal line. If this happens, all the current is forced to flow through the thin Ta liner layer, inducing significant Joule heating that leads to an open circuit failure. On the other hand, in M1 structures the maximum tensile stress develops at the Cu/Si₃N₄ interface near the cathode vias of the M1 lines. Therefore, an open-circuit failure will occur if a small-volume void forms below the via, such that the pathway for electron flow is blocked (see Figure 2.8). This asymmetry in the void volume required for failure also contributes to the length effects presented in the next section.

![Diagram](image)

Fig. 2.8. Schematic contrasts of void formation in M1 and M2-type of interconnects. (a) A small-volume fatal void in an M1 interconnect; (b) A large-volume partially-spanning non-fatal void in an M2 interconnect.
2.5 Line Length Effects

We tested M1 interconnect segments of different lengths. For all tests, the testing temperature was 350°C. The results are listed in Table 2.4. In this table, $j$ is the current density, $\sigma$ is the deviation in the log of the failure times, and '% unfailed' is the percentage of structures that did not fail. In this section, length dependencies of Cu interconnect reliability are discussed, and compared to those of Al interconnects.

We find that at short lengths, similar to Al-based interconnects, the reliability of Cu-based interconnects improves. Also like Al interconnects, some short Cu segments do not form voids that cause failure before back-stresses prevent the further growth of voids. However, unlike Al-based interconnects, there is no apparent deterministic current-density line-length product ($jL$) for which all lines are immortal. This is related

Table 2.4. Lifetimes data from electromigration experiments using M1-type interconnects at different lengths.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Length (µm)</th>
<th>Width (µm)</th>
<th>$j$ (MA/cm²)</th>
<th>$t_{50}$ (min)</th>
<th>$\sigma$</th>
<th>% unfailed lines</th>
<th>Test time (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 (Sematech)</td>
<td>1000</td>
<td>0.3</td>
<td>2.0</td>
<td>2430</td>
<td>$\approx$1.22</td>
<td>7.7</td>
<td>16631</td>
</tr>
<tr>
<td>M1 (Sematech)</td>
<td>100</td>
<td>0.3</td>
<td>2.0</td>
<td>996</td>
<td>0.48</td>
<td>0</td>
<td>2373</td>
</tr>
<tr>
<td>M1 (Sematech)</td>
<td>50</td>
<td>0.3</td>
<td>2.0</td>
<td>4356</td>
<td>$\approx$1.01</td>
<td>25.0</td>
<td>9691</td>
</tr>
<tr>
<td>M1 (IME)</td>
<td>800</td>
<td>0.28</td>
<td>2.5</td>
<td>1720</td>
<td>$\approx$1.07</td>
<td>6.7</td>
<td>28731</td>
</tr>
<tr>
<td>M1 (IME)</td>
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<td>0.28</td>
<td>2.5</td>
<td>1230</td>
<td>$\approx$0.85</td>
<td>6.3</td>
<td>11541</td>
</tr>
<tr>
<td>M1 (IME)</td>
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<td>0.28</td>
<td>2.5</td>
<td>1282</td>
<td>0.62</td>
<td>0</td>
<td>23189</td>
</tr>
<tr>
<td>M1 (IME)</td>
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<td>0.28</td>
<td>2.5</td>
<td>9820</td>
<td>$\approx$1.74</td>
<td>37.5</td>
<td>23189</td>
</tr>
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</table>
to the absence of a conducting refractory-metal overlayer in Cu-technology that can shunt current around small voids. Also unlike Al, we find that at long lengths a sub-population of Cu lines is immortal. We propose that this is the result of rupture of the thin refractory metal liner at the base of the dual-damascene Cu vias. As a consequence of this complex behavior, median times to failure and lifetime variations are minimum at intermediate line lengths.

2.5.1 Short Length Effects in Al Technology

As reviewed in section 1.2.2, the condition for immortality for an interconnect segment is [Ble 76]

\[
(jL)_{\text{critical}} = \frac{2\Delta \sigma_{\text{nucleation}} \Omega}{z^* q \rho}.
\]  (2.3)

For Al interconnects, \(\Delta \sigma_{\text{nucleation}}\) is estimated to be about 600MPa [Hau 00b], which translates to a \((jL)\) value of about 3000A/cm, taking \(z^*=4\) [Par 99] and at a temperature of 200°C.

In Al technology, highly EM-resistant refractory metal layers (TiN, Al₃Ti, or both) are usually used on the top and bottom of the lines. Therefore, even if the critical stress for void nucleation is reached in Al, a void can grow to fully span the Al layer without causing an open-circuit failure, because current can shunt around the void through the refractory metal layers. Once a void nucleates, it will continue to grow until the back stress balances the electron wind force. At this point, void growth will stop and the resistance of the interconnect line will saturate. If the increase in resistance at
saturation is lower than the failure criterion, the line is considered immortal due to resistance saturation. Under these conditions, the \((jL)\) product could be expressed as

\[
(jL)_{crit,AR} = \frac{\rho/A}{\rho/A_c} \frac{\Delta R_{crit}^{max}}{R} \frac{2\Omega B}{\varepsilon z * \rho}.
\]

(2.4)

where \(A\) and \(A_c\) represent the cross-sectional area of the high-conductivity metal and the shunt layer, respectively. Resistance saturation was first demonstrated experimentally by Filippi et al. [Fil 95, Fil 96]. For Al technology, the \((jL)\) value for immortality under resistance saturation, \((jL)_{AR}\), is about 4000A/cm [Fil 96].

### 2.5.2 Short Length Effects in Cu Technology

A number of investigations of the effects of decreasing line length on the reliability of dual-damascene Cu-based interconnects, similar to those used in our study, have been carried out. Ho et al reported that, using statistical analyses on M2-type test lines, \((jL)_{crit}\) is 3700A/cm [Oga 01, Lee 01]. Hau-Riege found that for M1-type test lines, the probability of failure drops dramatically for 10.5μm-long lines at a current density of 2.0MA/cm², compared to longer lines tested at the same current density [Hau 01, Hau 02]. This suggests that \((jL)_{crit}\) is less than 2100A/cm. However, as mentioned in section 2.4, the failure mechanisms for M1 and M2-type interconnects are fundamentally different [Gan 01]. Due to this difference in failure mechanisms, the aforementioned studies report critical \((jL)\) values for fundamentally different failure phenomena. The \((jL)\) value reported by Hau-Riege corresponds to an upper bound for \((jL)_{nucleation}\), while the \((jL)\) value reported by Ho et al corresponds to an equivalent \((jL)_{AR}\) for Cu. This aspect is important in explaining the lifetime dependencies in short Cu lines.
In today’s Cu-technology, Si$_3$N$_4$, an electrical insulator, is used as an inter-level diffusion barrier and as a capping layer for interconnects. Therefore, in M1-type test structures, even when a low-volume void forms below a via, it can cause an open circuit failure if it spans the bottom of the via, as shown in Figure 2.9(a) [Hau 02]. This is because the void will block current flow since the Si$_3$N$_4$ layer cannot shunt current as the refractory metal layers do in Al technology. Also, the Si$_3$N$_4$ layer provides sites for void nucleation, and contributes to the low stress needed for void nucleation in Cu. In S.P. Hau-Riege’s report [Hau 02], he estimated a probabilistic $(jL)_{nucleation}$ value less than 2100A/cm corresponds to a $\Delta\sigma_{nucleation}$ of less than 40MPa [Hau 02], using the lower limit of $z^*=1$ [Hu 99]. This value is extremely low compared to the equivalent value for Al technology ($\Delta\sigma_{nucleation}$=600MPa). This is due to the poor adhesion between Cu and SiN layers. Thus, in M1-type interconnects, true immortality requires that the conditions for void nucleation are not reached.

However, in M2-type interconnect structures, voids that nucleate and grow at the Cu/Si$_3$N$_4$ interface must grow to span the entire line and the refractory metal liner must fail for an open circuit failure to occur. Therefore, in M2-type structures, true immortality requires that the electron wind force not exceed the back stress, which is equivalent to the resistance saturation scenario in Al interconnects. However, actual resistance saturation is not observed experimentally, as the non-fatal voids that partially span the M2-type structures as shown in Figure 2.9(b) [Hau 02] do not significantly increase the resistance of the line.
We find that for M1 structures, as the line length is decreased, the median-times-to-failure are highest at a \((jL)\) product of 10000A/cm for the Sematech samples \((L = 50\mu m)\), and 5000A/cm for the IME samples \((L = 20\mu m)\). These line lengths were the minimum available on the fabricated structures. The \((jL)\) products suggest that void nucleation is highly probable inside the line, because they are higher than the \((jL)_{\text{nucleation}}\) reported by Hau-Riege [Hau 01, Hau 02]. Therefore, it is not surprising that the majority of the structures failed, as shown in Table 2.4. However, the \((jL)\) products are in the range of the \((jL)_{\text{crit}}\) reported by Ho et al [Oga 01, Lee 01]. This fact suggests that non-fatal voids could also exist in the M1-type interconnect segments, so long as the voids do not span the Cu. An example is shown in Figure 2.10. Therefore, in the range of short lines investigated here, all lines are expected to have voids, but whether or not these voids lead to failure depends on their location and shape.
2.5.3 Long Length Effects in Cu Technology

For the very long interconnect segments considered in this current study (1000µm and 800µm lines fabricated by Sematech and IME, respectively) high values of the lognormal variance, σ, were observed, and some lines never failed (see Figure 2.11). The stress difference, Δσ, that should develop in 1000µm-long lines tested at 2.0MA/cm², and 800µm-long lines tested at 2.5MA/cm², should both be approximately 5200MPa (taking a lower bound of z*=1 and ρ=4.0µΩ-cm at 350°C [Hau 02, Hu 99]). Clearly, this stress is more than sufficient to cause void nucleation if indeed the refractory-metal liners at the bottom of the vias block electromigration. However, the presence of a sub-population of immortal lines suggests that the refractory metal liners in one or both of the vias, in fact, did not block electromigration. We propose that the apparent immortality of a sub-population of long lines is the result of electromigration-stress-induced rupture of the Ta
liners at the vias, as schematically illustrated in Figure 2.12. Rupture of the liners would allow continuous flow of Cu to and from the connector lines and contact pads, which serve as large sinks and reservoirs for Cu [Hu 01]. It should be pointed out that while liner rupture can lead to an improved reliability in these and similar test structures, the presence of reservoirs and sinks would contribute to a reduced reliability in connecting lines on a circuit-level.

![Graph showing cumulative failure percentage vs. TTF](image)

**Fig. 2.11.** Example lognormal plot showing high values of lognormal variance, $\sigma$, and failure distributions that exhibit multiple modes of failures. This experiment was performed at $350^\circ$C and $2.0\text{MA/cm}^2$, using $1000\mu\text{m}$ long M1 lines.
The results from these experiments using straight-line structures demonstrate two major characteristics of the reliability of Cu interconnects. First, the Cu/SiN interface degrades the reliability of Cu by providing a site for easy void nucleation and fast electromigration. Second, the Cu-filled vias may not be fully blocking. The combination of the two aspects gives rise to the multiple failure mechanisms summarized in this chapter. This also suggests that characterization and improvements of Cu reliability should revolve around these two issues. These results further suggest that different reliability models should be applied to M1 and M2-type structures, and that, if liners can rupture, interconnect trees are no longer fundamental reliability units whose reliabilities are independent. Both of these results constitute profound differences from Al, and call for significant revision of circuit-level reliability assessment methodologies.

**Figure 2.12.** A schematic view of a ruptured liner at the bottom of a dual-damascene via, in a long interconnect segment.
2.6 Conclusions

Our phenomenological studies using straight-line structures have revealed that voids easily nucleate in Cu interconnects, primarily at the Cu/Si$_3$N$_4$ interface. As a consequence, the void volume required for failure is different between M1- and M2-type interconnect lines, which results in an asymmetry between the reliability of the two types of interconnect lines. Our length-effect reliability studies have shown that at short lengths, a range of small-volume voids may exist that can be tolerated or can be fatal, depending on the void shape and location. Consequently, for M1 test structures, $(jL)_{GR}$ is non-deterministic, which contrasts with Al technology. At long line lengths, bi-modal failure statistics are observed. Some lines failed relatively rapidly due to void formation and growth, and others do not fail even after very long times, presumably because the liners at vias rupture so that lead lines and contacts provide sinks and reservoirs for Cu flow. The phenomenology reported here for Cu interconnects is very different from that of similar Al-based interconnects. Our findings point to the need for new test and reliability assessment strategies for Cu-based interconnects.
Chapter 3  MEASUREMENTS OF Cu ELECTROMIGRATION

DRIFT VELOCITIES IN DUAL-DAMASCENE INTERCONNECTS

Electromigration-induced failure normally occurs through void nucleation and subsequent growth. In current Cu-based interconnect technology, void nucleation is known to occur easily at low stresses – 40MPa or less [Hau 02]. The lifetime of Cu-based interconnects is therefore often dependent on the rate of void growth, a measure of which is given by the drift velocity, \( v_d \).

Measurements of electromigration drift velocities provide important insight into the kinetics of electromigration. The Nernst-Einstein relationship correlates the electromigration drift velocity with the product of the effective diffusivity, \( D_{\text{eff}} \), and the effective charge, \( z^* \) [Hu 99],

\[
(Dz^*)_{\text{eff}} = \frac{v_d k T_{\text{test}}}{q \rho j}.
\]

(3.1)

where the effective diffusivity captures the contributions from all transport paths present in an interconnect line [Hu 99]

\[
(Dz^*)_{\text{eff}} = D_B z^* n_B + D_I z^*_I \delta_I \left( \frac{2}{w} + \frac{1}{h} \right) + D_S z^*_S \delta_S \left( \frac{1}{h} \right) + D_{GB} z^*_GB \frac{\delta_{GB}}{d} \left( 1 - \frac{d}{w} \right).
\]

(3.2)

Here, \( n \) is the electron density, \( \delta \) is the width of the interfaces, and \( d, h, \) and \( w \), are the grain size, line thickness, and line width, respectively. The sub-indices \( B, I, S \), and \( GB \) denote the bulk lattice, interfaces with the refractory metal liner, surface at the Cu/overtlayer interface, and grain boundary, respectively. In current Cu technology, the dominant diffusion path is the Cu/SiN surface. Therefore, the term containing \((Dz^*)_S\) is

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expected to dominate in Equation (3.2). As a result, \((Dz^*)_\text{eff}\) has the following form:

\[(Dz^*)_\text{eff} \propto (Dz^*)_S \propto (D_0 z^*)_S \exp\left(-\frac{E_{a,S}}{kT}\right).\]  \hspace{1cm} (3.3)

Combining Equations (3.1) and (3.3), we can see that \(\nu_d\) contains the electromigration activation energy, and we expect \(\nu_d\) to be linearly proportional to the current density.

Drift velocities may also serve as quantitative indications of the reliability of a given Cu metallization process. Recent literature indicates that the failure distributions in Cu electromigration stress tests are frequently multi-modal [Gan 01, Wei 02, Gil 02]. Such distributions are due to multiple failure mechanisms that are present in Cu interconnects with respect to the current directions and line lengths [Gan 01, Wei 02]. As a result, conventional interpretations of experimental data fit using a mono-modal lognormal distribution function may not be accurate. On the other hand, measurements of the electromigraiton drift velocity provide more fundamental knowledge than lifetimes. Therefore, measurement of the drift velocity provides a quantitative assessment of the electromigration process that precedes all failure mechanisms.

Conventionally, drift velocities are determined through ‘Blech’ drift experiments (see section 3.1). Such a method is not without disadvantages, which are discussed in the following section. Currently, simple and reliable experimental techniques for drift velocity measurements are still lacking. In this chapter, we describe a method for measurements of the drift velocity using results from electromigration stress tests of dual-damascene Cu interconnects – both M1- and M2-type. In both cases, we observed that in a significant fraction of the test population, the resistance of the lines increased linearly with time prior to failure. We postulate that this gradual increase in resistance results from void growth and that the rate of resistance increase correlates with the
electromigration drift velocity.

3.1 Conventional ‘Blech’ Drift Experiments

Shortly after the microelectronic industry felt the impact of electromigration on reliability, an experimental technique for estimating the drift velocity was developed by Blech et al. [Ble 76, Ble 76b, Ble 77]. These kinds of experiments are referred to as ‘Blech’ drift experiments, for which patterned-line structures are fabricated. For example, first, a bi-layer film of Al and TiN is patterned into stripes with widths of 20 to 25 μm. The top Al layer is then further patterned into line segments with controlled lengths using a selective etch. During electromigration testing, a fixed current is applied to the sample. The current flows predominantly through the Al line rather than the TiN under-layer since Al’s resistivity is less than 1% of that of TiN. If the structures were fabricated without a passivation layer, then the electromigration tests were usually conducted in a reducing ambient (containing H₂ gas) or a high vacuum ambient, to prevent the Al lines from oxidizing. Alternatively, the structure could be fabricated with a layer of passivation, such as SiN, encapsulating the Al lines both on the top and on the sides (see Figure 3.1). During these ‘Blech’ experiments, the displacement of the edge of the high-conductivity metal strip is observed in-situ using tools like top-view SEM [Ble 76]. The passivation also serves as blocking boundaries [Ble 76, Kno 97]. Using passivated samples, Blech was able to demonstrate that a minimum strip length was required for electromigration to occur. This length is referred to as the Blech length, which served as the basis for the concept of the (jL) immortality conditions that are discussed in Chapter 2 [Kno 97]. After the introduction of Cu interconnects, such in-situ
SEM observations have been made using Cu-based Blech drift structures and their dual-damascene derivations [Lee 95, Lin 02, Lan 03] (see Figure 3.2).

![Diagram of Blech drift structure with passivation and edge displacement.]

**Fig. 3.1.** The Blech drift structure with passivation.

![SEM image of void growth in a M2-type dual-damascene Cu interconnect line.]

**Fig. 3.2.** Void growth observed in a M2-type dual-damascene Cu interconnect line using a top-view *in-situ* SEM apparatus [Lin 02, Lan 03]. The drift velocity is calculated by estimating the void edge motion as a function of time.
Although such observations are straightforward, there are some disadvantages. The fabrication steps for the structures used in the in situ SEM experiments are usually different from those for the standard dual-damascene interconnects. For example, the top passivation layer must be thin enough for in-situ SEM observations to be made. This may result in less mechanical constraint than that for the standard test structures. Also, void formation under vias or in the lower levels of metallization cannot be detected. We present a technique for characterizing the electromigration drift velocity directly from constant-current stress experiments using fully processed Cu interconnect structures.

3.2 Experimental

For this investigation, we conducted electromigration stress experiments on both M1 and M2 type fully processed Cu dual-damascene interconnect lines. The structures were fabricated by Intel Corp., International Sematech Corp., and the Institute of Microelectronics in Singapore. For the M1 structures, the refractory metal diffusion barrier surrounding the Cu interconnect lines at the sides and bottom consists of a bi-layer of 100Å of Ta above 150Å of TaN. For the M2 structures, the barrier is a single layer of 250Å of Ta. For all interconnect lines, a Si₃N₄ layer caps the top. Figure 3.3 shows the line and via dimensions, as well as the via placement in the structures.
Fig. 3.3. Schematic top views of the M1 and M2-type interconnect test structures and their dimensions.

In these experiments, the test population was 16-18 samples per test. The failure criterion was a 100% change of the initial resistance, with a tolerance of 0.1% change of the initial resistance in fluctuations. In the M1-type structures, such a change corresponds to about 0.1Ω at 300°C. We used a number of combinations of conditions in testing the M1-type structure (see Table 3.1). We tested M2 structures with $j = 2.0$ and 2.5MA/cm² at 350°C at two different lengths, 500 and 1000µm.

3.3 Results

For both M1- and M2-type structures, we observed regimes in which the resistance of the structures increased linearly with time. In the M1-type interconnects, the resistance of the metal lines remained constant for an incubation period. Following this period, we observed that the resistance gradually increased over a period of time
prior to failure. This can be easily shown in a normalized $R$ verses $t$ plot (see Figure 3.4a and 3.4b). The $y$-axis corresponds to the resistance increase, $\Delta R = R - R_0$. The $x$-axis, $t^*$, designates the difference between the actual test time and the incubation period, $t_0$. Here, $t_0$ was taken to be the time required for the first non-zero $\Delta R$ measurement.

For M2-type interconnects, the resistance of the lines also remained constant for a period. Following this period, however, only a fraction of the population of M2 interconnects showed a region of steady resistance increase. This region ranged over a much longer period of time than that observed for M1 interconnects (see Figure 3.4c and 3.4d). For M2 structures, the drift regime was preceded by a 'jump' in resistance ranging from 15 to 70$\Omega$ in magnitude. Another fraction of the M2 population showed an abrupt resistance increase without a steady increase regime. A third, small fraction (up to 3 samples per test) of the M2 population did not show any resistance increase at all during the entire testing period (see Figure 3.9).
Fig. 3.4. Schematic Resistance versus time trends observed for (a) M1-type and (c) M2-type interconnects. (b) and (d) are examples of normalized R vs t plots showing a regime of steady resistance increase for M1-type and for M2-type structures, respectively. The y-axis corresponds to the resistance increase, $\Delta R = R - R_0$. On the x-axis, $t^*$, designates the difference between the actual test time and the incubation period, $t_0$. 

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3.4 Discussion

3.4.1 Drift in M1-type Interconnects

For the experiments performed using M1-type interconnects (see Table 3.1), the lowest value of the \( jL \) product was 7000A/cm. This value is larger than the \( (jL)_{\text{crit.nucleation}} \) reported by Hau-Riege [Hau 01, Hau 02]. This fact suggests that voids are expected to form inside the Cu. We postulate that the resistance increase observed was due to void growth in the interconnects. It has been reported that in M1 interconnects, the void location is most likely to be directly below the cathode-end via [Hau 01, Hau 02, Gan 01, Gan 02]. The volume for a void in M1 structure is usually small and slit-like. We confirmed this in the structures for our experiments (see Figure 3.5). Therefore, during void growth in the M1-type structures, the contact area between the via and the M1 line would decrease. Inversely proportional to such a decrease of the contact area, we would expect the via resistance of the structure to increase. Open failure occurs when the slit-like void growth spans the entire via-M1 line contact area. We considered that the void nucleates near the edge of the cathode end of the line and grows under the via as shown in Figure 3.6. Other void nucleation locations would not result in a slit-like void shape as observed in failure analyses. We assumed that during the initial growth period, the void below the via grows in a uniform fashion, which corresponds to the steady state resistance increase. Therefore, for this phase of void growth, we can correlate the motion of the void front, i.e., \( v_d \) to the rate of the resistance increase. During the later stage, we postulate that the void growth process would become unstable because as the contact area between the via and the M1 line decreases, the current density in the remaining contact area increases, which in turn accelerates voiding in a run-away process. This would lead
to the observed dramatic resistance increases, which lead to failures in the structures, after steady state growth.

Fig 3.5. Post-mortem analysis of an M1-type interconnect. Figure shows a small void formed directly below the M1 cathode end via for an M1 line that is in the perpendicular direction of the viewing plane. The void formation is similar to that reported by Hau-Riege, and Gan [Hau01, Hau02, Gan01, Gan02].
Fig. 3.6. Cross-sectional view illustration of slit-like void growth process in M1-type interconnects due to electromigration. During the growth, the contact area between the via and the M1 line decreases causing the overall resistance of the structure to increase.

We assume that at $t^* = 0$, a void would have nucleated near the edge of the cathode end via and it has begun to grow. The void front would uniformly propagate below the cathode end via. We define the position of the void front from the edge of the via to be $x$ (see Figure 3.7). It follows that the contact area between the via and the line is $A = L(L-x)$, and

$$\frac{dA}{dt} = (-L) \frac{dx}{dt}. \quad (3.4)$$

As mentioned, the electromigration drift velocity, $v_d$, is the speed of the void front propagation, i.e., $dx/dt$ in Equation 3.4. We can correlate $v_d$ to the rate of resistance increase through the following simple model

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\[ \nu_d = \frac{dx}{dt} = \frac{\left( \frac{dR}{dt} \cdot L \right)}{R_{\text{via,0}}} , \quad (3.5) \]

where \( R_{\text{via,0}} \) is the via resistance at the testing temperature.

The slopes of the normalized \( R \) vs. \( t \) plots at \( t^*=0 \) were used to estimate \( \nu_d \) using Equation 3.5. The estimated electromigration drift velocities under different test conditions are summarized in Table 3.1. The average activation energy is 0.80±0.06eV for M1-type interconnects (see Figure 3.8a). The value of the activation energy value is consistent with that obtained for the MTF determined for the same structures, which is 0.8±0.1eV. Furthermore, this value of activation energy is also in close agreement with literature values, which range from 0.7 to 0.9eV [Hu 99, Lin 02, Lan 03, Par 91].

**Fig. 3.7.** Definition of the axis for void growth in M1-type interconnects.
The data in Table 3.1 also show that the electromigration drift velocity is nearly linearly proportional to the current density. The average value of the current density exponent is $1.1 \pm 0.3$. The current density exponent is obtained through a linear fit of $\log(v_d) \text{ vs } \log(j)$ for structures tested at the same temperature (see Figure 3.8b). Since a current density exponent of one is expected from the Nearest-Einstein relationship, the measured current density exponent of 1.1 further supports the accuracy of our technique.

Table 3.1. Values of $v_d$ [$\times 10^4 \mu$m/hr]; values of $E_a$ [eV]; and values of $j$-exponent. $E_a$ was obtained from linear fitting of $\ln v_d$ vs $1/T$ at the same current densities. $j$-exponent was obtained from linear fitting of $\log v_d$ vs $\log j$ at the same temperatures.

* ** The M2 structures used at the two different current densities shown here were fabricated by two different companies. All of the M1 structures were fabricated at the same third location.

*** This $v_d$ value was extrapolated using $j$-exponent=0.9, at T=350°C.

<table>
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<th>(M2)</th>
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<td>0.9±0.3</td>
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</tr>
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</table>
Fig. 3.8. (a) Plot of log($v_d$) vs. 1/T at different current densities; (b) plot of log($v_d$) vs log($j$) at different temperatures. The slopes of the best-fitting lines are (a) the activation energies divided by the Boltzmann’s constant, and (b) the current density exponents.
3.4.2 Drift in M2-type Interconnects

As mentioned above, three types of resistance verses time behaviors were seen in our experiments using M2 interconnect lines. Similar observations have also been reported by Gill et al. [Gil 02]. Type I behavior represents 'immortality'. The overall resistances of the lines do not change during the entire experiment. Such immortality is thought to be the result of non-blocking boundaries at the bottom of the vias as discussed in Chapter 2. Type II behavior corresponds to abrupt open failures. The resistance of the test lines remains nearly constant until the resistances increase dramatically over an extremely short time. Type III behavior represents steady drifts prior to failure. In this case, we observed that small 'jumps' were followed by regions of steady resistance drift (see Figure 3.9).
Fig. 3.9. Resistance versus time curves for M2-type structures with L=1000μm, W=0.3μm, T=350°C, and j=2.0MA/cm². Three types of behaviors are seen here.

We propose that the causes of type II and III behaviors are the following. In the experiments using M2 interconnects, the smallest \(jL\) product is 12500 A/cm, which significantly exceeds the \(jL_{\text{nucleation}}\) condition described by Hau-Riege [Hau 01, Hau 02]. Therefore, we expect voids to form near the cathode. Due to the low energy required for void nucleation at the Cu/Si₃N₄ interface (~40MPa [Hau 02]), in M2-type interconnects, voids are expected to nucleate at the top surface, rather than inside the via where Cu is bounded by Ta liner on all sides. After nucleation, a void would grow downward to fully span the cross section of the Cu line. Failure analysis supporting this hypothesis (see Figure 3.10) has been reported in the literature [Gan 01, Gan02, Hau 01, Hau 02]. At this
point, electrons are forced to flow through a section of the very thin, high-resistivity liner material that surrounds the fully spanning void on the bottom and the sides. If the section of liner undergoes a lot of Joule heating, it might melt and cause type II behavior, abrupt open failures. On the other hand, if the section of the liner is able to support the electron flow, the liner will act as a shunt layer, and the fully spanning void could further grow along the line. Due to the difference between the resistivities of Cu and the liner material, this growth gives rise to the steady resistance increase, which corresponds to type III behavior, drift.

![Image](image.png)

**Fig. 3.10.** Cross-sectional SEM micrograph of a cathode end terminal via in an M2 line. Here, L=500μm, and W=0.3μm. The structure was tested at 350°C and 2.5MA/cm². A large-volume void formed above the cathode-end via prior to failure.
In all type III samples, prior to the steady growth in resistance, a small 'jump' in resistance was observed, ranging from 15 to 70Ω. We postulate that this is caused by the final step when a void becomes fully spanning to expose a small section of the liner material. Such values in resistance change roughly corresponds to a minimum length of 0.05 to 0.1µm, using $\text{TCR}_{\text{Ta}}=4.08\times10^{-3}\text{K}^{-1}$, temperature of 350°C, and line width of 0.3µm.

The type III behavior described above is similar to that observed using in-situ SEM tools for estimating the Cu drift velocities in interconnects (Figure 3.2) [Lin 02, Lan 03]. Therefore, we can correlate the gradual resistance increase in type III behavior to the drift velocity. We define the position of the void edge as $x$ as shown in Figure 3.11. Therefore, it follows that

$$\frac{dR}{dt} = \frac{\rho_{\text{Ta}}}{W_{\text{Ta}} h_{\text{Ta}}} \frac{dx}{dt} - \frac{\rho_{\text{Cu}}}{W_{\text{Cu}} h_{\text{Cu}}} \frac{dx}{dt}.$$  \hspace{1cm} (3.6)

Here, we assume a uniform void growth. Following the fact that the resistivity of Ta is much greater than that of Cu (more than 40 times at 300°C), Equation (3.6) can be simplified to be

$$v_d = \frac{dR}{dt} \left[ \frac{W_{\text{Ta}} h_{\text{Ta}}}{\rho_{\text{Ta}}} \right].$$  \hspace{1cm} (3.7)
Fig. 3.11. (a) Side view of the void growth process with x denotes the position of the void front. (b) Cross-sectional view of the M2 interconnect line.

We applied this simple model to the results for type III behavior seen in M2 interconnects, and determined that $v_d = 0.030 \pm 0.0056 \mu m/hr$ at a current density of 2.0MA/cm$^2$ and temperature of 350°C, for 1000μm long lines, and $v_d = 0.025 \pm 0.015 \mu m/hr$ at a current density of 2.5MA/cm$^2$ and temperature of 350°C, for 500μm long lines.

Especially given the fact that the M1-type, the 1000μm long M2-, and the 500μm long M2-type interconnect lines used in our experiments were fabricated by three different vendors, these $v_d$ values are in close agreement with each other.

3.5 Conclusion

We obtained values for the electromigration drift velocity by conducting constant current stress experiments. We found that this technique is a useful method to gain quantitative knowledge about electromigration in Cu interconnects. Contrary to lifetime measurements, the drift velocity results were consistent, among other aspects, with
respect to different structural configurations. The values of the electromigration drift velocities determined in M2 lines were similar to those measured in M1 lines. As shown in Chapter 2, M1 and M2 structures are known to have very different lifetimes under the same stress conditions [Gan 01, Gan 02, Hau 01, Hau 02]. Given that the stress for void nucleation should be the same, the observation that the rate of void growth is the same supports the proposal that the asymmetry in reliability in the two different configurations is associated with differences in the void sizes required to cause failure. This emphasizes that drift velocity is a more fundamental measure for electromigration than lifetime measurements.
Chapter 4  EXPERIMENTAL CHARACTERIZATION OF THE
RELIABILITY OF CU INTERCONNECT TREES

Basic phenomenological observations using straight two-terminal via-to-via lines are important for the study of electromigration. Through these investigations, we were able to identify the dominant diffusion path, characterize the main failure mechanisms, and estimate the fundamental rate of electromigration in Cu interconnects, as described in the previous chapters.

However, in a real integrated circuit, most interconnects form collections of segments that have multiple terminals and junctions. A unit of continuously connected segments lying within one layer of metallization is defined as an *interconnect tree* [Rie 98]. Within a tree, atoms can diffuse freely because individual segments do not have blocking boundaries. Consequently, the stress evolution in each segment is coupled with diffusion in other segments [Hau 00d]. However, most of the existing circuit-level reliability assessment methods are based on breaking up trees into individual segments and assessing the reliability of each segment separately by applying the results from straight via-to-via test directly. Generally, this is inaccurate because the reliabilities of the different segments in a tree are not independent of each other.

Therefore, in carrying out circuit-level reliability assessments, it is important to be able to assess the reliability of trees. Hau-Riege *et al.* conducted extensive experimental characterization and modeling studies of the reliability of the Al-based interconnect trees [Hau 00, Hau 00d, Hau 01b, Hau 01c]. It has been argued that an interconnect tree is the appropriate fundamental reliability unit (FRU) for circuit-level assessments of the
reliability of Al-based metallization [Hau 01b]. FRUs have reliabilities that can be treated independently, and the overall reliability can be characterized by the product of each FRU’s reliability. We performed experiments in order to characterize the reliability of Cu interconnect tress. This chapter summarizes the results we have obtained.

4.1 Experiments using the ‘Dotted-I’ Interconnect Trees

4.1.1 Experiments

A ‘dotted-I’ structure is a straight line that terminates with a via at each end, but also has a via in between that creates two linked segments. For this study, we investigated the reliability of dotted-I interconnect tree with a ‘drain’ segment having a fixed current. We performed electromigration tests using dotted-I interconnect trees fabricated by International Sematech and IME. The dotted-I tree is the simplest multi-segmented interconnect structure. The dual-damascene processing technology is the same as that described in Chapter 2. We used dotted-I trees with the length L=500μm, and the line width W=0.3μm (see Figure 4.1). All trees were fabricated in M2 with connector lines in M1 connected to vias.

![Schematic of dotted-I interconnect tree](image)

Fig. 4.1. Schematic top and side views of a dotted-I interconnect tree.
We used five different current density configurations in this experiment (see Figure 4.2(a)). All five tests were performed at a temperature of 350°C. The current density in the left limb, $j_e$, was 2.5MA/cm$^2$ for all configurations, while the current density in the right limb varied from test to test. In all tests, the current densities in the left and the right limbs were controlled independently. Failure was defined as a 30% increase over the initial resistance in either limb.

4.1.2 Results and Discussion

Figure 4.2(b) shows the times-to-failure for the five current density configurations used in our experiment. These results clearly show that the overall reliability of the whole interconnect tree depends on the direction and magnitude of the electron current in the right segment of the dotted-I structure. This was also demonstrated for Al-based interconnects by Hau-Riege [Hau 01b], whose results have been reproduced in Figure 4.3.
Fig. 4.2. (a) Schematic diagrams of dotted-I test structures with the five different current configurations used in the experiments. Tests were carried out at $T = 350^\circ C$ and $j_e = 2.5$ MA/cm$^2$. The arrows show the direction of electron flow. (b) Times-to-failure for 500$\mu$m-long, 0.28$\mu$m-wide dotted-I structures with the different electron current configurations shown in (a).

Fig. 4.3. (a) Times-to-failure for Al lines, defined as a 30% increase in electrical resistance in either segment, for 3.0$\mu$m-wide lines tested at $T = 250^\circ C$ and $j = 1\times10^6$ A/cm$^2$ for electron current configurations shown in (b). The line length $l = 500\mu$m. [Hau 01b]
However, we can see that the reliability characteristics of Cu dotted-I trees are different from that of Al dotted-I trees [Gan 02, Gan 02b] by comparing the five similar current density configurations employed in both the Cu and Al dotted-I tree experiments (see Figure 4.2 and Figure 4.3). The most obvious difference is to compare the reliability of configuration (1) in the Cu dotted-I tree experiments to that of configuration (iv) in the Al dotted-I tree experiments. In both cases, the electron flows with constant current density from the right-hand via toward the left-hand via. For Cu interconnects, this configuration showed a bi-modal distribution of failure times (Figure 4.3), where a subpopulation of samples did not fail, while the Al dotted-I trees did not show signs of multi-modal failures. The lower lifetime distribution in the case of Cu dotted-I trees has a $t_{50}$ that is actually lower than that of case (4). This trend would be the same as that of the Al dotted-I structures, if the immortal subpopulation were absent [Hau 00, Hau 01b, Gan 02]. On the other hand, the higher lifetime distribution has the largest $t_{50}$ compared to all other cases, with about 46% of the samples not failing after more than 800 hours of stressing. This failure characteristic is different from the results reported for Al-metallization [Hau 01b]. This behavior is similar to that of very long lines discussed in Chapter 2. High stresses that evolve at the ends of the long dotted-I structures (500$\mu$m) could cause rupture of the diffusion barrier layer [Wei 02]. As a result, the vias no longer act as blocking boundaries and the lifetime increases dramatically [Hu 01]. This means that for Cu interconnects, the reliability of segments can be affected by the reliability of neighboring segments that lie in different levels of metallization. The fundamental reliability unit defined for Al metallization, the interconnect tree, therefore cannot serve as a fundamental unit for Cu technology.
The second difference manifests in configuration (2) and (3) in the experiments on Cu dotted-I trees. In both cases, the right segment acts as an atomic reservoir for the left segment, which is passive and active for case (2) and (3), respectively. In both cases, the presence of an atomic source slowed the tensile stress build-up near the central via in the left segment, the highest stressed segment of the tree. Thus, t50's of configurations (2) and (3) are higher than those of (4) and (5), in which the right segment acts as an additional atomic sink away from the central via.

In configuration (2), where a passive atomic reservoir is present, as a tensile stress develops above the central via, Cu atoms from the unstressed right segment diffuse towards the central via due to the resulting stress gradient. During failure analysis, we confirmed that voids may extend from the central via into the right limb for up to 2μm in length (see Figure 4.4). Such a large volume required for failure corresponds to the long times-to-failure for configuration (2). On the other hand, in configuration (3), due to the low tensile stress required for void nucleation in current Cu technology, 40MPa or less [Hau 01, Hau 02], the right segment in configuration (3) is also prone to failures despite the fact that the left segment is stressed at a higher current. As a result, configuration (3) is less reliable than configuration (2) in Cu dotted-I structures, which is completely different from what was seen in Al dotted-I structures. In configuration (3), Cu atoms flow from the right segment toward the central via, slowing the rate of tensile stress development in the left segment. Even after the tensile stress around the central via is relieved by void nucleation, the difference between the electron wind force in the left and right segments would also cause the void to drift and elongate toward the right segment. Meanwhile, the atomic flow in the right-hand segment causes a tensile stress increase.
near the right-most via. In addition to void formation at the central via, voids could also form at the right-most via. The combination of the large void volume required for failure in configuration (2) and the possibility of multiple sites for void nucleation in configuration (3) causes the $t_{50}$ for configuration (3) to be lower than that of configuration (2) for Cu dotted-I trees.

Fig. 4.4. FIB images of voids in the middle via of a representative failed dotted-I structure for test condition (2). Samples were stressed at $T = 350^\circ$C and $j_e = 2.5$ MA/cm$^2$. The arrows show the direction of electron flow.
4.1.3 Summary on Dotted-I Trees Experiments

These experiments suggest that neither individual segments nor trees are fundamental reliability units for Cu, and the reliabilities of Cu interconnect trees are different from those of Al interconnect trees. These conclusions from the dotted-I tree experiments have inspired us to seek a via- or junction-based reliability assessment model for Cu interconnects. In order to complement these findings, we need to study the failure characteristics of the next simplest tree, the T-structure.

4.2 Experiments using T-structure Interconnect Trees

4.2.1 Experiments

We accomplished several objectives through the examination of the reliability of T-structures (Figure 4.5). We characterized the reliability of the T-structure (a junction connected to three neighboring segments) with one segment fixed as a constant atomic drain and another as an atomic source, while varying the current density in the third segment. The results from these experiments were contrasted to those obtained using the dotted-I structures. We also investigated the effect of the location of the additional atomic source segment on the reliability of the interconnect tree. Lastly, we examined the effect of the segment length on the reliability of the T-structures. We conducted constant-current electromigration stress experiments on the T-structures and ‘+-’-structures fabricated by International Sematech and IME. We used symmetric T-structures with \( L = 500 \mu m \) and 100\( \mu m \), and asymmetric T-structures with \( L = 500 \mu m \) (see Figure 4.5). Similar to the dotted-I structures, these tree structures were fabricated in second metallization level (M2) with connector lines in the first metallization level (M1).
All experiments were performed at a temperature of 350°C, and the failure criterion was defined as a 100% increase over the initial resistance for the overall structure.

We performed package-level electromigration stress experiments using the T-structure interconnect tree with five different current density configurations (see Figure 4.6). In all five configurations, the current density in the left-most segment was set at 2.5MA/cm², except for configurations (IV) and (V) where the current density is 5.0MA/cm². The ‘bottom’ segment (see Figure 4.6) acted as either a passive atomic reservoir (no stress current), or an active atomic source (an electron current density of 2.5MA/cm² flowing toward the central via). The electron current density in the right-most segment was set to be either 2.5MA/cm² flowing toward the central via, or 2.5MA/cm² flowing away from the central via, or zero. We used one power supply per package for configurations (I), (II), and (III). We used two power supplies per package for configurations (IV) and (V). The times-to-failures are shown in Figure 4.6.

![Diagram](image)

Fig. 4.5. Schematic top view of the (a) symmetric T-structure; (b) asymmetric T-structure; (c) ‘+’-structure.
4.2.2 Results and Discussion

For configuration (I), we observed a bi-modal failure distribution, similar to that seen for long dotted-I tress. As discussed in Chapter 2 and in the previous section, the bimodality shown by the failure distribution is related to the long-length effects. When the segment length is very long (500µm in this case) the high stresses developed at the end vias could possibly rupture the diffusion barriers in a subpopulation of samples, allowing Cu atoms to flow from bond pad to bond pad, so that the lifetime increases substantially.

Configurations (II) and (III) are analogous to configuration (2) in the dotted-I experiments (see Figure 4.2). Here, one or two segments of the T-structure trees act as atomic reservoirs connected to the cathode end of the drain segments. As shown in the discussion on the dotted-I tree, such configurations result in a void nucleating above the central via, and the void subsequently grows toward the unstressed limb(s). In configuration (II), there are two unstressed segments acting as atomic reservoirs, and there is only one stressed segment serving as an atomic drain. On the other hand, in configuration (III), there are two segments draining atoms away from the central via, and there is one unstressed segment. Consequently, the stress gradient present in the unstressed segment in configuration (III) would be much higher than that present in the unstressed segments in configuration (II). Therefore, the lifetimes for configuration (II) are longer than those for configuration (III) for Cu T-structure trees.

For configurations (IV) and (V), the ‘bottom’ and the right-hand-side segments serve as active atomic sources, similar to the scenario in configuration (3) in the dotted-I experiments (see Figure 4.2). As discussed in the previous section, when active atomic
sources are present, due to the low threshold for void nucleation in current Cu technology, voids not only could nucleate above the central via, but also would nucleate at the cathode-end vias of the active atomic source segments and subsequently increase the possibility for failure compared to the case in which only passive atomic reservoirs are present. The failure site statistics support this postulate (see Table 4.1), from which we can see that the majority of failures in configuration (IV) and (V) occur in the less stressed segments. Similar to the observations made using the dotted-I tree, the lifetimes for the configurations with active atomic sources are lower than those with passive atomic reservoirs for T-structure trees as well. Thus, configurations (IV) and (V) are less reliable than configurations (II) and (III).

Furthermore, configurations (IV) and (V) also compare the effect of the location of the active atomic sources on the overall reliability. In configuration (V), the left-most segment becomes 100\(\mu\)m long and the right-most segment becomes 400\(\mu\)m long. As a result, the probability of failures occurring in the right-most segment drastically increases, as shown in the failure site statistics comparisons shown in Table 4.1. This is because the stress development in a segment is directly proportional to the segment length. Therefore, in configuration (V), voids nucleate faster near the cathode-end in the right-most segment than in the bottom segment. Therefore, configuration (V) has a lower \(t_{50}\) than configuration (IV).
Table 4.1. Failure site statistics for the symmetric and asymmetric T-trees

<table>
<thead>
<tr>
<th></th>
<th>(a) symmetric T</th>
<th>(b) asymmetric T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Failure limb site</td>
<td>% of the total population</td>
<td>Failure limb site</td>
</tr>
<tr>
<td>LEFT</td>
<td>20</td>
<td>LEFT</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>45</td>
<td>BOTTOM</td>
</tr>
<tr>
<td>RIGHT</td>
<td>35</td>
<td>RIGHT</td>
</tr>
</tbody>
</table>

Fig. 4.6. Times-to-failure for 500μm-long, 0.30μm-wide T-structures with the different electron current configurations shown on the right. Tests were carried out at T = 350°C and $j_e = 2.5 \text{ MA/cm}^2$. Each arrow represents the electron flow direction, with a magnitude of $j_e$ except in configurations (IV) and (V), where the left most segment has a current density of 5.0MA/cm².
We can examine the effect of the ‘bottom’ segment as an additional atomic reservoir on reliability by comparing configurations (I), (II), and (III) in the T-structure experiments to configurations (1), (2), and (5) in the dotted-I tree experiments (see Figure 4.7, where these configurations are re-named using capital letters). Overall, we can conclude that there are no significant changes in the reliability when additional atomic reservoirs are present. This is illustrated by the comparison between the times-to-failure plots for configuration (F) with those of configurations (C) and (G). In the comparisons between configurations (A) and (D) with (B) and (E), the exact cause is unknown for the discrepancies in lifetimes, where configurations (D) and (E) are less reliable than (A) and (B), respectively. Nevertheless, our results suggest that the addition of atomic reservoirs to junctions will not improve the reliability of the junction. This is because the threshold for void nucleation is very low in Cu interconnects. Prior to void nucleation, i.e., stress relaxation in the atomic reservoirs, there is not enough time for stress development to cause appreciable atomic flux in the additional atomic reservoirs.

This conclusion is in agreement with Gan’s observation that the reliability of Cu interconnect trees is independent of the number of segments connected at the middle via [Gan 03]. In Gan’s experiments, the lifetimes for different types of Cu interconnect trees with the same current density through the middle via were recorded (see Figure 4.8). Figure 4.8 shows that the failure times are the same for dotted-I, T-shaped, and +-shaped interconnect trees when the central via is stressed at the same current density. Here, due to the low stress required for void nucleation in current Cu technology, the reliability of a via does not depend on the number of connected atomic drain segments, rather, it depends only on the stresses through the central via.
Fig. 4.7. Comparison of times-to-failures between T-structures and dotted-I trees. Here, the bottom segment in the symmetric T-structure serves as a passive atomic reservoir. In the illustration of the current density distributions on the right, each arrow corresponds to a current density of 2.5MA/cm² with the electrons flowing in the directions of the arrows.
Fig. 4.8. Schematic diagrams of Cu (a) dotted-I, (b) ‘T’, and (c) ‘+’ interconnect trees with the same current density of 5.0 MA/cm² flowing through the middle via. The arrows show the direction of electron flow and $j_t$, $j_r$ and $j_c$ are $2.5$ MA/cm², $1.67$ MA/cm² and $1.25$ MA/cm², respectively. (d) Times-to-failure for the different interconnect tree structures shown in (a), (b) and (c).

Lastly, we investigated the effect of segment length on the reliability of the T-structure interconnect tree (see Figure 4.9). We compared the reliabilities of the symmetric T-structure interconnect trees with $L=500\mu$m and that with $L=50\mu$m using the
current density configurations (a) and (b) shown in Figure 4.9. We can see that the
segment length has no clear effect on the reliability of the T-structure.

Fig. 4.9. Comparison of the effects of limb lengths on the reliability of the symmetric T-
structures. Here, the open points correspond to T-structures with L=50μm, and the solid
points for T-structure with L=500μm. Circles correspond to configuration (a), and
triangles correspond to configuration (b). (T=350°C, j_e=2.5MA/cm²)
4.2.3 Conclusions

Characterization of the reliability of dotted-I and T interconnect trees provides the background knowledge necessary to develop a via-centric circuit-level reliability assessment model. This model must be different from the analogous model used for Al interconnects (which is a tree-based model), due to the possibility of non-blocking vias and the low tensile stress required for void nucleation in current Cu technology. The consequences of these two effects in Cu trees have been shown in our experimental results in both the dotted-I and T structures. Through comparison between the Cu dotted-I and T-shaped tree structures, we see that active atomic sources reduce the reliability of a structure compared to inactive reservoirs. Also, atomic reservoirs do not improve the reliability of the structure. This suggests that a conservative void growth model, in which nucleation is assumed to be easy and no beneficial reservoir effects exist, should be employed in developing reliability assessment methods for Cu.
Chapter 5 SUMMARY AND FUTURE WORK

5.1 Summary

In order to reduce the RC delay for microelectronic devices, in recent years, Cu has become the metal of choice for IC interconnects, due to its lower resistivity than Al. However, failures caused by electromigration are still a grave reliability concern for current Cu-based interconnect technology. This concern will increase as the microelectronics industry progresses toward smaller feature sizes and more compact circuits. Understanding electromigration in Cu interconnects is crucial in the assessment of the reliability of circuits.

Cu has very different chemical properties from Al. Unlike Al, a reactive metal, Cu is a near noble metal that does not react with SiO$_2$ or SiN to form new compounds. In contrast, Al reduces SiO$_2$ and refractory metal over and underlayers to form low-diffusivity interfaces. Consequently, the fastest diffusion path in Al is along Al grain boundaries. In Cu interconnects, since Cu reacts very little with the surrounding materials, interfaces are candidates for fast diffusion paths. Specifically, experimental evidence has shown that the interface between Cu and the top capping layer, SiN, is the dominant path for diffusion in current Cu technology [Hau 01, Hau 02, Gan 01, Gan 02, Gan 02c, Hu 99, Arn 00, McC 00, Pro 00]. Furthermore, the low reactivity of Cu causes the Cu/SiN interface to have the lowest threshold for void nucleation [Hau 01]. The stress required for void nucleation in Cu systems is about 40MPa, which is extremely small compared to that for Al interconnects, 600MPa.
The properties of the Cu/Si₃N₄ interface profoundly affect the reliability of interconnects. The most direct effect is the lifetime asymmetry with respect to the electron flow direction [Gan 01, Gan 02c, Hau 01, Hau 02]. When electrons flow from a lower level to a higher level of metallization, as in our M2 test structures, the maximum tensile stress is reached at the base of the vias, where Cu is bounded by metallic liners on all sides. However, due to the low tensile stress required for void nucleation, voids preferentially nucleate at the Cu/Si₃N₄ interface rather than the Cu/Ta interface. After nucleation, the void will initially grow in the direction of the electron flow, resulting in a partially spanning void. An open-circuit failure will result only when the void grows to span the whole thickness of the metal line. On the other hand, when electrons flow from a higher level to a lower level of metallization, as in our M1 test structures, the maximum tensile stress develops at the Cu/Si₃N₄ interface near the vias in the lower metallization layer. Therefore, voids nucleate and grow directly beneath the cathode-end via. Unlike Al interconnects, there is no refractory metal layer in Cu technology that can shunt electron flow around small-volume voids at the base of a via. As a result, an open-circuit failure can occur when a small-volume void forms below the cathode via, such that the pathway for electron flow is blocked. This difference in void volume required for failure results in a difference in lifetimes for interconnects having different directions of electron flow with respect to the cathode via.

Related to the lifetime asymmetry mentioned above is the reliability behavior at short lengths for Cu interconnects. In M1 structures, the void volume required for failure is small compared to that required for M2 structures. Therefore, the reliability for M1 structures is dominated by void nucleation. On the other hand, failures in M2 structures
require fully-spanning large-volume voids. Therefore, the reliability for M2 structures is
governed by void growth and the back stress that develops in an interconnect segment
can oppose the electron wind force for electromigration. Because of this difference, the
experimental observations for the \((jL)_{critical}\) values for immortality mode using the two
different types of interconnects are different. Hau-Riege has found the \((jL)_{critical}\) value for
M1-type interconnects to be less than 2100A/cm [Hau 01, Hau 02]. This value is an
upper bound for the reliability of M1-type interconnects because a minor fraction of the
total population failed at lower \(jL\) values, when very small voids spanned the base of the
cathode via. Whether or not a void leads to failure depends on its location and shape. In
contrast, Ho et al. have estimated a lower bound for \((jL)_{critical}\) for M2-type interconnects
segments of 3700A/cm [Oga 01, Lee 01], which corresponds to immortality due to void
growth saturation.

In studying the behavior of Cu interconnects at very long lengths, we observed
multi-modal failure distributions, in which a fraction of the lines appeared to be
'immortal' [Wei 02]. We propose that the apparent immortality of a sub-population of
long lines is the result of rupture of the Ta liners at the vias caused by the high stresses
developed during electromigration. Such a rupture would allow continuous flow of Cu to
and from the connector lines and contact pads, therefore causing the apparent lifetime to
increase dramatically.

As a result of the complexity of the electromigration behavior in Cu
interconnects, conventional lifetime measurements are not sufficient to capture the
fundamental kinetics of electromigration-induced failure. However, drift velocity
measurements can provide fundamental information for the kinetics that precedes various
failure modes. We developed a set of methods to estimate the electromigration drift velocity using fully processed Cu interconnects. Unlike in-situ observations on Blech-like structures, the top mechanical constraint is not compromised in our study. We monitored the resistance increase prior to failure in both M1- and M2-type interconnects. By assuming small-volume void growth below the cathode via in M1-type interconnects and fully spanning void growth in M2-type interconnects, we correlated the rate of the resistance increases to the rate of void growth, i.e., the drift velocity [Wei 03]. We found the activation energy for electromigration-induced void growth in Cu interconnects to be 0.80±0.06eV, and also found that the drift velocity scales approximately linearly with current density, as expected from the Nernst-Einstein relationship (the measured current density exponent is 1.1±0.3). Our results are in agreement with literature reports as well as results obtained from the lifetime measurements on the same samples.

In order to better understand how to apply the phenomenology observed in two-terminal Cu test structures to the analyses of the reliability of interconnects in real circuits, we investigated electromigration-induced failures in multi-segmented tree structures. More specifically, we investigated the reliability characteristics of the dotted-I, symmetric T, and asymmetric T tree structures. We found that the reliability of an individual segment in an interconnect tree is dependent on the direction and magnitude of electron flow in neighboring segments [Gan 02]. Therefore, the conventional circuit-level reliability assessment approach of carrying out analyses by analyzing the reliability of individual segments is not accurate. From comparisons of the results of Cu dotted-I trees to those of Al dotted-I trees, we found their behaviors to be different. Their differences are attributed to the low void nucleation threshold and the possibility of non-
blocking vias in current Cu technology. Through the reliability characterization of T-shaped trees, we found that additional atomic reservoirs would not increase the reliability of a junction, and segment length does not have a significant effect on the reliability characteristics of Cu interconnect trees.

5.2 Implications of Results

Our findings that indicate the possibility of non-blocking vias implies that the reliability of an individual segment may depend on the stress conditions in neighboring segments in different metallization levels, so that interconnect trees are not the fundamental reliability units in current Cu metallization schemes. This conclusion points to the need for a via- or junction-based reliability assessment model for Cu interconnects. Such a tool would incorporate our finding on the complex behavior as well as the fundamental kinetics of electromigration in Cu interconnects. Quantitative analyses of the experimental results on the dotted-I and T-shaped trees would lead to the development of such a model.

5.3 Future Work

Low-K materials are being substituted for SiO₂ as inter-level dielectric materials in order to further reduce the R-C delay [ITRS 01]. In low-k materials, the reduction in the dielectric constant is achieved in a number of ways: reducing the density of Si-O covalent bonds by introducing H- or organic- (such as methyl-) terminating groups, creating nano-pores in the SiO₂ network, or replacing SiO₂ entirely with polymeric materials. In addition to the difficulties introduced during processing, low-K materials
pose as a huge reliability assessment challenge as well. This is because the mechanical properties of the low-K materials are not known in detail, though generally the reduction in mechanical integrity accompanies the reduction in dielectric constant. As a result, it has been reported that the electromigration behavior in Cu/low-K systems is different from that in Cu/SiO₂ interconnects [Lee 02]. The mechanical properties affect the stress evolution inside interconnect segments, and therefore affect the circuit-level reliability characteristics as well.

Mechanical characterization is the key to understanding the impact of low-K materials on interconnect reliability. Several experimental approaches should be pursued in parallel. First, we can study the thermomechanical properties of a given low-K material using wafer curvature measurements through a temperature cycle. Second, we can estimate a low-K thin film/substrate systems' mechanical properties using nano-indentation techniques. Third, we can determine low-K film properties by fabricating free-standing cantilever beams. These experimental techniques and finite element modeling would enable us to predict the mechanical response of the Cu/low-K system. Thus, we can develop circuit-level reliability assessment tools for Cu/low-K interconnect systems. During this process, we should pay close attention to mechanical characterization of low-K materials that are viscoelastic, whose mechanical response depends on temperature and stress history. Finally, all predictions could be confirmed by performing electromigration stress experiments using fully processed Cu/low-K interconnect segments and trees, followed by failure analyses.
Bibliography


