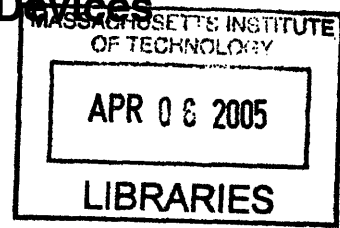# Towards In-Situ Device Fabrication: Electrostatic Lithography and Nanowire Field Effect Devices

by

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B.Tech. Ceramic Engineering
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SUBMITTED TO THE DEPARTMENT OF MATERIALS SCIENCE AND
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Towards In-Situ Device Fabrication: Electrostatic Lithography and Nanowire Field Effect Devices.

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Abstract

Electron beams were used to deposit fine line-width charge in electret materials. The electrets were exposed to charged or polarizable nanoparticle precursors. These nanoparticles decorate the charge pattern. Electret materials including Mylar, Polyamide and Teflon were used for this process. Nanoparticles used ranged from carbon black, gold, silver, iron oxide, aluminum oxide and silicon oxide. Multiple nanoparticle delivery methods were employed including immersion in a nanoparticle solution, exposure to a nanoparticle aerosol, electrosprayed nanoparticles and in-situ delivery of nanoparticles. The technique was adapted to produce the fastest known electron beam resist with exposure dosage as low as 10 nC/cm^2. We have termed the new resist an electrostatic resist and the technique electrostatic lithography.

A novel technique to fabricate logic elements from semiconducting nanowires grown using vapor-liquid-solid mechanism was also developed. The technique involves source, drain, gate-oxide and gate material fabrication using electron beam induced chemical vapor deposition. Field effect transistor and ring oscillator architectures were fabricated using this process. Nanowires were characterized using scanning electron microscopy and transmission electron microscopy. Current-voltage measurements were performed on the nanowire field effect transistors.

Thesis Supervisor: Joseph Jacobson
Title: Associate Professor of Media Arts and Sciences

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Without Mike Houlihan, our group would have been dysfunctional. Thanks Mike, for keeping it all together. Materials Science graduate administrators, Kathleen Farrell and Steve Malley are deeply thanked for helping me coast through the rigors of graduate student life.

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exposed to potassium, to convert the region in the window to n-CNT-FET, while other remains p-type [9]. 65

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1 Introduction

Presently there is great interest in the fabrication of functional semiconductor devices with length scales below 100 nm, i.e. nanoelectronics. The laws of physics allow, in theory, the building of logic devices such as transistors with characteristic length scales on the order of about 1 nm. Reaching these limits, however, is difficult and expensive.

Methods for fabricating devices below 100 nm include both top down and bottom up approaches. Conventional top down approaches such as photolithography or electron beam lithography utilize formation and selective removal of various levels to form functional devices. Top down processes are very expensive for devices with features below 100 nm. In addition, such methods can generally be used only to build two-dimensional logic, typically on a planar silicon wafer, and historically have followed Moore's law yielding only a factor of two increase in device density every 18 months.

Direct-write top down approaches have included atomic force microscopy (AFM) direct writing of liquids, i.e. dip pen nanolithography and scanning tunneling microscopy (STM) writing of oxides and charge replicas. These methods suffer from slow speeds, lack of a general set of building materials for fabricating electronic components, and a constraint to two-dimensional structures.

Tools for creating three-dimensional structures employ, for example, electron beam and ion beam decomposition of chemical vapor precursors. Such tools have been useful in

mask and chip repair and have been shown to be capable of writing three-dimensional structures. Typically, organometallic precursor gases adsorbed onto substrate surfaces are decomposed using energy supplied from incident beams, depositing the desired metal or insulator. This technique facilitates deposition of nanometer- to micrometer-size structures with nanometer precision in three dimensions and without supplementary process steps such as lift-off or etching procedures. Moreover, this deposition method does not generally require the high temperatures typically used in silicon processing. Although successful in creating high-resolution three-dimensional structures, both scanning electron microscopy (SEM) and focused ion beam (FIB) chemical vapor deposition (CVD) suffer from significant contamination by the organic components of the precursor gas. Carbon contamination from typical precursor gases can exceed 50%, thus altering device conductivities to levels unacceptable for many desired applications. Device fabrication by energetic-beam CVD is also constrained by an inherently small number of available precursor gases, thus limiting the variety of materials that can be deposited. Finally, because existing processes are serial and sufficient beam energy must be applied to decompose the precursor, deposition speeds are very slow.

In bottom up approaches, layers are selectively applied to (rather than removed from) a substrate. For example, nano-scaled building blocks, like nanowires, nanotubes, nanoparticles etc., synthesized precisely by chemistry or other methods may later be assembled by, e.g., self-assembly.

Nanowires and nanotubes have attracted a lot of attention in recent years. The unique properties of one-dimensional structures like nanowires and nanotubes make them attractive as building blocks for future nano-devices. Semiconducting nanowires and carbon nanotubes have been proposed as building blocks for future electronic and photonic devices. These materials exhibit diverse electronic behavior, whereby they can be used as the semiconducting component of a device and simultaneously act as interconnect wires. They would help shrink both gate lengths and interconnect dimensions. The kind of mobilities that have been achieved in nanotubes is also much more than in bulk. However, to date nothing much more complex than a FET, diodes, laser diodes have been fabricated. To achieve complexity there is a need for a better assembly technique for these nano building blocks.

This work demonstrates novel assembly and functionalization techniques for nanoscale building blocks. For nanoparticles and nanoclusters, electrostatics directed assembly is further developed. This work also led to the development of a new lithography technique based on electrostatics, termed as "Electrostatic Lithography". Electrostatic lithography is the fastest electron beam process that currently exists. It requires electron beam doses as low as $10nC/cm^2$, which is at least 10 times smaller than the fastest commercial resist.

Energetic beam induced chemical vapor deposition (CVD) process is used to develop the least laborious process for fabricating logic devices using nanowire and nanotube building blocks. This process overcomes difficulties faced by conventional electron beam

lithography processes used to do the same work. Energetic beam CVD, thus provides a technique for fabricating the most complex nanowire / nanotube logic devices.

The thesis is divided into five chapters. Chapter 2 discusses synthesis and delivery schemes for nanoscale building blocks. In chapter 3, the use of electrostatics in nanoparticle assembly is discussed. Chapter 3 also talks about the development of electrostatic lithography. Functionalization of nanowire building blocks is discussed in chapter 4. Finally, chapter 5 summarizes and discusses future direction of work.

2 Building Blocks – Nanoparticles and Nanowires

The increasing difficulty, both technically and economically, to continue along the Moore's Law using conventional top-down fabrication techniques like optical lithography has led researchers to explore alternative fabrication schemes. Much interest has been generated in performing bottom-up fabrication. Bottom-up fabrication involves directing the assembly of nanoscale building blocks like nanowires, nanotubes and nanoparticles. This chapter details the synthesis and delivery schemes for nanoparticle and nanowire building blocks.

2.1 Nanoparticle Building Blocks

The most advanced techniques for nanoparticle / nanocluster generation includes metal evaporation, laser ablation, solution vaporization, wire explosion, pyrolosis, colloidal and electrochemical synthesis and generation from plasmas. Currently a wide variety of nanoparticles are commercially available. It is possible to synthesize metallic, semiconducting or insulating nanoparticles. As discussed in subsequent chapters, these nanoparticle building blocks were functionalized using energetic beams. The nanoparticles used in this work were mostly commercially obtained. In one of the schemes however, the nanoparticles were generated in-house, using a nanocluster-sputtering source. Different techniques were then developed to deliver these nanoparticles to the substrate of interest. This chapter provides details on the melting point depression in nanoparticles, synthesis using nanocluster source and nanoparticle delivery schemes.

2.1.1 Size Dependent Melting Point Suppression:
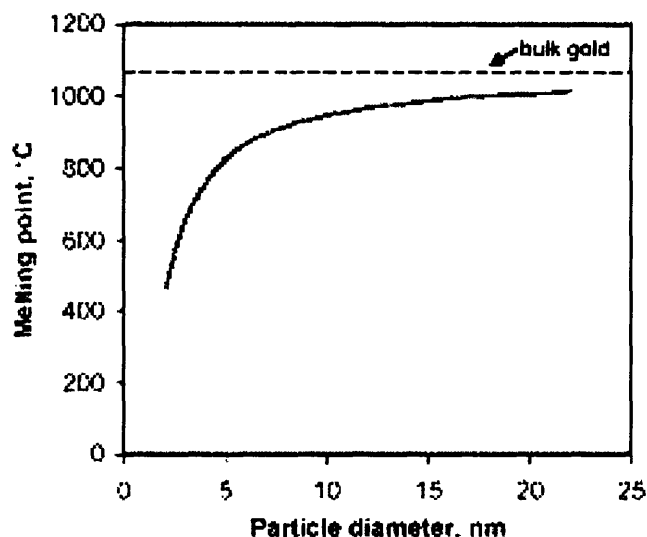
Figure 2.1: Melting point of gold particles as a function of diameter [1].

It is now widely know that almost all nanoparticles, with the exception of tin, melt at much lower temperatures than their bulk counterparts [1]. Recently this property has been utilized in direct fabrication of devices and MEMS from nanoparticle precursors [12], [13]. Small particles have lower melting point than bulk material. The physical cause lies in the fact that small particles have a higher proportion of surface atoms than larger particles – surface atoms have fewer nearest neighbors and are thus more weakly bound and less constrained in their thermal motion than atoms in the body of a material. A linear reduction of the melting point as a function of the inverse cluster radius is observed. Figure 2.1 shows the melting point suppression affect in gold [1].

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The melting point of small particles is not only of scientific interest, but also has some technological implications. In sintering processes, fine powders are compressed and heated until they coalesce. If extremely fine powders are employed, a lower sintering temperature could be used. Also, the present drive towards nanoscale technology leads to smaller and smaller geometric dimensions with a reduction of and consequently reduced electrical and mechanical stability at elevated temperatures.

2.1.2 Nanoparticle Delivery Scheme

There is a lot of interest in making devices of importance using nanoparticles as building blocks. However, it has been difficult to develop a scheme for easy pick and place of nanoparticles. In this section, solid, liquid and gaseous suspension schemes for the delivery of nanoparticles are described.

2.1.2.1 Solid Nanoparticle Suspension

This is the simplest of the three schemes. Commercially obtained metal and insulating nanoparticles such as silver, aluminum oxide, silicon oxide etc. are directly applied to substrates of interest. The substrate was immersed into a heap of these nanoparticles for an optimized duration of time. Details of how these nanoparticles decorate the substrates would be provided in subsequent chapters. Figure 2.2 shows substrate immersed in nanoparticle powder heap.
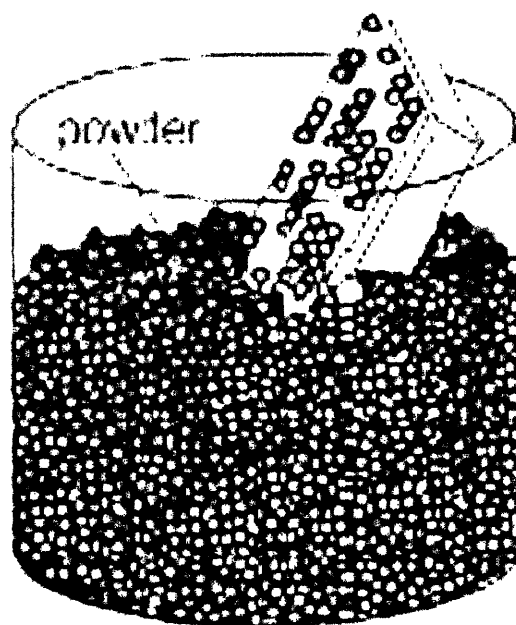
Figure 2.2: Substrates of interest are immersed in a nanoparticle powder heap for an optimized duration of time [2].

2.1.2.2 Liquid Nanoparticle Suspension

Again in this scheme, commercially obtained metallic and insulating nanoparticles were used. These nanoparticles were dispersed in a non-polar solution. Non-polar solutions such as Isoparrafin, hexane etc. were used as the dispersing solvent. The solution was then ultrasonicated to uniformly disperse the nanoparticles in the solution. Ultrasonication also breaks down nanoparticle agglomerates into individual nanoparticles. Figure 2.3 shows a schematic of nanoparticles dispersed in a hexane solvent.
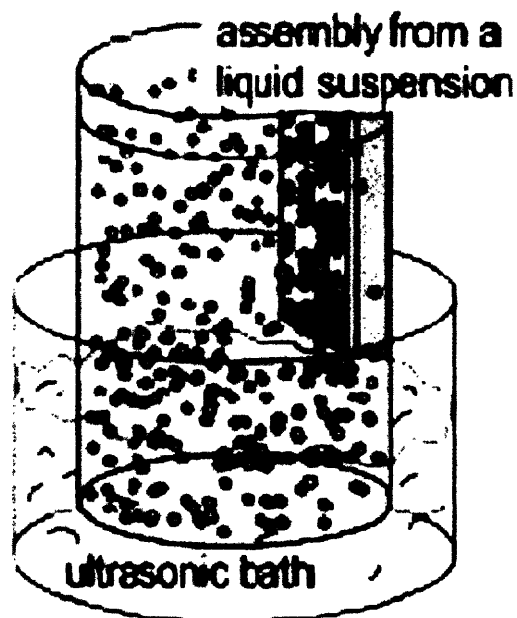
Figure 2.3: Nanoparticles dispersed in a non-polar solvent. The solution is ultrasonicated to uniformly disperse the nanoparticles and also to break down agglomerates [2].

2.1.2.3 Gaseous Nanoparticle Suspension

In this scheme, nanoparticles are suspended in a carrier gas. This was achieved by using a nanocluster source, an electrospray source and a nanoparticle aerosol. Nanocluster source both generates and suspends the nanoparticles is a carrier gas. For the electrospray source and the nanoparticle aerosol source, commercially available nanoparticles were employed. This section details the mechanism of each of these sources.

Nanocluster Source

Oxford Applied Research's nanocluster source NC200U and quadrupole mass filter QMF200 (Figure 2.4) were used to generate mass selected metallic and semiconducting nanoparticles. The core of the source is a DC magnetron, which is used to sputter

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material into a water-cooled, high-pressure aggregation/ drift region. The clusters formed in this region and are then channeled though apertures into the quadrupole mass filter. The quadrupole mass filter includes ion steering plates on the exit aperture to steer the mass selected clusters off axis to the neutral beam. These mass selected clusters are then channeled into the deposition chamber. Figure 2.5 shows a schematic of the nanocluster source.

The cluster size can be adjusted by varying three main source parameters: the length in which the clusters aggregate, the power to the magnetron and the flow of the aggregation gas. For a large number of materials the source is capable of producing clusters consisting of a few tens of atoms up to particles with diameters greater than 10nm. It is also capable of depositing at rates between <0.001nm/s and >0.5nm/s (measured at a distance of 100mm for Cu clusters). The deposition rate achieved depends on a number of parameters, which includes the material, and the size of clusters deposited.

A large percentage of the clusters generated by the source are ionized (typically 40% for Cu clusters). An ionised beam can be accelerated towards a substrate to form highly adherent and uniform coatings. In our scheme, the ionized clusters are electrostatically manipulated in the deposition system. Also the nanoclusters generated were determined to be monocrystalline in nature. Figure 2.6 is a TEM micrograph of silicon nanoclusters, showing that the clusters were single crystal in nature. TEM was also performed on copper nanoclusters and they were shown to be monocrystalline as well [11].
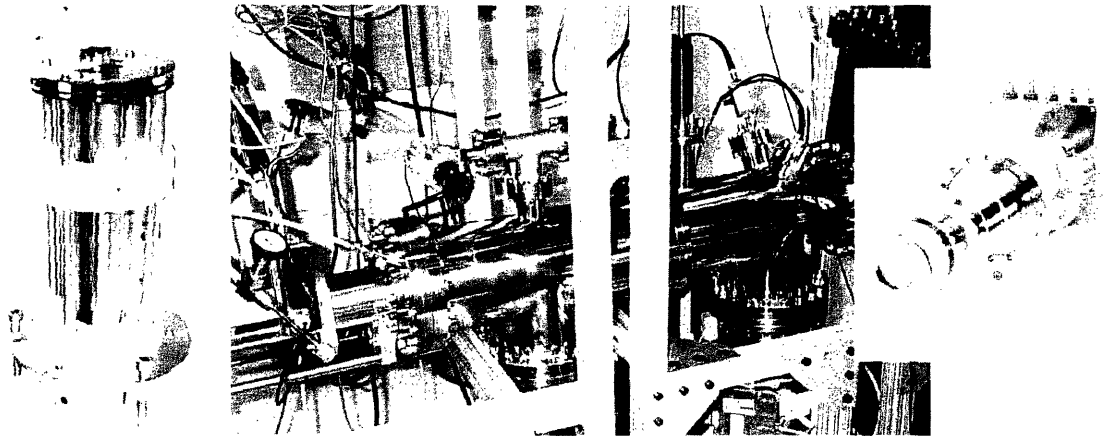
Figure 2.4: The center pictograph shows the NC200U nanocluster source and the QMF200 quadrupole mass filter. The right pictograph shows the DC Magnetron of the nanocluster source. The left pictograph shows the details of a quadrupole mass filter (courtesy David Kong).
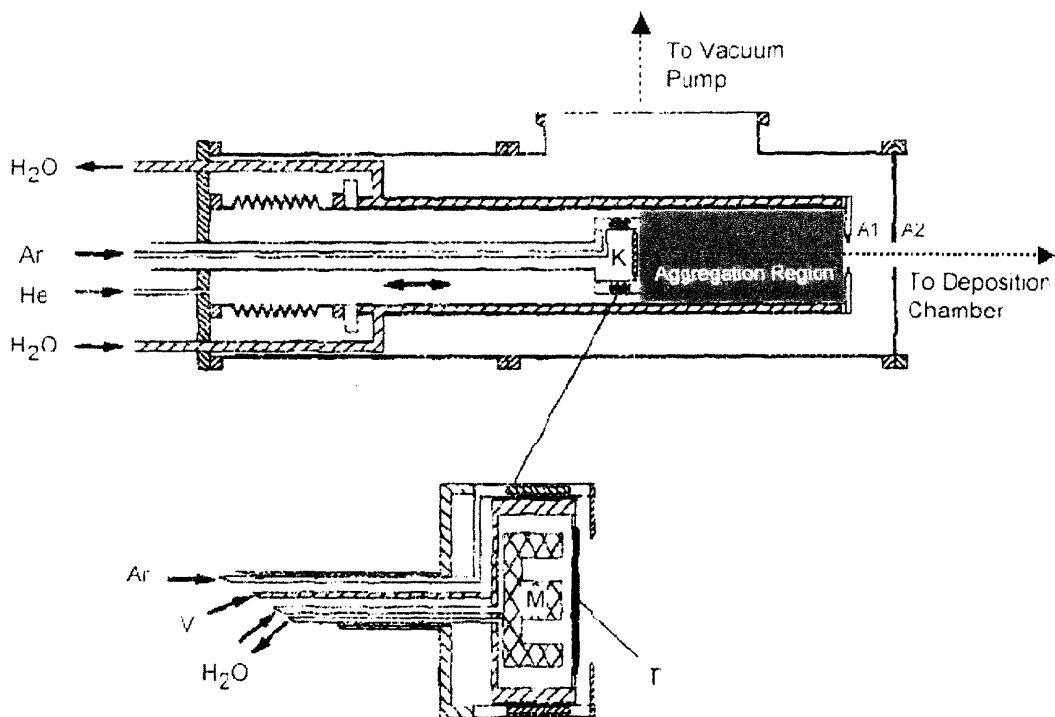
Figure 2.5: Schematic of the nanocluster source [14].

Figure 2.6: TEM image showing silicon cluster deposited using the nanocluster source (courtesy Oxford Applied Research).

Nanoparticle Electrospray Source

Electrospray atomization is based on the formation of conical spray at the interface between a conducting liquid and a surrounding dielectric medium, generally a gas. Under optimized conditions, the cone tip emits a microscopic jet that then breaks into an aerosol [15]. Drops of initial diameters as small as 20 nm can be produced from high conductivity solutions. Their drying then can produce particles a few nanometers in diameter. Some of the most novel uses of electrospray thus is for nanoparticle science and technology. Figure 2.7 shows the schematic of an electrospray source. In our experimental setup the capillary was filled with 5nm size silver nanoparticles (obtained from Nanophase) dispersed in toluene. The liquid was forced into the needle with the help of a syringe pump at a pumping speed of ~3µl/sec. The initial droplet size depends upon the diameter of the needle used. The finer the needle diameter the smaller was the initial droplet size. Needles of different diameters were tested in this work. In the ultimate setup a needle of 250µ inner diameter was used. The problem with very fine needles was

that the nanoparticle solution could clog them. In order to prevent this, the needles were washed with pure toluene after each run. A high voltage of about ~2KV was applied to the needle. The size of the droplets also depends upon the voltage applied to the needle. For our setup ~2KV was found to be an optimal voltage corresponding to the 250µ diameter needle. The extractor is kept at a much smaller positive potential. With such a setup positively charged droplets containing silver nanoparticles were extracted. The solution in the capillary could be replaced with other nanoparticle solution to generate droplets containing other nanoparticles.
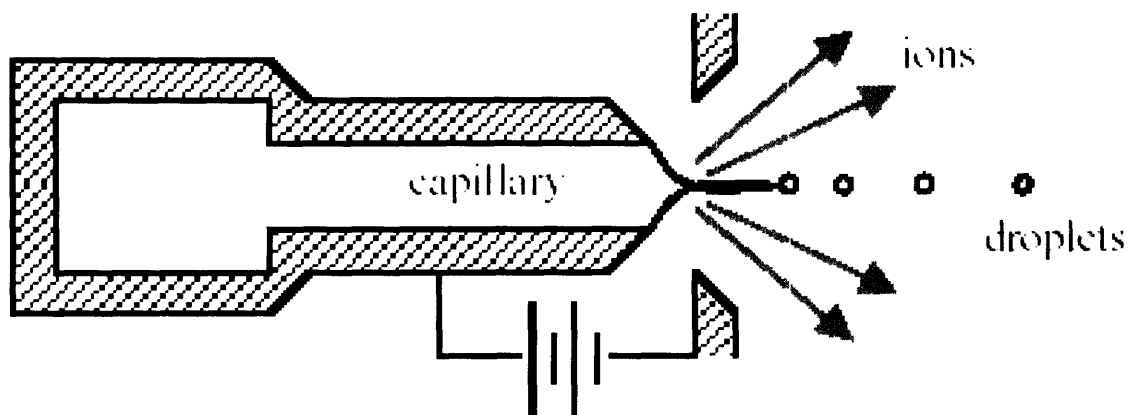
Figure 2.7: Schematic of an electrospray source used to generate positively charged droplets of silver nanoparticles [3].
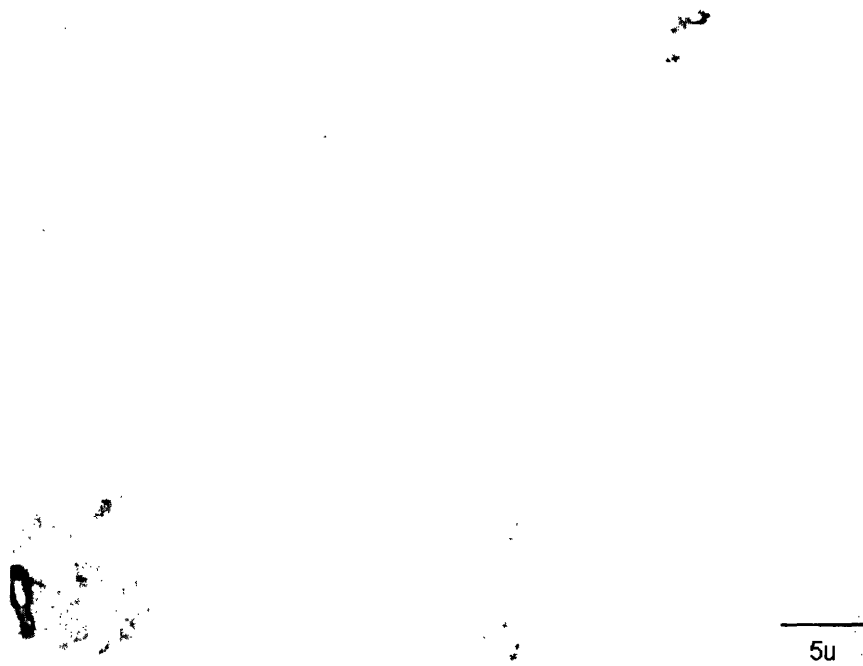
Figure 2.8: Optical micrograph showing electrosprayed silver nanoparticle droplets on a glass substrate. The potential on the needle was ~2KV.

Nanoparticle Aerosol

Commercially obtained nanoparticle powder was suspended in air using either a high frequency piezoelectric disc or by a pressurized air jet. In the first method, the nanoparticle powder heap was placed on top a high frequency piezoelectric disc. The disc was powered up and vibrated. The vibrations cause the nanoparticles to become air borne, thereby generating an aerosol. In the second method, pressurized air was blown into the nanoparticle powder heap to make the nanoparticles airborne, leading to an aerosol.
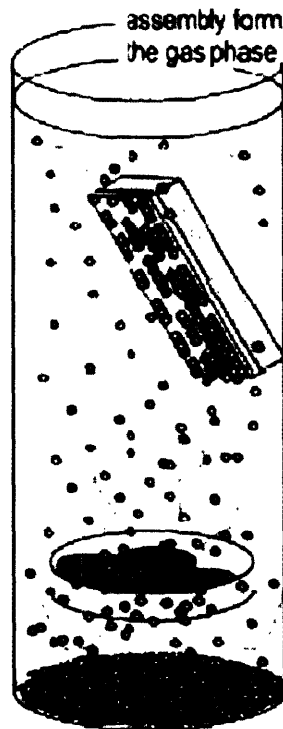
Figure 2.9: Schematic demonstrating a methodology to generate a nanoparticle aerosol by blowing pressurized gas.

2.2 Nanowire Building Blocks

Since the discovery of carbon nanotubes in 1991 by Iijima [16], in the soot at the negative electrode of an arc discharge, there has been wide interest in one-dimensional structures. Carbon nanotubes have diameters as small as 0.4 nm and lengths up to a million times their diameter. With their remarkable electrical properties, simple electronic logic circuits have been fabricated. These structures are promising for usage in miniaturizing semiconductor devices. Depending on the chirality of the tubes, carbon nanotubes can be metallic or semiconducting. There are still no controlled growth procedures that produces only semiconducting or only metallic nanotubes. Nanotube

bundles are a heterogeneous mix of metallic and semiconducting nanotubes. The easiest way to test which one is which remains difficult. It would involve similar procedures, as for CNT-FETs, to contact the tubes with metal electrodes and then test their conductivity. Fabricating p-n junctions, or any other junction, is quite complicated as well [17].

The synthesis of crystalline semiconductor nanowires, like Si, Ge and GaAs, is promising for device applications. These semiconducting nanowires can overcome a lot of problems that carbon nanotubes face. Most importantly being able to synthesize only semiconducting or only metallic wires, as required. Since both semiconducting and metallic components can be reliably produced as one-dimensional structures, device made out of these components could be greatly miniaturized. In such a device, semiconducting components could be used to perform logic functions, while metallic components could be used as interconnects. Several successful routes for the synthesis of carbon nanotubes are known, but the different chemistry of carbon compared with Si and Ge would require an alternative approach for controlling the formation of nanowires from gas-phase reactants [18].

This section of nanowire building blocks details on some unique properties of nanowires, their synthesis methods and the delivery schemes developed.

2.2.1 Nanowire Synthesis – Vapor Liquid Solid Method

Vapor-liquid-solid mechanism of anisotropic crystal growth is one of the most popular methods to synthesize semiconductor nanowires. This mechanism was first proposed for the growth of single crystal silicon whiskers 100nm to hundreds of microns in

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diameter[19]. Growth of nanowires using VLS involves the absorption of source material from the gas phase into a liquid droplet of a catalyst. A molten particle of gold on a silicon substrate was used as a catalyst in the original work[19]. Disproportionation of SiI_2 or hydrogen reduction of $SiCl_4$ was used to provide the silicon source material from the gas phase. Upon supersaturation of the liquid alloy, a nucleation event generates a solid precipitate of the source material. This seed serves as a preferred site for further deposition of material at the interface of the liquid droplet, promoting the elongation of the seed into a nanowire or a whisker, and suppressing further nucleation events on the same catalyst. Since the liquid droplet catalyzes the incorporation of material from the gas source to the growing crystal, the deposit grows anisotropically as a whisker, whose diameter depends on the diameter of the initial liquid alloy droplet. The nanowires thus obtained are of high purity, except for the end containing the solidified catalyst as an alloy particle. Real-time observation of the alloying, nucleation and elongation steps in the growth of germanium nanowires from gold nanoclusters by the VLS method has been recorded by in-situ TEM[20].

Reduction of the average wire diameter to the nanometer scale required the generation of nanosized catalyst droplets. However, due to the balance between the liquid-vapor surface free energy and the free energy of condensation, the size of the a liquid droplet, in equilibrium with its vapor, is usually limited to the micrometer range. In recent years, this obstacle has been overcome by several new methodologies: 1) Advances in the synthesis of metal nanoclusters have made monodispersed nanoparticles commercially available. These can be dispersed on a solid substrate in high dilution so that when the temperature

is raised above the melting point, the liquid clusters do not aggregate[21]. 2) Alternatively, metal islands of nanoscale sizes can self-form when a strained thin layer is grown or heat treated on a non-epitaxial substrate[22]. 3) Laser-assisted catalytic VLS growth is a method used to generate nanowires under non-equilibrium conditions [18]. 4) Also, by the optimization of the material properties of the catalyst-nanowire system, conditions can be achieved for which nanocrystals nucleate in a liquid catalyst pool supersaturated with the nanowire material [23].

2.2.2 Nanowire Synthesis – Experimental

GaAs nanowires were grown using the vapor-liquid-solid (VLS) mechanism using gold as the catalyzing agent. Details of the growth process are provided in this section.
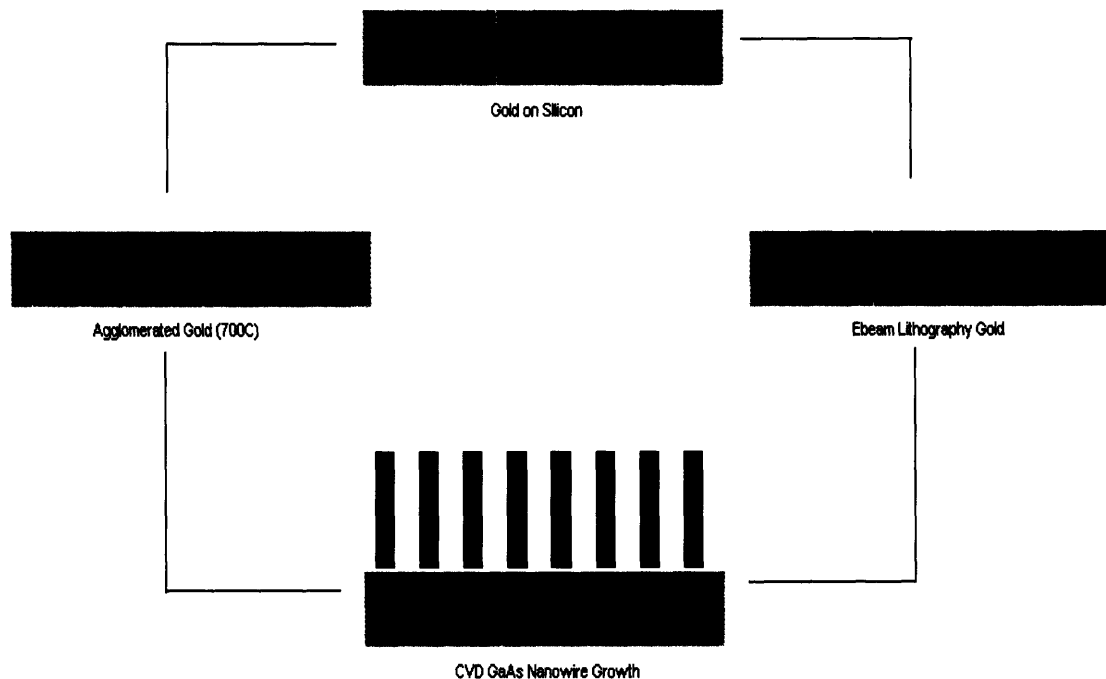
Figure 2.10: Schematic diagram, showing two different routes for the synthesis of nanoscale catalysts and subsequent nanowire growth.

2.2.2.1 Nanoscale Gold Catalyst Synthesis

Oxide on silicon was used as the base substrate for nanowire growth in all of this work. And gold was used to catalyze the growth of nanowires. Two different methodologies were adopted to obtain nano-sized gold droplets (Figure 2.10). In the first method, gold was thermally evaporated directly on the oxide on silicon substrate. The thickness of the film was monitored using a quartz crystal monitor (QCM) and was kept under 20 nanometers. This thin film of gold was thermally annealed at 600C for 80 minutes to obtain isolated nano-sized gold droplets. The final diameter of these droplets is determined by the initial thickness of the deposited film.

In the second method, PMMA was spin-coated on an oxide on silicon wafer at a speed of 1000 rpm for 15 seconds initially, followed by a speed of 2500 rpm for 60 seconds. Wafer with the PMMA film on it was then heated at 170C for 15 minutes. The 4-inch wafer was cut into smaller dies, which were easier to work with. Electron beam lithography was performed on these PMMA coated oxide on silicon dies. The exposure pattern was an array of different diameter dots. The exposure pattern controls the final diameter of the gold dots. The electron beam exposure conditions used were – accelerating voltage of 30 KV, spot size 2, working distance of 7 cm and charge dosage of 170μc/cm^2. The exposed die was then developed in 1:1 MIBK:IPA solvent for 1-2 minutes followed by an IPA rinse. Nitrogen was then used to blow-dry the die. This development procedure exposes the oxide on silicon, which was previously coated by PMMA. Using thermal evaporation, a thin layer (~20nm) gold was deposited on the die. Gold gets deposited on the PMMA and also on the exposed oxide wafer. This was

followed by an acetone dip. Acetone strips the PMMA along with the gold, which was deposited on it leaving behind only the gold that was deposited on the bare oxide. This produces a gold dot array on the bare oxide (Figure 2.11).
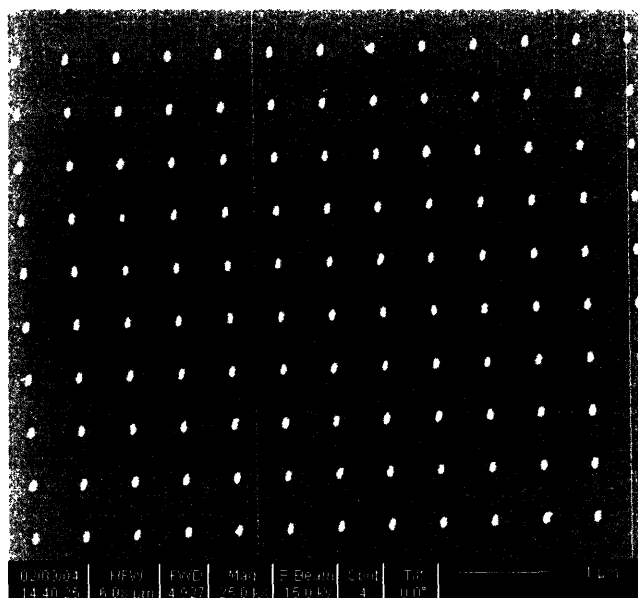
Figure 2.11: An array of gold nanoclusters produced using electron beam lithography over an oxide on silicon wafer.

2.2.2.2 Nanowire Growth

After the gold cluster formation process, the substrate was placed in a Chemical Vapor Deposition (CVD) chamber. The temperature of the substrate was raised to 700C and AsH$_3$ was introduced in the chamber when the temperature is 350C. The substrate was kept at 700C for 5 minutes and then the temperature was lowered to 420C. Gold catalysts break the CVD precursor gases, leading to nanowires growth. The temperature was maintained at this value for nanowire growth. The growth duration determines the length of the nanowires. Figure 2.12 shows a schematic of the growth process.
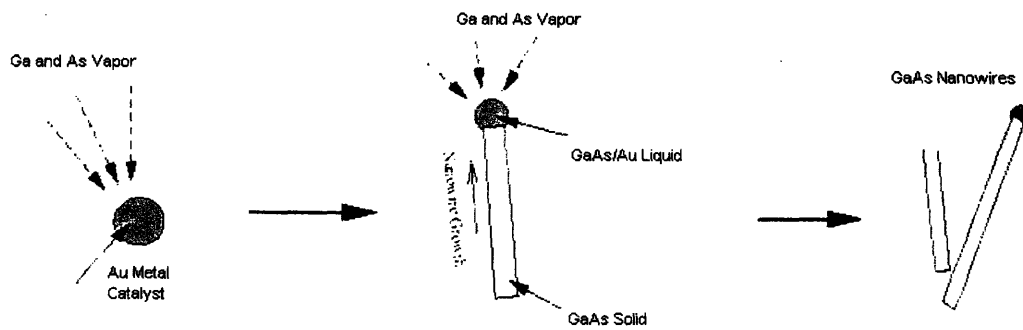
Figure 2.12: Gold metal drops catalyzing gallium and arsenic vapors leading to nanowire growth.

2.2.2.3 Nanowire Lift-off

The substrate with the nanowires grown on it was then ultrasonicated in isopropyl alcohol (IPA) for five minutes. This releases the nanowires from the substrate into IPA. A solution having a random nanowire distribution was finally obtained (Figure 2.13).
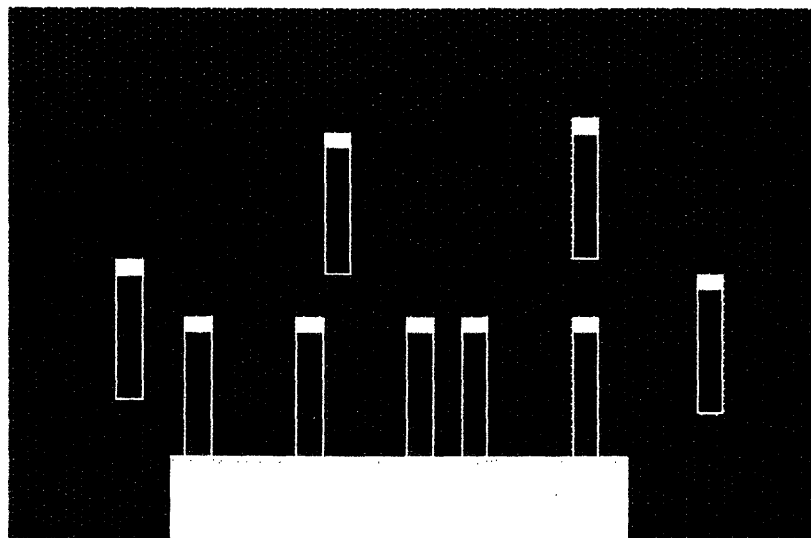
Figure 2.13: Schematic showing nanowire grass on the oxide on silicon was lifted-off by Ultrasonicating it in IPA.

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2.2.3 Nanowire Characterization

2.2.3.1 Scanning Electron Microscopy

Figure 2.14 shows scanning electron micrographs of GaAs nanowires, which were grown using different sized initial gold catalysts and were also varied in their growth times. Greater growth times increase the length of the nanowires.

2.2.3.2 Transmission Electron Microscopy

For improved semiconducting properties, it was essential that the nanowires were single crystal. TEM analysis of nanowires was done to determine their structure. Figure 2.15 shows the TEM image of a single nanowire. It shows that the core of the wire is crystalline and is covered by a sheath of amorphous material. The core is single crystal GaAs and the amorphous material forming the sheath is its oxide. Figure 2.16 is a selective area diffraction pattern performed on the core on the nanowires. The SAD again shows that the core of the nanowires was crystalline (Figure 2.16).
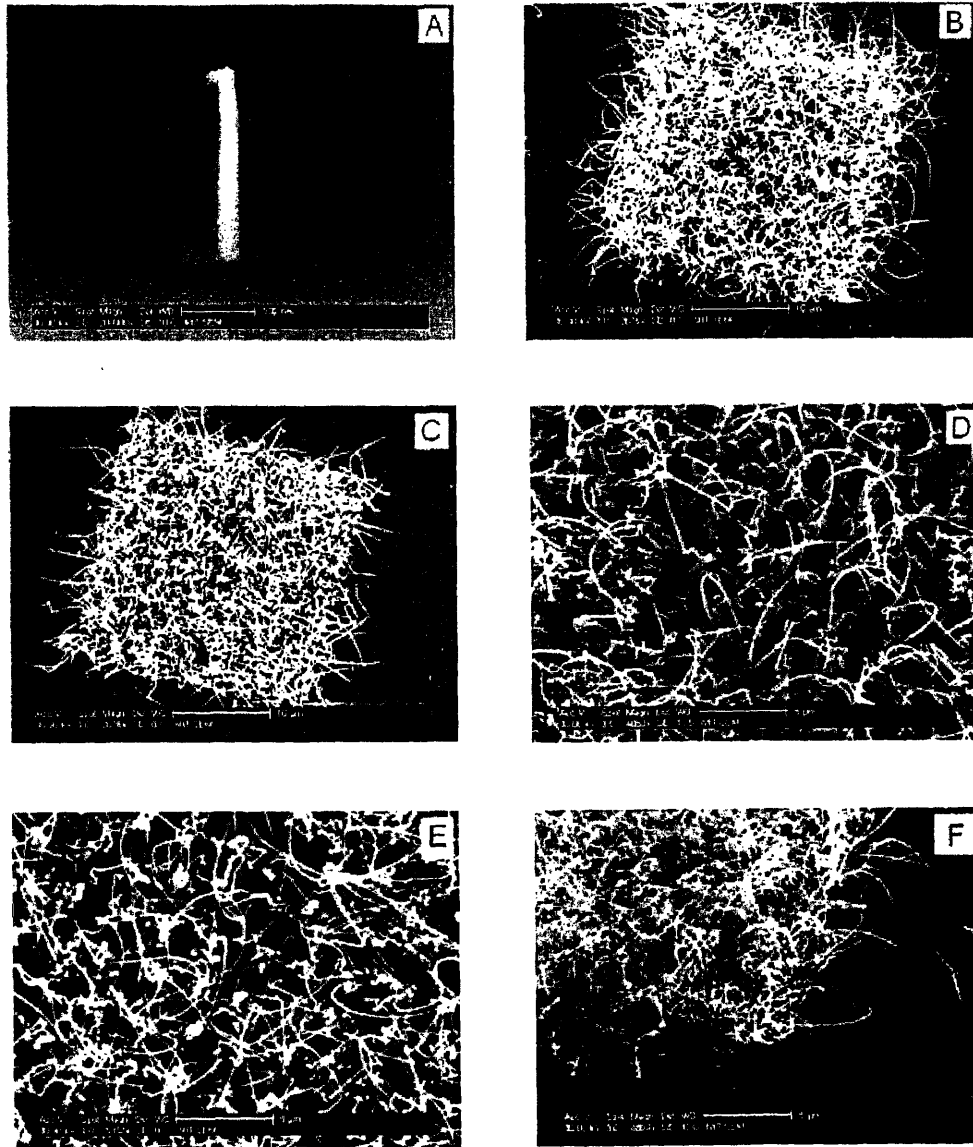
Figure 2.14: Scanning Electron Micrographs of GaAs nanowires grown on oxide on silicon substrates using VLS method. The catalyst used was gold. Different images correspond to different initial catalyst size and different growth durations. (A) 10min growth (B) 45min growtt-25nm drop (C) 45min growth-50nm drop (D) 45min growth-100nm drop (E) 45min growth-200nm drop (F) 45min growth-500nm drop.
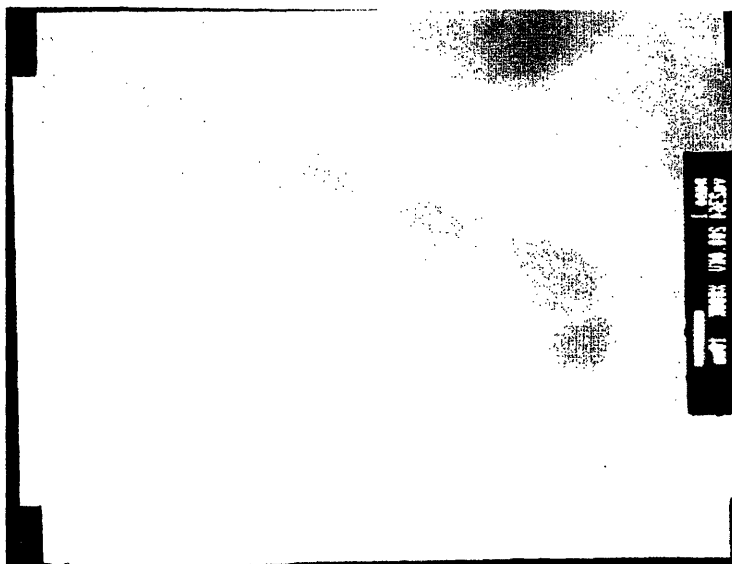
Figure 2.15: Transmission Electron Micrograph showing nanowires with a crystalline core. An amorphous sheath surrounds the crystalline core.

Figure 2.16: TEM Selective Area Diffraction (SAD) pattern of the core, showing that it is monocrystalline.

2.3 Conclusion

All three different mediums i.e., gaseous, liquid and solid were used to deliver nanoparticles to substrates of interest. Within these three broad categories, multiple techniques were developed, namely – nanocluster source, electrospray, aerosol, nanoparticle powder heap, and nanoparticle liquid suspension. Nanowire building blocks were also synthesized. GaAs nanowires were grown in a CVD chamber using the Vapor-Liquid-Solid Mechanism. Here gold metal was used as the catalyst. Two routes were taken to synthesize nanoscale gold droplets. One was using electron beam lithography to exactly define the location of gold wires. Another was by strain induced cracking of a thin film of gold and subsequent drop formation due to surface tension. The length of the grown nanowires depended upon the growth duration and their diameter depended upon the initial gold droplet size. TEM analysis suggested that the nanowires have a monocrystalline core, which was surrounded by an amorphous sheath.

3 Nanoparticle Assembly Using Electrostatics

3.1 Electrostatic particle assembly – Background

Photocopiers and laser printers are some of the most useful inventions by mankind. Both of these are based on electrostatics driving particle assembly. In a photocopier, there is a photoconductive drum, which can store electrostatic charge. The ink that prints on the paper is composed of charged black carbon particles called toner. These particles are attracted by the charge placed on the drum. The surface of the drum is charged positively and a light beam scans the original paper on the glass window. White portion of the original paper reflects light, whereas black areas do not. The reflected light strikes the photoconductive drum and it emits an electron. The electron neutralizes the positive charge on the drum. On the drum, only areas corresponding to the black areas on the paper remain charged. This charge attracts negatively charged toner particles to it. Now a positively charged paper is passed over the drum. This paper attracts the toner particles to itself. The paper is then heated and pressed to fuse the image formed by the toner to the paper's surface. In a laser printer, initially the drum is given a total positive charge by the charge corona wire. As the drum revolves, the printer shines a tiny laser beam across the surface to discharge certain points. In this way, the laser "draws" the letters and images to be printed as a pattern of electrical charges - an electrostatic image. Figure 3.1 is a schematic diagram showing the working of a laser printer.
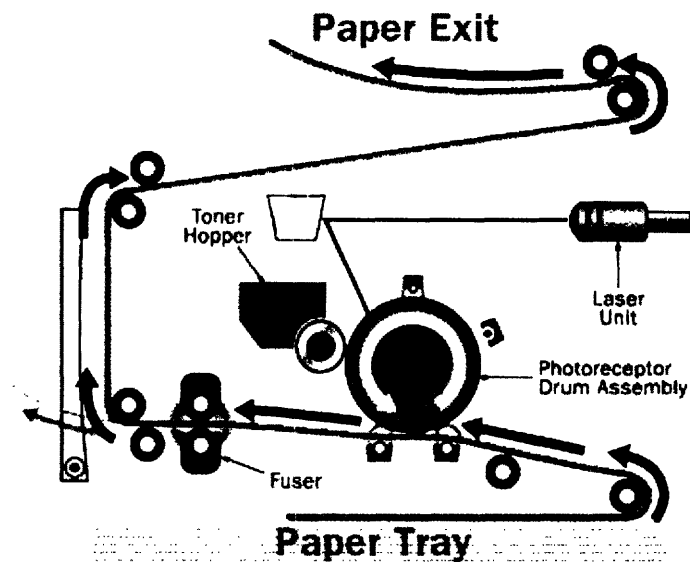
Figure 3.1: Schematic diagram showing the working of a laser printer (courtesy How Stuff Works Inc.).

The toner particles used in photocopiers and laser printers are around 1 micron in diameter. The best feature size that these particles can generate is around 10 microns. Nanoparticles, only a few nanometers in diameter, are now commercially available. Researchers are now trying to develop techniques, which can print nanometeric sized features using these nanoparticles. Directing the assembly of nanoparticles using electrostatics is termed Nanoxerography. Nanoxerography is essentially based on the same principle as conventional xerography, except that charge writing method and the particles used are different. Using light to generate electrons on a photoconductive material cannot give high-resolution feature sizes. In order to accomplish charge transfer at a nanoscale researchers use – scanning probe microscopy tips with potential on them, focused beam of electrons or ions or by charge transfer through stamps, which have

nanoscale features on them. Each of these techniques is capable of making high resolution charge depositions. The charge feature sizes can be of sub-10nm dimensions. Now since the diameter of the developing particles is in nanometeric dimensions, much smaller final features can be obtained.

3.2 Electrostatic Particle Assembly – Principle

Assume a spherical particle in an insulating medium is placed in the vicinity of a charged spot on an electret substrate. The charged spot creates a spatially non-uniform electric field, E. This electric field induces a dipole moment in the particle, p. The interaction of the induced dipole and the inherent charge on the particle with the electric field generates a coulombic force and a gradient force respectively. The interaction of charge with the electric field leads to a coulombic force, F_{COU}. The gradient force is known as the dielectrophoretic (F_{DEP}) force. These forces are expressed by the following equations [24], [25]:

$$F_{COU} = qE \qquad (i)$$

$$F_{DEP} = 2\pi r^3 \epsilon_1 \epsilon_0 [(\epsilon_2 - \epsilon_1)/(\epsilon_2 + 2\epsilon_1)]\nabla E^2 \qquad (ii)$$

Where q is the native charge on the particle, r is the radius of the particle, ϵ_1 is the relative dielectric constant of the dispersion medium and ϵ_2 is the relative dielectric constant of the particle.

The total force acting on the particle is called the electrostatic force F_{ELE}. The electrostatic force is a composite of the coulombic force and the dielectrophoretic force. Electrostatic force, F_{ELE}, can be represented by the following equation:

$$F_{ELE} = F_{COU} + F_{DEP} \qquad (iii)$$

$$F_{ELE} = qE + 2\pi r^3 \epsilon_1 \epsilon_0 [(\epsilon_2 - \epsilon_1)/(\epsilon_2 + 2\epsilon_1)]\nabla E^2 \qquad (iv)$$

The electrostatic force is an attractive force, which attracts the particles to the charged spot on the electret substrate. The above analysis was for a charged spot. It can be similarly extended to an arbitrary charge pattern.

3.3 Electrification Techniques

Hiroshi Fudouzi and other researchers have demonstrated the ability to form high resolution charge patterns using electron and ion beams on ceramic substrates [4]. The formation of electrified pattern was carried out with a 5kV electron beam and with a 30kV focused ion beam of Ga^+ ions (Figure 3.2).
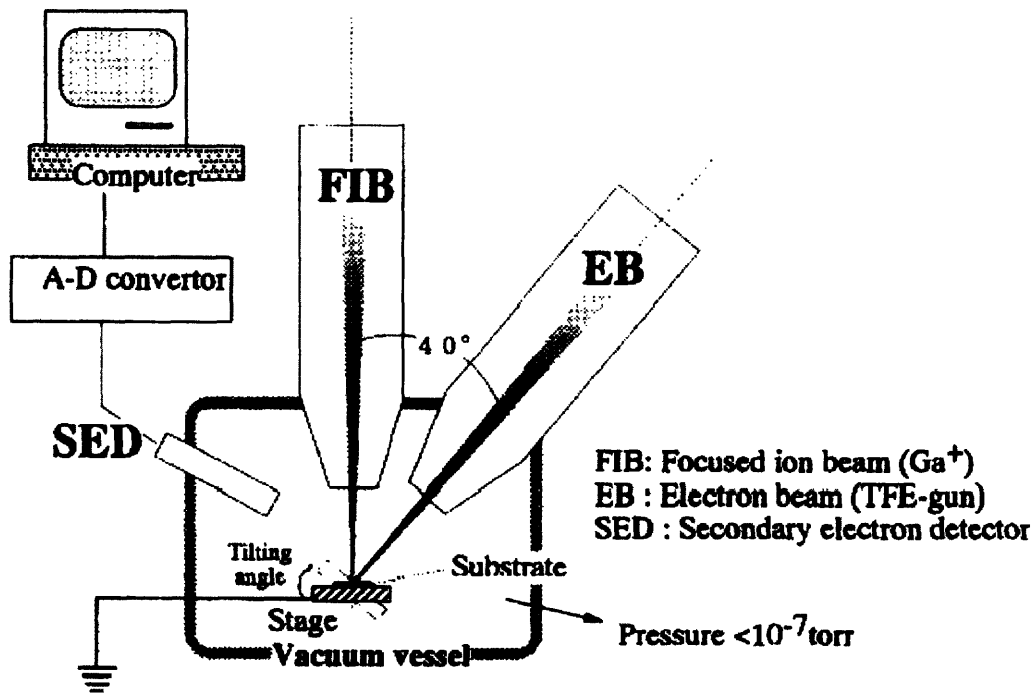
Figure 3.2: Schematic diagram of a dual beam system used for electrification of substrates [4].

In 2001, Heiko Jacobs and George Whitesides demonstrated submicrometer patterning of charge in thin-film electrets[26]. Here the authors used a flexible, micropatterned electrode to pattern an electret thin film in a parallel process by injecting and trapping charges. A PDMS (polydimethylsiloxane) stamp patterned in bas-relief and supporting a gold film, was brought in contact with a film of PMMA (polymethylmethaacrylate) supported on doped silicon. A voltage pulse between the gold film and the silicon transfers charge at the contact areas between the gold and the polymer electret (Figure 3.3). Areas of ~1 cm^2 were patterned with trapped charges at a resolution better than 150 nm in less than 20 seconds. The method is called electrical microcontact printing.

Because the electrode is flexible, it can make sufficiently intimate electrical contact with

a solid surface to produce uniform pattern transfer by charging.
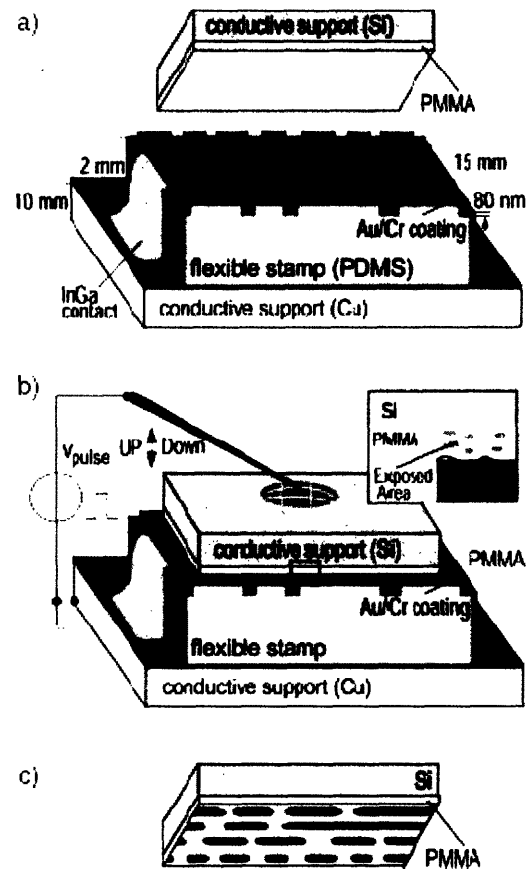
Figure 3.3: (A) A thin film of PMMA supported on a doped, electrically conducting Si wafer is placed on top of a flexible, metal-coated stamp. (B) An external voltage was applied between the Au and the Si to write the pattern of the stamp into the electret. (C) The Si chip is removed with the PMMA carrying a charge pattern [2].

Another technique to store charge in electret materials is by using scanning probe microscopy (SPM) tips. Here a potential is applied to the tip, which rasters the substrate in contact mode (Figure 3.4). This causes contact electrification of the electret material with. The charge stored is of the same polarity as the polarity of the potential on the tip. The electrification can be later imaged with a SPM tip having an opposite potential as before and rastering in a non-contact mode[5].
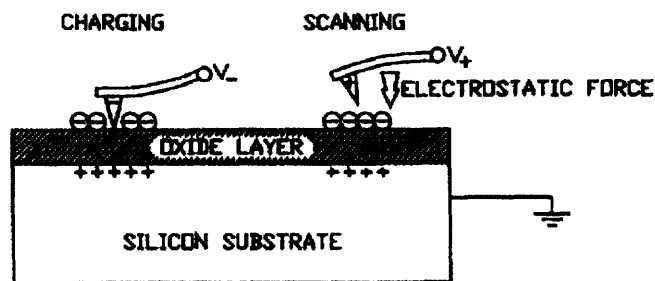
Figure 3.4: SPM tip electrificates an oxide on silicon substrate. The negative charge on the tip induces a negative charge deposition in the electret film. Reversing the polarity on the tip and operating it in non-contact mode can be used to image the charge[5].

3.4 Electrostatic Nanoparticle Assembly – Past Work

In this technique nanoparticles are used as the building blocks to decorate the electrified substrates. The use of nanoparticles as building blocks, regardless of the application, requires novel assembling techniques. Most current approaches like single particle manipulation has inherent disadvantages. Single particle manipulation is useful to fabricate and explore new device architectures. However, the process is very slow and not useful for any commercial application. Fabrication strategies that rely on mechanisms

of self-assembly show promise. Self-assembly is a parallel process, which leads to a multifold increase in yield. There is a great interest in using self-assembly techniques to assemble nanoparticles on to substrates. Our group has developed some novel techniques for directly printing nanoparticle precursors on different substrates of interest [27], [28], [29]. In one of the techniques a nanoparticle film was melted and sintered using electron and ion beams [29]. In another technique, elastomeric stamps with positive relief were wetted with nanoparticles. The stamp then embosses the nanoparticles on the substrate [28].

Electrostatic interactions to direct the self-assembly process of nanoparticles have been an area of great interest. Apart from different electrification methods and the type of nanoparticle used, another variable is the mechanism used to deliver the nanoparticles. Fudouzi [6] and others have delivered nanoparticles from a liquid suspension. Figure 3.5 shows a schematic of electron beam charging of electrets and subsequent development using a liquid nanoparticle suspension. Figure 3.6 is an electron micrograph of the substrates developed using liquid nanoparticle suspension.
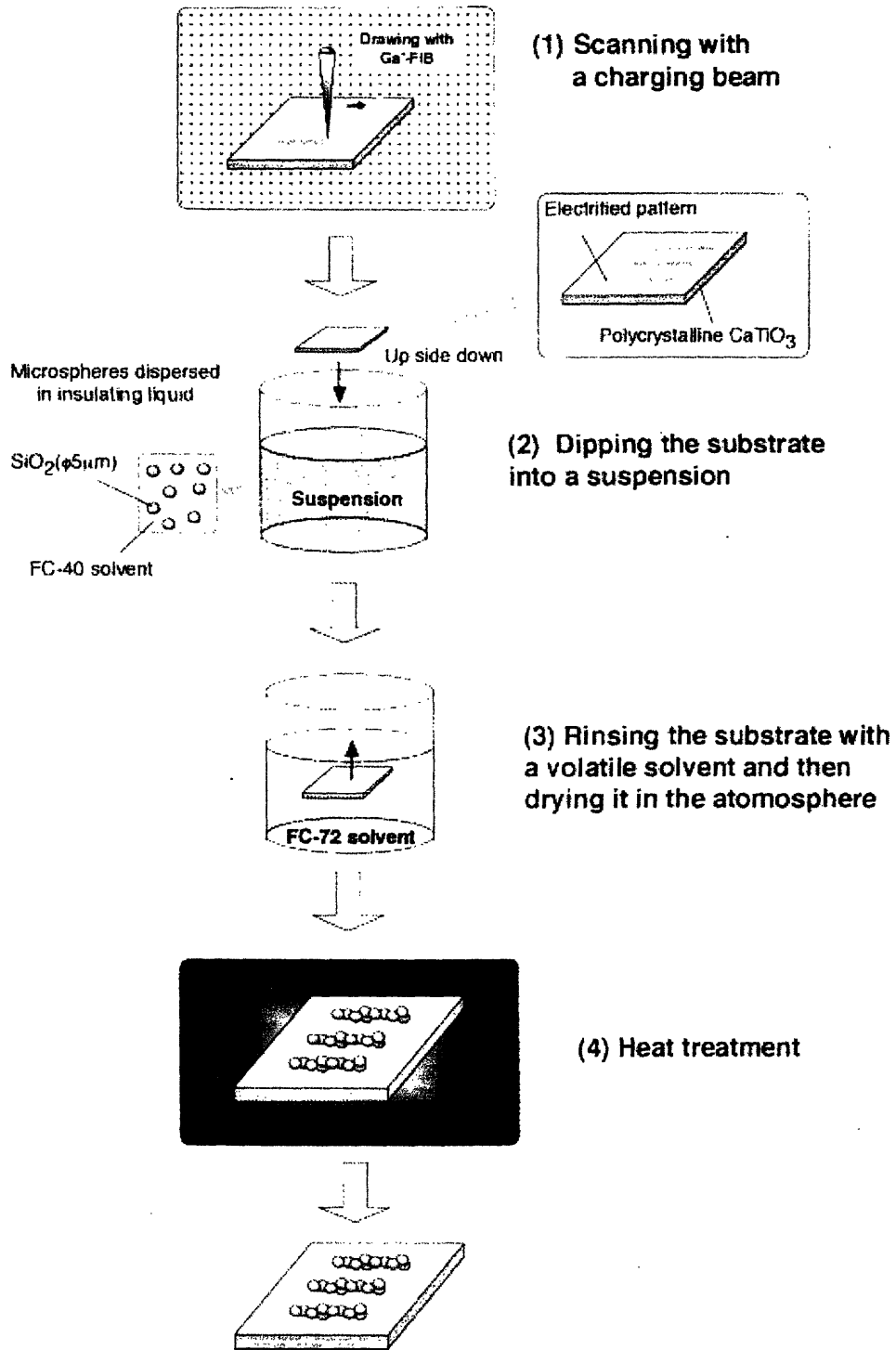
Figure 3.5: Schematic illustration of steps required for arrangement of microsized particles [6].
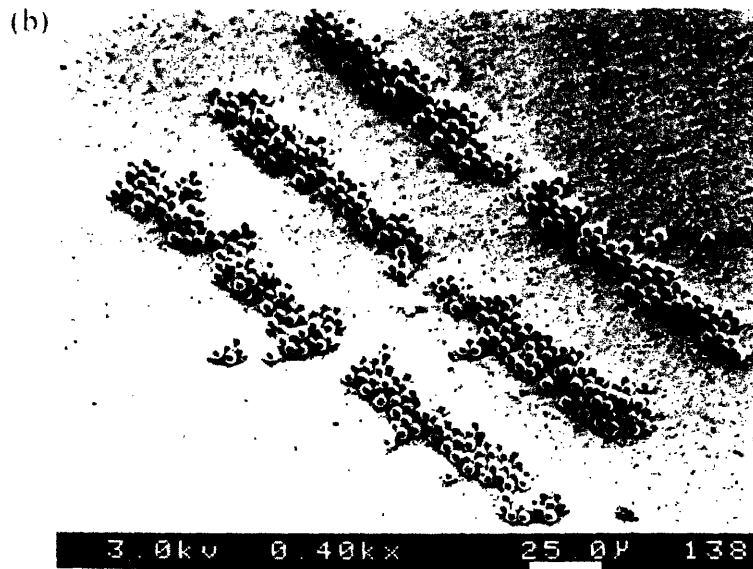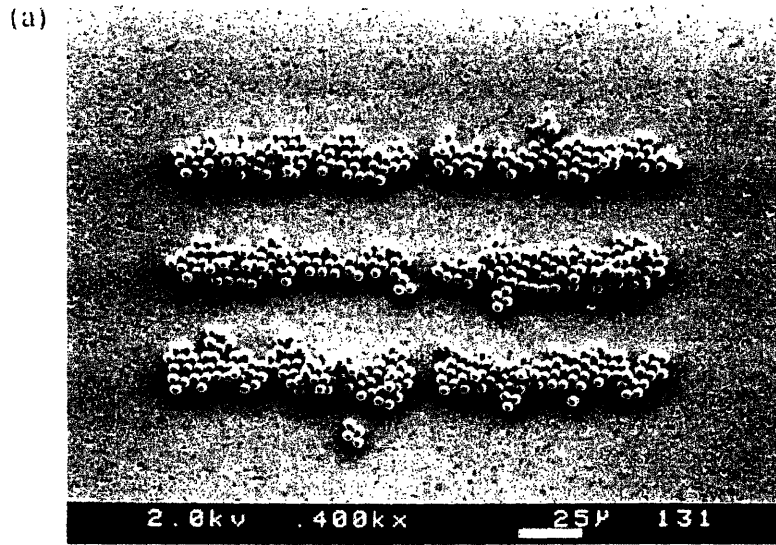
Figure 3.6: (a) SEM image of the patterned SiO_2 particles on the positively electrified pattern (b) SEM image of the patterned SiO_2 particles after heat treatment at 1150 C for a half-hour. The SiO_2 particles were adhered strongly to the substrate [6].

Delivery from liquid suspension could result in deposition at un-charged regions as well. Gas phase delivery of nanoparticles has also been demonstrated [2], [30]. Barry and others used a particle assembly module to accomplish the directed assembly of nanoparticles. The module consists of a cavity that holds the sample, two electrodes to generate a global electric field that directs incoming charged particles towards the sample surface and an electrometer to count the charge of the assembled particles. This module is attached to a tube furnace that generates the nanoparticles by evaporation and condensation.
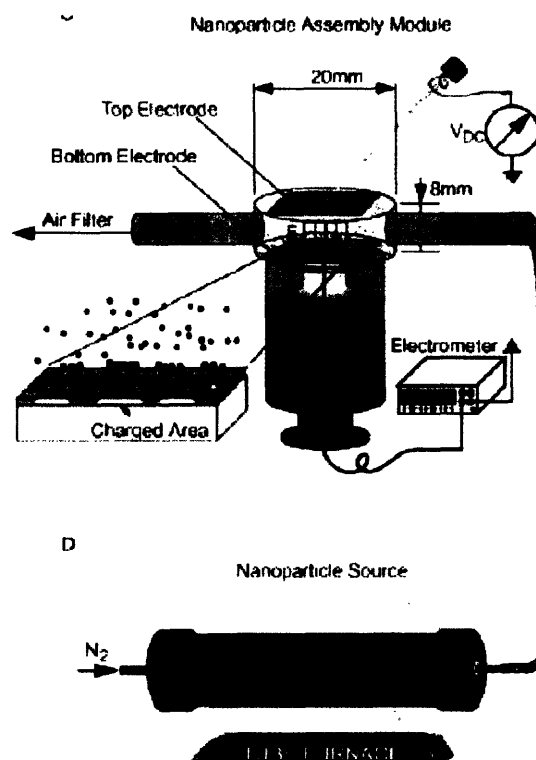
Figure 3.7: The directed assembly of the nanoparticles occurs in the particle assembly module. An external potential, VDC, applied to the top electrode directs incoming nanoparticles to the charged sample surface. The electrometer measures the number of assembled, charged particles during the assembly process [2].

44

3.5 Electrostatic Nanoparticle Assembly – This work

Energetic electron and ion beams were used to electrify electret substrates. The electrified substrates were then decorated by nanoparticle building blocks described in Chapter 2. Three major components in developing a good assembly scheme are electret material used, electrification technique and nanoparticle building blocks. This section describes the electret substrates and electrification technique used in this work.

3.5.1 Electrets

Some of the materials used in this work were polyamide, mylar, teflon, spin-coated PMMA, HMDS coated silicon oxide, ceramic titanates etcetera. A good electret is one that can store charge for long periods of time. Polyamide and mylar have been shown to be among the best electrets along this dimension. Another important property is the electrets ability to constrain charge into a small dimension. Again, empirically polyamide was determined to be the best electret to dimensionally confine storage of charge.

3.5.2 Electrification

Electrification of the above electret materials was mostly accomplished by exposing them using a focused beam of electrons. FEI XL30 Environmental scanning electron microscope (ESEM) was modified into electron beam lithography tool using NPGS. The accelerating voltage varies between 1-30KV for XL30. For charge writing, the voltage was optimized to be around 5KV. The beam current can be varied by changing the electron beam column apertures or by changing the beam spot size. Spot size optimization requires a trade-off between focus and beam diameter. The best condition

was optimized at beam spot size 2. Figure 3.8 shows a schematic of a focused beam of electron rastering across an electret material to deposit charge.
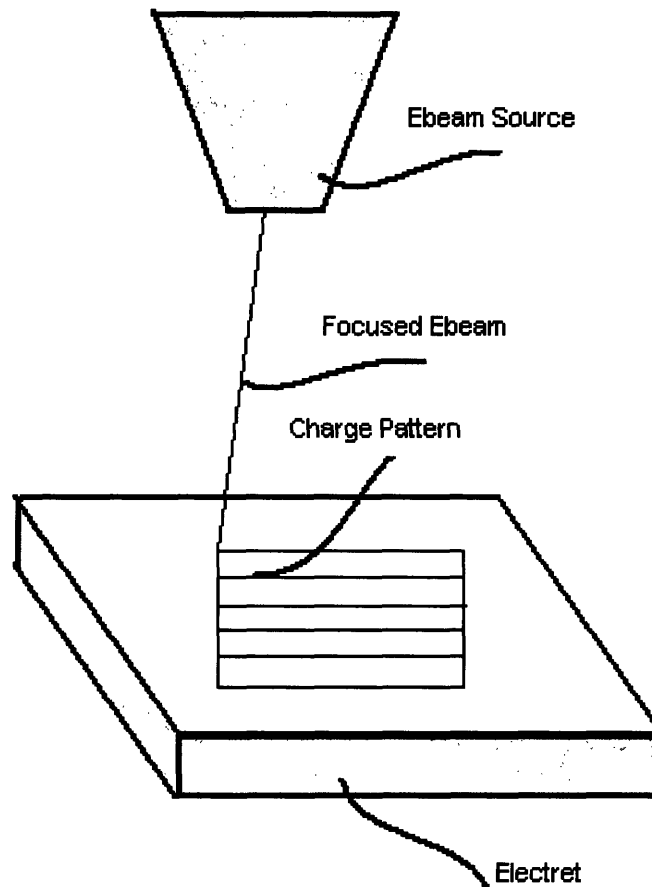
Figure 3.8: Schematic of a focused beam of electron rastering across an electret to deposit charge.

XL30 electron beam can only deposit negative charge in the substrate. In order to deposit positive charge a focused beam of positive ions can be used. FEI DB235, a dual beam tool, which has both electron and ion beam columns, was also used for substrate

electrification. The ion beam column focuses a beam of gallium ions. Gallium ions are positively charged, and as for an electron beam before, they can be rastered across the substrate to deposit positive charge.

3.5.3 Charge Imaging

Charge in electrified substrates is conventionally imaged using scanning tunneling microscopy (STM) [31], atomic force microscopy (AFM) [32] or Kelvin probe force microscopy (KFM) [33] [7].
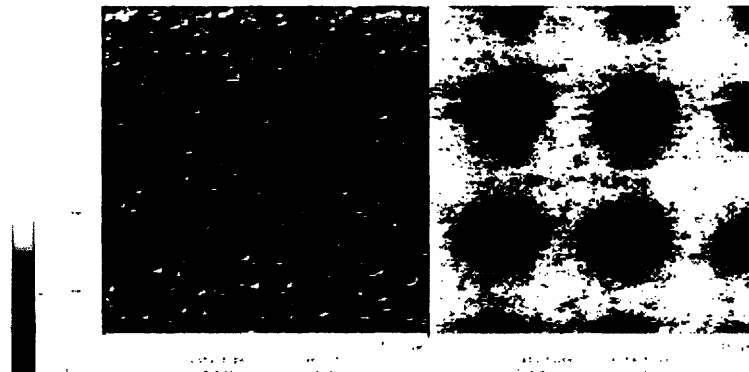
Figure 3.9: The left hand image is a topography map of the electret and the right hand image is a KFM surface potential map. Positive charge in the form of circular dots was deposited in the electret. The darker regions in the right hand image correspond to positive charge [7].

One of the goals of this project was also to perform on the fly feedback correction. It would be difficult to incorporate a SPM technique into an electron or ion beam operating chamber. Also the SPM techniques are inherently very slow, using them for imaging charge could significantly slow down the overall process. In this work the electron beam,

which was used to deposit charge was also used for charge imaging purposes. For charge imaging the beam is operated at lower accelerating voltages and at lower spot sizes. This is to insure that the imaging beam does not interfere with already deposited charge. Figure 3.10 shows an electron beam micrograph of electron beam charged mylar substrate. The charge was deposited at an accelerating voltage of 10KV and spot size 2. The charge imaging was performed at an accelerating voltage of 2.5KV and spot size 2.
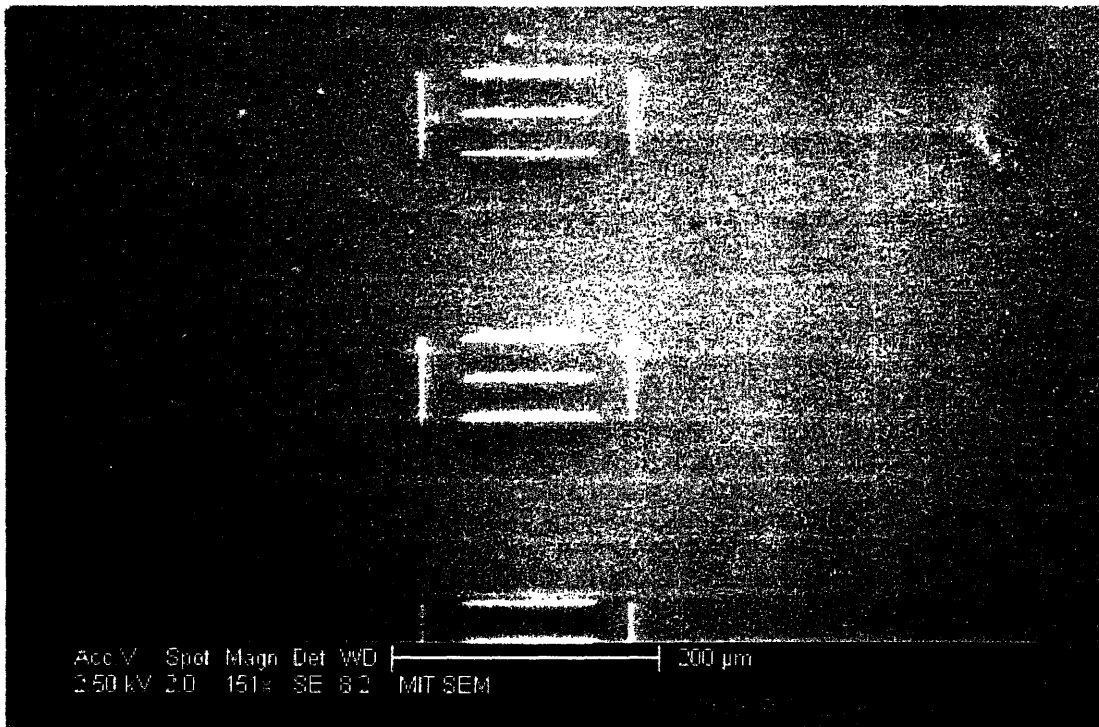
Figure 3.10: Electron beam micrograph of a mylar substrate in which negative charge was stored using an electron beam.

3.5.4 Nanoparticle Charge Decoration

Nanoparticle and nanocluster precursors produced using techniques described in previous chapter were used to decorate the electrified substrates. In some schemes the precursors were pre-charged. In other schemes they were polarized by the stored charge in the electrified substrate. This section describes how different kind of nanoparticle precursors were decorated on to electrified substrates.

3.5.4.1 Nanoparticle Solid Suspension

Nanoparticle solid suspension is described in Section 2.1.The charged electret substrate was directly immersed into this heap of nanoparticles. These nanoparticles were usually uncharged. However, the stored charge in the substrate polarizes these nanoparticles and attracts them to charged regions of the electrified substrate. Figure 3.11 is an electron micrograph, which shows silver nanoparticles decorating a charged mylar substrate.

Figure 3.11: Electron micrograph showing silver nanoparticles decorating a charged mylar substrate.

Another scheme for an in-situ delivery of nanoparticles from a solid suspension was also developed. Here the electret substrate and the nanoparticle powder were placed in a micro-chamber. The micro-chamber was built on a stub, which was placed in the XL30 ESEM chamber. The electron beam charged the substrate and concurrently the nanoparticles got polarized and were attracted to the charge pattern on the substrate. Figure 3.12 shows silicon oxide nanoparticles decorating a negative charge pattern on a mylar substrate.
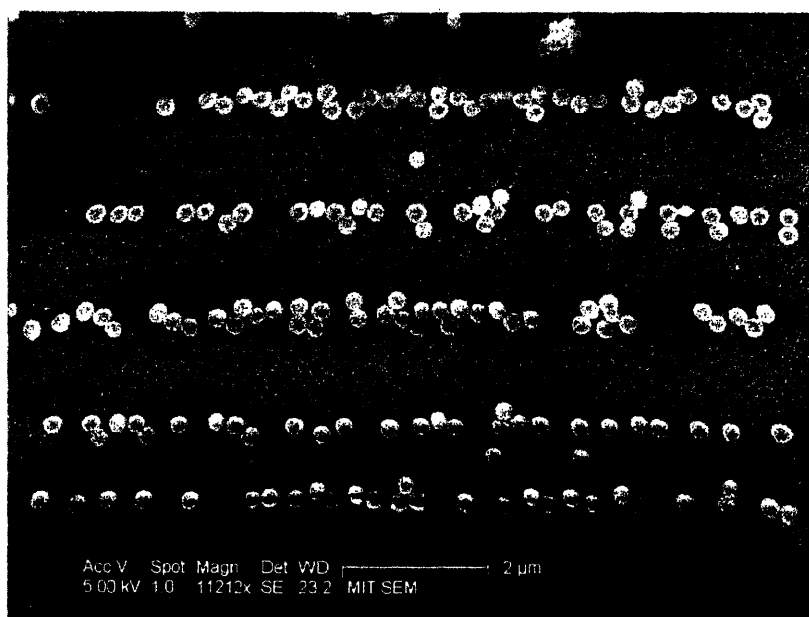
Figure 3.12: Silicon oxide nanoparticles decorating a negative charge pattern on a mylar substrate. The nanoparticles were delivered by an in-situ source.

The in-situ delivery scheme provides live feedback of nanoparticles decorating the charge pattern. In this scheme, the electron beam was operated in a line scan mode and the contrast signal was analyzed. In line scan mode, the electron beam rasters along over a

line specified by the user. And the secondary electron detector produces a contrast signal · for the rastered line. Rastering the line over an electret substrate deposits charge along that line. This charged line then polarizes nanoparticles and attracts them towards itself. Regions where nanoparticles get deposited are brighter and a high contrast signal was obtained. Regions where there were no nanoparticles were darker and a low contrast signal was generated.

3.5.4.2 Nanoparticle Liquid Suspension

Nanoparticle liquid suspension is described in Section 2.1. In this scheme, the electrified substrate is immersed in a solution containing nanoparticles. Here two kinds of nanoparticles were employed – pre-charged nanoparticles and polarized nanoparticles. Pre-charged nanoparticles, were graphite particles usually used as a xerography toner. Immersing an electrified substrate into either of these nanoparticle solutions causes the nanoparticles to migrate towards the substrate and decorate the charge pattern. Figure 3.13 shows assembly from a liquid suspension.
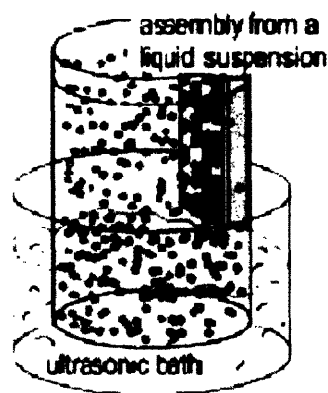
Figure 3.13: Schematic of assembly from a liquid nanoparticle suspension [2].

Figure 3.14 shows assembly of pre-charged graphite nanoparticles dispersed in a hexane solution onto an electrified polyamide substrate.

Figure 3.14: Optical micrograph of an electrified polyamide substrate decorated by pre-charged graphite nanoparticles dispersed in hexane.

3.5.4.3 Gaseous Nanoparticle Suspension

Gaseous nanoparticle suspension is described in chapter 2. For nanoparticle charge decoration from the gaseous phase - electrospray was used as the primary source. Silver nanoparticles, ~5 nm in size, obtained from Nanophase Inc., were dispersed in toluene. The nanoparticle dispersion was loaded into a syringe, which was pumped using a syringe pump. The outlet of the syringe was attached to a 250μ bore needle. The needle was kept at a high potential of around 2KV. Positively charged silver nanoparticles were

electrosprayed to form a cloud over the electrified polyamide substrate. The positively charged nanoparticles decorate the negatively charged electron beam pattern on polyamide. Figure 3.15 show optical micrographs of electrified polyamide substrates after being dusted by electrosprayed silver nanoparticles.

(a)

___ 5u

(b)

— 5u
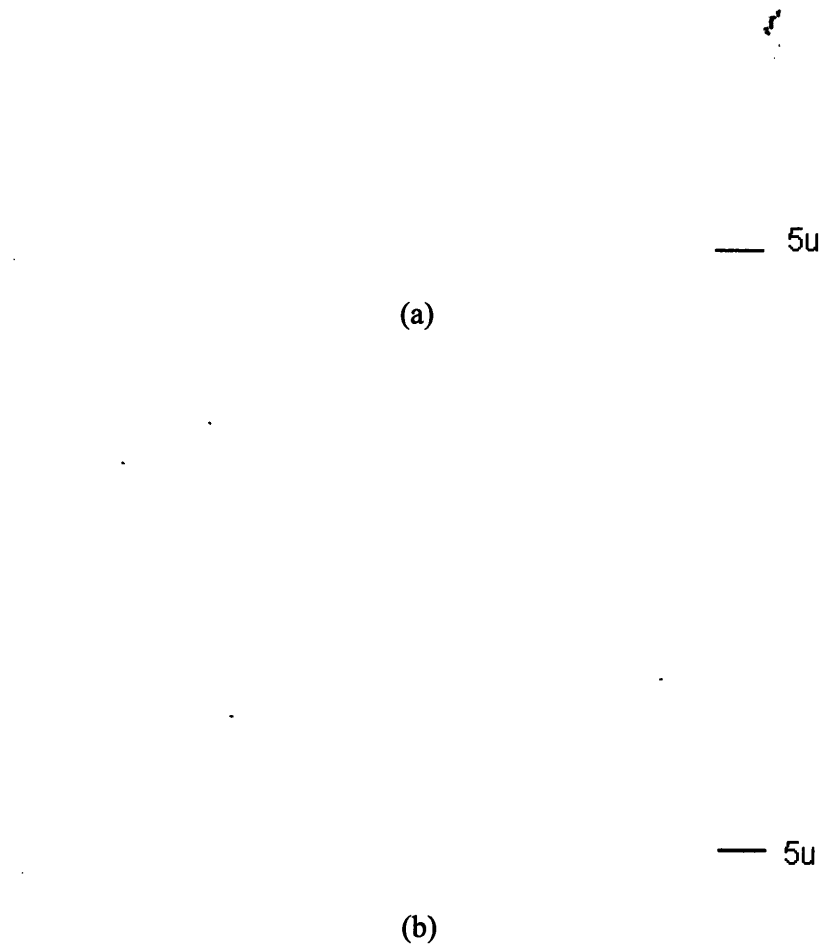
Figure 3.15: Optical micrograph showing polyamide substrate dusted using electrosprayed silver nanoparticles. (a) Some deposition occurs outside of charged regions (b) Dusting with a lower flux of electrosprayed nanoparticles results in a cleaner pattern.

3.6 Electrostatic Resist

3.6.1 Electron Beam Lithography

The very small spot size of a focused beam of electrons leads to an electron beam lithography technique for fabricating nanostructures. Electron beam lithography has been used to create sub-10nm features [34]. Whereas the resolution in optical lithography is limited by the wavelength of light used for the exposure, the electron beam has wavelength so small that diffraction no longer defines the lithographic resolution. However, optical exposure is a parallel process. Whereas, in electron beam lithography the beam rasters serially for exposure.

Electron beam resists find wide application in photomask production. It is the preferred technique for masks because of its flexibility in providing rapid turnaround of a finished part described only by a CAD file. Ebeam lithography has the remarkable ability to meet stringent line width control and pattern placement specifications, on the order of 50nm each. Another application is direct write for advanced prototyping of integrated circuits and manufacture of small volume specialty products, such as gallium arsenide integrated circuits and optical wave-guides. Ebeam lithography is widely employed for research into the scaling limits of IC's and studies of quantum effects and other novel physics phenomena at very small dimensions.

In spite of its ability to overhaul the Moore's Law by a long way, electron beam lithography has not found application in direct exposure of resists for IC manufacture. Primary reason for this is a lack of a highly sensitive electron beam resist.

3.6.2 Resists

The electron beam exposure time is limited by the sensitivity of the employed resist. Sensitivity of a resist is measured in microcoulombs per square centimeter ($\mu c/cm^2$). Poly methyl methacrylate (PMMA) is the most commonly used electron beam resist. PMMA needs an exposure dosage of around $100\mu c/cm^2$. Most other commercial resists also require exposure dosage in the range of $1-100\mu c/cm^2$. Table 3.1 lists electron beam resists and their dosage numbers.

Resist	Tone	Sensitivity $\mu c/cm^2$	Developer
PMMA	Positive	100.0	MIBK:IPA
EBR-9	Positive	10.0	MIBK:IPA
PBS	Positive	1.0	MIAK:2-pentanone 3:1
ZEP	Positive	30.0	Xylene:p-dioxane
AZ5206	Positive	6.0	KLK PPD 401
COP	Negative	0.3	MEK:ethanol 7:3
SAL-606	Negative	8.4	MF312:water
Ag-capped nanoparticles (FIB Direct Write)	Positive	5	Hexane
Electrostatic	**Negative**	**0.01**	**Acetone**

Table 3.1: Electron beam resists and their exposure dosages [10], [11].

Electron beam lithography works by exposing a pattern and removing, by etching or dissolution, the exposed portion of the polymer resist film (positive resist). The result

from exposing a resist is that the molecular linear chain is broken and the average molecular weight of the polymer-exposed area is reduced. Reducing the molecular weight of the polymer is accompanied by an increase of the solubility, i.e. the etching rate [35].

Chemical amplification is based on generation of a chemically stable catalytic species – designated as a proton H+. Rather than using exposure energy to directly cause a solubility switch, chemically amplified resists use exposure energy only to generate a catalytic species. The generated catalyst then initiates a chain reaction or promotes a cascade of solubility-switching reactions in the exposed regions of the resist. The apparent quantum efficiency for the solubility switching reaction in such a system is the product of the quantum efficiency for catalyst generation and the catalytic chain length. Catalytic chain lengths in the many hundreds are common, so in effect the quantum efficiency can be greater than one. One chemical conversion can cause several chemical reactions, and thus the exposure can be termed "chemically amplified." In this manner, lithographic imaging can be accomplished with very low exposure doses [35].

Chemically amplified resists have a major limitation: It is possible for the catalyst generated in exposed regions to diffuse into unexposed regions, causing blurring of the latent image. The migration of the acid effectively results in a bias between the distribution of exposure energy and the final distribution of exposure products. This bias depends upon the resist chemistry and the processing conditions, but is largely independent of the exposure conditions and therefore cannot be eliminated by improving the exposure process [35].

Electrostatic resists utilizes electrons to store electronic charge in substrates. Each electron stored in the substrate generates an electric field around it. The electric field can polarize and attract a cluster with hundreds of atoms towards the electron storage spot. Thus each electron has the capability of attracting hundreds of atoms to it. This resist is thus very highly amplified due to electrostatics. The efficiency of the process allows the usage of exposure doses as low as $0.01\mu c/cm^2$, which is at least 100 times lower than most commercially available resists.

3.6.3 Electrostatic Resist – Experimental

Figure 3.16 shows a schematic flowchart for the development of an electrostatic resist. The substrate shown in step (A) is a polyamide electret, which has been electrified using an electron beam. Electron beam exposure was done at an accelerating voltage of 5KV and an electron dose of $0.01\mu c/cm^2$. Post-electrification the electret was developed by nanoparticle building blocks (step B). These building blocks could be delivered using any of the gaseous, liquid or solid nanoparticle suspensions. In this case, a liquid nanoparticle suspension of graphite nanoparticles is hexane was used. Step (A) and step (B) are exactly the same as described is prior sections of this chapter. Subsequently, in step (C) ~100nm of gold film was thermally evaporated on the nanoparticle decorated electret substrate. In step (D), the substrate is ultrasonicated in acetone for five minutes, which lifts-off the nanoparticles and the gold deposited on the nanoparticles.
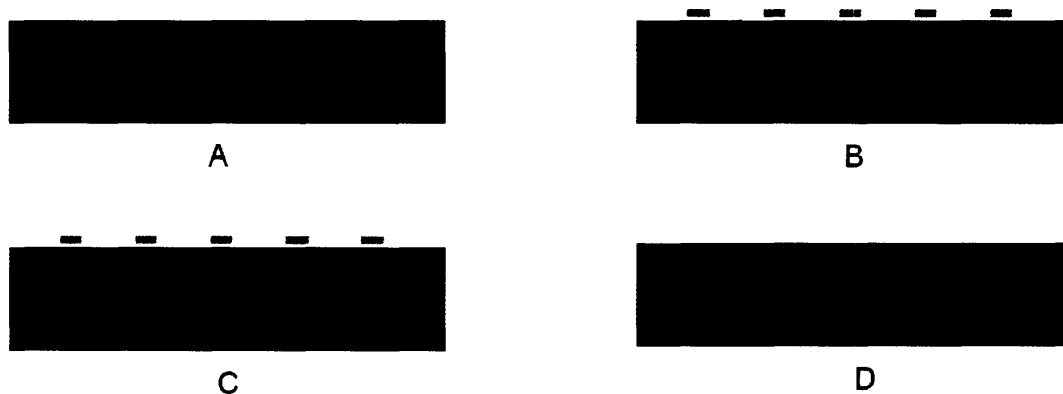
Figure 3.16: Schematic showing the flowchart for the development of an electrostatic resist (a) electron beam charged electret substrate, (b) charged or polarized nanoparticles decorating the electret substrate, (c) gold deposited over the nanoparticle decorated electret substrate, (d) gold posts left standing after lifting-off nanoparticles.

3.6.4 Electrostatic Resist – Results

Electrostatic resist was utilized to fabricated lift-off structures of gold over polyamide. Following the steps described in previous section a discontinuous gold film was fabricated on a polyamide substrate (Figure 3.18). Nested L shaped lifted-off lines cause the film to be discontinuous.

5u
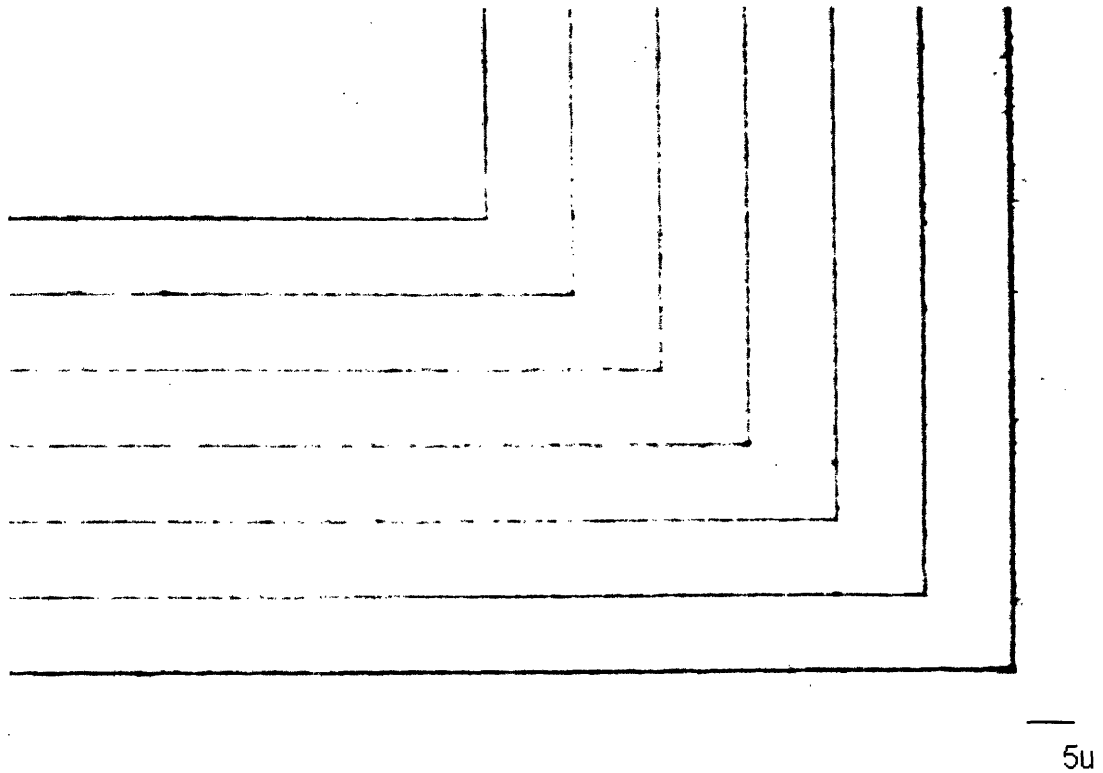
Figure 3.17: Optical micrograph of a gold film deposited on polyamide substrate. Nested L shaped lifted-off lines makes the film discontinuous.

Electrostatic resist was also used to deposit gold pads and resistivity measurement was performed to demonstrate that lift-off was clean. Figure 3.18 is an optical micrograph of nanoparticle decorated polyamide substrate. As described for the substrate in Section 3.6.4, similar steps were followed for this substrate and isolated gold pads were fabricated. Probe station was used to measure resistivity between the fabricated gold pads. Figure shows the resistivity measurements across the fabricated gold pads and also for the continuous gold film deposited on the polyamide. Note that no conduction was observed between the pads
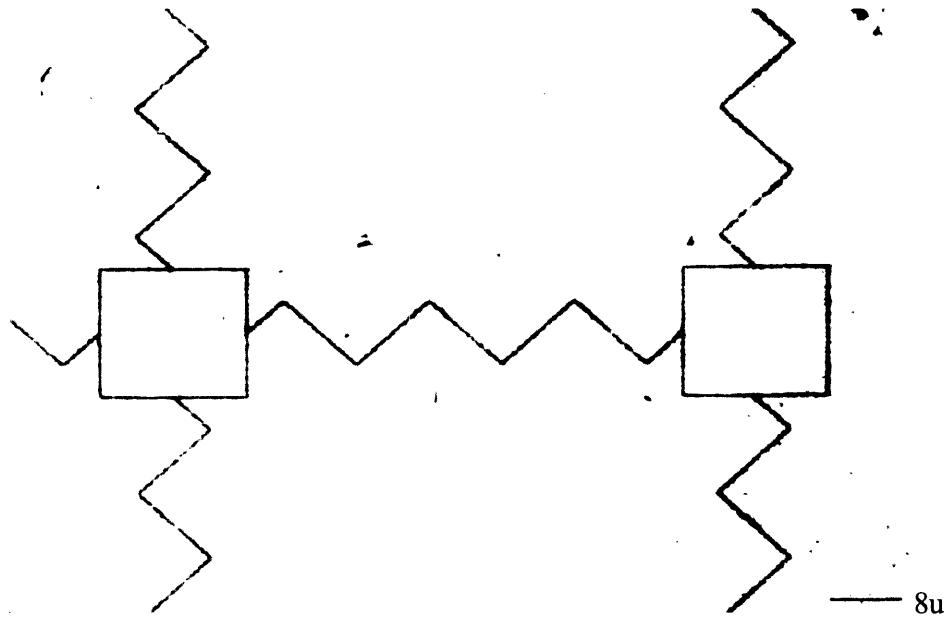
(a)
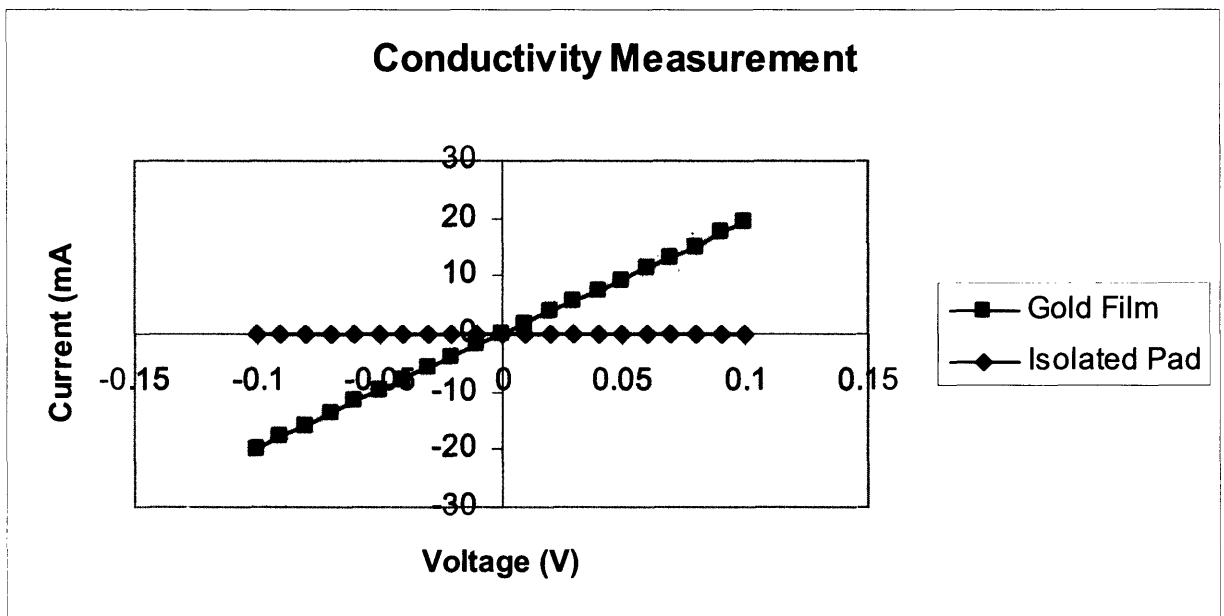
(b)

Figure 3.18: (a) Optical micrograph of a nanoparticle decorated polyamide substrate (b) Graph showing difference in conductivity of isolated gold pads and a discontinuous gold film.

3.7 Conclusion

Focused beams of electron and ions were used to deposit charge in electret materials. Amongst the materials used, polyamide was empirically found to be the best electret material to store charge over long periods of time and also in its ability to laterally constrain charge. Electrified substrates were then decorated with various nanoparticle building blocks. In different schemes, these nanoparticles were delivered by solid, liquid or gaseous nanoparticle suspensions. A new technique to deliver metallic nanoparticles using electrospray was also developed.

The key result of this work was the development of a new electron beam lithography process. A new kind of electron beam resist was developed, which has been termed as the electrostatic resist. Electrostatic resist is about 100 times faster than the fastest available commercials resist. Electrostatic resist requires $0.01 \mu c/cm^2$ of electron dose for complete exposure. This is the lowest dose that our electron beam lithography instrument FEI XL30 can currently deliver. With hardware modification the dosage numbers can be expected to be lower.

Electron beam lithography can be used to fabricate sub-10nm features quite easily. However, it has long suffered from slow exposure speeds. With the development of an electrostatic resist, which exposes at $0.01 \mu c/cm^2$, the problem of slow write speeds may finally be overcome.

4 Functionalizing Nanowire Building Blocks

Since both semiconducting and metallic components can be produced as one-dimensional nanowires, device made out of these components could be greatly miniaturized. In such a device, semiconducting components could be used to perform logic functions, while metallic components could be used as interconnects [18]. Arranging nanowires into useful structures is a challenge that needs to be addressed in order to realize their full potential for applications. Nanotubes is another one-dimensional structured material, which have been researched since 1991 [16]. Nanotubes also exist both as metals and semiconductors. The transport properties depend upon the chirality of their structure. Fabricating logic devices using nanowires is very similar to fabricating logic devices using nanotubes. This chapter describes prior work on carbon nanotube logic device fabrication and details on GaAs nanowire logic device fabrication using energetic beams.

4.1 One-Dimensional Structures - Logic Device Fabrication

Since carbon nanotubes (CNT) can be semiconducting, metallic or even insulating makes them very attractive materials for fabricating nanometer scale logic circuits composed of multiple transistors. Several research laboratories have demonstrated electronic devices where nanotubes are the functional materials. Essential devices like field effect transistors (FET) have been fabricated. For FET's nanotubes are used as channels. At its ends, they are attached to electrodes, which act as source and drain respectively. Current in the nanotube channel can be switched on or off using the third gate electrode. It has been shown that on application of field, via the gate electrode, the conductivity of CNT can be

changed by a factor of million or more as compared to conventional silicon. Because of its small size a nanotube device switches very reliably. Also such a small device can operate at clock speeds of terahertz or more [17].

CNT-FET's are fabricated by placing the tubes over an oxide on silicon wafer. The wafer has pre-fabricated metal electrodes on it. An electron beam resist is spun and exposed to connect the nanotubes to the metal electrodes. Lift-off deposition of a metal is subsequently done to complete the connection of nanotubes and the metal electrodes. The oxide on the wafer is used as the gate-oxide and the backing silicon is used as the back gate. First nanotube transistors operated at very low temperatures, but in 1998 the first room temperature transistor was reported with characteristics remarkably similar to silicon devices [36] (Figure 4.1).
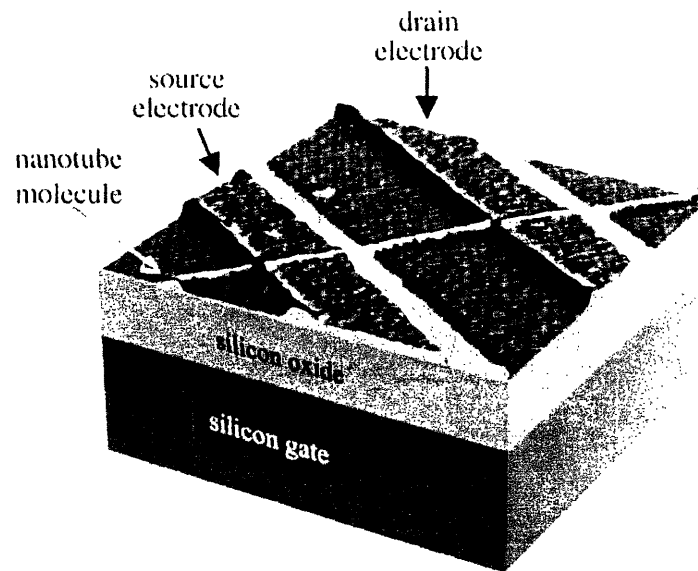
Figure 4.1: Field effect transistor - a nanotube channel connected to two metal electrodes. Silicon is used as the back gate [8].
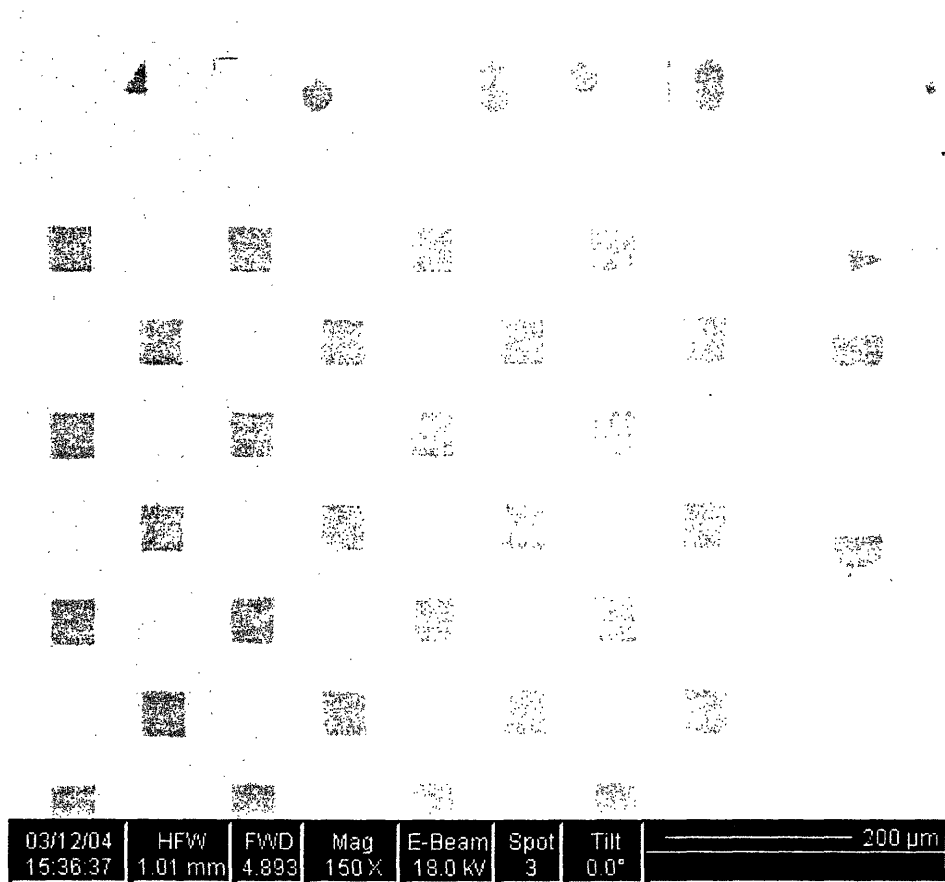
Figure 4.3: Metal pads fabricated on an oxide on silicon wafer using optical lithography.

4.2.2 Nanowire Dispersion

GaAs nanowire solution, as explained in section 2.2, was used to deliver the nanowires. The delivery was accomplished by either using a dropper or substrate immersion. In the first scheme nanowire solution was loaded in a dropper. The dropper then placed a drop of nanowire IPA solution was placed on the substrate. In the immersion technique, the metal pad die was immersed in the nanowire solution for 1 minute. IPA was then allowed to vaporize and a random distribution of nanowires was obtained on the substrate.
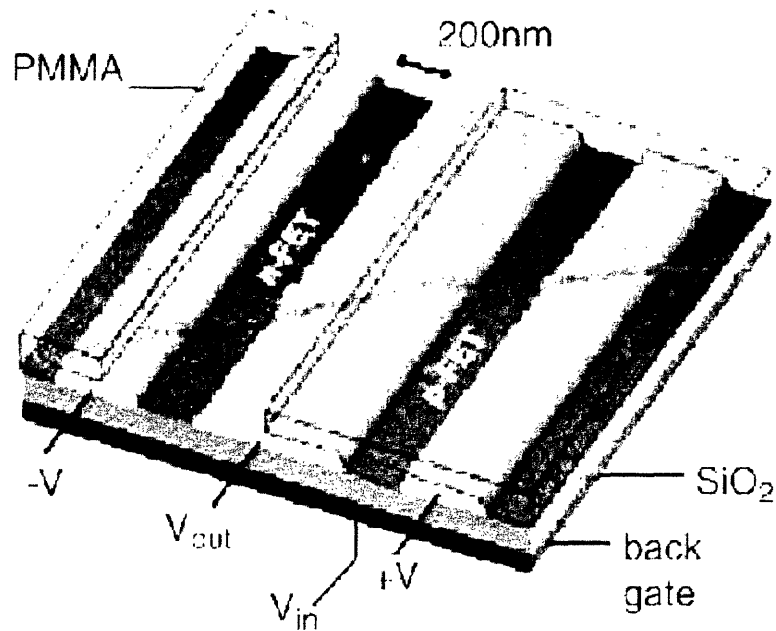
Figure 4.2: An AFM illustration of a logic gate consisting of a single nanotube bundle, positioned over two metal electrodes to produce two p-type CNT-FETs in series. PMMA is spun-on and a window is opened using electron beam lithography. CNT bundle is then exposed to potassium, to convert the region in the window to n-CNT-FET, while other remains p-type [9].

4.2 Nanowire Logic Devices – This work

This section describes the nanowire functionalization process using energetic electron beams.

4.2.1 Metal Pad Fabrication

Optical lithography was used to fabricate gold metal padded substrates. An oxide on silicon wafer was employed to insure that the metal pads are electrically isolated from each other. Wafer was cleaned using acetone and isopropyl alcohol followed by blow-

drying using compressed air. To remove all moisture, the wafer was then dried in an oven at 135C for 10 minutes. It was then coated with AZ 4620 positive resist by spin coating at 3000 rpm for 1 minute. The resist was soft-baked at 90C for 45 minutes followed by a 25 second long UV exposure through a mask. The mask was designed in Corel and was printed on a transparency slide by Pageworks Inc. The wafer was then developed in AZ 440 developer for 3 minutes. The developer was agitated while developing the resist. This was followed by a DI water rinse and a postbake at 90C for 30 minutes. AZ 4620 being a positive resist, the UV exposed regions were removed and the underneath wafer was exposed. Using an electron beam evaporator, 30nm of titanium and 100nm of gold was evaporated on the wafer. The metals deposit on the wafer wherever the resist had been removed. Metal also deposits on the resist. Immersing the wafer in acetone stripped the resist and the metal deposited on it. The wafer was then cleaned using IPA and a DI water rinse. This process fabricates 100-micron square metal pads on the wafer. The wafer was cut into smaller dies, which were easier to work with.

4.2.3 Energetic Beam Processing

Subsequent processing was done using the FEI Strata DB-235 dual beam tool. The tool has an electron beam column, a gallium ion beam column, two chemical vapor deposition (CVD) chambers – one for platinum metal and the other for insulator deposition and an EDAX. The electron beam column can be used as a conventional scanning electron microscope. It can also be used to breakdown the CVD metal or insulator precursor gases to cause localized deposition of these material sets. Alternatively, the ion beam column can also be used for imaging, deposition or milling purposes. Figure 4.4 shows a schematic of a gallium ion beam being used to crack CVD gases.

Basic principle focussed ion beam system

liquid metal ion source

suppressor

extractor

gallium ion beam

lens 1

aperture

objective lens

detector

gas injector

sample
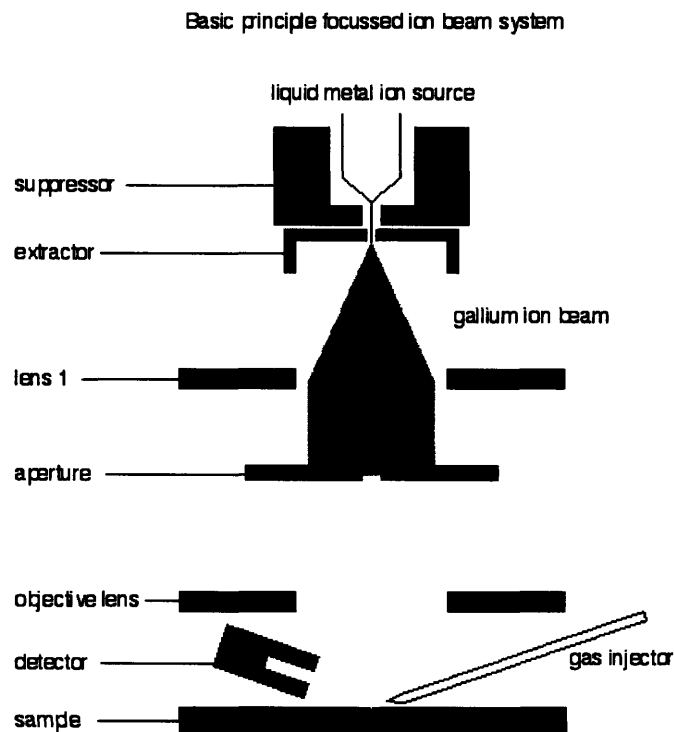
Figure 4.4 Schematic diagram showing CVD gas being cracked using a focused gallium ion beam (courtesy FEI Inc.)

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The randomly distributed nanowires were located using the imaging mode of the electron beam. Most of the nanowires existed in an individual state. But some of them were twined with other nanowires or existed as spaghetti of nanowires. The first step to make logic devices using nanowires was to make transistors. To make a transistor from a nanowire the following have to be fabricated - source, drain, gate-oxide and gate.

After determining the exact location of a nanowire, the electron beam was switched to the deposition mode. Platinum metal was deposited at the ends of the wire to fabricate source and drain electrodes. Connections were made to the nearest gold pad by again using platinum. The exposed nanowire was then covered by an insulator deposition. The insulator used was TEOS and was deposited on the nanowire by breaking its vapors downs using the electron beam. This insulator was used as the gate oxide material. On top of the gate oxide, platinum gate was deposited again using the electron beam breakdown of platinum metal precursor. Using the same process, the gate electrode was connected to the nearest available gold electrode. This completed all the requisite connections and the fabrication of a single nanowire transistor. Figure 4.5 is a schematic diagram of the functionalization process. This process was also used to fabricate a transistor using a nanowire from spaghetti of nanowires. Also, on long nanowires, multiple transistors were fabricated on the same nanowire.
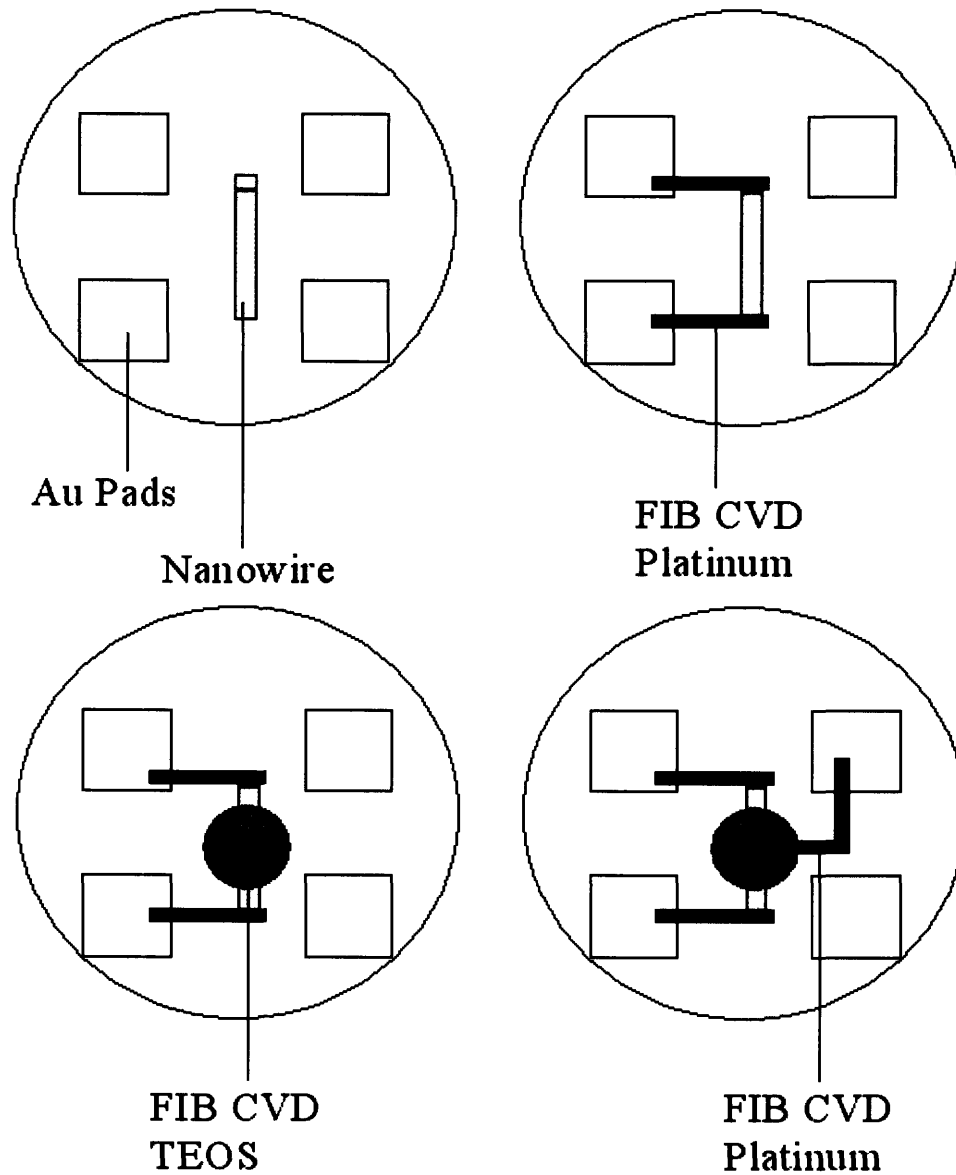
Figure 4.5: Source, drain, gate-oxide and gate materials are deposited using electron beam induced chemical vapor deposition. The electrodes are then connected to pre-fabricated gold pads by again using electron beam chemical vapor deposition.

4.3 Results and Discussion

Functionalizing nanowires using energetic beam induced chemical vapor deposition is the least laborious process that currently exists for fabricating nanowire logic devices. This process provides a capability to fabricate the most complex nanowire logic devices. Figure 4.6 is a series of electron micrographs showing different stages in nanowire transistor processing using a single nanowire or a nanowire in spaghetti of nanowires. Figure 4.7 is an electron micrograph showing multiple nanowire transistors fabricated on the same die. This process was also extended to fabricate more complex ring oscillator architectures (Figure 4.8).
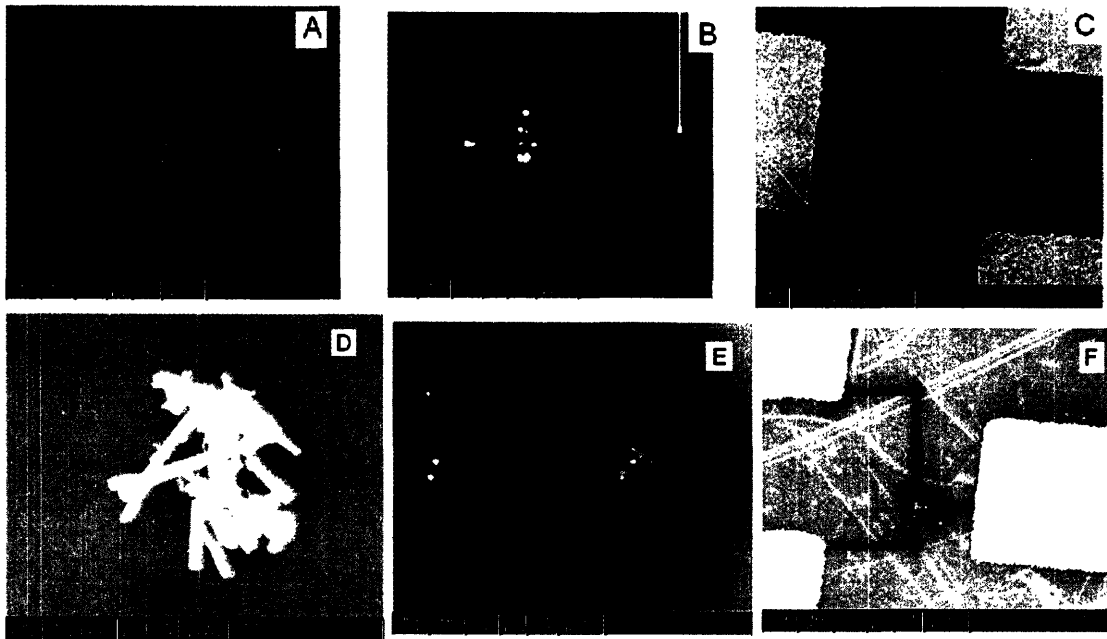
Figure 4.6: Electron micrographs showing nanowire transistor processing steps. (A) A single GaAs nanowire dispersed on an oxide on silicon substrate (B) Source, Drain, Gate-oxide and Gate material deposited on the nanowire (C) Source, Drain and Gate electrodes connected to gold metal pads (D) Spaghetti of nanowires lying on an oxide on silicon

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substrate (E) Source and Drain connections made using Pt deposition (F) Source, Drain

and Gate electrodes were connected to gold metal pads.
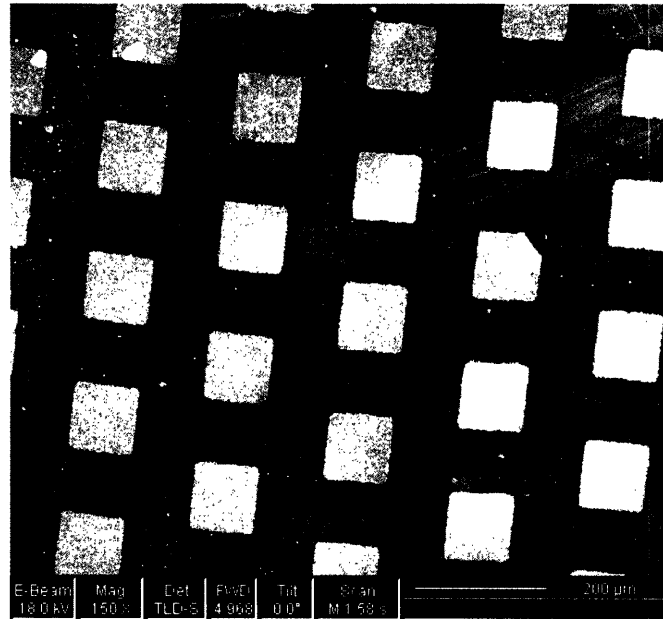
Figure 4.7: Electron micrograph showing multiple nanowire transistor architectures.
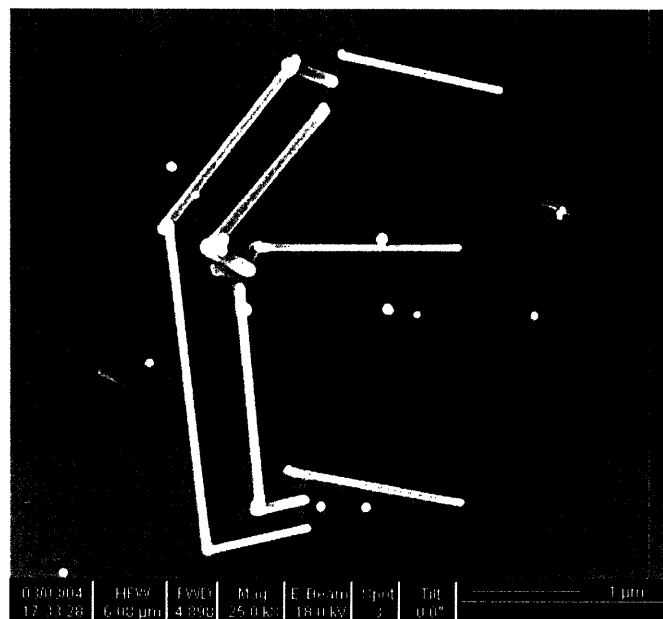
Figure 4.8: Electron micrograph showing ring oscillator architecture using three single

GaAs nanowires.

4.3.2 Electrical Properties

Drain current versus drain voltage (I-V) measurements were performed on the fabricated single nanowire transistors. Gate voltage was varied from – 1 volts to +1 volts in steps of 1 volt. Changing the gate voltage changes the I-V characteristic of the nanowire demonstrating transistor behavior.
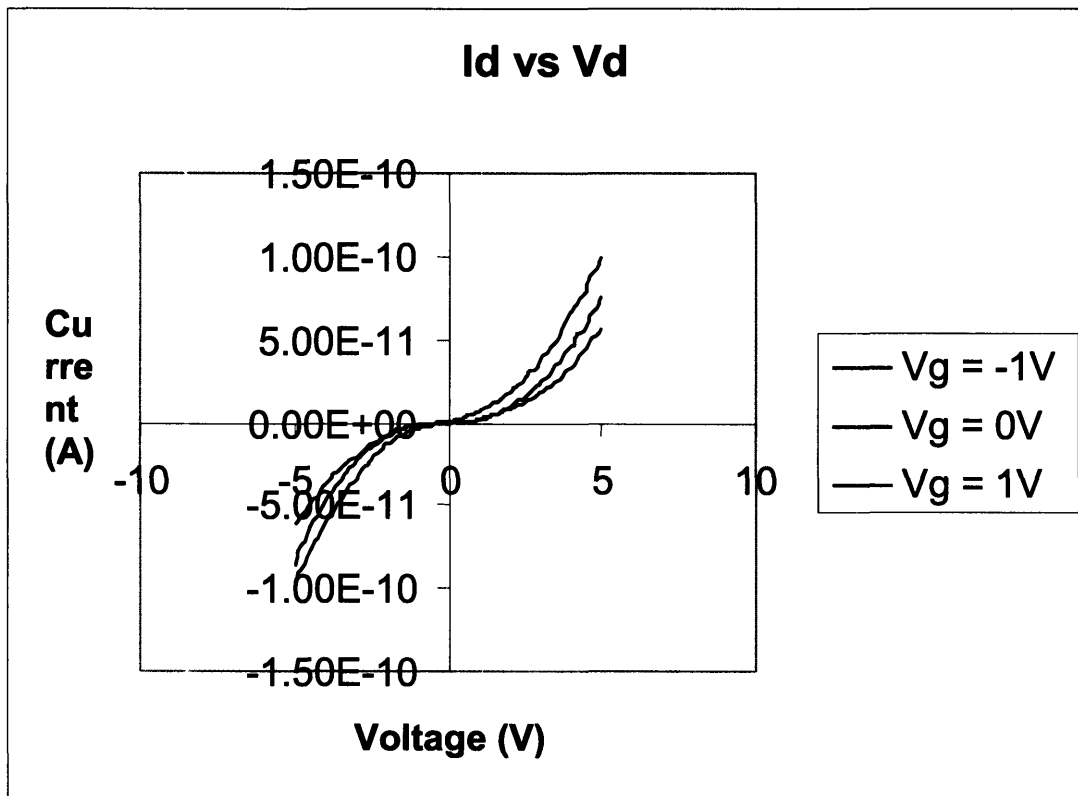
Figure 4.9: I-V characteristics of a single nanowire transistor.

4.4 Conclusion

A novel method to fabricate transistors and other logic devices from semiconducting nanowires or nanotubes has been developed. The material system used in this case was gallium arsenide nanowires. They were grown using the vapor-liquid-solid (VLS) mechanism using gold as the catalyst. The diameter of the nanowires was controlled by the initial droplet size of the gold catalyst. Nanometeric gold droplets were achieved by either electron beam lithography or by annealing a thin gold film. Nanowire growth was performed in a CVD chamber using Tri-methyl gallium liquid and arsene gas (AsH_3) as precursors.

Nanowires were lifted-off into an IPA solution and randomly distributed over an oxide on silicon substrate. The oxide on silicon substrate had electron beam evaporated metal pads pre-fabricated on it. Source, drain, gate oxide and gate material was deposited using electron beam induced chemical vapor deposition on nanowires. Connections between these electrodes and the metal pads were again made using electron beam induced chemical vapor deposition of platinum metal. The above steps were used to fabricate multiple logic devices including transistors on single nanowires, transistors on spaghetti of nanowires, multiple transistors on a single nanowire and ring oscillator architectures.

5 Summary and Future Work

Focused energetic beams of electron and ions were used to functionalize nanoparticle and nanowire precursors. Commercially obtained nanoparticles were used as nanoparticle precursors. In one of the schemes however, nanoparticles were generated using a nanocluster sputtering system. These nanoparticles were then suspended in gaseous, solid or liquid mediums. Electrospray was developed as a new nanoparticle delivery technique for electrostatic assembly. Electrostatic assembly before that was mostly done for insulator particles. With electrospray charged metallic particles can be generated. This allows the usage of electrostatics to direct the assembly of metallic nanoparticles. Silver nanoparticles dispersed in toluene medium were electrosprayed and assembled on electrified polyamide substrates.

Future electrostatic assembly work would be directed towards the development of an in-situ source for nanoparticle delivery. It is planned to use electrospray and/or a nanocluster source for this purpose. Currently, electrospray is being used in atmosphere for nanoparticle delivery. It is proposed to interface this system with the FEI DB Strata235 vacuum system to develop a system that can perform a single pump down fabrication. An in-situ source would also allow feedback to be introduced in the system. Oxford Applied Research's nanocluster source already operates in vacuum. This source generates pure metallic, insulating or semiconducting particles. This would also be interfaced with the dual beam system to develop a scheme for very high purity single pump down fabricator.

A new technique for lithography – "Electrostatic Lithography" was developed. To our knowledge electrostatic lithography is the fastest known electron beam process that currently exists. Electrostatic resist exposure requires as low as $10nC/cm^2$ of electron dose. It is based on the same fundamentals of electrostatic nanoparticle assembly. Once the nanoparticles were assembled on the electret, thermally evaporated metal was subsequently deposited on it. The electret material with the nanoparticles and the metallic film is then ultrasonicated in acetone to remove the nanoparticles and perform lift-off. Metal film in regions where nanoparticles were not present where left standing. Gold lines and pads where fabricated in this manner. Future work in electrostatic lithography would be to use smaller nanoparticles, in order to get better resolution. Currently the exposure tools used FEI-XL30 cannot deliver below $10nC/cm^2$ of electron dose. This is because the lowest dwell time for the electron beam is 10 microseconds at each dwell spot. Installing new apertures in the electron beam column and/or using a tool which has lower electron beam dwell times would allow the delivery of lower dosages. It is expected that electrostatic resist can be exposed at electron doses much lower than $10nC/cm^2$.

GaAs nanowires were grown using the vapor-liquid-solid mechanism on oxide on silicon substrates using gold as a catalyst. These nanowires were lifted-off by ultrasonication into an IPA solution. The solution then randomly dispersed these nanowires on another oxide on silicon substrate. The second substrate had metal pads prefabricated on it using optical lithography. Energetic beam chemical vapor deposition of platinum and TEOS was performed using FEI DB Strata235. Platinum was used as the gate material, source

material and drain material. TEOS was used as an insulator gate-oxide material. Platinum was also used as a connector between transistor electrodes and prefabricated metal pads. Using this scheme, transistor and ring-oscillator architectures were fabricated. Current-voltage measurements performed on these devices confirmed transistor behavior. However, the measured currents were very low. The explained scheme is the least labor-intensive process that currently exists. This would thus allow the fabrication of more complex devices using nanowire and nanotube precursor. Future work would be to fabricate better and more complex devices and to make the process even simpler. To improve the device properties a number of schemes shall be implemented. First of all it is planned to synthesize doped GaAs nanowires. Contact between GaAs nanowires and the energetic beam CVD metal and insulator can be improved by introducing an annealing step in the process. Vertical standing nanowires are also proposed. Contacts to these nanowires would also be made using the energetic beam CVD. Vertical standing nanowires would occupy even lower foot space, thereby giving higher devices per square inch. Figure 5.1 shows a schematic of vertical standing nanowires used to make ring oscillator architectures.
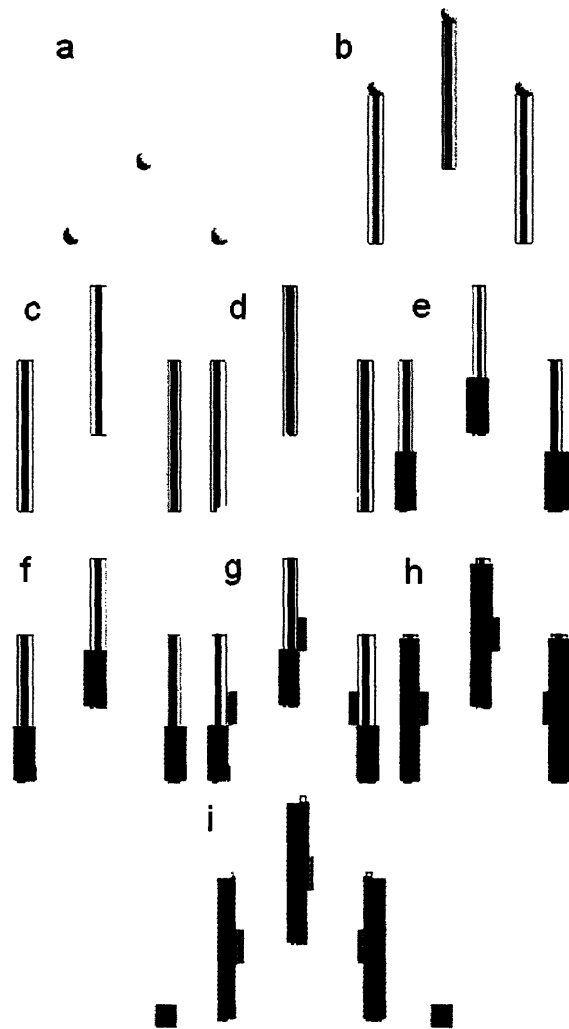
Figure 5.1: Schematic showing the use of vertical nanowires for fabricating a ring oscillator. (a) Gold nanoclusters are deposited on an oxide on silicon substrate (b) GaAs nanowires sheathed by its oxide are grown using vapor-liquid-solid mechanism (c) gold catalysts drops are milled from the top of the nanowires using focused ion beams (d) platinum metal source electrodes are attached to the bottom of the nanowire (e) insulating TEOS is deposited as a spacer material (f), (g) gate material is deposited (h) the entire nanowire is sheathed in TEOS (i) drain electrode are connected to prefabricated metal pads.

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