Solder Self-Assembly for MEMS Fabrication

by

Hin Meng Au

B.S., Mechanical Engineering (2001)
University of Michigan, Ann Arbor

Submitted to the Department of Mechanical Engineering
in Partial Fulfillment of the Requirements for the Degree of

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at the

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Signature of Author.....
Department of Mechanical Engineering
August 6, 2004

Certified by.....
.....
Carol Livermore
Assistant Professor of Mechanical Engineering
Thesis Supervisor

Accepted by.....
Ain A. Sonin
Chairman, Department Committee on Graduate Students

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ABSTRACT

This thesis examines and demonstrates self-assembly of MEMS components on the 25 micron scale onto substrates using the capillary force of solder. This is an order of magnitude smaller than current solder self-assembly in the literature. This thesis also examines self-assembly of high aspect ratio (2:1) microfabricated structures, which poses a greater challenge in terms of alignment and orientation compared to self-assembly of flat structures. The goal of the assembly is to construct a DEP-based cell trap, which consists of sets of high aspect ratio conducting posts on a pyrex substrate, along with electrical connections to the posts.

The posts and substrates are fabricated separately and then combined together through a self-assembly process. The posts are made of silicon and are 25 μm in diameter and 50 μm tall with a thin gold cap on one end to serve as a wetting site. The substrates are pyrex wafers which are patterned with arrays of binding sites and electrical connections, and selectively coated with a low melting point bismuth solder alloy on the binding sites. Self-assembly of the posts onto the substrate is then driven by the free surface energy minimization of solder when the gold-capped ends of the silicon posts come into contact with the solder bumps.

In this project, self-assembly has been successfully demonstrated with a yield of about 50%. However, it also becomes increasingly difficult to control component placement and orientation at these small size scales, because deviations in components and sites from their ideal geometries become relatively pronounced as feature size is reduced. It is observed that post concentration, agitation, and solder wetting of the substrate and posts binding sites are critical for successful assembly. Solder de-wetting, and the peeling of gold caps due to prolonged HF exposure, also limits the yield and the orientation of the assembled posts.

Thesis Supervisor: Carol Livermore
Title: Assistant Professor of Mechanical Engineering

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My most sincere thanks go out to the staff at the Microsystems Technologies Laboratories (MTL), especially Kurt Broderick and Paul Tierney, for their responsiveness and eagerness to help when and wherever possible. I would also like to thank Luis Fernando and Dennis Ward for their invaluable advice on microfabrication processing and recipes. I owe my present fab skills and working knowledge to all these people, Prof Carol Livermore, and many more who have so willingly shared their potpourri of microfabrication experiences.

I would also like to thank Sunghwan for being such a wonderful group-mate all this while. I admire him for his intellect, and I will always relish the myriad diverse and wonderful conversations we have had.

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Last but not least, I would like to thank my parents, Cheong Choy Lin and Au Kok Wing, for putting me through school and for their unbounded love, support and encouragement all these years. Also, I would like to express my heartfelt gratitude to my grandmother Ho Seong, and my aunt and uncle-in-law, Au Oi Sung and Tan Ngak Liang; without their kindness and support, I would not have had the opportunity to pursue an overseas education.

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Chapter 1 Introduction

1.1 Background

The next generation of powerful complex microsystems will require the seamless integration of microelectromechanical systems (MEMS) sensors and actuators with other classes of microcomponents – electronic, optical, and fluidic – onto a single substrate to enable myriad systems-on-chip [1]. There are two possible integration approaches to the above: One would be to microfabricate the components in the desired locations using a serial micromachining 2-D process, and the other approach would be to fabricate diverse microstructures separately and then position and integrate them in the final system using microassembly techniques. At present, the former approach remains a major challenge since the fabrication sequences and material requirements of the different components are often incompatible due to chemical compatibility or fabrication temperature issues. Currently, for the latter approach, there exist several methods focused on microassembly, but each suffers from some limitations. For instance, the serial pick and place process is inefficient with large numbers of components; it is also ineffective with components of dimensions smaller than 100 μm because adhesive forces often dominate gravitational forces on that scale. On the other hand, both micromanipulator-based assembly and wafer-to-wafer transfer methods work poorly on non-planar surfaces, in cavities, and in the fabrication of three-dimensional (3-D) systems [2]. Self-assembly offers an alternative approach to assembling such systems. With self-assembly, free energy minimization drives the system into a desired configuration.

Recently, capillary-based self-assembly has been successfully demonstrated by several groups on the sub-millimeter scale, with lateral dimensions down to 150 μm. The Whitesides' group used a solder-based self-assembly method to fabricate a cylindrical display [2] (Figure 1-1), and the Howe group used a heat-curable acrylate-based adhesive to assemble micromirrors onto microactuators [1,3] (Figure 1-2). The above-mentioned self-assembly methods are intrinsically parallel and offer the potential for submicrometer accuracy in positioning [2].

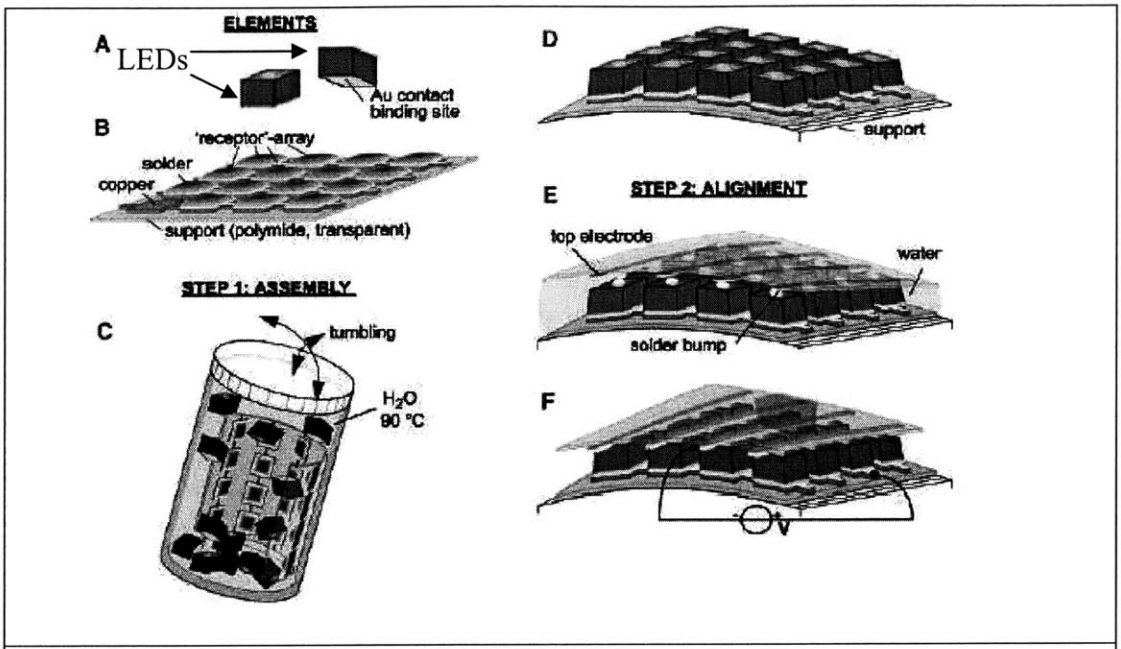


Figure 1-1: Self-assembly (using solder) demonstrated by the Whitesides' group [2]

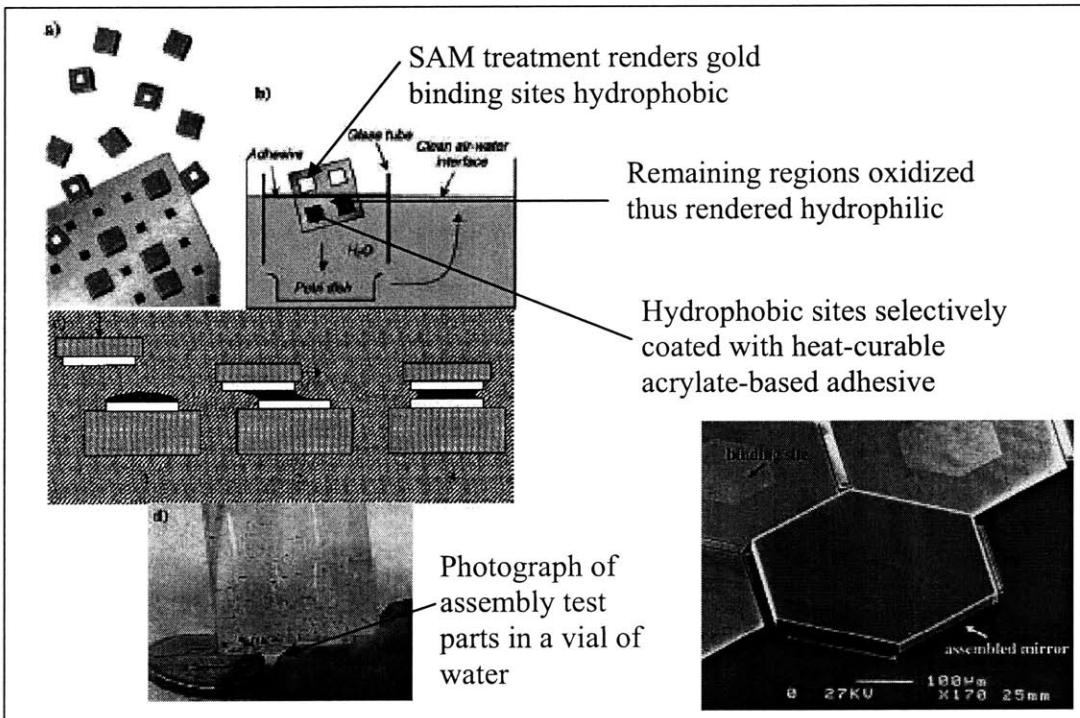


Figure 1-2: Self-assembly (using self-assembled monolayers and a heat-curable acrylate-based adhesive) demonstrated by the Howe group [3]

This thesis strives to improve upon the work done by the previous groups by demonstrating self-assembly of smaller and higher aspect ratio parts onto separately fabricated substrates. The feature size is on the sub-100 μm (10^1~10^2 μm) scale and is an order of magnitude smaller than the parts used in current MEMS self-assembly found in the literature [1,2,3,16]. This project is also motivated by the belief that successful and reliable means of self-assembly will impact the next generation of MEMS by integrating different and previously incompatible regimes, thereby allowing greater flexibility in the design of MEMS and processes. At the same time, by decoupling the current serial micromachining processes (into parallel), more efficient use of materials and lower yield losses can be achieved.

As with all enabling processes, self-assembly should be researched with an application or device in mind, and Prof Voldman's extruded dielectrophoresis (DEP)-based cell trap [4] (discussed below) provides a good avenue for investigating self-assembly. At the same time, this project also aims to alleviate some problems in Prof Voldman's original microfabrication process.

1.2 Extruded DEP cell trap

A DEP-based cell trapping array is used as a cytometer to screen cells for complex behavior [4]. It is designed to have the capability to hold and sort single cells so that assays may be performed on them. The traps use the phenomenon of dielectrophoresis, which is the action of polarizable bodies in a non-uniform electric field, to make electrically addressable potential energy wells as shown in Figure 1-3. An AC field applied to the quadrupole cell trap induces a dipole in the cell, and the driving force will be toward a field minimum (n-DEP) at the center, which traps the cell on the central axis.

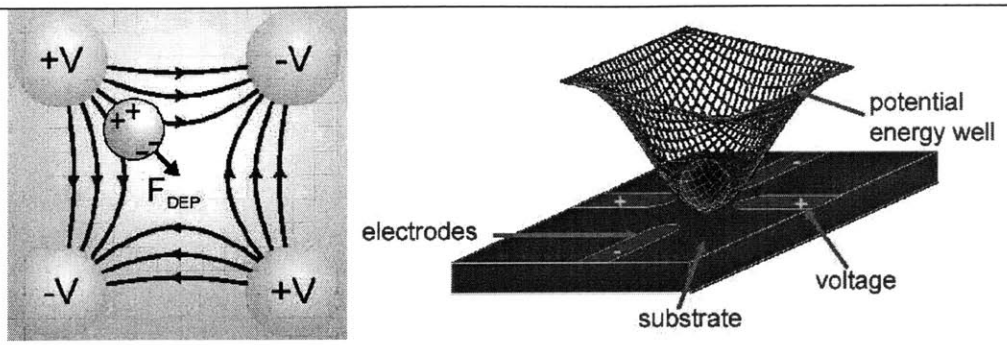


Figure 1-3: Dielectrophoresis and the creation of a potential energy well at the center of the quadrupole due to a non-uniform AC field [4]

The extruded DEP-based cell trap described in Prof Voldman's work [4] consists of arrays of high aspect ratio conducting posts on a pyrex substrate, along with electrical connections to the posts. Figure 1-4 shows the fabrication process for the extruded posts, which essentially involves electroplating into a mold. In step 1, 170 nm of Ti and 500 nm of Au are evaporated onto the pyrex wafer using an e-beam. Following deposition, the substrate interconnect is defined using standard contact lithography and patterned etching of the gold in step 2. The gold is etched using a potassium iodide-based etchant [4], which displays high selectivity to titanium and glass. In step 3, a 60 μm thick SU-8 layer is spun on and patterned, and this forms the mold for electro-plating. SU-8 is an epoxy-based negative photoresist which is useful because it can be patterned with contact photolithography into high aspect-ratio microstructures. In step 4, gold is electroplated into the mold to form the posts and interconnects. In step 5, the SU-8 mold is removed and in step 6, the titanium layer is removed (except for the adhesion layer beneath the gold).

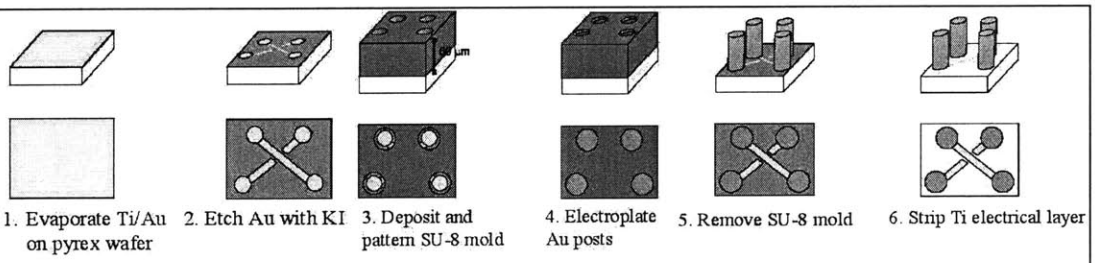


Figure 1-4: Fabrication process for the extruded DEP-based cell trap [4]

The packaging/encapsulation steps will not be depicted here since they are not central to the focus of this project on self-assembly. For more details about the fabrication process, please refer to [4].

1.3 Fabrication issues

There are several problems or issues associated with the above process; these are described in more detail in [4]. Firstly, it is difficult to remove all the organic debris at the bottom of the holes at the end of step 3 due to the thickness of the SU-8 mold. This interferes with the electroplating process in step 4 since a clean gold surface is required for the process to initiate. Ashing helps to improve the yield of post initiation, but it has to be minimized and timed well because overashing will reduce the adhesion of the SU-8 to the substrate and cause underplating. Secondly, SU-8 shrinkage in PGMEA induces stress, causing cracks as shown in Figure 1-5. These cracks can affect adhesion to the substrate and cause subsequent underplating, depending on the pattern and total stress involved. Thirdly, it is difficult to achieve uniformity both in posts' height and width with high aspect ratio electroplating. The post heights varied ~10% across the wafer and showed a slight taper due to the shape of the hole in the electroplating mold [4] (Figure 1-6). Lastly, the Ti layer that provides electrical contact for electroplating needs to be removed or else it will short the posts together. This is done using a dilute $HF:H_2O$ etch, but needs to be endpointed carefully because the titanium adhesion layer under the gold can be undercut, consequently leading to lift-off and yield loss.

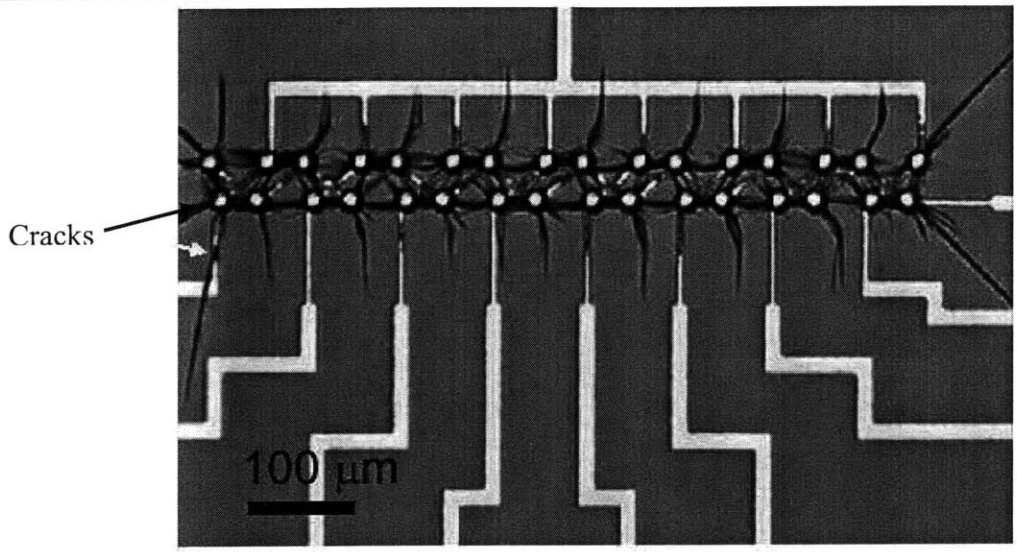


Figure 1-5: SU-8 shrinkage in PGMEA causing cracks [4]

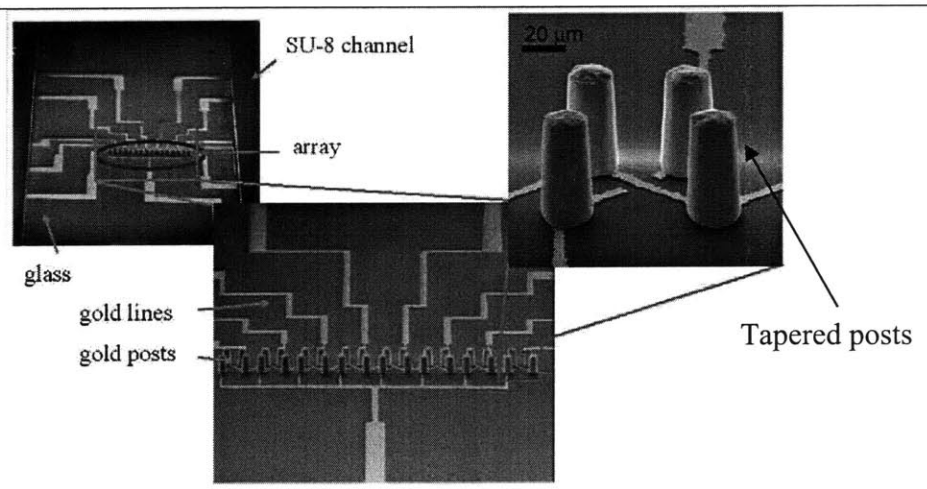


Figure 1-6: Prof Voldman's extruded DEP-based cell trap [4]

1.4 Self-assembly

It is hoped that using a self-assembly process can alleviate some of the above problems by approaching the fabrication from a different standpoint. Through the use of different processes, the posts and substrate can be fabricated separately, thus allowing more flexibility in the choice of materials and processes used. The use of SU-8 and the

electroplating process can be circumvented if the fabrication process for the posts and substrate is decoupled, thereby eliminating the source of the above issues (posts' taper, process irreproducibility, posts' non-uniformity, yield, etc). Also, the posts can be fabricated from a different process other than electroplating and need not be gold, as will be shown in Chapter 2.

In this project, solder is used as the adhesive between the posts and substrate because electrical connections are needed in order for dielectrophoresis to work. Gold is used to define the receptor sites on the substrate because it is easily wetted by solder [5,6,7]. Dipping the patterned substrate into a solder bath will then result in the solder only selectively wetting (and coating) the gold receptor sites on the substrate, and not coating the non-wettable regions elsewhere on the substrate. After that, the solder-coated substrate and posts are placed into a fluid for assembly, and the self-assembly process will be driven by the free surface energy minimization of the solder bumps when the wettable ends of the posts come into contact with the solder bumps on the substrate as shown in Figure 1-7.

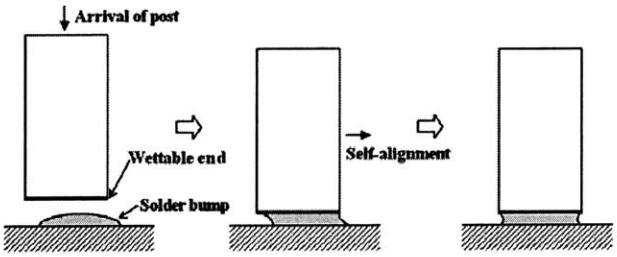


Figure 1-7: Schematic of how the solder self-assembly for the posts works

Chapter 2 Design

2.1 System requirements

In order to ensure functionality of the newly designed cell trap, the following aspects that should be fundamental to both systems (old and new) are identified. Firstly, the substrate or chip has to include a flow chamber for biological fluids. Secondly, thin film electrodes and interconnects are required in order to apply an externally driven AC field to the quadrupole array of posts. Lastly, the posts have to be extruded (50 μm tall), uniform in size and height, and electrically connected to the electrodes. One of the objectives is to eliminate the taper observed in the previous gold posts.

2.2 Design of cell trap

The glass (Pyrex 7740) substrate is adopted from the previous design since it has good rigidity and is also a commonly used biocompatible material. More importantly, it is not wetted by solder, thus requiring only the patterning of (wettable) gold receptor sites on the substrate.

A new process is created to fabricate the posts. Instead of building the posts from bottom up (i.e. through multiple layer deposition or growth), the posts can be etched down into a substrate and then released for collection. In micromachining, it is often easier to etch to a large depth than to deposit a film of the same thickness. The idea of using silicon as the posts' material evolved since there are many well-developed processes for silicon micromachining and also due to the availability of SOI (silicon on insulator) wafers. SOI consists of a device (or mechanically active) layer of single crystal silicon on an intermediate (sacrificial) layer of silicon dioxide grown on a silicon substrate (handle wafer). The MEMS structures are usually defined by vertical plasma etching in the device layer, and locally released by using HF to etch the sacrificial oxide layer [6]. In these experiments, the posts are etched in an SOI wafer. This approach allows quick and large scale fabrication of high quality posts with which to examine the self-assembly

process on this size scale. However, the relatively high cost of SOI wafers would make this economically not viable for commercial applications. Another source or method for fabricating the posts would then be required when a stable and reliable self-assembly process is developed.

Figure 2-1 shows a close-up of the geometry and layout of the new cell trap. The array consists of interdigitated fingers of metallic interconnects which has an AC voltage of reverse polarity applied to alternate lines. The interdigitated fingers do not meet, or else the system will short. The receptor sites are connected by the interconnecting lines, and this wiring pattern creates the quadrupole pattern over arrays of arbitrary size. The aim of this project is to position the posts in the given configuration on the receptor sites through self-assembly, with the solder providing the adhesion and electrical connection. The circled region in the figure shows an effective cell-trap.

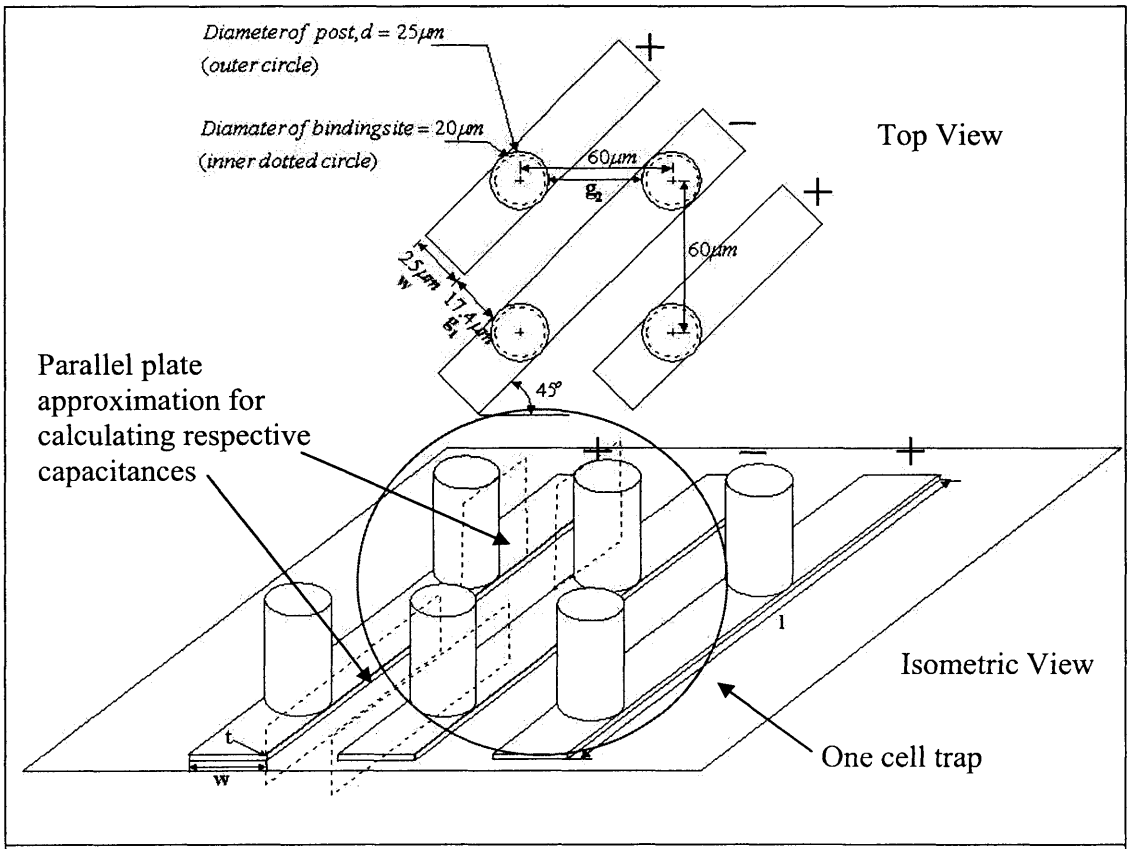


Figure 2-1: Schematic of how the solder self-assembly for the posts works

However, the feasibility of the system using silicon posts has first to be determined from its RC time, which needs to be faster than the high frequency AC field driven at 10's of MHz [7]. A rough approximation of the RC time is made by considering the resistance and capacitance of the electrodes (interdigitated lines) and posts. A parallel plate approximation is used to simplify the capacitance calculations for both the electrodes and the posts, which will yield a conservative (long) estimate of the RC time. In this approximation, features are replaced by parallel plates at the point of closest approach as shown in Figure 2-1. Tables 2-1 and 2-2 list the important parameters and show the results of the calculations using Equations 2-1 to 2-3:

$$R = \frac{\rho l}{A_{flow}} \tag{2-1}$$

$$C = \frac{\varepsilon A_{plate}}{g} \tag{2-2}$$

$$\tau = R\,C \tag{2-3}$$

where R is the resistance, ρ is the resistivity, l is the length, A_{flow} is the cross-sectional area of flow, C is the capacitance, ε is the permittivity of glass, A_{plate} is the area of the capacitor plate, g is the dielectric gap distance between parallel interconnects, and τ is the RC time.

Parameter	**Lines (Au)**
Linewidth of electrode/interconnect, w	25 μm
Thickness of electrode/interconnect, t	100 nm
Dielectric gap distance between parallel interconnects, g_1	17.4 μm
ε	$4\varepsilon_0$
Length of interconnect, l_1	Ranges from 0.1 mm to 10 mm (use a high value, 10 mm, for a conservative estimate)
Capacitance $C = \frac{\varepsilon w l_1}{g_1}$	**5.1×10^{-13} F**

Resistivity ρ_{Au}	2.44 x 10^{-8} Ω.m
Cross-sectional area $A_{plate} = t\,w$	2.5 x 10^{-12} m^2
Resistance $R = \frac{\rho l_1}{A}$	**97.6 Ω**
***RC* time**	**5.0 x 10^{-11} s**
Table 2-1: RC time for Au electrodes	

Parameter	**Posts (Si)**
Diameter of post, d	25 μm
Length of post, l_2	50 μm
Area used in parallel plate approximation, $A_{plate} = \frac{\pi d l_2}{2}$	2.0 x 10^{-9} m^2
Dielectric gap distance between adjacent posts (edge to edge), g_2	40 μm
ε_0	8.85 x 10^{-12} F/m
Capacitance $C = \frac{\varepsilon A_{plate}}{g_2}$	**4.3 x 10^{-16} F**
Resistivity ρ_{Si}	Ranges from 8 x 10^{-5} to 2 x 10^{-4} Ω.m (use the higher value, 2 x 10^{-4} Ω.m, for a conservative estimate)
Cross-sectional area $A_{flow} = \frac{\pi d^2}{4}$	4.9 x 10^{-10} m^2
Resistance $R = \frac{\rho_{Si} l_2}{A_{flow}}$	**20.4 Ω**
***RC* time**	**8.9 x 10^{-15} s**
Table 2-2: RC time for Si posts	

Assuming a minimum driving frequency of 1 MHz, the RC time needs to be much less than 10^{-6} sec for the signal to reach the posts. The results in Tables 2-1 and 2-2 show that the RC times using the gold interconnect lines and silicon posts are many orders of

magnitude below the 10^{-6} sec limit due to the small length-scale of the system, thus ensuring the feasibility of using silicon posts and the above given linewidth/space in the new system.

Three masks were designed: two for the substrate fabrication and one for the posts fabrication (from the SOI). Figure 2-2 shows a single array of traps from the first mask (clear-field) used for patterning the interconnect lines, and Figure 2-3 shows a single array from the second mask (dark-field) used for patterning the gold contact pads for the solder coating. Figure 2-4 displays what an array pattern should look like under a microscope at the end of the fabrication. Figure 2-5 shows the superposition of the two masks for the substrate fabrication, and the critical dimensions for the array. A 4" pyrex wafer having undergone successful completion of microfabrication contains 6 full-sized actual chips, each with 8 arrays of receptors sites, and 6 dummy chips for testing and solder characterization.

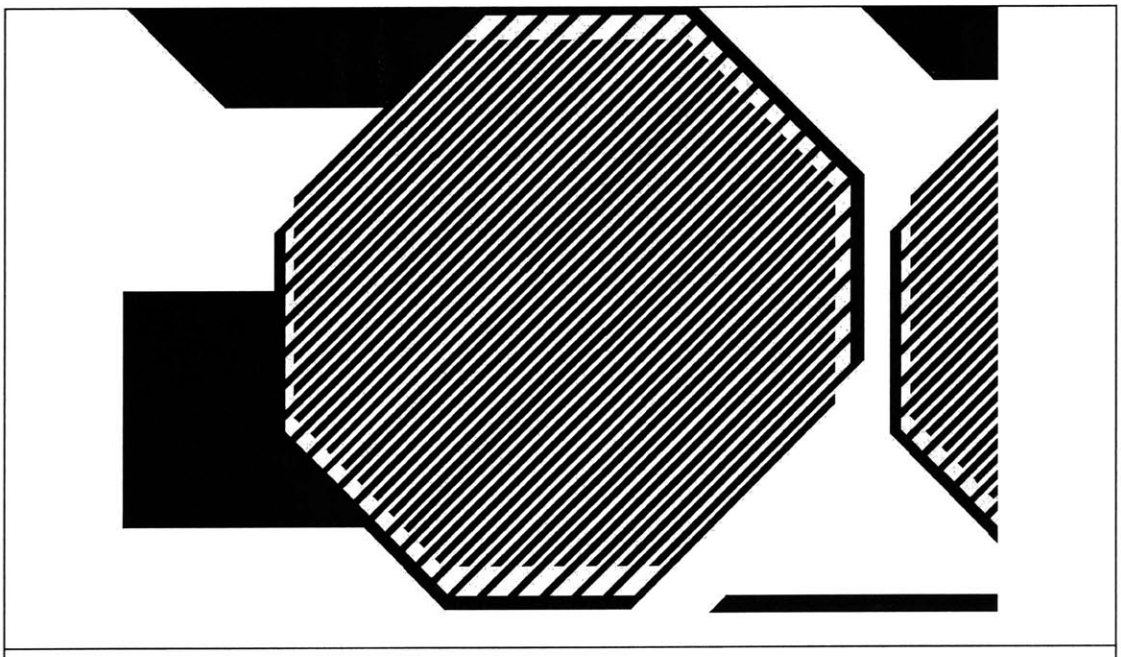


Figure 2-2: Clear-field mask (zoom-in view) for fabricating the interconnect lines on the substrate

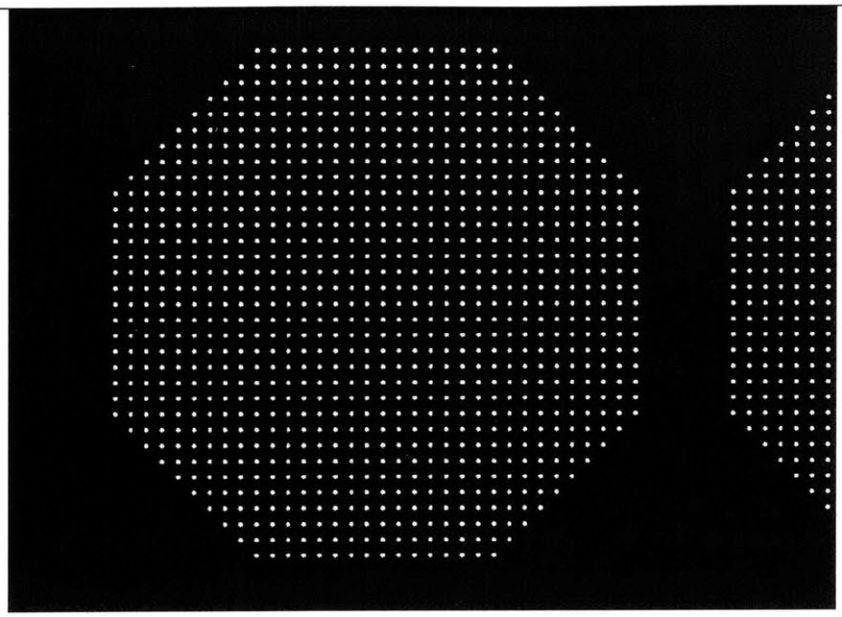


Figure 2-3: Dark-field mask (zoom-in view) for fabricating the contact pads (binding sites) on the substrate

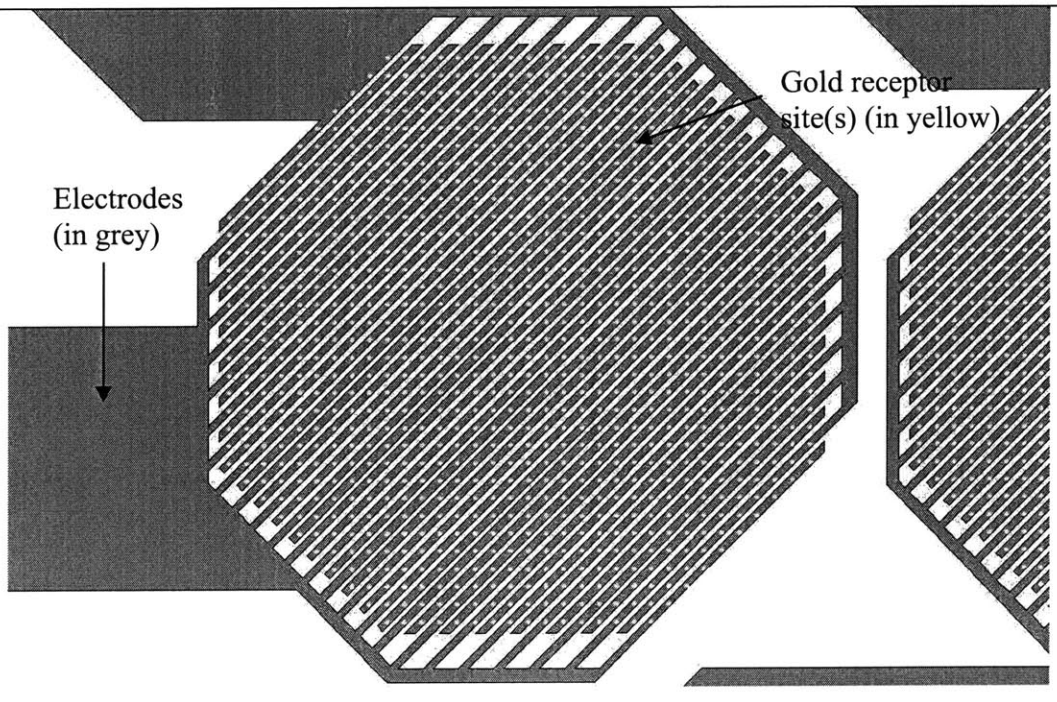


Figure 2-4: Schematic of how the substrate should look like at the end of the fabrication

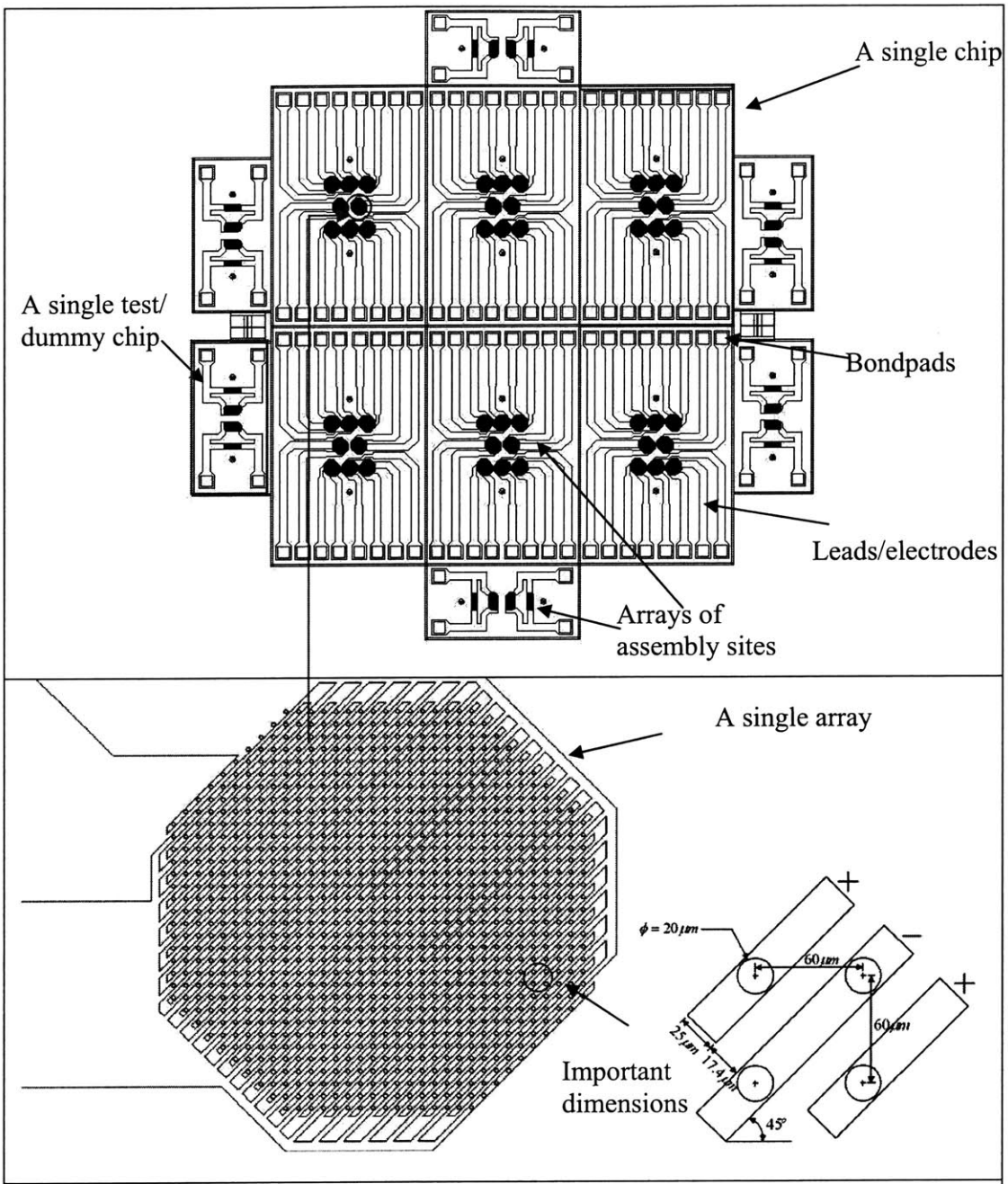


Figure 2-5: Overlay of substrate fabrication masks with details

Chapter 3 Device fabrication

3.1 Design of fabrication processes

The cell trap primarily consists of posts, and substrates, and the material providing the capillary force for self-assembly, which is a low melting point bismuth alloy (Small Parts, Miami Lakes, Florida, LMA-117 [15]). In this chapter, the fabrication processes for the posts and substrates will be listed in detail. The micromachining processes used are serial and inherently 2-D in nature, and involve a series of steps such as photolithography, thin film deposition, and etching. The posts and substrates were fabricated using the clean room facilities in the Integrated Circuits Lab (ICL), Technology Research Lab (TRL), and Exploratory Materials Lab (EML), all collectively coming under the MIT Microsystems Technologies Laboratories (MTL).

3.1.1 Silicon posts fabrication

The starting materials for making the silicon posts are 6" SOI (silicon on insulator) wafers. The posts are defined by vertical plasma etching in the device layer, and locally released by using HF to etch the sacrificial oxide layer. The specifications of the SOI wafers (Ultrasil Corporation, Hayward, CA) used are given in Table 3-1. The key parameters to note are the device layer resistivity which needs to be low (i.e. highly-doped) so that the resistance of the posts is low to allow good conductivity, and the device layer thickness which determines the height of the silicon posts in the cell traps. The 2 μm buried oxide layer is sufficient to act as an etch stop for the deep reactive ion etching (DRIE) process since it has etch selectivities ranging from 120 to 200:1.

Size (mm)	150±0.2
Type / Dopant	N / Sb
Orientation	<100>
Device thickness (μm)	50±2

Device resistivity (Ω-cm)	0.008 to 0.02
Buried oxide thickness (μm)	2
Handle wafer thickness (μm)	600±20
Handle wafer resistivity (Ω-cm)	0.01 to 0.05

Table 3-1 : SOI wafer specifications

The fabrication processes for the silicon posts can be broadly divided into photolithography, plasma etching, electron-beam evaporation and wet processing such as HF etch release and metal lift-off using acetone. The processing will be detailed in the following sections, as well as any special steps taken for precaution.

A brief overview on photolithography is given because it is the key method for pattern transfer and comprises a major portion of the processing. Lithography is the process in which patterns on the mask are transferred onto the substrate by selectively exposing (and developing) areas on a light-sensitive photoresist. An overview of a standard lithography process is depicted in Figure 3-1.

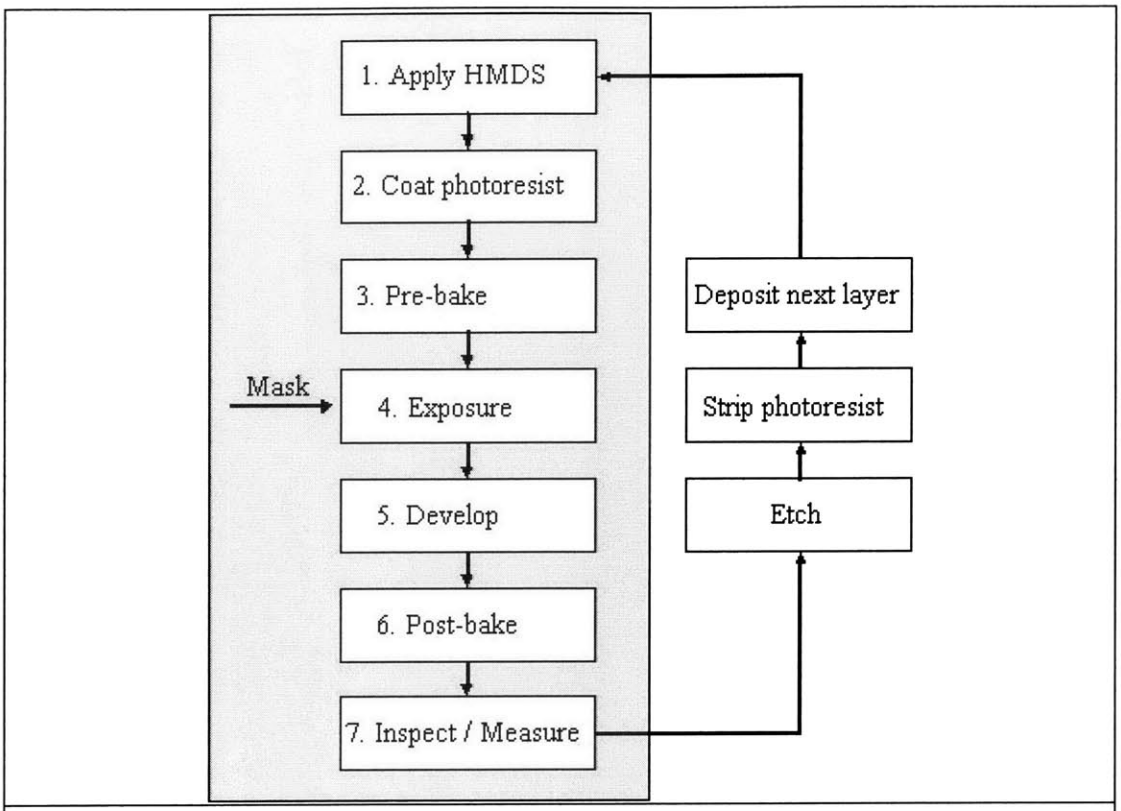


Figure 3-1: Standard lithography process (in yellow area)

Figure 3-2 shows the mask for the posts fabrication, and also lists the important dimensions. The close-up of a corner of one die is shown in the lower half of the figure, which indicates that it is clear-field within each die (the total number of dies on a wafer is 32) and dark-field outside of the dies.

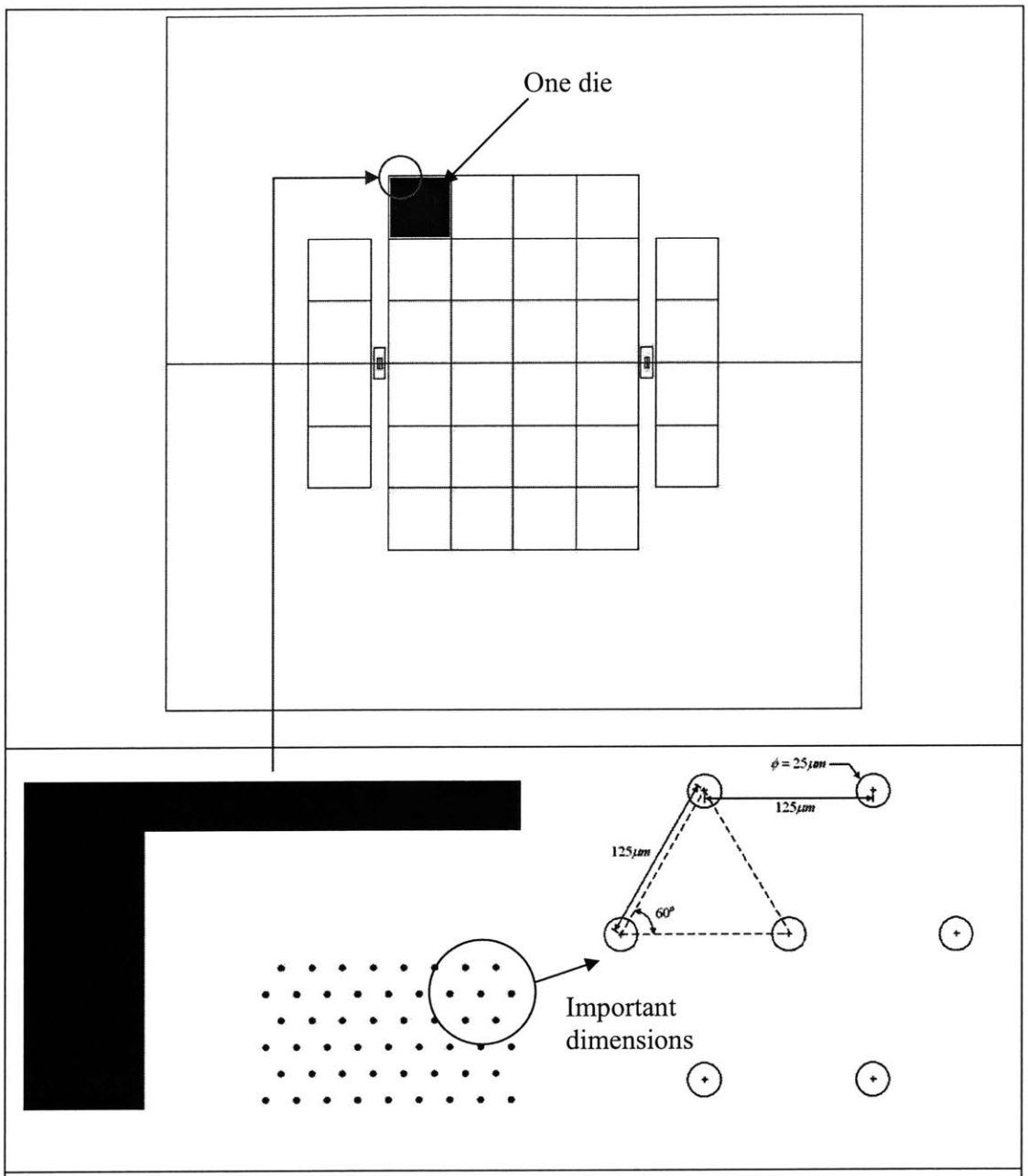


Figure 3-2: Mask layout for the posts fabrication

(The die layout is shown in the upper half of the figure, and a close-up view of some posts is shown in the bottom half)

Figure 3-3 shows the process flow for the posts fabrication.

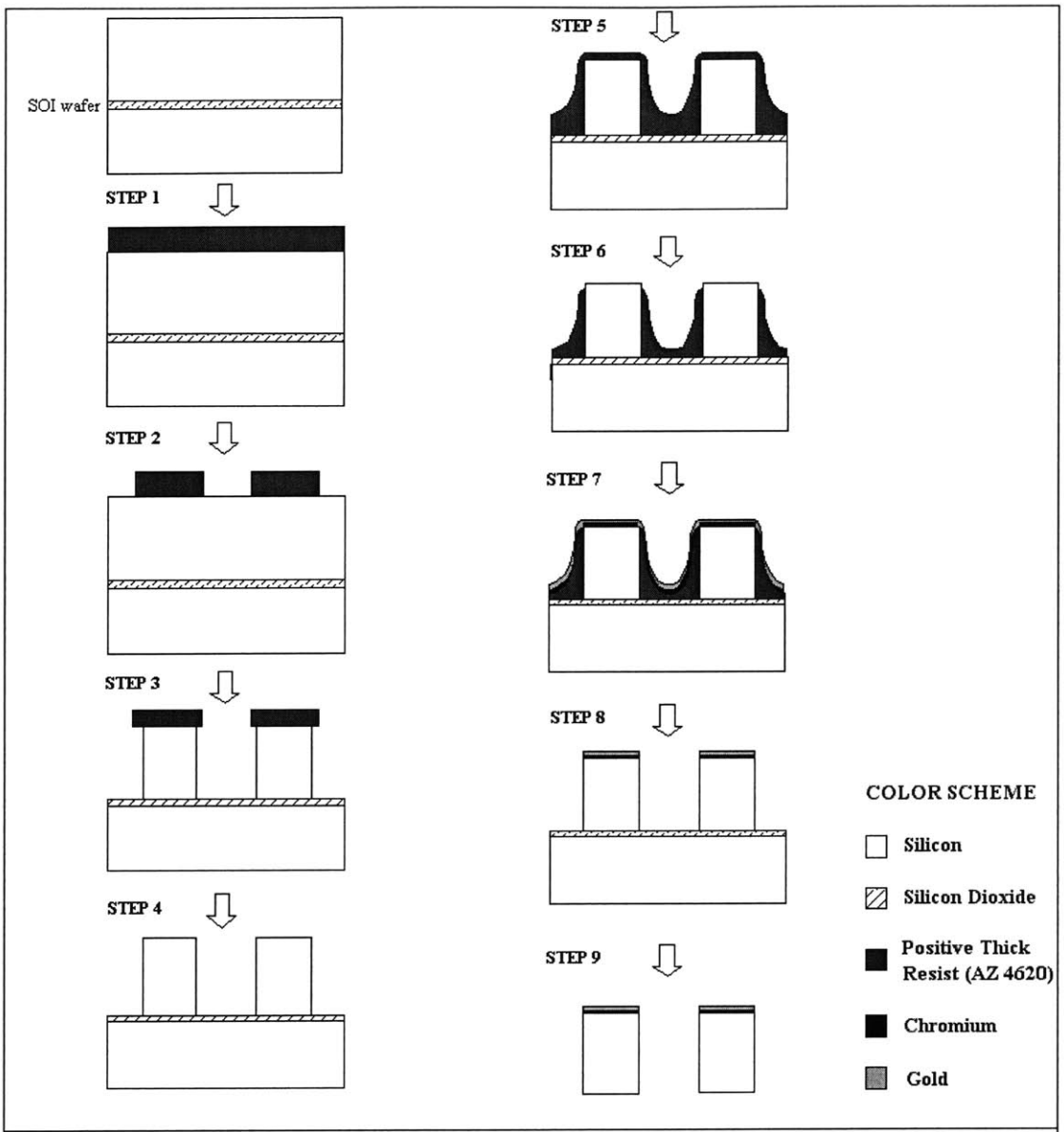


Figure 3-3: Process flow for posts fabrication

In step 1, the SOI wafers are first put into the HMDS oven in the TRL for a 15 minute dehydration bake to dry off the water. Next, the wafers are primed with hexamethyldisilizane (HMDS) which is an adhesion promoter for the photoresist. HMDS converts the hydrophilic native oxide layer on the silicon wafer to create a hydrophobic surface, to which the photoresist will adhere readily. For AZP 4620 positive thick photoresist, recipe 3 in the TRL HMDS oven (60 secs HMDS dispense) is used which gives a photoresist contact angle of 55^{o} after the bake, exposure and development. After

allowing the wafers to cool for five minutes, AZP 4620 thick resist is dynamically dispensed onto the wafer in the TRL coater at 1750 rpm for 12 secs, followed by spreading of the resist at 3500 rpm for 60 secs, and finally a spin of 5000 rpm for 10 secs. The spreading speed determines the thickness of the AZP 4620 resist which is about 7 μm after post-bake. The spread speed (giving this thickness of the photoresist) is chosen due to the type of photoresist available in the TRL, which does not have photoresist of intermediate thickness range from 2 to 5 μm. It is difficult to achieve good resist coats at high speeds due to the vortices, which introduces resist non-uniformity and defects. The above photoresist recipe is used because it gives uniform, consistent resist coats with few defects. The final 10 secs high speed spin helps to reduce edge-beads which form at the circumference of the wafers during thick resist coating. In addition, holding a fab swab 5 to 10 mm away from the edge of the spinning wafer during the coating process helps to reduce particles, edge-beads, and other defects on the resist coat. Before coating the actual SOI wafers with the resist, the process is carried out on a dummy silicon wafer to practise obtaining a good photoresist coat, which is often dependent on the eccentricity of the wafer on the vacuum chuck and the centering of the dispensing nozzle tip.

After the resist coating, the Teflon carrier holding the SOI wafers is placed into the TRL pre-bake oven for a 60 minute pre-bake at 95° C. This is to drive off the residual casting solvent from the photoresist film.

In step 2, the wafers are exposed on the TRL EV1, which is an Electronics Visions EV620 Mask Aligner. The exposure system uses a 350-watt high pressure mercury lamp and has an exposure controller with 3 channels: constant power, or constant intensity (CI) 1 or 2. CI 1, set at 10 $mW/cm^2/sec$, is always used, and the wavelengths are 365-405 nm [8]. The exposure settings are as follow:

1. Maskholder size (7") and thickness (3.045mm or 0.12");
2. Substrate size (6"), thickness (0.53mm);
3. Separation distance (45 um),
4. Process (top side) and mode (transparent),
5. Exposure mode (interval),

6. Contact mode (soft contact).

The soft contact mode is usually used for the first mask since no alignment between the mask and wafer is necessary. The exposure is carried out in 3 intervals of 5 sec each with a 5 sec delay in between, giving a total exposure time of 15 sec for the 7 μm thick AZP 4620 resist. The 5 sec delay is to allow the resist to cool down between exposures to prevent resist bubbling.

After exposure, the resist is developed in AZ 440 for about 1 min 45 secs (until the patterns become clear). The developing is done in a beaker just bigger than the wafer, with about ¼" (1/2 cm) of developer. For AZP 4620 thick resist, the developer is agitated in a non-repetitive pattern, as the developing is diffusion rate limited. The wafers are then rinsed with water for 3 mins after the development.

Following development is a 30 minute hard bake at 95° C, which is used to harden the resist against further energetic processes such as plasma etching.

Step 3 uses Deep Reactive Ion Etching (DRIE) to etch the posts in the device layer. DRIE relies on an inductively coupled plasma source and successive cycles of etching and passivation to achieve high aspect ratio silicon structures. The alternating between the etching and passivation steps is known as "TMDE"-Time Multiplexed Deep Etch [9]. The machine used is the STS2 in TRL, which is developed by Surface Technology Systems (STS) using their advanced silicon etch (ASE™) process. A schematic of the STS DRIE etcher can be seen in Figure 3-4. The plasma is created within the plasma chamber, using an induction coil connected to a 13.56 MHz RF source to create excitation of the gas. A second 13.56 MHz RF source is connected to a platen where the wafer to be etched is placed. This second RF source creates a bias between the plasma and wafer which is required for the ASE process. The passivation cycle is to minimize lateral etching of the sidewalls from the highly reactive neutrals of the RIE chemical component. It involves the deposition of a Teflon-like (polymerized CF_2) polymer about 50 nm thick on the side walls and the base of the features by the ionization and dissociation of octaflurocylcobutane (C_4F_8). The chamber is then evacuated of C_4F_8 prior

to the etch step beginning. The etch step introduces SF_6 and O_2 into the chamber, decoupling them into ions and radicals (a neutral species). The ion bombardment rapidly removes the polymer from the horizontal base surface, and serves to enhance the etching process by damaging the silicon surface making it more susceptible to reaction with the fluorine radicals. The sidewalls remain protected by the polymer which receives no ion bombardment (since the ions are columnated), and consequently no chemical etch, either [9]. One drawback is that the process leaves scalloped sidewalls on the features as a result of the multiplexing, as can be seen in Figure 3-10.

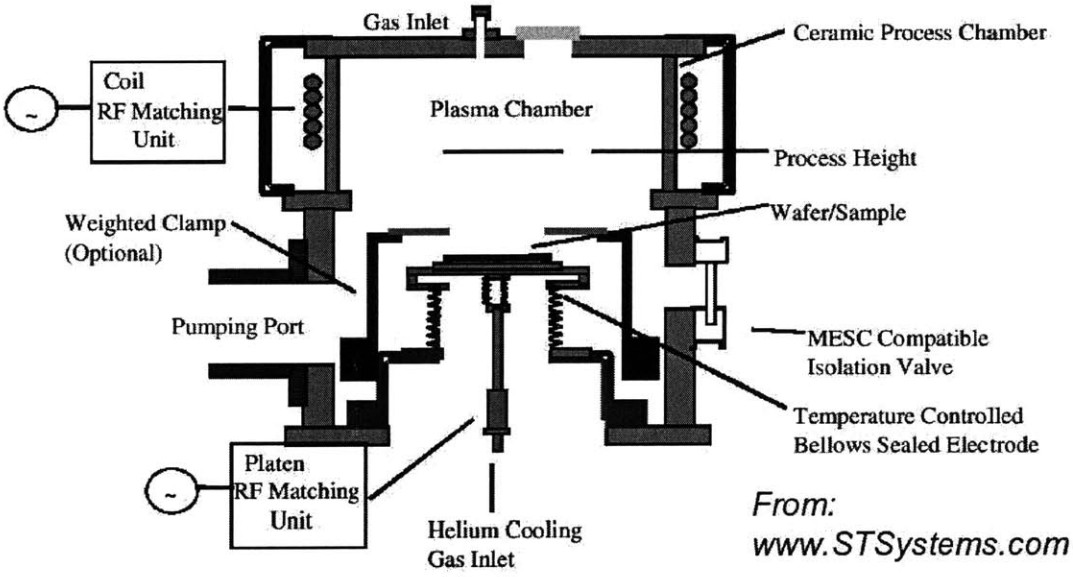


Figure 3-4: Schematic diagram of an STS inductively coupled etch system used for ASE™

The STS2 uses a mechanical clamp made up of eight ceramic 'fingers' to pin down the edge of the wafer and hold it onto the chuck. The chuck provides He backside cooling to the wafers. This keeps the wafer cool enough during the plasma process so that the resist does not etch too quickly (selectivity to silicon is about 75:1), and also to minimize resist burning [10]. The wafer to chuck interface is aided by a lip seal which stops the He from leaking into the chamber and changing the etch rate. As such, the backside of the wafers needs to be clean of resist or debris which if present will break the seal. If the pressure on the screen is greater than 15 mtorr/min (indicating a high He leak-out rate), the

process will not begin and the backside of the wafer needs to be cleaned of particles or resist using a fab swab dipped in methanol in the solvent hood. After cleaning with methanol, it is good practice to put the wafer into the pre-bake oven for one or two minutes to drive off any remaining solvent before putting it into the STS2 chamber for subsequent etching. It is suspected that trace amounts of solvents remaining on the wafer may contribute to patches of photoresist scum on the wafer surface during the etch.

The recipe used is <OLE3>, which is a variation of <MIT37_A>. <MIT37_A> is a recipe that reliably yields vertical sidewall profiles and good etch uniformity between small and large features. The profile of the etched silicon posts needs to be straight and is important since one of the objectives of this project is to reduce post taper and to produce more uniform posts. The recipe for <OLE3> is given in Table 3-2. The <OLE3> recipe is first run on a patterned silicon dummy wafer to determine the etch rate. This is because the etch rates for the STS2 vary both across the wafer (macroscopic non-uniformity) and for different mask layouts and geometry (microscopic non-uniformity) [11]. For better etch uniformity, the wafer is rotated after each time interval. The total etch depth after each time interval is shown in Table 3-3.

	General settings	**Parameter**
Process	Pump down time	20 secs
	Gas stabilisation	10 secs
	Process time	Entered by user based on etch rate and desired etch depth
	Process pressure (mTorr)	31 mTorr
	Pump out time	30 secs
Order (etch first)	Etch step	14
	Passivate step	12.5
Gas Flows	C_4F_8 (sccm)	SF_6 (sccm)
Etch step	0	140
Passivate step	95	0
RF power	Platen generator	Coil generator

settings		
Etch step	140 W	600 W
Passivate step	0 W	600 W

Table 3-2: <OLE3> recipe, STS2

Etch pass	Time (min)	Etch depth (μm)	Etch rate (μm/min)
1	20	15	0.75
2	20	28	0.65
3	15	40	0.8
4	13	50	0.77

Table 3-3: Typical etch rates for <OLE3> using the mask layout in Figure 3-2

From the above table, it is seen that it takes 68 mins to etch 50 μm of the silicon dummy wafer. The average etch rate is calculated to be about 0.74 μm/min. From this test, a ballpark estimate of the time required to etch the silicon posts on the SOI in the STS2 is obtained.

For the etching of the SOI wafer, it is ensured that each process interval ended on an etch step instead of a passivation step. The system is vented and the wafer is rotated between etch time intervals; typical time intervals are (17:53, 17:53, 17:53, 13:53). The first glimpse of the buried oxide layer is observed 3 mins into the third interval. The oxide layer has a purple color and the etch front is seen to advance inwards from the edge of the wafer, which means that the outside etches faster than the inside. This "bulls-eye" pattern is usually due to depletion effects as the gas flows from the outside of the wafer to the inside [11]. Since the etch pattern on the wafer is uniform, microloading is not an issue. Microloading occurs when etch rates vary over small distances on the surface of the wafer due to differences in the density of the unmasked area [11]. Because of nonuniformities in the etch rate, a certain amount of overetching is done to ensure that complete etching is achieved everywhere on the wafer. This is often 10-20%, in terms of time, past the endpoint detection [11]. For etching the posts in this project, the endpoint

detection is when most of the field is etched to down to the oxide and is visible (by color), and the etch is not extended beyond the endpoint detection. This is because when using the STS plasma etcher to etch SOI wafers, there is a problem known as "notching" as the plasma etches through to the oxide layer [9]. Notching takes the form of cavities at the base of the etched features adjacent to the oxide layer. This is caused by a charging effect on the oxide layer which scatters previously columated ions into the sidewalls, causing impact damage to the sidewalls in local proximity to the oxide layer. When the following passivation layer is deposited, it is unable to completely coat the newly created cavity and therefore does not protect the damaged areas from further chemical etching, thus enhancing the impact damage [9].

Figure 3-5 shows an SEM micrograph of the base of etched silicon posts on a plain silicon dummy wafer, and Figure 3-6 shows an SEM micrograph of the base of etched silicon posts on an SOI wafer. For the dummy wafer, the silicon continues to be etched because there is no etch stop, and this results in a sloped profile at the base of the silicon posts. For the SOI wafer, vertical etching slows down considerably at the buried oxide etch stop layer, but lateral etching at the base of the posts continues due to notching.

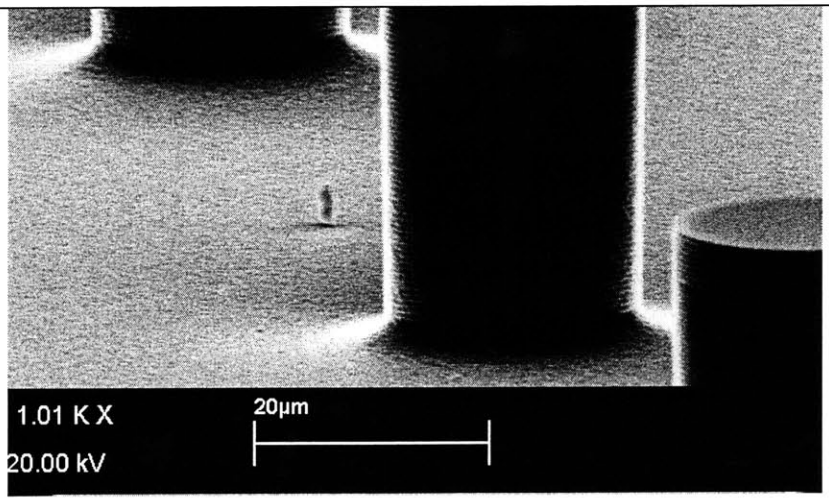


Figure 3-5: Base profile of etched silicon posts on a dummy Si wafer

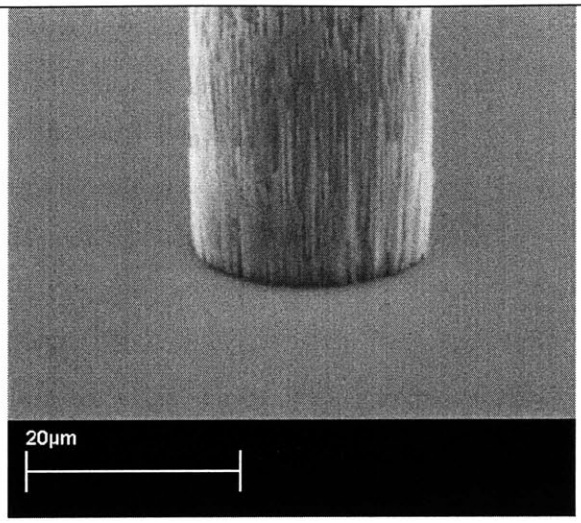


Figure 3-6: Base profile of an etched silicon post on an SOI wafer

In step 4, after the SOI wafers have been etched to completion, they are immersed for 10 mins in a glass beaker containing a solution of 3 H_2SO_4 : 1 H_2O_2 in the acid-hood. This solution is commonly known as "Piranha" and is used to strip photoresist off wafers and for general wafer cleaning. After the photoresist is removed, the wafers are rinsed for 3 cycles in the dump-rinser and then spun-dry.

To remove the Teflon-like polymer on the sidewalls of the silicon posts, the SOI wafers are ashed for 30 mins in the TRL asher. This dual-barrel downstream asher uses an oxygen plasma generated by a 1200 W 13.56mHz RF power supply to remove organic films and contamination from wafers by exposing them to the chemical reactivity and kinetic energy of oxygen ions [8]. After the chamber pressure has stabilized to 0.09 mm Hg with both the vacuum and oxygen switched on, the RF forward power dial is adjusted to 1000 W.

In steps 5 and 6, photolithography is performed on the etched SOI wafers in preparation for the self-aligned process. The self-aligned process in principle works similar to a lift-off process, except that it does not require a mask and uses the existing topography of the wafer (and the resist) to lay down metal patterns. This potentially leads to cost savings in masks since one mask less is required, compared with the approach of depositing and etching the Pt metal.

No HMDS priming is necessary for this step because the resist adhesion to the substrate and its resistance to etch are not crucial for the self-aligned process. In fact, it works better in the reverse case since it is essentially a variant of the lift-off process. AZP 4620 thick resist is dispensed onto the center of the stationary wafer in the TRL coater for 18 secs and allowed to sit for 10 secs to let the bubbles rise. If insufficient time is allowed to let the bubbles rise, they will manifest as defects on the resist coat. Any visible bubble is lightly removed by a fab swab before the spread cycle at 750 rpm for 10 secs, and then the spin cycle at 1000 rpm for 60 secs. After the resist coating, the SOI wafers are placed into the TRL pre-bake oven for a 60 minute pre-bake at 95° C.

In Step 6, the wafers are flood exposed for 2 secs under the EV1. The theory is that the thin layer of resist on the top of the posts will be fully exposed while the rest of the field will be under or little exposed. Upon developing, the top of the posts will be cleared of resist while most of the field still has a thick layer of resist. The wafers are then developed in AZ 440 for 20-25 secs. Figure 3-7 shows a picture of the wafer at this stage, which has a honeycomb-like pattern due to etch non-uniformity in the regions between the posts. It is advisable to develop first for 15 secs and then inspect under the microscope to see if there is still any resist on the top of the silicon posts. Colored rings on the top of the silicon posts will be observed if resist is still present, as seen on the left of Figure 3-8. If necessary, develop further until the top of the silicon posts is cleared of resist as seen on the right of Figure 3-8. The wafers are then rinsed with water for 3 mins after the development. No further post-bake is necessary.

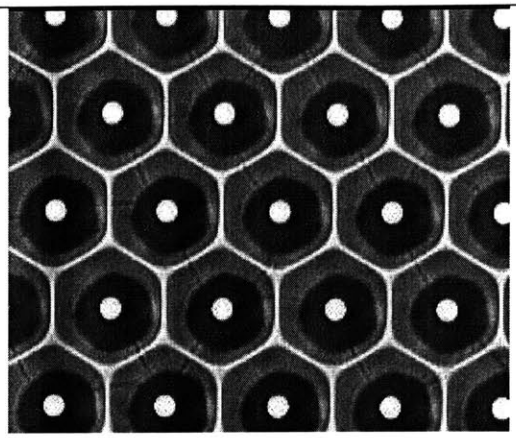


Figure 3-7: Honeycomb-like pattern field

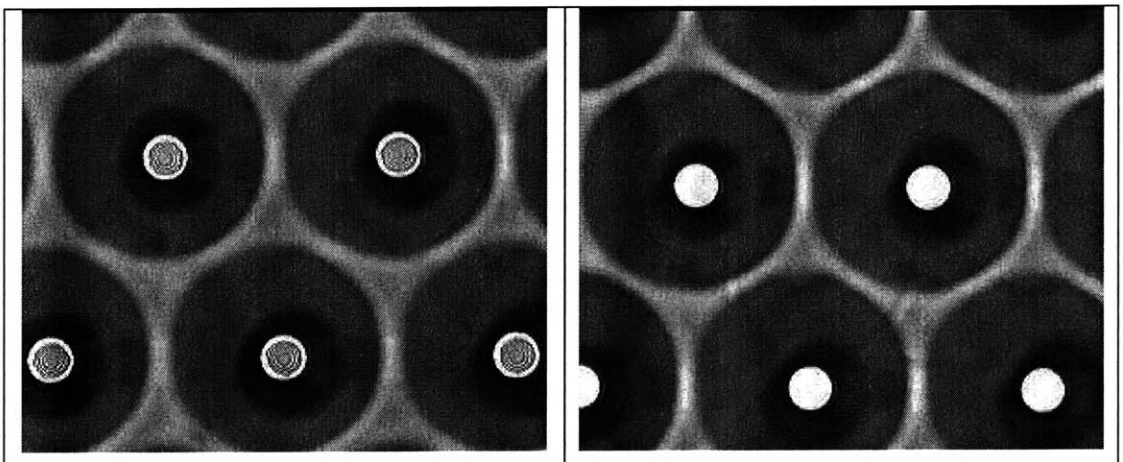


Figure 3-8: Tops of silicon posts showing uncleared resist (left) and clear of resist (right)

Step 7 is the electron beam evaporation of a 10 nm Cr / 120 nm Au layer onto the SOI wafers using the TRL ebeam. The Cr is necessary as an adhesion layer for Au, which is a relatively non-reactive noble metal. An electron beam (10 keV, 200 mA) is scanned over the Cr and Au targets respectively in a vacuum chamber at $2x10^{-6}$ Torr, generating a vapor for deposition [8]. The step coverage for electron beam evaporation is poor because of the molecular ballistic flow of the evaporated atomic flux (long mean free path) in the vacuum chamber [12]. This is useful for our purpose since we only want metal caps on top of the posts and not on the sidewalls. Furthermore, the poor step

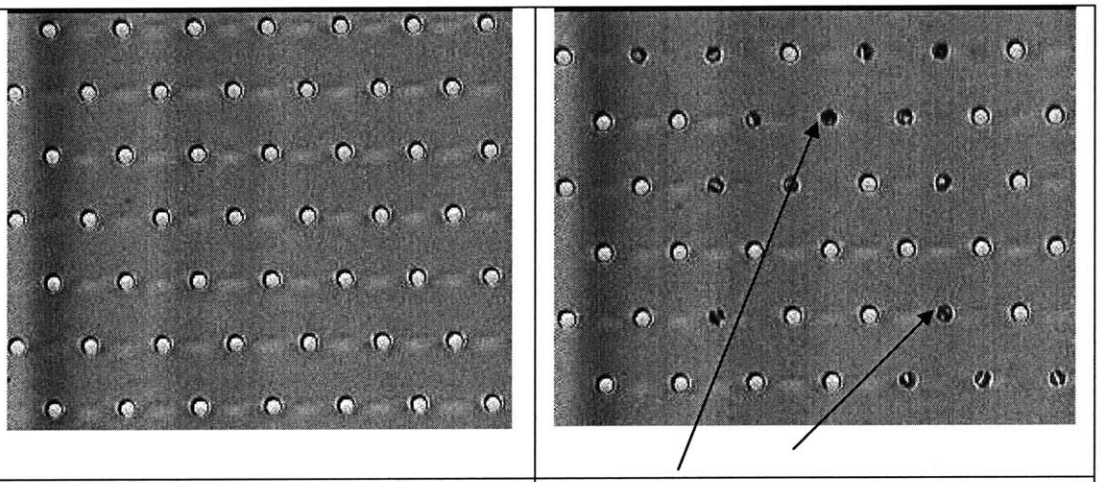
coverage aids in the subsequent lift-off process, which would be very difficult if the film were conformally deposited, for instance, using sputtering. Sputtering is not used because of the high baking temperature and considerable heating of the substrate from the secondary electrons emitted from the target, which hardens the photoresist and makes it difficult to remove for the metal lift-off. The parameters for the Cr and Au evaporation process are shown in Table 3-4. The lift-off plate is used instead of the planetary carrier, and to achieve a more uniform coating, the lift-off plate is rotated using a motor during the deposition.

Process	**Chromium**	**Gold**
Rise time (min)	1.3	2
Soak time (min)	2	2.3
Predeposit time (min)	0.3	1.3
Setpoint	0	0
Soak power (%)	15	15
Predeposit power (%)	16	16
Maximum power (%)	18	25
Idle power (%)	0	0
Deposition rate (A/sec)	**2**	**3**
Thickness (kA)	**0.1**	**1.2**
Source/sensor	11	11
Response	15	10
Error limit	10	10
Tooling (%)	61	55
Density of material	7.2	19.3
Acoustic impedance	28.9	23.18
* Make sure crystal health is greater than 85% before starting process		

Table 3-4: Process parameters for electron beam evaporation of Cr and Au

Step 8 is the lift-off patterning of the Cr/Au caps on the tops of the silicon posts. The thick resist field acts as a "sacrificial" mask, and is dissolved in acetone, in the process

"lifting off" the unwanted metal. The lift-off is carried out in an ultrasonic bath to speed up the process. After most of the field is clear of Au (and resist), the SOI wafers are rinsed in methanol, followed by isopropanol, and then water. Care must be taken not to allow the acetone on the SOI wafers to dry while transferring the wafers between beakers for cleaning, because this will make the Au debris and resist scum stick onto the wafers, where it is very difficult to remove in the subsequent cleaning steps. The left-hand side of Figure 3-9 shows a picture of the silicon posts with Cr/Au caps after the lift-off. The Au color will be a distinct gold/yellow when observed under the microscope. The right side of Figure 3-9 shows the loss of some silicon posts (< 5%) due to the energy of the ultrasonic agitation. Figure 3-10 is an SEM micrograph showing the Cr/Au cap on the top of a silicon post.



Before ultrasound agitation	Loss of posts after ultrasound agitation

Figure 3-9: Silicon posts with Cr/Au caps after lift-off process

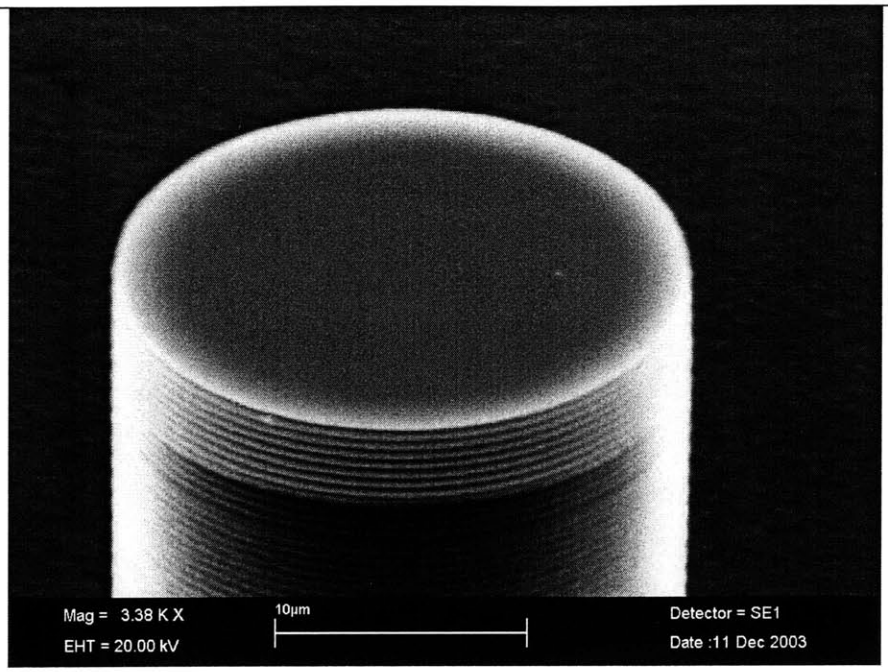


Figure 3-10: Cr/Au cap on top of the silicon post

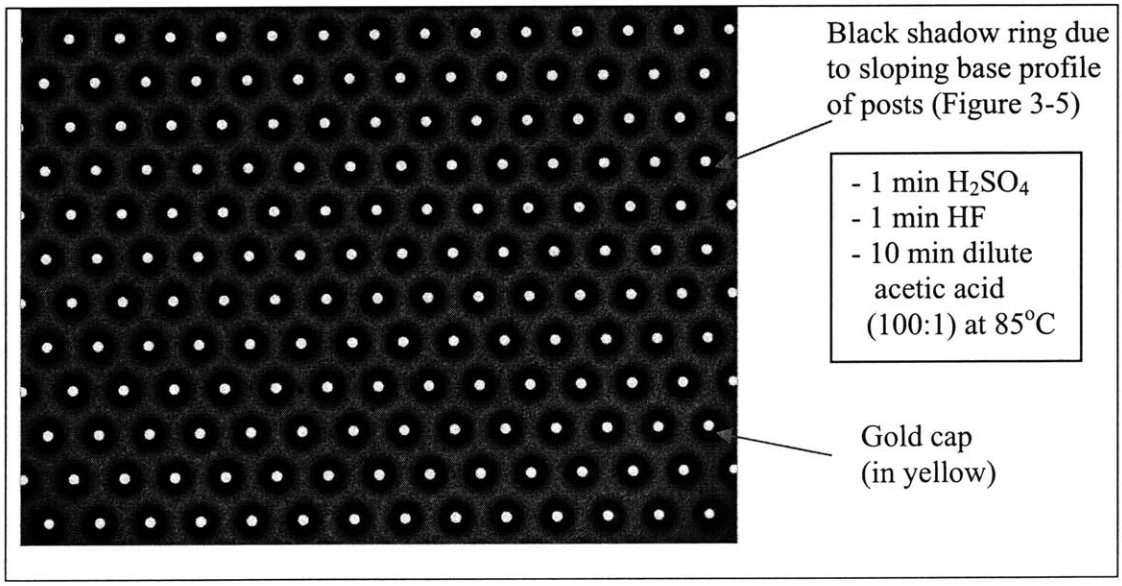
Between steps 8 and 9, the dicing of the SOI wafers is carried out in the ICL packaging room. The wafers are first coated with AZP 4620 thick resist (followed by a 1/2 hr pre-bake at 90°C) to protect the silicon posts and Cr/Au caps prior to the die-saw. Before beginning the die-saw, it is necessary to check if the correct blade (thick silicon blade – 220 μm) is on the spindle and that it is clamped properly. The wafer must also be mounted carefully on the adhesive tape to minimize air gaps between the bottom of the wafer and the tape. If there are large air gaps, the wafer piece will shift or lift during the die-sawing process, and this will lead to both wafer and blade damage. All the above precautions are necessary to make clean cuts and for safety reasons. The standard cutting speed for silicon wafers (0.0031 inches/sec) is used [8].

After die-sawing the wafer into 32mm x 32mm chips, the protective photoresist on the chips is removed using acetone. The chips are then rinsed with methanol, IPA, and water in the EML solvent hood.

Prior to the HF release of the silicon posts on the SOI wafers in step 9, a test is conducted on dummy silicon chips with gold-capped posts to see how the Cr/Au caps withstand HF

attack. This is important because HF is used to release the posts from the substrate, and it is necessary that the Cr/Au caps not be removed in the process. The Cr/Au caps are necessary for the solder to wet and for the self-assembly of the posts to take place. It is found in literature [13] that Au is not etched by HF, while for Cr films, some peeling may be observed. The objective of the test is to determine if the Cr adhesion layer can withstand the HF long enough for the buried oxide layer to be etched and the posts released, without peeling off and lifting off the Au cap with it. Posts without Au caps are rendered useless because they will not be wetted, and these constituted a large proportion of the posts in early batches when little was known then about the effect of the acids on the caps.

The dummy silicon chips, which had etched posts capped with Cr/Au, were subjected to the release and cleaning steps that they would undergo under several cleaning scenarios, such as the H_2SO_4 clean, HF release, and the exposure to the water/dilute acetic mixture (flux used in the solder coating and assembly). The H_2SO_4 cleaning protocol is for removing organics which may impede solderability, while the water/dilute acetic mixture acts as a flux for removing oxides on the solder during the solder coating and self-assembly processes. Figure 3-11 shows the time characterization of the effect of HF on the posts' Cr/Au caps.



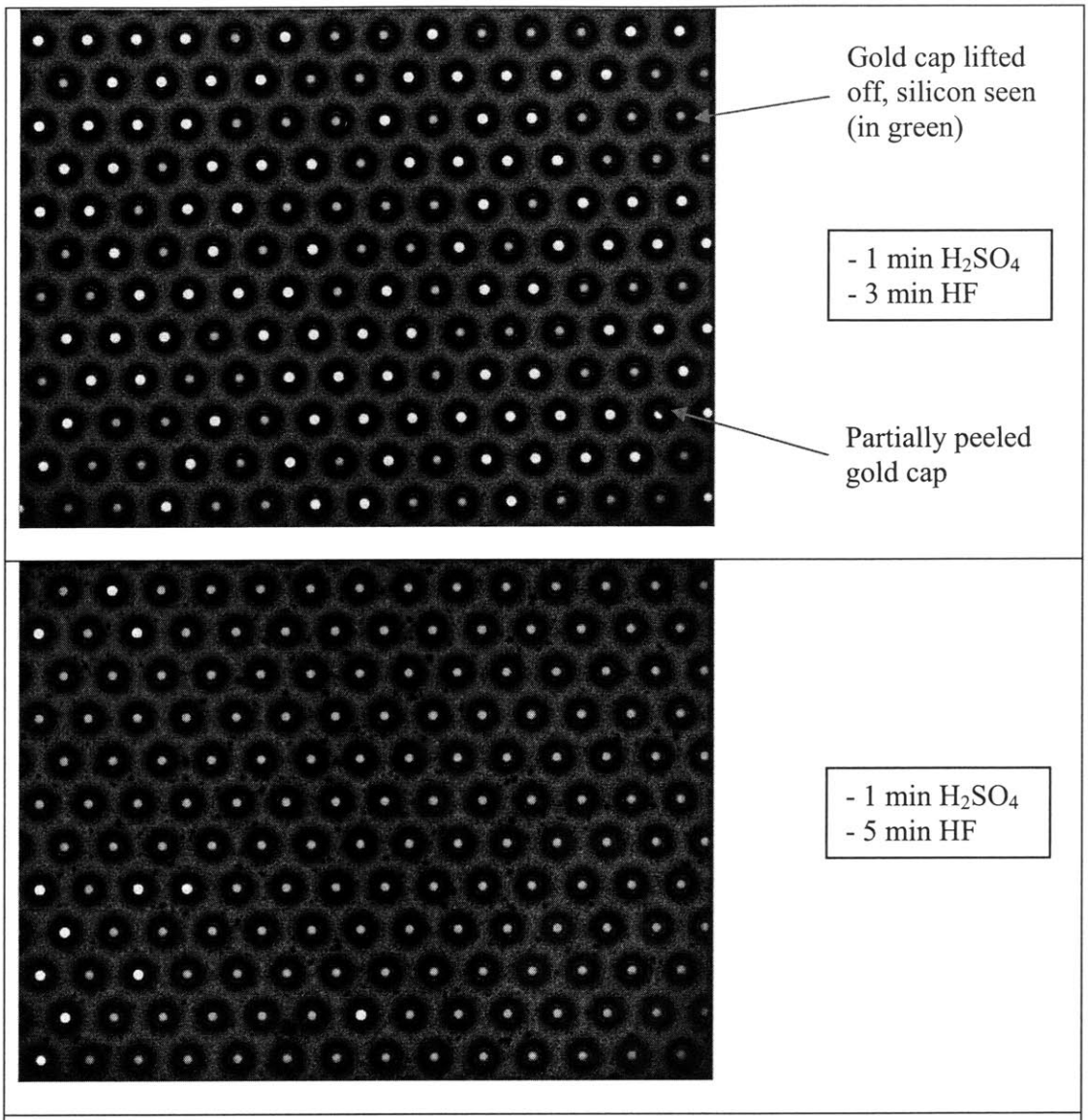


Figure 3-11: Loss of Cr/Au caps over time due to HF attack

It is optimal to minimize the amount of acid used and the time involved, so that the parts can be easily and quickly cleaned or diluted to a level that will not attack the Cr/Au caps. The etch rate for thermally grown wet oxide using concentrated 49% HF is 2.4 μm/min [13] and based on this etch rate, it should take about 5 minutes to etch laterally from the edge of the post to its center. However, the original HF release process using a shallow level of HF on the SOI die in a small beaker showed the oxide etched to completion (observable by the change in color) in about 3 minutes. This suggests that the etch rate is much faster than that listed in [13]. Another approach to minimize the amount of HF

used (by using HF vapor) did not work well since one needed to lift the cover occasionally to inspect if the oxide had been etched and this allowed the fumes to escape, making the etch very difficult to control or characterize. In principle, it worked essentially like a wet etch since the HF vapor (high vapor pressure) condenses onto the surface of the SOI die. Also, the etch rate across the die is not uniform, and this could be related to the (fluctuations in) circulation of HF fumes within the beaker.

The HF vapor method inspired the use of the droplet approach in which a few drops of HF are released using a plastic pipette onto the die surface. The advantages of this method are as follows: Firstly, only a minute amount of HF is used, thus allowing the HF to be contained on the surface of the die itself. Secondly, there is much less HF introduced into the dilution beaker since most of the HF droplet on the die either etched (reacted with) the oxide or evaporated inside the acid hood. Thirdly, the posts will stick onto the surface after release and can then be rinsed with water into the dilution beaker. The water from the beaker is extracted using a pipette and successively rinsed with fresh DI water to dilute the HF. No posts are lost during the transfer compared to previous methods in which many released posts floated off the top of the die into the HF bath due to the liquid movements during the transfer between beakers. In the previous methods, it was then a risk to try to retrieve these posts because it meant introducing more acid into the dilution beaker, which would subject the caps to more aggressive acid attack since it will take a longer time to neutralize. It has been observed that it does not require the oxide layer to be completely etched for the posts to be released. The posts will be released after 1 min in HF, and the oxide layer is still clearly present. This could be attributed to the HF attacking the silicon/oxide interface much more rapidly than the field oxide layer. This is positive news with regard to the integrity of the Cr/Au caps on the posts since the HF release time has been reduced from the original 3 minutes to 1 minute, resulting in a lower loss of Cr/Au caps.

The pH of the water in the vial containing the posts needs to be as close to neutral as possible because prolonged storage in dilute HF can lead to peeling of the Cr/Au caps. The successive dilution steps take a long time, but it is necessary too with regard to safety reasons during future handling. As a result, the pH of the water in all the bottles and vials

containing the posts is always checked with pH paper before the containers leave the fab for the group lab for the solder coating and assembly process.

Figure 3-12 shows a picture of the posts after they have been released. Figure 3-13 shows evidence of the gold cap as can be seen by the rim at the top of the posts (circled). Figure 3-14 shows further evidence that the gold cap is still intact, as can be seen by the bright yellow ring at the top of the posts.

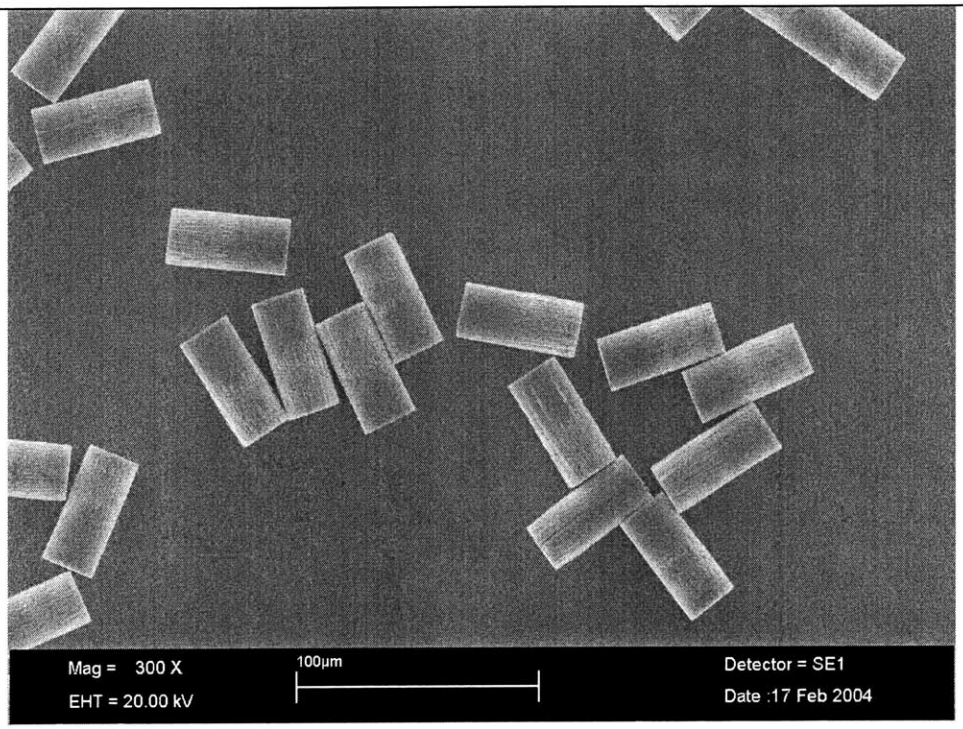


Figure 3-12: Released silicon posts lying on substrate

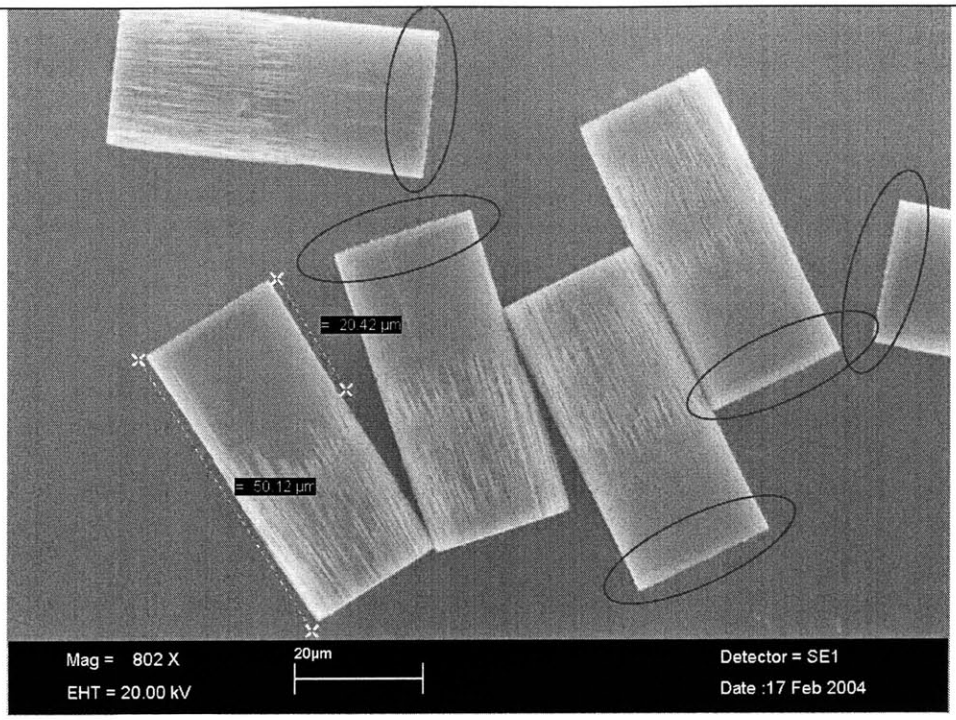


Figure 3-13: Dimensions of silicon posts and evidence of gold cap

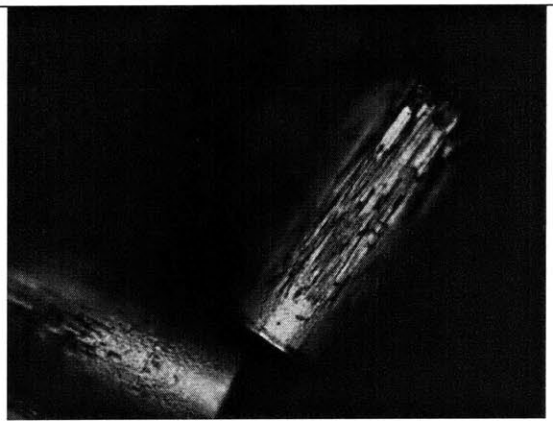


Figure 3-14: Rim of gold cap observed under an optical microscope

3.1.2 Substrate fabrication

The process flow for the substrate fabrication is shown in Figure 3-15 (the masks are described in Chapter 2).

The starting materials are 4" Pyrex wafers of 700 μm thickness. In step 1, the pyrex wafers are put into the HMDS oven in the TRL for a 15 minute dehydration bake to dry off the water. Next, the wafers are primed with HMDS, which is especially necessary to promote adhesion since glass is hydrophilic. Recipe 5 in the TRL HMDS oven (10 secs HMDS dispense) is used which gives a photoresist contact angle of 72° after the bake, exposure and development. AZ 5214 image reversal photoresist is used, and since it is a negative photoresist, exposed areas remain after development. After allowing the wafers to cool for five minutes, AZ 5214 resist is dynamically dispensed onto the wafer in the TRL coater at 500 rpm for 6 secs, followed by spreading of the resist at 750 rpm for 6 secs, and finally a spin at 4500 rpm for 30 secs. The thickness of the resist is about 1.2 μm. After a 30 min softbake at 95°C, the wafers are exposed for 1.5 secs using the EV1 in step 2. The mask used is the one for patterning the interconnect lines as seen in Figure 2-2. Following that is a 30 min post-exposure bake at 95°C and then a 45 sec flood exposure (without mask) using the EV1. Finally, the resist is developed in AZ 422 for about 65 secs until the pattern becomes clear. The wafers are then rinsed with water for 3 mins after the development. No further post-bake is necessary.

Step 3 is the electron beam evaporation of a 20 nm Cr / 200 nm Au / 20nm trilayer onto the above pyrex wafers using the TRL ebeam. The top Cr layer acts as an adhesion layer for the top silicon dioxide layer which is subsequently deposited in Step 5. If the top Cr layer is not present, the silicon dioxide layer will not adhere well to the Au and water will seep in during any subsequent photolithography development and wet processing steps. Step 4 is the metal lift-off of the Cr/Au/Cr using acetone, methanol, IPA and water. Ultrasonic agitation is not necessary for this lift-off process, and in fact, it is observed that the substrates are cleaner (with less residual metal particles) without having gone into the ultrasound bath.

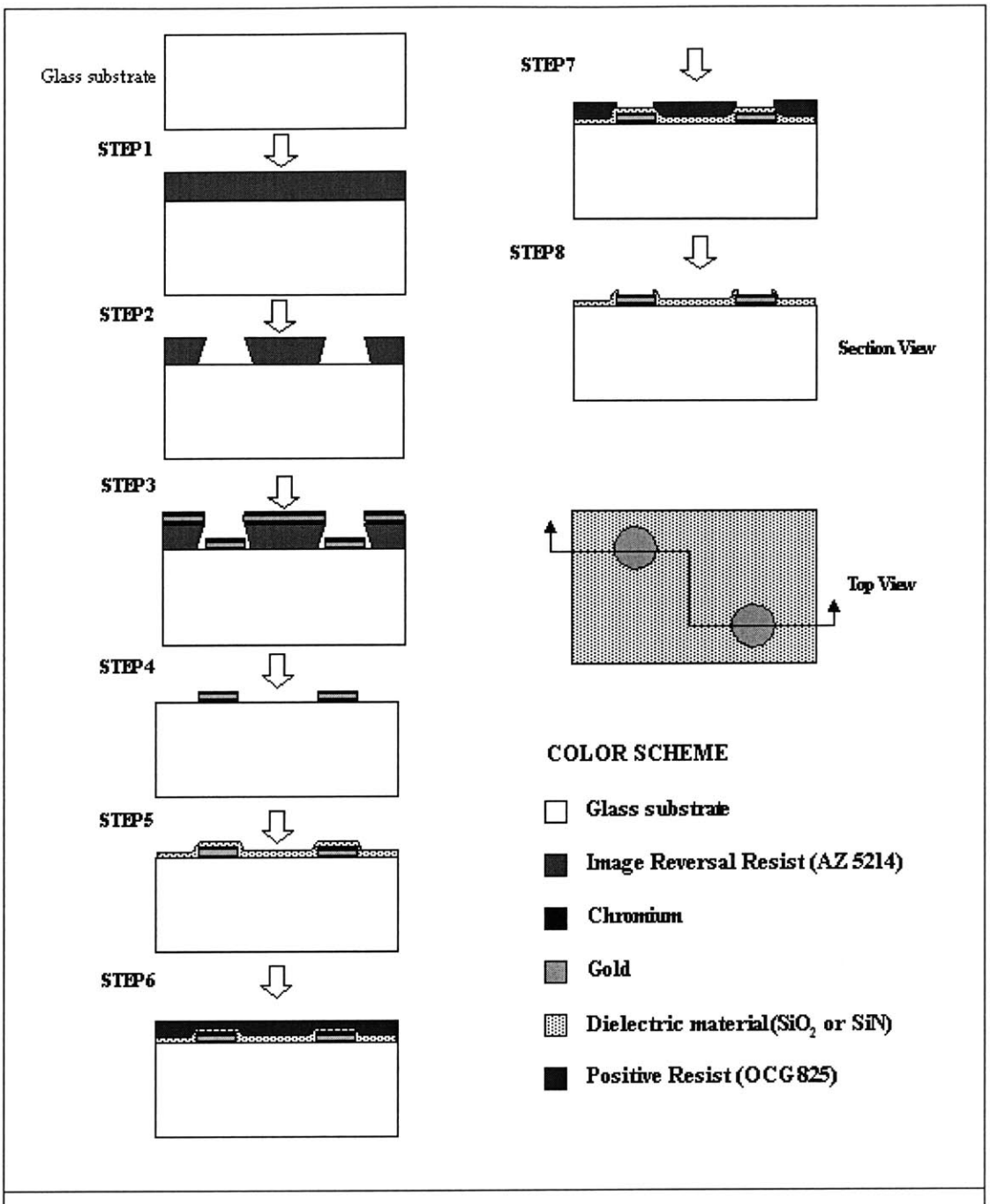


Figure 3-15: Process flow for substrate fabrication

Step 5 is the deposition of the dielectric layer onto the patterned pyrex wafers using the TRL Plasmaquest, which is an Electron Cyclotron Resonance (ECR) enhanced Reactive Ion Etcher (RIE) and Chemical Vapor Deposition (CVD) system. Either silicon dioxide or silicon nitride can be used, but the following process description will only be on

silicon dioxide since more processing has been done with it. The silicon dioxide layer makes the field non-wettable so that the solder will only coat selectively on the gold sites that have been exposed (it has been demonstrated later in a modified process that the silicon dioxide layer is not necessary since the Cr is not wetted by solder). For ECR-CVD depositions, the temperature should be set to 80° C [8]. A cleaning step using the recipe <EtchCln> is run for 600 secs to clean the chamber prior to beginning the deposition, and after every micron deposited. If the deposited material is allowed to accumulate on the sidewalls of the chamber, it will start flaking once it becomes too thick. The flakes or particles will fall off and contaminate the substrates during the deposition, which will result in a poor non-uniform coating and stresses in the film. The silicon dioxide film is deposited as a result of the reaction between silane (SiH_4) and oxygen, and the recipe used is <SiO2-dep> which is given in Table 3-5. Step 1 is the standby step, and step 2 is a transient step which is usually added to allow the ECR power to stabilize and ramp up before the deposition in step 3. For CVD using the Plasmaquest, only ECR is used and one has to adjust the microwave tuning stubs during the deposition to ensure that the reflected power is less than 10 watts [8].

Processing parameters	**Step 1**	**Step 2**	**Step 3**
O_2 (sccm)	12	12	12
SiH_4 (sccm)	105	105	105
Pressure (mtorr)	20	20	20
ECR system (watts)	0	10	200
Chuck temperature (°C)	80	80	80
Step processing time (sec)	30	5	440

Table 3-5: <SiO2-dep> recipe, ECR-CVD (Plasmaquest)

The process is first run on a 4" plain Si dummy wafer to determine the deposition rate by measuring the film thickness using the TRL Nanospec. Since the substrates are pyrex wafers, they cannot be used for film thickness characterization because they are transparent, as is the silicon dioxide layer. The Nanospec has a precision

microspectrophotometer head, which can measure in the wavelength range of 370 to 800nm, using a computer-controlled grating monochromator, photomultiplier tube detector, and amplifier [23]. When the MEAS key is pressed, the spectrophotometer head scans, generating a corrected spectrum by computing a ratio to a bare silicon reference previously stored. The resulting spectral data is then analyzed by the computer, which determines the exact film thickness corresponding to the interference pattern [14]. By dividing the average film thickness by the process time, the deposition rate for the recipe is found to be 6.82 A/sec. For a film thickness of 300nm, a process time of 440 secs in step3 is required.

Steps 6 and 7 show the photolithography on the substrates in preparation for the final etch to the gold receptor sites. The substrates are primed with HMDS recipe 5 (10 secs HMDS dispense) following a 15 minute dehydration bake. OCG 825 is used, which is a positive photoresist. After allowing the wafers to cool for five minutes, OCG 825 resist is dynamically dispensed onto the wafer at 500 rpm for 6 secs, followed by spreading of the resist at 750 rpm for 6 secs, and finally a spin at 3000 rpm for 30 secs. The thickness of the resist is about 1 μm. After a 30 min softbake at 95°C, the wafers are exposed for 2 secs using the EV1. The mask used is the one for patterning the gold receptor sites. The resist is then developed in OCG 934 1:1 for about 55 secs until the pattern becomes clear. The wafers are then rinsed with water for 3 mins and spun dry before a 30 min postbake at 95°C.

The silicon dioxide layer can either be dry or wet etched in step 8. For RIE using the Plasmaquest, both ECR and RF are used and as before in the CVD step, and one has to adjust the microwave tuning stubs during the etch process to ensure that the reflected power is less than 10 watts [8]. For plasma etching of silicon dioxide, recipe <etchSiO2>, shown in Table 3-6, is used. Steps 1, 2, and 3 are the standby, transient, and etch steps respectively. The etch rate for this recipe is about 7.84 A/sec as determined by etching the previous dummy silicon wafer and measuring the remaining film thickness using the Nanospec. To ensure that the silicon dioxide on top of all the gold receptor sites is fully etched, the process time is extended to 150% of the calculated required time. The overetch does not result in undercutting of the oxide since the plasma etch is directional

in nature due to the RF source [11]. Alternatively, the silicon dioxide can also be etched using BOE. This is carried out in a water bath with a degas option in order to remove air bubbles, which may form at some of the receptor sites and impede the etch. The etch is complete once the end contact pads on the substrate change color from violet (silicon dioxide on Cr) to grey (Cr only), and this takes about 50 secs. The etch must be timed carefully and the substrates must be rinsed well to prevent further under-cutting of the oxide.

Processing parameters	Step 1	Step 2	Step 3
O_2 (sccm)	4	4	4
CF_4 (sccm)	40	40	40
Pressure (mtorr)	20	20	20
ECR system (watts)	0	1	100
RF system	0	20	20
Chuck temperature (^oC)	25	25	25
Step processing time (sec)	30	5	450

Table 3-6: <etchSiO2>, RIE (Plasmaquest)

The second part of Step 8 involves the etching of the top Cr layer at the receptor sites to expose the underlying Au. By putting the substrates into the asher for 3 hrs, the Cr layer on top of the Au receptor sites can be removed. Finally, the substrates are coated with thin resist for protection and diced into chips using the die-saw.

3.1.2.1 Modified substrate fabrication

The solder coating and self-assembly experiments uncovered problems with the substrates produced using the original process flow for substrate fabrication. The diagnosis of these problems is described in Chapter 4, and the motivation behind the process change will start in Section 4.3.1. The resulting design is shown in Figure 3-16, which shows the modified process flow for the substrate fabrication. This is the eventual

process used in the fabrication of the substrates, but one should note that this process flow should not be considered the final solution for the DEP-based cell trap device.

The processes are almost the same as the previous one (Figure 3-15) except for the use of standard OCG 825 positive resist for a metal lift-off process from step 5 onward, the electron beam evaporation of a Cr/Cu/Au stack in step 7, and the omission of a deposited oxide layer. The photolithography step for the OCG 825 resist is the same as in the original process described earlier, except for the final spin speed which is at 2000 rpm to give a thickness of about 1.2 μm. The mask used is the one for patterning the gold receptor sites. In step 7, the thickness of the metal stack is 30nm Cr : 150nm Cu : 20nm Au.

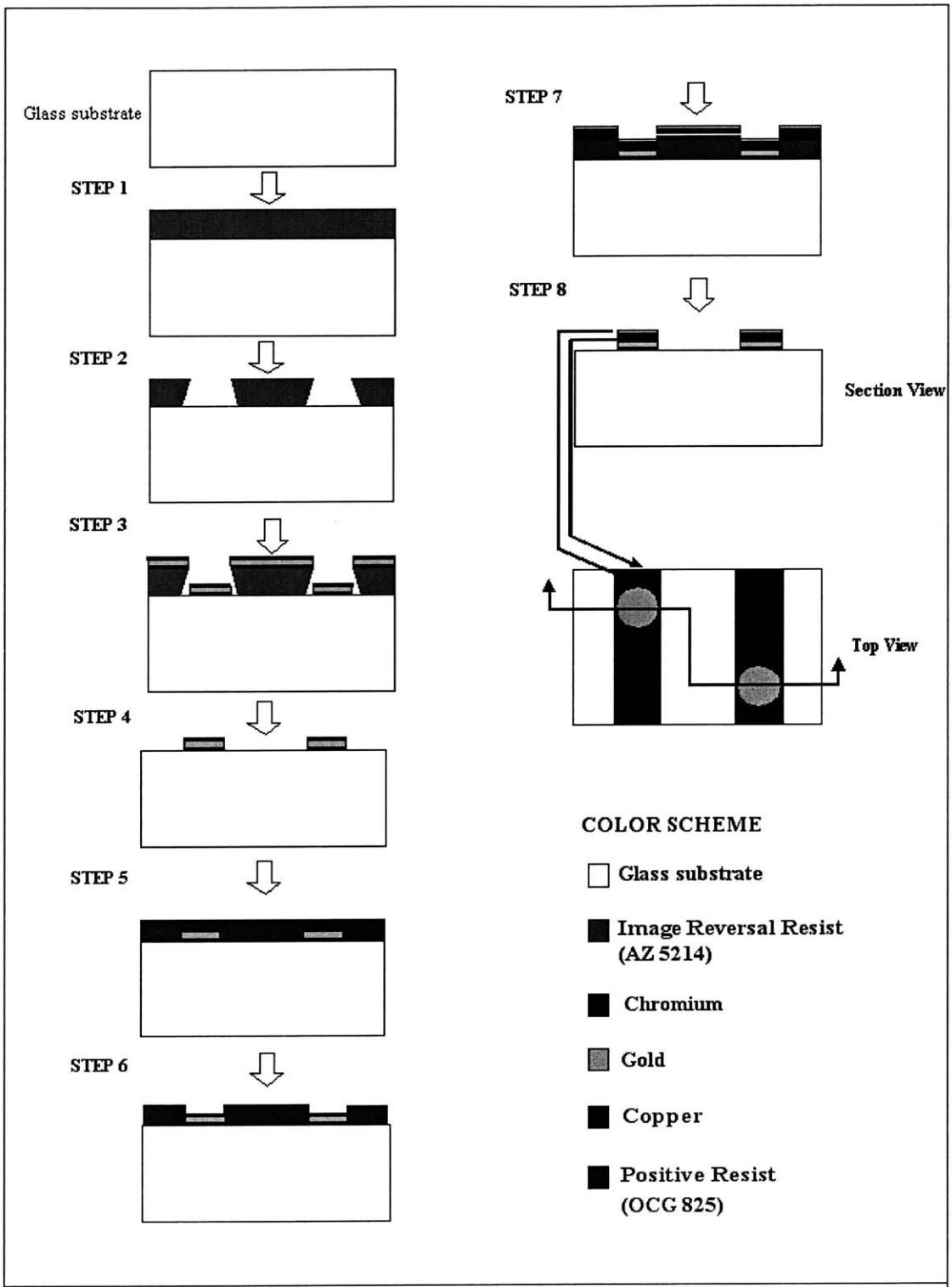


Figure 3-16: Process flow for modified substrate fabrication

3.2 Fabrication issues

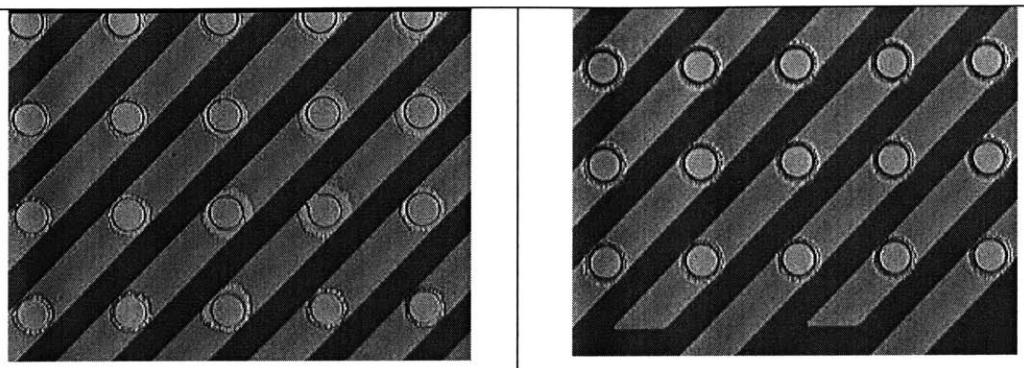
The following are some issues uncovered in the course of fabricating the posts and substrates, and this section discusses the steps to either solve or circumvent the problems.

Etching of platinum

Platinum is a noble metal that is very difficult to etch. Initially, the approach was to etch circular patterns on the deposited platinum on the SOI, and then cover the platinum caps with photoresist for the DRIE step. The platinum was etched using dilute aqua regia (HNO_3 : HCl : H_2O = 1:8:7) at 65°C; however, a layer of scum often appeared on different regions of the wafers. The scum is basically photoresist and un-etched Ti, which is due to the HNO_3 attacking the resist causing parts of it to delaminate. Also, since the concentration of HNO_3 is high, the Ti will be partially passivated because of heavy oxidation once the upper layer of Pt has been etched (however, the HCl will dissolve some of the Ti). Due to the presence of the scum, some regions get etched faster than others, and at the same time, there is a lot of lateral under-cutting, which gives rise to severely under-sized (5 μm diameter) Ti/Pt caps. The best way to pattern platinum is to use a lift-off process. However, due to machine and process incompatibility in the TRL, this method cannot be used. Subsequently, the Pt wet etch process was discarded in favor of the self-aligned process as shown earlier in steps 5 to 8 of Figure 3-3.

Etching of silicon dioxide layer

The wet etching of silicon dioxide using BOE, if not timed or controlled properly, will lead to the under-cutting of the oxide layer as shown in Figure 3-17. Despite the fact that there is usually a minute amount of under-cutting even under the best circumstances, wet etching of the oxide is preferred over the dry etch using Plasmaquest. This is because the etch differed greatly across the substrate, which becomes very evident after etching the top Cr layer with the chrome etchant CR-7 (Figure 3-18). The cause is unknown; however, it has been speculated that it might be due to the inter-digitated metal lines charging up during the etch inside the Plasmaquest chamber due to the RF.



More severe under-cutting	Less severe under-cutting

Figure 3-17: Under-cutting of oxide layer using BOE wet etch

Etching of top Cr adhesion layer

The chrome etchant CR-7, with an etch rate of 110nm/min [13], was originally used to etch the top Cr layer at the receptor sites to expose the underlying Au. However, since the top Cr layer is only 30nm thick, the etch proceeded very quickly and a significant amount of under-cutting in an erratic manner is observed as seen in Figure 3-18. There is a dearth of information on the dry etching of Cr, but nevertheless, discussions with staff members of the MTL yielded some information on Cr being etched by an oxygen plasma ash, albeit slowly. The Cr dry etch approach was taken, which does not result in any under-cutting of the Cr. Since the Au and SiO_2 layers are not etched by the oxygen plasma, the end-point for the Cr dry etch is not critical.

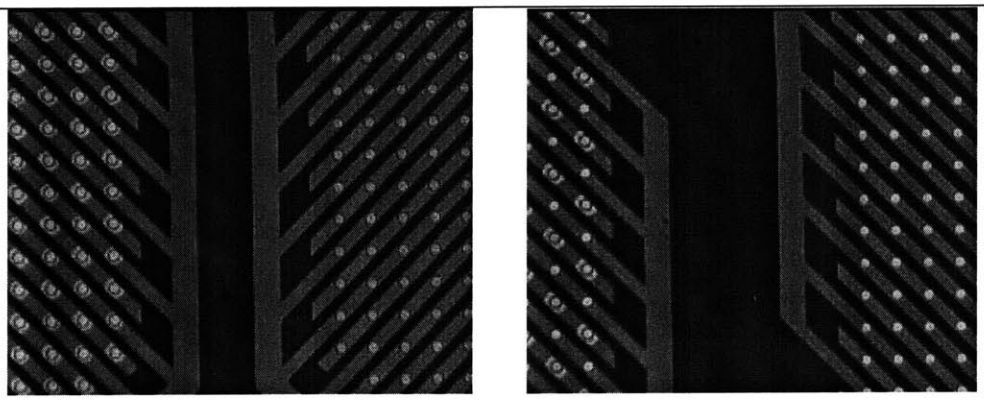


Figure 3-18: Extreme variations in the under-cutting of Cr using a CR-7 wet etch (after the oxide dry etch)

Chapter 4 Solder Technology

The first two sections of this chapter provide some background details on solder and wetting to aid in understanding or explaining some of the observations in the latter sections of this chapter, which describes the procedures and results of the solder coating process.

4.1 Solder alloy

Solders are generally classified as low melting alloys with liquidus temperature below 400°C [14]. It is usually used in a paste form, which is a homogeneous and kinetically stable mixture of solder alloy powder, flux, and vehicle [14]. Under a given set of soldering conditions, the solder paste is capable of forming metallurgical bonds and making reliable and consistent solder joints. The functionality of the major components of the solder paste is as given: The vehicle is primarily a carrier for solder powder and provides a desirable rheology, which refers to the flow and deformation of solder paste under a given set of conditions; the flux maintains a clean and metallic state on the solder and the surfaces to be joined, so that good wetting and metallic continuity is formed between the solder and the surfaces [14].

Both vehicle and flux are removed by the completion of the soldering process, either partially escaping during the heating stage through volatization, decomposition, and reaction, or being removed during the subsequent cleaning step [14]. Nevertheless, they are crucial to the formation of a reliable, permanent bond. On a permanent basis, the alloy powder part is the only functional component in the final metallurgical bond [14].

The solder used in this project is a low melting point bismuth alloy (LMA-117, Small Parts) which has the composition shown in Table 4-1 [15] and a eutectic temperature of 47°C. The solder is chosen primarily for three reasons: Firstly, it is to determine the feasibility of solder (capillary fluid) self-assembly on the 25 μm scale; secondly, other groups (Whitesides [2], Howe [16]) have demonstrated successfully the use of this solder

in self-assembly, albeit on higher scale regimes; thirdly, the low melting point of the solder makes it easy to work with, without requiring special high temperature fluxes. In addition, Table 4-1 also shows that the quinary eutectic has negligible expansion or contraction after solidification, which is ideal for the cell-trap application since orientation of assembled posts is an important factor. However, since the alloy contains cadmium making it toxic [5], precautionary measures need to be taken during the processing, for instance handling with gloved hands and carrying out the experiments inside a fumehood since cadmium has a high vapor pressure [5]. This also means that the solder alloy will not be biocompatible, rendering it inappropriate for an actual cell trap. It must be iterated once again that this is but a feasibility study on self-assembly, and that there are other potential non-toxic low melting point solder alloy alternatives available (an example is shown in Table 4-2) should future endeavors be undertaken in the construction of a cell trap using solder assembly.

Alloy information	**LMA-117**
Melting temperature (°C)	47 °C
Weight (lb/in^3)	0.32
Composition (%)	
Bismuth	44.7
Lead	22.6
Tin	8.3
Cadmium	5.3
Indium	19.1
Time after casting	Growth/Shrinkage (inches per inch)
6 min	+.0002
30 min	.0000
1 hour	-.0001
5 hours	-.0002
24 hours	-.0002
21 days	-.0002

Table 4-1: Low melting point bismuth alloy specifications [15]

Alloy information	Alternative solder
Melting temperature (°C)	61
Composition (%)	
Sn	16
Bi	33
In	51

Table 4-2: Potentially non-toxic biocompatible low melting solder alloy

4.1.1 Solderability

Solderability is the ability to achieve a clean, metallic surface on both the solder powder and on substrates during the dynamic heating process, so that good wetting of molten solder on the surface of the substrates can be formed [14]. The solderability relies on both the fluxing efficiency provided by the solder paste and the wettability of the two surfaces to be joined [14,17].

However, a major unresolved gap in the understanding of the soldering process is the relationship between wettability and solderability. Wettability can be directly measured while solderability cannot be directly measured in a quantifiable way and its relationship to wettability has not yet been explicitly defined [17].

4.2 Wetting of surfaces

Wetting is an essential prerequisite for soldering, and it refers to the specific interaction that takes place between the liquid solder and the solid surface of the part to be soldered, resulting in the formation of an intermetallic layer. For wetting to occur, the solder needs to come into immediate contact with the surface of the designated metal layer. Any firmly adhering contamination such as oxides or organics on the surface to be soldered will act as a barrier to metallic continuity and thus prevent wetting. Therefore, the surfaces need to be clean and the metal atoms positioned immediately at the interface, in order for wetting to take place. The solder atoms are now able to combine with the atoms

of the (highly solderable) metal, in the process forming an alloy at the interface, which ensures good electrical contact and good adhesion. The formation of the alloy at the interface means that wetting is an irreversible process [5,14,17].

When discussing the wetting characteristics of a surface by molten solder, there are two important factors: 1) the extent of wetting, and 2) the rate of wetting [17]. The degree of wetting (as indicated by the contact angle in Figure 4-1 and discussed in the following section) is an equilibrium case governed by the laws of thermodynamics and dependent on the surface and interfacial energies involved at the liquid-solid interface. The rate of wetting (how fast the solder wets and spreads) is governed by the thermal demand of the system, the ability of the heat source to supply heat, the efficacy of the flux, the viscosity of the solder and the chemical reactions occurring at the interfaces. The magnitude of the wetting time is dependent on the temperature, specimen dimension, and the speed and depth of immersion [17].

4.2.1 Surface tension

The extent to which a liquid solder will spread across a surface depends on the surface tensions acting between the interfaces involved. The surface tension of a liquid, γ_{LV}, is a thermodynamic quantity, and is equal to the amount of work needed to enlarge (isothermally) the liquid surface area [5]. From thermodynamics it is known that a system strives to a minimum value of its free energy, and hence to a minimum surface area. Figure 4-1 shows the well-known situation of a liquid-solder droplet on a solid metal cap/surface [5]. Since the size of the solder bumps in this self-assembly project is very small (20 μm diameter), gravity, which will give rise to a flattened spherical cap, is ignored. Thus the shape of the droplet is determined solely by γ_{SV}, γ_{SL}, and γ_{LV}, which are the solid-vapor, solid-liquid, and liquid-vapor surface tensions respectively [5]. For soldering, the vapor phase will be replaced by the flux.

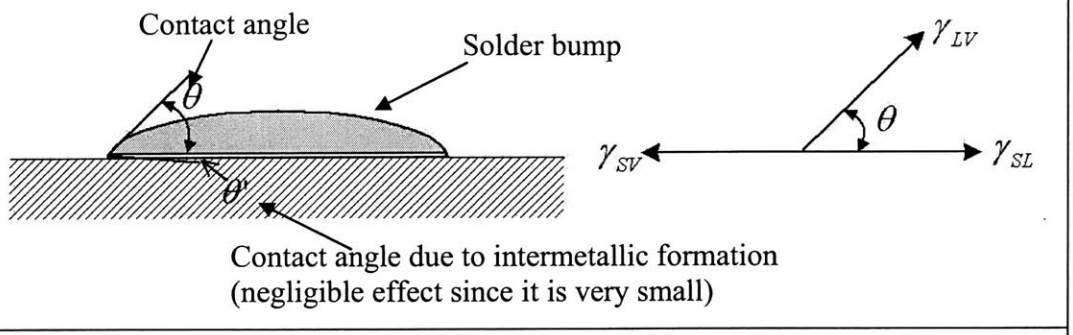


Figure 4-1: Schematic of wetting angle and wetting forces

As the system tends towards minimum free energy, the areas of the interfaces and the free surfaces will want to minimize. However, in doing so, they counteract one another in that the reduction of one area leads to the enlargement of another. Eventually, the droplet selects that shape for which the total surface free energy, $F_{surface}$, has its minimum value [5]:

$$F_{surface} = \gamma_{SV} A_{solid} + \gamma_{LS} A_{interface} + \gamma_{LV} A_{liquid} \quad (4\text{-}1)$$

where A_{solid} is the solid surface area, $A_{interface}$ is the interfacial area, and A_{liquid} is the liquid spherical area.

Young's equation can be obtained from the above condition as shown in [5]:

$$\gamma_{SV} = \gamma_{SL} + \gamma_{LV} \cos \theta \quad (4\text{-}2)$$

The angle θ, enclosed between the tangent to the solder surface and the base metal/solder interface at their line of intersection, is called the contact angle. The contact angle so defined is an equilibrium value found on a perfectly smooth solid surface, with both droplet and base material consisting of homogeneous and continuous matter, and no chemical reaction between the liquid and solder substrate [5]. It should be realized that the shape in Figure 4-1 is the result of a calculation in which it was assumed that gravity could be ignored and that the solid surface is flat. In practice, the base metal will

dissolve in the molten solder and a chemical reaction forming one or more intermetallic compounds will occur, giving rise to another contact angle θ' at the solid-liquid(solder) interface [5]. However, this angle is very small since the metal film is usually very flat, thus $\gamma_{SL} \cos \theta' \approx \gamma_{SL}$ in Equation (4-1). In most cases the assumption that the surface is flat holds fairly well, as does Young's equation.

For optimum wetting, the contact angle θ must be minimized. From Equation (4-2), it is clear that wetting will be promoted by small values of γ_{LV} and γ_{SL} in combination with a relatively large value of γ_{SV} [5].

The surface tensions of oxides are distinctly lower than the values for the corresponding metals [5]. An effective reaction of a flux with the oxide on a solid surface causes an increase of the surface tension γ_{SV} by removal of the oxide, thus promoting wetting. Usually, it is impossible to wet the surface of a solid metal as long as it is oxidized. However, the effect of removal of the oxide film from molten solder is not so clear and may seem contradictory since a decrease of γ_{LV} is favorable for wetting [5]. On the one hand it is seen in literature [5] that oxidized solder gives a larger spread (i.e. smaller contact angle) than unoxidized solder, but on the other hand, there is a reduction of γ_{LV} under the influence of fluxes (which will be covered later). In any case, the influence of γ_{SV} in general dominates that of γ_{LV}, because its magnitude is much larger. The solid oxide skins on the molten solder may impede spreading and correct flow of the solder, with the result that in soldering practice, the oxide should always be completely removed [5].

Although γ_{LV} is a function of the solder composition, the flux covering the liquid solder, and the temperature, its value is normally close to 0.4 J/m [17]. This is the same value as the surface tension of the solder/water interface used in this project, as well as the other groups [2,16].

As for the surface tension of a surface, it is determined by the interatomic bond energies of the atoms. The atoms in the surface layer possess a higher potential energy than the bulk atoms, because they are incompletely surrounded by the other atoms [5].

In soldering, frequent use is made of systems in which intermetallics form as a result of the soldering [5]. The occurrence of these compounds means that there exists a strong affinity between the atoms of the two elements involved. The great stability of such compounds is demonstrated by their high melting points in comparison with the melting points of the pure elements [5]. The occurrence of intermetallics implies that dissimilar atoms 'attract' each other more than do similar ones. If intermetallics are formed at the interface, the interfacial energy should consequently be relatively low [5]. For the use of LMA-117 solder in this project, the wetting is highly likely to be promoted by the Sn in the solder, which forms intermetallic compounds with the Au metal on the receptor sites.

The discussions on the surface tensions are based on the assumption that the wetting parameters do not change; i.e. the values of the surface tensions are constant. In soldering practice this is not true for several reasons [5]:

(i) Due to the formation of the diffusion layer, a gold surface that has been wetted by solder will never become a clean gold surface again. Thus, for spreading, the surface tensions of the interface, liquid solder, and gold film apply, but for the receding (or reflow), the surface tension of the gold film must be replaced by the surface tension of alloyed gold intermetallic layer.

(ii) During soldering, parts of the gold and copper dissolve in the liquid solder, which changes the solder composition, and in turn altering the solder surface tension.

(iii) If the flux becomes exhausted (through evaporation) or flows away during soldering, reoxidation takes place, again changing the wetting conditions. Thus, care must be taken to replenish the flux before it boils or evaporates off.

(iv) Considerable temperature gradients exist during the soldering/coating process. Thermal equilibrium is seldom attained because the soldering operation is completed in most cases before the equilibrium temperature is reached. If

temperature gradients are present, the liquid solder tends to flow in the direction of the highest temperature, because in general, the surface tensions are smaller at higher temperatures. This may explain the inconsistency of the solder bump coating across the substrate, resulting in different extents of wetting and solder spreading on the gold contact sites as will be seen later in this chapter.

4.2.2 Need for flux

Fluxes are used primarily to improve the wetting properties of the solder-substrate system. The most important function of the flux is to increase γ_{SV} through the removal or dispersion of oxides and contaminants, which lower the surface energy of the substrate [17]. During soldering, the flux also maintains a local environment around the surfaces being joined, which protects them from re-oxidation as well as enhances heat transfer from the heating source to the substrate and solder [5]. As a result, wettability is enhanced.

From a chemical point of view, the inorganic chemicals such as strong acids, strong bases, and certain salts, are highly reactive, and thus are not suitable [14]. The flux also has to be chemically compatible with the substrate and silicon posts. Organics containing active functional groups such as carboxylic (-COOH) groups and amine ($-NH_2$, -NHR, $-NR_2$) are good fluxing agents [14]. The flux used for our solder coating and self-assembly processes is a solution of glacial acetic acid (CH_3COOH) in water (1:100 by volume) with a pH of 3, which is adapted from [2,16].

4.2.3 Degrees of wetting

The rate of wetting is dependent on the temperature of the soldering process and on the rate of cleaning of the surfaces by the flux [5].

The following conditions may be observed after removing the substrate from the solder [5]:

(i) Non-wetting: the surface becomes uncovered again, without any visible interaction with the solder. The gold surface retains its color. Non-wetting on some of the gold sites may be due to a thin layer of silicon dioxide or tiny air bubbles preventing wetting from taking place. The thin layer of oxide may have been present due to varying etch rates across the wafer in the Plasmaquest (Figure 3-18) or air bubbles during the oxide wet etch using BOE.

(ii) Wetting: an intermetallic forms at the gold surface (changing its color), and subsequently solder bumps are seen. Perfect wetting is associated with a uniform, smooth, unbroken solder bump adhering to the base metal.

(iii) Partial wetting: the surface has some regions showing wetting and other regions showing non-wetting.

(iv) Dewetting: the substrate appears to wet fully initially. After a period of time, the molten solder begins to recede (ball-up), exposing substrate area that had initially been covered with molten solder, and resulting in a combination of dewetted regions and irregularly shaped solder droplets. Dewetting is often unevenly distributed over the surface. Figure 4-2 shows a schematic of the de-wetting process.

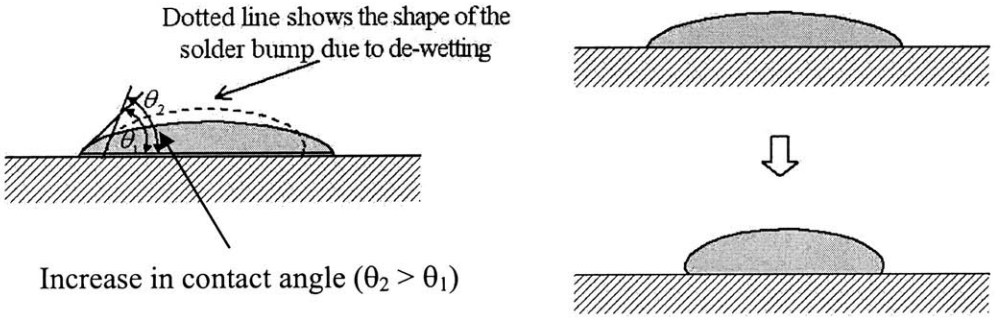


Figure 4-2: Schematic of solder de-wetting

De-wetting could be due to [5]:

(i) dissolution of a wettable coating on a non-wettable substrate:

Coatings of gold readily dissolve in Sn-based solder. When the coating on the pyrex substrate is soldered, excellent wetting takes place initially. After some time, the film dissolves, exposing the pyrex surface to the solder which will then withdraw.

(ii) non-wettable spots on a wettable surface :

A variety of non-wettable spots can promote dewetting. These may be rolled-in or brushed-in particles, spots consisting of a thick oxide or corrosion layer, intermetallic crystals grown on the outer surface, etc.

(iii) contaminated solder

4.3 Coating of solder on substrate

This section describes the coating of solder bumps on the substrate chips in preparation for the self-assembly step.

As mentioned earlier in Section 4.2.2, the flux used is a solution of 1 part of glacial acetic acid (CH_3COOH) in 100 parts of water (by volume), giving a pH of 3. It is a good practice to check the pH of the solution prior to coating to avoid dissolution of the solder if the pH is too low [2]. Before using the flux in the solder coating and self-assembly processes, N_2 is bubbled through the solution overnight to de-oxygenate the water which reduces the formation of oxides in the solder later on [2,16]. Proper de-oxygenation and pH control of the solution is imperative for preventing oxide formation on the solder alloy at the water interface; such an oxide creates a skin that pins the interface, inhibiting capillary fluid flow [16]. It is also noted in [18] that the addition of nitrogen will improve the solder's wetting characteristics, presumably for the same reasons.

In order for the solder to wet the gold binding sites on the substrate and for spreading to occur, the melted solder alloy needs to be clean, without any oxide skins at the solder/flux interface. The oxide skins appear as bits and pieces of crud and also give the melted solder bath a dull grayish color. This is what the first melt of the solder ingots

will look like, and any solder coating experiment done at this point will be futile. Storage of the solder ingots under atmospheric conditions over a prolonged period of time gave rise to the oxide skins. It was observed that high temperature heating of the solder bath (>95°C) and constant replenishing of the evaporated flux dissolves the oxide skins, and cleans the solder very effectively. This gives rise to a clean solder bath with a smooth shiny silvery surface, which will then be ready for the solder coating process.

In Surface Mount Technology (and in manufacturing), the solder reflow temperature is about 30°C to 50°C above the melting temperature. For instance, tin lead, which is typically 63% Sn and 37% Pb and has a melting point of about 183°C, uses reflow solder-joint temperatures of about 220° to 230°C [19]. Literally, reflow is a misnomer; in the context of solder paste technology, it means to flow or melt the paste, rather than to re-flow. Also, other groups using the same low melting point bismuth alloy (LMA-117) have carried out solder coating using temperatures of 70°C (Howe, [16]) and 90°C (Whitesides, [2]), which is in the range of about 20°C to 40°C above its melting temperature of 47°C. All this points to the need for a higher working temperature (above the liquidus temperature) in order for wetting to occur and solder bumps or joints to form.

Initial solder coating experiments were conducted at two temperatures (70°C and 85°C) to determine the rate of wetting, using Pyrex chips with Cr/Au/Cr/SiO_2 and Cr/Au/Cr/SiN layers etched at selective sites to expose the Au contact pads. The Pyrex chip is held in a pair of plastic tweezers and immersed into the layer of hot flux above the molten solder for 5 secs. This is done to preheat the substrate and to clean the surface (with flux) before the solder coating step. The substrate is then dipped into the solder bath vertically and held for the required length of time for the formation of solder bumps. In order to determine the wetting time, the substrate is removed periodically and inspected under the microscope. It should be briefly mentioned that a 45° removal angle and a roughly 1cm/sec removal speed is adopted here based on the experimental procedure outlined by Scott and Howe [16], and since the primary aim of the experiment here is to determine the wetting time based on temperature, these two parameters will remain unchanged throughout. Also, any visible air bubbles should be removed by stirring the solder since

the air bubbles will clearly impede the wetting of a large area (and number)of contact pads, and prevent the formation of solder bumps.

The Pyrex chips with the Cr/Au/Cr/SiO_2 (and Cr/Au/Cr/SiN) layer showed unusually long wetting times (more than 20 minutes for the formation of solder bumps) and different rates of wetting across the contact pad arrays (Figure 4-3). After running a few solder coating experiments at 70°C, it was concluded that the wetting rate is too slow and that a higher temperature is required for the proper formation of solder bumps. The observations showed the gold contact pads changing to a brown color indicating the formation of intermetallics, but the intermetallic appeared to recede after 15 minutes without the full formation of solder bumps (Figure 4-4, Figure 4-5).

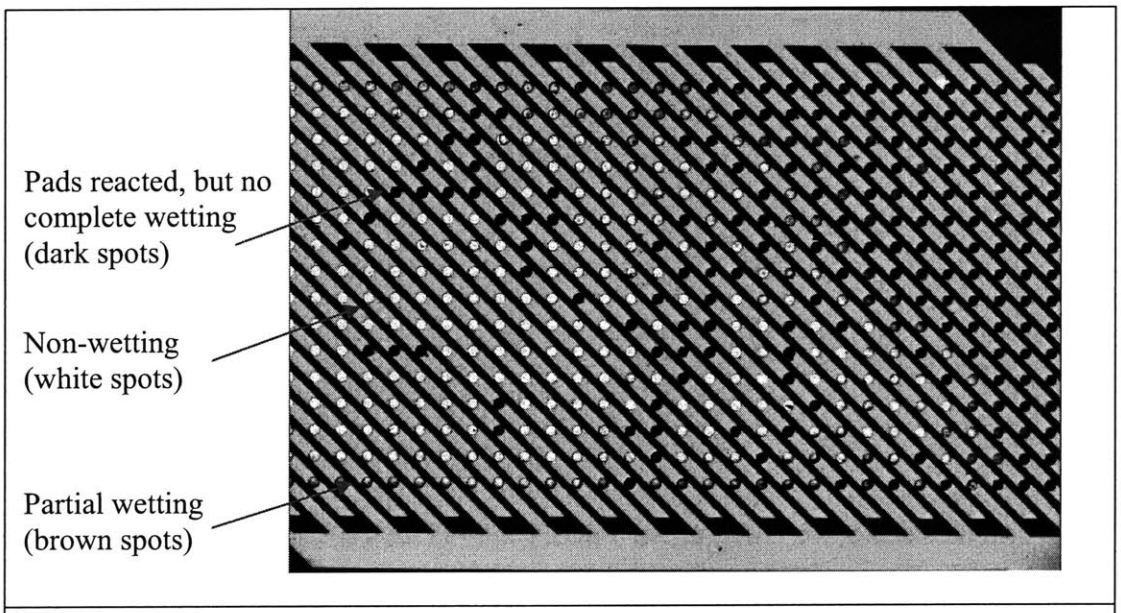


Figure 4-3: Different rates of wetting for a Pyrex chip with Cr/Au/Cr/SiO_2

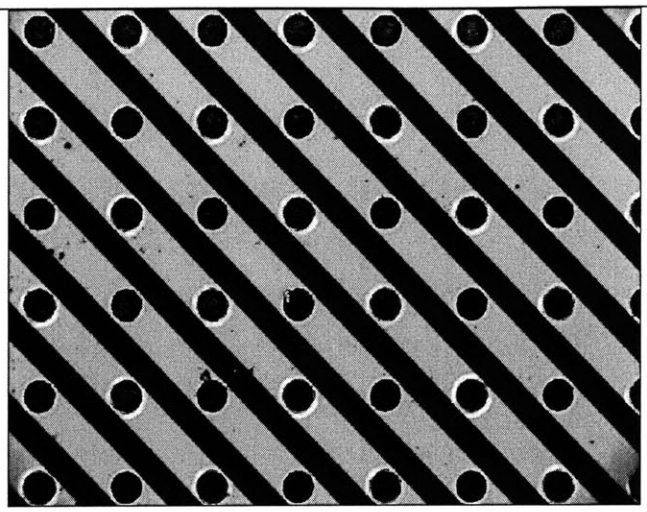


Figure 4-4: Intermetallic formation after 5 minutes in solder bath at 70°C
(no formation of full solder bumps)

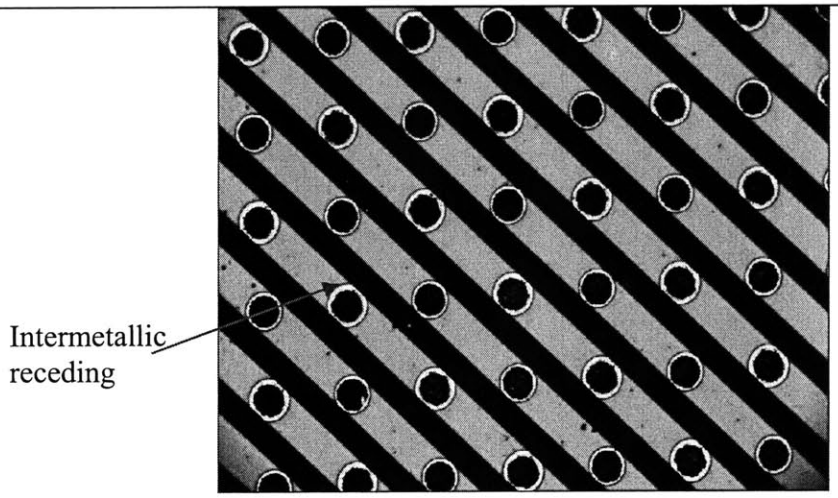


Figure 4-5: Intermetallic receding after 15 minutes in solder bath at 70°C
(no formation of full solder bumps, c.f. Figures 4-6 and 4-7)

More success in the formation and yield of the solder bumps was obtained using a higher temperature of 85°C. The glint on the solder bumps in Figure 4-6 and Figure 4-7 is actually the light reflecting off the top of the spherical solder bumps. However, the wetting time remained as long and different rates of wetting were still observed across the substrate (Figure 4-6). Also, the dissolution of the gold layer led to de-wetting of the

solder bumps from the surface. As a result, the edge of the solder bumps is observed to have visibly receded after 15 minutes (Figure 4-7).

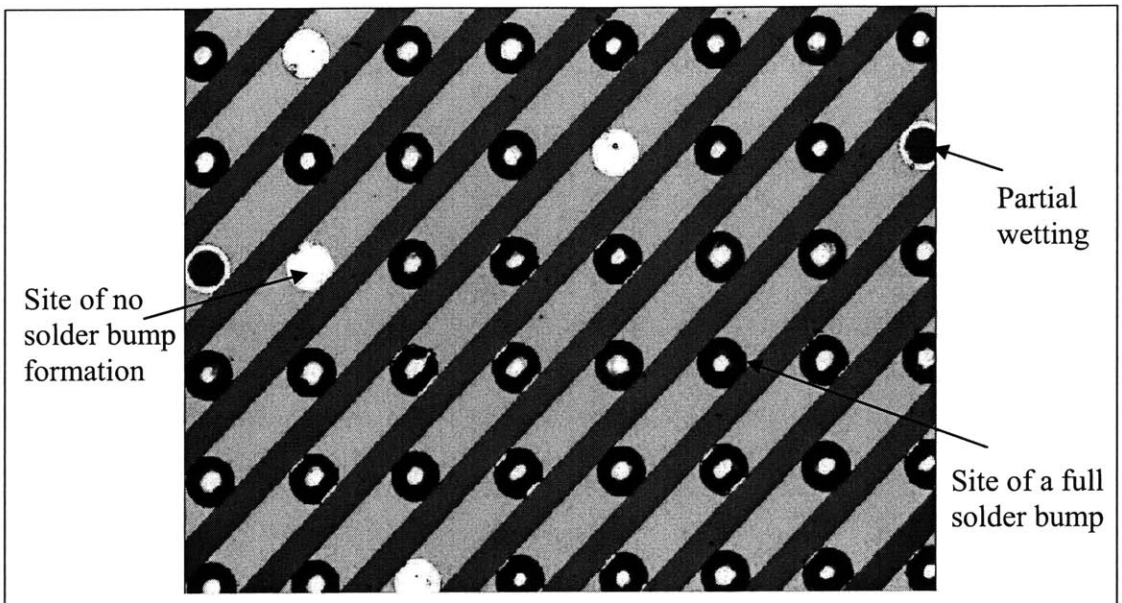


Figure 4-6: Solder bump formation after 10 minutes in solder bath at 85°C

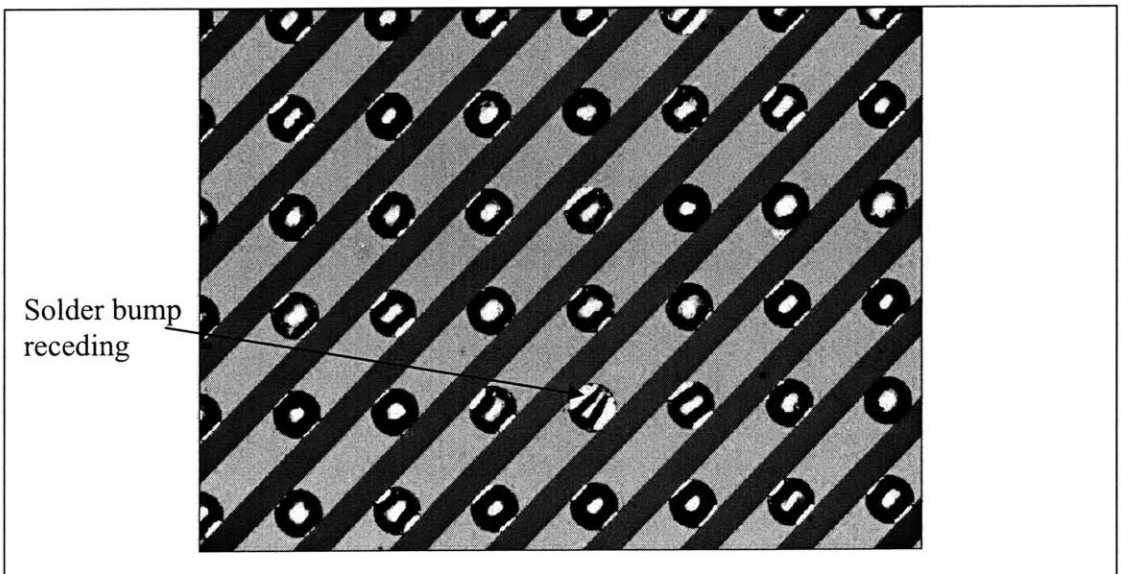


Figure 4-7: Solder bumps receding after 15 minutes in solder bath at 85°C

De-wetting and receding of the solder bumps were also observed on a Pyrex chip with Cr/Au/Cr/SiN under the same conditions (Figure 4-8).

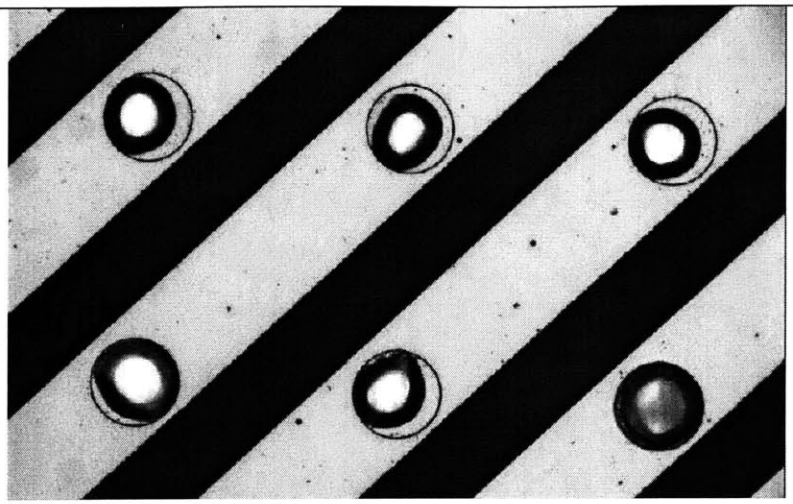


Figure 4-8: Solder bumps receding on a Pyrex chip with Cr/Au/Cr/SiN

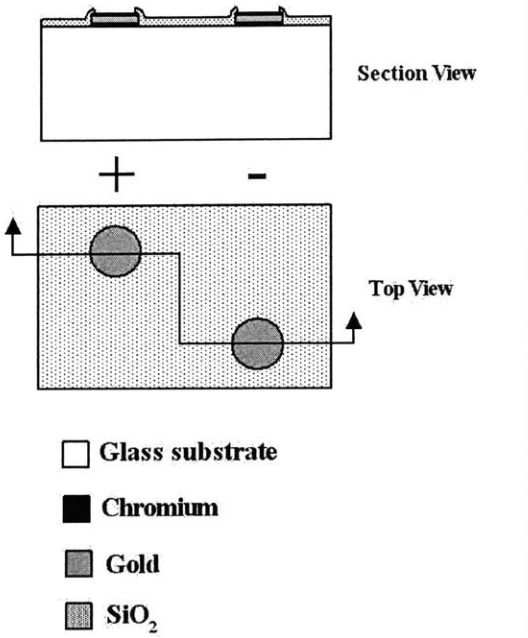
The de-wetting phenomenon can be explained by the fact that during wetting, the gold contact pads dissolve into the molten solder. The rapid dissolution of gold in tin-containing solders is well-known [5,17], and this is due to the strong interaction between gold and tin, making gold highly soluble in molten tin and reacting to form the intermetallic $AuSn_4$. The rate of dissolution depends on various factors such as substrate metal, solder composition, temperature and flow velocity of the solder [5,17].

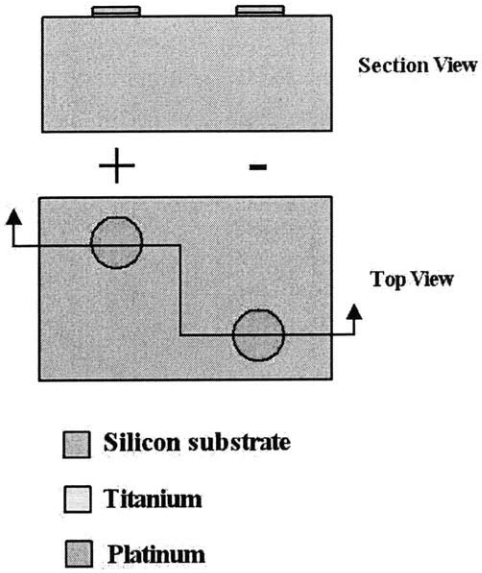
4.3.1 Fabrication change (addition of copper)

It has been shown that the dissolution of gold is greatly reduced by using tin-free solders or In-based solders [5,17]. Since the solder alloy (LMA-117) used has a low tin composition, it is safe to say that the rate of dissolution of gold is not as high as one would expect with other conventional solders containing higher percentages of tin. Nevertheless, to counter this problem, it was decided that the 220 nm thick gold layer be replaced in favor of a 150 nm thick copper layer with a thin (20 nm) layer of gold as a protective metallization against oxidation. This is because in general, the dissolution of copper in molten solders is much less rapid than gold [5]. Moreover, copper is commonly used as a base metal for many soldering processes, including the well-known flip chip technology [20,21]. Even though a thicker copper layer would last longer

against dissolution, the thicknesses of copper and gold layers are chosen because the thickness of the metal stack is constrained by the lift-off process shown in Figure 3-16.

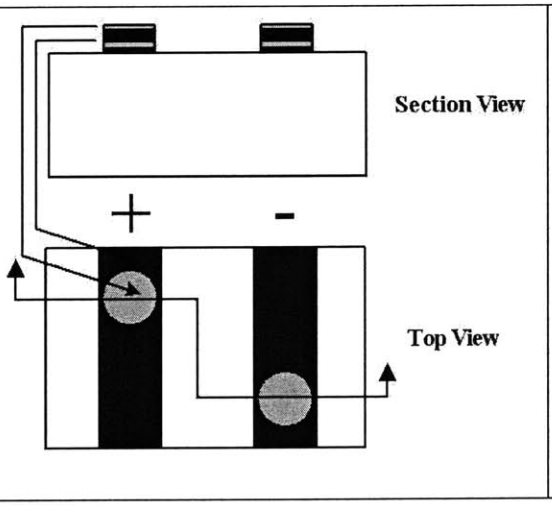
The long wetting time observed with the Cr/Au/Cr/SiO_2 substrates could be attributed to one or several of the following reasons: uncleared oxide or chromium on the contact pads, cleanliness of the contact pads, oxides in the molten solder, diffusion of chromium atoms into the gold layer at the interface. Earlier solder coating (wetting) experiments with severely over-etched (~5 μm) circular platinum contact pads on a silicon wafer (the platinum was the last film deposited) showed solder bumps had formed after 1 min in the solder bath. Since gold and platinum are in the same class of noble metals with nominally similar excellent wettability characteristics [5,14], the wetting times should not have differed by so much on the same size scale. This observation points to the main difference between the two experiments, which is the order of deposition of the noble metal (Pt was the last layer deposited while the Au was not). Figure 4-9 shows the different substrates and their relative wetting times and it seems to suggest that depositing the noble (highly wettable) metal layer in the final surface micromachining step will help in alleviating many of the above possible issues with regard to the long wetting time and variable rates of wetting. Since chromium is not wetted by solder, a slightly different process is designed which builds upon the existing chromium lines (inter-digitated fingers) using Cr/Cu/Au pads from a lift-off process shown in Figure 3-16 and described in Section 3.1.2.1. Figure 4-10 shows the cross-sectional profiles for the modified substrate design, and a simplified design to test the solderability of the new Cu/Au pads.

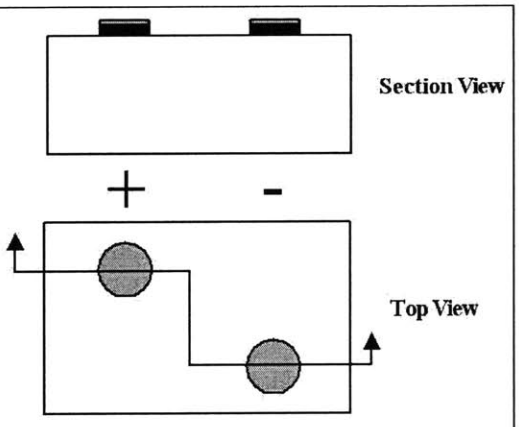




- Long wetting times - Variable rates of wetting across substrate * Au is not the last film deposited	- Short wetting times - More uniform wetting across substrate * Pt is the last film deposited

Figure 4-9: Comparison between different substrate designs and wetting characteristics





Glass substrate | Chromium | Copper | Gold

Modified substrate design	Simplified substrate design

Figure 4-10: New and simplified substrate designs

During the cleaning of the modified substrates in preparation for the solder coating process, a mistake was made through the use of concentrated sulphuric acid (to remove organics), which severely undercut the copper leading to under-sized solder bumps and a high percentage of de-wetting (Figure 4-11, not to scale).

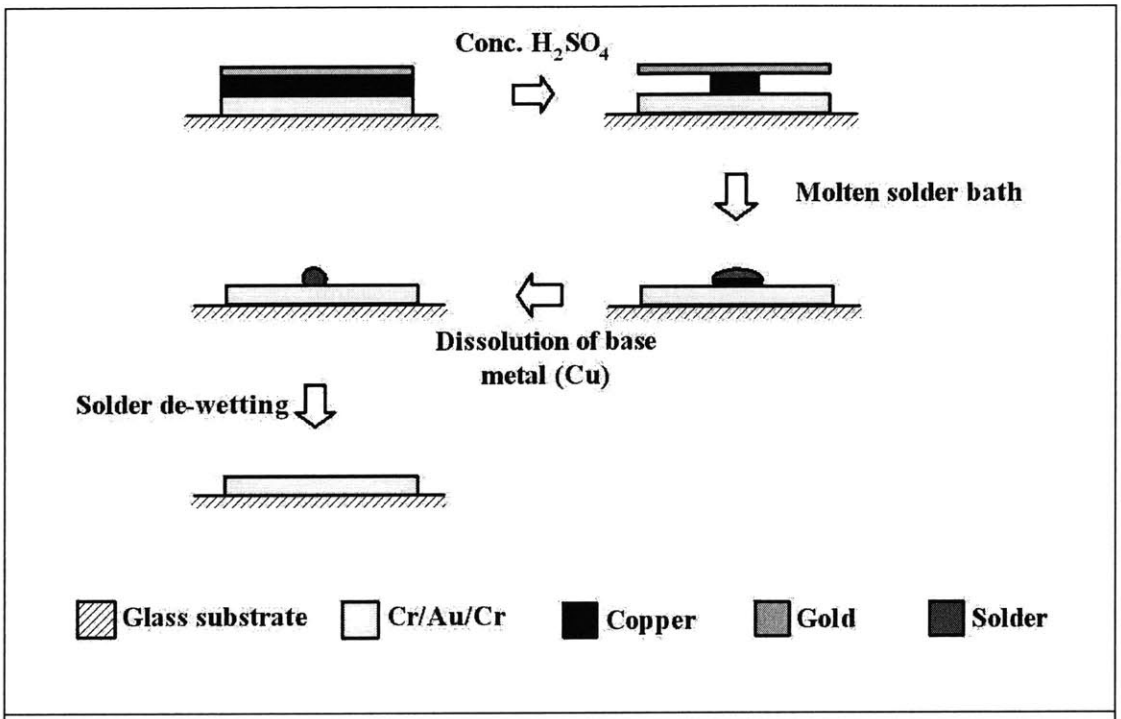
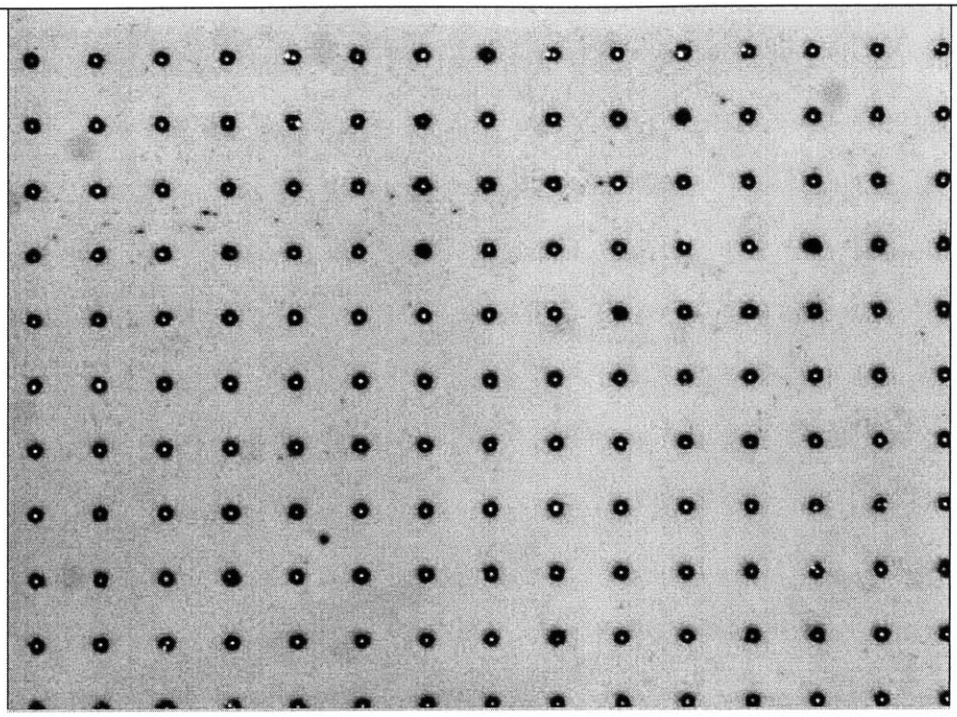


Figure 4-11: Solder de-wetting due to under-cutting of copper during H_2SO_4 clean

Since the turn-around time for the simplified substrate design is much shorter and the aim is to test the solderability of the new metal stacks (with copper as the base metal), the subsequent batch of substrates was fabricated using the simplified design shown in Figure 4-10.

The solder coating test using the simplified substrates displayed very positive results in terms of wetting time and uniformity of wetting across the chip. Using the same dilute acetic acid flux as before and a solder temperature of 85°C with a 45° removal angle and about 1cm/sec removal speed, it takes 1 min to reach the solder bump formation as shown in Figure 4-12.



* The small dark blue circles are the solder bumps; the white speck at the center of each circle is due to the light reflecting off the top of each solder bump.

Figure 4-12: Faster and more uniform solder wetting using the simplified substrate design

Figure 4-13 shows two pictures of solder bumps taken at higher magnifications. It is observed that the edges are not smooth and that there is slight de-wetting of the solder at the edges. This seems to suggest that the solder bump has begun receding and that the dissolution of the copper in the solder is much faster than anticipated. This may be due to the very thin copper film used (150 nm); the thickness of the Cr/Cu/Au stack is limited by the height of the photoresist in the lift-off process using the OCG 825 positive resist. It is also noted that there is a lack of information on the dissolution rate of copper in the solder since the solder LMA-117 is not widely used in industry (due to its very low melting point and cadmium content) and thus has not been well-characterized compared to the common tin-lead solder. Nevertheless, this marks a major improvement in the solder coating process.

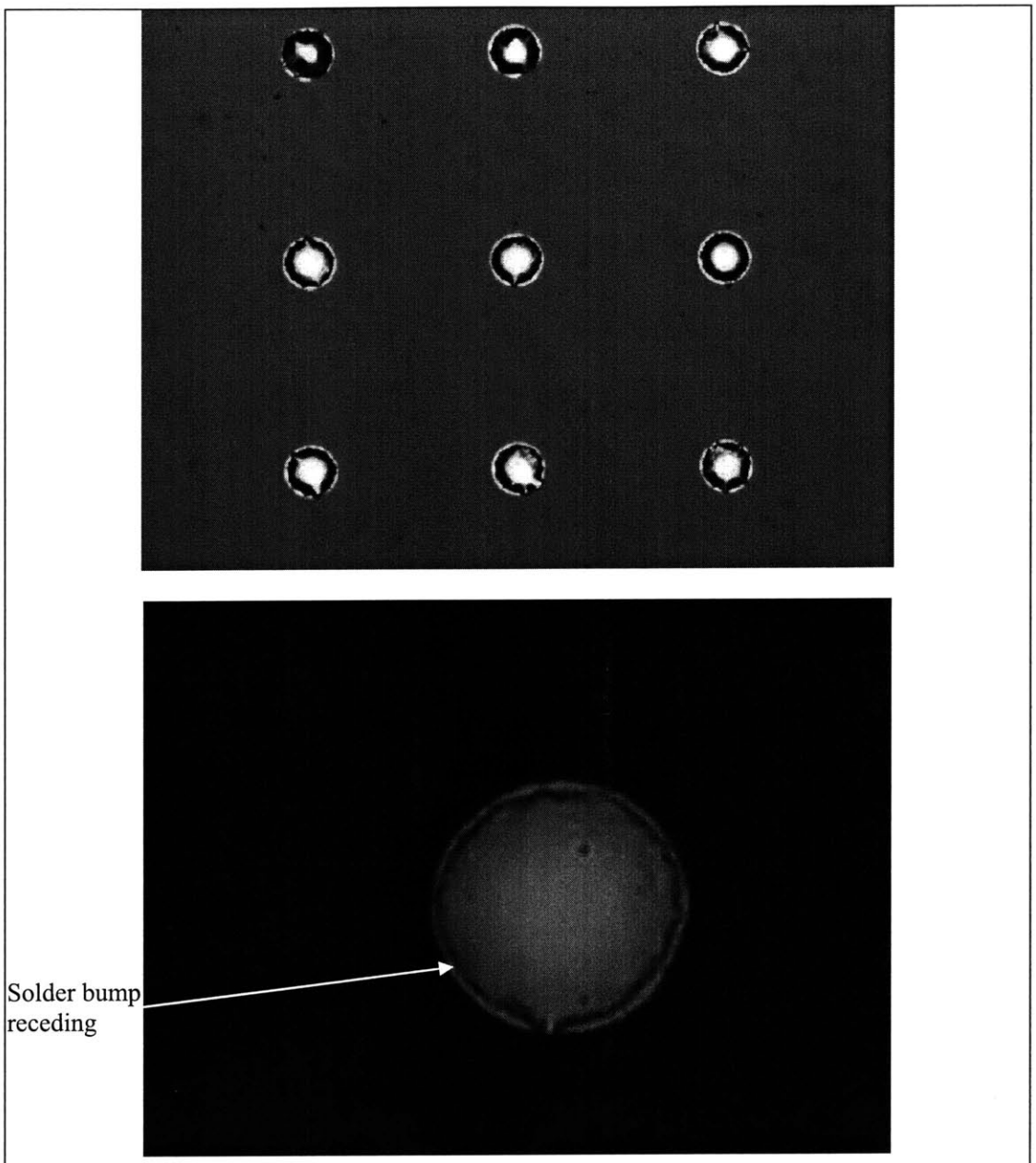


Figure 4-13: Signs of solder receding at the edges after 1 min (simplified substrate design)

Chapter 5 Testing and Characterization

5.1 Assembling the posts

By definition, self-assembly is a spontaneous process that occurs in a statistical, non-guided fashion [22]. During the self assembly process, the chip is flooded with posts and where a particular post lands and its initial orientation is a random event. Minimization of the free energy of the solder-water interface provides the driving force for the assembly. More specifically, fluidic self-assembly is driven by the gradient in interfacial free energy when the post approaches a substrate binding site. An effective self-assembly system will exhibit a clear global minimum for the desired assembly configuration, while avoiding (as much as possible) local minima or regions of low energy gradient corresponding to undesired configurations in which the posts could get stuck [22].

The self-assembly process is the final and most crucial step, and is the focus of this project. The step only takes a few minutes compared to the many hours of microfabrication, but in the matter of that few minutes, one can determine the relative success or failure of the self-assembly experiment. Utmost care must be taken to clean and prepare the chips and the silicon posts for the self-assembly process, or else the time spent in the fab would go down the drain. This section discusses the findings and conclusions drawn along the way from the time the author increased the yield from zero to 2 out of 7500 possible sites, and to the latest yield of slightly more than 50%.

Table 5-1 compares the parameters for the solder self-assembly among the different groups. Several parameters are found to be important factors affecting the self-assembly yield, as will be discussed shortly. Some of the information is estimated or inferred from the papers [2,16].

Parameter	Whitesides (prototype) [2]	Whitesides (larger scale assembly) [2]	Howe, Scott [16]	Cell trap self-assembly
Substrate material	flexible copper-polyimide composite sheets (cylindrical)	flexible copper-polyimide composite sheets (cylindrical)	No info, probably silicon	Pyrex
Die/chip size	170 mm^2 (cylindrical with 3mm diameter)	5 cm^2 (cylindrical with diameter < 5mm)	1 cm^2 (square)	656 mm^2 (20.5 mm x 32 mm)
Size of a receptor site	280 μm square	280 μm square	400 μm square	20 μm diameter
Receptor material	Copper	Copper	10 nm Cr and 120 nm Au	30 nm Cr : 150 nm Cu : 20 nm Au
Number of assembly/receptor sites	113	1600	No info	7 536
Area occupied by assembly sites (including spaces within the arrays)	38 mm^2	5 cm^2	No info	56 mm^2 (7 mm x 8 mm)
Parts material	GaAs/GaAlAs LEDs (with a	Silicon blocks with 10 nm Cr	JFETs (Junction Field	Silicon posts with 10 nm Cr

	small circular gold contact and a large square gold contact on opposite faces)	and 400 nm Au on one face	Effect Transistors) with Au on the backside	/ 120 nm Au caps
Part size	280 μm x 280 μm wide x 200 μm tall	280 μm x 280 μm wide x 400 μm tall	400 μm x 400 μm wide x 200 μm tall	25 μm diameter x 50 μm tall
Type of assembly beaker	Cylindrical 1-ml vial with inside diameter of 5 mm	Cylindrical 1-ml vial with inside diameter of 5 mm	Flat dish, no additional info	Droplet method
Vol of flux used	No info, but can be up to 1 ml	No info, but can be up to 1 ml	No info	9 to 12 drops (each drop about 45 μL)
Number of parts/posts used	No info	~5000	No info	About 30 000
Heat source	Heat gun	Heat gun	No info, probably hotplate	Hotplate
Temperature	90°C	90°C	70°C	85°C
Assembly time	1 to 2 mins	3 mins	1 to 2 mins	4 mins
Assembly yield	100%	98%	No info	~50%

Table 5-1: Comparison between the self-assembly methods in different groups

A variety of self-assembly experiments was conducted under different conditions and set-ups to determine the important parameters affecting yield, and the results will be discussed shortly. Many of the experiments with low yield are associated with one or more of the following reasons:

1. Low concentration of posts (too much flux and/or too few posts)
2. Non-ideal assembly beaker (too large) which correlates to the first reason because posts are distributed around the beaker and not solely concentrated at the assembly sites
3. Lack of agitation of the flux and posts which translates to low sampling frequency
4. Poorly wetted chips (varying rates of wetting and incomplete array of solder bumps)
5. Long time lapse between solder coating and assembly steps, during which the solder bumps are oxidized in air (ambient conditions)
6. Extended assembly time and temperature leading to base metal consumption by the solder and de-wetting
7. Cleanliness of the silicon posts
8. Gold caps peeling off the silicon posts due to prolonged HF exposure under-cutting the chromium adhesion layer

Concentration of posts and size/type of beaker used for assembly

The quantity of posts in the assembly liquid (henceforth termed posts concentration) determines greatly the self-assembly yield. Due to the limited quantities of the posts (in terms of volume) and the efforts required in fabricating and collecting them, and also the lack of knowledge regarding the self-assembly process, the posts were used sparingly in the initial assembly experiments, thus leading to zero or very low yield. Figure 5-1 shows one early example of solder self-assembly on this scale using a rather low posts concentration. It is hard to quantify low concentration, but it would suggest something on the order of several thousand posts in more than 15ml of flux. Figure 5-2 shows an increase in yield when the posts concentration is increased (on the order of 10^4 posts in about 10 ml of flux, or about 1000 posts/ml). In this experiment, the flux level is only

slightly above the top surface of the chip so that when the beaker is agitated, and the suspended posts can circulate about the solder sites.

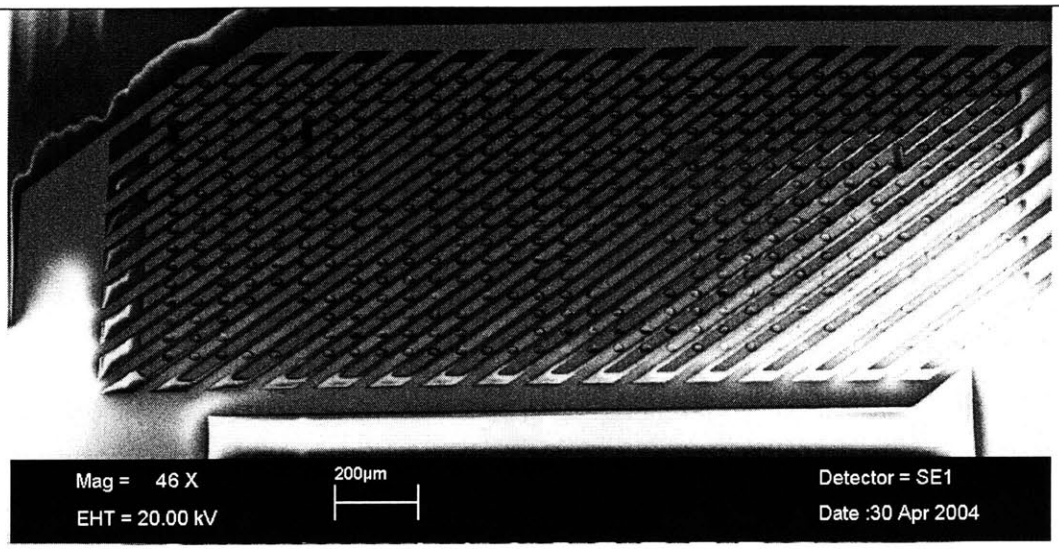


Figure 5-1: Low assembly yield

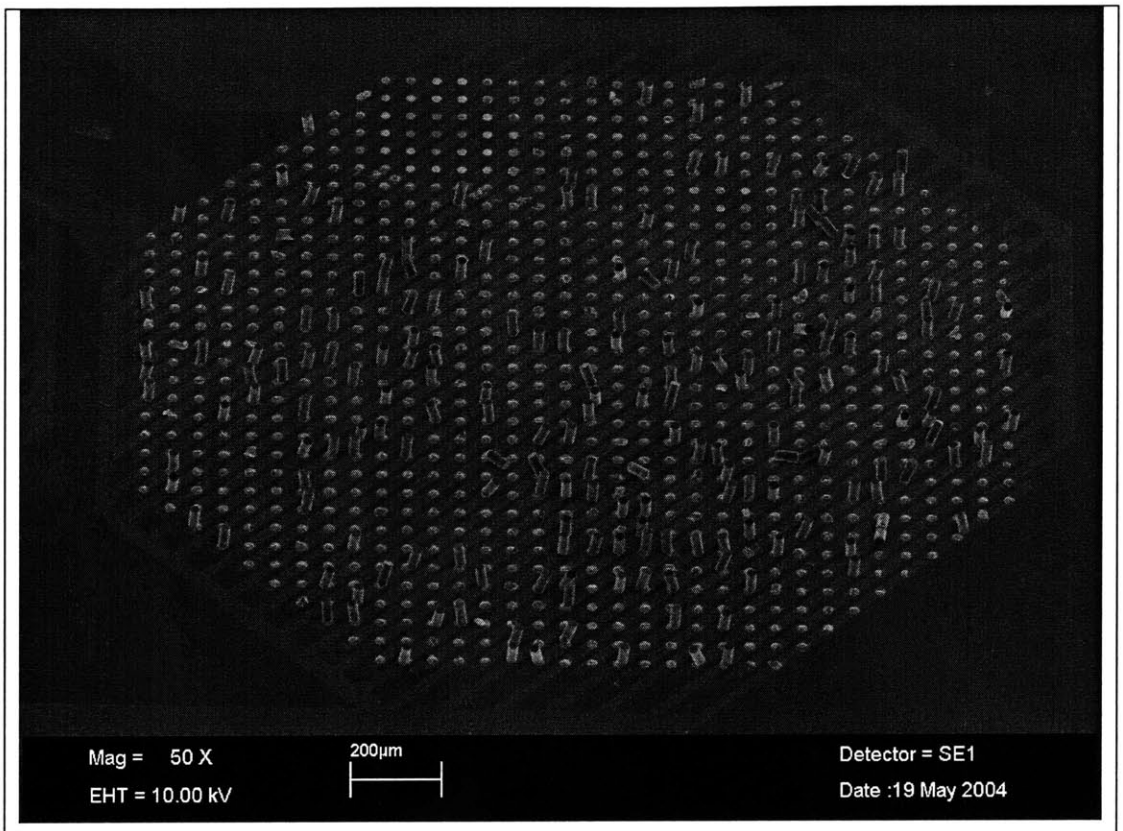


Figure 5-2: Moderate assembly yield

For the final experiment runs, the quantity of posts can be estimated. There were 16 749 posts on one SOI die 16mm by 16mm and the posts on 48 dies were released and stored in 12 vials. Assuming a (conservative) 10% loss of posts during the dilution and collection steps, there are roughly about 60 000 posts in one 1.5 ml vial (±20% since it is very difficult to estimate the quantity of the micron-sized posts in the vial and due to variations during collection).

To improve the self-assembly, an attempt was made to localize the flux and posts onto the contact sites using a 'beaker' on the chip. The 'beaker' is made from PDMS and molded in the form of a chamber shown in Figure 5-3. The chip with the PDMS chamber was placed onto an aluminum foil surface on the hotplate right after solder coating, and approximately 2 ml of flux with 60 000 posts (1 vial) (for a concentration of about 30 000 posts/ml) was then dispensed into the chamber using a pipette. This method worked fine,

but many posts were stuck on the sides of the PDMS chamber due to hydrophobic interactions. The posts could not be washed off even after rinsing and soaking the PDMS chamber with methanol. This approach was abandoned due to the loss of posts to the PDMS, and also the difficulty in planting the PDMS chamber without too long a lapse after the solder coating (oxidation). It should be noted that PDMS adheres very well to hydrophobic surfaces (the Pyrex substrate is an example), and also the surface tension of water prevents any leakage during the assembly process.

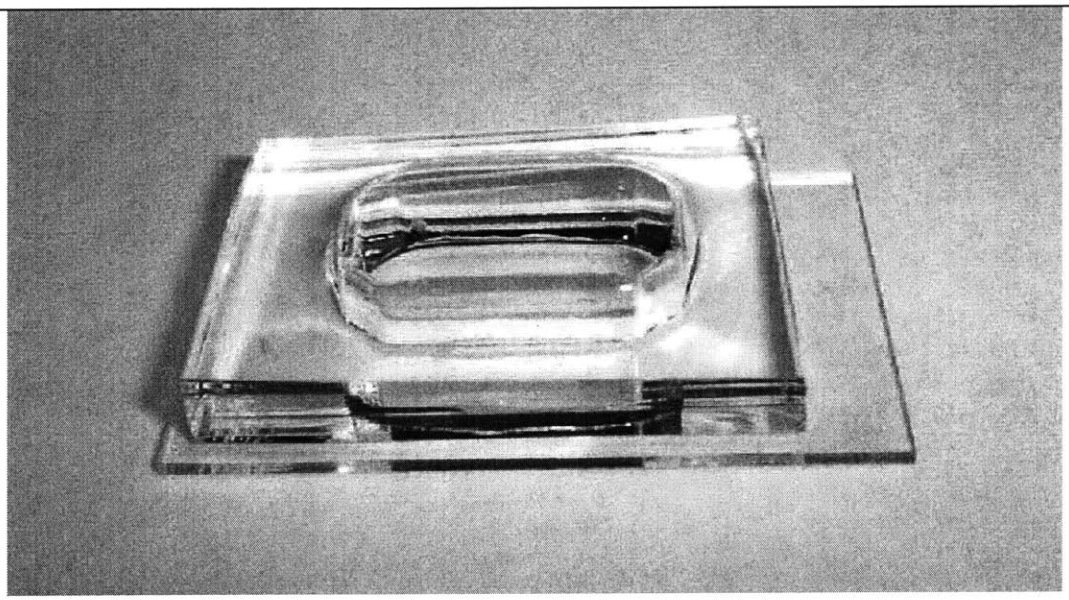


Figure 5-3: PDMS chamber

The PDMS chamber inspired another idea regarding localization of the assembly process. This uses the surface tension of water (dilute acetic acid) to concentrate the posts in a single large droplet on the contact sites area as shown in Figure 5-4. Most of the water in the vial was removed and replaced with about 0.5 ml of flux (slightly more than enough to cover the posts in the vial). About 9 to 12 drops of the flux and posts (one drop is approximately 45 μL) were drawn using a pipette a little at a time, and then directed carefully onto the center of the chip where the solder bumps are. Since it was not possible to extract all or most of the posts in the vial (without using more flux to rinse the remaining posts off the sidewalls of the vial), it is estimated that about 30 000 posts were dispensed on the chip (the concentration is about 2 500 000 posts/ml). The assembly

time was 5 minutes on the hotplate with occasionally swirling (using a pair of tweezers to hold the chip). The highest yield to date (>50%) was obtained using this droplet method (see Figure 5-5). However, the droplet method suffers from an agitation limitation as will be discussed shortly.

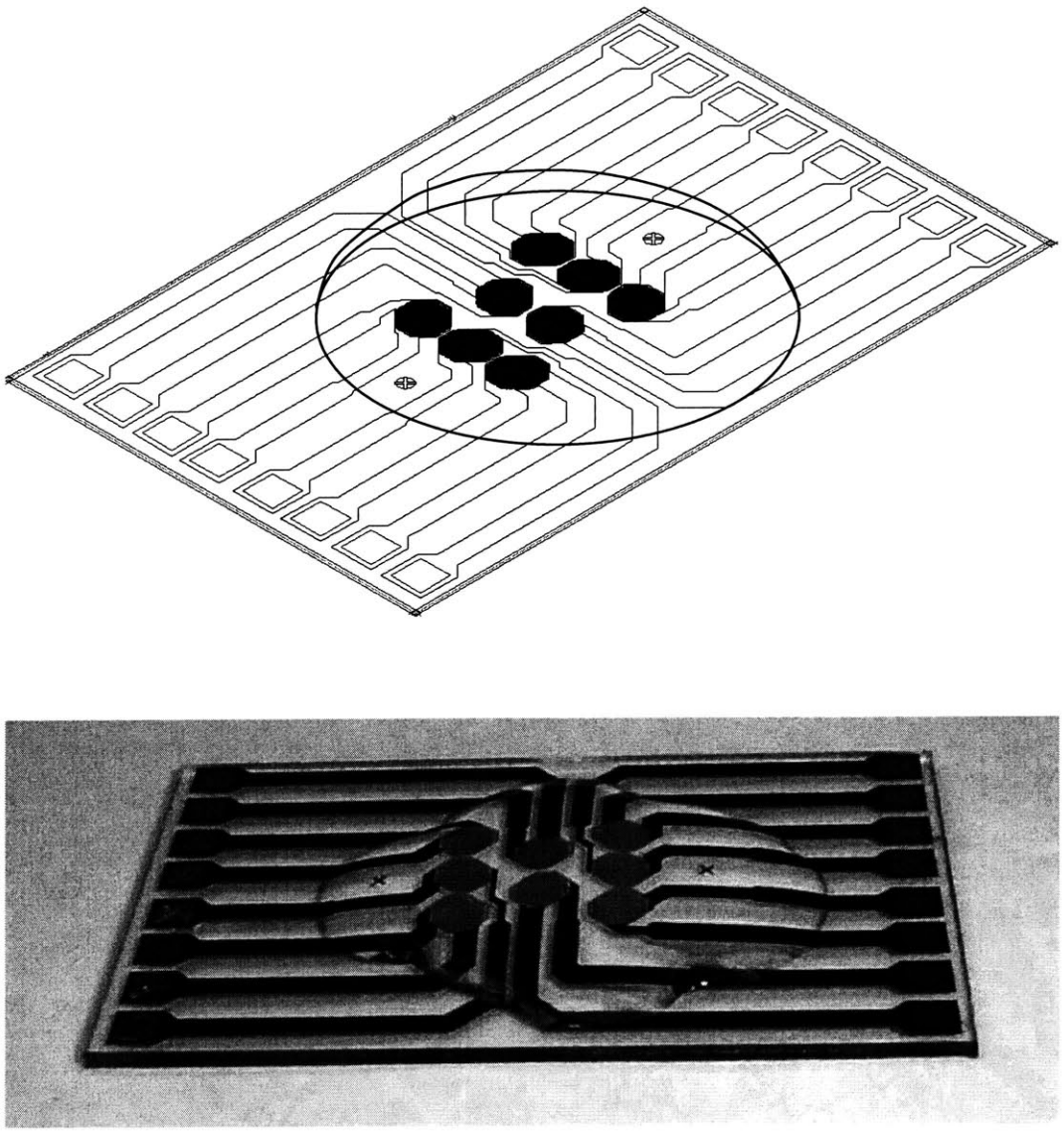


Figure 5-4: Droplet assembly method

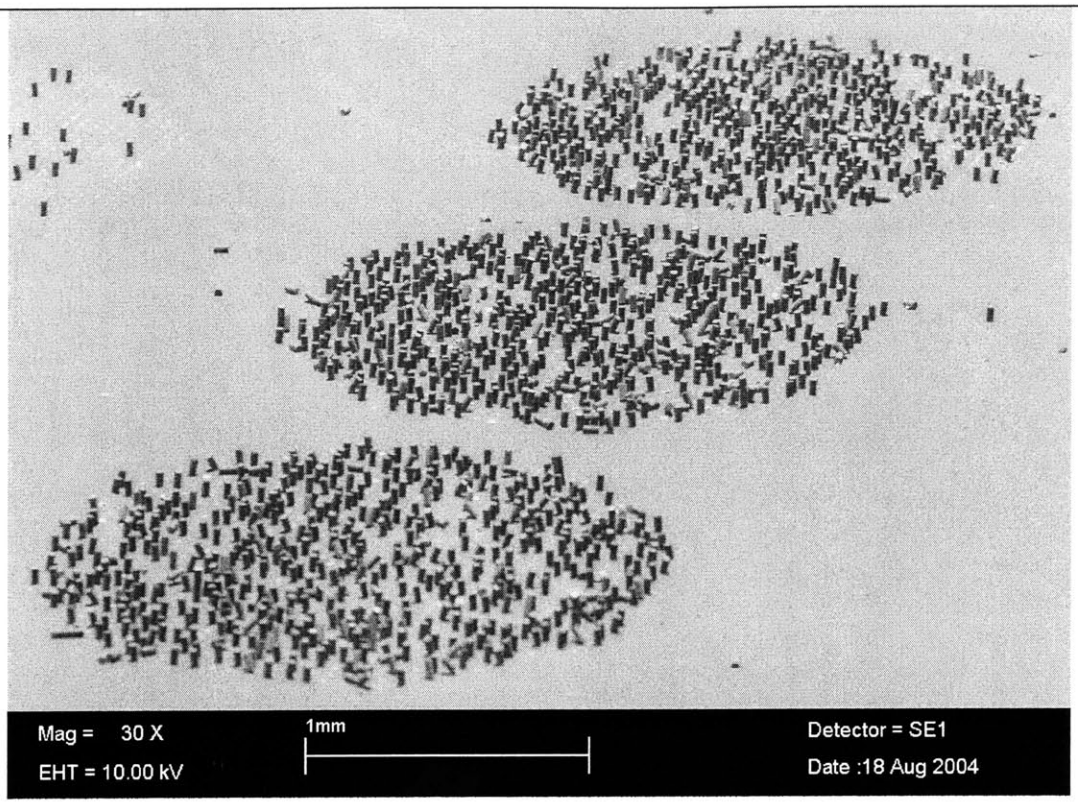


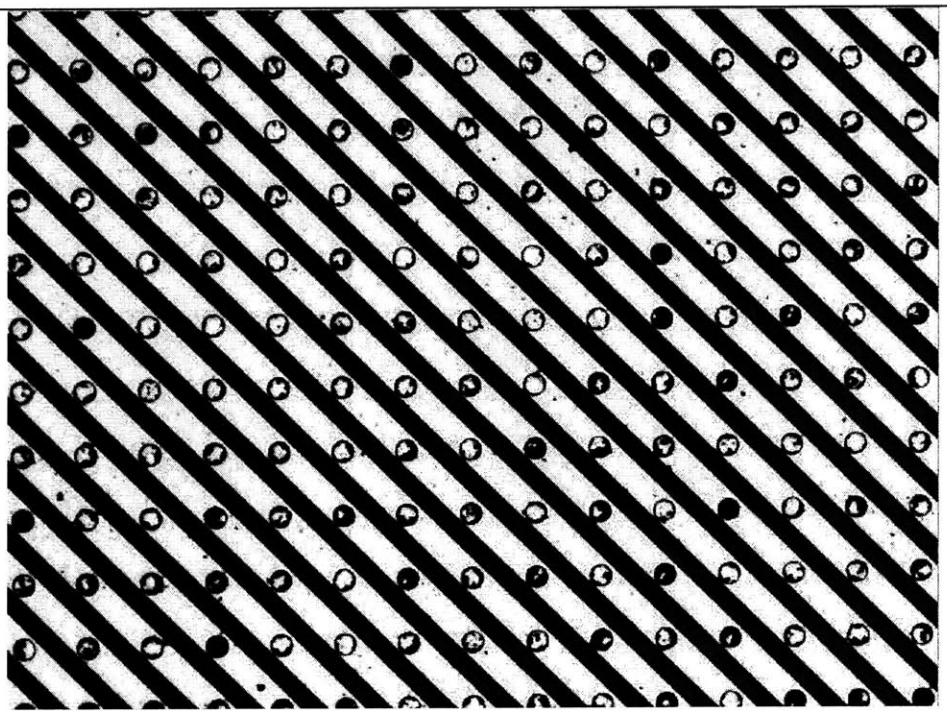
Figure 5-5: High assembly yield

Stirring/shaking during assembly process

During the assembly step, lack of agitation of the flux and posts translates to low sampling frequency which reduces the yield. Without shaking the assembly beaker and its contents, the posts will settle to rest on the bottom of the beaker and on the chip. Intuitively, it is clear that the probability of a post reaching an assembly site is very low if the process were static. Circulation of the flux is required to carry the posts around so that more sites can be sampled and for assembly to take place. However, one might expect that constant shaking makes the process too dynamic and even though the sampling frequency increases a lot, there is not enough time for the solder bumps to wet the gold cap of the posts once they come into contact. Thus, intermittent shaking should be ideal; in the assembly experiments conducted, typical agitation patterns were about 10~15 secs agitation at about 1 min intervals. The agitation step is also visual based, and one of the main objectives is to concentrate the posts onto the center of the chip (where the assembly sites are) by swirling the beaker or chip which causes the posts (carried by

the flux) to spiral inward. It is very difficult to characterize the agitation process due to the dynamics involved and the small size of the posts and also since the shaking is carried out manually by hand. Suffice to say, circulation of the parts/posts is an important aspect since the posts are large enough for gravity to have a considerable effect on them.

Early experiments on self-assembly using ultra-sound to direct the posts to the substrate met with failure. The solder-coated chip was placed in a small Pyrex beaker, and a glass pipette was used to draw the flux and posts from a plastic vial, and to dispense it onto the chip. The beaker with its contents was then placed into a water ultra-sound bath at 68°C for 3 minutes. The energy of the ultra-sound knocked off parts of the micron-sized solder bumps as shown in Figure 5-6. The ultra-sound method proved too aggressive and had zero yield, and was thus discontinued.



* Note the bits and pieces of the solder bumps chipped off by ultrasound in water.

Figure 5-6: Effect of ultrasound on solder bumps

It has been observed that the incidence of posts lying horizontally is higher within the arrays than elsewhere on the chip (Figure 5-7). This is especially evident for the droplet self-assembly method in which the assembly liquid is contained on the chip rather than in a beaker. This limits the agitation since all swirling has to be carried out slowly and with care to prevent the assembly liquid from flowing over the sides of the chip. Posts often get wedged within the array due to the layout of the chip and the high aspect ratio of the silicon posts. At the same time, the assembled posts will also obstruct the other free posts from accessing the sites within the array. This problem could be more prominent if the external regions of the arrays are filled with assembled posts first because the free posts have to arrive from above the height of the posts (either vertically or at an angle) in order to access the inner regions of the arrays. It is very difficult for the posts to tunnel within the arrays due to the spacing between assembled posts; the length (50 μm) and width (25 μm diameter) of the posts is large relative to the 35 μm gap size between two vertically and correctly aligned assembled silicon posts. In addition, it has been calculated that since the posts sink very quickly (a rough calculation assuming a silicon sphere of the same volume as the post gave a terminal velocity in water of about 2.7 mm/sec), agitation of the chip during the assembly step is necessary both to circulate the posts and to attempt to remove wedged posts within the arrays.

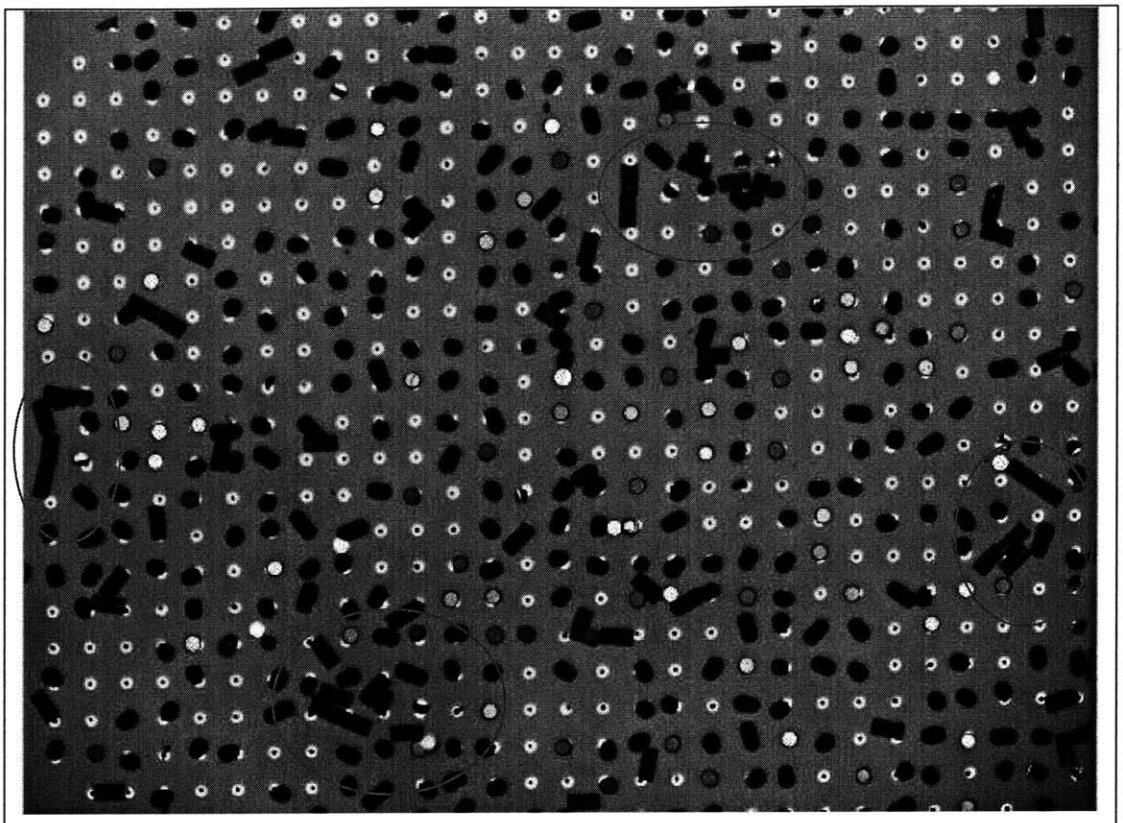


Figure 5-7: Horizontal posts within an array (circled)

Poorly wetted chips

This problem occurred primarily on the substrates with the original design on which the gold layer was not the final layer deposited and had to be exposed by etching back the dielectric layer (SiO_2 or SiN) and top chromium layer respectively (Figure 3-15). Using the modified or simplified designs (Figure 4-10), this problem was solved, even though occasionally a small percentage of the arrays (<5%) do not wet, and it is usually concentrated in a small region, i.e. there are no stand-alone non-wettable contact pads. This could be due to organics not removed in the cleaning process, oxides in the solder, or air bubbles as discussed previously.

Time lapse between solder coating and assembly step

The assembly step should begin right after the substrate is coated with solder and removed from the solder bath. It had been observed in early experiments that chips

which were rinsed with water after the solder coating and subjected to a long time lapse between the two steps showed very low yield after the assembly process. This is likely because the solderability of the solder bumps is affected by the surface degradation due to oxidation and/or contamination during the shelfing period. Therefore, to assure good surface quality of the coated solder bumps, the shelf time and storage temperature must be minimized, and the self-assembly step should be carried out in the shortest time possible after the solder coating step.

Assembly time

Other groups reported assembly times ranging from 1 to 3 minutes [2,16] using the same solder for self-assembly. It is speculated that most of the assembly occurs in the first couple of minutes, and the assembly time used in this project is about 4 minutes. Interestingly, it has been observed that the yield does not increase (or at least significantly) with time. In theory, a longer assembly time would allow more sampling of the sites and lead to a higher yield of assembled posts. However, this is different in the case for solder self-assembly. During the self-assembly process in which thousands of silicon posts contained in a dilute acetic acid are directed towards the substrate, the molten solder bumps continue to consume the underlying base metal on the substrate chip as well as the gold caps on those silicon posts which have been assembled. De-wetting occurs, and the solder bumps recede even further and begin balling up. In extreme cases, under extended periods of self-assembly at elevated temperatures, the solder bump can de-wet totally and lift off the substrate, together with the silicon post (if assembled). Attempts to subject chips that had undergone the assembly process (and been cleaned) to a second round of assembly process to see if there is a further increase in assembly yield had been met with futile. This could be due to oxidation of the solder bumps as mentioned earlier. Thus, it can be concluded that long assembly times can be very detrimental to the self-assembly process yield, and that the process should be planned and carried out carefully since there is only one valid try per chip.

Assembly temperature

In the experiments described here, it is difficult to measure the assembly temperature because of the low volume of flux used, especially when the chip is placed on the hotplate (for the droplet self-assembly method). The accelerated evaporation of the flux at such high temperatures (estimated to be between 85° to 100° C) often lowers the flux level by so much that the chip surface is exposed to air, and the posts get stuck on the surface when the flux dries up. Additional flux has to be introduced into the assembly beaker to wet the posts and to circulate them around the chip. This causes temperature fluctuations within the assembly flux/beaker and thus, it is impossible to reach steady-state and thermal equilibrium under the above conditions. There is a trade-off between using too much flux for the assembly step which lowers the concentration, and using too little flux which evaporates much quicker. For the droplet assembly method, the trade-off is removed since the chip surface can only accommodate about 6 to 8 drops of highly 'concentrated' flux before it over-flows the sides. However, placing the chip on the hotplate increases the heat transfer greatly since it is now in direct contact with the heating source, and the elevated temperatures can cause the solder to consume the base metal much faster, leading to greater de-wetting and smaller solder bumps in the same length of assembly time (Figure 5-8). Thus, temperature control during the assembly process is very important in order for the solder bumps to withstand long enough assembly times to obtain a good yield. It is also noted that if a larger scale assembly set-up (more posts and flux in the same high concentration) were available, the process could be conducted in an enclosed beaker thus ensuring better temperature stability.

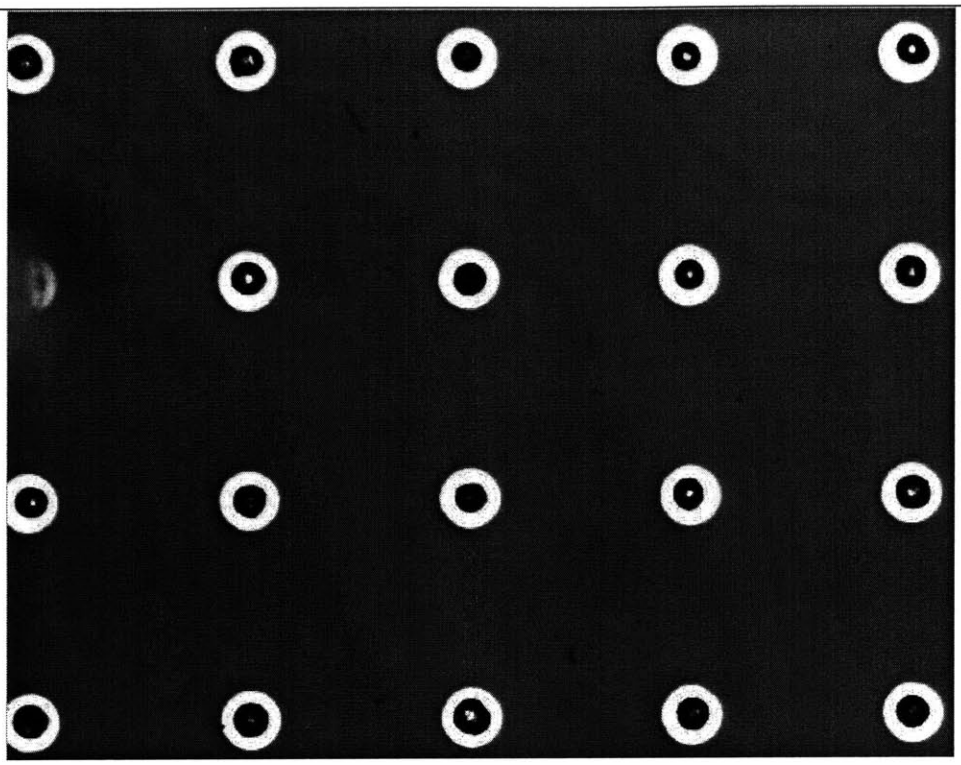


Figure 5-8: More severe de-wetting of solder bumps using droplet method

Cleanliness of silicon posts

The gold caps on the silicon posts need to be very clean and free of organics for solder wetting to take place. The cleaning step involves removal of the protective resist using acetone, methanol, IPA, water, and a 1 min concentrated sulphuric acid dip prior to the HF release step. After that, the posts are rinsed with water (using successive dilutions) and stored in water. Very high self-assembly yield has been obtained using these 'fresh' posts. It has been observed that experiments using posts which have been 'recycled' have very low assembly yield. This could be due to contamination and the use of methanol and water to collect and clean the posts from the beakers. Several attempts had been made using concentrated sulphuric acid to clean the 'recycled' posts but they led to high loss of posts. This is because the acid is very viscous and the posts will suspend in the acid. Also, since sulphuric acid is a strong acid, copious amount of water is needed for dilution and each successive extraction of water leads to further loss of posts since the posts do not sink fast. Moreover, if the acid is not diluted fast enough (over the course of

a few minutes), the Cr/Au caps on the posts will be attacked and will begin peeling. The difficulty of the sulphuric acid primarily reflects the limit of the equipment available. A microfuge is used to extract the posts, but its small size ensures that the extraction process will take a long time. Nevertheless, the sulphuric acid clean for 'recycled' posts could be carried out if a bigger centrifuge were available.

Peeling and lifting of gold caps

Under prolonged HF and/or H_2SO_4 exposure, the chromium adhesion layer on the silicon posts will be under-cut which leads to peeling and lifting of the Cr/Au caps. Without the caps, the posts are useless since they will not be wetted and these constituted a large proportion of the posts in early batches when little then was known about the effect of the acids on the caps. At the same time, some of the lifted Cr/Au caps will stick onto the solder bumps and occupy potential assembly sites as shown in Figure 5-9. Also, the partially peeled caps will curl, thus making it more difficult to wet or causing the posts to assemble at an angle as shown in Figure 5-10, and consequently resulting in a very weak solder joint.

Even though the amount of acid used and time in acid has been reduced as described in Chapter 3, the problem of the Cr/Au caps peeling is still not totally eliminated.

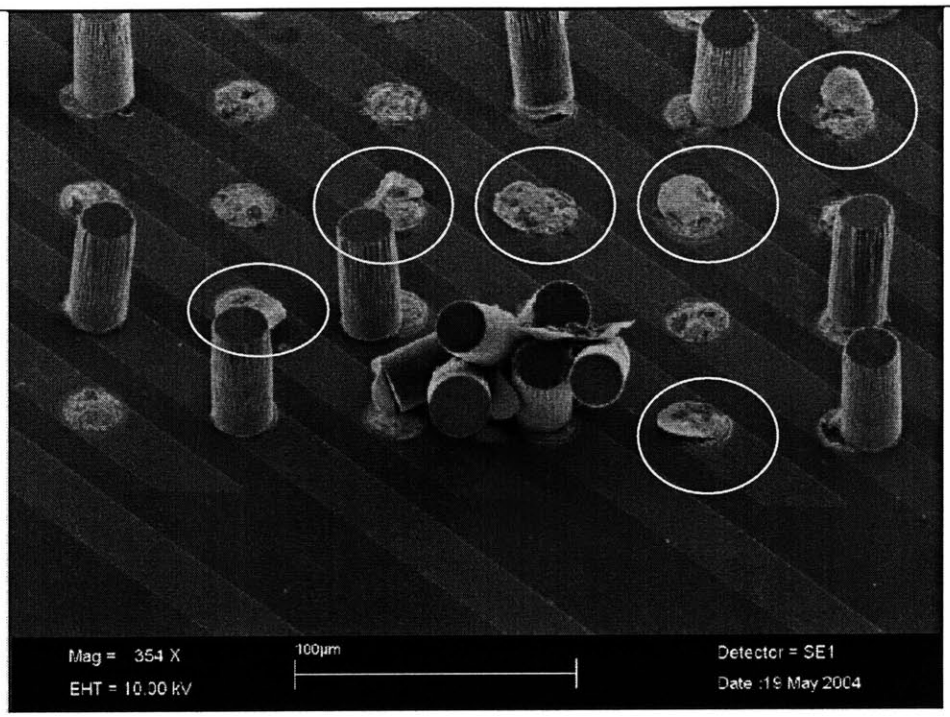


Figure 5-9: Cr/Au caps on assembly sites (marked in yellow circles)

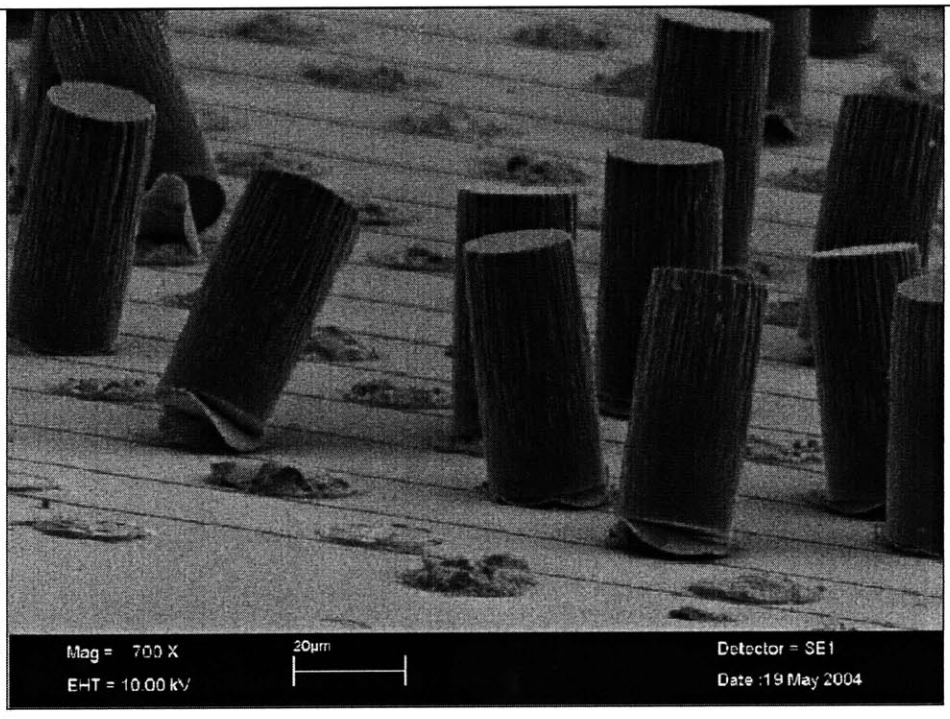


Figure 5-10: Peeling of caps leading to posts assembling at different angles

Orientation and alignment of assembled posts

Once the wetting process of the gold caps by the solder bumps is complete, the posts will align to an equilibrium position corresponding to an energy minimum. Figure 5-11 shows many posts assembled at different angles. This could be due to the posts arriving at an angle (or offset) and/or the solder de-wetting as shown in Figure 4-2. It is speculated that due to conservation of mass during the base metal dissolution in the solder, the solder bump will ball up. The bulge curvature will be similar to that described in the paper by Howe [16] which shows that no tilt correction will occur and the posts will remain assembled at the angle of arrival. In addition, the presence of asymmetric 'whiskers' on the solder bumps as shown in Figure 5-12 can also be a contributing factor to the above.

Only a small fraction of posts has been assembled vertically centered in the desired orientation. This can very much be due to the post landing with a larger area of overlap between its gold cap and the solder bump, which would imply an almost vertical arrival on the chip. These posts are less likely to reach a tilted equilibrium since the entire gold cap will be wetted by the solder and self-alignment to reach the global minimum will take place.

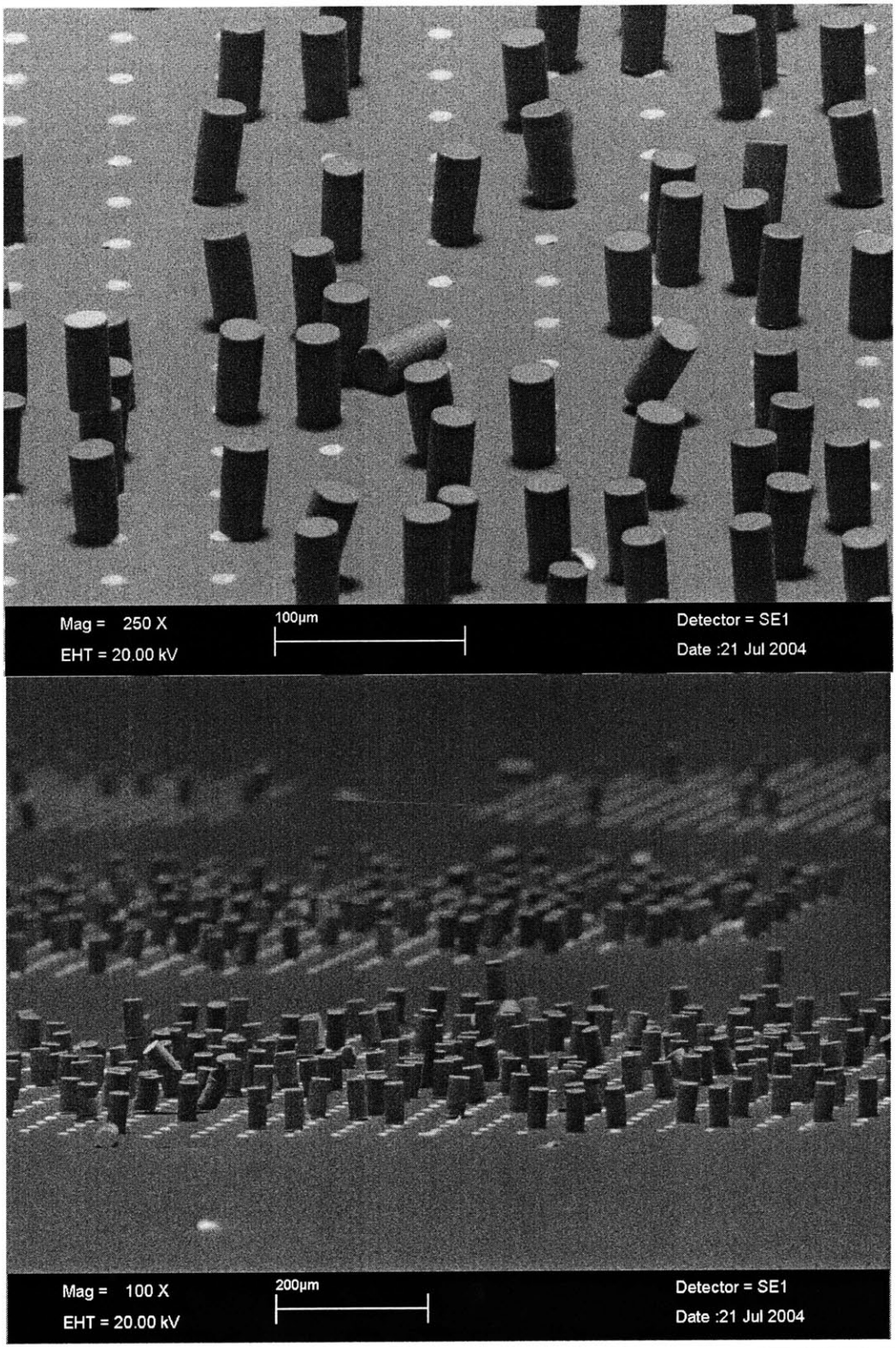


Figure 5-11: Posts assembled at different angles

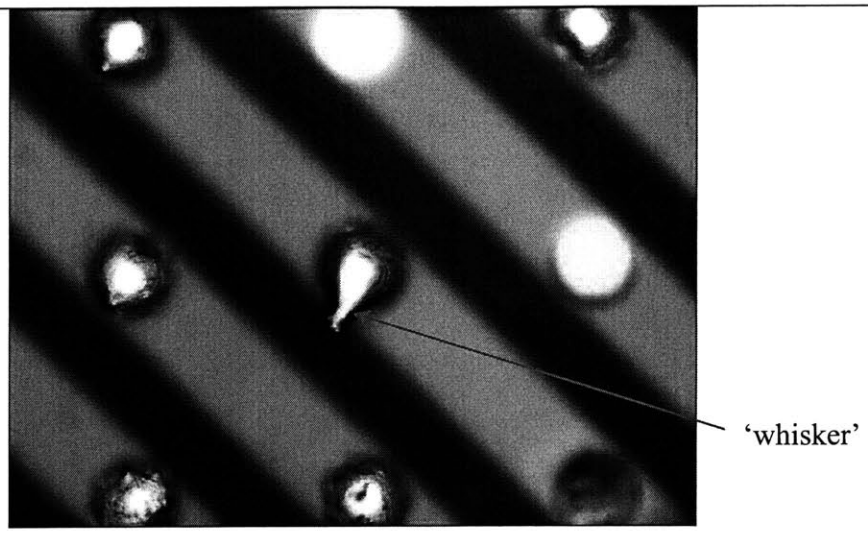


Figure 5-12: 'Whisker' on a solder bump

It has been shown theoretically that for circular shape-matched fluidic self-assembly, there exists only one global minimum at the center [22]. Figure 5-13 however shows posts assembled at a lateral offset from the center of the solder bumps, and this seems to suggest that there are local energy minima as well. This could be attributed to the fact that the gold circular pad is not purely 2-D, but has a lip on the sidewall extending about 3 μm down the top of the post (Figure 3-10), making it more like a very flat cup. When the posts arrive laterally shifted from the center of the solder bump, they will assume a local minimum position (Figure 5-13 and Figure 5-14).

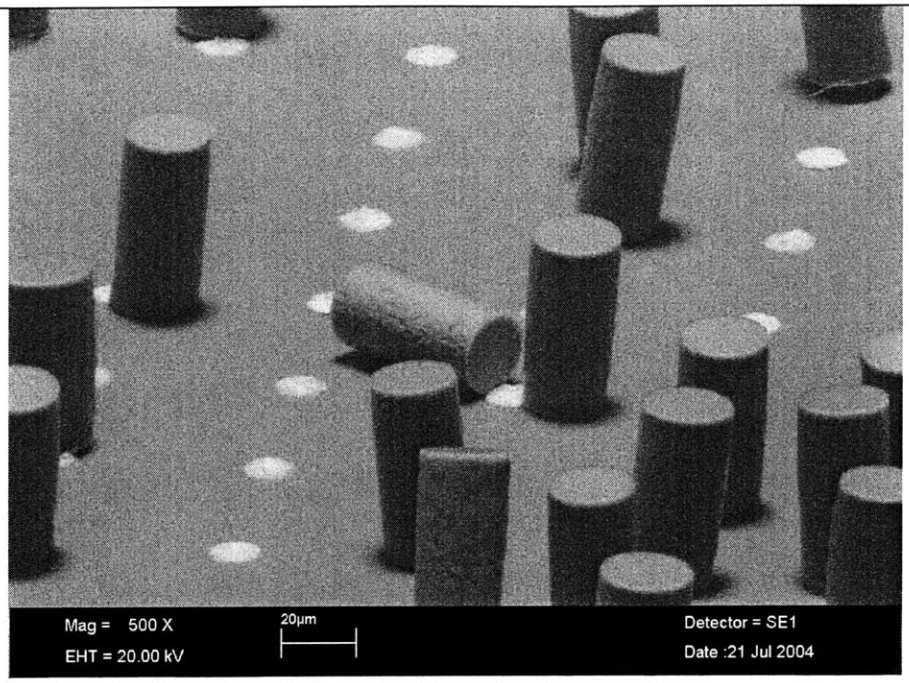


Figure 5-13: Posts assembled at a lateral off-set from center

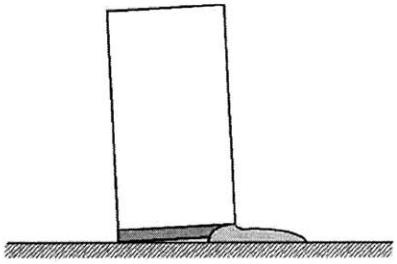


Figure 5-14: Schematic of a possible local energy minimum

Chapter 6 Summary

6.1 Summary and conclusions

In this project, self-assembly has been successfully demonstrated on high aspect ratio (2:1) parts on the 25-μm scale. This represents an order of magnitude smaller than the parts used in current MEMS self-assembly in literature, which are also mostly low aspect ratio (flat) plates. The highest assembly yield obtained was about 50%, and the critical factors in achieving these yields were high posts concentration, cleanliness of the substrate and silicon posts, temperature of the solder coating and assembly process, and agitation during assembly.

However, it is found that it becomes increasingly difficult to control component placement and orientation at these small size scales. This is because deviations in components and sites from their ideal geometries become relatively pronounced as feature size is reduced. At this scale, deviations in the size of the solder bumps and dewetting become critical. Small absolute changes in site diameter (a few microns) correspond to large relative variations in diameter (~10%) and area (~20%). These large relative variations can influence the final orientation of the assembled posts. In addition, the cleanliness of the gold contact sites is crucial since it can influence the rate at which the solder wets the surface. In cases where the contact sites are contaminated or have particles which can easily block off the entire site or regions (due to the small scale of the regime), wetting may not even proceed.

It may be possible to build this large an array of traps, but spacing and configuration of the sites relative to each other need to be redesigned in order to ensure circulation and easy access to sites within the array. The proximity and spacing between binding sites have to be designed with the diameter and length of the posts in mind.

Self assembly is a statistical process, and sufficient time and agitation are needed in order for all sites to be sampled. However, in solder assembly, more time can lead to solder recession and de-wetting, which may not have a large effect on self-assembly on the 200 to 300 μm scale, but which have considerable effects as the scale size decreases. The solder receding in this project is easily observed since it is large relative to the scale size, and as a result, self-assembly on decreasing scale size is greatly limited by the assembly time and temperature which contributes to solder recession and de-wetting.

The results have shown the posts to be assembling at different angles and orientation. This is highly likely due to solder recession (which causes the solder bump to ball up to form a more spherical shape) and the angle at which the posts arrive on the sites (which can affect whether the posts settle in a local or global minima). It is also noted that the solder recession effect is more significant at the smaller scale. Also, the offset positioning of the posts could be due to the lip of gold on the edge of the posts, which introduces some local energy minima.

In conclusion, solder self-asembly may not be the ideal method to make cell traps. The DEP-based cell trap depends on mainly three factors for its functionality: small size, conductive connections, and positioning/orientation. The solder self-assembly demonstrated is only able to achieve two out of the three factors reliably: small size and conductive connection. Due to the aspect ratio of the parts and the myriad reasons associated with the solder binding sites, it is very difficult to achieve the third. Nevertheless, the solder-assembly at this scale can be used for other applications which are non-orientation specific and use flat parts. The current status of this research limits it to applications in which the angular orientation and translational position is less important.

6.2 Future work

Self-assembly on the sub-100 μm scale can be achieved by other means such as SAM and hydrophobic adhesives [1,3], which are non-conductive by nature. Silver epoxy is a

conductive adhesive, but its viscosity makes it inappropriate for capillary-driven assembly. This also implies that it does not possess good self-alignment properties. At this size scale, electrical connectivity of components to substrate is hard to achieve because of the current limitations and instability of the solder process. A more robust solder process will greatly improve the chances of self-assembly on this small scale.

To achieve ideal orientation of high aspect ratio parts, one of the areas of improvement lies in the solder coating process. In theory, the size of the solder bumps can be controlled as shown in flip chip technology. A less expensive but viable method would be to evaporate the respective layers of the alloy metals onto the substrate in the right composition and desired thicknesses, and reflow the solder pad. This method would be limited by the metals available in an electron beam evaporation system, but would largely ensure uniformity in the size of the solder bumps.

Loss of posts during cleaning and collection is an issue since it constitutes a constant decline of the microscopic posts. A more efficient system could be designed to clean and collect the posts, automatically change the fluid within the vial, and also channel the posts and the flux to the binding sites during the self-assembly process.

In all the solder coating experiments, process reproducibility is a major limiting factor because in the first place, most soldering operations simply are not as precisely controlled with regard to local geometry and heat flow as we could hope. A better system or apparatus for controlling the temperature and agitation during the assembly will aid in improving the process. The assembly process should ideally be carried out in an enclosed vial to prevent the evaporation of the assembly liquid, and to maximize the area of contact (or minimize the distance) between the posts (in the assembly liquid) and substrate.

With the implementation of the above improvements, solder self-assembly has the potential to become a part of the microfabrication toolbox in the future.

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