SOLAR PHOTOVOLTAIC TECHNOLOGY:
CURRENT PROCESSES AND FUTURE OPTIONS

DREW BOTTARO AND JACOB MOSCOWITZ

DECEMBER 1977

MIT ENERGY LABORATORY REPORT - MIT-EL 77-041WP
This paper supports the Photovoltaics Technology Supply Industry task of the project entitled "Planning and Analysis for Development of Photovoltaic Energy Conversion System" supported at the MIT Energy Laboratory by the U.S. Energy Research and Development Administration (since incorporated in the U.S. Department of Energy). The task ran over the period from June 1 to August 31, 1977, and the information contained herein is valid as of that period.

The work reported here is not a completed study. A number of the important hypotheses need to be clarified and tested. However, because it is uncertain whether the effort on this task will be resumed, a summary of research through August 1977 is presented.

Lawrence H. Linden was the Principal Investigator on this task. The data-gathering efforts and early drafts were the primary responsibility of Jacob Moscowitz. Drew Bottaro was responsible for the day-to-day management of the task and the preparation of the final draft. During the period for which the task ran, the MIT Photovoltaic Program has been under the overall leadership of David O. Wood and Richard D. Tabors.

A number of individuals in the public and private sectors contributed their time to interviews; we hereby express our appreciation. However, the opinions or findings expressed herein are the responsibility of the authors alone. Neither the MIT Energy Laboratory nor the U.S. Department of Energy necessarily concur.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PREFACE</strong></td>
<td>1</td>
</tr>
<tr>
<td><strong>INTRODUCTION</strong></td>
<td>3</td>
</tr>
<tr>
<td><strong>I. Principles of Photovoltaic Generation</strong></td>
<td>4</td>
</tr>
<tr>
<td>A. Rudiments of Photovoltaic Electric Generation</td>
<td>4</td>
</tr>
<tr>
<td>B. Basic Design Considerations</td>
<td>5</td>
</tr>
<tr>
<td>1. Factors Affecting Cell Efficiency</td>
<td>6</td>
</tr>
<tr>
<td>2. Factors Affecting Module Efficiency</td>
<td>8</td>
</tr>
<tr>
<td>3. Factors Affecting Lifetime</td>
<td>9</td>
</tr>
<tr>
<td><strong>II. Silicon Process Technologies</strong></td>
<td>10</td>
</tr>
<tr>
<td>A. Overview of Stages of Production</td>
<td>10</td>
</tr>
<tr>
<td>B. Stages of Production</td>
<td>10</td>
</tr>
<tr>
<td>1. Mining: Obtaining Raw Silicon Dioxide</td>
<td>10</td>
</tr>
<tr>
<td>2. Materials Preparation: Reduction of Silica</td>
<td>12</td>
</tr>
<tr>
<td>a. Intermediate compound</td>
<td>13</td>
</tr>
<tr>
<td>b. Zone refining</td>
<td>15</td>
</tr>
<tr>
<td>c. Reactive gas blow-through melt purification</td>
<td>15</td>
</tr>
<tr>
<td>a. Ingot technologies</td>
<td>16</td>
</tr>
<tr>
<td>i. Czochralski</td>
<td>16</td>
</tr>
<tr>
<td>ii. Float zone refining</td>
<td>18</td>
</tr>
<tr>
<td>iii. Heat exchanger</td>
<td>18</td>
</tr>
<tr>
<td>b. Noningot technologies</td>
<td>19</td>
</tr>
<tr>
<td>i. Edge-defined film growth (EFG)</td>
<td>21</td>
</tr>
<tr>
<td>ii. Dendritic web growth</td>
<td>22</td>
</tr>
<tr>
<td>iii. Crystalline silicon sheet</td>
<td>22</td>
</tr>
<tr>
<td>iv. Amorphous</td>
<td>24</td>
</tr>
<tr>
<td>5. Cell Blank Manufacturing: Slicing, Sawing and Cutting</td>
<td>24</td>
</tr>
<tr>
<td>6. Cell Manufacturing: Etching</td>
<td>26</td>
</tr>
<tr>
<td>7. Cell Manufacturing: Junction Formation</td>
<td>26</td>
</tr>
<tr>
<td>a. Diffusion</td>
<td>27</td>
</tr>
<tr>
<td>b. Epitaxial growth</td>
<td>28</td>
</tr>
<tr>
<td>c. Corona discharge</td>
<td>29</td>
</tr>
<tr>
<td>8. Cell Manufacturing: Collector Metallization</td>
<td>29</td>
</tr>
<tr>
<td>9. Cell Manufacturing: Passivation and AR Coating</td>
<td>31</td>
</tr>
</tbody>
</table>
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>10. Module Manufacturing: Interconnection and Placing in Module</td>
<td>32</td>
</tr>
<tr>
<td>11. Module Manufacturing: Encapsulation</td>
<td>33</td>
</tr>
<tr>
<td>III. Cadmium Sulfide Process Technology</td>
<td>37</td>
</tr>
<tr>
<td>A. Overview of Process Technologies</td>
<td>37</td>
</tr>
<tr>
<td>B. Stages of Production</td>
<td>37</td>
</tr>
<tr>
<td>1. Raw Material</td>
<td>37</td>
</tr>
<tr>
<td>2. Encapsulation</td>
<td>38</td>
</tr>
<tr>
<td>3. CdS Active Layer</td>
<td>39</td>
</tr>
<tr>
<td>4. Junction Formation</td>
<td>40</td>
</tr>
<tr>
<td>5. Metallization</td>
<td>40</td>
</tr>
<tr>
<td>IV. Other Technologies</td>
<td>42</td>
</tr>
<tr>
<td>REFERENCES</td>
<td>45</td>
</tr>
</tbody>
</table>
INTRODUCTION

The development of new energy technologies is an important public policy measure which can be undertaken to aid in the resolution of future energy problems. In our system of economic organization, the selection of technical options and their final development and ultimate entrance into the economic structure of the nation will be managed by private industry. The performance of these industries in this task is thus of paramount public concern. However, our understanding of the process of technological development in industry is very incomplete, leaving efforts to facilitate that process without sound guidance. In the U.S. economy, further confusion arises from the complex role the federal government plays in affecting private industrial behavior.

The main effort of this project (Linden, Bottaro, et. al., "The Solar Photovoltaics Industry: The Status and Evolution of the Technology and the Institutions") resulted in a preliminary effort to understand the technology development process. This paper presents the technical options which are available for development of photovoltaics. Designed to support the principal effort, it aims to provide the technical background necessary to make intelligent analysis of the complex issues pertaining to the commercialization of new energy technologies raised in the main report. It begins by discussing the rudiments of photovoltaic design and operation. Section II then discusses the dominant technology, silicon, and the options for technological change in silicon process technology. Section III does likewise for cadmium sulfide technologies. Finally, section IV briefly surveys other technologies.
I. PRINCIPLES OF PHOTOVOLTAIC GENERATION

To appreciate the significance of various photovoltaic process steps, and of possible changes in such steps, a basic understanding of the operation of PVs and of some elementary design considerations is necessary. The remainder of this section reviews principles of photovoltaic generation briefly\(^1\) and sets forth several factors which affect the cost and output of photovoltaics.

A. RUDIMENTS OF PHOTOVOLTAIC ELECTRIC GENERATION

Photovoltaics operate by converting sunlight to electricity. This conversion occurs when valence electrons in the photovoltaic cell absorb light (photons) of sufficiently high energy to cause the electrons (and the "holes" they leave) to become mobile. Ordinarily such motion is random; however, if, as in the case of photovoltaics, the absorbing material contains a semiconductor with a p-n junction, the motion of the electrons can be made to follow one direction more than others, thus producing an electric current.

Usually semiconductors are made with crystalline silicon. Silicon forms a tetrahedral crystal structure due to its tetravalent nature. One can diffuse into this structure a small number of atoms which are not tetravalent. If the dopant has five (or more) valence electrons, the doped structure has an excess of mobile electrons and is known as an n-type semiconductor; if the dopant has three (or

\(^1\)For a more thorough but still relatively nontechnical exposition of these principles, see Chalmers, Adler, and Meinel.
fewer) valence electrons, the doped structure has an excess of holes and is known as a p-type conductor. Joining a p-type semiconductor and an n-type semiconductor will, by statistical diffusion in opposite directions of holes and electrons, produce a static electric field which will make holes and electrons move in opposite directions. If a circuit connects the portions of the two semiconductors away from the junction, current will thus flow when the joined semiconductor absorbs light.

One may also use crystalline materials other than silicon; these materials produce current similarly. Also, the requirement of crystallinity may be relaxed somewhat; the photovoltaic cell need not be a single crystal (monocrystalline), but may be composed of many smaller crystals. Such a cell is termed polycrystalline or semicrystalline. The problem with such material is that the grain boundaries between crystals tend to induce recombination of electrons and holes (i.e., an electron filling a hole before the built-in electric field can separate them) before they reach the external circuit. However, if the crystals are large enough, many carriers will reach the external circuit before hitting a grain boundary. For some materials even an amorphous structure (noncrystalline or "disordered") will suffice (see Adler for a detailed explanation).

B. BASIC DESIGN CONSIDERATIONS

The aim of photovoltaic design is to produce maximum output per unit cost, or conversely to minimize the cost per unit output. To the extent that use of space matters in a particular application, maximizing output per unit area may also be a design aim. However, satisfying this aim
will reduce cost only so long as the space costs saved by reducing the space required for a given output exceed the increase in the sum of the manufacturing and installation costs incurred in order to reduce the space required for the given output. This implies that the problem is really one of minimizing total costs per unit output, where total costs include the space costs associated with a particular application. Therefore, to understand the significance of any potential design improvement one must understand how the improvement is intended to reduce the costs of a given module while increasing its output or at worst decreasing it less than proportionately.

The rest of this section will address what design factors affect a photovoltaic module's output through time.

1. Factors Affecting Cell Efficiency

Many potential design improvements affect the efficiency of the cell, i.e., the percentage of light energy reaching the cell which the cell converts to electricity. Higher cell efficiency implies that less surface area of cell is needed to produce a given output, and in applications where area-related costs are positive, higher efficiency may be desirable even if other costs per unit output increase. However, some potential design improvements would lower efficiency somewhat while reducing a given module's costs more than proportionately.

The type of material used in the cell affects the cell's efficiency. Different materials have differing maximum theoretical efficiencies. For example, gallium arsenide (GaAs) and cadmium telluride (CdTe) are among the highest (over 24%) and are very close to the maximum
theoretical efficiency of an ideal cell (Chalmers, p. 41). Silicon is slightly lower at 22% (id.), and cadmium sulfide (CdS) lower still at 16% (OTA, p. XIII-149). However, lower unit cost processing techniques for the less efficient cells often result in lower cost per unit output than for, say, GaAs. Also, in operation, some materials may approach their theoretical efficiencies much more closely than others do.

Also affecting the efficiency is the structure of the semiconductor used in the cell. Pure crystalline structures with an optimal amount of dopant will produce the highest operating efficiencies. Lower purity crystals will have lower efficiencies, but not necessarily lower cost per unit output. The same holds true for a less crystalline (polycrystalline or semicrystalline) and possibly for an amorphous structure as well.

The thinness of the cell may also affect efficiency, ceteris paribus. While too thin a cell will reduce efficiency, too thick a cell adds nothing but cost and will reduce efficiency. In practice, cells often exceed the necessary thickness, thereby increasing costs. In such situations techniques which reduce the amount of crystalline material needed to make cells would reduce costs without lowering efficiency.

A fourth factor affecting cell efficiency is the amount of light reaching the cell. Some light is reflected by the cell, instead of being absorbed by the cell. The texture of the cell's surface affects the cell's reflectivity; a polished cell will reflect more light than a rough cell. Also, a coating on the cell of a proper thickness will reduce the reflected light by inducing destructive interference between light reflected from the coating and light reflected from the cell surface.

Another source of reflection is the metal collector on the cell's surface. The collector serves to gather the electrons (or holes) which
travel to the cell's surface and conducts them to the circuit. As a good conductor, metal reflects electromagnetic radiation, including light. Therefore, the greater the cell area covered by metal, the more light is reflected. However, with thinner and sparser metal "fingers" forming the collector, series resistance increases (increasing power loss and heating the cell) and fewer electrons (or holes) make it to the collectors, reducing the power output.

The cell's temperature also affects efficiency. Different materials respond differently to temperatures higher than room temperature; some materials decline in efficiency much faster with temperature increases than do others. Applications using concentrators without cooling systems will be affected most by a particular material's ability to remain relatively efficient at higher temperatures.

2. Factors Affecting Module Efficiency

The manner in which the photovoltaic module manufacturer makes the module also affects the output. Here, however, efficiency is defined as the percentage of radiant energy reaching the module which the module converts to electricity.

A module generally comprises several cells connected in series. The series connection of cells serves to increase the voltage to the desired level (from the approximately 1/2 volt potential in each cell).

To use each cell in the series string to capacity, the current output of all the cells must be equal; if not, the cell with the lowest current will limit the string's current, thereby wasting the additional current output of the string's other cells.
The "packing factor" also affects module efficiency. It is the ratio of the area of the cells in the module to the module's entire area. The lower the packing factor, the greater the amount of space one needs per unit output. Also, with a lower packing factor more substrate and arraying structure are required per unit output.

3. Factors Affecting Lifetime

As the lifetime of a photovoltaic module increases, its value (as compared to alternatives for the application in question) increases, discounted by the user's discount rate. Given a particular module design, added lifetime implies added cost. Whether the user considers the extra cost acceptable depends upon the use to which the user puts the photovoltaic module.

The encapsulant and method of seal largely determine the photovoltaic module's lifetime. Failure of the encapsulant generally causes the module to fail prematurely, either by moisture destroying the cells (more likely with some semiconductors than with others) or by exposing them to physical destruction. Different encapsulants and seals perform differently in operation, some withstanding the elements at the user's site more than others.

Also, different encapsulants absorb different amounts of dirt (which blocks the sunlight and creates the need for maintenance and replacement of the module) and are suited for different user environments.
II. SILICON PROCESS TECHNOLOGIES

A. OVERVIEW OF STAGES OF PRODUCTION

Table 1 presents the stages of production for monocrystalline silicon cell processes. The eleven stages are grouped into five categories; within each category the stages are functionally related.

Figure 1 presents in diagram form current processes and related alternatives. (Because the figure folds out, we present it at the end of the section (pp. 35-36) to facilitate referring from text to figure and back.) In the figure, solid lines connect currently used processes while dotted lines connect processes which are proposed or under development. Vertical lines meeting a box should be construed as passing behind the box; they indicate that the box they meet vertically is not an intermediate step. The vertical gray lines divide the production processes into the categories listed in Table 1.

The remainder of Section II presents the details of the silicon cell manufacturing processes shown in Figure 1.

B. STAGES OF PRODUCTION

1. Mining: Obtaining Raw Silicon Dioxide

Silicon dioxide (silica) is the major constituent of most sands. It is also found in a crystalline (and hence pure) form, quartz, in

---

2Since the figure is intended to show current processes and potential improvements thereon, radically different alternatives having little similarity with current processes such as those based on amorphous semiconductors, could not be included without making the figure unreadable and hence are omitted from the figure.
Table 1
MONOCRYSTALLINE SILICON CELL PROCESSES AND RELATED TECHNOLOGY

A. Mining
   1. Obtaining raw silicon dioxide

B. Materials Preparation
   2. Reduction of silica
   3. Further purification

C. Cell Blank Manufacturing
   4. Crystal growing
   5. Slicing, sawing, and cutting

D. Cell Manufacturing
   6. Etching
   7. Junction formation
   8. Collector metallization
   9. Pa-sivation and AR coating

E. Module Manufacturing
   10. Interconnection and placing in module
   11. Encapsulation
quartzite rock. Silicon is second only to oxygen in abundance in the earth's crust, and physical scarcity is not a problem. Raw SiO$_2$ is far cheaper than the purified silicon used for semiconductors and solar cells. The 1972 price for sand was less than $0.005/kg (Curin, et al., p. 368) compared to $65/kg for semiconductor-grade silicon (see subsection 3 below). Sand is used mostly for construction.

While both sand and quartzite are now used for silicon production, quartzite might be mined specifically for silicon cells if they were produced in sufficient quantities. Large deposits of pure quartzite are common, costing pennies per pound. The steel industry uses most of the purified silicon dioxide (see subsection 2 below); because it is indifferent to having some mineral impurities, it gains no advantage by starting from purer quartzite. The small quantities demanded by the semiconductor industry apparently do not justify mining pure quartzite either, even though some costs arising from purification might be reduced if quartzite were the starting material. Also, certain impurities (such as boron) which are now removed during purification could remain as dopants (Mlavsky, 1977).

2. Materials Preparation: Reduction of Silica

The silica is heated in a furnace with coke (carbon) to remove the oxygen. In the submerged arc reduction process, used by Dow Corning and others sand and coke are dumped over an electric arc. This leaves silicon of 96-98% purity, sufficient for many metallurgical uses. The metallurgical grade cost about $0.65/kg in 1975 (Merrigan, p. 56). Metallurgical silicon's price will depend somewhat on coal and coke prices because carbon is oxidized in silica reduction.
Only a small fraction (.05% in the 1960s) of the 96-100% pure metallurgical silicon is used for semiconductors (Kirk-Othmer, 18:119). Most of it is used for making steel, hence the term "metallurgical" silicon (Currin, et al., p. 368). Total production of this grade in 1974 amounted to 141,000 short tons (Minerals Yearbook, 1974).

Other silica reduction methods exist, such as those using aluminum as a reducing agent, but are rare in use (Kirk-Othmer, 18:120).

The reduction process has the potential for producing a lower purity (and hence lower resulting cell efficiency) "solar grade" silicon. Dow Corning believes that $10/kg can be attained by a modification of its submerged arc reduction process (INFORM, p. 109). If so, most of the purification process can be integrated with the reduction process, eliminating the need for the chlorinated silane steps (see Subsection 3.a below) currently being used. In Figure 1, the flow would be from the submerged arc coke reduction step directly to zone refining (and probably production of a single crystal), making the next stage fall under the cell blank manufacturing category.

3. Materials Preparation: Further Purification

As can be seen from Figure 1, after silica reduction several pathways exist for purifying the silicon further. Only one, using chlorinated silanes, is in present use, although others are possible.

a. Intermediate compound

Methods using an intermediate compound for further silicon purification work by reacting the metallurgical grade silicon with
another compound, producing an intermediate compound easily separable from the impurities remaining in the metallurgical grade silicon. Trichlorosilane \((\text{HSiCl}_3)\) is the most commonly used, while silicon tetrachloride \((\text{SiCl}_4)\) and silane \((\text{SiH}_4)\) may also be used.

The chlorinated silanes \((\text{SiCl}_4 \text{ and HSiCl}_3)\) are made by reacting silicon carbide \((\text{SiC})\) byproducts with chlorine gas to make silicon tetrachloride and silicon (or copper silicon powder) with hydrogen chloride gas \((\text{HCl})\) to make trichlorosilane. Silicon in this chlorinated form is generally used in the further purification processes required by the semiconductor trade. Boron and phosphorus are removed from these compounds by fractional distillation and absorption. These purified \((99.999\%)\) chlorides are reduced by heating with purified hydrogen in quartz containers, leaving \(99.999\%\) silicon behind (Currin, et al., p. 368). Silicon of this purity is referred to as semiconductor-grade silicon. The 1968 price of \(\text{SiCl}_4\) was about $0.33/kg for the high purity used by the semiconductor industry. Semiconductor purity \(\text{HSiCl}_3\) cost about $6/kg in 1972 (Currin et al., p. 368).

Silane \((\text{SiH}_4)\) gas may also be used as an intermediate compound, but it is costly (Chu, 1975, p. 303) and difficult to handle. It decomposes when heated, leaving pure Si behind. The methods using \(\text{HSiCl}_3\) are currently favored for solar cell production (Meinel, p. 533) (Currin, et al.). \(\text{HSiCl}_3\) is primarily used to make silicones in the chemical industry, while the pure crystallized silicon is mainly used for semiconductors (Currin, et al., p. 368). Semiconductor-grade silicon produced this way costs $65-70/kg in 1976 (INFORM) (Chalmers) (Energy Daily, July 11, 1977).
b. Zone refining

An alternative to the intermediate compound method is zone refining. When a purity of at least 99.999% has been attained, zone refining may be used to attain further impurity reductions (Angrist, p. 119). Because of liquid silicon's well known propensity to dissolve its containers, the floating zone method, a slightly modified form of zone refining, is used. Here a silicon rod is held vertically at both ends while a small segment is melted. The zone subjected to melting is gradually moved downwards, sweeping away the impurities. This method has the added advantage of producing single crystals (see subsection 4 below). Repeated slow passes are necessary to attain semiconductor purity through zone refining.

Leaching can improve the purity of metallurgical grade silicon to better than 99.7% (Meinel, p. 533), not good enough for the semiconductor industry. Leaching might be used in conjunction with some other physical purification process such as zone refining (as opposed to the chemical intermediate compound processes) to attempt bypassing the trichlorosilane method, thus resulting in a solar grade of silicon. See Figure 1.

c. Reactive gas blow-through melt purification

In this method a gas such as chlorine or oxygen is bubbled into molten metallurgical grade silicon, reacting with the impurities in the silicon (and to some extent with the silicon itself). These reacted impurities generally have lower boiling points than silicon and will boil out of the melt. Zone refining of some sort may then follow, increasing the purity further. To date, reactive gas blow-through melt purification
has reduced the impurities in metallurgical grade silicon by 46-96%.


The greatest range of technological options occurs in the crystal-growing stage. The options can be classified into two categories, ingot and noningot. Different cell manufacturing process automation possibilities arise depending upon the type of crystal-growing options considered; these possibilities are discussed further in subsection b below.

The lower three boxes in the left-hand side of Figure 1's section entitled "CELL BLANK MANUFACTURING" represent ingot technologies; the next three up represent noningot technologies. (The reader is reminded that vertical lines meeting a box should be construed as passing behind the box and not into it.)

a. Ingot technologies

All ingot technologies produce a monocrystalline ingot of various diameters. Only one technology, the Czochralski melt-and-pull, is currently in use.

i. Czochralski

In the Czochralski method a seed crystal of silicon is pulled slowly (less than 4 in/hr) from a quartz crucible containing liquid silicon at 1450°C. The crystal is rotated as it is withdrawn and solidifies into a cylindrical ingot up to several feet long. While diameters of six inches have been achieved (Kirk-Othmer 18:122),
three-inch diameters are more common (Electronics, 6/76) (Chalmers). The ingots are only about 99.999% pure (Currin, et al., p. 368) due to contamination from the crucible. Also, the crucible usually breaks when the uncrystallized silicon remaining in the crucible after the ingot is made hardens, adding about $20 per kg to an ingot's cost (M. Wolf, 1975, pp. 307, 314). Starting from 70 lbs of pure silicon, a 50 lb perfect Czochralski crystal results. After trimming the useless ends off, a 40 lb cylinder remains (Mlavsky, 1977). The entire process results in ingots costing $250/kg (Currin, et al., p. 364).

The Czochralski process was adopted for use in the transistor and integrated circuit industries, where the ultimate product contains a chip of silicon about a millimeter or two across. Czochralski ingots are used primarily for producing small signal semiconductors. The crystal's cross-sectional shape and area would then not be important, except as they would affect manufacturing capacity.

The largest silicon cells commercially available, used by Solarex and Solar Power Corp. (Addiss), have four-inch diameters. Motorola uses three-inch cells (Motorola). Both Solar Power Corp. and Solarex also use three-inch cell in modules available for lower current applications. While most present (1977) solar cell manufacturers buy the sliced polished wafers, Spectrolab and OCLI grow their own crystal ingots because they, as space cell manufacturers, must meet certain trace-ability requirements for product quality (Yerkes) (Spectrolab) (OCLI Ann. Rep., 1976). Sensor Technology buys the crystal ingots and does its own slicing. Solarex buys both ingots and wafers, doing some slicing in-house (Clifford).
ii. Float zone refining

Another method of crystal fabrication is essentially float zone refining (see subsection 3.b above). No contacting surfaces are available to contaminate the melt, and impurities are swept to one end (zone refining), producing very pure crystals. Maximum diameter for this method was only 2 inches in 1968 (Mlavsky, 1977). Note that purification and crystallization occur simultaneously; hence in Figure 1 the box for float zone refining falls under two categories, materials preparation and cell blank manufacturing.

iii. Heat exchanger

Originally developed and already in commercial production for sapphire crystals, the heat exchanger method is now at the experimental stage for silicon. In this method, developed by Crystal Systems Inc., a seed crystal is centered on the bottom of a crucible filled with melted silicon. A precisely controlled heat exchanger cools the crucible from the center outward. The silicon solidifies from the center outward in a solid crystal whose lattice is determined by that of the original seed crystal. An important advantage claimed for this system (Electronics June 24, 1976) is that low-purity silicon may be used in the melt, since zone refining apparently occurs at the slowly growing solid/liquid interface, pushing impurities off to the side. Other advantages which reduce subsequent handling and processing costs are larger diameter crystals than Czochralski crystals (six inches expected routinely) and monocrystals bearing the shape of the crucible. Presumably, rectangular ingots could be grown in rectangular crucibles, thereby permitting high packing factors.
Crystal Systems' approach improves upon the older Chalmer method, where liquid silicon slowly cools from one end of the crucible. Chalmers' method and the related Bridgman method (in which the solidification proceeds up a vertical tube) share the drawbacks of vessel contamination and vessel deformation (because of the temperature differential).

b. Noningot technologies

The noningot technologies comprise several largely unrelated process possibilities. Two technologies, Mobil Tyco's edge-defined film growth (EFG) method and the dendritic web growth method, produce crystalline silicon in thin ribbons and hence are termed ribbon technologies. Two other methods which produce sheet silicon are the cast silicon method and peeled film technology. Lastly, one possible method still primarily in the research phase uses amorphous semiconductors.

Noningot technologies, particularly the ribbon technologies, offer opportunities for departure from the current batch processes for cell manufacture (see subsections 6 through 9 below). Currently, each stage in a batch process requires stopping the product flow and inserting or removing cells, carrying them from one machine to the next by hand. However, noningot technologies might be able to use a continuous belt process in which the unbroken ribbon or sheet winds from melt through etching baths, diffusion furnace tunnels, and silk screening without pause. Similarly, a substrate ribbon or rolled sheet could be continuously coated with the active semiconductor and similarly treated. In both cases, slicing would follow cell manufacturing, changing the
order in which the stages now progress under batch processing. Figure 1 depicts this by showing that noningot technologies (unlike ingot technologies) have the option of proceeding to the continuous process box in the cell manufacturing section, with slicing or scribing following in the module manufacturing section. Wafers and sheets could of course be processed on conveyor belts to achieve some of the same continuous processing economies (e.g., continuous use of diffusion process heat, no intermittent power cycling wear, lower labor costs) but with less ease than inherently continuous processes such as ribbon growth.

Furthermore, noningot technologies would practically eliminate the waste of nearly half the ingot due to sawing (see subsection 5 below) even if continuous processes are not used.

Most noningot technologies use polycrystalline or semicrystalline silicon which, while lower in efficiency than monocrystalline silicon, costs less. Cost per unit output might be lowered further if some low-cost method of improving the crystalline structure were interposed between the crystallization stage and subsequent stages. The uppermost box in the left-hand side of Figure 1's "CELL BLANK MANUFACTURING" section ("FLOAT ZONE RECRYSTALLIZATION") represents this optional recrystallization stage between three of the noningot technologies (represented by two boxes labeled "EFG MELT & PULL" and "CAST SHEET OR PEELED FILM Si CRYSTALLIZATION," and referred to at the top of Figure 1 as "POLYCRYSTALLINE Si RIBBON, SHEET") and further processing. The remaining noningot technology, dendritic web, would not benefit from recrystallization since it apparently produces monocrystalline silicon (see subsection ii below).
i. Edge-defined film growth (EFG)

In this method molten silicon is drawn through a die with an opening of approximately 2-5 cm in width and 0.1 cm in thickness. Initially the molten silicon rises through the die due to capillary action and then is drawn. Because the growing EFG ribbon is thermally isolated from the melt (Ravi, et al., p. 280), the crucible can be refilled without disturbing the growing crystal, thus eliminating broken crucibles. The silicon ribbon produced is not truly monocrystalline silicon but an intermediate form having many large crystals (Mlavsky, 1977). Impurities from the die, however, rather than recombination at grain boundaries, cause lower efficiency than that of Czochralski silicon (Id.). Apparently EFG proceeds too fast for zone refining to occur during crystal solidification (Id.). Efficiencies reach 8-9%, and 12% has been achieved in the lab.

Tubular cells through which coolant may be circulated have also been made by the EFG process (Mlavsky, 1977). These are most useful for locating at the focus with a line-focusing concentrator. Also, one may trim the rounded corners of oval tubular cells, thus producing cleaner edges, and improving cell performance (Mobil-Tyco, Patent No. 4,036,666, 1977).

To reduce costs, ribbon wider than the present one-inch and growth rates faster than the present two and one-half inches/second must be achieved (id.). Wider material will probably require an annealing (or recrystallization) step after the initial crystallization. Widths up to three inches have been achieved under lab conditions (Mlavsky, 1977). The prospects for mass production include multiple-die machines producing
many ribbons simultaneously but which one person could control, and use of optical electronic sensors to inspect the ribbon for serious faults as it leaves the die.

Silicon ribbon production may also become cheaper if the orbiting space factory becomes commercially practical, thus permitting ribbon growing without physical contact by any contaminating materials.

ii. Dendritic web growth

This method employs two coplanar crystalline silicon dendrites which are drawn from the silicon metal. A web freezes between the dendrites as they are pulled. The resultant web, 0.01 to 0.015 inches thick, breaks easily (Angrist, p. 23). Performance comparable to Czochralski silicon is claimed (Backus, p. 299) (Seidensticker) apparently because the web is monocrystalline and nothing touches it but the dendrites as it grows. The subject of extensive research in the 1960s, dendritic web methods never became economical (Currin, et al., p. 365).

iii. Crystalline silicon sheet

Several largely experimental techniques fall under this heading. Figure 1 shows two of them, cast silicon and peeled film technology, because activity with these seems less conjectural.

Among production techniques for thin film photovoltaics are chemical vapor deposition (CVD), dipcoating, sputtering, and heteroepitaxial growth. One chemical vapor deposition technique is to decompose silane gas onto a substrate leaving a layer of pure polycrystalline silicon
This method suffers from the expense of silane. Trichlorosilane (HSiCl$_3$) can also be used for CVD with purified hydrogen as a reducing agent on graphite and bulk polysilicon substrates (Chu, 1975, pp. 303-305). Wolf (1975, p. 309) proposes to use CVD with SiF$_2$ (silicon difluoride) on polycrystalline silicon. Honeywell's Advanced Development Laboratories are experimenting with dipcoating carbonized Mullite with molten silicon. As the silicon hardens, silicon carbide (SiC) forms, bonding the polycrystalline silicon layer to the Mullite.

Wacker-Chemitronic in West Germany is experimenting with polycrystalline silicon sheet made by carefully controlling the freezing rate of molten silicon in hot graphite molds (Yerkes). Although the resulting sheet is polycrystalline, the grains are large enough to give a conversion efficiency of up to 10% (id.). If grain boundaries can be constrained to run perpendicular to the cell surface, presumably even higher efficiencies could be reached. Impurities from the mold are apparently blocked by a silicon "skin" that forms between the graphite and silicon melt. Solarex also has cast sheet cells and reports 10% efficiency with solar cells have one millimeter average grain sizes (Lindmayer, 1976); the technique may be quite similar to Wacker-Chemitronic's.

Another crystalline sheet concept is peeled film technology (PFT). In PFT, an epitaxial layer of silicon is grown onto a crystal layer of different material, then "peeled" off intact by means of a vacuum chuck or an attached rider slab after melting the intermediate crystal layer (Milnes, 1975). Recrystallization, using float zone refining (see 3.b above), can be used with polycrystalline sheet to fuse adjacent grains
into larger crystallites (Wolf, 1975, p. 309). Narrow molten zones will be necessary because of the sheets' meager thickness, and electron beam heating may be required for this (id.).

iv. Amorphous

Certain amorphous materials can behave as semiconductors (Adler). Although the amorphous semiconductor effect, known as "ovonics," has been known since 1958, only with recent theoretical advances have electronic applications appeared (id.). Amorphous silicon also has a shallower absorption depth than crystalline silicon (1 micron vs 100 microns), which, together with its aperiodic structure, suit it well for thin film applications.

Researchers at RCA are attempting to use glow discharge to deposit the amorphous silicon. Instead of doping, a Schottky junction is formed (Bereny, p. 150). Energy Conversion Devices recently claimed to have achieved "modification" (similar to doping in crystalline semiconductors) by mixing different materials to make amorphous semiconductors (New York Times, July 6, 1977).

Amorphous semiconductors are not depicted in Figure 1 because present information on process technologies is lacking and because the process may differ radically from the crystalline silicon model which Figure 1 assumes, thereby making its meshing with the rest of the figure confusing.

5. Cell Blank Manufacturing: Slicing, Sawing, and Cutting

To prepare thin, flat wafers for the semiconductor industry from the cylindrical ingot, the ingot is repeatedly sliced with an inside-
diameter) saw blade. This rotary saw has an abrasive-coated cutting blade running along the edge of a large hole in the center. Taking the 40 lb Czochralski ingot mentioned in subsection 4.a.1 above, we find that half of it disappears as sawdust in slicing. These 20 lbs of wafers are at least 12 mils thick, three times the necessary thickness (Mlavsky, 1977). Only about 40 wafers per inch of ingot are obtainable by present techniques.

One possible improvement under investigation is the use of closely spaced diamond-impregnated wires as a multiple saw. The wafer would be only six mils thick (as opposed to 15-16 mils now) (up to 40 mils, Meinel), wasting an additional four mils for cutting. It is hoped eventually to have thousands of such wire "blades" per machine (Electronics, June 1976). Four mils is expected to be the optimum Si thickness for solar absorption (Mlavsky, 1974, p. 7).

Solarex presently employs a Varian multiblade wafer "breadboard" saw employing many parallel blades in reciprocating motion to slice ingots (Clifford).

For outer space applications, where efficient utilization of space is necessary and cost is less of a consideration, the circular cells are scribed, then broken into rectangular or hexagonal shapes for closer packing. OCLI, Solar Systems, and Solarex supply rectangular cell models. Most terrestrial modules simply use the complete circular wafer, saving silicon, but wasting space at the ultimate application site due to spaces between the circular wafers. Intermediate approaches, such as cutting the circular wafer into sextants which permit close packing without wasting silicon, are used for some applications.
Noningot technologies, as mentioned in subsection 4.b above, could use simpler cutting methods less wasteful of the silicon. As Figure 1 shows, for these technologies the slicing or scribing step would most likely occur before the cell manufacturing steps in a batch processing set-up but after in the case of a continuous process.

6. Cell Manufacturing: Etching

In present commercial fabrication of semiconductors, after cell blank manufacturing the wafer is then hand-lapped and polished to remove the roughness left by sawing (Meinel, p. 534; Angrist), then buffed to optical smoothness, and it is in this form that most present solar cell manufacturers obtain their silicon wafers (Yerkes). However, not only is such polishing not required for solar cells but also roughing the cell surface (surface texturizing by etching with acid has been shown to improve absorption significantly and hence improve conversion efficiency). Motorola's cells, for example, are currently supplied in this form (Motorola). Here the photovoltaic industry's needs diverge from those of the semiconductor industry, and the polishing step is not necessary.

7. Cell Manufacturing: Junction Formation

Once the complete single crystal wafer has been prepared, articulating further structure is accomplished by creating one or more different layers on the wafer surface. In the semiconductor industry, highly complicated structures can be formed by repeated layering through photographically etched masks. Such procedures are of limited usefulness
to junction formation in photovoltaics, which typically have only one junction-forming layer.

The junction is formed at the interface of two differently doped crystals with similar crystal lattice dimensions. One side of the junction is the bulk crystal. It is doped just before the crystal-growing process by introducing impurities such as boron (p-doping) or phosphorus (n-doping) into the melt. Extremely minute quantities of these dopants are used. Concentrations range from 5-1,000 parts per billion for transistors and integrated circuits. Formation of the other side of the junction is by either diffusion, epitaxial growth, or possibly corona discharge (see Subsections a, b, and c below).

Adding another junction on the back of the cell can be used to create a back surface field (BSF) which accelerates carriers to the collector, reducing both the time they linger and the chance of recombination. This junction is formed between the substrate semiconductor and a more heavily doped layer of the same type (Electronics, March 18, 1976, p. 48). A typical method of forming these BSFs is to apply aluminum to the back of the cell either by evaporation (Mandelkorn, 1972) or by applying aluminum paste (Ralph), then heating in a diffusion furnace (Id.). The diffusing aluminum atoms will heavily dope the back surface of the cell with "holes" (p+) (Id.). Solarex claims its cells have such a field (Solarex, p. 3). As shown in Figure 1, the BSF step is an optional one, usually preceding normal junction formation.

a. Diffusion

In diffusion, heating the crystal in an atmosphere of the evaporated
dopant (for an n-doping, phosphorus pentoxide; for p-doping, diborane gas or boron nitride gas) allows the dopant to diffuse into the material. Conventional diffusion techniques have been slow, especially when deep layers (and hence long migration distances) are desired and therefore have been largely supplanted by epitaxial growth (see Subsection b below) for most semiconductor purposes. Photovoltaic semiconductors still use diffusion for their junctions, however.

GE has been developing a thermomigration process which speeds diffusion. In thermomigration, a temperature gradient of about 50°C/cm is maintained across the bulk crystal substrate while it is in an 1100°C diffusion oven. The dopant has earlier been deposited as a solid on the crystal surface and in the oven migrates toward the hotter surface. Diffusion times of ordinarily a week have been reduced to a few minutes (Energy Daily, June 1977). Also, the oven temperature is as much as 200°C lower than for a conventional diffusion oven (1300°C), reducing heat degradation of the junctions as they form (id.) Furthermore, much deeper, more sharply defined penetrations are possible, which suggest the feasibility of fabricating such new cells as edge-illuminated vertical multijunction devices. Thermomigration is probably less useful for the conventional topology of solar cells (which have the junction plane parallel to the surface) because they typically have shallower junctions (0.1 to 1 micron, Angrist, p. 280) than other semiconductors (170 microns, Energy Daily, June 1977).

b. Epitaxial growth

Epitaxial growth refers to the growing onto a substrate crystal material of a differently doped form of that material or a different
material, thus forming a p-n junction. The substrate crystal is cut to match the growing crystal's orientation and dimensions. Growth may be accomplished from either the liquid or vapor. Of the two, vapor phase epitaxy is more common. It can be done by direct evaporation or chemical reactions similar to those used to obtain pure silicon from \( \text{HSiCl}_3 \) (trichlorosilane) or \( \text{SiCl}_4 \) (silicon tetrachloride), thermal decomposition of \( \text{SiH}_4 \) (silane), or hydrogen reduction of \( \text{SiCl}_4 \) or \( \text{HSiCl}_3 \) (Kirk-Othmer, 18:124). The dopant (e.g., diborane, phosphine, boron triboride) is added in gaseous form to the reducing hydrogen gas. RCA is exploring the use of epitaxially grown junctions in silicon solar cells (Kressel, et al.). It claims superior performance for solar cells made of EFG ribbon (id., p. 1). The higher impurity and crystal fault concentrations in EFG ribbon apparently interferes with conventional diffusion junction formation (id.).

c. Corona discharge

The corona discharge method operates by using a gaseous electrical discharge of dopant compound (such as \( \text{BF}_3 \)) to implant the dopant into the semiconductor's surface. It has the advantage of producing shallow diffusion (and hence a shallow junction) which is of particularly high value for polycrystalline cells, since dopant atoms tend to diffuse along grain boundaries to the back contact, lowering efficiency.

8. Cell Manufacturing: Collector Metallization

Metallization is done now by photographically etching away portions of a vapor-deposited aluminum coating (photolithography), leaving the
familiar fine ladder or grid pattern. This process was developed for the integrated circuit industry where microscopic precision is necessary. Aluminum is normally used for metallization because it reduces any oxides formed on the silicon surface, thus bonding well to the silicon, and because aluminum "does not contaminate the silicon" (Kirk-Othmer, 17:880). Other presently used methods include evaporation of chromium or titanium through a mask with silver, gold, and nickel layers following (Angrist, p. 230). The transistor industry uses reaction of the silicon with sputtered platinum vapor, forming a platinum silicide metallization layer when heated to 700°C in an inert atmosphere. Motorola's cells use palladium silicide coated with nickel for solderability (Motorola).

A cheaper metal deposition technique, silk screen printing promises to reduce costs here significantly. Silk screening of thick films (of silver paste?) is used by Solar Technology at a cost of 15¢ for a three-inch diameter wafer or about $300/kW peak (Yerkes). Spectrolab currently screenprints silver onto their cells but is experimenting with silk screening and less expensive metals such as aluminum, copper, and nickel (Solar Energy Intelligence Report, June 13, 1977). While some other manufacturers refrain from disclosing their production processes, it may be assumed that screen printing is either in use or soon to be adopted by all of the major terrestrial solar cell makers for metallization. Only for concentrations beyond 50 suns is the use of fine-line (i.e., 13 to 254 micron line widths) photolithography (line widths down to about two microns are possible with ultraviolet light (Electronics, May 12, 1977, p. 91)) or mask evaporation economically justifiable (Office of Technology Assessment, p. 167). Photolithography
"adds" $500 per peak kilowatt of cell (Id.). Typical "ultrafine-line screen printing" can produce line widths down to 50 to 70 microns (MFP), although such fine lines are not used in present nonconcentrating commercial arrays.

Collector-related losses can amount to 10% of the total power output, an especially serious concern for concentrator cells in which large current fluxes create large voltage drops (hence, power losses) across the cell. Spectrolab has licensed Comsat's "violet cell" which, among other improvements, uses more numerous, but thinner, collector fingers. It also has a heavily doped back plane which improves conductivity (i.e., lowers resistance losses in the cell) (Office of Technology Assessment). Researchers at the University of Madrid have reported good results with heavy doping on the top surface to increase conductivity under the metallization (collector) (Energy Daily, June 1977). They report that these heavily doped layers transmit 50% of the incident light in spite of their good conductivity (Id.). American Cyanamid has developed cadmium stannate (Cd$_2$SnO$_4$) transparent optical coatings that serve as both collector and AR coating (see subsection 9 below). These coatings have better conductivity when thicker but have reduced transmission of light to the cell, and the converse is true with thinner coatings (Patent Nos. 3,811,953 and 3,957,029).


The passivation layer, formed on the top of a semiconductor device, prevents chemical reaction of the active material with the air or encapsulant. Silicon oxides are commonly used. Motorola uses silicon nitride (Si$_3$N$_4$) which also serves as the AR coating.
AR coatings are normally applied under vacuum (Ralph, p. 315). Typically they are silicon oxides (which also serve as a passivation layer) evaporated onto the cell surface (Angrist); Solarex uses tantalum oxide (Solarex, p. 3) and Motorola uses silicon nitride. Research on titanium dioxide-silicon dioxide (TiO₂ - SiO₂) AR coating which can be "spun-on" and fired without the need for vacuum equipment or when vacuum step shows promise (Ralph).

10. Module Manufacturing: Interconnection and Placing in Module

Before the cells are connected, they are matched for similar electrical characteristics. Presently a technician checks the electrical characteristics of a large group of cells, arranging each according to the location of points on its characteristic voltage-current (I-V) curve. The most similar clusters of cells go into the same module. At Solar Power Corporation, at least, part of the cell testing is done automatically; a high-speed X-Y plotter produces a complete I-V curve for each cell in about a second. However, the sorting of cells, inspecting of joints, and hooking up to the test probes, are all done manually.

The cells are then connected in series. Some manufacturers use short lengths of screening to connect the cells. Others use solid foil strips to simplify production; use of a flexible copper kapton-lamination "circuit board" has been proposed (Scheel, 1972). Motorola is using such a system in their present modules (Motorola); flexible tabs are to be attached either to the top or underside of the cell. Because the laminate is a printed circuit, various series-parallel combinations are possibly simply by changing the photographic mask.
In integrated circuits where the bonded structures and metallization are much smaller, thermocompression welding of gold wire is often used to make connection to the integrated circuit "chip" (Kirk-Othmer, 17:881). The "beam lead" is more elaborate, having greater strength. It involves several layers of metals upon a platinum silicide metallization pattern (see below). The top layer is gold, which forms a chemically more stable bond with the gold connecting wire than does aluminum metallization.

Parallel gap welding, ultrasonic welding, and thermocompression are also under study. These three were found most promising in a NASA study of many methods and could eventually replace soldering or sintering.

After connection, the series string is placed into a module and soldered or sintered to the module's wiring. To reduce arraying costs, Solar Power Corporation and Spectrolab use modules which embody structural supports for the full array. Solar Power Corp. uses thick cast-plastic with molded bracing and circular depressions for the cells (Adiss) and Spectrolab module substrates are based on aluminum I-beams. These improvements are necessary for present applications of cells on offshore platforms or mountaintops where they would be subject to strong wind forces. For residential rooftop applications, however, the building itself would provide structural support for the array, if the roof were suitably sloped and positioned.

11. Module Manufacturing: Encapsulation

Typical encapsulants presently used are, in order of increasing cost, RTV silicone rubber, glass, and lexan, a hard plastic used in aircraft windows which offers the best protection from harsh environments (Adiss,
1977). RTV or other transparent potting compounds frequently fill the space between the cells and the glass or lexan covers to provide a cushion against shock and to minimize reflection due to the different refractive index of the faceplate and any airspace under it.
Mount Figure 1
Figure 1 (continued)
III. CADMIUM SULFIDE PROCESS TECHNOLOGY

A. OVERVIEW OF PROCESS TECHNOLOGIES

Unlike silicon process technology, no standard process technology for cadmium sulfide (CdS) cells exists. Since cadmium sulfide processes use thin-film polycrystalline material, the processes are more flexible. Hence the various stages of production shown in Table 2.2 do not necessarily proceed sequentially; in fact, the two domestic manufacturers (SES and Photon Power) reverse stages 3 through 5, and stage 2 (encapsulation) occurs throughout the entire manufacturing process.

The remainder of this section presents the stages listed in Table 2.2 in the order listed:

<p>| Table 2.2 |</p>
<table>
<thead>
<tr>
<th>CADMIUM SULFIDE CELL PROCESSES</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Raw material</td>
</tr>
<tr>
<td>2. Encapsulation</td>
</tr>
<tr>
<td>3. CdS active layer</td>
</tr>
<tr>
<td>4. Junction formation</td>
</tr>
<tr>
<td>5. Metallization</td>
</tr>
</tbody>
</table>

B. STAGES OF PRODUCTION

1. Raw Material

Cadmium sulfide is the most common mineral form of cadmium and is known as Greenockite (Kirk-Othmer, 3:885). Like all cadmium ores, it is
found with zinc ores (Id.), and is produced at present only as a by-product of zinc production since cadmium is relatively rare and not found in large enough ore deposits to mine separately (Minerals Yearbook 1975). Production of CdS was 1000 short tons in 1974 (Minerals Yearbook, 1975); CdS is mainly used as a pigment. The technical grade sold for $1.85/lb in 1963; pigment grades are more expensive. SES buys pure CdS in powder form as its starting material while Photon Power starts from pure cadmium (Johnson).

2. Encapsulation

Early experimental CdS cells used simple coatings upon cheap substrates such as metal foil with plastic coatings. If successful, these cells would have been extremely inexpensive. Unfortunately, enough moisture or oxygen permeates the plastic to cause irreversible degradation of the cell. To avoid this, both SES and Photon Power appear to be contemplating glass/metal hermetically sealed encapsulation for their CdS cells.

SES plans to apply an insulated ceramic coating to the bottom of a shallow metal plan. A metallization pattern is next applied, then a segmented active CdS layer. The pan is then filled with an RTV-like gel, to cushion the cell and to match the glass refractive index (thus minimizing reflection), then topped with glass having copper-diffused edges (Johnson). These edges are soldered to the top rim of the metal pan, hermetically sealing and completing the module. This elaborate encasulation accounts for more than one-half the cost of the SES module (Johnson). Photon Power almost reverses this in its planned process: as a hot glass sheet leaves the glass production line floating on a bed of
molten tin, a transparent conductive coating of tin oxide is sprayed on. The active \( \text{Cu}_2S - \text{CdS} \) semiconductor layers are sprayed next. Copper metallization backed by lead "passivation" layers is then sprayed on. Finally, the assembly is backed by sheet aluminum which is then folded over at the edge and sealed to the glass (INFORM, p. 103). In operation, light shines through the glass "substrate" which has now become the "superstrate."

For remote applications in harsh environments, these hermetically sealed encapsulation methods are necessary. Merrigan (pp. 80, 81) proposes a continuous belt-processing plant for making large quantities of inexpensive plastic-based CdS cells. While these cells might degrade after 5 years, their initial low cost may make them economical.

3. CdS Active Layer

Working CdS cells may be made by pressing or sprinkling CdS in powder form into the substrate and then sintering it (Merrigan, p. 67), but vacuum vapor deposition has been more widely used (Id., p. 69) and is being used now by SES (Johnson). SES has recently acquired a 10-ton vacuum deposition machine for large-scale production. It allows semicontinuous processing by means of airlocks that free the system from the requirement of having to pump down to a vacuum from atmospheric pressure whenever a new rack of substrates is inserted. This feature and the larger substrate capacity of the machine will speed production.

Photon Power plans to spray on all its active layers. The CdS layer should be from 5-50 microns thick (Merrigan, p. 69), compared to silicon which must be at least 150 microns thick.
One advantage of the thin-film approach is that many "cells" may be formed simultaneously by depositing active material selectively onto the substrate. SES does this to achieve a series connection of 24-cell "areas" on one substrate module to give an open-circuit voltage of 11 volts and 6 volts at the operating point. A 6-volt module or cell cannot be produced in one step like this with present or near-term silicon technology.

4. Junction Formation

Unlike silicon cells, CdS cells use junctions formed by two different compounds (cadmium sulfide [CdS] and copper sulfide [Cu₂S]) to produce the semiconductor effect. To form the Cu₂S-CdS heterojunction, a thin layer of copper sulfide (Cu₂S) must be formed on the CdS deposited. SES accomplishes this by dipping the coated substrate into a copper salt solution. This chemically converts a thin layer of the CdS to copper sulfide (Johnson). Photon Power plans to spray a .7 micron layer of Cu₂S on the CdS (INFORM, p. 103).

Sputtering or flash evaporation are other possible methods (Merrigan, p. 69). The Cu₂S layer should be less than 3.5 microns thick (Id.).

5. Metallization

Because of the close electrical and chemical similarity between cadmium on the one hand and zinc, indium, and tin, the latter three metals are most often used for the metallization contacting the CdS layer (Merrigan, p. 66). Similarly, copper or gold is best for the Cu₂S
layer (Id.). Photon Power plans to use tin oxide ($SnO_2$) as the CdS metallization, and copper for the $Cu_2S$ side, both sprayed depositions (INFORM, p. 103). SES originally used gold-plated copper for top metallization, but abandoned that due to the cost (Johnson). It now screenprints a copper pattern, then builds up the grid by electrodepositing (in a bath) more copper into it. Vapor deposition through a mask or vapor deposition succeeded by photolithography (to etch the pattern desired) are alternative (but more expensive) processes.
IV. OTHER TECHNOLOGIES

Besides silicon and cadmium sulfide solar cells, many possible configurations of device types and materials exist. Their application to PV energy conversion ranges from purely speculative to early serious development. In theory, either germanium or selenium, elemental semiconductors from Group IVa of the periodic table, will display a photovoltaic effect to some wavelength of electromagnetic radiation. Compound semiconductors can be formed in general from any combination of elements from groups IIIa and Va, e.g., gallium arsenide and indium phosphide, or from combinations from transition metals (Groups IIb down) and Group VIA, e.g., cadmium sulfide, copper sulfide, zinc sulfide.

These materials may be used as homojunctions, in which the junction is formed between differently doped versions of the same material (e.g., conventional silicon cells) or as heterojunctions, e.g., cadmium sulfide/copper sulfide, where the junction field is established without extrinsic doping. Some promising heterojunctions recently fabricated at Bell Laboratories include polycrystalline CdS deposited on monocrystalline copper, indium selenide (5.7% efficiency) and CdS on indium phosphide (12.5% efficiency). Cells may have more than one junction for greater efficiency; photons that fail to match the band-gap energy of the upper junction, may match that of the lower junction, making more efficient use of the available spectrum. These tandem junction cells (also known as multijunction cells) could theoretically reach conversion efficiencies of 40%. Material may be monocrystalline (conventional silicon), "semicrystalline" (large-grain size
polycrystalline, e.g., cast sheet), polycrystalline (e.g., cadmium sulfide), or amorphous.

Junctions need not even be between two semiconductors: junction effects may be displayed at a metal-semiconductor interface. Commercial semiconductor devices presently make use of this Schottky effect, and Schottky experiments for PVs are ongoing. The potential for cost reduction by eliminating doping or a vapor deposition step is great, since the collector metallization would serve also as part of the device. Schottky cells tend to have lower voltage output than conventional semiconductor cells. Metal-insulator-semiconductor (MIS) junctions, in which an oxide layer is built up between the metal and semiconductor in a Schottky device, have higher voltage outputs and are in the experimental stage of development. Amorphous semiconductors have been formed with oxide, sulfide, or selenide glasses and may be applicable to photovoltaic conversion.

The photovoltaic effect will be exhibited under many circumstances, including electrolytic solutions (photogalvanic) and organic materials. These have until now shown insignificant conversion efficiencies.

Gallium arsenide (GaAs) cells have shown the highest efficiencies so far (22% at IBM's Watson Research Center), accomplished with a device consisting of a gallium aluminum arsenide heterojunction atop a gallium arsenide homojunction. GaAlAs/p-GaAs/n-GaAs is structurally a multijunction device, but the photovoltaic effect is predominantly contributed by the GaAs homojunction, with the GaAlAs layer serving mainly to slow surface recombinations. Since the device is monocrystalline, Czochralski methods similar to those described above for
silicon would be used in GaAs production, with the probable addition of a GaAlAs epitaxial growth step. GaAs cells have characteristics well suited for concentrator cells, with high efficiency retained at high temperatures. Since the cell itself is not the primary cost factor in concentrator arrays, the high cost of GaAs may not be a strong disadvantage.
REFERENCES


ANGRIST, Stanley W., Direct Energy Conversion, 1976, Allyn & Bacon.


CLIFFORD, A., Meeting at Solarex, Rockville, MD with Joseph Lindmayer, Pres., and Anthony Clifford, Asst. to the Pres., 8/77.


INFORM - Herman, S.W. and Cannon, J.S. Energy Futures, INFORM, Inc., N.Y. 1976. Ballinger Publ. Co., Cambridge, MA. Note: Page numbers are different for the Ballinger and (earlier) INFORM Editions, and are unfortunately mixed in this report. Usually, however, the source may be found from the context or by checking the other version.


MERRRIGAN, Joseph A., Sunlight to Electricity, 1975, MIT Press.


MLAVSKY, A., Seminar at MIT Faculty Club, June 30, 1977, sponsored by NESEA.


(OTA-PV) Office of Technology Assessment, U.S. Congress, Ch. XIII, Section 3, "Photovoltaic Power", unless otherwise indicated.


SCHEEL, H., IEEE-PV-72, pp. 201--205.

SOLAREX - Solarex product brochure 6100-5-77, 1977, Solarex Corp.

SPECTROLAB - Product literature.


YERKES, Bill, Founder of Spectrolab, Founder and President of Solar Technology; personal communication, July, 1977.