

Design of High Quality Factor Spiral Inductors in RF MCM-D

by

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Abstract

This thesis studies the design and fabrication of spiral inductors for use in Radio Frequency (RF) applications. A design methodology is developed to search an inductor design space efficiently using existing simulation software. The methodology allows designers to specify a desired inductance, total area, and frequency of operation instead of the geometrical parameters required by most design software. An implementation of the methodology that finds devices with optimal quality factor at a given frequency is presented. Several inductor designs are generated using this implementation, and the devices are fabricated in the Draper Laboratory, Inc. Multichip Module-Deposited (MCM-D) process. Simulated characteristics of the devices are verified using experimental measurements, and deviations from predicted performance are discussed.

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Publication of this thesis does not constitute approval by Draper of the findings or conclusions contained herein. It is published for the exchange and stimulation of ideas.

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Chapter 1

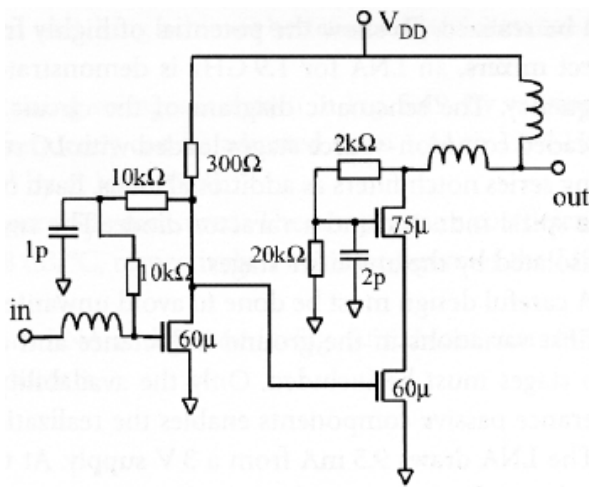
Introduction

1.1 Motivation

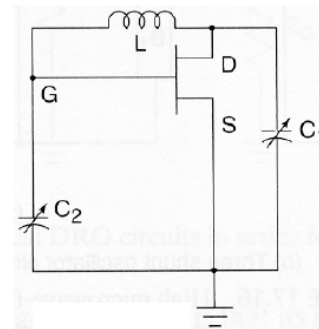
Inductors are an essential part of many Radio Frequency (RF) systems. Their use is particularly common among both wireless and wired communication applications. With the recent explosion of portable consumer electronics relying on wireless communications, however, the size and performance of inductors has become an increasingly large factor of the overall size and performance limitations for many systems. Inductors have simply not been able to keep up with the pace of continual miniaturization and improvements in active devices (transistors) and with the extraction of additional performance from existing communication channels. The compact integration and packaging of inductors with surrounding circuitry has become a priority for many process engineers. Along with all the difficulties of fabricating small inductors comes the formidable challenge of designing them to electrical specifications. This thesis focuses on developing a solution for both the design and fabrication of integrated inductors.

Inductors have long been a critical passive circuit element used in power conversion, sensor, oscillation, and filtering applications at low and intermediate frequencies. With the growing trend of designing low-power, high-frequency circuits, however, RF inductor applications such as impedance matching for low-noise and distributed amplifiers, tank circuits for voltage-controlled oscillators, and bias chokes for power

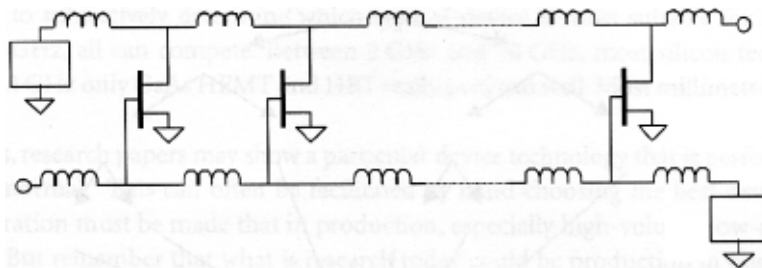
sources have become increasingly common [18]. Figure 1-1 shows the use of inductors in several of these applications [8, 24]). The use of inductors at these high frequencies often calls for inductances that can be realized in very small sizes. Two common approaches to packaging these small inductors with other circuitry include the fabrication of "on-chip" inductors contained completely within the metallization layers of an active die and the board-level integration of pre-packaged surface-mount inductors. Another intermediate approach that offers attractive benefits when compared to the methods just mentioned is the "on-package" integration of inductors within the metallization layers of a chip packaging approach such as Multichip Module-Deposited (MCM-D) or Low-Temperature Co-Fired Ceramic (LTCC).



(a) Low-Noise Amplifier [8]



(b) Voltage-Controlled Oscillator [24]



(c) Distributed Amplifier [8]

Figure 1-1: RF circuit applications of inductors

The use of on-chip (or on-die) passives typically results in increased area, lower yield, and higher expenses in active dice. For a packaging process such as MCM-D, where dice are purchased from vendors and integrated within the smallest possible space, the use of on-chip passives offsets many of the primary reasons for choosing that process [7]. On-chip inductors also typically suffer from significant performance problems due to the close proximity of the devices to a conductive silicon substrate [18].

Surface-mount components, on the other hand, typically consume a much larger area than the dimensions of an integrated component. In an MCM-D process, they usually must be mounted outside of the module, often adding undesired overall thickness. They can also suffer from increased parasitic effects due to the vias and external contacts required to connect them to devices inside a module. Furthermore, in a typical RF module, the necessary surface-mount components that cannot be integrated may require as much as three or four times the real-estate (area) as the underlying active silicon components, expensively increasing module size.

The on-package integration of inductors in MCM-D alleviates many of these problems [2, 7, 23]. In this approach, the inductors are integrated directly into the metallization layers of a module in a manner similar to that of on-chip integration in silicon back-end processing. This solution offers an alternative to surface-mount inductors with potentially smaller area costs and no additional thickness costs. It can also offer increased performance over traditional on-chip inductors due to increased separation from a conductive substrate, more conductive metallization, and a larger available area budget.

Draper Laboratory, Inc. (Draper) uses a custom MCM-D process to package bare silicon dice for applications with demanding size and performance requirements. MCM-D offers extremely high-density integration of bare dice into a single module using planar interconnect. The process has been continually improved to integrate many types of chips into the die layer, but some components, such as large passives, cannot easily be integrated. Draper produces modules containing RF components, but on-package integrated inductors have not yet been fully characterized within the process. For these reasons, the development of fabrication and design techniques for

on-package inductors would mark an important advancement for the process and for RF module fabrication. This work begins that development.

Additionally, the design of integrated inductors within any fabrication process can be very complicated. RF circuit designers would often like to specify simple electrical parameters for an inductor, but existing design tools force them to guess at some initial geometric layout and refine the design through exhaustive simulation and potentially expensive fabrication and testing. This work studies these problems within integrated inductor design as well.

1.2 Objective

The design of integrated inductors is not straightforward. The electromagnetic behavior of these devices can only be fully described by numerically solving several of Maxwell's equations—a tedious task that requires significant computational resources. Several software packages have been developed to approximate the behavior of integrated inductors, but the design method employed by many packages remains unsophisticated. A major development of this thesis is a straightforward design methodology that could potentially be used in combination with many available simulation tools. Using this methodology, an RF design engineer would simply specify a desired area, inductance, and operating frequency. From this information, an integrated inductor layout that lies within some tolerance of the desired specifications and exhibits an optimal quality factor would be produced. The methodology removes much of the guesswork involved in inductor design and allows RF engineers instead to focus their efforts on circuit design.

Another objective of this work is the fabrication and characterization of integrated inductors in MCM-D modules. The accuracy of simulation software in fully describing the effects experienced by MCM-D integrated inductors is not assured. This study compares simulation results to measurements and comments on potential improvements to accuracy and modeling specific to the Draper process. Additionally, further work aimed at eventually replacing most or all of the surface-mount and on-chip RF

inductors used in Draper MCM-D modules will be discussed.

1.3 Overview

This thesis is organized into six parts. The principles and background of integrated inductors are first presented, followed by an explanation of the design and experimental processes.

The next chapter explains the concept of inductance. It also clarifies several definitions of the “quality factor” metric.

The third chapter discusses possible topologies for integrated inductors. It explains several loss mechanisms of spiral inductors and discusses the influence of layout parameters on a spiral inductor’s performance.

Chapter four describes the simulation and modeling of spiral inductors. It discusses simulation techniques, extraction of equivalent circuits, and popular simulation software packages.

The fifth chapter introduces a new design methodology for spiral inductors. Both motivations and an implementation of the methodology are discussed. Simulation results studying the available quality factor of a device constrained by a given area budget are presented.

Chapter six describes the fabrication of integrated spiral inductors in the Draper MCM-D process. Details of the fabrication and measurement are explained, and the measurements of fabricated devices are compared with theory.

The final chapter discusses conclusions drawn from the research, simulations, and experimental analyses undertaken. It describes some of the lessons learned from this work and highlights future progress that could stem from these ideas.

Chapter 2

Inductor metrics

This chapter explains the concept of inductance. It also clarifies several definitions of the “quality factor” metric.

2.1 Inductance

An inductor is a component that stores energy in the form of a magnetic field. Maxwell’s equations imply that current moving through a conductor induces a magnetic field. Similarly, changes in a magnetic field near a conductor induce changes in the current flowing inside that conductor.

As current flows through an inductor, it creates a directional magnetic field surrounding the inductor. The presence of that field opposes any change to the current flowing inside the inductor. When the current changes (i.e. stops flowing or changes direction), the presence of the magnetic field causes current to continue to flow as before. Hence energy is stored in the induced magnetic field that allows current to persist in the absence of electrical energy. Inductance is a measure of how much energy can be stored in the magnetic field of a given device.

2.1.1 Self Inductance

From Ampere's law, we know that current moving through a loop of conductive material creates a magnetic field with intensity, \vec{H} :

$$\nabla \times \vec{H} = \vec{J} \quad (\text{Ampere's law}) \quad (2.1)$$

The magnetic field intensity, \vec{H} , is related to the magnetic flux density, \vec{B} , within a given material by that material's permeability, μ , according to:

$$\vec{B} = \mu \vec{H} \quad (2.2)$$

Using the divergence law and Faraday's law, an expression can be derived for the flux linkage, Ψ , through a given cross-sectional surface area, S [14]:

$$\nabla \cdot \vec{B} = 0 \quad (\text{divergence law}) \quad (2.3a)$$

$$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \quad (\text{Faraday's law}) \quad (2.3b)$$

$$\Psi = \iint_S \vec{B} \cdot d\vec{S} \quad (2.3c)$$

If the permeability, μ , is constant within a material, then the relationship between Ψ and the current, I , that created the magnetic field is linear. The constant of proportionality of this relationship is defined as the self-inductance, L , of the loop:

$$\Psi = LI \quad (2.4)$$

2.1.2 Mutual Inductance

Mutual inductance represents the effect of the magnetic field created by one loop on the magnetic flux (and thus inductance) within another nearby loop. A change in voltage is induced in loop i due to a change in current (and thus magnetic field intensity) in a nearby loop j . This change gives rise to a mutual inductance in loop i ,

M_{ij} , due to the current, I_j flowing in loop j that creates an impinging magnetic flux, Ψ_i , within loop i according to [18]:

$$M_{ij} = \frac{\Psi_i}{I_j} \tag{2.5}$$

The voltage change depends on the strength of the magnetic field interaction between the loops and consequently relates inversely to the separation distance between the loops. The resulting mutual inductance is seen by *both* loops equally if they are symmetric and carrying equal currents.

Using a method introduced by Ruehli in [25], it is possible to define a "partial inductance" of a non-closed conductor. While this quantity does not have the same physical interpretation as inductance because it is a quantity measured on an open-loop structure, it provides a useful mechanism for calculating the inductance of an integrated inductor composed of many conductor segments. Chapter 4 discusses this calculation and the concept of partial inductance in more detail. For now, it suffices to say that in the context an integrated inductor, a non-looped segment of conductor possesses a partial inductance that contributes (through self and mutual inductance) to the overall inductance of connected segments forming loops.

Since the magnetic field interaction between nearby conductor segments decreases with both increasing separation distance and increasing separation angle (measured as the smallest angle between two conductors), mutual partial inductance in planar integrated inductors is most significant for nearby parallel conductors such as adjacent metal lines. For two nearby conductors in which current flow is in the same direction, the voltage change caused by the mutual inductance of each on the other is constructive or positive—it adds to the self-inductance created by the current flow in each conductor. For nearby conductors with current flowing in opposite directions, the induced voltage change due to magnetic field coupling is destructive or negative mutual inductance—it subtracts from the self-inductance created by the current flowing in each conductor.

The total inductance of a conductive loop is the sum of the self-inductance and

all mutual inductances experienced by that loop.

2.2 Quality factor

Quality factor is a specification associated with all energy storage elements. Fundamentally, it represents the ratio of the amount of energy stored in a device to the amount of energy dissipated in a device—acting as a metric of storage efficiency. The quality factor is generally defined using the energy stored per cycle E_{stored} and the energy dissipated per cycle $E_{\text{dissipated}}$ as follows [18]:

$$Q = 2\pi \frac{E_{\text{stored}}}{E_{\text{dissipated}}} \quad (2.6)$$

As a device that stores magnetic energy, an inductor has an associated quality factor, Q . The last chapter alluded that inductors contribute to a diverse set of applications, and Q offers some insight into an inductor’s performance in each of these applications. However, the performance demands of each application differ, which has led to different (but related) definitions of Q depending on the application. Several of these definitions are described below.

2.2.1 Impedance definition

The most common definition of quality factor in inductors is drawn directly from the energy dissipation idea [21]:

$$Q = 2\pi \frac{E_{\text{stored}}}{T \times P_{\text{dissipated}}} \quad (2.7a)$$

$$\approx \frac{\omega (|\overline{W}_m| - |\overline{W}_e|)}{P_{\text{dissipated}}} \quad (2.7b)$$

$$= \frac{\text{Im}\left(\frac{1}{y_{11}}\right)}{\text{Re}\left(\frac{1}{y_{11}}\right)} = -\frac{\text{Im}(y_{11})}{\text{Re}(y_{11})} \quad (2.7c)$$

Energy is dissipated as power during each period of operation, T . The total energy stored in an inductor can be approximated as the difference between the average stored magnetic energy $|\overline{W}_m|$ and the average stored electrical energy $|\overline{W}_e|$. For a 2-port model of an inductor, the approximated formula can be simplified using network theory to a definition in terms of the device’s 2-port admittance parameters (or y -parameters) [21]. This approximation is only valid, however, when the average stored magnetic energy is much greater than the average stored electrical energy. In the case of an integrated inductor exhibiting internal parasitic capacitance, the electrical energy storage can become significant (particularly at high frequencies), causing this definition of Q to deviate from the total energy efficiency as described by Equation (2.6) [21].

2.2.2 Bandwidth definition

As explained, the definition above deviates from the ideal energy storage definition at high frequencies where the lines in an integrated inductor begin to exhibit significant capacitive effects with nearby metal (particularly, with adjacent conductors and with the substrate). With the addition of these capacitances, the inductor behaves like a second-order system. In particular, the inductor exhibits a frequency at which the system resonates, called “self-resonance” or ω_0 .

At self-resonance, the magnitude of the imaginary impedance is zero (the inductive and capacitive parts cancel), yielding a Q of zero according to Equation (2.7c). Clearly the inductor is still able to store both magnetic and electrical energy at resonance (in fact, it stores them in equal parts). It is in this instance that the correlation between Equations (2.7a) and (2.7b) breaks down, and the definition of Q from Equation (2.7c) becomes inadequate to characterize the system’s energy storage for some applications.

Certain bandpass filters and various other RF applications use integrated inductors at or near resonant frequencies. A more accurate metric of energy storage efficiency for these applications can be drawn directly from the bandwidth (or frequency selectivity) of a resonant system. If the poles of a second-order resonant system occur

at $s = -\alpha \pm j\omega_d$, then the Q of the system can be defined as:

$$Q = \frac{\omega_0}{2\alpha} = \frac{\omega_0}{\Delta\omega} \quad (2.8)$$

where $\Delta\omega$ is the 3-dB bandwidth of the system and ω_0 is the resonant frequency of the system related to the poles by $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$. Figure 2-1 graphically depicts the bandwidth of a second-order resonant system [5].

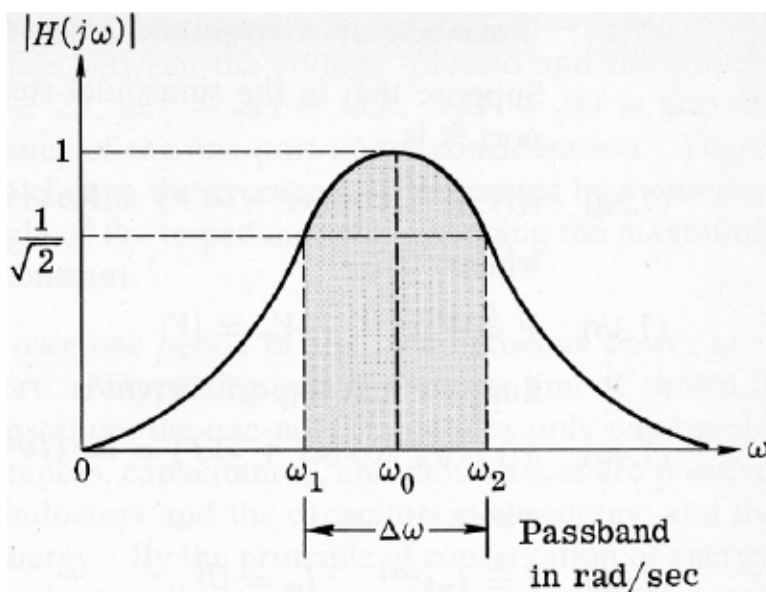


Figure 2-1: Bandwidth of a second-order system [5]

This definition of Q provides information about a system's energy efficiency independently of impedances or power ratios by relating the resonant frequency to an associated bandwidth around that frequency. A good example of the flexibility of this approach can be found in the difference between the Q of parallel and series RLC resonant circuits (see Figure 2-2) as described below:

$$Q_{\text{parallel}} = \frac{\omega_0}{2\alpha} = \omega_0 CR = \frac{R}{\omega_0 L} \quad (2.9)$$

$$Q_{\text{series}} = \frac{\omega_0}{2\alpha} = \frac{\omega_0 L}{R} \quad (2.10)$$

The resulting definitions of Q for these systems agree with the intuition that a high

quality resonator is one that does not dissipate much energy at resonance. In the parallel case, a high quality resonator is one with large R , such that most of the current will be forced through the L and C storage elements. In the series case, a high quality resonator is one with small R such that little energy is dissipated in the element at resonance. Note the discrepancy between this definition and that of Equation (2.7b), however. The bandwidth-derived values for Q for the parallel and series systems are reciprocal in terms of their circuit elements ($\omega_0 = 1/\sqrt{LC}$ for both systems), whereas the definition of Q from Equation (2.7b) yields zero for both systems at ω_0 .

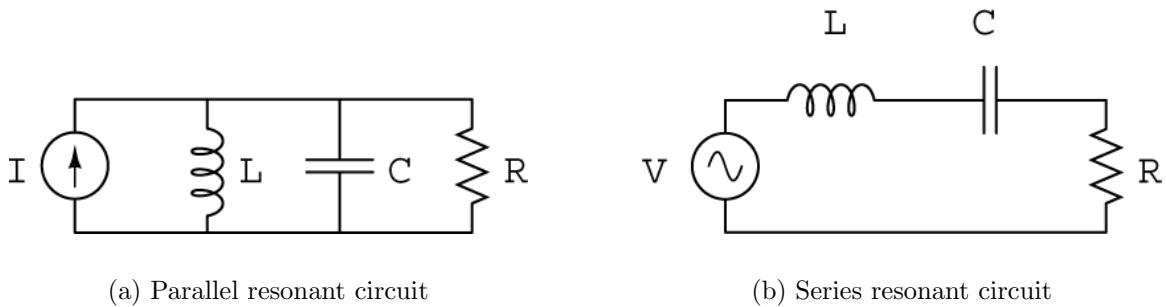


Figure 2-2: RLC resonant circuits

2.2.3 Phase definition

In other RF inductor applications such as oscillators and amplifiers, phase stability and phase noise are important parameters related to Q . This relationship results from the fact that the open-loop output voltage of a resonant system must be exactly 180° out of phase (for negative feedback) with the input voltage at the resonant frequency. In practice, however, short-term changes in phase are often introduced to the closed-loop resonant system causing some small phase shift. The sensitivity of the system to such phase changes can be characterized by the frequency (or phase) stability factor, S_F . The frequency stability factor of an oscillator (usually operating at ω_0) is defined as the change in phase, $\Delta\phi$, divided by the normalized change in

frequency, $\Delta\omega/\omega_0$ [27]:

$$S_F = -\omega_0 \left. \frac{d\phi}{d\omega} \right|_{\omega=\omega_0} \quad (2.11)$$

In a second-order system, such as one of many inductor-based resonators, this expression can be reduced to [27]:

$$S_F = -\omega_0 \left. \frac{d}{d\omega} \left[-\tan^{-1} \left(Q \left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \right) \right) \right] \right|_{\omega=\omega_0} \quad (2.12a)$$

$$= -\omega_0 \left(\frac{-2Q}{\omega_0} \right) \quad (2.12b)$$

The frequency stability factor, then, yields another definition of Q for an integrated inductor [21]:

$$Q = \frac{S_F}{2} \quad (2.13)$$

While Equations (2.8) and (2.13) yield higher values of Q at a given frequency than Equation (2.7c), they maintain similar qualitative behavior (or trends) at frequencies below self-resonance. This is largely because losses associated with the real impedance of y_{11} directly affect both the 3-dB bandwidth and the frequency stability factor of a second-order system. Even when an inductor is used in the context of a larger system (for example, with the addition of an outside capacitor in an LC tank), the definitions of Q from Equations (2.8) and (2.13) can be still be useful to quickly estimate the performance of the entire system [21]. This result stems from the fact that the energy storage efficiency (and thus frequency selectivity) of the entire system is limited by the efficiency (and selectivity) of the worst part of the system—usually the integrated inductor.

To more accurately characterize a larger system of this type (instead of relying on the estimate that a system is only as good as its worst component), the inductor can be analyzed directly in the context of the surrounding system. For example, a more accurate Q related to the phase stability or the 3-dB bandwidth of an LC tank using an external capacitor can be easily calculated from measured or simulated y_{11} data simply by adding the capacitor's admittance, $j\omega C$, in parallel with the y_{11} data [21]. Q calculated from this lumped system information is generally referred to as the

”loaded Q ” and offers another useful metric to RF designers.

The design methodology introduced in Chapter 5 focuses on designing devices operating below their self-resonant frequencies. Due to the widespread acceptance of the conventional quality factor definition in Equation (2.7c) for inductors at these frequencies, both the methodology in Chapter 5 and the verification in Chapter 6 use that definition to represent Q .

Chapter 3

Integrated inductor specification and loss

This chapter discusses possible topologies for integrated inductors. It also explains several loss mechanisms of spiral inductors and discusses the influence of layout parameters on a spiral inductor's performance.

3.1 Topologies

The incorporation of inductors into a planar integrated process such as MCM-D limits the available topologies for design. If the inductor is restricted to a single layer, available topologies include a transmission line inductor, a loop inductor, and a meander inductor (layouts (a), (b), and (c) respectively in Figure 3-1) [2]. Designs using the first two topologies yield only very small inductances due to the lack of positive mutual inductance between segments. Meander inductors can provide a larger number of segments, but the mutual inductance between nearest neighbor conductors is negative, yielding poor performance.

If the planar constraint is relaxed to allow the use of two or more layers, new topologies become available. A 3-dimensional solenoid structure (see Figure 3-1(e)) can be constructed in a planar fabrication process by using vias for the vertical connections, but the use of a large number of vias may introduce prohibitively large resis-

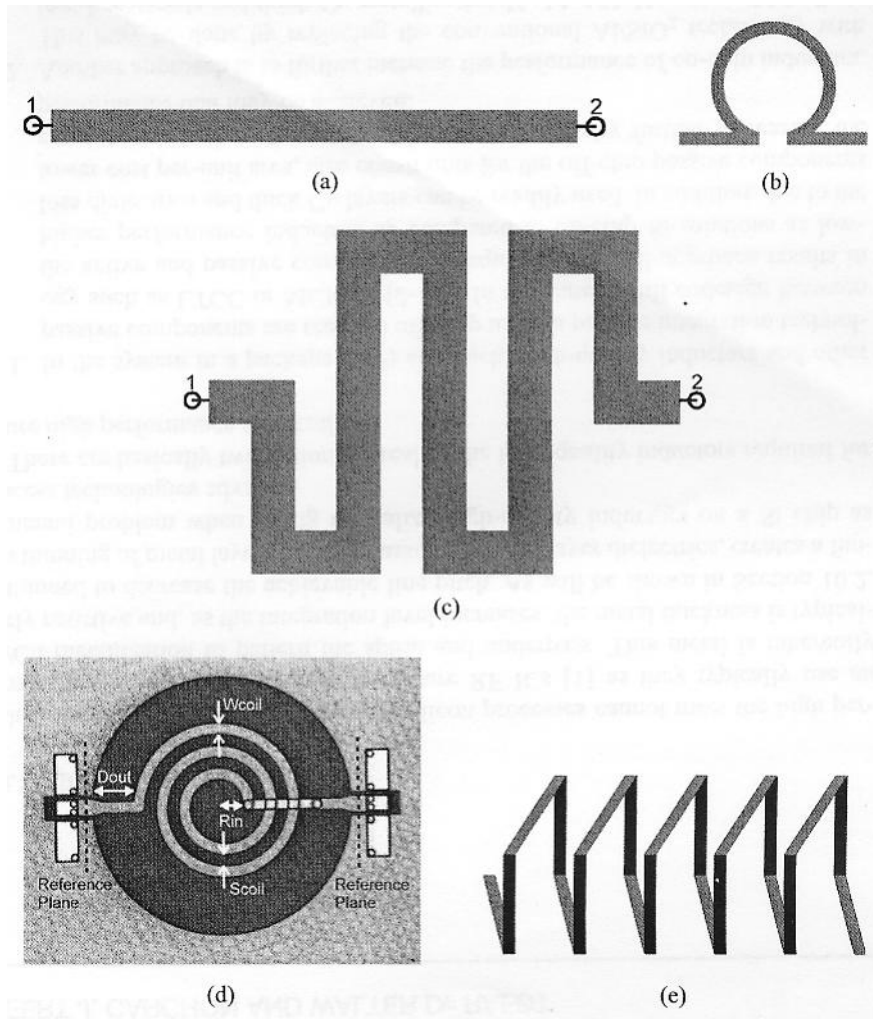


Figure 3-1: Layout topologies of (a) transmission line inductor, (b) loop inductor, (c) meander inductor, (d) circular spiral inductor, and (e) solenoid inductor [2]

tance values. The introduction of an additional layer also makes the spiral inductor topology (see Figure 3-1(d)) available through the use of an underpass connection in a different metal layer to connect to other nodes. For a reasonable center diameter size, all of the nearest conductors in a spiral inductor exhibit positive mutual inductance with each other. This allows spiral inductors to create a larger inductance within a given area than the other single-layer topologies mentioned.

Even within the domain of spiral inductors, several topologies exist. The spiral can consist of an n -sided polygon or a circular shape. Among these, polygon spirals with high values of n and circular spirals are thought to produce inductors with the

highest quality factor and with very uniform magnetic fields (due to the lack of sharp field discontinuities at corners [23]). In [3], it was found that for equivalent values of inductance, circular- and octagonal-shaped spiral inductors exhibited 10 percent lower resistance (at 1GHz). In [2], the authors describe another study comparing circular and rectangular layouts with equivalent area consumption. Again, they found that circular spirals produce higher inductance per unit area as well as higher maximum quality factors than square spirals. While this area efficiency of circular spirals is an important finding, the study in [2] neglected to account that circular spirals are usually surrounded by other rectangular components in a physical layout. In this situation, a more useful metric of area consumption is the rectangular bounding box area of the inductor. For this definition, data from the same study in [2] show that square spirals have higher inductance per unit area than circular spirals.

While quality factor and area are certainly very important characteristics for integrated inductors, there are other constraints to consider in preparing a design. Some of the most rigid constraints are imposed by the physical limitations of the fabrication process used. Many processes restrict designs to manhattan geometries (in which shapes are constrained to rectangular dimensions and perpendicular intersections). In such situations, the photolithographic process cannot create features used in circular spirals, so square spirals must be used. In other instances, sharp angles are not reproduced with high accuracy in the photolithographic and etching processes. For such processes, circular spirals are preferred for their rounded features.

One area where a process may not be as tightly constrained is in the number of metal layers, and the utilization of additional metallization can offer a new degree of freedom in the design process. Spirals can be stacked on multiple layers within a planar process and connected together either in series or in parallel to save area. Vertical magnetic coupling between series-connected multi-layer inductors can enhance the total inductance value (through mutual inductance effects), but the parasitic capacitive coupling between inductors can greatly reduce the self-resonant frequency. Parallel-connected multi-layer inductors can offer lower resistive losses for a given inductor design (by effectively acting like a thicker metal layer with a large surface

area), but again the capacitive losses can be problematic.

For simplicity of design and ease of computational modeling, this study focuses on square spiral inductors utilizing a single layer for the spiral and an adjacent layer for the underpass connection.

3.2 Loss mechanisms

Spiral inductors (and many other inductor topologies) exhibit several mechanisms for resistive and capacitive losses, especially at high frequencies. The most dominant mechanisms are discussed below.

3.2.1 Eddy currents

The magnetic fields created by the conductors under consideration (i.e. metal lines in the MCM-D process) also affect other conductive materials such as other conductors (metal lines), silicon die substrates, ground planes, some dielectric materials, and magnetic materials. A magnetic field created by a conductor can intersect a nearby conductor and induce small circular currents (“eddy currents”) within the new conductor. These eddy currents in turn produce a magnetic field that opposes the original field, generating a loss in the efficiency with which the field can change direction (as it does often in the case of high frequency alternating current). Additionally, these eddy currents dissipate energy in the form of heat as they flow through the conductor, further decreasing the efficiency of energy storage.

3.2.2 Skin effect

Eddy currents are also responsible for the skin effect, in which changing magnetic fields produced by a conductor induce eddy currents inside the center of that conductor. At high frequencies, the opposing fields created by eddy currents are strongest in the center of the conductor, causing the current density in this region to decrease sharply. Most of the current flows much more strongly near the surface of the con-

ductor, causing the apparent cross-sectional area of the current-carrying conductor to decrease (and consequently causing the AC resistance to increase). Figure 3-2 shows an example of the skin effect on current densities within a conductor¹.

A measure of how deeply the current and magnetic flux can “penetrate” into a material is the skin depth, which is defined as the depth in the conductor at which the current density has fallen to $1/e$ or approximately 37 percent of its value at the surface. An approximation of the skin depth can be calculated using the magnetic permeability, μ , and the electrical conductivity, σ , of the material, as well as the frequency of operation, ω , using the following equation [18]:

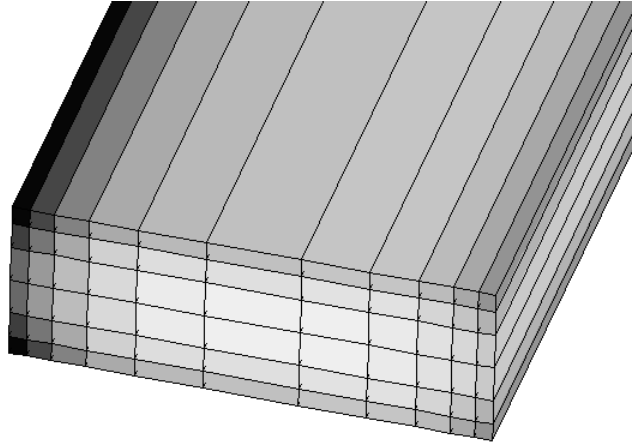
$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \quad (3.1)$$

If the skin depth is significantly larger than the conductor thickness at a given frequency, then the skin effect is negligible at that frequency in that conductor. Thus, designing inductors such that the conductor thickness is smaller than the skin depth at operating frequencies can be a useful rule of thumb, though other constraints may not always permit this design decision.

3.2.3 Proximity effect

The proximity effect is another instance of eddy currents, in which nearby conductive material experiences induced eddy currents due to the magnetic field of a separate conductor. An example of this phenomenon is “substrate loss” or ground plane loss when eddy currents are induced in the silicon die substrate (or in a ground plane) directly below a CMOS integrated inductor. The eddy currents dissipate power as heat in the substrate (or ground plane) and can significantly decrease the efficiency of the system [2, 18]. Proximity effect is also an important loss mechanism when the distance between adjacent conductors in a spiral inductor is made very small.

¹The figure was produced using Fastmaxwell software [4] through the simulation of an inductor with traces $15\mu\text{m}$ wide and $5\mu\text{m}$ thick at 4GHz operating frequency.



(a) Current density magnitude is depicted by a linear grayscale with the largest current density normalized to black. Skin effect causes current density to decrease within the conductor. Proximity effect from a nearby conductor to the right causes current crowding on the left side of this conductor.

Figure 3-2: Eddy currents acting within a conductor at 4GHz

3.3 Influence of parameters

Figure 3-3 shows the parameters of a square spiral inductor layout. The number of turns (n), conductor width (w), spacing between conductors (s), conductor thickness (h), and spacing to ground (s_g) all influence the electrical properties and losses of a spiral inductor. The exact physical nature of the interaction between these parameters and a device’s resulting electrical properties remains a mystery—there is no closed-form representation, for example—but the qualitative relationship is understood and is discussed below.

The first parameter used to specify a spiral inductor layout is the number of turns, n . Note that due to the ”partial inductance” concept explained in the next chapter, n does not have to be an integer. An open-loop device can be simulated by considering the partial inductances of all of its segments. n has the largest influence of any parameter on the inductance, area consumption, and maximum quality factor

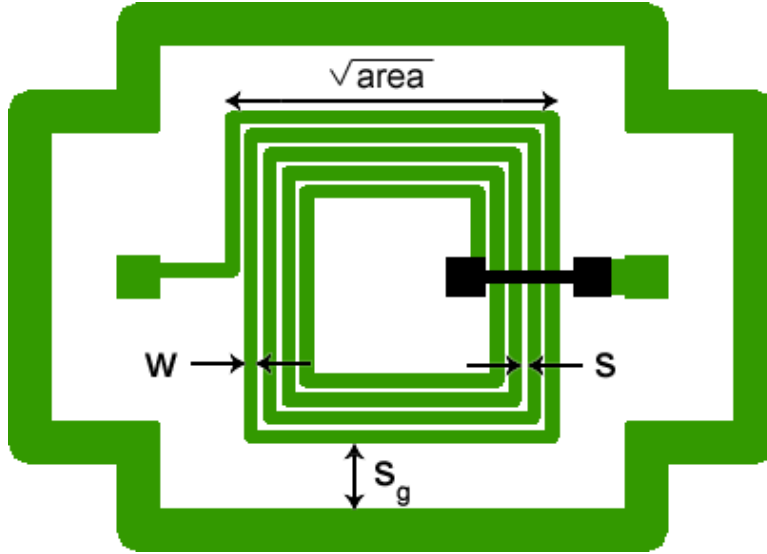


Figure 3-3: Layout parameters of a square spiral inductor

of a spiral inductor [22]. With increasing n , the total self-inductance of the device is increased through the addition of new conductors, and the total mutual inductance of the device is increased through additional magnetic coupling. At the same time, greater parasitic capacitances are present because of the additional metal-to-substrate capacitance of the new turns as well as the increased metal-to-metal capacitance between wires. From these phenomena, it can be seen that the most prominent result on the device of an increase in n is an increase in inductance coupled with a decrease in resonant frequency.

Another important parameter in specifying a spiral inductor layout is the conductor width, w . At DC, an increase in w increases the inductance of the spiral, while at the same time decreasing its resistance (and consequently improving its quality factor) [22]. As the frequency of operation increases, the improvement in resistance achieved by increasing w begins to diminish due to the skin effect. If w is kept below the skin depth at the frequency of operation, this diminishing return effect is minimal. In some instances, however, a lower resistance (and higher quality factor) is desired than that available using a conductor width of one skin depth. In such cases, a w can still be increased to reduce resistive losses. The resulting device has weaker current density over a large region in the center of the conductor, but the overall conductance

can still be large (i.e. a small current density times a very large cross-sectional area still equals a large conductance). At such large values of w , the metal-to-substrate capacitance can become very significant. In order to obtain useful inductors within this design space, great care can be taken to reduce the substrate capacitance through patterned ground shielding, micromachining techniques, increased separation from the substrate, and/or non-conductive substrate materials. In many MCM-D processes, which are restricted to large enough minimum line widths that sub-skin depth designs are not an option, non-conductive substrates can be utilized. As long as inductors are not placed within the module directly above an active die containing a conductive substrate, the substrate proximity effect can nearly be eliminated.

The conductor thickness, h , behaves somewhat similarly to the width. As the thickness is increased, the resistance decreases and quality factor improves, but diminishing returns are experienced at thicknesses much greater than a skin depth. Another consideration in varying h is the additional vertical surface area introduced with a thicker metal. This can result in a larger metal-to-metal parasitic capacitances between wires. While this effect can significantly reduce the frequency of resonance within a device, changes in thickness do not have a very significant effect on the inductance of a device. This result follows from a largely unchanged geometry with respect to magnetic coupling between conductors as h varies. Although h could seemingly be used to trade lower resistance for higher capacitance at fixed inductance, it turns out that this approach to design is impractical. In general, h is fixed by the fabrication process, leaving it unchangeable by the designer. In [2], a method of varying h through shunting together spirals on several layers is discussed, but the increased capacitance between the resulting shunted layers often reduces a device's resonant frequency prohibitively.

The spacing between conductors, s , can have a profound effect on metal-to-metal capacitance. For small values of s under operation at high frequencies, signals can couple directly between adjacent wires through this parasitic capacitance. For this reason, s often dominates the resonant frequency of a spiral, and the determination of the smallest s that allows useful operation at a given frequency can be an impor-

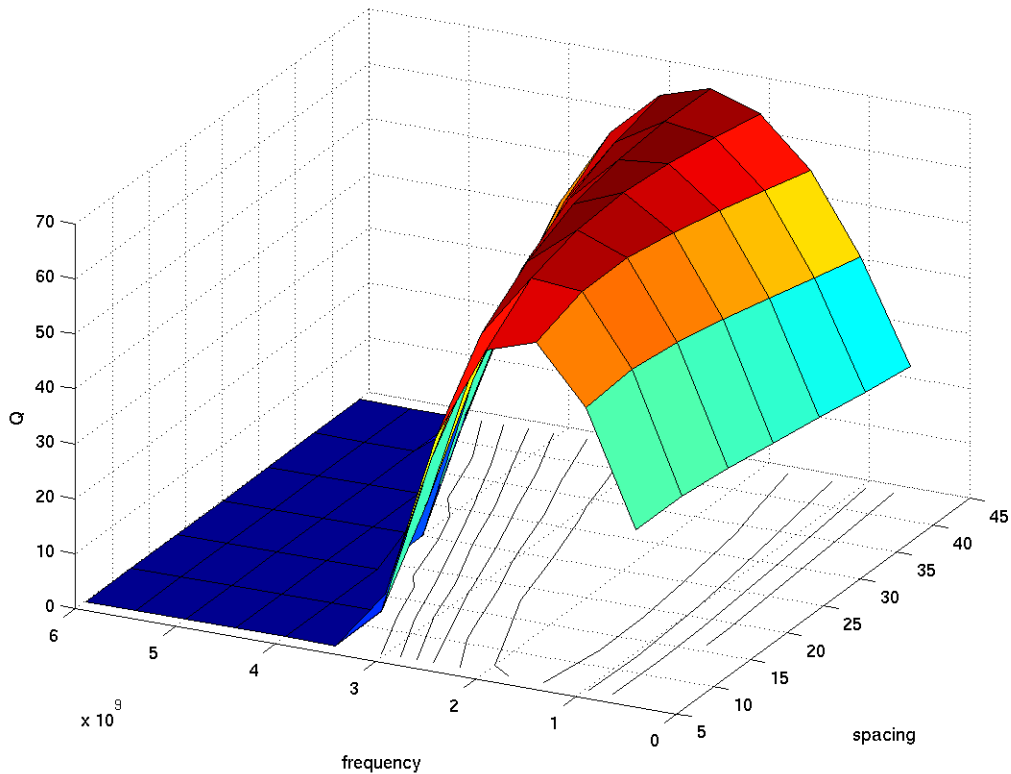


Figure 3-4: Simulation data showing the effect of spacing on quality factor

tant tool in design. At frequencies below resonance, however, the effect of s is less pronounced. Figure 3-4 shows simulation data² of several 0.5625mm^2 spiral inductors with varied spacing. From the figure, contour lines at low frequencies are nearly parallel to the s -axis—implying that the variation of s does not affect the quality factor plotted in the vertical direction. For an MCM-D process with large minimum-feature sizes and modules operating at relatively low RF frequencies, inductors can typically utilize the minimum value for s allowed by process design rules and still achieve reasonably high resonant frequencies.

The distance, s_g between a device and a nearby grounded conductor can be a very important parameter in integrated inductor losses. Whether this distance represents the vertical separation between a device and a conductive substrate (as in most silicon

²The simulations were run using *ASITIC* software [19] on inductors with a constant line width of $25\mu\text{m}$ and spacing varying from $6.25\mu\text{m}$ to $62.5\mu\text{m}$.

integrated inductors) or the distance between a device and a surrounding ground ring (as in the Co-Planar Waveguide (CPW) inductors studied in this thesis), the loss mechanism remains the same—proximity effect. The magnetic field generated by the conductors induces eddy currents in the grounded material and magnetic energy is lost to heat. In CPW designs and particularly in those with large area budgets such as some MCM-D designs, this distance can often be set to a large enough distance to avoid significant loss.

Chapter 4

Integrated inductor analysis

This chapter describes the simulation and modeling of spiral inductors. It discusses simulation techniques, extraction of equivalent circuits, and popular simulation software packages.

4.1 Analysis methods

Several methods of analyzing spiral inductors are available, based on different electromagnetic simulation technologies. The methods may include finite-difference time-domain, finite-element, or method-of-moments simulation techniques [11]. These techniques can vary widely in exactly how the electromagnetic interactions within an inductor are transformed into mathematical relations, and in the computational resources required to solve these relations. Some of the less computationally intensive simulation and analysis methods for integrated inductors are briefly described here.

As discussed in Chapter 2, inductance can be expressed in terms of the self-inductance of a loop conductor and the mutual-inductance (either positive or negative depending on the direction of current flow) exhibited between nearby loops. In [9], Greenhouse introduces a simple method for approximating the inductance of two-dimensional rectangular inductors as that of several interacting loops. The self-inductance, L_i , of each conductor and the mutual inductance, M_{ij} , between each pair of conductors i and j are summed to estimate the total inductance (his computa-

tion is simplified by considering only parallel conductors in the mutual inductance calculations):

$$L_{tot} = \sum_{i=1}^N L_i + \sum_{i=1}^N \sum_{j \neq i}^N M_{ij} \quad (4.1)$$

For the computations of the self- and mutual-inductances involved in Equation (4.1), Greenhouse relied on formulas published by Grover [10] using two quantities called the geometric mean distance (GMD) and the arithmetic mean distance (AMD). The GMD is method of reducing two conductors with volume to infinitely small wires. It represents the distance between two infinitely small wires such that their mutual inductance is the same as that of the original conductors [9]. The AMD is the average of all possible distances between points lying within one conductor and points lying with another conductor [9].

Two years before Greenhouse’s work, Ruehli introduced a method for calculating inductances of more complex geometries in [25] based again on formulas by Grover in [10]. The calculations in this work utilize segments of the inductor structure, with each segment exhibiting a ”partial inductance” $L_{p_{ij}}$ that can be added to other partial inductance expressions to form an expression for the overall inductance. This partial inductance is calculated by solving an integral equation derived from Maxwell’s equations.

While Ruehli’s segmentation approach allowed discretization of an integrated inductor structure into smaller filaments for more accurate characterization, neither his nor Greenhouse’s original work accounted for loss mechanisms experiences in inductors at high frequencies (see Chapter 3). In [26], however, Ruehli extends his original work into a more sophisticated tool, the partial element equivalent circuits (PEEC) model, which included capacitive loss calculations.

The PEEC model has undergone significant developments in 30 years, as described and referenced in [18], to improve its accuracy and speed and to include new models of loss determination. In many recent implementations of PEEC, Maxwell’s equations are first converted into a linear system of equations using Green’s functions. The partial inductance and partial capacitance matrices resulting from a quasi-static numeri-

cal integration of Green's functions are assembled into a larger system of equations by applying fundamental electrical principles—Kirchoff's Current Law (KCL), Kirchoff's Voltage Law (KVL), and Conservation of Charge—to the topology of the inductive device [18]. The system is solved using computational techniques for efficiently reducing and inverting large matrices, from which the solution can be expressed in terms of the system's impedance, admittance, or scattering network parameters (z -, y -, or s -parameters respectively). A major advantage of the PEEC approach is that it can obtain reasonable accuracy for a much smaller computational cost than many three-dimensional simulation approaches.

Another analysis model is based on a method-of-moments simulation technique. Both an advantage and a drawback of this technique are that it considers only metal surfaces in formulating field quantities for solution. This greatly reduces the computational complexity of the model, but at the same time can fail to take into account some three-dimensional effects occurring within the conductors. Thin film metal layers are reduced to infinitely-thin (two-dimensional) metal panes for calculation. Vertical interconnection between metal layers is also achieved using two-dimensional metal panes to represent vias. This approach has given rise to the name "2.5-dimension" simulation due to the limited modeling of the vertical dimension [2].

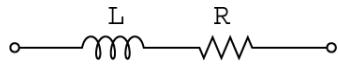
A method-of-moments formulation often begins as in PEEC with an integral formulation of Maxwell's equations. The equations are solved using planar meshes consisting of polygonal panels representing the metallization present in the geometry. The surrounding substrate and dielectric material properties are specified to impose boundary conditions on the panels for solution [11]. Again the solution can be expressed in terms of z -, y -, or s -parameters that completely characterize the device's behavior. Both the accuracy and the computational intensity of this approach relies on the size and density of the metallization mesh and the complexity of surrounding materials [2].

4.2 Circuit models

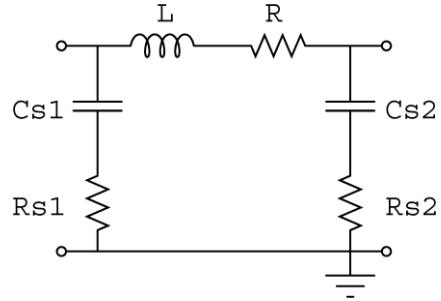
While many simulation techniques focus on determining the complete network behavior of an integrated inductor such as its 1- or 2-port s -parameters, this information is not always in the most useful format for designers. Certainly, a lot can be understood about the behavior of a device from its s -parameters, but designers are usually interested in including an inductor device in the context of a larger circuit or system. In this instance, it is useful to have a more compact representation of the device for inclusion in a larger system simulation. Several compact circuit models representing integrated inductors have been developed for this purpose.

The simplest model available for representing integrated inductors is composed of an inductor in series with a resistor that represents ohmic losses along the length of the inductor (see Figure 4-1(a)). This representation can be easily extracted directly from the 1-port complex impedance of the device, $Z_{in} = R + j\omega L$, and it can be useful for characterizing the device's behavior at low frequencies. At higher frequencies, however, the conductors begin to exhibit parasitic capacitances, and a model that accounts for these effects becomes more appropriate.

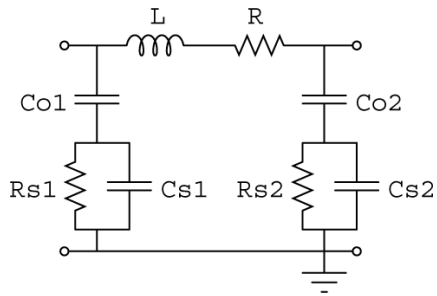
The simple "II" circuit model of Figure 4-1(b) does a reasonable job of accounting for loss effects over a range of frequencies. The additional components, C_{s_i} and R_{s_i} , are added to model capacitance and conductance observed from the conductors to a grounded substrate or other surrounding features. The model can still be extracted from measured or simulated 2-port y -parameters using simple network theory (refer to Chapter 6 for more information about 2-port measurement of spiral inductors). By assuming that the second port of the model is shorted to ground (and provides a return path through ground for the inductance loop), the y_{21} parameter—the current flowing through the shorted second port divided by the voltage at the first port—represents the admittance of the series inductor and the series resistor in the model. With this knowledge along with other simple admittance transformations, the elements of the



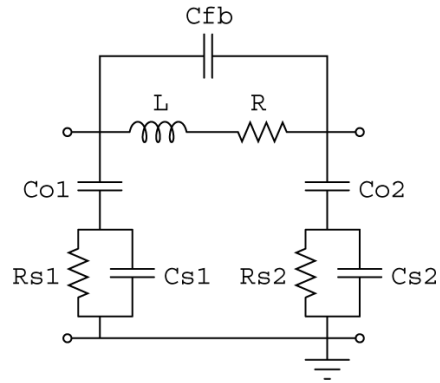
(a) Simple 1-port model



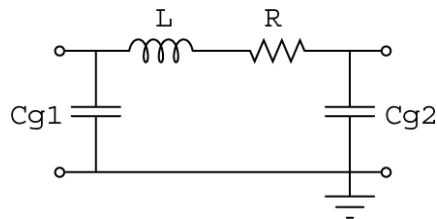
(b) Simple II model



(c) II model with more accurate substrate elements



(d) II model with feedback capacitor



(e) Simple II model for a non-conductive substrate

Figure 4-1: Equivalent circuit models for integrated inductors

model can be easily extracted as follows [2]:

$$L = -\text{Im} \left(\frac{1}{y_{21}} \right) \times \frac{1}{\omega} \qquad R = -\text{Re} \left(\frac{1}{y_{21}} \right) \qquad (4.2a)$$

$$C_{s1} = \frac{\text{Im}(y_{11} + y_{12})}{\omega} \qquad C_{s2} = \frac{\text{Im}(y_{21} + y_{22})}{\omega} \qquad (4.2b)$$

$$R_{s1} = -\text{Re} \left(\frac{1}{y_{11} + y_{12}} \right) \qquad R_{s2} = -\text{Re} \left(\frac{1}{y_{21} + y_{22}} \right) \qquad (4.2c)$$

The simple Π model has evolved as researchers work to make its performance more accurately match that of measured inductors. This evolution is not limited to the model's topology, however. It extends to how the model is applied. While Π models were originally developed as a means to fit measured or simulated data to a circuit with equivalent behavior, techniques have been introduced to predict inductor behavior by directly calculating approximate values for circuit elements within a model. In [16], for instance, the model shown in Figure 4-1(c) was used with a method-of-moments analysis in a distributed fashion. The new circuit elements, C_{o_i} , R_{sub_i} , and C_{sub_i} were used to more accurately model the oxide capacitance and the substrate's capacitance and resistance. To perform the calculations, each straight segment of metal conductor was analyzed and modeled by the 8-element Π model shown. Additional circuit elements were used to model the interconnection of the segments, and the resulting distributed circuit model was simulated to yield the overall inductor performance¹.

Another example of the two-fold focus in developing the Π model is that of Yue et al. in [28] and [29]. In [28], he uses the circuit model shown in Figure 4-1(d) to fit extracted measurement data to a circuit. The addition of the feedback capacitor C_{fb} models the capacitance between the inductor and the underpass connection, which is effectively a capacitance from input to output. In [29], however, he uses the model as an analysis technique, explaining how each circuit element can be calculated independently to predict an inductor's performance.

The equivalent circuit from Figure 4-1(d) turns out to model an inductor quite

¹A similar study using the updated circuit model in Figure 4-1(d) followed in [17].

well, but only over a narrow frequency range. When extracting the circuit elements from measured or calculated network parameters, there is no straightforward method or equation to extract a single value for C_{fb} because it represents a frequency-dependent capacitance and because its placement in the circuit exhibits a prominent influence on the overall circuit behavior. For these reasons, an optimization routine is often used to fit data to the circuit over a narrow range of frequencies. In [1], a more complex "2-II" equivalent circuit is developed to model the behavior of an inductor over a wide band of frequencies. The distributed model is somewhat complex, and while its parameters can be calculated directly from the inductor layout (again acting as an analysis tool as in [29]), fitting measured data to the equivalent circuit requires an optimizer.

The presented models are widely applicable to integrated inductors over a conductive silicon substrate. In the MCM-D process used for fabrication in Chapter 6, the substrate material is composed of high-purity alumina, making it essentially non-conductive. Thus, this thesis uses a modified version of the single-II equivalent circuit model for highly resistive substrates shown in Figure 4-1(e) [2].

4.3 Simulation software

Many commercially and freely distributed software packages are available for the simulation of integrated inductors. FastHenry [12] is one such package that uses an accelerated iterative method to extract inductances at any frequency. The solution uses the magnetoquasistatic (MQS) assumption that no significant displacement current exists, so that it can discretize an arbitrary input geometry to slender filaments with uniform current and then apply a Generalize Minimal Residual (GMRES) algorithm to solve the matrix system [13]. FastHenry was a novel development in that it offered greatly improved computational efficiency in reducing and solving the equations over previously available implementations. It is limited, however, by its sole reliance on volume filaments. With this approach, it can model eddy currents and proximity effect but not high frequency capacitive loss or self-resonance.

FastImp [31] was later developed by the same research group that produced FastHenry. It takes advantage of a new surface integral formulation for numerically expressing Maxwell's equations and of a fast method of matrix system solution using pre-corrected Fast-Fourier Transforms (pFFT) [30]. The new approach allows FastImp to solve problems using a full-wave formulation rather than a quasi-static approximation such that geometries with dimensions near the wavelength of interest can be accurately simulated. Both the standard QMS approximation and a new electromagnetoquasistatic (EMQS) approximation are available to speed up simulations compared to the full-wave approach. Additionally, FastImp adds discretized panels to the surfaces of metallization within a geometry. Using these panels, its calculations can account for capacitive effects over a wide range of frequencies, including the effect of resonance, and it is able to extract general impedances rather than simple inductances. Still, neither FastHenry or FastImp allows the specification of fabrication process parameters (such as a nearby substrate or dielectric material) that influence the losses experienced within an integrated inductor.

ASITIC [19] is an implementation of the PEEC formulation offering inclusion of information about the fabrication process stack-up in the calculation. It is also a design tool for integrated inductors and transformers, offering a great deal of automation in the specification of structures to be simulated. Its analysis can optionally include the effect of a conductive substrate on the quality factor of the device—an important option for nearby grounded conductive substrates that can cause significant loss due to ground eddy currents. One limitation of *ASITIC* simulations is that inductive filaments and capacitive panels are discretized uniformly. For small filament width (i.e. at high frequencies), this approach can result in very long simulation times. Several other simulation software packages allow the specification of a ratio for filament discretization, such that smaller filaments are used near the edges of a conductor and progressively larger filaments are used toward the center (this effect can be seen in the filaments of the conductor in Figure 3-2). For large conductors or high frequencies, this approach takes advantage of the smaller changes in current density that occur at the center of a conductor due to the skin effect.

Momentum is a commercially available simulation tool offered by Agilent EEsof EDA. Using the Agilent Advanced Design System, layouts can be generated directly from geometrical parameters for spiral inductor models. The resulting metal geometries can be simulated while accounting for specified loss information about the surrounding substrate and dielectric layers, boundary conditions of the layout, and loss mechanisms such as surface roughness. Momentum uses the "2.5-dimension" method-of-moments technology described above to simulate structures.

While each of these tools was investigated and utilized, this thesis relies on *ASITIC* software to specify and simulate a large number of inductor topologies. The design methodology introduced in the next chapter, while applicable to most simulators, was implemented using *ASITIC*.

Chapter 5

New Design Methodology

This chapter introduces a new design methodology for spiral inductors. Both motivations and an implementation of the methodology are discussed. Simulation results studying the available quality factor of a device constrained by a given area budget are presented.

5.1 Geometrical vs. Electrical Specification

Most commercially and freely distributed inductor simulation software packages are focused on optimizing electromagnetic calculations. Their purpose is the efficient and accurate transformation of arbitrary geometric configurations of conductive and non-conductive elements into an electrical representation—often s -parameters or a circuit model. What many of these software packages lack, however, is an interface accessible to designers.

During the course of this work, several software packages were evaluated, and it was found that each package involved the application of simulation-specific knowledge. Often this knowledge stemmed from the area of numerical computation—such as the understanding that simulated inductor data should be checked for convergence to a single solution and for bounds on accuracy by varying a computation’s meshing size or discretization of filaments. Other times, the packages simply required familiarity with proprietary input formats for designs, simulation parameters, and materials

information. The most common unknown among these packages was the procedure for beginning a simple inductor design.

Most designers turn to an inductor simulator when they are in need of a specific part for a circuit. They have some idea about specifications for that part, but this idea usually takes the form of desired ranges for inductance, quality factor, frequency of operation, frequency of resonance, etc.—in other words, parameters *derived* from the electrical representation of an inductor. Most simulation software, on the other hand, generally asks for geometric inputs such as the number of turns, the conductor width, the spacing between conductors, a location relative to other devices, or even a tedious description of exactly where each segment in the device should be placed. Designers—even ones familiar with spiral inductors—simply do not know how many turns to specify for an arbitrary inductor design. They are forced to make some initial guess as to the design geometry before proceeding.

Thankfully, some software packages include a library of inductor sizes as a starting point for generating a custom integrated inductor. Others trust that the designer will find and use some closed-form approximation for inductance to generate an initial geometry. Some software packages even go so far as to include limited searching or fitting capabilities to find a design within a range of inductances. Still, these approaches fail to provide mechanisms for custom searching of the design space or optimization over desired parameters. The approach presented here generalizes the available search and optimization capabilities by externalizing their control from the simulation software package.

5.2 Searching the Design Space

This study developed an algorithm to control and interact with an inductor simulator in an automated way. The simulator chosen was *ASITIC* [19] for reasons of free distribution and ease of interfacing, but the principle behind this approach can be applied to virtually any simulation software. The algorithm begins by querying the designer for information about the desired inductor—inductance, frequency of operation, cost

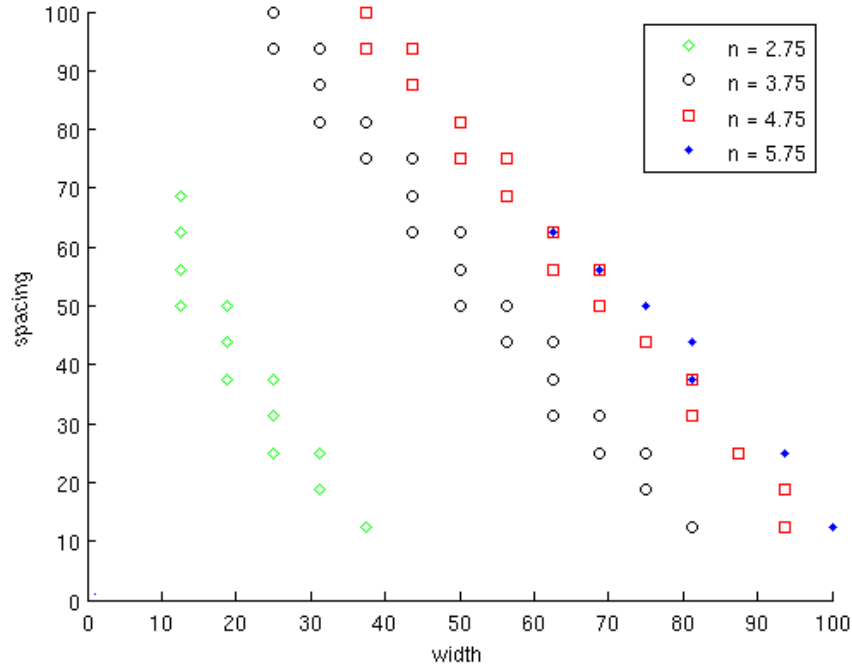
(area), and tolerances on these specifications. The algorithm then searches the design space in an automated and efficient manner to narrow the field to inductors matching the given specifications (since many different designs can realize a single inductance). From the remaining designs, the designer can choose the most appropriate inductor for his or her application by viewing additional information about the electrical behavior and physical parameters of each design.

The idea of methodically searching a design space is certainly not new. Some of the software packages previously discussed even have internal commands to search a narrowly defined space. The benefit to the approach presented here is its freedom and flexibility in designing a search. By changing how the design space is traversed within the algorithm, the search can be completely customized. As an example, an implementation of the algorithm discussed in the next section takes advantage of the availability of two different types of analysis within the *ASITIC* simulator—a fast and less accurate command to narrow the often enormous design space, and a much slower and more accurate command to search for exact matches to the specifications. The resulting design process takes much less time to search the space than *ASITIC*'s internal search command. For example, the design search for an optimal 20nH inductor operating at 1GHz and measuring 1mm² took under 18 minutes on a 1.8GHz Pentium 4 computer. *ASITIC*'s internal search using the `sweep` command took over 6 hours on the same machine to produce identical results¹. The performance of this approach versus `sweep` improves even more drastically for searches utilizing larger areas.

The script also allows the application of other techniques to increase the search speed. For example, many designs meeting the same specification are often found within a localized area. This results from the principle that small changes in geometric parameters cause correspondingly small changes in electrical parameters. Figure 5-1

¹It should be noted that details of the search implementation differed from those presented below. They were adjusted to mimic `sweep`'s analysis approach by using of a smaller increment for n , removing ground structures from the analysis, simplifying the inductor geometry, etc. Additionally, the size of the design space was dramatically reduced for both simulations by setting the maximum width and spacing values to 37.5 μ m. This adjustment was made to provide a reasonable upper bound on the time required by `sweep`.

shows an example of the spacial locality observed during a search for a 2.25mm^2 , 22nH inductor operating at 1GHz . Several other searches showed very similar trends in the location of solutions. This locality could potentially be exploited by the script by simulating several random data points throughout the space then searching locally around any areas containing a near match.



(a) Data points represent inductors matching the design criteria found with the width and spacing parameters shown (refer to Chapter 3 for more information about how width, spacing, and n are defined). The shape of each data point indicates the number of turns in the matching inductor. Some matching inductors overlap because they have identical width and spacing but slightly different n . In this case, both inductors fit within the tolerance of the search. For example, the addition of another turn may change the device's inductance from 21nH to 22nH in the search shown.

Figure 5-1: 22nH inductors found by searching the design space

The availability of several closed-form expressions approximating inductance directly from geometric parameters could also be exploited by the script. The formulas could be used to narrow the search space before simulation or as a means of feedback to control the simulator by estimating the direction of likely solutions within the

space from given simulation results. As an example of how the script could predict the "direction" of solutions in the design space, note the linear trend of solutions found with a given number of turns in Figure 5-1. A simple linear interpolation from two solutions could provide probable locations of a large number of additional solutions. Alternatively, if an objective of the search was the optimization of inductor quality factor, an external optimization routine could be called from the script to narrow in on an optimal solution quickly.

In fact, optimization of quality factor is often a realistic goal for the design process. In the script used to generate the data shown in this chapter, design spaces were searched for the inductor exhibiting the highest possible quality factor at a given frequency. It is important to remember, however, that the resulting quality factor, as with all the results of this method, are limited by the accuracy of the simulator used.

5.3 Implementation of the search

A condensed but functional Perl [6] implementation of the algorithm mentioned above can be found in Appendix A. The script searches the design space methodically to find inductors matching a given inductance, area, and frequency of operation (within some tolerance) by varying several parameters and performing analyses on the resulting devices. The approach used to search the design space is presented below. Recall that n is the number of turns in a device, w is the conductor width, and s is the spacing between conductors.

Refer to the pseudocode in Figure 5-2 for a concise description of this method. The outer loop of the script increases w incrementally and the next loop increases s . n has been chosen as the inner loop parameter because of its dramatic impact on inductance compared to the other parameters. For each set of parameters, *ASITIC*'s `pi` command is used for preliminary analysis. The command produces a simple Π equivalent circuit model by generating a 2-port circuit model for each segment of the inductor, connecting the models together, and reducing the resulting distributed circuit model in a manner similar to that of the study in [16]. The resulting modeled

```

for w = min_w to max_w {
  for s = min_s to max_s {
    while L < L_lower_bound {
      Increment n
      Quickly analyze spirals with (w,s,n)
    }

    while L < L_upper_bound {
      Accurately analyze spirals with (w,s,n)
      Increment n
    }
  }
}

```

Figure 5-2: Pseudocode describing the method used to search the design space

inductance is compared with the lower bound provided by the design specifications and tolerances. The calculation is repeated for increasing n until the calculated value reaches or exceeds the smallest possible matching inductance. The method of analysis is adjusted at this point because extensive testing of the `pi` command verified its results as a consistent overestimate for inductance compared to more accurate simulation techniques. By using the `pi` command initially, smaller inductances can be quickly pared away from the design space without expensive simulation.

The next step of the algorithm is the use of *ASITIC*'s `pix` command to analyze the smallest matching spiral according to `pi` calculations. The `pix` command automatically segments the inductor into small filament sizes based on a fraction of the skin depth and the wavelength at the frequency of operation. It calculates and solves partial inductance and capacitance matrices at a given frequency based on the filaments and produces a Π equivalent circuit model. The modeled inductance value resulting from the simulation is compared to the target value, and both electrical and physical parameters are recorded if a match occurs. n is incremented, and `pix` analyses are run until the calculated inductance increases beyond the specified tolerance to the target inductance or until no additional area is available to increase n .

It is worthwhile to note that the approach described above will find all matching inductors within the range specified because all devices potentially within the toler-

ance bounds for specified inductance are analyzed by the more accurate command, `pix`. Any devices with less turns than the smallest analyzed device are verified as not meeting inductance criteria by `pi`, and any devices with more turns than the largest analyzed device are guaranteed to exhibit greater inductance than the upper bound criteria (since inductance increases monotonically with n).

Following the exhaustion of all possible n for a given s and w , s is incremented and the process begins again. Once a specified maximum value of s is exceeded, w is incremented in the outer loop and the iterative process starts over with minimum values for s and n . The search ends when a maximum w is reached.

The search algorithm presented here is a brute-force implementation designed to cover the entire design space and guarantee an optimal solution. The influence of parameters discussed in Chapter 3 as well as closed-form and optimization techniques mentioned in the previous section could be used to guide the search more efficiently. Alternatively, other approaches to varying the parameters such as fixing s to minimum dimensions and searching the resulting space of w , n , and inductor area could be used². The most significant advantage provided by the external script approach is its flexibility in designing and specifying custom searches for a desired application.

5.4 Quality vs. Cost

As described in Chapter 2, the quality factor of inductors can be complicated due to widely varying definitions and meanings for this parameters. Still, in almost any form quality factor provides a useful indication of an inductor's performance, whether it specifically relates to impedance, frequency selectivity, or phase stability. For this reason, designers often desire the highest quality factor possible within some constraint, usually cost-related. For integrated inductors, cost translates into area consumed by a layout. Figure 5-3 shows data from several thousand simulations performed by the

²It is important to note that the approach taken should reflect the realities of the fabrication process to be used (using reasonable increments for w and s , for example) and should allow small variations in inductance to be achieved as parameters are swept (to increase the likelihood of matching a given tolerance and value).

script described above to study the relationship between cost and available quality factor.

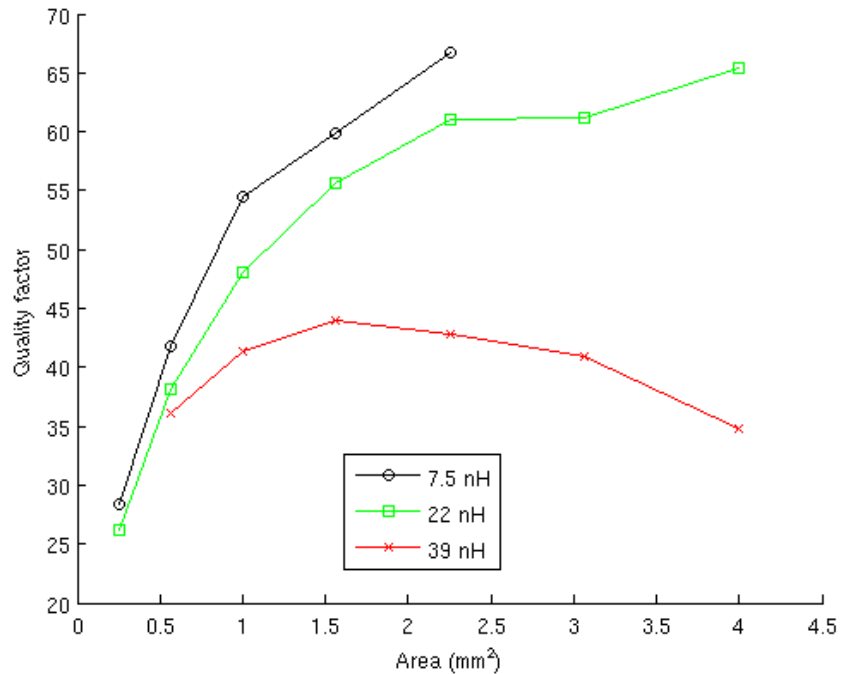


Figure 5-3: Available quality vs. cost for several inductors at 1GHz

Before discussing its results, it is first important to note the definition of area used to generate Figure 5-3. For a given area, the inductors are specified to fill the entire area. For the data shown at 1mm^2 , all inductors in the design search contained a $1\text{mm} \times 1\text{mm}$ outermost loop. This is a distinct from a search that includes inductors of any size less than or equal to 1mm^2 .

The general trend of the figure, as expected, is that an increase in cost (measured by an increase in the area consumed by an inductor) leads to the availability of a higher quality factor. It is also clear, though, that increasing costs yield a diminishing margin of return in quality. This is because the quality factor of inductors can only be increased finitely. As the area is increased, designs can make use of increased conductor width to decrease series resistance, but the increased width eventually causes significant additional parasitic capacitance to nearby grounded structures. Additionally, the inner radius of a spiral can be increased to reduce the current crowding

experienced by inner turns due to proximity effect, but the resulting larger area increases the overall conductor length and causes higher series resistance. The device is physically limited to gains in quality factor by parasitic effects.

A point of interest from the figure is the observation that at some area, inductors matching the criteria can no longer be found within the design space. This phenomenon results from an upper bound on the loop size that can realize a given inductance. As the area that an inductor must occupy increases, the design reaches a point at which a single loop inductor ($n = 1$) produces more inductance than the target value, and no inductors can be found at that area. The resolution with which the layout parameters are incremented in the search can also limit whether inductances are found at a given area.

Another trend in the data that calls for explanation is the decrease in available quality factor for 39nH inductors as area is increased above 1.5mm². This decrease results from the influence of self-resonance. The simulated resonant frequency of the 39nH inductors is near the simulation frequency of 1GHz. For the smaller devices, it is near 2GHz, but as the area that the inductor must occupy increases, the resonant frequency decreases due to the increased capacitive effects of a physically larger inductor. The resonant frequency approaches the frequency of simulation (1GHz), resulting in much lower quality factors exhibited in the devices (since the quality factor at resonance is 0 as explained in Chapter 2).

The complexities introduced by resonance, while initially confusing, are a direct result of the physical behavior of inductors. Through the figure, they indicate that smaller designs can yield better quality factor when devices are operating near resonance. For its clarity in capturing and presenting this phenomena along with other affects of area on quality factor, Figure 5-3 can be a important tool for designers. It provides a useful guideline on how cost (area) and quality factor can be traded off by a designer.

Chapter 6

MCM-D Verification

This chapter describes the fabrication of integrated spiral inductors in the Draper MCM-D process. Details of the fabrication and measurement are explained, and the measurements of fabricated devices are compared with theory.

6.1 Design preparation

In order to verify the design methodology introduced in the last chapter, an MCM-D module containing several spiral inductors was fabricated and tested. A range of inductance values that might be encountered in a typical RF module was selected for the experiment. Within that range, the available area budget was varied to evaluate the effect of cost on quality factor. Additionally, the separation distance from an inductor to its surrounding co-planar ground structure was varied to study the significance of eddy current losses to ground.

The design goals of 7.5nH, 22nH, and 39nH inductors of varying area were first simulated and optimized using the design methodology from the previous chapter. A 2-port ground-signal-ground (GSG) configuration was chosen for the inductor test structure to allow for a more accurate de-embedding of the capacitances generated by the output pads than that of a signal-ground (SG) approach [20]. Due to the large spacing between the two GSG ports, capacitive coupling effects between the input and output pads are significantly reduced. The measured open-circuit y -parameters of the

calibration structure can simply be subtracted from the inductor's y -parameters to de-embed pad-to-ground capacitance¹.

To ensure a common ground for both GSG probes and to provide a path for return ground currents, a $125\mu\text{m}$ -wide co-planar ground ring was placed around each inductor at a distance² of $200\mu\text{m}$. Figure 6-1 shows the layout of both a typical spiral in the design (a) and an open-circuit calibration structure (b). Note that in the spiral layout shown, $n = k + 0.75$, where k is an integer. This unusual fractional number of turns is used to provide ample separation between the input and output ports. In order for the structure to exhibit a physical inductance, however, a return path must exist to close the inductance loop between the two ports. This return path usually resides in the closest grounded structure (in this case the ground ring). For inductors designed to connect to other integrated parts (i.e. in applications where a GSG output pad structure isn't necessary), it would be more prudent to use a whole number value for n in order to reduce the distance between the input and output of the device and consequently reduce the unpredictable effects of a long return path.

Nine inductor layouts were chosen for fabrication, plus four open-circuit calibration structures. Each layout was prepared using CAD tools, and several test structures for in-process measurements were added to the overall design. Photolithographic masks and laser drilling instructions were produced for fabrication in the process described below.

6.2 Fabrication process

The MCM-D process at Draper uses deposited and patterned metal interconnect to package several bare silicon dice with very high density. The process is chips-first—meaning that the dice are placed initially, then the interconnect is aligned to them (as opposed to a chips-last process in which metal interconnection is placed first,

¹This capacitance turns out to be very small in the measured devices due to the large distance ($375\mu\text{m}$) between signal and ground pads. The technique would be more useful for smaller pad pitches.

²This distance was adjusted for designs included to study the effect of varied spacing to ground.

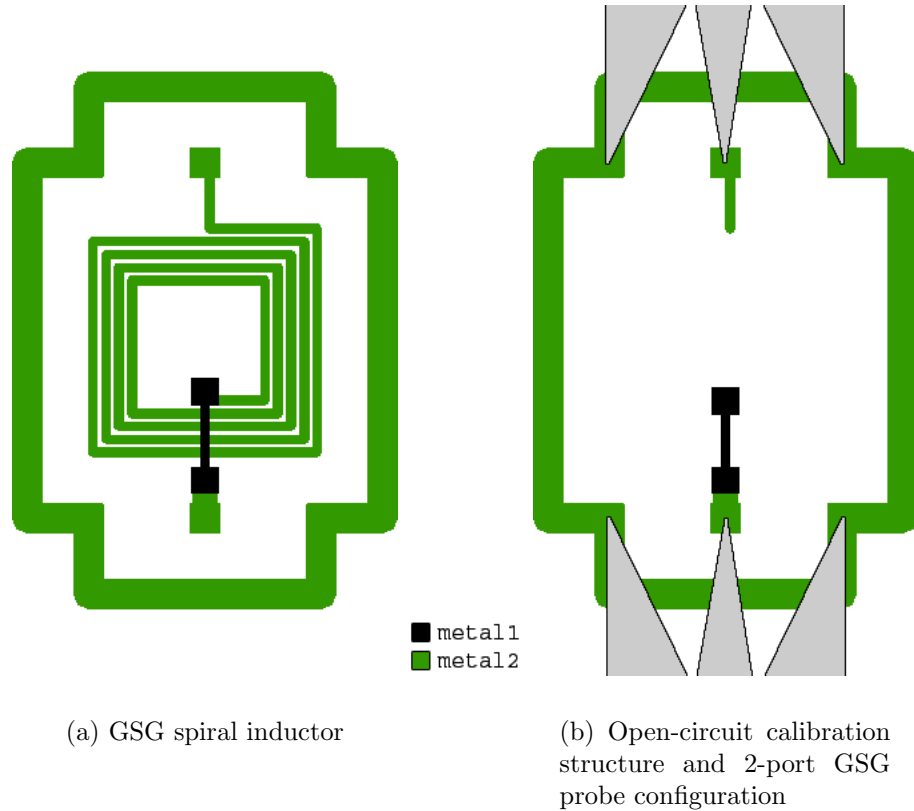


Figure 6-1: Typical inductor layouts used in the design

after which dice are aligned and placed). The chips-first idea allows highly accurate placement of metallization directly onto the die pads, rather than connection using solder bumps (as in chips-last).

The first step of the Draper MCM-D process (which is summarized in Figure 6-2 [15]) is the mechanical thinning of the dice. This thinning reduces the height of all components to 6 mils, thereby reducing the overall height of the module significantly (an important accomplishment for applications with extremely demanding size requirements). Additionally, the thinning allows dice of different thicknesses to be integrated into a single planar layer. The thinned dice are placed on a stiff non-conductive substrate with adhesive to prevent movement. A “window frame” is prepared from a polyimide layer, with space cut out for each component in the die layer [15]. The thickness of this frame (or “spacer”) is matched to the thickness of the dice to provide a planar surface across the module once the spacer is bonded



Figure 6-2: Diagram of Draper MCM-D process [15]

to the substrate. After bonding the spacer, the first layer of polyimide dielectric is laminated to the module. Vias are drilled through the dielectric to the underlying metal contacts using pulsed laser ablation [15]. The laser has little selectivity for the polyimide over the underlying metal pads, so its power must be carefully controlled. Once the underlying layer is reached, the module is plasma cleaned to remove any waste material left from the laser ablation.

In the next sequence of the process flow, the metal layer is formed. A 1000\AA Ti interfacial/barrier layer is first sputter-deposited, followed by a 2000\AA Cu seed layer. Cu is then electroplated to the desired thickness, followed by another sputter-deposited 2000\AA Ti layer [15]. This combination allows a high-conductance (due to Cu) and uniformly thick (due to electroplating) metal layer that will readily adhere to many metal and dielectric surfaces (due to Ti).

Following metal deposition, photoresistive chemicals are deposited and lithographically patterned in a manner similar to a standard CMOS front-end process flow. Again in the standard CMOS process vein, the unwanted photoresist and metal are chemically etched, and the masking photoresist is removed. A patterned metal layer

remains on the module surface. The lithography and chemical etch processes enable the metal to be patterned with a very fine resolution and a large aspect ratio, allowing the high density of interconnect required to integrate several high-output dice in a small area.

The dielectric lamination, via drilling and cleaning, metal deposition, patterning and etching steps are then repeated for as many metallization layers as desired for the module [15]. Finally a passivation layer of dielectric is placed and a ball-grid array of solder bumps is deposited to maximize the number of outputs available from the module. For board-level packaging, a module may be flip-chip bonded to a printed circuit board or other interface, then protected by an underfilling encapsulant.

The inductors in this study were fabricated using two layers of $5\mu\text{m}$ -thick Cu. The specific materials used in their fabrication are approximately characterized in Table 6.1. An optical photograph of the inductor region of the completed module is shown in Figure 6-3.

| | | | | |
|--------------|---------------------------------------|-----------------------|--|------------------|
| Metal 2 | Copper | $t = 5\mu\text{m}$ | $\sigma = 3.4 \text{ m}\Omega/\square$ | |
| Dielectric 2 | R/flex [®] 1000 ¹ | $t = 25\mu\text{m}$ | $\rho = 1.5 \times 10^{17} \Omega\text{-cm}$ | $\epsilon = 3.4$ |
| Metal 1 | Copper | $t = 5\mu\text{m}$ | $\sigma = 3.4 \text{ m}\Omega/\square$ | |
| Dielectric 1 | R/flex [®] 1000 ¹ | $t = 150\mu\text{m}$ | $\rho = 1.0 \times 10^{17} \Omega\text{-cm}$ | $\epsilon = 3.5$ |
| Substrate | 96% Alumina | $t = 25 \text{ mils}$ | $\rho = 1.0 \times 10^{14} \Omega\text{-cm}$ | $\epsilon = 9.9$ |

Table 6.1: Approximate MCM-D process parameters for this study

6.3 Electrical analysis

6.3.1 Measurement setup

The completed modules were measured using an Agilent E8363B PNA Series Network Analyzer. 40A-GSG-500 Picoprobes from GGB Industries, Inc. with $500\mu\text{m}$ pitch

¹R/flex[®] 1000 flexible circuit material is a registered trademark of Rogers Corp. The laminate dielectric material used in this study between the metal layers consists of 0.5 mil thick Kapton[®] HN (a registered trademark of DuPont) polyimide film and 0.5 mil thick thermosetting phenolic butyral adhesive. The laminate above the substrate layer consists of 5 mils thick Kapton[®] and 1 mil thick adhesive.

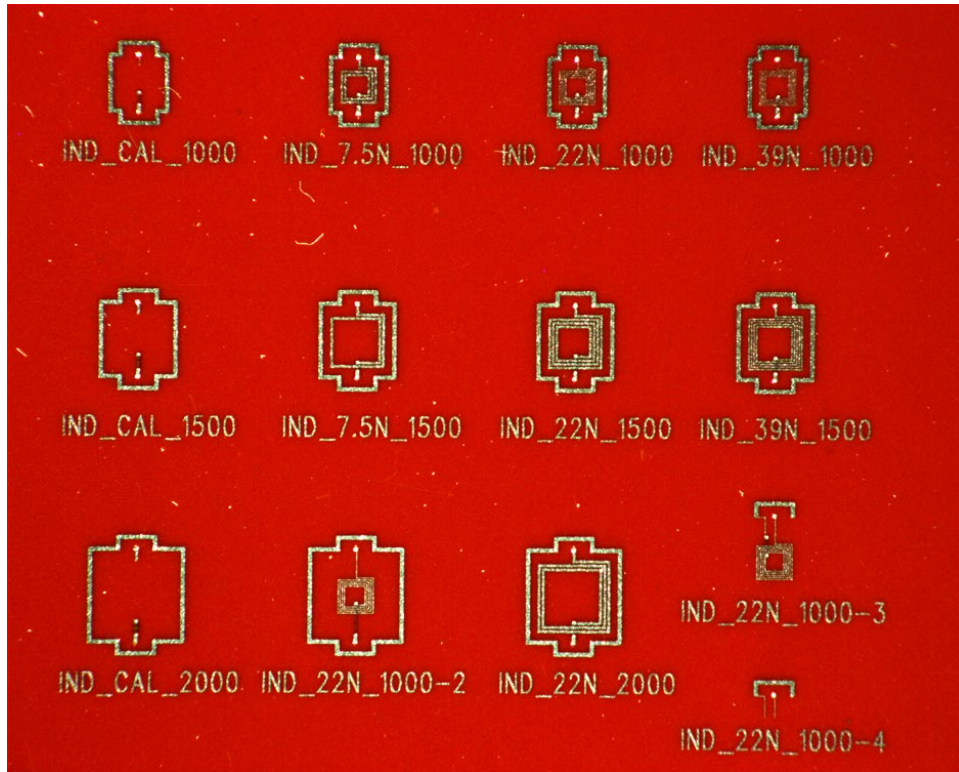


Figure 6-3: Photograph showing fabricated inductors

for $125\mu\text{m}$ capture pads were used with a Cascade Microtech Analytical and High Frequency Wafer Probe Station. Shielded cables with 50Ω characteristic impedance were connected from the analyzer to the probe station. The probes were initially calibrated using an Open, Short, Load, Through (OSLT) calibration procedure on a CS-9 Calibration Substrate from GGB Industries, Inc. to de-embed the test setup equipment (probes, cables, etc.) from the measurements.

For all 2-port measurements, the GSG input probe was connected to the top of the device as oriented in Figure 6-1, and the output probe was connected to the bottom. With this configuration, the 2-port characteristics of the devices could be measured from each input port to a common ground. This 2-port technique allows for easier extraction of equivalent circuit parameters than a 1-port measurement (see Chapter 4 for more information about equivalent circuit extraction). The network analyzer measured the 2-port s -parameters of each device over the range of 10MHz to 10GHz. The frequency of measurement was swept linearly over this range in

increments of approximately 6.25MHz, and 10 measurements were taken and averaged at each frequency point to provide greater measurement stability.

Measurements using the enabled options and power settings on the Agilent E8363B Network Analyzer are accurate to within 0.2dB of magnitude and 1.3° of phase. The accurate correlation of the measurements to a particular device’s behavior, however, is determined by the accuracy of the calibration procedure. While highly accurate standards can be used to de-embed the effects of test equipment from the measurements, errors are commonly introduced during the calibration procedure by failing to establish adequate contact between the probes and the standards or by using incorrect spacing between probes for certain ”through” calibration standards. It is important to calibrate the test equipment carefully and to verify the measurements of calibration standards in order to obtain accurate device measurements.

6.3.2 Results

The resulting measurements were saved electronically and analyzed using MATLAB^{®4} software. In the discussion of simulation and measurement data that follows, s -parameters are converted to y -parameters using the following equations [32]:

$$y_{11} = \frac{1}{Z_0} \frac{(1 + s_{22})(1 - s_{11}) + s_{12}s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} \quad (6.1a)$$

$$y_{12} = \frac{1}{Z_0} \frac{-2s_{12}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} \quad (6.1b)$$

$$y_{21} = \frac{1}{Z_0} \frac{-2s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} \quad (6.1c)$$

$$y_{22} = \frac{1}{Z_0} \frac{(1 + s_{11})(1 - s_{22}) + s_{12}s_{21}}{(1 + s_{11})(1 + s_{22}) - s_{12}s_{21}} \quad (6.1d)$$

From these y -parameters, values for quality factor and equivalent circuit models are extracted from the data as discussed in Chapters 2 and 4, respectively.

While s -parameter to y -parameter conversion allows for easy extraction of circuit information, one considerable drawback of this approach is its sensitivity to errors. Consider the y_{11} parameter, which is used to calculate quality factor. If each

⁴MATLAB[®] is a registered trademark of The MathWorks, Inc.

s -parameter in Equation (6.1a) is varied, the resulting real part of y_{11} can vary enormously. For instance, when varying the measured s -parameter data from a 22nH inductor at 1GHz by only 5 percent, the converted value of $\text{Re}(y_{11})$ was found to vary by over 300 percent—an amount that would certainly affect the calculated quality factor. This wide variation results from the influence of the imaginary parts of two complex numbers on the real part of their product. As an example, consider the error term introduced to the numerator of Equation (6.1a) by the $s_{12}s_{21}$ term. Using the assumption that $s_{12} \approx s_{21}$, the error term introduced by setting $s'_{21} = s_{21}(1 \pm \epsilon)$ is approximately $\Delta \approx \pm 2\epsilon s_{21}^2$. Now assume that $s_{21} = a - jb$, a generalized complex transmission coefficient. The real part of the $s_{12}s_{21}$ error term becomes $\text{Re}(\Delta) = \pm 2\epsilon(a^2 + b^2)$. In the case of an integrated inductor, where imaginary admittances are much larger than real admittances (i.e. the accumulation of 'b' values can be two orders of magnitude larger than the accumulation of 'a' values in the overall y_{11} expression), the associated real error can explode in magnitude due to terms similar to b^2 . Since this phenomenon can translate very small variations in s -parameters to large variations in y_{11} , values of quality factor derived from y_{11} can suffer from significant "noise" and questionable accuracy. It would be much more effective to measure quality factor data using other means as discussed in Chapter 2, but measurement configurations such as external resonant systems were not available in this work.

Figure 6-4 shows both the measured and simulated s -parameter data for a "7.5nH," 1mm² spiral inductor. The device's inductance measures approximately 8.5nH. This value differs from the target of 7.5nH due to variations in simulation parameters unknown at the time of design. One such variation of particular significance is that of conductor width as discussed in Section 6.4. The fabricated conductor width varies by 10–15 μ m from the specified width in every design. The actual width was measured for each device, and the measured values were used in the simulation data shown. As can be seen in the figures, the simulated s -parameter data⁵ are in reasonable agreement with measurements. In fact, the accuracy is within 3 percent at all frequencies

⁵ s_{12} is omitted from the data presented because it is nearly identical to s_{21} .

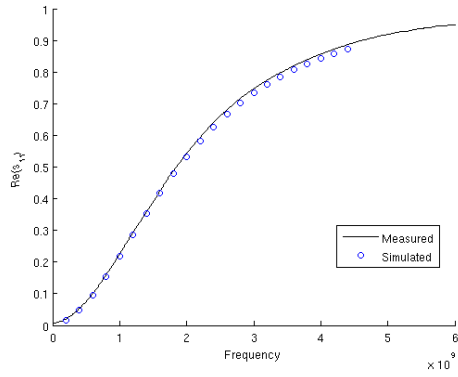
except those where an s -parameter approaches zero. In this case, the discrepancy between simulation and measurement jumps to around 10 percent or more due to the small denominator in the error term near zero.

After conversion of both measured and simulated data from s -parameters to an equivalent inductance and quality factor, the data compares as shown in Figure 6-5. The discrepancy increases noticeably between measurement and simulation because the error terms are amplified by the conversion equations as explained above. Still, the simulated data for this device are within 5 percent of the measured inductance data and within 30 percent of the measured quality factor data.

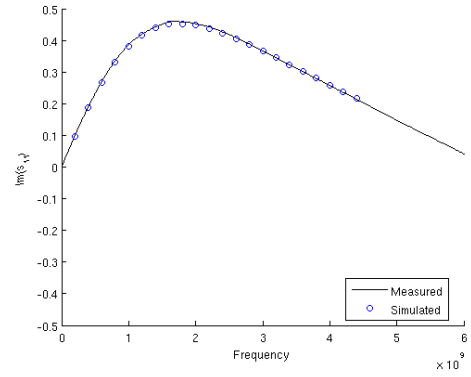
A notable trend within the inductance data is an increasing discrepancy between measured and simulated values with increasing frequency. This trend is caused by the grounded ring surrounding the inductor. The *ASITIC* simulation software does not account for the nearby grounded structure when formulating its partial inductance matrix [19], but the structure does affect the magnetic fields creating inductance. Thus, the effect of increasing inductance as the system approaches resonance is completely absent from the simulation.

Even though it is affected by the data conversion errors discussed, the "7.5nH" simulation presented above largely agrees with measurement. Some other measurements, however, yielded significantly worse quality factor data than expected. Figures 6-6 and 6-7 show the s -parameter, inductance, and quality factor data for the device exhibiting the largest discrepancy in quality factor, a "22nH" spiral measuring 1mm². Again, the s -parameter data is in reasonable agreement, though slightly larger discrepancies are observed than those in the previous inductor along with some small oscillations. The simulated inductance of approximately 25nH also matches the measurements fairly well. The measured quality factor, on the other hand, is much lower than that of simulation data, with the values varying by as much as a factor of 3 near their peaks.

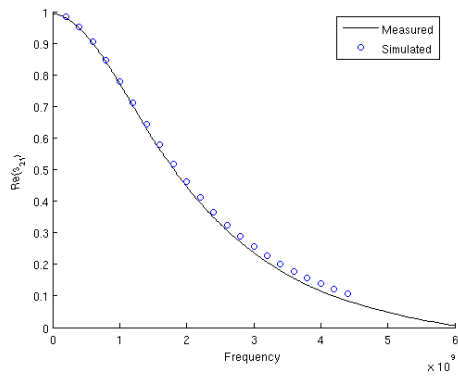
Though conversion errors likely play a role in the discrepancy between measured and predicted quality factor in this situation, it is believed that the nearby ground ring surrounding the inductor plays a larger role. The simulations in *ASITIC* were pre-



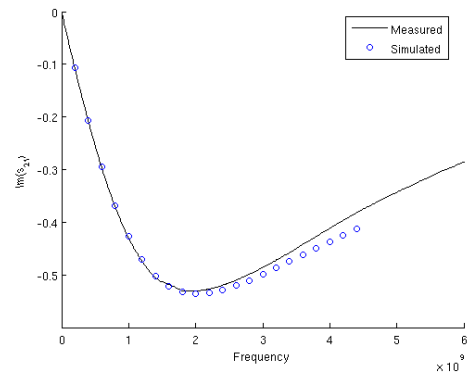
(a) Real part of s_{11}



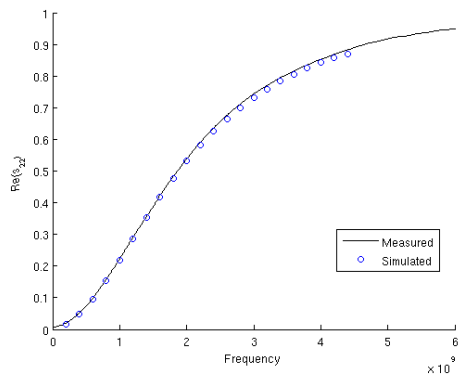
(b) Imaginary part of s_{11}



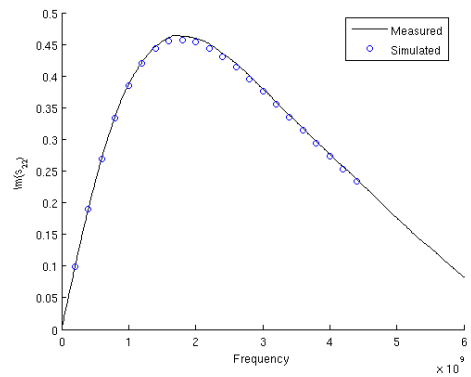
(c) Real part of s_{21}



(d) Imaginary part of s_{21}

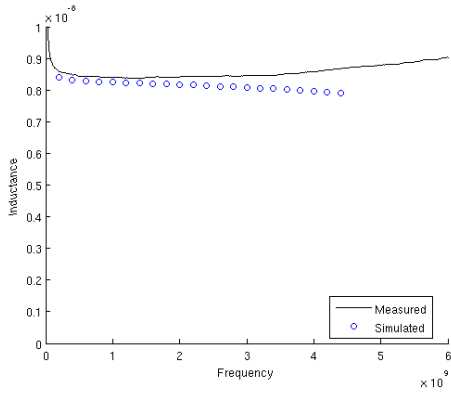


(e) Real part of s_{22}

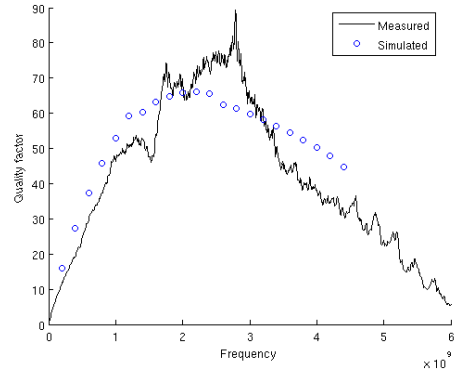


(f) Imaginary part of s_{22}

Figure 6-4: Measured and simulated s -parameters for a 7.5nH device



(a) Inductance data. Self-resonance effects are not included in simulations.

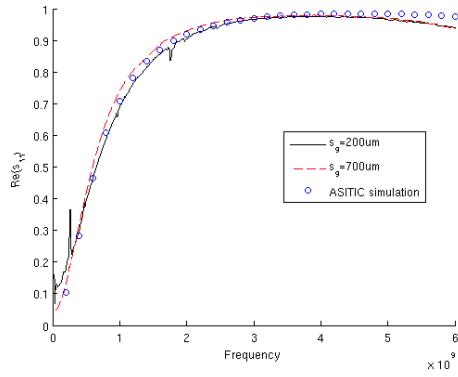


(b) Quality factor data. Calculated quality factor can exhibit significant errors due to translation between s - and y -parameters.

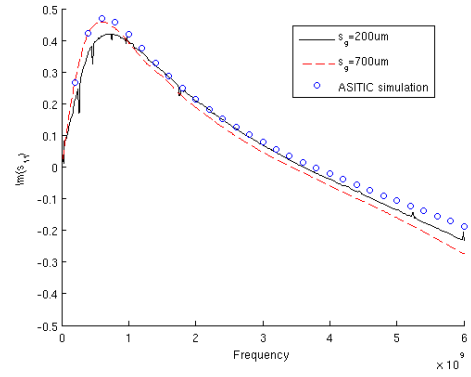
Figure 6-5: Calculated inductance and quality factor for a 7.5nH device

pared using a grounded 1-turn spiral to model the effect of this ground ring. As mentioned above, however, the analysis accounts only for the effect of a specified ground structure in the capacitance calculations, not in the inductance calculations [19]. This feature of *ASITIC* enables fast simulations that can model the effects of a patterned ground shield on a structure’s parasitic capacitances without requiring detailed information about a pattern within the shield. Unfortunately, for the purposes of this simulation, the feature led to an overly optimistic prediction of quality factor in the presence of a nearby ground ring. The disparity is much more dramatic than that observed in the ”7.5nH” inductor because the effect of neglecting ground currents in the partial inductance matrix of the ”22nH” device is much more significant (due to both an increased number of turns and a lower self-resonant frequency). The disparity between simulation and physical behavior was not noticed before the design and fabrication of the module used in this thesis, so a majority of the inductors were designed with small s_g and their losses are accordingly large.

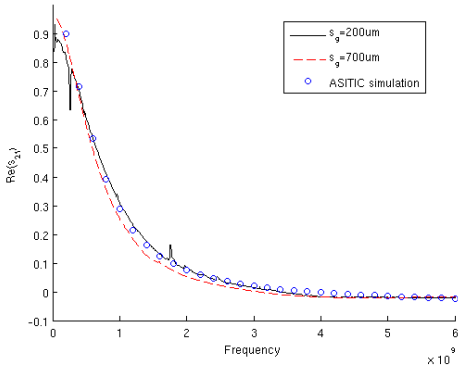
Figures 6-6 and 6-7 also present data measured from the same spiral inductor geometry with a larger distance to the surrounding ground ring, $s_g = 700\mu\text{m}$ (recall that the other devices have $s_g = 200\mu\text{m}$). The measured inductance of this device



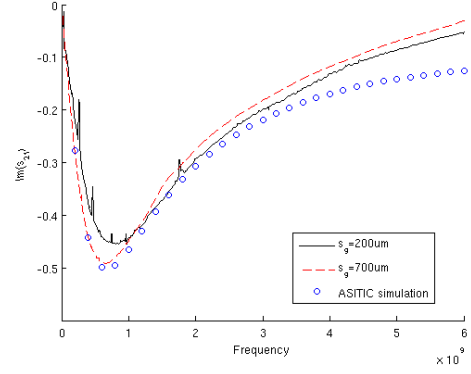
(a) Real part of s_{11}



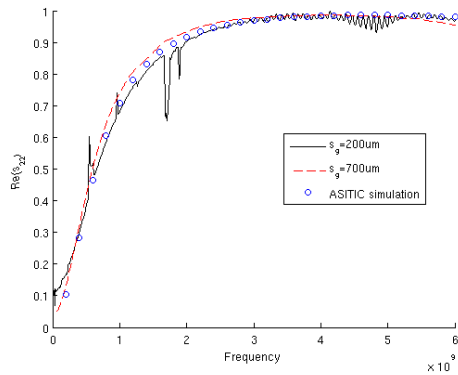
(b) Imaginary part of s_{11}



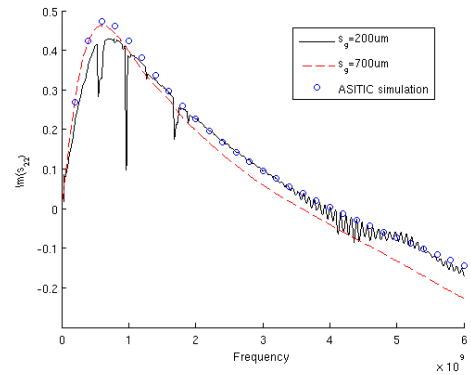
(c) Real part of s_{21}



(d) Imaginary part of s_{21}

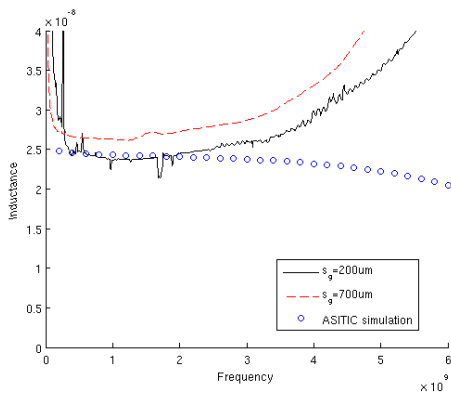


(e) Real part of s_{22}

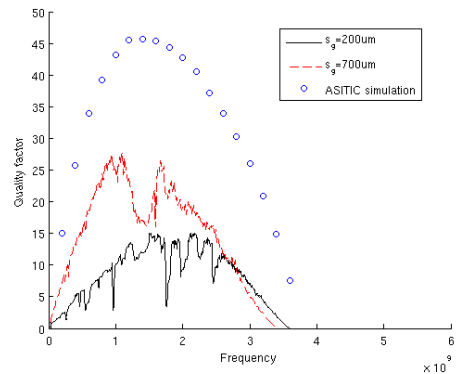


(f) Imaginary part of s_{22}

Figure 6-6: Measured and simulated s -parameters for a 22nH device



(a) Inductance data. Self-resonance effects are not included in simulations.



(b) Quality factor data. Calculated quality factor can exhibit significant errors due to translation between s - and y -parameters.

Figure 6-7: Effect of spacing to ground on inductance and quality factor

is higher because of the additional $500\mu\text{m}$ metal lines required to connect the spiral to the both the input pad and the output pad. The increase in the device's calculated quality factor, however, is likely a result of the increase in s_g . The new device experiences smaller eddy current losses to ground than the original device because the grounded structure is much further away. This comparison shows that s_g was originally underestimated as a factor in design. It is now understood that s_g should be made large in order to obtain higher quality factors.

Another possible contribution to the observed disparities in real impedance and quality factor is that of surface roughness. As discussed in Chapter 3, the skin effect causes most of the current in a conductor to flow near the metal surface at high frequencies. When this surface is roughened by chemical etching, the effective cross-sectional area for current flowing near the surface is reduced, resulting in a higher resistance at high frequencies and a correspondingly lower quality factor. *ASITIC* does not have a mechanism for including the effect of surface roughness in a device, so the simulation data does not reflect the lower quality factor brought about by chemically etching the metal layers in the fabrication process.

Closer inspection of the measurement data presented thus far reveals several ques-

tionable features. The first feature is that at low frequencies, the inductance data approaches infinity rather than the finite DC inductance of the device. This results from discrepancies in the measured s -parameter data. In particular, the forward transmission coefficient does not reach the ideal value of $s_{21} = 1 + j0$ at low frequencies. This is because the measurement system, however well-calibrated, will always experience some transmission loss through the inductor since it is not a perfect short. The drastic nature of the increase observed is related to the sensitivity to error of the inductance expression. Frequencies in the 10MHz range require a very high admittance to produce a reasonable inductance. Even small transmission losses can reduce the calculated admittance and produce the observed asymptotic effect in low frequency inductance. The DC inductance of the device can be interpolated from the measured inductance at slightly higher frequencies, such as 400MHz.

Another curious effect observed in the measurements is that of sharp discontinuities in some s -parameter and quality factor data. These discontinuities are present in the real part of calculated y_{11} data but not in the imaginary part. This implies that their presence is not the result of a resonance, which would cause a sudden change in imaginary admittance. The discontinuities instead occur because the real admittance of the device suddenly increases at some frequencies, which is likely an artifact of RF interference passing through the device.

A final observation based on the measurement data is the existence of a large discontinuity in quality factor between approximately 1GHz and 1.7GHz. Figure 6-8 shows differing intensities of this effect over the same frequency range for most of the devices fabricated. The precise cause of this effect is unknown, though it is unlikely that the effect is related to a resonance due to its uniformity over different inductances and conductor spacings. It is more likely that the effect is related to the probe station test setup, which remains constant for each measurement. The calibration routine may not have accurately de-embedded the effects of the probes and cables over this frequency range due to an error in one of the calibration standard measurements.

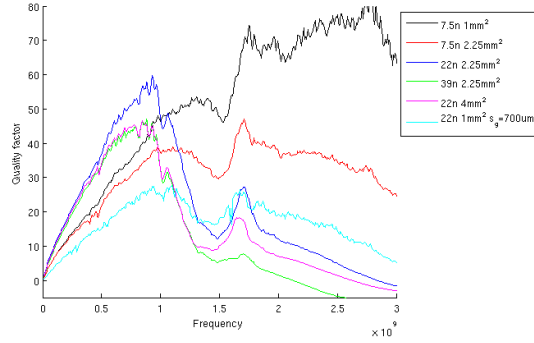


Figure 6-8: Discontinuity in quality factor of several devices from 1–1.7GHz

6.4 Physical analysis

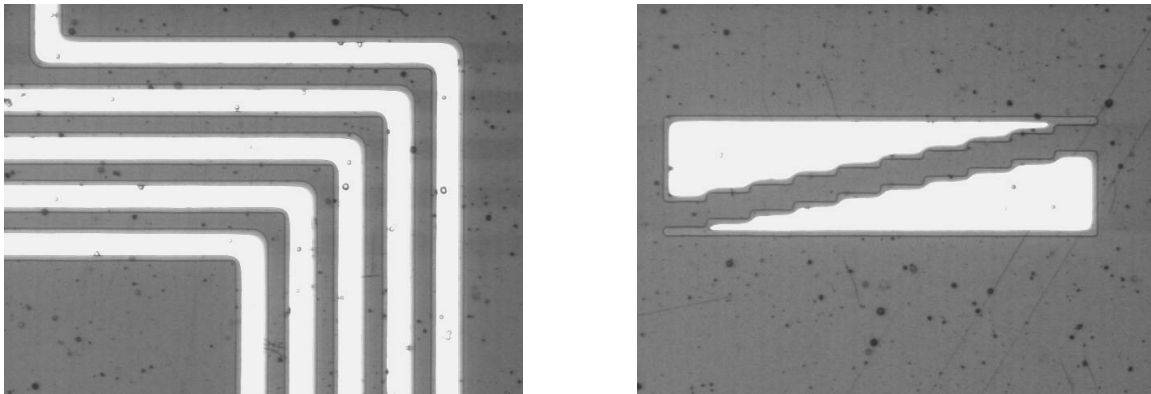
6.4.1 Measurement setup

After fabrication, physical characteristics of the module were thoroughly investigated. Optical microscopes were used to inspect both the photolithographic masks and the module itself. The width of conductors making up each device on the module was measured using a Nikon VMR-3020 metrology tool. This tool uses a camera to view device features at high magnification and uses software that automatically detects sharp contrasts (denoting metal edges) in the visible image. Measurements using the Nikon tool are accurate to within $2.5\mu\text{m}$.

The metal layer thickness was also measured using a Veeco Metrology Group Dektak³ST Surface Profiler. The Dektak tool puts a small stylus in contact with the surface of a device and gently drags the stylus across the surface. The vertical displacement of the stylus is measured in order to calculate the surface profile of the device. The measured profile height is repeatable within 10\AA . The profile was measured in multiple locations on the surface to determine the approximate thickness of the metal layers.

6.4.2 Results

The photomasks were found to be very accurately produced to specification (within the measurement accuracy of the Nikon tool). A severe disparity was observed, however, between the specified conductor widths and those measured on the fabricated devices. Figure 6-10 shows the average⁶ measured width of each device plotted against the specified width (this data is also presented in Table 6.2). The data should ideally lie on the 45° line shown. Clearly the fabricated conductor width of every device falls short of the specified width by approximately 10–15 μm . The most likely reason for this trend is that the metal was over-etched (chemically or reactively etched for a long enough period of time that the exposed metal sidewalls beneath the masking photoresist began to be etched). Figure 6-9(a) shows an example of the over-etched metal. The white lines are the metal traces of a spiral inductor, while the faint darker outlines show the width to which the metal should extend.



(a) Over-etched spiral inductor

(b) Over-etched test structure

Figure 6-9: Fabricated features exhibiting over-etched metal

Several test structures were also included on the module to study how well the line width could be controlled in the process. The goal of the structures was to determine how finely the width and spacing parameters should be incremented in the script presented in Chapter 5. Figure 6-9(b) shows one of the structures that

⁶While the data presented is average, the standard deviation of all observed data was very small—less than 1 μm .

was designed to incrementally increase in width. The structure shown was designed to exhibit $10\mu\text{m}$ increments in width after every $50\mu\text{m}$ of length. The over-etch has considerably distorted the structure from its designed specifications.

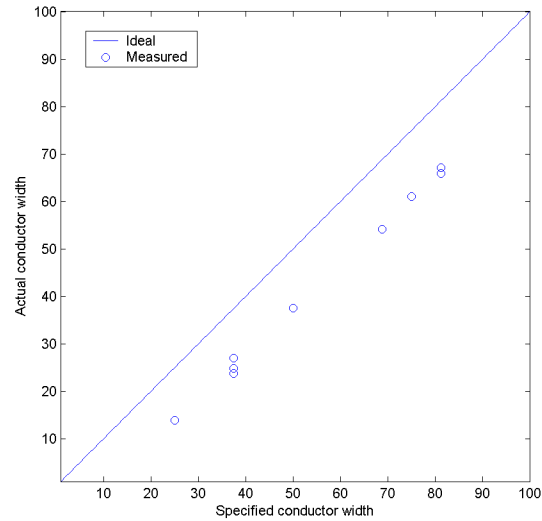


Figure 6-10: Specified vs. measured conductor width

| Target Inductance (nH) | Area (mm^2) | Specified w (μm) | Measured w (μm) |
|------------------------|------------------------|---------------------------------|--------------------------------|
| 7.5 | 1 | 68.75 | 54.1 |
| 7.5 | 2.25 | 81.25 | 65.9 |
| 22 | 1 | 37.50 | 27.0 |
| 22 | 1 | 37.50 | 23.7 |
| 22 | 1 | 37.50 | 24.9 |
| 22 | 2.25 | 75.00 | 61.1 |
| 22 | 4 | 81.25 | 67.1 |
| 39 | 1 | 25.00 | 13.9 |
| 39 | 2.25 | 50.00 | 37.6 |

Table 6.2: Specified vs. measured conductor width

Line width control is very important to spiral inductor design. While the line width can vary over a small range and produce a consistent inductance (as long as the pitch—width plus spacing—is kept fixed), the quality factor of a device can decrease significantly for decreased line widths (see Chapter 3 for more information). In light of the poor line width control demonstrated in this sample, it is suggested

that further study be devoted to characterizing and improving line width control in the Draper process.

The metal thickness was also measured on both Cu layers to vary between $5\text{--}6\mu\text{m}$ across the surface of the device. In a chemically etched process, the metal thickness of a particular trace can vary due to its width and length as well as due to the proximity of other metal features. In a spiral inductor where many microstrips are in close proximity, metal thickness is typically consistent.

Chapter 7

Conclusions

7.1 Accomplishments

This thesis presented a study on the design and fabrication of on-package integrated inductors. It began with an explanation of the background and the fundamental principles of designing and quantifying these devices. It then briefly explained existing techniques that can be used to simulate their characteristics and introduced a new methodology for designing spiral inductors. Finally, it presented experimental results from inductors fabricated in the Draper MCM-D process.

The new design methodology developed in Chapter 5 allows for flexible and efficient searching of a design space using existing simulation software. The design space is specified using electrical parameters, such as inductance, area, and frequency of operation, rather than the geometrical parameters required by most existing design tools. This fundamental change in the focus of how inductors are designed allows RF designers to work with familiar concepts instead of forcing them to learn and understand the physical principles of integrated inductor design and simulation.

The inductor fabrication undertaken in Chapter 6 compares the simulation of integrated inductors with experimental measurements. Through this comparison, several factors affecting the accuracy of device simulation and measurement are identified. In particular, discrepancies between measured and simulated quality factor data are observed in some measurements due to (1) the error amplification associated with

conversion from s -parameters to y -parameters, (2) the simulator's failure to account for all of the effects of a nearby co-planar grounded structure, and (3) the metal surface roughness introduced by chemical and reactive etching. From this information, it is concluded that quality factor data should be measured using different methods if possible and that the spacing to ground, s_g , of future designs should be increased and accounted for in simulation.

The devices from this experiment were also physically characterized, and it was found that a large amount of over-etching occurs during fabrication. Because the electrical characteristics of the devices can be significantly altered by the over-etching, it is concluded that the process line width control must be further characterized to permit the accurate design of spiral inductors.

The overall results in both the design of inductors and the influence of fabrication parameters have made significant progress in developing on-package integrated inductors for use in the Draper MCM-D process. As described below, further study is required for on-package integrated inductors to replace the on-chip and surface-mount inductors currently utilized in the process.

7.2 Future work

Several ideas were generated by this work that were not pursued due to both resource and time constraints. In particular, the experimental results exhibited some discrepancies with simulation, and progress could be made in making both the prediction and the measurement of inductor behavior more accurate.

For instance, the s -parameters measured from the devices are plagued with both narrow-band and wide-band discontinuities at several frequencies. Greater care could be taken to calibrate and measure the devices to alleviate the effects of RF interference and source mismatch observed in the results. Alternatively, in light of the amplification of small errors in transforming s -parameters to y -parameters, a different mechanism could be employed for measuring quality factor data. For example, a loaded quality factor based on the bandwidth or phase stability of a resonant system

could be directly measured with the introduction of an external capacitor in parallel with the device.

A large amount of work related to the development of the Draper MCM-D process can also be suggested from the results. First, additional modules could be fabricated to study the variation of both electrical and physical parameters of identical devices between fabrication batches. In particular, the effect of over-etching on line width control could be studied in detail, and the reliability of device behavior across modules could be assessed.

Accurate characterization of many materials and structures from the MCM-D process could also improve the accuracy of simulations that include material properties in their loss calculations. For example, the R/flex[®] 1000 dielectric material is a composite of a well-characterized Kapton[®] polyimide and a proprietary, largely uncharacterized adhesive. Electrical characterization of the cured R/flex[®] 1000 material would allow dielectric losses to be accounted for not only in inductor simulations, but also in a wide variety of RF package simulations.

Other material properties can have even more profound effects on simulation accuracy than dielectrics. One such property that significantly influences quality factor data is metal resistance. Variations in both the thickness and the sheet resistance of the fabricated Ti/Cu/Ti metallization layers could be studied, allowing more accurate simulation of resistive losses in the metal.

Another method of improving simulation accuracy is the introduction of additional simulation methods. The design methodology could be expanded to interface with other simulation software packages to provide alternative simulation data in the design phase. Independent verification of simulation results through several methods would increase the confidence that the simulations accurately reflect device behavior.

Finally, the design methodology introduced in this work could be significantly expanded. Apart from interfacing it with additional simulation software packages, several other approaches to searching the design space could be implemented and tested. For instance, an optimization-based approach might be able to reduce the required computational resources even further than the algorithm presented.

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Appendix A

Design Script

```
#!/usr/local/bin/perl
```

```
#####  
# usage: perl opt_ind.pl 10 1 1 #  
# # #  
# Searches a design space to find an integrated inductor with the #  
# highest possible quality factor according to specified design criteria. #  
# # #  
# ARGS are: $target_inductance in nH #  
#           $area in mm^2 #  
#           $frequency in GHz #  
# # #  
# This implementation uses ASITIC's "pi" command to quickly pare the #  
# search space and the "pix" command to accurately test potential matches. #  
# # #  
# The implementation also works around a frequent glitch discovered in #  
# ASITIC. For very wide conductors at high frequencies, ASITIC's generated #  
# partial inductance matrix is sometimes singular. In this instance, the #  
# simulation slows down significantly, often taking several hours to #  
# determine that the matrix cannot be converted. A time-out has been #  
# introduced to work around these unnecessarily slow calculations. #  
#####
```

```
use POSIX;  
use IPC::Open2;  
use File::Copy;  
use warnings;
```

```

#####
# CONFIGURATION INFO #
#####

$tekfilesize = "3000"; # chip size for simulation
$tekfile = "mcm_$tekfilesize.tek";
$logfile = "opt_ind.log";
$datafile = "opt_ind.dat";
$ASITICpath = "~/asitic/bin/";
$tolerance = 0.1;      # tolerance to which spec. params. should match
$time_out  = 900;     # time (in secs) after which calc. should time-out
$gnd_width = 200;    # width of ground ring surrounding CPW inductor
$w_min     = 12.5;   # minimum conductor width
$w_max     = 50;     # maximum conductor width
$w_step    = 6.25;   # size of increment in width search
$s_min     = 12.5;   # minimum conductor spacing
$s_max     = 50;     # maximum conductor spacing
$s_step    = 6.25;   # size of increment in spacing search

# read arguments from function call
$target_inductance = $ARGV[0];
$area = $ARGV[1];
$frequency = $ARGV[2];

# open input & output pipes to ASITIC
$pid = open2(*THEOUTPUT, *THEINPUT, $ASITICpath."asitic -t $tekfile -g" );
open STDOUT, "| tee $logfile" or die "can't write to $logfile: $!\n";
open DATA, "> $datafile" or die "can't write to $datafile: $!\n";

#####
# ANALYSIS #
#####

&wait_for_asitic(*THEINPUT,*THEOUTPUT); # wait for load
$start_time = time;
print "\n\nAnalysis started ", ctime($start_time), "\n";

# Compute coordinates of inductor and create ground ring
$length = sqrt($area) * 1000; # length in um
$spiral_coords = ($tekfilesize - $length) / 2;
$gnd_length = $length + 800;
$gnd_coords = $spiral_coords - $gnd_width - 200;
print THEINPUT "sq NAME=gnd LEN=$gnd_length W=$gnd_width S=0 N=1 " .
    "METAL=m3 EXIT=no XORG=$gnd_coords YORG=$gnd_coords\n";

```

```

# pre-condition loop with tolerances on L
$l_upper_bound = (1+$tolerance)*$target_inductance;
$l_lower_bound = (1-$tolerance)*$target_inductance;
$best_q = 0;

for ($w = $w_min; $w <= $w_max; $w = $w + $w_step) {
  for ($s = $s_min; $s <= $s_max; $s = $s + $s_step) {

    # initialize number of turns for 2-port measurement
    # and calculate the largest possible inductor for this w+s
    $n_upper_bound = floor(($length/2) / ($w+$s));
    $n = 0.75;
    $l = 0;

    # use pi to find smallest reasonable inductor
    while (($l < $l_lower_bound) and ($n < $n_upper_bound)) {
      ($l,$q) = &pi_spiral($length,$w,$s,$n,$spiral_coords,
        $frequency,*THEINPUT,*THEOUTPUT);
      $n++;
    }

    $n--; # go back to last iteration (to re-simulate it)
    $l = 0;

    # now call pix until you exceed bounds
    while (($l < $l_upper_bound) and ($n < $n_upper_bound)) {
      ($l,$q,$srf) = &pix_spiral($length,$w,$s,$n,$spiral_coords,
        $frequency,*THEINPUT,*THEOUTPUT);

      &print_and_save;
      $n++;
    }
  }
}

# Print parameters of the best inductor found by the search
$now = time;
print "\n Analysis took: ", &get_time($now - $start_time), "\n\n";
if($best_q>0) {
  print "Best match found for L=$target_inductance, Len=$length @ f=$frequency GHz:\n";
  print &format_results(0,$best_w,$best_s,$best_n,$best_l,$best_q,$best_srf), "\n\n";
} else {
  print "No match found for L=$target_inductance, Len=$length @ f=$frequency GHz.\n";
}

```

```

close DATA or die "can't close $datafile: $!";
close STDOUT or die "can't close $logfile: $!";
&wait_for_asitic(*THEINPUT,*THEOUTPUT);
print THEINPUT "exit\n";
close THEINPUT or die "can't close ASITIC input: $!";
close THEOUTPUT or die "can't close ASITIC output: $!";

#####
#   FUNCTIONS   #
#####

# make the inductor '$name' of size $length,$w,$s,$n
# use: print &make_spiral($name,$length,$w,$s,$n,$spiral_coords)
sub make_spiral {
    my ($name,$length,$w,$s,$n,$spiral_coords) = @_;
    return "sq NAME=$name LEN=$length W=$w S=$s N=$n METAL=m3 EXIT=m2 " .
        "XORG=$spiral_coords YORG=$spiral_coords CBEGIN=true CEND=true EXIT90=true\n";
}

# delete the inductor '$name'
# use: print &delete_spiral($name)
sub delete_spiral {
    my ($name) = @_;
    return "del $name\n";
}

# wait for ASITIC to finish saving, etc before exiting
# use: &wait_for_asitic(*INPUTHANDLE,*OUTPUTHANDLE)
sub wait_for_asitic {
    my ($write_fh,$read_fh) = @_;
    my $line;

    print $write_fh "ver\n"; # print the version to let us know ASITIC is done saving
    do {
        $line = <$read_fh>;
    } until $line =~ /version/;
}

# converts time in seconds to time in hour:min:sec
# use: print &get_time($time)
sub get_time {
    my ($seconds) = @_;
    my ($minutes,$hours);

    $minutes = floor($seconds / 60);

```

```

    $seconds = $seconds % 60;
    $hours    = floor($minutes / 60);
    $minutes = $minutes % 60;

    return sprintf "%2.2d:%2.2d:%2.2d", $hours, $minutes, $seconds;
}

# run PI analysis on $name [default: ind] and return L and Q
# use: ($l,$q) = &run_pi($name,$frequency,*INPUTHANDLE,*OUTPUTHANDLE);
sub run_pi {
    my ($name,$frequency,$write_fh,$read_fh) = @_;
    my ($line,$l,$q);

    # analyze the inductor using pi
    print $write_fh "pi $name $frequency\n";

    # wait for analysis to complete
    do {
        $line = <$read_fh>;
    } until $line =~ /Pi Model/;

    # extract info from the analysis
    ($q) = ($line =~ /Q = (\d+.\d*) ,/);
    $line = <$read_fh>;
    ($l) = ($line =~ /L = (\d+.\d*) nH/);

    # if pi reports a pure capacitance, force pix to begin
    if(!defined($l)) {$l = $l_lower_bound;}

    return ($l,$q);
}

# run PIX analysis on $name [default: ind] and return L and Q
# use: ($l,$q,$srf,$timed_out) =
#       &run_pix($name,$gnd,$frequency,*INPUTHANDLE,*OUTPUTHANDLE);
sub run_pix {
    my ($name,$gnd,$frequency,$write_fh,$read_fh) = @_;
    my ($line,$rin,$rout,$elapsed,$ready,$l,$q,$srf);

    # analyze the inductor using pi
    print $write_fh "pix $name $frequency $gnd\n";

    # scroll thru output until "capacitance matrix"
    do {
        $line = <$read_fh>;

```

```

} until $line =~ /capacitance matrix/;

# read "generating inductance matrix" line or time-out
$rin="";
vec($rin, fileno($read_fh),1)=1;
my $began = time;
do {
    $ready = select($rout=$rin, undef, undef, $time_out);
    $line="";
    if($ready) {
        $line =getc $read_fh;
    }
} until (($line eq "\n") or (!$ready));

# wait for analysis to complete (or time-out)
if(!$ready) {
    my $a = time;
    &restart_asitic;
    print "took ", time - $a , " to kill.";
    return (0,0,0,1); # time-out and move to the next n++
} else {
    # extract info from the analysis
    $line = <$read_fh>;
    ($q) = ($line =~ /Q = (\d+.\d*) ,/);
    $line = <$read_fh>;
    ($l) = ($line =~ /L = (\d+.\d*) nH/);
    $line = <$read_fh>;
    $line = <$read_fh>;
    ($srf) = ($line =~ /Resonance = (\d+.\d*)/);

    return ($l,$q,$srf,0);
}
}

# Create, pi analyze, and delete spiral
# use: ($l,$q) = &pi_spiral($length,$w,$s,$n,$spiral_coords ,
#                          $frequency,*THEINPUT,*THEOUTPUT);
sub pi_spiral {
    my ($length,$w,$s,$n,$spiral_coords,$frequency,$write_fh,$read_fh) = @_;

    print $write_fh &make_spiral("ind",$length,$w,$s,$n,$spiral_coords);
    ($l,$q) = &run_pi("ind",$frequency,$write_fh,$read_fh);
    print $write_fh &delete_spiral("ind");
}

```



```

    return ($l, $q);
}

# Create, pix analyze, and delete spiral
# use: ($l, $q, $srf) = &pix_spiral($length, $w, $s, $n, $spiral_coords,
#
#                                     $frequency, *THEINPUT, *THEOUTPUT);
sub pix_spiral {
    my ($length, $w, $s, $n, $spiral_coords, $frequency, $write_fh, $read_fh) = @_;

    print THEINPUT &make_spiral("ind", $length, $w, $s, $n, $spiral_coords);
    ($l, $q, $srf, $timed_out) = &run_pix("ind", "gnd", $frequency, $write_fh, $read_fh);
    if(!$timed_out) { # look for time-out
        print THEINPUT &delete_spiral("ind");
    }

    return ($l, $q, $srf);
}

# returns a formatted list of analysis results
# use: print &format_results($matlab, $w, $s, $n, $l, $q, $srf)
sub format_results {
    my ($matlab, $w, $s, $n, $l, $q, $srf) = @_;
    my $format;

    if($matlab) {
        $format = "%6.2f %6.2f %5.2f %7.3f %6.2f %5.2f";
    } else {
        $format = "w=%6.2f s=%6.2f n=%5.2f L=%7.3f Q=%6.2f SRF=%5.2f";
    }

    return sprintf $format, $w, $s, $n, $l, $q, $srf;
}

# save analysis results for future search
# use: &print_and_save;
sub print_and_save {
    print &format_results(0, $w, $s, $n, $l, $q, $srf);
    $now = time;
    print " ". &get_time($now - $start_time);
    if(($l_lower_bound < $l) && ($l < $l_upper_bound)) {
        print DATA &format_results(0, $w, $s, $n, $l, $q, $srf), "\n";
        if($q > $best_q) {
            $best_w=$w; $best_s=$s; $best_n=$n;
            $best_l = $l; $best_q=$q; $best_srf=$srf;
        }
    }
}

```

```

        print " *\n";
    } else {
        print "\n";
    }
}

# kill and restart asitic after a time-out
# use: &restart_asitic;
sub restart_asitic {
    print "Skipping: ";
    close THEINPUT or die "can't close ASITIC input: $!";
    close THEOUTPUT or die "can't close ASITIC output: $!";
    kill 9, $pid;
    waitpid($pid,0);

    $pid = open2(*THEOUTPUT, *THEINPUT, "asitic -t $tekfile -g" );
    print THEINPUT "sq NAME=gnd LEN=$gnd_length W=$gnd_width S=0 N=1 METAL=m3"
        . " EXIT=no XORG=$gnd_coords YORG=$gnd_coords\n";
}

```