

# SIMOX BOX Metrology

## Using Physical and Electrical Characterization

by

Jung Uk Yoon

Submitted to the Department of Materials Science and Engineering in  
partial fulfillment of the requirements for the degree of

Master of Science in Materials Science and Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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### **Abstract**

As the SOI manufacturers are poised to move onto high-volume production in response to renewed interest in using SIMOX materials for CMOS VLSI applications where low-power consumption and higher density are important, it is imperative for the manufacturers and consumers to have a quality-monitoring technique at their disposal. Traditional methods such as transmission electron microscopy and copper plating offer a long turn-around time and are not comprehensive enough. An electrical technique using high-field conduction testing is developed as an attempt to answer this problem. Electrical testing has the advantage of shorter turn-around time compared to TEM and provides important materials parameters which were available only via several methods before. Use of high-field testing for SIMOX buried oxide metrology is evaluated through physical verifications. High-field tunneling characteristics are measured and physical parameters such as silicon island density and BOX non-stoichiometry are extracted from these characteristics. Then extracted parameters are compared to the values measured via physical means. Although the correlation is not perfect, it gives the possibility of using this technique for actual metrology technique in manufacturing line.

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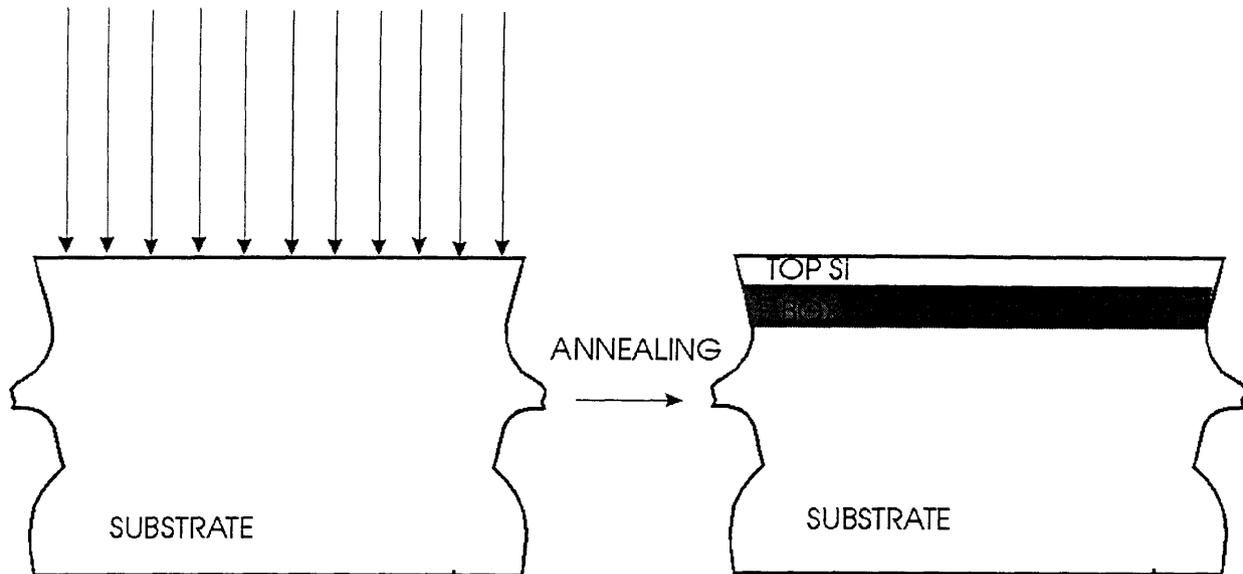
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## Introduction

There has been a great interest in the development of SOI(Silicon-On-Insulator) in recent years. SOI is a promising alternative substrate technology to bulk silicon in CMOS VLSI(Very Large Scale Integration) integrated circuit technology.[1, 2] The interest lies in the existence of an electrically insulating layer underneath an active silicon layer. Resulting isolation of devices from the substrate can reduce the parasitic capacitance associated with transistors and improve speed and lower the power consumption. Also this isolation makes SOI devices less susceptible to short-channel effects than conventional bulk devices.[3, 4] In addition, intrinsic electrical isolation eliminates the need for well isolation and reduces the cost by reducing the complexity of fabrication process and increasing the packing density.

One of the leading processes for manufacturing SOI substrates is SIMOX(Separation by IMplantation of OXYgen) technique.[5] SIMOX is created by implanting a large dose of high energy oxygen ions into a silicon substrate followed by a high temperature annealing, creating a continuous layer of BOX(buried oxide).[6] [Figure 1] High implantation temperature such as 600°C of the substrate is necessary in order to produce high quality crystalline top silicon layer.[6, 7] High temperature annealing following the implantation is required to cure the implant damage of top-layer silicon and produce higher quality oxide.[8] SIMOX is the leading technology because it is the most mature process and produces wafers with superior silicon-layer thickness uniformity compared to other technologies.[1] The thickness uniformity of SIMOX is +3nm for a thickness of 200nm and that of BSOI(Bonded SOI), which is the next leading technology, is +10nm for a thickness of less than 200nm.[9] Silicon-layer-thickness uniformity is important for fully depleted CMOS devices.



**Figure 1 Fabrication of SIMOX by implantation of oxygen and high temperature annealing**

Current disadvantages of SIMOX are its cost and the issue of quality and reliability of the material. Its cost is about 10 times more than bulk silicon wafers.[10] In order for SIMOX to be a viable replacement for bulk silicon, its quality and reliability must be shown to be comparable to bulk silicon and the price must be lowered. Quality and reliability of SIMOX is the crucial issue in bringing SOI to mainstream manufacturing. Accordingly, the quality and reliability of SIMOX BOX(Buried Oxide) becomes important because BOX properties are indicative of overall wafer quality and uniformity. Also quality and reliability of BOX itself is important for overall VLSI reliability. In order to increase the quality and reliability of SIMOX wafers, a feedback mechanism for manufacturers's process control and a method for users's materials evaluation needs to be developed.

The only technique that is currently being used in the industry for characterizing BOX is spectroscopic ellipsometry for thickness measurement. Thus, there is a need for a more comprehensive metrology technique to evaluate the quality of BOX. In response to this need, an electrical technique for SIMOX BOX metrology is developed to provide the necessary feedback for quality control. Advantages of electrical

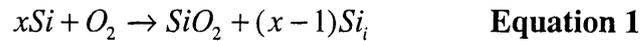
characterization are several. It is possible to gather similar information previously available only via physical analysis such as TEM(transmission electron microscopy) and SEM(scanning electron microscopy). It has the ability to acquire large statistical amount of data for statistical process control. Also electrical testing has excellent measurement sensitivity. The developed technique can be used to monitor silicon-island density and BOX non-stoichiometry which are indicative of BOX quality; the technique and details of BOX micro-defects will be discussed in details in later sections.

## SIMOX Buried-Oxide Characteristics

### *SIMOX Buried Oxide Formation Mechanisms*

Typical single implant SIMOX substrates are fabricated by implanting  $2 \times 10^{18}$   $O^+$ /cm<sup>2</sup> of 200keV oxygen ions into silicon substrate followed by a high temperature annealing for 6 hours at approximately 1325°C. During implantation, oxide precipitates form underneath a damage crystalline silicon layer due to exceeding solubility limit of oxygen in silicon.

In growing oxide, the conversion of silicon to oxide would require 2.2-fold increase in volume. This can be accommodated by two mechanisms. One is volume expansion through the viscous flow of the oxide which is the mechanism in normal thermal oxide. Another mechanism is by emission of Si atoms which become self-interstitials according to the equation



In normal thermal oxide, this second mechanism is insignificant because silicon interstitials have a high formation energy. However, in the case of BOX, the conversion of silicon to oxide occurs via the second mechanism because there is a volume constraint which restricts the viscous flow of the oxide and the energy to break silicon bonds are provided by energetic oxygen ions.[11] Completely strain-free precipitation requires the emission of 0.63 interstitial Si atom for each precipitate.[12]

The diffusivity of silicon in SiO<sub>2</sub> is very low ( $3.3 \times 10^{-17}$  cm<sup>2</sup>/s at 1300°C) which is eight orders of magnitude lower than that of oxygen in SiO<sub>2</sub>. [13] Thus, only silicon interstitials close to the SiO<sub>2</sub>/Si interface can migrate to the silicon layers. Other interstitials are trapped by oxide precipitates that exist.[14] If the concentration of trapped silicon interstitials is high, they may take the form of silicon islands. Other trapped silicon interstitials become point defects such as strained  $O_3 \equiv Si - Si \equiv O_3$  bonds [11] or excess silicon.

At the initial stage of high temperature annealing, there is a dissolution of smaller precipitates in the region near the surface and oxygen atoms migrate inwards. The

size of a stable precipitate increases with the annealing temperature.[15] Thus, the number of oxide precipitates decreases and the ones bigger than the critical size grow eventually forming one continuous layer. This process is known as “Ostwald ripening”. The final thickness of the buried oxide layer after high temperature annealing is determined by the competition between the rate of the oxide-coalescence process and that of the dissolution process and diffusion.[16]

### ***SIMOX Buried-Oxide Microstructure***

#### **Buried-Oxide Silicon Islands**

During annealing, the buried oxide grows preferentially towards the front surface which acts as an infinite sink for silicon interstitials that are generated by the conversion of silicon into oxide.[17] The preferential growth is also due to heavier implantation damage where many silicon-silicon bonds are broken, reducing the energy needed to form oxide.[18, 19] As oxide precipitates coalesce, silicon interstitials are generated and there is supersaturation built up stopping the oxidation reaction[according to equation 1] in the unoxidized silicon trapped by oxide precipitates due to the low diffusivity of silicon in oxide.

For doses above  $1.7 \times 10^{18} \text{ O}^+ \text{ cm}^{-2}$  silicon islands are observed only near the BOX/substrate interface. These islands are about 30nm thick and 30 to 200 nm long, and are situated at an almost constant distance (25nm) from the interface. For doses between  $1.7$  and  $1.4 \times 10^{18} \text{ O}^+ \text{ cm}^{-2}$  they form at both upper and lower interfaces. When the dose is below the critical value for formation of a continuous oxide layer they appear everywhere in BOX.[14] In the case of standard single-implant SIMOX, silicon islands occupy 2% of the volume in the BOX.[11]

From study on Si-rich  $\text{SiO}_2$ , it is known that  $\alpha$ -Si precipitates with a mean size of 10nm exist if the annealing temperature is lower than  $1100^\circ\text{C}$ . Above this temperature the  $\alpha$ -Si is completely crystallized. It is experimentally verified that silicon islands are crystalline with well developed facets along (001) and (111) planes. Most islands have

the same orientation as the substrate but there are islands which are off by small degrees. Figure 2 shows two silicon islands with different orientation. The smaller island has lattice orientation that is off by about 10 degrees from that of substrate orientation. The reason for their mismatch in orientation is unclear at the moment. However, the implantation temperature affects the orientation and existence of silicon islands. Ishikawa and Shibata found that crystal orientation of islands coincided with those of the substrate at high substrate temperature (485°C) while the orientation became random at low substrate temperature (280°C).[20]



**Figure 2 Silicon islands with mismatched orientations**

### **Buried-Oxide Non-Stoichiometry**

High density of oxygen vacancies in the form of the strained Si-Si bonds exists in the BOX.[17] At  $2.0 \times 10^{18} \text{ O}^+ \text{ cm}^{-2}$  dose, the refractive index of BOX is higher than that of fused silica indicating a strained structure of  $\text{SiO}_2$  [21] in agreement with the theory of excess silicon. The presence of silicon precipitates in the oxide attests to the likelihood of

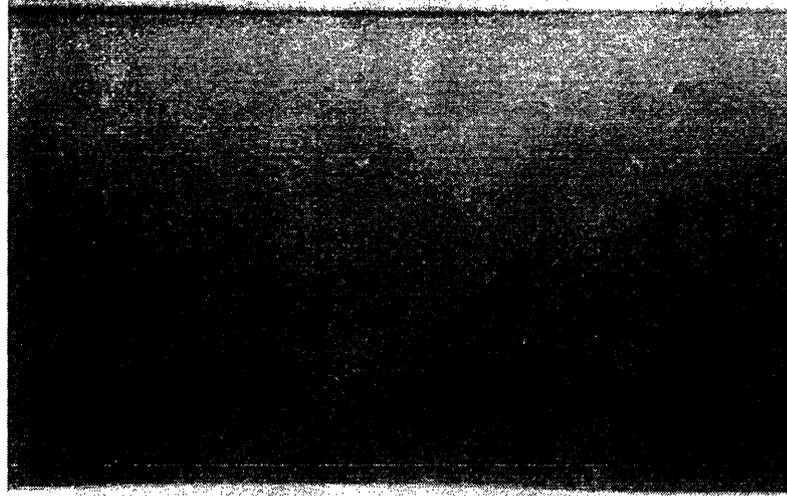
substoichiometry which would lead to an enhanced density of neutral oxygen vacancies,  $O_3 \equiv Si - Si \equiv O_3$ . [22] Excess silicon in various forms is present in BOX that range from Si-Si bonds to crystalline silicon clusters. [23]

ESR (Electron Spin Resonance) studies show that BOX has a higher density of paramagnetic defect centers compared to thermal oxide. Paramagnetic defect centers in SIMOX thin films are all related to oxygen deficiency. There are three types of EPR (Electron Paramagnetic Resonance)-active centers found in BOX. They are oxygen vacancy  $E\gamma'$  centers ( $O_3 \equiv Si - Si \equiv O_3$ ), delocalized  $E\delta'$  centers which may be clusters of ~5 Si atoms, and  $D$  centers ( $\bullet Si \equiv Si_3$ ). [24] Vanheusden et al found that there is a fairly uniform defect generation sensitivity with a strong decline towards the BOX/substrate interface. [25] Direct evidence of excess silicon in BOX comes from the etch rate study. It is found that etch rate of BOX is slower than that of thermal oxide which may be due to excess silicon or densification. [26, 27] Etch rate has been correlated with the ESR signals to show that etch rate is indeed indicative of excess silicon in BOX rather than densification. [25]

In addition, interpretation of spectroscopic ellipsometry points to BOX non-stoichiometry. Using a model to interpret spectroscopic ellipsometry data, BOX is found to contain 0.5% of excess silicon. [28] Using electroluminescence, Bota et al. speculated that 2.7eV band is produced by an intrinsic defect related with oxygen deficiency like the neutral oxygen vacancy defect. [29]

### **Other Types of SIMOX Materials**

Much effort has been expended on to produce SIMOX materials without above described defects. One way is to use multiple implantation rather than single implantation. In this case, small doses of oxygen ions are implanted with high temperature annealing in between. The total dose is the same as that of standard single-implant SIMOX. Such procedure has produced high quality BOX with a very few silicon islands and top silicon layer with low defect density. [12, 30] As shown in figure 3, BOX contains no silicon island. However, multiple implant is not used in commercial settings because of increased cost, resulting from longer annealing cycle.



**Figure 3 TEM cross-section of a multiple-implant SIMOX**

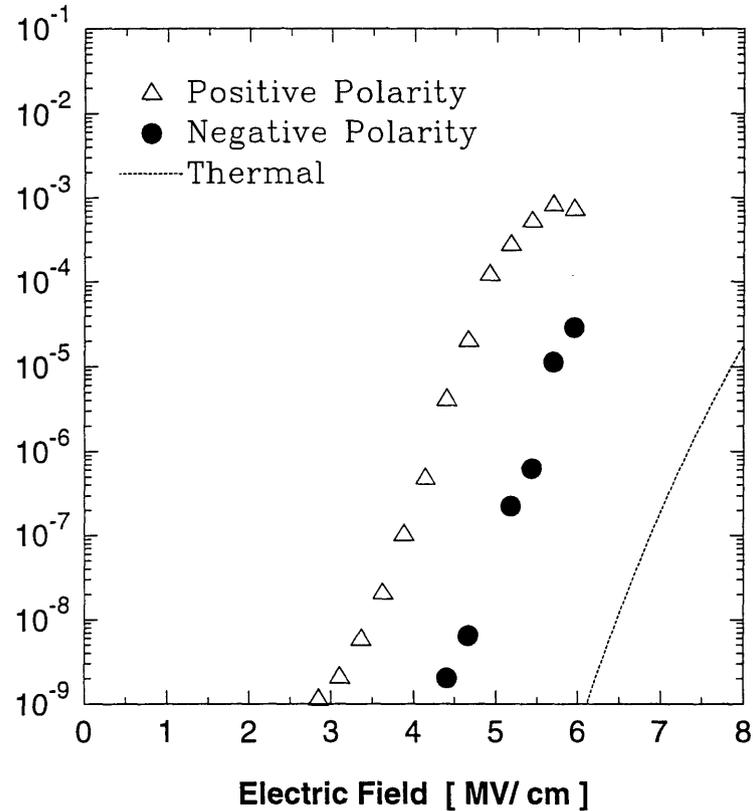
In addition to multiple implant, there has been much interest in finding a “window” of single-implant oxygen dose at which high quality BOX is produced. In this process, low dose of oxygen ions is coupled with low implantation energy. Several researchers have achieved high quality BOX without silicon islands using a variation of this method. Energy ranges from 20keV to 200keV and dose ranges from  $3.3 \times 10^{17}/\text{cm}^2$  to  $8 \times 10^{17}/\text{cm}^2$  [31, 32, 34]

### ***Buried-Oxide High-Field Electrical Characteristics***

#### **Electric-field dependence**

Figure 4 shows a typical single-implant SIMOX BOX high-field conduction characteristics with a thermal oxide high-field conduction characteristics as a comparison. The tunneling regime of the SIMOX BOX has a lower onset compared to the thermal oxide. [34] In addition, the onset electric field for electron injection from the bottom interface is significantly smaller than that for the electron injection from the top interface. The onset for thermal oxide is 6 MV/cm while the onsets for the buried oxide are 3

MV/cm and 4.5 MV/cm for injection from the substrate and from the top silicon layer respectively.



**Figure 4 Typical single-implant SIMOX BOX high-field conduction characteristics**

### Temperature dependence

Figure 5 shows that the conduction behavior of the buried oxide is not dependent on the temperature. For both injection from the substrate and from the top silicon layer, the current density stayed relatively independent of temperature from 29 °C to 250 °C. This independence suggests that high-field conduction in SIMOX BOX conduction is most likely due to Fowler-Nordheim tunneling instead of Frenkel-Poole Emission. Fowler-Nordheim tunneling is an oxide barrier narrowing effect modeled by the *wkb* approximation[35] whereas Frenkel-Poole emission is a trap-assisted conduction mechanism which is dominant in insulators such as silicon nitride.[9]

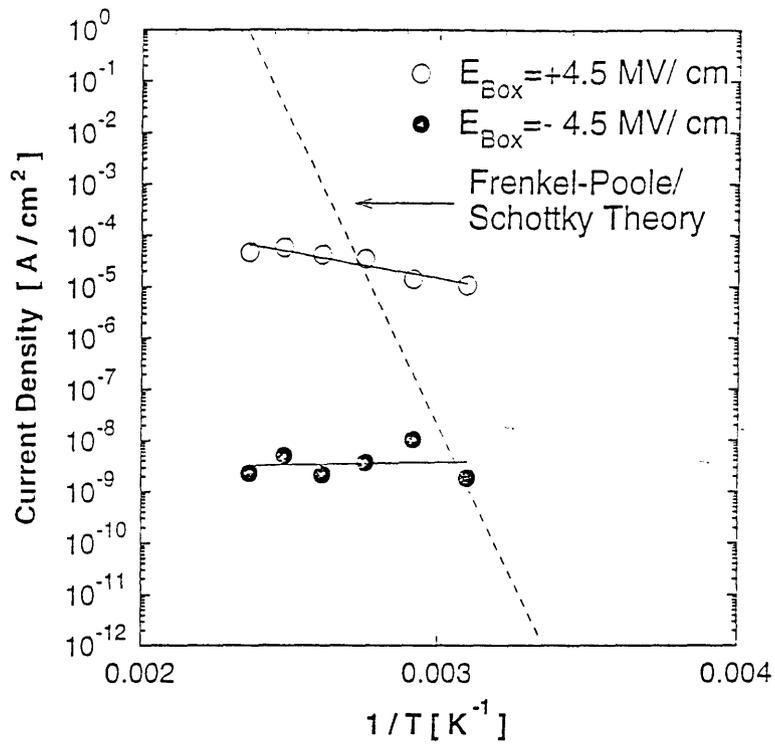


Figure 5 Temperature dependence of SIMOX BOX high-field conduction

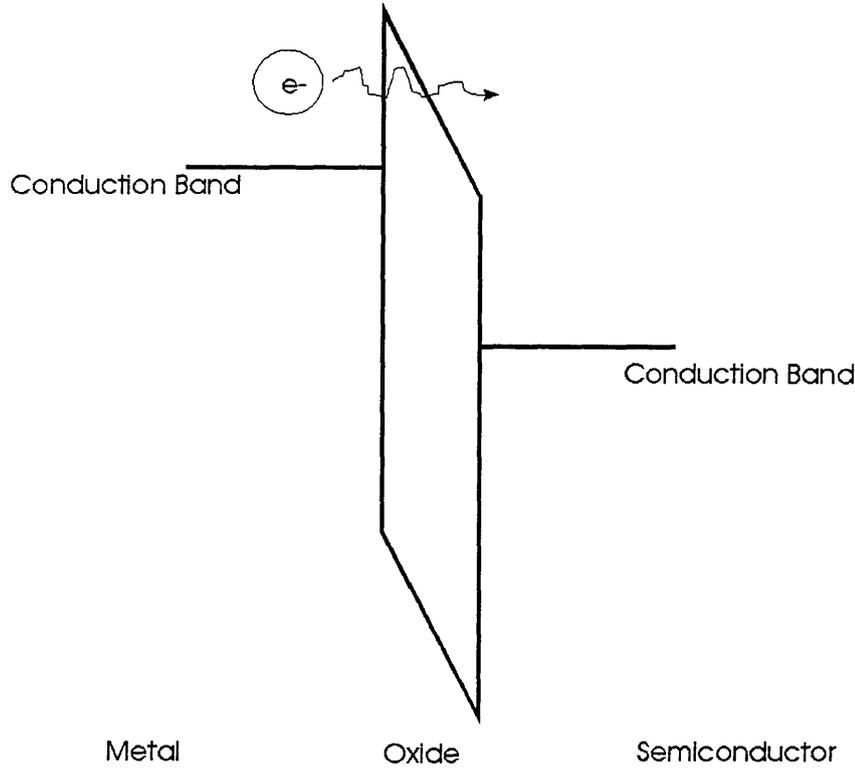
## **SIMOX Buried-Oxide Conduction Model**

This model is based on the electrical characteristics which point to Fowler-Nordheim tunneling as the dominant mechanism in SIMOX BOX at high-field. It links physical characteristics of BOX with the manifested electrical characteristics. The model accounts for both the earlier onset of high-field regime and the polarity dependence. Finally, the Fowler-Nordheim equation is modified to incorporate physical parameters.

### ***Buried-Oxide Conduction Mechanisms***

#### **Fowler-Nordheim Tunneling**

Fowler-Nordheim tunneling occurs when a high electric field is applied across an insulator. Applied high-field bends the energy band as to narrow the barrier which electrons must tunnel across. This narrowing effect will increase the possibility of electrons tunneling across the insulator. The model accurately describes the conduction of thermally grown oxides thicker than approximately 10nm. Figure 6 shows the mechanism by which electrons tunnel across the insulator.



**Figure 6 Fowler-Nordheim tunneling across an insulator**

The governing equation for the Fowler-Nordheim tunneling theory is

$$J = AE^2 e^{-B/E}$$

$$A = \frac{q^3 m_t^*}{8\pi\hbar m_{ox}^* q\phi_B} \frac{c\pi}{\sin c\pi}$$

$$B = \frac{4\sqrt{2} m_{ox}}{3\hbar q} [q\phi_B]^{3/2}$$

$$\frac{c\pi}{\sin c\pi} = \text{weak function of temperature}$$

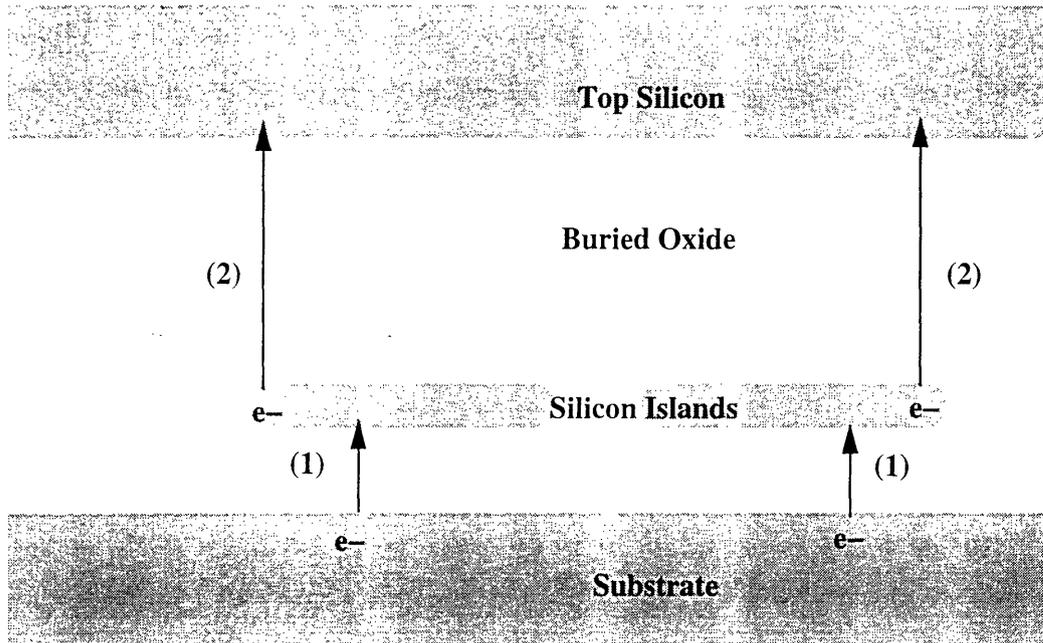
According to this first order model, C is the only term with temperature dependence, and it is a very small number. Therefore, sinc/c becomes approximately unity and consequently J becomes temperature independent for temperatures of interest. Both B and A are functions of  $\Phi_b$  which makes  $\Phi_b$  the determining factor in the onset of Fowler-Nordheim tunneling. The theoretical value of  $\Phi_b$  for thermal oxides is 3.2 eV, and the theoretical values of A and B are  $3 \times 10^6$  A/MV<sup>2</sup> and 240 MV/cm respectively.

### **Positive Polarity**

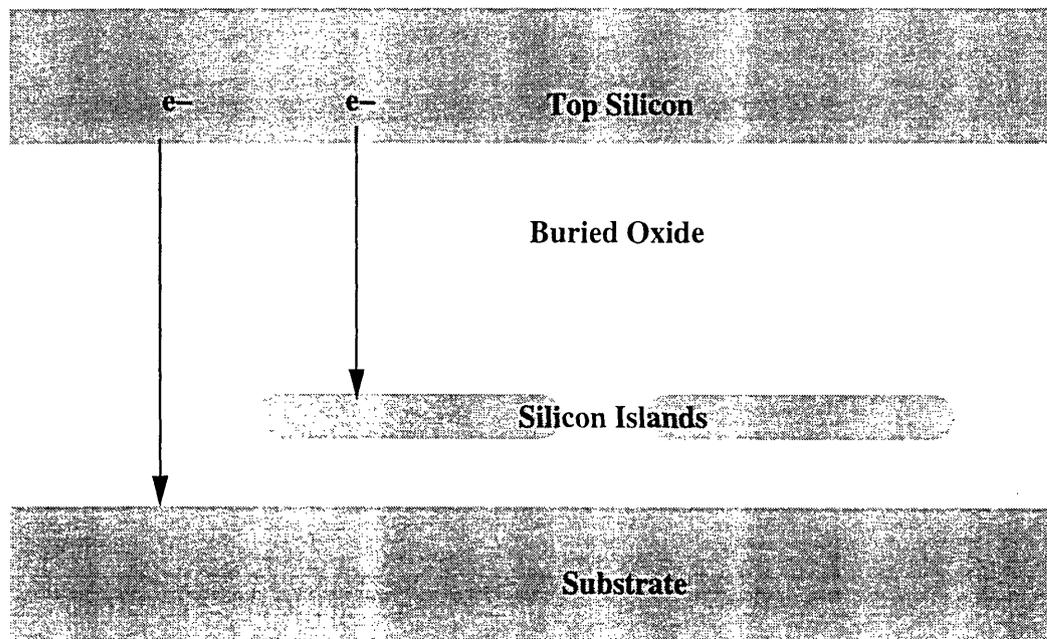
In positive polarity, electrons are injected from the bottom interface. The onset of tunneling regime is lower than that for thermal oxide. This earlier onset can be explained in terms of field-enhancement at the edges of silicon islands which are present near the bottom interface of BOX. Figure 7a describes the physical mechanism for SIMOX BOX conduction.

Since the islands are in a close proximity of the substrate, electrons can tunnel into the silicon islands at low electric fields. Because silicon islands have well developed facets, there is electric field crowding at the edges of these islands where facets meet. At these edges, the electric field seen by an electron is greater than the electric field applied to the buried-oxide. Due to this enhanced electric field, electrons are injected into the bulk of the buried oxide from the top surface of the silicon islands at lower electric field than that for thermal oxide. In positive polarity, this “electric-field enhancement” is the dominant factor.

a) Positive Polarity Conduction



b) Negative Polarity Conduction



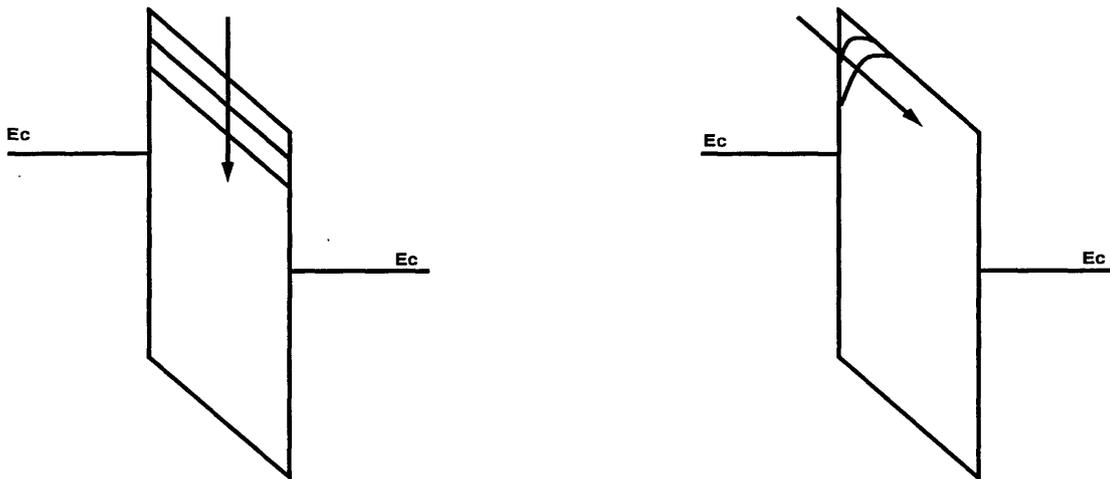
**Figure 7 Physical Mechanisms for SIMOX BOX conduction. a) Positive Polarity: electron tunneling is affected by E-field enhancement at the silicon islands b) Negative Polarity: electron tunneling is affected by oxide non-stoichiometry.**

### Negative Polarity

In negative polarity, electrons are injected from the bottom interface. The onset of tunneling regime is lower than that for thermal oxide but higher than that for positive polarity. This earlier onset can be explained in terms of BOX non-stoichiometry assisted tunneling of electrons. Fig 7b describes the physical mechanism.

Buried-oxide has excess silicon which may assist in tunneling. Research in silicon-rich oxide has shown that as the silicon content in oxide is increased, onset electric field for tunneling is lowered.[36] Excess silicon may affect the barrier for tunneling in two different ways: barrier lowering and barrier narrowing. They are pictorially described in the figure 8.

Barrier lowering is based on the uniform distributed excess silicon in the buried oxide to act as hopping centers for electrons to tunnel from one trap to another. This “electron hopping” mechanism causes the energy band of the oxide to appear lower than normal, which translates into earlier onset for tunneling.[37] Barrier narrowing is based on excess silicon that are concentrated near the interface between the top silicon layer and BOX. These excess silicon will lower the band in that small region which results in general narrowing of the band. This will also results in earlier onset of tunneling as electrons can tunnel through the oxide at a lower electric field.



**Figure 8 Pictorial description of barrier narrowing and barrier lowering effects**

Non-stoichiometry of the buried oxide is the dominant mechanism in negative polarity. Electric-field enhancement at silicon islands as described in the preceding section do not affect the tunneling in negative polarity because e-field enhancement is localized to near the silicon islands.

### ***SIMOX Buried-Oxide Fowler-Nordheim Equation***

Fowler-Nordheim equation is modified to include physical parameters which are responsible for the early onset of high-field tunneling regime.

$$J = k_a \left[ \frac{A_o}{\Phi_B} \right] (k_e E_o)^2 \exp\left( \frac{-B_o \Phi_B^{3/2}}{k_e E_o} \right) \quad \text{Equation 2}$$

where  $\Phi_b$  is the effective barrier height in the energy band, E is the applied macroscopic electric field, and  $A_o$  and  $B_o$  are physical constants, as shown below.

$$A_o = 9.6 \left[ \frac{\mu A - eV}{V^2} \right] \quad \text{Equation 3}$$

$$B_o = 42 \left[ \frac{MV}{cm - eV^{3/2}} \right] \quad \text{Equation 4}$$

$$E_o = \frac{V_{BOX}}{t_{BOX}} \left[ \frac{MV}{cm} \right] \quad \text{Equation 5}$$

$A_o$  and  $B_o$  are calculated from the theoretical values of A, B, and  $\Phi_b$  for thermal oxides.

$k_a$  is the effective area of injection related to silicon island density,  $k_e$  is field enhancement factor due to silicon islands, and  $\Phi_b$  is effective barrier height which is affected by BOX non-stoichiometry.

## **SIMOX Buried-Oxide Electrical Metrology**

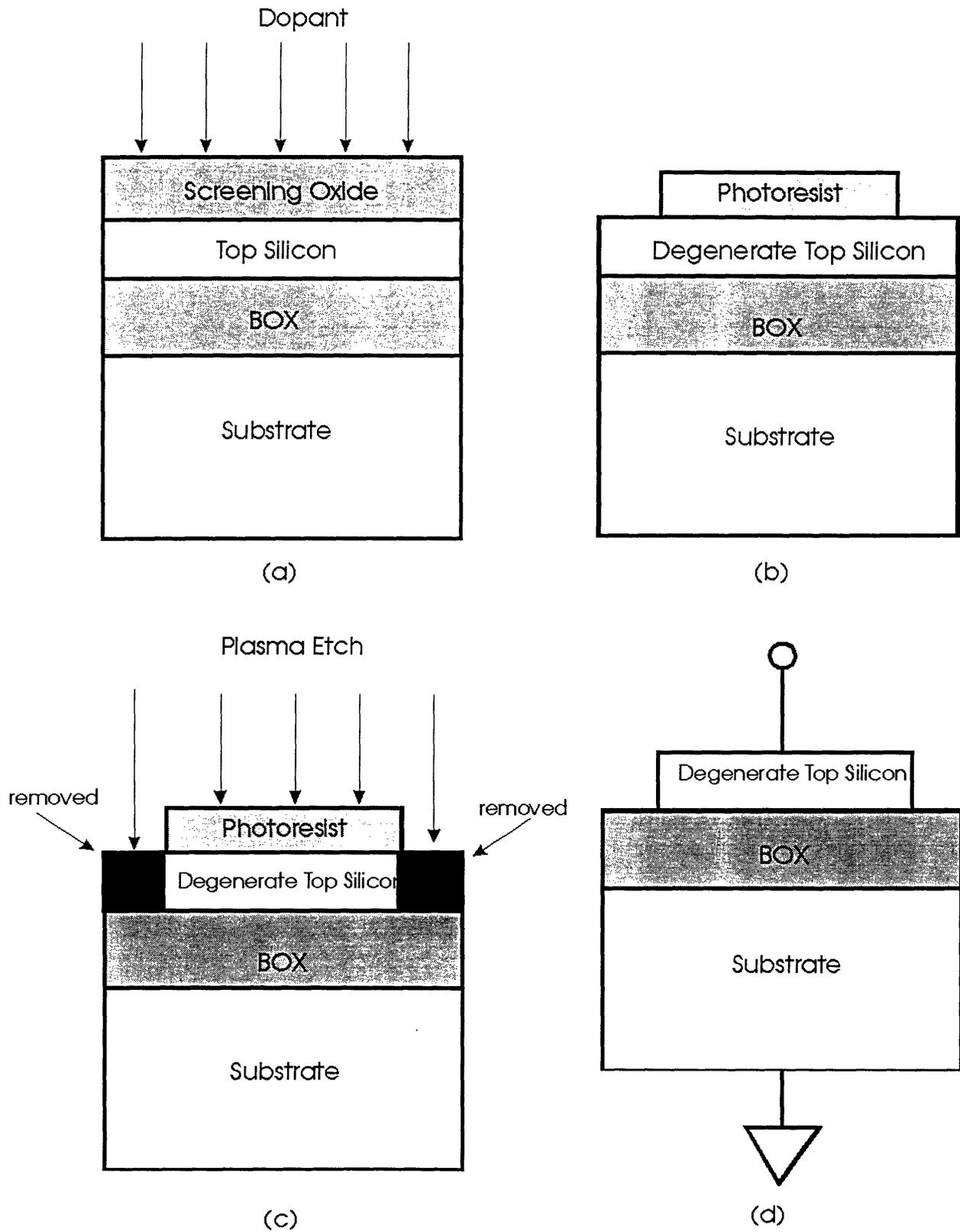
### ***Electrical Testing Procedure***

#### **Structure**

The device used for SIMOX BOX conduction study is a simple MOS capacitor with the top silicon layer as the top gate, the buried oxide as the dielectric, and the substrate as the bottom gate. Because this device requires very few processing steps, any damage from processing is minimized. Figure 8 shows the process for making the capacitors.

The top silicon is degenerately doped by ion-implantation through a screening oxide. Then the top layer is patterned and plasma etched, forming trenches between devices. MESA isolation rather than LOCOS (Local Oxidation of Si) is utilized because it requires less processing steps and produces devices with more consistent high electric field regime characteristics.[9] Traveller for the process is found in appendix A.

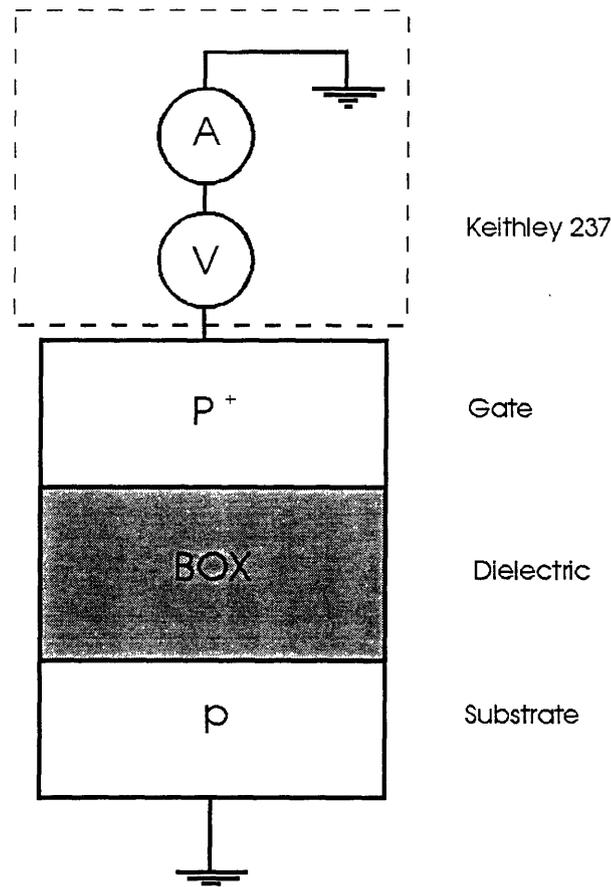
The size of capacitors was either  $0.0025 \text{ cm}^2$  or  $0.001 \text{ cm}^2$ . It is assumed that conduction characteristics of the capacitors has no area dependence.



**Figure 9** Fabrication process of MOS capacitors

### High-field testing

Keithley 237 High Voltage Source Picoammeter is used for high field testing. Figure 10 shows the standard setup with the substrate grounded and the voltage source and ammeter connected to the gate of the capacitor.



**Figure 10 Testing set up for high-field conduction**

The static J-E method is used to eliminate the time dependence of the tunneling characteristics. In this method, the current density is measured after a constant electric field has been applied to an unused capacitor after a set amount of time. Electric field is varied and the current density is again measured after the same length of time on a new device. J-E curve is constructed from these set of current density and electric field.

Because the method uses new devices for each measurement, implicit assumption is that there is little variation among devices.

### ***Buried-Oxide Silicon-Island Characterization***

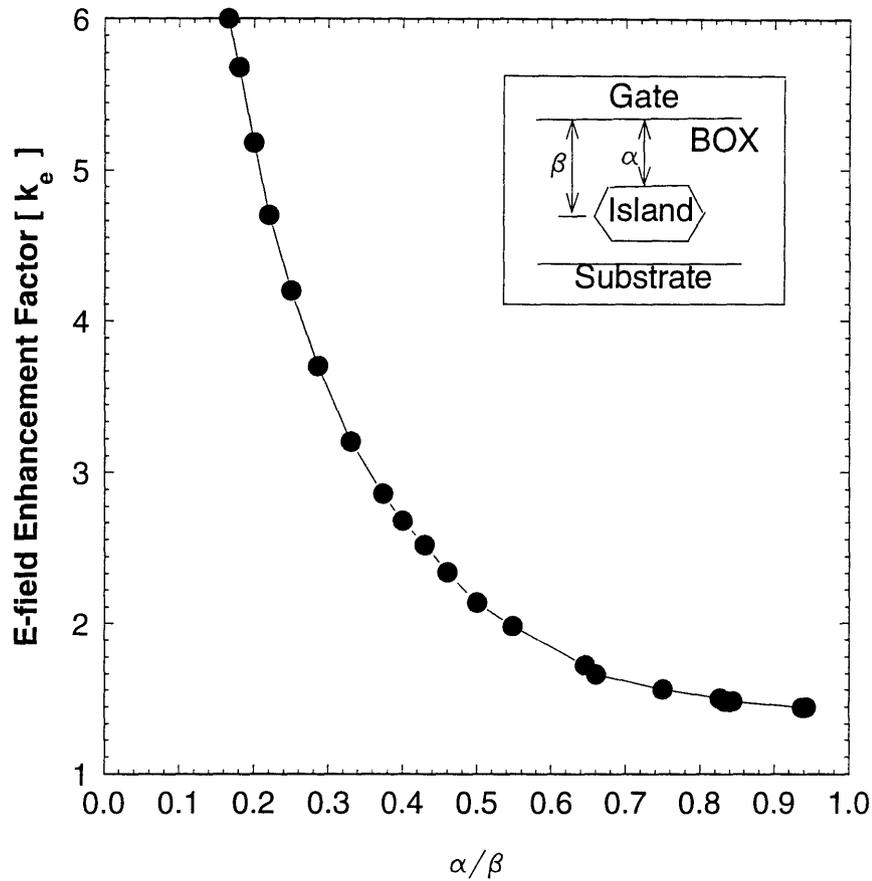
This section describes use of electrical characterization as a means to extract out silicon island density which is an important physical parameter to describe the buried oxide quality.

#### **Electrical BOX metrology**

Two standard single-implant SIMOX wafers were used. They were p-type substrates with <100> orientation and 10 to 22  $\Omega\text{cm}$  resistivity. They are standard wafers from two leading SOI manufacturers. Their materials specifications are found in appendix B. Several assumptions are made in order to simplify the procedure and extract out a meaningful parameter from electrical characteristics. Assumptions are then verified using either electrical or physical techniques.

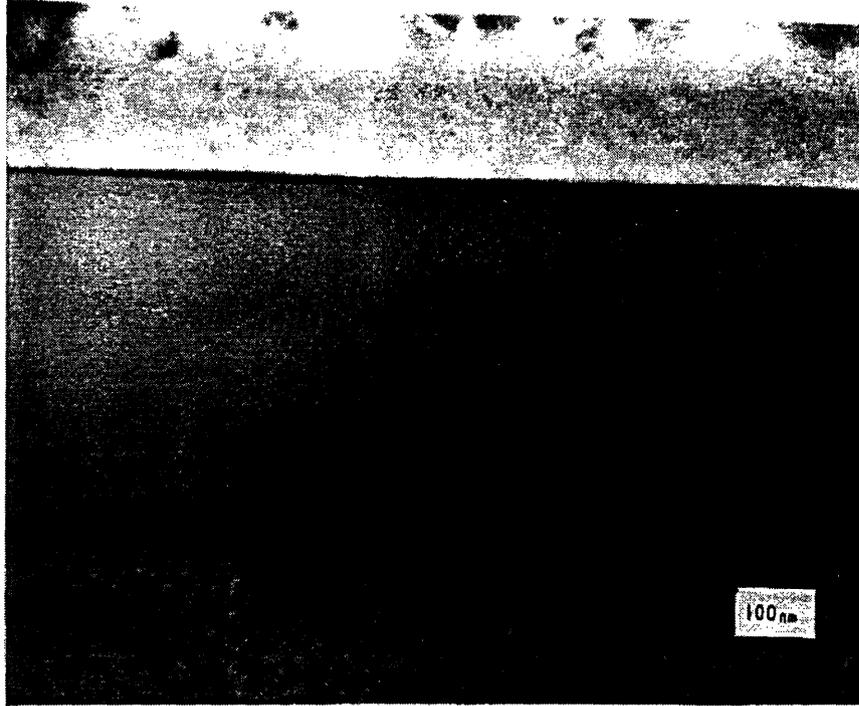
First assumption is that silicon islands are uniform in shape and their centroid location is the same. The impact of this assumption is that  $k_e$  which is field-enhancement factor becomes a constant and that  $k_a$ , which is effective area of injection, becomes a function of only one variable, silicon island density. Apparently, the assumption simplifies the calculation tremendously.

Simulation of  $k_e$  with respect to its centroid location inside BOX is carried out. Figure 11 shows the result of simulation made in Medici<sup>TM</sup>. The curve flattens out as the value of  $\alpha/\beta$  which is the ratio of distance between the top of silicon islands and the top interface and the distance between the middle of islands and the top interface approaches one. Thus, a small variation in the location of islands does not translate to a big change in the value of  $k_e$  if the islands are located close to the back interface.



**Figure 11 Simulation of field-enhancement at silicon islands**

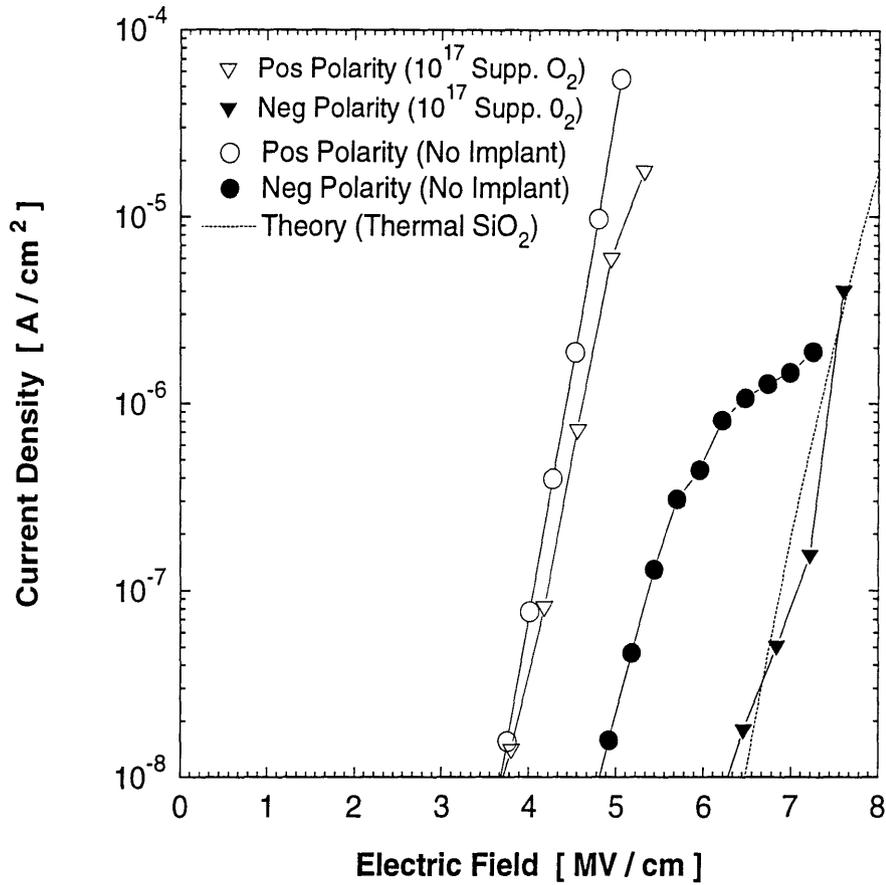
Cross-sectional TEM(transmission electron microscopy) is carried out using JEOL 200CX (tungsten filament) at 200keV to study the silicon island shape and its centroid location inside the buried oxide. Figure 12 shows a typical micrograph of the standard single-implant SIMOX substrate used for this experiment. Islands are located at similar distance away from the bottom interface. Thus,  $\alpha/\beta$  approaches one and the first assumption is checked. As expected, silicon islands have well developed facets and there is a little variation in their shape.



**Figure 12 Typical single-implant SIMOX BOX cross-sectional view**

Second assumption is that field-enhancement at the edges of islands is the only factor affecting the fowler-nordheim tunneling in the buried oxide.. Another assumption following this is that the effective barrier height for tunneling is the same as that of thermal oxide. This way,  $k_a$  becomes the only factor affecting the onset of tunneling regime.

In order to check this assumption, electrical testing is carried out on a standard single-implant wafers that have been implanted with supplemental oxygen. It is known to have stoichiometric oxide similar to thermal oxide.[17, 38, 39] Figure 13 shows the result where positive polarity conduction for these samples is the similar to standard single-implant whereas negative polarity conduction is returned to the thermal characteristics. In positive polarity conduction, the onset of tunneling regime did not shift in response to this returning of stoichiometry to thermal value; the onset of positive polarity conduction did not change. Thus, BOX non-stoichiometry does not play a major role in positive polarity conduction.



**Figure 13 High-field conduction characteristics of supplemental implant of oxygen**

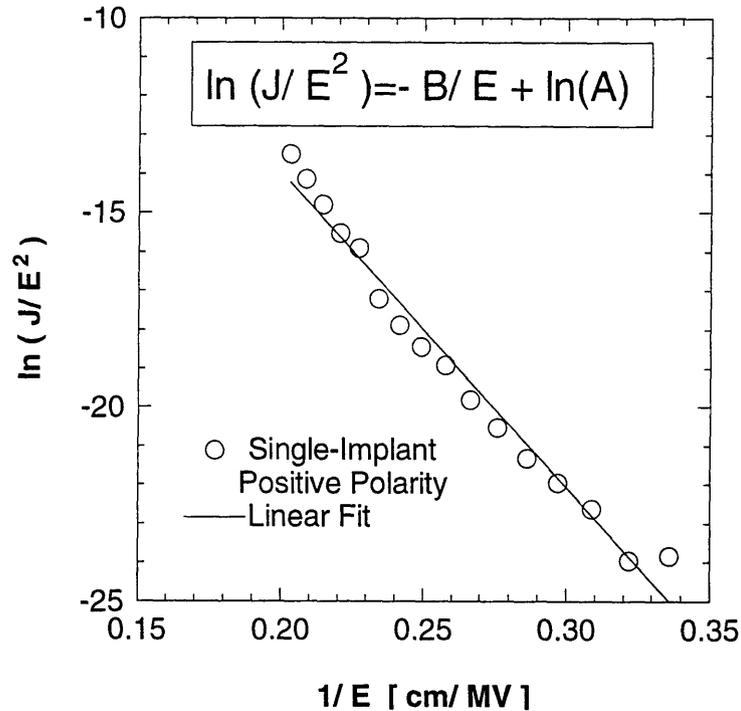
Based upon these two assumptions, the extraction of  $k_a$  from electrical characteristics is carried out. J-E graph obtained from the static J-E testing is first converted to  $\ln(1/E)$  vs  $J/E^2$  curve as shown in figure 14. This graphical conversion is the same as converting the fowler-nordheim equation to

$$\ln\left(\frac{J}{E^2}\right) = -\left(\frac{B}{E}\right) + \ln(A) \quad \text{Equation 6}$$

$$A = \frac{k_a A_o k_e^2}{\Phi_B} \quad \text{Equation 7}$$

$$B = \frac{B_o (\Phi_B)^{3/2}}{k_e} \quad \text{Equation 8}$$

where  $-B$  is the slope and  $\ln(A)$  is the intercept of a straight line. By using the least-square linear approximation, a best linear fit through the data is found. From that fitted line, both the slope and intercept is measured. From the slope  $-B$ ,  $k_e$  is calculated by plugging in the values of  $B_0$  and  $\Phi_b$  for thermal oxide. Using the calculated  $k_e$  and the measured intercept  $\ln A$ ,  $k_a$  is extracted.



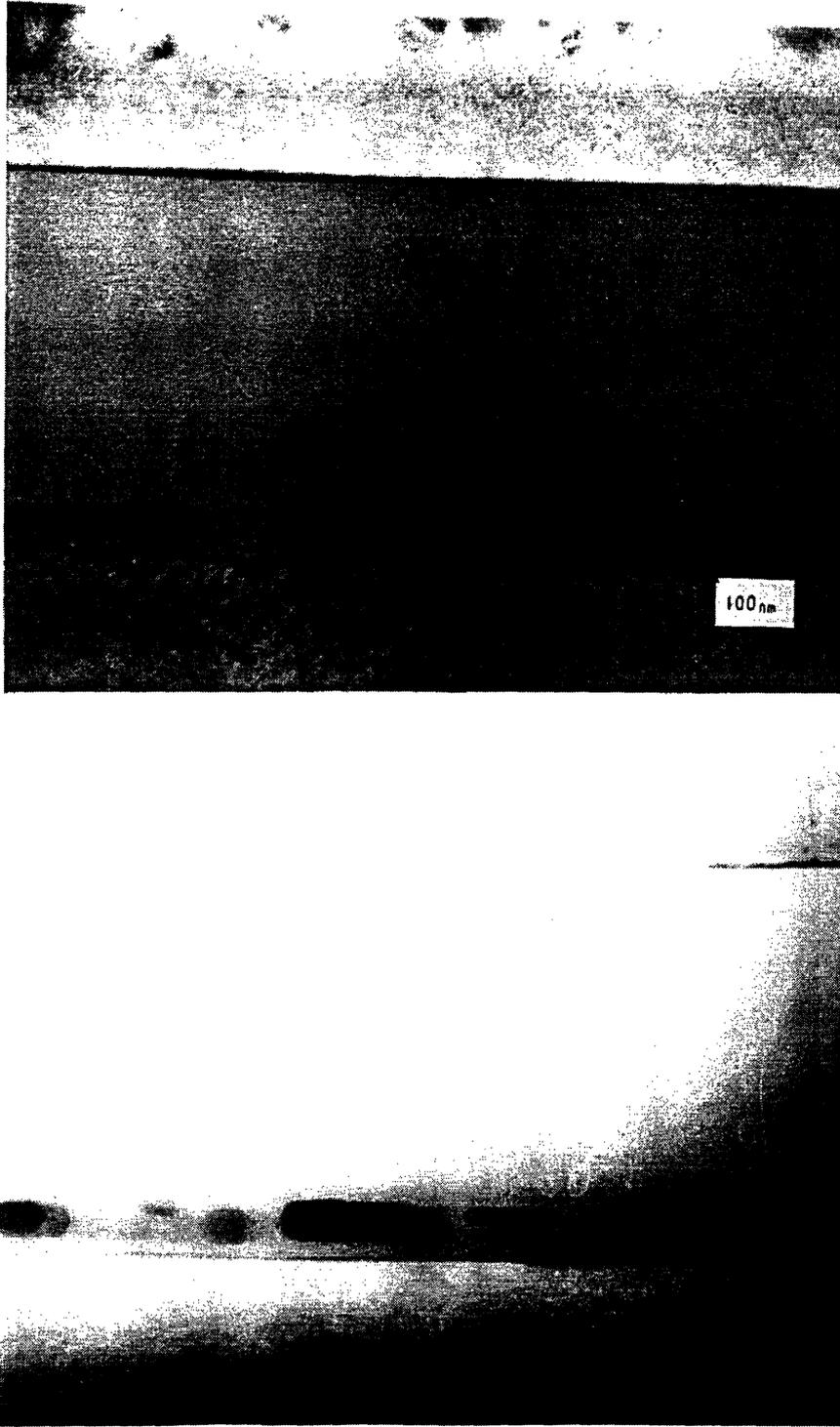
**Figure 14 Converted J-E graph with a fitted line for parameter extraction**

#### **Physical measurement of BOX silicon-island density**

MESA isolated capacitor structure is utilized in order to measure the silicon island density. Exposed buried oxide between devices is etched away in BOE(Buffered Oxide Etch) leaving behind silicon islands on top of the substrate surface.[40, 41] BOE contains 6:1  $\text{NH}_4\text{F}:\text{HF}$  (ammonium fluoride: hydrofluoric acid) by volume. The etching time was from 16 to 20 minutes for complete removal of oxide from the surface of the substrate. Samples are then washed in deionized water. The resulting samples are viewed using Electroscan ESEM(environmental scanning electron microscope) which requires no special treatment of samples. Beam energy used is 30keV and the magnification ranges from 10,000X to 30,000X. From the micrographs, silicon-island density is measured.

## **Results and Analysis**

Figure 15 and 16 show TEM and SEM pictures of the two samples that were used for this experiment. Figure 17 gives the comparison of calculated  $k_a$ , which is directly proportional to silicon-island density, and actual measured silicon-island density. The ratio of  $k_a$  between the two samples is 1:3 while the ratio of silicon island density between the two is 1:4.



**Figure 15** TEM cross-sections of samples 1 and 2

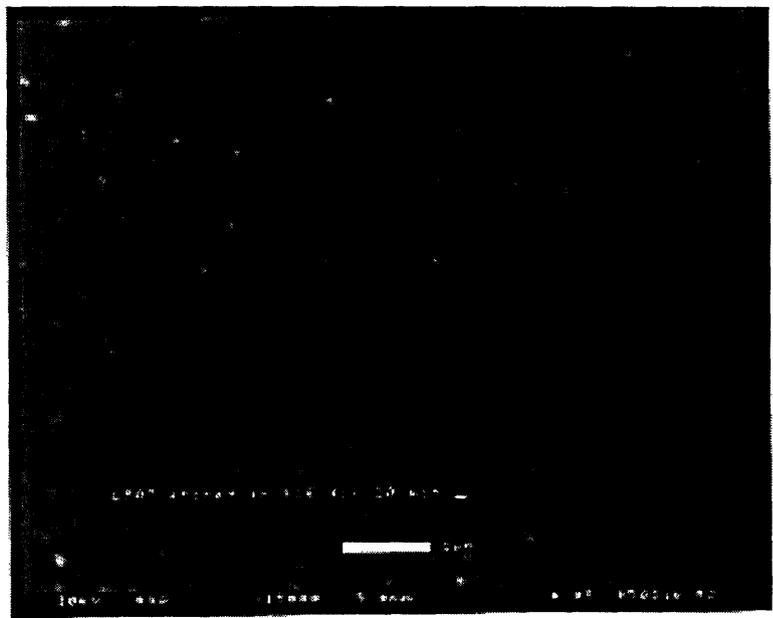
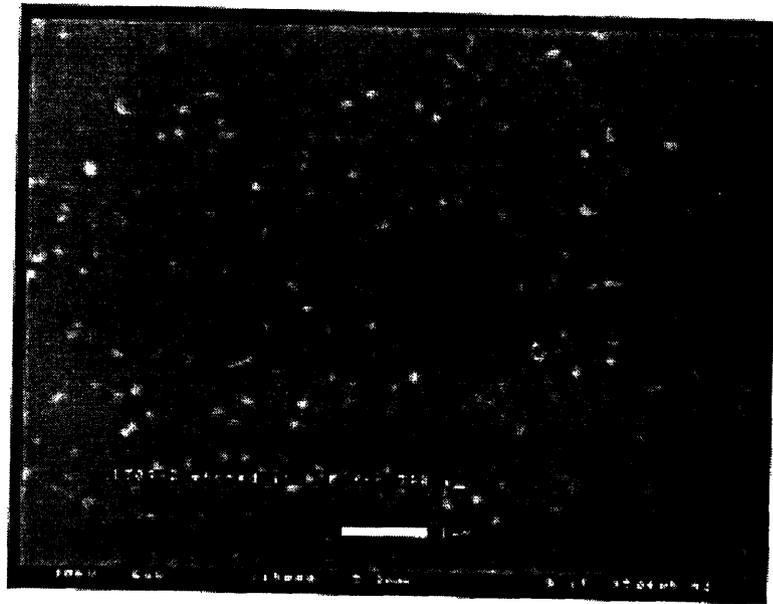
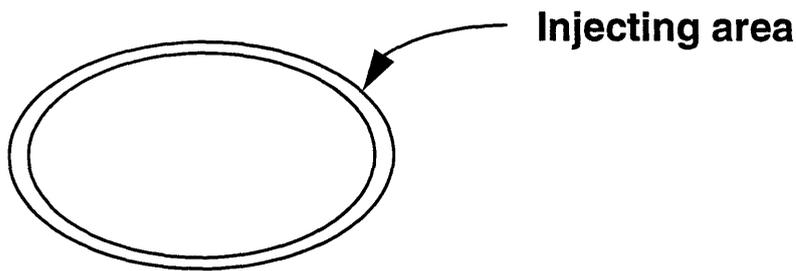


Figure 16 SEM of two samples used for silicon island density

Samples	$k_a$ (% of injecting area)	Measured Si-island density [ $\#/\mu\text{m}^2$ ]
Single-implnat 1	0.039	16.6
Single-implant 2	0.014	4.3

**Figure 17 comparison of extracted parameters with measured parameters**

The comparison of two ratios shows that there is a fair correlation between the two. The reason why the percentage of injection area is very small is that field-enhancement is present only at the edges of silicon islands. As shown in figure 18, the area at which there is field-enhancement is small compared to the size of silicon islands. Thus, injecting area is very small compared to the size of islands.



**Figure 18 Field-enhancement occurs only at edges effectively cutting the percentage of injecting area**

There are many factors which may have affected the correlation between the measured island density and calculated percentage. Wainwright and Hall has proposed that the early tunneling onset is caused by interface asperity induced e-field enhancement.[42] Although interface asperities are not confirmed by physical characterization, the difference in interface roughness may affect the conduction characteristics.

Another source of error is the fitting of a straight line through scattered data. Implicit assumption in the static J-E method is that there is a little, if any, variations in electrical characteristics from device to device. However, if there is a big variation, it is

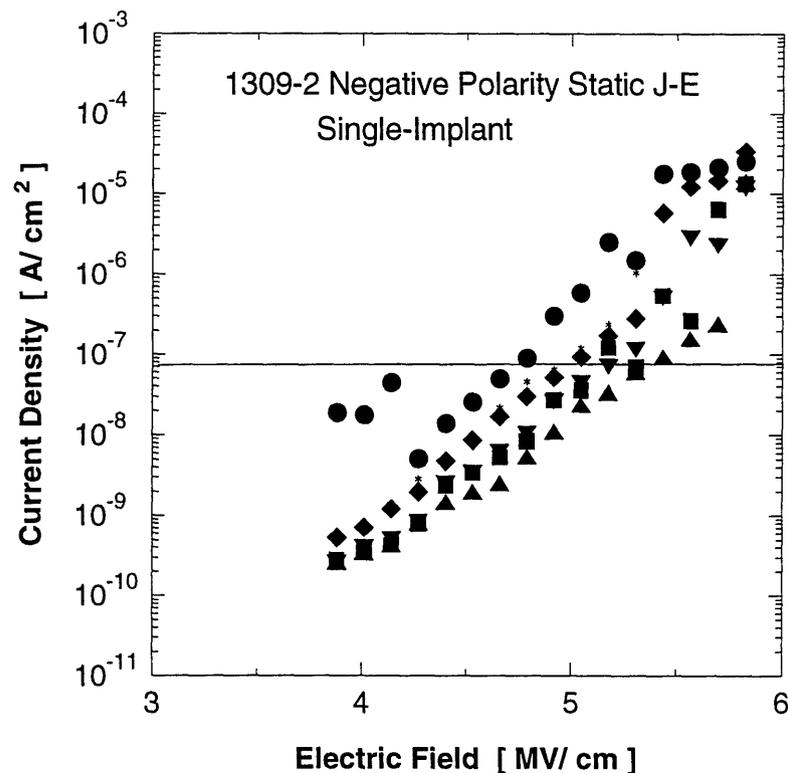
difficult to fit one straight line that is representative of all device characteristics. A small change in slope will result in a big change in the intercept since the intercept is extrapolated from the line fitted away from the y-axis.

In addition, physical characterization may contain errors. One source of error is the possibility of small islands floating off the surface during etching. Although the magnitude of island-density measured through this technique matches that calculated from cross-sectional TEM[43], there is still a possibility of losing some islands during etching process. This would result in a wrong measurement of silicon island density.

## Buried Oxide non-stoichiometry characterization

### Electrical BOX metrology procedure

The premise of this experiment is that etch rate is related to the non-stoichiometry of BOX and that the shift in high-field tunneling regime is related to the non-stoichiometry of BOX. Thus, from the change in non-stoichiometry can be linked to the shift in tunneling regime through etch rate comparison. For the comparison of shifts, a certain current density in the middle of the tunneling regime is chosen. Then electric field value corresponding to that current density is extracted from each device characteristics.[Figure 19] Thus, bigger E-field will correspond to less shift from the thermal tunneling regime. Several assumptions are made for comparison.



**Figure 19 Extraction of shift in tunneling regime**

First assumption is that small changes in non-stoichiometry will be translated into both a big change in tunneling characteristics and etching characteristics. Non-

stoichiometry affects  $\Phi_b$ , barrier height, which is in the exponential term of the fowler-nordheim equation. A small change in the exponential term will bring upon a big change in  $J$ , current density. However, the amount of changes in  $\Phi_b$  is not linearly proportional to non-stoichiometry. Thus, the exact ramification of changes in non-stoichiometry on barrier height characteristics and consequently on current density is not certain.

The second assumption is that BOX non-stoichiometry is the dominant factor which affects the shift in tunneling regime. Conduction studies on multiple and supplemental oxygen implant samples show that when BOX is stoichiometric, tunneling regime coincides with that of thermal oxide. Assumption that the only difference between the standard SIMOX and other types of SIMOX is BOX non-stoichiometry. Figure 20 shows a high-field conduction characteristics of multiple-implant and theoretical thermal oxide with coinciding tunneling regimes.

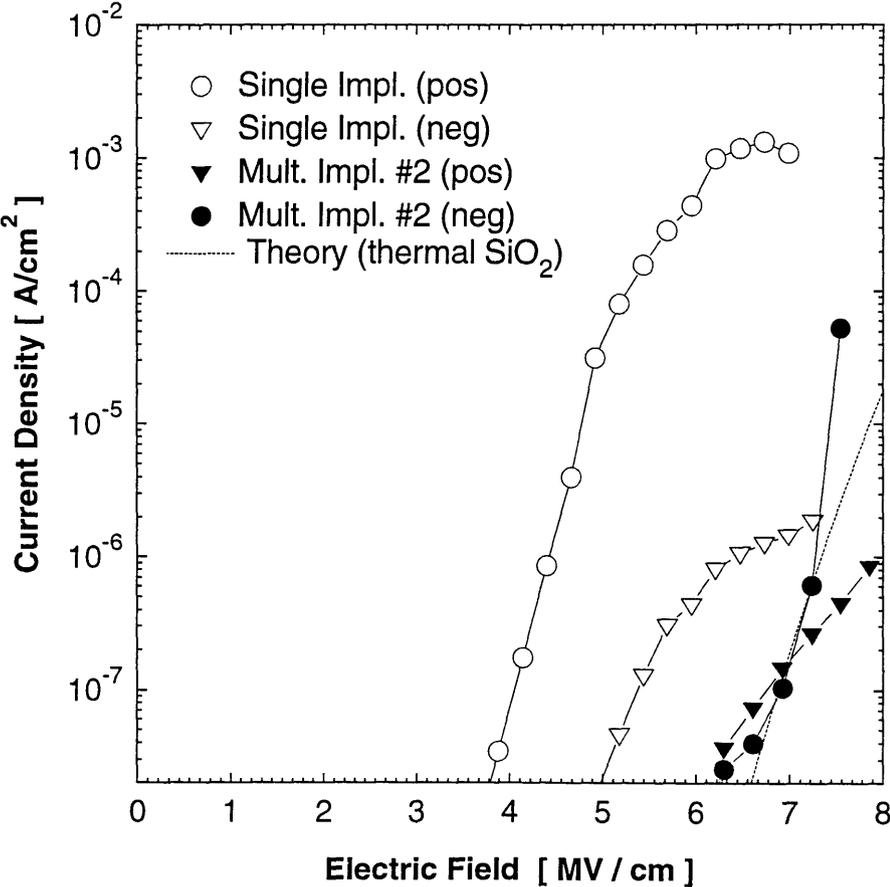
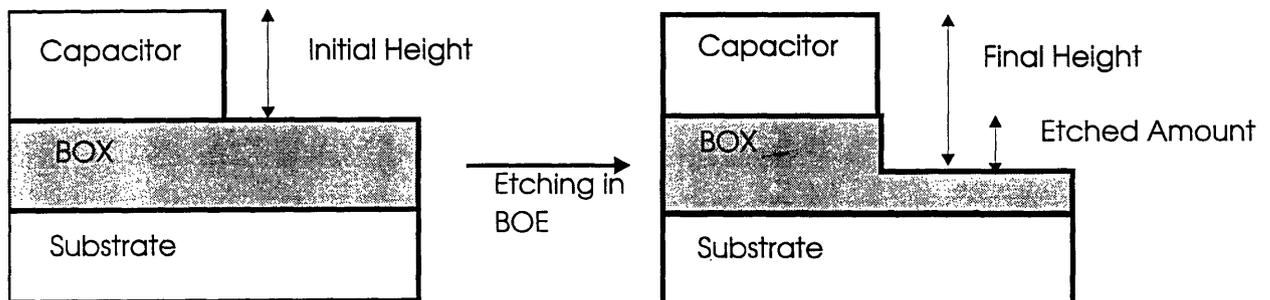


Figure 20 High-field conduction characteristics of multiple implant

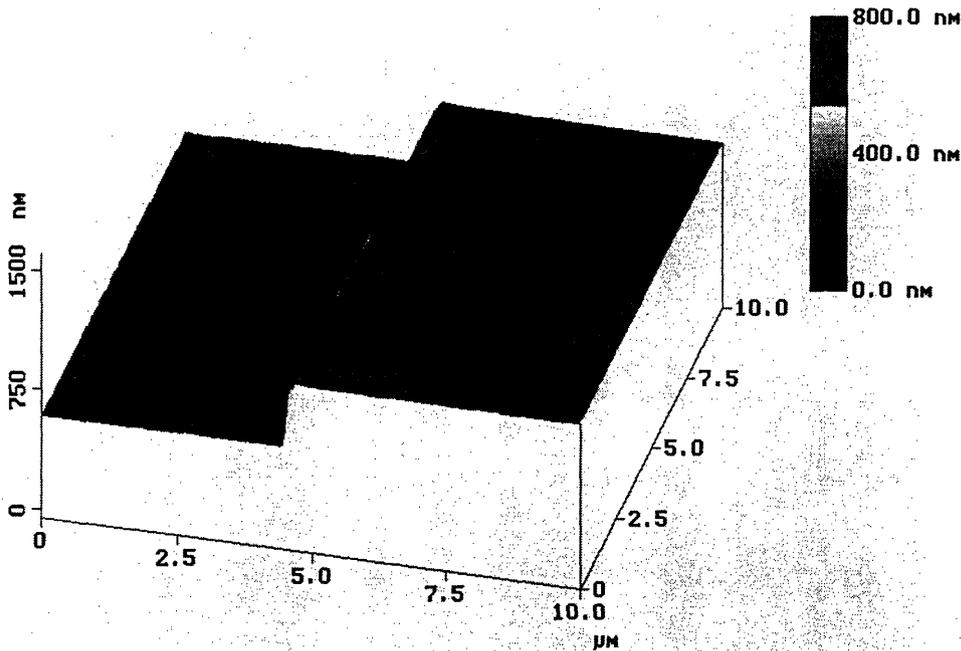
## Physical measurement of BOX non-stoichiometry

BOX etch rate is measured by utilizing the capacitor structure that has been built on the wafer for electrical characterization. Figure 21 describes how the structure is used. First the relative heights of BOX surface and capacitor surface are measured using AFM(atomic force microscope). AFM is used instead of a profilometer because each scan consists of 256 line scans and provides 3-D picture of the surface. Thus, the possibility of scanning a damaged surface and getting a wrong height information is reduced. Digital Instrument 1000 with tapping mode is used for this purpose. Two different scans away from each other are taken on a device. Figure 22 shows a 3-D picture from a typical scan of steps.

After the initial scanning of heights, samples are etched in BOE(Buffered Oxide Etch) for 80 seconds and rinsed in DI water. Samples are constantly swirled to ensure uniform etching. Then the heights are measured again using the AFM. The resulting difference between the initial and final height gives the etched amount of BOX. The etched height divided by the etching time gives the etch rate of the device. Average is taken from scans on two different sections on a device.



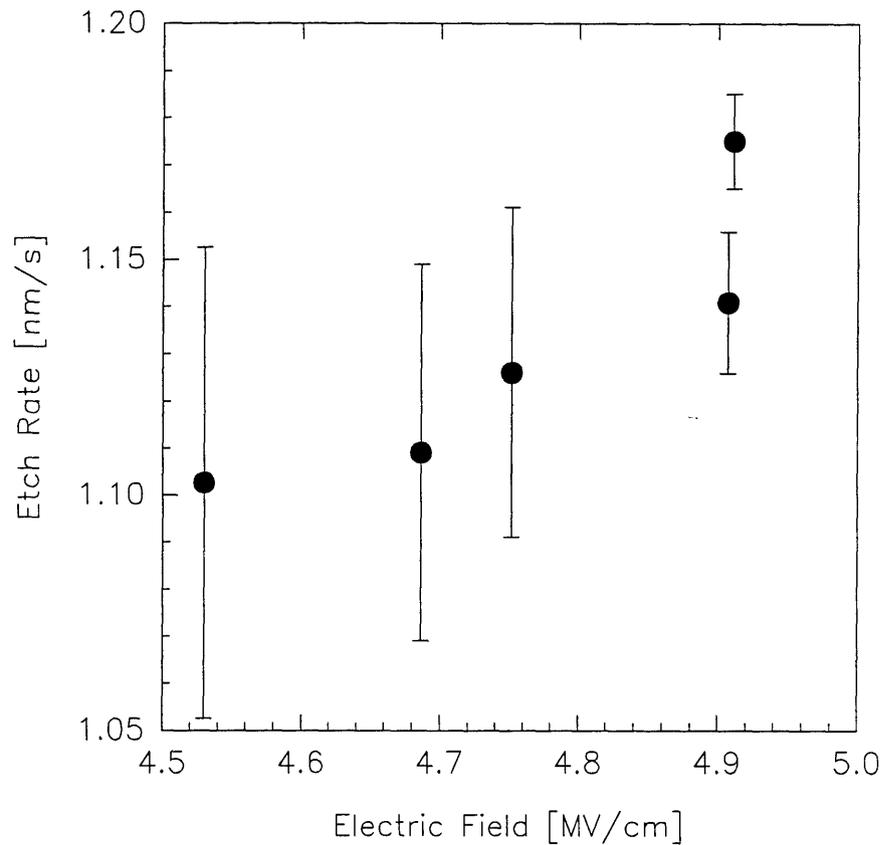
**Figure 21 Etch rate measurement procedure**



**Figure 22 3-D scanned image of a step**

### **Results and Analysis**

As shown in figure 23, there is a correlation between the etch rate and the shift in the tunneling regime with respect to the thermal oxide. As expected, there is a direct correlation as the increase in etch rate corresponds to more stoichiometric oxide which in turn corresponds to bigger value of the electric field at the chosen current density. The correlation factor between the two is 0.89. Big error bars correspond to bigger spread in the tunneling characteristics.



**Figure 23 Correlation between etch rate and electric field**

There are factors which affect the resulting correlation between the non-stoichiometry and the tunneling characteristics. The first factor is interface roughness.[34] As discussed in the section on silicon-island density, interface roughness may cause field-enhancement at asperities. This effect would be greater in negative polarity. In positive polarity, field-enhancement due to interface roughness, if any, would be small in magnitude compared to field-enhancement due to silicon islands. This is due to the sharper edges of silicon islands. In negative polarity, there are no islands that cause field-enhancement. Thus, field-enhancement due to interface roughness could be a bigger factor affecting the fowler-nordheim tunneling of buried oxide.

Second source of error might be in the methodology used to extract the shift in tunneling regime. Many devices are used in order to construct a complete tunneling curve. If the devices have vastly different BOX non-stoichiometry, then the curve will not

be smooth but contain noise. The far-left curve in the figure 19 shows that this noise could be big. Presence of noise makes it harder to pick a current density value which will give a representative value of the shift in electric-field for that die. Depending on the current density value chosen, different device characteristics become the representative of the die and change the correlation.

This source of error is in the possible non-uniform etching of BOX. As the concentration of BOE may differ from one region to another, BOX may etch non-uniformly from sample to sample, resulting in an inaccurate etch rate measurement.

## Summary

In response to the need for a comprehensive technique for SIMOX Buried Oxide metrology, an electrical technique utilizing high-field conduction model is developed. Materials parameters such as silicon island density and BOX non-stoichiometry are extracted from J-E characteristics of BOX. They are then compared to physically measured values. Although the correlation is not perfect due to possible sources of error, the result shows that the developed technique has the potential to be used as an in-line process monitor for the quality of SIMOX BOX.

The electrical testing has many further applications such as mapping out silicon island density variation across a wafer as well as BOX non-stoichiometry across a wafer. Figure 24 shows a contour plot of a standard single-implant SIMOX which shows an electric field at a given current density. This can be translated into a map of BOX non-stoichiometry where high value of electric field corresponds to more stoichiometric oxide.

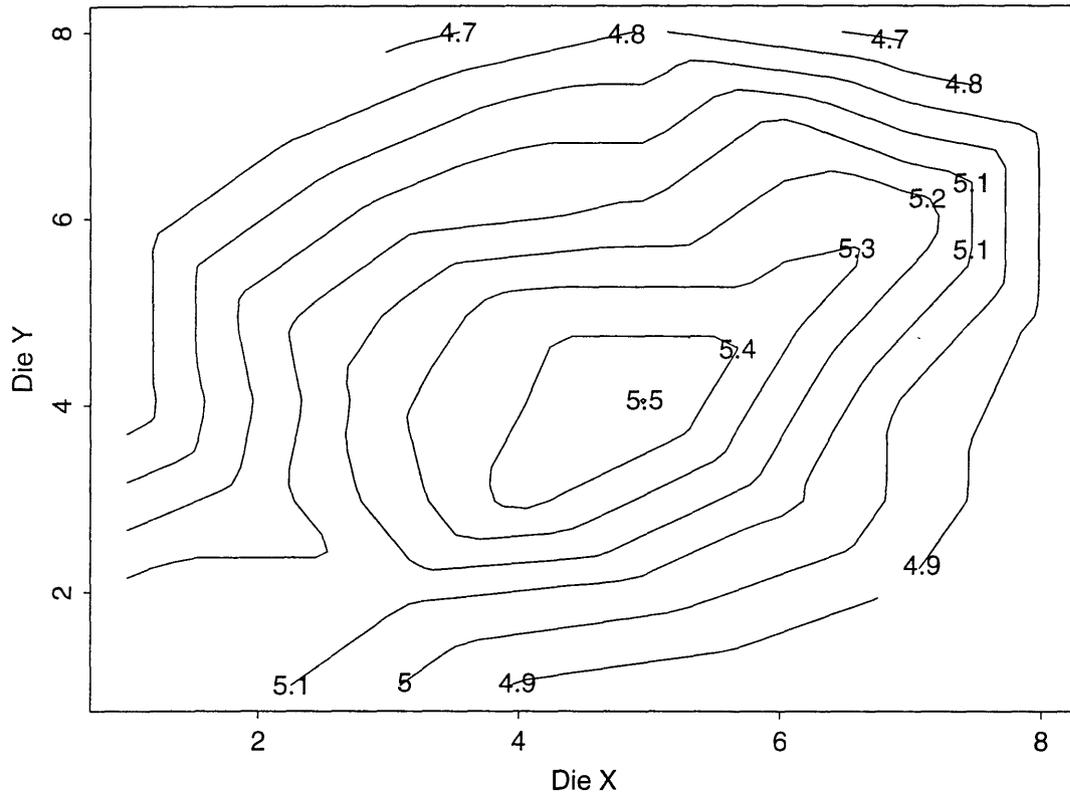


Figure 24 Wafer map of electric field at  $J = 1 \times 10^{-7} \text{ A/cm}^2$

## Appendix A

### *SIMOX Buried-Oxide Capacitor Process Traveler*

Step No.	Step Description
<b>1</b>	<b>Screening Oxide</b> Deposit a layer of oxide to control implant depth
<b>2</b>	<b>Ion Implantation of Dopant</b> 1016 ions/cm <sup>2</sup> BF <sub>2</sub> at 40 keV to degenerately dope the top silicon
<b>3</b>	<b>Wet Oxide Etch</b> DI rinse and BOE dip until oxide dewets
<b>4</b>	<b>Pattern Silicon Electrode</b> Photolithography step involving photoresist application and patterning of the resist
<b>5</b>	<b>Plasma Silicon Etch</b> Remove the exposed silicon
<b>6</b>	<b>Resist Strip</b> Strip away the photoresist
<b>7</b>	<b>N<sub>2</sub> Anneal</b> Anneal wafer at high temperature for redistribution and electrical activation of dopants
<b>8</b>	<b>HF dip</b> Dip in HF for surface cleaning

## Appendix B

### Wafer Specifications

#### Sample 1 : 1309-2 from Ibis Technology Corp.

Origin	MEMC
Size	4"
Orientation	<100>
Type	P
Resistivity (Wcm)	10.0 to 20.0
Preheat Substrate Temperature (°C)	460
Actual Substrate Temperature (°C)	650
Dose ( $10^{18}\text{cm}^{-2}$ )	1.73
Energy (keV)	200
Beam Current (mA)	38.5
Anneal Temperature (°C)	1310
Anneal Time (hr)	5.00
Average Si Thickness (A)	2267
Si Uniformity (+-A)	4.4
Average SiO <sub>2</sub> Thickness (A)	3863
SiO <sub>2</sub> Uniformity (+-A)	5.9

#### Sample 2: L507 from Soitec

Origin	MEMC
Size	4"
Orientation	<100>
Type	P
Resistivity (Wcm)	14-22
Oxygen	Medium
Time (hr)	6:21
Substrate Temperature (°C)	>600
Energy (keV)	190
Dose ( $10^{18}\text{cm}^{-2}$ )	1.78
Anneal Temperature (°C)	1320
Anneal Time (hr)	6
Average Si Thickness (A)	2046
Si Uniformity (Max-Min) (A)	30
Average SiO <sub>2</sub> Thickness (A)	4018
SiO <sub>2</sub> Uniformity (Max-Min) (A)	46

**Multiple Implant: L868 from Soitec**

Origin	MEMC
Size	4"
Orientation	<100>
Type	P
Resistivity (Wcm)	14.0 -22.0
Oxygen	Medium
Time (hr)	6:47 triple implant
Substrate Temperature (°C)	> 600
Energy (keV)	190
Dose ( $10^{18} \text{cm}^{-2}$ )	1.79
Uniformity Dose (Max-Min) (%)	1.2
Anneal Temperature (°C)	1320
Anneal Time (hr)	6
Average Si Thickness (A)	2071
Si Uniformity (Max-Min) (A)	31
Average SiO <sub>2</sub> Thickness (A)	3856
SiO <sub>2</sub> Uniformity (Max-Min) (A)	33

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## **Biographical Note**

Jung Uk Yoon was born in Suwon, Republic of Korea on December 9th, 1971. He grew up in Korea until 1985 when he came to the United State of America. He graduated from Forest Hills High School and went on to major in materials science and engineering at Cornell University. Having graduated from Cornell with B.S. in May, 1993, he came to MIT. He has been studying SIMOX materials under professor James E. Chung.

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