Coupled-Magnetic Filters with Adaptive Inductance Cancellation

by

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Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

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Abstract

Conventional filter circuits suffer from a number of limitations, including performance degradation due to capacitor parasitic inductance and the size and cost of magnetic elements. Coupled-magnetic filters have been developed that provide increased filter order with a single magnetic component, but also suffer from parasitic inductance in the filter shunt path due to imperfectly-controlled coupling of the magnetics. This document proposes a new approach to coupled-magnetic filters that overcomes these limitations. Filter sensitivity to variations in coupling is overcome by adaptively tuning the coupling of the magnetic circuit with feedback based on the sensed filter output ripple. This active coupling control enables much greater robustness to manufacturing and environmental variations than is possible in the conventional coupled-magnetic approach, while preserving its advantages. Moreover, the proposed technique also adaptively cancels the deleterious effects of capacitor parasitic inductance, thereby providing much higher filter performance than is achievable in conventional designs. The new technique is experimentally demonstrated in a dc/dc power converter application and is shown to provide high performance.

Thesis Supervisor: David J. Perreault Title: Associate Professor of Electrical Engineering and Computer Science

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Chapter 1 Introduction

1.1 Background

Electrical filters are an integral part of most electronic systems, and are particularly important in power electronics. Control of switching ripple is the primary factor in sizing the magnetics and filter components that comprise much of the size, mass, and cost of a power converter. Design techniques that mitigate converter ripple are therefore valuable for reducing the size of power electronics and the amount of electromagnetic interference (EMI) that is generated.

The low-pass filters used in power electronics typically employ capacitors as shunt elements and magnetics, such as inductors, as series-path elements. The attenuation of a filter stage is determined by the amount of impedance mismatch between the series and shunt paths. Minimizing shunt-path impedance and maximizing series-path impedance at high frequencies are thus important design goals. An important limitation of conventional filters is the effect of filter capacitor parasitic inductance, which increases shunt path impedance at high frequencies [1–5], illustrated in Figure 1.1 (courtesy of T.C. Neugebauer).



Figure 1.1: Typical capacitor high-frequency model, (a), the impedance magnitude plot for the high-frequency capacitor model, (b), and the measured impedance magnitude for an X-type (safety) capacitor (Beyschlag Centrallab 2222 388 24 224, 0.22 μ F, 275 V_{ac}), (c).

Introduction

Common methods for overcoming the deteriorated filter performance caused by capacitor parasitic inductance include placing various types of capacitors in parallel to cover different frequency ranges and increasing the order of the filter network. Both approaches increase filter size and cost.

The size of magnetic components is also of importance, particularly in multi-section filters, such as that illustrated in Figure 1.2. One technique that has been explored for reducing magnetic component count and size is the use of coupled magnetics (e.g. by realizing inductors L_A and L_B in Fig. 1.2 with a coupled magnetic circuit wound on a single core). Coupled magnetics have been used with capacitors to achieve "notch" filtering [6–9], as well as so-called "zero-ripple" filtering [10–14]. Despite the name "zero-ripple," it has been shown that the performance of of these coupled-magnetic filters is equivalent to filters without magnetically-coupled windings [10, 11]. The advantage of coupled-magnetic filters is that they enable a high-order filter structure to be realized with a single magnetic component. However, they suffer from their dependence on very precise coupling within the magnetic circuit. Any mismatch in this coupling, such as that induced by small material or manufacturing variations, temperature changes, or variations in operating point, can dramatically reduce ripple attenuation. The sensitivity of this approach to magnetic coupling has limited its value in many applications, despite its other advantages.



Figure 1.2: Example of a multi-section filter.

1.2 Objectives and Motivation

The work of this thesis introduces a new approach to coupled-magnetic filters that overcomes the limitations described above. Filter sensitivity to variations in coupling is overcome by adaptively tuning the coupling of the magnetic circuit with feedback based on the sensed filter output ripple. The major objectives of the work presented herein include:

- Design and implementation of an adaptive coupled-magnetic filter.
- Development of a control strategy for the proposed adaptive inductance cancellation method.

• Implementation of the control method and its experimental validation.

As will be shown, the proposed active coupling control enables much greater robustness to manufacturing and environmental variations than are possible in the conventional coupledmagnetic approach, while preserving its advantages. Moreover, the proposed technique also adaptively cancels the deleterious effects of capacitor parasitic inductance, thereby providing much higher filter performance than is achievable in conventional designs.

1.3 Thesis Organization

This document is organized as follows: Chapter 2 describes the principles underlying the proposed filters, including active coupling control and its use in capacitor-path inductance cancellation. Chapter 3 presents the prototype coupled-magnetic filter in a dc/dc converter application. The adaptive control technique used to maintain high performance across operating conditions and simulation of the control methods are described in Chapter 4. The implementation of the adaptive inductance cancellation control circuitry is detailed in Chapter 5. Chapter 6 presents the experimental results illustrating the high performance of the cancellation approach and the comparison of the adaptive coupled-magnetic filter to conventional filter designs. Finally, Chapter 7 summarizes and concludes the work presented herein.

Chapter 2

Adaptive Coupling Control and Parasitic Inductance Cancellation

2.1 Introduction

This chapter presents the principles of active coupling control and adaptive inductance cancellation. Conventional coupled-magnetic filters are discussed in Section 2.2 and the limitations of using such filters are described in Section 2.3. An overview of the principles behind active coupling control and the proposed adaptive inductance cancellation approach is presented in Section 2.4.

2.2 Coupled-Magnetic Filters

Coupled magnetic filters can be built using two windings on a single core. Two possible implementations of such a coupled magnetic device are depicted in Figure 2.1. In both configurations, each winding links flux with itself and mutually with the other winding. The coupling is designed to yield the desired performance.



Figure 2.1: Coupled magnetic windings in a center-tapped, (a), and end-tapped, (b), connection.

Electromagnetic analysis of the magnetic circuit of Fig. 2.1b, for example, leads to the following description [2,3]:

$$\begin{bmatrix} \lambda_1 \\ \lambda_2 \end{bmatrix} = \begin{bmatrix} \frac{N_1^2}{\Re_{11}} + \frac{N_1^2}{\Re_M} & \frac{N_1 \cdot N_2}{\Re_M} \\ \frac{N_1 \cdot N_2}{\Re_M} & \frac{N_2^2}{\Re_{22}} + \frac{N_2^2}{\Re_M} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$
$$= \begin{bmatrix} L_{11} & L_M \\ L_M & L_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}$$
(2.1)

in which λ_1 and λ_2 are flux linkages (the time integrals of individual coil voltage), i_1 and i_2 are individual coil currents, N_1 and N_2 are the number of turns in each coil, and \Re_{11} , \Re_{22} , and \Re_M are the self and mutual magnetic reluctances. An equivalent circuit model can be obtained from the two-port description, as illustrated in Figure 2.2. Details of the mathematical analysis used to obtain the model may be found in [5].

Traditionally, coupled magnetic filters of this type are designed to make inductance $L_{\rm C}$ of Figure 2.2 ideally zero. The coupled magnetic element can then provide two inductances in a multi-section filter such as that of Fig. 1.2, without contributing inductance to the shunt path. However, zeroing of the shunt-path inductance, $L_{\rm C}$, requires very preciselycontrolled coupling between the two windings, which is difficult to achieve in practice. Consequently, such circuits are sometimes designed to make the effective inductance, $L_{\rm C}$, somewhat negative and an external trimming inductor is used to try to null the total shuntpath inductance [12,13]. Even with such design tricks, inductance variations with operating conditions and part-to-part variations make it impossible to completely null the shunt-path inductance.



Figure 2.2: Equivalent circuit "T-model" for the magnetically-coupled windings of Fig. 2.1.

To fully appreciate the notion of trimming the shunt-path inductance, it is useful to revisit the magnetic circuit model (2.1). Energy conservation considerations dictate the following condition:

$$L_M \leq \sqrt{L_{11}L_{22}} \tag{2.2}$$

which states that the mutual inductance between the windings must be less than or equal to the geometric mean of the two self-inductances. However, the mutual inductance may still be larger than one of the self-inductances, in which case one branch of the T-network (the L_C branch in the context of this document) appears to have a negative inductance. It must be stressed that this does not violate any physical laws since the inductance seen across any two terminals of the T-model is clearly positive. Thus, when L_C of Fig. 2.2 is made slightly negative, the trimming inductor can be used to bring the overall shunt-path inductance to zero.

2.3 Practical Limitations of Conventional Coupled-Magnetics Designs

Unfortunately, the coupled-magnetic strategy described in the previous section is not robust, as it is very sensitive to changes in operating conditions, such as small material or manufacturing variations, temperature changes, and flux levels. Furthermore, even in the ideal case of precise coupling, an additional limitation to high frequency filter performance is the parasitic inductance of the shunt-path capacitor. While the effects of parasitic inductance are significant, the value of this inductance is quite small – approximately 10 - 50 nH for typical capacitors used in power electronics applications [2, 3]. Generally, these values are well below the practical limits of trimming the shunt-path inductance.

2.4 Adaptive Coupling Control

This section presents the use of adaptive magnetic coupling control to maintain low shuntpath inductance under all operating conditions. Feedback control is used to maintain coupling precisely at the point that optimizes attenuation performance, thereby overcoming the limitations of conventional designs. In principle, coupling control may be achieved by adding an auxiliary winding to the coupled magnetic device, which would serve to drive part of the magnetic core a controlled amount into saturation, thereby controlling coupling [15–18]. However, for simplicity the experimental work here uses a small separate electronically-controlled trimming inductor in the shunt path of the filter. Direct extensions to a fully-integrated implementation realized on a single core are clearly possible.

This electronically-controlled trimming inductor is realized as a cross-field reactor consisting of two magnetically-orthogonal sets of windings on the same core (Fig. 2.3). When the windings are positioned in this way, there is no mutual magnetic coupling between them. One of the windings carries the shunt-path ripple current, while the other carries a controlled DC current. The control current is used to drive the magnetic core partly into saturation, thereby changing the permeability of the core. Effectively, this changes the inductance seen in the signal path, and the device acts as an electronically-controlled variable inductor. The measured inductance vs. control current of the cross-field reactor used in the prototype system (described in Chapters 3 and 5) is shown in Fig. 2.4.

The cross-field reactor then allows control of the overall shunt-path inductance of the filter. In this way, it is possible to not only compensate for coupling mismatch of the coupled magnetic device, but to also cancel the parasitic inductance of the capacitor. Moreover, by measuring output ripple performance and placing the coupling under closed-loop control, attenuation can be maximized under all operating conditions. The control strategy for the proposed active tuning approach is detailed in Chapter 4. Experimental results demonstrating the high performance of this approach are presented in Chapter 6.



Figure 2.3: Structural diagram of a cross-field reactor. A single magnetic core is wound with two orthogonal windings, a toroidal coil and annular coil, which are not magnetically coupled.



Figure 2.4: Effects of varying control current on the cross-field reactor inductance.

Chapter 3 Prototype System

3.1 Introduction

The control strategy proposed in Chapter 4 is presented in the context of a switching dc/dc power converter. A buck converter was chosen to validate the proposed control strategy. This chapter presents the prototype buck converter having a coupled-magnetic output filter, as illustrated in Figures 3.1 and 3.2 and Tables 3.1 and 3.2. Section 3.2 describes the prototype buck converter, Section 3.3 presents the design guidelines for the adaptive coupled-magnetic filter, and Section 3.4 describes the buck converter voltage regulation.

3.2 Prototype Buck Converter

The buck converter operates under averaged current-mode control at a switching frequency of 400 kHz, and is designed to regulate the output at 14 volts (V) from a nominal input of 42 V. This conversion function is relevant to some emerging automotive applications, for example [19]. The converter is designed to support a load range of 16 watts (W) to 65 W. The complete buck converter schematic is presented in Appendix A.

In addition to the coupled-magnetic element (described in detail in Section 3.3), the output filter comprises capacitors C_1 and C_2 . C_1 is implemented as a 10 μ F high-ripple, low-



Figure 3.1: Circuit schematic of the buck converter and output filter.



Figure 3.2: Model of buck converter and coupled magnetic filter.

inductance film capacitor (ITW Paktron 106K050CS4). C₂ is implemented as a parallel combination of a 20 μ F polypropylene capacitor (Cornell-Dubilier 935C1W20K), a 2200 μ F electrolytic capacitor (50V, R_{ESR} = 0.040 Ω), and a 0.1 μ F ceramic capacitor. The large electrolytic capacitor appears resistive at frequencies of several kHz, and it was added to the output filter to provide additional damping to the inner and outer control loops at these frequencies. The capacitance comprises the electrolytic capacitor DC model, while its parasitic resistance, R_{ESR} comprises the AC model (Appendix A, Section A.4). Furthermore, the capacitor also helps to provide additional holdup capacitance at the output. The non-magnetic output filter components are summarized in Table 3.1.

Additionally, a large 27 mF electrolytic capacitor was placed in parallel with the load (physically away from the converter output). This was done to represent the behavior of the battery that would be present in an automobile, for example, or the hold up capacitor that appears in many applications. Because this capacitor is in parallel with the remote load, away from the actual converter output, it does not have a significant impact on the converter output switching ripple or serve to attenuate EMI. The capacitor does, however, provide low-frequency voltage holdup during load transients.

3.3 Output Filter Design Using a Coupled-Magnetic Device with Adaptive Inductance Cancellation

The end-tapped configuration of the coupled-magnetic device (Fig. 2.1b) was chosen and implemented with the two windings separated on the bobbin in such a way as to minimize the capacitance across them. One winding was wound on the top half, while the other was wound on the bottom half of the bobbin. An RM10/I A315 3F3 core was used to construct the coupled-magnetic device. A turns ratio of 5:4 (N_{DC} : N_{AC} of Fig. 3.1) was used. For the DC winding, AWG 12 wire was used, and for the AC winding, Litz 175/40 wire was used.

C ₁	$10 \ \mu F$	ITW Paktron 106K050CS4
C_2	$20 \ \mu F$	Cornell-Dubilier 935C1W20K
(parallel combination)		100V, Polypropylene
	$2200 \ \mu F$	Electrolytic, 50 V
		$(R_{\rm ESR} = 0.040\Omega)$
	$0.1 \ \mu F$	Ceramic
Q	IRF1010E	N-Channel Power Mosfet
D	MUR3020WT	Common Cathode Diode

Table 3.1: Device parameters for the buck converter of Fig. 3.2 (magnetics are detailed in Section 3.3 and Table 3.2).

The resulting coupled-magnetic device parameters are listed in Table 3.2. Experimental measurements indicate that the windings appear inductive for frequencies up to ~ 11 MHz.

The variable inductor was designed such that its tunable range captured the inductance to be cancelled, namely the sum of the shunt-path inductance of the coupled-magnetic device and the parasitic inductance of the shunt-path capacitor. Construction of the variable inductor was as follows: two turns of the coupled-magnetic AC winding were wound conventionally on the bobbin of a P14/8 A315 3F3 core. The smallest size core within the practical design guidelines was desired. Thus, the smallest core that was able to handle the maximum ripple current and provide the proper tunable inductance range was chosen.

The control winding was constructed using 77 turns of AWG 28 wire wound through the center-post hole of the core (orthogonally to the inductance winding), as illustrated in Fig. 3.3. In order to reduce the control current required to partially saturate the variable inductor core, a high number of turns for the control winding was used. In principle, the geometry of the core is the main constraint for the maximum number of windings that can be added.

Magnetics	Tuned Coupled Magnetic Filter	
Construction	RM10/I, A315, 3F3 Core	
	5:4 Turns	
L _A	$6.13 \ \mu \mathrm{H}$	
L _B	$1.67 \ \mu \mathrm{H}$	
L _C	- 0.82 μH	

Table 3.2: Design parameters for the coupled-magnetic device. Inductances L_A , L_B , and L_C correspond to those in Fig. 3.2.



Figure 3.3: Variable inductor.

3.4 Buck Converter Output Voltage Regulation

The buck converter is designed to regulate the output voltage at 14 V from a nominal input of 42 V. Averaged current-mode control is used to achieve the desired regulation. The following figures illustrate the dynamics of the buck converter control circuitry. The full mathematical assessment of stability is presented in Appendix A. Figures 3.4 - 3.6 illustrate the control behavior prior to the addition of the large electrolytic capacitor damping leg. On the contrast, Figures 3.7 and 3.8 present the open loop dynamics of the converter inner and outer control loops following the addition of the capacitor. It can be seen from the open-loop Bode plots that both loops are now much better damped. The inner control loop has a phase margin greater than 60 degrees and a gain margin greater than 20 dB, while the outer loop has a gain margin greater than 40 dB and a phase margin greater than 90 degrees. Thus, as can be seen in Fig. 3.9, the overall closed-loop response is well-behaved. The closed-loop poles and zeros of the buck converter control transfer function are shown in Table 3.3. Without the damping provided by the electrolytic capacitor, the system was stable, but small ($\sim 20 \text{ mV}$) ringing could typically be observed at the output, indicating poor damping. The loop transfer functions and the mathematical analysis used to describe the converter dynamics are presented in Appendix A.

Closed-Loop Poles [Hz]	Closed-Loop Zeros [Hz]
- 8.55	- 8.54
- 71.21	$-2.12 \cdot 10^4$
$-7.17 \cdot 10^3$	$-9.41 \cdot 10^4$
- 4.47 \pm 8.76 \cdot 10 ³ j	- $4.32 \pm 14.88 \cdot 10^5$ j
- 2.45 $\pm \ 48.55 \cdot 10^3 \ {\rm j}$	
$-2.09 \cdot 10^4$	
$-9.40 \cdot 10^4$	

Table 3.3: Poles and zeros of the closed-loop buck converter control transfer function.



Figure 3.4: Open-loop frequency response of the buck converter inner control loop prior to the addition of the large electrolytic capacitor.



Open–Loop Frequency Response for the Converter Outer Loop

Figure 3.5: Open-loop frequency response of the buck converter outer control loop prior to the addition of the large electrolytic capacitor.



Figure 3.6: Closed-Loop frequency response of the buck converter control loop prior to the addition of the large electrolytic capacitor.



Figure 3.7: Open-loop frequency response of the buck converter inner control loop following the addition of the electrolytic capacitor damping leg.



Open-Loop Frequency Response for the Converter Outer Loop

Figure 3.8: Open-loop frequency response of the buck converter outer control loop following the addition of the electrolytic capacitor damping leg.



Closed-Loop Frequency Response of the Converter Control Loop

Figure 3.9: Closed-Loop frequency response of the buck converter control loop following the addition of the electrolytic capacitor damping leg.
Chapter 4 Adaptive Control Methods

4.1 Introduction

The proposed adaptive inductance cancellation method relies on feedback control. The adaptive controller is presented here in the context of the buck converter described in Chapter 3. Sections 4.2 and 4.3 describe the mathematical control model for the adaptive tuning approach, while Section 4.4 describes the simulation used to verify the efficacy and the stability of the approach and presents the simulation results.

4.2 Control Strategy

The proposed design approach uses feedback control based on sensed buck converter output ripple to maintain good performance. The controller measures the root-mean-square (RMS) of the converter output ripple voltage (V_{ripple}^{RMS}) and electronically tunes the inductance of the cross-field reactor to minimize the ripple seen at the filter output. A Lyapunov control strategy similar to those described in [8, 20–22] has been implemented. The block diagram of Figure 4.1 illustrates the basic control strategy employed.



Figure 4.1: Simplified closed-loop adaptive inductance tuning model.

The control method is integral in nature. The controller generates a small, exogenous, low frequency sinusoidal variation in the cross-field reactor control current that controls the shunt-path inductance. This consequently results in small variations in V_{ripple}^{RMS} as the shunt-path inductance varies. The controller then correlates the changes in V_{ripple}^{RMS} with the sinusoidal variation in $I_{control}$ by multiplying the two and integrating the product. When the average value of the product is negative, $I_{control}$ is below the optimal operating point and the integral is driven to increase $I_{control}$. Conversely, when the average value of the product is positive, $I_{control}$ is above the optimal operating point and the integral of the product drives $I_{control}$ down. At the optimal operating point, the average value of the integrator input is ideally zero and the operating point is maintained.

The small sinusoidal signal is added to the negated output of the integrator and the sum is used as the control current to the variable inductor. This control strategy drives the DC component of the control current to the minimum of the V_{ripple}^{RMS} vs. I_{control} function, where the integral output holds constant. The control method assumes that the RMS value of the output ripple as a function of I_{control} is unimodal in the range of interest. Experimental measurements confirm this assumption for the prototype system described in Chapter 3 (Fig. 4.2). The close-fitting 4th order polynomial helps to further demonstrate the unimodal behavior of the function on the control current range of interest.



Figure 4.2: Scaled V_{ripple}^{RMS} as a function of the variable inductor control current for the prototype system (as measured at the output of AD637 of Fig. 5.2) and its 4th order polynomial fit.

The function of Fig. 4.2 was obtained by manually controlling the value of the cross-field reactor control current and measuring V_{ripple}^{RMS} . A power supply was used to inject the desired amount of DC control current into the control windings. V_{ripple}^{RMS} was measured using the AD637 RMS-DC converter IC located on the adaptive cancellation controller board (described fully in Chapter 5). The scaling factor of 148.3 at the switching frequency reflects the gain of the high-pass filter stage at the input of the AD637 (Fig. 5.2).

4.3 Stability Analysis of the Control Method

The proposed control approach is inherently stable. Consider the local average dynamics [23] of the system in Fig. 4.1 over an averaging period of the sinusoidal variation:

$$\frac{d\bar{\imath}_{cntrl}(t)}{dt} = \frac{-k}{T} \int_{t-T}^{t} \left(\widehat{I}sin(\omega\tau) + f(\widehat{I}sin(\omega\tau) + i_{cntrl}(\tau)) \right) d\tau$$
(4.1)

Observing the function $f(\bar{\imath}_{cntrl}(t)) = V_{ripple}^{RMS}$ of Fig. 4.2 and the control function of Eq. 4.1, it is evident that at the minimum of f, $\frac{d\bar{\imath}_{cntrl}(t)}{dt}$ tends to zero. Thus, the minimum of the V_{ripple}^{RMS} vs. $\bar{\imath}_{cntrl}(t)$ function, \hat{i}_{cntrl} , is an equilibrium point of the system.

On the region of the state-space that contains the equilibrium point, the requirements for a Lyapunov function, $V(\bar{\imath}_{cntrl}(t))$, are the following [24]:

- 1. V must be continuous.
- 2. V must have a unique minimum at \hat{i}_{cntrl} .
- 3. The value of V must not increase along any trajectory of $\bar{i}_{cntrl}(t)$ on the state-space that contains \hat{i}_{cntrl} .

Consider the function $f(\bar{\imath}_{cntrl}(t)) = V_{ripple}^{RMS}$ as the Lyapunov function of the system. Figure 4.2 confirms that the function meets the first two requirements. To demonstrate that the third requirement is also satisfied, consider the control strategy of Fig. 4.1 and Eq. 4.1. Taking the local average output of the integrator as the state variable of interest, it is observed that the trajectories of $\bar{\imath}_{cntrl}(t)$ can only tend toward the minimum, forcing V to decrease. Therefore, the function $f(\bar{\imath}_{cntrl}(t)) = V_{ripple}^{RMS}$ of Fig. 4.2 is a Lyapunov function of the system and \hat{i}_{cntrl} is a stable equilibrium point.

4.4 Simulation

To validate the efficacy of the control strategy, a time domain simulation of the approach was implemented in Simulink (Mathworks Inc., Cambridge, MA) as shown in Fig. 4.3. The complete Simulink implementation of the control approach is illustrated in Appendix B. A simplified average state-space model was developed for the buck converter (described more fully in Section 4.4.1), and is represented by the $I_{control}$ to V_{ripple} block. The effects of varying the control current on the value of the variable inductance were determined empirically and modeled with a close-fitting 5th order polynomial (Fig. 2.4). Transfer function blocks reflecting the dynamics and characteristics of circuit components to be used in the design of the physical control circuitry (Chapter 5) were derived for the controller. The model was then used to assess the dynamic performance of the controller.



Figure 4.3: Simulink model of the proposed control control strategy.

4.4.1 Buck Converter State-Space Model

The simplified model of the buck converter, shown in Fig. 4.4, was used to develop the state-space model used in Simulink. An average state-space model was used to simulate the dynamics of the converter. The buck converter input filter was ignored, as it was designed in such a way as its dynamics did not interfere with those of the rest of the converter. Only the essential components of the output filter were included, and the parasitics present in the system were ignored for the purposes of the model. The average voltages across the two capacitors, v_{C1} and v_{C2} , and the average currents through the inductances L_A and L_C were chosen as the state variables.

The signal V_d represents the voltage seen at the diode cathode (Fig. 3.2). This signal is



Figure 4.4: Simplified time-averaged model of the buck converter used to obtain the statespace model of Eq. 4.2.

modeled as a square pulse with the frequency of 400 kHz, which corresponds to the converter operating frequency, an amplitude of 42 V corresponding to the nominal converter input voltage, and a duty ratio of $\frac{1}{3}$, which provides the 42 V to 14 V conversion function. The passive components reflect the converter output filter, and their values are detailed in Tables 3.1 and 3.2. It must be noted, however, that the output filter capacitor C₂ does not include the 2200 μ F electrolytic capacitor damping leg or the 0.1 μ F ceramic capacitor. The value of 8 Ω was used for R_L, corresponding to 35% of converter maximum power. From the model of Fig. 4.4, the following state-space description of the converter was obtained:

$$\begin{bmatrix} \mathbf{i}_{A} \\ \mathbf{i}_{C} \\ \mathbf{v}_{C1} \\ \mathbf{v}_{C2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-L_{B}}{L_{A}L_{B} + L_{A}L_{C} + L_{B}L_{C}} & \frac{-L_{C}}{L_{A}L_{B} + L_{A}L_{C} + L_{B}L_{C}} \\ 0 & 0 & \frac{-(L_{A} + L_{B})}{L_{A}L_{B} + L_{A}L_{C} + L_{B}L_{C}} & \frac{L_{A}}{L_{A}L_{B} + L_{A}L_{C} + L_{B}L_{C}} \\ 0 & \frac{1}{C_{1}} & 0 & 0 \\ \frac{1}{C_{2}} & \frac{-1}{C_{2}} & 0 & \frac{-1}{RC_{2}} \end{bmatrix} \begin{bmatrix} \mathbf{i}_{A} \\ \mathbf{i}_{C} \\ \mathbf{v}_{C1} \\ \mathbf{v}_{C2} \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{L_{B} + L_{C}}{L_{A}L_{B} + L_{A}L_{C} + L_{B}L_{C}} \\ \frac{L_{B}}{L_{A}L_{B} + L_{A}L_{C} + L_{B}L_{C}} \\ 0 \\ 0 \end{bmatrix} V_{d}$$
(4.2)

The model of Eq. 4.2 assumes that the variable inductance of the cross-field reactor changes slowly relative to the rest of the system. The slow time change of the variable inductance was, in fact, taken as a requirement in the design of the adaptive cancellation control circuitry. The use of the slow-varying (500 Hz) sinusoidal signal to sweep the V_{ripple}^{RMS} vs. I_{control} function and the integrator in the feedback path (Fig. 4.3) forced the dynamics of the control to be slow compared with the dynamics of the converter. This design strategy ensured that the variable inductor included in the output filter of the buck converter could indeed be treated as time-invariant for the purposes of the buck converter dynamics. Thus, it was included in the overall shunt-path inductance, L_C. The Simulink diagram of the model in Eq. 4.2 is shown in Appendix B.

4.4.2 Simulation Parameters

The final simulation model of Appendix B was used to assess the dynamics and stability of the control strategy, with the following simulation parameters:

Simulation Time	0 - 0.5 seconds
Fixed Step Size	$2.5 \cdot 10^{-8}$ seconds
Solver Method	ode5 (Dormand-Prince)
Stored Data Decimation Rate	10000

Table 4.1: Control model simulation parameters.

The largest allowable step size was chosen for the simulation. The switching frequency of the buck converter, reflected in the input variable V_d of Fig. 4.4 and the pulse of Fig. B.2 provided the upper boundary on the magnitude of the step size. The simulation data were decimated by a factor of 10000 due to the large size of the files provided by simulation. This forced signals such as the converter output ripple to appear undersampled. However, since the dynamics of the adaptive cancellation control are on the time scale of hundreds of milliseconds, the decimation did not prove detrimental to the simulation analysis. The simulation time of 0.5 seconds ensured that the system had reached steady state.

4.4.3 Simulation Results

In order to view the effects of the adaptive inductance cancellation, the converter was first allowed to reach steady state. The adaptive tuning was then enabled at time t = 0.1 seconds. This was performed by multiplying the control current by a step function with a

delay of 0.1 seconds (Fig. B.1). The simulated transient behavior of the control current, the converter output ripple, and converter V_{ripple}^{RMS} are depicted in Figs. 4.5 – 4.7.

Simulation results indicate that the proposed active tuning control method exhibits good static and dynamic behavior. A factor of 20 reduction is predicted for the converter output ripple (Fig. 4.5) and for V_{ripple}^{RMS} (Fig. 4.6) when $I_{control}$ reaches its DC steady state value of 0.53 amperes (A) (Fig. 4.7) after approximately 200 milliseconds (ms).

The simulated average steady state control current, \hat{i}_{cntrl} , matches that predicted by the manual tuning of Fig. 4.2 within the limits of the model. The converter output voltage ripple, and V_{ripple}^{RMS} , however, are predicted to be lower than experimental manual tuning results suggest. These discrepancies may be attributed to the unmodeled parasitics of the prototype system.



Figure 4.5: Simulated transient performance of the converter output ripple as active tuning is enabled at time t = 0.1 seconds.



Figure 4.6: Simulated transient performance of the RMS of the converter output ripple, V_{ripple}^{RMS} , as active tuning is enabled at time t = 0.1 seconds.



Figure 4.7: Simulated transient performance of the variable inductor control current as active tuning is enabled at time t = 0.1 seconds.

Chapter 5

Controller Implementation

5.1 Introduction

The proposed control strategy of Chapter 4 was implemented on a printed circuit board (PCB) using standard circuit components, as illustrated in Fig. 5.2. This chapter details the design of the adaptive inductance cancellation control board circuitry. Section 5.2 outlines the design guidelines for the control board and Section 5.3 describes the implementation of the control board circuitry.

5.2 Control Board Design

The diagram of Fig. 5.1 illustrates the relevant blocks of the control circuitry and the approximate signals levels at the input and output of each block. The signal levels correspond to a buck converter system having an adaptive coupled-magnetic output filter. The control current for the variable inductor is assumed to be in the range of 0.05 - 0.95 A. These conditions determine the range of the converter output ripple amplitude to be 5 - 40 mV_{pp}.

The output of the buck converter constitutes the input to the system. The differential high-pass filter serves to isolate the ripple from the converter output signal and to provide additional gain. The gain is required by the AD637 RMS-DC converter in order to ensure adequate bandwidth. The differential high-pass filter was implemented in two stages in order to yield appropriate gain and bandwidth. The resulting gain of the high-pass stage in the range of the first two harmonics of the switching frequency (400 kHz – 800 kHz) was measured to be 148.3.

In order to increase the signal-to-noise ratio at the output of the AD633 multiplier a gain of 4.73 was incorporated. A gain of -1000 (at 1 radian/sec.) was added to the integrator to increase the response speed of the system, resulting in the following transfer function: $\frac{-1000}{s}$. The 1 – 9 V voltage limiting circuitry was added to maintain the variable inductor control current in the range of 0.05 – 0.95 amps, following the addition of the sinusoidal signal



Figure 5.1: Block diagram of the adaptive inductance cancellation control circuit.

and the scaling of the resulting sum by 0.1 during the voltage to current conversion. The variable inductor current was chosen to be in the aforementioned range because this range was experimentally confirmed to contain the minimum of the V_{ripple}^{RMS} vs. I_{control} function (Fig. 4.2).

Finally, the amplitude of the sine wave at the output of the XR2206 monolithic function generator was chosen such that it produced enough variation in the variable inductor control current signal to induce a change of $\sim 10 - 20$ mV at the output of the AD637 near the optimal operating point, \hat{i}_{cntrl} , of the V_{ripple}^{RMS} vs. $I_{control}$ function. Thus, the value of 0.5 V was chosen for the amplitude. However, in practice, a slightly smaller amplitude could also have been chosen, without negatively affecting the control performance.

5.3 Control Board Circuitry

The blocks of Figures 4.3 and 5.1 are implemented as follows: the sinusoidal variation is implemented using an XR2206 monolithic function generator. An AD637 RMS-to-DC converter is used for the RMS block and an AD633 multiplier for the product block. Addition, integration, buffering, and voltage to current conversion are performed using the LF347 quad operational amplifier. The variable inductor control current is provided using a TIP29C NPN power bipolar transistor. A zener diode and the LM317 adjustable voltage regulator serve to constrain the voltage at the output of the integrator in the range of 1 - 1

9 volts. Finally, a differential high-pass stage is added using two LM6361 wide bandwidth operational amplifiers to provide additional gain and to decouple the DC component of the output from the control circuitry. The resulting control circuit schematic is illustrated in Figure 5.2.

The circuit of Figure 5.2 was implemented on a printed circuit board using the Eagle (CadSoft Computer GmbH) layout editor. A four layer, FR4 PCB was used for the control board. The Eagle circuit schematic and the masks for each of the resulting layers of the printed circuit board are included in Appendix C.



Figure 5.2: Schematic of the control board circuitry.

Chapter 6 Experimental Results

6.1 Introduction

This chapter presents the experimental results for the adaptive inductance cancellation. The prototype buck converter of Chapter 3 and the adaptive inductance cancellation control board described in Chapter 5 were used to experimentally demonstrate the control strategy proposed in Chapter 4. Section 6.2 presents the experimental results for a buck converter having an adaptive coupled-magnetic output filter (as detailed in Chapter 3), while Section 6.3 presents the comparison of the adaptive cancellation method with conventional filter designs.

6.2 Experimental Results for Adaptive Cancellation

The tuning method was implemented using the buck converter and the adaptive coupledmagnetic device described in Chapter 3 and the control board of Chapter 5.

6.2.1 Comparison of Output Ripple Using the Adaptive Coupled-Magnetic Filter With Active Tuning Disabled and Enabled

Time and frequency domain measurements were performed for the converter operating at 35% of maximum load ($R_L = 8 \Omega$) both with adaptive inductance cancellation disabled and enabled. All time domain experimental measurements were bandwidth limited to 20 MHz, though this was not seen to have a significant impact on the results. Figures 6.1 and 6.2 illustrate a reduction of greater than a factor of 5 in the peak-to-peak output ripple amplitude when active tuning is enabled.



Figure 6.1: Measured converter output ripple using the adaptive coupled-magnetic filter with adaptive inductance cancellation disabled. Note the scale of 5 mV/division.



Converter Output Ripple with Adapative Tuning Enabled

Figure 6.2: Measured converter output ripple using the adaptive coupled-magnetic filter with adaptive inductance cancellation enabled. Note the scale of 5 mV/division.



Figure 6.3: Measured spectrum of the converter output ripple using the adaptive coupledmagnetic filter with active tuning disabled.

Measurements of the spectra of the output ripple with adaptive cancellation disabled and enabled were also made using an Agilent 4395A Network/Spectrum/Impedance Analyzer with an Agilent 1141A AC-coupled differential probe. Results reflect an improvement of approximately 16 dBuV for the first two harmonic components (Figs. 6.3 and 6.4). These components are the main contributors to time-domain ripple, and the measured results are consistent with the peak-to-peak values observed in the time domain.

6.2.2 Transient Performance of the Adaptive Cancellation

The transient performance of the adaptive inductance cancellation method was also experimentally assessed. To test the dynamic performance of the tuning, the output of the converter was allowed to reach steady state. Once steady state was reached, adaptive cancellation was enabled by turning on the power supply to the control circuitry, and experimental measurements for the variable inductor control current, the converter output ripple, and the converter output ripple RMS were made. As illustrated by Figs. 6.5 - 6.8, the maximum reduction in output ripple amplitude and output ripple RMS is achieved after approximately 100 ms when the DC component of $I_{control}$ reaches its steady state value of 0.49 A and remains stable. The experimental results illustrate that the adaptive control is stable and effective at reducing the output ripple.

Two plots of the converter output ripple RMS are presented (Figs. 6.6 and 6.7). Both



Figure 6.4: Measured spectrum of the converter output ripple using the adaptive coupledmagnetic filter with active tuning enabled.

measurements were taken at the output of the AD637 RMS-DC converter of the control board of Figs. 5.1, 5.2, and C.1. Figure 6.6 shows the converter ripple RMS scaled by the gain of 148.3 of the high-pass filter stage of the control board to reflect the RMS ripple at the converter output, while Figure 6.7 presents the unscaled RMS measurement. Comparison of Figure 6.7 to the manual tuning results of Figure 4.2 shows that the results of the active tuning are consistent with those obtained by manually tuning the variable inductor to achieve the greatest reduction in ripple amplitude.

The experimental results match the simulation predictions of Section 4.4.3 within the limits of the model. The minor differences between the simulation predictions and experiment are within the bounds expected due to modeling simplifications. For example, the optimal value of $I_{control}$ is reached faster than is predicted by simulation (Figs. 4.7 and 6.8). Likewise, the predicted reduction in ripple, as well as the peak-to-peak and RMS ripple values predicted by simulation are lower than those measured experimentally (Figs. 4.5, 4.6, 6.5, and 6.6). This is due to the fact that the simplified state-space model that was used for the converter contains only the essential components that influence the overall converter dynamics and neglects some of the parasitics present in the system. Nevertheless, it can be seen from the experimental results that the adaptive system is stable and effective at reducing power converter output ripple.



Figure 6.5: Measured transient response of the converter output ripple as active tuning is enabled. The measured signal is highly undersampled.



Figure 6.6: Measured transient response of the converter output ripple RMS as active tuning is enabled. This signal was measured at the output of the AD637 RMS-DC converter of the control board of Chapter 5 and scaled by the gain of the control board high-pass filter stage to reflect the V_{ripple}^{RMS} seen at the converter output.



Figure 6.7: Measured transient response of the converter output ripple RMS as active tuning is enabled. This signal was measured at the output of the AD637 RMS-DC converter of the control board of Chapter 5.



Figure 6.8: Measured transient response of the variable inductor control current as active tuning is enabled.

6.2.3 Load Transient Performance of the Buck Converter Having an Adaptive Coupled-Magnetic Output Filter

The performance of the adaptive tuning method was also assessed in the presence of a slow-varying load. The converter load consists of a parallel combination of a resistor and a 27 mF electrolytic capacitor, physically distant from the converter output. The large capacitor was added to represent the behavior of the battery that would be present in an automobile, for example, or the hold-up capacitor that appears in many applications. Because this capacitor is in parallel with the remote load, away from the actual converter output, it does not have a significant impact on the converter output switching ripple or serve to attenuate EMI. The capacitor does, however, provide low-frequency voltage holdup during load transients.

The load transient measurements shown in Figures 6.9 and 6.10 were performed for a load step corresponding to 35 - 70% of maximum output power. A 3% fluctuation in the converter output voltage is observed for this load transient. Additionally, experimental results under maximum load step conditions (25 - 100% step in power) show a less than 5% transient in output voltage.



Figure 6.9: Measured converter output during a 35 - 70 % of maximum power load transient.

Observing the (undersampled) switching ripple during the transient by AC coupling the output voltage measurement (Fig. 6.10), it is seen that the adaptive control is able to provide the desired ripple cancellation without undesired interactions with the output voltage control.



Figure 6.10: Measured converter output ripple during a 35 - 70 % of maximum power load transient. The ripple is measured by AC coupling of the output voltage measurement. The measured signal is highly undersampled.

6.3 Comparison with Conventional Filter Designs

For comparison purposes, two conventional output filter designs have also been implemented. The conventional designs include a standard buck converter inductor and a "zeroripple" filter. Simplified schematics for the converter and its equivalent model, Figs. 3.1, 3.2, and Table 3.1, are repeated here for convenience (Figs. 6.11, 6.12, and Table 6.1).



Figure 6.11: Circuit schematic of the buck converter and output filter.



Figure 6.12: Model of buck converter and coupled magnetic filter.

C_1	$10 \ \mu F$	ITW Paktron 106K050CS4
	$\frac{10 \mu}{20 \mu}$	Cornell Dubilior 025C1W20K
C_2	$20 \mu r$	
(parallel combination)		100V, Polypropylene
	$2200~\mu{ m F}$	Electrolytic, 50 V
		$(R_{\rm ESR} = 0.040\Omega)$
	$0.1 \ \mu F$	Ceramic
Q	IRF1010E	N-Channel Power Mosfet
D	MUR3020WT	Common Cathode Diode

Table 6.1: Device parameters for the buck converter of Fig. 6.12 (magnetics are detailed in Table 6.2).

6.3.1 Conventional Filter Designs

To provide an even comparison, the same magnetic core type was utilized in each case with similar values for the total series-path inductance $(L_A + L_B \text{ in Fig. 6.12})$. In each of the comparison cases, the non-magnetic buck converter output filter components are the same as those described in Section 3.2 and summarized in Table 6.1. The characteristics of all three magnetic component designs are shown in Table 6.2.

Magnetics	Inductor	"Zero-Ripple"	Tuned Coupled
	Filter	Filter	Magnetic Filter
Construction	RM10/I, A315	RM10/I, A315	RM10/I, A315
	3F3 Core	3F3 Core	3F3 Core
	5 Turns	5:5 Turns	5:4 Turns
L _A	$8.04 \ \mu H$	$7.70 \ \mu H$	$6.13 \ \mu \mathrm{H}$
L _B	$0 \ \mu \mathrm{H}$	$0.34 \ \mu \mathrm{H}$	$1.67 \mu \mathrm{H}$
L _C	$0 \ \mu \mathrm{H}$	$0.17 \ \mu \mathrm{H}$	- 0.82 μH

Table 6.2: Device parameters for the comparison of the three filter topologies using the buck converter of Fig. 6.12

The first conventional design is a standard buck converter inductor without coupled magnetics. In this implementation, capacitor C_1 appears in parallel with C_2 (reducing the order of the filter), but there is no coupling sensitivity in the design. The second conventional design utilizes a "zero-ripple" coupled-magnetic device in which the shunt-path inductance (L_C in Fig. 6.12) is designed to be as close to zero as possible without external trimming. It was found that a 5:5 turns ratio ($N_{DC} : N_{AC}$) provided an effective shunt-path inductance of approximately 170 nH under low flux conditions, yielding the best approximation to a "zero-ripple" design within the overall design requirements. The capacitors C_1 and C_2 are realized in the same manner as in the adaptive design described in Chapter 3.

Figures 6.13 and 6.14 show the time and frequency domain ripple measurements for the buck converter using a conventional inductor. Comparing these results to those of Figs. 6.2 and 6.4, it can be seen that the coupled-magnetic filter with adaptive inductance cancellation provides more than a factor of 10 (> 20 dB) improvement in output ripple performance as compared to a buck converter with the same passive component size.



Figure 6.13: Measured converter output ripple using a conventional inductor filter. Note the scale of 10 mV/division.



Figure 6.14: Measured spectrum of the converter output ripple using a conventional inductor filter.

It is also interesting to compare these results to the "best designed" "zero-ripple" filter, in which "shunt-path" inductance is minimized. Results from this design are shown in Figs. 6.15 and 6.16. It can be seen that the performance of this design is substantially better than that of the converter without coupled magnetics, but falls far short of those achieved with the adaptive inductance cancellation. In fact, performance of this filter (with minimized shunt-path inductance) is slightly worse than the performance of the coupled magnetics design with adaptive cancellation disabled. This is attributed to the fact that despite having a higher shunt-path impedance (without active cancellation), inductance L_B of Fig. 3.2 is higher in the design for active cancellation, thereby providing a better second filter stage. Ultimately, it may be concluded that the ripple performance of the coupledmagnetic filter with inductance cancellation is a factor of more than five better than any of the other options explored, and provides a much higher robustness to manufacturing and operating point variations owing to its use of closed-loop control.



Figure 6.15: Measured converter output using a "zero-ripple" filter. Note the scale of 10 mV/division.



Figure 6.16: Measured spectrum of the converter output ripple using a "zero-ripple" filter.

6.3.2 Performance of Filter Designs Across Varying Load Conditions

Finally, the performance of the two conventional designs and of the coupled-magnetic filter with adaptive inductance cancellation enabled and disabled is compared across varying load conditions. Figures 6.17 and 6.18 illustrate the converter output ripple and output ripple RMS for each type of filter as the load current is increased from minimum to maximum. It can be seen that the coupled-magnetic filter with adaptive inductance cancellation provides the greatest ripple attenuation across the specified prototype buck converter load range. At the maximum output power, the adaptive coupled-magnetic filter demonstrates more than a factor of three improvement over the coupled-magnetic filter with tuning disabled, a factor of five improvement over the "zero-ripple" filter, and more than a factor of eight improvement over the conventional inductor, both in the peak-to-peak converter output ripple and the output ripple RMS.





Figure 6.17: Comparison of measured peak-to-peak converter output ripple vs. load current for four output filter designs: the adaptive coupled-magnetic with active tuning enabled, with tuning disabled, the "zero-ripple" filter, and a conventional inductor.



Converter Output Ripple RMS vs. Load Current

Figure 6.18: Comparison of measured converter output RMS vs. load current for four output filter designs: the adaptive coupled-magnetic with active tuning enabled, with tuning disabled, the "zero-ripple" filter, and a conventional inductor.

It can be seen in Figs. 6.17 and 6.18 that in each filter type the peak-to-peak and RMS ripple increases with load current. This change can be attributed to a reduction in the permeability of the main filter magnetics as flux levels increase, which reduces filter attenuation. This effect is smallest in absolute terms, but largest in percentage terms, for the coupled-magnetic filter with adaptive inductance cancellation. Further increase in load current rapidly degrades the performance of the filter with active cancellation, as the small cross-field reactor used to adapt the filter begins to saturate for high ripple currents. Nonetheless, the adaptive coupled-magnetic filter provides the best ripple attenuation over the entire rated load range. Changes in performance of all the filters with the load can in principle be amended by designing the output filter magnetics to present smaller changes in inductance over the load range.

Chapter 7

Summary and Conclusions

7.1 Thesis Summary and Contributions

Conventional filter circuits suffer from a number of limitations, including performance degradation due to capacitor parasitic inductance and the size and cost of magnetic elements. Coupled-magnetic filters have been developed that provide increased filter order with a single magnetic component, but also suffer from parasitic inductance in the filter shunt path due to imperfectly-controlled coupling of the magnetics. This thesis presents a novel inductance cancellation method that overcomes the problems associated with traditional inductor and coupled-magnetics filter designs.

The major contributions of the work of this thesis include the design of an adaptive coupled magnetic filter; the development of an active inductance cancellation strategy and cancellation control methods; and the implementation and experimental validation of the adaptive inductance cancellation approach.

7.2 Conclusions

This thesis introduces coupled-magnetic filters with adaptive inductance cancellation control. The proposed approach provides a robust method of increasing filter order and canceling the effects of parasitic inductance without a substantial increase in filter size and cost. Simulation and experimental results confirm the high performance of the proposed approach in a dc/dc power converter application. It may be concluded that the proposed approach offers greatly improved ripple attenuation and robustness in circuits employing coupled-magnetic filters, and has merit where these advantages justify the needed control circuitry.

Appendix A Prototype Converter

A.1 Introduction

This appendix presents the details of the buck converter of Chapter 3 that was used to present the results of the adaptive inductance cancellation approach. In particular, Section A.2 shows the complete buck converter circuit schematic, while Sections A.3 and A.4 detail the analysis of the buck converter control circuitry.

A.2 Buck Converter Circuit

The prototype buck converter was designed using Protel 99 SE (Altium Ltd., Sydney, Australia) PCB layout software. A four-layer, FR4 board, having a ground and a power plane, was used for the converter layout. The final buck converter Protel schematic is shown in Fig. A.1. The printed circuit board that was used in the prototype contained four of the converter modules of Fig. A.1, which were once used in a four-stage buck converter design [25]. Only a single module was used for the testing of the adaptive inductance cancellation methods. Components, C_3 ', C_3 ", C_{10} , C_{21} , R_{17} , R_7 , R_8 , R_9 , and U_1 were added following the manufacture of the board. Additionally, although space was provided on the board for the damping resistors R_3 and R_4 , these resistors were not used. The bill of materials used in the assembly of the buck converter is shown in Table A.1.



Figure A.1: Protel schematic of the prototype buck converter.

Prototype Converter

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Num.	Part Type	Designator	Footprint	Description
1	.68 uF	C14	CAP100/28/50	Capacitor
2	$0.1 \mathrm{uF}, 100 \mathrm{V}$	C34	CAP200/28/150	Capacitor
3	$0.1 \mathrm{uF}$	C3'	AXIAL-0.3	Ceramic Capacitor
4	0.1 uF	C8	AXIAL-0.3	Capacitor
5	$0.1 \mathrm{uF}$	C9	AXIAL-0.3	Capacitor
6	0.1 uF	C20	AXIAL-0.3	Capacitor
7	0.1 uF	C17	AXIAL-0.3	Capacitor
8	0.1 uF	C16	AXIAL-0.3	Capacitor
9	0.1 uF	C19	AXIAL-0.3	Capacitor
10	$0.1 \mathrm{~uF}$	C18	AXIAL-0.3	Capacitor
11	0.1 uF	C6	CAP200/28/150	Capacitor
12	0.1 uF	C7	CAP200/28/150	Capacitor
13	$0.1 \mathrm{uF}$	C4	CAP200/28/150	Capacitor
14	$0.1 \mathrm{uF}$	C5	CAP200/28/150	Capacitor
15	ZVN3310A	Q2	TO-92A	Diode
16	0.01	R6	R1100/60	Resistor
17	1 K	R29	POT1	Potentiometer
18	1N4148	D8	D350/40	Diode
19	1N4148	D7	D350/40	Diode
20	1N4746	D10	D350/40	Schottky Diode
21	$1\mathrm{k}$	R8	AXIAL-0.3	Resistor
22	1 k	R16	AXIAL-0.3	Resistor
23	1 k	R14	AXIAL-0.3	Resistor
24	1 k	R15	AXIAL-0.3	Resistor
25	$1\mathrm{k}$	R7	AXIAL-0.3	Resistor
26	1n4739	D11	D350/40	Schottky Diode
27	$1 \mathrm{nF}$	C27	AXIAL-0.3	Capacitor
28	1 uF	C15	CAP100/28/50	Capacitor
29	$1 \mathrm{~uF}$	C29	CAP100/28/50	Capacitor
30	$1 \mathrm{uF}$	C33	CAP100/28/50	Capacitor
31	$1 \mathrm{~uF}$	C32	CAP100/28/50	Capacitor
32	2.2 n	C30	C_1N	Capacitor
33	2.5 k	R9	AXIAL-0.3	Resistor
34	3.6 k	R21	AXIAL-0.3	Resistor
35	3.6 k	R22	AXIAL-0.3	Resistor
36	3.9 k	R17	AXIAL-0.3	Resistor
37	3 k	R26	AXIAL-0.3	Resistor
38	4.7 k	1W	R19	R_2W Resistor
39	5.1 k	R18	AXIAL-0.3	Resistor
40	5.6k	R30	AXIAL-0.3	Resistor
41	6.2 k	R10	AXIAL-0.3	Resistor
42	6.2k	R20	AXIAL-0.3	Resistor

43	6.2 k	R11	AXIAL-0.3	Resistor
44	6.8 uF	C21	CAP150/50/150	Capacitor
45	9.1 k	R12	AXIAL-0.3	Resistor
46	10 k	R28	AXIAL-0.3	Resistor
47	10 uF	C31	CAP100/28/50	Capacitor
48	10 uF	C12	CAP150/50/150	Capacitor
49	10 uF	C13	CAP150/50/150	Capacitor
50	$10 \mathrm{uF}$	C24	CAP150/50/150	Capacitor
51	10 uF	C25	CAP150/50/150	Capacitor
52	$10 \mathrm{uF}$	C28	CAP150/50/150	Capacitor
53	10 uF	C26	CAP150/50/150	Capacitor
54	10 uF	C10	DIP-10	Resistor
55	$20 \mathrm{~uF}$	C2	935C1W20K	Capacitor
56	$20 \mathrm{~uF}$	C1	935C1W20K	Capacitor
57	20 uF	C3	935C1W20K	Capacitor
58	33 k	R27	AXIAL-0.3	Resistor
59	47	R23	AXIAL-0.3	Resistor
60	180	R24	AXIAL-0.3	Resistor
61	180	R25	AXIAL-0.3	Resistor
62	220	R5	Axial-0.3	Resistor
63	220	R13	R_2W	Resistor
64	330	R31	AXIAL-0.3	Resistor
65	$470 \ \mathrm{pF}$	C22	C_1N	Capacitor
66	$470 \ \mathrm{pF}$	C23	C_1N	Capacitor
67	$200 \ 1W$	R1	R_2W	Resistor
68	2200 uF, 50 V	C3"	AXIAL-0.3	Electrolytic Capac-
				itor
69	3303	U2	DIP-14	Resistor
70	Closed = On	J3	CON2A	Connector
71	FET_DIODE	$\mathbf{Q1}$	FET_DIODE	Heatsink
	HEATSINK		HEATSINK	
72	$0.61 \mathrm{~uH}$	L1	L800	Inductor
73	INDUCTOR3	L2	LVAR	Inductor
74	IR2125	U6	DIP8	IC
75	LM317	U4	TO-220	IC
76	LM6142	U3	DIP-8	IC
77	LM7805	U8	TO-220	IC
78	LM7815	U5	TO-220	IC
79	LT431	U1	TO-92A	IC
80	MBR0540T1	D3	DIODE1	Schottky Diode
81	MBR0540T1	D6	DIODE1	Schottky Diode
82	MBR0540T1	D2	DIODE1	Schottky Diode
83	MBR0540T1	D4	DIODE1	Schottky Diode
84	MBR0540T1	D5	DIODE1	Schottky Diode

85	Pow In	J1	CON2D	Connector
86	Pow Out	J2	CON2D	Connector
87	not used	$\mathbf{R3}$	AXIAL-0.3	Resistor
88	not used	R4	AXIAL-0.3	Resistor
89	0.3	R2	R_2W	Resistor
90	TRANS1	T1	RM10	Resistor
91	UC3823A	U7	DIP16	Resistor
92	UG06B	D9	D350/40	Diode
93	IRF1010E	Q3	TO-220	N-Channel Power
				Mosfet
94	MUR3020WT	$\mathbf{Q4}$	TO-247	Common Cathode
				Diode

Table A.1: Bill of materials for the buck converter of Fig. A.1.

A.3 Block Diagram Model of the Buck Converter Control Circuitry

The following block diagram shows the buck converter control model that was used to assess the stability and the performance of the converter. A regulated voltage of 5 V was used as the reference for the converter. The output voltage was appropriately scaled by the output sensor transfer function, H_{ol} , and compared to the reference. The difference was input to the outer loop compensator, C_{ol} , the output of which produced the reference current, I_{ref} used in the inner control loop. The inner loop compensator then forced the sensed current at the output of the buck converter output filter inductor (or coupled-magnetic device) to the reference value. The corresponding MATLAB (Mathworks Inc., Cambridge, MA) code used to analyze the model and the transfer functions of Fig. A.2 are presented Section A.4.



Figure A.2: Block diagram for the buck converter controller model.
A.4 MATLAB Model for the Buck Converter Control Circuitry

function Control()

% This function determines and plots the inner and outer control loops of % the buck converter. The input filter is assumed to be designed such that % its effects on the control transfer functions is negligible.

% This code does not assume that the inductance is zero in the current path % of the variable inductor. Added inductance is L3, which constitutes the % sum of the variable inductance when the control current is zero and % the inductance Lc of the T model of the coupled-magnetic device.

```
%constants
Vin = 42;
C1 = 10e-6;
C2 = 20e-6;
C3 = 2200e-6;
Rc = 0.4;
R1 = 8;
L1 = 6.13e-6;
L2 = 1.67e-6;
L3 = 44e-9;
% R1=8 is 35% of max. power; 3 is full power - 65W; 12 is min. power - 16 W;
% DC model for the capacitor C3 is the capacitance and its Resr in series
% Isense/Vd - Inner loop plant (essentially the output filter)
num4 = Rc*Rl*C1*C2*C3*L3;
num3 = Vin*(Rc*C1*C3*L3+R1*C1*C2*L3+R1*C1*C3*L3);
num2 = Vin*(C1*L3+Rc*R1*C2*C3);
num1 = Vin*(Rc*C3+R1*C2+R1*C3);
num0 = Vin;
den5 = Rc*Rl*C1*C2*C3*(L1*L2+L1*L3+L2*L3);
den4 = R1*C1*C3*(L1*L2+L1*L3+L2*L3)+Rc*C1*C3*(L1*L2+L1*L3+L2*L3)+
R1*C1*C2*(L1*L2+L1*L3+L2*L3);
den3 = L1*L2*C1+C1*L1*L3+C1*L2*L3+R1*Rc*(C1*C3*L1+C2*C3*L1+C2*C3*L2+
C1*C3*L3);
den2 = (C1*R1*L1+C2*R1*L1+C2*R1*L2+C1*R1*L3+Rc*C3*L1+Rc*C3*L2+R1*C3*L1+
R1*C3*L2);
den1 = (L1+L2+Rc*Rl*C3);
```

```
den0 = Rl;
numH1 = [num4 num3 num2 num1 num0];
denH1 = [den5 den4 den3 den2 den1 den0];
% Isense/Vd
H1 = tf(numH1, denH1);
Rs1 = 180;
Rs2 = 3.6e3;
Rs3 = 0.010;
Cs1 = 470e-12;
Ls1 = 23e-9;
numS = Rs2*[Ls1 Rs3];
denS = Rs1*[Rs2*Cs1 1];
% I/Isense - current sensor transfer function
Hsen = tf(numS, denS);
Cil = tf(1500, [1 0]);
rltool(H1,Cil);
% Add Hsen to the feedback loop
sisotool(H1,Cil,Hsen);
sys1 = H1*Cil;
IL = feedback(sys1,Hsen);
% Outer loop plant
% AC model for the capacitor C3 is Rc -- its Resr
num0=Rl+Rc;
den0=Rc+R1;
den1=Rl*C2*Rc;
numH2=[num0];
denH2=[den1 den0];
% Vo/I_sense
H2 = tf(numH2, denH2);
```

Col = tf(234,[1 37.7]);

Hol = tf(5/14); rltool(H2*IL,Col); % Add Hol to the feedback path sisotool(H2*IL,Col,Hol);

Appendix B SIMULINK Simulation

B.1 Introduction

This appendix includes the SIMULINK block diagrams that were used to model the adaptive inductance cancellation control method. Figures B.1 - B.4 show the overall control block diagram and the contents of its masked blocks.

B.2 SIMULINK Block Diagrams

The gain blocks shown in Fig. B.1 correspond to the gains of the individual stages of the control circuit, discussed in detail in Chapter 5. Similarly, the saturation blocks represent the voltage saturation limits of the integrated circuits used on the controller board. The 1 V - 9 V saturation block represents the voltage limiting that was used to ensure that the control current remained between 0.05 and 0.95 A. The constant block subtracted from the output of the V_{ripple} block represents the AC coupling present in the system to isolate the ripple from the converter output (implemented as a differential high-pass filter of Fig. 5.2). Finally, a step function of amplitude 1 and a delay of 0.1 seconds multiplied by the control current was used to demonstrate the effects of the adaptive cancellation by first allowing the converter to reach steady state with $I_{control}$ maintained at zero. Then at t = 0.1 seconds, the control current was enabled.

The state-space block diagram describes the buck converter averaged state-space model of Eq. 4.2. The pulse block represents the voltage V_d of Fig. 4.4, which is a square wave with the buck converter switching frequency of 400 kHz, an amplitude of 42 V, corresponding to the nominal buck converter input voltage, and a duty ratio of $\frac{1}{3}$, corresponding to the 42 V to 14 V conversion function. The inductance block is shown in Fig. B.3, and represents the block diagram used to generate the following gain:

$$\frac{1}{L_A L_B + L_A L_C + L_B L_C}$$

which constitutes a scaling factor for many elements of the gain matrices of Eq. 4.2.

The block diagram of Fig. B.4 represents the mathematical model used to generate $V_{\text{ripple}}^{\text{RMS}}$ from V_{ripple} , and is depicted by the RMS block in Fig. B.1. The time constant for the RMS function was chosen to be $\frac{0.0001}{2\pi}$ seconds, corresponding to a cutoff frequency of 10 kHz. This cutoff frequency was chosen to be high enough such as not to include the RMS of the low frequency (500 Hz) sinusoidal oscillation, but to calculate only the RMS of the converter output ripple. The resulting low-pass transfer function is: $\frac{1}{\left(\frac{0.0001}{2\pi}s+1\right)}$, shown as the $\frac{1}{den(s)}$ block in Fig. B.4.



Figure B.1: SIMULINK model of the adaptive inductance cancellation control.



Figure B.2: State-Space model for the buck converter, represented by the $I_{control}$ to V_{ripple} block in Fig. B.1.



Figure B.3: SIMULINK block diagram used to generate the inductance block of Fig. B.2.



Figure B.4: SIMULINK block diagram that generates the RMS function used to obtain V_{ripple}^{RMS} from V_{ripple} , represented by the RMS block of Fig. B.1.

Appendix C

Adaptive Inductance Cancellation Control Board

C.1 Introduction

This appendix presents the schematic, the bill of materials, and the printed circuit board masks for the adaptive inductance cancellation control board of Chapter 5.

C.2 Eagle Layout Editor Schematic

The circuit of Figure 5.2 was implemented on a printed circuit board using the Eagle (CadSoft Computer GmbH) layout editor. The resulting Eagle schematic is presented in Figure C.1. Table C.1 details the materials used in the assembly of the board. It must be noted that the following components were added after the manufacture of the board: D_3 , R_{23} , R_{24} , R_{25} , and R_{27} . The components added across the variable inductor (D3 and R_{23}) were soldered across the inductor control current leads, while the resistors added for the AD633 multiplier offset circuitry (R_{24} , R_{25} , and R_{27}) were soldered onto the protoboard space in the corner of the control board (Figs. C.3 – C.6). Thus, the footprints for these components are not present on the masks for the PCB layers.



Num.	Part	Value	Device	Package	Description
1	AD633	AD633	AD633	DIL08	AD633
2	AD637	AD637	AD637	DIL14	AD637
3	ADD_OUT	PTR1	PTR1	$TEST_PT$	TEST PIN
4	C1	$1\mathrm{u}$	C2,5-3	C2.5-3	CAPACITOR
5	C2	0.1u	C2.5/4	C2.5-4	CAPACITOR
6	C3	0.01u	C2.5/4	C2.5-4	CAPACITOR
7	C4	0.01u	C2.5/4	C2.5-4	CAPACITOR
8	C5	0.01u	C2.5/4	C2.5-4	CAPACITOR
9	C6	0.068u	C2.5/5	C2.5-5	CAPACITOR
10	C7	0.1u	C2.5/4	C2.5-4	CAPACITOR
11	C8	0.1u	C2.5/4	C2.5-4	CAPACITOR
12	C9	0.1u	C2.5/4	C2.5-4	CAPACITOR
13	C10	0.1u	C2.5/4	C2.5-4	CAPACITOR
14	C11	0.1u	C2.5/4	C2.5-4	CAPACITOR
15	C12	0.1u	C2.5/4	C2.5-4	CAPACITOR
16	C13	0.1u	C2.5/4	C2.5-4	CAPACITOR
17	C14	0.1u	C2.5/4	C2.5-4	CAPACITOR
18	C15	0.1u	C2.5/4	C2.5-4	CAPACITOR
19	C16	.00068u	C2.5/4	C2.5-4	CAPACITOR
20	C17	0.1u	C2.5/4	C2.5-4	CAPACITOR
21	C18	0.1u	C2.5/4	C2.5-4	CAPACITOR
22	C19	0.1u	C2.5/4	C2.5-4	CAPACITOR
23	C20	0.1u	C2.5/4	C2.5-4	CAPACITOR
24	CADJ	C2.5/5	C2.5-5	CAPACITOR	
25	D1	1N4001	1N4001	DO41-10	DIODE
26	D2	9.1	V	ZENER-	DO41Z10
				DIODE	Zener Diode
27	D3	1N4001	1N4001	DO41-10	DIODE
28	GND_1	PTR1	PTR1	TEST_PT	TEST PIN
29	GND_2	PTR1	PTR1	$TEST_PT$	TEST PIN
30	GND_3	PTR1	PTR1	TEST_PT	TEST PIN
31	GND_4	PTR1	PTR1	$TEST_PT$	TEST PIN
32	GND_5	PTR1	PTR1	TEST_PT	TEST PIN
33	HP_FILTER	PTR1	PTR1	TEST_PT	TEST PIN
	OUT				
34	LF347	LF347N	LF347N	DIL14	OP AMP
35	LM317	317	317	TO220V	Positive
					VOLTAGE
					REGULA- TOP
26	I M6261 1	Ĩ M741D	T 1/7/1D		IUN OD AMD
30 97	T M6961 0				
31	LIVI0301_2	LN1/41P	LM(41P)	DILU8	OP AMP

38	LVAR1	LVAR	LVAR	P14/8_CORE	Cross-Field
39 40	MULT_OUT R1	PTR1 200	PTR1 R- US_0207/10	TEST_PT 0207/10	Reactor TEST PIN RESISTOR, American
41	R2	1k	R- US_0207/10	0207/10	RESISTOR, American
42	R3	20k	R- US_0207/10	0207/10	RESISTOR, American
43	R4	16k	R- US_0207/10	0207/10	RESISTOR, American
44	R5	10k	R- US_0207/10	0207/10	RESISTOR, American
45	R6	10k	R- US_0207/10	0207/10	RESISTOR, American
46	R7	10k	R- US_0207/10	0207/10	symbol RESISTOR, American
47	R8	10k	R- US_0207/10	0207/10	symbol RESISTOR, American
48	R9	9.1k	R- US_0207/10	0207/10	symbol RESISTOR, American
49	R10	1k	R- US_0207/10	0207/10	symbol RESISTOR, American
50	R11	1	R- US_0414/15	0414/15	symbol RESISTOR, American
51	R12	100	R- US_0207/10	0207/10	symbol RESISTOR, American
52	R13	100	R- US_0207/10	0207/10	symbol RESISTOR, American symbol

53	R14	1.5k	R- US_0207/10	0207/10	RESISTOR, American
54	R15	1.5k	R- US_0207/10	0207/10	RESISTOR, American
55	R16	100	R- US_0207/10	0207/10	RESISTOR, American
56	R17	1.5k	R- US_0207/10	0207/10	RESISTOR, American
57	R18	1k	R- US_0207/10	0207/10	RESISTOR, American
58	R19	47k	R- US_0207/10	0207/10	RESISTOR, American
59	R20	15k	R- US_0207/10	0207/10	symbol RESISTOR, American
60	R21	91	R- US_0207/10	0207/10	symbol RESISTOR, American
61	R22	240	R- US_0207/10	0207/10	symbol RESISTOR, American
62	R23	390	R- US_0414/15	0414/15	symbol RESISTOR, American
63	R24	300k	R- US_0207/10	0207/10	symbol RESISTOR, American
64	R25	15k	R- US_0207/10	0207/10	RESISTOR, American
65	R27	50k	TRIM_US- RS3	RS3	SYMBOL POTENTIO- METER
66	BMS OUT	PTR1	PTR1	TEST PT	TEST PIN
67	SAT OUT	PTR1	PTR1	TEST PT	TEST PIN
68	SINE OUT	PTR1	PTR1	TEST PT	TEST PIN
60	TIP20C		TIP20C	TO220V	NPN Transis-
09	111 230	VERTICAT	VEBTICAI	1 0 4 4 0 4	tor
70	VDEC OUT	VERIUAL DTD 1	PTP1	TEST PT	TEST PIN
70	VREGLUUT	FIRI	LIUI		TEDITIN

C.2 Eagle Layout Editor Schematic

Adaptive Inductance C_{i}	ancellation	Control	Board
-----------------------------	-------------	---------	-------

71 V_EMITTER 72 X1 73 X3 74 X4 75 XR2206	PTR1 MPT2 MPT2 MPT2 XR-2206	PTR1 2POL254 2POL254 2POL254 DIL16	TEST_PT PHOENIX PHOENIX PHOENIX Monolithic	TEST PIN CONNECTOR CONNECTOR FUNCTION GENERA- TOR
--	---	--	--	--

Table C.1: Bill of materials for the control board of Fig. C.1.

C.3 PCB Layer Masks for the Adaptive Inductance Cancellation Control Board

Figures C.2 – C.6 show the silkscreen, component side, ground, layer 3, and solder side layer masks, respectively, for the printed circuit board of the controller of Fig. C.1. The "dimension" layer is included on every mask to designate the board edges. Pads and vias are also shown on the component and solder side masks. The masks are shown in their actual physical dimensions. It must be noted that layer 3 does not contain signal connections. Additionally, although space was allotted on the board for the 10 μ F high-ripple, lowinductance film capacitor (ITW Paktron 106K050CS4) located in the variable inductor path, the capacitor was placed on the buck converter printed circuit board instead. This was done to minimize the parasitic inductance in the ground path of the capacitor.







Figure C.3: Adaptive inductance cancellation controller PCB component side layer.



C.3 PCB Layer Masks for the Adaptive Inductance Cancellation Control Board

Figure C.4: Adaptive inductance cancellation controller PCB ground layer. By convention, the ground layer is shown inverted, with the conductor depicted in white.



Figure C.5: Adaptive inductance cancellation controller PCB layer 3 (shown inverted, with the conductor depicted in white).



C.3 PCB Layer Masks for the Adaptive Inductance Cancellation Control Board

Figure C.6: Adaptive inductance cancellation controller PCB solder side layer.

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