

An Optical-Electrical Sub-Sampling  
Down-Conversion Receiver with Continuous-Time  
 $\Sigma\Delta$  Modulation

by

Matthew Park

Submitted to the Department of Electrical Engineering and Computer  
Science

in partial fulfillment of the requirements for the degree of

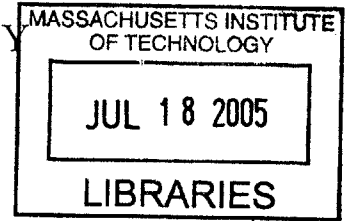
Master of Engineering in Electrical Science and Engineering

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May 2005

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## Abstract

This thesis describes the design and implementation of an optical-electrical sub-sampling down-conversion receiver that employs  $\Sigma\Delta$  modulation. Accurate sub-sampling of an electrical RF signal in the optical domain is achieved by using a low-jitter mode-locked-laser and a high-bandwidth interferometer. The sub-sampled information is then digitized by an optical-electrical continuous-time (CT)  $\Sigma\Delta$  analog-to-digital converter (ADC). Here, photodiodes and low-jitter pulses from the mode-locked-laser are leveraged to perform signal clocking and quantizer pre-amplification, overcoming digital-to-analog converter (DAC) clock jitter and quantizer metastability issues that plague traditional electronic implementations. The optical-electrical converter achieves 76.5 dB of SNR (12.4 ENOB) with a 1 MHz signal bandwidth and a sampling rate of 780 MHz. The chip was implemented using a standard bulk 0.18  $\mu\text{m}$  CMOS process from National Semiconductor, occupies a total area of 3  $\text{mm}^2$ , and consumes 45 mW of power.

Thesis Supervisor: Michael H. Perrott  
Title: Assistant Professor



*I praise God,  
because he did not reject my  
prayer  
or keep back his constant love  
from me.*

—Psalm 66:20



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# Chapter 1

## Introduction

With large-scale monolithic integration of both circuits and optical devices less than a decade away, the field of optoelectrics is poised for a rapid and comprehensive transformation. Indeed, the numerous benefits that accompany full system integration (e.g., lower cost, area and power consumption, better matching, greater device customization etc.) will enable designers to create high-performance optoelectrical communication systems that are more affordable and more portable. This reality has the potential to galvanize the telecommunications industry while providing consumers with the next generation of high-speed products.

But full-scale monolithic integration also raises an exciting, fundamental question: where should the boundary between the optical and electrical worlds exist? Current optical-electrical systems use expensive discrete optical devices, and have limited flexibility in setting the optical and electrical boundaries due to cost and space considerations. In contrast, integrated optoelectronics open the door to a host of optical-electrical circuits that gives designers much greater freedom in setting the optical and electrical boundaries. Indeed, the integrated approach promises the ability to leverage optical devices and their unique properties in system architectures that were once exclusively implemented in either the optical or electrical domain. Now, the entire spectrum of signal processing afforded by both domains can be utilized to design hybrid systems that have superior speed and precision, and are less wasteful of critical resources, such as power and area. Such high performance systems will

find innumerable applications in all sectors of industry, and may even spur on new technological innovations and inventions.

To that end, this thesis strives to demonstrate the great potential in optoelectronics through the design, analysis, and implementation of an optical-electrical sub-sampling down conversion receiver employing continuous-time  $\Sigma\Delta$  modulation. Optical signals and devices are leveraged to realize a receiver that can mix RF signals modulated at tens of GHz down to baseband with minimal signal distortion. Continuous-Time (CT)  $\Sigma\Delta$  modulation is utilized as a means to seamlessly interface the optical-electrical worlds and digitize the down-converted information with maximum signal-to-noise ratio (SNR). Finally, optics are exploited in the design of the  $\Sigma\Delta$  ADC in an effort to find optical solutions for common problems in high-speed CT  $\Sigma\Delta$  modulation.

The framework for this thesis will now be described.

Chapter two discusses the motivation for using optics, and describes two key optical devices, the mode-locked laser and the interferometer. Concepts of direct-down conversion and subsampling are compared. Sub-sampling in the optical domain is proposed, and  $\Sigma\Delta$  modulation is introduced as an ideal means to interface the two media, and digitize information. Chapter three details the design challenges of current discrete-time (DT) and continuous-time (CT)  $\Sigma\Delta$  modulators. In particular, various compensation schemes that have been developed for CT modulators to counter the topology's sensitivity to certain non-idealities are discussed. Chapter four proposes two novel optical-electrical circuits to further enhance the performance of high-speed CT modulation. Chapter five outlines the chosen architecture for the  $\Sigma\Delta$  modulator, and draws attention to the design of the remaining analog and digital blocks. Chapter six summarizes results from behavioral and circuit simulations. Chapter seven reviews the contributions made by this thesis.

# Chapter 2

## An Optical-Electrical Approach

### 2.1 The Optical Advantage

Today, systems that employ optical components are almost always exclusively used for communications-related applications. Here, the large bandwidths of optical devices are leveraged to perform high-speed *digital* data transmission through fiberoptics. This thesis, however, focuses more on the ability of using optical signals to perform noise sensitive *analog* processing. Indeed, the primary application of this work, described later as a sub-sampling down-conversion receiver, leverages the low-jitter timing streams available from mode-locked-lasers and the high bandwidth of interferometers.

#### 2.1.1 The Mode-Locked Laser

Ever since its invention more than three decades ago, the mode-locked laser has become extremely popular due to its ability to generate very low-jitter, narrow pulses (see Figure 2-1). Recently, a laser setup demonstrating only 14 femtoseconds of timing jitter over a 10 Hz to 375 MHz bandwidth was demonstrated [15]. Previous work in the optical-electrical area capitalized on this near-ideal optical impulse train to perform sampling of electrical signals at the input of high-speed analog-to-digital converters [11].

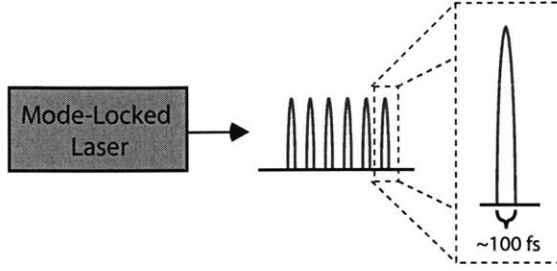


Figure 2-1: Illustration of the low-jitter, narrow optical pulses generated by the mode-locked laser.

### 2.1.2 The Interferometer

In the most general sense, the interferometer is a device that splits power in a differential fashion according to an applied voltage. Figure 2-2 illustrates the concept, with optical power entering the device splitting into two separate paths, or “arms”. The bottom path in the diagram, referred to as the “strong arm”, emits optical power according to:

$$P_{out,strong}(t) = P_{in} \cos^2 \left( \frac{\pi}{V_{\pi}} v_{IN}(t) \right) \quad (2.1)$$

where  $P_{in}$  is the input optical power and  $V_{\pi}$  is a scale factor that converts the input voltage,  $v_{IN}$  to a phase in radians. The second path, called the “weak arm”, transmits optical power in a complementary fashion:

$$P_{out,weak}(t) = P_{in} \sin^2 \left( \frac{\pi}{V_{\pi}} v_{IN}(t) \right) \quad (2.2)$$

Note that optical power is conserved from input to output since  $\cos^2(x) + \sin^2(x) = 1$ . While the interferometer can be implemented in different ways depending on whether a free-space laser or a fiber laser is being used, it always outputs power according to the relations described in Equations 2.1 and 2.2. The normalized input-output power relations for both paths are plotted in Figure 2-3. For the remainder of this discussion, it is assumed that the interferometer is biased at the point where the strong arm and weak arm curves intersect in Figure 2-3. This operating point ( $V_{IN} = \frac{V_{\pi}}{2}, P_{OUT} = 0.5$ ) corresponds to the point where both strong and weak arms are maximally linear.

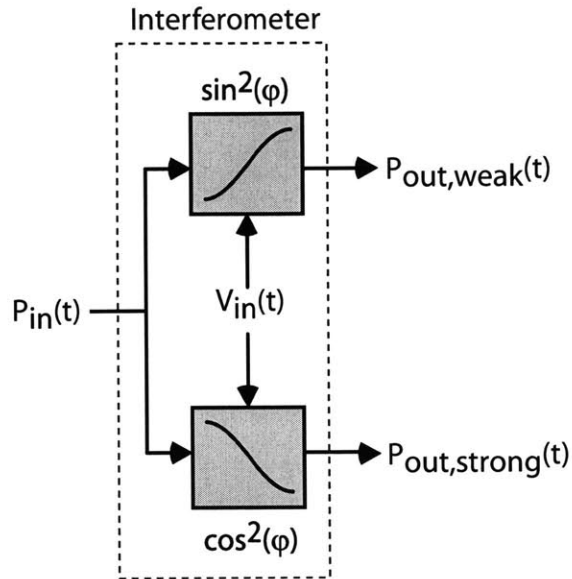


Figure 2-2: Diagram of the interferometer, which splits optical power into two complementary paths.

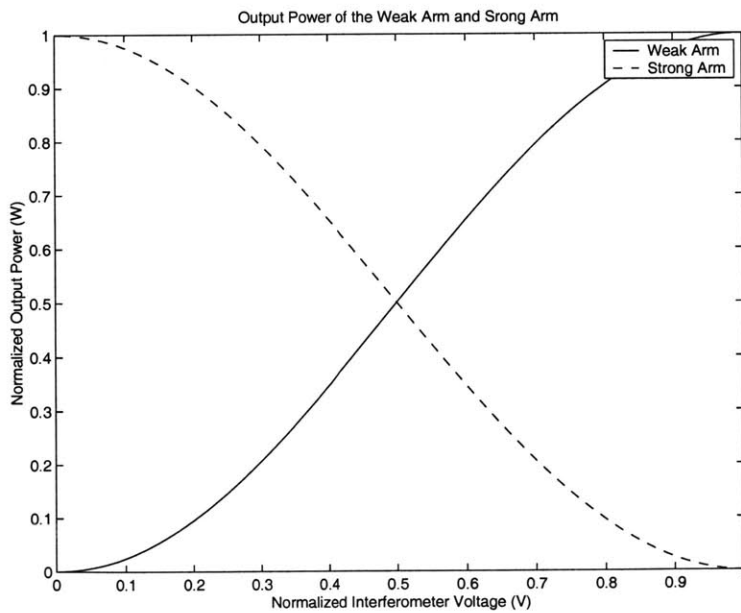


Figure 2-3: Plot of the output power of the strong and weak arms of the interferometer as the voltage  $v_{IN}$  is swept.

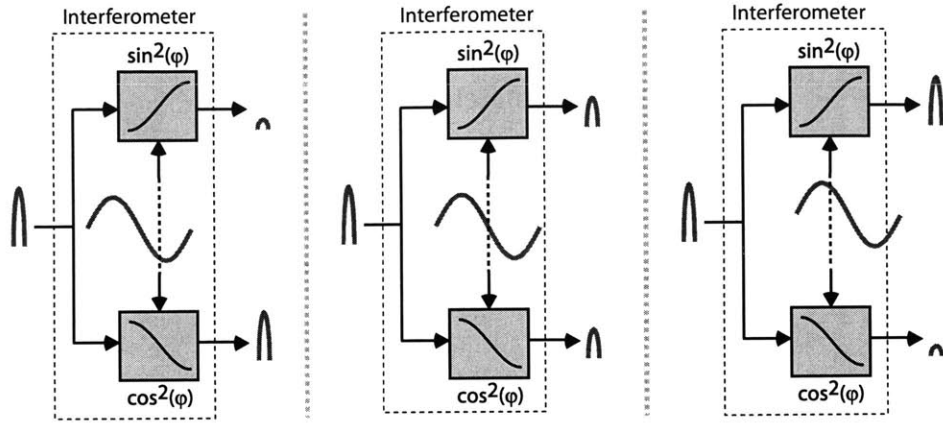


Figure 2-4: Illustration of the differential output power of the interferometer.

For the purposes of this thesis, it is of particular interest to consider what happens when pulses from the mode-locked laser enter the interferometer while a voltage,  $v_{IN}(t)$  is applied. Figure 2-4 illustrates three different scenarios, with the optical pulse coinciding in time (the dashed line) to different points on  $v_{IN}(t)$ . Observe in the left-most part of the figure that when pulse coincides with the minimum of the applied voltage, the strong arm outputs *most* of the pulse power, and the weak arm outputs *very little* of the pulse power. Conversely, as shown in the right-most part of the figure, when the pulse coincides with the maximum of the applied voltage, the strong arm outputs *very little* of the pulse power, and the weak arm outputs *most* of the pulse power. Finally, as shown in the center of the figure, when the pulse coincides with the midpoint of the applied voltage, both strong and weak arms output *equal* pulse power.

In essence, the applied voltage causes the interferometer to modulate the pulse power, making the overall structure appear like an amplitude modulator or mixer (see Figure 2-5). Furthermore, the modulation occurs in a differential manner since the power coming out of the strong and weak arms are complementary to each other. Finally, note that since the modulation depends on the value of the applied voltage *at the time instant* when the pulse enters the interferometer, the mode-locked laser pulses are effectively sampling the voltage signal. With this new understanding, it is clear that the cascaded system comprising the mode-locked-laser and the interferometer is

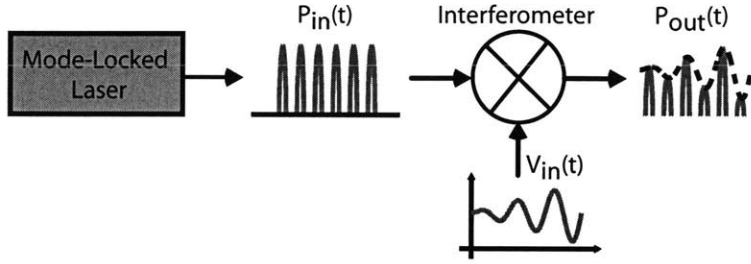


Figure 2-5: Representation of the interferometer as an ideal mixer (multiplier) when properly biased.

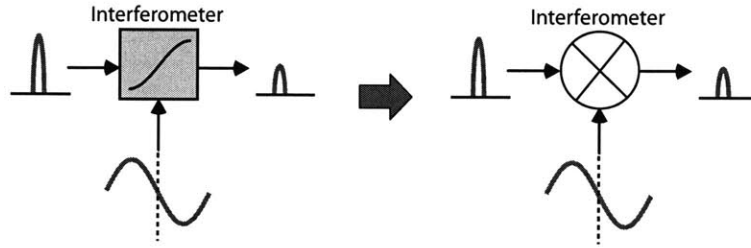


Figure 2-6: Representation of the mode-locked laser and interferometer pair as a sampling network.

equivalent to an optical sampling network (see Figure 2-6).

The optical sampling events can be mathematically described in the following manner (see Figure 2-7(a)):

The mode-locked-laser pulses are modelled as an ideal impulse train of period  $T$  and with area  $P_{opt}$ :

$$P_{impulse}(t) = P_{opt} \sum_{n=-\infty}^{+\infty} \delta(t - nT) \quad (2.3)$$

The interferometer is linearized about its operating point  $(V_{IN}, P_{OUT})$  (see Figure 2-7(b)):

$$\left. \frac{\partial P_{out}}{\partial v_{IN}} \right|_{v_{IN}=V_{IN}} = P_{opt} \frac{\pi}{V_{\pi}} \quad (2.4)$$

This leads to:

$$P_{sample}(t) \approx \left( P_{opt} \frac{\pi}{V_{\pi}} \right) \sum_{n=-\infty}^{+\infty} v_{in}(nT) \delta(t - nT) \quad (2.5)$$

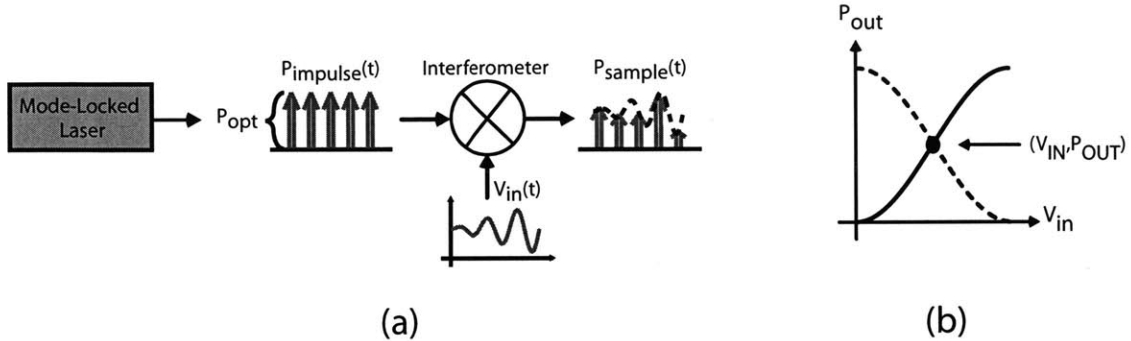


Figure 2-7: Mathematical model of (a) optical sampling using an ideal impulse train, and (b) the interferometer input-output characteristic and bias point.

## 2.2 Exploiting Optics in Mixed-Signal Architectures

The key question now concerns how to reap the maximal benefits from such a low-jitter optical sampling network. In prior work, the mode-locked laser and interferometer were used as a low-jitter reference and phase detector, respectively, for a phase-locked-loop (PLL) [10]. This optical-electrical PLL was able to synchronize a 2 GHz electrical clock signal to a 100 MHz mode-locked laser reference with less than 60 femtoseconds of relative timing jitter.

This thesis proposes leveraging low-jitter optical sampling and mixing to perform down-conversion using an optical-electrical sub-sampling architecture. But to understand why sub-sampling is a useful technique that is suited for the optical domain, classical direct down-conversion must first be reviewed.

### 2.2.1 Classical Direct Down-Conversion Receiver

Figure 2-8 illustrates the classical way of implementing a direct-down conversion receiver. Here, an RF signal of bandwidth  $f_B$  is mixed with a sine-wave local oscillator (LO) whose frequency ( $f_o = 40$  GHz) matches the carrier frequency ( $f_c = 40$  GHz) of the RF input. The Fourier transforms of the RF signal and the LO are shown in (a)



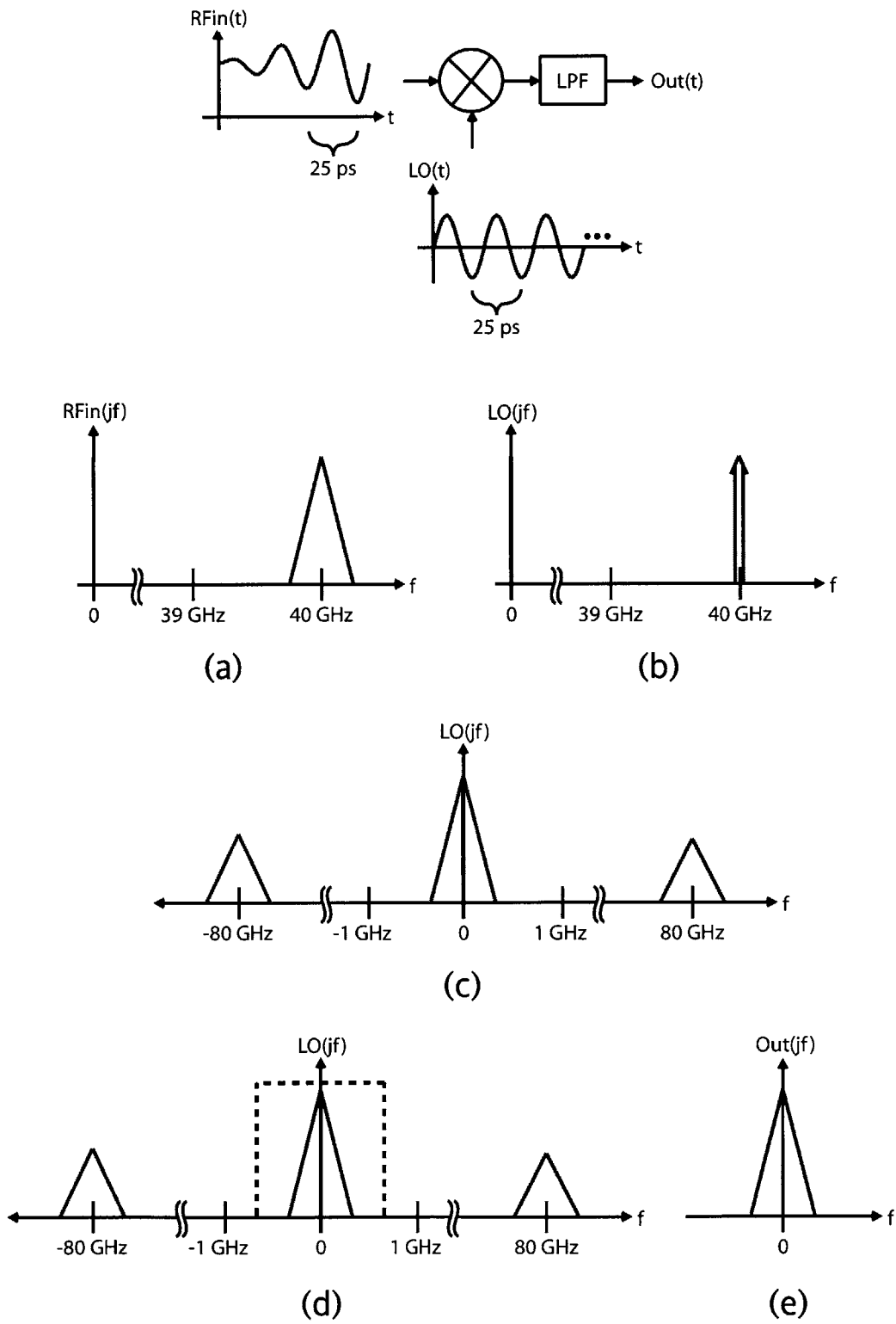


Figure 2-8: Illustration detailing the operation of a classical down-converter.

and (b), respectively. Mixing is multiplication in the time domain, and corresponds to convolution in the frequency domain, as illustrated in (c), which causes the desired RF signal to appear at baseband, and its images at twice the carrier ( $2f_o = 80GHz$ ). Low-pass filtering (d) removes the images, leaving only the desired signal (e).

While this approach is widely used and commonplace, it's utility hinges on the existence of a VCO with low phase-noise characteristics. As the carrier frequency increases beyond 10 GHz, it becomes exceedingly difficult to generate a LO from a VCO that has the required phase noise characteristics needed to down-convert the RF with negligible signal distortion.

### 2.2.2 An Optical-Electrical Sub-Sampling Down-Conversion Receiver

Optical-electrical sub-sampling offers an attractive alternative to direct-down conversion in that the LO does not have to be operating at the same frequency as the RF carrier. See Figure 2-9. Here, the mode-locked laser pulses sample the RF signal that is applied to the interferometer. In the frequency domain, the Fourier transforms of the RF signal (a) and the mode-locked laser impulse train (b) are convolved. If the RF carrier is some integer multiple of the impulse train sampling frequency ( $f_c = 40f_s = 40 \times GHz$  in the figure), and  $f_B < 2f_s$  ( $f_B = 1MHz$ ), then aliasing will occur, generating replicas of the RF signal at every harmonic of the impulse train, including one replica at baseband (c). Low-pass filtering (d) then extracts the baseband signal for further processing (e).

Note that sub-sampling relies on the LO closely matching an ideal impulse train. If there were significant jitter in the LO, then the situation shown in Figure 2-10 would result. Here, jitter causes spectral smearing of the higher harmonics of the impulse train (b), causing significant distortion of the desired signal after sub-sampling and low-pass filtering (c). Thus, sub-sampling such a high frequency RF signal is feasible primarily because the extremely low-jitter characteristics of the mode-locked laser pulses preserve the impulse train upper harmonics.

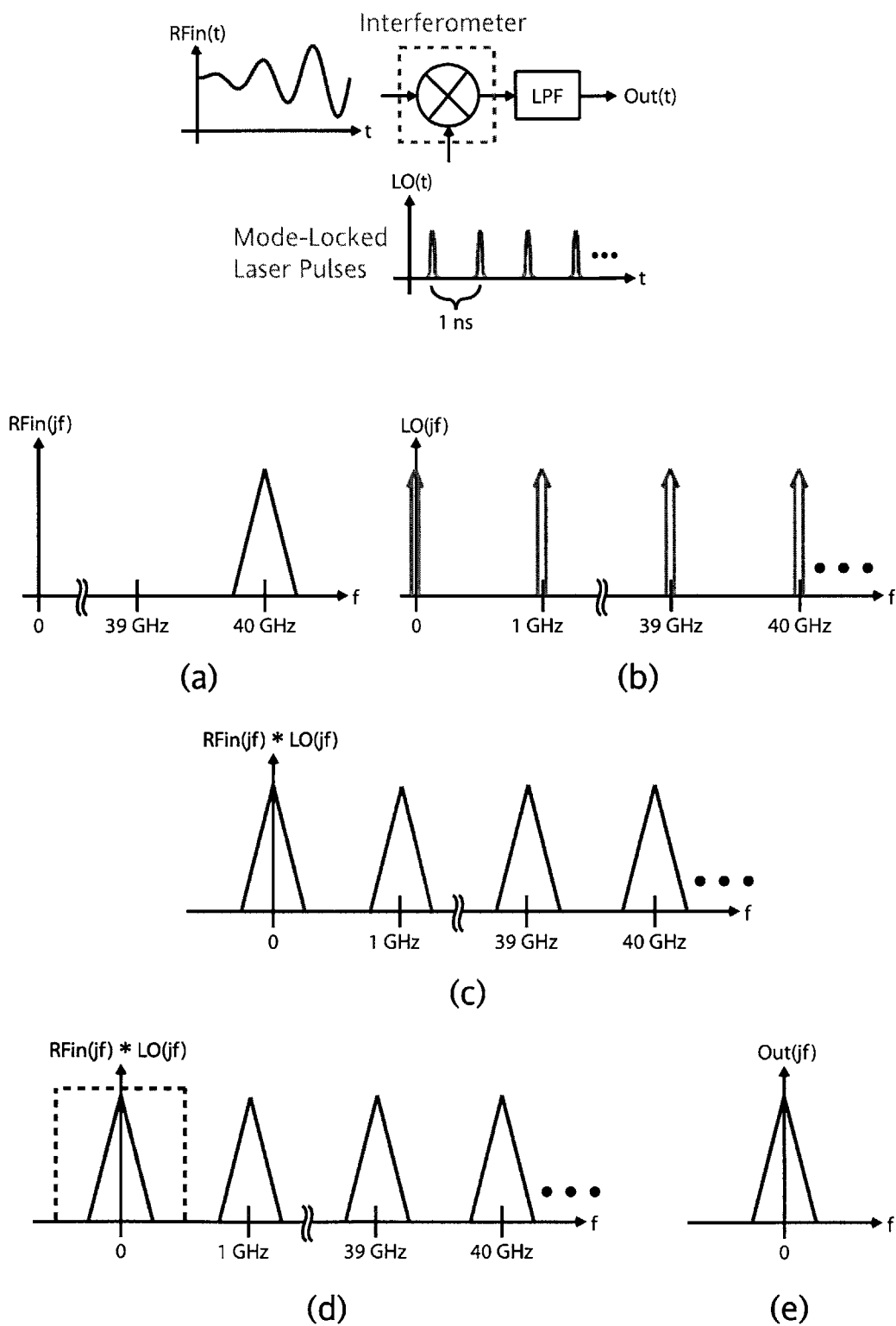


Figure 2-9: Illustration of the optical-electrical sub-sampling scheme for down-conversion.

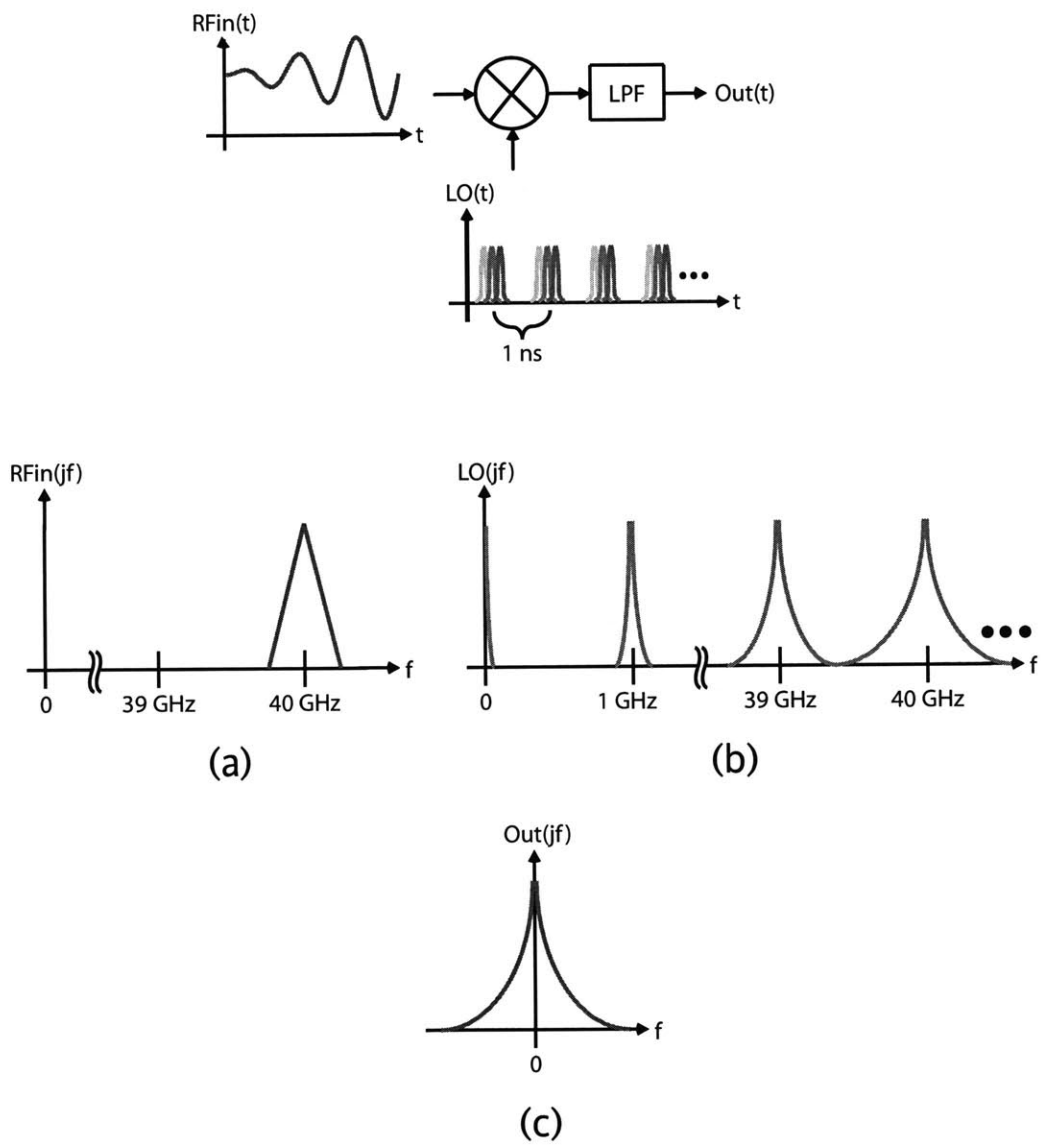


Figure 2-10: Illustration of the effect of jitter on sub-sampling.

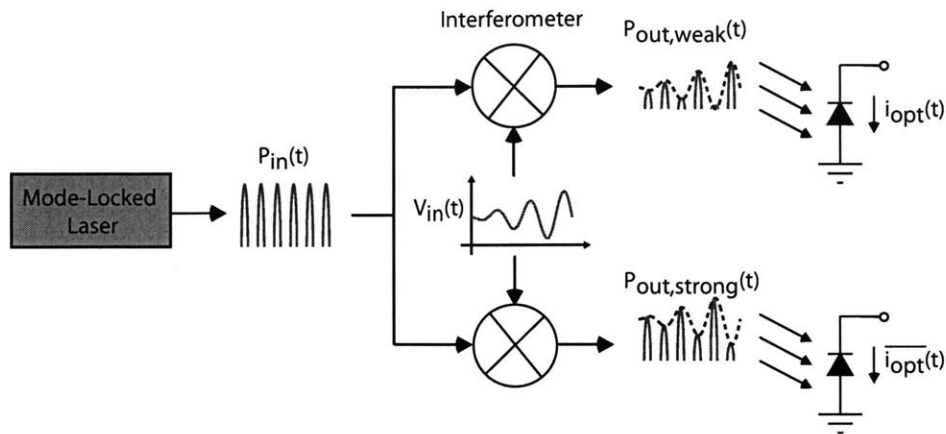


Figure 2-11: Converting the differentially modulated optical pulses into differential current pulses via a photodiode.

## 2.3 Digitizing Optical Information: the Optical-Electrical Boundary

Now that the narrowband RF information has been down-converted to baseband, a mechanism is needed to (1) convert the optical information into electrical information, and (2) digitize the resulting signal. Fortunately, the former of these two requirements is very simple to implement, and involves one photodiode for each amplitude-modulated optical pulse train (see Figure 2-11).

The photodiodes behave as ideal current sources with near infinite output impedances due to the reverse-biasing of the junction. The generated photocurrent density for a given incident optical power,  $P_{opt}$ , is described by the responsivity,  $R$ , of the photodiode, which has units [A/W] (see Appendix). For discrete photodiodes,  $R$  is supplied by the manufacturer enabling easy calculation of the photocurrent:

$$I_{ph} = RP_{opt} \quad (2.6)$$

It is important to note that although the optical pulses may behave very close to an ideal impulse train, the current pulses generated by the photodiode generally do not. In particular, practical photodiodes suffer from a finite carrier recombination time that manifests itself as an exponentially settling tail in the impulse response (see

Figure 2-12. Use of PIN photodiodes made of high mobility materials (i.e., GaAs, InP) with large reverse biases ( $> 5V$ ) can minimize the settling transient by inducing a high electric field that propels the settling carriers across the junction and speeding up the fundamental carrier recombination rate. Nevertheless, the settling behavior cannot be completely eliminated.

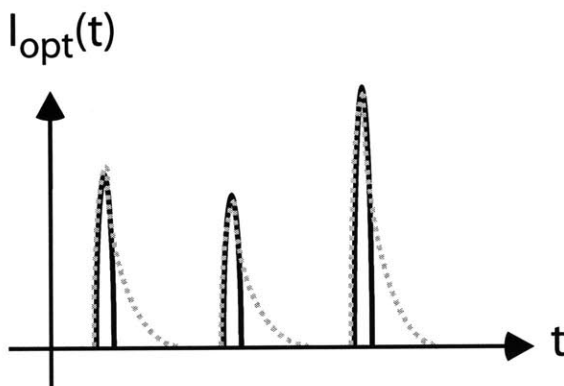


Figure 2-12: Comparison of an ideal current pulse (solid) and the actual current pulse transient (dashed). The exponentially decaying tail is caused by the finite recombination rate of the carriers in the photodiode

### 2.3.1 Charge Compartmentalization for Nyquist Conversion

While converting the optical information (photons) into electrical information (charge) is trivial with the use of a photodiode, finding ways to capture this information for digitization is not as simple. Prior work in optical-electrical data conversion have tried to capitalize on the high-speed nature of optical signals to perform high speed data conversion [9]. Consequently, a Nyquist converter (typically a flash or pipeline) was chosen to maximize the data rate, which necessitated the use of some form of sample-and-hold (S/H) circuitry at the converter input. A prototypical example of such a converter is described in [11], where mode-locked laser pulses were used to trigger a sample-hold event via a photoconductive material (see Figure 2-13).

The problem with this approach is that it places strict requirements on the timing of the sampling circuitry and the optical devices for proper operation (see Figure 2-14). Within a given sample period, charge must be completely compartmental-

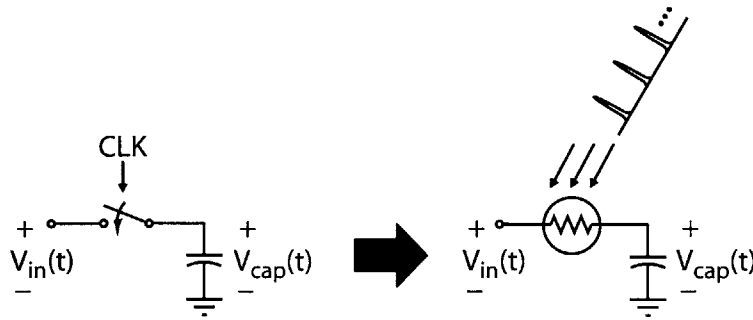


Figure 2-13: Optically-triggered sample-and-hold (S/H) using mode locked laser pulses to instantaneously alter the conductivity of a photoconductive material, such as polysilicon crystalline.

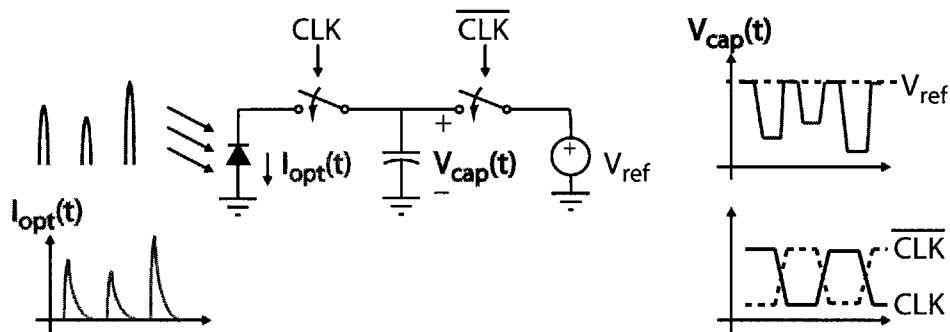


Figure 2-14: Problems with real S/H circuits: photodiode transients, complex clocking schemes, charge compartmentalization.

ized onto a capacitor, sensed by a regenerative amplifier (i.e., quantizer), and then completely discharged before the next optical sampling event occurs. Due to diode recombination issues described above, the photodiode must be extremely fast in order for the exponential tail to settle within the allotted time frame.

Even worse, real S/H circuits require the use of MOS switches to control the sampling and discharging events. This unfortunately introduces a host of undesirable effects into the input of the converter, including charge-injection, clock-feedthrough, and non-linear settling due to the non-linearity of the MOS on-resistance. Furthermore, the current pulses generated by the photodiode can be on the order of tens of milliamps, which makes the IR drop across the finite switch resistance non-negligible. Increasing switch devices can reduce this finite resistance, but at the cost of enhanced charge injection. Even the photoconductive S/H approach in [11] still required a MOS switch to discharge the capacitor, as well as a quasi-differential input buffering ampli-

fier to remove a common-mode component of the input signal that coupled through to the sampling capacitor. In addition to adding noise to the input, the buffering amplifier degraded the SFDR of the overall converter by introducing even order distortion.

### 2.3.2 Charge Integration for CT $\Sigma\Delta$ Data Conversion

From the previous discussion, it would seem advantageous to simply not have a S/H at the converter input. Removing the S/H from Figure 2-14 results in Figure 2-15. Here, the photodiode continuously integrates charge onto the capacitor, and all the non-linearity and noise-issues that plagued the S/H implementation are gone. Furthermore, since charge is not being compartmentalized and then discharged within the sampling period, the structure is not as sensitive to the photodiode recombination transients. But as shown in the figure, there is a new problem in that the diode will constantly discharge the capacitor—some other mechanism is required to recharge the capacitor.

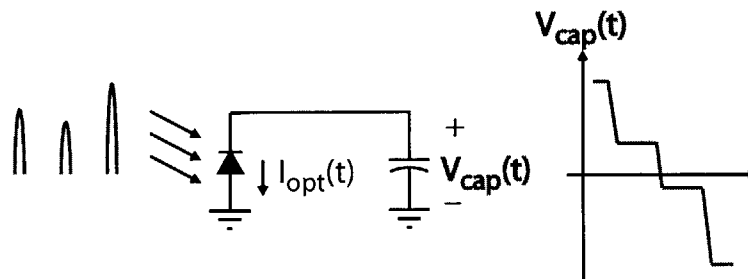


Figure 2-15: Eliminating the S/H circuitry and directly connection the photodiode anode to an integrating capacitor.

This thesis proposes the use of a continuous-time (CT)  $\Sigma\Delta$  modulator as not only a solution to the problem of continuous charge integration, but also an alternate, more desirable technique for digitizing the optical information (see Figure 2-16). Constant charge integration is a key mechanism in  $\Sigma\Delta$  modulation, which allows the removal of the S/H and a direct connection from the photodiode to the integrating capacitor. In the structure, the quantizer senses the diode discharge, and triggers the digital-to-analog converter (DAC) in the negative feedback loop to recharge the integrating



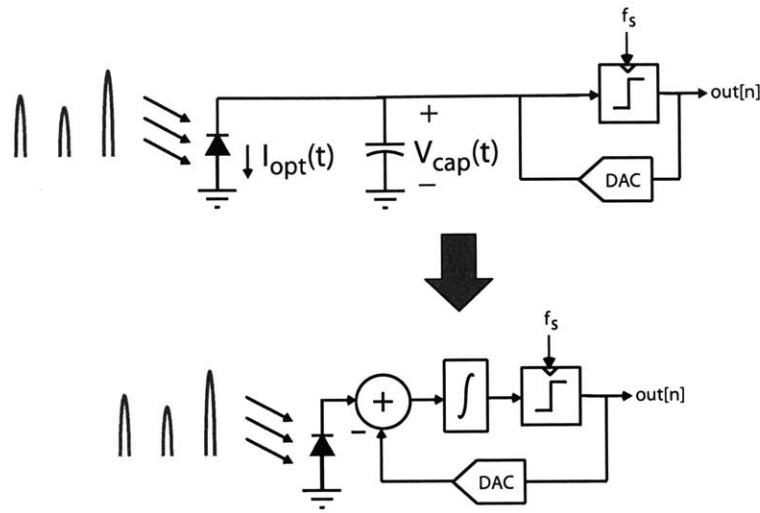


Figure 2-16: Using the photodiode and integrating capacitor as an input integrator to a CT  $\Sigma\Delta$  modulator.

capacitor.

Since the signals of interest resulting from the optical sub-sampling scheme are assumed to be narrowband in nature,  $\Sigma\Delta$  modulation is an ideal technique to digitize the down-converted information because of the superior SNR it affords over Nyquist converters for equivalent bandwidths and power dissipation. At the same time, CT  $\Sigma\Delta$  modulators come with an inherent antialiasing filter, which aids in the rejection of the signal replicas located at integer multiples of the sampling frequency. In short, CT  $\Sigma\Delta$  modulation provides a seamless transition between the optical and digital domains (see Figure 2-17).

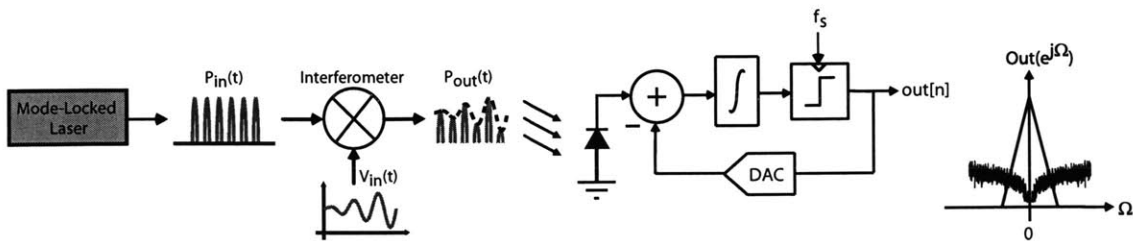


Figure 2-17: Diagram of the entire optical-electrical sub-sampling down-conversion receiver with  $\Sigma\Delta$  modulation.

## 2.4 Summary

This chapter introduced two key optical devices that are exploited in this thesis: the mode-locked-laser and the interferometer. The low-jitter of the mode-locked-laser pulses and the high-bandwidth of the interferometer can be leveraged to achieve accurate sub-sampling of high-frequency (10's of GHz) RF signals. The merits of the optical sub-sampling architecture over traditional down-conversion architectures were discussed. The problems associated with charge compartmentalization and MOS switch non-idealities were analyzed, and the removal of the entire S/H network proposed. Finally, CT  $\Sigma\Delta$  modulation was introduced as a mechanism to compensate for the continuous charge integration of the directly connected photodiode and capacitor, and as an elegant means to digitize the optical information.

# Chapter 3

## Continuous Time (CT) $\Sigma\Delta$ A/D Conversion

### 3.1 Overview: DT $\Sigma\Delta$ Modulation vs. CT $\Sigma\Delta$ Modulation

While pipe-line and flash data converters currently dominate the high-speed, high-resolution application space, the large power consumption that such converters typically require (hundreds of milliwatts) has limited their use in applications with a lower signal bandwidth and tighter power budget.  $\Sigma\Delta$  modulation is a much more attractive alternative for such an application space because of the power savings the structure can offer for a given precision. Indeed, low-power, high-resolution discrete-time (DT) modulators employing switch-capacitor (SC) filters have proven highly successful in applications with sub-megahertz signal bandwidths, such as high performance audio [1].

Unfortunately, DT  $\Sigma\Delta$  modulators with larger signal bandwidths are not easily implemented (see Figure 3-1). To achieve even moderately large over-sampling ratios (OSRs) of 32 or 64, the sampling rates of 64 MHz and 128 MHz, respectively, are needed for a conversion bandwidth of just 1 MHz. While such clock signals are easily realized in modern CMOS processes, the requirements that the topology dictates for

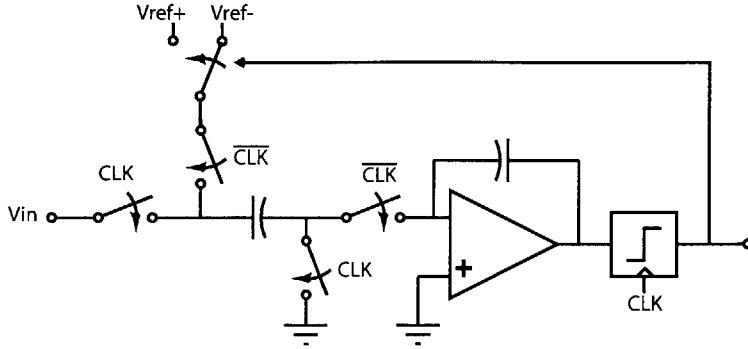


Figure 3-1: A switched-capacitor 1<sup>st</sup> order  $\Sigma\Delta$ .

the op-amp become prohibitive. Indeed, switch-capacitor implementations require high op-amp DC gain ( $> 40$  dB) and unity-gain bandwidths at least 5-10 times larger (320 MHz to 6.4 GHz in the above example) than the sampling rate to meet settling requirements. Neither requirement is easily met in sub-micron CMOS as the inherent transistor gain,  $g_m r_o$ , decreases with scaling, often requiring regulated-cascode amplifiers, which exacerbate noise and power consumption issues. Furthermore, op-amp gain-bandwidth requirements cannot be relaxed by simply scaling capacitors and switches. Precision requirements preclude scaling capacitors due to subsequently enhanced  $\frac{kT}{C}$  noise, clock-feedthrough, and charge injection errors, and finite MOS on-resistance preclude scaling switches due to longer settling transients.

Continuous-time (CT)  $\Sigma\Delta$  modulators do not have such strict requirements on amplifier gain-bandwidths. The conventional implementation, shown in Figure 3-2, involves an open-loop Gm-C integrator that does not require any feedback switches or capacitors. Instead, charge is dumped directly into the integrating capacitor at the output of the amplifier. Consequently, there are no settling-time requirements for the integrator, allowing for much lower amplifier gain-bandwidth products and decreased power consumption for a given sampling rate. Since CT modulators do not need to compartmentalize charge, they do not require sample-and-hold (S/H) circuitry at the input, reducing inband noise and improving linearity due to the absence of  $\frac{kT}{C}$  switching noise, clock-feedthrough, charge injection, and MOS on-resistance non-linearity. Finally, CT modulators provide an inherent anti-aliasing filter due to the sampling event occurring immediately before quantization [18].

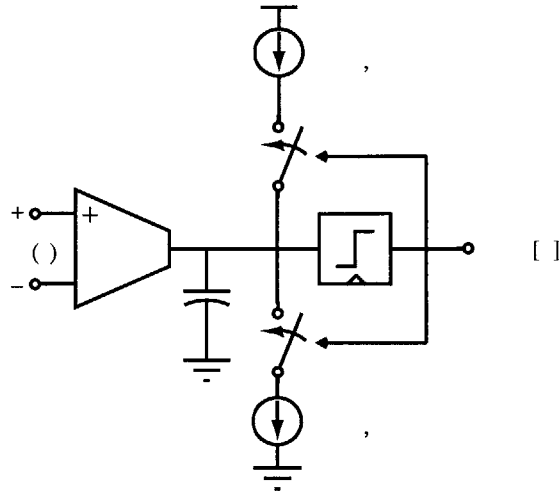


Figure 3-2: A simple 1<sup>st</sup> order CT  $\Sigma\Delta$  integrator.

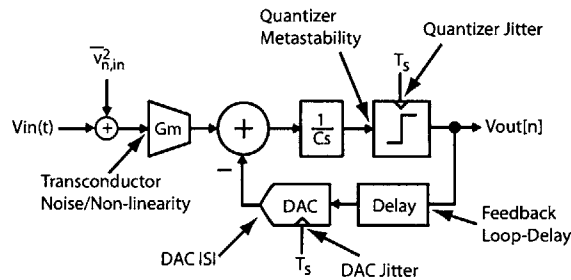


Figure 3-3: Non-idealities in block diagram for a 1<sup>st</sup> order CT  $\Sigma\Delta$ .

## 3.2 CT $\Sigma\Delta$ Limitations

Despite the numerous advantages that the CT  $\Sigma\Delta$  converter has over its DT counterpart, the topology does have some drawbacks: increased sensitivity to clock jitter, feedback loop delay, inter-symbol interference (ISI), quantizer metastability, and input transconductor noise and non-linearity. From Figure 3-3, note that all of these non-idealities either occur at the input or can be referred to the input,  $(\overline{v_{n,in}^2})$  and therefore will not be filtered out by the  $\Sigma\Delta$  action. Indeed, these noise sources are akin to the  $\frac{kT}{C}$  noise of the S/H in the DT case in that they “fill in” the noise-notch created by the zero at DC. Consequently, much work has been done in CT  $\Sigma\Delta$  design to compensate for these issues.

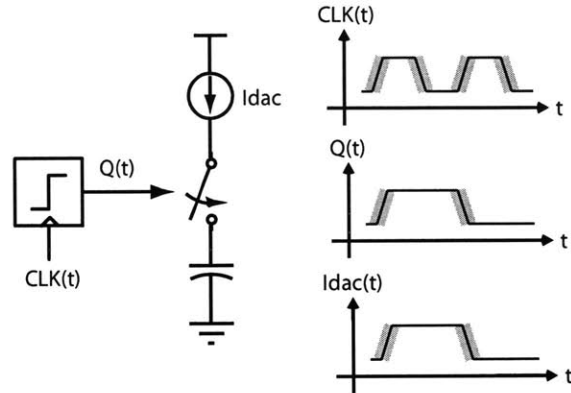


Figure 3-4: Illustration of the effect of DAC jitter on the  $\Sigma\Delta$  operation.

### 3.2.1 Compensating DAC Jitter

Clock jitter presents a serious challenge in high-speed CT  $\Sigma\Delta$  design, and can result in substantial SNR degradation [2],[12]. The effect of jitter on the system can be understood with the help of Figure 3-4. Quantizer and DAC clock jitter directly modulate the amount of charge supplied by the DAC in a given sample period. Since  $\Sigma\Delta$  modulators rely on charge conservation to realize the filter transfer function, any random modulation of the amount of charge stored on the integrating capacitors will result in a spectral “smearing” of the filter characteristic (see Figure 3-5).

Alternatively, the above results can be understood by noticing that DAC jitter contributes noise directly to the modulator input, and quantizer jitter can be directly referred to the input. Like thermal noise in the input stage transconductor, DAC jitter is unaffected by the noise-shaping dynamics of the  $\Sigma\Delta$  loop, and therefore appears as a white noise floor in the output spectrum. Ideally, quantizer jitter should not contribute to the noise floor of the output spectrum. However, many implementations of high-speed CT  $\Sigma\Delta$  converters use an asynchronous DAC that is driven by a synchronous quantizer in order to minimize loop delay. As a result, there is no distinction between quantizer and DAC jitter in such topologies.

Typically, the quantizer and DAC clocking signals are generated by buffering the output of a VCO. As a result, the unique phase noise characteristics of the VCO result in a non-white clock jitter [12]. Indeed, as shown in Figure 3-6, the accumulative noise

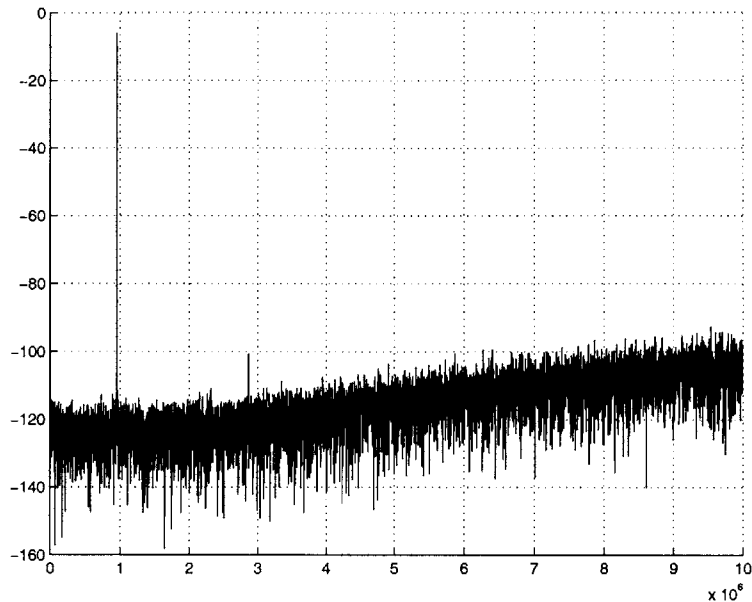


Figure 3-5: The effect of white clock jitter on the output spectrum of a 2<sup>nd</sup> order CT  $\Sigma\Delta$  modulator.

skirts of the VCO appear in the output spectrum, spaced at intervals equal to the signal frequency (in the diagram,  $f_{sig} = 953.6kHz$ ).

While clock-jitter is a problem for DT  $\Sigma\Delta$  converters as well, its effect is much more pronounced in CT  $\Sigma\Delta$  modulators. Comparing the DAC current pulse shapes in Figure 3-7, it is clear that clock jitter impacts a greater percentage of the DAC charge in the CT case. Note that simply changing the DAC pulse shape from non-return-to-zero (NRZ) to return-to-zero (RZ) will not help matters since an even greater percentage of the DAC charge will be affected by jitter [2].

Observing that the DT DAC is less sensitive to jitter because of the impulse like shape of the DAC current, several recent implementations have used SC DAC's for the first stage, demonstrating improved jitter tolerance [16]. However, as analyzed in [12], finite integrator gain causes the exponentially decaying current tail of SC based DAC's to become longer, which results in a greater percentage of the DAC charge being susceptible to jitter. At the same time, SC DACs introduce  $\frac{kT}{C}$  noise and all other switching non-idealities, such as clock-feedthrough, charge injection, and non-linear MOS on-resistance—all of which a designer presumably wishes to avoid with

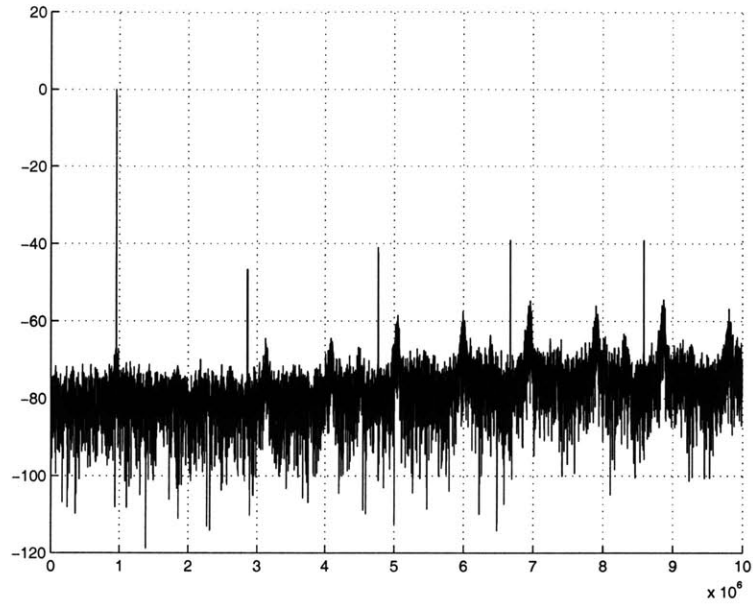


Figure 3-6: Effect of non-white VCO phase noise on the  $\Sigma\Delta$  spectrum.

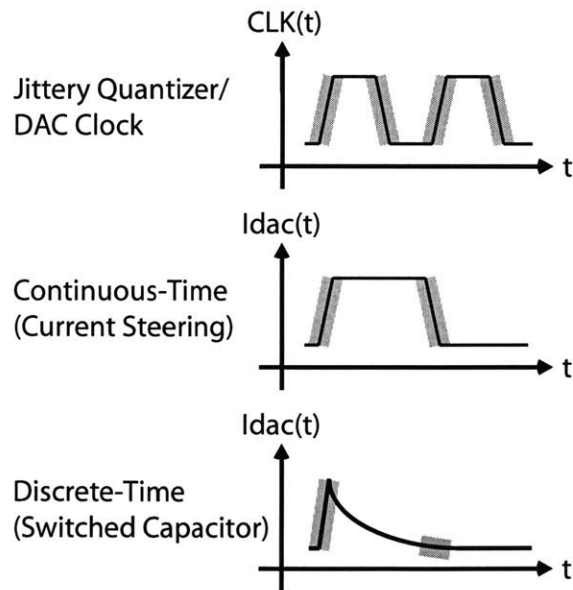


Figure 3-7: Current pulses for current-steered DAC and switch-capacitor DAC.



the CT approach.

Other methods for minimizing clock jitter include using a flash ADC with a multibit DAC, as shown in Figure 3-8. In addition to improving the SNR for a given OSR, the use of a flash ADC and multibit DAC can significantly reduce the amount of DAC charge being modulated by jitter (see Figure 3-9). However, this approach then places stringent linearity and precision requirements on the DAC that necessitate the implementation of current calibration loops and dynamic element selection algorithms to shape device mismatch. Consequently, decreased jitter sensitivity comes at the price of a significantly more complicated DAC implementation and greater power dissipation.

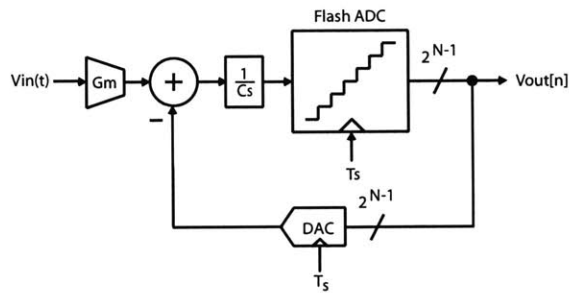


Figure 3-8: Block diagram of a multibit  $\Sigma\Delta$ .

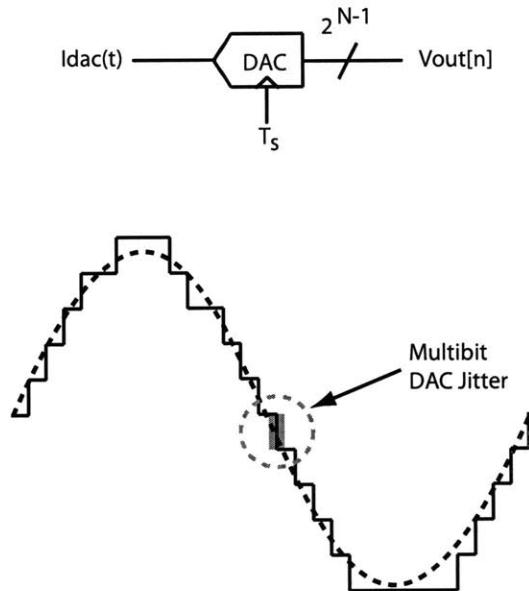


Figure 3-9: Jitter in a multibit DAC.

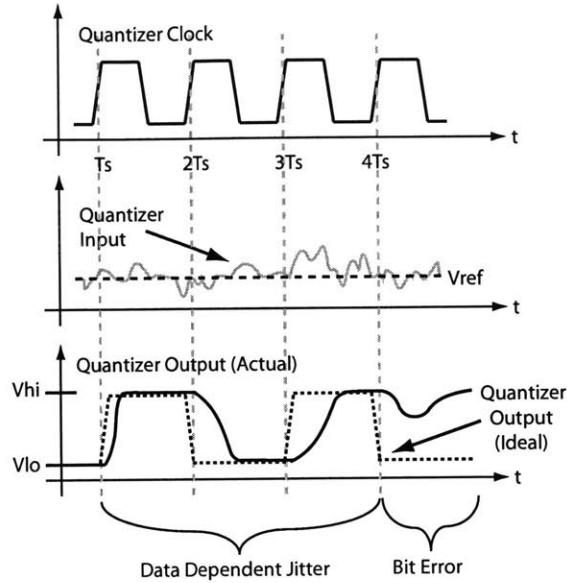


Figure 3-10: Illustration of quantizer metastability.

### 3.2.2 Compensating Metastability

Metastability occurs when the quantizer is unable to resolve its output to a logic high or low within the sampling period, resulting in a bit-error or signal-dependent quantizer output (see Figure 3-10). Since the effect of metastability worsens with smaller inputs [6]), typical  $\Sigma\Delta$  implementations utilize a broadband preamplifier, or cascade a second quantizer clocked a half sample period after the first quantizer (see Figure 3-11). Unfortunately, both forms of preamplification are limited by the finite gain-bandwidth product of the electronics, which typically result in either low-gain broadband amplifiers or quantizers with slow regeneration times. Furthermore, the latter of these two methods makes a tradeoff between quantizer resolution and delay. The authors of [3] showed that for modulators of order 2 or higher, delays in excess of 20% of the sampling period significantly degraded dynamic range (DR), and delays in excess of 50% of the sampling period drove the modulator to instability.

### 3.2.3 Compensating DAC ISI

Waveform asymmetry arises from non-zero rise and fall times of the DAC switching signal, and can be considered as a type of intersymbol interference (ISI). As shown

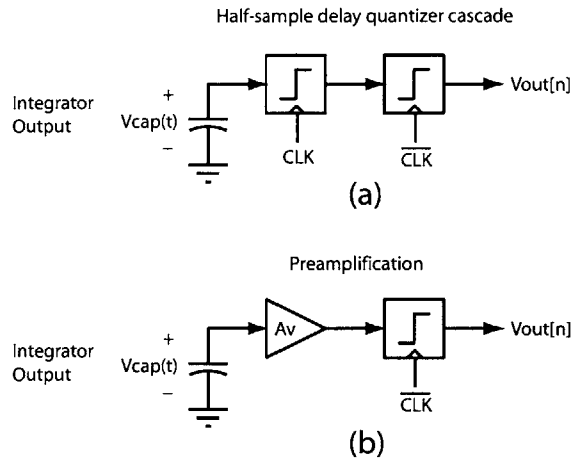


Figure 3-11: Reducing probability of quantizer metastability using a second quantizer (a) and a preamplifier (b).

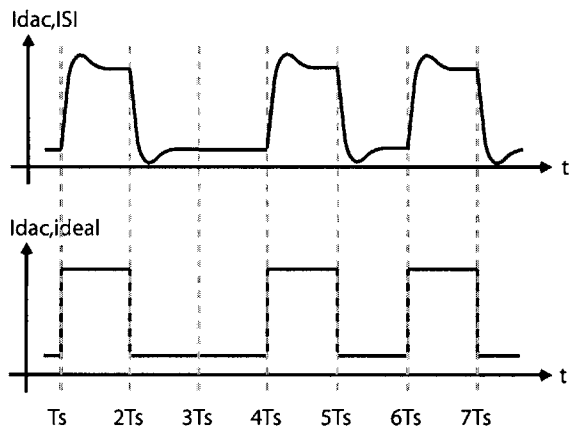


Figure 3-12: Illustration of DAC intersymbol interference (ISI).

in Figure 3-12, ISI causes signal information to be smeared into the next sampling period. Since the DAC charge is integrated on a capacitor, the resulting voltage signal may not settle before the quantizer samples the capacitor, resulting in either a sampling (bit) error or quantizer metastability. Either of these non-idealities can be described as a form of signal dependent jitter [2], and consequently manifests itself as a white noise floor in the output spectrum of the  $\Sigma\Delta$ .

A common solution to the problem of ISI is to use properly scaled return-to-zero (RZ) DAC pulses as opposed to non-return-to-zero (NRZ) pulses. When properly timed, such pulses can completely settle within the sampling clock period (see Figure 3-13).

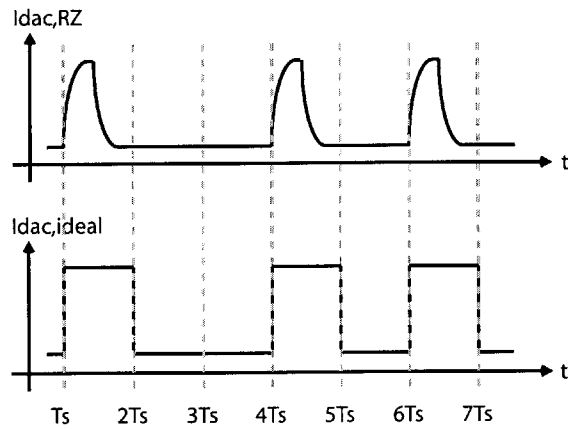


Figure 3-13: Illustration of ISI compensation using return-to-zero (RZ) DAC pulses.

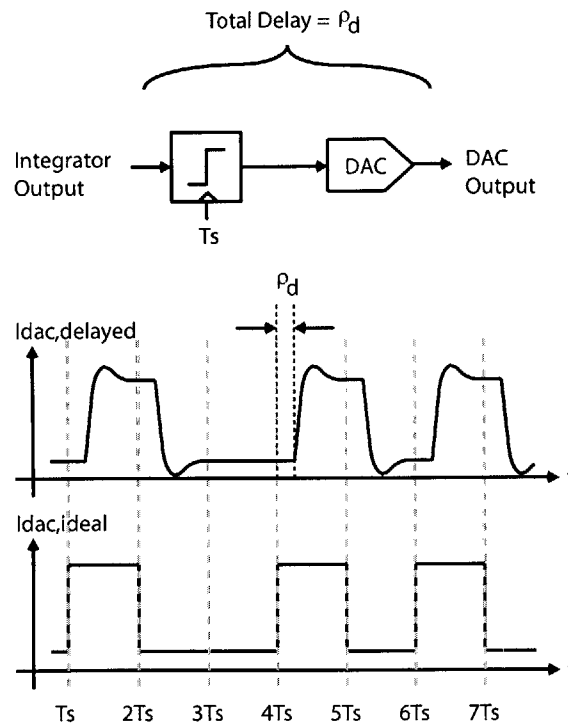


Figure 3-14: Illustration of clock-to-Q delay. Delay is measured from quantizer clock to the DAC output.

### 3.2.4 Compensating Feedback Loop Delay

Loop delay (or clock-to-Q delay) is a measure of the time required for the DAC to respond after the quantizer has been clocked. As analyzed and discussed in [3], loop delay in excess of 20% of the sampling period is a serious problem for CT modulators of order two or higher, resulting in distorted NTF and instability. These adverse effects arise from the delay causing a portion of the DAC signal to appear in the subsequent sampling period (see Figure 3-14). Mathematically, this fractional delay ( $\rho_d T_s$ ) causes the  $\Sigma\Delta$  loop filter transfer function to become higher in order, a consequence of an incomplete pole-zero cancellation that normally occurs when there is no delay. For a second-order CT modulator (see Figure 3-15) with feedback DAC currents  $k_1$  and  $k_2$  and loop delay  $\rho_d$ , the DT equivalent is as shown in Figure 3-16. The  $z$ -domain loop filter transfer function ( $H_{delay}(z)$ ) for this DT modulator is then:

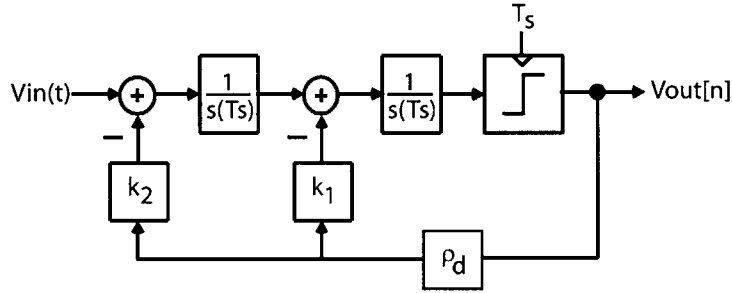


Figure 3-15: A second-order  $\Sigma\Delta$  with loop delay  $\rho_d$ .

$$H_{delay}(z) = \frac{a_2 z^2 + a_1 z + a_0}{8z(z-1)^2} \quad (NRZDAC) \quad (3.1)$$

where

$$a_2 = (k_1 + 4k_2) - (2k_1 + 4k_2)\rho_d + k_1\rho_d^2 \quad (3.2)$$

$$a_1 = (k_1 - 4k_2) + (2k_1 + 8k_2)\rho_d - 2k_1\rho_d^2 \quad (3.3)$$

$$a_0 = -4k_2\rho_d + k_1\rho_d^2 \quad (3.4)$$

In an ideal  $\Sigma\Delta$ , the delay would be zero ( $\rho_d = 0$ ), and the loop filter would then

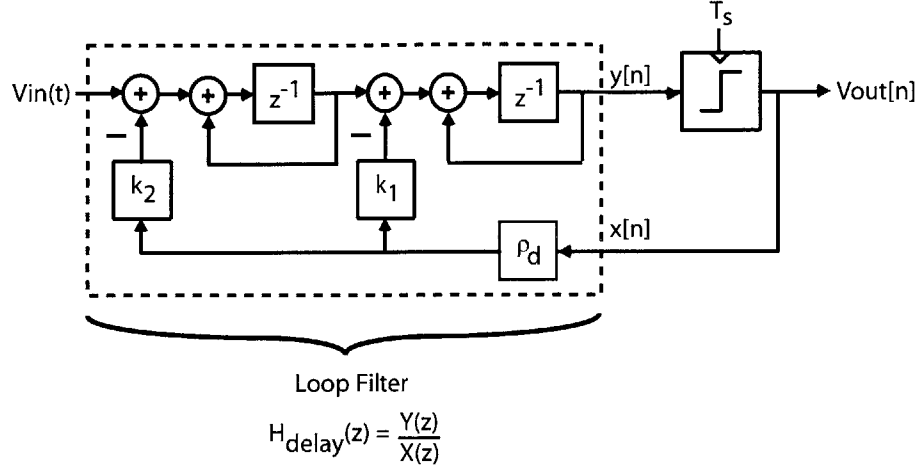


Figure 3-16: The discrete-time (DT) equivalent of the CT second-order  $\Sigma\Delta$  with loop delay  $\rho_d$  shown in Figure 3-15

become:

$$H_{delay}(z) = \frac{2z^2 - z}{z(z-1)^2} = \frac{2z-1}{(z-1)^2} \quad (Ideal) \quad (3.5)$$

To restore the proper signal transfer function, the authors of [3] proposed a return-to-zero (RZ) DAC scheme, as opposed to the conventional non-return-to-zero (NRZ) implementation (see Figure 3-17). In the NRZ DAC scheme, DAC current is steered from one integrating capacitor to another for the entire duration of the sampling period. However, in a RZ DAC scheme, DAC current is steered to the integrating capacitors for part of the sampling period, and cancelled for the remainder of the period. By properly scaling the DAC currents, the ideal NTF/STF can be attained. For example, in the second-order loop shown in Figure 3-16 using the RZ DAC scheme shown in Figure 3-17, the equivalent  $z$ -domain loop transfer function becomes:

$$H_{delay}(z) = \frac{(k_1 b_0 + k_2 b_1)z + (k_2 b_2 - k_1 b_0)}{(z-1)^2} \quad (RZDAC) \quad (3.6)$$

where

$$b_2 = \frac{1}{2}(\beta^2 - \alpha^2) \quad (3.7)$$

$$b_1 = \frac{1}{2}[\beta(2-\beta) - \alpha(2-\alpha)] \quad (3.8)$$

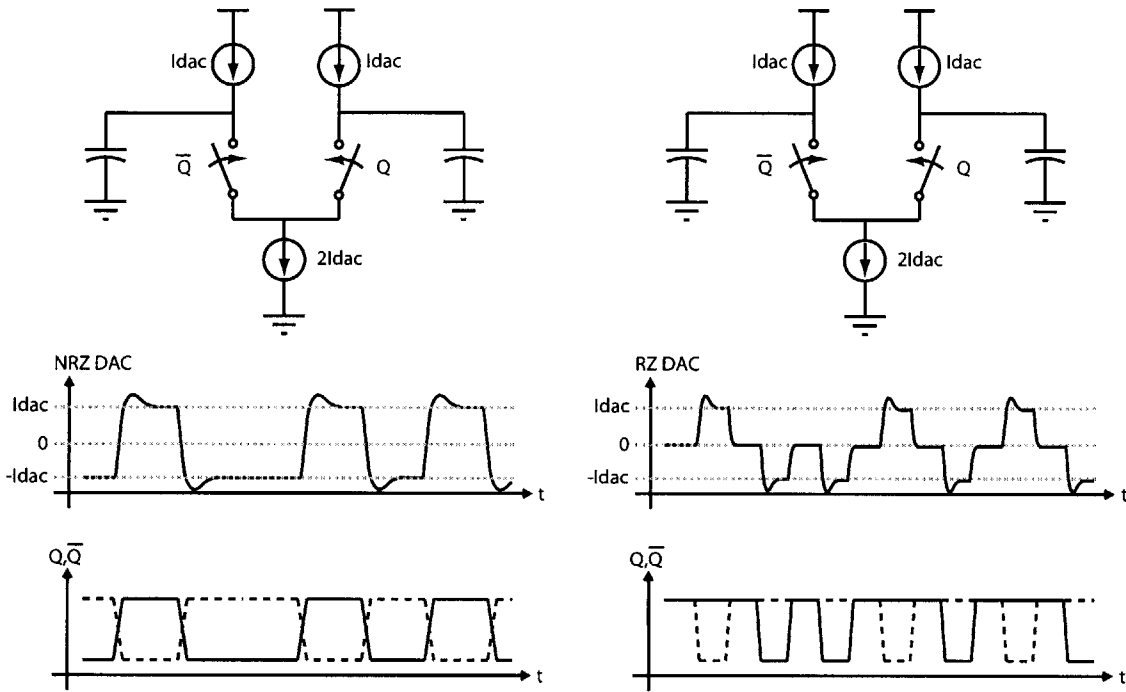


Figure 3-17: Illustration of delay compensation with RZ DAC pulses.

$$b_0 = \beta - \alpha \quad (3.9)$$

and where  $\alpha = \rho_d$  and  $\beta = 1 - PW - \alpha$ , as defined in Figure 3-18.

In order to get the ideal loop filter transfer function, one need only solve the system of equations above for  $k_1$  and  $k_2$  (see Appendix for MATLAB script). Similar methods for compensating band-pass and low-pass modulators of even higher order are detailed in [3]. This compensation scheme also enables the elimination of DAC ISI if the RZ pulses can settle within the sampling period.

An alternate feedback delay compensation method was implemented in [17] and is shown in Figure 3-19. Here, a delay of one sampling period is purposely introduced between the quantizer and the main DAC ( $DAC_A$ ). To still obtain the proper loop filter output by the next sampling instant, a second feedback loop delayed by half a period is introduced from the quantizer output to the quantizer input via a second DAC ( $DAC_B$ ). For example, for the second-order loop shown in Figure 3-16, the ideal impulse response ( $\rho_d = 0$ ) is given by the difference equation:

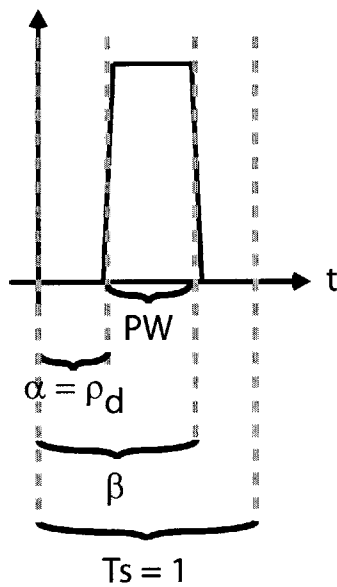


Figure 3-18: Illustration of  $\alpha$  and  $\beta$  as fractions of the normalized sample period ( $T_s = 1$ ). Note that  $\alpha = \rho_d$  in this framework.

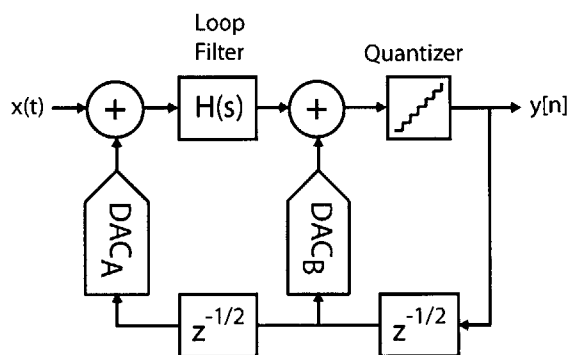


Figure 3-19: Illustration of loop delay compensation using the scheme described in [17].



$$y[n - 2] - 2y[n - 1] + y[n] = -2x[n - 1] + x[n - 2] \quad (3.10)$$

The resulting ideal impulse response is then:

$$h_{delay}[n] = (-1 - n)u[n - 1] \quad (Ideal) \quad (3.11)$$

Using the compensation method described above, the impulse response of the loop filter and  $DAC_B$  become:

$$h_{lf}[n] = (-1 - n)u[n - 2] \quad (3.12)$$

$$h_{DAC_B}[n] = -2\delta[n - 1] \quad (3.13)$$

Comparison of the time-domain impulse responses of the ideal delay-free loop filter and the compensation scheme described above shows that they are indeed equal (see Figure 3-20). This particular compensation scheme minimizes the probability of quantizer metastability since the quantizer now has effectively two sampling periods to resolve its input. However, since the scheme uses NRZ DAC pulses, it still suffers from DAC ISI.

### 3.2.5 Compensating Input Stage Noise and Non-Linearity

Since the input transconductor of the CT  $\Sigma\Delta$  modulators occurs outside the loop dynamics, it must meet the noise and linearity requirements of the entire converter. Typically, the first integrator in a CT  $\Sigma\Delta$  modulator is implemented using either the  $G_M C$  or RC topology. In  $G_M C$  integrators, greater linearity is achieved through some form of resistive degeneration or a cross-coupling and sizing of the input differential pair that results in a smaller effective  $G_M$  (see Figure 3-21 [8]). However, both implementations tradeoff linearity for excess noise.

In the case of a degenerated differential pair, the noise can be modelled as shown in Figure 3-22. The transfer function for each noise source referred to the output can

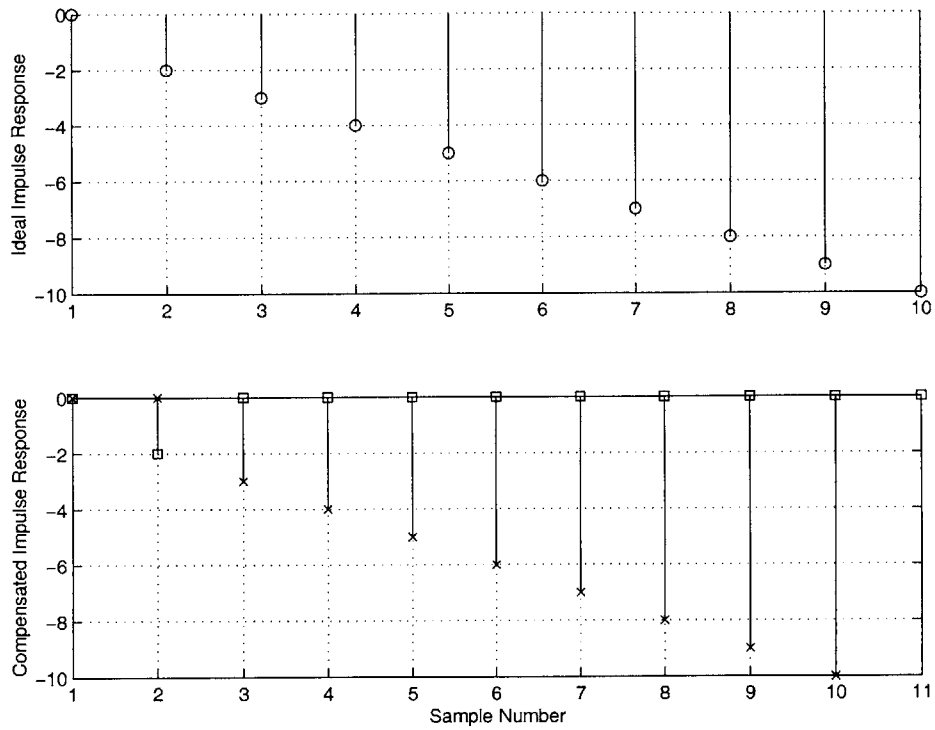


Figure 3-20: Ideal impulse response of a  $2^{nd}$  order loop and the reconstructed impulse response using delay compensation. The squares represent the output from  $DAC_B$  ( $h_{DAC_B}[n]$ ), and the X represents the output of the delayed loop filter ( $h_{lf}[n]$ ).

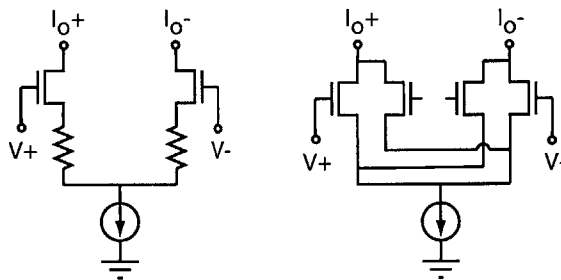


Figure 3-21: Illustration of the resistively degenerated and cross-coupled input pairs.

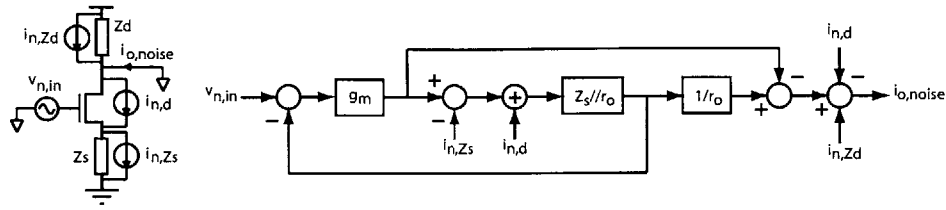


Figure 3-22: Noise model for (a) the degenerated amplifier with all noise sources included, and (b) block diagram used to calculate transfer functions.

be described as:

$$\left| \frac{i_{o,noise}}{i_{n,d}} = \frac{r_o}{Z_s + r_o + g_m r_o Z_s} \right| \quad (3.14)$$

$$\left| \frac{i_{o,noise}}{i_{n,Zs}} = \frac{Z_s + g_m r_o Z_s}{Z_s + r_o + g_m r_o Z_s} \right| \quad (3.15)$$

$$\left| \frac{i_{o,noise}}{i_{n,Zd}} = 1 \right| \quad (3.16)$$

When referred to the input, the output current noise is divided by the effective transconductance:

$$G_{m,eff} = \frac{g_m r_o}{r_o + Z_s + g_m r_o Z_s} \quad (3.17)$$

$$\overline{v_{n,in}^2} = \frac{\overline{i_{o,noise}^2}}{(G_{m,eff})^2} \quad (3.18)$$

The input referred noise of each of the noise sources then becomes:

$$\overline{v_{n,in,Zd}^2} = \left( \frac{4kT}{Z_d} \right) \left( \frac{r_o + Z_s + g_m r_o Z_s}{g_m} \right)^2 \Delta f \quad (3.19)$$

$$\overline{v_{n,in,Zs}^2} = (4kT Z_s) \left( \frac{1 + g_m r_o}{g_m r_o} \right)^2 \Delta f \quad (3.20)$$

$$\overline{v_{n,in,d}^2} = \frac{8kT\gamma}{3g_m} \Delta f + \frac{K}{WLC_{ox}f} \quad (3.21)$$

As expected, the input devices are scaled by  $\frac{1}{g_m}$  and can consequently be decreased by increasing their bias current and size. The noise contributed at the source of the input pair has an expected effect in that it is directly buffered to the output, as

the input devices look like common-gate amplifiers. However, the noise contribution from any devices at the drains of the differential pair (such as DAC and bias noise) is amplified by the degeneration factor and unaffected by changes in the input device  $g_m$ . With any degeneration, this noise will dominate, and grow with increasing degeneration (or equivalently, with decreasing  $G_{M,eff}$ . A similar result is reached when using cross-coupled input pairs since such topologies create a smaller  $G_{M,eff}$  by subtracting the  $g_m$ 's of the input devices.

RC integrators fare no better since they behave like  $G_M C$  integrators with  $G_{M,eff} = \frac{1}{R}$ . Consequently, DAC noise is still multiplied by  $R^2$  when input referred. At the same time, RC integrators further complicate design with op-amp stability issues, and suffer from any resistor and capacitor process variations that can distort the NTF/STF, leading to significant SNR degradation unless laser trimming and capacitor tuning is employed [12],[17]. Nevertheless, RC integrators are frequently used for the excellent linearity that the topology affords for a wide input voltage range. Indeed, the authors of [17] demonstrated 88 dB of dynamic range (DR) and a peak SNR of 84 dB with a 1.1 MHz signal bandwidth and an OSR of 32.

### 3.3 Summary

While CT  $\Sigma\Delta$  modulators present numerous advantages over DT  $\Sigma\Delta$  modulators, the topology still presents numerous design challenges. Many compensation techniques have been created to eliminate or mitigate the impact of non-idealities on the CT modulator. In the cases of DAC ISI and loop delay, existing electronic compensation techniques involving alternate pulse shapes and scaling DAC currents are sufficient. But compensation techniques for other non-idealities, such as quantizer metastability and DAC clock jitter, are limited by the inherent characteristics of the electronic devices that implement these circuits. Consequently, to achieve both high speed and high precision CT  $\Sigma\Delta$  modulation, the industry has had no choice but to seek more expensive, high-mobility bipolar technologies (SiGe, InP) [7].

# Chapter 4

## Optical-Electrical CT $\Sigma\Delta$ Modulation

The performance of existing high-speed, high-precision CT  $\Sigma\Delta$  modulators are hampered by the fundamental gain-bandwidth and clock jitter of the electronic devices. Given that the implementation of the VCO and mixer in the electronic direct down-conversion receiver was stymied by these same issues, it seems appropriate to investigate how optical signals and devices can be exploited in the design of CT  $\Sigma\Delta$  modulators. This chapter proposes two optical-electrical structures that strive to minimize the impact of DAC clock jitter and quantizer metastability. As in the optical-electrical sub-sampling network, the low noise and high gain-bandwidth of optics are leveraged to reduce jitter and improve the gain-bandwidth of the optical-electrical structures.

### 4.1 Reducing Clock Jitter

Once again, mode-locked lasers offer an attractive source for low-jitter clocking. In previous work [10], a phase-locked-loop (PLL) generated a 2 GHz RF signal using a mode-locked-laser reference at 100 MHz with only 60 fs of relative rms timing jitter. As mentioned in chapter 2, free-running high frequency ( $f_{rep} > 10kHz$ ) mode-locked lasers have jitter on the order of 10's of femtoseconds. Since an existing laser setup with a maximum repetition rate of  $f_{rep} = 780MHz$  was available, an electrical clock

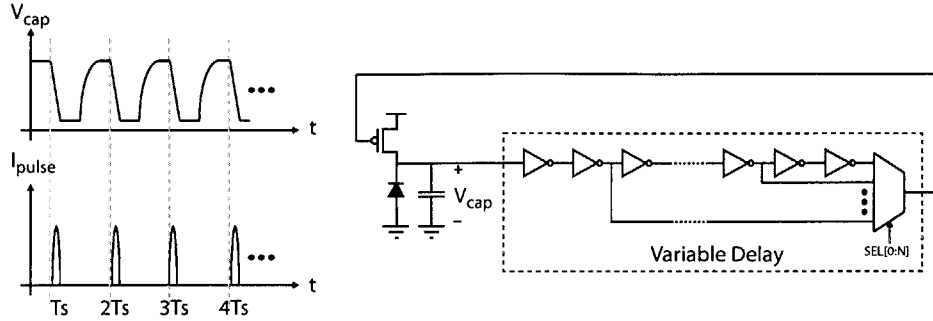


Figure 4-1: Schematic of the optical clock generator.

generated by the free-running laser was chosen over the complexity of designing an entire PLL. Even with a bandwidth of 1 MHz, the  $\Sigma\Delta$  would have an  $OSR = 390$ , which was sufficiently high for this prototype.

Since the mode-locked-laser pulses are used as a reference, the optical clock needs a photodiode to translate the optical timing information into the electrical domain. In an effort to demonstrate integrated optics and electronics, an on-chip N-well/P-substrate diode was chosen over a discrete device. As shown in Figure 4-1, the optical pulses incident on the photodiode generate a clean falling edge caused by the discharging of all capacitances at the diode anode. This edge then propagates through a variable delay line and then switches on the PMOS stacked on top of the photodiode, creating a rising edge. The duty cycle of the clock is controlled by the total delay encountered through the variable delay element. The resulting electrical clock signal is buffered by the fewest stages possible, and clocks the DAC off of the clean falling edge in order to minimize jitter.

Note that jitter generated in this structure is not the same as VCO accumulative jitter since the falling edge is completely independent of the rising edge. That is, the rising edge caused by the PMOS switching on does not trigger the subsequent falling edge since the optical source is decoupled from the generated electrical clock signal. Furthermore, observe that the jitter would improve if the fall-time of the falling edge were shorter. Indeed, faster fall times can be achieved by simply increasing the optical power. But as shown in Figure 4-2, increased optical power will eventually cause the diode to forward-bias. Forward-biasing the diode may cause severe substrate noise

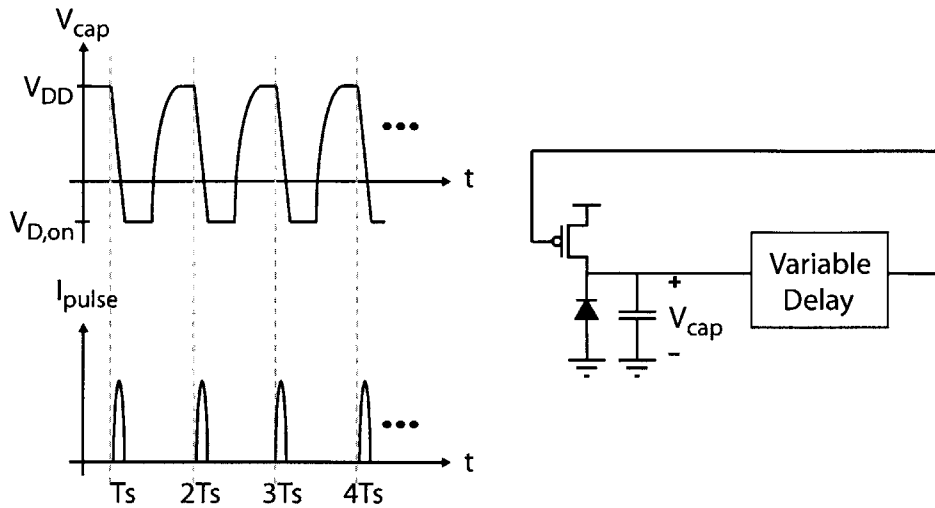


Figure 4-2: Illustration of optically generated current being injected into the substrate by the forward biasing of the photodiode.

issues, as a large number of carriers will be periodically injected into the substrate. This is particularly troublesome, as any noise coupling is enhanced due to the substrate being made of a low-resistivity material.

If off-chip photodiodes are an option, the clocking scheme shown in Figure 4-3 may yield an even lower jitter, though at the cost of extra complexity on the optical side. Here, two stacked photodiodes continuously charge and discharge the output node, but do so at opposite phases relative to each other. Where the delay was previously done in the electrical domain, here the delay occurs in the optical domain via a splitter and optical fiber. This optical technique is widely used since the delay can be controlled within femtosecond precision. This approach has another advantage in that edges can be made extremely sharp without the problems of substrate noise if the diodes are discrete devices.

## 4.2 Reducing Quantizer Metastability

As previously mentioned, electronic compensation techniques for metastability are limited by the gain-bandwidth of the devices. This hard limit typically resulted in low-gain, broadband preamplification, and longer loop-delays due to signal propagation

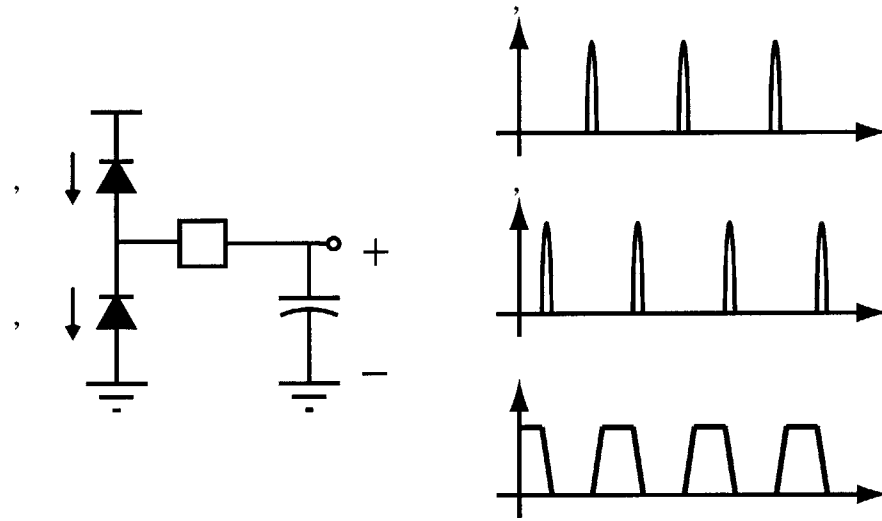


Figure 4-3: Schematic of the optical clock using stacked off-chip photodiodes.

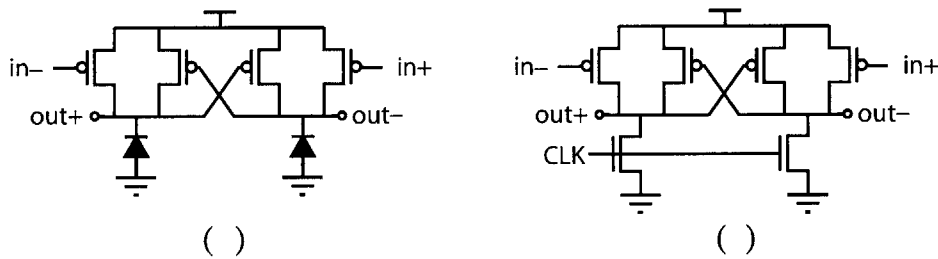


Figure 4-4: Schematic of the optical-electrical latch (a), and the purely electrical latch (b).

through cascaded regenerative flip-flops. Introducing optical devices into this classical electronic problem may result in a quantizer that can exceed the gain-bandwidth limitations of the electronics.

The proposed optical-electrical structure is shown in Figure 4-4(a). An electronic “equivalent” (Figure 4-4(b)) is juxtaposed to the proposed structure for comparison. Analysis in the following paragraphs will demonstrate three potential advantages that the optical-electrical structure affords compared to its purely electrical counterpart. For the basis of fair comparison, the PMOS structures in both circuits are identical, and the NMOS is sized such that its effective drain capacitance is equal to the effective photodiode depletion capacitance ( $\approx 20fF$ ). As with the optical-electrical clock, an on chip N-well/P-substrate diodes are assumed. While faster, discrete photodiodes



made of III-V materials (e.g., GaAs) would be preferred, the capacitive loading from the bond pads and the diode would be excessive ( $> 1$  pF), making the use of such devices impractical.

**Improved I/C Ratio** - Recall from chapter 2 that photodiode current is described by  $I_{opt} = RP_{opt}$ , where  $R$  is the responsivity [A/W] of the photodiode, and typically has a value of  $R \approx 0.1$  to  $0.5$ . Here,  $I_{opt} \propto P_{opt}$ , and more diode current can be generated by increasing  $P_{opt}$ . For example, assuming  $R = 0.2$  and  $P_{opt}$  is doubled to  $200mW$ , the resulting photocurrent is  $I_{opt} = 40mA$ . Current generated by the NMOS is described by:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[ (V_{GS} - V_T)V_{DS} - \frac{(V_{DS})^2}{2\kappa_s} \right] \quad (Triode) \quad (4.1)$$

$$I_{DS} = \kappa_s \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (Saturation) \quad (4.2)$$

The above equations are for the triode and saturation regimes, and indicate that high NMOS current requires high  $V_{GS}$ . However,  $I_{DS}$  can only be increased up to the point where  $V_{GS} = V_{DD}$ . Even if it were possible to drive the gate voltage beyond the supply voltage, the oxide breakdown voltage still limits the maximum overdrive (for this  $0.18\mu m$  process,  $V_{breakdown} \approx 4.2V$ ). Simulation shows that for  $V_{GS} = V_{breakdown}$ ,  $I_{DS,max} \approx 20mA$ , but in practice such an overdrive would cause irreparable damage to the device.

The informal analysis above indicates that the optical-electrical structure may be able to generate a larger current for a given device capacitance (i.e., larger I/C ratio) compared to the purely electrical structure. This result suggests that the optical approach allows for shorter edges, enabling the quantizer to reach the metastability threshold sooner and resolve to its final value faster than the electrical implementation. This result could also have great value for other unrelated structures where fast edges are critical, such as limit amplifiers.

**Improved Rise Time** - As mentioned in the previous chapter, mode-locked lasers

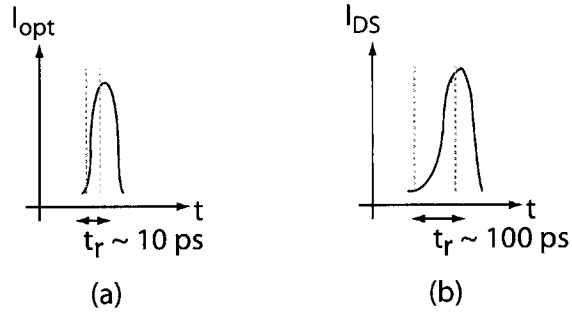


Figure 4-5: Illustration of the finite current pulse risetimes for (a) a photodiode, and (b) an NMOS transistor.

can generate optical pulses as narrow as 100 fs. When such pulses are incident on a photodiode, electrical carriers are created, generating equivalent current pulses. Due to the finite generation rate of carriers, the 100 femtosecond optical pulses will effectively be low-pass filtered by the photodiode, which widens the pulses so that they are on the order of tens of picoseconds. Despite this filtering, the rise time of the current pulses are still extremely fast, typically on the order of 10 picoseconds for a pulse with a peak current of 10 mA (see Figure 4-5(a)).

Generating such short pulses electronically is extremely challenging due to the finite gain-bandwidth of the transistors. SPICE simulations indicate that a minimum length ( $0.18 \mu\text{m}$ ) NMOS had to be  $22 \mu\text{m}$  wide to generate 10 mA of current when the gate overdrive was equal to  $V_{DD} - V_T$ . Such a large width is necessary because the NMOS is operated deep in the triode region, which weakens the current drive of the entire device. Unfortunately, increasing the device geometry simultaneously increases the effective gate capacitance of the transistor. Even with a well-buffered CLK signal, the loading presented by this gate capacitance resulted in simulated rise times on the order of 100 picoseconds (see Figure 4-5(b)).

**Improved Gain at Metastability** - When a latch enters a metastable state, an indefinite period of time must pass before the latch is able to resolve to a logic high or low. The amount of time that must transpire before the latch can resolve largely depends on the input signal levels at the moment the latch is triggered, and the gain of the latch at this metastable threshold [2]. Figure 4-6 shows the linearized small-signal

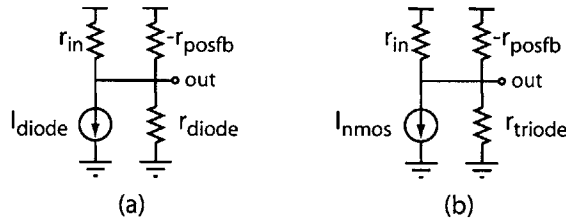


Figure 4-6: Linearized small-signal models at the metastable threshold for the (a) optical-electrical latch, and the (b) electronic latch.

model of the half circuits of the (a) optical-electrical (b) electrical latches depicted in Figure 4-4. This is based on the linearized model used in [6]. Note that the small signal resistance of the diode is enormous ( $M\Omega$  range) because the diode is reverse-biased. Consequently, the gain of the latch is determined purely by the PMOS input devices and cross-coupled pair. In contrast the gain of the electronic latch is degraded by the trioded NMOS, which presents a low-impedance ( $\approx 100\Omega$ ) to the output.

The above analysis suggests that the optical-electrical latch may provide a larger gain than the purely electronic version. A larger gain at the metastability threshold can translate to an overall shorter resolving time for the latch. It should be noted that since the optical properties of the photodiodes in this process are unknown, only an estimate of the actual performance can be given. Simulations using ideal current sources to mimic the photoelectric effect corroborate the informal analysis presented here, though photodiode transient behavior, such as the junction recombination, could not be simulated.

### 4.3 Summary

Optics offer an attractive alternative to electronics due to the low jitter and high speed afforded by mode-locked-lasers, and the near ideal current source behavior of photodiodes. Two structures employing integrated optical devices demonstrated potentially significant advantages over electronic equivalents. The optical-electrical clock generated low-jitter edges based on the mode-locked laser pulses and lacked the accumulative jitter of conventional electronic VCOs. The optical-electrical latch

enabled faster rise times due to the fast carrier generation rate of the photodiodes and consequently improved the effective gain-bandwidth product of the electronics. These preliminary results highlight the many possibilities of optoelectronics, and emphasize the need for further investigation into this growing area of research.

# Chapter 5

## System Architecture and Circuit Design

This chapter describes the overall architecture of the chosen  $\Sigma\Delta$  topology. Here the focus is on the design of the remaining electrical blocks.

### 5.1 General Architecture

A second-order (double-integrating) CT  $\Sigma\Delta$  architecture was chosen because it offered reasonable quantization noise-shaping for a moderately complex circuit implementation (see Figure 5-1). Furthermore, a single-bit quantizer and DAC were chosen for simplicity. While a multibit implementation would have yielded improved SNR and a reduced sensitivity to jitter, the implementation overhead would have been excessive, requiring complex DAC mismatch-shaping algorithms and current calibration circuitry.

An RZ DAC was chosen over the conventional NRZ DAC since it allowed for the DAC transients to completely settle within the  $\Sigma\Delta$  sample period. Consequently, any inband noise contributions from DAC ISI were almost completely eliminated. The RZ DAC also allowed for loop delay compensation. SPICE simulations, which included parasitics extracted from layout, indicated that the overall CLK-to-Q delay was approximately 500 picoseconds, or approximately 40% of the approximately 1.282

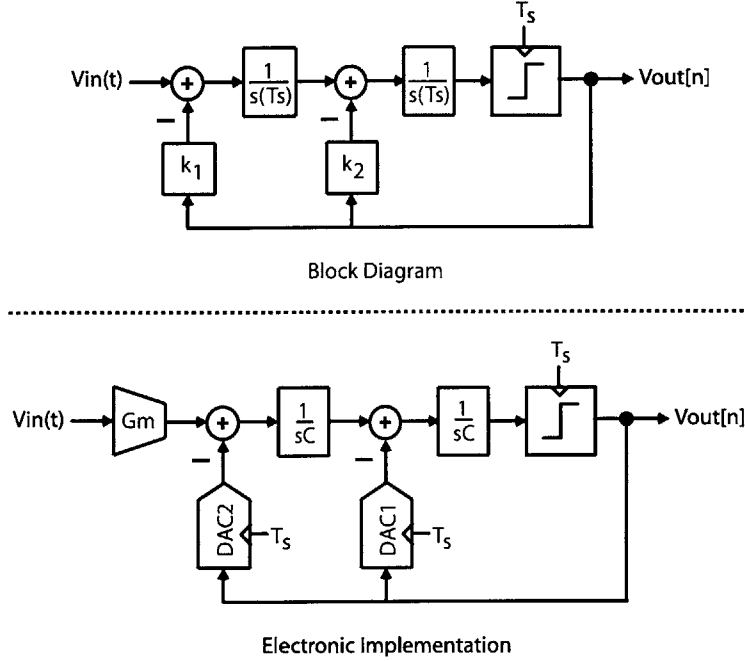


Figure 5-1: A block diagram of the  $2^{nd}$  Order  $\Sigma\Delta$  modulator chosen for this thesis.

nanosecond  $\Sigma\Delta$  period ( $f_s = 780MHz$ ) for the slowest process corner. Using the scheme proposed in [3] and described in the previous chapter, DAC currents were set to compensate for this delay such that the noise transfer function (NTF) was not distorted (see Appendix for script).

## 5.2 Analog Circuit Design

The analog core comprises two blocks: the first and second integrators. While the heart of this project is the use of the interferometer and photodiodes as the input to the  $\Sigma\Delta$ , an electronic input stage was also designed. This option allows for easy verification of the  $\Sigma\Delta$  operation, and provides a basis for comparison between the optical-electrical and purely electronic converters.

### 5.2.1 Optical Input Stage

While the interferometer and photodiode have been thoroughly analyzed in the previous chapters, little has been said concerning the biasing of this optical-electrical

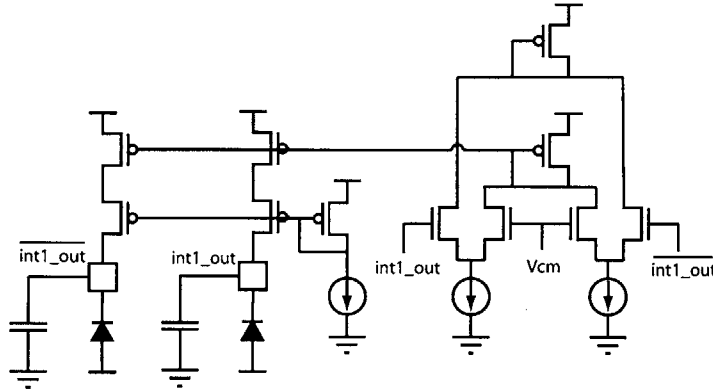


Figure 5-2: Schematic of the optical input stage with biasing and CMFB circuitry included.

circuit. Figure 5-2 shows the complete integrator topology including common-mode feedback (CMFB) circuitry. Behavioral simulations indicate that each output of the first integrator may swing as much as  $\pm 300$  mV around the common-mode output level ( $\frac{V_{DD}}{2}$ ). To meet the swing requirements with minimal distortion, as well as to ensure sufficient gain, a wide-swing cascode topology was chosen.

The CMFB circuitry shown in Figure 5-2 comes from [8], and is able to tolerate a large CM range. Long channel devices were used to minimize the  $\frac{1}{f}$  noise contribution of the top bias PMOS transistors as well as the NMOS differential pair transistors. Nevertheless, noise calculations indicate that the shot noise of the diodes will dominate, and that electronic thermal noise contribution is minimal. As an added bonus, the use of reverse-biased photodiodes enables larger gain since the PMOS output resistance is shunted by a near infinite resistance. Simulations indicate that the overall structure has a gain of approximately 45 dB.

The power dissipation of the optical input stage is largely dependent on the responsivity of the photodiodes, as well as the average optical power generated by the mode-locked laser. For example, assuming an average optical power of 5 mW and a photodiode responsivity of 0.5 A/W, the quiescent bias for each photodiode is 2.5 mA, which translates to a power dissipation of 9 mW. Assuming a total bias of 1 mA for the CMFB circuitry, the total power dissipation increases to about 11 mW. To allow

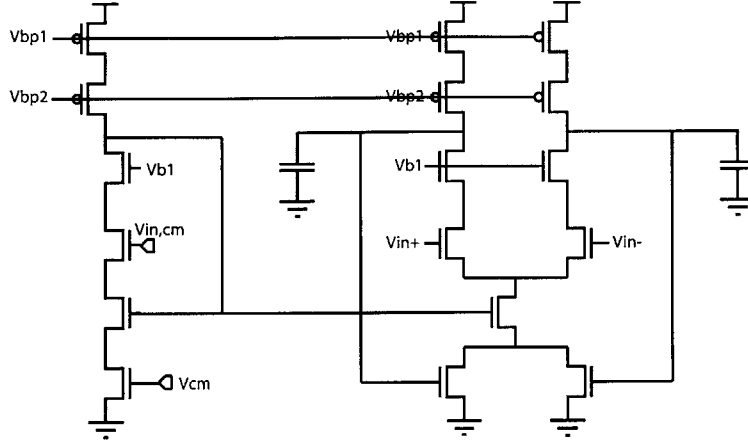


Figure 5-3: Schematic of the electronic input integrator.

for greater flexibility, the bias for the optical input stage will be made programmable to supply bias currents up to 5 mA per photodiode.

### 5.2.2 Electronic First Integrator

The electronic front-end integrator was designed using a similar structure to that described in [14] and is shown in Figure 5-3. A folded-cascode topology was chosen for maximum gain and minimal noise contribution. To minimize the total input referred noise, degeneration was avoided, which necessitates small signal swings. Simulations show that the transconductor behaves linearly even with  $\pm 50mV$  signals at each input node. As before, long-channel ( $L \approx 2\mu m$ ) devices were used to minimize the  $1/f$  noise contributions of the bias PMOS and input NMOS differential pair. An alternate CMFB scheme was used since it could be easily lumped into the bias tail of the integrator without causing significant headroom issues, and contributed no noise to the output. Simulations indicate that the structure achieves a gain of approximately 46 dB, and dissipates 4.3 mW (CMFB circuitry included).

### 5.2.3 Second Integrator

The second integrator is shown in Figure 5-4. Resistive degeneration was used to satisfy the large input voltage range (approximately  $\pm 600mV$  differential). Although



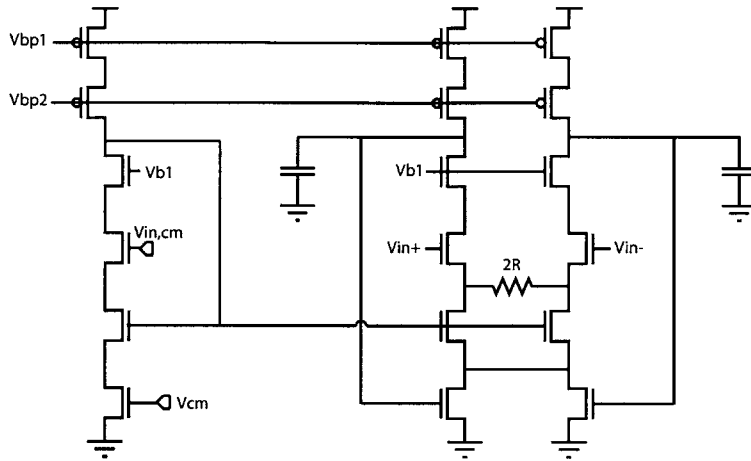


Figure 5-4: Schematic second integrator using resistive degeneration to maximize the linear range.

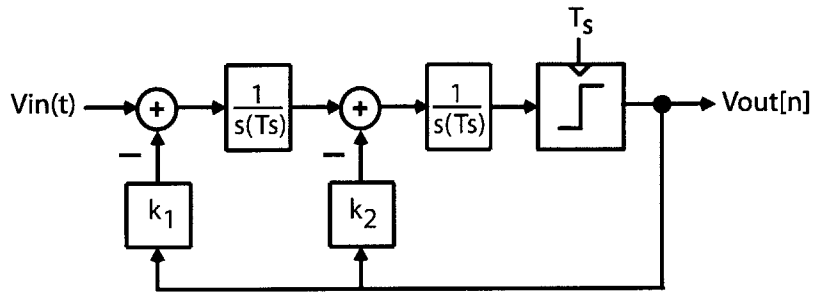
degeneration increases the input referred noise to the integrator by  $R^2$ , the noise contribution is negligible due to noise-shaping when referred to the input of the  $\Sigma\Delta$ . Behavioral simulations indicate that the output swing of the second integrator is only  $\pm 150mV$  differential, and therefore headroom is not a real concern. SPICE simulations indicate that the gain of the integrator is approximately 35 dB, and consumes only  $540 \mu W$ .

## 5.3 Digital Circuit Design

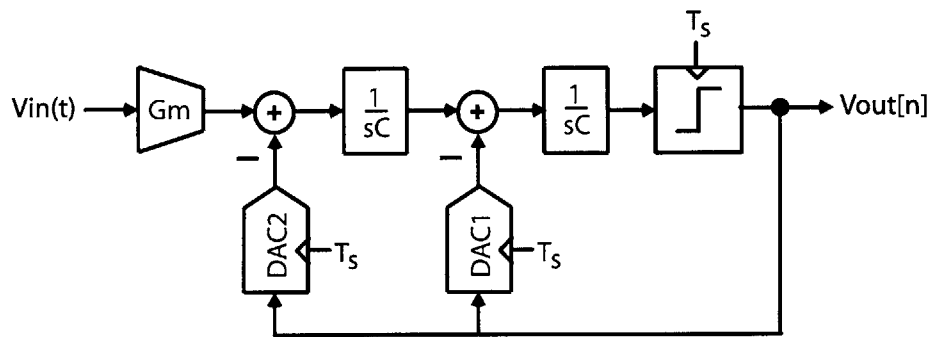
There are three key digital blocks for the  $\Sigma\Delta$  topology described in Figure 5-5: the quantizer, the four-phase DAC driver, and the DAC unit element. In addition there is a single-ended to differential clock generating circuit to drive the source-coupled logic (SCL).

### 5.3.1 Quantizer

The quantizer is shown in Figure 5-6, and is a standard master-slave flip-flop. An SCL topology was chosen for its speed, though at the price of static power dissipation. While a fully regenerative latch driving an RS latch could have been used as in [1], the longer clock-to-Q delay incurred was undesirable (on the order of 500 picoseconds).



Block Diagram



Electronic Implementation

Figure 5-5: A second-order  $\Sigma\Delta$  loop.

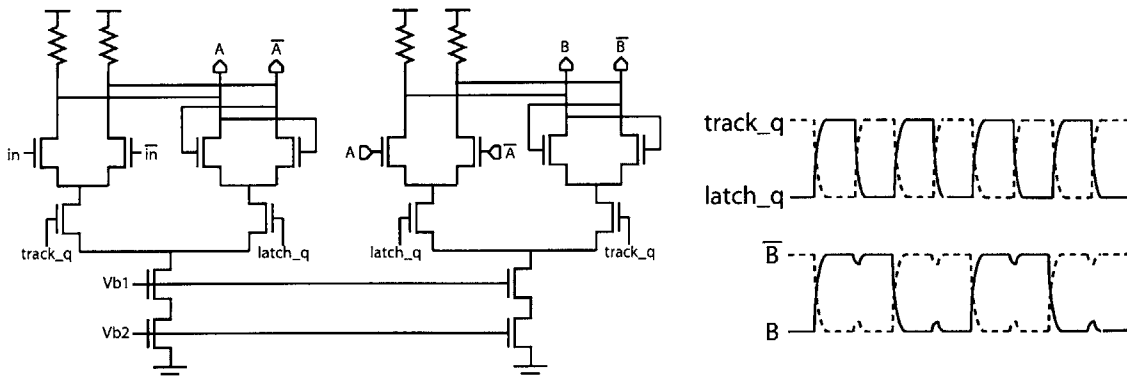


Figure 5-6: Schematic of the NRZ quantizer.

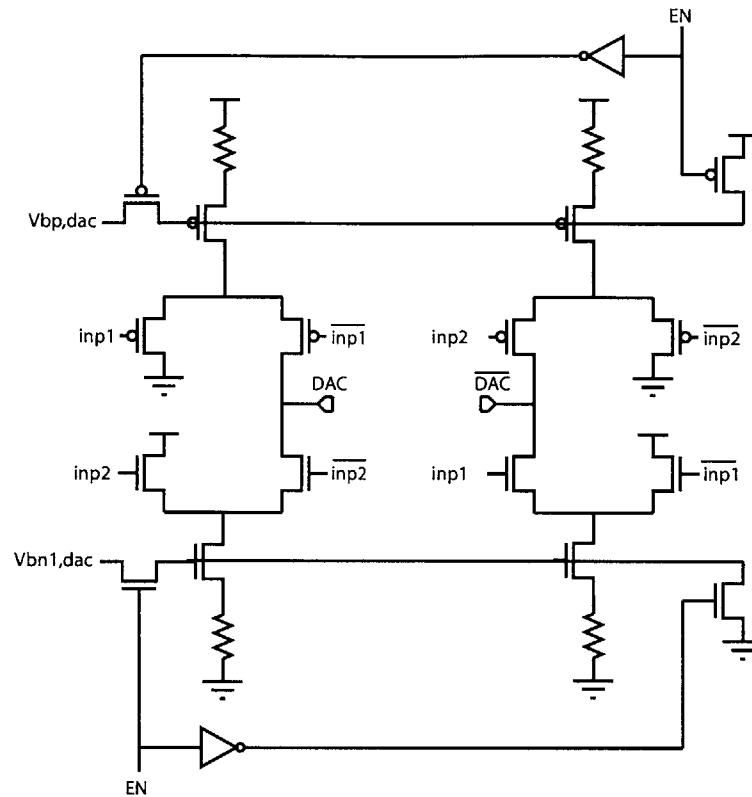


Figure 5-7: Schematic of the DAC unit element.

In contrast, the SCL structure depicted in Figure 5-6 has a 2 GHz bandwidth at the slowest process corner, and can usually resolve to a logic high or low in under 300 picoseconds. Metastability will of course prolong the latching time, though this is true for both the fully-regenerative and SCL topologies. The entire structure consumes less than 1.1 mW of power and has a 500 mV single-ended (1 V differential) output swing. It was designed using the script described in [5].

### 5.3.2 DAC Unit Element

The DAC unit element is shown in Figure 5-7. Since any noise from the first DAC contributes directly to the input of the  $\Sigma\Delta$ , extreme care was taken to minimize device noise. In particular, resistive degeneration was used to eliminate the  $1/f$  noise contribution to the output that would occur if an active device were used to establish the bias. The limited signal swings provided by the level shifting buffers ( $\pm 250mV$ )

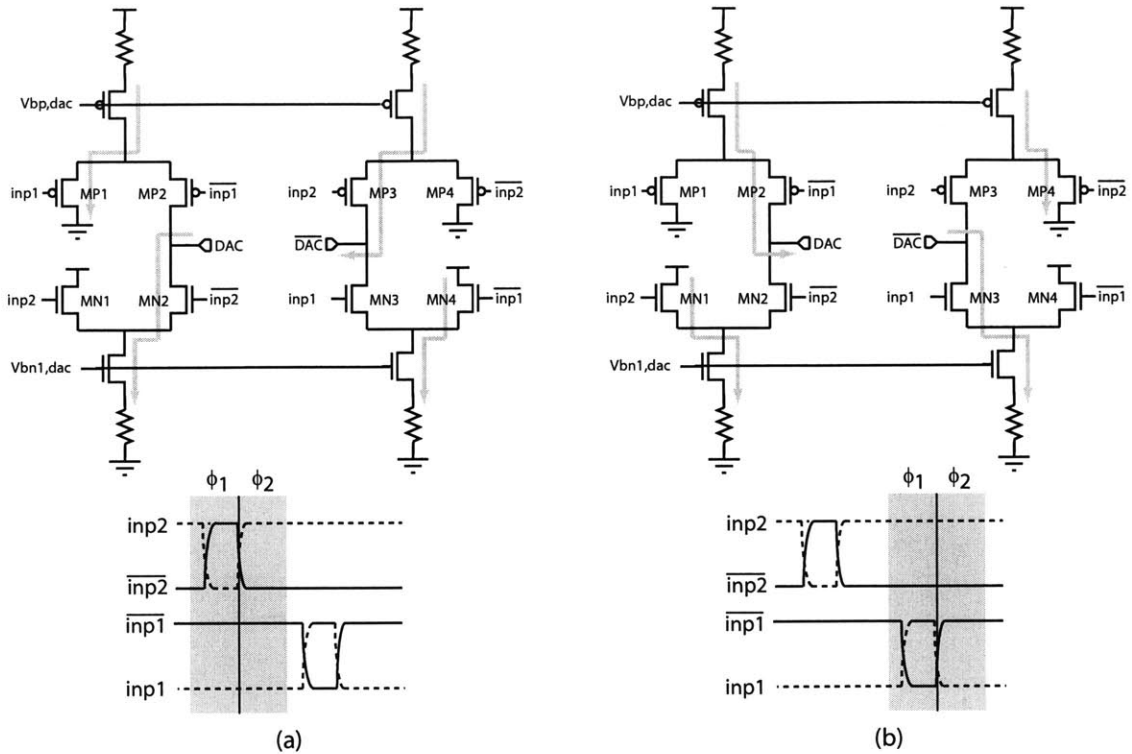


Figure 5-8: Illustration of the DAC unit element steering current when (a)  $inp2$  switches low and  $\overline{inp2}$  switches high, and (b)  $inp1$  switches high and  $\overline{inp1}$  switches low.

ensured that the switching devices would remain in saturation, maintaining a high output impedance.

To allow flexibility, the DAC gain was made configurable by being able to selectively turn on or off unit elements. For the first DAC, 9 parallel unit elements were created, each generating  $200\ \mu A$  of differential current. The second DAC had an identical structure and comprised 4 unit elements, with each generating  $20\ \mu A$  of differential current. The amount of DAC current was calculated using the equations described in [3] and estimates of the total loop-delay and clock duty cycle (see Appendix for MATLAB script). Assuming that all DACs are turned on, the power dissipation is approximately 3.4 mW.

This particular structure was chosen so that DAC current would either be steered into the DAC output node (into the integrating capacitors), or to supply or ground. See Figure 5-8(a). Observe that for the input signal levels indicated in the *first half*

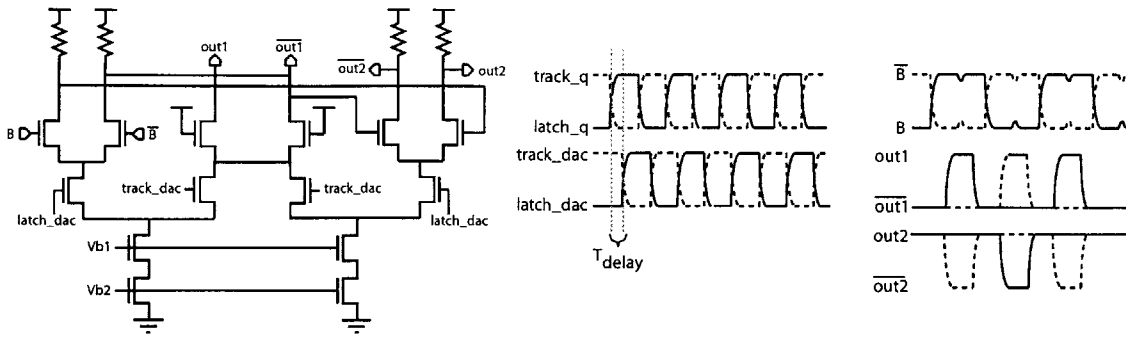


Figure 5-9: Schematic of the four-phase DAC driver.

of the shaded time region ( $\phi_1$ ), MN2 and MP3 are on, steering current to the output nodes, and MN4 and MP1 are on, steering current to supply and ground, respectively. Then, in the *second half* of the shaded time region ( $\phi_2$ ), MN2 and MP3 switch off, and MN1 and MP4 switch on, steering current to supply and ground, respectively. Therefore, the RZ DAC characteristic is achieved. Note that the combination of the two half-phases comprise one sample period of the  $\Sigma\Delta$ .

Figure 5-8(b) demonstrates the complementary situation, in which MN3 and MP2 switch on, steering current to the output for the first half of the shaded time region ( $\phi_1$ ), and then switches off during the second half of the time period ( $\phi_2$ ). Observe that DAC current is either switched into the output nodes, or into supply and ground. No current cancellation ever occurs, effectively eliminating noise contributions to the output nodes during half of the  $\Sigma\Delta$  sample period.

### 5.3.3 4-Phase DAC Driver

The DAC driver shown in Figure 5-9 was also designed using an SCL topology in order to minimize delay. The DAC driver generates the waveforms shown to the right of the schematic in Figure 5-9, and essentially behaves as a fully differential RS latch. As previously mentioned, the four phases are needed to switch the DAC currents in a particular manner such that no current cancellation occurs at the DAC output nodes. The structure was also designed with a 2 GHz bandwidth in mind, consumed less than 1.1 mW, and generates 1 V differential output signals.

Note that the four-phase DAC outputs swing from  $V_{DD}$  to an intermediate volt-

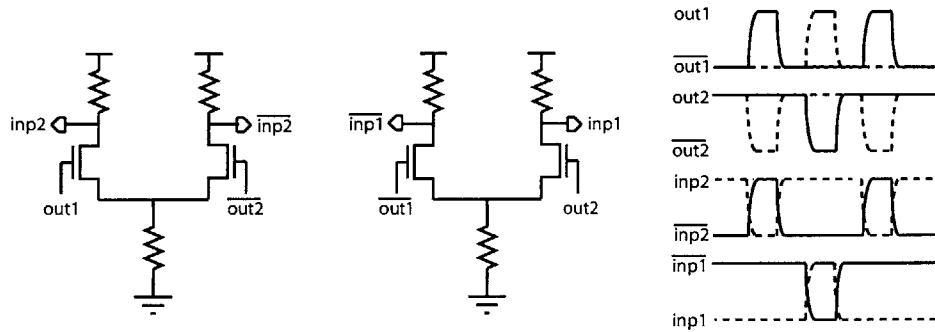


Figure 5-10: Schematic of the DAC level shifting buffers.

age of approximately 1.3 V. The DAC unit elements require a similar voltage swing, but centered at  $\frac{V_{DD}}{2}$  in order that the switching devices remain in saturation. Consequently, level shifting circuitry is needed. The level shifting buffers are shown in Figure 5-10, and are nothing more than resistively loaded differential pairs. However, unlike those used in the SCL logic, the differential pairs used here do not completely switch off. Static current is constantly flowing through either device, as set by the source resistor.

Since the bias of the differential pair is not well determined by the source resistor, a current source may seem more desirable. However, using an active current source to supply the desired current densities ( $\approx 3mA$ ) necessitates very large devices that capacitively load the source node. In contrast, use of a poly resistor at the source of the differential pair minimizes this loading, ensuring fast switching transients. Simulations over process and temperature corners demonstrated the circuit could still drive the DAC switching devices completely.

As previously mentioned, the level shifting buffers consume approximately 3 mA each for a total power dissipation of approximately 11 mW. Such large power dissipation was necessary because the DAC unit elements as well as the wiring parasitics extracted from layout presented a large load to the buffers. Furthermore, the choice of RZ pulses approximately 600 picoseconds wide required that the buffers have a large bandwidth to minimize ISI issues.

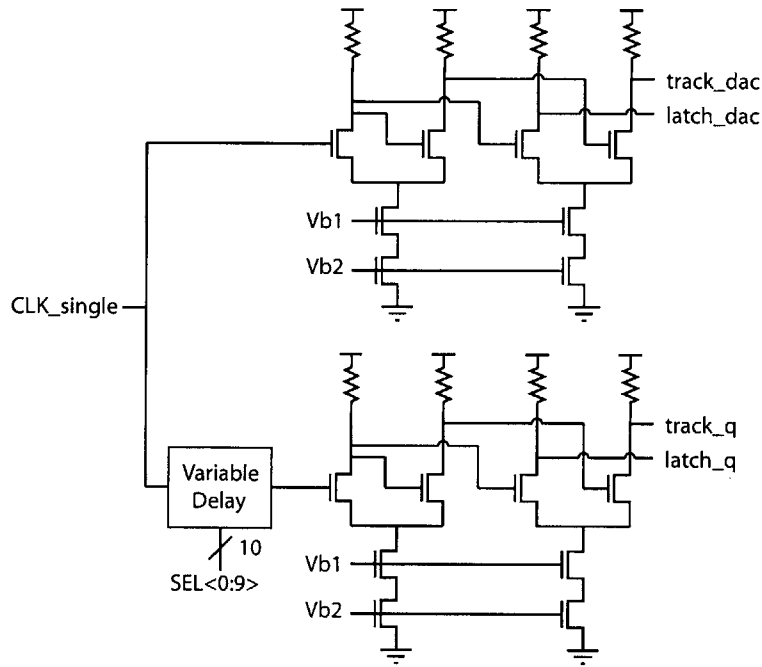


Figure 5-11: Schematic of the differential clock generator.

### 5.3.4 Clock Buffers

Since the on-chip and off-chip clock generating circuits all create full-swing single-ended signals, a differential clock generator is needed in order to drive the differential SCL logic. Figure 5-11 shows the circuitry used to generate the differential quantizer and DAC clock signals. The differential circuit was designed using the script described in [5] to generate 1V swings at each output node, and to have a bandwidth of 2 GHz at the slow process corner. Simulations indicated that skew between the differential outputs was minimal (on the order of 10 picoseconds or less), and did not have any visible effect on the quantizer or DAC driver circuitry.

Note that the variable delay element delays the quantizer clock by more than three-quarters of a sample period such that the quantizer clock precedes the DAC clock by approximately 250 picoseconds. This configuration initially may seem overly complicated since the DAC clock could be delayed relative to the quantizer clock using a much shorter delay line than that used to delay the quantizer clock. However, recall from the previous chapter that any DAC clock jitter contributes directly to the input of the CT  $\Sigma\Delta$  while quantizer clock jitter gets shaped by the  $\Sigma\Delta$  feedback

loop. Consequently, it is desirable to induce more quantizer clock jitter in exchange for minimal DAC jitter, which is what occurs in the scheme shown in Figure 5-11.

## 5.4 Summary

A second-order CT  $\Sigma\Delta$  architecture was presented, and the reasonable tradeoff between quantization noise-shaping and implementation complexity for this topology described. Single-bit quantizer and DACs were chosen for simplicity, and RZ DAC waveforms were adopted to compensate for ISI and loop delay. A four-phase DAC driver was described, and the benefits it affords in terms of reduced thermal noise explained. A clock-buffering scheme that delayed the quantizer clock relative to the DAC clock was also illustrated, and the reduced jitter that the structure contributes emphasized. Finally, the design of the two analog integrators was presented, and the linearity constraints on each stage were discussed.



# Chapter 6

## Results

This chapter presents system level simulation results generated by CppSim, a custom C++ behavioral simulator [13], and then processed by MATLAB. The behavioral model used for simulation includes calculated noise sources for each of the key blocks, including the first and second integrators, and the first and second DACs. Effects of feedback loop delay and ISI were included as well, as were the effects of accumulative jitter from an electronic VCO and white clock jitter from the optical electrical clock. Details of the chip layout, which is still under construction, is included as well.

### 6.1 Behavioral Simulation

An FFT of the digitized output from the  $\Sigma\Delta$  is shown in Figure 6-1 and Figure 6-2, and the key results are summarized in Table 6.1. Here, a 1.041 MHz unmodulated sinusoid was used as an input to the optical sampling network to test for the performance of just the data converter. As expected, the signal-to-noise ratio (SNR) of the converter is dominated by the shot noise of the diodes, which is more than ten times larger than the thermal noise contribution of the first DAC (see Table 6.2). The shot noise limit accounts for the “filled in” noise notch at DC. Clock jitter fell below the thermal noise floor, and thus did not degrade SNR. This was confirmed by behavioral simulations that used an ideal and jittery clock, and also coincides with the findings by the authors in [2].

Technology	0.18 $\mu\text{m}$ CMOS
Chip Area	3 $\text{mm}^2$
Input Signal	1.041 MHz Sine Wave
Signal Bandwidth	2.082 MHz (Nyquist Frequency)
Sampling Rate	780 MHz
OSR	390
SINAD	76.5 dB
ENOB	12.4
SFDR	55.2 dB (Relative to 3 <sup>rd</sup> Harmonic)
Estimated Power Dissipation	45 mW

Table 6.1: Calculated results based on behavioral simulations using noise sources shown in Table 6.2, and layout

Shot Noise ( $i_{n,sh}^2/\Delta f$ )	$3.2 \times 10^{-21} \text{A}^2/\text{Hz}$
DAC Thermal Noise ( $i_{n,DAC}^2/\Delta f$ )	$3.0 \times 10^{-22} \text{A}^2/\text{Hz}$
Total Input Referred Noise ( $v_{n,in}^2/\Delta f$ )	$1.3 \times 10^{-16} \text{V}^2/\text{Hz}$

Table 6.2: Simulated noise sources in optical input stage.

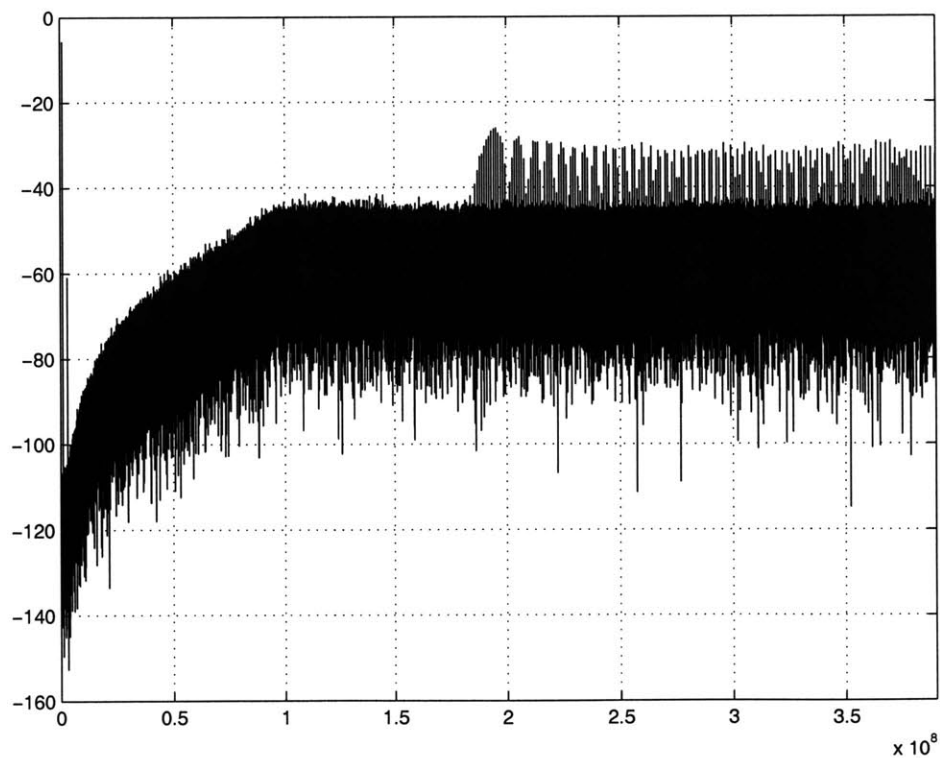


Figure 6-1: FFT of the  $\Sigma\Delta$  digital output with the noise sources described in Table 6.2 included.

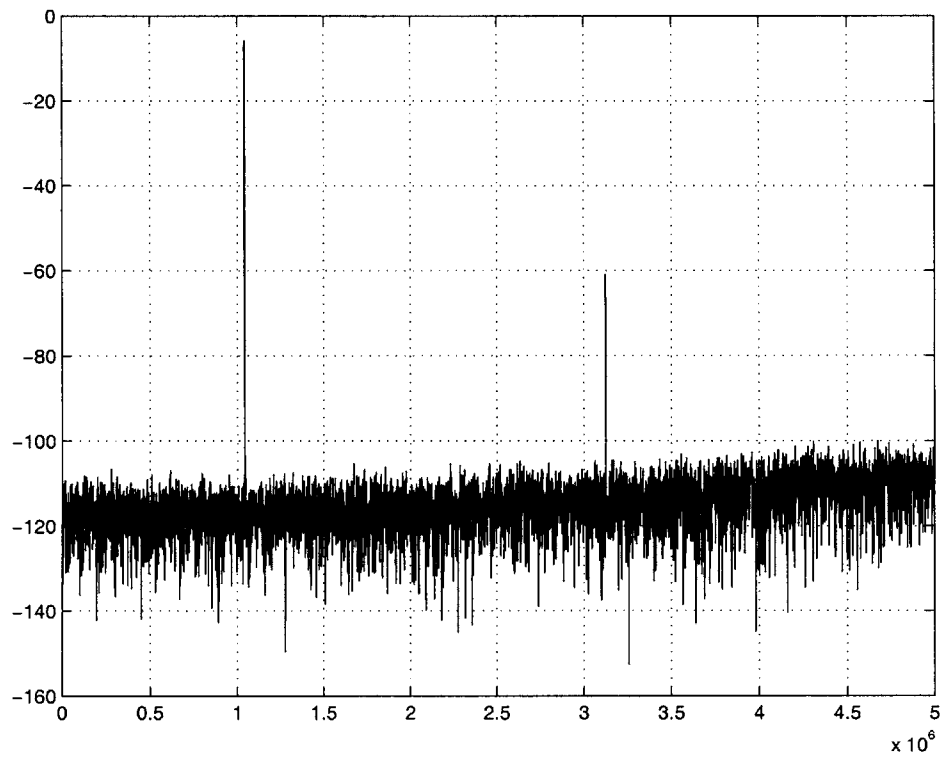


Figure 6-2: A zoom-in of the FFT of the  $\Sigma\Delta$  digital output with the noise sources described in Table 6.2 included.

To improve SNR beyond 76 dB, there must be three modifications to the topology. First, the effective transconductance,  $G_{M,eff}$ , of the optical input stage must be increased. This can be done easily by merely increasing the average optical power of the laser, which will then translate to a larger bias current for the photodiodes. Assuming shot noise dominates, increasing  $I_{BIAS}$  by a factor of  $N$  will decrease the input referred noise by approximately the same factor. This is in contrast to a standard electronic integrator in which increasing  $I_{BIAS}$  would result in a decreased input referred noise by only a factor of  $\sqrt{N}$  due to the MOSFET being a square-law device. Secondly, the maximum differential input current to the  $\Sigma\Delta$  must also increase by the same factor that the transconductance increases. That is, even if  $G_{M,eff}$  of the optical input stage increases, the SNR cannot improve if the voltage signal decreases to maintain the same differential input current. Thirdly, the maximum DAC current must also increase proportionately to the increase in the maximum differential input current. Without this final modification, an increased input current will overload the  $\Sigma\Delta$  modulator.

Unfortunately, increasing the DAC current effectively increases the number of DAC unit elements, which in turn increases the load that the DAC driving buffers must drive. Consequently, for the same sampling rate, more power must be dissipated to ensure that the buffers can drive all DACs and wiring capacitances. Again, the DAC buffers must dissipate a significant amount of power because RZ DAC pulses are used. While switching to an NRZ scheme would alleviate the bandwidth requirements for the DAC buffers, the  $\Sigma\Delta$  would then be susceptible to DAC ISI (signal dependent jitter) and dynamic range (DR) degradation and potential instability due to the clock-to-Q delay, which can be as large as forty percent of the sample period.

The spurious-free dynamic range (SFDR) of approximately -55 dB was limited by the nonlinearity of the optical input stage. An improvement in the SFDR was obtained by simply doubling the optical power, and halving the applied voltage to the interferometer, achieving an SFDR of -68 dB (see Figure 6-3). Nonlinearity of the second integrator made negligible differences when included in the behavioral model. This result matches well with intuition since any nonlinearities or offsets in the second

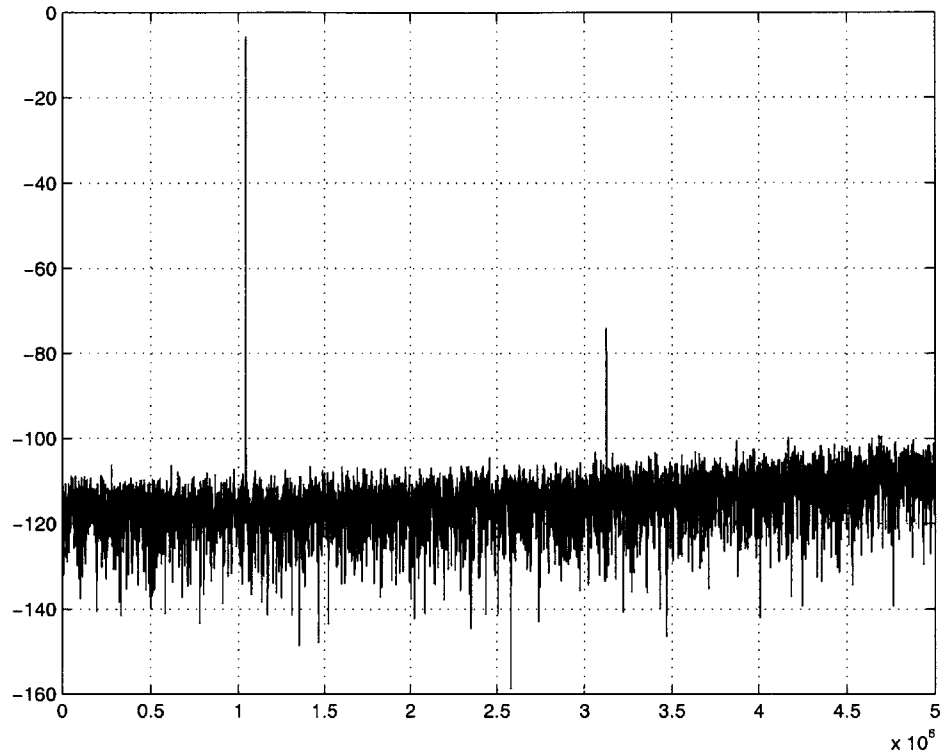


Figure 6-3: FFT of the  $\Sigma\Delta$  digital output, but with twice the average optical power and half the applied voltage to the interferometer.

integrator are effectively shaped by the  $\Sigma\Delta$  modulator when input referred.

## 6.2 Chip Layout

A preliminary die photograph of the unfinished chip is shown in Figure 6-4. As can be seen by the abundance of empty space, the chip is severely pad limited, which is largely due to the inclusion of the decimation filter on chip. The entire die is approximately 3 millimeters by 3 millimeters on a side, and will be fabricated in National Semiconductor's 0.18  $\mu\text{m}$  CMOS process.

## 6.3 Summary

An optical-electrical continuous-time  $\Sigma\Delta$  ADC with 12.4 ENOB and 55 dB SFDR in a 2 MHz signal bandwidth has been demonstrated. The converter is clocked at

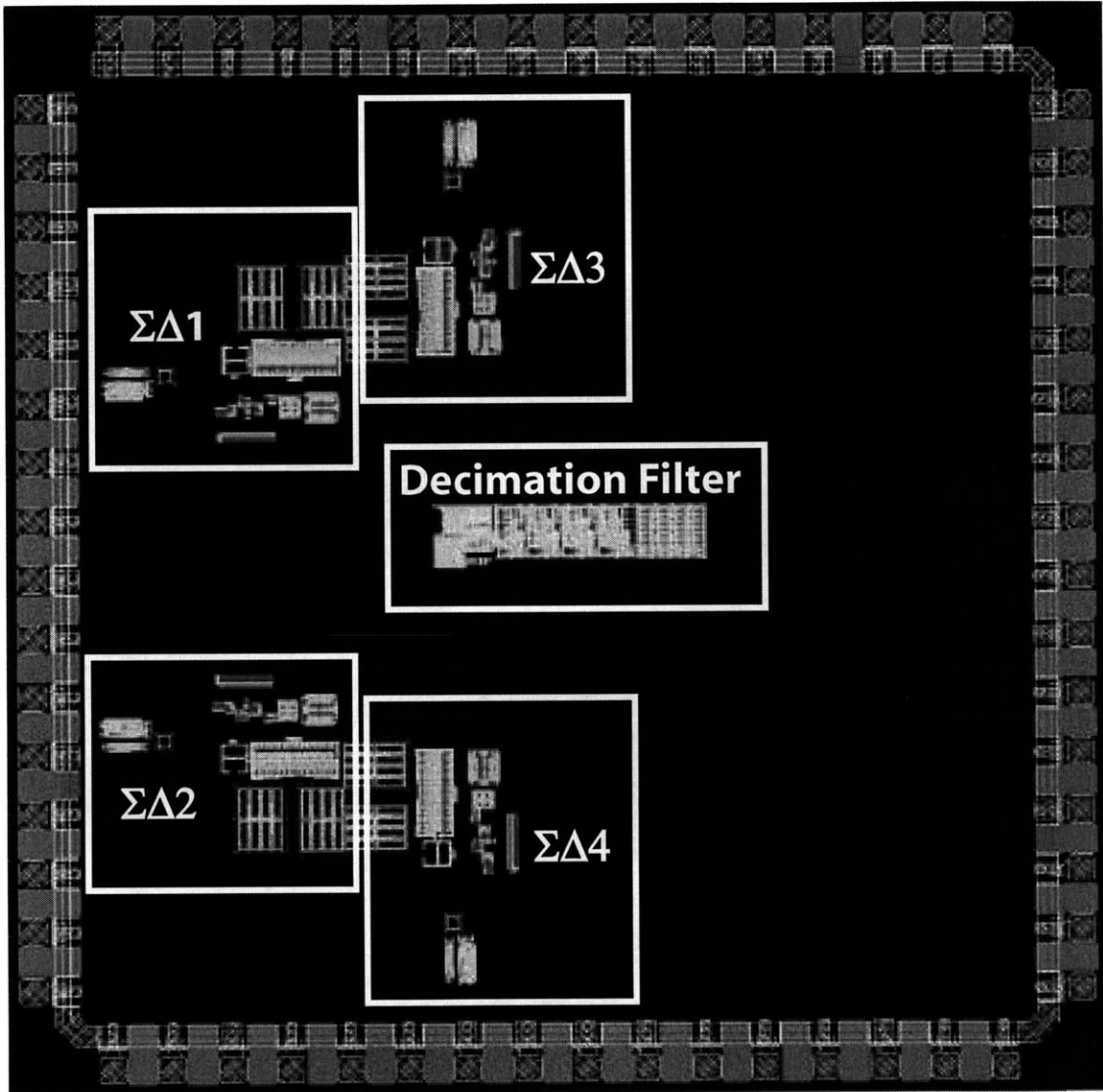


Figure 6-4: Preliminary die photo.

780 MHz for an effective OSR of 390, and consumes 45 mW of power. The design is verified through FFTs of digitized output data generated by behavioral simulations. The resolution versus power dissipation tradeoff is described, as is the ISI immunity versus DAC bandwidth tradeoff. Finally, a preliminary layout of the entire chip is shown.





# Chapter 7

## Conclusion

This thesis described the design and implementation of a novel optical-electrical architecture for use in down-conversion and analog-to-digital conversion. An optical-electrical approach to these traditionally electronic applications enabled precise sampling of a high-frequency RF signal, and low-jitter clocking for high-speed data conversion. This was achieved by using two key optical components: the low-jitter optical pulses from a mode-locked-laser, and a high-bandwidth interferometer.

Typical electronic direct down-conversion receivers rely on a high-frequency VCO with low-phase noise to mix down an RF signal to baseband. The architecture proposed in this thesis used the mode-locked-laser pulses and the interferometer to perform precise sub-sampling of a high-frequency RF signal. The aliasing caused by sub-sampling resulted in an image of the RF signal at baseband, which could then be extracted by low-pass filtering. The extremely low-jitter of the mode-locked-laser ensured that the extracted baseband replica would then have minimal distortion.

Continuous-time  $\Sigma\Delta$  modulation was introduced as a means to transition seamlessly between the optical and electrical domains. Unlike prior work that used the sample-and-hold network from the input stage of a pipeline or flash ADC to compartmentalize optically generated charge, this thesis proposed directly connecting the photodiode to the capacitor for continuous charge integration. This approach eliminated all non-idealities and errors caused by MOS switches and reduced the architecture's sensitivity to photodiode recombination transients. Continuous-time  $\Sigma\Delta$

modulation was then used as a mechanism to recharge the integrating capacitor and described as an elegant means to digitize the narrowband optical information.

Optical-electrical circuits were then leveraged in the design of the continuous-time  $\Sigma\Delta$  ADC. A brief comparative study of DT and CT  $\Sigma\Delta$  modulators was provided, and a survey of various compensation techniques for CT  $\Sigma\Delta$  modulator non-idealities was conducted. The gain-bandwidth and clock-jitter of the electronics was highlighted as the major limitation in all electronic compensation methods. Two new optical-electrical circuits that can potentially exceed these fundamental electronic limits were proposed. Both circuits leveraged the low-jitter mode-locked-laser pulses and the near-ideal current source characteristics of the photodiode.

Finally, the electronic circuits used in the remainder of the  $\Sigma\Delta$  were analyzed, and the results from behavioral and circuit simulations presented. A preliminary layout of the chip implemented in 0.18  $\mu\text{m}$  CMOS was also shown.

# Appendix A

## Appendix

### A.1 Photodiode Current Equations

The photodiode current equation is described as [4]:

$$J_{ph} = \frac{-q(1 - R_{par})\alpha P_o}{Ah\nu}(L_p + L_n)e^{-\alpha x} \quad (\text{A.1})$$

where  $q$  is Coulomb's charge [ $C$ ],  $A$  is the photodiode junction area [ $m^2$ ],  $R_{par}$  is the parasitic recombination and reflection coefficient,  $P_o$  is the incident optical power [ $W$ ],  $L_p$  and  $L_n$  are the diffusion lengths of holes and electrons respectively [ $m$ ],  $\alpha$  is the absorption coefficient of the material [ $m^{-1}$ ], and  $x$  is the distance from the junction [ $m$ ]. The values of all of these coefficients are dependent on the starting materials and processing steps in fabricating the photodiode. Consequently, for discrete photodiodes (as are used for this input stage), the manufacturer simplifies current calculations by specifying the responsivity [ $A/W$ ] of the photodiode:

$$R = \frac{J}{P_o A} = \frac{-q(1 - R_{par})}{h\nu}(L_p + L_n)e^{-\alpha x} \quad (\text{A.2})$$

Therefore, the generated photocurrent can be calculated very easily:

$$I_{ph} = RP_o \quad (\text{A.3})$$



# Appendix B

## MATLAB Code

### B.1 DAC Current Calculation Script

```
pulsewidth = 0.5; %RZ DAC pulses that are Ts/2 wide
alpha = 0.4; % 500ps delay for DAC to be clocked
beta = alpha+pulsewidth;
y01 = beta-alpha;
y12 = 0.5*(beta*(2-beta)-alpha*(2-alpha));
y02 = 0.5*((beta*beta)-(alpha*alpha));
exp1a = strcat('(k2a*',num2str(y12),'+k1a*',num2str(y01),'') = -2');
exp2a = strcat('(k2a*',num2str(y02),'-k1a*',num2str(y01),'') = 1');
[k1a,k2a]=solve(exp1a,exp2a)
I1 = 780e-6; %differential input current
C1 = 8e-12; %first integrator capacitor value
av1 = I1/C1;
fs = 780e6; %Sigma-Delta sampling rate
gm2 = 50e-6; %Effective transconductance of second integrator
I2 = gm2/(fs/av1); %Second DAC current
I DAC1 = k2a*I1
I DAC2 = k1a*I2
```



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