

**A MEMS-Based, High-Resolution  
Electric-Field Meter**

by

John Sawa Shafran

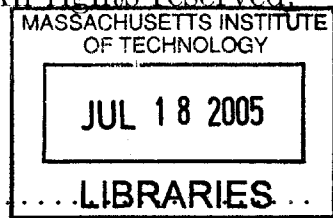
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**BARKER**



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## Abstract

In MEMS-based inertial sensors, such as accelerometers and gyroscopes, known electrical waveforms are applied to a modulating capacitive element to determine an unknown deflection. However, the inverse of this scheme can also be exploited — the capacitive element can be deterministically modulated to measure an electrostatic variable. This thesis presents the design, analysis, and evaluation of such a sensor — a MEMS-based, high-resolution electrostatic field-meter (ESF) — using the Analog Devices iMEMS process.

High-resolution sensing is achieved by optimizing the interface electronics for low-noise operation and applying feedback techniques to enhance the range-of-motion of the MEMS capacitive structure. The entire system consists of three components: the MEMS capacitive structure and two circuit subsystems — the sense block and the drive loop. The MEMS structure acts as a transducer to generate a dynamic current that is proportional to the magnitude and polarity of the electric field incident on the sensor. The drive loop is a closed feedback loop that modulates the MEMS capacitive structure at its resonant frequency to maximize its displacement and the magnitude of the dynamic current. The sense block ultimately converts the dynamic current into a dc voltage that is proportional to the magnitude and polarity of the incident electric field. The critical, front-end component of the sense block, a transimpedance amplifier, is implemented with a low-noise operational amplifier for optimum sensing resolution.

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# Chapter 1

## Introduction

### 1.1 Overview

The emergence of MEMS as a viable technology for implementing microscopic sensors has revolutionized the field of metrology. The integration of MEMS sensors and interface circuitry has yielded low-cost, high-performance instruments with excellent reliability. Inertial sensors, such as accelerometers and gyroscopes, are currently being utilized for demanding automotive applications, such as crash detection, rollover detection, and dynamic vehicle control.

Nonetheless, the application of MEMS technology is not limited to inertial measurements. Specifically, the Analog Devices iMEMS multi-layer process is suited for any measurement that can take advantage of modulating capacitors. In inertial sensing, deterministic electrical waveforms are applied to the MEMS capacitive element to determine an unknown deflection [1]. On the other hand, the inverse of this measurement method can also be exploited. The MEMS element can be deterministically modulated to measure an unknown electrical variable, such as electric field strength. This thesis presents the implementation of such a sensor, a MEMS-based, high-resolution electrostatic field-meter (ESF), using the Analog Devices iMEMS process.

## 1.2 Applications

Electric fields are associated with a variety of natural events. Aside from obvious electrical phenomena, such as lightning storms, evidence indicates that electric fields are present in dust devils, which are miniature, dust-filled tornadoes that frequently occur in dry regions of the world [2]. Also, certain species of fish in Africa and South America communicate by the generation and detection of electric fields [3].

A number of technologies also depend on the measurement of electric fields. New automobiles feature electric field imaging that determines the size of the occupant in a given seat. In the event of a crash, whether or not a specific airbag is deployed is based on this information [3]. The electric power systems and semiconductor manufacturing industries also rely on the monitoring of electric fields [2].

Presently available integrated circuit-based electric field sensors, such as the Motorola MC33794, do not actually measure an incident electric field. Rather, the MC33794 generates an electric field between two user-supplied electrodes and senses perturbations in the field due to changes in the medium [4]. The demand clearly exists for a true ESF that measures an external electric field by means of an integrated electrode.

## 1.3 Principle of Operation

### 1.3.1 Electrostatic Field-meter (ESF)

The output signal of a number of integrated sensors, such as the Analog Devices ADXL190 accelerometer and ADXRS150 gyroscope, is a voltage proportional to the magnitude and polarity of the measured variable [5], [6]. One method of realizing an integrated ESF with such an output signal is described in [7]. A conceptual illustration of the input stage of the ESF is shown in Figure 1-1.

The measurement of the electric field strength can be made by cutting the electric field lines between the target surface and an on-chip sense-plate conductor — this

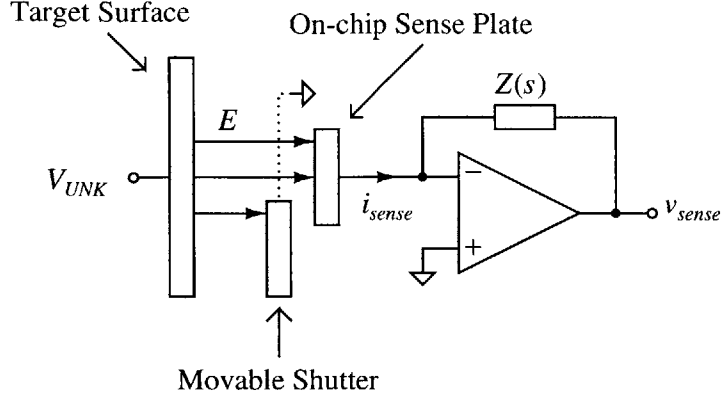


Figure 1-1: Conceptual illustration of the ESF input stage.

method is referred to as the field-mill principle [8]. Together, the target surface and the sense plate form a parallel-plate capacitor structure, denoted as the sense capacitor, or  $C_{sense}$ . Assume that an electric field  $E$  is present between the target surface and the sense plate, which each have an effective area  $A$ , determined by the amount of overlapping area between the two plates. Further assume that the target surface has a total surface charge  $+q$ , and that the sense plate has a total surface charge  $-q$ . The application of Gauss' Law to this system gives

$$E = \frac{q}{\epsilon_o A}, \quad (1.1)$$

where  $\epsilon_o$  is the permittivity of free space and is equal to  $8.85 \times 10^{-12}$  F/m. Ignoring fringing field effects at the edges of the plates, the voltage between the two plates is given by

$$V = V_{UNK} - V_{PLATE} = - \int_C E \cdot dl = \frac{qd}{\epsilon_o A} = Ed, \quad (1.2)$$

where  $V_{UNK}$  is the ground-referenced potential of the target surface,  $V_{PLATE}$  is the ground-referenced potential of the sense plate, and  $d$  is the distance of the gap between the target surface and the sense plate. Since the sense plate is held at ground potential, (1.2) reduces to

$$V = V_{UNK} = \frac{qd}{\epsilon_o A} = Ed. \quad (1.3)$$

Thus,  $V_{UNK}$  is proportional to the magnitude of electric field between the two plates. The value of the capacitance  $C_{sense}$  follows from (1.3) as

$$C_{sense} = \frac{q}{V} = \frac{q}{Ed} = \frac{q}{d} \frac{\epsilon_o A}{q} = \frac{\epsilon_o A}{d}. \quad (1.4)$$

A third conductor, the shutter, is held at the same potential as the sense plate and is swept laterally across the sense plate. The motion of the shutter serves to modulate the effective area of the sense capacitance relative to the target surface. Since  $C_{sense}$  is proportional to the effective area, the shutter motion creates a time-varying  $C_{sense}$  that results in a dynamic current given by

$$i_{sense} = C_{sense} \frac{dV}{dt} + V \frac{dC_{sense}}{dt}. \quad (1.5)$$

For an electrostatic field,  $E$  is constant and, thus,

$$\frac{dV}{dt} = \frac{d(Ed)}{dt} = d \frac{dE}{dt} + E \frac{dd}{dt} = 0 + 0 = 0. \quad (1.6)$$

Therefore, (1.5) reduces to

$$i_{sense} = V \frac{dC_{sense}}{dt}. \quad (1.7)$$

By the result previously given in (1.3), the expression for  $i_{sense}$  further reduces to

$$i_{sense} = V \frac{dC_{sense}}{dt} = V_{UNK} \frac{dC_{sense}}{dt} = Ed \frac{dC_{sense}}{dt}. \quad (1.8)$$

Thus, the dynamic current  $i_{sense}$  is proportional to the electric field between the target surface and the sense plate. The output of the transimpedance amplifier is a voltage  $v_{sense}$  given by

$$v_{sense} = i_{sense} Z(s) = V_{UNK} \frac{dC_{sense}}{dt} Z(s) = Ed \frac{dC_{sense}}{dt} Z(s). \quad (1.9)$$

As desired,  $v_{sense}$  is proportional to  $i_{sense}$ , and, thus, to the strength of the incident electric field.



### 1.3.2 Electrostatic Voltmeter (ESV)

A natural extension of the ESF is the non-contact electrostatic voltmeter (ESV). The output voltage  $v_{sense}$  of the transimpedance amplifier in Figure 1-1 is already proportional to  $V_{UNK}$ , as given by (1.9).

However, in some applications, such as the measurement of the potential on a photocopier imaging drum, true voltmeter operation of the ESV is desired. That is, the output of the ESV should be a voltage equal to  $V_{UNK}$  (that could subsequently be measured with a standard laboratory voltmeter) or a digital representation of  $V_{UNK}$ . One method of theoretically obtaining the latter output is shown in Figure 1-2.

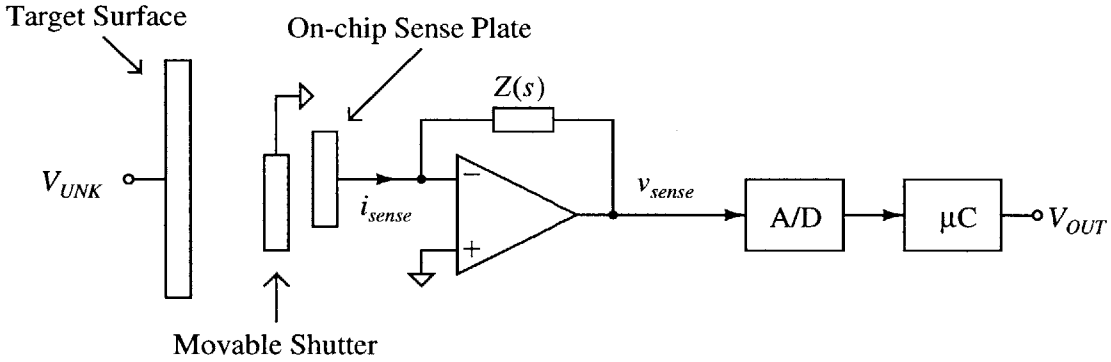


Figure 1-2: Non-contact ESV configured for a digital output. The analog-to-digital converter converts  $v_{sense}$  to digital form, and the microcontroller computes  $V_{UNK}$ .

Rearranging (1.9) gives

$$V_{UNK} = \frac{v_{sense}}{\frac{dC_{sense}}{dt} Z(s)}. \quad (1.10)$$

The voltage  $v_{sense}$  can be converted to digital form, and the microcontroller can compute  $V_{UNK}$  by dividing  $v_{sense}$  by  $(dC_{sense}/dt) Z(s)$ . Although theoretically sound, this method inherently assumes that  $dC_{sense}/dt$  is precisely known. Unfortunately, the MEMS field-mill structure suffers from sensitivity to environmental fluctuations. Recalling the expression for  $C_{sense}$  given in (1.4), examples of such fluctuations include gap variations between the target surface and the on-chip sense plate, and variations in the absolute shutter motion due to process and temperature variations.



of this thesis will be on implementing and testing a high-resolution ESF.

## 1.4 Previous Work

The feasibility of such an integrated ESF was proven in the graduate thesis work of Patrick Riehl [7]. Riehl designed, fabricated, and tested a proof-of-concept ESF with the Analog Devices iMEMS process — the process that will be utilized in this thesis.

Numerous features of the iMEMS process allow for the design and fabrication of a high-performance ESF. In reference to Figure 1-4, the iMEMS process provides direct connection between the interface circuit and the key MEMS structures. The

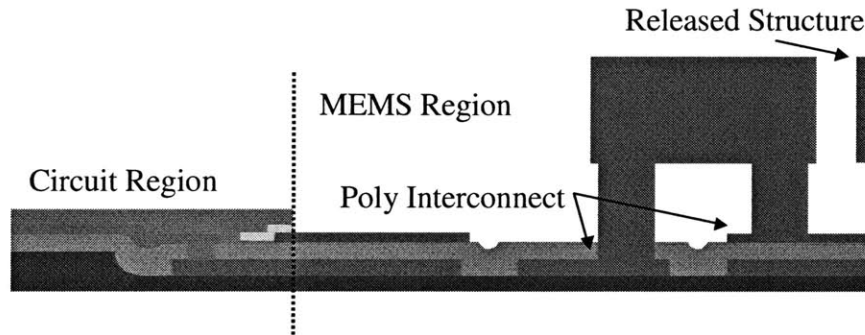


Figure 1-4: Cross-section of the iMEMS process. In the case of the ESF, the released structure is the movable shutter.

direct connection reduces parasitic capacitance, which improves the signal-to-noise ratio (SNR) of the device. Co-integration of the MEMS and the circuitry provides high reliability. The bottom two polysilicon layers beneath the sensor provide suitable conducting paths for the interconnects and the sense plate. The top polysilicon layer is free to move and serves as the mechanical shutter. A view of the composite system architecture is illustrated in Figure 1-5.

The proof-of-concept ESF designed by Riehl accurately measured electric field strength over a range of  $\pm 333$  V/mm, with the target surface spaced  $600\ \mu\text{m}$  above the on-chip sense plate transducer. Another key metric of an ESF is its input-referred noise, which is intimately tied to the SNR at the output of the device and ultimately

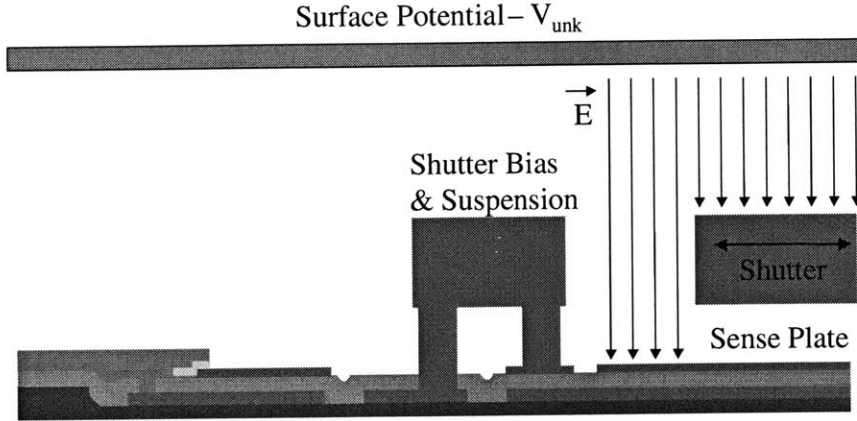


Figure 1-5: Composite MEMS transducer architecture with the iMEMS process.

determines the minimum detectable electric field. The input-referred noise of the Riehl ESF was calculated to be  $700 \text{ V/m}/\sqrt{\text{Hz}}$ .

## 1.5 Research Objective

The objective of this thesis is to greatly improve on the input electric field range and input-referred noise metrics of the Riehl ESF. This objective will be achieved by optimizing the interface electronics for low-noise operation and applying feedback techniques to enhance the range-of-motion of the MEMS shutter. The entire system will consist of three components: the MEMS capacitive structure and two circuit subsystems, the sense block and the drive loop. A block diagram-level schematic of the entire ESF is shown in Figure 1-6. The MEMS structure and the analog front-end circuitry will be fabricated together on an integrated circuit using the iMEMS process. For ease of debugging and testing, all other circuitry will be off-chip on a printed circuit board (PCB).

### 1.5.1 Sense Block

As shown in Figure 1-6, a transimpedance amplifier converts  $i_{sense}$  to a proportional voltage that is conditioned by off-chip circuitry. For optimal input-referred noise, the transimpedance amplifier will be implemented with a low-noise op amp. The off-chip

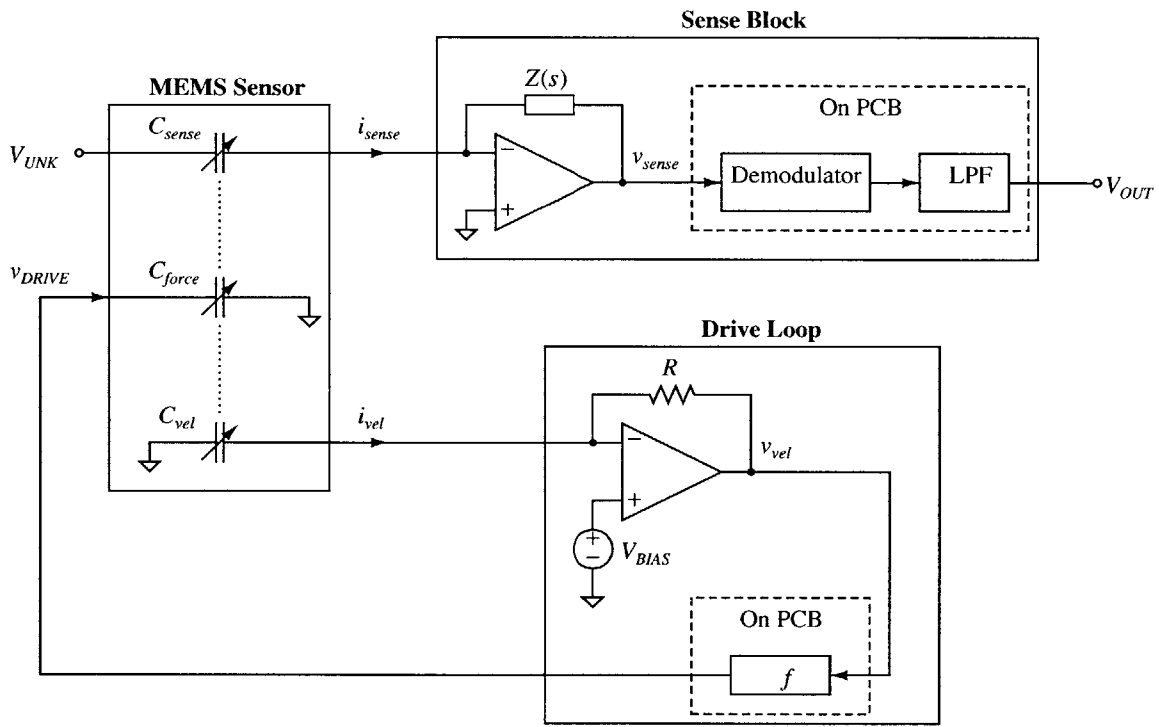


Figure 1-6: System level schematic of the ESF. The arrows through the three MEMS capacitors indicate that they are dynamic capacitors. The dotted lines between the capacitors indicate that they are mechanically coupled.

circuitry will consist of a demodulator and a low-pass filter that serves a dual purpose — to filter out the high-frequency components of the demodulated signal and to limit the noise bandwidth of the system. The transimpedance amplifier and the associated off-chip circuitry are collectively referred to as the sense block. Ultimately, the output of the sense block is a dc voltage that is proportional to the magnitude and polarity of the electric field between the target surface and the on-chip sense plate.

### 1.5.2 Drive Loop

In addition, it is desirable to drive the MEMS capacitive structure at its resonant frequency for maximum shutter motion and, accordingly, optimum system resolution [9], [10]. A closed feedback loop, referred to as the drive loop, is utilized to accomplish this task. The drive loop consists of another two sets of MEMS capacitances — the force drive capacitance  $C_{force}$  and the velocity sense capacitance  $C_{vel}$ . Both  $C_{force}$  and  $C_{vel}$  have one stationary plate and one dynamic plate, which is mechanically coupled to the shutter of  $C_{sense}$ .

A time-varying voltage  $v_{DRIVE}$  applied to the plates of  $C_{force}$  creates an electrostatic force that moves the dynamic plate of  $C_{force}$  and, thus, the shutter. A dynamic current  $i_{vel}$  is generated which is proportional to the shutter velocity. A transresistance amplifier converts  $i_{vel}$  to a proportional voltage  $v_{vel}$  which serves as the input to the drive loop feedback stage, denoted as  $f$ . The entire drive loop employs negative feedback to ensure that the voltage drive applied to the plates of  $C_{force}$  is at the resonant frequency of the shutter. Resonant excitation is enabled, resulting in maximum shutter displacement and, thus, maximum SNR at the system output node  $V_{OUT}$ .

### 1.5.3 Performance Specifications

A set of target specifications for the high-resolution ESF is given in Table 1.1. These specifications are based in part on proof-of-concept specifications for an ESV. Given a proposed nominal gap distance of 0.5 mm, all voltage specifications were converted to corresponding electric field values. Also included in Table 1.1 are the results from

the Riehl ESF where applicable.

Parameters	Target Specifications	Results of Riehl ESF
Input-Referred Noise	$200 \text{ V/m}/\sqrt{\text{Hz}}$	$700 \text{ V/m}/\sqrt{\text{Hz}}$
Input Electric Field Range	$\pm 500 \text{ V/mm}$	$\pm 333 \text{ V/mm}$
Nominal Gap Distance	0.5 mm	0.6 mm
Supply Voltages	$\pm 15 \text{ V}$	+ 20 V
Temperature Range	$- 40^\circ\text{C}$ to $+ 85^\circ\text{C}$	-

Table 1.1: Target specifications for the proposed ESF.

## 1.6 Thesis Outline

Chapter 2 covers the mechanical structure of the MEMS sensor. The sense, force, and velocity capacitances are discussed in detail, and their relationships with the surrounding circuitry are explored. The effects of non-idealities, including parasitic capacitances, are investigated. The chapter concludes with a frequency-domain analysis of the MEMS sensor as a mass-spring-damper system. The high- $Q$  nature of the sensor and its effect on the shutter displacement are covered.

Chapter 3 discusses the design of a low-noise operational amplifier. Such an amplifier is absolutely necessary for accurate sensing of the incident electric field. The noise models for BJTs and MOSFETs are presented, and techniques for reducing the input-referred noise of the amplifier are explored. The effect of the amplifier offset voltage is covered, and a method of nulling the offset voltage is presented. Simulations of the amplifier indicate that all noise and frequency-domain specifications are met.

Chapter 4 covers the design of the drive loop. The drive loop ensures that the force drive voltages oscillate at the resonant frequency of the MEMS sensor. The circuitry for one possible implementation of such a self-resonant loop is presented. Describing functions are utilized to evaluate the stability of the nonlinear feedback loop. A behavioral simulation of the drive loop shows agreement with predicted results.

Chapter 5 discusses the design of the sense block. The sense block performs the actual measurement of the incident electric field. The dynamic currents generated by the sense capacitance  $C_{sense}$  are converted into a dc output voltage that is proportional to the incident electric field. The input-referred noise and input electric field range specifications are considered foremost in the design of the sense block. A behavioral simulation of the sense block shows agreement with predicted results.

Chapter 6 covers the evaluation of the entire ESF system. The MEMS structure, along with all essential electronics, are contained on an integrated circuit. All auxiliary electronics are off-chip on a PCB for ease of debugging. The results of an experimental evaluation of the ESF are also presented. The collected data indicate that the ESF meets the input-referred electric field noise and input electric field range specifications from Section 1.5.3, and also improves on the reported parameters of the Riehl ESF.

Chapter 7 summarizes the design efforts and theoretical and experimental results of this thesis. It concludes with a discussion of future work and design improvements.

## 1.7 Notation

The notation for voltages, currents, and other physical quantities used throughout this thesis is as follows:

- Small-signal quantities are expressed with a lowercase variable and subscript, such as  $v_{test}$  and  $i_{test}$ .
- Large-signal quantities are expressed with an uppercase variable and subscript, such as  $V_{TEST}$  and  $I_{TEST}$ .
- Total quantities are expressed with a lowercase variable and uppercase subscript, such as  $v_{TEST} = V_{TEST} + v_{test}$  and  $i_{TEST} = I_{TEST} + i_{test}$ .
- Laplace transforms are expressed with an uppercase variable and lowercase subscript, and are followed by  $(s)$  to denote that they are a function of  $s$ . Examples include  $V_{test}(s)$  and  $I_{test}(s)$ .



# Chapter 2

## MEMS Capacitive Sensor

### 2.1 Overview

Through modulation of the shutter position, the MEMS capacitive sensor produces a dynamic current that is proportional to the magnitude and polarity of the incident electric field. The following sections describe the structure and operation of the sensor, including the force drive and velocity sensing capacitances. A frequency-domain analysis of the sensor as a mass-spring-damper system is also presented.

The entire MEMS capacitive structure is implemented in a differential configuration to minimize any errors due to clock feedthrough, which will be discussed in Section 2.5.4.

### 2.2 Sense Capacitance

The sense capacitance, along with the moving shutter, perform the actual transduction of the electric field into a dynamic current. A diagram of the differential sensor can be found in Figure 2-1.

The on-chip sense plate actually consists of two plates, the *sense+* plate and the *sense-* plate, which are both connected to virtual ground as shown in Figure 2-1. Let  $C_{sense+}$  and  $C_{sense-}$  be the effective capacitances between the target surface and the *sense+* plate and the *sense-* plate, respectively. Assume that the displacement

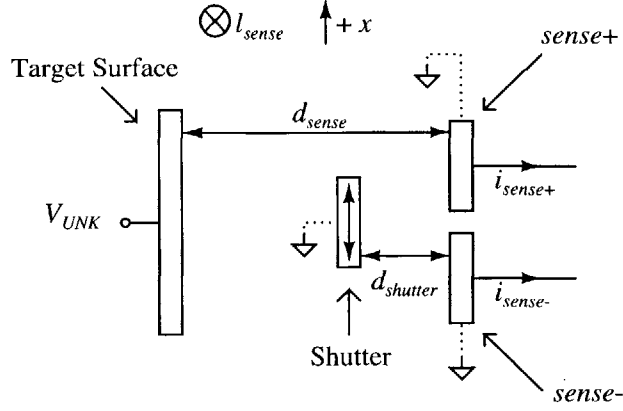


Figure 2-1: Diagram of sense capacitance structure. The dimension  $l_{sense}$  is represented by the depth of the plates into the paper. Note that  $+\hat{x}$  points in the upward direction.

of the movable shutter, which is held at ground potential, is given by

$$x(t) = x_o + x_m \sin(\omega_{res}t), \quad (2.1)$$

where  $x_o$  is the reference position halfway between the  $sense+$  and  $sense-$  plates,  $x_m$  is the maximum amplitude of the displacement in the  $\pm\hat{x}$  direction, and  $\omega_{res}$  is the resonant angular frequency of the MEMS structure. The drive loop ensures that the shutter will vibrate at  $\omega_{res}$ , as will be explained in Chapter 4. The oscillation of the shutter in the  $\pm\hat{x}$  direction modulates the areas of overlap between the target surface and the  $sense+$  and  $sense-$  plates. Since capacitance is proportional to area of overlap, the oscillation of the shutter also effectively modulates the sense capacitances  $C_{sense+}$  and  $C_{sense-}$ .

A mathematical description of this capacitance modulation is as follows. In reference to (2.1),  $C_{sense+}$  and  $C_{sense-}$  can be defined as

$$C_{sense+} = \frac{\epsilon_o l_{sense}}{d_{sense}} x_o + \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \sin(\omega_{res}t) \quad (2.2)$$

$$C_{sense-} = \frac{\epsilon_o l_{sense}}{d_{sense}} x_o - \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \sin(\omega_{res}t), \quad (2.3)$$

where  $l_{sense}$  and  $d_{sense}$  are as shown in Figure 2-1. The difference in sign for the second

term in the  $C_{sense+}$  and  $C_{sense-}$  expressions results from the fact that the shutter inherently modulates the capacitances exactly  $180^\circ$  out of phase. For instance, as the shutter reaches its peak displacement  $x_m$  in the  $-\hat{x}$  direction, the overlapping area between the target surface and the  $sense+$  plate is at a minimum, while, at the same time, the  $sense-$  plate is exposed to the target surface at its fullest extent.

Incidentally,  $d_{shutter}$  represents the distance between the shutter and the  $sense+$  and  $sense-$  plates.

From (1.8), the dynamic currents produced through the sinusoidal movement of the shutter are given by

$$\begin{aligned} i_{sense+} &= V_{UNK} \frac{dC_{sense+}}{dt} = V_{UNK} \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \omega_{res} \cos(\omega_{res} t) \\ &= E d \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \omega_{res} \cos(\omega_{res} t) \end{aligned} \quad (2.4)$$

$$\begin{aligned} i_{sense-} &= V_{UNK} \frac{dC_{sense-}}{dt} = -V_{UNK} \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \omega_{res} \cos(\omega_{res} t) \\ &= -E d \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \omega_{res} \cos(\omega_{res} t). \end{aligned} \quad (2.5)$$

As depicted in Figure 2-2 and discussed in detail in Chapter 5,  $i_{sense+}$  and  $i_{sense-}$  are converted to proportional voltages using transimpedance amplifiers. These voltages are then processed through several stages to create a dc output voltage proportional to the incident electric field. The sense plates are held at virtual ground due to the negative feedback configuration of the op amps. The capacitor symbols for  $C_{sense+}$  and  $C_{sense-}$  have arrows through them to indicate that they are dynamic capacitances. The arrows point in opposite directions to signify that the two capacitances are modulated  $180^\circ$  out of phase.

The signal-to-noise ratio (SNR) at the output of the transimpedance amplifier can be improved by increasing the magnitude of  $i_{sense+}$  and  $i_{sense-}$ . With respect to (2.4) and (2.5), although  $\omega_{res}$  is inherently determined by the composition and structure of the MEMS sensor, one possibility is to increase the effective sense capacitance by

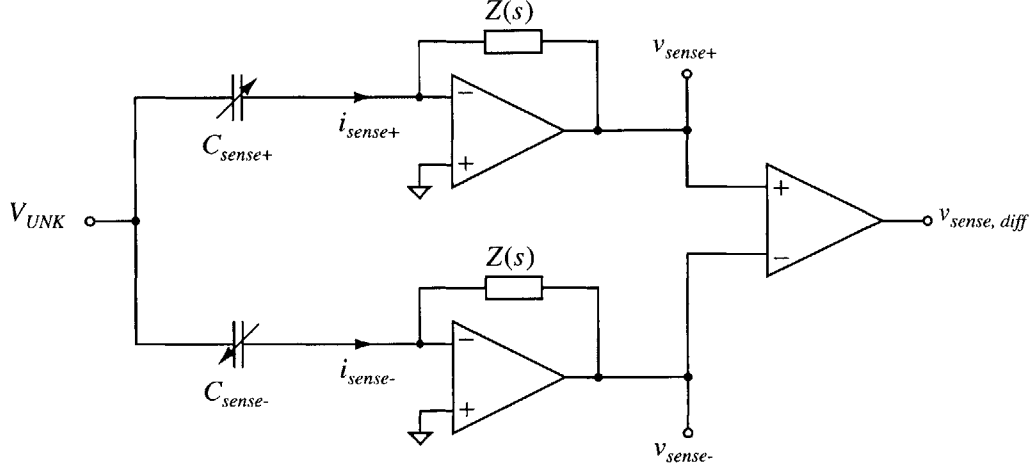


Figure 2-2: Overview of differential-to-single-ended conversion of  $i_{sense+}$  and  $i_{sense-}$  into  $v_{sense,diff}$ .

having multiple shutters and sense plates, as depicted in Figure 2-3. The shutters are mechanically coupled and are all held at the same potential, while the sense plates are electrically connected. Each shutter now experiences a displacement given by (2.1). Since capacitances sum in parallel,  $C_{sense+}$  and  $C_{sense-}$  are now given by

$$C_{sense+} = N_{sense} \frac{\epsilon_o l_{sense}}{d_{sense}} x_o + N_{sense} \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \sin(\omega_{rest} t) \quad (2.6)$$

$$C_{sense-} = N_{sense} \frac{\epsilon_o l_{sense}}{d_{sense}} x_o - N_{sense} \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \sin(\omega_{rest} t), \quad (2.7)$$

where  $N_{sense}$  is the number of sense shutters. Thus, the transduced currents are scaled by  $N_{sense}$  to

$$\begin{aligned} i_{sense+} &= N_{sense} V_{UNK} \frac{dC_{sense+}}{dt} = N_{sense} V_{UNK} \frac{\epsilon_o l_{sense}}{d_{sense}} \omega_{res} \cos(\omega_{rest} t) \\ &= N_{sense} E d \frac{\epsilon_o l_{sense}}{d_{sense}} \omega_{res} \cos(\omega_{rest} t) \end{aligned} \quad (2.8)$$

$$\begin{aligned} i_{sense-} &= N_{sense} V_{UNK} \frac{dC_{sense-}}{dt} = -N_{sense} V_{UNK} \frac{\epsilon_o l_{sense}}{d_{sense}} \omega_{res} \cos(\omega_{rest} t) \\ &= -N_{sense} E d \frac{\epsilon_o l_{sense}}{d_{sense}} \omega_{res} \cos(\omega_{rest} t). \end{aligned} \quad (2.9)$$

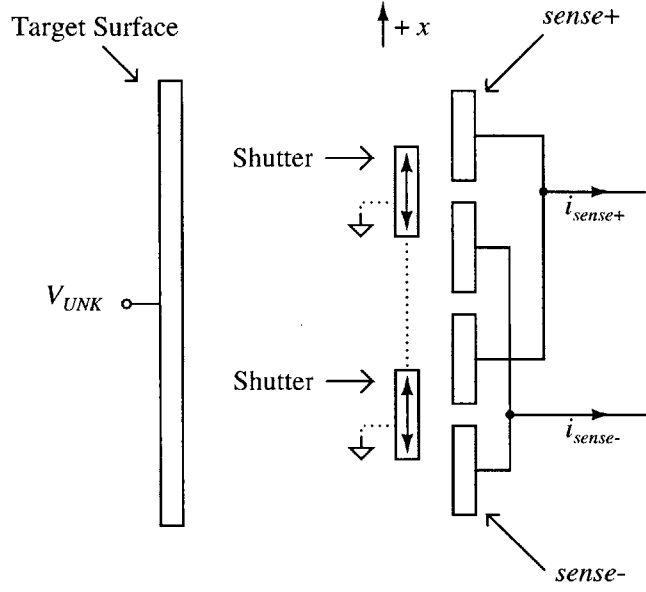


Figure 2-3: Diagram of sense capacitance with multiple shutters. The dotted line between the shutters indicates that they are mechanically coupled.

### 2.3 Force Drive Capacitance

The force capacitance  $C_{force}$  consists of two stationary plates  $force+$  and  $force-$  and one moving plate that is mechanically coupled to the shutter. Assume that  $C_{force+}$  is the effective capacitance between  $force+$  and the moving plate, while  $C_{force-}$  is the effective capacitance between  $force-$  and the moving plate. Like the shutter, the moving force plate is at ground potential. Although the actual structural geometry is more complex, a simplified but physically equivalent representation of the force capacitance is shown in Figure 2-4.

The underlying principle behind the actuation of the moving plate, and thus the shutter, is that a voltage applied to the plates of  $C_{force}$  will induce an electrostatic force that causes the moving plate to vibrate in the  $\pm \hat{x}$  direction. The magnitude of this electrostatic force is given by the derivative of the energy stored in  $C_{force}$  with respect to the  $\hat{x}$  position coordinate. Mathematically, the force is found by

$$\vec{F} = \frac{dE}{dx} = \frac{d}{dx} \left( \frac{1}{2} C_{force+} v_{DRIVE+}^2 + \frac{1}{2} C_{force-} v_{DRIVE-}^2 \right) \hat{x}, \quad (2.10)$$

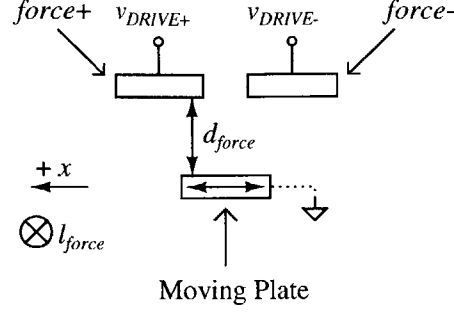


Figure 2-4: Diagram of force capacitance structure. The dimension  $l_{force}$  is represented by the depth of the plates into the paper. Note that  $+\hat{x}$  points in the left direction.

where  $v_{DRIVE+}$  and  $v_{DRIVE-}$  are voltages applied to the  $force+$  and  $force-$  plates, respectively.

The dynamic capacitances  $C_{force+}$  and  $C_{force-}$  can be defined as

$$\begin{aligned}
 C_{force+} &= \frac{\epsilon_o l_{force}}{d_{force}} x_o + \frac{\epsilon_o l_{force}}{d_{force}} x_m \sin(\omega_{rest} t) \\
 &= \frac{\epsilon_o l_{force}}{d_{force}} x_o + \frac{\epsilon_o l_{force}}{d_{force}} x_{dyn}(t)
 \end{aligned} \tag{2.11}$$

$$\begin{aligned}
 C_{force-} &= \frac{\epsilon_o l_{force}}{d_{force}} x_o - \frac{\epsilon_o l_{force}}{d_{force}} x_m \sin(\omega_{rest} t) \\
 &= \frac{\epsilon_o l_{force}}{d_{force}} x_o - \frac{\epsilon_o l_{force}}{d_{force}} x_{dyn}(t),
 \end{aligned} \tag{2.12}$$

where  $l_{force}$  and  $d_{force}$  are as defined in Figure 2-4, and  $x_{dyn}(t) \equiv x_m \sin(\omega_{rest} t)$  represents the dynamic displacement of the moving plate and shutter. Since the first terms in the expressions for  $C_{force+}$  and  $C_{force-}$  are constants, the derivatives of  $C_{force+}$  and  $C_{force-}$  with respect to the  $\hat{x}$  position coordinate are

$$\frac{dC_{force+}}{dx} = + \frac{\epsilon_o l_{force}}{d_{force}} \tag{2.13}$$

$$\frac{dC_{force-}}{dx} = - \frac{\epsilon_o l_{force}}{d_{force}}, \tag{2.14}$$

The expression for the force vector acting on the moving plate, and thus the shutter, is now given by

$$\begin{aligned}\vec{F} &= \frac{1}{2} \frac{\epsilon_o l_{force}}{d_{force}} v_{DRIVE+}^2 \hat{x} - \frac{1}{2} \frac{\epsilon_o l_{force}}{d_{force}} v_{DRIVE-}^2 \hat{x} \\ &= \frac{1}{2} \frac{\epsilon_o l_{force}}{d_{force}} \left( v_{DRIVE+}^2 - v_{DRIVE-}^2 \right) \hat{x}.\end{aligned}\quad (2.15)$$

If  $v_{DRIVE+}$  and  $v_{DRIVE-}$  are square-wave voltages that oscillate between  $V_O$  and 0 V and are 180° out of phase, as shown in Figure 2-5, then the electrostatic force  $\vec{F}$  on the moving plate will be

$$\vec{F} = \pm \frac{1}{2} \frac{\epsilon_o l_{force}}{d_{force}} V_O^2 \hat{x}.\quad (2.16)$$

Note that, as the magnitude of the force is proportional to the square of  $V_O$ , the direction of the force vector is independent of the polarity of  $V_O$ .

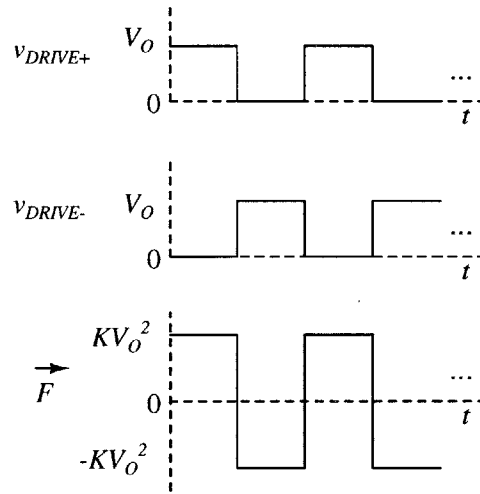


Figure 2-5: Force drive waveforms, where  $K \equiv \epsilon_o l_{force}/2d_{force}$ .

For maximum shutter displacement, the drive loop will maintain the frequency of  $v_{DRIVE+}$  and  $v_{DRIVE-}$  at the resonant frequency of the MEMS structure.

As with the sense capacitance, the force capacitance consists of a number of identical capacitive structures connected in parallel, where all of the moving plates are

mechanically coupled. For  $N_{force}$  such structures, the expressions for the dynamic capacitances become

$$\begin{aligned}
C_{force+} &= 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} x_o + 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} x_m \sin(\omega_{res} t) \\
&= 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} x_o + 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} x_{dyn}(t)
\end{aligned} \tag{2.17}$$

$$\begin{aligned}
C_{force-} &= 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} x_o - 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} x_m \sin(\omega_{res} t) \\
&= 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} x_o - 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} x_{dyn}(t),
\end{aligned} \tag{2.18}$$

while the effective electrostatic force scales to

$$\vec{F} = \pm \frac{1}{2} 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} V_O^2 \hat{x} = \pm N_{force} \frac{\epsilon_o l_{force}}{d_{force}} V_O^2 \hat{x}. \tag{2.19}$$

The capacitances and force are scaled by  $2N_{force}$  rather than  $N_{force}$  due to the comb finger structure of the MEMS sensor, as will be discussed in Section 2.5.

## 2.4 Velocity Sense Capacitance

As will be analyzed in Section 2.6, the force drive and the velocity of the shutter are in phase at resonance. This relationship will be exploited by the drive loop in order to drive the MEMS structure at its resonant frequency for maximum displacement of the shutter. The function of the velocity sense capacitance  $C_{vel}$  is to transduce a dynamic current that is proportional to the shutter velocity.

Similar to the other capacitive structures,  $C_{vel}$  consists of two stationary plates  $vel+$  and  $vel-$ , and a moving plate that is mechanically coupled to the shutter and held at virtual ground. A representation of  $C_{vel}$  is shown in Figure 2-6. Let  $C_{vel+}$  and  $C_{vel-}$  be the effective capacitances between the moving plate and the  $vel+$  and  $vel-$  plates, respectively. Two transresistance amplifiers bias  $vel+$  and  $vel-$  at  $V_{BIAS}$ . The



transduced currents are given by

$$i_{vel+} = -V_{BIAS} \frac{dC_{vel+}}{dt} \quad (2.20)$$

$$i_{vel-} = -V_{BIAS} \frac{dC_{vel-}}{dt}. \quad (2.21)$$

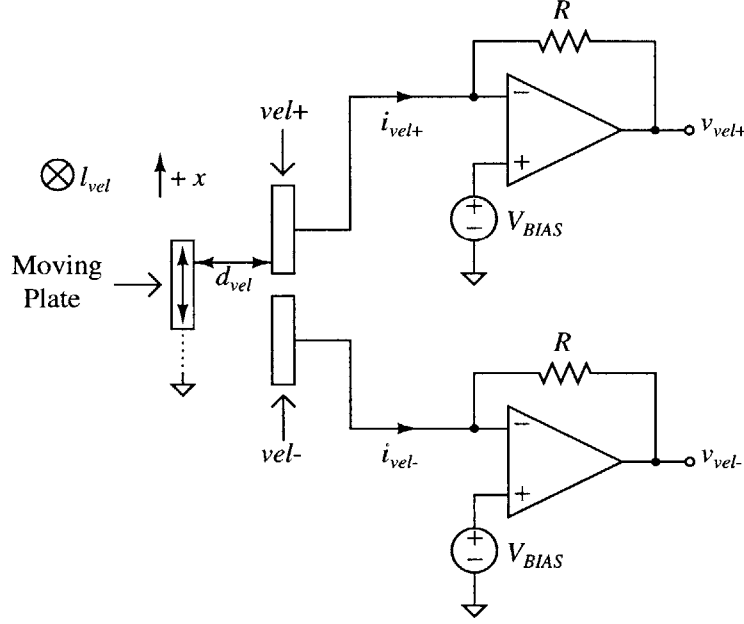


Figure 2-6: Diagram of velocity sense capacitance structure along with transresistance amplifiers. The dimension  $l_{vel}$  is represented by the depth of the plates into the paper. Note that  $+\hat{x}$  points in the upward direction.

As with the sense and force drive capacitances,  $C_{vel+}$  and  $C_{vel-}$  are defined as

$$\begin{aligned} C_{vel+} &= \frac{\epsilon_o l_{vel}}{d_{vel}} x_o + \frac{\epsilon_o l_{vel}}{d_{vel}} x_m \sin(\omega_{rest} t) \\ &= \frac{\epsilon_o l_{vel}}{d_{vel}} x_o + \frac{\epsilon_o l_{vel}}{d_{vel}} x_{dyn}(t) \end{aligned} \quad (2.22)$$

$$\begin{aligned} C_{vel-} &= \frac{\epsilon_o l_{vel}}{d_{vel}} x_o - \frac{\epsilon_o l_{vel}}{d_{vel}} x_m \sin(\omega_{rest} t) \\ &= \frac{\epsilon_o l_{vel}}{d_{vel}} x_o - \frac{\epsilon_o l_{vel}}{d_{vel}} x_{dyn}(t), \end{aligned} \quad (2.23)$$

where  $l_{vel}$  and  $d_{vel}$  are as defined in Figure 2-6. Since the first terms in the expressions for  $C_{vel+}$  and  $C_{vel-}$  are constants, the derivatives of  $C_{vel+}$  and  $C_{vel-}$  with respect to time are

$$\frac{dC_{vel+}}{dt} = + \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} \quad (2.24)$$

$$\frac{dC_{vel-}}{dt} = - \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt}. \quad (2.25)$$

Therefore,  $i_{vel+}$  and  $i_{vel-}$  are given by

$$i_{vel+} = -V_{BIAS} \frac{dC_{vel+}}{dt} = -V_{BIAS} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} \quad (2.26)$$

$$i_{vel-} = -V_{BIAS} \frac{dC_{vel-}}{dt} = +V_{BIAS} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt}. \quad (2.27)$$

As desired, the transduced currents are proportional to the velocity  $dx_{dyn}(t)/dt$  of the shutter. The transresistance amplifiers convert the currents into proportional voltages for interfacing with the other stages of the drive loop.

For  $N_{vel}$  such velocity sense structures, the expressions for the dynamic capacitances become

$$\begin{aligned} C_{vel+} &= 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_o + 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_m \sin(\omega_{rest}t) \\ &= 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_o + 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_{dyn}(t) \end{aligned} \quad (2.28)$$

$$\begin{aligned} C_{vel-} &= 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_o - 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_m \sin(\omega_{rest}t) \\ &= 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_o - 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_{dyn}(t), \end{aligned} \quad (2.29)$$

while the transduced currents scale to

$$i_{vel+} = -2N_{vel} V_{BIAS} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} \quad (2.30)$$

$$i_{vel-} = +2N_{vel} V_{BIAS} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt}. \quad (2.31)$$

The currents and capacitances are scaled by  $2N_{vel}$  rather than  $N_{vel}$  due to the comb finger structure of the MEMS sensor, which will be discussed in Section 2.5.

## 2.5 MEMS Structure

### 2.5.1 Overview

The physical structure of the entire MEMS sensor is shown in Figure 2-7. It was designed by a CAD engineer with the Analog Devices Micromachined Products Division. The sense capacitance  $C_{sense}$  is in the center of the structure. Identified in Figure 2-7 are the  $N_{sense}$  moving shutters, along with the underlying  $sense+$  and  $sense-$  plates, which are physically arranged to provide a differential readout. The force capacitance  $C_{force}$  and velocity capacitance  $C_{vel}$  are implemented with interdigitated finger capacitive structures for maximum capacitance per unit area.

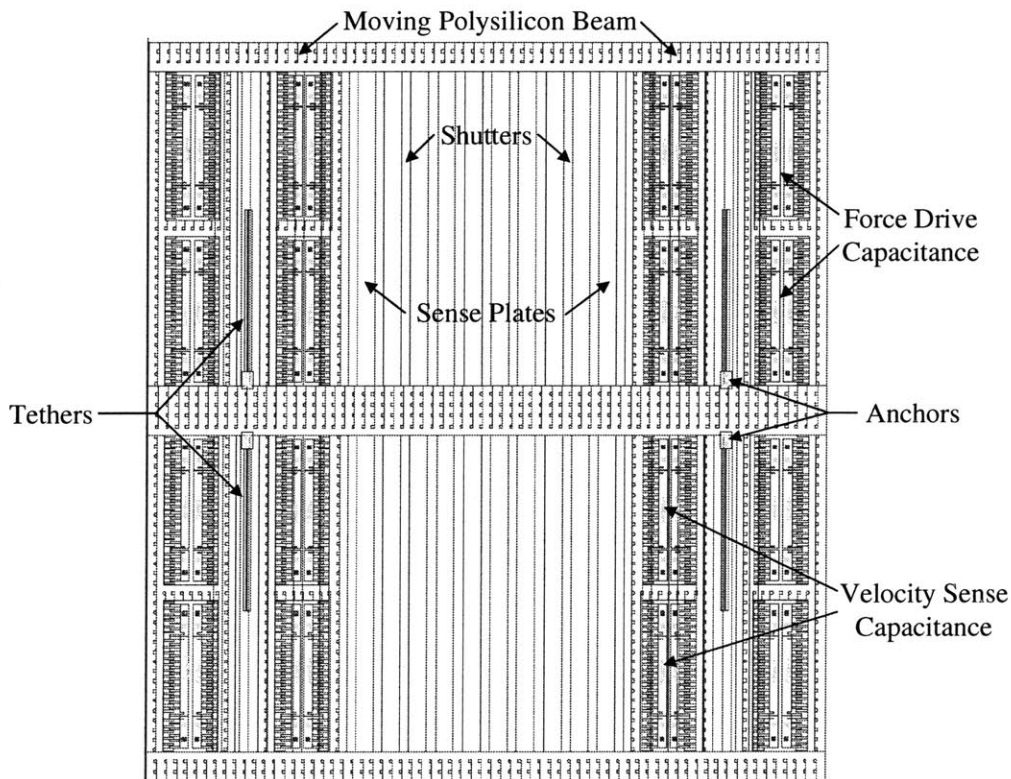


Figure 2-7: Physical structure of the MEMS sensor.

As was stated in Sections 2.3 and 2.4,  $C_{force}$  and  $C_{vel}$  each consist of one moving plate and two stationary plates. The stationary plates, identified as  $force+$ ,  $force-$ ,  $vel+$ , and  $vel-$  in Figure 2-8, are anchored to the underlying substrate. The moving shutters and the moving plates of  $C_{force}$  and  $C_{vel}$ , however, are formed with one large, moving polysilicon mass, or beam, that is held at ground potential. The beam is suspended on folded springs, or tethers, that are anchored to the substrate. The beam, tethers, and anchors are identified in Figure 2-7.

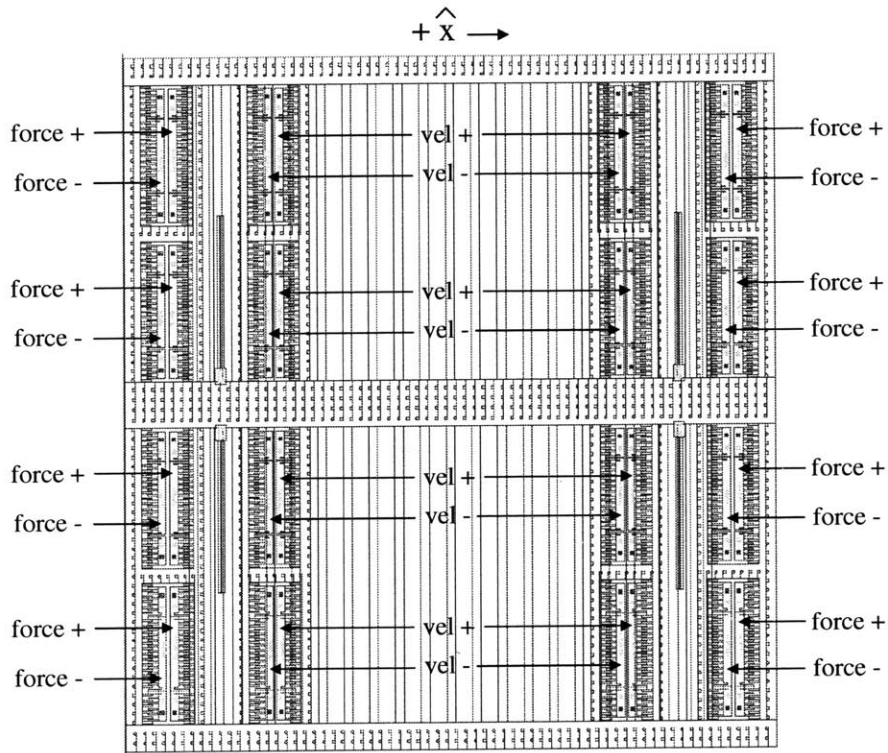


Figure 2-8: Locations of the  $C_{force}$  and  $C_{vel}$  plates on the MEMS structure. Note that the  $force+$  and  $vel+$  are generally on the right side of their structures, since  $+\hat{x}$  points in the righthand direction.

### 2.5.2 Parasitic Capacitances

As with any integrated circuit, the presence of parasitic capacitances can adversely affect system performance. In the case of the ESF covered in this thesis, parasitic capacitances arise from the capacitance of the interconnects between the sensors and

electronics, the dielectric isolation trenches, and other details of the Analog Devices iMEMS process [9], [10], [11], [12]. Two important issues that arise due to these capacitances are the possibility of system instability and errors due to clock feedthrough.

### 2.5.3 Instability

The presence of parasitic capacitances from the  $sense+$  and  $sense-$  electrodes to the underlying substrate can potentially cause stability problems in the transimpedance amplifier configuration shown in Figure 2-2. Since the substrate is small-signal ground, the effective transimpedance amplifier circuit can be represented as in Figure 2-9, where  $C_{p,sense}$  is the parasitic capacitance from  $sense+$  or  $sense-$  to the substrate. Also, the effective velocity sense transresistance circuit is shown in Figure 2-10, where  $C_{p,vel}$  is the parasitic capacitance from the  $vel+$  or  $vel-$  electrodes to the substrate. Compensation techniques for dealing with these capacitances will be covered in Chapters 4 and 5.

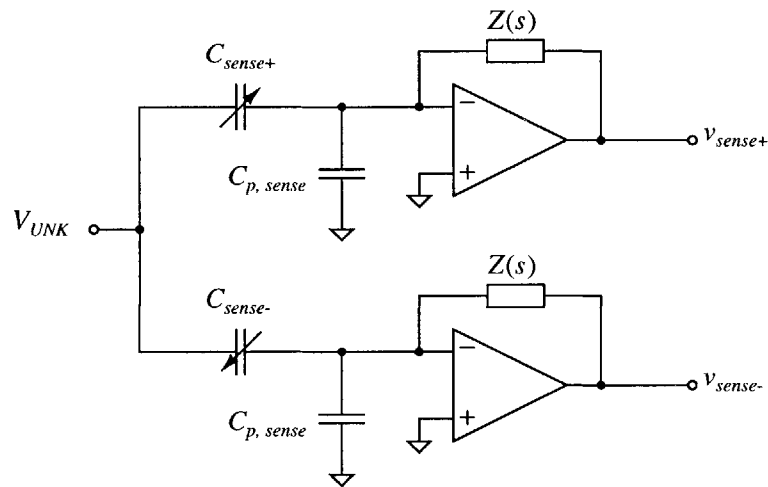


Figure 2-9: Transimpedance amplifiers with the  $C_{p,sense}$  parasitic capacitances due to the MEMS sensor.

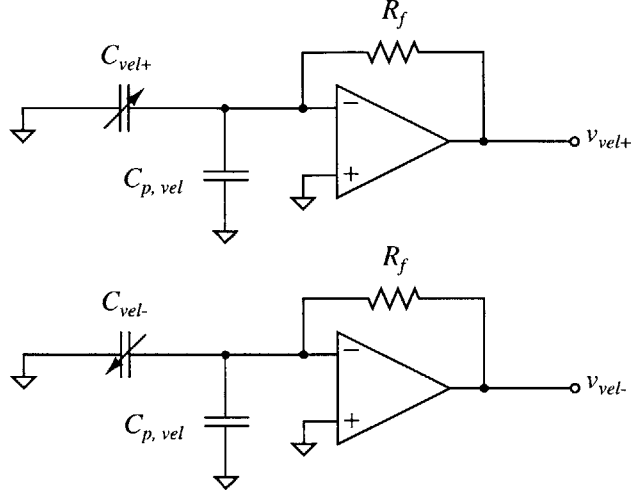


Figure 2-10: Transresistance amplifiers with the  $C_{p,vel}$  parasitic capacitances due to the MEMS sensor.

## 2.5.4 Clock Feedthrough

As discussed in Section 2.3, the electrostatic force acting on the beam is proportional to the square of the force drive voltages  $v_{DRIVE+}$  and  $v_{DRIVE-}$ . Thus, for maximum shutter displacement, the high state of the drive voltages should be set at the power supply rails. However, for larger drive voltages, the probability of charge coupling to the sense plates through parasitic capacitances — known as clock feedthrough — is greater. As shown in Figure 2-11, when the drive voltage transitions from its low state (0 V) to its high state ( $V_O$ ), or vice versa, short pulses of current can parasitically couple through stray structural capacitances onto the high-impedance summing node of the op amp. Although the stray capacitance is an undesired, parasitic capacitance, it is identified as  $C_{stray}$  to differentiate it from  $C_{p,sense}$ , the parasitic capacitance from the sense nodes to the substrate. The charge on  $C_{stray}$ , referred to as  $Q_{stray}$ , and the current through  $C_{stray}$ , identified as  $i_{stray}$ , are plotted in Figure 2-12. The voltage  $v_-$  on the inverting terminal of the op amp, assuming an ideal op amp, is given by

$$v_- = V_O \frac{C_{stray}}{C_{p,sense} + C_{sense} + C_{stray} + C_f} \approx V_O \frac{C_{stray}}{C_{p,sense}} \quad (2.32)$$

where it is assumed that  $C_{p,sense} \gg C_{sense} + C_{stray} + C_f$ . This assumption is valid for the circuitry used in this thesis. Thus, when  $v_{DRIVE}$  is in its high state at  $V_O$ , the resulting accumulation of charge on the high-impedance node acts as an undesirable offset voltage. Incidentally, although its presence poses potential instability issues, one benefit of a large  $C_{p,sense}$  is that it limits the magnitude of the offset voltage, as per (2.32).

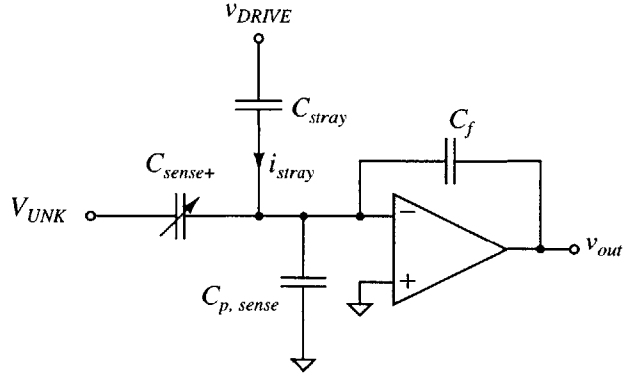


Figure 2-11: Schematic of effective clock feedthrough circuit with  $C_{stray}$ . Short pulses of current can parasitically couple through  $C_{stray}$  onto the high-impedance summing node of the op amp.

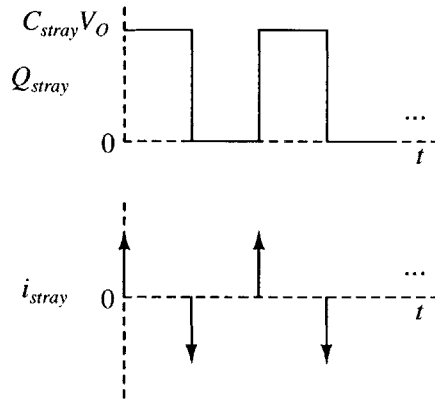


Figure 2-12: Ideal  $Q_{stray}$  and  $i_{stray}$  waveforms. Short pulses of current couple through  $C_{stray}$  whenever the force drive voltages transition from their low state to their high state, or vice versa.

Three steps are taken to reduce the deleterious effects of clock feedthrough on the sensor accuracy. First, as shown in Figure 2-2, a differential scheme is employed to

convert  $i_{sense+}$  and  $i_{sense-}$  to a proportional, single-ended voltage  $v_{sense,diff}$ . Given that stray capacitances affect both the the  $C_{sense+}$  and  $C_{sense-}$  circuit configurations, and assuming similar values for  $C_{stray+}$  and  $C_{stray-}$ , the resulting offsets largely cancel when  $v_{sense+}$  and  $v_{sense-}$  are passed through the differential amplifier.

Second, as shown in Figure 2-8, the  $C_{force}$  capacitances are physically positioned on the outside of the structure to minimize the likelihood of stray capacitances between the force drive electrodes and the sense plates.

Third, as indicated in Figure 2-13, drive voltages of opposite polarity are applied to Sector+ and Sector- of the force electrodes. Assuming that the parasitic capacitances from the Sector+ and Sector- force electrodes to the sense plates are matched, the net charge accumulation on the sense plates should be zero. Note that the direction of the electrostatic force generated by the Sector- force capacitance is not inverted by applying  $-V_O$ , since the force is proportional to the square of the drive voltage. To designate whether  $v_{DRIVE+}$  and  $v_{DRIVE-}$  are applied to the *force+* and *force-* plates of Sector+ or Sector-, new notation is introduced in Table 2.1.

Previous Notation	Sector+/Sector-	Drive Voltage	New Notation
$v_{DRIVE+}$	Sector+	$V_O = +15\text{ V}$	$v_{DRIVE++}$
$v_{DRIVE+}$	Sector-	$-V_O = -15\text{ V}$	$v_{DRIVE+-}$
$v_{DRIVE-}$	Sector+	$V_O = +15\text{ V}$	$v_{DRIVE-+}$
$v_{DRIVE-}$	Sector-	$-V_O = -15\text{ V}$	$v_{DRIVE--}$

Table 2.1: New notation for the force drive voltages. A plus or minus sign is added to  $v_{DRIVE+}$  and  $v_{DRIVE-}$  to designate whether the voltage is applied to the Sector+ or Sector- electrode.

### 2.5.5 Electric Field Termination Factor

The implicit assumption thus far in the determination of the transduced sense currents  $i_{sense+}$  and  $i_{sense-}$  has been that all of the electric field lines incident on the sensor terminate on the sense plates unless they are impeded by the shutter, as shown in Figure 2-14. However, a fraction of electric field lines that should terminate on the



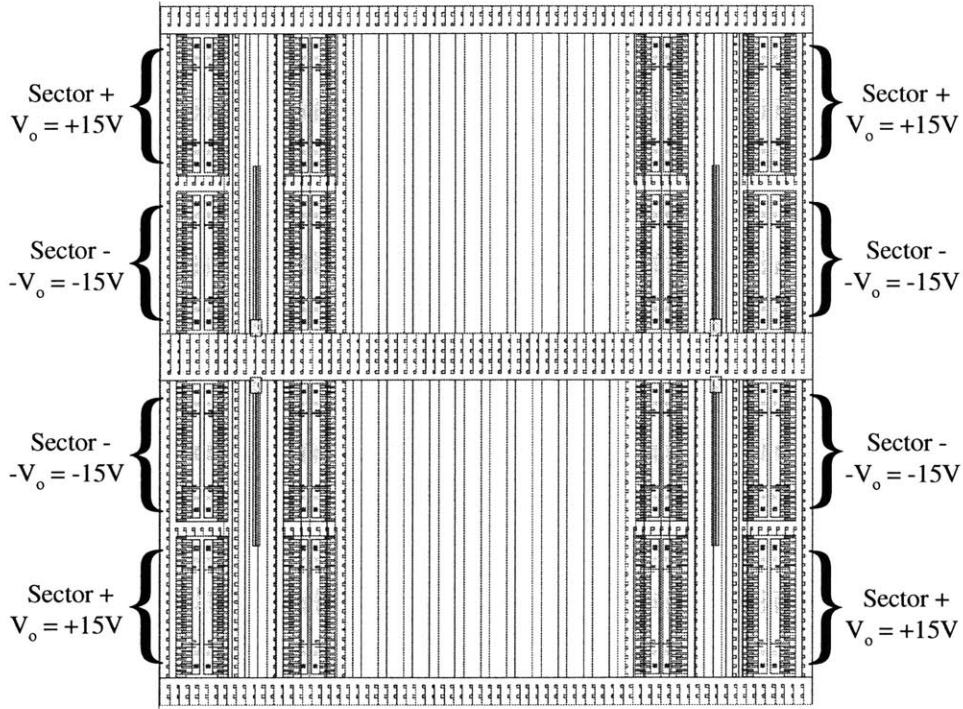


Figure 2-13: Locations of the Sector+ and Sector- force electrodes on the MEMS sensor.

sense plates, given the model in Figure 2-14, actually curve and terminate on the shutter. This scenario is depicted in Figure 2-15.

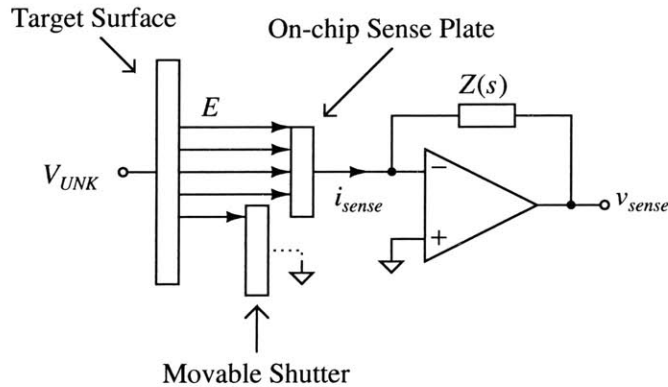


Figure 2-14: Ideal electric field-sensing mechanism, with all field lines terminating on the sense plate.

Let  $\alpha$  represent the fraction of electric field lines that do *not* experience this curvature effect and, thus, terminate on the sense plates. Therefore,  $i_{sense+}$  and

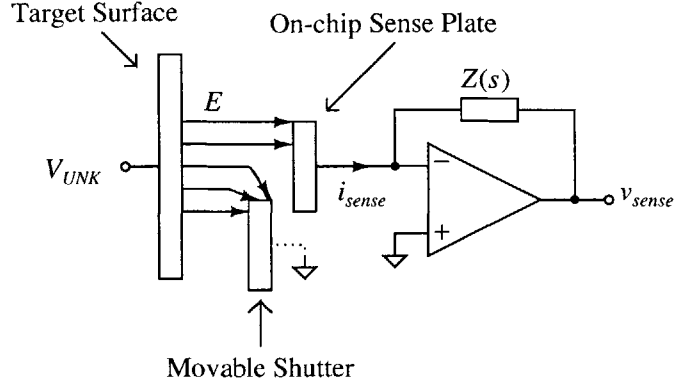


Figure 2-15: Actual electric field-sensing mechanism, with a fraction of the field lines terminating on the shutter.

$i_{sense-}$  are now given by

$$\begin{aligned}
 i_{sense+} &= \alpha N_{sense} V_{UNK} \frac{dC_{sense+}}{dt} \\
 &= \alpha N_{sense} V_{UNK} \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \omega_{res} \cos(\omega_{res} t) \\
 &= \alpha N_{sense} E d \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \omega_{res} \cos(\omega_{res} t) \quad (2.33)
 \end{aligned}$$

$$\begin{aligned}
 i_{sense-} &= \alpha N_{sense} V_{UNK} \frac{dC_{sense-}}{dt} \\
 &= -\alpha N_{sense} V_{UNK} C_{sense,m} \omega_{res} \cos(\omega_{res} t) \\
 &= -\alpha N_{sense} E d C_{sense,m} \omega_{res} \cos(\omega_{res} t). \quad (2.34)
 \end{aligned}$$

A finite element analysis of the MEMS structure found  $\alpha$  to be approximately 0.7 [13]. As dire as it might seem, the fact that a fraction of the field lines experiences this curvature effect does not prohibit the operation of a functional ESF. The desired output of the ESF is a dc voltage proportional to the incident electric field strength. The existence of a non-unity  $\alpha$  simply modifies the overall constant of proportionality between the input electric field and the output voltage.

Nonetheless, the non-unity  $\alpha$  is not entirely benign. It reduces the magnitude of the transduced sense current, which limits the minimum detectable electric field due

to noise considerations.

## 2.5.6 MEMS Sensor Parameters

A list of the actual values for the key sensor parameters is given in Table 2.2. These values assume that the sensor is being driven at its resonant frequency of 15 kHz. The definitions of the Dimensional and Force Parameters were previously defined in this chapter. The definitions and relevance of the Mechanical Parameters given in Table 2.2 will be discussed in Section 2.6, where the resonant frequency is derived using frequency-domain techniques.

The parameters  $C_{sense,m}$ ,  $C_{force,m}$ , and  $C_{vel,m}$  listed in Table 2.2 are defined as

$$C_{sense,m} = N_{sense} \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \quad (2.35)$$

$$C_{force,m} = 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} x_m \quad (2.36)$$

$$C_{vel,m} = 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_m. \quad (2.37)$$

They represent the peak magnitude changes in their respective dynamic capacitances, with all of the  $N$  capacitive structures acting in parallel. These parameters will be utilized in Chapters 4 and 5 for analyses of the drive loop and sense block. The capacitance values listed in Table 2.2 for  $C_{sense,m}$ ,  $C_{force,m}$ , and  $C_{vel,m}$  are somewhat less than what would be ideally expected given the values for  $N$ ,  $l$ ,  $d$ , and  $x_m$ , due to the effects of fringing fields [13].

The actual value of  $C_{p,sense}$  as defined in Section 2.5.3 is 3.7 pF. However, the  $C_{p,sense}$  value of 4.2 pF given in Table 2.2 includes the 0.5 pF contribution from the input capacitance of the op amp shown in Figure 2-9. The  $C_{p,vel}$  value of 1.0 pF given in Table 2.2 was similarly modified. These aggregate values of  $C_{p,sense} = 4.2$  pF and  $C_{p,vel} = 1.0$  pF will be used throughout the remainder of this thesis for notational simplicity.

Lastly, note that the value given for  $|F|$  given in Table 2.2 takes into account

<b>Dimensional Parameters</b>	
Parameter	Value
$x_m$	$3 \mu\text{m}$
$l_{sense}$	$324 \mu\text{m}$
$l_{force}$	$4 \mu\text{m}$
$l_{vel}$	$4 \mu\text{m}$
$d_{sense}$	$500 \mu\text{m}$
$d_{force}$	$1.3 \mu\text{m}$
$d_{vel}$	$1.3 \mu\text{m}$
$N_{sense}$	21
$N_{force}$	424
$N_{vel}$	424
$C_{sense,m}$	0.4 fF
$C_{force,m}$	45 fF
$C_{vel,m}$	45 fF
$C_{p,sense}$	4.2 pF
$C_{p,vel}$	1.0 pF
<b>Force Parameters</b>	
Parameter	Value
$V_O$	15 V
$ F $	$2.6 \mu\text{N}$
<b>Mechanical Parameters</b>	
Parameter	Value
$f_{res}$	$14.6 \text{ kHz} \approx 15 \text{ kHz}$
$m$	$2.5 \times 10^{-9} \text{ kg}$
$b$	$2.4 \times 10^{-6} \text{ N}\cdot\text{s/m}$
$k$	$2.1 \times 10^1 \text{ N/m}$
$\alpha$	0.7

Table 2.2: Dimensional, force, and mechanical parameters for the MEMS sensor.

$N_{force}$ , as per (2.19).

## 2.6 MEMS Frequency-Domain Analysis

The capacitive MEMS sensor can be treated as a mass-spring-damper system for purposes of frequency-domain analysis [12]. First, in the time-domain, the displacement of the moving shutter  $x$  due to an applied electrostatic force is given by

$$F(t) = m \ddot{x} + b \dot{x} + k x, \quad (2.38)$$

where  $m$  is the mass of the beam,  $b$  is the damping coefficient due to the Couette flow of air between the beam and substrate, and  $k$  is the effective spring constant of the tethers. Taking the Laplace Transform of (2.38) results in a frequency-domain representation of the dynamic system:

$$\frac{X}{F}(s) = \frac{1}{ms^2 + bs + k}. \quad (2.39)$$

As previously discussed, it is desirable to drive the MEMS sensor at its resonant frequency. At resonance, the  $ms^2$  and  $k$  terms in (2.39) cancel, or, equivalently,  $ms^2 = -k$ . Substituting in  $j\omega$  for  $s$  and rearranging terms gives the MEMS resonant angular frequency as

$$\omega = \omega_{res} = \sqrt{\frac{k}{m}}, \quad (2.40)$$

or, equivalently, a resonant linear frequency of

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{k}{m}} = 14.6 \text{ kHz} \approx 15 \text{ kHz}, \quad (2.41)$$

as given in Table 2.2.

The quality factor  $Q$  of the sensor is calculated as

$$Q = \frac{m \omega_{res}}{b} = 95 \quad (2.42)$$

[12]. The high- $Q$  nature of the  $X/F(j\omega)$  frequency response, shown in Figure 2-16, provides for the sinusoidal displacement of the shutter despite the square-wave force waveform shown in Figure 2-5. The Fourier Transform of  $x(t)$ ,  $X(j\omega)$ , is given by

$$X(j\omega) \equiv F(j\omega) \cdot \frac{X}{F}(j\omega), \quad (2.43)$$

where  $F(j\omega)$  is the Fourier Transform of the force drive waveform  $F(t)$ . Since  $F(t)$  is a square-wave waveform,  $F(j\omega)$  is a sinc function. Due to its high- $Q$  peak,  $X/F(j\omega)$  acts as a narrow-band, band-pass filter to suppress the frequency content in all frequencies in  $F(j\omega)$  except around  $\omega_{res}$ . Thus,  $X(j\omega)$  can be approximated by impulses in the frequency-domain, which corresponds to sinusoidal motion of the shutter in the time-domain [14].

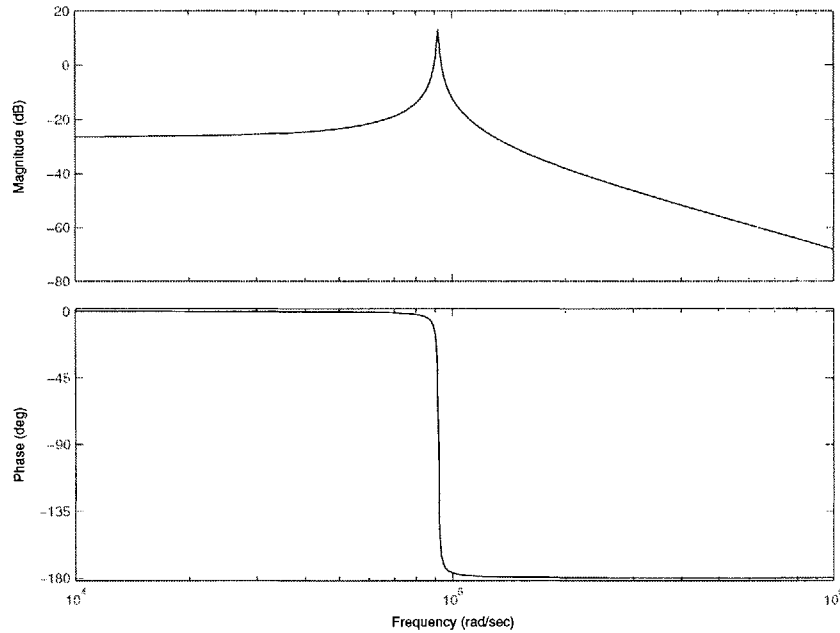


Figure 2-16: Force-to-displacement frequency response of the MEMS sensor, indicating its high- $Q$  nature.

As previously discussed, at resonance, the  $m s^2$  and  $k$  terms in (2.39) cancel,

leaving

$$\frac{X}{F}(j\omega_{res}) = \frac{1}{jb\omega_{res}}. \quad (2.44)$$

Rearranging terms gives

$$F(j\omega_{res}) = j\omega_{res}bX(j\omega_{res}), \quad (2.45)$$

or, in the time-domain,

$$F(t) = b \frac{dx}{dt}, \quad (2.46)$$

where  $dx/dt$  is the velocity of the shutter. Thus, at resonance, and only at resonance, the force drive and shutter velocity are in phase. This fortunate property is exploited to implement the self-resonating drive loop, which will be discussed in detail in Chapter 4.

## 2.7 Summary

The function of the MEMS capacitive sensor is to transduce the incident electric field into a proportional current, which is then converted to a voltage and processed by the sense block. The modulation of the shutter position generates the dynamic current. Auxiliary MEMS capacitances provide for electrostatic force actuation of the shutter and velocity sensing to ensure resonant operation of the sensor.

The actual MEMS structure consists of a moving polysilicon beam suspended above the substrate. Non-idealities associated with the structure include the presence of parasitic capacitances, as well as the curvature of the electric field lines and their resulting termination on the shutter rather than the sense plates. Lastly, a frequency-domain analysis of the force-to-displacement dynamics of the MEMS structure reveals its high- $Q$  nature and the fortunate and useful result that the force drive and shutter velocity are in phase at resonance.





# Chapter 3

## Low-Noise Operational Amplifier

### 3.1 Overview

At the heart of the on-chip circuitry is a low-noise operational amplifier. As will be discussed in Chapter 5, a low-noise op amp is absolutely necessary for implementing the transimpedance amplifier used in the electric field sense circuitry. The noise performance of this op amp ultimately determines the electric field sensing resolution of the ESF. This noise performance is optimized by implementing the op amp in a BiCMOS process, thereby taking full advantage of the distinct noise characteristics of each type of transistor.

### 3.2 Noise Analysis

#### 3.2.1 Noise Fundamentals

The three fundamental inherent noise phenomena present in electronic circuits are thermal, shot, and  $1/f$  noise [15]. Thermal noise is due to the random thermal excitation of charge carriers and is proportional to absolute temperature and the resistance of the conductor. Shot noise is found in all pn junctions and occurs because a current is not composed of a smooth, continuous flow of carriers, but rather, pulses of current due to individual carriers randomly flowing across the junction. Flicker,

or  $1/f$ , noise arises from impurities in a silicon crystalline structure which randomly trap and release charge carriers.

All noise sources are characterized by a certain noise spectral density in the frequency-domain. The noise spectral density is a function of frequency and is a measure of the normalized noise power — that is, the power delivered to a  $1\ \Omega$  load — over a 1 Hz bandwidth at that frequency. The noise spectral density of a voltage noise source can be denoted as  $V_n^2(f)$  and stated in units of  $V^2/\text{Hz}$ . Its corresponding root spectral density is given by  $V_n(f)$  and stated in units of  $V/\sqrt{\text{Hz}}$ . The spot noise of a noise source is an industry-standard term that is synonymous with root spectral density and is commonly specified at a certain frequency. Incidentally, the noise spectral density of a current noise source is similarly denoted as  $I_n^2(f)$  and stated in units of  $A^2/\text{Hz}$ .

Both thermal and shot noise can be modeled as white noise sources; that is, their noise spectral densities are constant over all frequencies. On the other hand, the spectral density of  $1/f$  noise is inversely proportional to frequency. For devices that exhibit both  $1/f$  and white noise components, such as MOSFETs and bipolar transistors, the  $1/f$  noise corner is defined as the frequency at which the  $1/f$  noise spectral density curve intersects the white noise spectral density curve. A graphical representation of the  $1/f$  noise corner can be found in Figure 3-1.

The concept of the  $1/f$  noise corner is equally applicable to op amps. The model of an op amp along with its noise sources is shown in Figure 3-2.<sup>1</sup> Since the frequency of the input signal to the op amp will be 15 kHz — the resonant frequency of the MEMS structure — it is desirable to have the  $1/f$  noise corner of the three op amp noise sources safely below 15 kHz, so that predominantly the white noise components will affect the output of the transimpedance amplifier.

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<sup>1</sup>Since noise in electronic systems is generally zero-mean, there is no concept of polarity of a noise source [16]. Rather, a noise source has a certain noise spectral density.

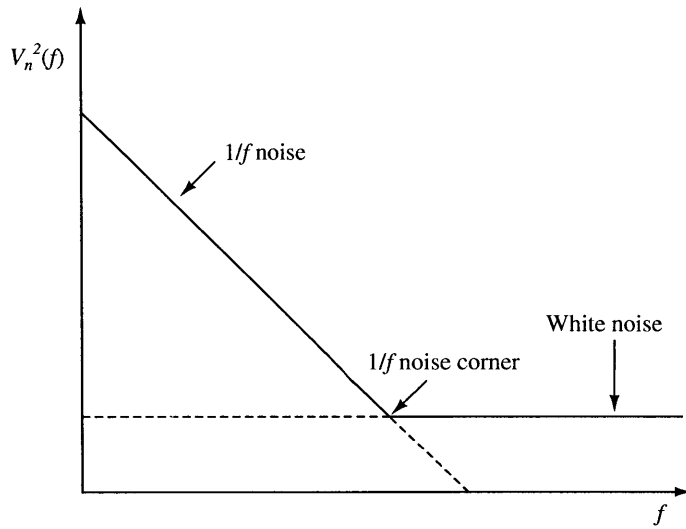


Figure 3-1: Graphical representation of the  $1/f$  noise corner.

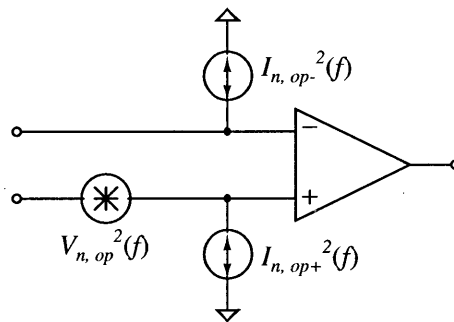


Figure 3-2: Noise model of an op amp.

### 3.2.2 BJT Input Stage Noise Analysis

The fundamental guideline for designing a low-noise op amp is that the noise characteristics of the transistors that compose the input stage of the op amp largely determine the overall input-referred noise characteristics of the op amp [16]. First, assume that BJTs are used for the input stage, as depicted in Figure 3-3. The complete noise model for a BJT is shown in Figure 3-4, where

$$V_{n,bjt}^2(f) = 4kT \left( r_b + \frac{1}{2g_m} \right) \quad (3.1)$$

and

$$I_{n,bjt}^2(f) = 2q \left( I_B + \frac{KI_B}{f} \right) \quad (3.2)$$

[15]. The variable  $k$  represents Boltzmann's constant ( $1.38 \times 10^{-23}$  J/K), while  $q$  represents the charge of an electron ( $1.6 \times 10^{-19}$  C). Also,  $T$  is the ambient temperature in kelvin, and  $K$  is a constant dependent on device characteristics. Lastly,  $I_B$  represents the dc base current,  $r_b$  the base resistance, and  $g_m$  the transconductance. Applying these noise sources to the input stage transistors, the circuit shown in Figure 3-5 is obtained. All transistor noise sources can be referred back to the input terminals of an op amp to determine the spectral densities of  $V_{n,op}^2(f)$ ,  $I_{n,op-}^2(f)$ , and  $I_{n,op+}^2(f)$  in Figure 3-2.

Nonetheless, only the contribution to  $I_{n,op+}^2(f)$  of the shot noise due to the base current of  $Q_1$  is analyzed and will be sufficient to see that the input bias current of a BJT precludes the feasibility of a BJT input stage for the desired low-noise op amp. Assume that now

$$I_{n,op+}^2(f) = I_{n,bjt}^2(f) = 2qI_B. \quad (3.3)$$

To analyze the effect of  $I_{n,op+}^2(f)$ , the impedance seen at the negative input terminal, denoted as  $v_-$  in Figure 3-5, must be considered. The intended transimpedance amplifier implementation calls for the configuration shown in Figure 3-6. Grounding

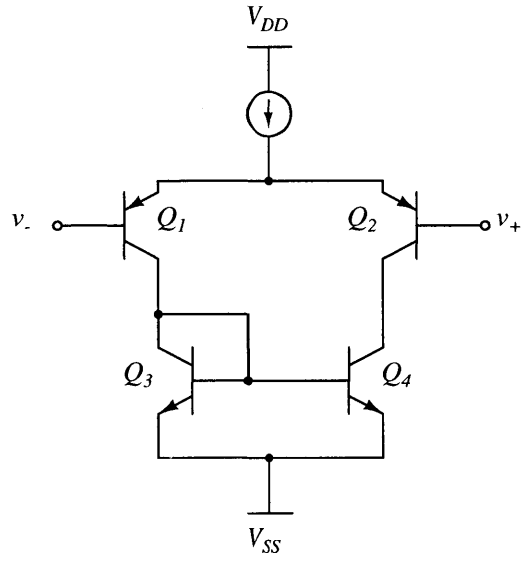


Figure 3-3: Op amp input stage composed of BJTs.

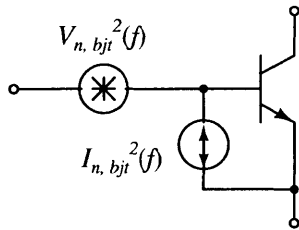


Figure 3-4: Noise model of a BJT.

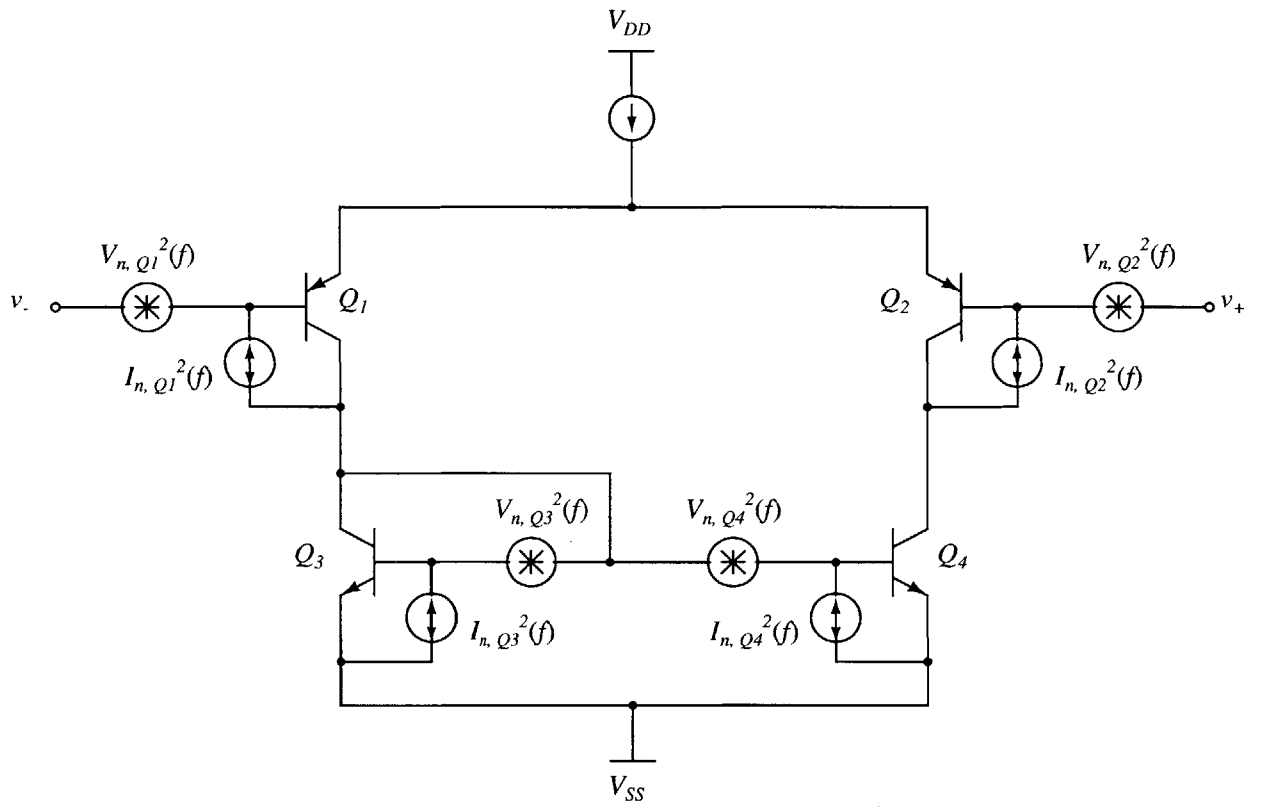


Figure 3-5: Op amp input stage with BJT noise models shown.

$V_{UNK}$  for purposes of this analysis, the impedance  $Z(s)$  seen at the base of  $Q_1$  is

$$Z(s) = \frac{1}{s(C_{sense} + C_{p,sense})}. \quad (3.4)$$

Since  $C_{p,sense} \approx 4.2 \text{ pF} \gg C_{sense} = 0.4 \text{ fF}$ ,  $Z(s)$  can be simplified to

$$Z(s) = \frac{1}{sC_{p,sense}}. \quad (3.5)$$

As discussed in [15],  $I_{n,op+}^2(f)$  can be replaced by an equivalent input voltage source of value

$$V_{ni,eq}^2(f) = I_{n,op+}^2(f) \cdot |Z(s)|^2. \quad (3.6)$$

Assuming reasonable values for the collector current ( $10 \mu\text{A}$ ) and  $\beta$  (100) of  $Q_1$ ,

$$I_{n,op+}^2(f) = 2qI_B = 2q \frac{I_C}{\beta} = 32 \times 10^{-27} \text{ A}^2/\text{Hz}. \quad (3.7)$$

The value of  $|Z(s)|$  is evaluated at  $\omega = 2\pi \cdot 15 \text{ kHz}$ , leading to

$$|Z(s)|^2 = \left( \frac{1}{\omega C_{p,sense}} \right)^2 = \frac{1}{2\pi \cdot 15 \text{ kHz} \cdot 4.2 \text{ pF}}^2 = 6.4 \times 10^{12} \Omega^2. \quad (3.8)$$

Therefore, the equivalent input voltage spot noise at 15 kHz due to the shot noise of  $Q_1$  is given by

$$\begin{aligned} V_{ni,eq}(f) &= \sqrt{I_{n,op+}^2(f) \cdot |Z(s)|^2} = \sqrt{32 \times 10^{-27} \text{ A}^2/\text{Hz} \cdot 6.4 \times 10^{12} \Omega^2} \\ &= 452 \text{ nV}/\sqrt{\text{Hz}}. \end{aligned} \quad (3.9)$$

While a complete list of the op amp specifications will be given in Section 3.3.1, the crucial, low-noise specification is a spot noise of  $10 \text{ nV}/\sqrt{\text{Hz}}$  at 15 kHz measured at the op-amp input. The  $452 \text{ nV}/\sqrt{\text{Hz}}$  value calculated in (3.9) is over one order of magnitude above the  $10 \text{ nV}/\sqrt{\text{Hz}}$  guideline. This calculation clearly shows why a BJT input differential pair is not suitable for a low-noise op amp in the desired application, where a high impedance is seen at the negative input terminal of the op

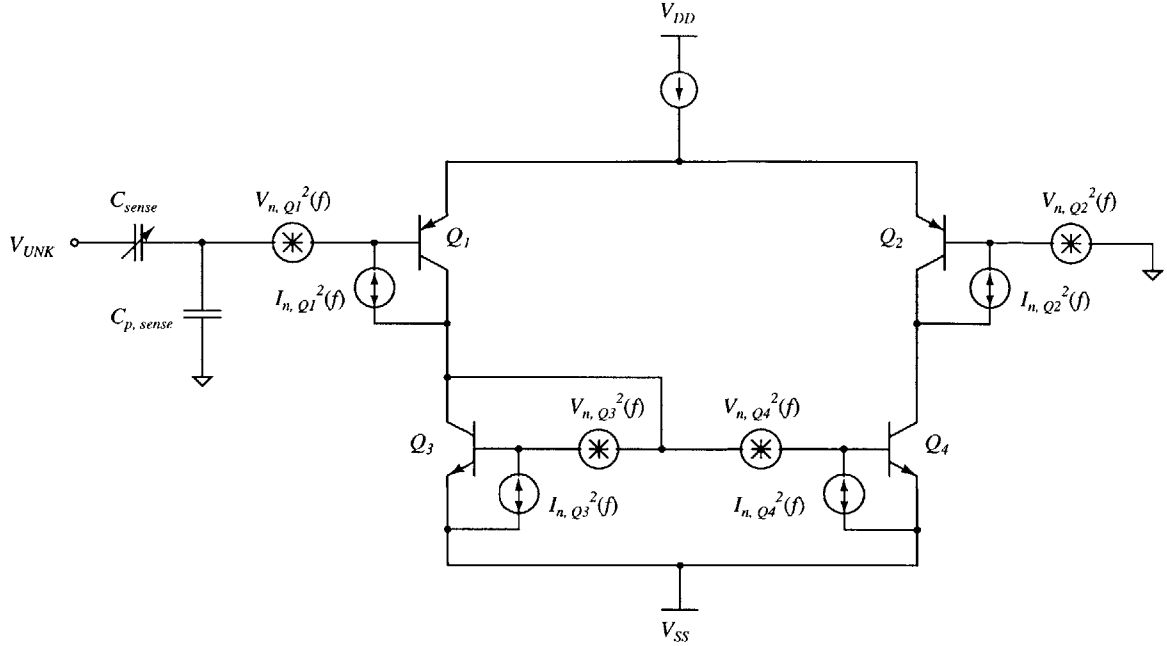


Figure 3-6: Op amp input stage with BJT noise models and capacitive impedances shown.

amp.

### 3.2.3 MOSFET Input Stage Noise Analysis

A low-noise op amp with a MOSFET input differential pair is now explored. Since the gate of a MOSFET is electrically isolated from the conductive channel, it never conducts dc current [15]. Thus, no shot noise is generated, and the previously discussed problem with BJT base currents is not encountered in a MOSFET input differential pair. For MOSFETs operating in the active region, the dominant noise sources are thermal and  $1/f$  noise. The low-to-moderate frequency noise model of a MOSFET is given in Figure 3-7, where

$$V_{n,mos}^2(f) = \frac{8}{3} \frac{kT}{g_m} + \frac{K}{WLC_{ox}f}, \quad (3.10)$$

[15]. The variables  $W$  and  $L$  represent the width and length, respectively, of the transistor, while  $C_{ox}$  represents its gate capacitance per unit area. As with the BJT,



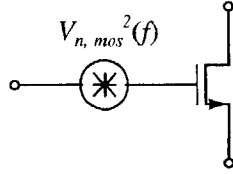


Figure 3-7: Noise model of a MOSFET.

$K$  is a constant dependent on transistor characteristics.

For an op amp with a MOSFET input differential pair, the op amp noise model previously shown in Figure 3-2 can be reduced to the model shown in Figure 3-8, with only a noise voltage source at its positive input terminal [15]. The magnitude of this noise source is predominantly determined by the input-referred noise of the input stage transistors [16]. The noise sources in the subsequent stages of the op amp are effectively reduced by the small-signal gains of the previous stages when referred to the input.

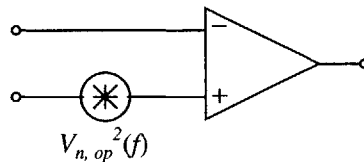


Figure 3-8: Noise model of an op amp with MOSFET input pair.

The input stage of a low-noise op amp with a MOSFET input differential pair is shown in Figure 3-9. All noise sources are also included in the figure. BJTs are used for the active current mirror load, as they have a lower  $1/f$  noise corner than MOSFETs [15], [18].

Though resistors generate thermal noise, the emitter-degeneration resistors included in the current mirror actually tend to reduce the total input-referred noise of the input stage [17]. An analysis of this seemingly counterintuitive result follows. The noise model of a resistor  $R$  is shown in Figure 3-10, where

$$V_{n,r}^2(f) = 4kTR \tag{3.11}$$



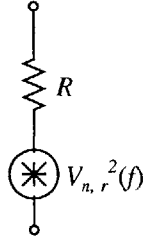


Figure 3-10: Noise model of a resistor.

[15].

Assume that only the noise contributions of  $R_2$  and the voltage noise source of  $Q_2$ ,  $V_{n,Q_2}^2(f)$ , are considered, as depicted in Figure 3-11. All noise sources are referred back to the positive terminal of the op amp, the gate of  $M_2$ , to find the equivalent input voltage noise. To do so, it is helpful to use simplified, low-frequency, small-signal models for the input-output relationship of a BJT and MOSFET, as shown in Figure 3-12. For a MOSFET in the active region,

$$i_d = g_m v_{gs}, \quad (3.12)$$

while for a BJT in the active region,

$$i_c = g_m v_\pi = g_m v_{be} = \beta i_b. \quad (3.13)$$

Since noise sources do not have polarities, the relative polarities of the various small-signal transistor voltages and currents will be ignored in the following analysis. First, assume  $R_1 = R_2 = 0$  to determine the input-referred noise of  $Q_2$  without any emitter-degeneration. Since  $Q_1$  is diode-connected, its input resistance is given by

$$r_{in,Q1} = \frac{1}{g_{m,Q1}}. \quad (3.14)$$

Using (3.12) and (3.13), one can solve for the drain current  $i_{d,M2}$  of  $M_2$  as follows:

$$v_{be,Q2} = \frac{r_{\pi,Q2}}{\frac{1}{g_{m,Q1}} + r_{\pi,Q2}} V_{n,Q1}(f) \quad (3.15)$$

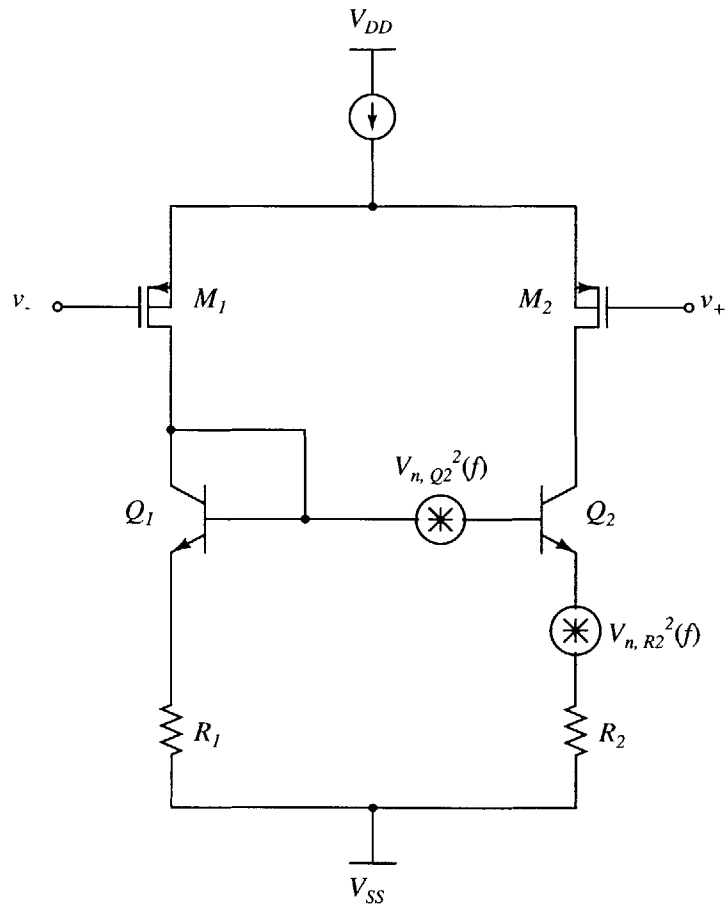


Figure 3-11: Op amp input stage with noise models of  $Q_2$  and  $R_2$  shown.

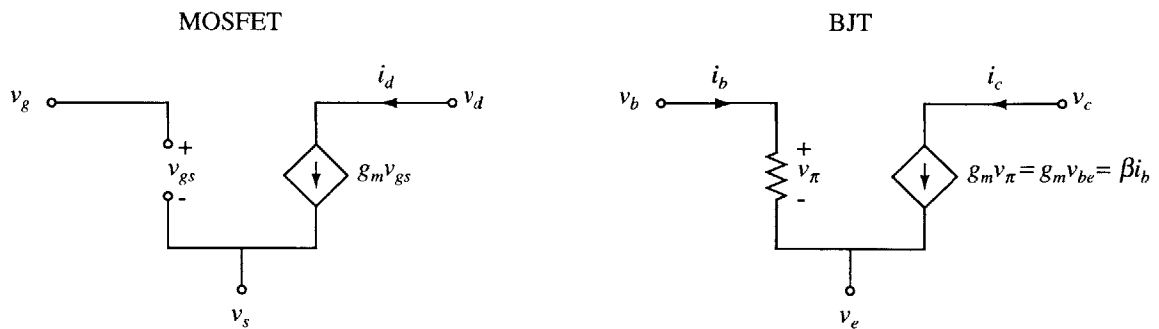


Figure 3-12: Simplified small-signal models for the input-output relationship of a BJT and MOSFET.

$$i_{c,Q2} = g_{m,Q2} v_{be,Q2} = i_{d,M2}. \quad (3.16)$$

For small-signal analysis of a differential amplifier, the source terminal of  $M_2$  is effectively grounded. Thus,  $v_{gs,M2} = v_{g,M2} = v_+$ , so any noise referred to  $v_{gs,M2}$  is effectively referred to the positive terminal of the op amp. Therefore,  $V_{n,op \rightarrow Q2}(f)$ , the input-referred noise due to  $V_{n,Q2}(f)$ , is given by

$$V_{n,op \rightarrow Q2}(f) = v_{gs,M2} = \frac{i_{d,M2}}{g_{m,M2}} = \frac{g_{m,Q2}}{g_{m,M2}} \frac{r_{\pi,Q2}}{\frac{1}{g_{m,Q1}} + r_{\pi,Q2}} V_{n,Q2}(f). \quad (3.17)$$

In reference to Figure 3-11, assume  $g_{m,Q2} = g_{m,M2}$ . Also, assuming the previously stated values for  $I_C$  ( $10 \mu\text{A}$ ) and  $\beta$  (100), the following small-signal parameters can be calculated:

$$g_{m,Q1} = g_{m,Q2} = g_{m,M2} = \frac{I_C}{V_T} = \frac{100 \mu\text{A}}{25 \text{ mV}} = 400 \mu\mathcal{S}, \quad (3.18)$$

$$r_{\pi,Q2} = \frac{\beta V_T}{I_C} = \frac{100 \cdot 25 \text{ mV}}{10 \mu\text{A}} = 250 \text{ k}\Omega. \quad (3.19)$$

Using (3.1) and with  $r_b = 0$ , we can solve for  $V_{n,Q2}(f)$ :

$$V_{n,Q2}(f) = \sqrt{\frac{4kT}{2g_{m,Q2}}} = 4.5 \text{ nV}/\sqrt{\text{Hz}}. \quad (3.20)$$

Thus, by (3.17),  $V_{n,op \rightarrow Q2}(f)$  is equal to

$$V_{n,op \rightarrow Q2}(f) = \frac{g_{m,Q2}}{g_{m,M2}} \frac{r_{\pi,Q2}}{\frac{1}{g_{m,Q1}} + r_{\pi,Q2}} V_{n,Q2}(f) = 4.5 \text{ nV}/\sqrt{\text{Hz}}. \quad (3.21)$$

Now, the effect on the input-referred noise with  $R_2 \neq 0$  will be shown. Specifically, assume  $R_2 = 5 \text{ k}\Omega$ , a reasonable emitter-degeneration resistor value. The input-referred noise due to  $V_{n,Q2}(f)$  is now given by

$$V_{n,op \rightarrow Q2}(f) = \frac{g_{m,Q2}}{g_{m,M2}} \frac{r_{\pi,Q2}}{\frac{1}{g_{m,Q1}} + r_{\pi,Q2} + (\beta + 1) R_2} V_{n,Q2}(f) = 1.5 \text{ nV}/\sqrt{\text{Hz}}. \quad (3.22)$$

Note that when considering one noise source, all other voltage noise sources must be

shorted, while current noise sources must be opened. The input-referred noise of  $R_2$  must now be taken into account. The thermal noise due to  $R_2$ , depicted in Figure 3-11, is given by (3.11) as

$$V_{n,R2}(f) = \sqrt{4kTR} = 9.1 \text{ nV}/\sqrt{\text{Hz}}. \quad (3.23)$$

As stated in [16],  $V_{n,R2}(f)$  is effectively in series with  $V_{n,Q2}(f)$ . Thus, (3.22) can be used to refer  $V_{n,R2}(f)$  to the input:

$$V_{n,op \rightarrow R2}(f) = \frac{g_{m,Q2}}{g_{m,M2}} \frac{r_{\pi,Q2}}{\frac{1}{g_{m,Q1}} + r_{\pi,Q2} + (\beta + 1)R_2} V_{n,R2}(f) = 3.0 \text{ nV}/\sqrt{\text{Hz}}. \quad (3.24)$$

Since  $V_{n,Q2}(f)$  and  $V_{n,R2}(f)$  are uncorrelated noise sources, the total input-referred noise due to both  $Q_2$  and  $R_2$  is found by

$$\begin{aligned} V_{n,op \rightarrow Q2,R2}(f) &= \sqrt{V_{n,op \rightarrow Q2}^2(f) + V_{n,op \rightarrow R2}^2(f)} \\ &= \sqrt{(1.5 \text{ nV}/\sqrt{\text{Hz}})^2 + (3.0 \text{ nV}/\sqrt{\text{Hz}})^2} = 3.4 \text{ nV}/\sqrt{\text{Hz}} \end{aligned} \quad (3.25)$$

[16]. Thus, the input-referred noise with emitter-degeneration is reduced to 75% of the value of  $4.5 \text{ nV}/\sqrt{\text{Hz}}$  with no emitter-degeneration given in (3.21). With reference to Figure 3-11, the input-referred noise contribution due to the voltage noise of  $Q_1$ ,  $V_{n,Q1}(f)$ , is similarly reduced by emitter-degeneration with  $R_1$ .

While the preceding op-amp input stage noise analysis was not exhaustive, it served as verification that emitter-degeneration of the input stage current mirror transistors lowers the total input-referred noise.

## 3.3 Op-Amp Transistor-Level Design

### 3.3.1 Op-Amp Specifications

The required op-amp specifications are shown in Table 3.1. These specifications are suitable to achieve the desired input-referred electric field noise presented in Chapter

Parameter	Specification
Supply Voltages	$\pm 12\text{ V}$
Output Voltage Swing	$-11\text{ V to }+11\text{ V}$
Quiescent Current	$< 150\ \mu\text{A}$
Input-referred Spot Noise at 15 kHz	$< 10\text{ nV}/\sqrt{\text{Hz}}$
Input-referred Offset Voltage	$< 50\ \mu\text{V}$
Unity-gain Bandwidth	$> 1.0\text{ MHz}$
Phase Margin	$\approx 60^\circ$
DC Gain	$> 1 \times 10^4$
Temperature Range	$-40^\circ\text{C to }+85^\circ\text{C}$

Table 3.1: Specifications for the low-noise operational amplifier.

1 [17].

### 3.3.2 Schematic and Low-Noise Design Methodology

With the goal of designing a low-noise op amp in mind, preliminary consideration was given to the distinct attributes — noise and otherwise — of each type of transistor. First, the use of PNP transistors was strongly discouraged due to their poor reliability in the iMEMS BiCMOS process [17], [18]. The p-channel MOSFETs (PFETs) have a lower  $1/f$  noise corner than n-channel MOSFETs (NFETs), since holes are less likely than electrons to enter the traps caused by defects in the semiconductor surface [15]. This quality makes PFETs the preferred choice for the input pair transistors. Also, as stated earlier, BJTs have a lower  $1/f$  noise corner than MOSFETs. Thus, NPNs were to be used wherever possible in place of NFETs.

Following these guidelines, the schematic for the low-noise op amp used in this thesis is shown in Figure 3-13. The corresponding list of transistor sizes and component values is given in Table 3.2. All MOSFET lengths are set at  $4\ \mu\text{m}$ , the feature size of the iMEMS process. This configuration is based on a low-noise op amp design for an Analog Devices integrated accelerometer [19]. Note that a discussion of the

Parameter	Size ( $W/L$ ) in $\mu\text{m}/\mu\text{m}$
$M_1$	160/4
$M_2$	160/4
$M_3$	170/4
$M_4$	40/4
$M_5$	240/4
$M_6$	120/4
$M_7$	40/4

Parameter	Component Value
$R_1$	4 k $\Omega$
$R_2$	4 k $\Omega$
$R_3$	60 k $\Omega$
$R_4$	100 k $\Omega$
$R_5$	900 k $\Omega$
$R_6$	1 k $\Omega$
$R_{pot}$	1 k $\Omega$
$C_C$	9.2 pF
$I_{REF}$	10 $\mu\text{A}$

Table 3.2: Transistor sizes and component values for the low-noise operational amplifier shown in Figure 3-13.

role of  $R_4$ ,  $R_5$ ,  $R_6$ , and  $R_{pot}$  will be postponed until Section 3.3.3.

The current source shown in Figure 3-13 is actually an off-chip resistor that sets  $I_{REF}$  to 10  $\mu\text{A}$ . Clearly, a resistor is not a form of temperature-independent biasing and would be unacceptable for a final product; however, a resistor current source was satisfactory for the proof-of-concept goal of this thesis. The total quiescent current consumption of the op amp is roughly 130  $\mu\text{A}$ . PFETs are used for the current mirrors due to the poor reliability of the PNPs in this process.

The input stage consists of  $M_1$  and  $M_2$  as the PFET input pair, and  $Q_1$  and  $Q_2$  as





the active current mirror. BJTs  $Q_1$  and  $Q_2$  are emitter-degenerated with  $R_1$  and  $R_2$ , respectively. Resistors  $R_1$  and  $R_2$  are thin-film resistors. MOSFETs  $M_1$  and  $M_2$  are each actually formed with two 80/4 transistors in parallel so that a common-centroid layout can be implemented. A common-centroid configuration cancels linear gradients in offset voltage, gate-oxide thickness, temperature, and other applicable parameters [20]. Also, nearly 50% of the total op-amp current is consumed by the input stage for low-noise performance. As evidenced by (3.1) and (3.10), the magnitude of the voltage noise of both BJTs and MOSFETs is inversely proportional to  $g_m$ , and, thus, inversely proportional to  $I_C$  or  $I_D$ . In addition, (3.10) indicates that having relatively wide input transistors lowers the  $1/f$  noise corner.

The output of the input stage is buffered by  $Q_3$  before it passes to the second gain stage, formed by  $Q_4$  and  $M_6$ . The thin-film resistor  $R_3$  sets the collector current of  $Q_3$ . The output stage of the op amp consists of  $M_3$  in a source-follower configuration. While all other MOSFETs are enhancement-mode devices,  $M_3$  is a depletion-mode, or native, NFET. Native MOSFETs typically have a gate-to-source threshold voltage of approximately 0 V [15]. With  $M_3$  as a native NFET, the output voltage is allowed to swing within  $V_{DS,sat,M6}$  of  $V_{DD}$  and within  $V_{CE,sat,Q5}$  of  $V_{SS}$ .

The op amp is internally compensated using the standard Miller-compensation technique discussed in the analog IC design literature [15], [21], [22]. Basically, without the compensation capacitor  $C_C$ , the op amp would have two high-impedance nodes — one at the collector of  $Q_2$  and the other at the collector of  $Q_4$  — that, combined with parasitic capacitances, would lead to two mid-frequency poles. The stability of any reasonable closed-loop system using such an op amp would likely be compromised. The addition of  $C_C$  results in the splitting of the two poles, creating a dominant pole and a high-frequency pole. The capacitor  $C_C$  can then be sized for the desired phase margin. A mathematical derivation of the pole-splitting phenomenon can be found in [15], [21], [22]; a more intuitive treatment of  $C_C$  as a minor-loop feedback path is presented in [23]. The compensation capacitor  $C_C$  in this thesis is implemented with a poly-n<sup>+</sup> capacitor, where the top plate is polysilicon and the bottom plate is an n<sup>+</sup> emitter diffusion.

### 3.3.3 Offset Reduction Technique

In addition to its spot noise, the offset voltage of the op amp is another important parameter. The implicit assumptions throughout Chapters 1 and 2 were that the shutter was held at true ground and that the *sense+* and *sense-* plates were held at virtual ground. While the former is completely valid, the latter is only approximately true. In reality, the sense plates are held at  $V_{OS}$ , the input-referred offset voltage.

A nonzero  $V_{OS}$  translates to more than just a nominal output-referred offset voltage. As depicted in Figure 3-14, a parasitic electric field, identified as  $E_p$ , is formed between the sense plates and the shutter. The magnitude of  $E_p$  is given by

$$|E_p| = \frac{|V_{OS}|}{d_{shutter}}, \quad (3.26)$$

where  $d_{shutter}$  is the distance between the sense plates and the shutter, and was identified as being  $2\ \mu\text{m}$  in Chapter 2. Although the systematic offset voltage of all op amps can be minimized by carefully sizing transistors, excessive minimization is fruitless because processing non-idealities cause component mismatches. These mismatches, in turn, result in an offset voltage, which, for an op amp with a MOSFET-based input pair, can be in the range of a few millivolts [24]. Assuming  $|V_{OS}| = 5\ \text{mV}$ , the magnitude of  $E_p$  is calculated using (3.26):

$$|E_p| = \frac{|V_{OS}|}{d_{shutter}} = \frac{5\ \text{mV}}{2\ \mu\text{m}} = 2500\ \text{V/m}. \quad (3.27)$$

In Table 1.1, the specification for the input-referred noise of the entire ESF was  $200\ \text{V/m}/\sqrt{\text{Hz}}$ . Using off-chip components, a noise bandwidth of 1 Hz is not unreasonable. The resulting rms value of the input electric field noise,  $E_{ni}(f)$ , is given by

$$E_{ni,rms} = E_{ni}(f) \cdot \sqrt{\Delta f} = 200\ \text{V/m}/\sqrt{\text{Hz}} \cdot \sqrt{1\ \text{Hz}} = 200\ \text{V/m (rms)}. \quad (3.28)$$

As stated in [16] and discussed in detail in Chapter 5, the peak-to-peak amplitude of a noise source is given by six times its rms value. Equivalently, the peak-to-ground

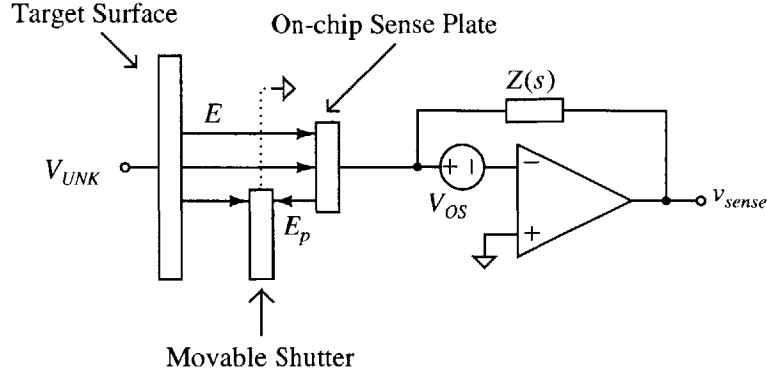


Figure 3-14: ESF input stage showing the parasitic electric field,  $E_p$ , due to the op amp offset voltage,  $V_{OS}$ .

amplitude is equal to three times the rms value of the noise source. Thus, the ESF should be able to detect incident electric fields down to

$$E_{min} = E_{ni,pk} = 3 E_{ni,rms} = 3 \cdot 200 \text{ V/m (rms)} = 600 \text{ V/m}, \quad (3.29)$$

which is considerably smaller than the parasitic electric field due to  $V_{OS}$  given in (3.27). With  $|V_{OS}| = 5 \text{ mV}$ , the minimum detectable field is not limited by the noise of the system, but rather, by the magnitude of  $E_p$ .

Offset nulling techniques, such as chopper stabilization [25], do exist, but a simpler method [26] was used here. With reference to Figure 3-13,  $R_4$ ,  $R_5$ ,  $R_6$ , and  $R_{pot}$  basically act as an adjustable current source. Adjusting the wiper position of potentiometer  $R_{pot}$  (and, thus, the voltage of the wiper) adjusts the miniscule amount of current that is injected into Node A via the  $1 \text{ M}\Omega$  resistance formed with  $R_4$  and  $R_5$ .

In order to null its offset voltage, the op amp is connected in the configuration shown in Figure 3-15, with an oscilloscope probe at  $V_{OUT}$ . The wiper position is then adjusted until  $V_{OUT} = V_{OS} \approx 0 \text{ V}$ . As was the case with the op amp biasing, this nulling scheme, though not temperature-independent, is suitable for the desired prototype ESF system.

Resistor  $R_4$  is an on-chip, thin-film resistor, while  $R_5$  and  $R_6$  are off-chip resistors. Resistor  $R_{pot}$  is a precision trimming potentiometer. The  $1 \text{ M}\Omega$  series resistance of  $R_4$

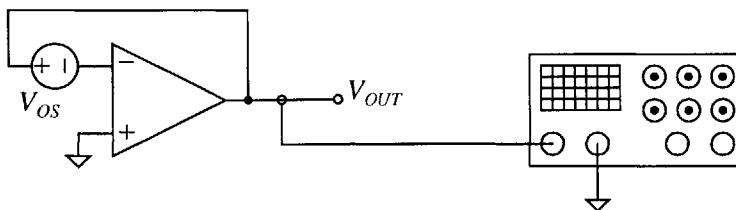


Figure 3-15: Op amp configuration for offset voltage measurement and nulling.

and  $R_5$  is split into two resistors because fabricating a  $1\text{ M}\Omega$  resistor on-chip would have been difficult due to die area limitations. However, directly connecting Node A to an external pin is also inadvisable. Having  $R_4 = 100\text{ k}\Omega$  of the effective  $1\text{ M}\Omega$  resistance on-chip protects  $Q_1$  and  $M_1$  from damage due to accidental shorts to  $V_{DD}$  or  $V_{SS}$ . Resistor  $R_6$  serves to protect from short circuits from GND to  $V_{SS}$ .

### 3.3.4 Simulation Results

The low-noise op amp was simulated using Analog Devices' proprietary simulation tool, ADICE. The power supplies were  $\pm 12\text{ V}$ , and the total quiescent current consumption was  $130\text{ }\mu\text{A}$ .

A Bode plot of the input-to-output frequency response of the op amp is given in Figure 3-16. The DC gain is  $2.3 \times 10^5$ . The unity-gain bandwidth is  $7.0\text{ MHz}$ , while the phase margin is  $60.2^\circ$ . Note that these are the simulated values for  $T = +27^\circ\text{C}$ . The Bode plot for  $T = -40^\circ\text{C}$  is given in Figure 3-17, while that for  $T = +85^\circ\text{C}$  is presented in Figure 3-18. Although the DC gain and bandwidth change over temperature, the phase margin remains at roughly  $60^\circ$ . Thus, assuming the loop is stable at  $T = +27^\circ\text{C}$  and the loop elements have reasonably low temperature coefficients, loop stability is ensured over the desired temperature range.

The input-referred noise is calculated by finding the noise root spectral density at the output, and then dividing by the open-loop gain over frequency. As shown in Figure 3-19, the input-referred spot noise at  $15\text{ kHz}$  is  $9.65\text{ nV}/\sqrt{\text{Hz}}$ .

The simulation results of the offset nulling scheme were very promising. First, without the nulling scheme, the (systematic) offset voltage was  $1.2\text{ mV}$ . By adjust-

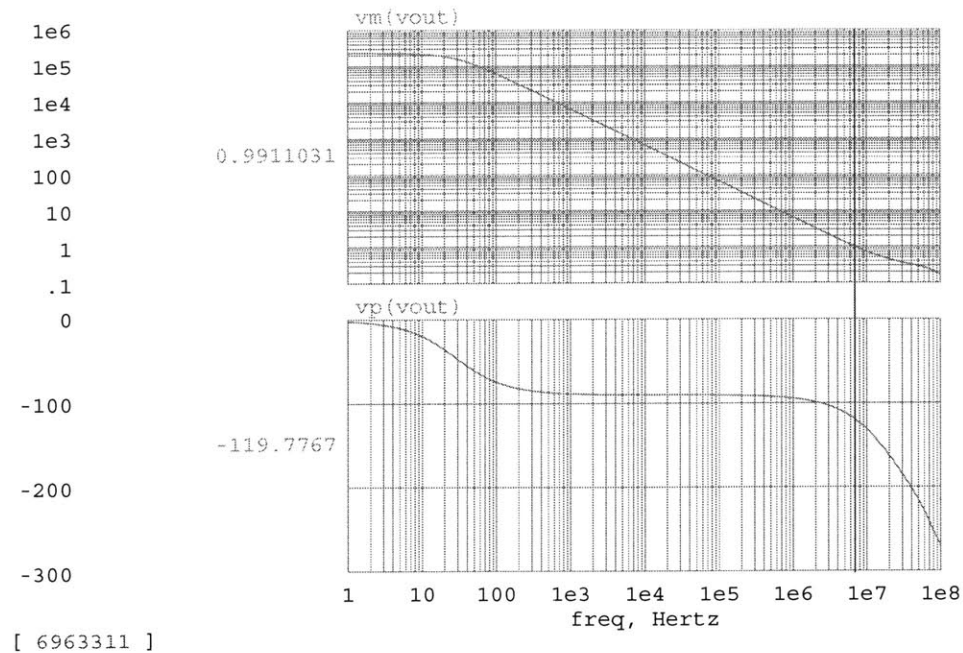


Figure 3-16: Input-to-output frequency response of the low-noise op amp at  $T = +27^{\circ}\text{C}$ . Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].

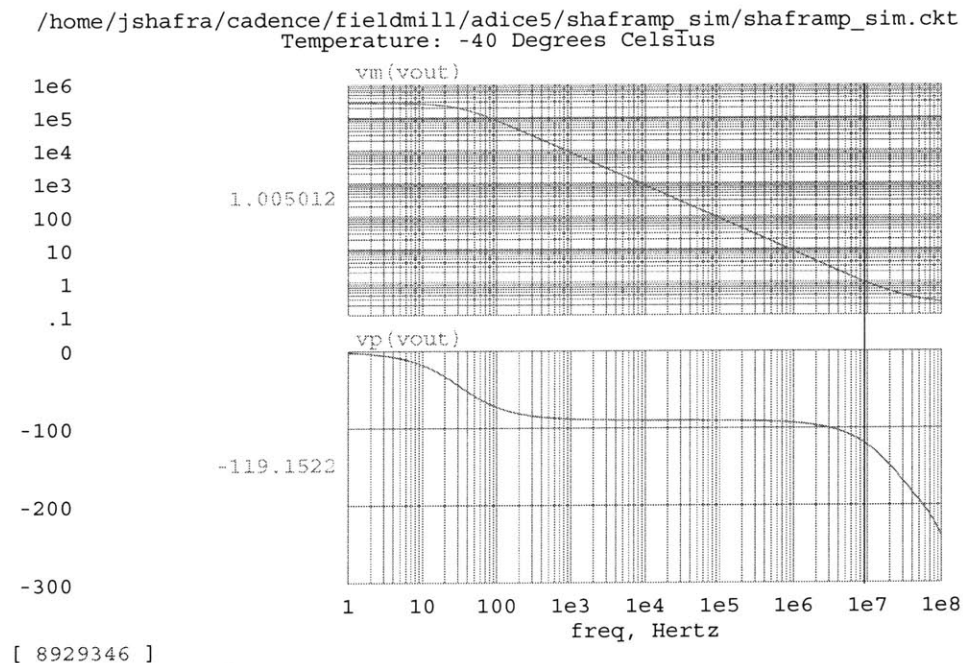


Figure 3-17: Input-to-output frequency response of the low-noise op amp at  $T = -40^{\circ}\text{C}$ . Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].

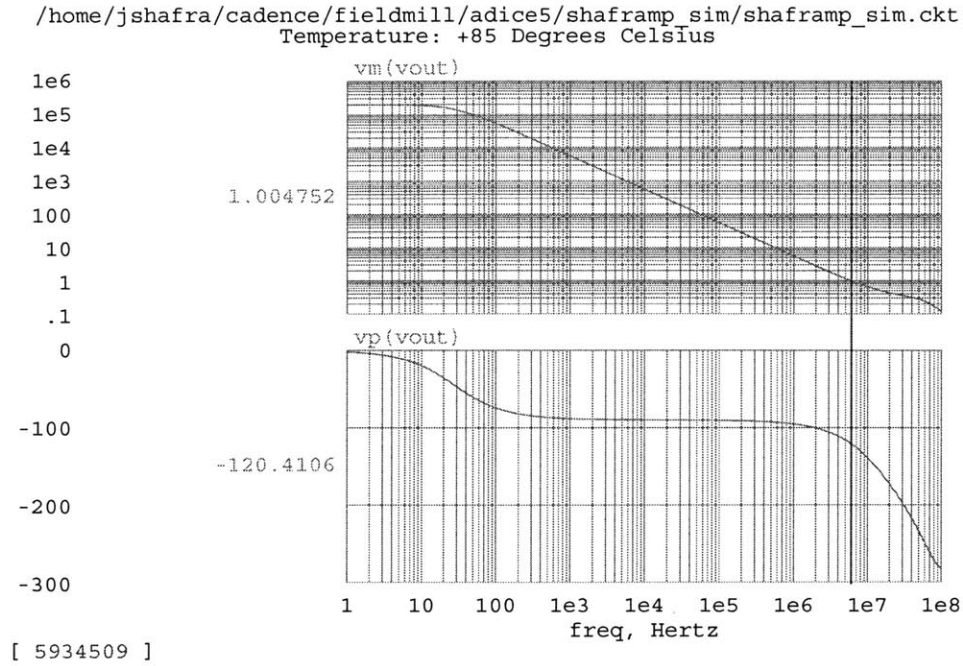


Figure 3-18: Input-to-output frequency response of the low-noise op amp at  $T = +85^\circ\text{C}$ . Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].

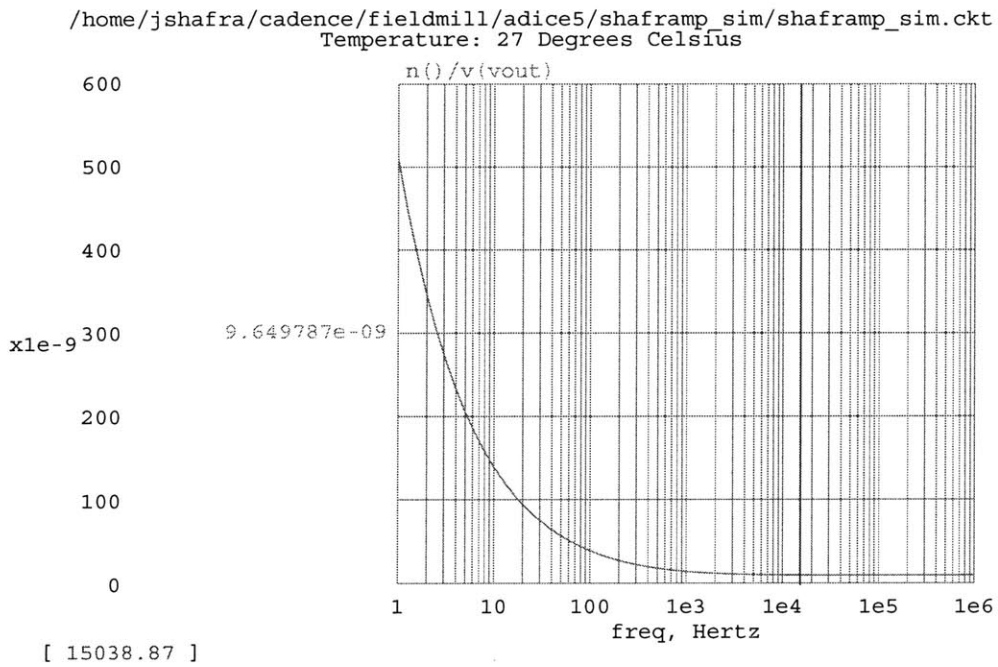


Figure 3-19: Input-referred noise frequency response of the low-noise op amp. Vertical axis: Input-referred noise [ $\text{nV}/\sqrt{\text{Hz}}$ ]. Horizontal axis: Frequency [Hz].

ing  $V_{ADJUST}$  in Figure 3-13 to a precision of one-hundredth of 1 V (specifically to  $-11.80$  V), the offset voltage was reduced to  $16 \mu\text{V}$ , as depicted in Figure 3-20. Obtaining a wiper potential precision of one-hundredth of 1 V, or, equivalently,

$$\frac{0.01 \text{ V}}{V_{Rpot}} = \frac{0.01 \text{ V}}{0.5 \cdot 12 \text{ V}} = \frac{0.01 \text{ V}}{6 \text{ V}} \approx 2000 \text{ ppm}, \quad (3.30)$$

is a reasonable expectation of a precision trimming potentiometer [27]. For  $|V_{OS}| = 16 \mu\text{V}$ ,  $|E_p|$  is now given by (3.26) as

$$|E_p| = \frac{|V_{OS}|}{d_{shutter}} = \frac{12 \mu\text{V}}{2 \mu\text{m}} = 6 \text{ V/m}, \quad (3.31)$$

which is two orders of magnitude smaller than the minimum detectable field of  $600 \text{ V/m}$ . The effect of the parasitic electric field is now negligible.

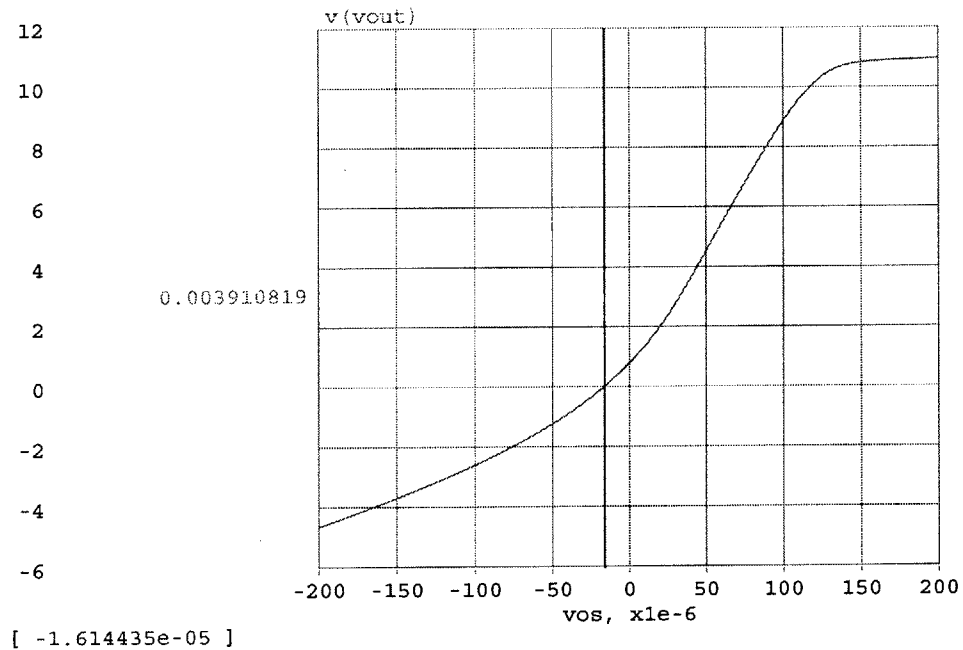


Figure 3-20: DC sweep of the low-noise op amp offset voltage. Vertical axis: Output voltage [V]. Horizontal axis: Offset voltage [ $\mu\text{V}$ ].

Lastly, in Figure 3-21, a dc sweep of the offset voltage indicates that the output voltage swings from  $-11.35$  V to  $+11.16$  V.

The simulation results are tabulated in Table 3.3 along with the corresponding



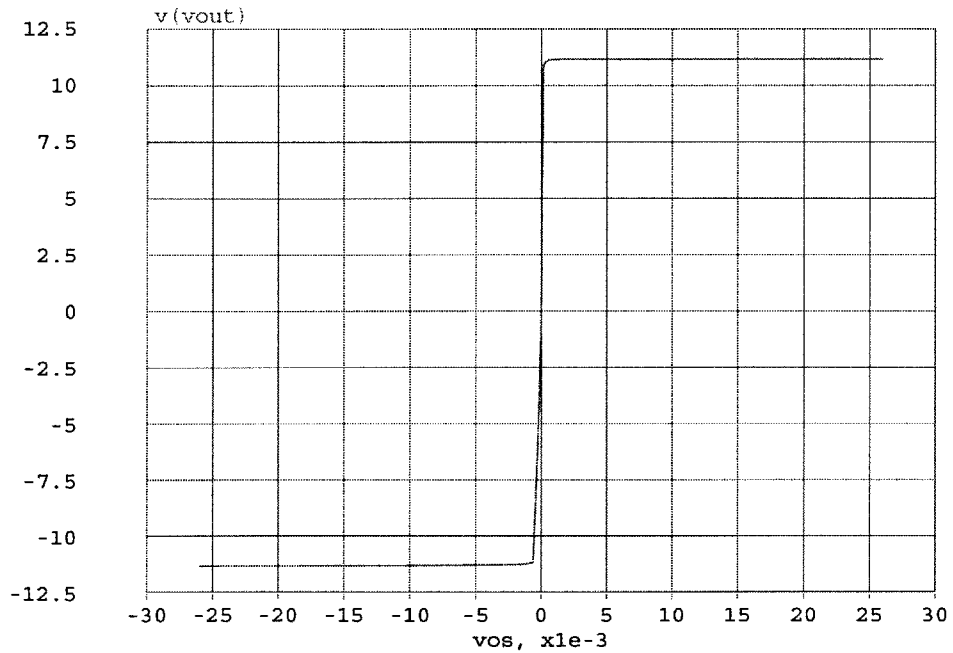


Figure 3-21: DC sweep of the low-noise op amp offset voltage to identify the output voltage swing. Vertical axis: Output voltage [V]. Horizontal axis: Offset voltage [mV].

specifications. All of the guidelines for the low-noise op amp were satisfied. Note that, as was mentioned in Chapter 2, the effective input capacitance of the op amp is 0.5 pF. This value was absorbed into the values of  $C_{p,sense} = 4.2$  pF and  $C_{p,vel} = 1.0$  pF given in Table 2.2.

Parameter	Specification	Simulation Result
Supply Voltages	$\pm 12\text{ V}$	$\pm 12\text{ V}$
Output Voltage Swing	$-11\text{ V to }+11\text{ V}$	$-11.35\text{ V to }+11.16\text{ V}$
Quiescent Current	$< 150\ \mu\text{A}$	$130\ \mu\text{A}$
Input-referred Spot Noise at 15 kHz	$< 10\text{ nV}/\sqrt{\text{Hz}}$	$9.65\text{ nV}/\sqrt{\text{Hz}}$
Input-referred Offset Voltage	$< 50\ \mu\text{V}$	$16\ \mu\text{V}$
Unity-gain Bandwidth	$> 1.0\text{ MHz}$	$7.0\text{ MHz}$
Phase Margin	$\approx 60^\circ$	$60^\circ$
DC Gain	$> 1.0 \times 10^4$	$2.3 \times 10^5$
Temperature Range	$-40^\circ\text{C to }+85^\circ\text{C}$	$-40^\circ\text{C to }+85^\circ\text{C}$

Table 3.3: Specifications and simulation results for the low-noise op amp.

## 3.4 Summary

As was discussed in Chapter 1, one of the major goals of this thesis is to improve on the noise performance of the Riehl ESF. Achieving this goal requires a low-noise operational amplifier for high-accuracy electric field sensing.

Since the input stage noise largely determines the overall input-referred noise of the op amp, the input stage is optimized for low-noise operation. Emitter-degenerating the active current mirror transistors decreases their effective transconductances, and the input-referred noise is reduced considerably. A BiCMOS op amp which incorporates this technique was presented, and simulation results indicate that it meets the desired spot noise guideline of  $10 \text{ nV}/\sqrt{\text{Hz}}$ . The op-amp offset voltage creates a parasitic electric field which can seriously limit the minimum detectable electric field. An offset-nulling scheme was developed to minimize the magnitude of this parasitic electric field and thus allow high-resolution sensing.



# Chapter 4

## Drive Loop

### 4.1 Overview

As was discussed previously, it is highly desirable to drive the MEMS structure at its resonant frequency for maximum shutter displacement. Maximum shutter displacement, in turn, results in maximum SNR at the sensor output. However, the actual resonant frequency  $f_{res}$  is not precisely known and can vary from sample to sample due to process variations. In addition, the  $f_{res}$  of a particular sample can change over temperature. Thus, a self-resonating feedback loop is necessary to robustly generate an oscillating force drive voltage at precisely  $f_{res}$ .

One implementation of such a loop is discussed in this chapter. This topology uses the fortunate result of the force drive and shutter velocity being in phase at resonance, which was covered in Section 2.6. Since this implementation uses a comparator — a nonlinear element — in the feedback loop, a describing function analysis is performed to determine the stability of the loop.

### 4.2 Ideal Analysis

The goal of the drive loop is to create force drive voltages that are in phase with the shutter velocity, thereby enabling resonant operation. A simplified schematic of the drive loop circuitry is illustrated in Figure 4-1. A description of the component

identities or values is given in Table 4.1. Note that all components other than the transresistance amplifiers are located off-chip on a PCB.

Parameter	Component Description
$U_1$	Low-Noise Op Amp
$U_2$	Low-Noise Op Amp
$U_3$	AD620AN Instrumentation Amplifier
$U_4$	AD790AQ Comparator
$U_5$	ADG333ABN Quad SPDT Switch
Parameter	Component Value
$R_{f+}$	200 k $\Omega$
$R_{f-}$	200 k $\Omega$
$R_{filter}$	100 k $\Omega$
$C_{filter}$	0.1 $\mu$ F

Table 4.1: Component descriptions or values for the drive loop circuit shown in Figure 4-1 [28], [29], [30].

The velocity sense currents  $i_{vel+}$  and  $i_{vel-}$  are generated with the  $C_{vel}$  configuration described in Section 2.4 and are proportional to the shutter velocity. Expressions for the currents were derived to be:

$$i_{vel+} = -2N_{vel} V_{BIAS} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} \quad (4.1)$$

$$i_{vel-} = +2N_{vel} V_{BIAS} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} \quad (4.2)$$

The currents are converted to voltages  $v_{vel+}$  and  $v_{vel-}$  by the transresistance amplifiers. The voltages are given by:

$$v_{vel+} = V_{BIAS} - i_{vel+} R_{f+} = V_{BIAS} \left( 1 + 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} R_{f+} \right) \quad (4.3)$$

$$v_{vel-} = V_{BIAS} - i_{vel-} R_{f-} = V_{BIAS} \left( 1 - 2N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} R_{f-} \right). \quad (4.4)$$

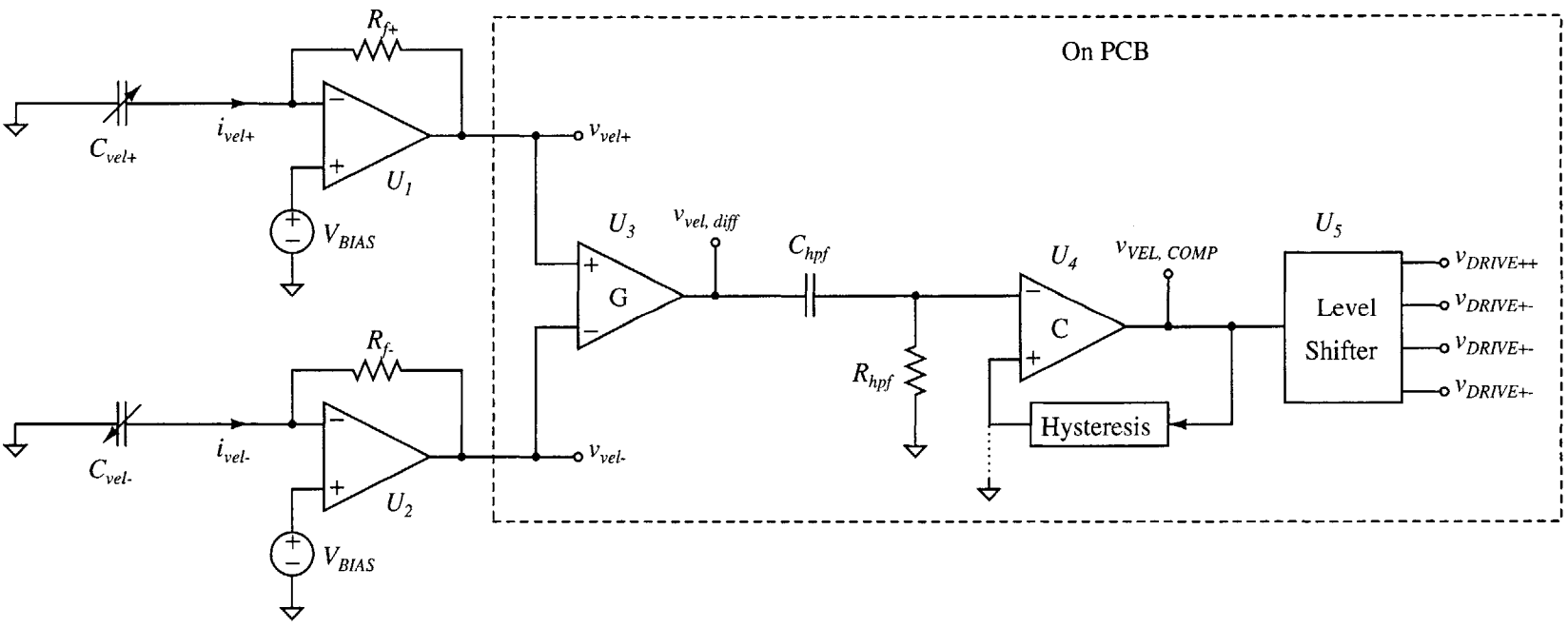


Figure 4-1: Simplified schematic of the drive loop circuitry.

Although low-noise operation is not crucial for velocity sensing, the low-noise op amps discussed in Chapter 3 are used for  $U_1$  and  $U_2$  for simplicity. Resistors  $R_{f+}$  and  $R_{f-}$  are thin-film resistors. Since a larger feedback resistor translates to a larger output voltage of the transresistance amplifier,  $R_{f+}$  and  $R_{f-}$  are set to 200 k $\Omega$ , a large, yet reasonable, value for integrated resistors [17].

An instrumentation amplifier  $U_3$  then performs a differential-to-single-ended conversion and outputs

$$\begin{aligned} v_{vel,diff} = G(v_{vel+} - v_{vel-}) &= G \left( 4N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} R_f \right) \\ &\equiv 4G N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} R_f, \end{aligned} \quad (4.5)$$

where  $G$  represents the gain of the instrumentation amplifier, and  $R_f = R_{f+} = R_{f-}$ . Recall from Chapter 2 that  $x_{dyn}(t) = x_m \sin(\omega_{res}t)$ . Thus,  $v_{vel,diff}$  is a sinusoidal voltage given by

$$\begin{aligned} v_{vel,diff} &= 4G N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} R_f \\ &= 4G N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{d}{dt} [x_m \sin(\omega_{res}t)] R_f \\ &= 4G N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} x_m \omega_{res} \cos(\omega_{res}t) R_f, \end{aligned} \quad (4.6)$$

for a peak-to-peak voltage of 5.2G mV (pp). Although the exact choice of  $G$  does not affect the functionality of the loop, a larger  $v_{vel,diff}$  makes it more easily viewable on an oscilloscope. For this reason, the gain is set to  $G = 10$ .

Ignoring  $R_{hpf}$  and  $C_{hpf}$  for the moment,  $v_{vel,diff}$  then serves as the inverting input to the comparator  $U_4$ . The comparator incorporates some form of hysteresis from its output to its non-inverting terminal to prevent oscillations near the comparator threshold voltage. A description of the innards of the hysteresis block will be best postponed until Section 4.4. For now, assume that the non-inverting terminal of  $U_4$  is held at ground. As illustrated in Figure 4-2, the output of the comparator  $v_{VEL,COMP}$  is a square-wave voltage that is 180° out of phase with  $v_{vel,diff}$ . While the phase shift



does not affect the functionality of the drive loop,  $v_{VEL,COMP}$  also serves as an input to the sense block circuitry, and having  $v_{vel,diff}$  and  $v_{VEL,COMP}$  out of phase actually reduces the number of components required for the sense block.<sup>1</sup>

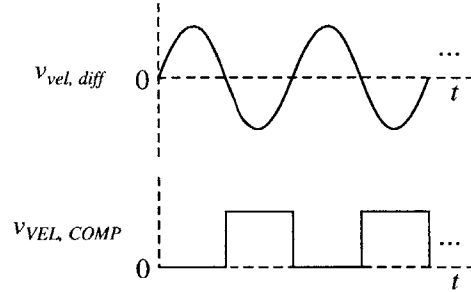


Figure 4-2: Ideal waveforms for  $v_{vel,diff}$  and  $v_{VEL,COMP}$ . The two waveforms are 180° out of phase.

Returning to the role of  $R_{hpf}$  and  $C_{hpf}$ , the dc component of  $v_{vel,diff}$  is ideally zero. However, a nonzero dc component can exist due to the offset voltages of  $U_1$ ,  $U_2$ , and  $U_3$ . As a result,  $v_{vel,diff}$  is passed through a high-pass filter to strip off any cumulative dc offset before serving as an input to the comparator. The input-to-output transfer function of the filter is given by

$$\frac{V_o}{V_i}(s) = \frac{sR_{hpf}C_{hpf}}{sR_{hpf}C_{hpf} + 1}. \quad (4.7)$$

The  $-3$  dB frequency of the filter is equal to

$$f_{-3\text{dB}} = \frac{1}{2\pi R_{hpf}C_{hpf}} = 15.9 \text{ Hz}. \quad (4.8)$$

The level-shifter  $U_5$  is actually a quad package of single-pole/double-throw (SPDT) analog switches. The switches are configured to output the voltages given in Table 4.2 based on the state of  $v_{VEL,COMP}$ . These output voltages then serve as the force drive voltages that are applied to the  $C_{force+}$  and  $C_{force-}$  electrodes on the MEMS sensor. A quad package is necessary because four distinct drive voltages are required. The

<sup>1</sup>The phase inversion is cancelled out because an active low-pass filter is used as the last element in the sense block. An active low-pass filter inherently has a phase inversion from input to output. The sense circuitry will be covered in detail in Chapter 5.

notation for these drive voltages was originally captured in Table 2.1 and is repeated in Table 4.3 for convenience.

$v_{vel,diff}$	<b>VVEL,COMP</b>	<b>VDRIVE++</b>	<b>VDRIVE+-</b>	<b>VDRIVE--+</b>	<b>VDRIVE--</b>
+	0 V	+15 V	-15 V	0 V	0 V
-	+5 V	0 V	0 V	+15 V	-15 V

Table 4.2: States of the force drive voltages based on  $v_{VEL,COMP}$  and the polarity of  $v_{vel,diff}$ .

<b>Previous Notation</b>	<b>Sector+ / Sector-</b>	<b>Drive Voltage</b>	<b>New Notation</b>
$v_{DRIVE+}$	Sector+	$V_O = +15\text{ V}$	$v_{DRIVE++}$
$v_{DRIVE+}$	Sector-	$-V_O = -15\text{ V}$	$v_{DRIVE+-}$
$v_{DRIVE-}$	Sector+	$V_O = +15\text{ V}$	$v_{DRIVE-+}$
$v_{DRIVE-}$	Sector-	$-V_O = -15\text{ V}$	$v_{DRIVE--}$

Table 4.3: New notation for the force drive voltages. A plus or minus sign is added to  $v_{DRIVE+}$  and  $v_{DRIVE-}$  to designate whether the voltage is applied to the Sector+ or Sector- electrode.

Figure 4-3 is a telling graphic that captures the state of the drive voltages versus shutter displacement and velocity. When  $v_{vel,diff} > 0$ , the *force+* electrodes are driven to  $\pm 15\text{ V}$ . On the other hand, when  $v_{vel,diff} < 0$ , the *force-* electrodes are driven to  $\pm 15\text{ V}$ . As one can see, the force drive waveforms and the shutter velocity are in phase.<sup>2</sup> In Section 2.6, a frequency-domain analysis indicated that the force drive and shutter velocity are in phase only at resonance. The conclusion is that the drive loop is a self-resonant loop that ensures resonant operation of the MEMS sensor. The fact that the force drive waveforms and the shutter velocity are in phase indicates that the drive loop is a positive-feedback system.

<sup>2</sup>The force drive and shutter velocity are not precisely in phase due to the finite bandwidths or response times of  $U_1-U_5$ , and any phase shift due to the high-pass filter. The effect of this phase shift between force drive and shutter velocity will be analyzed in Section 4.4.

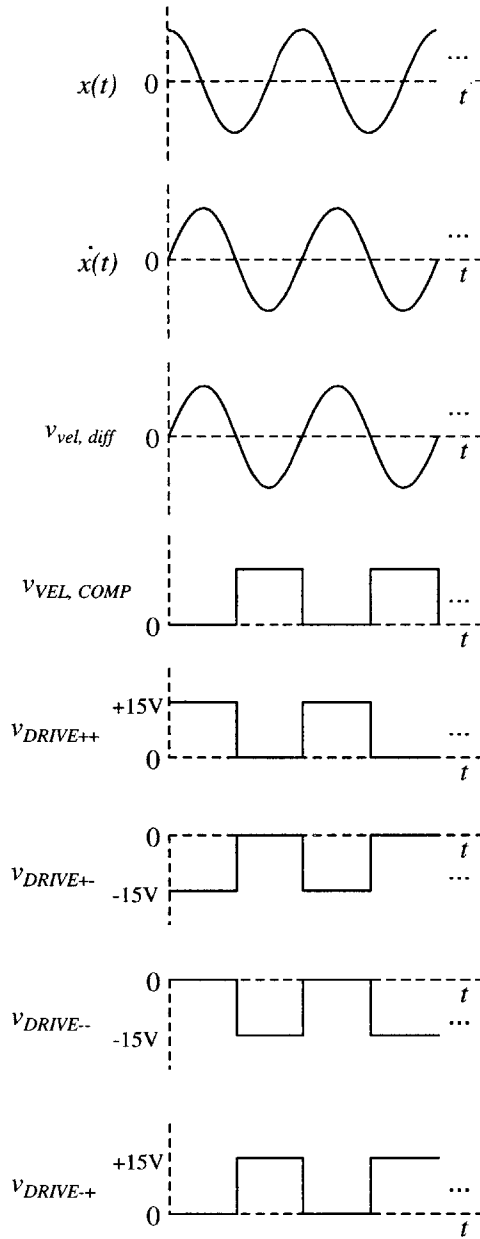


Figure 4-3: Ideal waveforms for  $x(t)$ ,  $\dot{x}(t)$ , and key drive loop voltages. The force drive voltages and shutter velocity  $\dot{x}(t)$  are in phase, which occurs only at resonance.

## 4.3 Feedback Analysis

### 4.3.1 Global Feedback Considerations

As discussed in [31], describing functions provide a method for analyzing feedback loops with nonlinear elements that is similar to standard linear system analysis. One application of describing function techniques is to predict whether limit cycles — constant-amplitude, periodic oscillations — can exist in a given system. The subsequent analysis will illustrate that limit cycles are possible for the drive loop.

If the input to the nonlinear element is of the form

$$v_i(t) = E \sin(\omega t), \quad (4.9)$$

then the output can be expanded in a Fourier Series that includes the fundamental component and all of the harmonic components. The describing function of the nonlinear element represents the amplitude and phase angle of the fundamental component relative to the sinusoidal input. Assuming that the feedback loop that contains the nonlinear element is generally low-pass in nature, the system dynamics can be accurately modeled with the inclusion of the describing function in the loop transfer function.

For purposes of determining if limit cycles are possible in a positive-feedback system, such as the drive loop, it is helpful to represent the system as shown in Figure 4-4.<sup>3</sup> For the drive loop, the nonlinear element is the comparator, while the MEMS dynamics and other circuitry are lumped into the linear element block. The details of this arrangement are illustrated in Figure 4-5.

The relationship between the force drive voltage and the magnitude of the force on the shutter was derived in Chapter 2 as

$$\vec{F} = \pm N_{force} \frac{\epsilon_o l_{force}}{d_{force}} V_O^2 \hat{x}. \quad (4.10)$$

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<sup>3</sup>In a negative-feedback system, an inversion block would be included in the loop representation.

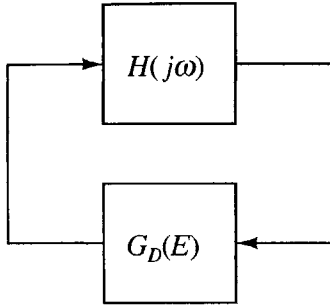


Figure 4-4: Representation for a nonlinear system connected in positive feedback.  $H(j\omega)$  denotes the linear elements, while  $G_D(E)$  denotes the describing function of the nonlinear element.

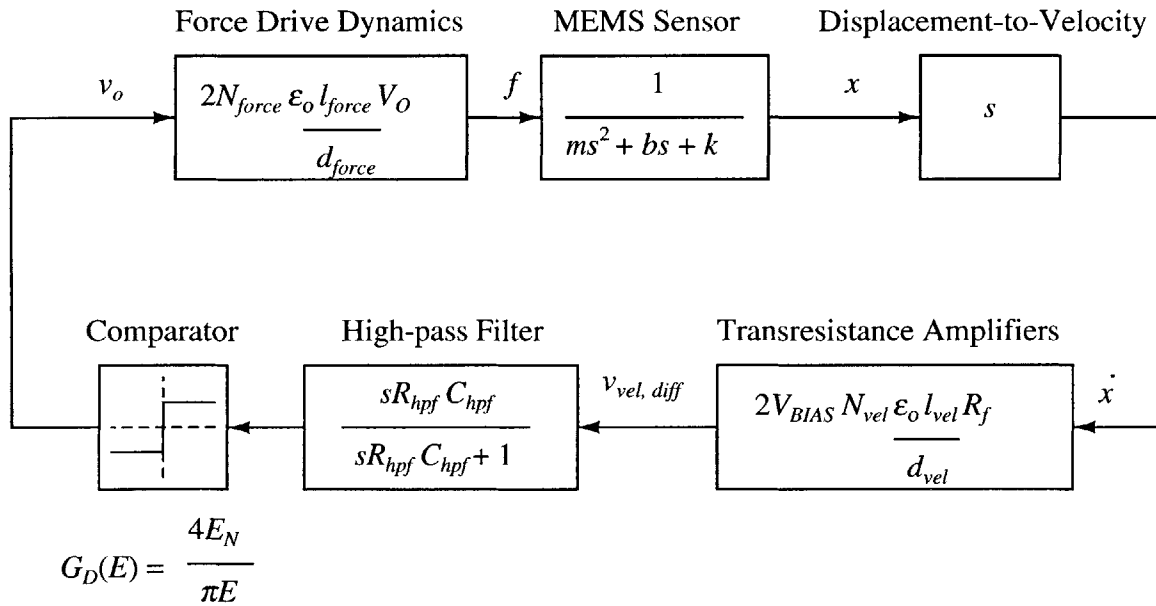


Figure 4-5: Feedback loop representation of the drive loop.

This relationship must be linearized for inclusion into the linear element block. Letting  $f$  represent the incremental portion of  $\vec{F}$ , it follows that

$$f = 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} V_O v_o. \quad (4.11)$$

Thus,

$$\frac{f}{v_o} = 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} V_O, \quad (4.12)$$

which is the incremental gain given in Figure 4-5. No specific polarity is assigned to  $f$ . Rather,  $f$  represents the incremental force in whichever direction  $\vec{F}$  is pointing. Therefore, the transfer function of the linear element is given by

$$\begin{aligned} H(j\omega) = & 2N_{force} \frac{\epsilon_o l_{force}}{d_{force}} V_O \cdot \frac{j\omega}{m(j\omega)^2 + b(j\omega) + k} \cdots \\ & 2V_{BIAS} N_{vel} \frac{\epsilon_o l_{vel}}{d_{vel}} R_f \cdot \frac{j\omega R_{hpf} C_{hpf}}{j\omega R_{hpf} C_{hpf} + 1}. \end{aligned} \quad (4.13)$$

The describing function for a comparator is given by

$$G_D(E) = \frac{4E_N}{\pi E}, \quad (4.14)$$

where  $E_N$  is the comparator output voltage, and  $E$  is the magnitude of the sinusoidal input voltage. For the drive loop comparator,  $E_N$  is effectively given by  $E_N = 15\text{ V}$  once the comparator output is level-shifted accordingly.

Constant-amplitude oscillations may be possible at a frequency  $\omega$  where

$$H(j\omega) G_D(E) = 1. \quad (4.15)$$

The other requirement for limit cycles is more clearly explained graphically. As shown in Figure 4-6 for the drive loop case,  $H(j\omega)$  and  $1/G_D(E)$  are plotted on a gain/phase plot. The intersection of the two curves is where  $H(j\omega) G_D(E) = 1$ . The stability of the system at this point can be examined by perturbing  $E$ . An incremental increase in  $E$  decreases the magnitude of  $G_D(E)$ . Since  $H(j\omega)$  remains constant throughout

the perturbation, the magnitude of  $H(j\omega)G_D(E)$ , the loop transmission, decreases and thus tends to restore  $E$  to its original value. On a practical level, the comparator functions as a variable gain block based on the amplitude  $E$  of the input sinusoid to the comparator. Since  $E$  is restored to its steady-state value upon perturbations, the drive loop can sustain limit cycles. The frequency of oscillation is the frequency at the intersection of the  $H(j\omega)$  and  $1/G_D(E)$  curves, which is given in Figure 4-6 as  $9.16 \times 10^4 \text{ rad/s} \equiv 14.6 \text{ kHz}$ , the resonant frequency of the MEMS system.

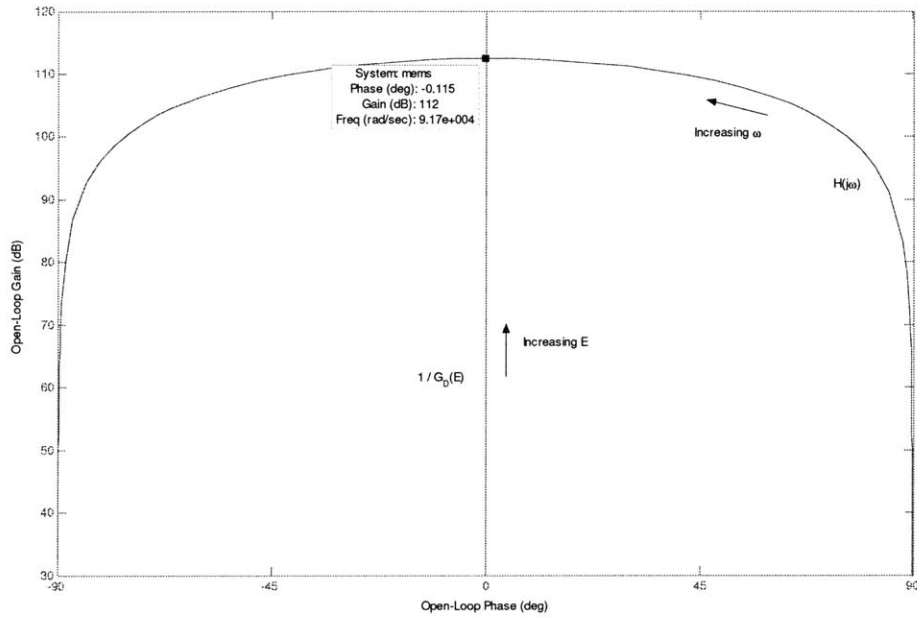


Figure 4-6: Gain/phase plots of  $H(j\omega)$  and  $1/G_D(E)$ .

### 4.3.2 Local Feedback Considerations

The presence of a parasitic capacitance  $C_{p,vel}$  from the  $vel+$  and  $vel-$  electrodes to the underlying substrate was introduced in Section 2.5.3. Although this capacitance was ignored in the previous ideal drive loop analysis, its impact on the stability of the transresistance amplifiers must be considered.

The schematic of the  $C_{vel+}$  transresistance amplifier is given in Figure 4-7 with  $C_{p,vel}$  included. The dynamic, modulating capacitance  $C_{vel+}$  does not lend itself well to linear feedback analysis. However, a workable equivalent model can be derived.

The basic expression for  $i_{vel+}$  is given by

$$\begin{aligned}
 i_{vel+} &= -2N_{vel} V_{BIAS} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{dx_{dyn}(t)}{dt} \\
 &= -2N_{vel} V_{BIAS} \frac{\epsilon_o l_{vel}}{d_{vel}} \frac{d}{dt} \left( x_m \sin(\omega_{res}t) \right) \\
 &= -2N_{vel} V_{BIAS} \frac{\epsilon_o l_{vel}}{d_{vel}} x_m \omega_{res} \cos(\omega_{res}t)
 \end{aligned} \tag{4.16}$$

Noting that  $(\epsilon_o l_{vel}/d_{vel}) x_m \equiv C_{vel,m}$ , an alternative expression for  $i_{vel+}$  is given by

$$i_{vel+} = -2N_{vel} C_{vel,m} \left( V_{BIAS} \omega_{res} \cos(\omega_{res}t) \right). \tag{4.17}$$

The exact same  $i_{vel+}$  can be obtained with the configuration shown in Figure 4-8, where  $C_{vel,m}$  is a static capacitance and  $v_i(t) = -2N_{vel} V_{BIAS} \sin(\omega_{res}t)$ . Now,  $i_{vel+}$  is found using the more familiar expression of

$$i_{vel+} = C_{vel,m} \frac{dv_i(t)}{dt}. \tag{4.18}$$

Note that the non-inverting terminal of the op amp is now at ground potential (both dc and small-signal). With this equivalent model configuration, standard linear superposition techniques (specifically grounding  $v_i$ ) can be applied to determine the composition of the transresistance amplifier feedback loop. This equivalent model is also particularly useful for simulating the MEMS capacitances and surrounding circuitry in a straightforward manner.

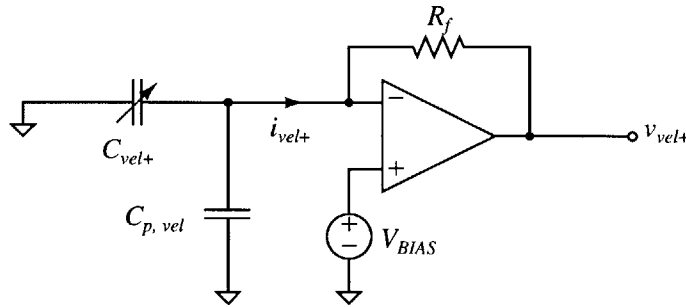


Figure 4-7: Schematic of the  $C_{vel+}$  transresistance amplifier with  $C_{p,vel}$  included.



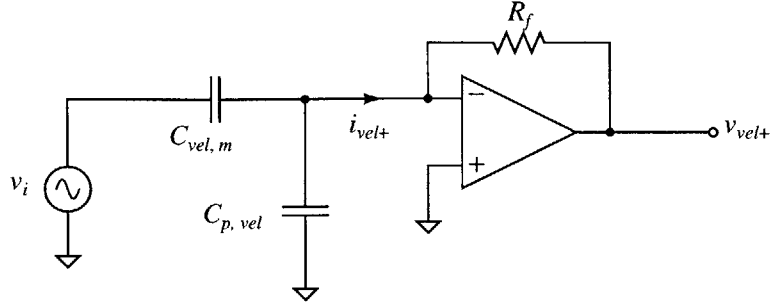


Figure 4-8: Equivalent model of the transresistance amplifier circuit shown in Figure 4-7. This model is suitable for standard linear feedback analysis.

The feedback loop for the circuit is given in Figure 4-9, where  $A(s)$  is the open-loop frequency response of the low-noise op amp covered in Chapter 3. The ideal, incremental input-output relationship for the circuit in Figure 4-9 is given by

$$\frac{V_{vel+}}{V_i}(s) = -sR_fC_{vel,m}. \quad (4.19)$$

However, the inner loop transfer function,  $L(s)$ , contains a pole at

$$f_p = \frac{1}{2\pi R_f (C_{vel,m} + C_{p,vel})} = 760 \text{ kHz}, \quad (4.20)$$

which is nearly an order of magnitude in frequency below the crossover frequency of  $A(s)$ , 7.0 MHz. If  $C_{p,vel}$  were not present, then  $f_p$  would occur at

$$f_p = \frac{1}{2\pi R_f C_{vel,m}} = 17.7 \text{ MHz}, \quad (4.21)$$

and  $L(s)$  could be well-approximated by  $A(s)$ . Nonetheless, the Bode plot of  $L(s)$  including the effects of  $C_{p,vel}$  is given in Figure 4-10. As one can see, the crossover frequency is 1.5 MHz, and the phase margin is only  $20^\circ$ . Although the system is stable, a phase margin of greater than  $45^\circ$  is desirable.

Lead compensation can be implemented in order to improve the phase margin. With the inclusion of capacitor  $C_f$  in parallel with  $R_f$ , as depicted in Figure 4-11, the feedback loop is modified to the form shown in Figure 4-12. The inner loop transfer

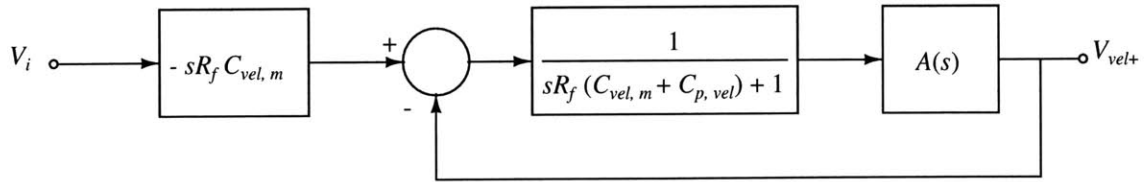


Figure 4-9: Feedback loop for the circuit shown in Figure 4-8.

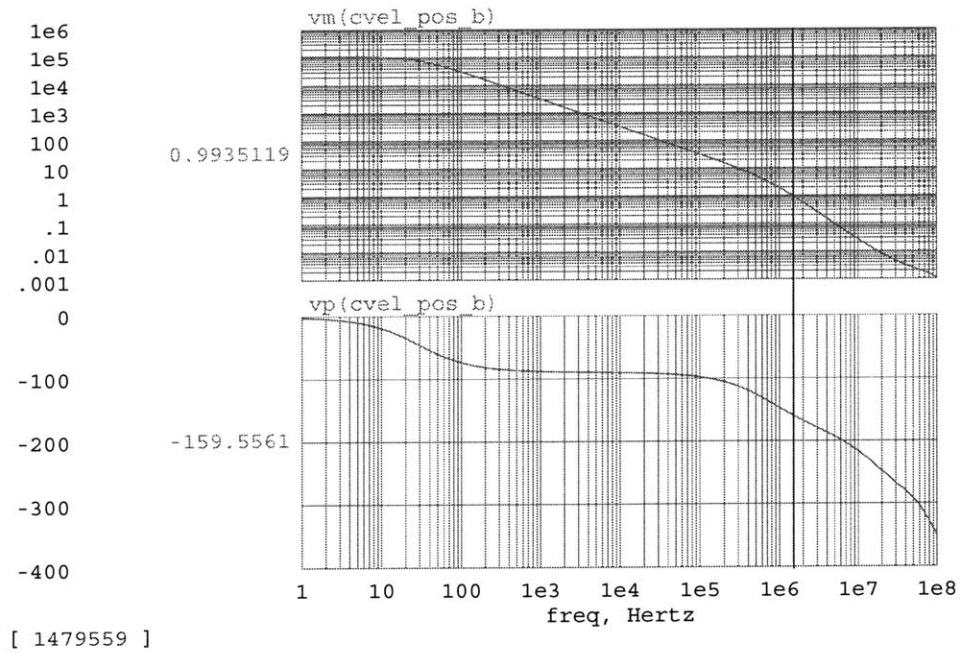


Figure 4-10: Bode plot of the  $L(s)$  shown in Figure 4-9. Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].

function  $L(s)$  now contains a zero at

$$f_z = \frac{1}{2\pi R_f C_f}. \quad (4.22)$$

Setting  $C_f = 600 \text{ fF}$  places the zero at

$$f_z = \frac{1}{2\pi R_f C_f} = 1.3 \text{ MHz}, \quad (4.23)$$

well below the 7.0 MHz crossover frequency of  $A(s)$ . Although the pole in  $L(s)$  is moved to a slightly lower frequency,

$$f_p = \frac{1}{2\pi R_f (C_{vel,m} + C_{p,vel} + C_f)} = 480 \text{ kHz}, \quad (4.24)$$

with the inclusion of  $C_f$ , the stability of the system is greatly improved due to the presence of the zero. The Bode plot of  $L(s)$  in Figure 4-13 illustrates that the crossover frequency remains at 1.5 MHz, while the phase margin is improved to  $60^\circ$ .

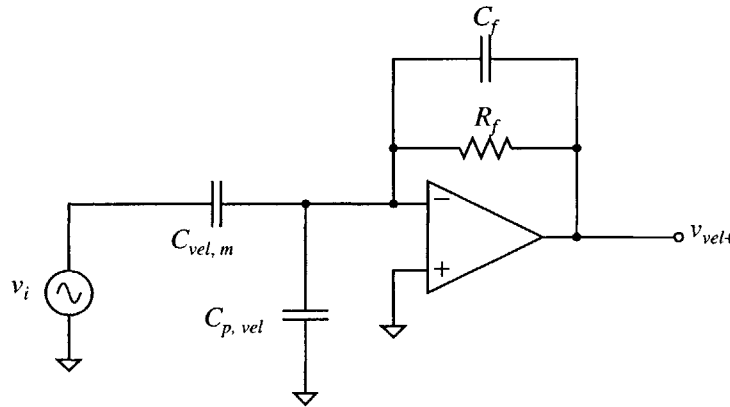


Figure 4-11: Equivalent model of the transresistance amplifier circuit with lead compensation.

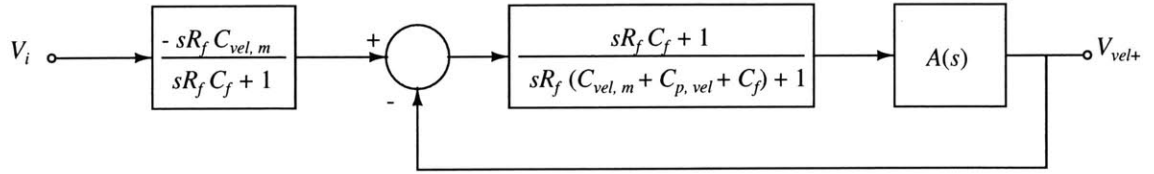


Figure 4-12: Feedback loop for the circuit shown in Figure 4-11.

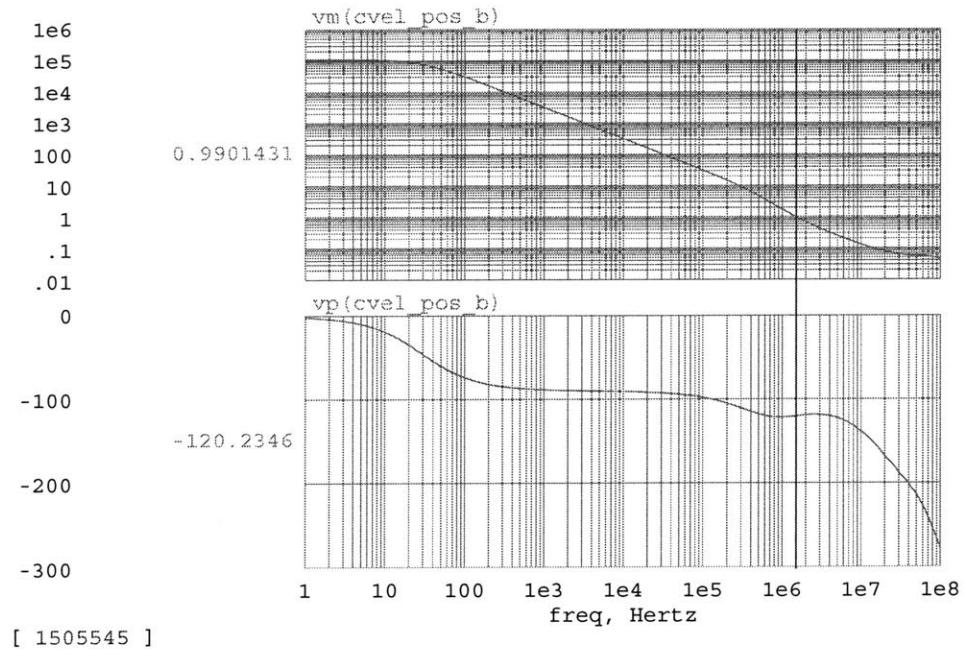


Figure 4-13: Bode plot of the  $L(s)$  shown in Figure 4-12. Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].

## 4.4 Phase Shift at Resonance

Ideally, the force drive waveforms and shutter velocity are perfectly in phase, and the MEMS sensor is driven at its exact resonant frequency. In reality, the finite bandwidths of the amplifiers and the finite response times of the comparator and level shifter lead to a small phase shift between the force drive and shutter velocity. Slight phase contributions at 15 kHz from the high-pass filter and the lead compensation capacitor also add to the total phase shift. An analysis follows of the exact contribution to the total phase shift from each of these sources. The effect of the phase shift on the maximum displacement of the shutter will also be considered.

First, as shown in Figure 4-12, the ideal input-output transfer function of the lead compensated transresistance amplifier is modified to

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_f C_{vel,m}}{sR_f C_f + 1} \quad (4.25)$$

from its uncompensated form of

$$\frac{V_o(s)}{V_i(s)} = -sR_f C_{vel,m}. \quad (4.26)$$

As depicted in the Bode plot of  $V_o(s)$  in Figure 4-14, the combination of the pole in (4.25) at 1.3 MHz and the finite bandwidth of the low-noise op amp leads to a phase of  $89.1^\circ$  at 15 kHz, or a phase shift of  $-0.9^\circ$  from the ideal.<sup>4</sup>

The small-signal  $-3$  dB bandwidth of  $U_3$ , the AD620AN instrumentation amplifier, is 800 kHz when  $G = 10$  [28]. The input-output gain over frequency,  $G(j\omega)$ , can be expressed as

$$G(j\omega) = \frac{10}{j\omega\tau + 1}, \quad (4.27)$$

where

$$\tau = \frac{1}{\omega_{-3\text{dB}}} = \frac{1}{2\pi \cdot 800 \text{ kHz}}. \quad (4.28)$$

---

<sup>4</sup>While (4.25) might suggest that the expected low-frequency phase of  $V_o(s)$  is  $-90^\circ$ , the phase is inverted by  $180^\circ$  because the input waveform  $v_i(t)$  is given by  $v_i(t) = -2N_{vel} V_{BIAS} \sin(\omega_{res}t)$ , which is proportional to  $-\sin(\omega_{res}t)$ .

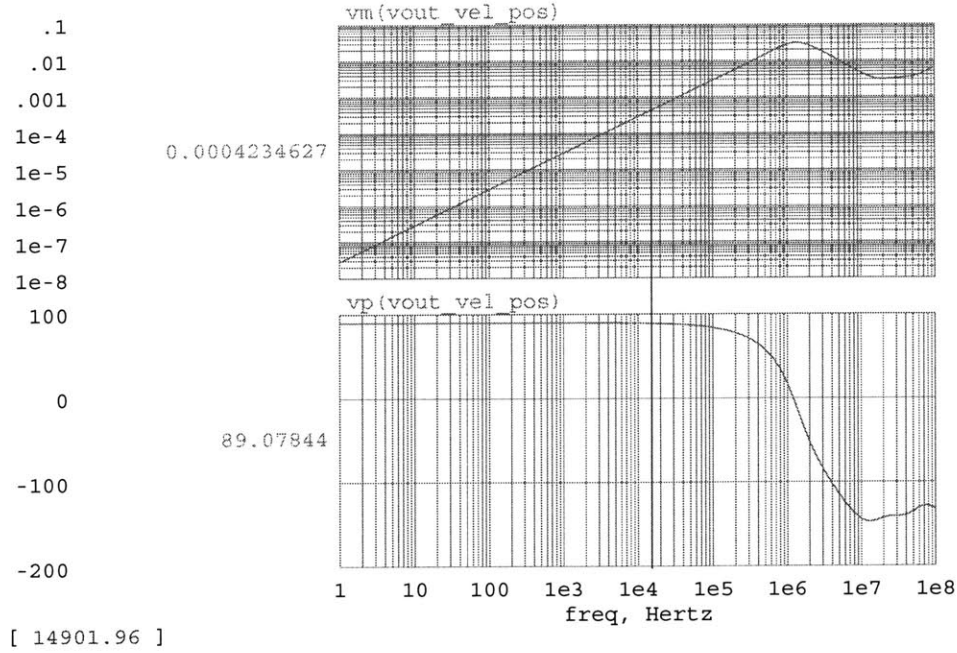


Figure 4-14: Bode plot of  $V_o(s) = -sR_f C_{vel,m} V_i(s)$ . Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].

The resulting phase shift at 15 kHz is given by

$$\angle G(j\omega) = -\arctan(\omega_{res}\tau) = -\arctan\left(\frac{2\pi \cdot 15 \text{ kHz}}{2\pi \cdot 800 \text{ kHz}}\right) = -1.1^\circ. \quad (4.29)$$

The input-output transfer function of the high-pass filter is

$$\frac{V_o}{V_i}(j\omega) = \frac{j\omega R_{hpf} C_{hpf}}{j\omega R_{hpf} C_{hpf} + 1}. \quad (4.30)$$

The residual phase shift at 15 kHz due to the filter is

$$\begin{aligned} \angle \frac{V_o}{V_i}(j\omega) &= 90^\circ - \arctan(\omega R_{hpf} C_{hpf}) \\ &= 90^\circ - \arctan(2\pi \cdot 15 \text{ kHz} \cdot 100\text{k}\Omega \cdot 0.1\mu\text{F}) = +0.1^\circ. \end{aligned} \quad (4.31)$$

The describing function of an ideal comparator has zero phase. However, an actual comparator has a finite response time, which leads to a slight delay between input and output. The AD790AQ comparator  $U_4$  has a maximum response time of 45 ns

[29]. This delay,  $D(j\omega)$ , can be modeled as an exponential of the form

$$D(j\omega) = e^{-j\omega T}, \quad (4.32)$$

where  $T$  is the delay time. For an input signal at a frequency of 15 kHz, the phase shift in degrees due to the delay is

$$\angle D(j\omega) = -\omega T \cdot \frac{180^\circ}{2\pi \text{ rad}} = -2\pi \cdot 15 \text{ kHz} \cdot 45 \text{ ns} \cdot \frac{180^\circ}{2\pi \text{ rad}} = -0.1^\circ. \quad (4.33)$$

Before proceeding to calculate the cumulative phase shift, now is the best time to discuss the details of the comparator hysteresis block originally shown in Figure 4-1. Without any hysteresis, the comparator output  $v_{VEL,COMP}$  would be prone to a series of oscillations following a change in output voltage. These oscillations would result from parasitic feedback paths through stray capacitances [10], [32]. The solution to this problem is to add hysteresis from the comparator output to the non-inverting terminal. The input-output transfer characteristics of one form of hysteresis, referred to as Schmitt trigger hysteresis, are shown in Figure 4-15. For instance, once the comparator output goes high, the input voltage at the inverting terminal must drop below  $-E_M$ , rather than zero, before the comparator output goes low. The describing function for a comparator with Schmitt trigger hysteresis is given by

$$G_D(E) = \frac{4E_N}{\pi E} \angle \arcsin\left(\frac{E_M}{E}\right), \quad (4.34)$$

where  $E_N$  and  $E_M$  are as defined in Figure 4-15, and  $E$  is the amplitude of the input sinusoid. Although this form of hysteresis solves the problem of output oscillations, there is a phase shift between the input sinusoid and the fundamental component of the output due to the memory-based nature of this technique. This phase shift would ultimately contribute to the aggregate phase shift between the force drive and shutter velocity due to the non-idealities of the drive loop.

To overcome this undesirable phase shift, a memoryless hysteresis technique, depicted in Figure 4-16, is implemented. The  $R_{hys}C_{hys}$  network provides a small amount

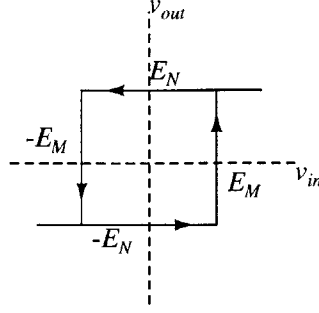


Figure 4-15: Input-output transfer characteristics of Schmitt trigger hysteresis.

of positive feedback between the output and non-inverting terminal. As illustrated in Figure 4-17, when the output voltage goes high to +5 V, the voltage at the non-inverting terminal  $v_{COMP+}$  exponentially decays down to 0 V with a time constant of  $\tau = R_{hys}C_{hys}$ . Output oscillations immediately following a change in the output state are thus prevented. The exact values of  $R_{hys}$  and  $C_{hys}$  are chosen such that  $v_{COMP+}$  decays to approximately 0 V before the next expected output transition half a period later, or

$$5\tau < \frac{1}{2} \cdot \frac{1}{f_{res}} = \frac{1}{2} \cdot \frac{1}{15 \text{ kHz}} = 33 \mu\text{s}, \quad (4.35)$$

or, equivalently,

$$\tau < 6.7 \mu\text{s}. \quad (4.36)$$

Using this guideline, values of  $R_{hys} = 9.1 \text{ k}\Omega$  and  $C_{hys} = 390 \text{ pF}$  were chosen. With this memoryless hysteresis technique, the only phase shift due to the comparator results from its finite response time.

Lastly, the ADG333ABN level-shifter  $U_5$  has a finite response time of 175 ns [30]. Using the delay model presented in (4.32), the resulting phase shift for an input signal of 15 kHz is

$$\angle D(j\omega) = -\omega T \cdot \frac{180^\circ}{2\pi \text{ rad}} = -2\pi \cdot 15 \text{ kHz} \cdot 175 \text{ ns} \cdot \frac{180^\circ}{2\pi \text{ rad}} = -0.5^\circ. \quad (4.37)$$



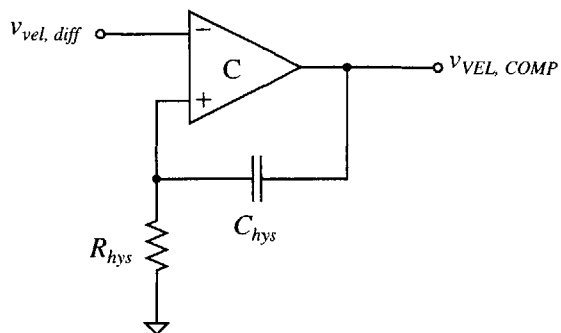


Figure 4-16: Comparator circuit with memoryless hysteresis.

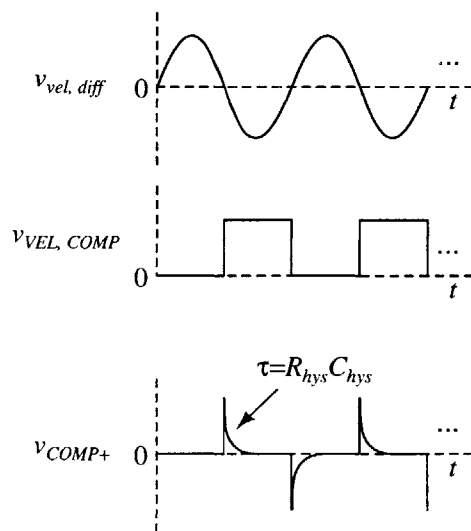


Figure 4-17: Ideal waveforms of  $v_{vel,diff}$ ,  $v_{VEL,COMP}$ , and  $v_{COMP+}$ . After a transition in state of  $v_{VEL,COMP}$ ,  $v_{COMP+}$  decays back to 0V with a time constant of  $\tau = R_{hys}C_{hys}$ .

The sum of all of the drive loop phase shifts is given by

$$\phi_{vel,total} = -0.9^\circ - 1.1^\circ + 0.1^\circ - 0.1^\circ - 0.5^\circ = -2.5^\circ. \quad (4.38)$$

Noting that the high-pass filter contributes a positive phase shift, it is technically possible to modify its frequency characteristics such that it cancels out the negative phase shifts. Maintaining this cancellation over changes in temperature and process variations, however, would be challenging.

In any case, despite the  $-2.5^\circ$  of phase shift between the force drive and shutter velocity, the shutter still reaches near-resonant maximum displacement, owing to the high- $Q$  nature of the MEMS sensor. The  $X/F(s)$  frequency response of the MEMS sensor is again presented in Figure 4-18. At a phase of  $90^\circ - \phi_{vel,total} = 87.5^\circ$ , the magnitude of the frequency response is 12.7 dB, only 0.5 dB off of the resonant peak magnitude of 13.2 dB. Thus, a  $-2.5^\circ$  phase shift leads to only a reduction of

$$1 - \frac{10^{12.7 \text{ dB}/20 \text{ dB}}}{10^{13.2 \text{ dB}/20 \text{ dB}}} = 1 - \frac{4.32}{4.57} = 0.06\% \quad (4.39)$$

in the maximum shutter displacement. The magnitude of the transduced sense current is not significantly reduced, and a high SNR is maintained at the system output.

As will be analyzed in Chapter 5, the sense block circuitry also experiences an input-output phase shift due to the finite bandwidth of its amplifiers. Since  $v_{VEL,COMP}$  is an input to the sense loop, it is noted here that the non-ideal phase shift from the drive loop transresistance amplifiers up to the comparator output is  $-2.0^\circ$ .

## 4.5 Complete Drive Loop Circuit

The schematic for the complete drive loop circuit is given in Figure 4-19. The corresponding component descriptions and values are captured in Table 4.4.

As was stated previously,  $R_{f+}$  and  $R_{f-}$  are thin-film resistors. Capacitors  $C_{f+}$  and  $C_{f-}$  are poly-p<sup>+</sup> capacitors, where the top plate is polysilicon, and the bottom

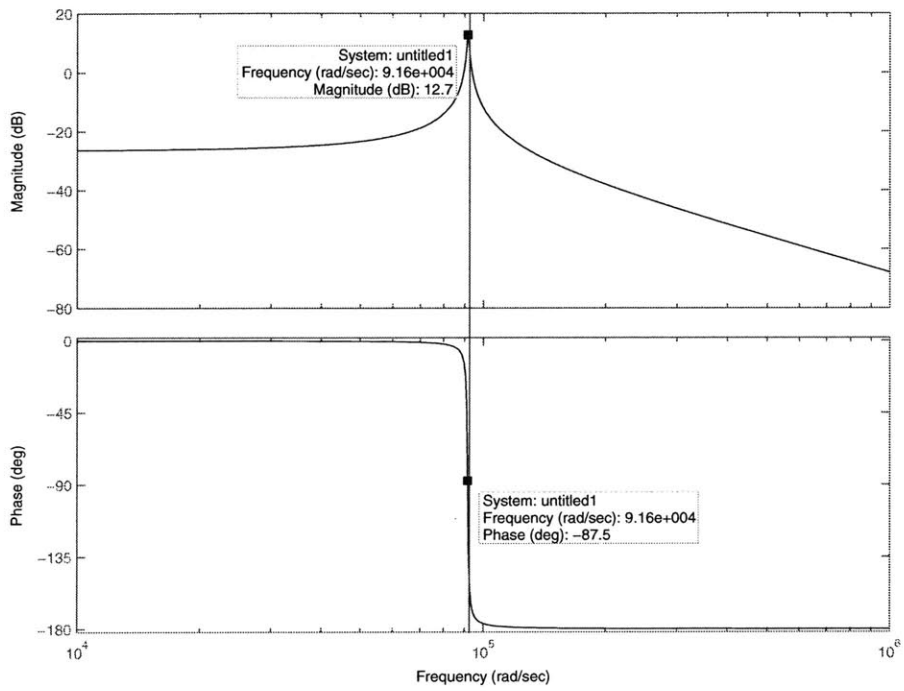


Figure 4-18: Frequency response of the force-to-displacement transfer function of the MEMS sensor.



Parameter	Component Description
$U_1$	Low-Noise Op Amp
$U_2$	Low-Noise Op Amp
$U_3$	AD620AN Instrumentation Amplifier
$U_4$	AD790AQ Comparator
$U_5$	ADG333ABN Quad SPDT Switch
$U_6$	LM78M05CT +5 V Regulator
Parameter	Component Value
$R_{f+}$	200 k $\Omega$
$R_{f-}$	200 k $\Omega$
$R_{hpf}$	100 k $\Omega$
$R_{hys}$	9.1 k $\Omega$
$R_1$	5.49 k $\Omega$
$R_2$	51 $\Omega$
$R_3$	51 $\Omega$
$C_{f+}$	613 fF
$C_{f-}$	613 fF
$C_{hpf}$	0.1 $\mu$ F
$C_{hys}$	390 pF
$C_1$ – $C_5$	10 $\mu$ F
$C_6$ – $C_{10}$	0.1 $\mu$ F

Table 4.4: Component descriptions or values for the complete drive loop circuit shown in Figure 4-19 [28], [29], [30], [33].

plate is a  $p^+$  base diffusion surrounded by an n-well. The n-well is shorted to the  $p^+$  base diffusion to prevent the forward-biasing of the pn junction.

Component  $U_6$  is an LM78M05CT +5 V voltage regulator, which supplies the +5 V required by  $U_4$  for its output high voltage [33]. Resistor  $R_1$  sets the gain of  $U_3$ , the instrumentation amplifier, to  $G = 10$ . Capacitors  $C_1$ – $C_{10}$  are bypass capacitors. All 10  $\mu\text{F}$  capacitors are electrolytic, while the 0.1  $\mu\text{F}$  capacitors are ceramic. Lastly,  $R_2$  and  $R_3$ , in conjunction with  $C_9$  and  $C_{10}$ , respectively, act as low-pass filters to prevent high-frequency oscillations in the  $V_{DD}$  or  $V_{SS}$  rails from reaching the power supply pins of  $U_4$ . Similarly, any high-frequency content on the power supply pins of  $U_4$  is filtered out before coupling to the  $V_{DD}$  or  $V_{SS}$  rails.

## 4.6 Simulation Results

The results of a behavioral, time-domain simulation of the drive loop circuitry are presented in Figure 4-20. Since an accurate model for a modulating MEMS capacitor requires over twenty interconnected behavioral blocks [9], the transresistance amplifier equivalent model introduced in Figure 4-8 is used for compatibility with standard simulation capabilities.

The simulation includes the actual transistor-level implementations of  $U_1$  and  $U_2$ , the low-noise op amps, as well as all elements in the transresistance amplifier feedback loop, including the parasitic capacitance  $C_{p,vel}$ . Capacitances of 22 pF are placed on the outputs of  $U_1$  and  $U_2$  to simulate the effect of the 2 pF input capacitance of the AD620AN instrumentation amplifier  $U_3$ , along with the 10 pF capacitance of an oscilloscope probe. Components  $U_3$  and  $U_4$ , the comparator, are modeled with ideal blocks. The level-shifter  $U_5$  was not included in the simulation because an ideal model for a quad package of SPDT analog switches was not readily available. Even if it were, promising simulation results would not guarantee that the actual IC was properly configured on the PCB. Thus, rather than develop a simulation model for  $U_5$ , it was much more practical to carefully review the ADG333ABN datasheet, analyze the output behavior of  $U_5$  for a given input logic state, and ensure proper wiring on

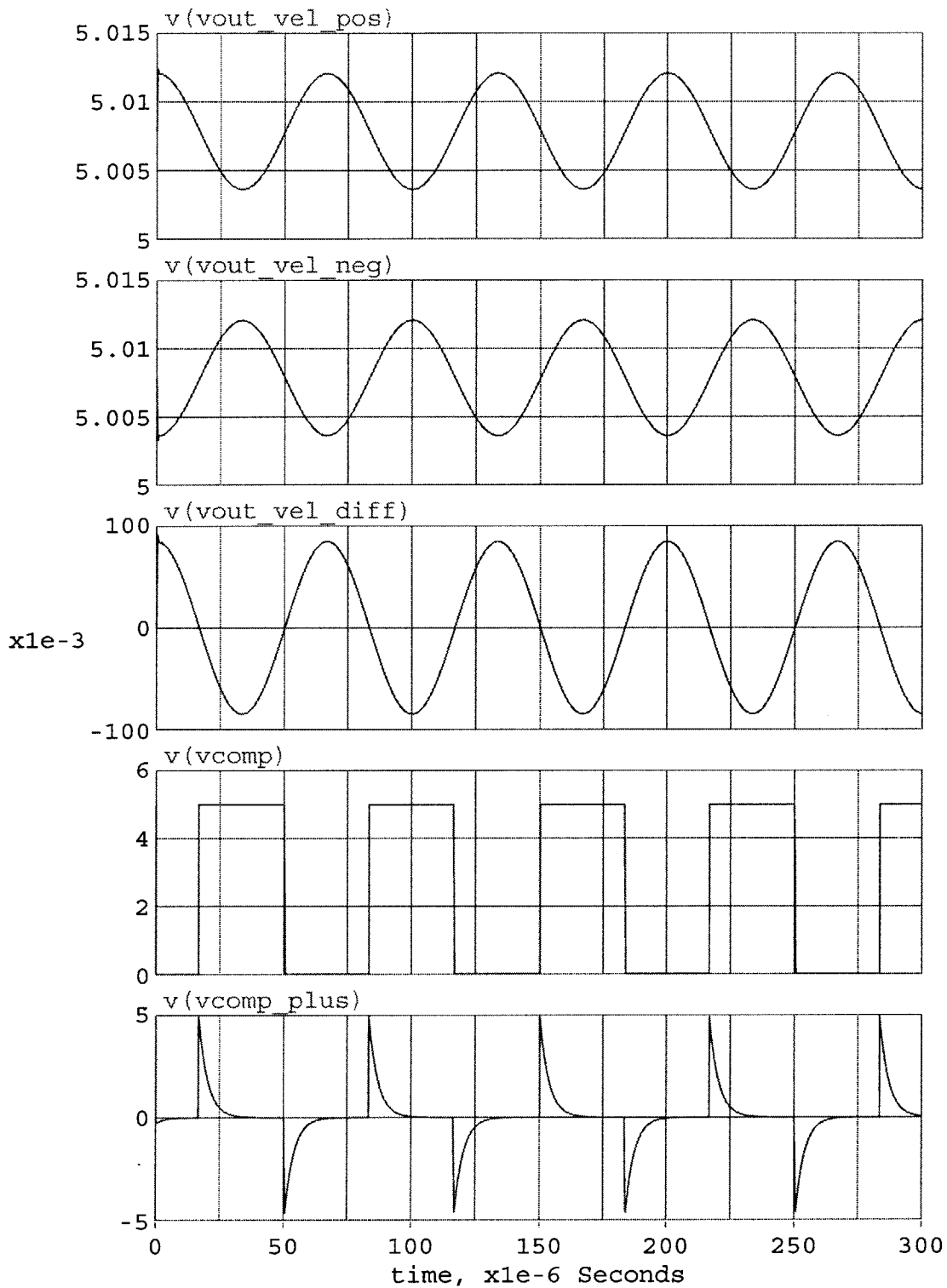


Figure 4-20: Results of a behavioral simulation of the drive loop circuitry. Vertical axis: (top)  $v_{vel+}$  [V], (second from top)  $v_{vel-}$  [V], (third from top)  $v_{vel,diff}$  [mV], (fourth from top)  $v_{VEL,COMP}$  [V], (bottom)  $v_{COMP+}$  [V]. Horizontal axis: Time [ $\mu$ s].

the PCB. The results of the input-output behavioral analysis were given in Table 4.2.

Referring to the equivalent transresistance amplifier model in Figure 4-8, recall that  $v_i$  is proportional to  $\sin(\omega_{res}t)$ , where  $v_i$  represents the shutter displacement,  $x(t)$ . As shown in Figure 4-20,  $v_{vel+}$  is proportional to  $\cos(\omega_{res}t)$ , and thus  $v_{vel+}$  leads  $v_i$  and the shutter displacement by  $90^\circ$ . Thus, as desired,  $v_{vel+}$  and  $dx(t)/dt$ , the shutter velocity, are in phase. Also, the lack of ringing in  $v_{vel+}$  upon system start-up is evidence of the effect of the lead compensation capacitor.

In addition, the effect of the hysteresis  $RC$  network can clearly be seen in the  $v_{COMP+}$  waveform in Figure 4-20. After  $v_{VEL,COMP}$  transitions to its high state,  $v_{COMP+}$  exponentially decays down to 0 V, thus preventing comparator output oscillations following the transition.

## 4.7 Summary

The function of the drive loop is to drive the MEMS sensor at its mechanical resonant frequency. The closed-loop control implementation discussed in this chapter exploits the fact that the force drive waveform and the shutter velocity are in phase only at resonance. Although there is a small phase shift between the force drive and shutter velocity due to component non-idealities, the resulting attenuation of the shutter displacement is negligible, owing to the high- $Q$  nature of the MEMS sensor.

A describing function analysis of the self-resonant loop verified the presence of limit cycles and, thus, the stability of the overall feedback loop. Lead compensation was also implemented to increase the stability of the local transresistance amplifier loops in light of the parasitic capacitances from the  $vel+$  and  $vel-$  electrodes to the substrate.

The results of a time-domain simulation of the drive loop agreed well with the predicted behavior.



# Chapter 5

## Sense Block

### 5.1 Overview

The measurement of the electric field incident on the ESF sensor is performed by the sense block. The sense block converts the dynamic currents generated by  $C_{sense}$  into a dc output voltage that is proportional to the magnitude and polarity of the input electric field. The required sub-blocks include a transimpedance amplifier, a phase shifter, a demodulator, and a low-pass filter. The output of the drive loop comparator also serves as an input to the sense block for phasing purposes.

As discussed in Chapter 1, the two critical performance specifications for the ESF are its input-referred noise and input electric field range. These two metrics must be considered foremost in the design of the sense block.

### 5.2 Ideal Analysis

A simplified schematic of the sense block circuitry is illustrated in Figure 5-1. A description of the component identities or values is given in Table 5.1. Note that all components other than the transimpedance amplifiers are located off-chip on a PCB.

The electric field sense currents  $i_{sense+}$  and  $i_{sense-}$  are generated with the  $C_{sense}$  configuration described in Chapter 2 and are proportional to the input electric field.

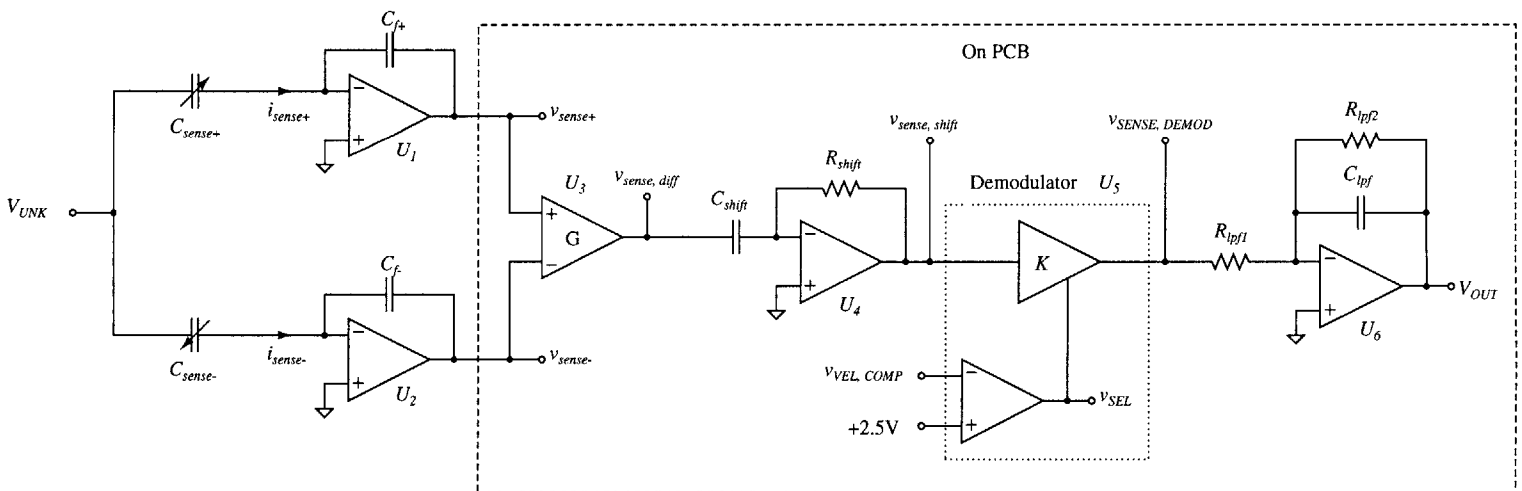


Figure 5-1: Simplified schematic of the sense block circuitry.

Parameter	Component Description
$U_1$	Low-Noise Op Amp
$U_2$	Low-Noise Op Amp
$U_3$	AD620AN Instrumentation Amplifier
$U_4$	AD8065AR FET-Input Op Amp
$U_5$	AD630BD Demodulator
$U_6$	AD8065AR FET-Input Op Amp
Parameter	Component Value
$R_{shift}$	200 k $\Omega$
$R_{lpf1}$	100 k $\Omega$
$R_{lpf2}$	100 k $\Omega$
$C_{f+}$	100 fF
$C_{f-}$	100 fF
$C_{shift}$	10 nF
$C_{lpf}$	0.1 $\mu$ F

Table 5.1: Component descriptions or values for the sense block circuit shown in Figure 5-1 [28], [34], [35].

Expressions for the currents were derived to be:

$$\begin{aligned}
i_{sense+} &= \alpha N_{sense} V_{UNK} \frac{dC_{sense+}}{dt} = \alpha N_{sense} V_{UNK} \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \omega_{res} \cos(\omega_{rest}) \\
&= \alpha V_{UNK} C_{sense,m} \omega_{res} \cos(\omega_{rest}) \quad (5.1)
\end{aligned}$$

$$\begin{aligned}
i_{sense-} &= \alpha N_{sense} V_{UNK} \frac{dC_{sense-}}{dt} = -\alpha N_{sense} V_{UNK} \frac{\epsilon_o l_{sense}}{d_{sense}} x_m \omega_{res} \cos(\omega_{rest}) \\
&= -\alpha V_{UNK} C_{sense,m} \omega_{res} \cos(\omega_{rest}). \quad (5.2)
\end{aligned}$$

The currents are converted to voltages  $v_{sense+}$  and  $v_{sense-}$  by the transimpedance amplifiers. The voltages are given by:

$$\begin{aligned}
v_{sense+} &= -i_{sense+} Z(s) = -i_{sense+} \frac{1}{sC_{f+}} \\
&\equiv \int -\alpha V_{UNK} \frac{C_{sense,m}}{C_{f+}} \omega_{res} \cos(\omega_{rest}) dt \\
&= -\alpha V_{UNK} \frac{C_{sense,m}}{C_{f+}} \sin(\omega_{rest}) \quad (5.3)
\end{aligned}$$

$$\begin{aligned}
v_{sense-} &= -i_{sense-} Z(s) = -i_{sense-} \frac{1}{sC_{f-}} \\
&\equiv \int \alpha V_{UNK} \frac{C_{sense,m}}{C_{f-}} \omega_{res} \cos(\omega_{rest}) dt \\
&= \alpha V_{UNK} \frac{C_{sense,m}}{C_{f-}} \sin(\omega_{rest}). \quad (5.4)
\end{aligned}$$

The transimpedance amplifiers, as the front-end of the sense block circuitry, must serve as low-noise current-to-voltage converters for optimal input-referred noise. The low-noise op amp covered in Chapter 3 was designed specifically for this purpose.

In addition, the capacitors  $C_{f+}$  and  $C_{f-}$  were selected as the feedback elements rather than resistors for a lower input-referred noise. Resistors have an equivalent voltage noise spectral density of

$$V_{n,r}^2(f) = 4kTR \quad (5.5)$$

while capacitors are noiseless elements [15]. Nonetheless, although capacitors are noiseless, using capacitors as feedback elements requires additional measures, as will be discussed in Section 5.3.1. Two competing considerations exist regarding the sizing of  $C_{f+}$  and  $C_{f-}$ . First, as shown in (5.3) and (5.4), a smaller  $C_{f+}$  and  $C_{f-}$  results in a larger  $v_{sense+}$  and  $v_{sense-}$ , and, thus, a larger SNR. However,  $C_{f+}$  and  $C_{f-}$  cannot be made so small that the exact capacitance is not accurately known, and  $C_{f+}$  does not equal  $C_{f-}$ . With both of these considerations in mind,  $C_{f+}$  and  $C_{f-}$  were set at 100 fF [17].

An instrumentation amplifier  $U_3$  then performs a differential-to-single-ended conversion and outputs

$$\begin{aligned} v_{sense,diff} = G(v_{sense+} - v_{sense-}) &= G \left( -2\alpha V_{UNK} \frac{C_{sense,m}}{C_f} \sin(\omega_{rest}) \right) \\ &\equiv -2G\alpha V_{UNK} \frac{C_{sense,m}}{C_f} \sin(\omega_{rest}), \end{aligned} \quad (5.6)$$

where  $G$  represents the gain of the instrumentation amplifier, and  $C_f = C_{f+} = C_{f-}$ . A gain of  $G = 1$  is selected for output voltage swing considerations, so  $v_{sense,diff}$  simplifies to

$$v_{sense,diff} = -2\alpha V_{UNK} \frac{C_{sense,m}}{C_f} \sin(\omega_{rest}). \quad (5.7)$$

The voltage  $v_{sense,diff}$  is then passed through a  $-90^\circ$  phase shifter, the output of which is denoted by  $v_{sense,shift}$ . The purpose of the phase shifter will be discussed shortly when the demodulator is covered. The input-output transfer function is given by

$$\frac{V_{sense,shift}(s)}{V_{sense,diff}(s)} = -sR_{shift}C_{shift}. \quad (5.8)$$

The values of  $R_{shift} = 1 \text{ k}\Omega$  and  $C_{shift} = 10 \text{ nF}$  are chosen such that  $|V_{sense,shift}(s)/V_{sense,diff}(s)| \approx 1$  at 15 kHz. As desired, the output is phase shifted by  $-90^\circ$  with respect to the input at 15 kHz (and at all frequencies). Thus,  $v_{sense,shift}$  is given in the time-domain by

$$v_{sense,shift} = -2\alpha V_{UNK} \frac{C_{sense,m}}{C_f} \sin(\omega_{rest} - 90^\circ)$$

$$= -2\alpha V_{UNK} \frac{C_{sense,m}}{C_f} \cos(\omega_{rest}). \quad (5.9)$$

The demodulator  $U_5$  acts as a voltage-dependent gain block [35]. The output of the demodulator  $v_{SENSE,DEMODO}$  is given by

$$v_{SENSE,DEMODO} = K v_{sense,shift}, \quad (5.10)$$

where  $K$  is the gain of the demodulator. The value of  $K$  for a given input is based on the output of a comparator internal to  $U_5$ . As shown in Figure 5-1, the inverting terminal of the comparator is connected to  $v_{VEL,COMP}$ , the drive loop voltage, and the non-inverting terminal is connected to +2.5 V. When  $v_{VEL,COMP}$  is low (0 V), the output of the  $U_5$  internal comparator,  $v_{SEL}$ , is high and  $K = +2$ . On the other hand, when  $v_{VEL,COMP}$  is high (+5 V),  $v_{SEL}$  is low and  $K = -2$ . The corresponding waveforms for the case when  $V_{UNK} > 0$  V are presented in Figure 5-2. As one can see, the effect of the demodulator on  $v_{sense,shift}$  is to multiply it by +2 when  $v_{sense,shift} < 0$ , and multiply it by -2 when  $v_{sense,shift} > 0$ . The resulting  $v_{SENSE,DEMODO}$  is a unipolar series of half-sinusoids. Also, the role of the  $-90^\circ$  phase shifter is now apparent from Figure 5-2 — the phase shifter shifts  $v_{sense,diff}$  by  $-90^\circ$  to align it with  $v_{VEL,COMP}$ .

Before the demodulation, the peak  $v_{sense,shift}$  voltage, denoted as  $V_{SENSE,SHIFT,PK}$ , was

$$V_{SENSE,SHIFT,PK} = -2\alpha V_{UNK} \frac{C_{sense,m}}{C_f}. \quad (5.11)$$

After the demodulation, the peak  $v_{SENSE,DEMODO}$  voltage, denoted as  $V_{SENSE,DEMODO,PK}$ , is given by

$$V_{SENSE,DEMODO,PK} = 2 \left( -2\alpha V_{UNK} \frac{C_{sense,m}}{C_f} \right) = -4\alpha V_{UNK} \frac{C_{sense,m}}{C_f}. \quad (5.12)$$

As can be seen in Figure 5-2,  $v_{SENSE,DEMODO}$  is composed of a dc component and a  $2 \cdot 15 \text{ kHz} = 30 \text{ kHz}$  component. The dc component, notated as  $V_{SENSE,DEMODO,DC}$ , is found by integrating one of the half-sinusoids over its period and then dividing by period. This operation is equivalent to integrating  $+4\alpha V_{UNK} (C_{sense,m}/C_f) \cos(\omega_{rest}t)$

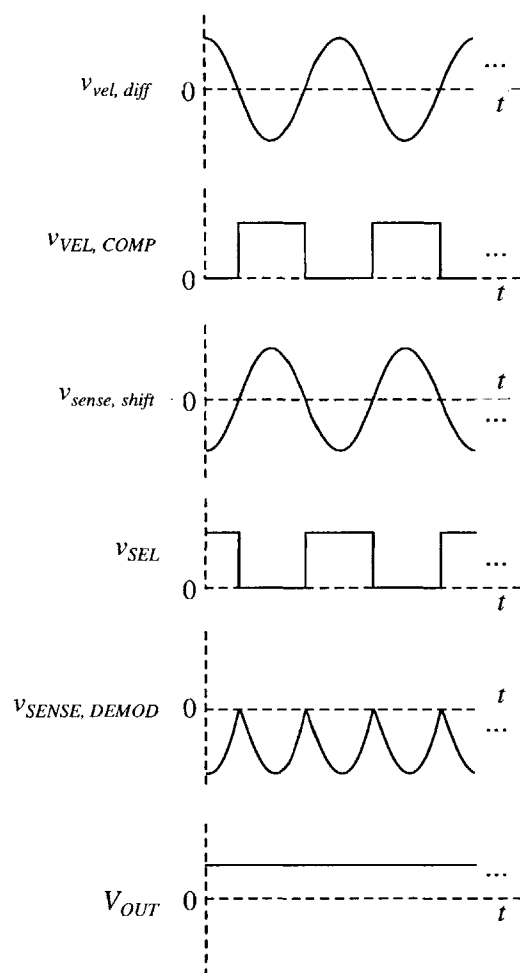


Figure 5-2: Ideal waveforms for key sense block voltages. The voltage  $v_{SENSE, DEMOD}$  is a series a half-sinusoids with a frequency of 30 kHz, and  $V_{OUT}$  is a dc voltage proportional to the amplitude of  $v_{sense, shift}$ .

over  $\pi/2 < \phi < 3\pi/2$  and dividing by  $\pi$ :

$$\begin{aligned}
V_{SENSE,DEM,DC} &= \frac{1}{\pi} \int_{\pi/2}^{3\pi/2} +4\alpha V_{UNK} \frac{C_{sense,m}}{C_f} \cos(\omega_{rest}t) d\phi \\
&= \frac{+4\alpha V_{UNK}}{\pi} \frac{C_{sense,m}}{C_f} \int_{\pi/2}^{3\pi/2} \cos(\omega_{rest}t) d\phi \\
&= \frac{+4\alpha V_{UNK}}{\pi} \frac{C_{sense,m}}{C_f} [\sin(3\pi/2) - \sin(\pi/2)] \\
&= \frac{-8\alpha V_{UNK}}{\pi} \frac{C_{sense,m}}{C_f}.
\end{aligned} \tag{5.13}$$

Note that the integrated signal is  $+4\alpha V_{UNK} (C_{sense,m}/C_f) \cos(\omega_{rest}t)$  because this signal is negative between  $\phi = \pi/2$  and  $\phi = 3\pi/2$ .

The only remaining operation is to attenuate the 30 kHz component of  $v_{SENSE,DEM,DC}$ , and that is the purpose of the low-pass filter shown in Figure 5-1. The input-output transfer function of the filter is given by

$$\frac{V_{out}}{V_{sense,demod}}(s) = -\frac{R_{lpf2}}{R_{lpf1}} \frac{1}{sR_{lpf2}C_{lpf} + 1}. \tag{5.14}$$

For simplicity, a gain of  $|V_{out}/V_{sense,demod}| \approx 1$  is desired at dc; therefore,  $R_{lpf1}$  and  $R_{lpf2}$  are set to the same resistance. The selection of the exact values of  $R_{lpf1}$ ,  $R_{lpf2}$ , and  $C_{lpf}$  is more involved. Two competing considerations exist for the component value selection. Setting the  $-3$  dB bandwidth,

$$f_{-3dB} = \frac{1}{2\pi R_{lpf2}C_{lpf}}, \tag{5.15}$$

as low as possible results in the greatest attenuation of the 30 kHz component. However, a lower  $f_{-3dB}$  corresponds to a slower response time to a change in  $V_{UNK}$ , since the time constant of the filter is

$$\tau = R_{lpf2}C_{lpf}. \tag{5.16}$$

A compromise between these two considerations is achieved by selecting  $R_{lpf1} = 100$  k $\Omega$ ,  $R_{lpf2} = 100$  k $\Omega$ , and  $C_{lpf} = 0.1$   $\mu$ F, which results in  $f_{-3dB} = 15.9$  Hz and



$\tau = 10\text{ms}$ . At 30 kHz, the magnitude of  $V_{out}(j\omega)/V_{sense,demod}(j\omega)$  is

$$\left| \frac{V_{out}}{V_{sense,demod}}(j\omega) \right| = \frac{R_{lpf2}}{R_{lpf1}} \frac{1}{\omega R_{lpf2} C_{lpf} + 1} = -65.5 \text{ dB} \quad (5.17)$$

Thus, the 30 kHz component is sufficiently attenuated, and the output voltage of the filter, and the entire system, is given by

$$V_{OUT} = -\frac{R_{lpf2}}{R_{lpf1}} \cdot V_{SENSE,DEMODO,DC} = \frac{8 \alpha V_{UNK}}{\pi} \frac{C_{sense,m}}{C_f}. \quad (5.18)$$

As desired from the outset of this thesis, the output of the ESF system is a dc voltage proportional to  $V_{UNK}$ , and, thus, to the input electric field. The constant of proportionality is

$$\frac{V_{OUT}}{V_{UNK}} = \frac{8 \alpha}{\pi} \frac{C_{sense,m}}{C_f} = 7.13 \times 10^{-3}. \quad (5.19)$$

## 5.3 Local Feedback Considerations

### 5.3.1 Transimpedance Amplifier

As shown in Figure 5-3, a parasitic capacitance  $C_{p,sense}$  is present from the inverting terminal of the transimpedance amplifier op amp to ground. Similarly to the case of the transresistance amplifier and  $C_{p,vel}$  discussed in Section 4.3.2, an equivalent model of the transimpedance amplifier can be derived for purposes of feedback analysis. Noting that  $i_{sense+}$  is given by

$$i_{sense+} = \alpha V_{UNK} C_{sense,m} \omega_{res} \cos(\omega_{res} t), \quad (5.20)$$

the exact same  $i_{sense+}$  can be obtained with the circuit shown in Figure 5-4. Now,  $C_{sense,m}$  is a static capacitance, and  $v_i(t) = \alpha V_{UNK} \sin(\omega_{res} t)$ . The feedback loop for this equivalent model is shown in block diagram form in Figure 5-5, where  $A(s)$  is the open-loop frequency response of the low-noise op amp. Unlike the case with  $C_{p,vel}$  and the transresistance amplifier of the drive loop,  $C_{p,sense}$  does not create a pole in

$L(s)$  and, thus, does not reduce the stability of the loop. The Bode plot of  $L(s)$  is shown in Figure 5-6. The unity-gain bandwidth is 84.6 kHz, while the phase margin is 89.1°. Note that the  $L(s)$  unity-gain frequency is much lower than the unity-gain frequency of the op amp due to the  $C_f / (C_{sense,m} + C_{p,sense} + C_f) = 0.023$  factor in  $L(s)$ .

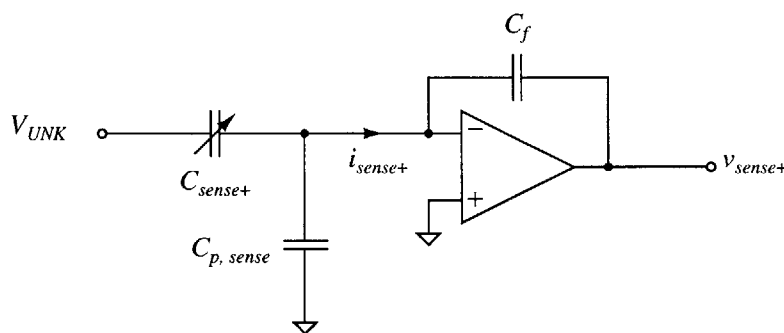


Figure 5-3: Schematic of the  $C_{sense+}$  transimpedance amplifier with  $C_{p,sense}$  included.

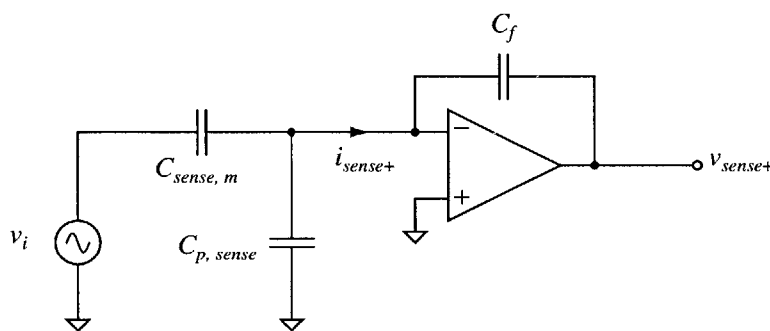


Figure 5-4: Equivalent model of the transimpedance amplifier circuit shown in Figure 5-3. This model is suitable for standard linear feedback analysis.

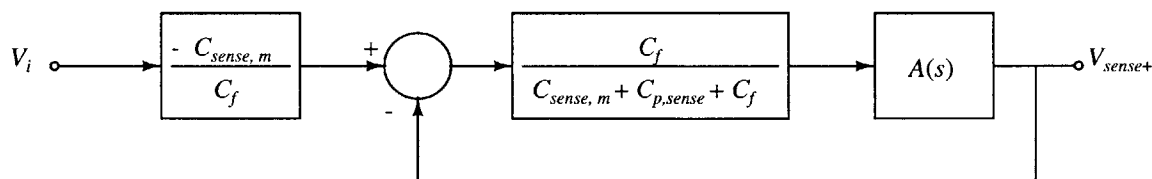


Figure 5-5: Feedback loop for the circuit shown in Figure 5-4.

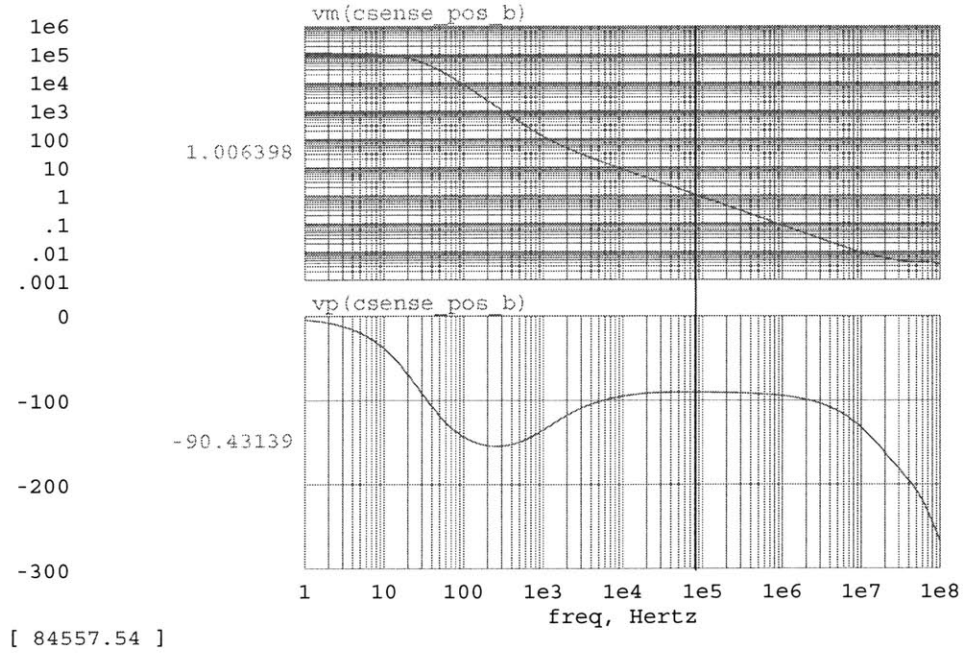


Figure 5-6: Bode plot of the  $L(s)$  shown in Figure 5-5. Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].

Nonetheless, a feedback consideration with the transimpedance amplifier must be addressed. In the ideal analysis of the sense block, it was assumed that  $v_{sense+}$  had no dc component. In reality, with a capacitor in the feedback loop, this will not be the case because there is no dc feedback to set the dc bias point of  $v_{sense+}$ , denoted as  $V_{SENSE+,DC}$ . With no dc feedback, the leakage current of the op amp input transistors will slowly charge  $C_f$  and will eventually cause  $V_{SENSE+,DC}$  to reach the upper or lower saturation limits of the op amp.

One method of overcoming this problem and regulating  $V_{SENSE+,DC}$  to suitable levels relies on including diode-connected transistors in the feedback loop to clamp the dc output voltage [17]. As illustrated in Figure 5-7, diode-connected NFETs are connected in parallel with  $C_f$ . They are arranged in a reverse-parallel configuration. The dc output level,  $V_{SENSE+,DC}$ , is now effectively clamped to between two diode drops above or below zero, or

$$-V_{GS,M1} - V_{GS,M2} < V_{SENSE+,DC} < V_{GS,M3} + V_{GS,M4}. \quad (5.21)$$

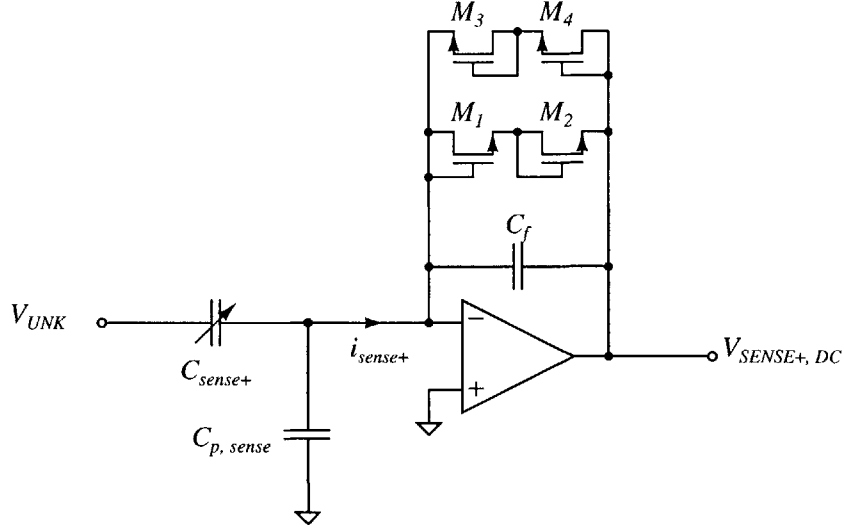


Figure 5-7: Schematic of the transimpedance amplifier with diode-connected NFETs for dc feedback.

The precise dc level will be determined by the magnitudes of the leakage currents of  $M_1$ – $M_4$  and the input transistors of the op amp.

Also, with only leakage current flowing through  $M_1$ – $M_4$ , their incremental resistances will be large, since the incremental resistance of a diode,  $r_d$ , is inversely proportional to its dc current,  $I_D$ . Specifically,  $r_d$  is given by

$$r_d = \frac{kT}{qI_D}. \quad (5.22)$$

The simulated incremental resistance for each of the transistors was given as  $\sim 10^{11} \Omega$  in ADICE. At 15 kHz, the impedance of  $C_f$  is

$$\frac{1}{\omega C_f} = \frac{1}{2\pi \cdot 15 \text{ kHz} \cdot 100 \text{ fF}} = 10^8 \Omega, \quad (5.23)$$

which is multiple orders of magnitude below  $10^{11} \Omega$ . Thus, as desired,  $C_f$  will determine input-output gain of the transimpedance amplifier. Note that, while  $r_d$  is a large resistance, it is used only for small-signal modeling purposes and does not contribute any thermal noise [15].

While the simulation results of the transimpedance amplifier with the diode-

connected NFETs were very promising, a back-up plan was suggested in case this technique did not work as expected [17]. As shown in Figure 5-8, an NFET that acts as a reset switch is placed in parallel with  $C_f$ . Since the source of  $M_5$  is at virtual ground,  $M_5$  will be on whenever  $V_{RESET} > V_{T,M5}$ . A possible  $V_{RESET}$  waveform is illustrated in Figure 5-9. The gate of  $M_5$  is driven high to a voltage  $V_{RESET,HIGH}$  for a fraction of a period to discharge  $C_f$ . Since this reset switch technique was only intended as a back-up measure, the exact frequency and duty-cycle of  $V_{RESET}$  necessary for proper operation were left to be determined experimentally.

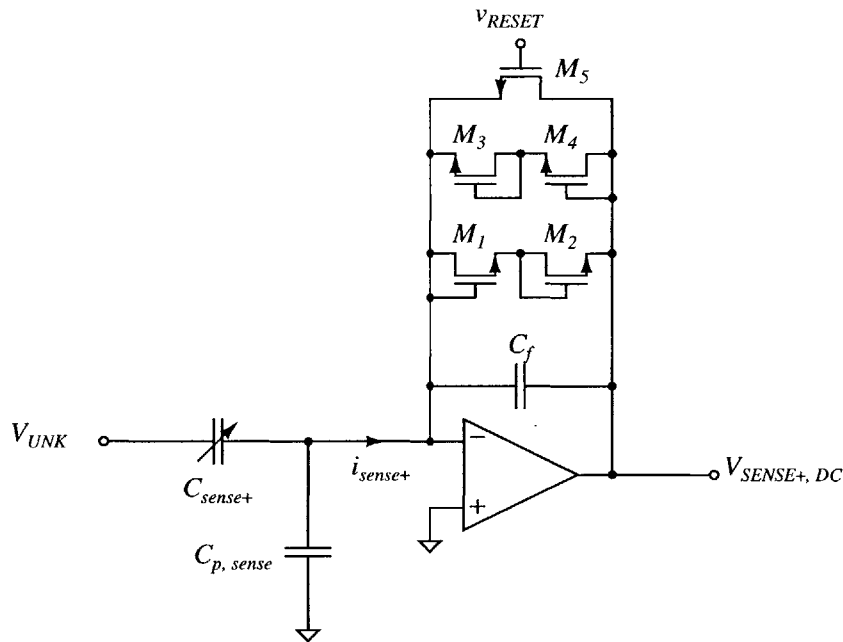


Figure 5-8: Schematic of the transimpedance amplifier with diode-connected NFETs and a reset switch NFET.

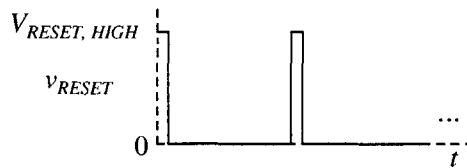


Figure 5-9: One possible  $v_{RESET}$  waveform, with brief pulses to  $V_{RESET,HIGH}$  to discharge  $C_f$ .

Nonetheless, designing at the integrated-circuit-level does not allow a loop stability

analysis with the reset switch to similarly be deferred for experimental evaluation. The incremental resistance of an NMOS transistor in the triode region is given by

$$r_{ds} = \frac{1}{\mu_n C_{ox} (W/L) (V_{GS} - V_T)}, \quad (5.24)$$

where  $\mu_n$  is the mobility of electrons,  $C_{ox}$  is the gate capacitance per unit area, and  $V_T$  is the threshold voltage of the transistor. Also, the channel charge of a transistor in the triode region is given by

$$Q_{CH} = -WLC_{ox} (V_{GS} - V_T). \quad (5.25)$$

In order to minimize any errors due to charge injection,  $M_5$  is sized at  $W/L = 5/4$ , the smallest transistor available in the iMEMS process. The incremental resistance of  $M_5$  in the triode region is

$$\begin{aligned} r_{M5} &= \frac{1}{\mu_n C_{ox} (W/L) (V_{GS} - V_T)} \\ &= \frac{1}{0.06 \text{ m}^2/\text{Vs} \cdot 476 \times 10^{-6} \text{ F/m}^2 \cdot (5/4) \cdot (V_{GS} - 1.83 \text{ V})}. \end{aligned} \quad (5.26)$$

The incremental transimpedance amplifier circuit including  $r_{M5}$  is shown in Figure 5-10. The incremental resistances of the diode-connected transistors  $M_1$ – $M_4$  are ignored due to their extremely large ( $\sim 10^{11} \Omega$ ) resistances. The feedback loop for this circuit is presented in Figure 5-11, where  $A(s)$  is the open-loop frequency response of the low-noise op amp. The inner-loop transfer function  $L(s)$  contains a pole at

$$f_p = \frac{1}{2\pi r_{M5}(C_{p,sense} + C_f)}, \quad (5.27)$$

and a zero at

$$f_z = \frac{1}{2\pi r_{M5}C_f}. \quad (5.28)$$

The pole at  $f_p$  can potentially lead to an unstable or weakly stable system.

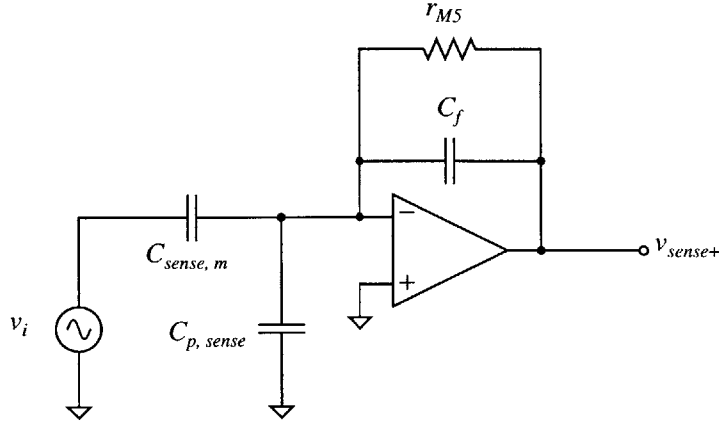


Figure 5-10: Equivalent small-signal model of the transimpedance amplifier with the reset switch NFET.

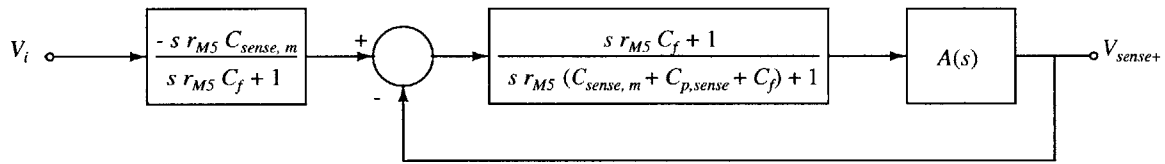


Figure 5-11: Feedback loop for the circuit shown in Figure 5-10.

For  $V_{RESET,HIGH} = 2\text{ V}$ ,  $r_{M5}$  is  $165\text{ k}\Omega$  according to (5.26). The pole in  $L(s)$  is located at  $f_p = 224\text{ kHz}$ , while the zero is at  $f_z = 9.6\text{ MHz}$ . Recall that the unity-gain bandwidth of the op amp is  $7.0\text{ MHz}$ . The Bode plot of  $L(s)$  is shown in Figure 5-12. As expected, since the pole is at such a low frequency, and the zero is beyond the unity-gain frequency of the op amp, the phase margin is a poor  $16.1^\circ$ .

Since  $M_5$  was already in the middle of the IC layout when the reset switch stability issue was considered, significantly modifying the size of  $M_5$  was not an option. However, by increasing  $V_{RESET,HIGH}$  to  $10\text{ V}$ ,  $r_{M5}$  decreases to  $3.4\text{ k}\Omega$ , and  $f_p$  moves to  $10.9\text{ MHz}$ , beyond the  $7.0\text{ MHz}$  op-amp unity-gain frequency. The Bode plot of  $L(s)$  with  $V_{RESET,HIGH} = 10\text{ V}$  is shown in Figure 5-13. The unity-gain frequency is  $2.7\text{ MHz}$ , and the phase margin improves to a reasonable  $46.7^\circ$ .

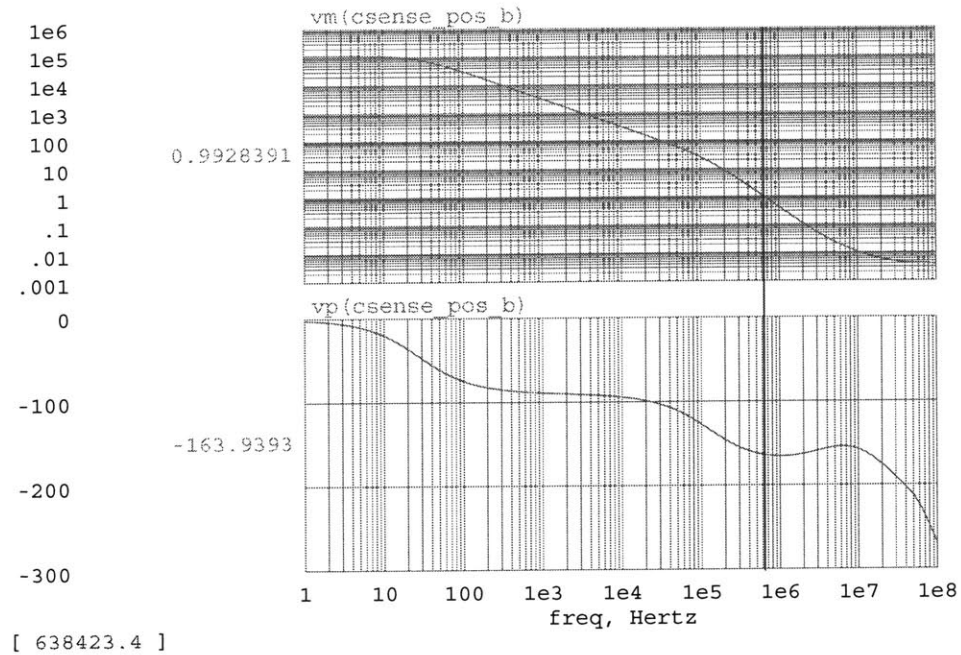


Figure 5-12: Bode plot of the  $L(s)$  shown in Figure 5-11 when  $V_{RESET,HIGH} = 2V$ . Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].

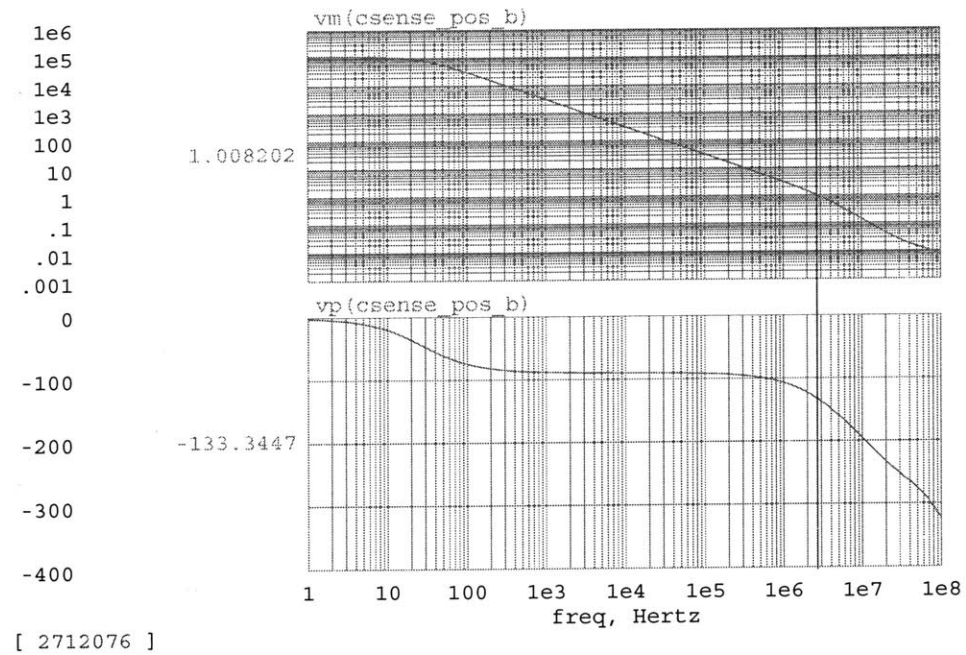


Figure 5-13: Bode plot of the  $L(s)$  shown in Figure 5-11 when  $V_{RESET,HIGH} = 10V$ . Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].



### 5.3.2 The $-90^\circ$ Phase Shifter

The ideal  $-90^\circ$  phase shifter circuit is repeated in Figure 5-14. The feedback loop for the phase shifter is given in Figure 5-15. The open-loop frequency response of the AD8065AR, the op amp used in the actual implementation, is represented by  $A(s)$ . Based on information available in the AD8065AR datasheet, an approximate representation for  $A(s)$  is

$$A(s) = \frac{4.5 \times 10^5}{(s/(2\pi \cdot 220 \text{ Hz}) + 1) (s/(2\pi \cdot 100 \text{ MHz}) + 1)} \quad (5.29)$$

[34]. The unity-gain frequency of the AD8065AR is approximately 60 MHz. The Bode plot of  $L(s)$  is presented in Figure 5-16. The phase margin is only  $0.01^\circ$ . As one can see, the pole in  $L(s)$  at

$$f_p = \frac{1}{2\pi R_{shift1} C_{shift1}} = 15.9 \text{ kHz} \quad (5.30)$$

seriously degrades the stability of the system.

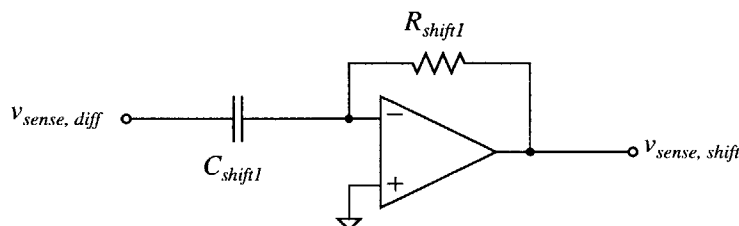


Figure 5-14: Schematic of the ideal  $-90^\circ$  phase shifter circuit.

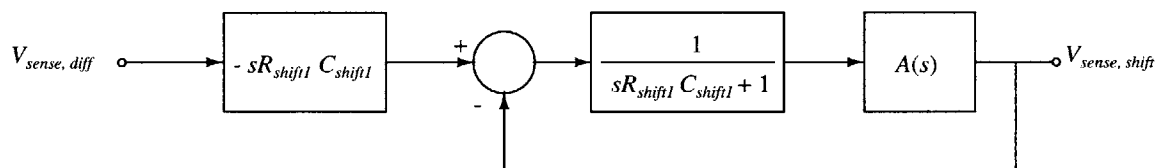


Figure 5-15: Feedback loop for the circuit shown in Figure 5-14.

Nonetheless, a form of lead compensation, depicted in Figure 5-17, can improve the phase margin of  $L(s)$  [31]. Adding a small-value resistor  $R_{shift2}$  in series with

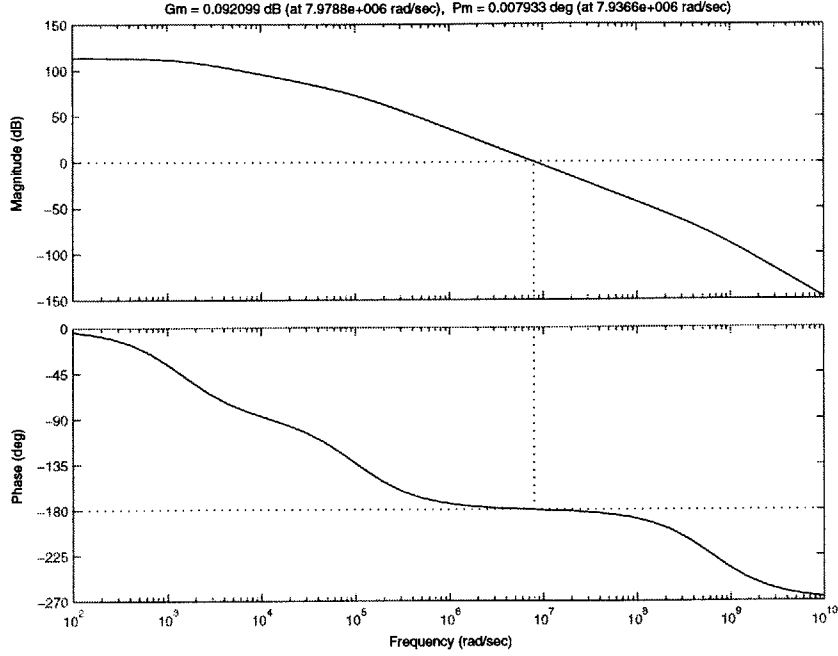


Figure 5-16: Bode plot of the  $L(s)$  shown in Figure 5-15.

$C_{shift1}$  results in the modified feedback loop shown in Figure 5-18. A zero at

$$f_z = \frac{1}{2\pi R_{shift2} C_{shift1}} \quad (5.31)$$

now exists in  $L(s)$  with the potential of increasing the stability of the loop. The ideal input-output transfer function is also modified to

$$\frac{V_{sense,shift}}{V_{sense,diff}}(s) = \frac{-sR_{shift1}C_{shift1}}{sR_{shift2}C_{shift1} + 1}. \quad (5.32)$$

The value of  $R_{shift2}$  must be chosen such that the zero in  $L(s)$  improves the phase margin, while, at the same time, the pole due to  $R_{shift2}$  in the ideal transfer function does not contribute any undesirable phase shift at 15 kHz. With these guidelines in mind,  $R_{shift2}$  is set to 15  $\Omega$ .

Lastly, as shown in Figure 5-19, a capacitor  $C_{shift2}$  is placed in parallel with  $R_{shift1}$ . The addition of  $C_{shift2} = 20$  pF creates a high-frequency pole that limits the

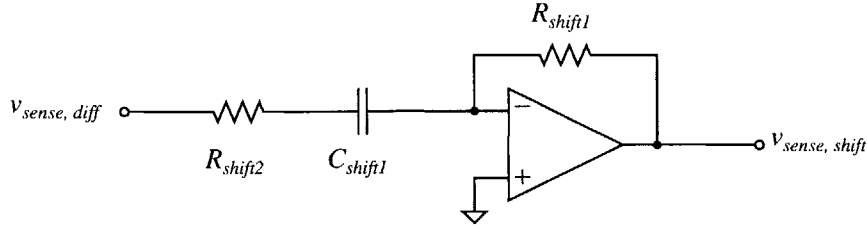


Figure 5-17: Schematic of the  $-90^\circ$  phase shifter circuit with the addition of  $R_{shift2}$  for lead compensation.

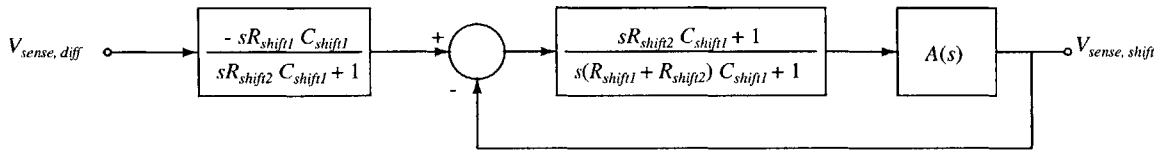


Figure 5-18: Feedback loop for the circuit shown in Figure 5-17.

high-frequency noise gain. This final modification results in the feedback loop shown in Figure 5-20. The Bode plot of this final  $L(s)$  is presented in Figure 5-21. The phase margin is improved from  $0.01^\circ$  to  $70.8^\circ$ .

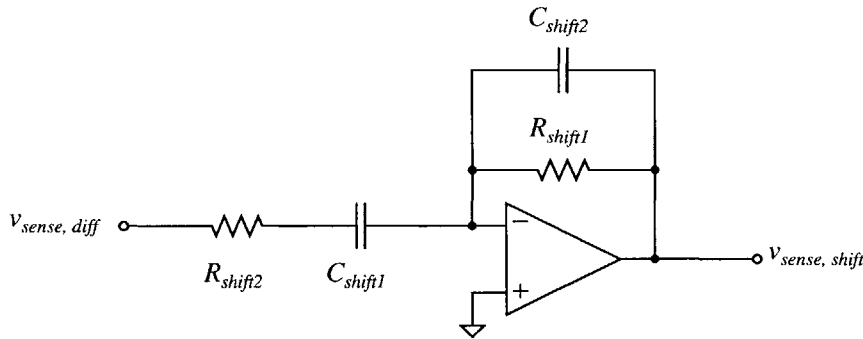


Figure 5-19: Schematic of the  $-90^\circ$  phase shifter circuit with the addition of  $C_{shift2}$  for high-frequency noise attenuation.

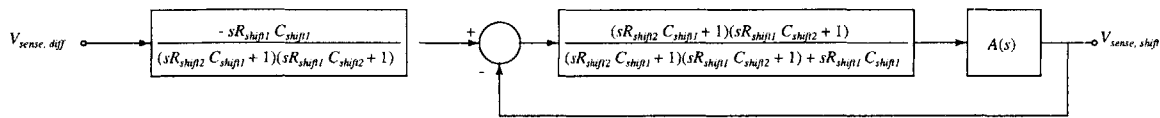


Figure 5-20: Feedback loop for the circuit shown in Figure 5-19.

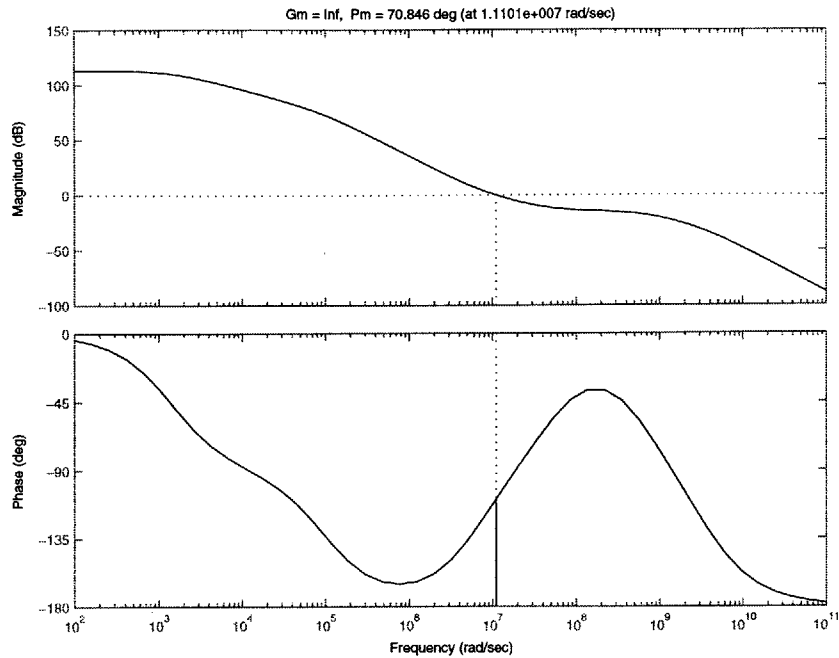


Figure 5-21: Bode plot of the  $L(s)$  shown in Figure 5-20.

### 5.3.3 Low-Pass Filter

The low-pass filter circuit is shown in Figure 5-22. The corresponding feedback loop is given in Figure 5-23. Since the op amp used for the filter is the AD8065AR,  $A(s)$  is as given in (5.29). Also,  $R_{lpf1} = R_{lpf2} = 100\text{k}\Omega$ , and  $C_{lpf} = 0.1\ \mu\text{F}$ . Since  $R_{lpf1} = R_{lpf2}$ , the pole and zero in  $L(s)$  approximately cancel each other out<sup>1</sup>, and stability is guaranteed. The Bode plot of  $L(s)$  is shown in Figure 5-24. The loop unity-gain frequency is 78.7 MHz, and the phase margin is 51.8°.

While low-pass filters, unlike differentiators, are not notorious for instability problems, the preceding analysis simply verified that stability was ensured.

<sup>1</sup>The phase margin is actually increased since the zero occurs before the pole.

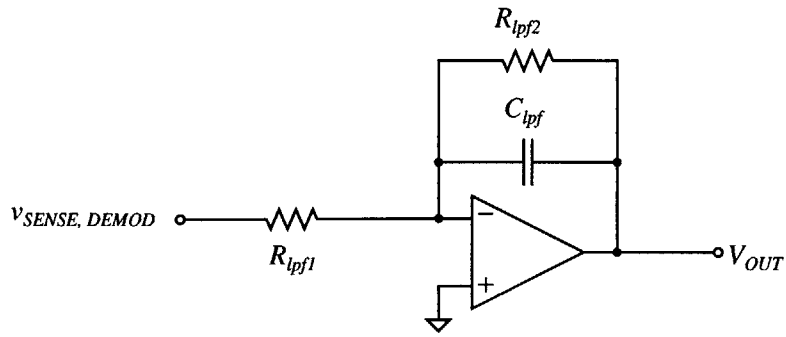


Figure 5-22: Schematic of the ideal low-pass filter circuit.

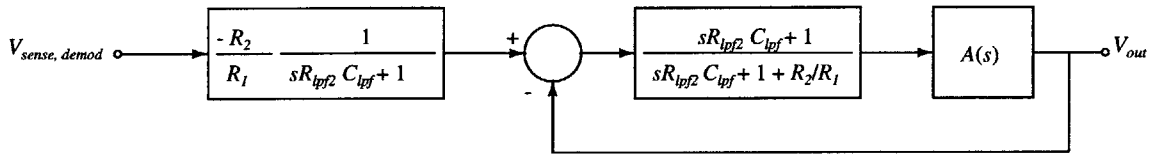


Figure 5-23: Feedback loop for the circuit shown in Figure 5-22.

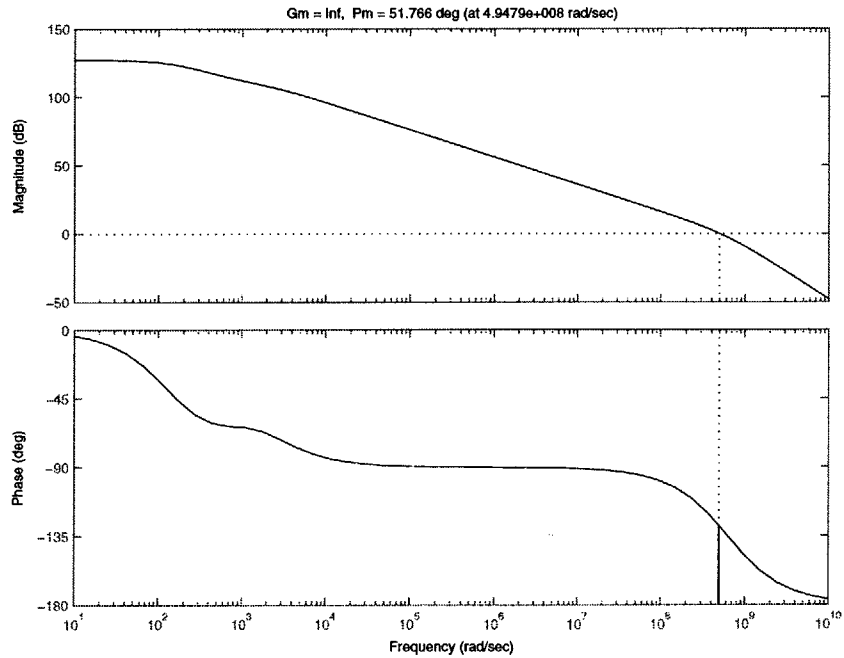


Figure 5-24: Bode plot of the  $L(s)$  shown in Figure 5-23.

## 5.4 Phase Shift at Resonance

As with the drive loop, the finite bandwidths of the components in the sense block lead to a small phase shift between the shutter displacement and the output of the demodulator. This phase shift ultimately results in a slight attenuation of the constant of proportionality between the input electric field and the dc output voltage.

The transimpedance amplifier with dc feedback was shown in Figure 5-7. As depicted in the Bode plot of  $V_{sense+}(s)$  in Figure 5-25, the finite bandwidth of the low-noise op amp, as well as any effects from the diode-connected transistors, lead to a phase of  $-185.9^\circ$  at 15 kHz, or a phase shift of  $-5.9^\circ$  from the ideal.

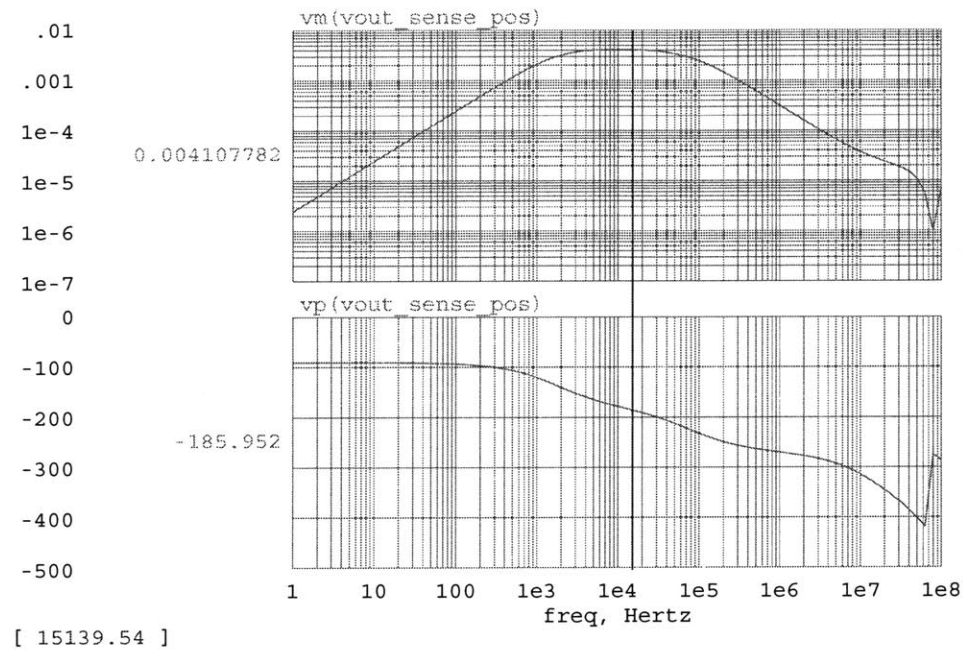


Figure 5-25: Bode plot of  $V_{sense+}(s)$  for the circuit in Figure 5-7. Vertical axis: (top) Magnitude [V/V], (bottom) Phase [degrees]. Horizontal axis: Frequency [Hz].

The net phase shift of the  $-90^\circ$  phase shifter is not precisely  $-90^\circ$  due to the finite bandwidth of the AD8065AR op amp and the effect of the lead compensation resistor [34]. The Bode plot of  $V_{sense,shift}(s)/V_{sense,diff}(s)$  is presented in Figure 5-26. The phase at 15 kHz is  $-90.9^\circ$ , for a phase shift of  $-0.9^\circ$  from the ideal.

Lastly, the AD630BD demodulator has a unity-gain bandwidth of 2 MHz [35]. Since it is configured to act as a demodulator with gain  $\pm 2$ , the net bandwidth

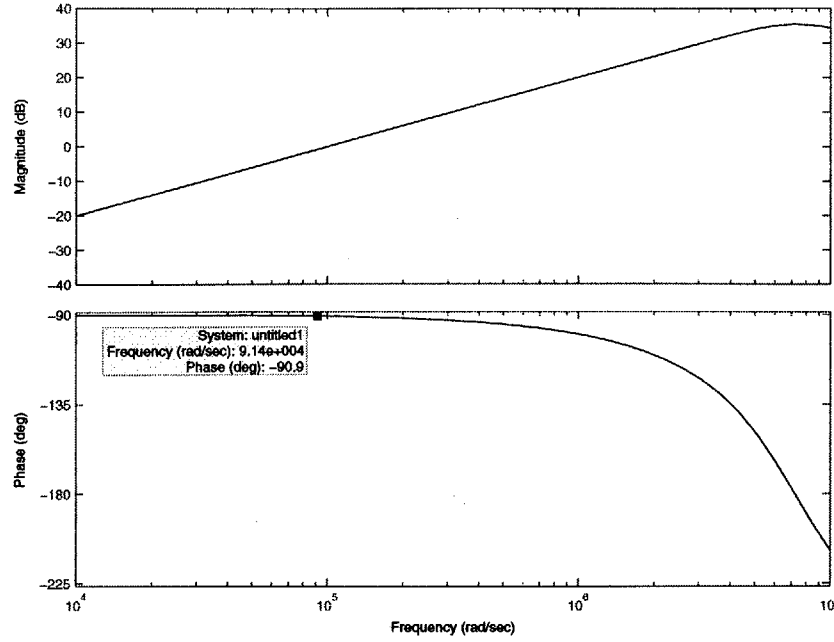


Figure 5-26: Bode plot of  $V_{sense,shift}(s)/v_{sense,diff}(s)$  for the circuit in Figure 5-19.

is actually 1 MHz. The input-output gain over frequency of the AD630BD can be expressed as

$$G(j\omega) = \frac{2}{j\omega\tau + 1}, \quad (5.33)$$

where

$$\tau = \frac{1}{\omega_{-3dB}} = \frac{1}{2\pi \cdot 1 \text{ MHz}}. \quad (5.34)$$

The resulting phase shift at 15kHz is given by

$$\angle G(j\omega) = -\arctan(\omega_{res}\tau) = -\arctan\left(\frac{2\pi \cdot 15 \text{ kHz}}{2\pi \cdot 1 \text{ MHz}}\right) = -0.9^\circ. \quad (5.35)$$

However, recall from Section 4.4 that  $v_{VEL,COMP}$ , a drive loop signal that serves as an input to the demodulator, experiences a phase shift of  $-0.5^\circ$  from the ideal. Thus, the net phase shift of the output of the demodulator is  $-0.9^\circ - 0.5^\circ = -1.4^\circ$ .

The sum of the transimpedance amplifier,  $-90^\circ$  phase shifter, and demodulator

phase shifts is given by

$$\phi_{sense,total} = -5.9^\circ - 0.9^\circ - 1.4^\circ = -8.2^\circ. \quad (5.36)$$

Note that since the output of the low-pass filter is a dc voltage, there is no concept of phase shift of the low-pass filter circuit.

Drawing a parallel between the ESF and a standard communication system,  $V_{UNK}$  is effectively modulated onto a 15 kHz carrier, only to be demodulated later. In a communication system, for a phase shift  $\phi_{shift}$  between the modulator and demodulator, the output of the low-pass filter following the demodulator is multiplied by a factor  $\cos(\phi_{shift})$  [14]. For the ESF, a nonzero  $\phi_{sense,total}$  amounts to a phase shift between the shutter displacement and the output of the demodulator,  $v_{SENSE,DEMODO}$ . The output of the low-pass filter,  $V_{OUT}$ , is modified from (5.18) to

$$V_{OUT} = \frac{8 \alpha V_{UNK} C_{sense,m}}{\pi C_f} \cos(\phi_{sense,total}). \quad (5.37)$$

Nonetheless, since  $\cos(\phi_{sense,total}) = \cos(-8.2^\circ) = 0.9898$ , the attenuation of  $V_{OUT}$  due to  $\phi_{sense,total}$  is negligible.

## 5.5 Analysis of Critical Performance Specifications

### 5.5.1 Input-Referred Electric Field Noise

The most critical specification of the ESF is its input-referred noise. As such, the sense block electronics were optimized for low-noise operation. Shown in Figure 5-27 is the equivalent noise circuit of the sense block.

As discussed in Chapter 3, the input-referred spot noise of the low-noise op amp, denoted as  $V_{n,op+}(f)$  and  $V_{n,op-}(f)$ , is  $9.65 \text{ nV}/\sqrt{\text{Hz}}$ . By the principles of superposition,  $V_{UNK}$  is grounded for purposes of noise analysis. The noise at the output of  $U_1$



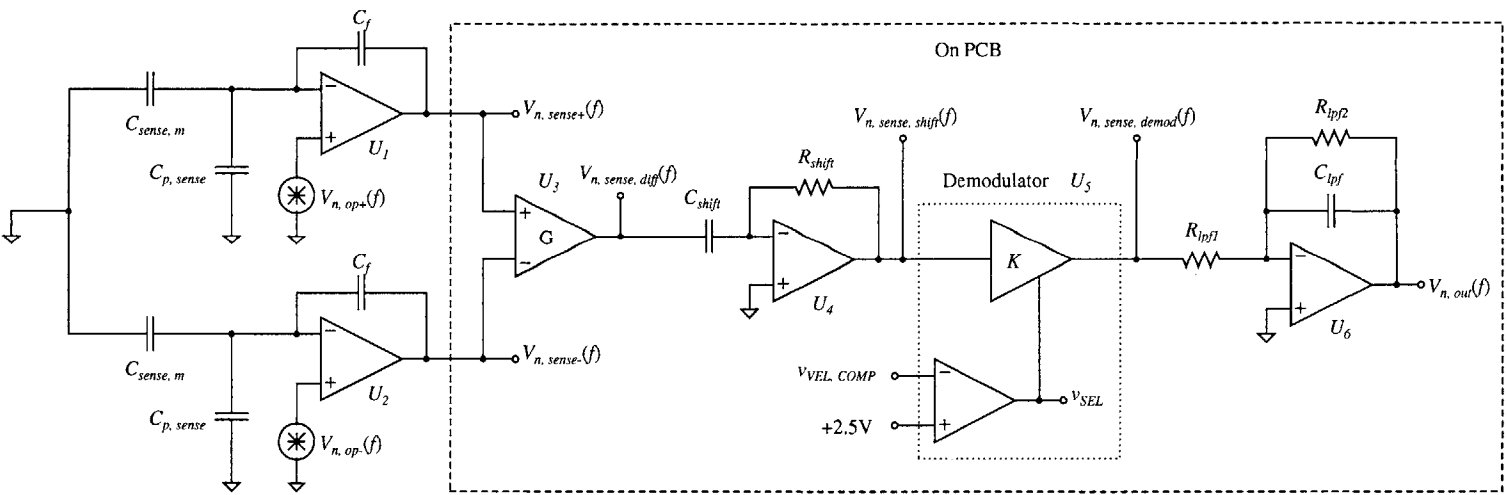


Figure 5-27: Equivalent noise circuit for the sense block.

is thus given by

$$\begin{aligned}
V_{n,sense+}(f) &= \left(1 + \frac{C_{p,sense} + C_{sense,m}}{C_f}\right) V_{n,op+}(f) \\
&= \left(1 + \frac{4.2 \text{ pF} + 0.4 \text{ fF}}{100 \text{ fF}}\right) \cdot 9.65 \text{ nV}/\sqrt{\text{Hz}} \\
&= 415 \text{ nV}/\sqrt{\text{Hz}}.
\end{aligned} \tag{5.38}$$

The noise at the output of  $U_2$ ,  $V_{n,sense-}(f)$ , is similarly found to be  $415 \text{ nV}/\sqrt{\text{Hz}}$ . Since  $V_{n,op+}(f)$  and  $V_{n,op-}(f)$  are uncorrelated,  $V_{n,sense+}(f)$  and  $V_{n,sense-}(f)$  are summed in an rms manner. Therefore, the noise output of the instrumentation amplifier, is given by

$$V_{n,diff}(f) = \sqrt{V_{n,sense+}^2(f) + V_{n,sense-}^2(f)} = 587 \text{ nV}/\sqrt{\text{Hz}}. \tag{5.39}$$

Note that the input noise of the AD620AN instrumentation amplifier is  $9 \text{ nV}/\sqrt{\text{Hz}}$ , which is much less than the values for  $V_{n,sense+}(f)$  and  $V_{n,sense-}(f)$ , and can thus be ignored [28].

Before proceeding with the noise analyses of the  $-90^\circ$  phase shifter, demodulator, and low-pass filter, it is helpful to first make note of the input noise specifications of the ICs in these circuits. The input noise of the AD8065AR, the op amp used in the  $-90^\circ$  phase shifter and low-pass filter, is  $7 \text{ nV}/\sqrt{\text{Hz}}$ , which is nearly two orders of magnitude less than  $V_{n,diff}(f) = 587 \text{ nV}/\sqrt{\text{Hz}}$  [34]. Also, while the input noise of the AD630BD, the demodulator IC, is not listed in its datasheet, it is likely considerably less than  $V_{n,diff}(f) = 587 \text{ nV}/\sqrt{\text{Hz}}$  [17]. Thus, all noise sources following  $V_{n,diff}(f)$  in the circuit path are negligible, and the input-referred noise can be accurately calculated by referring  $V_{n,diff}(f)$  back to the input terminal voltage  $V_{UNK}$ . From (5.7),

$$\left|\frac{v_{sense,diff}}{V_{UNK}}\right| = 2\alpha \frac{C_{sense,m}}{C_f}. \tag{5.40}$$

Therefore, the input-referred voltage noise of the ESF, denoted as  $V_{ni}(f)$ , can be

found by

$$V_{ni}(f) = \frac{V_{n,diff}(f)}{2 \alpha C_{sense,m}/C_f} = \frac{587 \text{ nV}/\sqrt{\text{Hz}}}{2 \cdot 0.7 \cdot 0.4 \text{ fF}/100\text{fF}} = 105 \mu\text{V}/\sqrt{\text{Hz}}. \quad (5.41)$$

Converting  $V_{ni}(f)$  to an equivalent input-referred electric field noise,  $E_{ni}(f)$ , involves multiplying it by  $d_{sense}$ , the distance between the target surface and the sense plates:

$$E_{ni}(f) = \frac{V_{ni}(f)}{d_{sense}} = \frac{105 \mu\text{V}/\sqrt{\text{Hz}}}{0.5 \text{ mm}} = 0.21 \text{ V/m}/\sqrt{\text{Hz}}. \quad (5.42)$$

This value is over three orders of magnitude lower than the input-referred noise of  $700 \text{ V/m}/\sqrt{\text{Hz}}$  given in the Riehl thesis and clearly meets the specification of  $200 \text{ V/m}/\sqrt{\text{Hz}}$  given in Chapter 1 [7].

The minimum detectable electric field can be determined by knowing the rms value of the input electric field noise. This quantity is given by

$$E_{ni,rms} = E_{ni}(f) \cdot \sqrt{\Delta f}, \quad (5.43)$$

where  $\Delta f$  represents the noise bandwidth. In this case, the noise bandwidth is ultimately determined by the  $-3 \text{ dB}$  bandwidth of the low-pass filter,  $f_{-3\text{dB}} = 15.9 \text{ Hz}$ . The noise bandwidth is then given by

$$\Delta f = f_{-3\text{dB}} \cdot \frac{\pi}{2} = 25.0 \text{ Hz}, \quad (5.44)$$

where the  $\pi/2$  factor arises from the definition of noise bandwidth [16]. The rms input electric field noise is thus equal to

$$E_{ni,rms} = E_{ni}(f) \cdot \sqrt{\Delta f} = 0.21 \text{ V/m}/\sqrt{\text{Hz}} \cdot \sqrt{25.0 \text{ Hz}} = 1.1 \text{ V/m (rms)}. \quad (5.45)$$

Many noise sources, including thermal noise, have a Gaussian distribution such that

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-(x-\mu)^2/(2\sigma^2)}, \quad (5.46)$$

where  $\mu$  represents the mean, and  $\sigma$  represents the standard deviation. A reasonable engineering approximation is that all electrical noise lies within  $6\sigma$  of the mean, which is zero for electronic noise sources [16]. In other words, the peak-to-peak amplitude of a noise source is given by six times its rms value. Equivalently, the peak-to-ground amplitude is equal to three times the rms value of the noise source. Thus, given the input electric field noise of 1.1 V/m (rms) found in (5.45), the ESF should be able to detect incident electric fields down to

$$E_{min} = E_{ni,pk} = 3 E_{ni,rms} = 3 \cdot 1.1 \text{ V/m (rms)} = 3.3 \text{ V/m.} \quad (5.47)$$

## 5.5.2 Input Electric Field Range

The input electric field range is ultimately limited by the sense block power supplies and output swing of the demodulator IC.

The largest (signal) voltage in the entire sense block is found at the output of the demodulator. The peak voltage of  $v_{SENSE,DEMODO}$  is

$$V_{SENSE,DEMODO,PK} = -4\alpha V_{UNK} \frac{C_{sense,m}}{C_f}. \quad (5.48)$$

Since the output swing of the AD630BD is  $\pm 10$  V for  $\pm 12$  V supply voltages, the maximum allowable input voltage to the ESF, denoted as  $V_{UNK,max}$ , is given by

$$V_{UNK,max} = \left| \frac{V_{SENSE,DEMODO,PK} C_f}{4\alpha C_{sense,m}} \right| = \left| \frac{10 \text{ V} \cdot 100 \text{ fF}}{4 \cdot 0.7 \cdot 0.4 \text{ fF}} \right| = 893 \text{ V} \quad (5.49)$$

[35]. Therefore, the maximum input electric field range is

$$E_{in,max} = \pm \frac{V_{UNK,max}}{d_{sense}} = \pm \frac{893 \text{ V}}{0.5 \text{ mm}} = \pm 1790 \text{ V/mm.} \quad (5.50)$$

The specification for an input electric field range of  $\pm 500$  V/mm is clearly met.

## 5.6 Complete Sense Block Circuit

The schematic for the complete sense block circuit is given in Figure 5-28. The corresponding component descriptions and values are captured in Table 5.2.

Capacitors  $C_{f+}$  and  $C_{f-}$  are poly- $n^+$  capacitors, where the top plate is polysilicon and the bottom plate is an  $n^+$  emitter diffusion. Transistors  $M_1$ – $M_{10}$  are enhancement-mode NFETs.

Component  $JP_1$  is an open jumper connection that effectively sets the gain of  $U_3$ , the instrumentation amplifier, to  $G = 1$ . The jumper is placed there to allow the possibility of changing the amplifier gain if necessary. Component  $U_7$  is an AD586BR +5 V precision voltage reference that, in conjunction with  $R_7$  and  $R_8$ , provides the +2.5 V input to the internal comparator of  $U_5$ , the demodulator [36]. Note that  $v_{VEL,COMP}$ , the drive loop signal, is also an input to the internal comparator of the demodulator. Resistors  $R_1$  and  $R_4$  are included at the non-inverting terminals of the  $U_4$  and  $U_6$  op amps to minimize errors due to input bias current.

Capacitors  $C_1$ – $C_{14}$  are bypass capacitors. All 10  $\mu\text{F}$  capacitors are electrolytic, while the 0.1  $\mu\text{F}$  capacitors are ceramic. Lastly, resistors  $R_2$  and  $R_3$ , in conjunction with  $C_7$  and  $C_8$ , respectively, act as low-pass filters to prevent high-frequency oscillations in the  $V_{DD}$  or  $V_{SS}$  rails from reaching the power supply pins of  $U_4$ . Similarly, any high-frequency content on the power supply pins of  $U_4$  is filtered out before coupling to the  $V_{DD}$  or  $V_{SS}$  rails. A similar configuration exists for  $U_6$ .

## 5.7 Simulation Results

The results of a behavioral, time-domain simulation of the sense block circuitry are presented in Figures 5-29 and 5-30. Similar to the drive loop simulation, the transimpedance amplifier equivalent model introduced in Figure 5-4 is used for compatibility with standard simulation capabilities.

The simulation includes the actual transistor-level implementations of  $U_1$  and  $U_2$ , the low-noise op amps, as well as all elements in the transimpedance amplifier

Parameter	Component Description
$U_1$	Low-Noise Op Amp
$U_2$	Low-Noise Op Amp
$U_3$	AD620AN Instrumentation Amplifier
$U_4$	AD8065AR FET-Input Op Amp
$U_5$	AD630BD Demodulator
$U_6$	AD8065AR FET-Input Op Amp
$U_7$	AD586BR +5 V Precision Voltage Reference
$M_1-M_{10}$	5/4 [ $\mu\text{m}/\mu\text{m}$ ]
Parameter	Component Value
$R_{shift1}$	1 k $\Omega$
$R_{shift2}$	15 $\Omega$
$R_{lpf1}$	100 k $\Omega$
$R_{lpf2}$	100 k $\Omega$
$R_1$	1 k $\Omega$
$R_2$	51 $\Omega$
$R_3$	51 $\Omega$
$R_4$	51 k $\Omega$
$R_5$	51 $\Omega$
$R_6$	51 $\Omega$
$R_7$	10 k $\Omega$
$R_8$	10 k $\Omega$
$C_{f+}$	100 fF
$C_{f-}$	100 fF
$C_{shift1}$	10 nF
$C_{shift2}$	20 pF
$C_{lpf}$	0.1 $\mu\text{F}$
$C_1-C_4$	10 $\mu\text{F}$
$C_5-C_{14}$	0.1 $\mu\text{F}$

Table 5.2: Component descriptions or values for the complete sense block circuit shown in Figure 5-28 [28], [34], [35], [36].

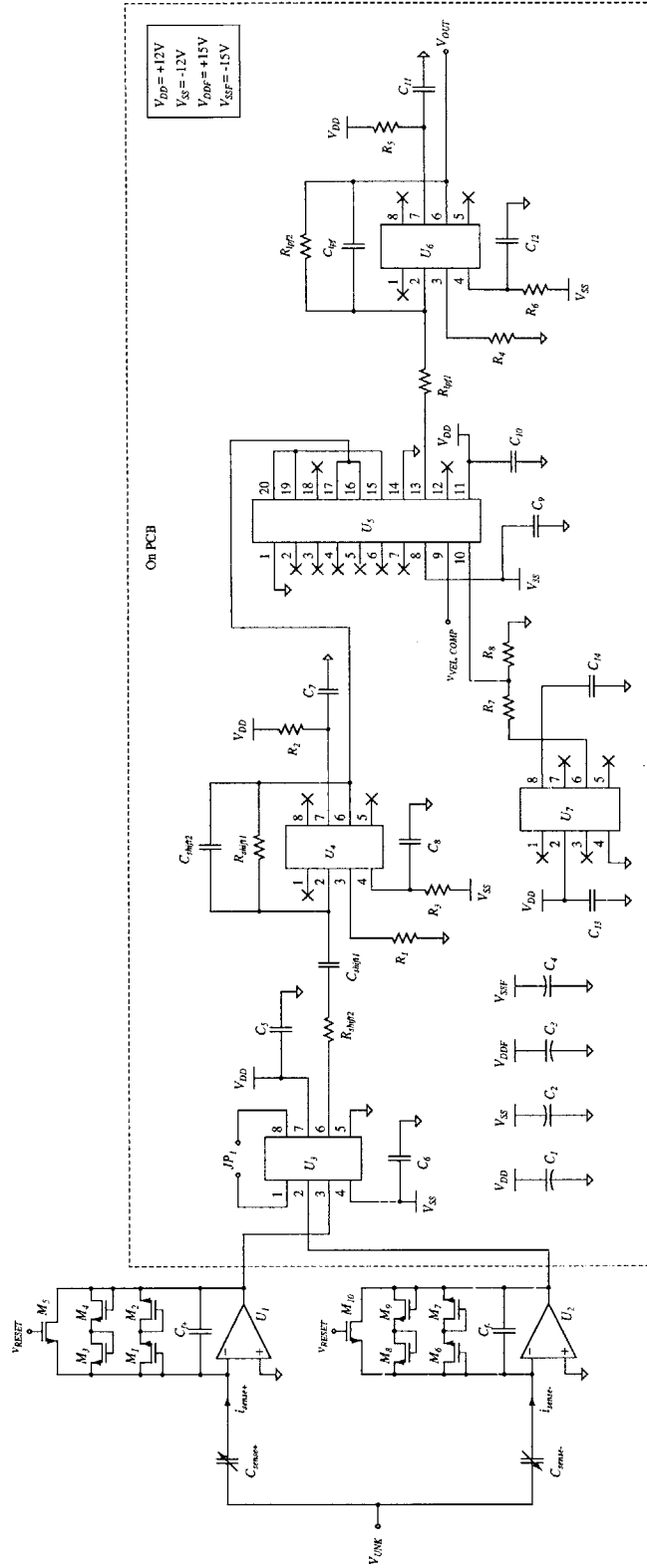


Figure 5-28: Complete schematic of the sense block circuitry.

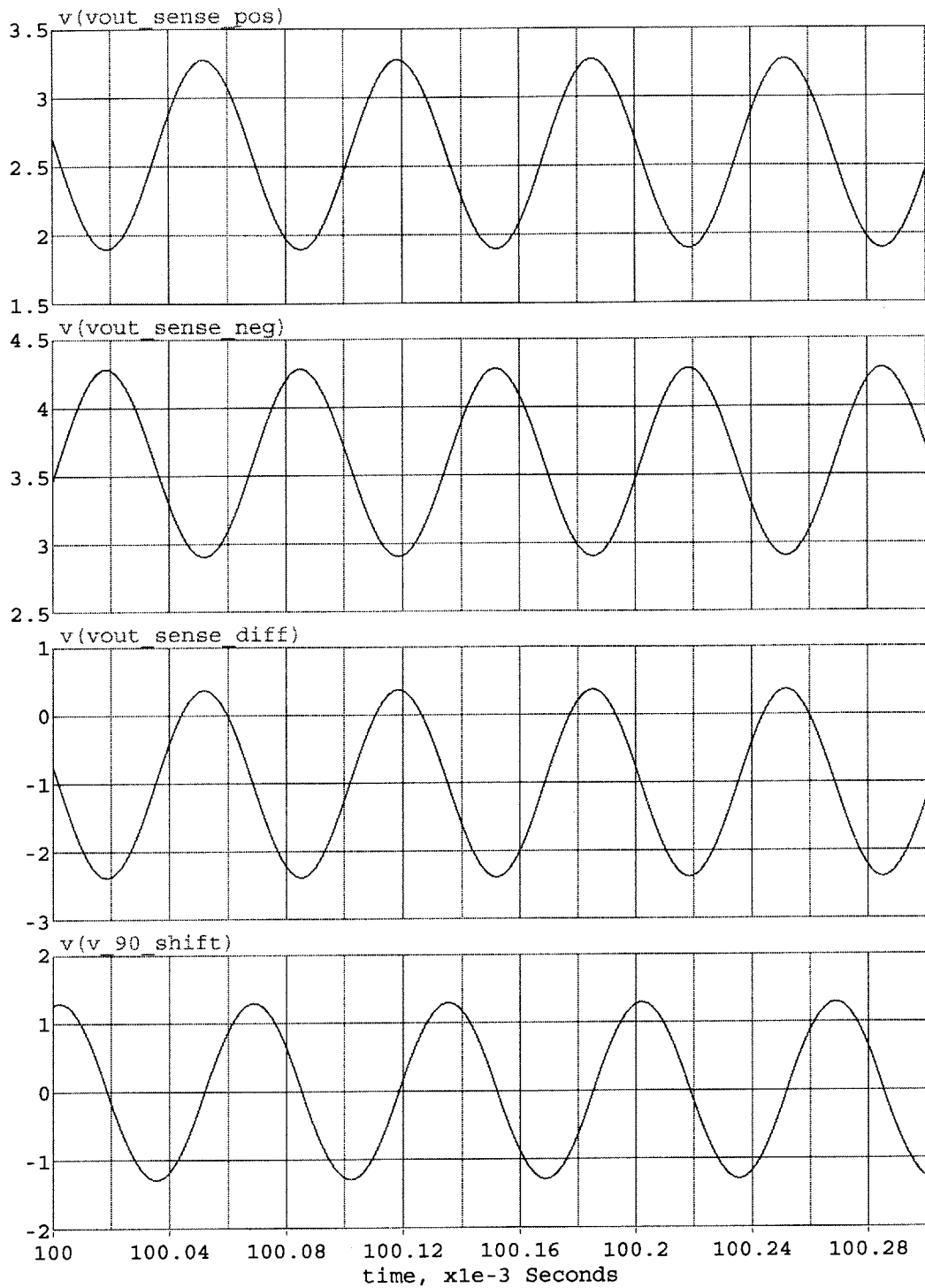


Figure 5-29: Results of a behavioral simulation of the sense block circuitry. Vertical axis: (top)  $v_{sense+}$  [V], (second from top)  $v_{sense-}$  [V], (third from top)  $v_{sense,diff}$  [V], (bottom)  $v_{sense,shift}$  [V]. Horizontal axis: Time [ms].



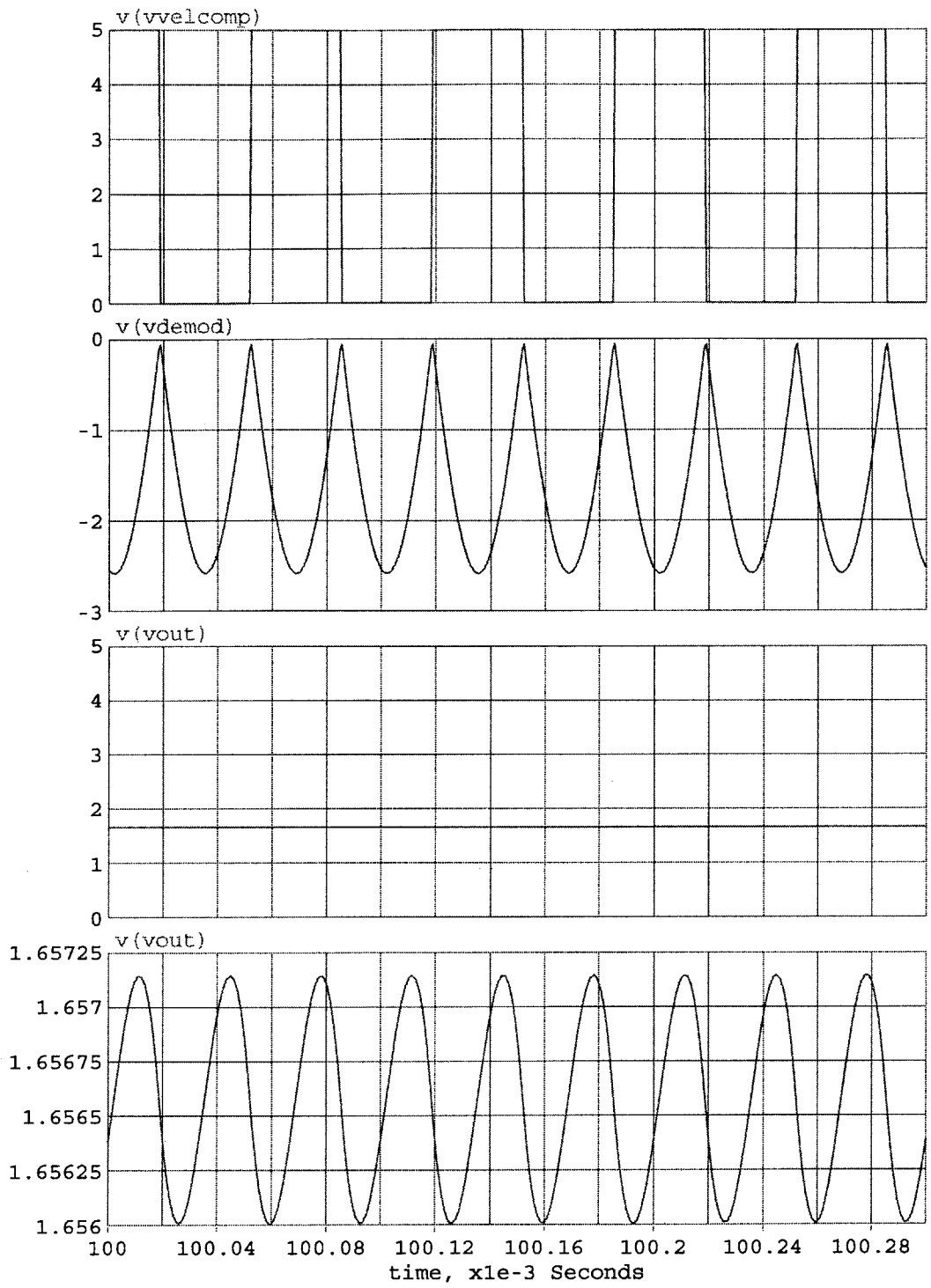


Figure 5-30: Results of a behavioral simulation of the sense block circuitry. Vertical axis: (top)  $v_{VEL,COMP}$  [V], (second from top)  $v_{SENSE,DEMODO}$  [V], (third from top)  $V_{OUT}$  [V], (bottom) Zoomed-in view of  $V_{OUT}$  [V]. Horizontal axis: Time [ms].

feedback loop, including the parasitic capacitance  $C_{p,sense}$ . Capacitances of 22 pF are placed on the outputs of  $U_1$  and  $U_2$  to simulate the effect of the 2 pF input capacitance of the AD620AN instrumentation amplifier  $U_3$ , along with the 10 pF capacitance of an oscilloscope probe. The  $U_3$  amplifier, along with  $U_4$  and  $U_6$ , the op amps, are modeled with ideal blocks. The demodulator  $U_5$  is modeled with a voltage-dependent gain block. When  $v_{VEL,COMP}$  is high, the gain of the block is  $-2$ . On the other hand, when  $v_{VEL,COMP}$  is low, the gain of the block is  $+2$ . This behavior mimics the ideal operation of the AD630BD.

The simulations were performed for  $V_{UNK} = +250$  V, or, equivalently, an input electric field of  $E = +500$  V/mm. As shown in Figure 5-29,  $v_{sense,shift}$  is shifted by  $-90^\circ$  with respect to  $v_{sense,diff}$ , as desired. Also, as depicted in Figure 5-30,  $v_{SENSE,DEMODO}$  consists of a unipolar series of half-sinusoids at a frequency of  $2 \cdot 15$  kHz = 30 kHz. The low-pass filtered output voltage  $V_{OUT}$  is 1.66 V. The bottom waveform shows that the ripple on  $V_{OUT}$  is sufficiently attenuated to a peak-to-peak voltage of 1.25 mV. The theoretical output voltage for  $V_{UNK} = +250$  V is given by (5.18) as

$$V_{OUT} = \frac{8 \alpha V_{UNK}}{\pi} \frac{C_{sense,m}}{C_f} = \frac{8 \cdot 0.7 \cdot 250 \text{ V}}{\pi} \frac{0.4 \text{ fF}}{100 \text{ fF}} = 1.78 \text{ V}. \quad (5.51)$$

The theoretical and simulated output voltages agree to within 6.7%.

## 5.8 Summary

The sense block performs the actual measurement of the incident electric field. The dynamic currents generated by the sense capacitance  $C_{sense}$  are converted into a dc output voltage that is proportional to the incident electric field.

The functions of each sub-block — the transimpedance amplifiers,  $-90^\circ$  phase shifter, demodulator, and low-pass filter — were discussed. DC feedback and lead compensation were added to the transimpedance amplifiers and  $-90^\circ$  phase shifter, respectively, to increase loop stability. Although there is a small phase shift between the

shutter displacement and the demodulator output due to component non-idealities, the resulting attenuation of the output voltage is negligible.

The two critical performance specifications for the ESF are its input-referred noise and input electric field range. The input-referred noise of the ESF was calculated to be  $0.21 \text{ V/m}/\sqrt{\text{Hz}}$ , while the input electric field range was calculated to be  $\pm 1790 \text{ V/mm}$ . Both of these metrics are improvements over those of the Riehl ESF.

The results of a time-domain simulation of the sense block agreed well with the predicted behavior.



# Chapter 6

## System Evaluation

### 6.1 Overview

As was initially presented in Chapter 1, the entire ESF system consists of the MEMS capacitances, the drive loop, and the sense block. The MEMS structure and all current-to-voltage converters — the transresistance amplifiers for the drive loop and the transimpedance amplifiers for the sense block — are contained on an integrated circuit fabricated using the Analog Devices iMEMS multi-layer process. For ease of testing and debugging, all other electronics are off-chip on a PCB. A physical overview of the ESF IC and PCB is presented in this chapter.

After overcoming two initial setbacks in the experimental evaluation of the ESF, the obtained results were extremely promising. The collected data verified that the ESF met the critical performance specifications — the input-referred electric field noise and input electric field range — outlined in Chapter 1. The measured values for input-referred noise and input electric field range were also improvements over those of the Riehl ESF. The input-to-output linearity of the ESF was also measured.

## 6.2 ESF Integrated Circuit

### 6.2.1 Layout

The layout of the ESF integrated circuit was carried out by a layout engineer with the Analog Devices Micromachined Products Division. A snapshot of the layout is presented in Figure 6-1. The locations of the MEMS structure, the sense block transimpedance amplifiers, and the drive loop transresistance amplifiers are all identified in the figure. It is necessary to have the transresistance and transimpedance amplifiers on-chip to prevent parasitic capacitances external to the IC from acting in parallel with  $C_{p,sense}$  and  $C_{p,vel}$ . Also shown are the electrostatic discharge (ESD) protection diodes that are found at each bond pad.

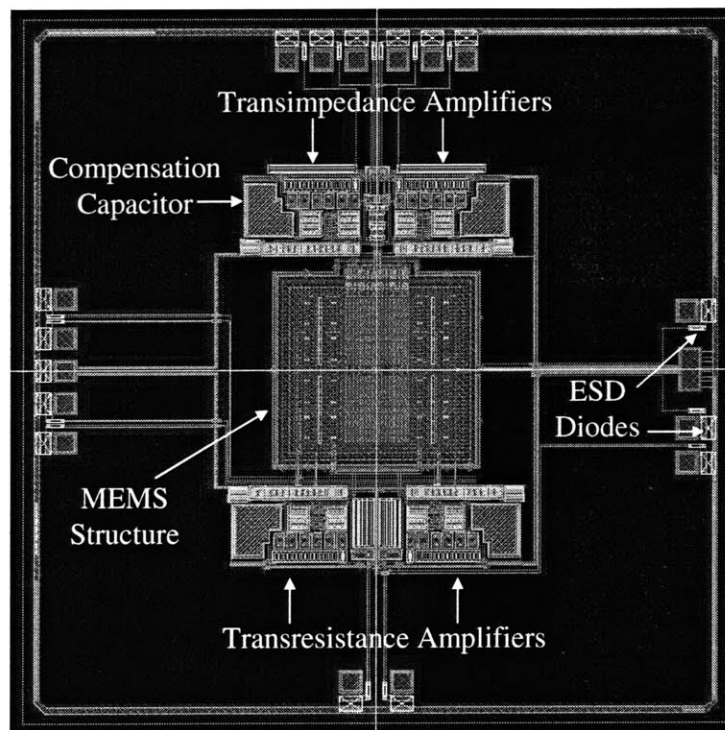


Figure 6-1: Snapshot of the ESF IC layout.

The specific process used was the iMEMS3, BiMOS2E process, and the IC was fabricated at the Analog Devices manufacturing facility in Cambridge, Massachusetts.

## 6.2.2 Packaging

The ESF integrated circuit was packaged in a 20-pin, 300 mil, ceramic side-braze dual-inline package (DIP). The package features a metal, solder-sealed lid which is at a floating potential. The lid will serve as the target surface for testing purposes. A photograph of the 20-pin DIP with metal lid is shown in Figure 6-2.

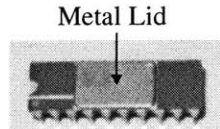


Figure 6-2: Photograph of the 20-pin DIP in which the ESF IC is packaged.

The pinout of the package is captured in Table 6.1. A brief description accompanies the identifier for each pin number.

## 6.2.3 Photomicrographs

Photomicrographs were taken of the ESF integrated circuit using both an optical microscope and scanning electron microscope (SEM).

Figures 6-3 and 6-4 were taken with the optical microscope. Figure 6-3 is a close-up of the MEMS structure, while Figure 6-4 is a photomicrograph of the entire IC, including the bonding wires.

The SEM was used for Figures 6-5, 6-6, and 6-7. The overall MEMS structure is seen in Figure 6-5. The comb-like structure that is used to implement  $C_{force}$  and  $C_{vel}$  is depicted in Figure 6-6. Lastly, Figure 6-7 is a close-up of the comb-like structure taken from a perspective of  $45^\circ$ . The square in the upper left corner of Figure 6-7 is an etch hole.

Pin #	Identifier	Description
1	$v_{sense+}$	Output of $C_{sense+}$ op amp.
2	$v_{RESET}$	Switch to $V_{DD}$ to null $V_{OS}$ of $C_{sense+}$ and $C_{sense-}$ op amps.
3	$V_{ADJUST+}$	To null $V_{OS}$ of $C_{sense+}$ op amp.
4	$v_{DRIVE+-}$	Apply $V_{SSF}$ to actuate shutter movement in $+\hat{x}$ direction.
5	$v_{DRIVE--}$	Apply $V_{DDF}$ to actuate shutter movement in $-\hat{x}$ direction.
6	$V_{DD}$	+12 V.
7	$v_{DRIVE--}$	Apply $V_{SSF}$ to actuate shutter movement in $-\hat{x}$ direction.
8	$v_{DRIVE++}$	Apply $V_{DDF}$ to actuate shutter movement in $+\hat{x}$ direction.
9	NC	Not connected.
10	$v_{vel+}$	Output of $C_{vel+}$ op amp.
11	NC	Not connected.
12	$v_{vel-}$	Output of $C_{vel-}$ op amp.
13	NC	Not connected.
14	$V_{BIAS}$	Connect to +5 V for biasing $C_{vel+}$ and $C_{vel-}$ op amps.
15	$V_{RES}$	Connect 560 k $\Omega$ resistor to $V_{SS}$ to set $I_{REF} = 10 \mu\text{A}$ per op amp.
16	$V_{SS}$	-12 V.
17	$V_{BEAM}$	Connect to GND to bias the MEMS beam at 0 V.
18	$V_{ADJUST-}$	To null $V_{OS}$ of $C_{sense-}$ op amp.
19	GND	0 V.
20	$v_{sense-}$	Output of $C_{sense-}$ op amp.

Table 6.1: Pinout of the ESF 20-pin DIP.



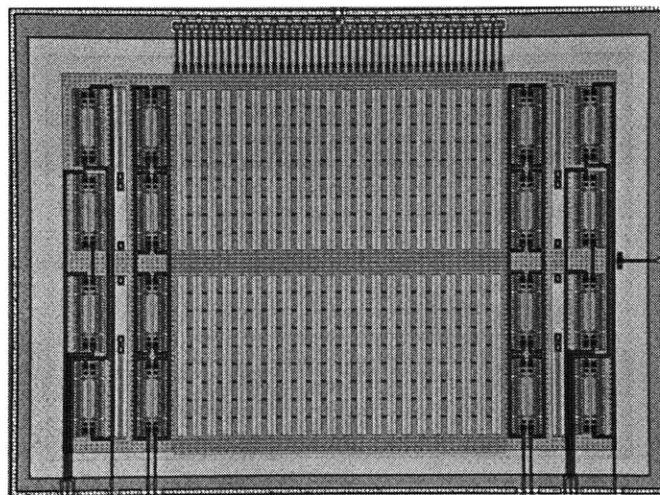


Figure 6-3: Photomicrograph of the MEMS structure (taken with an optical microscope).

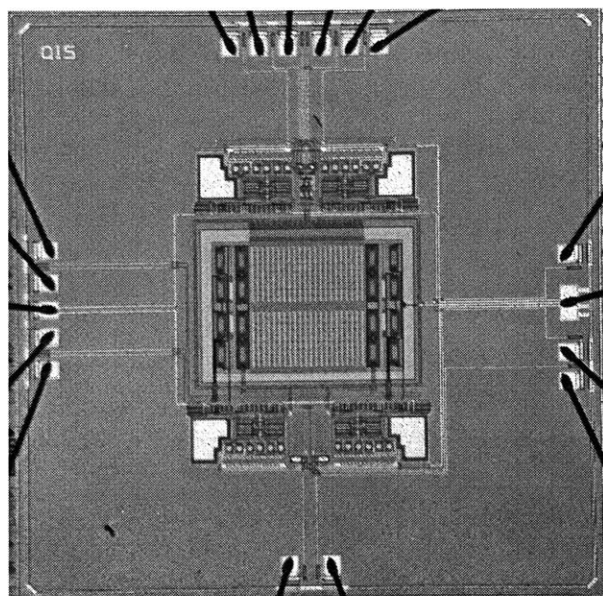


Figure 6-4: Photomicrograph of the entire ESF IC (taken with an optical microscope).

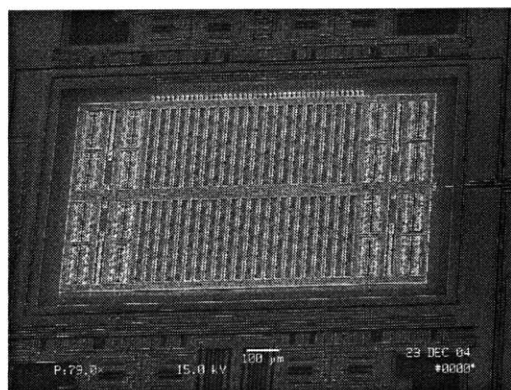


Figure 6-5: Photomicrograph of the MEMS structure (taken with a scanning electron microscope).

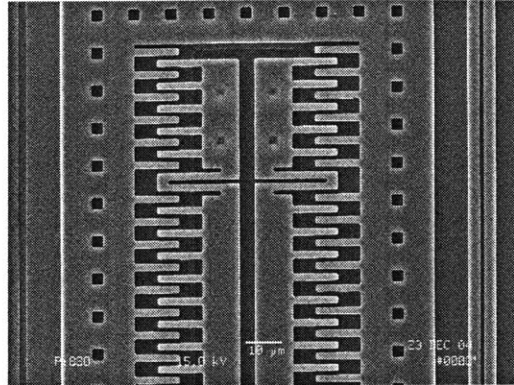


Figure 6-6: Photomicrograph of the MEMS comb-like structure used to implement  $C_{force}$  and  $C_{vel}$  (taken with a scanning electron microscope). The squares surrounding the comb-like structure are etch holes.

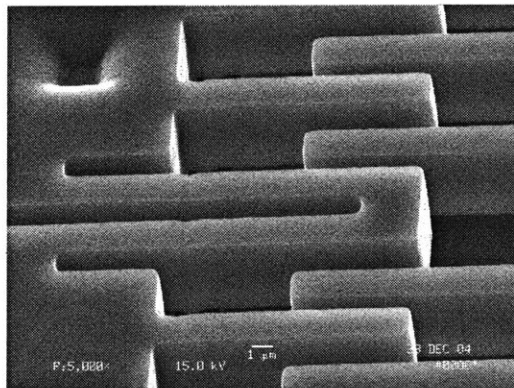


Figure 6-7: Photomicrograph of the MEMS comb-like structure taken from a perspective of  $45^\circ$  (taken with a scanning electron microscope). The square in the upper left corner is an etch hole.

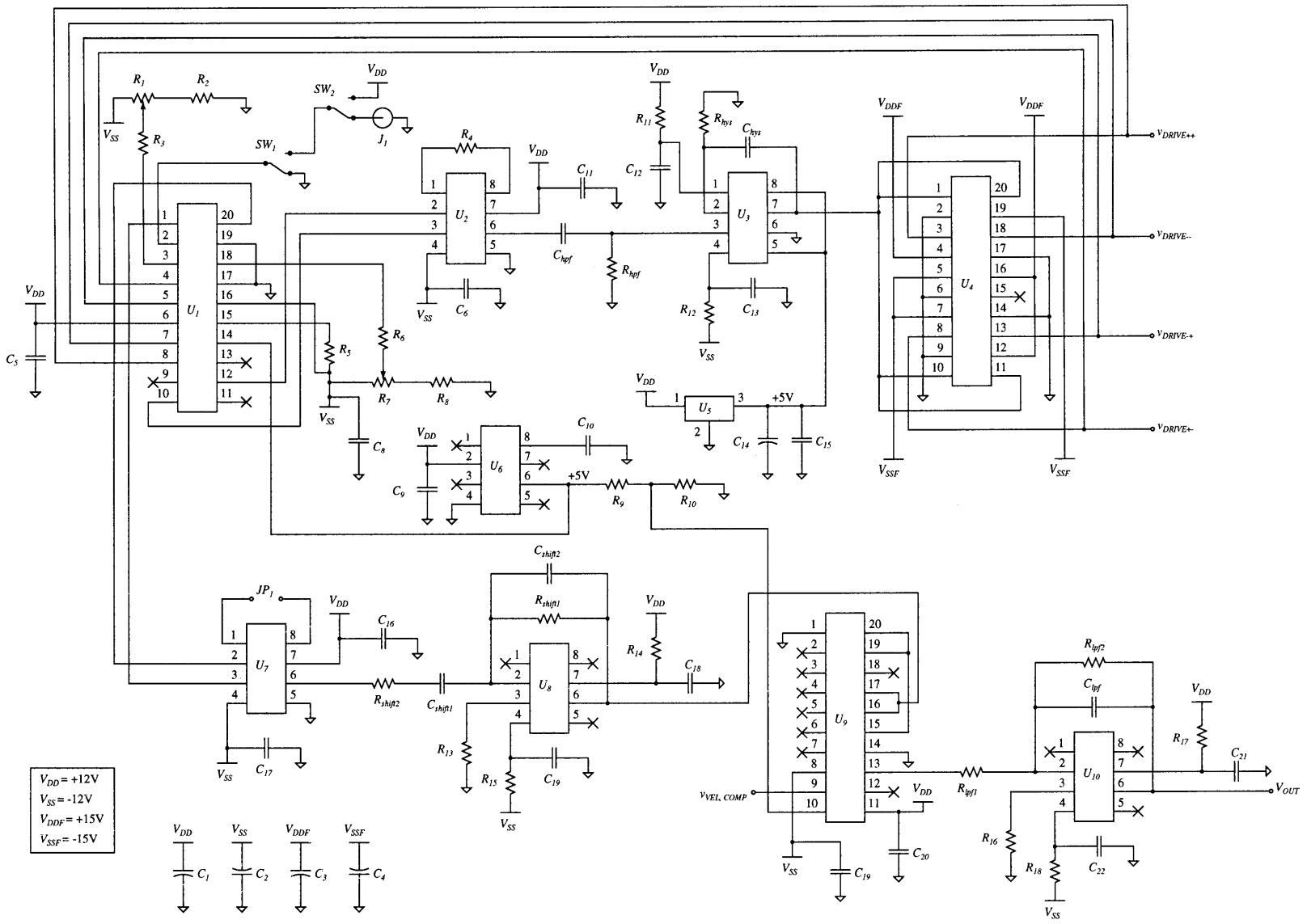
## 6.3 Printed Circuit Board

The PCB contains the ESF IC and all drive loop and sense block circuitry discussed in Chapters 4 and 5. The full schematic for the PCB is given in Figure 6-8. The descriptions for all ICs on the PCB are given in Table 6.2, while the values for all passive components are captured in Tables 6.3 and 6.4. A photograph of the PCB can be found in Figure 6-9.

The ESF IC is identified as  $U_1$ . The drive loop ICs consist of  $U_2$ – $U_5$ , which represent the instrumentation amplifier, comparator, level-shifter, and +5 V voltage regulator, respectively. Component  $U_6$  is the +5 V precision voltage reference that provides  $V_{BIAS}$  for the drive loop transresistance amplifiers, as well as the reference voltage that, after passing through a voltage divider, becomes the +2.5 V input voltage to the demodulator. The sense block ICs include  $U_7$ – $U_{10}$ , which are the instrumentation amplifier, phase-shifter op amp, demodulator, and low-pass-filter op amp, respectively.

All resistors and capacitors with non-numeric subscripts have functions that were previously discussed in Chapters 4 and 5. Of the numbered resistors,  $R_1$ – $R_3$  and  $R_6$ – $R_8$  form the offset null potentiometers and resistors for the  $C_{sense+}$  and  $C_{sense-}$  op amps, respectively. Resistor  $R_4$  sets the gain of the drive-loop instrumentation amplifier  $U_2$  to  $G = 10$ , while  $R_5$  sets the reference current for each of the four ESF op amps to  $10\ \mu\text{A}$ . Resistors  $R_9$  and  $R_{10}$  form the voltage divider which halves the +5 V generated by the precision voltage reference  $U_6$  to +2.5 V. Resistors  $R_{13}$  and  $R_{16}$  are included at the non-inverting terminals of the sense block op amps  $U_8$  and  $U_{10}$  to minimize errors due to input bias current. Of the numbered capacitors,  $C_1$ – $C_4$ ,  $C_{14}$ , and  $C_{15}$  are bypass capacitors. The remaining numbered resistors and capacitors are for local high-frequency filtering of the power supplies.

Components  $SW_1$  and  $SW_2$  are mechanical SPDT switches used to switch  $v_{RESET}$  between GND,  $V_{DD}$ , and a drive waveform given approximately by Figure 5-9 and provided by an external pulse generator. The signal is brought to the PCB via a BNC connector  $J_1$ .



$V_{DD} = +12V$   
 $V_{SS} = -12V$   
 $V_{DDF} = +15V$   
 $V_{SSF} = -15V$

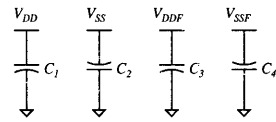


Figure 6-8: Complete schematic of the PCB circuitry.

Parameter	Component Description
$U_1$	ESF
$U_2$	AD620AN Instrumentation Amplifier
$U_3$	AD790AQ Comparator
$U_4$	ADG333ABN Quad SPDT Switch
$U_5$	LM78M05CT +5 V Regulator
$U_6$	AD586BR +5 V Precision Voltage Reference
$U_7$	AD620AN Instrumentation Amplifier
$U_8$	AD8065AR FET-Input Op Amp
$U_9$	AD630BD Demodulator
$U_{10}$	AD8065AR FET-Input Op Amp

Table 6.2: Descriptions of all of the ICs shown in the complete PCB schematic in Figure 6-8 [28], [29], [30], [33], [36], [34].

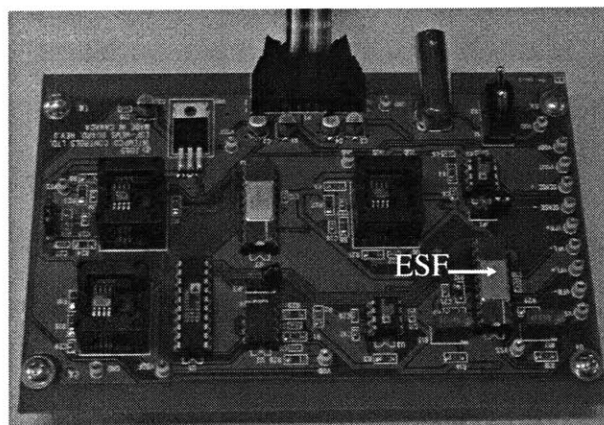


Figure 6-9: Photograph of the PCB.

Parameter	Component Description
$R_{hpf}$	100 k $\Omega$
$R_{hys}$	9.1 k $\Omega$
$R_{shift1}$	1 k $\Omega$
$R_{shift2}$	15 $\Omega$
$R_{lpf1}$	100 k $\Omega$
$R_{lpf2}$	100 k $\Omega$
$R_1$	1 k $\Omega$ potentiometer
$R_2$	1 k $\Omega$
$R_3$	910 k $\Omega$
$R_4$	5.49 k $\Omega$
$R_5$	560 k $\Omega$
$R_6$	910 k $\Omega$
$R_7$	1 k $\Omega$ potentiometer
$R_8$	1 k $\Omega$
$R_9$	10 k $\Omega$
$R_{10}$	10 k $\Omega$
$R_{11}$	51 $\Omega$
$R_{12}$	51 $\Omega$
$R_{13}$	1 k $\Omega$
$R_{14}$	51 $\Omega$
$R_{15}$	51 $\Omega$
$R_{16}$	51 k $\Omega$
$R_{17}$	51 $\Omega$
$R_{18}$	51 $\Omega$
$SW_1$	SPDT mechanical switch
$SW_2$	SPDT mechanical switch
$J_1$	BNC connector
$JP_1$	Open jumper connection

Table 6.3: Values for all of the resistors and mechanical components shown in the complete PCB schematic in Figure 6-8.

Parameter	Component Description
$C_{hpf}$	0.1 $\mu\text{F}$
$C_{hys}$	390 pF
$C_{shift1}$	10 nF
$C_{shift2}$	20 pF
$C_{lpf}$	0.1 $\mu\text{F}$
$C_1-C_4$	10 $\mu\text{F}$
$C_5-C_{13}$	0.1 $\mu\text{F}$
$C_{14}$	10 $\mu\text{F}$
$C_{15}-C_{22}$	0.1 $\mu\text{F}$

Table 6.4: Values for all of the capacitors shown in the complete PCB schematic in Figure 6-8.



## 6.4 Experimental Results

Two issues with the ESF system that arose before collecting any experimental data are discussed in Sections 6.4.1 and 6.4.2. The empirical data are presented and analyzed in Sections 6.4.3 through 6.4.7. Note that the output low-pass filter was modified to adjust its  $-3$  dB bandwidth from 15.9 Hz to approximately 100 Hz, which is the noise bandwidth high-end xerography machines, a potential application for the ESF, require.

Also, two versions of the ESF IC were fabricated for the future research benefit of Analog Devices engineers. One version, as previously discussed, had a MEMS resonant frequency of 15 kHz, while the other had a MEMS resonant frequency of 11.5 kHz. The experimental results in this section are for the lower-frequency 11.5 kHz device, as it provides a more conservative noise measurement due to its higher  $1/f$  noise content.

### 6.4.1 Current Overload Condition

Upon powering up the PCB, a current overload warning was given from the  $\pm 15$  V power supply. This overload condition was due to the forward-biasing of ESD diodes.

The ESD protection cell used for the ESF is shown in Figure 6-10, where  $D_1$  and  $D_2$  are ESD diodes, and the  $100\ \Omega$  resistor is a diffused resistor that provides additional protection. With  $V_{SS} = -12$  V applied to the substrate and  $-15$  V applied to the bond pad for a force drive voltage,  $D_2$  became forward-biased and effectively shorted the  $-12$  V and  $-15$  V supplies. Upon reducing the force drive voltages to  $\pm 12$  V, the supply overload warning disappeared.

### 6.4.2 Op-Amp Oscillations

In addition, persistent oscillations on the outputs of the sense and velocity op amps prevented any form of testing for a good amount of time. The first objective in finding the cause of the oscillations was to isolate one of the op amps from all other circuitry. As shown in Figure 6-11, one of the velocity amps was selected, and all

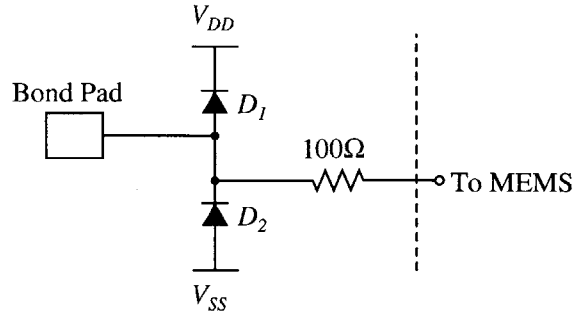


Figure 6-10: Schematic of an ESD protection cell used for the ESF.  $D_1$  and  $D_2$  are ESD diodes, and the  $100\ \Omega$  resistor is a diffused resistor that provides additional ESD protection.

interconnects between this velocity amp and the MEMS and sense op amps were severed using a laser-trim machine. This step ensured that parasitic capacitances from the MEMS or sense block circuitry would not affect the stability of the velocity op amp feedback loop. Nonetheless, with no input signal applied to the velocity op amp, the oscillations remained. Oscillations were also present on the op amp current bias pin, Pin 15. These findings suggested that the oscillations originated in the op amp current biasing, which was highly unexpected given that the biasing simply consisted of a resistor to set the current and a diode-connected MOSFET to mirror the current.

One initial suspicion was that, despite the fact that the simulations in Sections 4.6 and 5.7 suggested otherwise, the bias current was too weak to drive the output capacitances present at the amplifier outputs. This suspicion was confirmed upon placing a  $300\ \text{k}\Omega$  resistor in parallel with the external  $560\ \text{k}\Omega$  resistor that sets the reference current for all four of the on-chip op amps. The oscillations disappeared with the resulting increase in the per-op-amp reference current from  $10\ \mu\text{A}$  to  $30\ \mu\text{A}$ .

### 6.4.3 Linearity

After remedying the oscillation problem, the input-to-output linearity of the ESF was tested by applying a voltage  $V_{UNK}$  to the metal lid of the ESF IC, which creates an electric field normal to the MEMS sensor, and measuring the output voltage  $V_{OUT}$ .

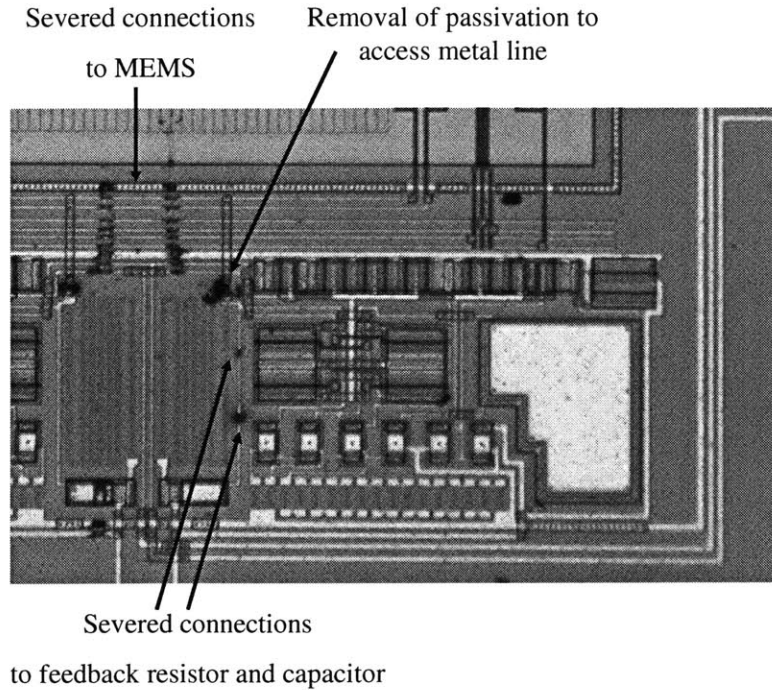


Figure 6-11: Photomicrograph of the isolated velocity op amp, with severed connections identified.

The raw data points of the  $V_{OUT}$  versus  $V_{UNK}$  measurement are shown in Figure 6-12. The dashed line is a linear, least-squares fit to the data. Oscilloscope screen captures of the ESF in steady state are given in Figures 6-13, 6-14, and 6-15.

Two initial observations of the data in Figure 6-12 are that the input-to-output relationship is highly linear and that an offset of  $-383\text{ mV}$  is present. The offset is likely due to a combination of the offset voltages of the amplifiers in the  $v_{sense}$  signal path up to  $V_{OUT}$ . Nonetheless, the offset is constant over the range of  $V_{UNK}$  and can be trimmed out in measurement. After removing the offset error, the integral nonlinearity (INL) error of the ESF based on the best-fit curve in Figure 6-12 is  $20\text{ mV}$  (using the data point at  $V_{UNK} = -350\text{ V}$ ). Note that the nulling procedure for the on-chip op-amp offset voltages was not performed since any offsets in the op amps were negligible compared to the  $-383\text{ mV}$  offset at the output.

The slope of the best-fit curve, which represents the constant of proportionality from input-to-output, is  $4.68 \times 10^{-3}$ . This value is 65.6% of the theoretical constant

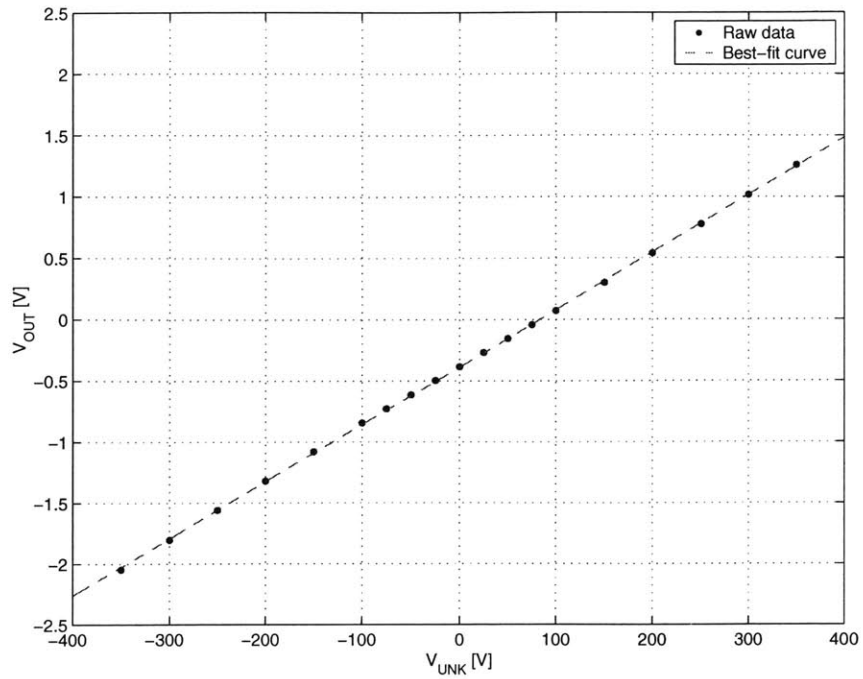


Figure 6-12: Plot of the raw data from the  $V_{OUT}$  versus  $V_{UNK}$  measurement. The dashed line is a linear, least-squares fit to the data, with a slope of  $4.68 \times 10^{-3}$  and offset of  $-383$  mV. The integral nonlinearity is 20 mV.

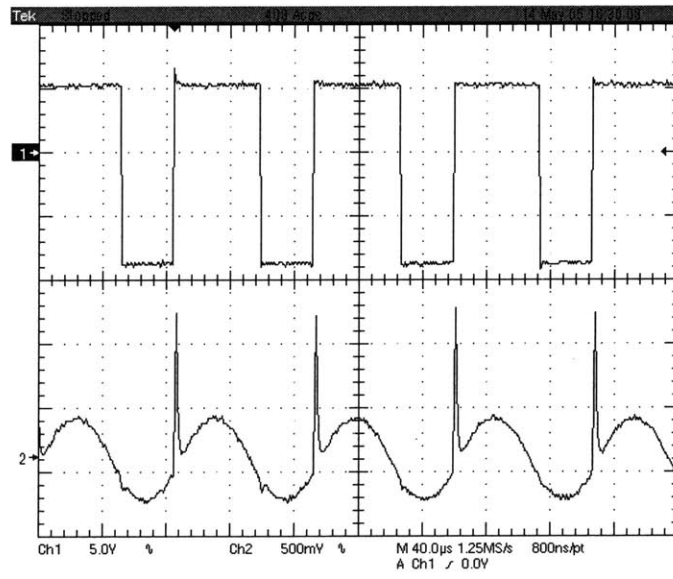


Figure 6-13: Oscilloscope screen capture of  $v_{DRIVE++}$  (top waveform) and  $v_{vel,diff}$  (bottom waveform). As desired, the two waveforms are in phase. The spikes in the  $v_{vel,diff}$  waveform are due to clock feedthrough. The asymmetrical nature of the spikes is likely due to an asymmetry in the ESF IC layout.

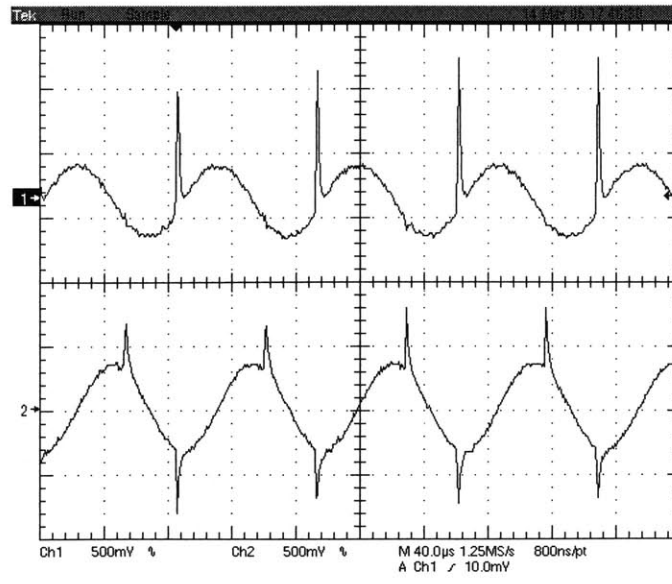


Figure 6-14: Oscilloscope screen capture of  $v_{vel,diff}$  (top waveform) and  $v_{sense,diff}$  (bottom waveform) for  $V_{UNK} = +50$  V. As desired,  $v_{vel,diff}$  leads  $v_{sense,diff}$  by  $+90^\circ$ . The  $-90^\circ$  phase shifter block will effectively bring  $v_{vel,diff}$  and  $v_{sense,diff}$  in phase for the demodulation. The spikes in  $v_{sense,diff}$  are due to clock feedthrough.

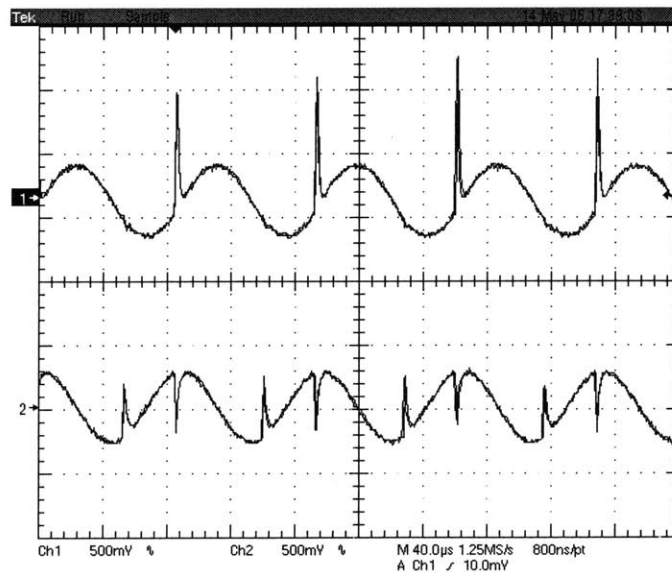


Figure 6-15: Oscilloscope screen capture of  $v_{vel,diff}$  (top waveform) and  $v_{sense,diff}$  (bottom waveform) for  $V_{UNK} = -50$  V. As desired,  $v_{vel,diff}$  lags  $v_{sense,diff}$  by  $+90^\circ$ . The  $-90^\circ$  phase shifter block will effectively bring  $v_{vel,diff}$  and  $v_{sense,diff}$   $180^\circ$  out of phase for the demodulation, which will result in a negative voltage at  $V_{OUT}$ . The spikes in  $v_{sense,diff}$  are due to clock feedthrough.

of proportionality derived in (5.19) to be

$$\frac{V_{OUT}}{V_{UNK}} = \frac{8\alpha}{\pi} \frac{C_{sense,m}}{C_f} = 7.13 \times 10^{-3}. \quad (6.1)$$

However, the  $7.13 \times 10^{-3}$  constant assumes a value for  $C_{sense,m}$  that is based on force drive voltages of  $\pm 15$  V. With the reduced force drive voltages of  $\pm 12$  V to avoid forward-biasing the ESD diodes, the actual value for  $C_{sense,m}$  decreases to

$$C_{sense,m} = 0.4 \text{ fF} \left( \frac{12 \text{ V}}{15 \text{ V}} \right)^2 = 0.256 \text{ fF}, \quad (6.2)$$

since the the maximum displacement of the  $C_{sense}$  shutter is proportional to the square of the force drive voltages. As a result, the updated theoretical constant of proportionality with  $C_{sense,m} = 0.256$  fF is

$$\frac{V_{OUT}}{V_{UNK}} = 4.56 \times 10^{-3}, \quad (6.3)$$

which differs from the empirical constant by only 2.6%.

#### 6.4.4 Step Response

The step response of  $V_{OUT}$  for a step in  $V_{UNK}$  from 0 V to +50 V is shown in Figure 6-16. The 10%-90% rise time of the waveform is consistent with the 100 Hz  $-3$  dB bandwidth of the first-order output low-pass filter, which implies that the MEMS dynamics in no way limit the step response time.

#### 6.4.5 Input Electric Field Range

Due to limitations of the available high-voltage power supply, the input voltage  $V_{UNK}$  was only swept from  $-350$  V to  $+350$  V. Nonetheless, the functionality of the ESF over this input range gives at the very least an input electric field range of

$$E_{in,max} = \pm \frac{350 \text{ V}}{d_{sense}} = \pm \frac{350 \text{ V}}{0.5 \text{ mm}} = \pm 700 \text{ V/mm}, \quad (6.4)$$

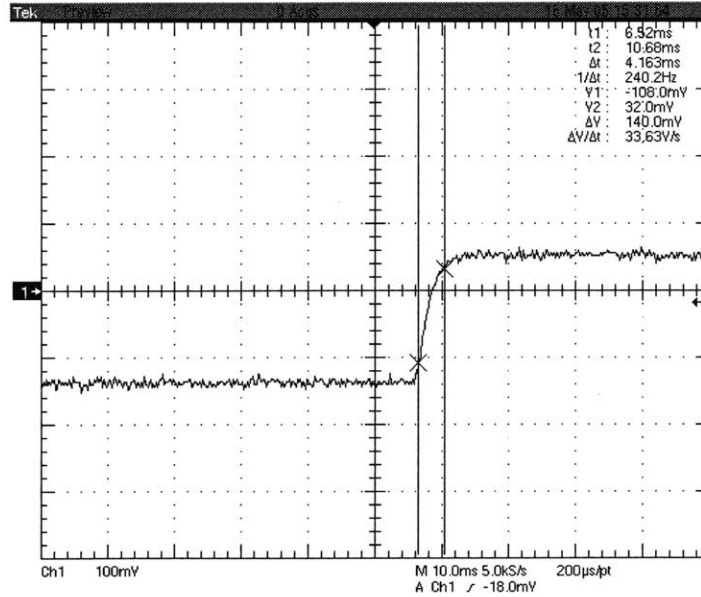


Figure 6-16: Oscilloscope screen capture of  $V_{OUT}$  for a step in  $V_{UNK}$  from 0V to +50V. The 10%-90% rise time of the waveform is consistent with the 100 Hz  $-3$  dB bandwidth of the output low-pass filter.

which meets the specification of  $\pm 500$  V/mm given in Chapter 1. This range is also an improvement over the Riehl input electric field range of  $\pm 333$  V/mm [7]. Given that  $V_{OUT}$  only varies from  $-2.0$  V to  $+1.3$  V as shown in Figure 6-12, a much larger input electric field range could be expected with a greater range of  $V_{UNK}$  since the system power supplies are  $\pm 12$  V.

#### 6.4.6 Input-Referred Electric Field Noise

The output voltage noise  $V_{n,out}(f)$  of the ESF was measured to be  $9.2 \mu\text{V}/\sqrt{\text{Hz}}$  over a frequency range of 20 Hz to 100 Hz. The measurement was performed using a Hewlett-Packard 3585B Spectrum Analyzer and a resolution bandwidth of 3 Hz. Given the empirical input-to-output gain of  $|V_{OUT}/V_{UNK}| = 4.68 \times 10^{-3}$  calculated in Section 6.4.3, the resulting input-referred voltage noise  $V_{ni}(f)$  is

$$V_{ni}(f) = \frac{V_{n,out}(f)}{|V_{OUT}/V_{UNK}|} = \frac{9.2 \mu\text{V}/\sqrt{\text{Hz}}}{4.68 \times 10^{-3}} = 2.0 \text{ mV}/\sqrt{\text{Hz}}. \quad (6.5)$$

The equivalent input-referred electric field noise  $E_{ni}(f)$  is thus

$$E_{ni}(f) = \frac{V_{ni}(f)}{d_{sense}} = \frac{2.0 \text{ mV}/\sqrt{\text{Hz}}}{0.5 \text{ mm}} = 4.0 \text{ V/m}/\sqrt{\text{Hz}}. \quad (6.6)$$

While this value meets the input-referred electric field noise specification of  $200 \text{ V/m}/\sqrt{\text{Hz}}$  given in Chapter 1, it is over an order-of-magnitude greater than the  $0.21 \text{ V/m}/\sqrt{\text{Hz}}$  value calculated in Section 5.5.1.

The reason behind this discrepancy lies with the incompleteness of the noise model used in Section 5.5.1. A simulation of one of the sense block transimpedance amplifiers revealed the noise  $V_{n,sense+}(f)$  at the output of the amplifier to be  $9.5 \mu\text{V}/\sqrt{\text{Hz}}$ , which is considerably greater than the calculated value of  $415 \text{ nV}/\sqrt{\text{Hz}}$ . An examination of the detailed results of the noise simulation indicated that the dominant noise source was the  $1/f$  noise of the diode-connected NFETs in the feedback loop. Any noise contributions from the NFETs were ignored in the noise calculations in Section 5.5.1.

Given the simulated value of  $9.5 \mu\text{V}/\sqrt{\text{Hz}}$  for  $V_{n,sense+}(f)$ , an equivalent simulated output noise voltage  $V_{n,out}(f)$  can be calculated. With respect to Figure 6-17, since  $V_{n,sense+}(f)$  and  $V_{n,sense-}(f)$  are uncorrelated,  $V_{n,sense,diff}(f)$  is given by

$$V_{n,sense,diff}(f) = \sqrt{2} V_{n,sense+}(f), \quad (6.7)$$

where it is assumed that  $V_{n,sense+}(f) = V_{n,sense-}(f)$ . The magnitude of the gain of the  $-90^\circ$  phase shifter is approximately one at 11.5 kHz (recall that the 11.5 kHz device was selected for testing), and the demodulator acts as an amplifier with a gain of two, so  $V_{n,sense,demod}(f)$  is given by

$$V_{n,sense,demod}(f) = 2\sqrt{2} V_{n,sense+}(f). \quad (6.8)$$

Lastly, the effective noise gain of the low-pass filter is  $2/\pi$ , which is the average of a rectified sine-wave. Thus, the simulated output-referred noise voltage  $V_{n,out}(f)$  is



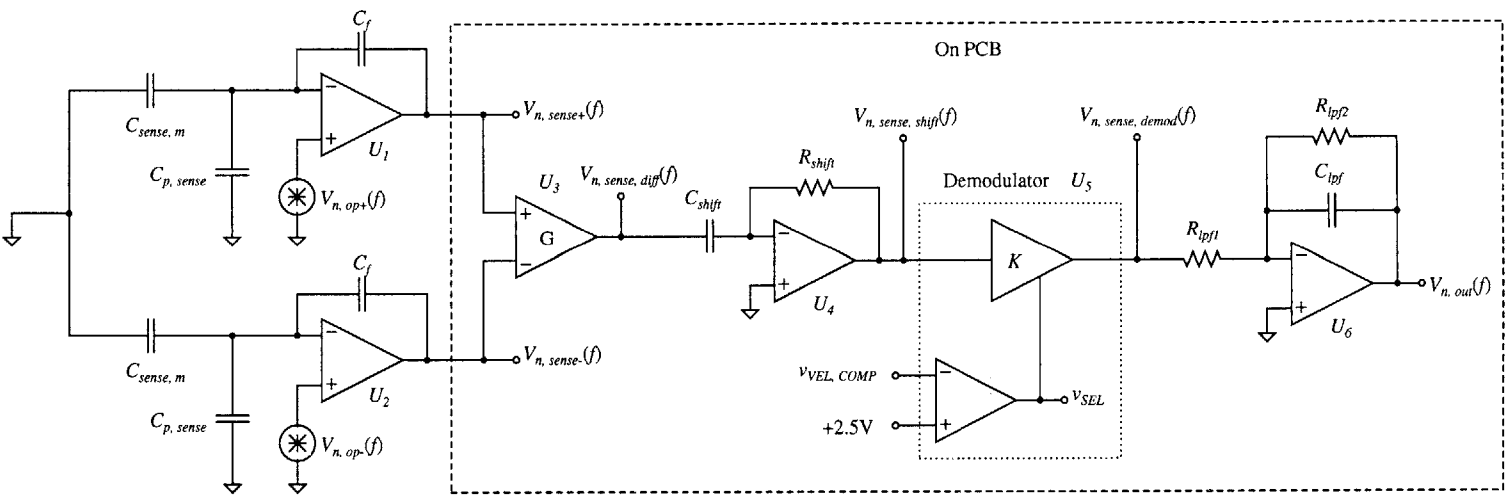


Figure 6-17: Equivalent noise circuit for the sense block.

given by

$$\begin{aligned}
 V_{n,out}(f) &= (2\sqrt{2})(2/\pi) V_{n,sense+}(f) \\
 &= (2\sqrt{2})(2/\pi) 9.5 \mu\text{V}/\sqrt{\text{Hz}} \\
 &= 17.1 \mu\text{V}/\sqrt{\text{Hz}},
 \end{aligned} \tag{6.9}$$

which is within a factor of two of the measured output-referred noise of  $9.2 \mu\text{V}/\sqrt{\text{Hz}}$ .

Since the model for  $1/f$  noise in MOSFETs in the ADICE simulation program is based on a fit to empirical data [18], and  $1/f$  noise can vary from wafer to wafer [16], this discrepancy between the simulated and experimental output-referred noise voltages is not unreasonable [37]. The difficulty in modeling  $1/f$  noise is exacerbated in MOSFETs with small drain currents, such as leakage currents, due to a larger percentage of the total number of carriers being close to the semiconductor surface [37].

#### 6.4.7 Analysis of Experimental Results

All of the performance parameters from the experimental results are captured in Table 6.5, as well as the target ESF specifications from Chapter 1 and the results of the Riehl ESF.

While a specification on the INL was not explicitly defined at the outset of the thesis, the experimental result is listed, along with the INL of the Riehl ESF. The INL of the Riehl ESF is calculated by converting the 630 V/m (rms) field error reported in [7] to an equivalent INL voltage of 378 mV by multiplying by the gap distance, 0.6 mm. As can be seen in Table 6.5, the collected data verify that the two critical performance specifications — input-referred electric field noise and input electric field range — are met.

Although not tested, based on the temperature ratings of all of the PCB components, as well as the simulated stability in Section 3.3.4 of the on-chip op amps over temperature, the ESF is expected to maintain functionality over the specified temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Parameters	Target Specifications	Results of Riehl ESF	Experimental Results
Input-Referred Noise	200 V/m/ $\sqrt{\text{Hz}}$	700 V/m/ $\sqrt{\text{Hz}}$	4.0 V/m/ $\sqrt{\text{Hz}}$
Input Electric Field Range	$\pm 500$ V/mm	$\pm 333$ V/mm	$\pm 700$ V/mm
Integral Nonlinearity (INL)	–	378 mV	20 mV
Nominal Gap Distance	0.5 mm	0.6 mm	0.5 mm
Supply Voltages	$\pm 15$ V	+ 20 V	$\pm 12$ V
Temperature Range	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	–	–

Table 6.5: Target performance specifications, results of the Riehl ESF, and experimental results of the thesis ESF. The input-referred noise and input electric field range specifications are satisfied based on the empirical data.

## 6.5 Summary

The ESF IC is packaged in a 20-pin DIP and consists of the MEMS structure, the transresistance amplifiers of the drive loop, and the transimpedance amplifiers of the sense block. It is imperative that these front-end amplifiers are on-chip to prevent parasitic capacitances external to the IC from acting in parallel with  $C_{p,vel}$  and  $C_{p,sense}$ . All other drive loop and sense block electronics are off-chip on a PCB for ease of debugging.

An initial issue with the testing of the ESF system was a current overload condition due to the forward-biasing of the ESD protection diodes. This issue was remedied by reducing the force drive voltages from  $\pm 15\text{V}$  to  $\pm 12\text{V}$ . The cause of the op-amp oscillations was determined to be a bias current that was too weak to drive the capacitances present at the amplifier outputs. This problem was solved by externally increasing the per-op-amp reference current from  $10\ \mu\text{A}$  to  $30\ \mu\text{A}$ .

The critical performance specifications for the ESF are its input-referred electric field noise and input electric field range. Experimental testing of the ESF verified that, with an input-referred noise of  $4.0\ \text{V}/\text{m}/\sqrt{\text{Hz}}$  and an input electric field range of  $\pm 700\ \text{V}/\text{mm}$ , the ESF meets both of the critical performance specifications outlined in Chapter 1. The ESF also features an integral nonlinearity (INL) of  $20\ \text{mV}$  over the measured input electric field range. All three of these parameters are significant improvements over the Riehl ESF.

# Chapter 7

## Conclusion

### 7.1 Design Summary

The three sub-systems of the ESF include the MEMS capacitive sensor, the drive loop, and the sense block.

The MEMS capacitive sensor produces a dynamic current that is proportional to the magnitude and polarity of the incident electric field. This current is then converted to a voltage and processed by the sense block. The modulation of the shutter position generates the dynamic current. The force and velocity capacitances are two auxiliary MEMS capacitances. The force capacitance provides for the electrostatic force actuation of the shutter, while the velocity capacitance generates a dynamic current proportional to the shutter velocity. This velocity current serves as an input to the drive loop, which ensures resonant operation of the MEMS sensor. A frequency-domain analysis of the MEMS structure dynamics revealed its high- $Q$  nature and the fortunate and useful result that the force drive and shutter velocity are in phase at resonance.

The thesis goal of implementing a high-accuracy ESF requires a low-noise operational amplifier at the front-end of the sense block electronics. The noise performance of this op amp ultimately determines the electric field sensing resolution of the ESF. A low-noise, BiCMOS op amp was developed that features an input-referred noise of  $9.65 \text{ nV}/\sqrt{\text{Hz}}$  at 15 kHz. The input stage of the op amp was optimized for low-noise

operation by emitter-degenerating the active current mirror transistors. An offset nulling scheme was developed to minimize the magnitude of the parasitic electric field that arises due to the op amp offset voltage.

The function of the drive loop is to drive the MEMS sensor at its resonant frequency for maximum shutter displacement. The drive loop implementation used in this thesis exploits the fact that the force drive waveform and shutter velocity are in phase only at resonance. A describing function analysis of the loop verified the presence of limit cycles, and, thus, confirmed the stability of the loop. Lead compensation was introduced to increase the stability of the local transresistance amplifier loops given the parasitic capacitances from the MEMS velocity capacitance electrodes to the substrate.

The sense block performs the measurement of the incident electric field by converting the dynamic currents generated by the sense capacitance into a dc output voltage that is proportional to the electric field. The sub-blocks include transimpedance amplifiers, a  $-90^\circ$  phase shifter, a demodulator, and a low-pass filter. DC feedback and lead compensation were added to the transimpedance amplifiers and  $-90^\circ$  phase shifter, respectively, to increase loop stability.

The MEMS structure, along with the transresistance amplifiers of the drive loop and the transimpedance amplifiers of the sense block, are contained on an integrated circuit fabricated using the Analog Devices iMEMS process. The IC is packaged in a 20-pin DIP. All other electronics are off-chip on a PCB.

## 7.2 Results Summary

### 7.2.1 Theoretical Results

The two critical performance specifications of the ESF are its input-referred electric field noise and its input electric field range. The thesis specifications outlined in Chapter 1 are an input-referred electric field noise of  $200 \text{ V/m}/\sqrt{\text{Hz}}$  and an input electric field range of  $\pm 500 \text{ V/mm}$ .

Based on both simulations and calculations detailed in Section 5.5, the theoretical values for the input-referred noise and input electric field range are  $0.21 \text{ V/m}/\sqrt{\text{Hz}}$  and  $\pm 1790 \text{ V/mm}$ , respectively. Both values clearly meet the specifications given in Chapter 1. In addition, both theoretical values are improvements over the values of  $700 \text{ V/m}/\sqrt{\text{Hz}}$  and  $\pm 333 \text{ V/mm}$  given in the Riehl thesis.

## 7.2.2 Experimental Results

The experimental values for the input-referred electric field noise and input electric field range are  $4.0 \text{ V/m}/\sqrt{\text{Hz}}$  and  $\pm 700 \text{ V/mm}$ , respectively. Both of these values meet the critical performance specifications outlined in Chapter 1. Also, while a specification on the integral nonlinearity (INL) was not explicitly defined at the outset of the thesis, the INL of the ESF over the measured input electric field range was  $20 \text{ mV}$ , while the Riehl ESF featured an INL of  $378 \text{ mV}$ . All three of these parameters are significant improvements over the Riehl ESF.

The measured input-referred noise is considerably greater than the calculated value due to incomplete modeling of all noise sources in the sense block transimpedance amplifier circuit. While the diode-connected NFETs were assumed to contribute no noise, the  $1/f$  noise of the NFETs was actually the dominant noise source. When the  $1/f$  noise is included in the noise model for the sense block, the measured and theoretical input-referred noise values correspond to within a factor of two.

## 7.3 Future Work

Three subsequent steps are recommended for a more complete characterization of the ESF. First, the performance of the ESF should be investigated over a wider range of input electric fields and force drive voltages. The expected maximum allowable force drive voltages are  $\pm 15 \text{ V}$ , given that the the breakdown voltage of the ESD protection circuitry is  $30 \text{ V}$ . Second, the cause of the  $-383 \text{ mV}$  offset present at the ESF output should be determined and remedied. Lastly, the performance of the ESF should be evaluated over the specified temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

After the ESF is fully characterized, further improvements to the ESF may be implemented in future design iterations. The following improvements assume that one of the ultimate future design goals is to integrate the entire ESF system onto one IC and to have the IC powered by a single supply, notated as  $V_{DD}$ .

One possible improvement is to move to true fully-differential op amps for the front-end amplifiers in the drive loop and sense block. A true fully-differential implementation would allow for better circuit symmetry, thereby improving clock feedthrough and substrate noise rejection. Clock feedthrough rejection is especially critical given the large ( $\pm 12\text{ V}$  to  $\pm 15\text{ V}$ ) force drive voltages present on-chip.

The primary challenge in moving to fully-differential op amps, however, is the design of the common-mode feedback circuitry. Although switched-capacitor common-mode feedback circuits are typically reserved for switched-capacitor systems [15], a switched-capacitor common-mode feedback implementation could be considered for the ESF. Any clock feedthrough due to the common-mode feedback circuitry would be negligible compared to the clock feedthrough contribution of the force drive voltages.

Another potential improvement lies with the current biasing scheme of the low-noise op amp. As discussed in Section 3.3.2 and shown in Figure 7-1(a), the current biasing scheme consists of an off-chip resistor and diode-connected transistor that acts as a current mirror. The transconductance of  $M_1$  is given by

$$\begin{aligned} g_{m1} &= 2 \mu_p C_{ox} (W/L)_1 (V_{SG1} + V_T) \\ &= 2 \mu_p C_{ox} (W/L)_1 (V_{DD} - V_{G1} + V_T), \end{aligned} \quad (7.1)$$

where  $V_T = V_{T0}$ . While appropriate for the prototype ESF in this thesis, such a biasing scheme is not independent of power supply voltage ( $V_{DD}$ ), process variations ( $C_{ox}$ ,  $V_T$ ), or temperature ( $\mu_p$ ). A biasing circuit that generates a stable transconductance is analyzed in [15] and shown in Figure 7-1(b). If  $M_1$  and  $M_2$  are matched



transistors, then the transconductance of  $M_2$  is given by

$$g_{m2} = \sqrt{\frac{\mu_p}{\mu_n} \frac{(W/L)_2}{(W/L)_6}} \cdot \frac{2 \left(1 - \sqrt{\frac{(W/L)_6}{(W/L)_5}}\right)}{R_1}. \quad (7.2)$$

To first-order,  $g_{m2}$  is independent of supply voltage, process variations, and temperature, and is determined solely by the  $W/L$  ratios of the transistors in the bias network.

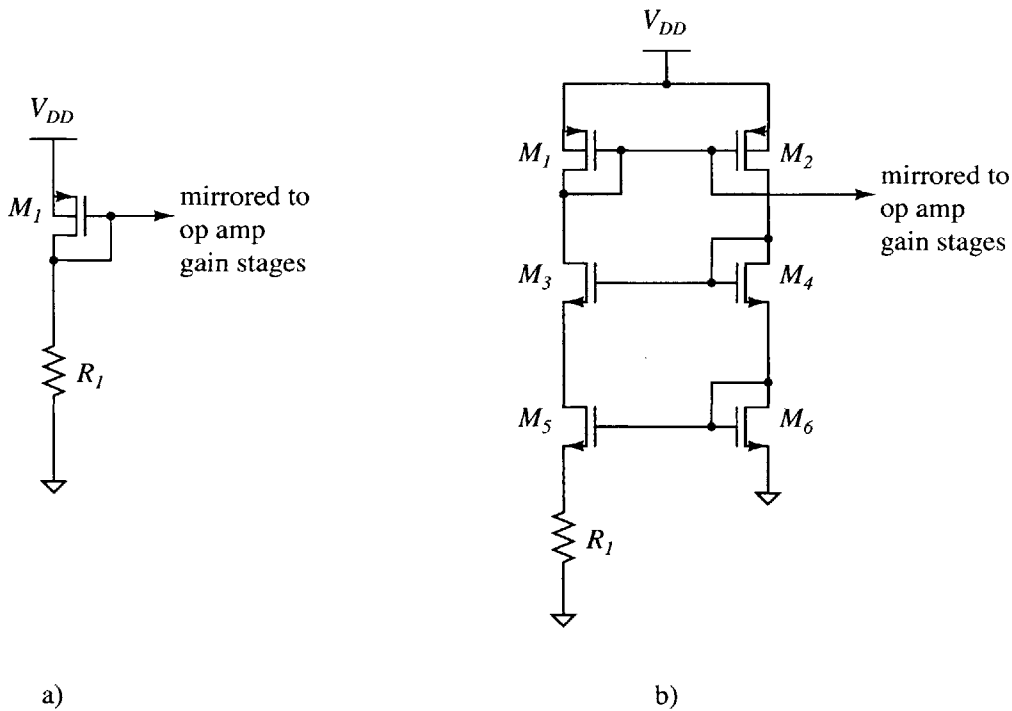


Figure 7-1: (a) Schematic of the op amp biasing scheme used for the low-noise op amp. (b) Schematic of the improved, stable transconductance biasing scheme.

In addition, while the simulated results illustrated the effectiveness of the op amp offset-nulling method discussed in Section 3.3.3, such a scheme would not be suitable for a future product-line ESF. Since the offset voltage is temperature dependent, the offset voltage would require re-nulling with every change in ambient temperature. Possible techniques for reducing the offset voltage to an acceptable (less than  $400 \mu\text{V}$ ) level include autozeroing schemes and laser-trimming of the input stage emitter-degeneration resistors.

Three offset-reduction techniques are presented in [25]: autozeroing, correlated double sampling, and chopper stabilization. Both autozeroing and correlated double sampling include at least one clock phase of sampling the offset voltage onto a capacitor. The offset is then effectively cancelled out during the signal processing clock phase. Chopper stabilization uses modulation/demodulation techniques to cancel out the offset voltage. However, chopper stabilization would not be recommended for the ESF front-end amplifiers due to the high source impedances generated by the MEMS capacitances [38]. All three of these techniques also reduce low-frequency  $1/f$  noise.

Laser-trimming of the input stage emitter-degeneration resistors is another offset-reduction method. As discussed in [39], a resistor ladder consisting of implant resistors separated by low-resistance TiW metal links would form one effective emitter-degeneration resistor. The offset voltage is measured, and the metal links are laser-cut in succession until the offset is below some threshold. The authors of [39] achieved post-trim offset voltages of less than  $\pm 10 \mu\text{V}$  using this technique. A similar method using polysilicon fuses in place of the TiW links could also be employed [40].

Lastly, while the  $\pm 15 \text{ V}$  (later reduced to  $\pm 12 \text{ V}$ ) force drive voltages for this thesis ESF were generated externally using a separate power supply, the presence of such large supply voltages may not be an option for a future product-line ESF. For instance, the maximum supply voltages for the ADXL190 accelerometer and ADXRS150 gyroscope are both  $+5.25 \text{ V}$  [5], [6]. One method of generating voltages that are larger than the maximum supply is through a Dickson charge pump [41]. The schematic of a Dickson charge pump that acts as a voltage-quadrupler is shown in Figure 7-2. Such a charge pump could be used for the case of generating approximately  $+17.6 \text{ V}$  from a  $V_{DD} = +5 \text{ V}$  supply. Charge is pumped along the diode chain as the capacitors are sequentially charged and discharged. The output voltage is given by

$$V_{OUT} = N (V_{DD} - V_{DIODE}), \quad (7.3)$$

where  $N$  is the number of stages and  $V_{DIODE}$  represents the diode voltage drop. Also, the effects of stray capacitance to the substrate are ignored, and a high load

impedance is assumed. For the charge pump shown in Figure 7-2, and for  $V_{DD} = +5\text{ V}$  and  $V_{DIODE} = 0.6\text{ V}$ , the output voltage of the charge pump is

$$V_{OUT} = N (V_{DD} - V_{DIODE}) = 4 (5\text{ V} - 0.6\text{ V}) = +17.6\text{ V}, \quad (7.4)$$

which is a suitable force drive voltage.

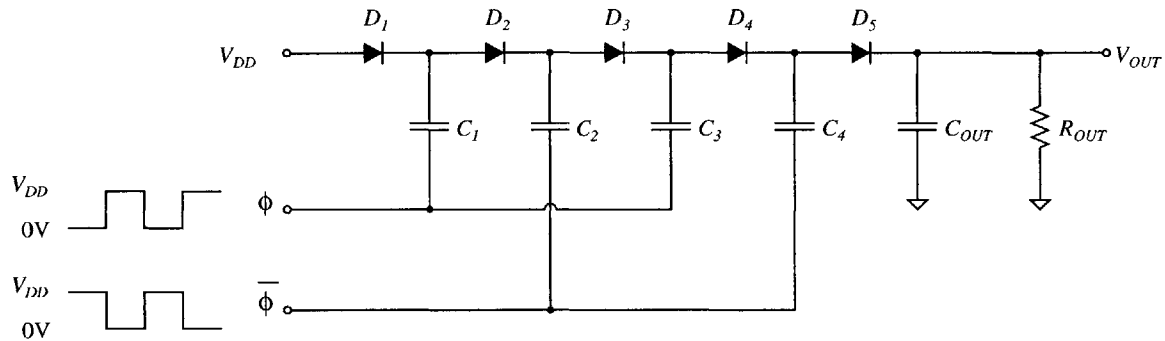


Figure 7-2: Schematic of a Dickson charge pump that generates approximately +17.6 V from  $V_{DD} = +5\text{ V}$ .

## 7.4 Concluding Discussion

The ESF presented in this thesis is an improvement in at least three different parameters over the one presented in the Riehl thesis, which is the current state-of-the-art ESF. It is also the world's first-known self-resonant ESF. By maintaining the vibration of the shutter at the resonant frequency of the MEMS sensor, the shutter experiences maximal displacement, which gives rise to a larger signal-to-noise ratio and explains its excellent noise performance. The measured input-referred electric field noise of  $4.0 \text{ V/m}/\sqrt{\text{Hz}}$  is over two orders of magnitude lower than the input-referred noise of  $700 \text{ V/m}/\sqrt{\text{Hz}}$  featured by the Riehl ESF.

Based on its promising experimental results, it is hopeful that, after implementing the aforementioned improvements, the ESF will evolve into a fully-integrated, high-performance MEMS inertial sensor.

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