Characterization of Organic Field Effect Transistors for OLED Displays

by

Kyungbum Ryu
B.S. Electrical Engineering
The Cooper Union, May 2003

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

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Abstract

This thesis explores the characterization of OFETs that will aid the circuit design of OLED pixel drivers. The contact resistance, flat band voltage, and mobility are extracted from top contact and bottom contact transistors with current-voltage (I-V) and low frequency capacitance-voltage (C-V) measurements. Extraction of contact resistance is found to be crucial in characterization of bottom-contact transistors as it obscures mobility extraction. An unambiguous method of extracting flat band voltage is explored and mobility is extracted with minimal assumptions by separation of charge and mobility from C-V measurements. Mobility is found to increase with gate voltage differing significantly from mobility dependence in crystal silicon MOSFETs.

Thesis Supervisor: Charles G. Sodini
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Contents

List of Figures

Chapter 1

Introduction

The field of organic electronics is evolving rapidly. Driven by many promising commercial applications such as inexpensive photovoltaic cells, better flat panel displays, and inexpensive large-area circuits and sensors, research is carried out in many areas that range from theory to organic electronic systems.

Organic field-effect transistors (OFETs), which use thin films of organic semiconductors, are interesting because of their capability to make large-area flexible circuits on plastics. In addition, their low processing temperatures and the wide variety of organic semiconductors enable them to be compatible with various flexible substrates. Functional devices on flexible plastics, paper, and cloth have been demonstrated by Jackson, et al. and Klauk, et al. [1], [2]. In addition, organic materials may be printed via ink-jet or roll-to-roll printing which can greatly reduce fabrication cost.

Due to these promising applications and the potential for low cost circuits, the number of research papers pertaining to OFETs is increasing rapidly, and new conferences that focus on OFETs have emerged. Currently, research is simultaneously performed on all levels from device physics to the design of functional circuits like decoders and AMLCD backplanes, but the focus is shifting from device fabrication towards circuit applications. This thesis explores the characterization of OFETs, which will identify OFET performance bottlenecks and aid the design of OLED pixel drivers for the optical feedback OLED display detailed in section 2.1.

There has been an effort to standardize the methods for characterizing OFETs be-

cause different characteristics result from the same device depending on measurement conditions, such as sweep time and hold time. This effort resulted in a consortium of leading OFET researchers to publish the IEEE standard 1620-2004, *IEEE Standard Methods for Characterization of Organic Transistors and Materials* [3]. The standard discusses the definitions of common abbreviations and terms, cautions to be taken when characterizing OFETs, and minimum requirements for reporting device characteristics. Although the standard is a good stepping-stone, it has many shortcomings.

First, the standard suggests mobility and threshold voltage extraction based on long-channel silicon MOSFET equations. As of now, there is no widely accepted model for OFET I-V characteristics. The most widely employed method of extracting OFET parameters is the curve fitting of I-V characteristics to models of single crystal silicon MOSFETs. Though such parameters may be simple and quick to provide a measure of the device performance, they are of limited use when predicting comprehensive circuit behaviors.

In addition, the standard does not specify a method to determine the contact resistance. Contact resistance in OFETs is high because the metal contacts to the semiconductor are non-ohmic and must be determined in order to correctly model I-V characteristics. This research focuses on the extraction of OFET contact resistance and mobility, based on physical principles.

This thesis is organized as follows: Chapter 2 introduces the optical feedback OLED project and the basic structure and operation of an OFET. Chapter 3 discusses a characterization method of OFETs using C-V, I-V characteristics, and its fundamental physics. It also discusses issues of non-ideal OFET characteristics. Finally, chapter 4 draws conclusions.

Chapter 2

Background

OFETs in this project are characterized with the specific goal of using them in an OLED display. Compatible fabrication processes of OFETs and OLEDs enable a combination of the two technologies to build large-area flexible displays. Specifically, the OFETs are to be used in MIT's optical feedback OLED display which will be described in the following section.

2.1 Optical Feedback OLED Display

Organic light emitting diodes (OLEDs) is a promising new technology that can be used to build large, thin, and flexible displays. Instead of filtering light like LCDs, OLEDs emit light, which increases the contrast, decreases the response time, and eliminates the need for back-lights. Thus we can make thinner digital flat panel displays with better picture quality. However, OLEDs exhibit non-linear light output characteristics, and their power efficiency degrades over usage which leads to burn-in type image artifacts as shown in Figure 2-1. The human eye is highly sensitive to such undesirable artifacts and can distinguish the effect even when the pixels are only 1% different in brightness. The 5% degradation in brightness intensities, the maximum acceptable error, occurs at operation time of 2000 hours for constant current driven efficient phosphorescent $Ir(ppy)_3$ OLED run at brightness of 200 cd/m^2 [4]. Such pixel aging poses as the key limiting factor in the usable lifetime of the OLED display.

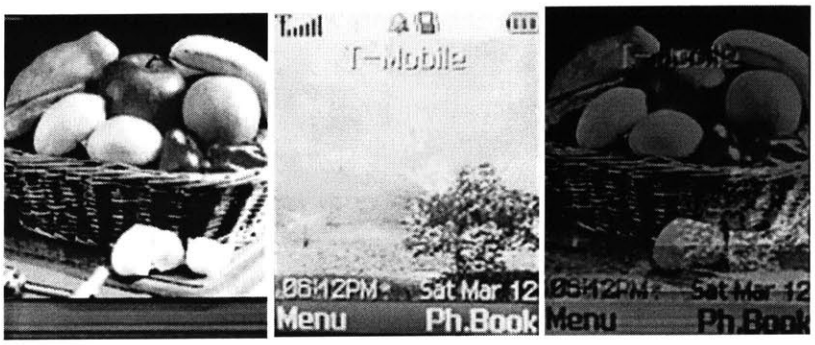

Figure 2-1: A sample image which shows burn-in artifacts. The perfect image on the left is degraded to the image on the right when the image in the center is displayed for a long time. The degradation is most severe in pixels that have the highest intensity brightness in the center image.

We propose to drive OLEDs to the desired brightness by using optical feedback from photo-detectors behind individual pixels. One may question the effectiveness of the optical feedback because it will accelerate the degradation of the OLEDs by driving it at a higher current. However, preliminary research [5] showed that optical feedback indeed increased the effective lifetime by tenfold. Figure 2-2 shows the brightness degradation as the OLED is driven in constant current at three different driving currents and consequently, three different brightnesses. The bottom curves show that the voltage required to drive the OLED increases over time at a set current, and the top curves show that at constant current, the light intensity degrades over time. From this data, we determine that the usable lifetime of the OLED display at a worst-case scenario is 2000 hours at brightness of 200 cd/m^2. Figure 2-3 combines I-V, EL intensity vs. current, and EL intensity vs. time measurements from [4] to show that when the driving voltage is allowed to change from 7 to 12 volts, the OLED lifetime can be extended to 27,000 hours at 200 cd/m^2. This is a more than a tenfold increase in lifetime, and similar lifetime increases can be seen at different brightnesses.

Currently at MIT there are efforts to build a complete feedback system that encompasses the design and fabrication of an integrated silicon control chip and an organic pixel/imager array, which together will form a stable, usable display with

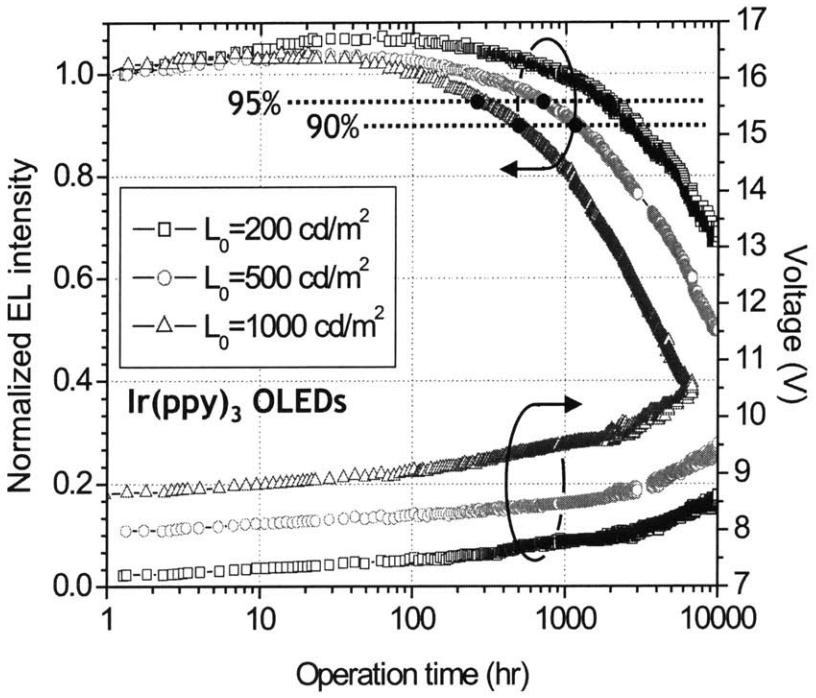

Figure 2-2: OLED EL efficiency drift as a function of time in $Ir(ppy)_3$ phosphorescent OLEDs [4].

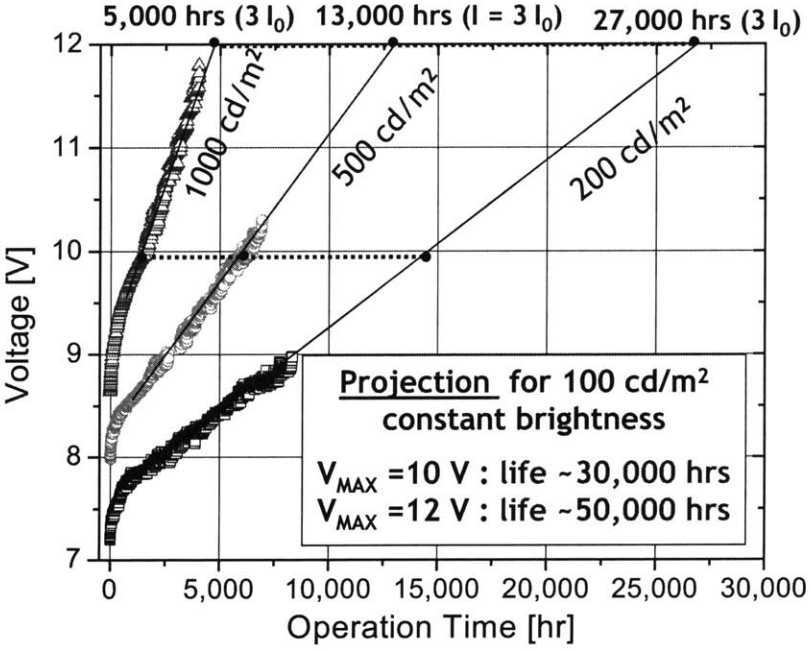

Figure 2-3: Voltage increase in optical feedback OLEDs [5].

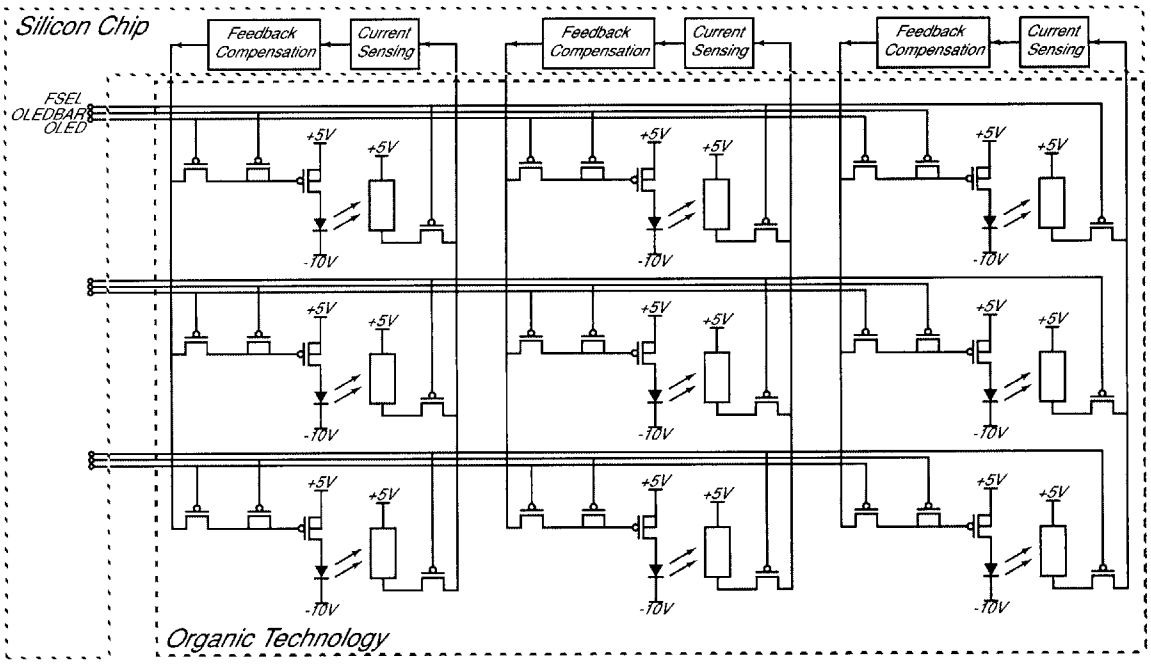

Figure 2-4: A sample 3x3 array of the pixel/imager array. The pixels on a single row are driven simultaneously in a column-parallel architecture. The various select line and the feedback compensation are fabricated on an integrated silicon chip off the backplane. The pixel/imager array consists of OLEDs, OFETs, and organic photoconductors fabricated by an integrated organic technology developed by I. Kymissis [6].

tenfold longer lifetime (Figure 2-4).

In the pixel/imager array, OFET current sources and switches are needed to drive and address one OLED pixel at a time. Figure 2-5 shows a preliminary circuit that combines the switch and the simplest current source, the common-source amplifier operating in saturation. Transistors M1 and M2 form a switch that controls the current flowing through M3. M2 is the dummy transistor that serves to hold the voltage at the gate of M3 constant when M1 is switched off by mitigating the effects of charge injection [7]. In order for the switch to be useful, M1 has to hold the charge at M3 stable until the next time the pixel is refreshed, which requires M1 to have a low leakage current. It is preferable that M3 has high enough mobility so that it can pass sufficient current to drive large area OLEDs to achieve a high fill factor. In addition, it is preferable to have a low subthreshold slope so that the OLEDs can

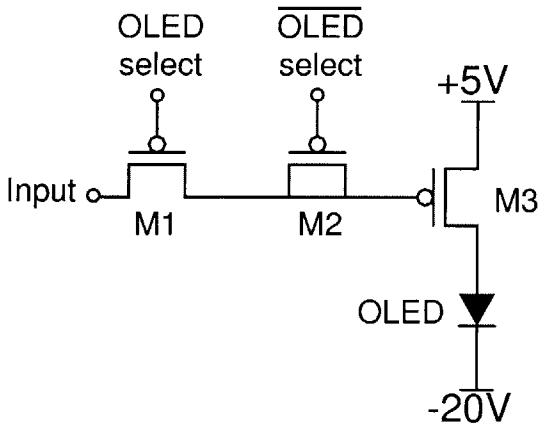

Figure 2-5: A preliminary OLED driver that will be made out of OFETs.

be driven with low voltages compatible with standard integrated CMOS circuits and reduce power dissipation. This project aims to characterize OFETs to aid the design of a more accurate driver that preserves the stability of the OLED output.

2.2 Organic Field-Effect Transistors

Electronic properties of organic materials have been studied for use in electronic devices as early as the 1940s [8]. Because of the rapid development in silicon devices, interest declined in organic electronics, but it has been revived in 1987 when C. Tang reported fabrication of a low voltage, highly efficient OLED. For more than a decade now, organic field effect transistors based on organic molecules, or conjugated polymers have been envisioned as complementary/alternative materials for silicon in large-area thin-film transistors. The processing characteristics and demonstrated performance of OFETs suggest that they can be competitive for novel thin-film transistor applications that require large-area coverage, structural flexibility, low-temperature processing, and low cost. Applications that are being considered include circuits for active-matrix OLED displays, low-end smart cards, and radio-frequency identification tags.

The structure of an OFET is similar to that of a traditional silicon metal-oxide-semiconductor field effect transistor (MOSFET). Figure 2-6 shows the structures of

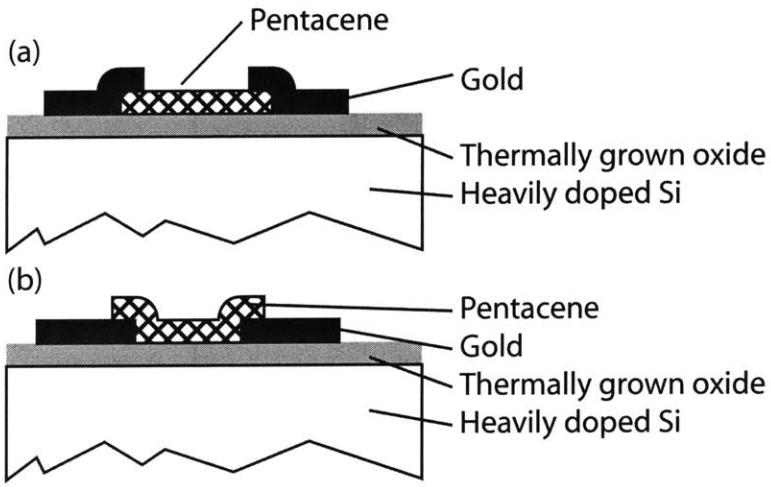

Figure 2-6: Structure of (a) a top contact OFET (b) a bottom contact OFET.

common top contact and bottom contact OFETs. The structures are inverted in the sense that the channel and the source/drain are on top of the gate, in contrast to silicon MOSFETs. The heavily doped silicon substrate at the bottom serves a dual function of the gate electrode and mechanical support. The silicon dioxide is the insulator, the pentacene is the channel layer, and the gold is the source/drain electrode. These transistors are also called thin-film-transistors, because structurally, the channel material is a vacuum-deposited thin film (about 100 nm). This type of transistors is widely used in display backplanes, because large-area single crystalline silicon wafers are difficult to fabricate. Operation-wise, these transistors are field effect transistors; they operate by changing the conductance of the channel by modulating the charge with the gate field. OFETs with degenerately doped silicon gates are widely used in research because of the ease of fabrication and the availability of silicon wafers.

Structurally, OFETs are classified as top contact and bottom contact transistors depending on where the contact is located relative to the channel. Figure 2-6(a) is a structure of a top contact transistor, and Figure 2-6(b) is that of a bottom contact transistor. Top contact transistors report better performance, which is attributed to a smaller contact resistance.

In this thesis, we will characterize top contact OFETs fabricated on silicon wafers

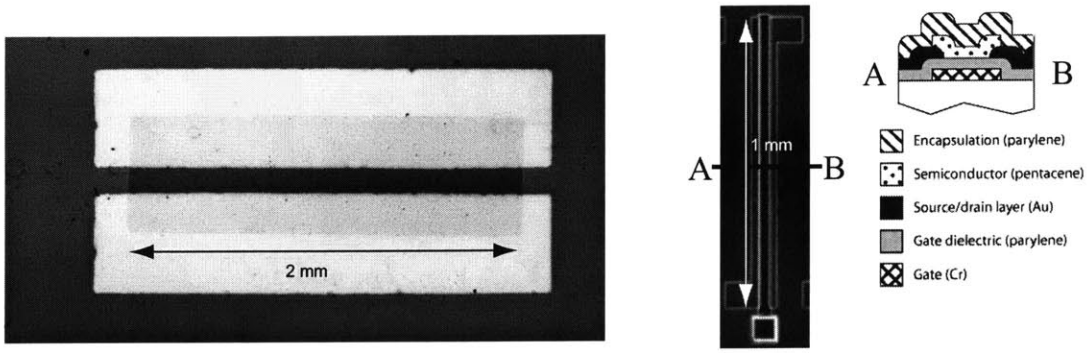

Figure 2-7: (Left) The photo of the shadow mask patterned top contact transistor (Set 1). (Right) The photo of the lithographically patterned bottom contact transistor (Set 2).

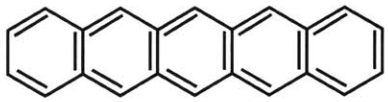

Figure 2-8: Structure of pentacene

and bottom contact OFETs on glass. The former set of transistors was patterned by shadow masks made from Photo Etch Technology, and the latter set was patterned by lithography. For convenience, we will refer to the top contact OFETs as Set 1 and the bottom contact OFETs as Set 2. Because of the limitation in each technology, the shortest channel lengths achievable are 50 μm and 5 μm in the shadow mask and lithographically patterned transistors, respectively. Detailed fabrication procedures and physical descriptions are available in Appendix A.

All the transistors characterized in this research use pentacene as the semiconductor, since it is one of the most widely studied organic electronic materials and has been reported to have good mobility. Figure 2-8 shows the chemical structure of pentacene. It is a conjugated molecule with five benzene rings. Electronic transport over macroscopic scale is possible in this type of materials because there is a direct overlap between the extended π orbitals on neighboring molecules. The majority carriers in pentacene are holes and hence pentacene is a p-type material. Additionally, electron mobility is a lot lower than hole mobility [9], so most pentacene OFETs are pFETs, and we use V_{SG} and V_{SD} instead of V_{GS} and V_{DS} despite the fact that they are the

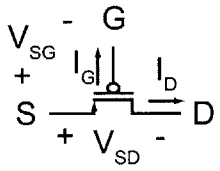

Figure 2-9: The definition of V_{SG}, V_{SD}, I_D, and I_G.

standard terms used in the field. The polarity of the voltages and the direction of the currents used in this thesis are defined as shown in Figure 2-9.

It is noteworthy that pentacene OFETs operate in the accumulation region [10, 11]. Therefore in the place of the threshold voltage in silicon devices, the flat band voltage (V_{FB}), which describes the onset of charge accumulation, will be used.

2.3 Previous Characterization of OFETs

Increasing interest in OFETs has led to the publication of an IEEE standard on the characterization of organic devices to facilitate interpretation of a growing number of research results [3]. In circuit applications, two important parameters are the flat band voltage (V_{FB}) and the mobility (μ). In the IEEE standard [3], OFET parameters are extracted by fitting organic transistors' $I_D - V_{SG}$ characteristics at different V_{SD} to crystal silicon MOSFET model either in the saturation region (Eq. 2.1) or the triode region (Eq. 2.2).

Saturation region: [1]

$$I_{D,sat} = \frac{W}{2L}\mu C_{ox}(V_{SG} - V_{FB})^2 \tag{2.1}$$

Triode region:

$$I_{D,lin} = \frac{W}{L}\mu C_{ox}(V_{SG} - V_{FB} - 0.5V_{SD})V_{SD} \tag{2.2}$$

However, conduction in organic materials is not through band transport mechanisms, so there is no a priori basis for assuming a square law characteristic in the saturation

[1] we use V_{SG} and V_{FB} instead of V_{GS} and V_T here because pentacene OFETs are pFETs and operate in accumulation region.

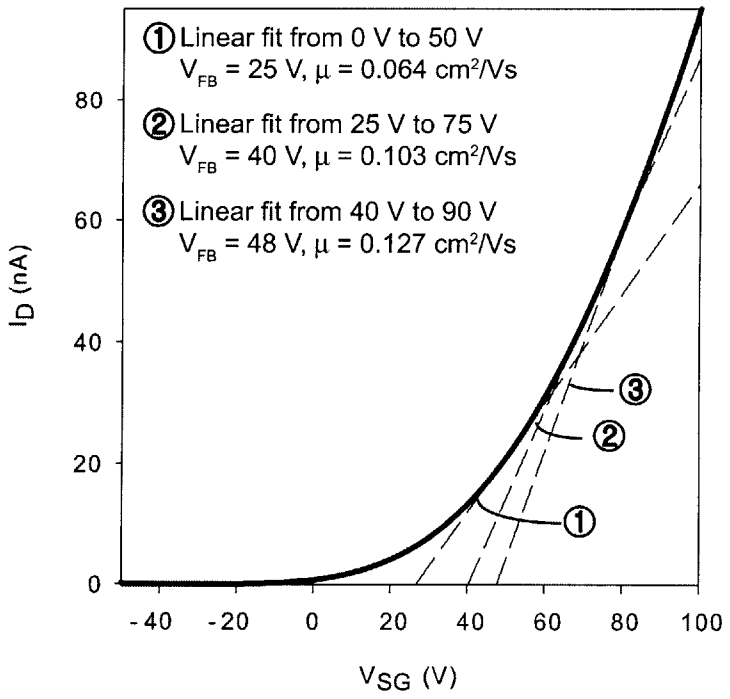

Figure 2-10: Mobility extraction by fitting the I-V characteristic curve at three different range of data to the single crystalline MOSFET model. I-V characteristic curve shown here is the average of two curves swept in both directions. Extracted mobility and the flat band voltage change significantly according to the range of data used for the linear fit.

region. In addition, charge accumulated in organic semiconductors may be different from silicon semiconductors, so there is no reason to assume that induced charge is linearly proportional to the gate voltage. Additionally, trapping effects can modulate the conduction through the channel as the surface potential is changed, which causes mobility dependency on the gate voltage. In pentacene OFETs, the presence of such mobility dependency prohibits the use of MOSFET model-based mobility extraction introduced above; depending on the range of I-V data used, the extracted mobility and flat band voltage differ by a factor of two as illustrated in Figure 2-10. Some studies showed that the MOSFET model can be empirically adjusted by setting $\mu_{OFET} = \mu_0(\frac{V_{SG}-V_{FB}}{V_{AA}})^{\gamma}$, where γ and V_{AA} are empirical parameters, to account for the mobility dependence on the gate voltage [12]. Although this method may empirically model mobility accurately, there are still no methods to extract V_{FB} through I-V measurement alone.

Chapter 3

Characterization of OFETs

In this chapter, we explore the characterization of pentacene OFETs. OFETs have high contact resistance, which make extraction of parameters difficult [13, 14]. Additionally, mobility that increases as a function of gate bias has been reported [12], while many papers continue to report mobility extracted from the crystal silicon MOSFET model which assumes constant mobility. In this chapter, we will discuss the extraction of contact resistance and mobility based on fundamental physics.

3.1 Contact Resistance

Organic transistors have high contact resistances because the contacts between the organic semiconductor and the source/drain metal are not ohmic. Currently there is no clear physical understanding of the charge injection process which governs the efficiency of the contacts. The metallic/organic interface is commonly modeled as a Schottky-diode in series with a contact resistance [13, 15] (see Figure 3-1(a)). This model is physically based on the fact that a Schottky diode is likely to form as the pentacene semiconductor is not degenerately doped, and that the gap between the gold electrode and the pentacene molecules lead to a high series contact resistance. To show how the contact resistance affects device performance and mobility extraction, we characterize two sets of OFETs; Set 1 top contact transistors have relatively low contact resistances and Set 2 bottom contact transistors have relatively high contact

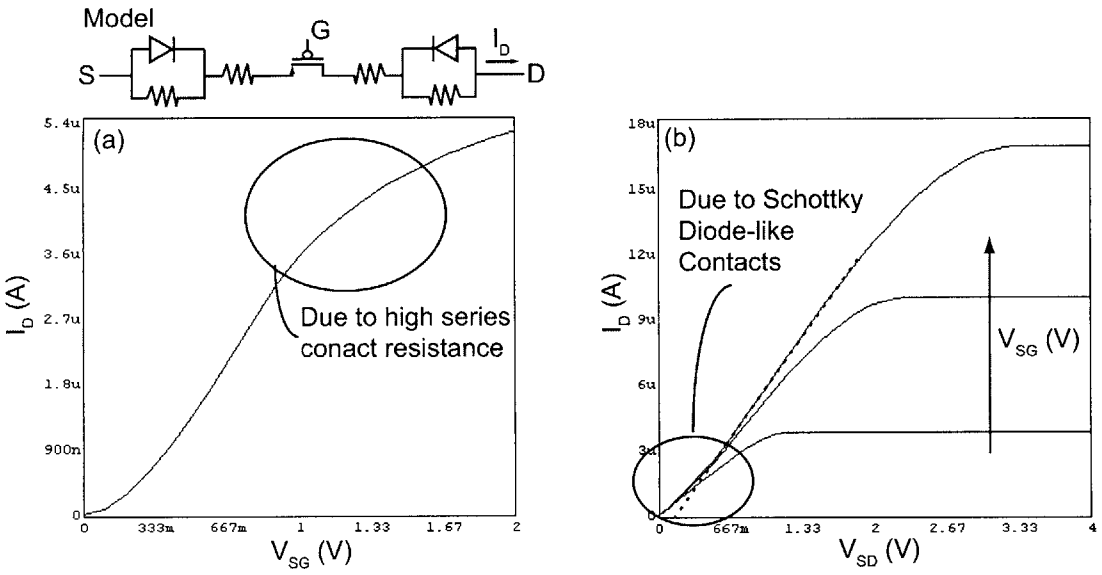

Figure 3-1: Contacts in OFETs are commonly modeled as a Schottky diode in series with a contact resistance. (a) Simulated I_D-V_{SG} characteristics of a transistor with the modeled contacts. (b) Simulated I_D-V_{SD} characteristics of a transistor with the modeled contacts.

resistances.

The quality of the contact in an OFET can be easily assessed by observing the I-V curves. A high series contact resistance drops a substantial amount of V_{SD} across it as the transistor passes more current. As shown in Figure 3-1(a) the presence of high contact resistance can be identified by observing the decrease in the transconductance at a high gate voltage. Figure 3-2 show I_D-V_{SG} curves in the triode region for both sets of transistors. As we had claimed, the contact resistance is higher in Set 2 than in Set 1 as a greater decrease in the transconductance at high V_{SG} indicates. It is noteworthy that the current is proportional to ${V_{SG}}^{\alpha}$ where $\alpha > 1$ in the top contact transistor. In the bottom contact transistor, the transconductance of the transistor falls with increasing gate bias akin to the effect of mobility degradation at high gate bias. However, the decrease in transconductance is more prevalent in the short channel transistors. This observation indicates that the decrease in transconductance is due to the high contact resistance because mobility degradation would affect all the different-length transistors equally.

The effect of the contact resistance can be balanced by super-linear increase in

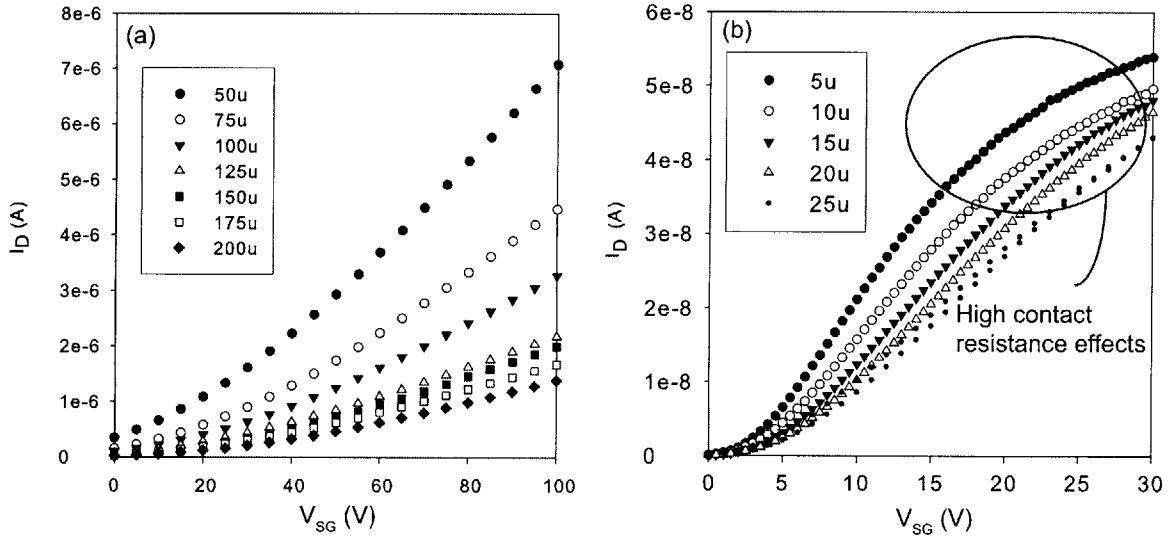

Figure 3-2: I_D-V_{SG} characteristics in Set 1 transistors with $V_{SD} = 1V$ (a) and in Set 2 transistors with $V_{SD} = 0.1V$ (b).

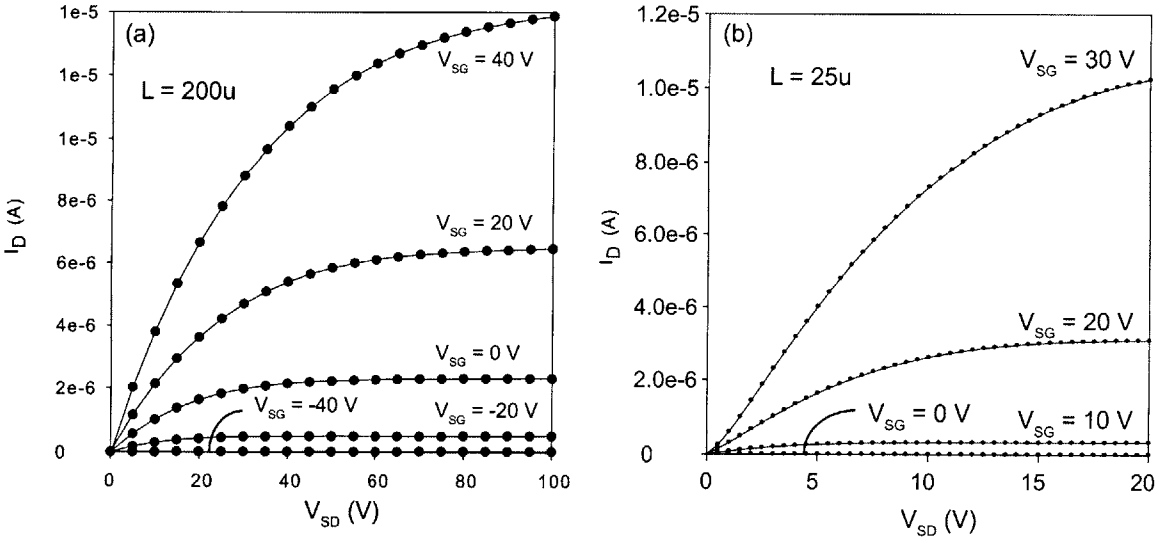

Figure 3-3: I_D-V_{SD} characteristics in a Set 1 transistor with L = 200 μm (a) and in a Set 2 transistor with L = 25 μm (b).

the transistor to produce linear current-voltage relationship as shown in the I-V characteristics for $L = 25\mu$m in Figure 3-2(b). It will be shown later in this section that the current in Set 2 OFETs also has the same characteristics as Set 1 OFETs with the effect of the contact resistance removed.

The Schottky diode-like behavior of the contact can be identified by the change in resistance of the I_D-V_{SD} curve in the deep triode region (see Figure 3-1(b)). At low V_{SD}, the diode is off and the current is passed by the high parasitic resistance in parallel with the ideal diode. At high V_{SD}, the diode barrier is easily overcome and does not affect the overall behavior of the transistor. Both sets of transistors characterized in this research do not exhibit Schottky diode-like contacts as seen in Figure 3-3.

Without the Schottky diode-like contacts, the contact resistance can be extracted using I-V measurements from different-length transistors as in [16]. In the triode region, the channel can be modeled as a simple resistor, and as the length of the channel increases, the resistance increases linearly. If the measured resistance is plotted as a function of the length, the linearly extrapolated resistance at the y intercept ($L = 0$) is the contact resistance. Figure 3-4 and Figure 3-5(a) show application of this extraction method to determine the contact resistance for transistors in Set 1 and Set 2, respectively. W is multiplied to normalize the measured resistance. As seen in Figure 3-5(b), the contact resistance changes as a function of the gate bias, similar to the observations made in [13] and [17].

The contact resistance is alternatively expressed as $R_{contact} = R_{DS} + A\Delta L$ where R_{DS} is the drain-source contact resistance which is free of gate bias dependency, and A is the channel resistance per unit length, and ΔL is the difference between the patterned length and the effective length. R_{DS} and ΔL can be extracted using the method introduced in [16]. Since R_{DS} does not have gate bias dependency, curves for different applied gate bias have a single intercept point with coordinates $(\Delta L, R_{DS})$ as seen in Figure 3-4. In Set 1 transistors, the negative contact resistance indicates that the effective length is shorter than the physical channel length which can be explained by the doping of the channel when evaporating the gold contacts through

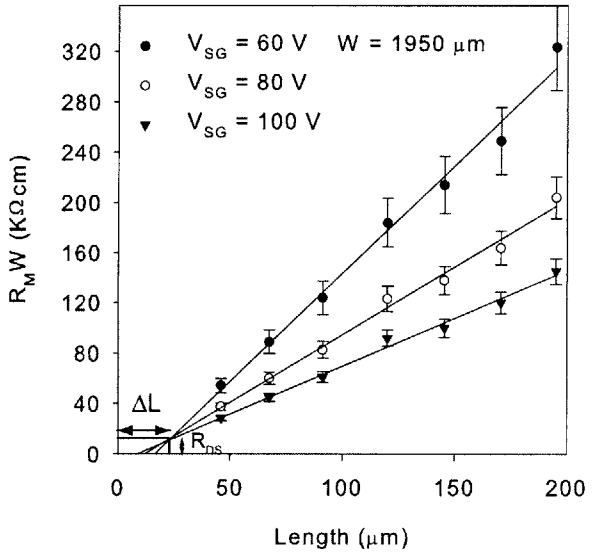

Figure 3-4: Extraction of contact resistance at various V_{SG} for Set 1.

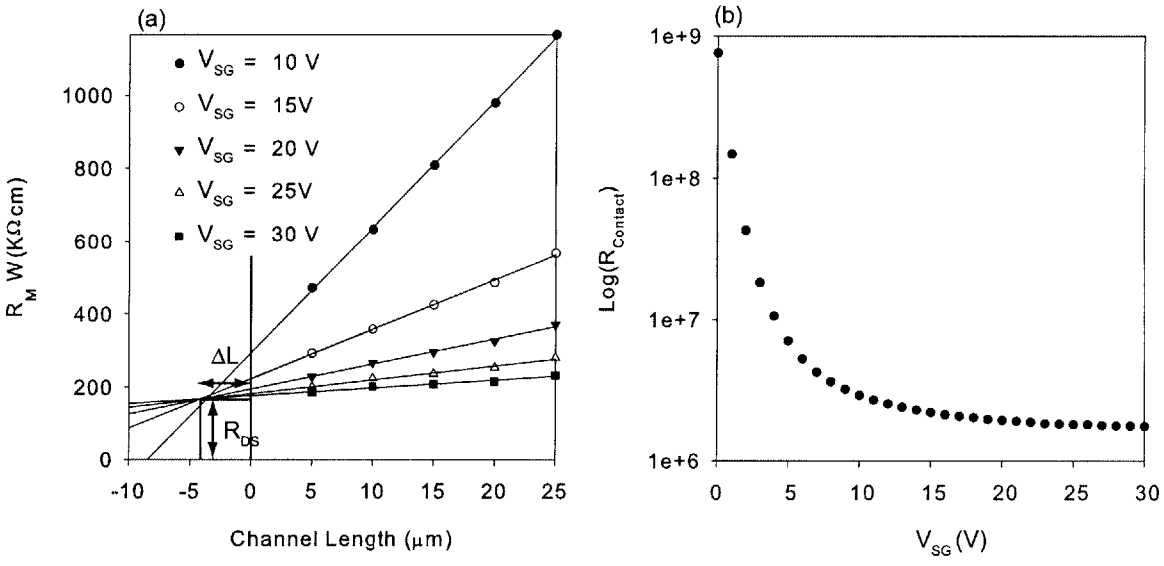

Figure 3-5: (a) Extraction of the contact resistance at various V_{SG} (b) The contact resistance as a function of the gate bias for Set 2.

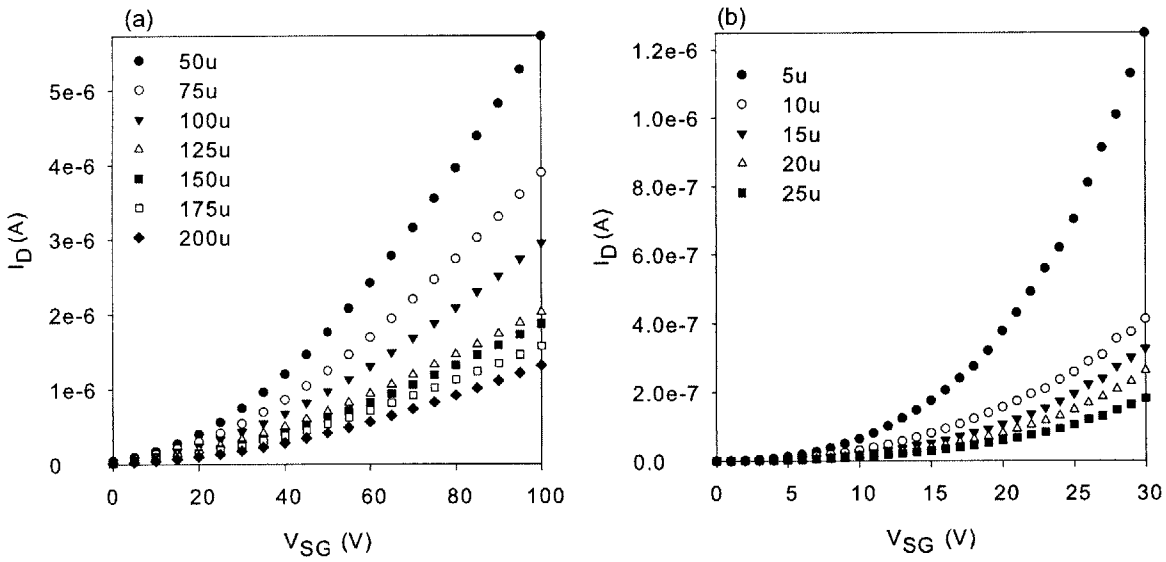

Figure 3-6: I_D-V_{SG} with the contact resistance removed for transistors in Set 1 (a) and Set 2 (b).

the shadow mask. ΔL is found to be 20 μm and R_{DS} is 10 KΩcm. The same method yields ΔL of 4.8 μm and R_{DS} of 170 KΩcm in Set 2 transistors. The effective channel length is longer than the patterned channel length because the channel is patterned by subtractively wet-etching the unprotected source-metal.

As reported elsewhere [17], the measured contact resistance is higher in the bottom contact transistors. Such results are explained by the orientation of the pentacene molecules in the film. Pentacene growth on Au has different orientation from that on dielectric like silicon dioxide, which leads to discontinuity of the crystal lattice in the bottom contact transistors [18]. In the top contact transistors, there are no such discontinuities as pentacene is entirely deposited on the dielectric. However, there are on-going studies for decreasing contact resistance in metal/organic interfaces which may make this statement invalid in the future [19].

Transistor behavior without the contact resistance can be extracted by calculating the source-drain voltage applied to the intrinsic transistor: $V_{SDi} = V_{SDa} - I_D R_{contact}$, where V_{SDa} is the applied source-drain voltage. The I_{Di}, the drain current had there been no voltage drop in the contacts, is calculated by: $I_{Di} = I_D \frac{V_{SDa}}{V_{SDi}}$. Figure 3-6 shows behavior of both sets of transistors had there been no contact resistance. We

can clearly see that the current has similar gate voltage dependency which was not apparent before.

3.2 Charge Density Calculation and Flatband Voltage Extraction from C-V measurement

Although a common characterization tool in silicon MOSFETs, C-V measurements have not been used much in OFETs because of the difficulty of measuring capacitance in OFETs. High contact resistance and low mobility in OFETs limit current flow into the channel. Therefore, ultra low frequency, quasi-static capacitance voltage (QSCV) measurements must be taken to correctly determine the capacitance of an OFET. Unlike conventional C-V measurements, which run a small sinusoidal AC voltage on top of a DC voltage to measure the capacitance, QSCV measures capacitance by slowly ramping up the voltage, which generates a small current that is equal to $I = Cdv/dt$, where dv/dt is the ramp rate. A typical ramp rate is 1 V/sec. This ramp rate can be approximated to a sinusoidal frequency by setting $dv/dt = \frac{d}{dt}(A \sin wt) = Aw \cos wt$, which results in 160 Hz at 1 mV. This low frequency is not attainable with a conventional LCR meter like the HP 4275. Figure 3-7 shows C-V measurements on a sample transistor in Set 2 at various frequencies using both the Agilent 4156C parameter analyzer and the HP 4275 LCR meter. The coinciding results from various measurement conditions of QSCV indicates that quasi-equilibrium is reached at the measurement frequency. In contrast, quasi-equilibrium is not met at frequencies used by the LCR meter as the capacitance changes with measurement frequencies. C-V measurement can be used to extract the induced charge density in the channel and the flat band voltage.

In order to extract charge density from a C-V measurement, the channel capacitance needs to be separated from parasitic capacitances. A structure akin to an OFET but without the pentacene thin film, which we will refer to as a metal-insulator-metal (MIM) structure, is measured to extract the parasitic capacitances. The channel re-

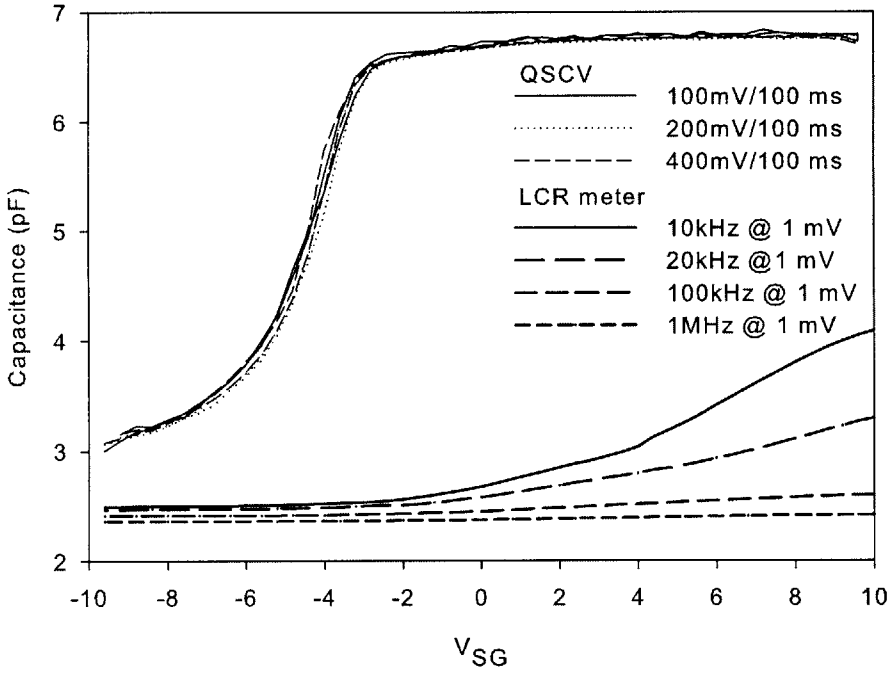

Figure 3-7: Capacitance measurement at various frequencies of a transistor with W/L = 1000/20 μm in Set 2

sistance is calculated as $C_{ch} = C_{OFET} - C_{MIM}$ and the induced charge per area in the channel is determined by Eq. 3.1.

$$Q = \int_{-\text{inf}}^{V_{SG}} \frac{C_{ch}}{WL} dV \tag{3.1}$$

For practical reasons, Eq. 3.1 is integrated from -100 V or below the breakdown voltage of the dielectric.

Figure 3-8(a) shows the QSCV measurement of an OFET in Set 1. The observed hysteresis is attributed to dynamic processes in the charging of the organic film and will require further exploration. One possible cause of this hysteresis could be the doping of the channel from atmospheric particles, which Set 1 is particularly susceptible to as Set 1 OFETs do not have encapsulation. The dip in the center of the C-V measurement is due to the depletion of underlying gate silicon. The gold source-drain pads form MOS structures and deplete when the gate bias is around the flat band

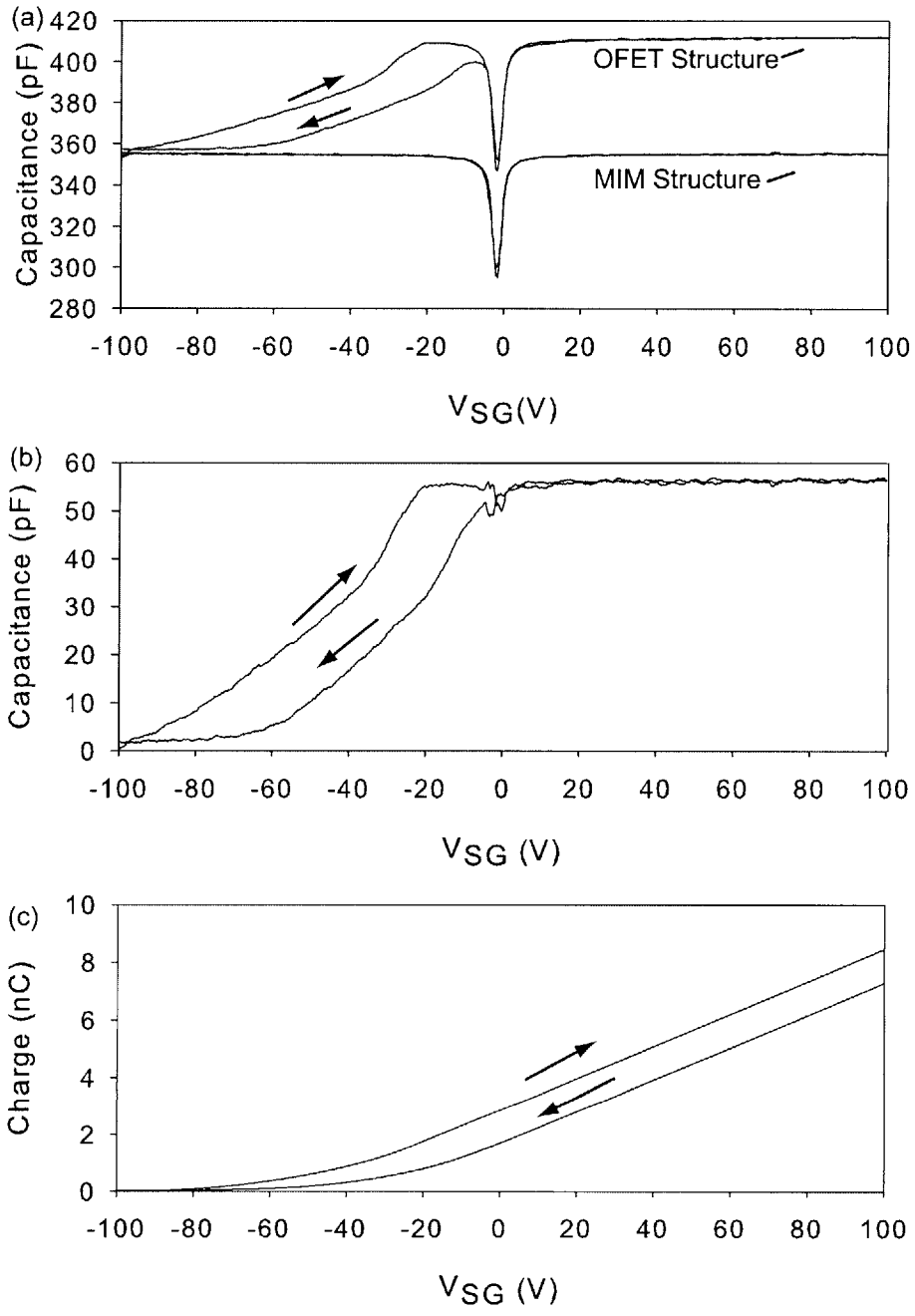

Figure 3-8: (a) QSCV measurements of a MIM structure and a OFET with W/L = 1950/200 μm) The dip around zero volts is due to the depletion effect in the underlying silicon. (b) The channel capacitance, C_{ch}, is derived by $C_{OFET} - C_{MIM}$. (c) The induced charge density determined by Eq. 3.1

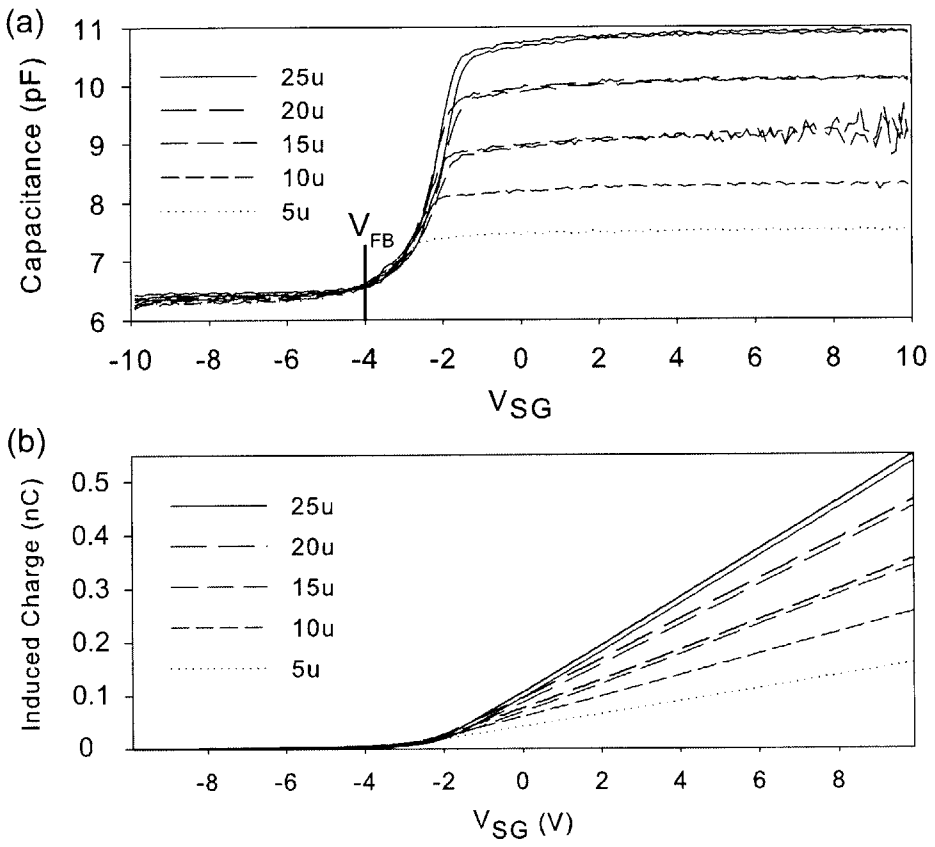

Figure 3-9: (a) QSCV measurements of OFETs of different lengths in Set 2. V_{FB} is extracted to be -4V. (b) The induced charge density determined by Eq. 3.1.

voltage of the silicon. The depletion capacitance underneath the source-drain pads in series with the oxide capacitance decreases the total measured capacitance. Since both MIM and OFET have similar parasitics, the dip is cancelled out when the channel capacitance is extracted from $C_{OFET} - C_{MIM}$, as shown in Figure 3-8(b). Lastly, the charge density is extracted according to Eq. 3.1 in Figure 3-8(c).

There are a few notable features in the measurement. One notable feature is that the overlap capacitance can be directly extracted from the OFET C-V measurement, obviating the need for MIM structures. A comparison between the C_{MIM} and the C_{OFET} in Figure 3-8(a) shows that the C_{OFET} in the depletion region ($V_{SG} = 100$V) is due to the overlap capacitance. Figure 3-9(a) shows the QSCV measurement of OFETs in Set 2. As the capacitance in deep depletion is equal to the overlap capacitance, we can extract the channel capacitance and determine the induced charge in

the channel, as shown in Figure 3-9(b).

As noted above, V_{FB} is difficult to extract from I-V characteristics alone in disordered crystalline structures. In poly-crystalline silicon transistors, research has shown that it is beneficial to extract V_{FB} from the C-V measurement as using such a flat band voltage leads to identical model parameters in transistors with different aspect ratios from the same batch [20]. Hence, here we explore the determination of the flat band voltage from the C-V measurement.

In order to determine the flat band voltage, the Debye length needs to be determined. The flat band voltage is the voltage when the measured OFET capacitance is equal to $\frac{C_i C_s}{C_i + C_s}$, where C_i is the capacitance per area of the gate dielectric, and C_s is the semiconductor capacitance per area when there is no band-bending. C_s is calculated as ϵ_s / L_D, where ϵ_s is the permittivity of the semiconductor and L_D is the Debye length. The Debye length for pentacene is inversely proportional to the intrinsically trapped hole density (p_{ti}) (see Appendix B). However, experimentally measuring p_{ti} is difficult [21]. For this reason, p_{ti} is estimated to be between 10^{10} cm^{-3} and 10^{12} cm^{-3} given that for a-Si, p_{ti} is 10^{11} cm^{-3}. At this range of p_{ti}, the L_D is about 2 - 20 μm, and C_s is 0.2 - 2 nF/cm^2. The resulting C_s is small compared to C_i, which is about 15 nF/cm^2 for Set 1 OFETs and 20 nF/cm^2 for Set 2 OFETs. Therefore, the flat band voltage is defined as the voltage when C_{OFET} starts to increase. Figure 3-9(a) shows the V_{FB} determined from the QSCV measurement of different length transistors in Set 2. The flat band voltages are approximately the same for different geometry devices as expected. Severe hysteresis in Set 1 transistors makes it difficult to extract a meaningful flat band voltage.

3.3 Direct Mobility Extraction

With the knowledge of the charge density from the C-V measurement, we can extract mobility with minimal assumptions. The drift mobility, μ, is defined as the velocity, v, of the carriers divided by the electric field, E. In an OFET, if I_D is measured under the bias condition $V_{SD} \ll V_{SG} - V_{FB}$, mobility can be extracted from the following

fundamental relationship:

$$\mu = \frac{I_D}{WQE}, \tag{3.2}$$

where W is the width of the OFET channel and Q is the induced charge per area. As $V_{SD} \ll V_{SG} - V_{FB}$, the electric field across the entire channel is approximately constant, and E can be expressed as $E = V_{SD}/L$. Lastly, Q can be determined through the C-V measurement, as the total charge induced will be uniformly distributed along the channel. Such low frequency C-V measurements have been previously used in silicon MOSFETs to separate charge and mobility and determine the gate bias dependency of mobility [22].

Mobility is extracted from both sets of transistors. To minimize effects of the contact resistance, I_D vs. V_{SG} at $V_{SD} = 100$ mV is taken from the longest channel transistor with W/L = 1950/200 μm (inset of Figure 3-10). The induced charge in the channel is determined by the method introduced in Section 3.2, and with the W and E known, mobility is easily extracted. Figure 3-10 shows the resulting mobility. The extracted mobility is plotted as a shaded area to reflect the uncertainties introduced by the hysteresis in the C-V measurement and the I_D-V_{SG} sweep. Although significant errors were introduced, it is evident that the mobility increases with the gate voltage and varies from 0.002 to 0.05 cm^2/Vs.

Figure 3-11 shows mobility calculated from transistors of various lengths in Set 2. At first glance, mobility seems akin to MOSFET mobility, reaching a constant mobility at high enough gate bias. However, mobilities extracted from the same semiconductor differ by a factor of four, which is highly unlikely. If we correct for the contact resistance by using the I-V characteristics with the effect of contact resistance removed in Figure 3-6(b), mobility that increases with gate bias results, as shown in Figure 3-12. In addition, the corrected mobility is approximately the same across devices of different lengths.

The increase in mobility with gate bias, shown here and in numerous other articles [12, 23, 24], illustrates that the conduction mechanism in pentacene OFETs is different from that in crystalline silicon MOSFETs, but is similar charge transport

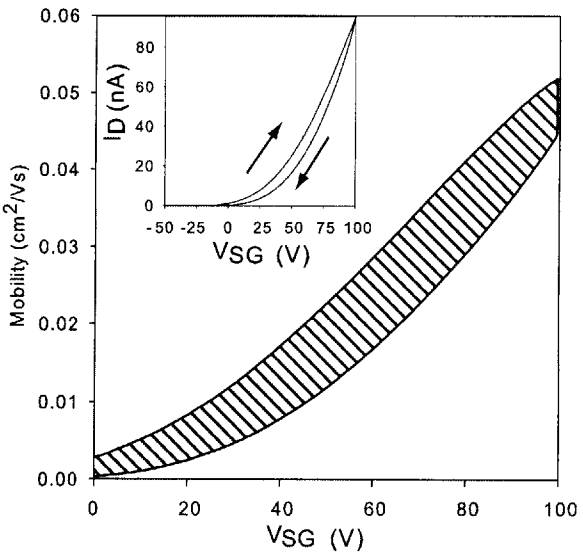

Figure 3-10: Mobility extracted from a W/L = 1950/200 μm transistor in Set 1. Mobility is shown as a shaded band with the upper and lower bound set by hysteresis in C-V and I-V measurements. Mobility dependence on V_{SG} is observed. The inset shows the I-V measurement from which mobility was extracted.

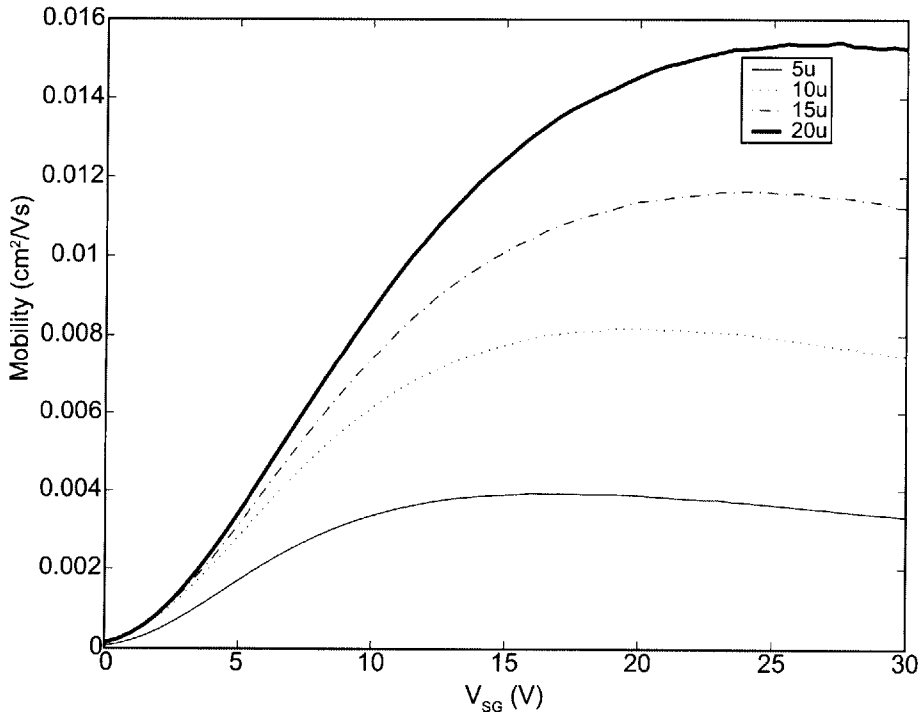

Figure 3-11: Mobility extracted from transistors in Set 2 not accounting for the series contact resistance. No clear dependency on gate-bias.

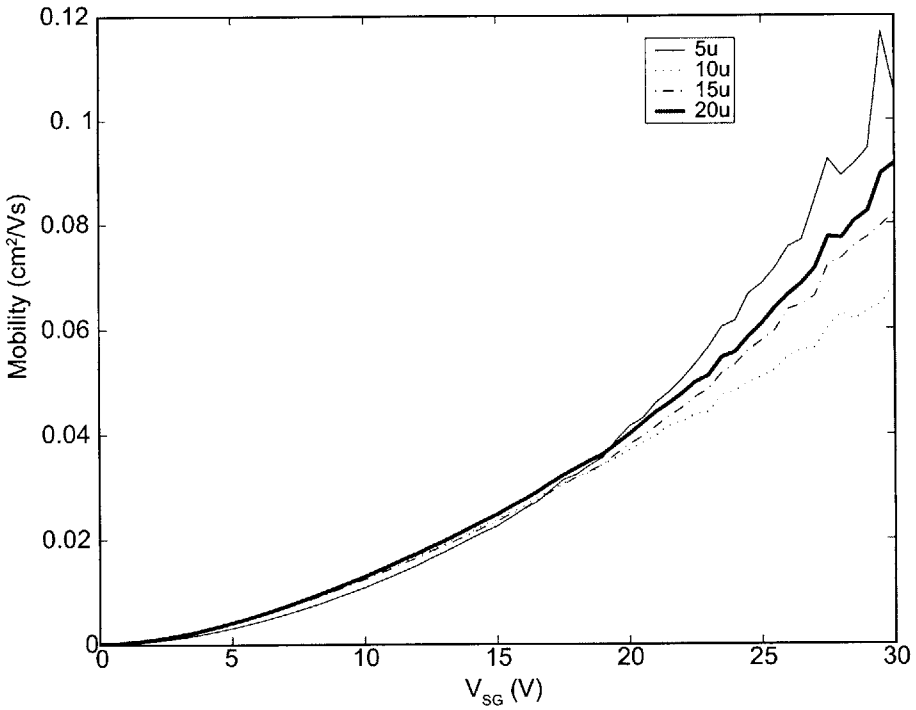

Figure 3-12: Mobility extracted from transistors in Set 2 taking into accounting the series contact resistance. The same mobility dependency on gate bias as the transistor in Set 1 is observed, and devices of different lengths yield the same mobility.

in amorphous Si (a-Si) TFTs. Akin to a-Si, the electronic states of organic crystal semiconductors are extended in the periodic structure of the crystal and localized at the crystal grain boundaries. The localized states, which arise from the disorder in the organic film, lead to trapping of the induced charges, with the charge transport in the OFET channel alternating between trapped and free states. By adopting the analysis of charge mobility in disordered inorganic semiconductors [25], the apparent OFET channel mobility is given by:

$$\mu_{OFET} = \mu_{free}\frac{Q_{free}}{Q_{induced}} = \mu_{free}\frac{Q_{free}}{Q_{free} + Q_{trapped}} \tag{3.3}$$

where μ_{free} is the mobility of the carrier when it is in an extended state of the organic crystals, while Q_{free} and $Q_{trapped}$ are the free and trapped fraction of the gate-bias-induced charge, $Q_{induced}$. With increase in magnitude of the negative gate bias, the Fermi energy level sweeps into the pentacene trap-state energies, filling the deep hole-

traps and increasing the Q_{free} fraction of the induced charge. Consequently, μ_{OFET} increases with fewer unfilled traps and larger Q_{free}.

We note that the mobility calculated from the proposed method is significantly smaller than that derived from the MOSFET equation (see Figure 2-10). The MOSFET equation (Eq. 2.2) necessitates a choice of the flat band voltage, which sets the starting limit of the Eq. 3.1 integral. The integral, then, significantly underestimates charge in the channel, which is offset in Eq. 3.2 by the apparent increase in the calculated mobility. In contrast, our analysis avoids using an arbitrary flat band voltage and calculates the number of carriers in the channel by integrating all the charge carriers that are induced in the channel. We note that this carrier count also includes carriers that are trapped at the organic/dielectric interface, with the consequence that the measured mobility is the average mobility of all the carriers, trapped and free, induced in the channel. The separation of trapped from mobile charge is a subject of future work.

3.4 Dealing with OFET Non-idealities

Two non-idealities that introduce errors to extraction of parameters are gate leakage current and hysteresis. Gate leakage current is substantial in OFETs because OFETs require a large gate field in order to induce enough charge to attain a reasonable conductance. In the initial stage of this research, high gate leakage current made it impossible to use QSCV even with the leakage current cancellation technique. The gate leakage current is drawn out from the source and drain currents and changes the trend in I-V characteristics as illustrated in Figure 3-13. Such a leakage current is a problem not only for device characterization but also for designing OLED drivers. Therefore, gate leakage current should be always monitored to make sure it is less than 0.1% of I_D, as suggested by the IEEE standard [3].

Hysteresis in OFETs can be severe, as seen in the C-V measurement (Figure 3-8), which is measured with a delay time of 200 msec at 100 mV steps and a ramp rate of 1 V/sec. Hysteresis is caused by the various defect-states resulting from impurities,

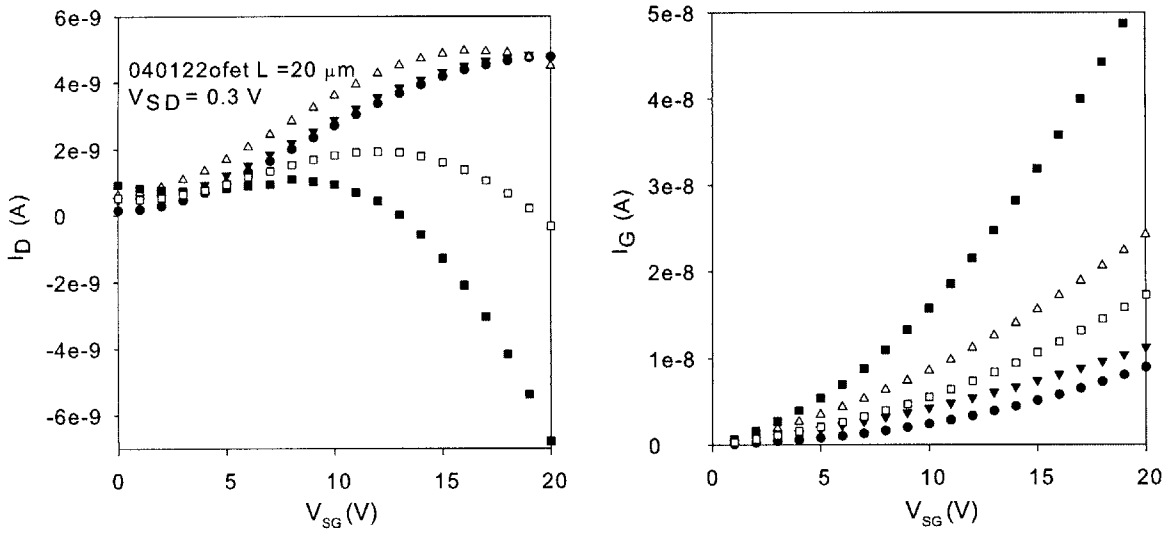

Figure 3-13: I_D vs. V_{SG} and I_G vs. V_{SG} for five devices with the same geometric size. Different gate leakage current drastically change the shape of I_D-V_{SG} curve.

structural defects in the crystalline structure like point defects, dislocations, and grain boundaries.

Chapter 4

Conclusion

The characterization of OFETs focusing on the extraction of contact resistance, flat band voltage, and mobility has been performed. Mobility is successfully extracted with minimal assumptions using QSCV measurements to separate induced charge from mobility. High contact resistance in the bottom contact transistors has been found to obscure I-V characteristics and hide the apparent mobility dependency on the gate voltage. With the effects of contact resistance removed, mobility from both top contact and bottom contact transistors increased with the gate bias. This mobility dependency indicates that the pentacene semiconductor in the devices characterized is amorphous crystalline and implies that higher mobility can be achieved by forming a more ordered film. The dependency also exemplifies the inadequacy of the standard MOSFET model to describe the operational behavior of OFETs. The extracted mobility is the average mobility of all the induced carriers, trapped and free, and separating the free carriers to determine free carrier mobility will be a focus of future work.

Appendix A

Detailed Fabrication Procedures

A.1 Shadow mask patterned top contact transistors

1. Clean silicon substrate with 2000 Å of SiO_2 [1]

2. Deposit pentacene (Pentacene deposition system in Akinwande lab)

3. Deposit Au for source-drain contacts (Perkin Elmer)

[1] Cleaning process to eliminate organic impurities from glass substrates was performed in Vladimir's lab

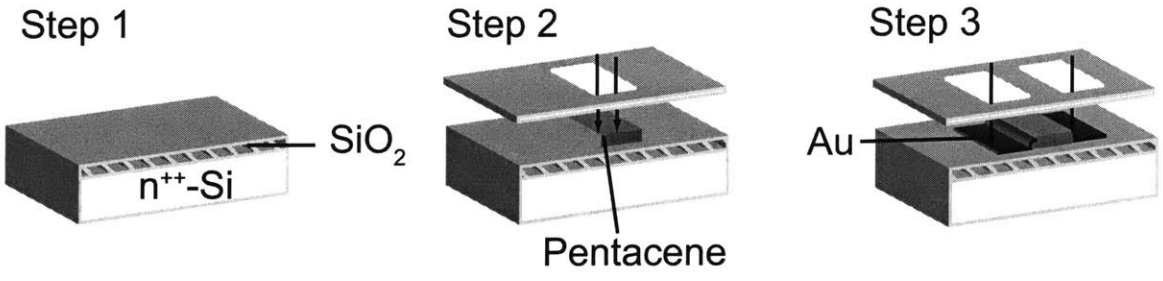

Figure A-1: Illustration of the shadow mask patterning process

A.2 Lithographically patterned bottom contact transistors

1. Wafer cleaning

   Pirahna (3:1 H_2SO_4:H_2O_2) dip for 10 minutes, rinse in H_2O, SRD[2]

2. Gate layer

   E-beam deposition of 500 Å Cr and then 500 Å Au

   Photolithographically pattern gate layer [3]

   Etch Au with KI Trans-Etch then etch Cr in Cr etch (Acid-hood)

   Strip photoresist (Photohood)[4]

3. Parylene gate dielectric

   CVD 3000 Å of Parylene (SCS 2010 Lab Coater in Akinwande lab)

   Photolithographically pattern Parylene

   Etch via in parylene (Plasmaquest) [5]

   Strip photoresist (Photohood)

4. Source-drain layer

   Deposit 600 Å of Au (Perkin-Elmer) [6]

   Photolithographically pattern source-drain layer

   Etch Au (Acid-hood)

   Strip photoresist (Photohood)

5. Channel layer

   Deposit 100 Å of Parylene

   Deposit pentacene (Pentacene deposition system in Akinwande lab)

   CVD Parylene for encapsulation

Figure A-2 shows the process of the lithographically patterned bottom-contact transistors. The figure was adapted from from Kymissis et al. [6].

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[2]Spin Rinse Dry

[3]Photolithography includes the following steps: Spin on OCG925 positive resist with no HMDS, Prebake 30 min at 95 °C, Expose (EV1), Develop in OCG825, Rinse

[4]10 min soak and 5 min sonic agitate in Microstrip, rinse, SRD

[5]30 s stabilization, 30 s power ramp up, 300 s etch

[6]1 KW power, 8 mTorr, 50 sccm Argon

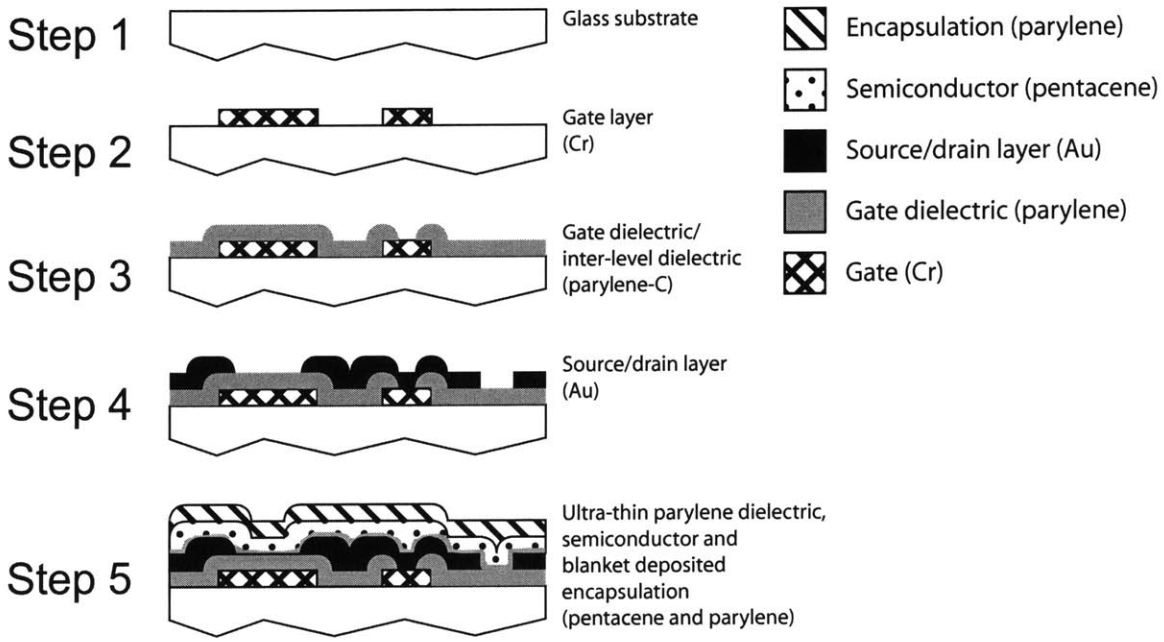

Figure A-2: Illustration of the lithography patterning process [6].

A.3 Physical description of the transistors

	Set 1	Set 2
Topology	top contact	bottom contact
Substrate	silicon	glass
Gate metal	silicon	50 nm chrome, 50 nm gold
Gate dielectric	200 nm SiO_2	300 nm parylene
Source-drain metal	50 nm gold	60 nm gold
Semiconductor	pentacene	pentacene
Width	2000 μm	1000 μm
Length	50, 75, 100, 125, 150, 175, 200 μm	5, 10, 15, 20, 25 μm

Table A.1: Physical descriptions of transistors in Set 1 and Set 2

Appendix B

Calculation of the Debye Length

The Debye length is the characteristic length, which the perturbations to the charge density and potential in a semiconductor material tend to fall off with. In amorphous crystalline semiconductor, it is calculated as [26]:

$$L_D = \sqrt{\frac{\epsilon v_{th}^2}{qV_{pt}p_{ti}}}, \tag{B.1}$$

where ϵ is the permittivity of the semiconductor, v_{th} is the thermal voltage, V_{pt} is the exponential slope of the valence band tail states, and p_{ti} is the density of trapped hole at $E_F = E_i$. In intrinsic pentacene crystalline semiconductor, ϵ=4ϵ_0 according to [27]. The V_{pt} is measured from I_D-V_{SG} measurement to be 36 mV and 50 mV for Set 1 and Set 2 transistors, respectively. The calculated Debye length is shown in Figure B-1 as a function of p_{ti}. In amorphous silicon, the typical p_{ti} is 2.7×10^{11} cm^{-3} [28]. At trapped hole density of 10^{11} cm^{-3}, the Debye length is 6.4 μm and 5.5 μm, which corresponds to C_s of 0.55 nF/cm^2 and 0.65 nF/cm^2 for Set 1 and Set 2 transistors, respectively.

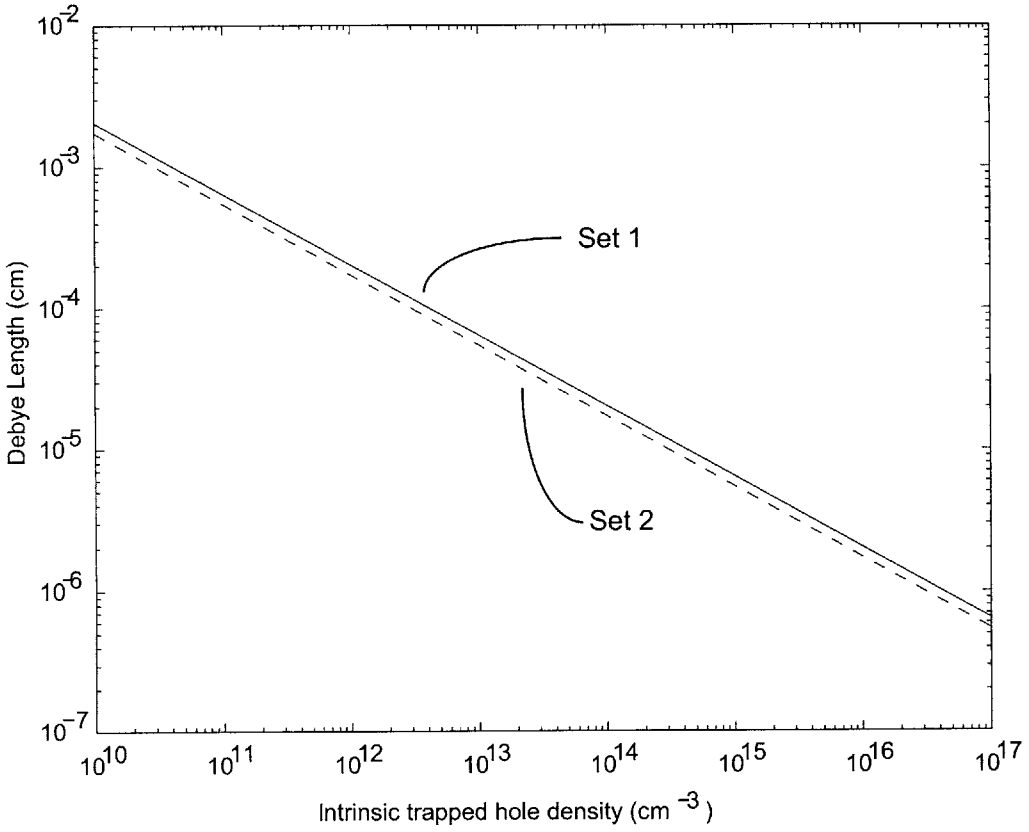

Figure B-1: The Debye length as a function of the intrinsically trapped hole concentration

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