Effect of Varying Gate-Drain Distance on the RF Power Performance of Pseudomorphic High Electron Mobility Transistors

by

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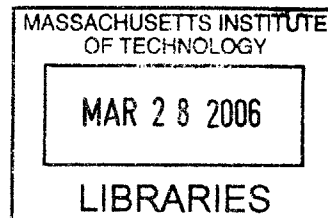Department of Electrical Engineering and Computer Science
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Abstract

AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistors (PHEMTs) are widely used in satellite communications, military and commercial radar, cellular telephones, and other RF power applications. One key figure of merit in these applications is RF power output. Increasing the gate-to-drain length (L_{RD}) of the PHEMT leads to an increase in its breakdown voltage. This should theoretically allow the selection of a higher drain operating voltage and consequently result in higher output power at microwave frequencies. However, experimentally, a decrease in output power and peak power-added efficiency is generally observed with increasing L_{RD}. In order to understand this, we have studied in detail the RF power performance of industrial PHEMTs with different values of L_{RD}. We have found that there is an optimum value of L_{RD} beyond which the maximum RF power output that the device can deliver drops. In addition, we have found that the output power of long L_{RD} devices declines significantly with increasing frequency. We explain the difference in RF power behavior of the different devices through the evolution of load lines with frequency, L_{RD}, and operating voltage. We have found that the presence of oscillations in the NDR region limit the maximum allowable operating voltage of long L_{RD} devices through catastrophic burnout. The maximum voltage of short L_{RD} devices is limited by electrical degradation. Pulsed I-V measurements have revealed that long L_{RD} devices increasingly suffer from surface state activity that limit the maximum drain current under RF operation. A delay time analysis has shown an increasing extension of the depletion region toward the drain with increasing L_{RD} that limits the frequency response of long L_{RD} devices.

Acknowledgements

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In addition, I would like to dedicate this work to the memory of my grandmother, Fung S. Lee, whose generosity, humility, and selflessness continue to inspire me. I know you are smiling down on us from heaven.

No words can express the immense gratitude I have for Joseph Jankowski, the love of my life and unequivocally the most brilliant and irreverent person I have ever met, toward making these past few years among the best of my life. Your unwavering belief in my success kept me going when times got tough. Thank you for keeping me young at heart and being my pillar of support. I look forward toward embarking on many more adventures with you as we grow old and wrinkly together!

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Chapter 1: Introduction

1.1   GaAs PHEMTs for high-frequency power applications

AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistors (PHEMTs) are widely used in satellite communication modules, transmit receive modules for military radar applications, and cellular telephones. Due to the relative maturity of GaAs PHEMT technology, excellent RF power performance can be achieved at reasonable cost [1, 2].

In RF power applications, the most important figures of merit are power gain, output power, and power added efficiency (PAE) at a certain frequency. The gain can be expressed as the ratio of different powers; for instance, the transducer power gain G_T is represented by the ratio of the power delivered to the load and power available from the source. The output power is usually specified at a certain gain compression level (i.e., 3-dB), which occurs as the device enters large-signal operation. Lastly, the PAE is one way to measure amplifier efficiency and takes into
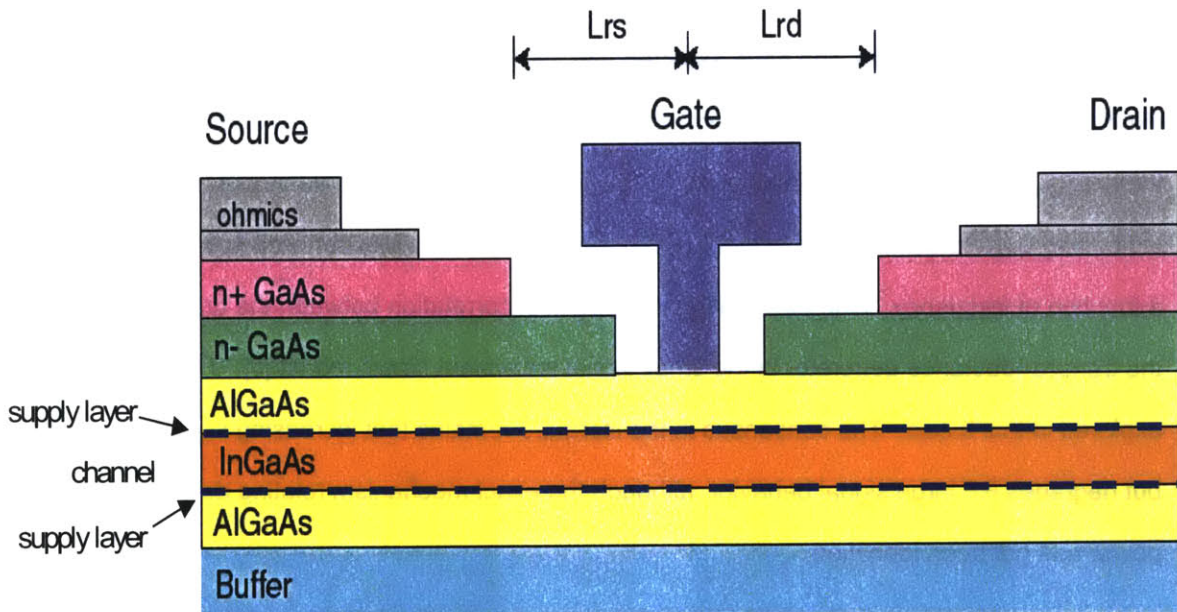
Fig. 1-1: Schematic cross-section of doubled-doped PHEMT.

account the input power.

One key attribute of a good power PHEMT is high output power, which can be achieved with a higher drain bias. To provide a high drain bias voltage, the drain-gate breakdown voltage BV_{off} should be made as high as possible, which is especially critical when the device is biased in Class AB operation. Fig. 1-1 shows the cross section of a typical RF power PHEMT. An increase in BV_{off} can be obtained by a double-recess gate design (shown in Fig. 1-1) that effectively widens the separation between the gate and drain electrodes and thereby reduces the peak electric field in the gate-drain region. For the devices studied in this thesis, increasing the wide gate-drain recess length (L_{RD}) leads to a corresponding increase in BV_{off}. In turn, the increase in BV_{off} allows an increase in output power due to the increased operating voltage that is possible.

However, previous studies have reported that the output power actually decreases with increasing L_{RD} partly due to drain current degradation [3] and a degraded frequency response [4, 5]. Other studies performed varying L_{RD} and the gate-source wide recess L_{RS} simultaneously have shown similar results and have asserted that the RF degradation is a result of the parasitic extension of the depletion region located between the gate and drain due to surface states [6, 7]. Intrinsic g_m and maximum available gain (MAG) have been reported to decrease along with increasing L_{RD}. In addition, the longer L_{RD} devices experience a steeper drop in output power as a function of frequency. One explanation is a potential correlation between the drain delay and the transconductance generator in the small signal equivalent circuit model [8]. This will be explored in this thesis. The consensus in the literature remains that increasing L_{RD} improves BV_{off} but degrades RF large signal behavior, although the exact mechanism relating delay and output power has not been identified.

Another perplexing feature of the studied devices is the presence of negative differential resistance (NDR) in the DC measurements when L_{RD} is sufficiently long and the gate is forward

biased (Fig. 1-2). Interestingly, it is most prominent for intermediate forward gate voltages. Since I_G does not increase in a corresponding way as I_D decreases, the possibility of real space transfer of electrons from the 2DEG into the gate electrode has been ruled out [9]. We have explored a possible connection between the appearance of NDR and power degradation since, under some conditions, the load line may pass through the NDR region.

To understand the full impact of L_{RD} on RF power performance, we will map out in detail the RF power characteristics of PHEMTS as a function of L_{RD} and study the evolution of output power with operating voltage and frequency to identify the physical origin of the obtained characteristics. Lastly, we will provide suggestions for designing optimum L_{RD} PHEMTs.
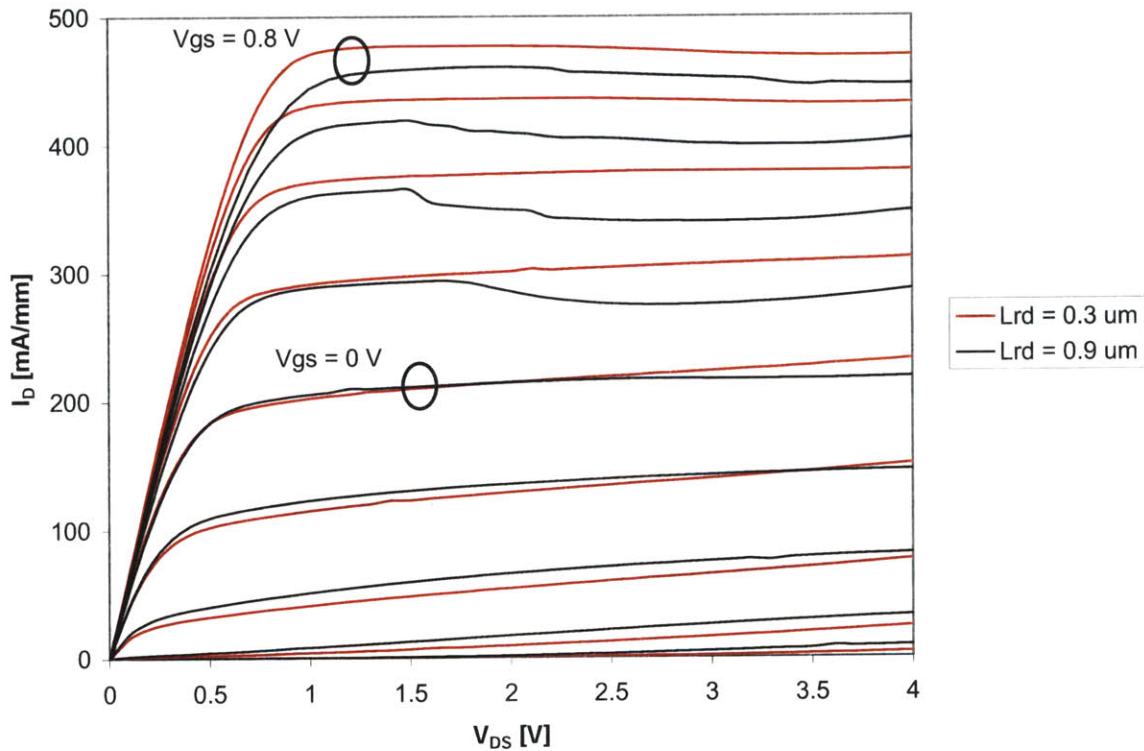
Fig. 1-2: I_D vs. V_{DS} for the L_{RD} = 0.3 and 0.5 um Al gate PHEMT. V_{GS} is stepped from –0.8 V to 0.8 V in 0.2 V increments.

1.2 Outline of Thesis

This thesis is organized in the following manner. Chapter 2 will describe the experimental devices and measurement setup used to perform the RF measurements on the PHEMTs. The load pull optimization methodology is described in detail and the RF figures of merit used to monitor RF performance are defined. The de-embedding procedure used to extract the intrinsic equivalent circuit model from the S-parameter measurements is also explained.

Chapter 3 presents experimental results showing the impact of L_{RD} on the RF performance across I_D, V_{DD}, and frequency through large signal measurements. We will show that there are consistent trends in large signal performance as a function of L_{RD}. In an attempt to maximize V_{DD} for each transistor design, we will track the degradation that results from operation at high V_{DD} for each device. In order to do this, verification measurements will be carried out to monitor the device characteristics at a benign V_{DD} and at the same impedance points after each successive optimization. In addition, we will investigate the impact of L_{RD} on small signal performance by extracting equivalent circuit models. Performing a delay time analysis will provide further insight into the device physics.

Chapter 4 discusses the negative differential resistance and other anomalous behavior observed in the forward biased gate region of the longer L_{RD} devices. In this region, we will investigate oscillations under DC conditions using a spectrum analyzer, power meter, and through examination of the transfer characteristics. Evidence of unstable behavior will also be investigated through S-parameter measurements, which may provide a clue to their physical origin.

In Chapter 5, we link the presence of oscillations with the anomalous behavior shown in the large signal measurements to explain the limiting factors to RF performance. We will introduce the

concept of load lines and present on- and off-state breakdown data. Load lines will be shown across L_{RD}, V_{DD}, and frequency.

In Chapter 6, the conclusions of this work are presented with the identified origins of the anomalous trends in the RF power characteristics. This section also contains suggestions for choosing an optimum L_{RD} and other possible sources of further investigation regarding this research topic.

The appendix will discuss the DC and large signal results obtained from buried WSi PHEMTs with different L_{RD}. Similar to the Al gate devices, they also exhibit anomalous behavior with increasing L_{RD}. We seek to explain the origins of this behavior through load line analysis.

Chapter 2: Experimental

2.1 Introduction

This chapter first describes the experimental GaAs PHEMTs that are studied in this thesis. Then the experimental setups for the various measurements are also presented. The load pull methodology, key RF figures of merit, and small signal analysis are also discussed.

2.2 Device Technology

The GaAs PHEMT under study was designed and fabricated by Mitsubishi Electric. Figure 2-1 shows the epitaxial layer structure of the device. The foundation of any good power transistor lies within its material stack and geometry. The channel consists of a narrow band-gap InGaAs layer sandwiched between δ-doped wide band-gap AlGaAs layers. The δ-doped supply layers provide the carriers for current conduction in the InGaAs channel while the undoped AlGaAs spacers minimize Columbic scattering. A conduction band discontinuity (ΔEc) exists between the InGaAs and AlGaAs layers, which confines electrons to the narrow band-gap material. The n+ and n-GaAs contact layers prevent the underlying AlGaAs Schottky layer from oxidizing and thus greatly reduces the access resistance and a double recess gate structure enables a high breakdown voltage [3, 10, 11]. With power applications in consideration, the top δ-doped supply layer is the most critical [11]. The PHEMT structure allows high maximum channel current, good carrier confinement within the channel, low output conductance, and solid pinch-off [12, 13].
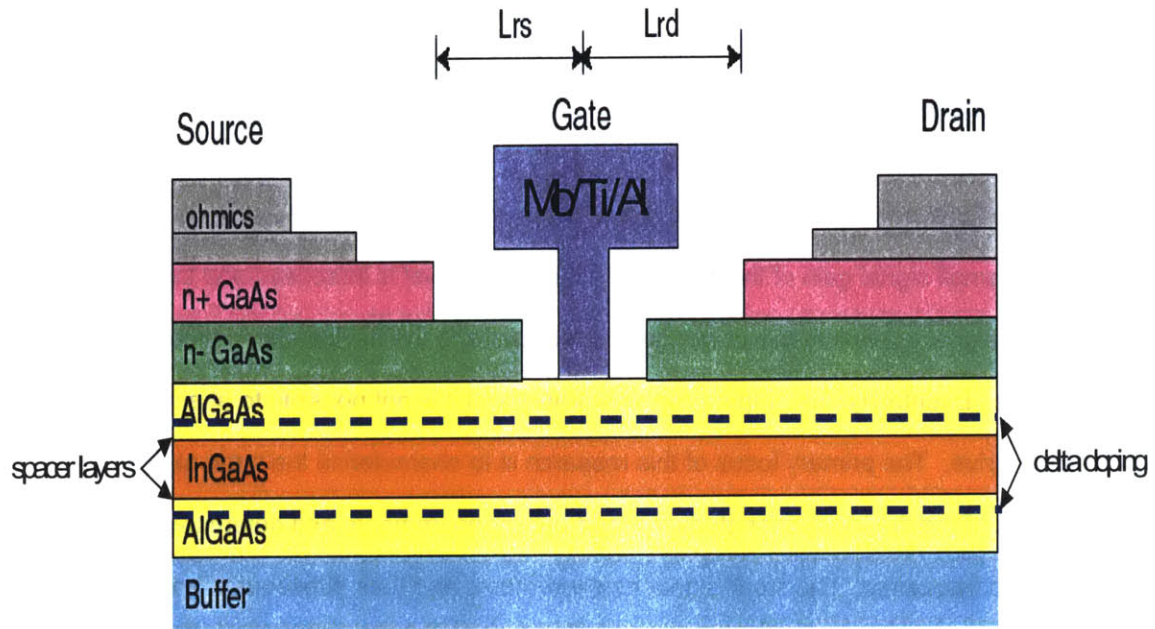
Fig. 2-1: Schematic cross-section of Al gate GaAs PHEMT under study

The PHEMT studied has a Mo/Ti/Al gate with a Schottky barrier height ϕ_B of 0.8 eV, determined by analysis of the C-V characteristics [14]. The gate length of the device is 0.25 μm and the gate width is 160 μm (4 fingers x 40 μm). Devices with L_{RS} = 0.4 um and four different values of L_{RD} will be measured (0.3, 0.5, 0.7, 0.9 um) while all other dimensions are held constant.

For a typical standard Al gate PHEMT, a typical value of the source resistance is R_S = 0.59 Ω-mm, while the drain resistance is R_D = 0.73 Ω-mm. The drain current at V_{DS} = 1.2 V and V_{GS} = 0 V is I_{DSS} = 205.9 mA/mm, and the threshold voltage is –0.66 V. The maximum current I_{MAX} that can be extracted from the device is 465 mA/mm and occurs when V_{DS} = 1.0 V and V_{GS} = 0.8 V. The peak transconductance (g_{m2} = 430 mS/mm) occurs at V_{DS} = 1.2 V and V_{GS} = 0.07 V. In addition, the output conductance g_{o2} = 16.8 mS/mm at this bias point. The off-state breakdown voltage BV_{off} is 15.1 V.

2.3 Measurement Setup

Under small signal power conditions, the power transfer characteristic (P_{OUT}/P_{IN}) is linear and is equal to the small signal gain of the device. As the power level is increased and the transistor enters large signal operation, the power gain is reduced and the device experiences gain compression. Eventually, the output power saturates and it is not possible to attain higher power with higher drive. The primary focus of this research is to characterize the large signal performance of the devices under study via load pull measurements and determine trends across L_{RD}, V_{DS}, and frequency. The small signal measurements and their subsequent analysis via equivalent circuit extraction and delay time decomposition provide a means of understanding the device physics behind large signal operation.

2.3.1 RF Large Signal Measurements

The principle of large-signal characterization, namely, the "source pull/load pull" technique, is to present adjustable impedances at both ports of the transistor and determine the impedances required to extract the most efficient transfer of power by a transistor under large signal
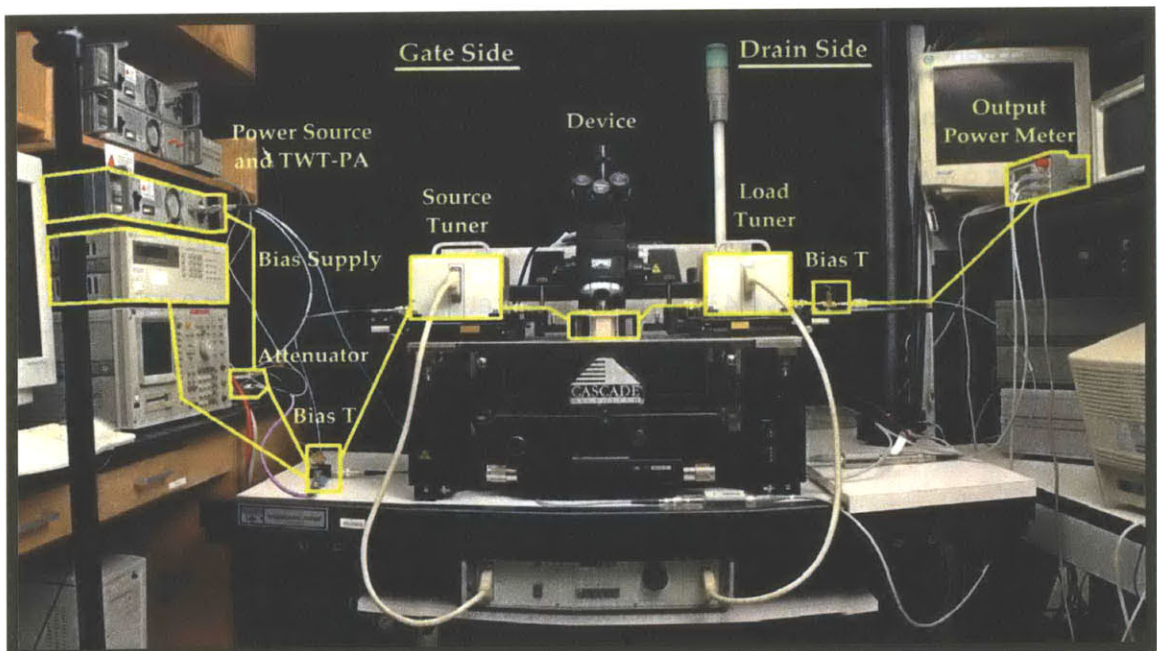
Fig. 2-2: MIT load pull station experimental setup.

conditions. Load-pull measurements are a well-known technique for characterizing the nonlinear behavior of microwave power transistors. For these nonlinear applications, it is necessary to characterize the performance of the device when terminated with source or load impedances other than 50 Ω. A schematic of the load-pull measurement system is shown in Fig. 2-2. It consists of an 8" Cascade Microtech on-wafer probe station equipped with Maury Microwave automated tuners and a 10 W TWT-PA supplying up to 200 mW at the DUT. Measurements can be made between 2-18 GHz. Directional couplers detect the incident and reflected waves at the device input and output ports in terms of voltage. Attenuators inserted in the coupled signal line provide control over the measurable power levels of the device under test (DUT). A range of load impedances is presented to the DUT by controlling the magnitude and phase of the signal injected into the output port of the DUT. The device output impedance is a function of the injected signal and the transfer function of the DUT. Loss present in the system restricts the range of measurable impedances that can be presented at the input and output of the device; as a result, typical values for the maximum $|\Gamma_S|$ and $|\Gamma_L|$ available are 0.87 and 0.78, respectively.

In our load pull optimization methodology, we tuned the source and load impedances for maximum PAE at the 3-dB compression point (Fig. 2-3). This procedure was automated using a program developed by Joerg Scholvin at MIT in Microsoft Visual Basic. Some of the advantages of this automated program over commercial Maury Microwave software include the ability to load a test plan for long-term measurements, make verification measurements to track device degradation during a V_{DS} sweep, and save the history (source pull/load pull iterations, intermediate power sweeps, etc.) of the optimization procedure.

In the measurement plan, optimizations were initially carried out at $V_{DD} = 2$ V and subsequently V_{DS} was ramped in 1 V steps, with each measurement using the impedance points determined by the previous optimization as a starting point. Since the optimal impedance points do not change much when V_{DS} is increased by small increments, an optimization consisting of one source pull and one load pull measurement converges at a speed of approximately 20 minutes per V_{DD}. For

both device types under study, the RF induced I_G was limited to −10 mA/mm for the devices under study in order to prevent excessive damage to the device under high RF drive and to prolong its ability to deliver repeatable measurements. For all of the measurements, V_{GS} is selected to attain the desired I_D under small signal conditions (I_{DO}) as specified by the user. To achieve I_{DO} = 100 mA/mm, V_{GS} was typically around −0.2 V for all of the devices under study. Once V_{GS} is set, it does not change during the optimization procedure.

Another load pull procedure attempted during the course of this research was optimizing for P_{OUT} at the 3-dB compression point. Since optimizing for P_{OUT} is synonymous with optimizing for gain, the optimized impedances would have small signal gains in excess of 20 dB, which is undesirable because it can cause oscillations and early gain compression. To get around this problem, we limited the small signal gain to 15 dB but this added restriction made the data difficult to automate and time consuming to obtain. We found that the same phenomena observed with the data obtained with this methodology could also be observed using the methodology for maximum PAE
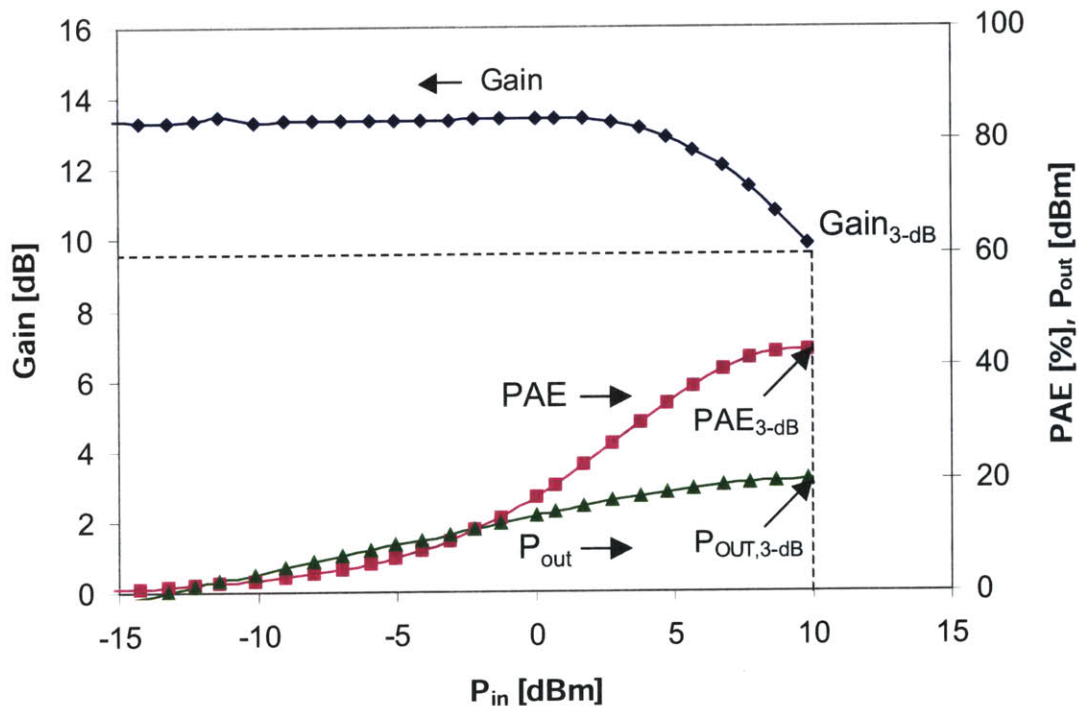
Fig. 2-3: Typical RF power measurement showing the definition of the 3-dB compression point.

at the 3 dB compression point. Hence, we have focused primarily on collecting large signal data

using a load pull procedure that optimizes for PAE. We will now describe three figures of merit

used to assess large signal performance: P_{out}, gain, and PAE.

We have defined $P_{OUT,3\text{-}dB}$ as the P_{OUT} when the small signal gain is reduced by 3-dB as the

device is driven into compression under high RF drive (Fig. 2-4). $P_{OUT,3\text{-}dB}$ is a figure of merit that

will be used frequently as a means of comparison between the behavior of different devices and

is commonly used in the trade.

The gain referenced in this research is defined as the transducer power gain G_T and is

represented by

$$G_T = \frac{P_L}{P_{AVS}}$$

where P_L is the power delivered to the load and P_{AVS} is the power available from the source.

The power added efficiency (PAE) is defined as

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT} - P_{IN}}{I_D V_{DS} + I_G V_{GS}}$$

where P_{IN} is the RF drive power. In general, the gain should be greater than 10 dB or else the

drain efficiency, which is the same as PAE but without the P_{IN} term in the numerator, will suffer as

a result. We will also track I_D and I_G with increased drive level. Unfortunately, due to the

limitations of the biasing system (HP 6628A), the gate current resolution is only 1 mA.

2.3.2 Small Signal Measurements

A HP 8510B vector network analyzer (VNA) is used to measure the S-parameters of the devices under small signal conditions from 0.05 – 40 GHz. The VNA generates a calibrated RF signal and measures the incident, reflected, and transmitted voltages. The RF signal generator of the VNA provides the sinusoidal test signal and the output is calibrated in dBm using a 50 Ω load. The devices are probed on a Cascade Microtech probe station using Picoprobe GGB 40A microwave probes. Incident power on the device input was –20 dBm to ensure small-signal operation. A short-open-line-thru (SOLT) calibration is performed using a standard ceramic substrate supplied by Cascade. WinCal software allows repeatable, accurate VNA calibrations. In the following sections, we will describe two important frequencies of merit: f_t and f_{max}.

2.3.2.a f_T

The short-circuit transit frequency f_T is an important figure of merit that is defined as the frequency at which $|H_{21}| = 1$. It can be estimated by calculating H_{21} from the S-parameters and assuming
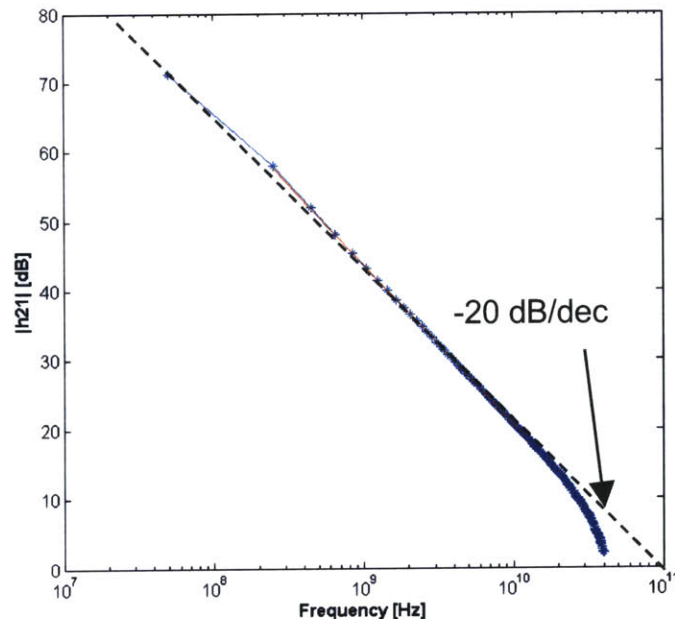
Fig. 2-4: Typical measurement to determine f_T on a L_{RD} = 0.3 um device at V_{DS} = 5 V, I_D = 100 mA/mm.

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that $|H_{21}|$ rolled off at −20 dB/dec with frequency according to the following relationship:

$$f_T = |H_{21}| \cdot f$$

f_T is the frequency where $|H_{21}|$ approximates 0 dB (Fig. 2-4). If the parasitic elements are not de-embedded correctly, the slope of $|H_{21}|$ versus frequency will deviate from the theoretical -20 dB/dec slope because of feedback inductances and capacitances at high frequencies and diode conductance in parallel with the input capacitance at low frequencies [15]. Typically, the extrinsic f_T (f_{Text}) will be less than the intrinsic f_T (f_{Ti}). To extract f_{Ti}, the parasitic elements must first bede-embedded from the raw S-parameters to extract the intrinsic components. Plots of f_{Ti} versus bias provide insight into the effect of bias on high frequency performance. In addition, the time constants of the intrinsic device can be extracted from f_{Ti}.

2.3.2.b f_{max}

The maximum frequency of oscillation f_{max} is an important figure of merit for power gain and is defined as the frequency at which the unilateral power gain G_{TU} is unity. It was estimated by
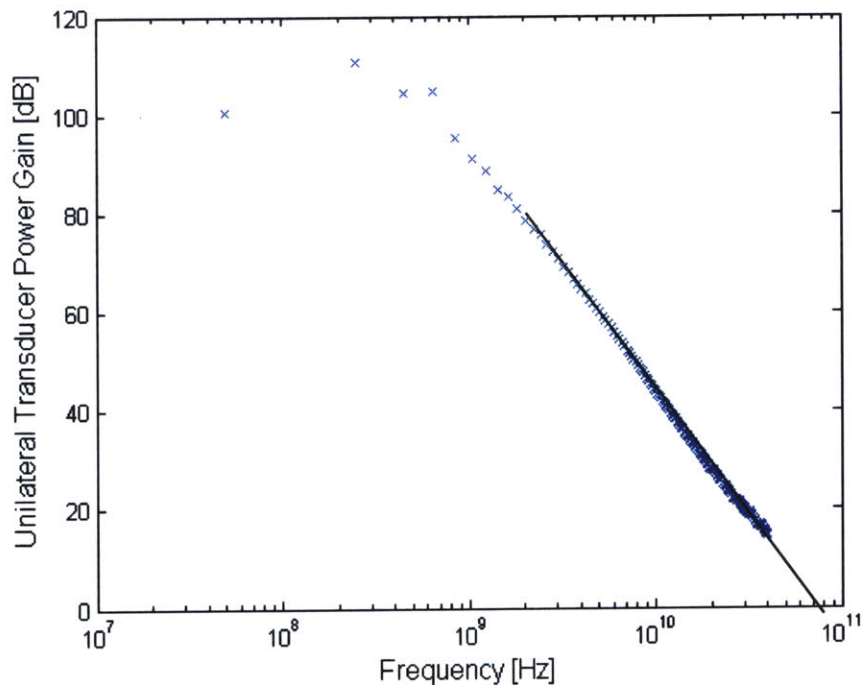
Fig. 2-5: Typical measurement to determine f_{max} on a L_{RD} = 0.3 um device at V_{DS} = 5 V, I_D = 100 mA/mm.

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extrapolating G_{TU} to the frequency where it is equal to one (Fig. 2-5). Since f_{max} encompasses parasitic as well as the intrinsic element values [16], the G_{TU} roll-off can deviate strongly from −20 dB/dec. Plots of f_{max} vs. bias help select the optimum bias point for high-frequency operation.

2.3.2.c Small Signal Equivalent Circuit Extraction

The extraction of a small signal equivalent circuit of the PHEMT is critical to understanding the evolution of the device physics with V_{DS} and L_{RD}. To analyze the bias dependence of the intrinsic small signal equivalent circuit elements, the S-parameters are measured at several bias points and used to extract equivalent circuit values for each point. However, an excellent fit of the model to as-measured S-parameters is not sufficient to ensure that the equivalent circuit values were accurately determined. To correctly identify physical values, the device must be modeled over a broad range of bias conditions.

Extracting the intrinsic equivalent circuit elements is a twofold process with involves first extracting the pad parasitic capacitances (i.e., C_{PG} and C_{PD}) and secondly extracting the rest of
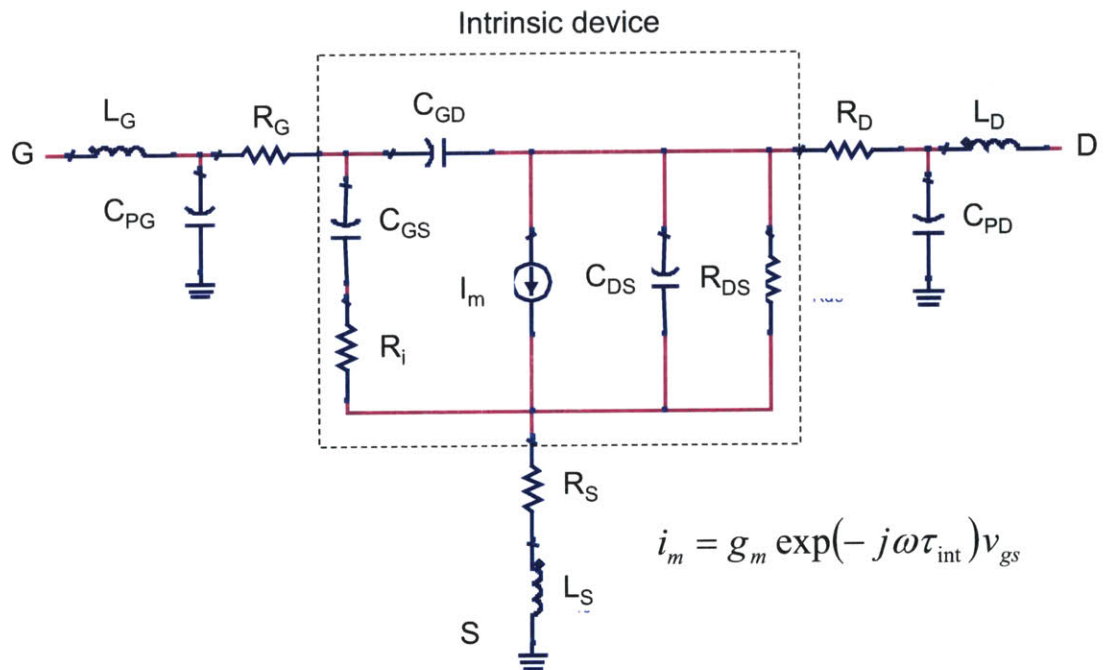
Fig. 2-6: PHEMT equivalent circuit model.

$$i_m = g_m \exp(-j\omega\tau_{int})v_{gs}$$

the extrinsic elements (i.e., L_S, L_G, L_D, R_S, R_G, R_D) [17-19]. The small signal model shown in Fig. 2-6 represents the PHEMT equivalent circuit model. Using a HP 8510 vector network analyzer and 40A GGB Picoprobes, S-parameter measurements were measured from 0.05 to 40 GHz. The parasitic gate and drain capacitances were estimated from the low-frequency (<5 GHz) Y-parameters of the device biased beyond pinch-off at zero drain voltage [20]. Ideally, the pad parasitic elements should be measured using a special open structure of the pad structure without the device [19]. However, such a structure was not available on the wafer and we were not able to proceed with this version of the de-embedding of the pad parasitics. In general, since the pad capacitances are on the same magnitude as the intrinsic capacitances, they should be de-embedded from the as-measured Y-parameters of the device under test before proceeding to the extrinsic elements.

Using a procedure described by Caddemi, we extracted the extrinsic elements from the Z-parameters of the device with $V_{DS} = V_{GS} = 0$ V [19]. After de-embedding the parasitic capacitances and extrinsic elements, we extracted the small signal circuit elements using the following formulations [16]:

$$Y_{gs} = Y_{11} + Y_{12} \tag{1}$$

$$Y_{gd} = -Y_{12} \tag{2}$$

$$Y_{ds} = Y_{22} + Y_{12} \tag{3}$$

$$Y_{gm} = Y_{21} - Y_{12} \tag{4}$$

$$C_{gs} = -\frac{1}{\omega \cdot \text{Im}\left(1 / Y_{gs}\right)} \tag{5}$$

$$R_i = \frac{1}{\text{Re}\left(Y_{gs}\right)} \tag{6}$$

$$C_{gd} = -\frac{1}{\omega \cdot \text{Im}\left(1 / Y_{gd}\right)} \tag{7}$$

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$$R_{ds} = \frac{1}{\mathrm{Re}(Y_{ds})} \tag{8}$$

$$g_m = g_{m0} \cdot e^{-j\omega\tau_{int}} = Y_{gm} \cdot \left(1 + j \cdot \omega \cdot \tau_{gm}\right) \tag{9}$$

$$g_{m0} = \left| Y_{gm} \cdot \left(1 + j \cdot \omega \cdot \tau_{gm}\right) \right| \tag{10}$$

$$\tau_{int} = \angle\left(Y_{gm} \cdot \left(1 + j \cdot \omega \cdot \tau_{gm}\right)\right) \cdot \frac{1}{\omega} \tag{11}$$

In the equation (9), τ_{gm} models the roll-off of Y_{gm} at high frequencies. Since the values for the circuit elements are only approximate, we enlisted the aid of HP Advanced Design Software (ADS) to refine our values to get as accurate a fit as possible. Using the extracted values as initial values, we performed an optimization against the raw S-parameters while allowing the intrinsic component values to vary by 50% and extrinsic component values by 10%. The extrinsic value components did not vary much in the optimization, which is as expected and provides evidence that the initial values were accurate starting points.

2.3.2.d Delay Analysis

To gain insight into what factors contribute to the performance of the PHEMT, it is useful to extract the intrinsic delay τ_{int} from f_{Ti}. After performing the de-embedding procedure described in section 2.3.2.c, we determine f_{Ti} from the −20 dB/dec roll-off of the current gain and compute the intrinsic delay with the following formula:

$$\tau_{int} = \frac{1}{2\pi f_{Ti}}$$

where τ_{int} can be decomposed into two components as a function of V_{DS}: the drain delay ($\tau_{tr,d}$) associated with carrier transport across the depletion region on the drain side and the intrinsic transit delay ($\tau_{tr,i}$) associated with carrier transport across the gate region [21]. As an example, τ_{int} of the L_{RD} = 0.3 um device is plotted against V_{DS}. The minimum τ_{int} at roughly $V_{DS,SAT}$ represents

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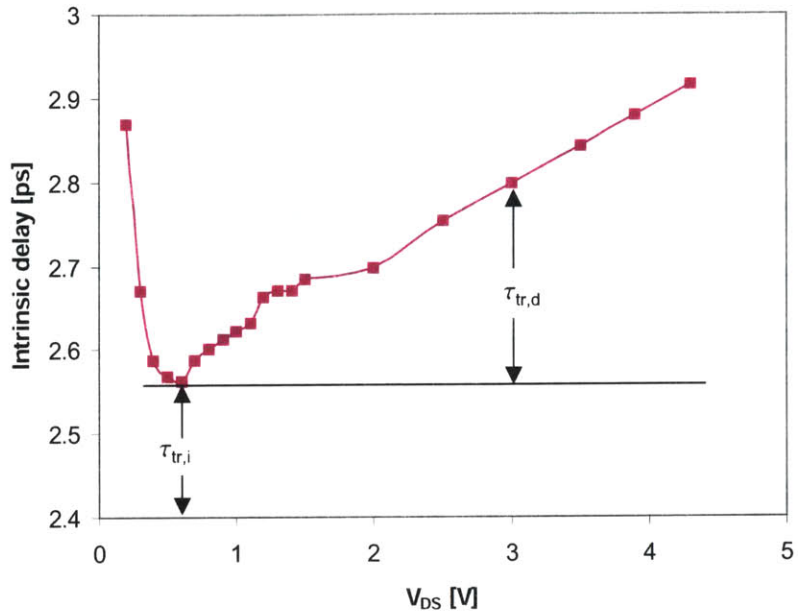
Fig. 2-7: Intrinsic delay τ_{int} versus V_{DS} of a $L_{RD} = 0.3$ um device. V_{GS} was chosen to be -0.2 V to attain the smallest τ_{int} possible for this device.

$\tau_{tr,i}$ while the increase in τ_{int} with increasing V_{DS} is attributed to $\tau_{tr,d}$ (Fig. 2-7). An in-depth discussion of the delay analysis is described in Chapter 3.

2.4 Conclusions

We will be performing large signal measurements on a load pull station that utilizes automated and commercially available Maury Microwave software. We will also be measuring and analyzing S-parameter measurements performed over a wide range of biases. To determine the intrinsic small signal equivalent circuit elements, we must strip the pad parasitic and extrinsic elements from the as-measured S-parameters in a twofold process. From the intrinsic equivalent circuit model, we can determine f_{Ti} and extract τ_{int}. In addition, we can take the small signal analysis a step further by decomposing τ_{int} into its individual components.

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Chapter 3: Impact of L_{RD} on RF Measurements

We will investigate the RF performance of PHEMTs with different values of L_{RD} under two modes of operation: small signal and large signal. We have examined the impact of bias current, bias voltage, and frequency. The goal is to identify the optimum L_{RD} as a function of frequency and to uncover the physical origin of the RF performance of the devices.

3.1 Large Signal Measurements

We have performed load pull measurements on devices with different L_{RD} and seek to identify trends in the large signal behavior across I_{D0}, L_{RD}, V_{DD}, and frequency.

3.1.1 Across I_{D0}

At 8 GHz, we have conducted load pull measurements with small signal drain currents $I_{D0} = 100$ mA/mm, 150 mA/mm, and 200 mA/mm to explore their impact on power performance on devices with different values of L_{RD} (Figs. 3-1 to 3-8). For all of the measurements, we have optimized the source and load impedances for maximum PAE at the 3-dB compression point. Comparing the gain compression behavior when I_{D0} is varied from 100 mA to 200 mA in Figs. 3-1 through 3-4,
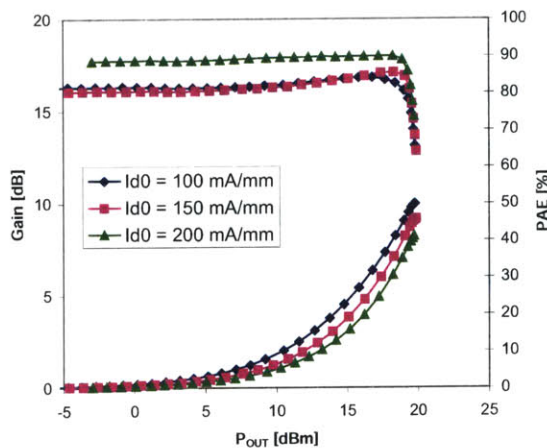
Fig. 3-1: Gain and PAE of $L_{RD} = 0.3$ um device with $V_{DD} = 6$ V and $I_{D0} = 100$, 150, and 200 mA/mm.
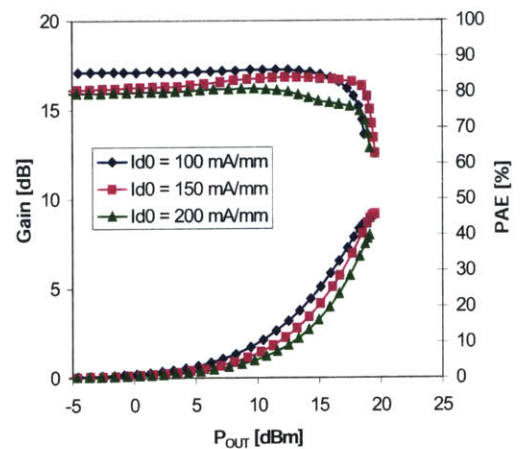
Fig. 3-2: : Gain and PAE of $L_{RD} = 0.5$ um device with $V_{DD} = 6$ V and $I_{D0} = 100$, 150, and 200 mA/mm.

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there is very little improvement in $P_{OUT,3-dB}$ (no more than 0.2 dBm for all four devices). The PAE at the 3-dB compression point suffers as I_{D0} is increased due to the increase in DC power consumption; in fact, the drop in PAE at the 3-dB compression point is much more severe across I_{D0} the longer L_{RD} becomes. This is one reason why it is more advantageous to bias a device at a high V_{DD}, low I_{D0} rather than a low V_{DD}, high I_{D0} for RF power applications. For a given device, the rise in I_G occurs at approximately the same P_{OUT} regardless of I_{D0}; however, the degree of self-bias appears to lessen as I_{D0} is increased (Figs. 3-5 to 3-8).

These results suggest that there is no significant advantage in increasing I_{D0} to attain higher $P_{OUT,3-dB}$. In general, the devices experience greater self-bias as I_{D0} decreases. Even though the self-biased I_D at the 3-dB compression point is slightly higher when I_{D0} = 200 mA/mm, this condition does not ensure a greater $P_{OUT,3-dB}$. Between class A and class AB operation, $P_{OUT,3-dB}$ is roughly constant [22].
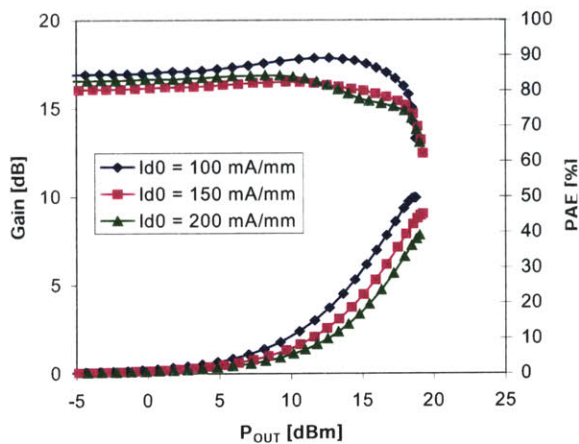
Fig. 3-3: Gain and PAE of L_{RD} = 0.7 um device with V_{DD} = 6 V and I_{D0} = 100, 150, and 200 mA/mm.
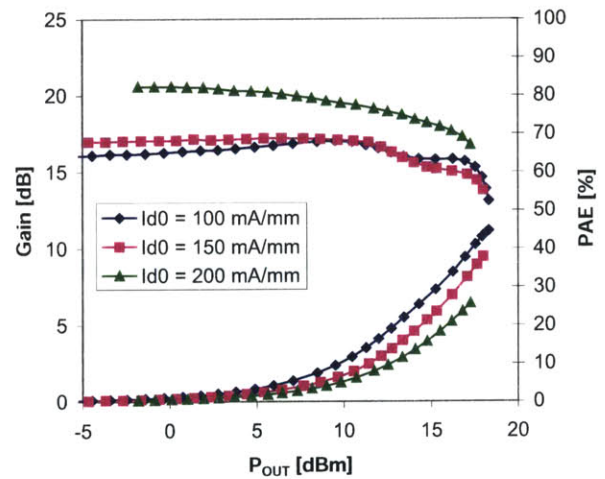
Fig. 3-4: Gain and PAE of L_{RD} = 0.9 um device with V_{DD} = 6 V and I_{D0} = 100, 150, and 200 mA/mm.
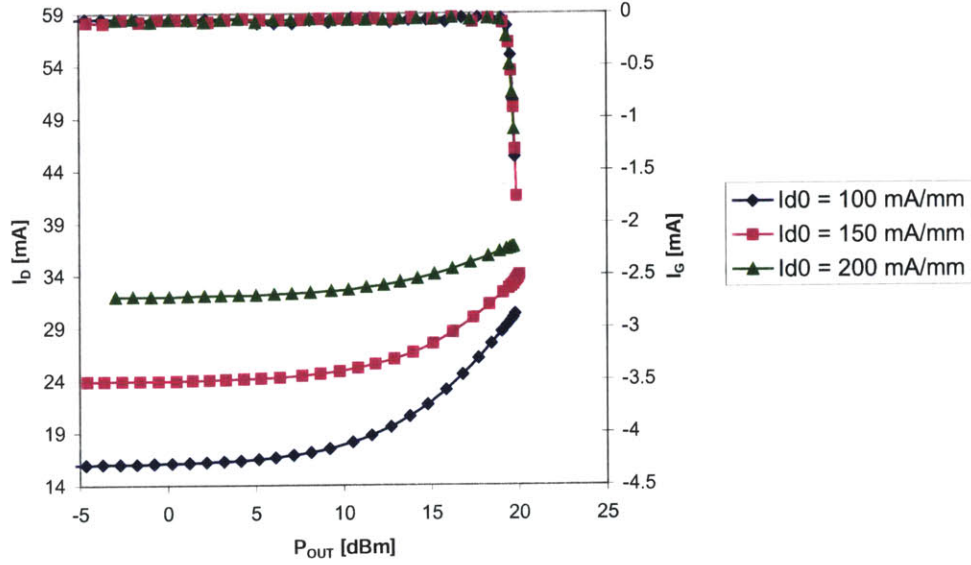
Fig. 3-5: I_D and I_G of L_{RD} = 0.3 um device with V_{DD} = 6 V and I_{D0} = 100, 150, and 200 mA/mm. The resolution of the gate current is 1 mA.
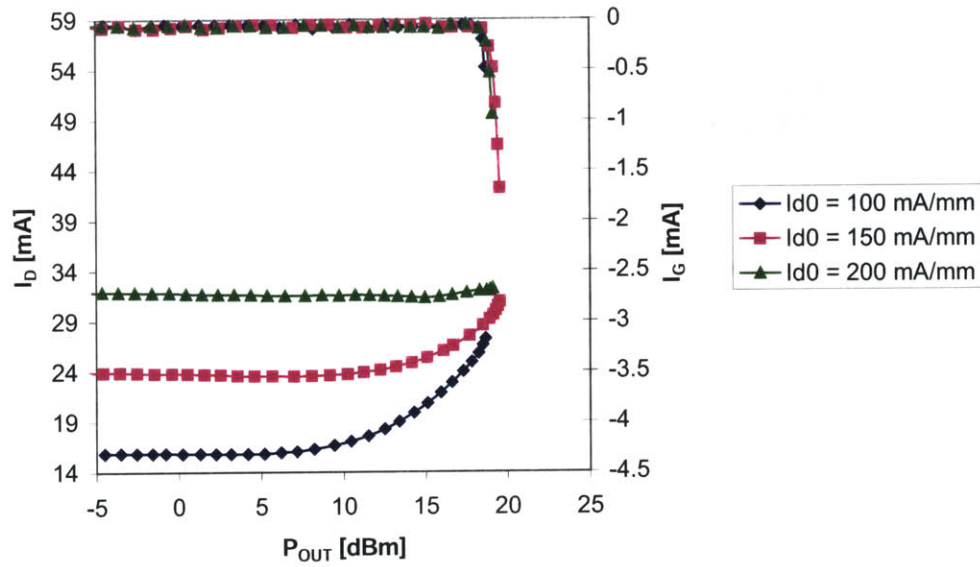
Fig. 3-6: I_D and I_G of L_{RD} = 0.5 um device with V_{DD} = 6 V and I_{D0} = 100, 150, and 200 mA/mm. The resolution of the gate current is 1 mA.
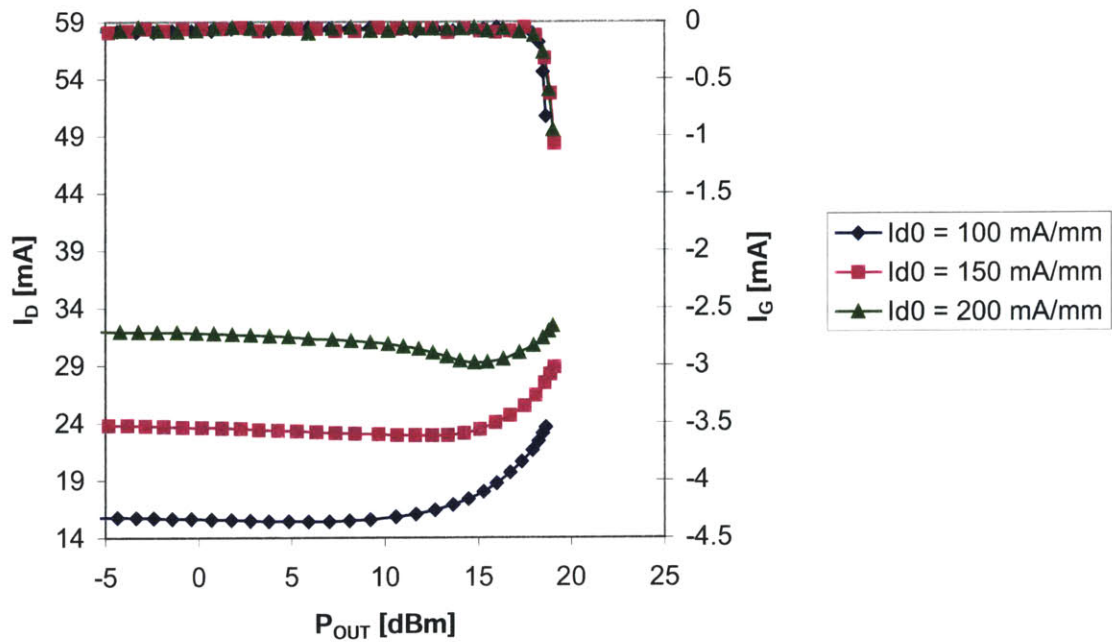
Fig. 3-7: I_D and I_G of L_{RD} = 0.7 um device with V_{DD} = 6 V and I_{D0} = 100, 150, and 200 mA/mm. The resolution of the gate current is 1 mA.
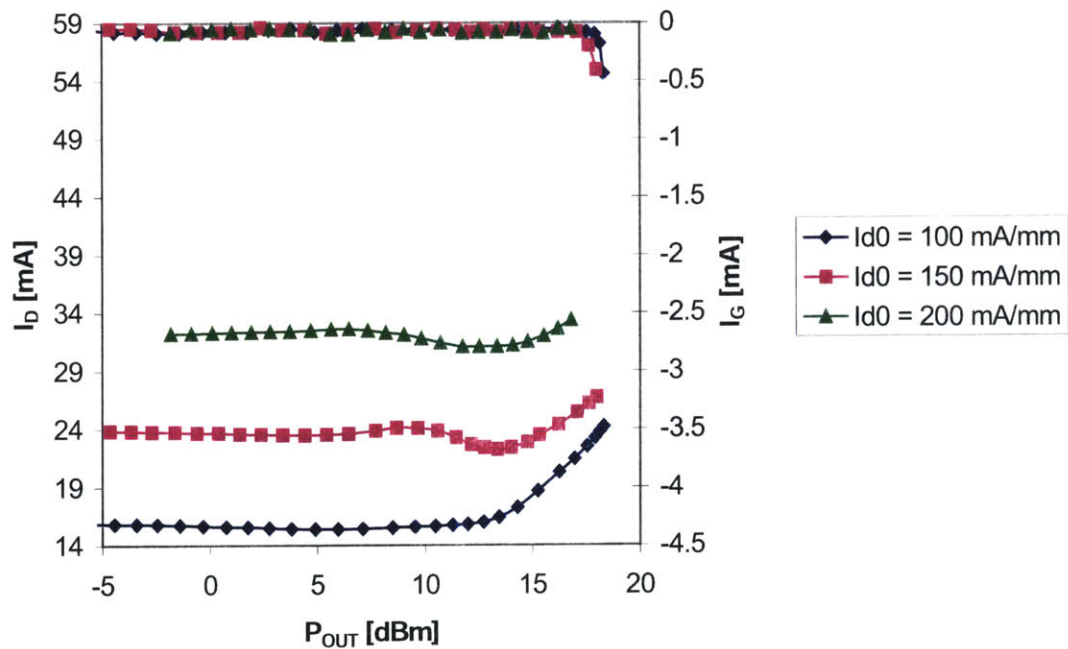
Fig. 3-8: I_D and I_G of L_{RD} = 0.9 um device with V_{DD} = 6 V and I_{D0} = 100, 150, and 200 mA/mm. The resolution of the gate current is 1 mA.

3.1.2 Across L_{RD}

As L_{RD} is increased from 0.3 to 0.9 um at 12 GHz, the gain compresses in an increasingly premature fashion, leading to a decrease in $P_{OUT,3-dB}$ (Fig. 3-9). The L_{RD} = 0.9 um device also exhibits very soft compression compared to the L_{RD} = 0.3 um device. In addition, the PAE at the 3-dB compression point decreases with increasing L_{RD}; for instance, the PAE at the 3-dB compression point decreases from 47% for the shortest L_{RD} device to 28% for the longest L_{RD} device (Fig. 3-9).

The different L_{RD} devices also exhibit different RF induced biasing behavior; the shorter L_{RD} devices (0.3, 0.5 um) devices consistently experience a higher degree of self-bias than the longer L_{RD} (0.7, 0.9 um) devices as they are driven into compression (Fig. 3-10). For all device types, I_G increases dramatically as the gain approaches the 3-dB compression point despite key differences in BV_{off}. The longer L_{RD} is, the sooner the devices experience an increase in I_G. This is consistent with the premature compression of the long L_{RD} devices.
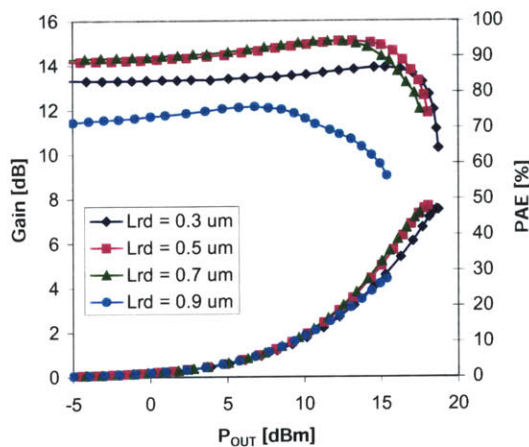
Fig. 3-9: Gain and PAE versus P_{OUT} for devices with varying L_{RD} at 12 GHz and V_{DD} = 5 V, I_{D0} = 100 mA/mm.
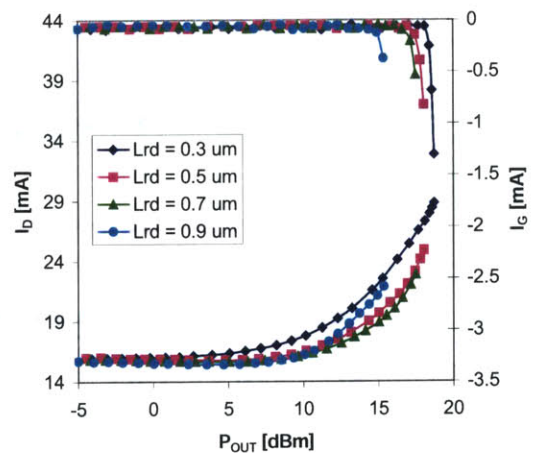
Fig. 3-10: Drain and gate current versus P_{OUT} for devices with varying L_{RD} at 12 GHz and V_{DD} = 5 V, I_D = 100 mA/mm. The resolution of the gate current is 1 mA.

3.1.3 Across V_{DD}

We have studied in more detail the behavior of the shortest L_{RD} (0.3 um) and longest L_{RD} (0.9 um) device as a function of V_{DD} at 12 GHz. In general, increasing V_{DD} directly translates into a higher $P_{OUT,3-dB}$. The gain compression behavior is softer at higher V_{DD} for the L_{RD} = 0.9 um device than the L_{RD} = 0.3 um device (Figs. 3-11 to 3-12). The PAE at the 3-dB compression point is consistently higher for the L_{RD} = 0.3 um device than the L_{RD} = 0.9 um device; for instance, at V_{DD} = 6 V, it decreased from 41% to 33% as L_{RD} is increased from 0.3 to 0.9 um.
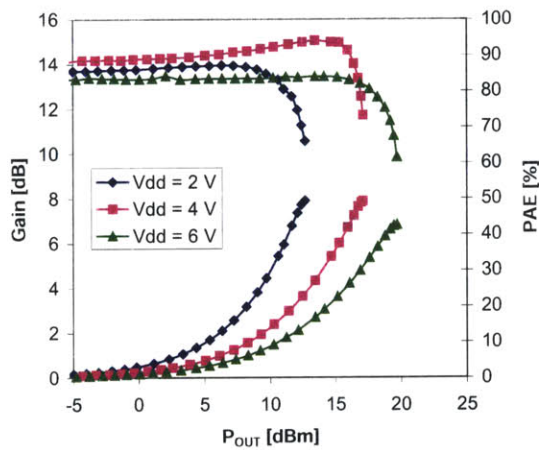
Fig. 3-11: Gain and PAE versus P_{OUT} for device with L_{RD} = 0.3 um for varying V_{DD} and I_{D0} = 100 mA/mm at 12 GHz.
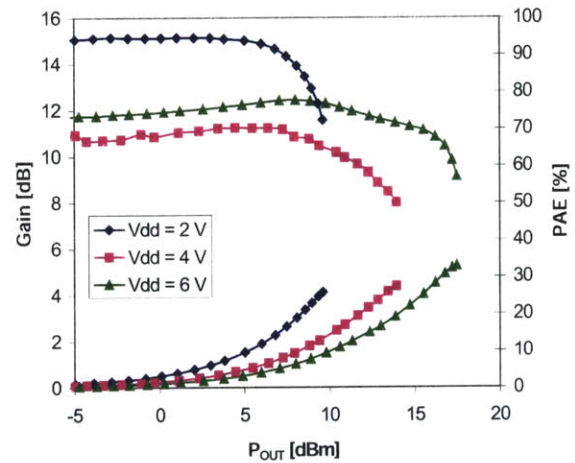
Fig. 3-12: Gain and PAE versus P_{OUT} for device with L_{RD} = 0.9 um for varying V_{DD} and I_{D0} = 100 mA/mm at 12 GHz.
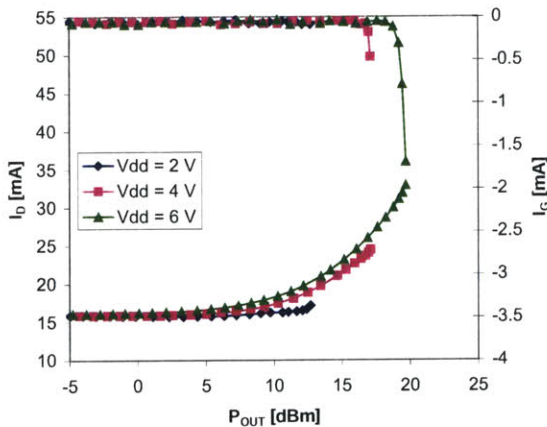
Fig. 3-13: Drain and gate current versus P_{OUT} for device with L_{RD} = 0.3 um for varying V_{DD} and I_{D0} = 100 mA/mm at 12 GHz. The resolution of the gate current is 1 mA.
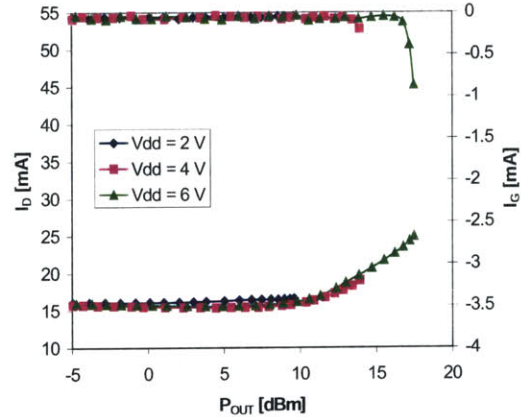
Fig. 3-14: Drain and gate current versus P_{OUT} for device with L_{RD} = 0.9 um for varying V_{DD} and I_{D0} = 100 mA/mm at 12 GHz. The resolution of the gate current is 1 mA.

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A useful indicator of the physical mechanism dominating power saturation is the RF induced gate current as a function of P_{IN}. If reverse breakdown is dominating power saturation, I_G will be negative [23]. The gate breakdown mechanism places a fundamental limit upon the RF power capability of the device by limiting the maximum swing of the drain voltage and current waveforms. As the drain voltage waveform enters the breakdown voltage region, significant waveform clipping occurs and I_G increases rapidly as holes generated by impact ionization exit the gate. The RF performance soon degrades, limiting the magnitude of the drain bias that can be applied. On the other hand, if the drain bias is too low, power saturation will be dominated by either forward conduction or the RF-IV curves hitting $V_{DS,SAT}$. If forward conduction occurs, we expect that the sign of the RF induced I_G will be positive; if the RF-IV curves are hitting $V_{DS,SAT}$, I_G will not rectify as the device enters saturation [23]. Rectification of I_G is accompanied by a shifting of the quiescent point, which occurs with a rise in I_D. The rise in I_D with RF drive is referred to as the self-bias and generally increases as the device enters compression.

In general, as V_{DD} is increased, the device experiences a higher degree of self-bias and higher levels of I_G due to a greater interaction with the breakdown voltage region. At V_{DD} = 2 V, only a very slight rise in I_G or self-bias is observed for either the L_{RD} = 0.3 or 0.9 um device (Figs. 3-13 and 3-14). Since the load line does not interact with the breakdown voltage at V_{DD} = 2 V, it makes sense that I_D and I_G did not change much from their respective DC levels. However, as V_{DD} increased to 4 and 6 V, the L_{RD} = 0.3 um device (Fig. 3-13) experiences an increasing level of degree of self-bias and I_G than the L_{RD} = 0.9 um device (Fig. 3-14). This is most likely attributed to the lower BV_{off} of the L_{RD} = 0.3 um device.

The next step is to compare $P_{OUT,3-dB}$ for the different devices as a function of drain bias. At 8 GHz, the highest $P_{OUT,3-dB}$ can be achieved with the L_{RD} = 0.7 um device at V_{DD} = 9 V due to the higher allowable maximum V_{DD} that is possible before the device degrades rapidly; however, a higher $P_{OUT,3-dB}$ could not be achieved with the L_{RD} = 0.9 um device at a drain bias of 10 V (Fig. 3-

15). At 12 and 16 GHz, the L_{RD} = 0.5 um device yields the highest $P_{OUT,3-dB}$ across drain bias (Figs. 3-16 and 3-17). At these two frequencies, catastrophic burnout limited the maximum drain bias that can be applied to the longer L_{RD} devices. This will be explored in further detail in Section 3.1.5. At 8 GHz, the L_{RD} = 0.3 um device consistently exhibits higher PAE than the L_{RD} = 0.9 um device across V_{DD} (Fig. 3-18). At 12 and 16 GHz, the PAE at the 3-dB compression point is very close for the L_{RD} = 0.3 through 0.7 um devices while the longest L_{RD} device consistently exhibits the lowest PAE (Figs. 3-19 and 3-20).
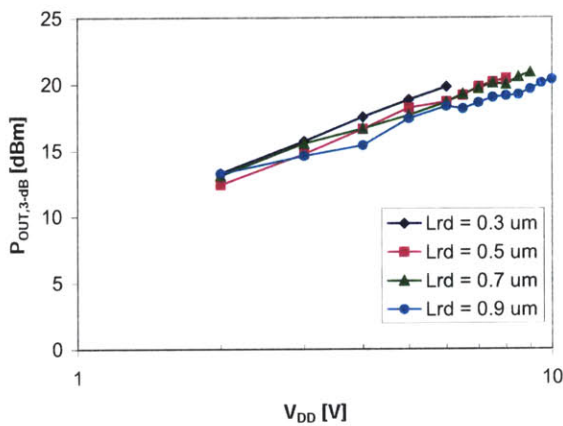
Fig. 3-15: $P_{OUT,3-dB}$ versus V_{DD} for different L_{RD} devices at 8 GHz and I_{D0} = 100 mA/mm.
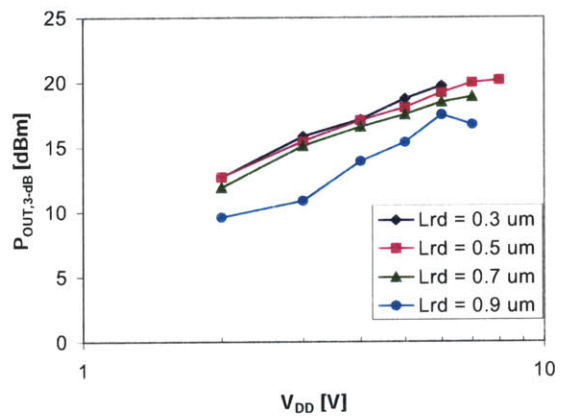
Fig. 3-16: $P_{OUT,3-dB}$ versus V_{DD} for different L_{RD} devices at 12 GHz and I_{D0} = 100 mA/mm.
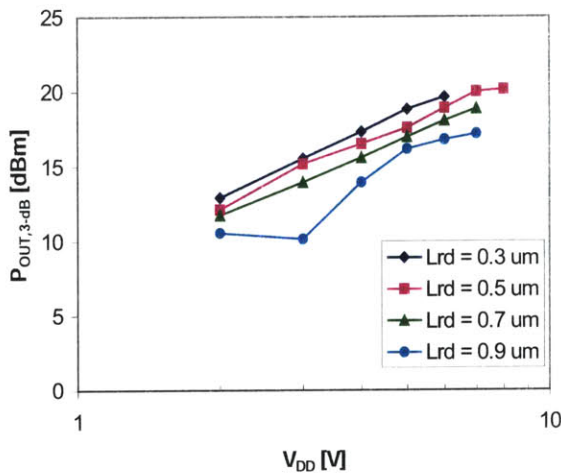
Fig. 3-17: $P_{OUT,3-dB}$ versus V_{DD} for different L_{RD} devices at 16 GHz and I_{D0} = 100 mA/mm.
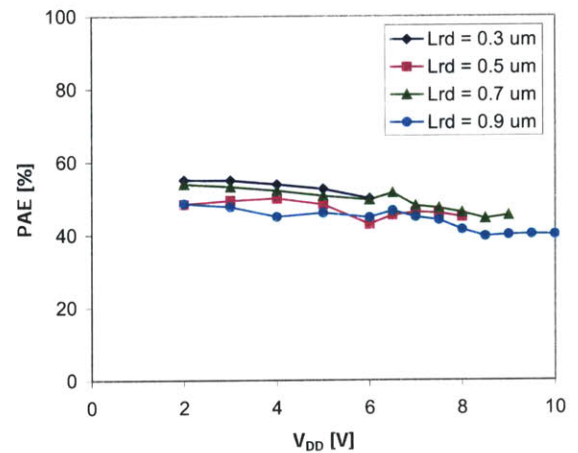
Fig. 3-18: Peak PAE versus V_{DD} for different L_{RD} devices at 8 GHz and I_{D0} = 100 mA/mm.

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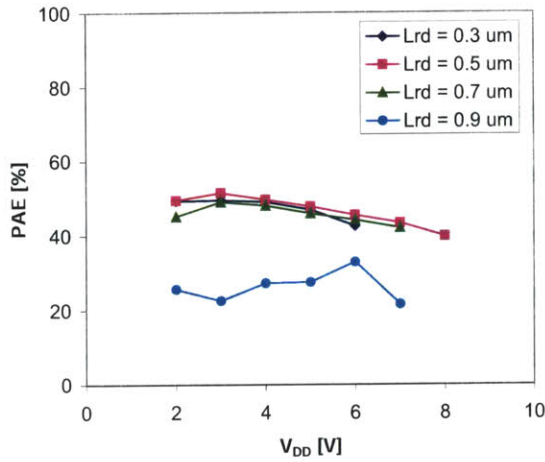
Fig. 3-19: Peak PAE versus V_{DD} for different L_{RD} devices at 12 GHz and I_{D0} = 100 mA/mm.
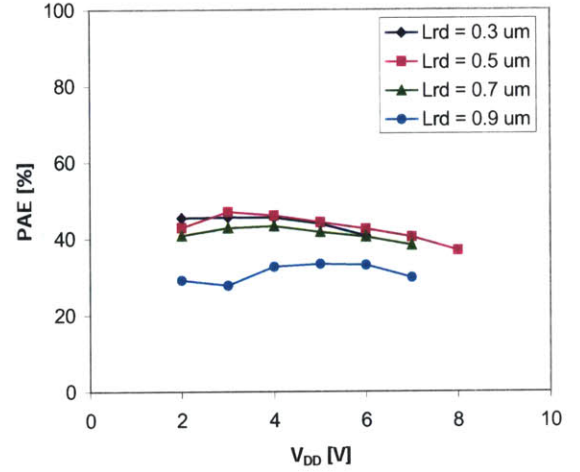
Fig. 3-20: Peak PAE versus V_{DD} for different L_{RD} devices at 16 GHz and I_{D0} = 100 mA/mm.

3.1.4 Across Frequency

If we consider the output power as a function of frequency, the steepness of the decline in $P_{OUT,3\text{-}dB}$ depends strongly on L_{RD} (Fig. 3-21). The L_{RD} = 0.3 um device experiences virtually no change in $P_{OUT,3\text{-}dB}$ when the frequency is increased from 8 to 16 GHz; however, a progressively larger spread in $P_{OUT,3\text{-}dB}$ is observed as L_{RD} is increased. The spread is the largest for the L_{RD} = 0.9 um device, with $P_{OUT,3\text{-}dB}$ decreasing from 18.3 dBm at 8 GHz to 16.8 dBm at 16 GHz. The steep decline in $P_{OUT,3\text{-}dB}$ device for the L_{RD} = 0.9 um is a anomalous feature that cannot be explained by large signal models [8]. The drop in $P_{OUT,3\text{-}dB}$ may be attributed to the extension of the depletion region with increasing L_{RD} as seen later in Section 3.2.4. There is a frequency response associated with the mechanisms responsible for this extension of the depletion region [24]. The exact nature of this behavior is highly dependent on the severity of surface states, which we will explore in further detail in Section 5.4.
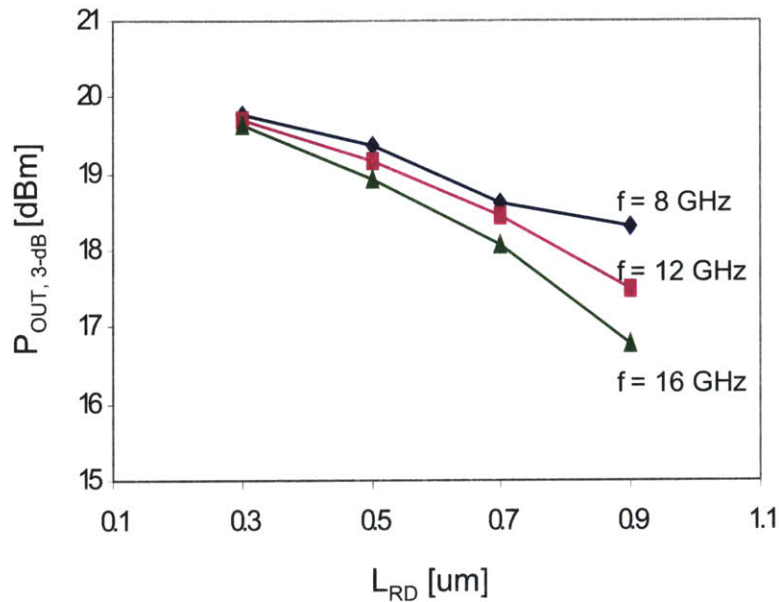
Fig. 3-21: $P_{OUT,3-dB}$ versus L_{RD} at small signal bias of V_{DD} = 6 V and I_{D0} = 100 mA/mm. $P_{OUT,3-dB}$ for the L_{RD} = 0.3 and 0.5 um do not fluctuate much with frequency. However, the 0.7 and 0.9 um devices experience an increasingly larger drop in $P_{OUT,3-dB}$ with increasing frequency.

3.1.5 Reliability Study

We are interested in defining what mechanism limits the maximum V_{DD} that can be applied to the devices under study. This is because the higher the V_{DD}, the higher the power that can be extracted from the device. In each load pull measurement plan, V_{DD} was ramped starting at 2 V and was increased in 1 V increments. The source and load impedances were optimized for PAE at the 3-dB compression point. After a full RF characterization was performed at the target V_{DD} point, a verification measurement was performed at a benign bias of V_{DD} = 2 V and I_{D0} = 100 mA/mm at the initial optimized impedances after each load pull measurement to track the degree of resultant degradation experienced by the device. As V_{DD} is increased, the device experiences increasing damage as evidenced in the change in V_{GS}, gain, PAE, and $P_{OUT,3-dB}$. Although we do not change the initial optimized impedances used for each verification measurement, these impedance points no longer reflect the true optimum impedances at V_{DD} = 2 V as the device degrades. Ultimately, we found that the maximum V_{DD} possible for each device is limited by either excessive degradation or catastrophic burnout. The measurements shown here are from

data taken at 8 and 16 GHz. Unfortunately, we were only able to collect verification data for the L_{RD} = 0.5 um up to V_{DD} = 4.5 V at 8 GHz due to probe problems.

3.1.5.a V_T

As the device degrades during the V_{DD} sweep, I_{D0} slowly increases and causes V_{GS} to increase in order to maintain the same I_{D0} as before. In other words, the threshold voltage V_T shifts negative as degradation is occurring. At 8 GHz, all four devices experience degradation evidenced by the change in V_T (Fig. 3-22). The onset of V_T shift increases with increasing L_{RD} and the maximum allowable V_{DD} is set by degradation for all of the devices under study. At 16 GHz, as L_{RD} increases from 0.3 to 0.5 um, the onset of degradation is also postponed due to the increase in BV_{OFF}. However, when L_{RD} is increased to 0.7 and 0.9 um, the device suddenly experiences catastrophic burnout (as indicated by the black symbols shown in Fig. 3-23) before they reach the same level of maximum V_{GS} degradation observed for the smaller L_{RD} devices and at 8 GHz. The different limiting factors for attaining maximum V_{DD} for the long L_{RD} devices at 8 and 16 GHz imply that these mechanisms are frequency dependent.
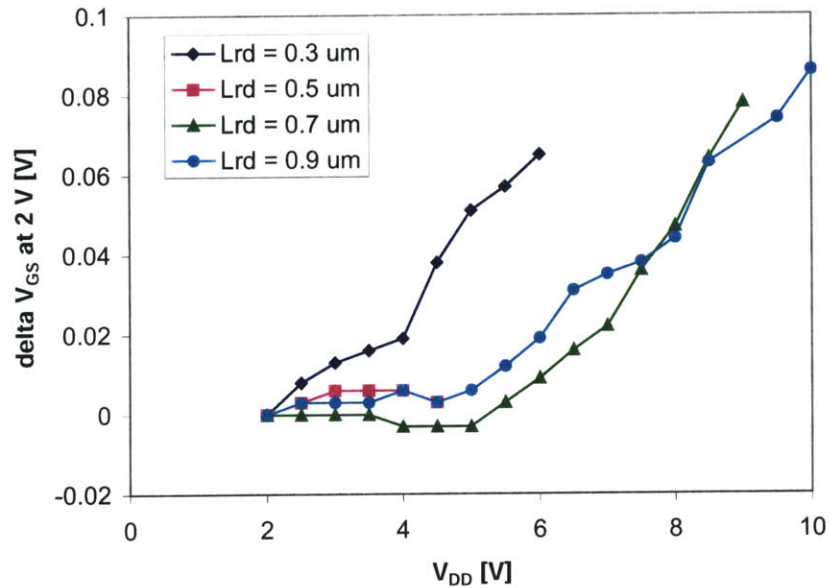
Fig. 3-22: Difference between initial V_{GS} measurement at 2 V needed to maintain I_{D0} = 100 mA/mm and subsequent gain measurements at 2V following measurements at higher V_{DD} indicated on the x-axis at 8 GHz.

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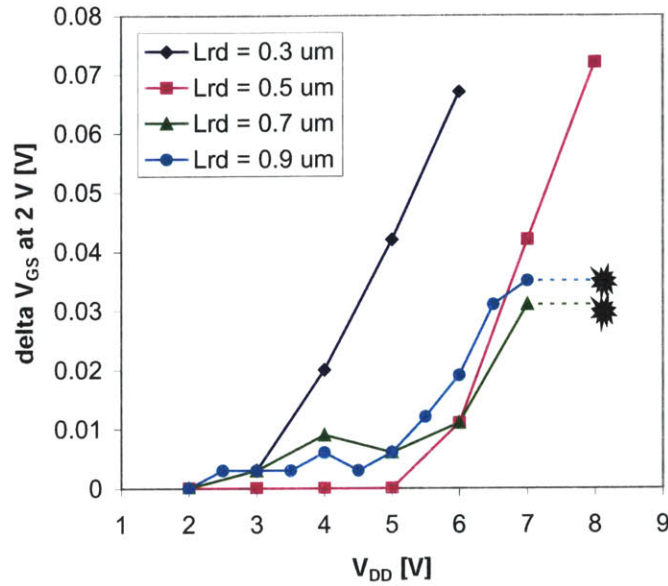
Fig. 3-23: Difference between initial V_{GS} measurement at 2 V needed to maintain $I_{D0} = 100$ mA/mm and subsequent gain measurements at 2V following measurements at higher V_{DD} indicated on the x-axis at 16 GHz. The black marks indicate catastrophic burnout for the $L_{RD} = 0.7$ and 0.9 um devices.

3.1.5.b $P_{OUT,3\text{-}dB}$

Fig. 3-22 tracks the degradation of $P_{OUT,3\text{-}dB}$ with increasing V_{DD} as the device is being slowly damaged by the invasive load pull procedure at 8 GHz. Due to its lower BV_{off}, the $L_{RD} = 0.3$ um device experiences a sharp decrease in $P_{OUT,3\text{-}dB}$ as V_{DD} approaches 6 V. The longer L_{RD} devices appear more robust than the $L_{RD} = 0.3$ um device, with the $L_{RD} = 0.9$ um device showing relatively little fluctuation in $P_{OUT,3\text{-}dB}$ up to $V_{DD} = 10$ V. For all four devices at this frequency, the maximum allowable V_{DD} centers the operating point between $V_{DS,SAT}$ and BV_{off} and is given by [25]:

$$V_{DD} < \left(V_{DS,SAT} + BV_{off}\right)\!/2$$

At 16 GHz, the $L_{RD} = 0.3$ and 0.5 um devices experience a sharp drop in $P_{OUT,3\text{-}dB}$ when V_{DD} becomes high enough (Fig. 3-25). Consequently, it is not possible to attain a higher $P_{OUT,3\text{-}dB}$ with a higher V_{DD}. On the other hand, the $L_{RD} = 0.7$ and 0.9 um devices have very little variation in

$P_{OUT,3\text{-}dB}$ at voltages where the L_{RD} = 0.3 and 0.5 um devices are experiencing sharp degradation. Hence, it was surprising to find that they burned out during the load pull optimization at V_{DD} = 8 V. Even when the optimization was performed on virgin long L_{RD} devices on different chips at V_{DD} = 8 V, they still burnt out during the load pull procedure. This leads us to believe that this effect is a universal problem for longer L_{RD} devices at higher frequencies.
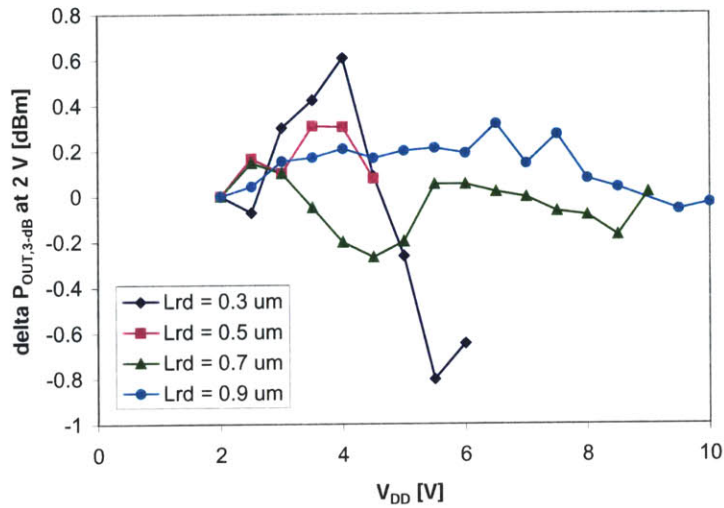
Fig. 3-24: Difference between initial $P_{OUT,3\text{-}dB}$ verification measurement at 2 V and subsequent $P_{OUT,3\text{-}dB}$ measuremzents at 2V following measurements at higher V_{DD} indicated on the x-axis at 8 GHz.
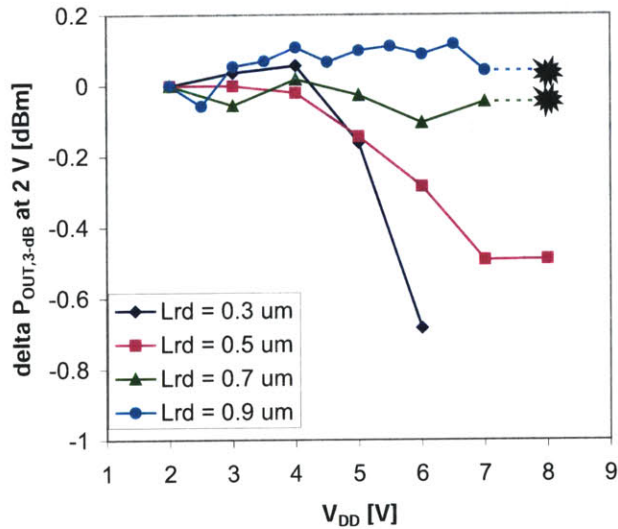
Fig. 3-25: Difference between initial $P_{OUT,3\text{-}dB}$ verification measurement at 2 V and subsequent $P_{OUT,3\text{-}dB}$ measurements at 2V following measurements at higher V_{DD} indicated on the x-axis at 16 GHz. The black marks indicate catastrophic burnout for the L_{RD} = 0.7 and 0.9 um devices.

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3.1.5.c Gain

Similar to the trends shown in the $P_{OUT,3\text{-}dB}$ measurements, the devices suffer a decrease in gain as they are being slowly damaged by the load pull measurement at higher V_{DD}. At 8 GHz, the L_{RD} = 0.9 um device seems to be the most robust of the group; the longer L_{RD} is, the less the gain drops for a given V_{DD} (Fig. 3-26). At 16 GHz, the L_{RD} = 0.3 um device first experiences a decrease in gain at V_{DD} = 4 V (Fig. 3-27). The L_{RD} = 0.5 um device also experiences a decrease in gain but in a less steep fashion than the L_{RD} = 0.3 um device. Finally, the gains of the L_{RD} = 0.7 and 0.9 um devices do not fluctuate more than 0.1 dB before they burn out during the optimization performed at V_{DD} = 8 V.
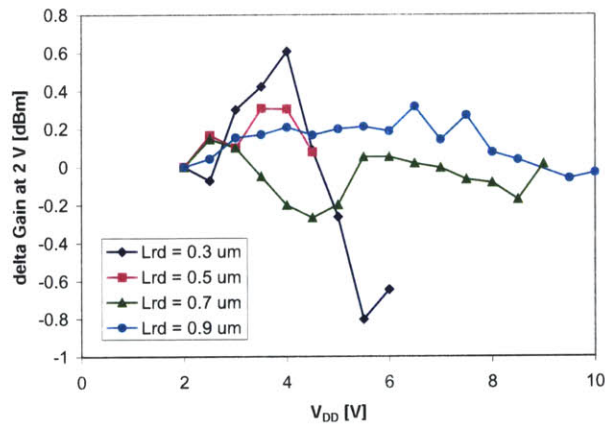
Fig. 3-26: Difference between initial gain verification measurement at 2 V and subsequent gain measurements at 2V following measurements at higher V_{DD} indicated on the x-axis at 8 GHz.
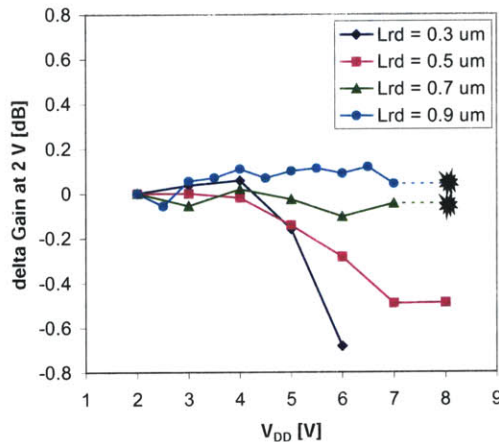
Fig. 3-27: Difference between initial gain verification measurement at 2 V and subsequent gain measurements at 2V following measurements at higher V_{DD} indicated on the x-axis at 16 GHz. The black marks indicate catastrophic burnout for the L_{RD} = 0.7 and 0.9 um devices.

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3.1.5.d PAE

At 8 GHz, the devices show large fluctuations in PAE (±5%) that are most likely due to poor contact between the probes and pads, making it difficult to distinguish a trend (Fig. 3-28). These probing issues were resolved by the time we took the 16 GHz measurements. At 16 GHz, the PAE decreases from its nominal value as the device degrades from load pull measurements performed at successively higher V_{DD} (Fig. 3-29). The L_{RD} = 0.3 and 0.5 um devices begin to show an increase in ΔPAE starting at V_{DD} = 4 V while the L_{RD} = 0.7 um device shows little fluctuation before burnout at V_{DD} = 8 V. Strangely enough, the ΔPAE for the L_{RD} = 0.9 um device appears to increase as high as 5% as V_{DD} goes from 2 to 4.5 V; the large fluctuation is most likely due to a bad initial reading at V_{DD} = 2 V. The low I_G resolution of 1 mA may also contribute to the rough ΔPAE readings.
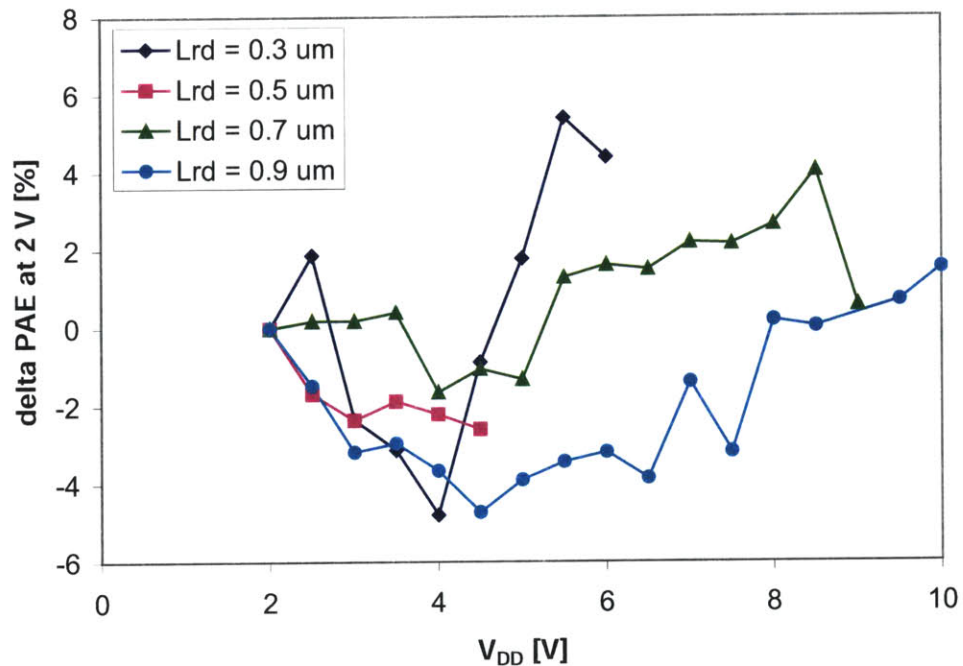
Fig. 3-28: Difference between initial PAE verification measurement at 2 V and subsequent PAE measurements at 2V following measurements at higher V_{DD} indicated on the x-axis at 8 GHz.
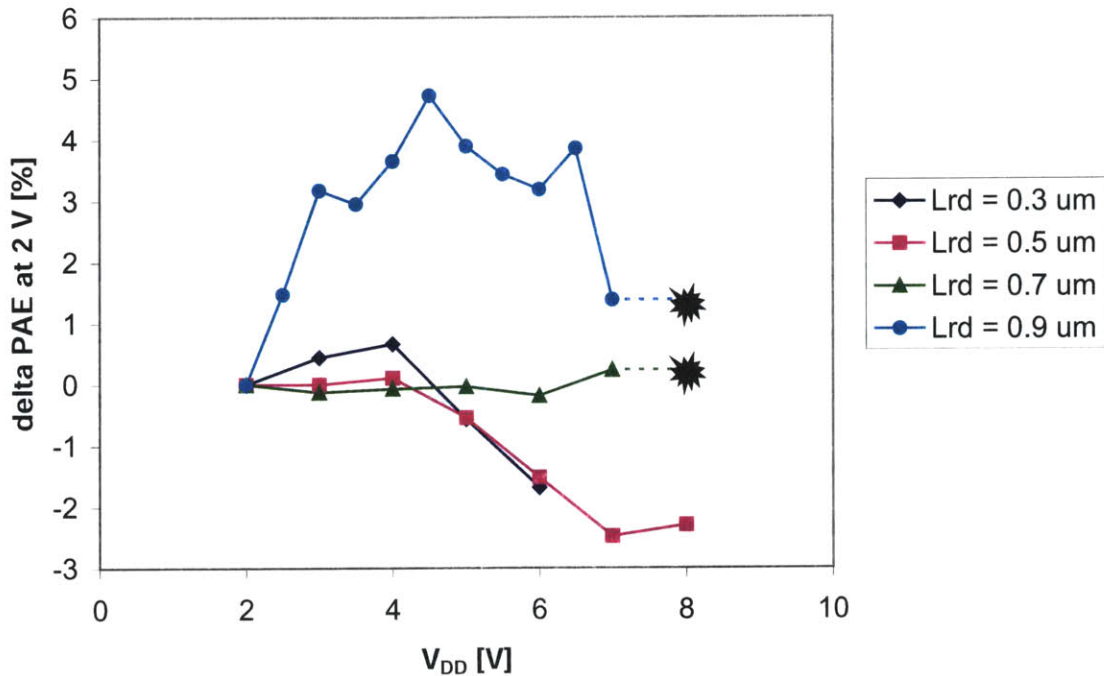
Fig. 3-29: Difference between initial PAE verification measurement at 2 V and subsequent PAE measurements at 2V following measurements at higher V_{DD} indicated on the x-axis at 16 GHz. The black marks indicate catastrophic burnout for the L_{RD} = 0.7 and 0.9 um devices.

3.2 Small Signal Measurements

The ability to model and simulate the small signal characteristics under a wide range of biases is essential to understanding the operation and device physics of the PHEMT. Physical models that predict the Y-parameters of PHEMTs can be used for designing better PHEMTs; for instance, understanding the behavior of f_T vs. bias is important for finding the optimum bias point. Using the procedure described in Chapter 2, we have extracted an equivalent circuit model using S-parameters measured between 0.05 to 40 GHz. This technique has allowed us to extract extrinsic elements at fixed bias points under "short" and "open" conditions and intrinsic elements at the operating bias.

3.2.1 Equivalent Circuit Extraction

Each element of the small signal equivalent circuit model provides insight into the operation of the PHEMT (Fig. 2-6). The transconductance g_m represents the multiple conductive paths (i.e. InGaAs channel, AlGaAs spacer, etc.) that are possible in the device structure. The output resistance R_{ds} is the inverse of the output conductance g_{ds}, which is the incremental change in I_D with respect to V_{DD} while V_{GS} is held constant. The delay time τ_{int} represents the intrinsic delay for the electrons to traverse underneath the gate and across the depletion region on the drain side of the device. The gate-to-source capacitance C_{GS} represents the depletion region under the gate and channel carrier concentration, which depends on V_{GS} and lateral channel potential, and is connected to the channel by a resistance R_i. The gate-to-drain capacitance C_{GD} represents the coupling between the gate and drain. Lastly, the drain-to-source capacitance C_{DS} is representative of the multiple paths of electron conduction within the device structure. Extrinsic inductances L_S, L_G, L_D and extrinsic resistances R_S, R_G, and R_D are included to model the gold bonding pads. In addition, extrinsic package capacitances between the gate electrode and source substrate and drain electrode and source substrate are modeled by C_{PG} and C_{PD}, respectively.

Equivalent circuit extraction was performed at $I_D = 100$ mA/mm and $V_{DD} = 3, 5,$ and 7 V for all four devices with L_{RD} varying between 0.3 and 0.9 um. In regard to accuracy, the extraction of the five main intrinsic parameters of the $L_{RD} = 0.3$ um device (C_{GS}, C_{GD}, C_{DS}, g_m, g_{ds}) are the most accurate because the associated simulated Y-parameters are in good agreement with the experimental data (Figs. 3-30 to 3-33). As L_{RD} increases, it becomes more difficult to maintain the accuracy in fit at high frequencies using the same equivalent circuit model and optimization weights. The comparison between measured and modeled Y-parameters for the $L_{RD} = 0.9$ um device is shown in Figs. 3-34 to 3-37.
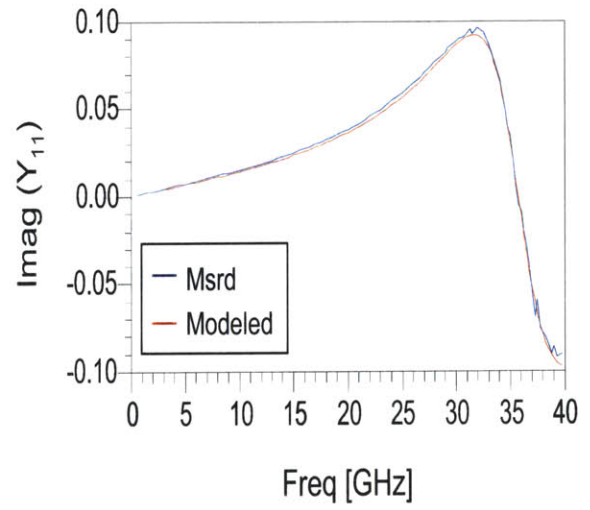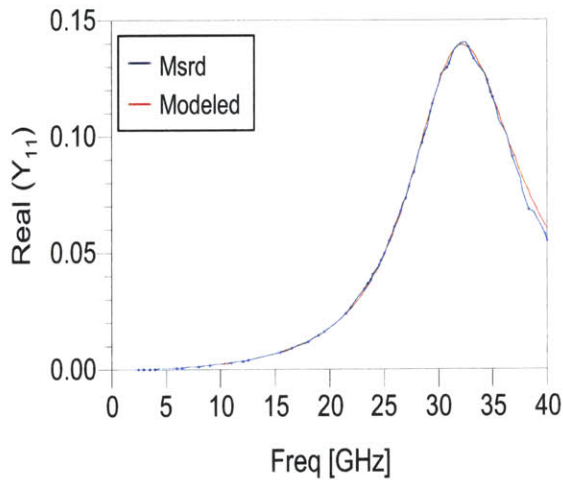
Fig. 3-30: Comparison between measured and modeled Y_{11} for the L_{RD} = 0.3 um device at V_{DD} = 5 V and I_{D0} = 100 mA/mm.
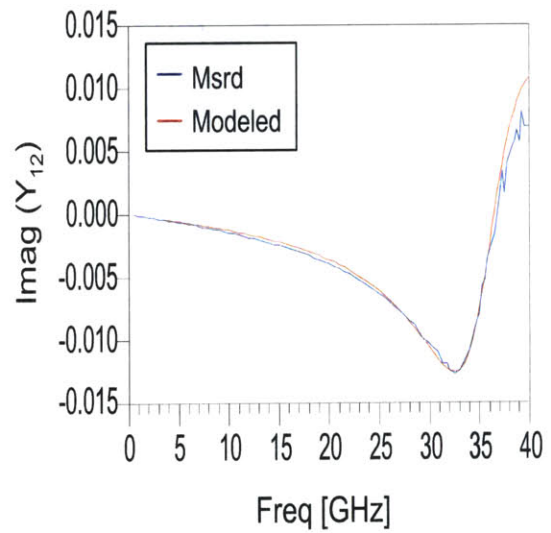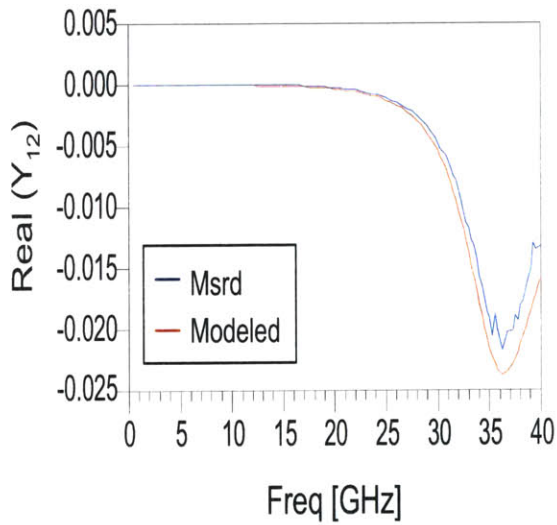
Fig. 3-31: Comparison between measured and modeled Y_{12} for the L_{RD} = 0.3 um device at V_{DD} = 5 V and I_{D0} = 100 mA/mm.

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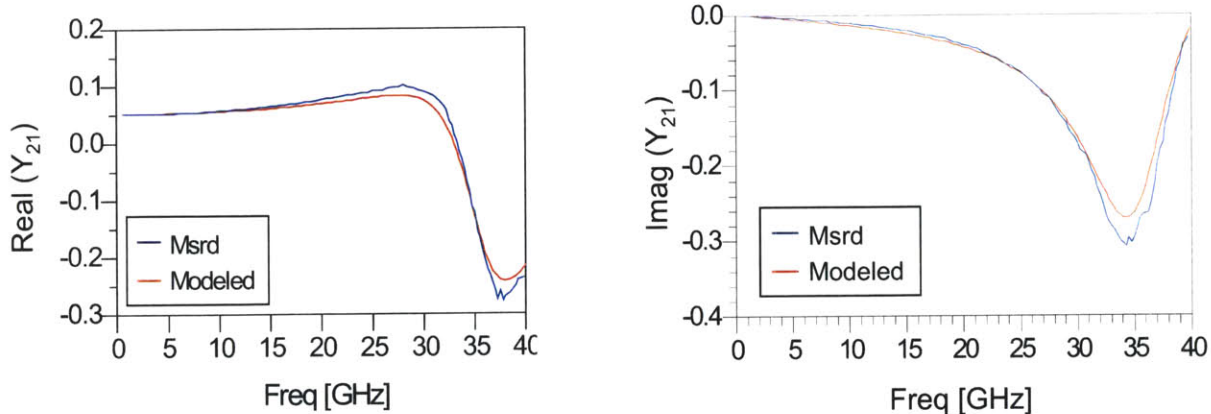
Fig. 3-32: Comparison between measured and modeled Y_{21} for the L_{RD} = 0.3 um device at V_{DD} = 5 V and I_{D0} = 100 mA/mm.
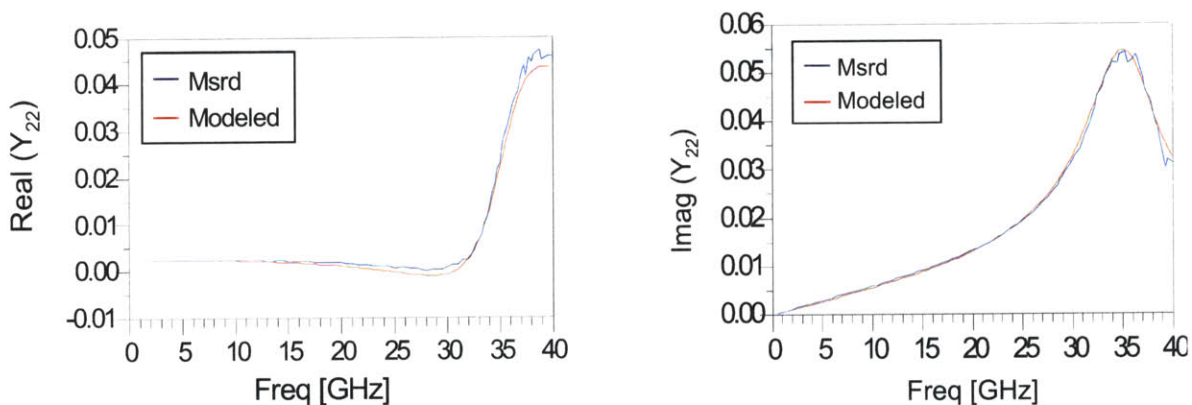
Fig. 3-33: Comparison between measured and modeled Y_{22} for the L_{RD} = 0.3 um device at V_{DD} = 5 V and I_{D0} = 100 mA/mm.
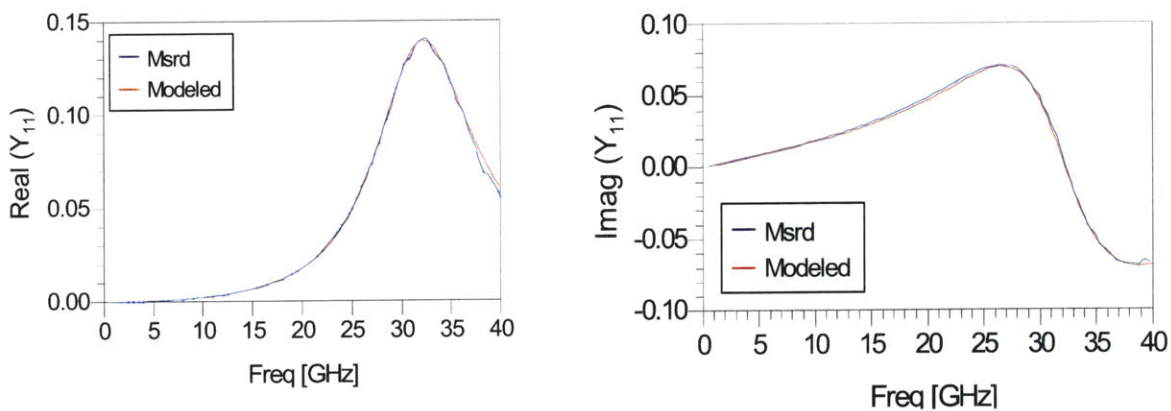
Fig. 3-34: Comparison between measured and modeled Y_{11} for the L_{RD} = 0.9 um device at V_{DD} = 5 V and I_{D0} = 100 mA/mm.
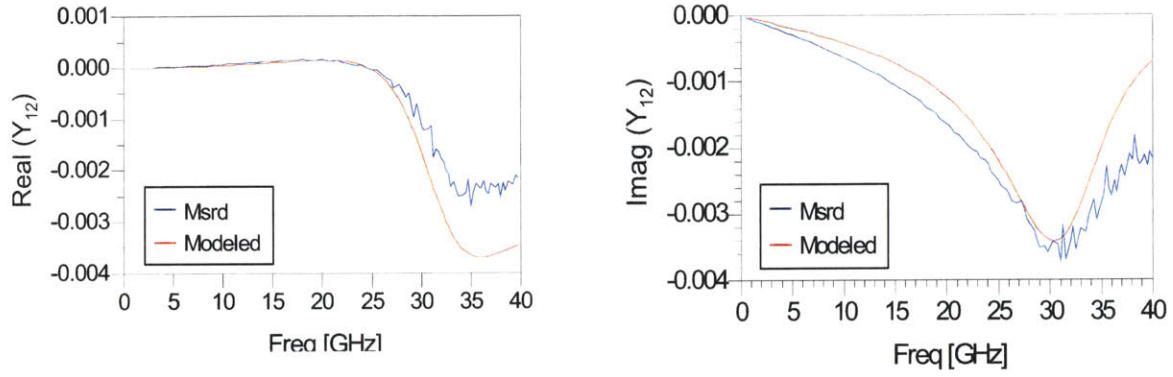
Fig. 3-35: Comparison between measured and modeled Y_{12} for the $L_{RD} = 0.9$ um device at $V_{DD} = 5$ V and $I_{D0} = 100$ mA/mm.
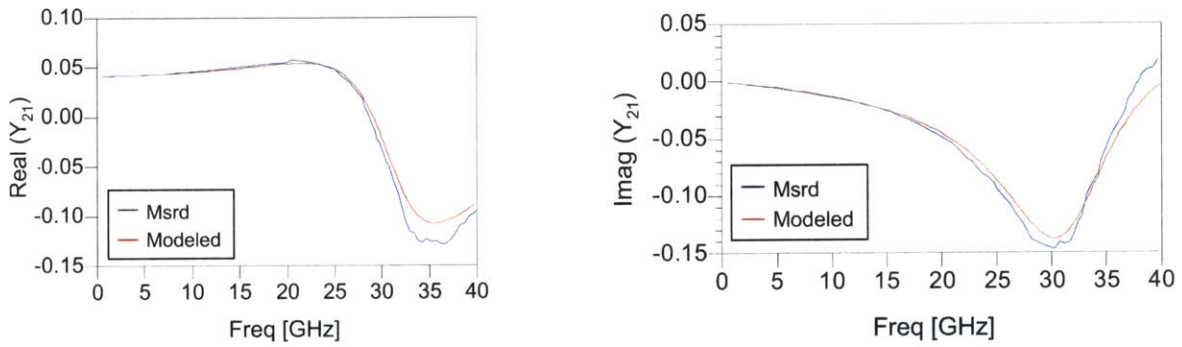
Fig. 3-36: Comparison between measured and modeled Y_{21} for the $L_{RD} = 0.9$ um device at $V_{DD} = 5$ V and $I_{D0} = 100$ mA/mm.
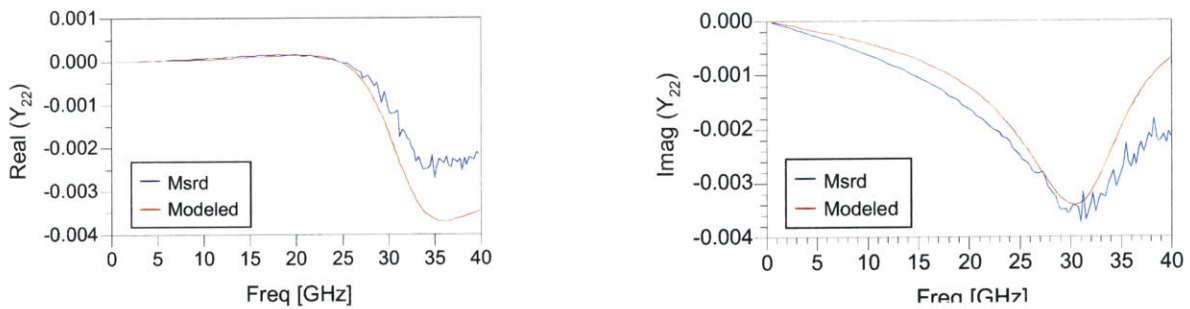
Fig. 3-37: Comparison between measured and modeled Y_{22} for the $L_{RD} = 0.9$ um device at $V_{DD} = 5$ V and $I_{D0} = 100$ mA/mm.

Figs. 3-38 to 3-41 shows the evolution of the small signal parameters L_S, L_D, L_G, R_S, R_D, R_G, C_{PG}, and C_{PD} versus L_{RD} at V_{DD} = 3, 5, and 7 V and I_D = 100 mA/mm. The extrinsic inductances and resistances are independent of bias, with the exception of R_D, which tends to increase with increasing L_{RD}.

The intrinsic small signal elements exhibit both positive and negative trends for microwave performance as a function of varying L_{RD}. C_{GD} decreases monotonically with increasing L_{RD}, which is beneficial to f_T (Fig. 3-42). Effects detrimental to microwave performance include the increase in C_{GS} with increasing L_{RD} (Fig. 3-42). The rise in C_{GS} seems to increase with the extension of the depletion region on the drain side with increasing L_{RD}, which will see in the next section [16]. Additionally, the increase in C_{GS} may also be attributed to the drain contact being effectively more isolated from the channel with increasing L_{RD}, therefore increasing the gate-channel coupling through the source [26]. We also observe that C_{DS} remains relatively constant (Fig. 3-43) and g_m decreases with increasing L_{RD}, which is accounted for in Section 5.4 (Fig. 3-44). For all devices, τ_{int} increases slightly with increasing L_{RD} (Fig. 3-44), which is also correlated with decreasing f_T and is also discussed in further detail in section 3.2.2. A favorable effect of increasing L_{RD} is the decrease in g_{ds} (Fig. 3-45).
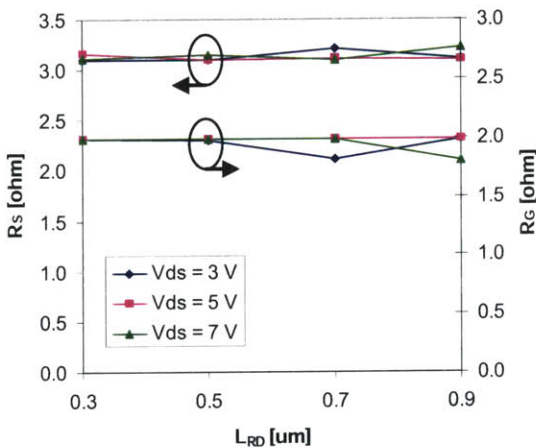
Fig. 3-38: Series resistance R_S and gate resistance R_G for devices with varying L_{RD} at V_{DD} = 3, 5, and 7 V and I_{D0} = 100 mA/mm.
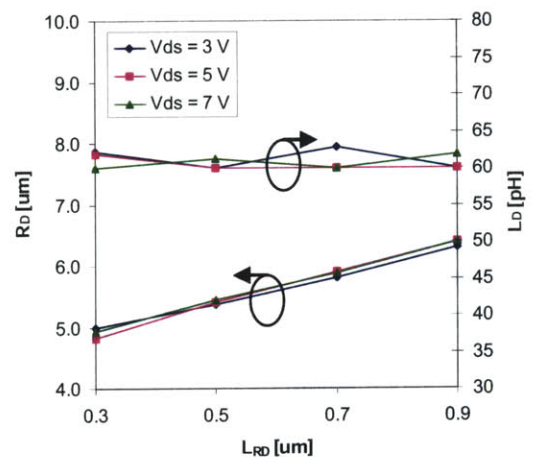
Fig. 3-39: Drain resistance R_G and inductance L_D for devices with varying L_{RD} at V_{DD} = 3, 5, and 7 V and I_{D0} = 100 mA/mm.
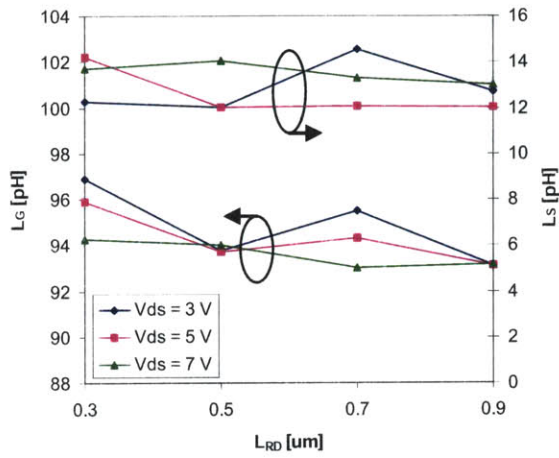
Fig. 3-40: Gate inductance L_G and source inductance L_S for devices with varying L_{RD} at V_{DD} = 3, 5, and 7 V and I_{D0} = 100 mA/mm.
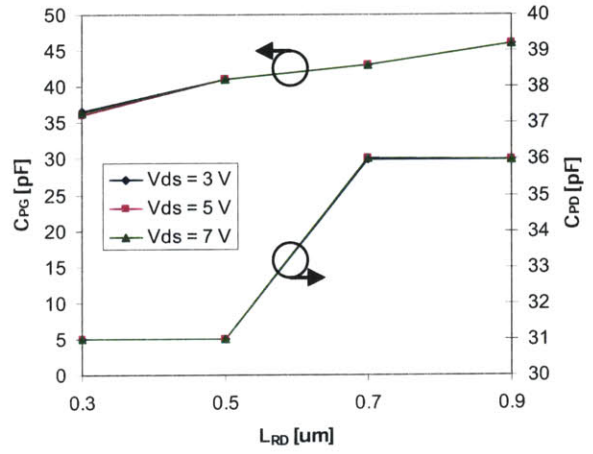
Fig. 3-41: Pad-to-gate parasitic capacitance C_{PG} for devices with varying L_{RD} at V_{DD} = 3, 5, and 7 V and I_{D0} = 100 mA/mm.
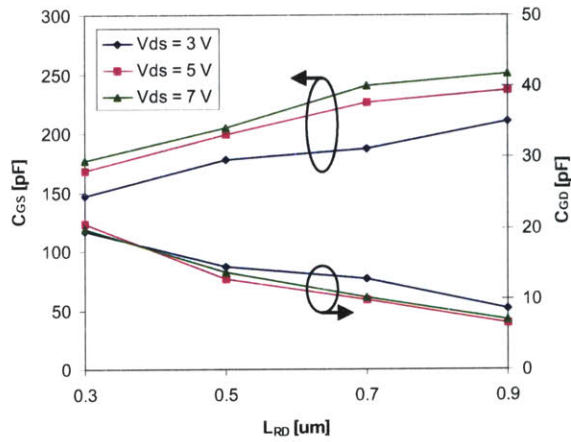
Fig. 3-42: Gate-to-source capacitance C_{GS} and gate-to-drain capacitance C_{GD} for devices with varying L_{RD} at V_{DD} = 3, 5, and 7 V and I_{D0} = 100 mA/mm.
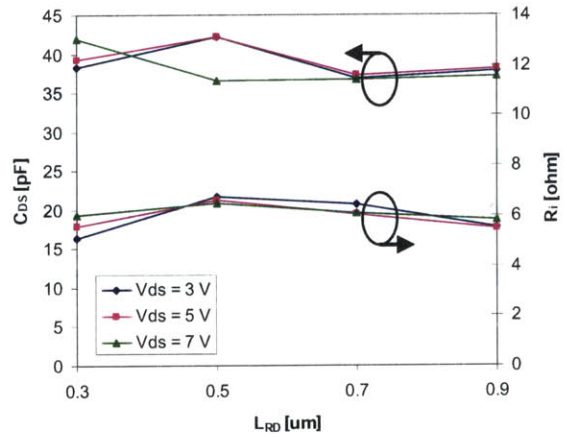
Fig. 3-43: Drain-to-source capacitance C_{DS} and gate-to-source resistance R_i for devices with varying L_{RD} at V_{DD} = 3, 5, and 7 V and I_{D0} = 100 mA/mm.
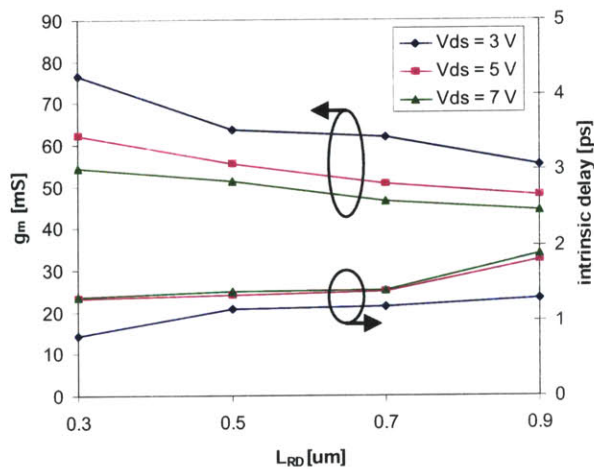
Fig. 3-44: Gate-to-drain capacitance C_{GD} and intrinsic delay τ_{int} for devices with varying L_{RD} at V_{DD} = 3, 5, and 7 V and I_{D0} = 100 mA/mm.
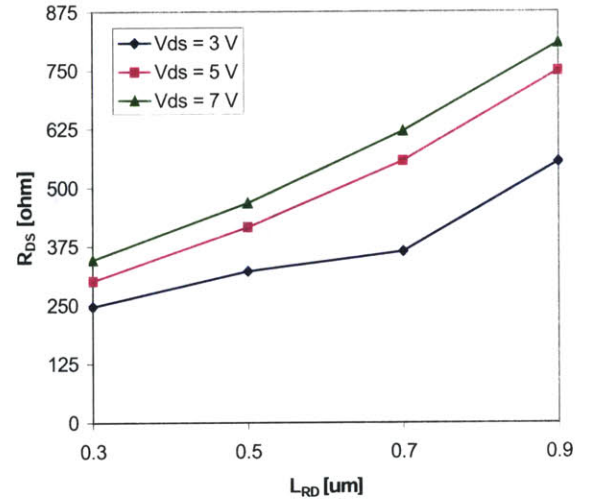
Fig. 3-45: Drain-to-source resistance R_{DS} for devices with varying L_{RD} at V_{DD} = 3, 5, and 7 V and I_{D0} = 100 mA/mm.

3.2.2 f_T

The short-circuit current-gain cut-off frequency f_T was extracted from de-embedded S-parameter measurements (Fig. 3-46). For all devices, f_T increases rapidly with increasing drain voltage when V_{DD} is below $V_{DS,SAT}$; however, as the devices begin to operate in the saturation region, f_T peaks and begins to decline as V_{DD} is increased. The longer L_{RD} is, the steeper the drop in f_T. For the L_{RD} = 0.3 um device, f_T remains relatively flat as V_{DD} increases to 7 V. On the other hand, the L_{RD} = 0.9 um device experiences a steep drop with increasing V_{DD}; f_T drops by nearly half from V_{DD} = 0.9 V to 7 V.

L_{RD} directly affects the behavior of f_T vs. V_{DD} because a longer L_{RD} translates to a longer depleted cap layer. This in turn can lead to a drastic degradation of f_T at high V_{DD} [27]. The L_{RD} = 0.3 um device exhibits behavior that is closely correlated to a PHEMT with a partially depleted cap, which is desirable for RF power operation. As L_{RD} increases to 0.5 um, the cap layer becomes increasingly depleted. When L_{RD} is increased further to 0.7 and 0.9 um, the effects of deep surface depletion are evident in the drop in peak f_T and steeper decline in the f_T characteristic with increasing V_{DD}.
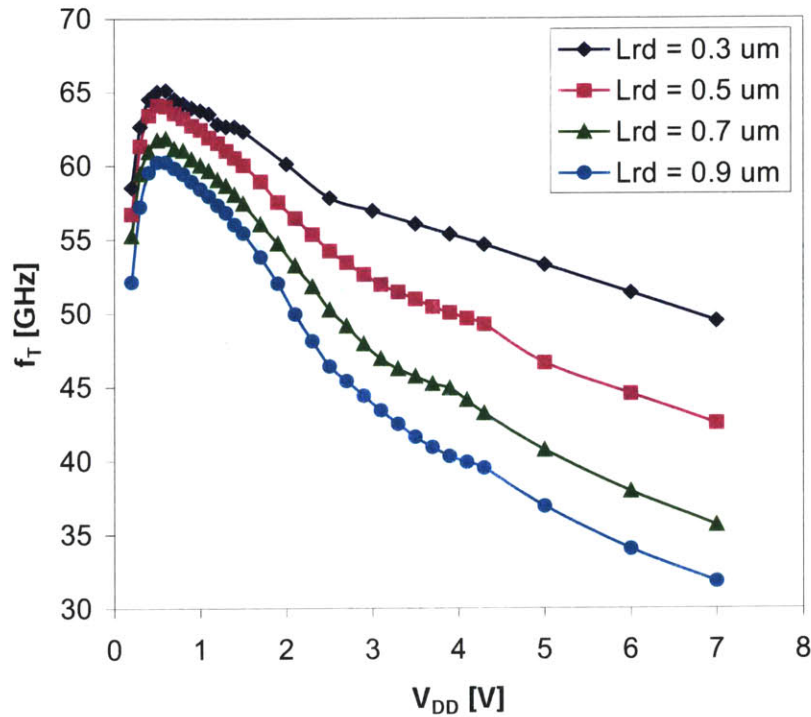
Fig. 3-46: f_T versus V_{DD} for devices with varying L_{RD} and I_{D0} = 100 mA/mm.

3.2.3 f_{max}

The maximum frequency of oscillation f_{max} was extracted from S-parameter measurements for devices with varying L_{RD} (Fig. 3-47). In general, across the range of V_{DD} measured, the smallest L_{RD} device has the smallest f_{max} while the largest L_{RD} device has the largest f_{max}. Unlike the large variation observed in the f_T measurements, the spread in frequency for all of the f_{max} measurements is relatively small at approximately 10 GHz. For all of the devices under study, it is remarkable that f_{max} stays relatively constant while f_T decreases sharply across V_{DD}. The reason for this behavior can be attributed to the fact that the g_m/g_{ds} ratio increases with increasing L_{RD}. Although g_m was shown to decrease with increasing L_{RD}, g_{ds} decreases at a faster rate and hence offsets the decrease in f_T at a given V_{DD} [28]. For instance, at V_{DD} = 5 V, the g_m/g_{ds} ratio nearly doubles from 20.2 to 37.9 when L_{RD} is increased from 0.3 to 0.9 um. The same trends in g_m/g_{ds} are also observed at V_{DD} = 3 and 7 V; hence, similar behavior in f_{max} is shown by the data obtained from the equivalent circuit models extracted at V_{DD} = 3 and 7 V in Section 3.2.1.

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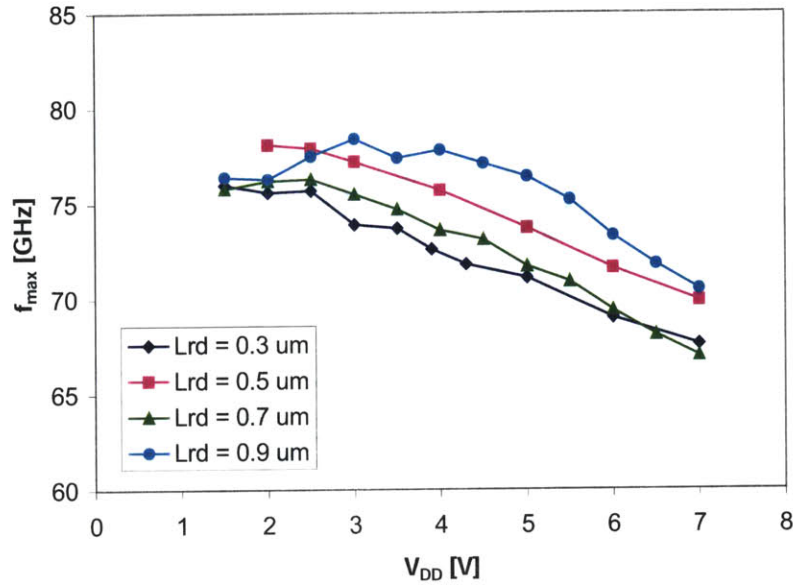
Fig. 3-47: f_{max} versus V_{DD} for devices with varying L_{RD} and I_{D0} = 100 mA/mm.

3.2.4 Delay Time Analysis

The total delay τ is extracted from the as-measured S-parameters and is increasing as a function of $1/I_D$ due to the presence of the parasitic delay τ_{par}, defined as $\tau - \tau_{int}$ (Fig. 3-48). To prevent τ_{par} from affecting the extrapolation of the drain delay $\tau_{tr,d}$, we must de-embed the extrinsic elements and pad parasitic capacitances to extract the intrinsic delay τ_{int}. From Fig. 3-48, τ_{int} only slightly increases with $1/I_D$, which indicates that it still contains the channel charging time τ_{cc} as predicted by Moll [21]. Using Moll's method of extrapolating τ_{int}, τ_{cc} is the source/drain charging time associated with the parasitic resistance and capacitance in the access region. For the devices under study, it is largely negligible compared to τ_{par}.

Fig. 3-49 shows the evolution of the τ_{int} with increasing V_{DS} for devices with varying L_{RD} and is the sum of $\tau_{tr,i}$ and $\tau_{tr,d}$. The minima of τ_{int} can be interpreted as $\tau_{tr,i}$, which represents the transit of electrons under the gate, and the difference between τ_{int} and $\tau_{tr,i}$ with increasing V_{DD} represents $\tau_{tr,d}$, which is associated with the extension of the depletion region on the drain side [29]. Since the gate length is 0.25 um, we expect that $\tau_{tr,i}$ is the same for all four devices. As V_{DS} increases,

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$\tau_{tr,d}$ increases for each device. In addition, $\tau_{tr,d}$ increases considerably as L_{RD} is increased with $\tau_{tr,d}$ of the L_{RD} = 0.9 um device approximately 1 ps longer than the L_{RD} = 0.3 um device at V_{DD} = 4 V.

The sharp increase in $\tau_{tr,d}$ suggests that the depletion region is extending farther toward the drain with increasing L_{RD}, which is the most significant finding of the delay time analysis. Due to traps in the gate-drain region (see Section 5.4), the depletion region cannot respond instantaneously to microwave frequencies. The additional delay shown by the longer L_{RD} devices may explain why P_{OUT} degrades more rapidly with these devices at higher frequencies. Additionally, this behavior will also translate to a higher drain resistance and $V_{DS,SAT}$ under RF operation [25].
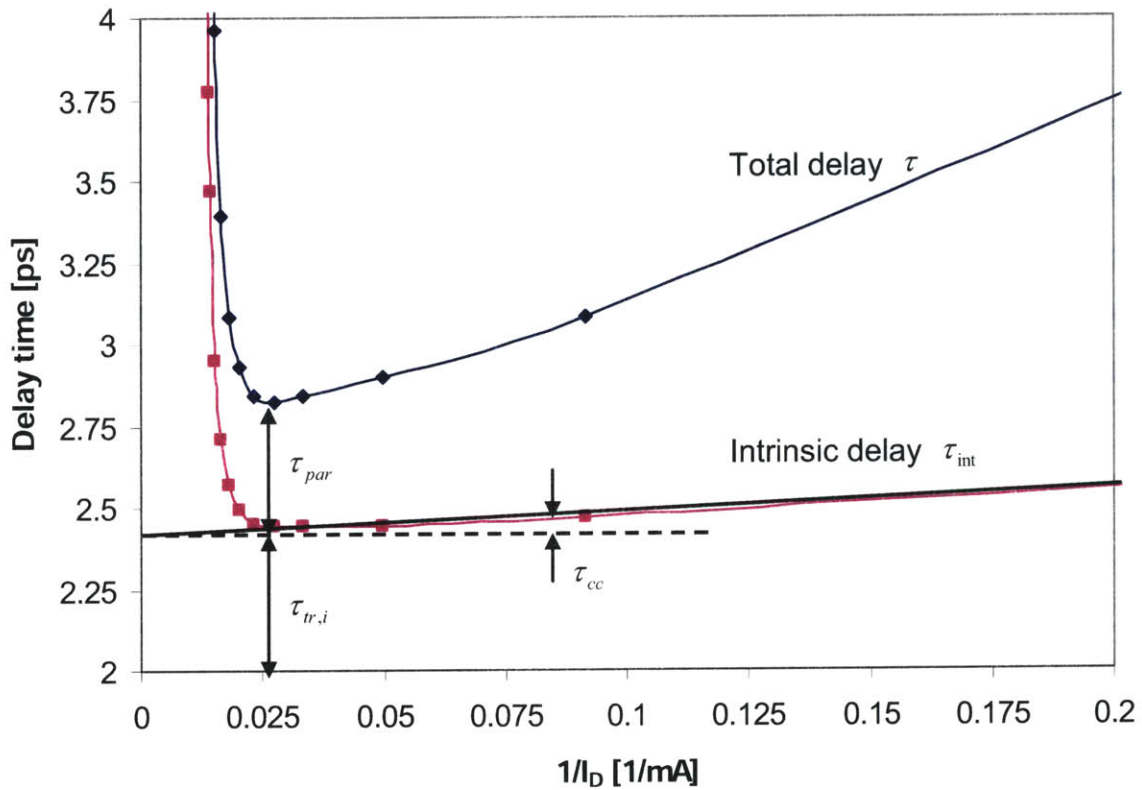
Fig. 3-48: Total and intrinsic delay versus $1/I_D$ for a L_{RD} = 0.5 um device. To obtain the smallest τ_{int}, V_{GS} was chosen to be –0.2 V.

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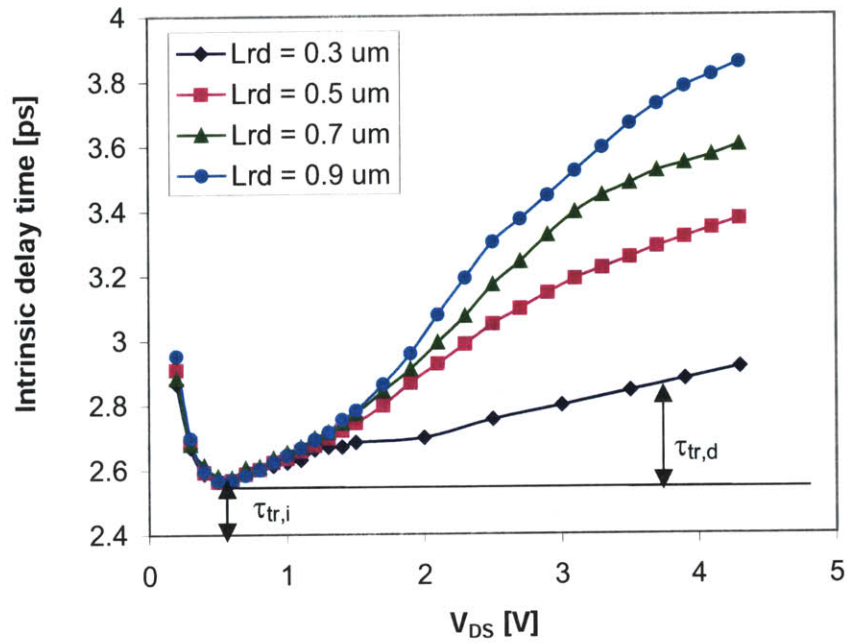
Fig. 3-49: Intrinsic delay time τ_{int} versus V_{DS} for a L_{RD} = 0.5 um device with gate length of 0.25 um. To obtain the smallest τ_{int}, V_{GS} was chosen to be −0.2 V.

A comparison of the small signal equivalent circuits extracted from S-parameters revealed key differences between the intrinsic elements with increasing L_{RD}: an increase in C_{GS}, τ_{int}, and R_{DS} and a decrease in C_{GD} and g_m. The decrease in g_m and increase in C_{GS} directly translate to a decrease in f_T with increasing L_{RD}. However, an increasing g_m/g_{ds} ratio with L_{RD} causes f_{max} to remain relatively constant across L_{RD}.

3.3 Conclusions

At 8 GHz, the L_{RD} = 0.7 um device delivered the highest $P_{OUT,3-dB}$ at V_{DD} = 9 V while at 12 and 16 GHz, the L_{RD} = 0.5 um device delivered the highest $P_{OUT,3-dB}$ at V_{DD} = 8 V. From the verification measurements, it appears that the longer L_{RD} (0.7, 0.9 um) devices are the most robust out of the group at 8 GHz. However, at 12 and 16 GHz, the longer L_{RD} (0.7, 0.9 um) devices are much less robust than the shorter L_{RD} (0.3, 0.5 um) devices during large signal operation and are susceptible to catastrophic burnout. In Chapter 5, we will explore the role of oscillations in the unexpected catastrophic burnout of these long L_{RD} devices at moderate V_{DD}. As L_{RD} increases, we have also seen that $P_{OUT,3-dB}$ decreases at a steeper rate with frequency. We find that this is due to the degradation in high-frequency characteristics that arises from an extension of the drain depletion region with increasing L_{RD} and that they may be frequency dependent mechanisms associated with it.

A comparison of the small signal equivalent circuits extracted from S-parameters revealed key differences between the intrinsic elements with increasing L_{RD}: an increase in C_{GS}, τ_{int}, and R_{DS} and a decrease in C_{GD} and g_m. The decrease in g_m and increase in C_{GS} directly translate to a decrease in f_T with increasing L_{RD}. However, an increasing g_m/g_{ds} ratio with L_{RD} causes f_{max} to remain relatively constant across L_{RD}.

Chapter 4: Impact of L_{RD} on Device Stability

We have investigated the stability of the different L_{RD} devices under DC and RF operation. The L_{RD} = 0.7 and 0.9 um devices have exhibited anomalous behavior relating to stability that have appeared in the form of NDR, positive $|S_{22}|$, negative g_{ds}, output spectra under DC conditions, and large unstable regions shown by the stability circles. Since the stability has a profound impact on the large signal characteristics, it is important to understand the different ways oscillations manifest themselves and the conditions under which they occur.

4.1 DC Measurements

We have discovered anomalous behavior in the DC characteristics of the devices that is exacerbated by increasing L_{RD} and is most likely due to device instability. This behavior may be responsible for the premature burnout of devices with L_{RD} = 0.7 and 0.9 um that was found in Chapter 3.

4.1.1 NDR in the Output Characteristics

A comparison between the output characteristics of the different L_{RD} devices reveals dramatic differences in the forward biased gate region as a function of L_{RD} (Fig. 4-1). In general, for $V_{DS} >$ 1.5 V and $V_{GS} > 0$ V, a prominent negative differential resistance region (NDR) is seen in the output characteristics of the devices with L_{RD} = 0.7 and 0.9 um. To ensure that the NDR originates from the device and not the experimental setup, the output characteristics were measured in a 50 Ω environment to prevent circuit instability.
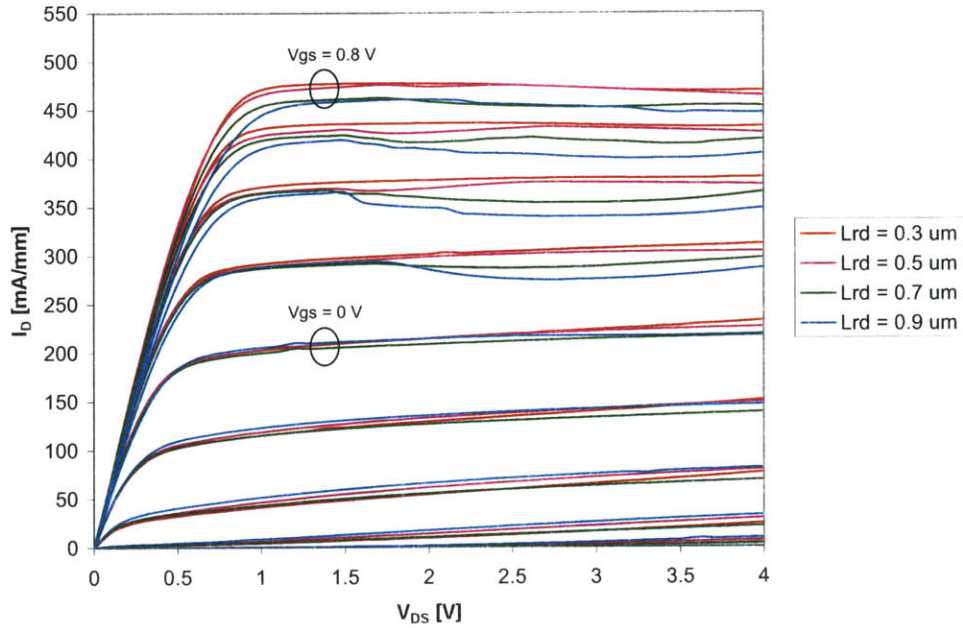
Fig. 4-1: Output characteristics of different L_{RD} devices. V_{GS} = -0.8 to 0.8 V in 0.2 V increments.

The NDR appears to be a function of both V_{GS} and V_{DS}, which seem to indicate that it could be potentially due to real space transfer (RST) of carriers from the InGaAs channel to the AlGaAs donor layer as a result of thermionic emission at high drain fields and thermally assisted tunneling at high gate fields followed by electron extraction by the gate [30]. Phenomena concurrent with real space transfer have been reported to be excess gate current due to hot electrons resulting from impact ionization [31], gate-controlled NDR in the drain current [9], and high frequency, high-field instability [32]. However, for the longest L_{RD} device, a decrease in I_D is not simultaneously accompanied by an increase in I_G, the hallmark of RST (Fig. 4-2). Other studies reporting RST have shown that as V_{DS} is lowered, a higher V_{GS} is required for the onset of NDR and beyond a high enough V_{GS}, no NDR is observed [33, 34]. These trends in NDR were also observed in the long L_{RD} devices.

The appearance of NDR in the L_{RD} = 0.7 and 0.9 um devices is significant because it could potentially be related to the catastrophic burnout of these devices at high V_{DS} and high frequency. Since the load line may pass through the NDR region, anomalous behavior in this region will affect the large signal characteristics. This warrants a thorough investigation into the anomalies
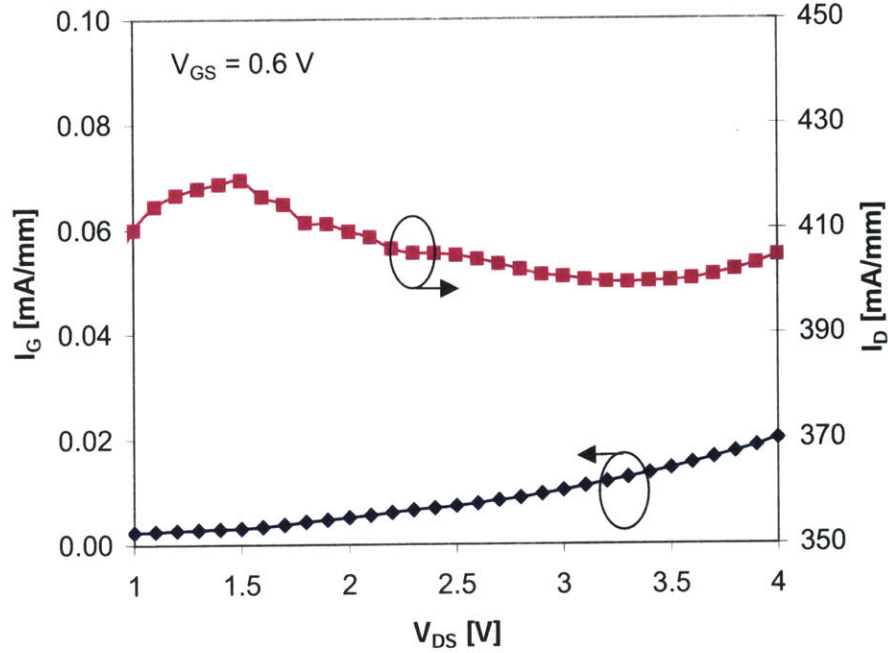
Fig. 4-2: I_G and I_D vs. V_{DS} for the L_{RD} = 0.9 um device at V_{GS} = 0.6 V.

that have been observed in other aspects of the DC and RF characteristics of the long L_{RD} devices. For the rest of this chapter, we explore anomalous behavior in the characteristics of the long L_{RD} devices that might be associated with the NDR observed in the output characteristics and the appearance of oscillations.

4.1.2 Impact Ionization in the Transfer Characteristics

At a given bias voltage, as L_{RD} is reduced, the peak electric field becomes larger in the drain-gate region. When the electric field in a semiconductor is increased above a certain value, the carriers gain sufficient energy to generate electron-hole pairs by impact ionization. While the electrons are accelerated toward the drain by the high drain-gate field, the generated holes flowing toward the source may surmount the valence band discontinuity and form a negative gate current as they are collected by the gate electrode. Since the maximum V_{DG} possible for a device increases with L_{RD}, we expect that the impact ionization rate would decrease with increasing L_{RD}.

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To explore the role of impact ionization, we have measured the transfer characteristics to compare the behavior of Al gate devices with different L_{RD} at several values of V_{DS} (Figs. 4-3 to 4-5). The bell-shaped I_G-V_{GS} curve is a classic characteristic of impact ionization. Impact ionization appears to decrease as L_{RD} is increased from 0.3 to 0.5 um but then begins to increase as L_{RD} is increased from 0.5 to 0.7 and 0.9 um at V_{DS} = 6 V (Fig. 4-3). However, impact ionization appears to be slightly less for the L_{RD} = 0.7 um than the L_{RD} = 0.5 um device when V_{DS} is
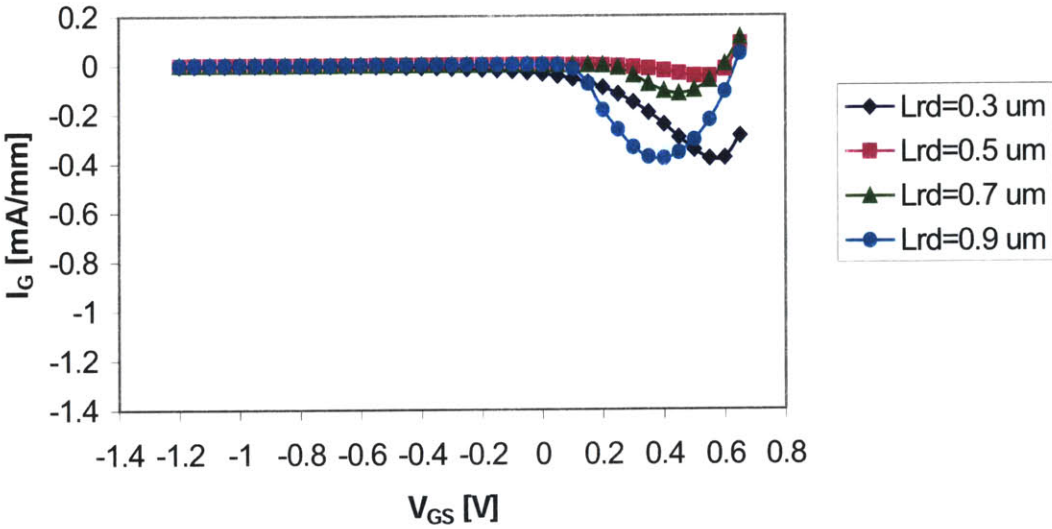
Fig. 4-3: I_G vs. V_{GS} at V_{DS} = 6 V for devices with different L_{RD}.
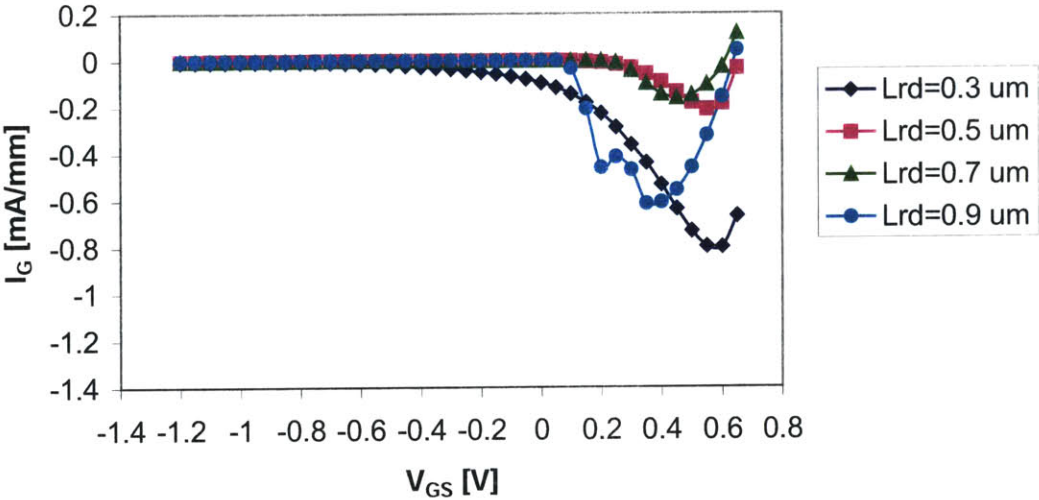
Fig. 4-4. I_G vs. V_{GS} at V_{DS} = 6.5 V for devices with different L_{RD}.

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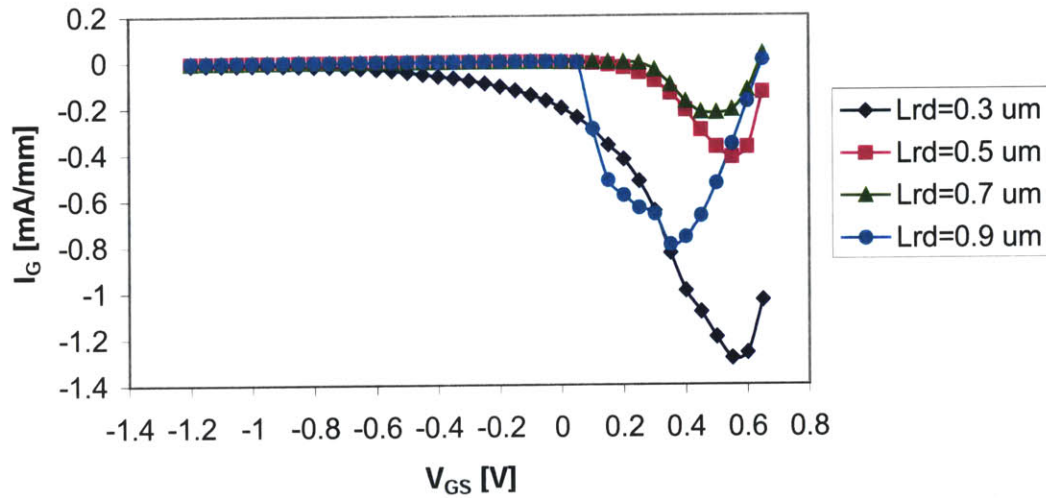
Fig. 4-5. I_G vs. V_{GS} at $V_{DS} = 7$ V for devices with different L_{RD}.

increased to 6.5 V (Fig. 4-4). At high enough V_{DS}, the impact ionization is clearly less for the L_{RD} = 0.7 um device than the L_{RD} = 0.5 um device, although the L_{RD} = 0.9 um device consistently displays a higher level of impact ionization regardless of V_{DS} (Fig. 4-5). This anomalous increase in impact ionization is most likely attributed to oscillations that appear in the NDR region of the output characteristics. With the rapid increase in I_G with V_{GS}, it is unlikely that the increase in impact ionization is a true phenomenon for the longer L_{RD} devices.

4.2 P_{OUT} under DC Conditions

If oscillations exist, RF power will appear at the output of the device in the absence of RF drive. To examine the occurrence of oscillations in the devices under study, we have used a power meter to monitor the amount of reflected power at the output of the devices under DC conditions. In an ideal PHEMT, when V_{DS} is increased to approximately $V_{DS,SAT}$, P_{OUT} increases from the noise floor and plateaus off to a constant level depending on the V_{GS} applied. This constant level represents the noise generated in the channel as a result of conduction. Under normal conditions without the presence of oscillations, the output power should remain constant when the device is operated in the saturation regime.

Normal behavior is shown for the L_{RD} = 0.3 um device in the NDR region (Fig. 4-6). However, as L_{RD} is increased, we begin to observe the increasing presence of anomalous behavior as soon as the device enters saturation. For the L_{RD} = 0.5 um device, P_{OUT} exhibits spikes when V_{GS} = 0 and a slight increase when V_{GS} = 0.4 V and V_{DS} is between 2-5 V (Fig. 4-7). As L_{RD} is increased further to 0.7 and 0.9 um, the degree of reflected power becomes very high. When V_{GS} is between 0.2 and 1.0 V, the L_{RD} = 0.7 um device outputs power as high as –22 dBm (Fig. 4-8). The L_{RD} = 0.9 um device is capable of producing even higher output power for all values of V_{GS}; at V_{DS} = 1.7 V, V_{GS} = 0.4 V, the output power was –10 dBm (Fig. 4-9).
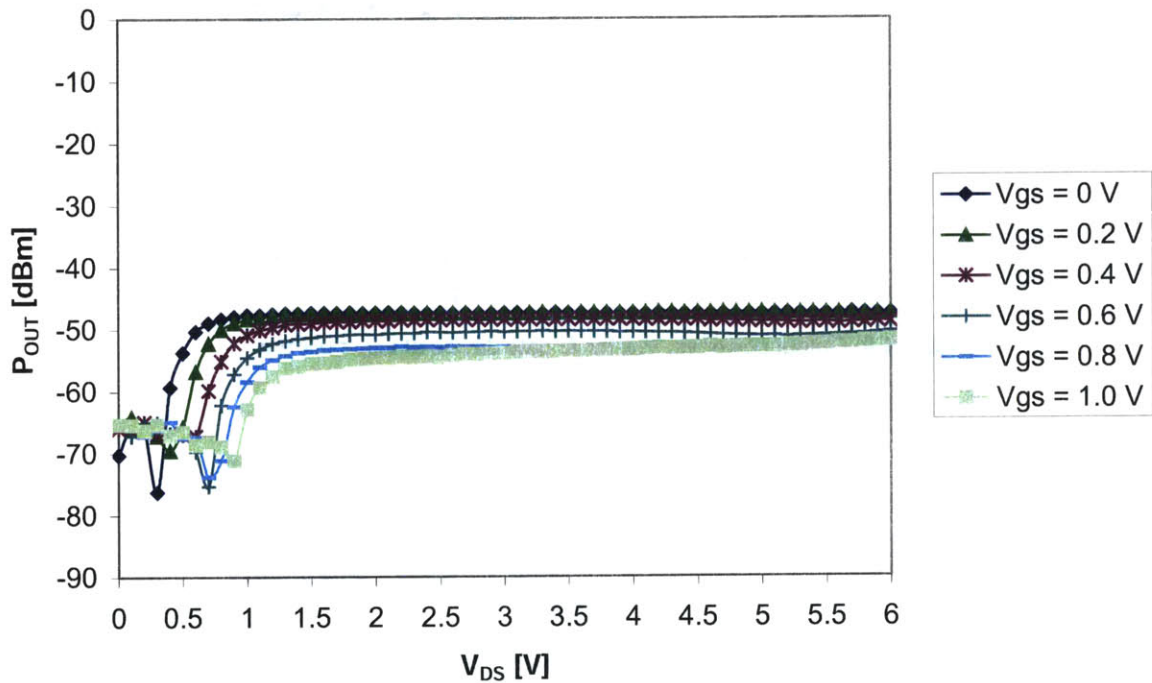
Figure 4-6: Output power vs. V_{DS} for Al gate device with L_{RD} = 0. 3 um
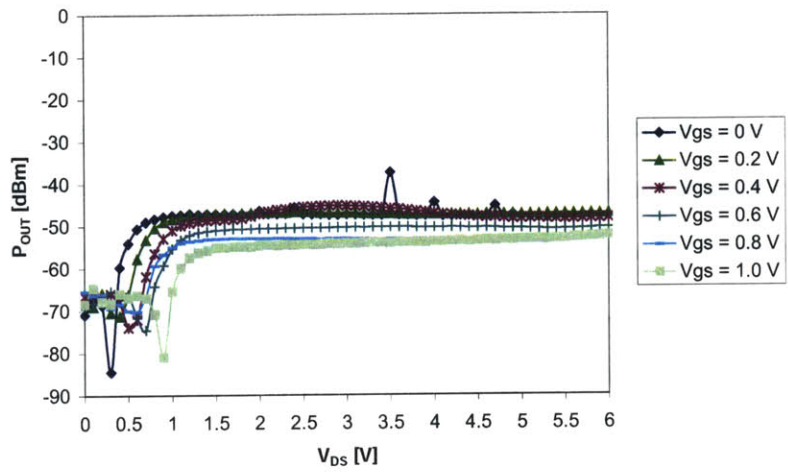
Figure 4-7: Output power vs. V_{DS} for Al gate device at L_{RD} = 0.5 um
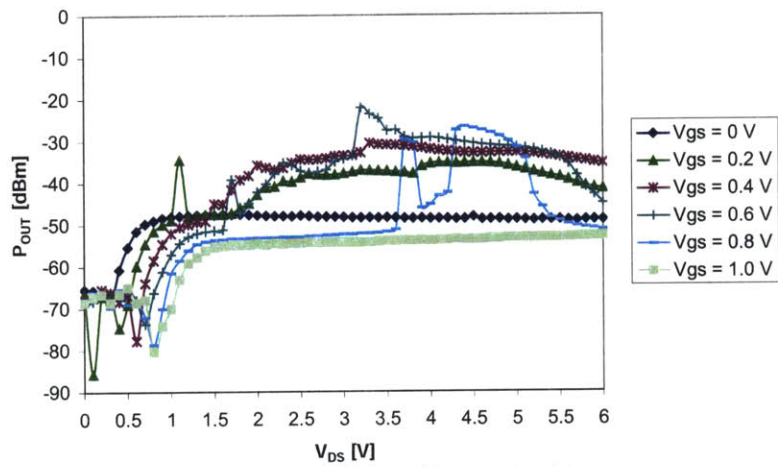
Figure 4-8: Output power vs. V_{DS} for Al gate device at L_{RD} = 0.7 um
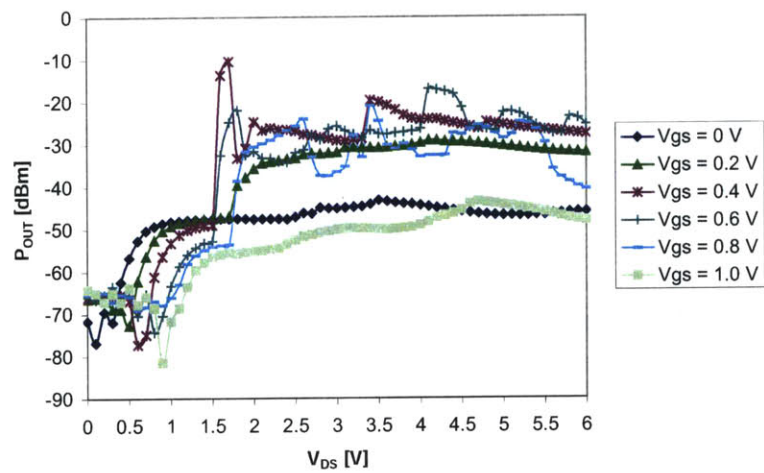
Figure 4-9: Output power vs. V_{DS} for Al gate device at L_{RD} = 0.9 um

We have mapped out the presence of anomalously high reflected power on the output characteristics for the L_{RD} = 0.7 and 0.9 um devices (Figs. 4-10 and 4-11). For both devices, they occur primarily within the NDR region.
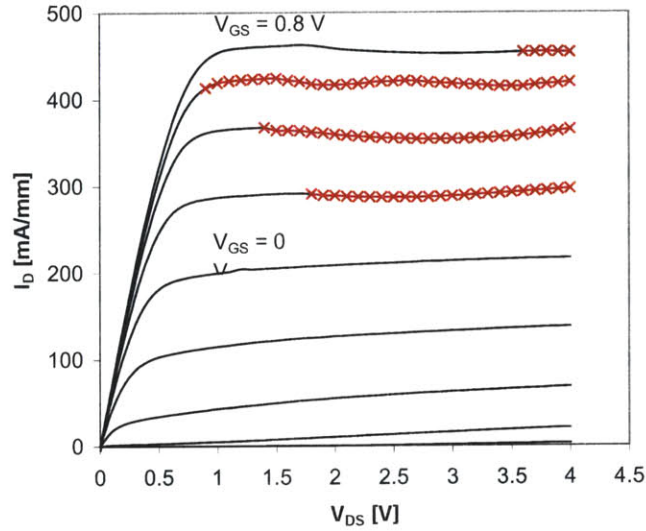
Figure 4-10: Presence of reflected power (red X's) mapped against the output characteristics of the L_{RD} = 0.7 um device. V_{GS} is from –0.8 to 0.8 V stepped in 0.2 V increments.
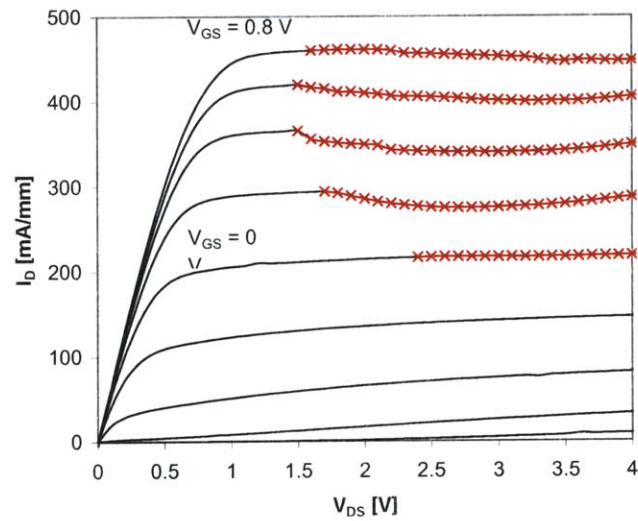
Figure 4-11: Presence of reflected power (red X's) mapped against the output characteristics of the L_{RD} = 0.9 um device. V_{GS} is from –0.8 to 0.8 V stepped in 0.2 V increments.

4.3 Spectrum Analyzer

In addition to the NDR in the DC I-V curves, oscillations have been observed at microwave frequencies when V_{GS} is forward biased. To analyze the frequency dependence of the spurious signals, we attached an Agilent 8595E spectrum analyzer to the RF terminal of the output bias tee and measured the output spectra up to 6.5 GHz. For maximum visibility of the spectra, the resolution bandwidth, which affects how closely a small signal can be seen in the presence of a large one, was 3 MHz and the video bandwidth, which determines the stability of the signal, was 1 MHz. If no oscillations are present, P_{OUT} should be at the noise floor (approximately -60 dBm) throughout the entire frequency scan.

For all four devices, the negatively biased gate region did not exhibit oscillations. The forward biased gate region, particularly within the NDR region for the longer L_{RD} devices, revealed different behavior among the different L_{RD} devices. Aside from the spurious signal at 0 GHz that is present in all of the measurements due to the instrumental settings, the shorter L_{RD} devices (0.3, 0.5 um) did not exhibit any anomalous output spectra (Fig. 4-12).


```
  10:54:25 AUG 27, 2004
 /gr
 REF  .0 dBm          AT 10 dB
 PEAK
 LOG
 10
 dB/
       RES BW
       1.0 MHz


 WA SB
 SC FC
  CORR


 CENTER 3.250 GHz              SPAN 6.500 GHz
   #RES BW 1.0 MHz    VBW 1 MHz    SWP 130 msec      RL
```
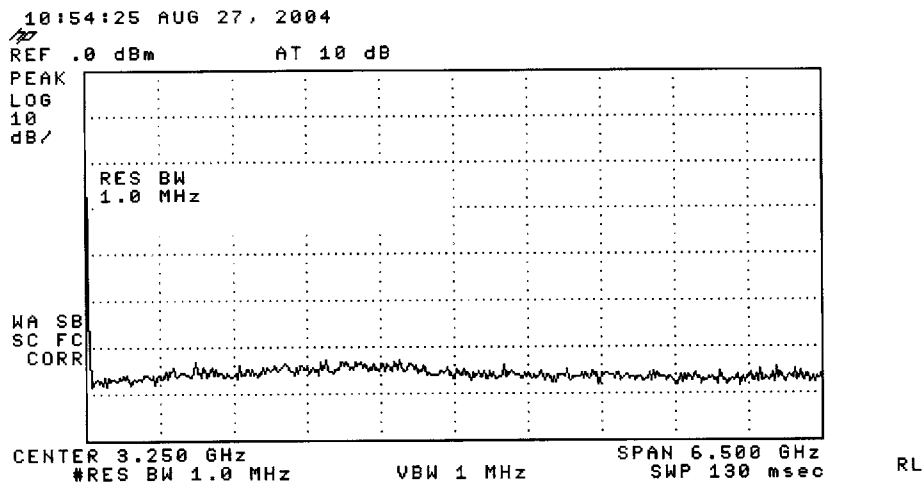
Fig. 4-12: Snapshot of the spectrum analyzer display for the L_{RD} = 0.5 um device at V_{DS} = 4 V and V_{GS} = 0.6 V.

Output spectra were examined outside and within the NDR region for the longer L_{RD} devices (0.7, 0.9 um). For the L_{RD} = 0.7 um device, no anomalous output spectra were observed at forward biased gate voltages; there was no difference between the spectral output within and outside the NDR region (Fig. 4-13). However, the L_{RD} = 0.9 um device burst into oscillations as soon as it entered the saturation region, with prominent spurious signals clearly shown at 3.9 and 4.4 GHz (Fig. 4-14). In fact, for all values of V_{GS}, spurious signals were consistently present at approximately 0.5, 3.9, and 4.4 GHz.
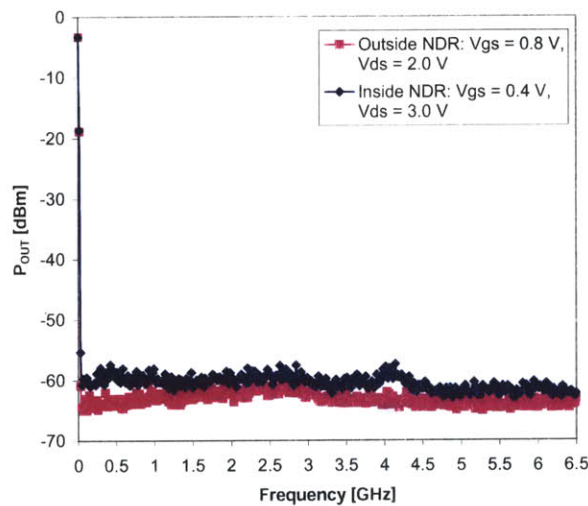
Fig. 4-13: Output spectra of the L_{RD} = 0.7 um device within the NDR region (V_{DS} = 2.0 V, V_{GS} = 0.8 V) and outside the NDR region (V_{DS} = 4.0 V, V_{GS} = 0.4 V).
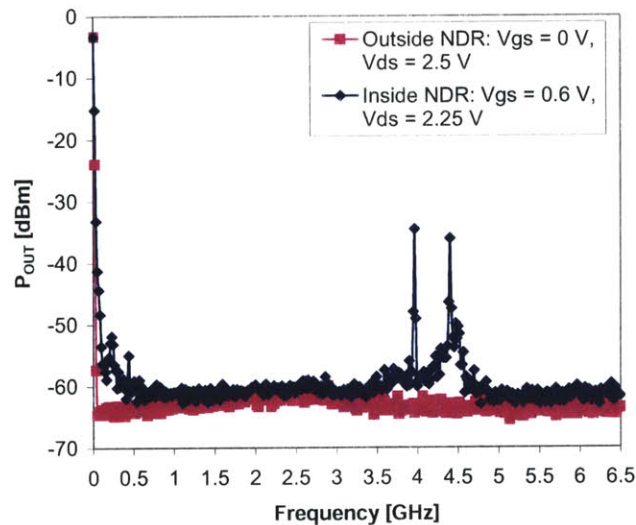
Fig. 4-14: Output spectra of the L_{RD} = 0.9 um device within the NDR region (V_{DS} = 2.5 V, V_{GS} = 0 V) and outside the NDR region (V_{DS} = 2.25 V, V_{GS} = 0.6 V).

The frequencies at which oscillations appear may give a clue to their origin. For the $L_{RD} = 0.9$ um device, Figs. 4-15 to 4-18 track the difference between the output power of the spurious signal and the noise floor at a constant value of V_{GS}. No spurious signals were seen at $V_{GS} = 0$ V. When $V_{GS} = 0.2$ V, only three spurious signals were observed of relatively slight but varying magnitude depending on V_{DS} (Fig. 4-15). However, when V_{GS} is increased to 0.4 V (Fig. 4-16) and 0.6 V (Fig. 4-17), the output spectra contains many more signals at different frequencies. Depending on V_{DS}, the magnitudes of the oscillations at various frequencies vary in magnitude. When $V_{GS} = 0.8$ V, the presence of spurious signals drops dramatically but gradually increases at V_{DS} approaches 3.75 V (Fig. 4-18).
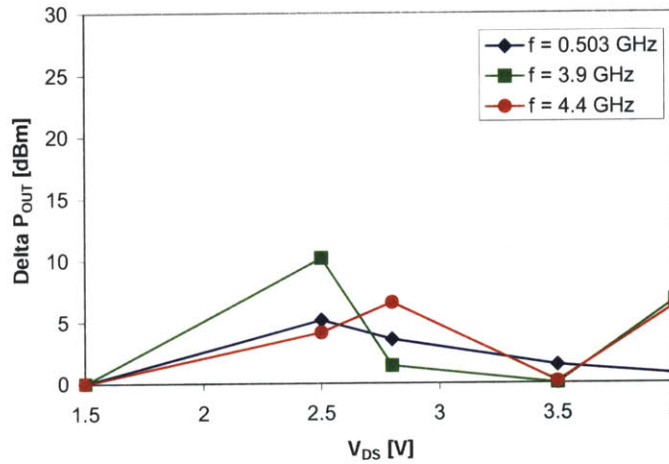
Fig. 4-15: Difference between P_{OUT} and noise floor for the $L_{RD} = 0.9$ um device at $V_{GS} = 0.2$ V
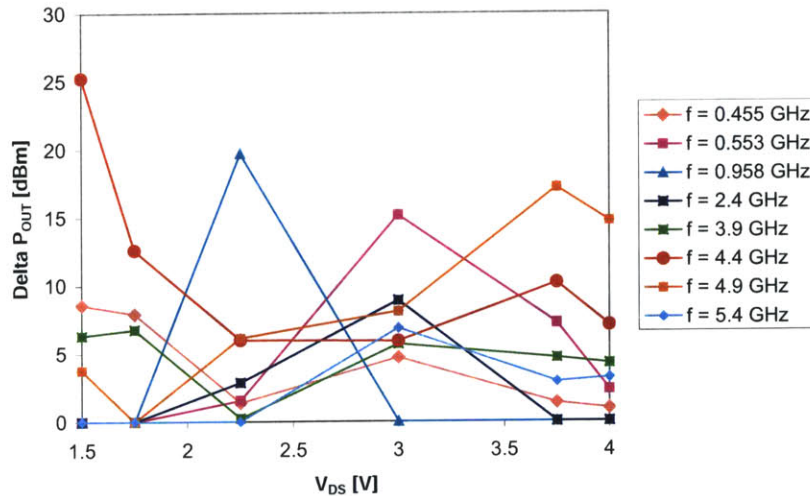
Fig. 4-16: Difference between P_{OUT} and noise floor for the $L_{RD} = 0.9$ um device at $V_{GS} = 0.4$ V

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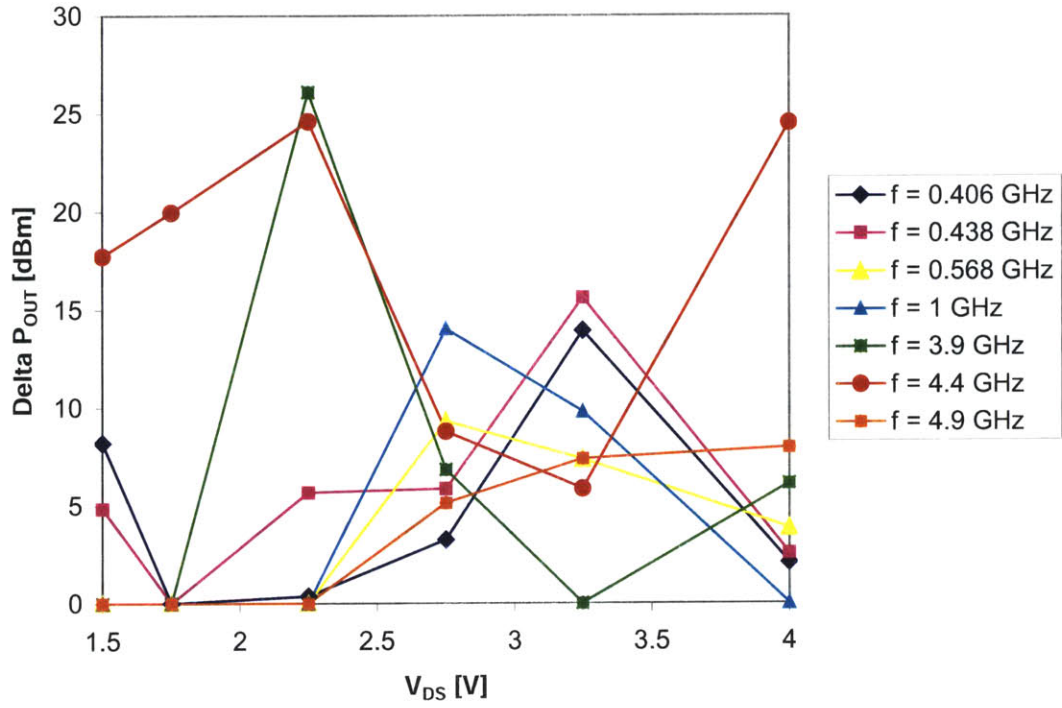
Fig. 4-17: Difference between P_{OUT} and noise floor for the L_{RD} = 0.9 um device at V_{GS} = 0.6 V
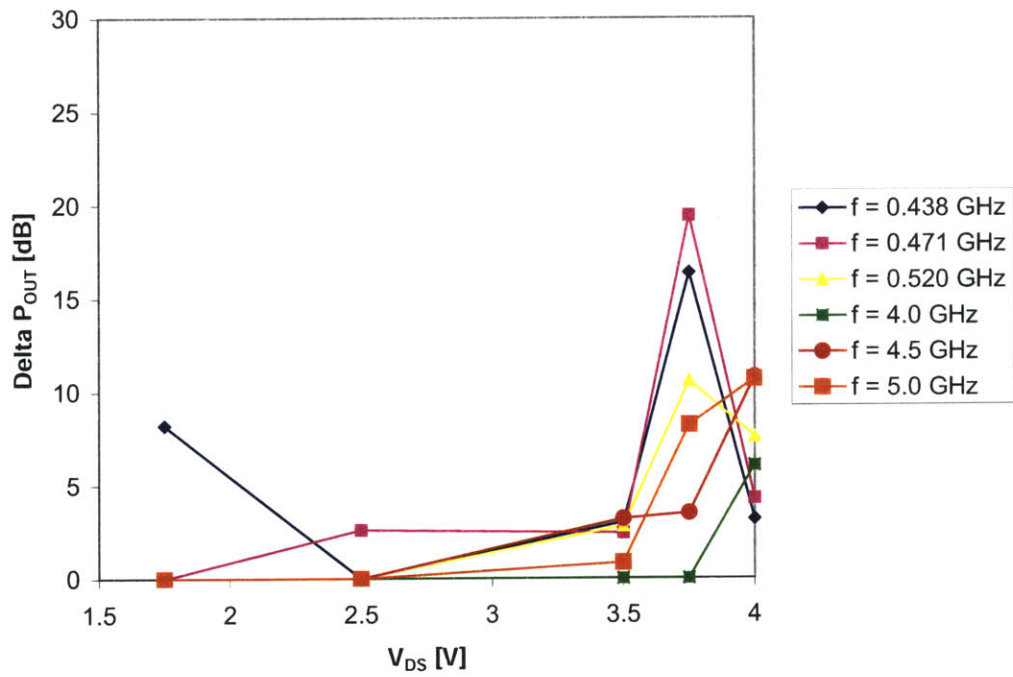
Fig. 4-18: Difference between P_{OUT} and noise floor for L_{RD} = 0.9 um device at V_{GS} = 0.8 V

It is possible that the oscillations may be due to the Gunn effect, which has been observed in Gunn diodes and some GaAs MESFETs with long drift regions [35]. However, the appearance of spurious signals at many frequencies indicates that this may not be the case. Gunn domains are typically characterized by a constant transit time that is determined by the geometry of the high field region and velocity of the domain and does not vary much with V_{DS} [36]. In addition, we can rule out the possibility of the kink effect as the source of NDR because it is related to trapping and plays no role at microwave frequencies [37].

To summarize the results of our spectral analysis, we have mapped our findings at each measured bias point against the output characteristics of the L_{RD} = 0.9 um device, the only device under study to exhibit such behavior (Fig. 4-19). Multiple spectra at the output of the device were observed frequently throughout the NDR region and lend significant evidence to the existence of oscillations.
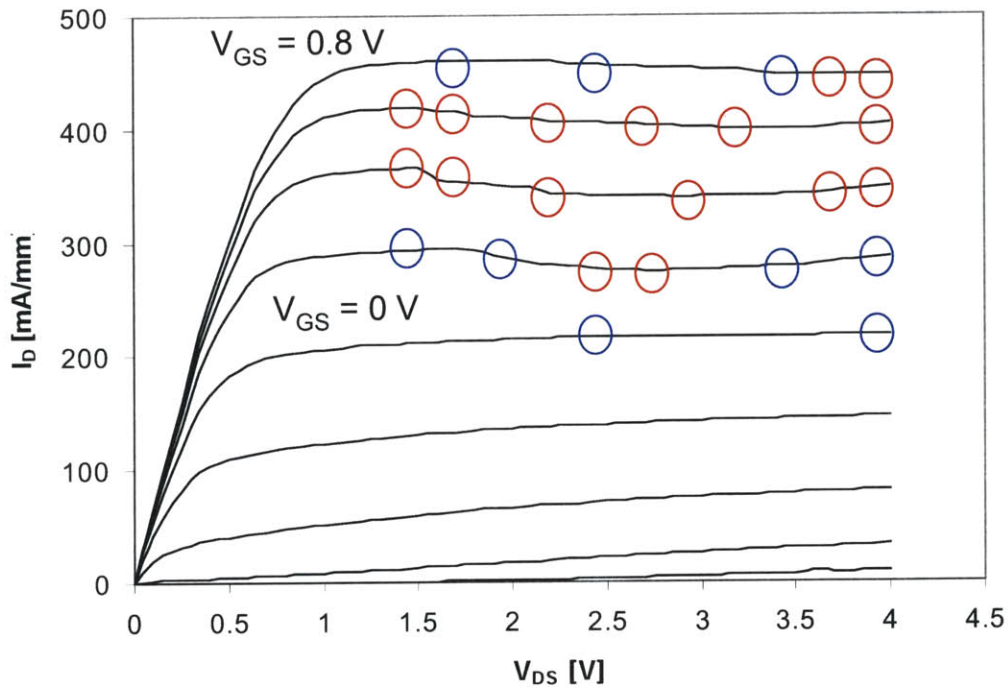
Fig. 4-19: Summary of the occurrence of output spectra in the forward biased gate region of the L_{RD} = 0.9 um device. V_{GS} is from −0.8 to 0.8 V in 0.2 V increments.

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4.4 S-parameter Analysis

The S-parameters of the L_{RD} = 0.7 and 0.9 um devices were measured in the NDR region from 0.05 to 40 GHz. The S_{22} of a two-port PHEMT, with the gate defined as the first port and the drain defined as the second port, represents the ratio between the reflected and incident power at the drain with the gate terminated at 50 Ω. In a two port network, oscillations are possible when either the input or output port present a negative resistance. This situation occurs for a unilateral device (defined as a transistor with S_{12} equal to zero) when $|S_{11}| > 1$ or $|S_{22}| > 1$. When S_{22} is greater than unity, an amplified RF signal is delivered to the drain.

The L_{RD} = 0.7 um device exhibited $|S_{22}| > 1$ when V_{DS} = 2 V and V_{GS} = 0.4 V (Fig. 4-20). The L_{RD} = 0.9 um device also experienced $|S_{22}| > 1$ under certain bias conditions and a higher degree of instability; when V_{DS} ranges from 2 to 3.25 V, $|S_{22}|$ is larger than unity depending on V_{GS} (Fig. 4-21). However, when V_{DS} is lower than 2 V or greater than 3.25 V, $|S_{22}|$ is always less than one.
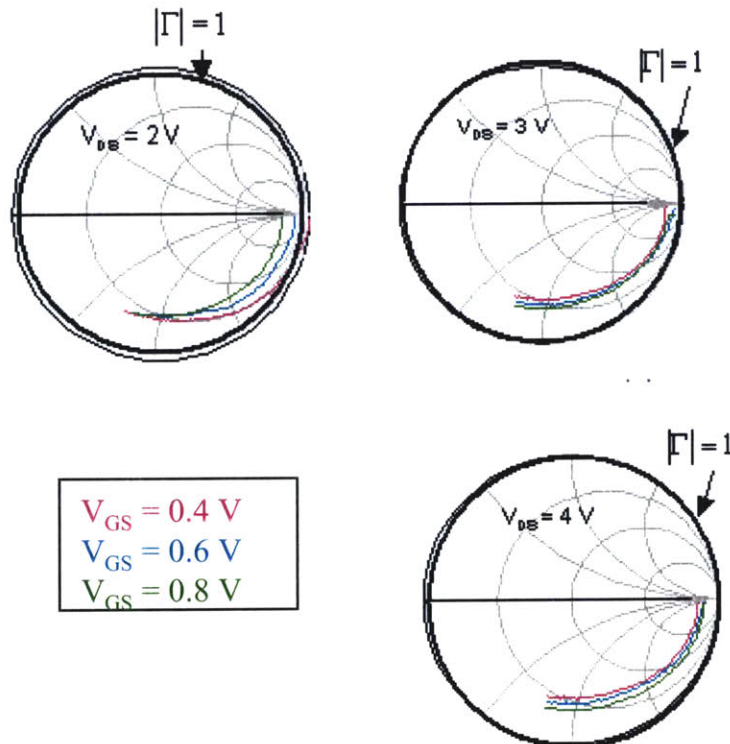
Fig. 4-20: S_{22} of the L_{RD} = 0.7 um device at different bias points.
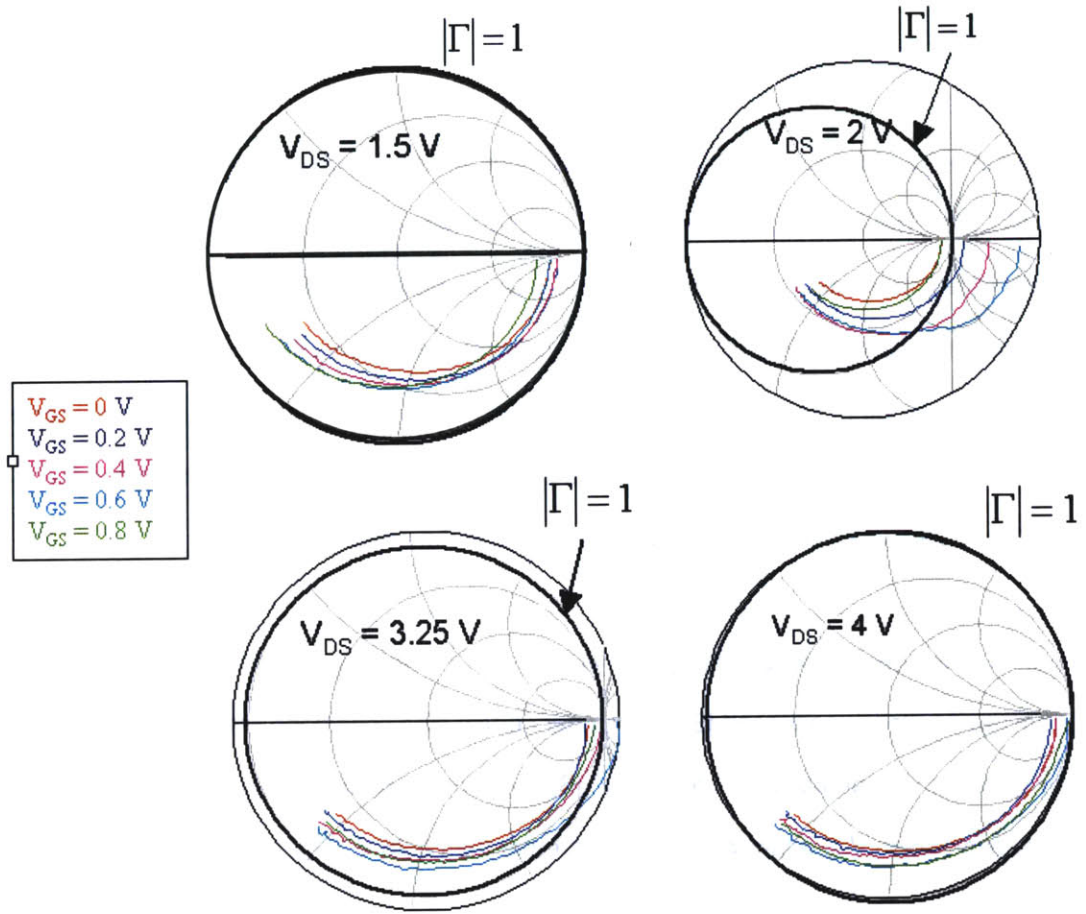
Fig. 4-21: S_{22} of the L_{RD} = 0.9 um device at different bias points.

To obtain a better idea of the behavior of the NDR versus bias, we have plotted the magnitude of S_{22} against V_{DS} for the L_{RD} = 0.9 um device at 6 GHz (Fig. 4-22). The figure indicates that $|S_{22}|$ peaks at V_{DS} = 2 V and decreases as V_{DS} is increased to 4 V. When V_{GS} = 0.6 V, the device experiences its highest degree of instability. As $|S_{22}|$ becomes higher, the data points become more scattered as the instability increases. Despite the frequent occurrence of $|S_{22}| > 1$, $|S_{11}|$ did not change much with bias within the NDR region, indicating that the instability exists within the output (or drain) circuit. These problems with stability may have to be accommodated or prevented for short gate length, high power PHEMTs [33].
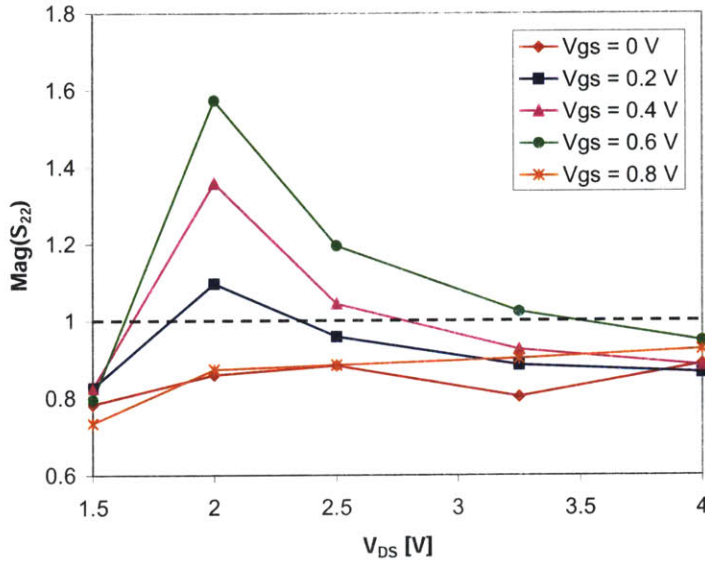
Fig. 4-22: $|S_{22}|$ of the L_{RD} = 0.9 um device at 6 GHz as a function of V_{DS}.

We have summarized our findings and compared them to their respective locations in the positive V_{GS} region of the output characteristics (Figs. 4-23 and 4-24). In the NDR region, the L_{RD} = 0.9 um device exhibits many more occurrences of $|S_{22}|$ > 1 than the L_{RD} = 0.7 um device. Since the NDR region encompasses a much larger region of the output characteristics for the L_{RD} = 0.9 um device than the L_{RD} = 0.7 um device, these observations make sense.
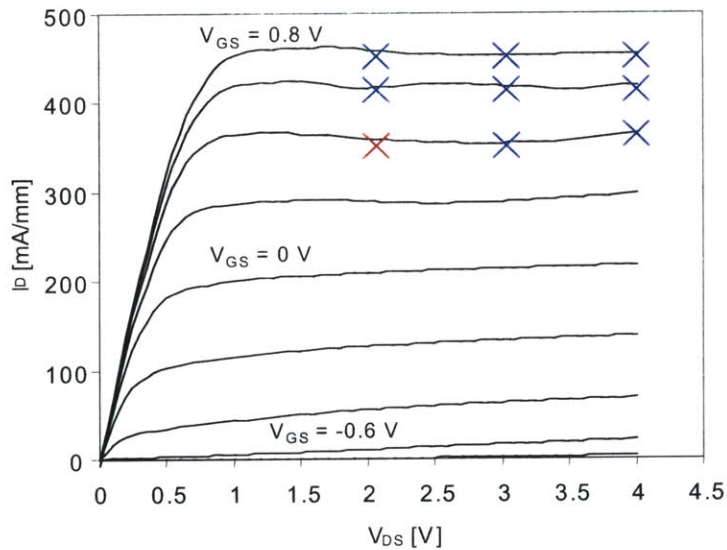
Fig. 4-23: Summary of $|S_{22}|$ behavior in the forward biased gate region of the L_{RD} = 0.7 um device. V_{GS} is from –0.8 to 0.8 V in 0.2 V increments. Red X: $|S_{22}|$ > 1, Blue X: $|S_{22}|$ < 1.

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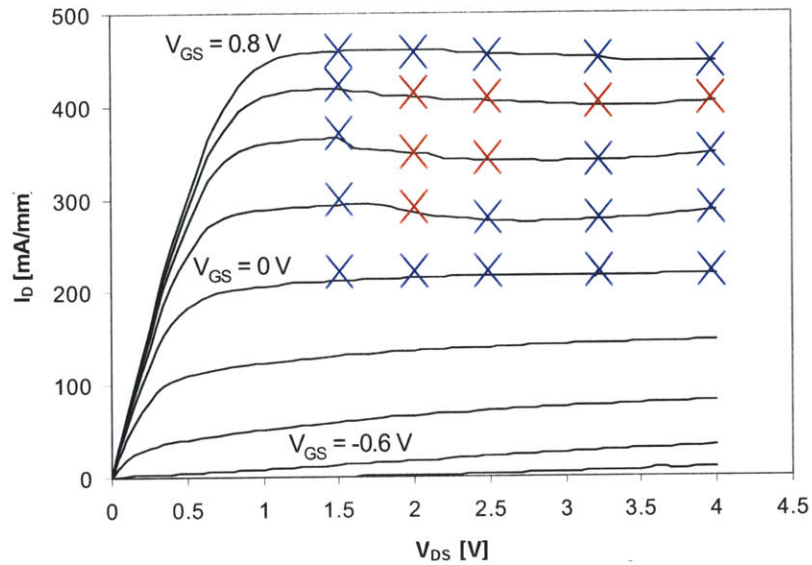
Fig. 4-24: Summary of $|S_{22}|$ behavior in the forward biased gate region of the $L_{RD} = 0.9$ um device. V_{GS} is from −0.8 to 0.8 V in 0.2 V increments. Red X: $|S_{22}| > 1$, Blue X: $|S_{22}| < 1$.

4.5 Negative g_{ds}

The intrinsic S-parameters were converted to Y-parameters [38] and analyzed at forward gate voltage biases. For a typical low-noise device at low frequencies (less than 5 GHz), the output conductance g_{ds} is the real part of Y_{22} [18]. At low frequencies (<10 GHz), g_{ds} remains positive for the $L_{RD} = 0.3$ um device regardless of bias (Fig. 4-25). However, for the $L_{RD} = 0.9$ um device, there is a strong correlation between negative g_{ds} and the existence of a NDR region. For instance, when $V_{GS} = 0.4$ V, g_{ds} remains negative until $V_{DS} = 4.0$ V and the device is no longer in the NDR region (Fig. 4-26). When $V_{GS} = 0.8$ V, g_{ds} is mostly positive for all values of V_{DS} (Fig. 4-27). This effect significantly affects the magnitude of S_{22}, which was discussed in the previous section.

Figs. 4-28 and 4-29 summarize our results regarding g_{ds} for the $L_{RD} = 0.7$ and 0.9 um devices. The appearance of negative g_{ds} exists within the NDR region of the output characteristics and indicates anomalous behavior. The occurrence of negative gds is much more prevalent with the $L_{RD} = 0.9$ um device than the $L_{RD} = 0.7$ um device.

80
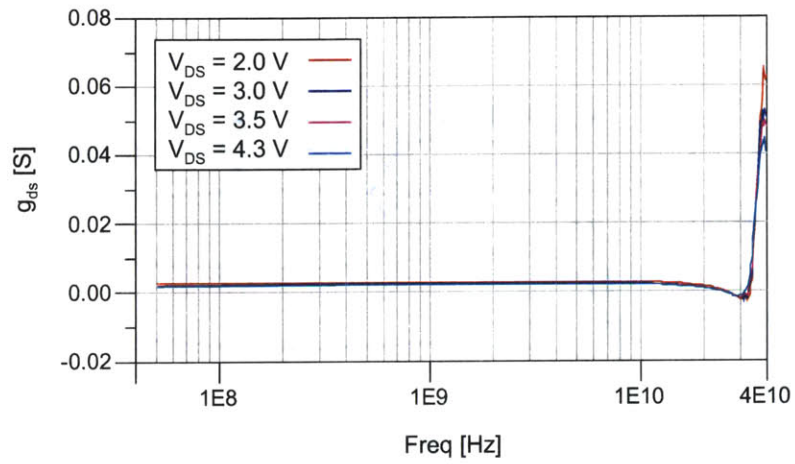
Fig. 4-25: g_{ds} versus frequency for the $L_{RD} = 0.3$ um device at $V_{GS} = 0.2$ V.
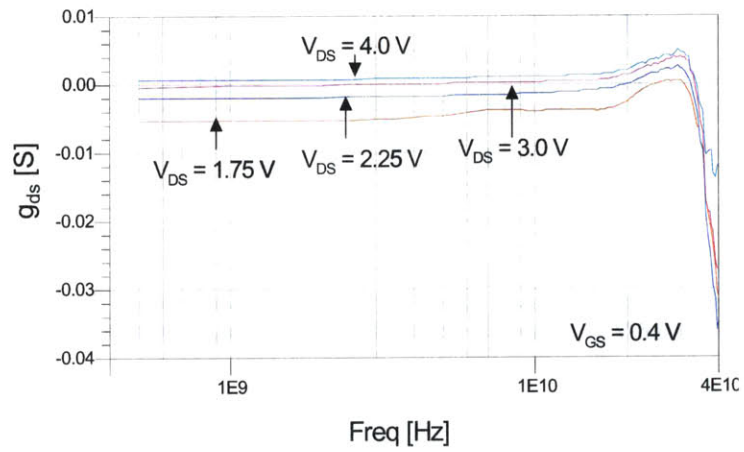
Fig. 4-26: g_{ds} versus frequency for the $L_{RD} = 0.9$ um device at $V_{GS} = 0.4$ V.
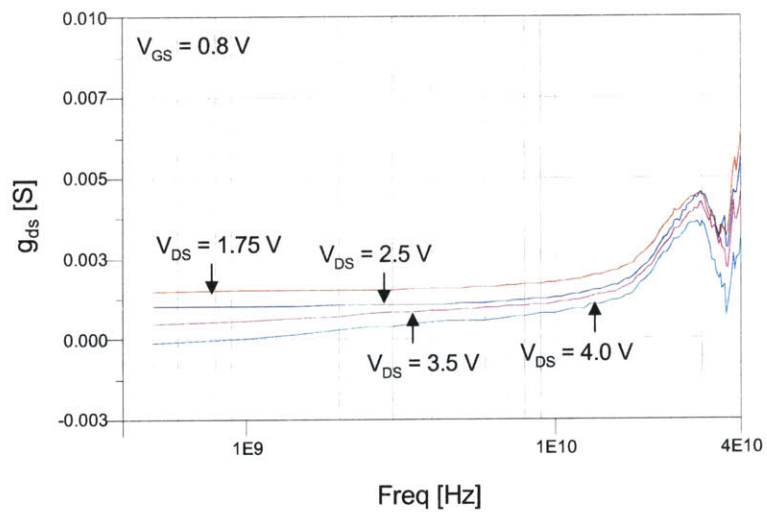
Fig. 4-27: g_{ds} versus frequency for the $L_{RD} = 0.9$ um device at $V_{GS} = 0.8$ V.

81
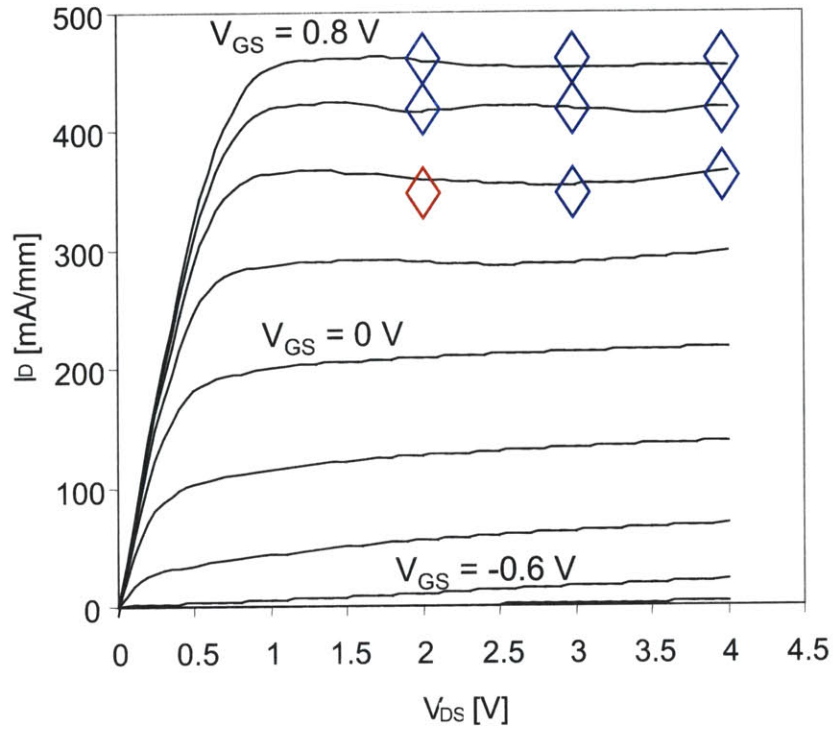
Fig. 4-28: Summary of g_{ds} behavior in the forward biased gate region of the $L_{RD} = 0.7$ um device. V_{GS} is from -0.8 to 0.8 V in 0.2 V increments. Red diamond: $g_{ds} < 0$, blue diamond: $g_{ds} > 0$.
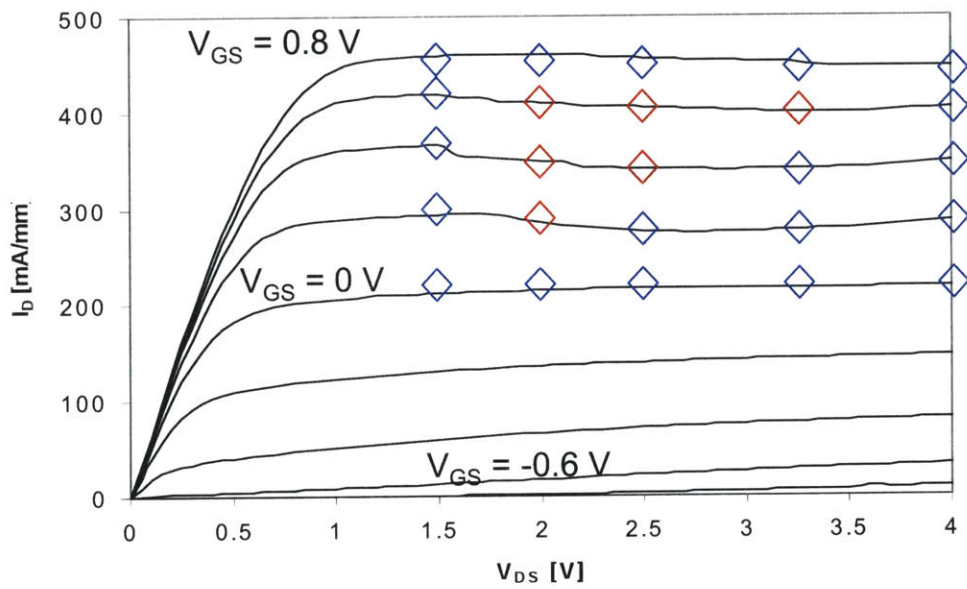
Fig. 4-29: Summary of g_{ds} behavior in the forward biased gate region of the $L_{RD} = 0.9$ um device. V_{GS} is from -0.8 to 0.8 V in 0.2 V increments. Red diamond: $g_{ds} < 0$, blue diamond: $g_{ds} > 0$.

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4.6 Stability Circles

When the two-port network in Fig. 4-30 is potentially unstable, passive source and load

terminations exist that can produce input and output impedances with a negative real part. These

values of Γ_S and Γ_L can be determined via a graphical procedure that maps the location of the

stability circles. This graphical analysis is useful in the analysis of potentially unstable transistors.
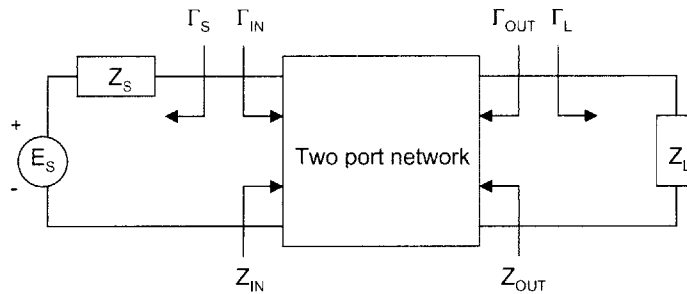
Fig. 4-30: Stability of a two-port network.

First, the circular regions where Γ_S and Γ_L can produce $|\Gamma_{IN}| = 1$ and $|\Gamma_{OUT}| = 1$ must be

determined. The radii and centers of these circles are given by [39]:

Γ_L **values for $|\Gamma_{IN}| = 1$ (Output Stability Circle):**

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \qquad \text{(radius)}$$

$$C_L = \frac{\left(S_{22} - \Delta S_{11}^*\right)^*}{|S_{22}|^2 - |\Delta|^2} \qquad \text{(center)}$$

Γ_S **values for $|\Gamma_{OUT}| = 1$ (Input Stability Circle):**

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \qquad \text{(radius)}$$

$$C_L = \frac{\left(S_{22} - \Delta S_{11}^*\right)^*}{\left|S_{11}\right|^2 - \left|\Delta\right|^2} \qquad \text{(center)}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$. With the S-parameters of a two-port device at one frequency, the stability circles can be plotted out on the source and load planes and the set of values corresponding to $|\Gamma_{IN}| = 1$ and $|\Gamma_{OUT}| = 1$ can be obtained. On one side of the source stability circle boundary, we will have $|\Gamma_{IN}| < 1$ and on the other side $|\Gamma_{IN}| > 1$. Likewise, on one side of the load stability circle boundary, we will have $|\Gamma_{OUT}| < 1$ and on the other side $|\Gamma_{OUT}| > 1$.

We have computed the stability circles of the $L_{RD} = 0.7$ and 0.9 um devices at 6 GHz at bias points within the NDR region. Within these stability circles exist regions of instability. The $L_{RD} = 0.7$ um device does not show stability circles that contain the 50 Ω point. At $V_{GS} = 0.4$ and 0.6 V, the load stability circle for the $L_{RD} = 0.9$ um device takes up half of the load plane and contains the 50 Ω point (Fig. 4-31). In addition, the $V_{GS} = 0.6$ V source stability circle begins to intrude further into the Smith Chart. As we continue to increase the gate bias to $V_{GS} = 0.8$ V, the device appears much more stable because the source and load stability circles are now almost outside of the Smith Chart.

Source stability circles   Load stability circles
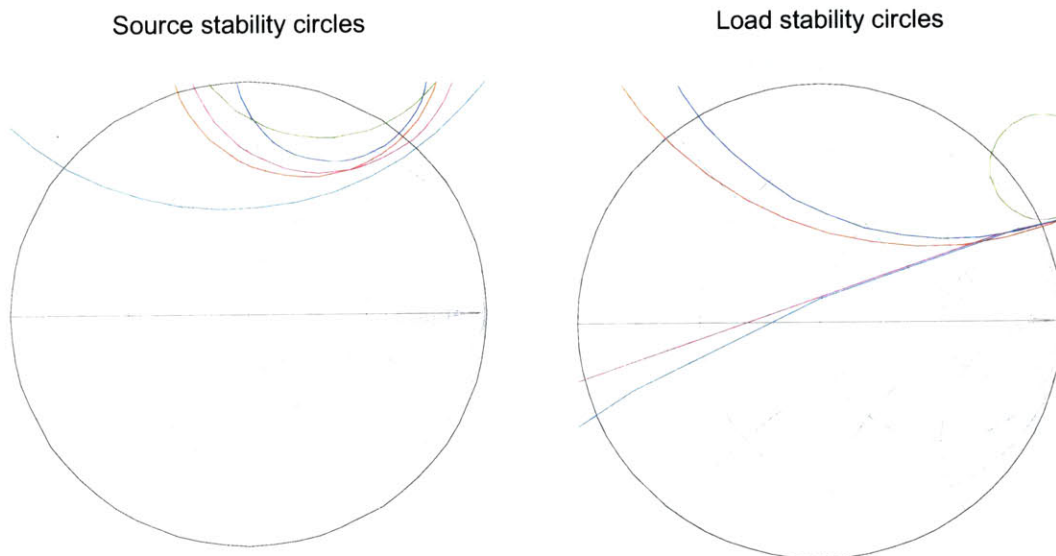
Fig. 4-31: Stability circles at 6 GHz for the $L_{RD} = 0.9$ um device at $V_{DS} = 4.0$ V and different V_{GS}. Red: $V_{GS} = 0$ V, Blue: $V_{GS} = 0.2$ V, Magenta: $V_{GS} = 0.4$ V, Cyan: $V_{GS} = 0.6$ V, Green: $V_{GS} = 0.8$ V.

Figs. 4-32 and 4-33 summarize our results at each bias point measured for the L_{RD} = 0.7 and 0.9 um devices, respectively. The bias points where potential instability is observed (i.e., when the unstable region of the stability circles includes the 50 Ω point) are confined primarily to the NDR region of the output characteristics.
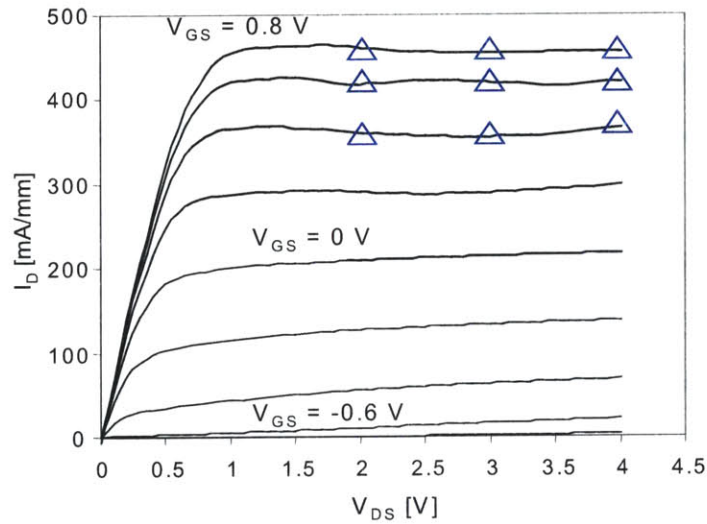
Fig. 4-32: Summary of stability behavior as determined by the stability circles in the forward biased gate region of the L_{RD} = 0.7 um device. V_{GS} is from –0.8 to 0.8 V in 0.2 V increments. Blue triangle: stable.
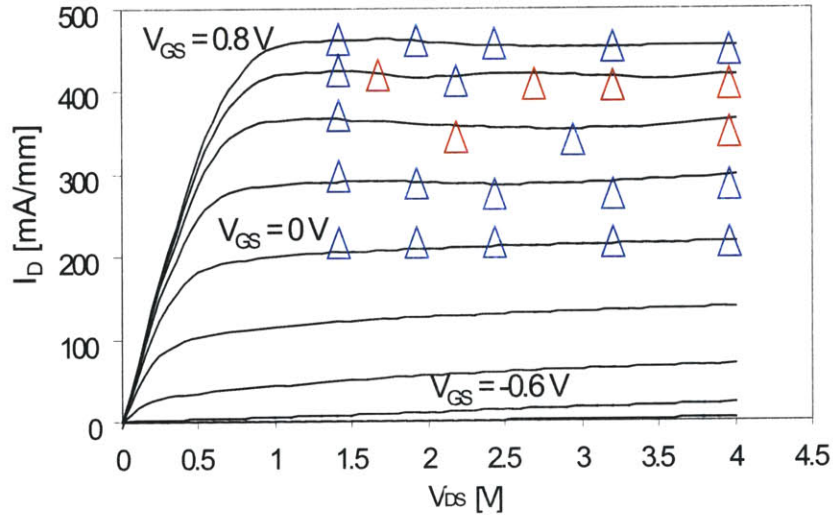
Fig. 4-33: Summary of stability behavior as determined by the stability circles in the forward biased gate region of the L_{RD} = 0.9 um device. V_{GS} is from –0.8 to 0.8 V in 0.2 V increments. Blue triangle: stable, red triangle: potentially unstable.

4.7 Conclusions

Our results shown so far provide ample and definitive evidence that the NDR region of the output characteristics of the long L_{RD} devices is strongly correlated with the presence of oscillations and other anomalies. The results of all measurements for the L_{RD} = 0.7 and 0.9 devices are summarized in Figs. 4-34 and 4-35. The appearance of oscillations is much stronger in the L_{RD} = 0.9 um device than the L_{RD} = 0.7 um device due to its larger NDR region.

First, we observed significant levels of P_{OUT} above the noise floor under DC conditions as L_{RD} was increased from 0.3 to 0.9 um. Second, we detected numerous oscillation frequencies in the NDR region via a spectrum analyzer connected to the output of the L_{RD} = 0.9 um device. Third, we found that $|S_{22}| > 1$ in the NDR regions of the L_{RD} = 0.7 and 0.9 um devices, causing an amplified RF signal to be reflected into the drain electrode. Through examination of the Y-parameters, we found that g_{ds} was negative when $|S_{22}| > 1$ for the two aforementioned devices.
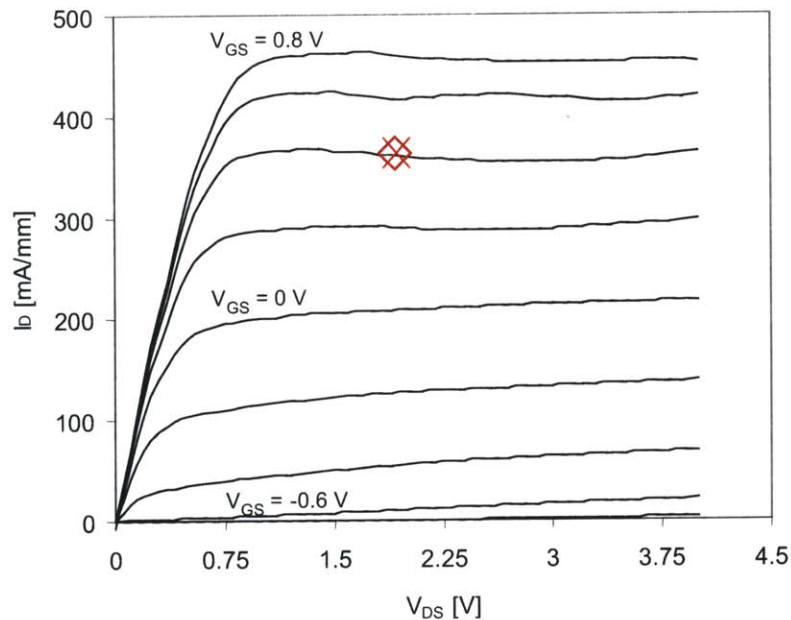
Fig. 4-34: Two affirmative criteria for oscillations plotted against the output characteristics of the L_{RD} = 0.7 um device. X: $|S_{22}| > 1$, diamond: negative g_{ds}. V_{GS} is ramped from –0.8 to 0.8 V in 0.2 V increments.
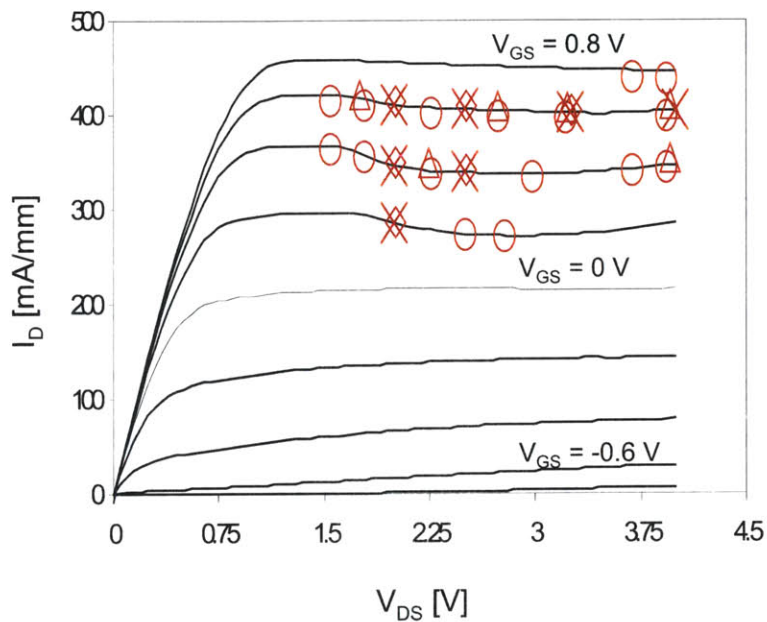
Fig. 4-35: Four affirmative criteria for oscillations plotted against the output characteristics of the $L_{RD} = 0.9$ um device. X: $|S_{22}| > 1$, diamond: negative g_{ds}, triangle: potentially unstable as determined from stability circles, circle: spurious signals observed with a spectrum analyzer at the output. V_{GS} is ramped from –0.8 to 0.8 V in 0.2 V increments.

Lastly, the stability circles for the $L_{RD} = 0.9$ um device at 6 GHz show a large intrusion of the load stability circle into the load plane when $V_{GS} = 0.4$ and 0.6 V that encompasses the 50 Ω point. The next step is to examine the connection, if any, between the presence of oscillations in the long L_{RD} devices and their anomalous large signal performance. This is investigated in the next chapter.

Chapter 5: Discussion

5.1 Introduction

In this chapter, we will attempt to piece together the anomalous RF behavior with other various phenomena shown by the devices under study. First, we will analyze the discrepancy between the calculated and measured $P_{OUT,3\text{-}dB}$ across L_{RD} and frequency. We seek to explain the difference in RF power behavior of the different devices through the evolution of load lines with frequency, L_{RD}, and V_{DD}. To arrive at this understanding, we must first explore the impact of BV_{off}, BV_{on}, and oscillations as observed in the NDR region on the placement of the load lines. Pulsed I-V measurements will reveal if the devices under study are besieged by surface states.

5.2 Calculated vs. Measured $P_{OUT,3\text{-}dB}$

The presence of significant self-biasing makes a direct comparison between devices difficult. We have been exploring alternative ways to assess the impact of L_{RD} on the RF power performance. A way to do this is to look at the difference between the actual measured P_{OUT} and the expected maximum P_{OUT} based on the bias point at the 3-dB compression point. A simple estimate of the maximum saturated output power delivered by the device is given by

$$P_{OUT,SAT} = \frac{1}{2}V_{DD}I_{DC}$$

where I_{DC} is the self-biased drain current at the 3-dB compression point. This expression represents a classical class A linear amplifier with a drain efficiency of 50%.
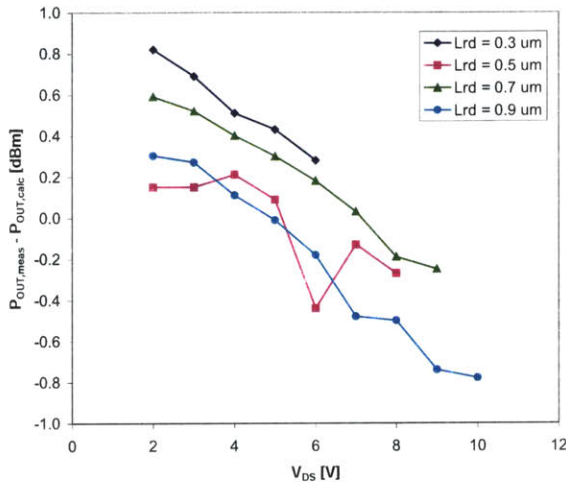
Fig. 5-1: $P_{OUT,meas} - P_{OUT,calc}$ versus V_{DS} at 8 GHz.
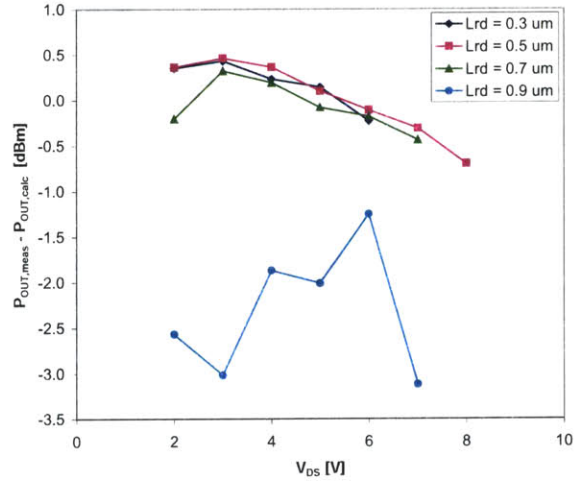
Fig. 5-2: $P_{OUT,meas} - P_{OUT,calc}$ versus V_{DS} at 12 GHz.

Using this ideal model, the farther the measured P_{OUT} deviates from the calculated P_{OUT}, the more the device deviates from ideal behavior. Figs. 5-1 through 5-3 show the difference between measured and calculated P_{OUT} in dBm (or ratio of calculated to measured P_{OUT}) versus V_{DS} at 8, 12, and 16 GHz. $P_{OUT,MEAS} - P_{OUT,CALC}$ may experience changes in polarity because the model is simplistic and overestimates P_{OUT}. As the devices are driven to compression, $P_{OUT,MEAS} - P_{OUT,CALC}$ approaches zero as they self bias to a greater extent. At all three frequencies, the
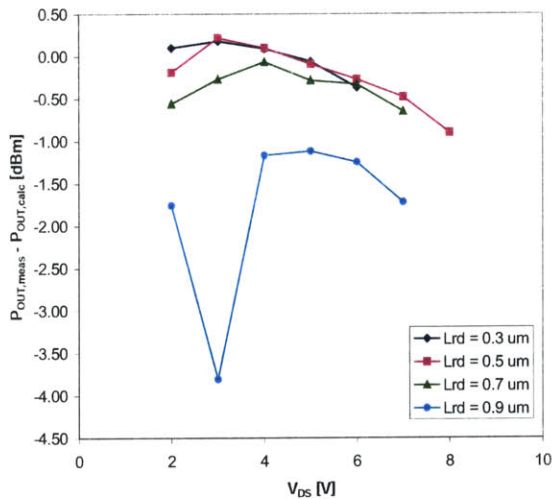
Fig. 5-3: $P_{OUT,meas} - P_{OUT,calc}$ versus V_{DS} at 16 GHz.
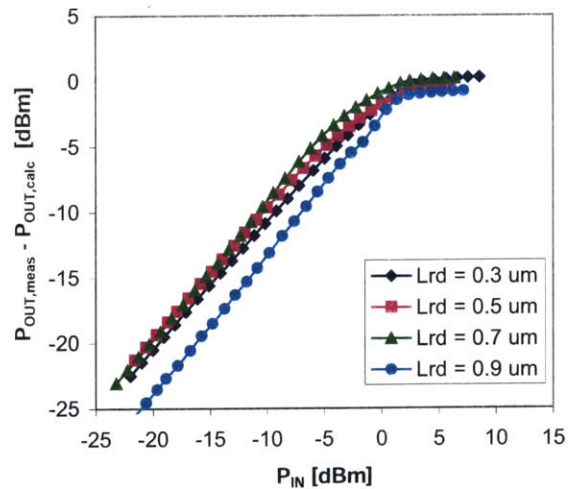
Fig. 5-4: $P_{OUT,meas} - P_{OUT,calc}$ versus P_{IN} at 8 GHz. The bias point is $V_{DS} = 6$ V, $I_{D0} = 100$ mA/mm.

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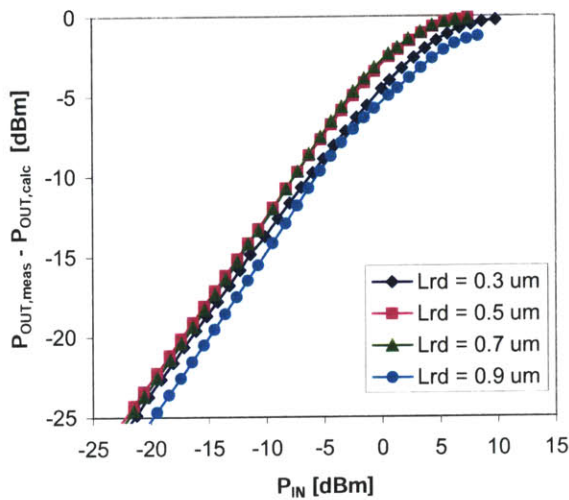
Fig. 5-5: $P_{OUT,meas} - P_{OUT,calc}$ versus P_{IN} at 12 GHz. The bias point is $V_{DS} = 6$ V, $I_{D0} = 100$ mA/mm.
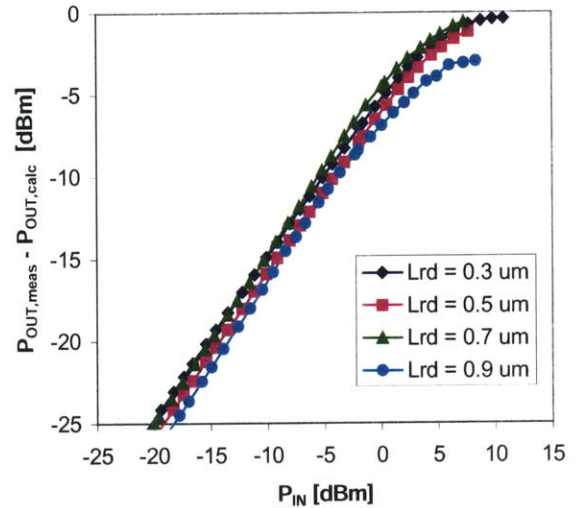
Fig. 5-6: $P_{OUT,meas} - P_{OUT,calc}$ versus P_{IN} at 16 GHz. The bias point is $V_{DS} = 6$ V, $I_{D0} = 100$ mA/mm.

longest L_{RD} device consistently exhibited the largest deviation from zero with RF drive and hence the highest error (Figs. 5-4 through 5-6).

Although this method of calculating the maximum saturated power is approximate in nature, the disparity between measured and calculated output powers is too large to be ascribed to the calculation procedure or any small experimental errors (typical power measurement errors are < ± 0.5 dB). These observations indicate anomalous behavior exists that is most strongly affecting the longest L_{RD} device and is preventing it from achieving its RF power potential.

5.3 Load Lines

Graphing the load lines provides insight to the behavior under large signal conditions. The starting point of this discussion begins with the basic, load line-matched, class A amplifier, optimized for maximum output power (Fig. 5-7). Optimal RF power performance is obtained when the drain and gate bias center the load line such that the onset of saturation is caused by the simultaneous and balanced interaction of the load line with the breakdown and forward gate conduction regions [23]. In other words, the quiescent point must be placed halfway between the

$V_{DS,SAT}$ and BV_{off} as well as 0 and I_{MAX} to maximize the excursions of the peak-to-peak voltage and current waveforms during linear swing. Beyond the maximum linear swing, a symmetrically clipped waveform will be generated. The device loading condition governs the slope of load line and the equation for output power is
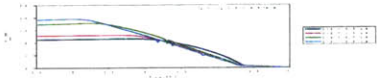
By this relation, it follows that the shortest L_{RD} device, which has a BV_{off} of approximately half that of the longest L_{RD} device, should deliver the least output power. As L_{RD} and BV_{off} increases, we expect $P_{OUT, 3\text{-}dB}$ to increase as well. Even though we have experimentally established that this does not occur, we can relate the drop in $P_{OUT, 3\text{-}dB}$ with the placement of the load lines.

The voltage waveform is a simple Ohm's Law scaling of the current waveform where the load behaves as sink while the device behaves as a generator. To compute the load resistance R_L and the placement of the load line, we assume that the RF coupled load consists of shunt-connected parallel resonant RLC circuit with a conceptual harmonic short. In this way, it is assumed that we are only considering the RF energy of the fundamental. All harmonics of the
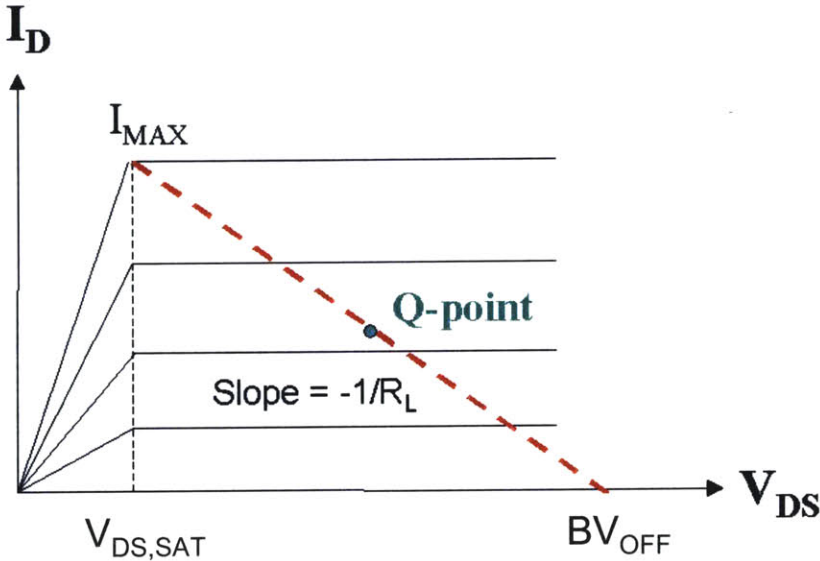
Fig. 5-7: Ideal load line for maximum output power in Class A operation.

load are shorted and do not generate voltage; therefore, the drain voltage is a sinusoid whose magnitude will be set by R_L to generate the maximum possible waveform excursion. If the load lines were measured by a Microwave Transition Analyzer (MTA), they would exhibit distortion in the form of hysteresis as the device enters compression [25]. However, a resistive load analysis provides a good starting point for understanding the large signal behavior of the PHEMT.

Depending on the device design, either BV_{off} or the on-state breakdown BV_{on} can limit the maximum allowable drain voltage of a PHEMT [40]. In the next few sections, we will determine BV_{off} and the placement of the BV_{on} loci of the devices under study to determine which metric governs the optimum placement of the load line. Since the BV_{on} loci begin at a lower V_{DS} than BV_{off}, they are of primary importance when considering the maximum V_{DS} that can be achieved by the load line.

5.3.1 Off-state Breakdown

The off-state breakdown (BV_{off}) is a parameter of primary important for power devices and limits the maximum power density of a PHEMT. A significant body of work has been dedicated toward understanding the origin of BV_{off}. As a result, it is possible to engineer PHEMTs with a desired BV_{off} [40-42]. The gate current injection method was utilized to determine the BV_{off} of the devices under study [42]. While maintaining a constant $I_D = 0.1$ mA/mm, V_{GS} was swept from 0 to 3.5 V. BV_{off} is defined as the peak V_{DG} which occurs when $I_S = 0$ mA/mm and $I_D = -I_G = 0.1$ mA/mm (Fig. 5-8). A comparison of BV_{off} between the devices under study is shown in Fig. 5-2. Clearly, increasing L_{RD} is advantageous for BV_{off}; as L_{RD} is increased from 0.3 to 0.9 um, BV_{off} doubles from 11.5 to 21.2 V. A higher BV_{off} should allow the selection of a higher operating voltage V_{DD} that ought to lead to a higher P_{OUT}.
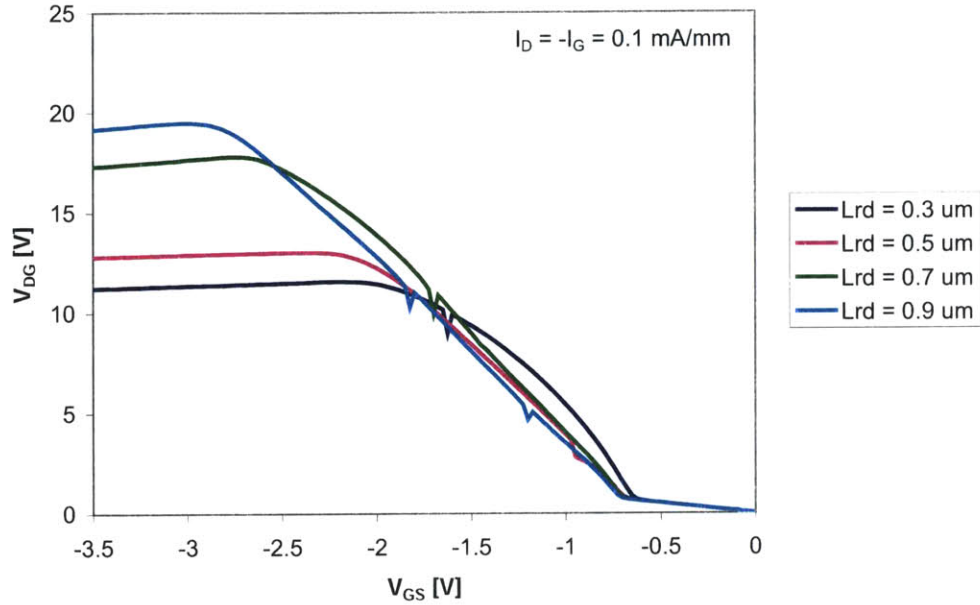
Fig. 5-8: Measurement of BV_{off} for the L_{RD} = 0.5 um PHEMT.

5.3.2 On-state Breakdown

The shape of the on-state breakdown (BV_{on}) locus is critical to a device's power potential and dictates the placement of the maximum output power load line [23]. To obtain clues for the physical mechanism that limits power for the devices, the on-state breakdown characteristics have been extracted for all four devices via the gate current extraction technique described by Somerville et al [40]. During the measurement, I_G was held constant at −0.1 mA/mm while the I_D was ramped up to 150 mA/mm (approximately 30% of I_{MAX}). The gate current extraction method traces a BV_{on} locus of V_{DS} vs. I_G and shows that increasing L_{RD} also increases the onset of the BV_{on} loci, which is favorable for RF power performance (Fig. 5-9). Unfortunately, only the smallest L_{RD} device survived this measurement; the rest of the devices were destroyed through catastrophic burnout before I_D could reach 150 mA/mm.

An analysis of the power dissipated in the device during the measurement reveals that the maximum dissipated power of the three devices that experienced burnout was 1400 mW/mm while the maximum dissipated power of the sole surviving device was only 1178 mW/mm (Table

1). For the three devices that were destroyed, we can conclude that burnout was attributed to thermal destruction. Since the BV_{on} loci begin at V_{DS} lower than their respective BV_{off}, they may pose the greater limitation depending on the precise placement of the load line. As the load line hits against the BV_{on} loci, significant carrier multiplication via impact ionization occurs and causes the device to degrade.
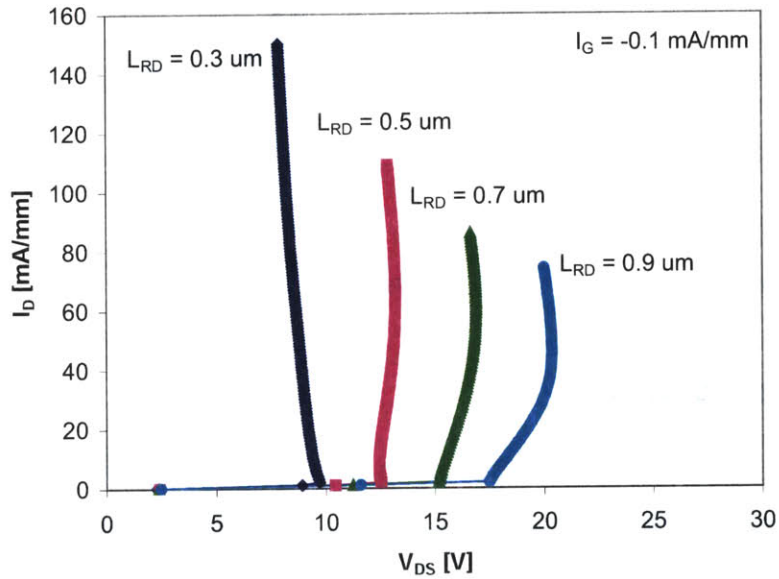
Fig. 5-9: BV_{on} versus I_D for 100 um (2 x 50 um) PHEMTs for devices with different L_{RD} at I_G = -0.1 mA/mm. A constant current is extracted from the gate while the drain current is swept from the off-state (0.1 mA/mm) to the on-state.

L_{RD} [um]	V_{DS} [V]	I_D [mA]	Power [mW/mm]
0.3	7.85	150.1	1178
0.5	12.85	109.1	1402
0.7	16.64	86.1	1432
0.9	20.00	74.1	1482

Table 1: Electrical characteristics at burnout resulting from BV_{on} experiment

5.3.3 Load lines across L_{RD}

Using the optimized load impedance, we have calculated the load line placement for the different L_{RD} devices at $V_{DS} = 6$ V and $I_{DO} = 100$ mA/mm. At 8 GHz, the shorter L_{RD} is, the more optimal the load line is for RF power (Fig. 5-10). The load line for the shortest L_{RD} device maximizes the I-V plane by balancing its placement between I_{max} and BV_{off} while the load line for the longest L_{RD} device falls short of both the BV_{off} region and I_{max}. The load lines for the $L_{RD} = 0.7$ and 0.9 um devices also appear to be avoiding the NDR region in the output characteristics. The same trends observed at 8 GHz also appear at 12 and 16 GHz (Figs. 5-11 and 5-12). In general, for a given bias point, the load lines become more ideal for optimum RF power as L_{RD} decreases.
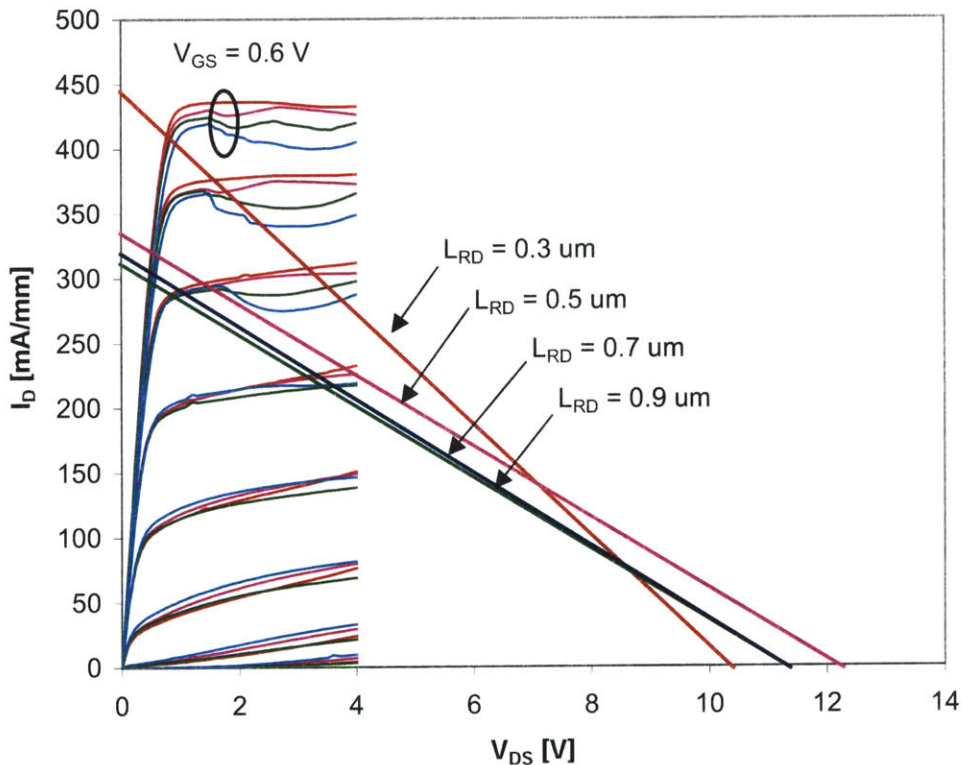
Fig. 5-10: Load lines for devices with different L_{RD} at 8 GHz and $V_{DS} = 6$ V, $I_{D0} = 100$ mA/mm
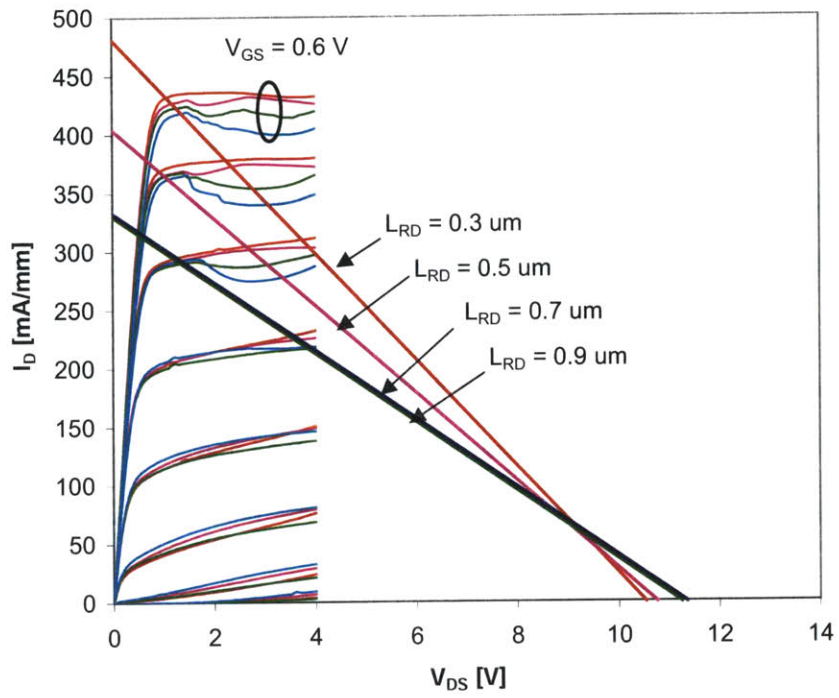
Fig. 5-11: Load lines for devices with different L_{RD} at 12 GHz and V_{DS} = 6 V, I_{D0} = 100 mA/mm
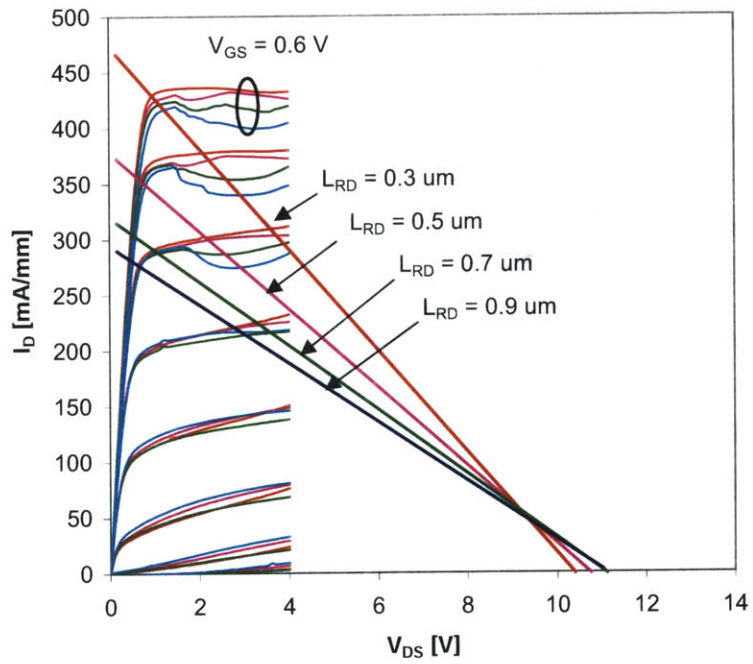
Fig. 5-12: Load lines for devices with different L_{RD} at 16 GHz and V_{DS} = 6 V, I_{D0} = 100 mA/mm

5.3.4 Load lines across V_{DD}

In this section, we will study the behavior of the load lines as a function of V_{DD} for the shortest L_{RD} (0.3 um) and longest L_{RD} (0.9 um) device at three different frequencies; the behavior of the other two devices under study is expected to fall somewhere in between. As V_{DD} is increased, the device is capable of delivering more power. At 8 GHz, the L_{RD} = 0.3 um experiences a higher degree of self-bias with increasing V_{DD}, and when V_{DD} = 6 V, the load line is hitting up against BV_{on} and I_{max} (Fig. 5-13). Similar load line trends with V_{DD} are also observed for the L_{RD} = 0.3 um device at 12 and 16 GHz (Figs. 5-14 to 5-15). Since BV_{off} (10.5 V) occurs at a greater V_{DD} than the onset of BV_{on}, BV_{on} is the bottleneck and BV_{off} is of secondary importance when it comes to placing the optimum power load line [43]. As the devices interact more strongly with the breakdown region, they are forced into power saturation caused by RF induced gate current breakdown as holes exit the channel due to impact ionization (see Section 3.1.3). A rise in I_D occurs along with the sharp increase in I_G as the devices enter compression. Recall in Section 3.1.5 that the L_{RD} = 0.3 um device incurs severe degradation due to impact ionization under large signal operation at V_{DD} = 6 V.
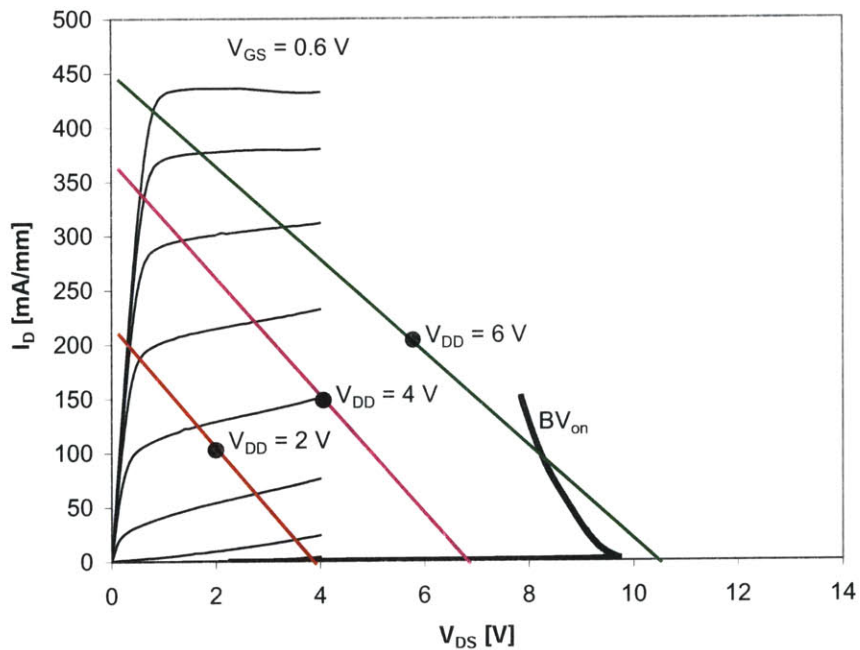
Fig. 5-13: Load lines for the L_{RD} = 0.3 um device at 8 GHz and V_{DS} = 2, 4, 6 V and I_{D0} = 100 mA/mm
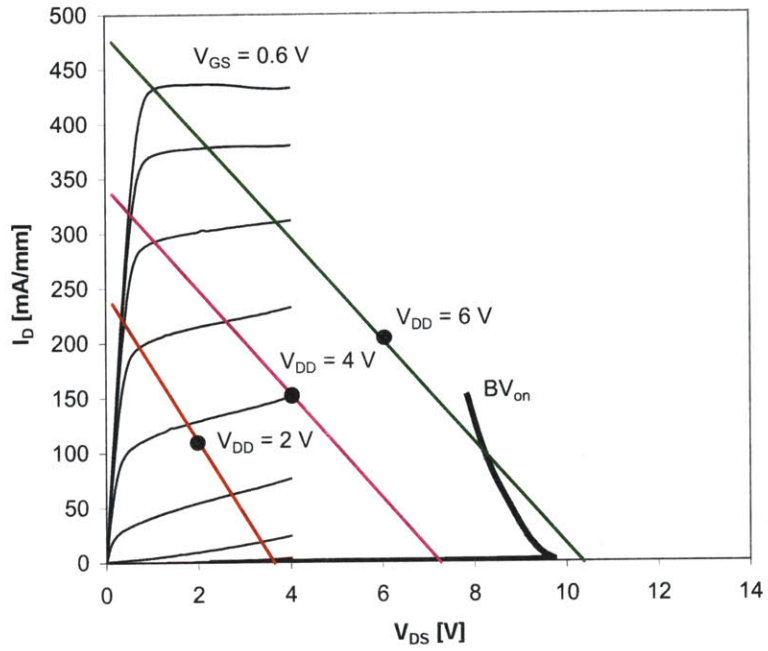
Fig. 5-14: Load lines and BV$_{on}$ locus for the L$_{RD}$ = 0.3 um device at 12 GHz and V$_{DD}$ = 2, 4, 6 V and I$_{D0}$ = 100 mA/mm.
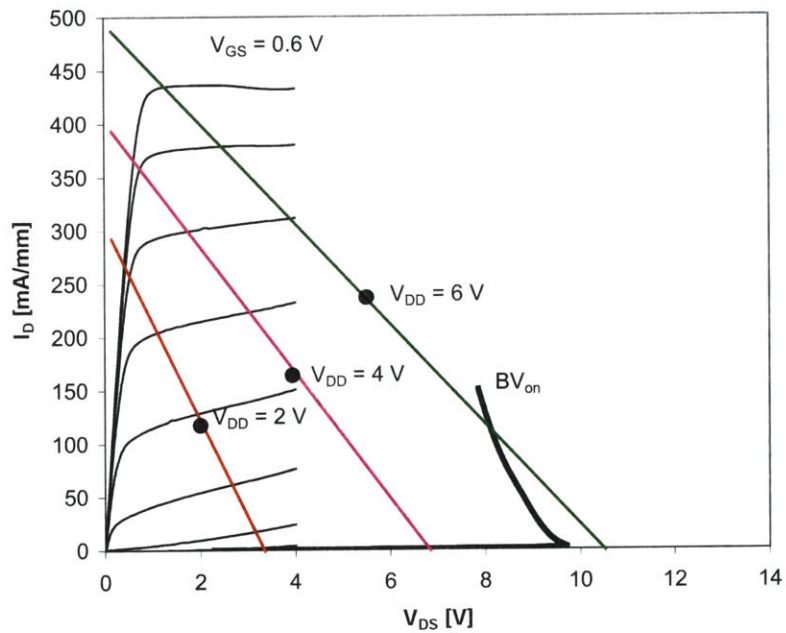
Fig. 5-15: Load lines and BV$_{on}$ locus for the L$_{RD}$ = 0.3 um device at 16 GHz and V$_{DD}$ = 2, 4, 6 V and I$_{D0}$ = 100 mA/mm

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The load line behavior of the L_{RD} = 0.9 um device is drastically different from the behavior shown by the L_{RD} = 0.3 um device. Due to the much higher BV_{off} and BV_{on} of the L_{RD} = 0.9 um device, it is possible to apply drain biases as high as 10 V at 8 GHz (Fig. 5-16). However, the ability to apply a high drain bias is not enough to ensure high output power. Unfortunately, the load lines do not maximize the I-V plane because the current waveform swing is drastically limited as a result of the low maximum I_D that can be achieved. The same behavior in the load lines is also observed at 12 GHz, except the maximum allowable V_{DD} before catastrophic burnout was 7 V (Fig. 5-17). During the successive ramping of V_{DD} on a single L_{RD} = 0.9 um device at 16 GHz, the maximum allowable V_{DD} before catastrophic burnout was also 7 V; however, an optimization was successfully performed at V_{DD} = 8 V on a second virgin device after which the device immediately burned out (Fig. 5-18). The resulting load line at V_{DD} = 8 V passes through the anomalous NDR region, which most likely caused the catastrophic burnout due to the presence of oscillations. We conclude that the load lines for the L_{RD} = 0.9 um device are more susceptible to burnout at higher frequencies due to the device entering its unstable bias region.
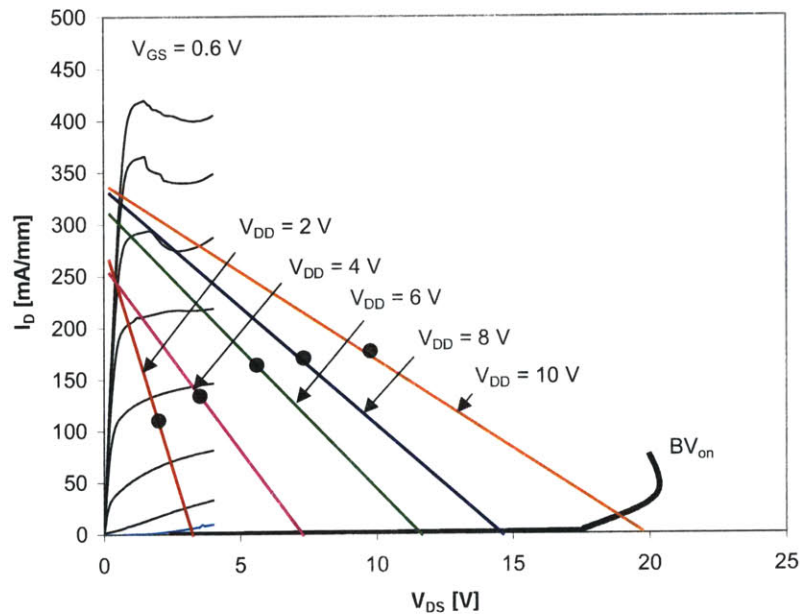
Fig. 5-16: Load lines and BV_{on} locus for the L_{RD} = 0.9 um device at 8 GHz and V_{DD} = 2, 4, 6, 8, 10 V and I_{D0} = 100 mA/mm
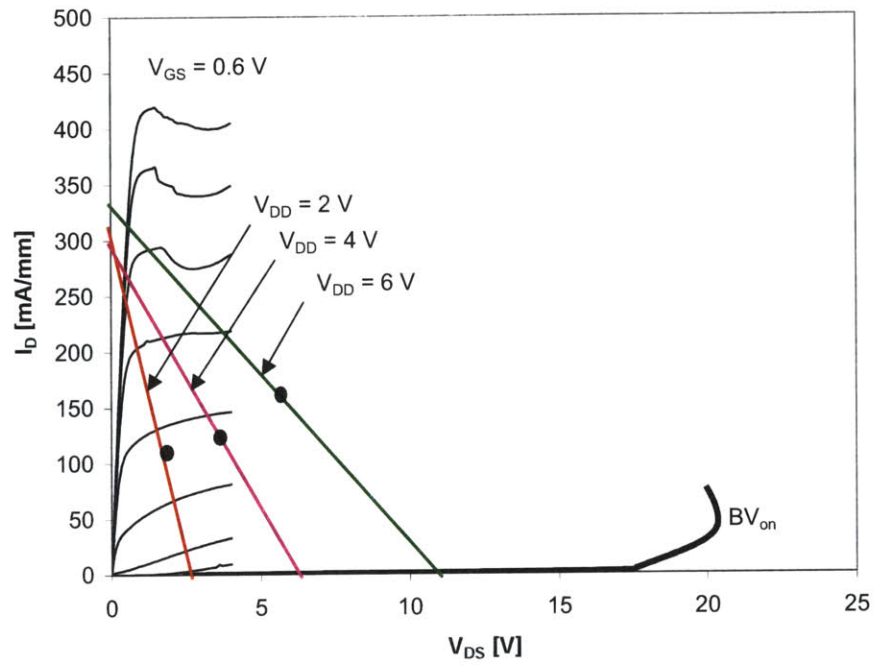
Fig. 5-17: Load lines and BV_{on} locus for the L_{RD} = 0.9 um device at 12 GHz and V_{DD} = 2, 4, 6 V and I_{D0} = 100 mA/mm
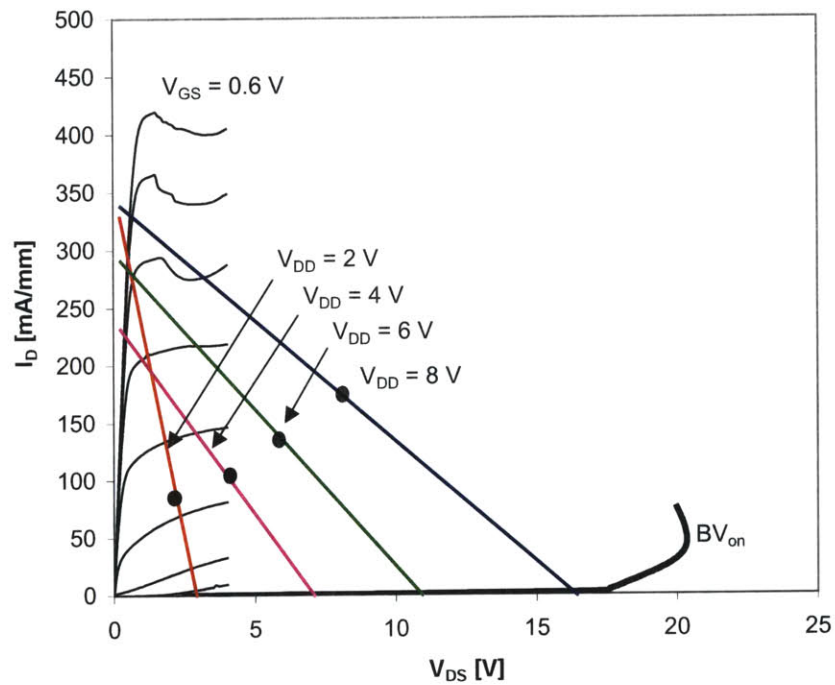
Fig. 5-18: Load lines and BV_{on} locus for the L_{RD} = 0.9 um device at 16 GHz and V_{DS} = 2, 4, 6 V and I_{D0} = 100 mA/mm. The device burned out immediately after optimization at V_{DD} = 8 V.

5.4 Pulsed IV Measurements

To explore the possibility of drain current degradation due to surface states, pulsed I-V measurements were carried out at Mitsubishi Electric on the different L_{RD} devices. In these measurements, pulses of one microsecond duration with a one millisecond duty cycle were made from a static quiescent bias point (V_{DSQ} and V_{GSQ}) to defined locations in the IV plane. Four different quiescent bias points were examined. Such a measurement more accurately resembles RF operation; since charge trapping and detrapping effects do not have sufficient time to occur in the time scale that is studied, the trap charge state depends only on the choice of quiescent point [5]. To get a complete picture of the pulsed I-V behavior, the four quiescent points considered are: (1) $V_{DSQ} = 0$ V, $V_{GSQ} = 0.6$ V; (2) $V_{DSQ} = 0$ V, $V_{GSQ} = -0.6$ V; (3) $V_{DSQ} = 4$ V, $V_{GSQ} = 0.6$ V; (4) $V_{DSQ} = 4$ V, $V_{GSQ} = -0.6$ V. For all of the measurements, the pulse that was applied ramped V_{DS} from 0 to 5 V while V_{GS} was ramped from –1 V to 0.8 V in 0.2 V increments.

The minimum time constant of the trapping conditions can vary since trapping is dependent upon the quiescent bias point in RF operation. Due to these variable trapping conditions, the pulsed I-V measurement gives a more accurate set of I-V curves for a PHEMT that are relevant for RF power operation [44]. The severity of the surface effects is determined by examining how much the pulsed I-V measurements deviate from the DC I-V curves. Fig. 5-19 shows that the pulsed I-V curves of the $L_{RD} = 0.3$ um device exhibit bias dependence, with the highest drain current collapse occurring when $V_{DSQ} = 4$ V, $V_{GSQ} = -0.6$ V. For the $L_{RD} = 0.5$ um device, a stronger collapse occurs in the pulsed I-V curves when $V_{DSQ} = 4$ V and $V_{GSQ} = -0.6$ V; however, the I-V curves appear fairly constant at the other three quiescent points (Fig. 5-20). The $L_{RD} = 0.7$ um device shows yet an even stronger collapse in I_D when $V_{DSQ} = 4$ V and $V_{GSQ} = -0.6$ V (Fig. 5-21) but not nearly as high of a degree of sensitivity at the other quiescent points. Finally, the $L_{RD} = 0.9$ um device is clearly besieged by surface states as demonstrated by the severe current collapse of the pulsed drain current when $V_{DSQ} = 4$ V and $V_{GSQ} = -0.6$ V (Fig. 5-22).
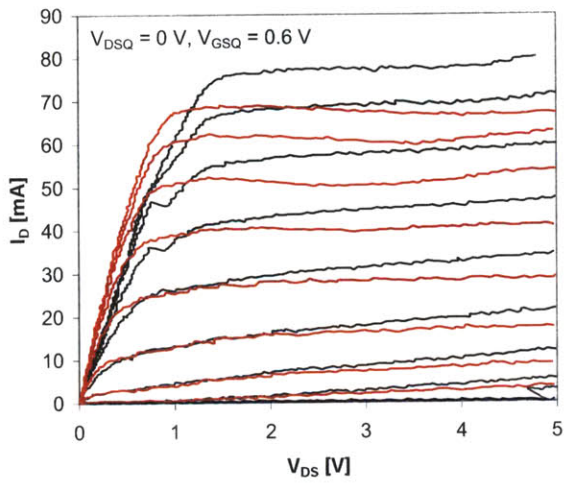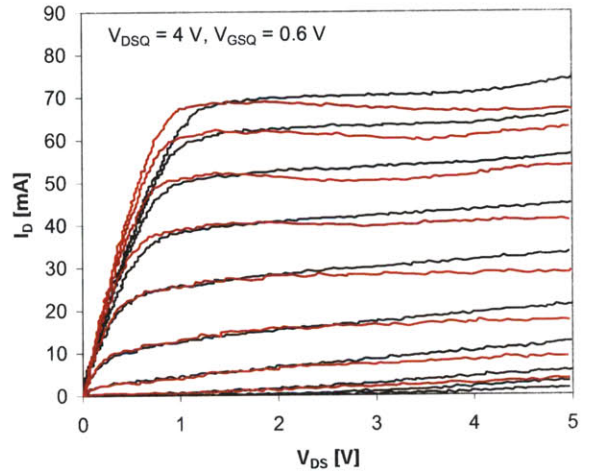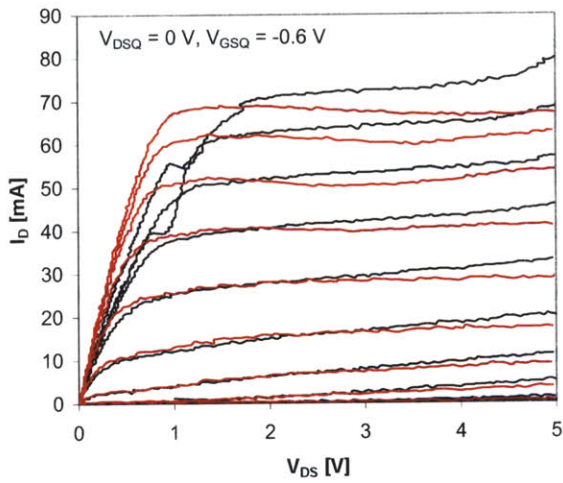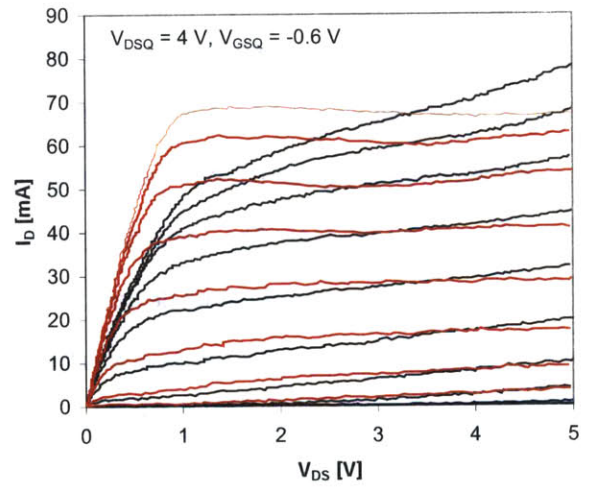
Fig. 5-19: Comparison between the pulsed I-V (black) and DC characteristics (red) of the L_RD = 0.3 um device. The quiescent points are indicated in the figures.
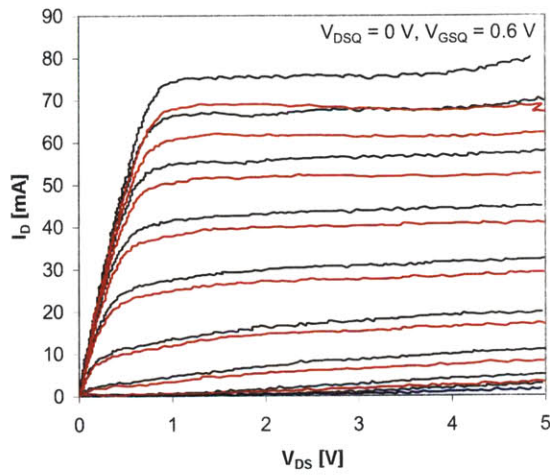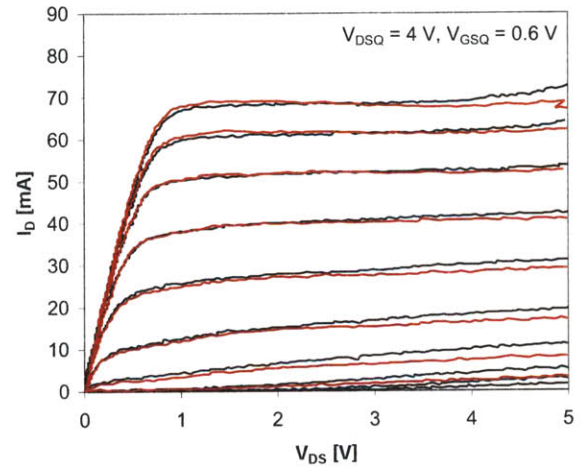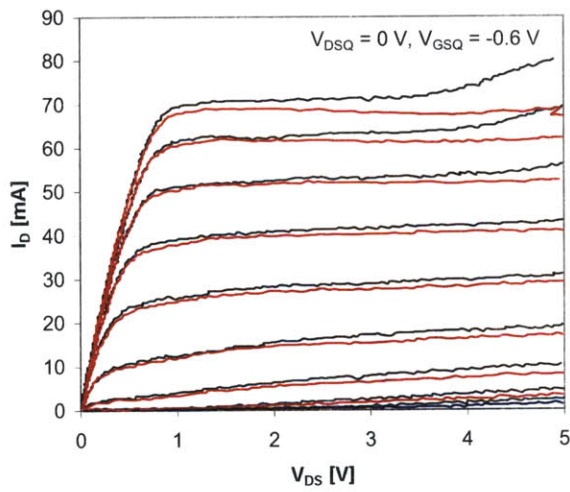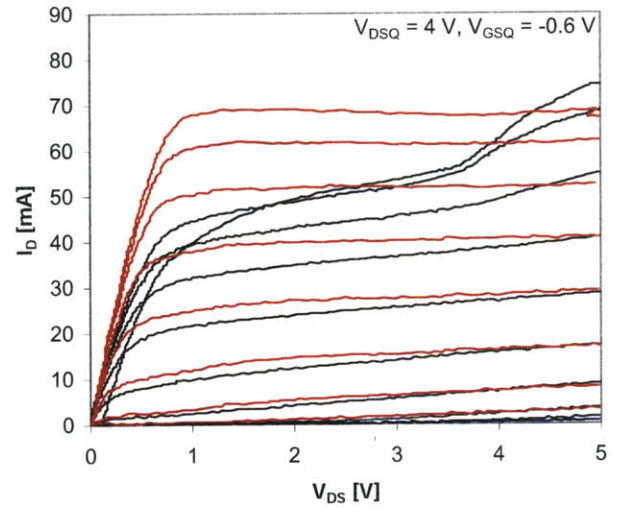
Fig. 5-20: Comparison between the pulsed I-V (black) and DC characteristics (red) of the L_{RD} = 0.5 um device. The quiescent points are indicated in the figures.

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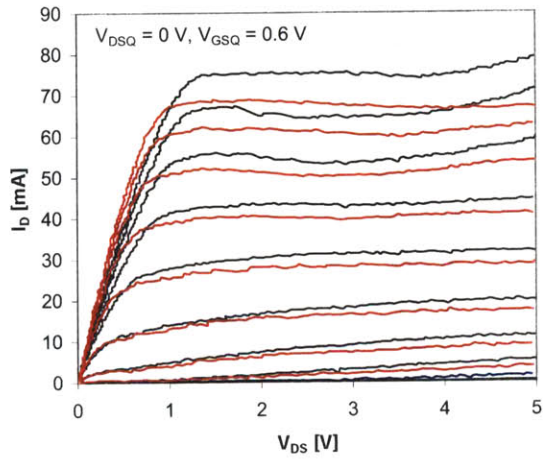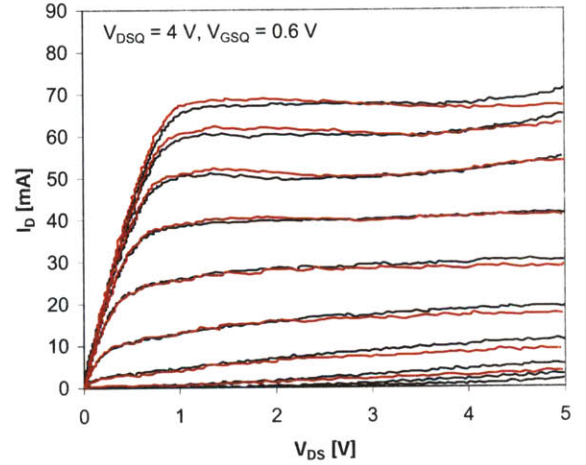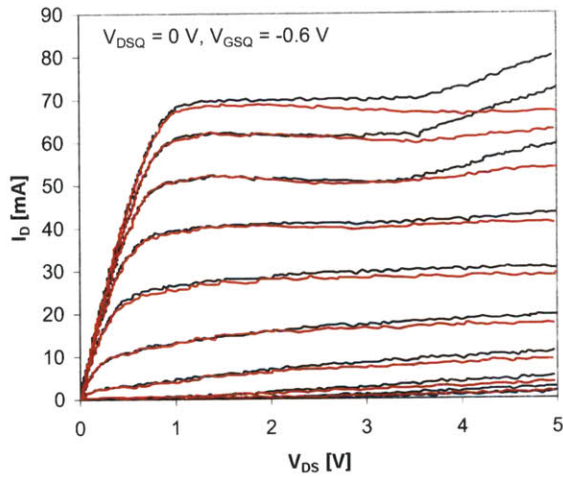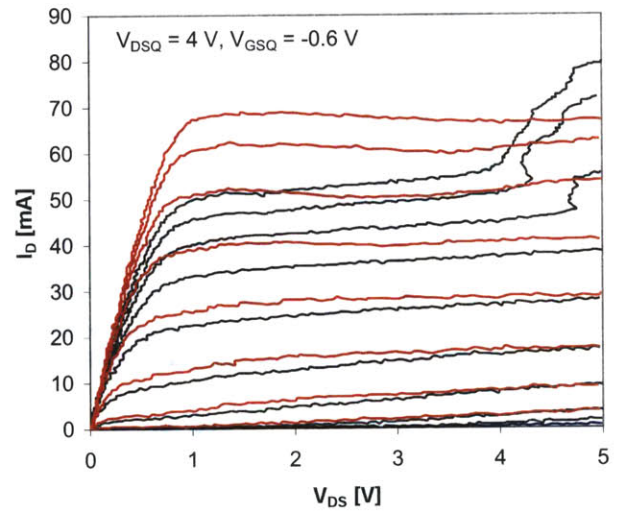
Fig. 5-21: Comparison between the pulsed I-V (black) and DC characteristics (red) of the L_{RD} = 0.7 um device. The quiescent points are indicated in the figures.
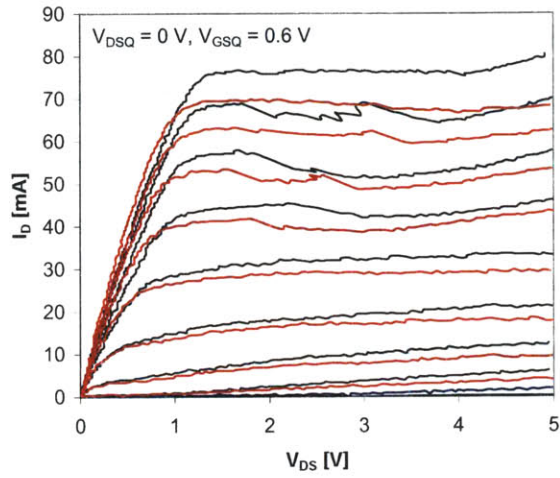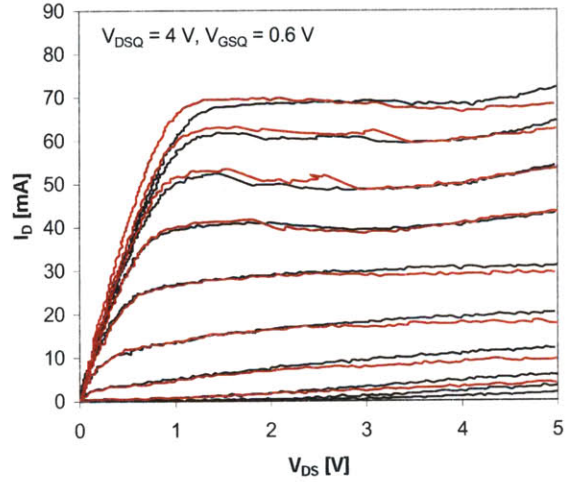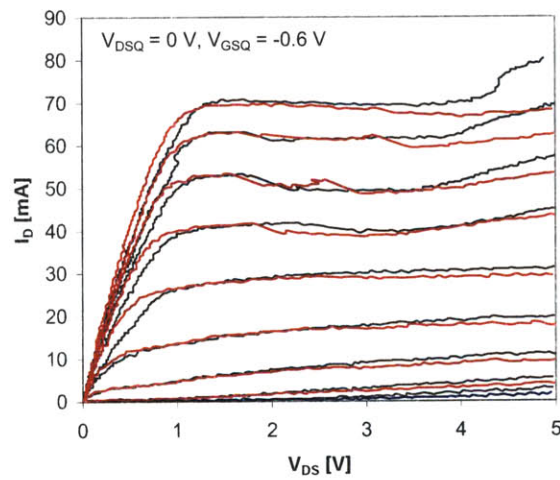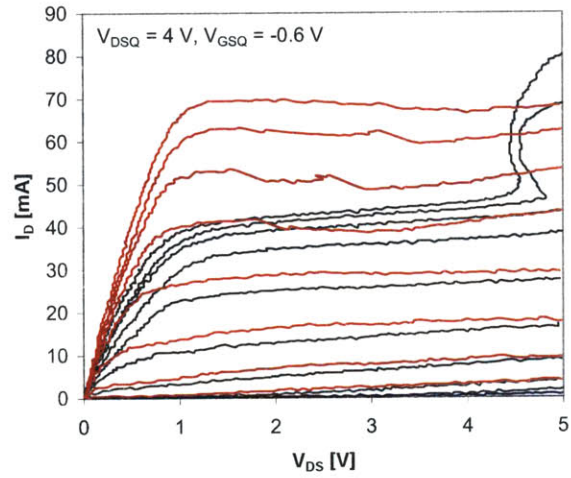
Fig. 5-22: Comparison between the pulsed I-V (black) and DC characteristics (red) of the $L_{RD} = 0.9$ um device. The quiescent points are indicated in the figures.

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From the results shown, it is clear that the devices under study become more sensitive to surface effects the longer L_{RD} becomes despite the double-recess gate structure. Due to the large bias voltages used during a microwave power measurement, surface states trap electrons and form a negatively charged parasitic gate in the gate-drain access region [5]. If there exists negative charge on the surface, the surface potential is made negative, depleting the channel of electrons and leading to the extension of the gate depletion region toward the drain. Evidence of this gate depletion region extension is given by the increase in drain delay with increasing L_{RD} (see Section 3.2.4). Due to the slow time constant of the trapping/detrapping transient, it takes time for the surface charge to be modulated and the extrinsic channel cannot respond instantaneously; as the bias point swings across the load line. Therefore, the extrinsic drain next to the gate remains with a surface charge situation that corresponds to the bias condition of the lower right corner of the load line, where the depletion region is typically wide, the drain current is small, and R_D is high.

The traps in the device cause a reduction of the output current as a function of frequency of RF drive. Since the electrons contained in the surface layer cannot fully modulate the channel charge during large signal RF operation, the current waveform swing is reduced and adversely affects the output power. Studies performed on the nature of current collapse when the device is operated as an amplifier and driven to saturation have shown that the extent of drain current collapse is larger at larger drain biases [45]. In addition, the higher $V_{DS,SAT}$ and reduction in I_D and g_m in the DC measurements with increasing L_{RD} can be explained by electron capture at interface states that exist in the gate-drain region between the GaAs/passivation or in the passivation itself [7, 46]. To improve the RF power capability of these devices, it is necessary to improve the screening of the excess surface charges that cause the parasitic gating effect; one possible option is applying a field-plate process [47].

5.5 Conclusions

Through comparison of the measured and calculated $P_{OUT,3\text{-}dB}$, the longest L_{RD} device consistently shows the largest discrepancy across frequency and L_{RD}. Across the range of frequencies measured, the load lines become shallower and less ideal for optimum power performance as L_{RD} is increased. When V_{DD} was increased from 2 to 6 V, the load line for the $L_{RD} = 0.3$ um reached an optimal location in the I-V plane and was eventually limited by the BV_{on} locus. On the other hand, the load lines for the $L_{RD} = 0.9$ um device exhibited reduced current waveform swing capability across frequency and V_{DD}. At 12 and 16 GHz, the devices experienced catastrophic breakdown during optimization at $V_{DD} = 8$ V, most likely due to the load line passing through the NDR region of the output characteristics.

The pulsed I-V curves of all devices exhibit varying degrees of bias dependence that become more severe as L_{RD} is increased. This finding suggests that surface effects are present either at the GaAs/passivation interface or in the passivation itself. The presence of a parasitic gate on the gate-drain adjoining the gate explains the poor large signal performance since the surface charge cannot respond instantaneously to microwave frequencies. In addition, the parasitic gate will also cause a reduction in I_D and g_m as well as an increase in $V_{DS,SAT}$, all phenomena which we have seen in the devices under study.

Chapter 6: Conclusions and Suggestions for Further Work

6.1 Conclusions

Using an automated measurement scheme, we have performed an exhaustive analysis of the RF power performance of GaAs Pseudomorphic High Electron Mobility Transistors (PHEMTs) with different gate-drain gap lengths. Despite the improvement in BV_{off} with increasing L_{RD} that should allow a theoretical increase in maximum operating voltage and hence an increase in power, we have experimentally found that the long L_{RD} devices actually deliver less output power than the short L_{RD} devices. In addition, the decline in output power is steeper for long devices than short L_{RD} devices with increasing frequency. At higher frequencies, catastrophic burnout limits the maximum allowable V_{DD} that can be applied to the long L_{RD} devices. To gain additional understanding to the origins of these anomalous behaviors, we have also studied the DC, pulsed, and small signal characteristics to provide insight into the device physics.

In our RF power measurements, we have observed that all things being equal, $P_{OUT,3\text{-}dB}$ decreases with increasing L_{RD}. This can be explained by a load line analysis: while the shorter L_{RD} (0.3, 0.5 um) devices show load lines suitable for optimum RF power, the longer L_{RD} (0.7, 0.9 um) devices exhibit load lines that fall short of this criteria and experience premature current waveform clipping as a result. We have also shown that the longer L_{RD} is, the steeper the decline in $P_{OUT,3\text{-}dB}$ as a function of frequency. In addition, the maximum allowable operating voltage was limited by degradation for the shorter L_{RD} devices and catastrophic burnout for the longer L_{RD} devices. At 12 and 16 GHz, the maximum V_{DD} was actually less for the longer L_{RD} devices than the smaller L_{RD} devices.

Small signal equivalent circuit extraction revealed trends regarding the intrinsic elements with increasing L_{RD}: an increase in C_{GS}, τ, and R_{DS} and a decrease in C_{GD} and g_m. As a result, f_T

suffers as L_{RD} is increased. A delay time analysis shows that the increase in drain delay with increasing V_{DS} becomes more rapid with L_{RD} and can be interpreted as a growing extension of the depletion region toward the drain. Pulsed I-V measurements show that while all of the devices exhibit some degree of dependence on the quiescent point, the situation is worst for the long L_{RD} devices. This finding reveals the existence of a parasitic gate in the gate-drain region due to surface effects that becomes more prominent with increasing L_{RD}; this detracts from real I_{max} at RF frequencies and therefore the devices deliver less power.

An investigation into device stability has shown that the long L_{RD} devices suffer from oscillations in the region of the output characteristics that is characterized by a NDR region. These oscillations pose a problem as the load lines might enter this region at high enough V_{DD}. In our studies, the oscillations manifest themselves as output spectra under DC conditions, negative R_{DS}, positive $|S_{22}|$, and unstable regions of the stability circles that enclose a large portion of the source and load Smith charts.

6.2   Suggestions for Further Work

Although our current research on impact of L_{RD} on RF power performance of GaAs PHEMTs has concluded, there are still many more studies and experiments than deserve further consideration. They will provide helpful insight into the device physics and mechanisms affecting RF power performance.

Perhaps the most important concern regarding these devices is mitigating surface effects in the drain-gate region and eliminating the deleterious "parasitic gate", whose presence becomes stronger as L_{RD} increases. We have shown that surface states cause the RF performances of the devices degrade rapidly as L_{RD} increases. Additionally, the influence of surface effects have been shown to have an adverse effect on reliability in previous studies [48]. To improve the screening of surface effects from the channel, it is necessary to improve the quality of the device
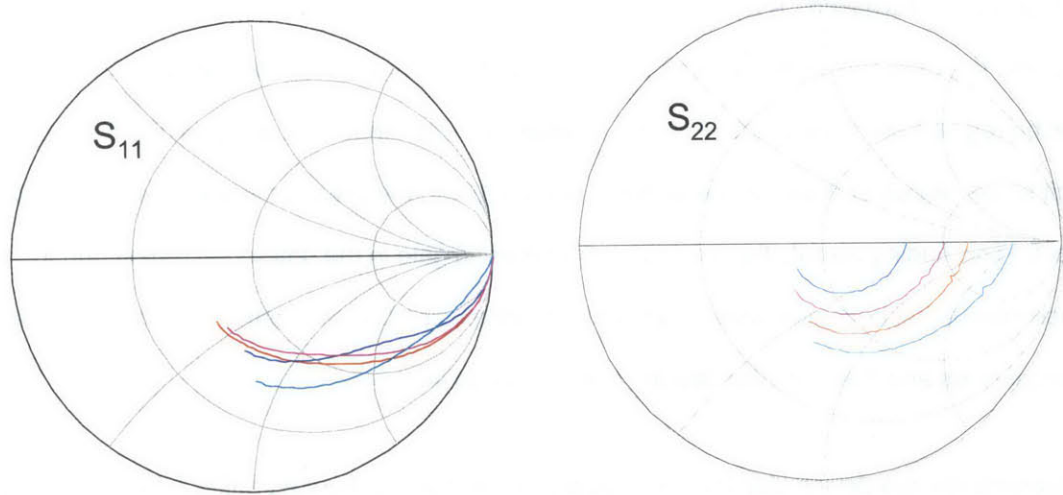
Fig. 6-1: S_{11} and S_{22} of four "open" structures consisting of the pad structures with the metal lines to the active region severed via laser ablation.

passivation using alternative techniques. To further characterize the nature of the surface states, a deep level transient spectroscopy (DLTS) characterization could be performed that would reveal the detailed nature of the traps affecting the device [49].

To accurately extract the intrinsic small signal equivalent circuit, it is of primary importance to de-embed the parasitic pad capacitances from the as-measured S-parameter measurements before proceeding with the de-embedding of the extrinsic parasitic elements [29]. Since the appropriate test structure (the probing pads without the active region) was not available, we attempted to create an equivalent test structure by severing the gold lines connecting the PHEMT to the gate and drain electrodes via laser ablation. Four such structures were fabricated in the Technology Research Laboratory (TRL) at MIT and their respective S_{11} and S_{22} measurements are shown in Fig. 6-1. Due to the difficulty in controlling the depth of the cut, the structures exhibit a large variation in R_{DS} that depend on the connection between the source and drain through the channel and are not suitable for de-embedding the pad parasitic capacitances. Thus, the only appropriate structure to use must consist only of the probing pads without an active region.

We initially attempted to create a 2D simulation of the standard PHEMT using ISE TCAD (now Synopsys) software to gain additional insight into the device physics, especially the impact

ionization in the longer L_{RD} devices. However, we were unable to successfully calibrate the device simulation to measured data within the time constraints of this research; this stringent procedure required the simultaneous fitting of currents and capacitances extracted from measured S-parameters as well as the fitting of the necessary transport and interface models [50-52]. A realistic representation between the ohmic contacts and of the channel based on a SIMS profile analysis would aid tremendously in future calibration efforts.

In addition, the possibility of the formation of Gunn domains on the drain side of the device, either dipoles or accumulation layers, has not yet been completely ruled out. Monte Carlo studies done on AlGaAs/GaAs HEMTs have shown that Gunn dipoles can cause NDR in the output characteristics and total failure when small alterations to the device design are made [53]. If Gunn domains indeed exist, an increased understanding of the existence of these dipoles may lead to preventing their formation and the subsequent adverse effects on the RF performance of these devices.

Lastly, the resolution of I_G in the load pull measurements could have been improved from 1 mA to 1 nA if we had used a HP 4145 instead of a HP 6628 for our biasing system. Unfortunately, the HP 4145 would produce oscillations at high RF drive, most likely due to grounding issues between the coax to triax connections. Resolving this problem would allow us to make better correlations between the RF induced behavior of I_D and I_G.

Appendix A: Buried WSi PHEMTs

i. Device Structure

In this research, a second type of PHEMT was studied. This device has a similar epitaxial structure as the Al gate PHEMT but with a buried WSi gate. The gate length of the device is 0.25 μm and the gate width is 600 μm (6 fingers x 100 μm). The large signal measurements of devices with three different values of L_{RD} (0.6, 1.4, 2.2 um) will be obtained while all other dimensions are held constant.

For a typical WSi gate PHEMT with L_{RD} = 1.4 um, a typical value of the source resistance is R_S = 1.26 Ω-mm, while the drain resistance is R_D = 1.63 Ω-mm. The drain current at V_{DS} = 1.2 V and V_{GS} = 0 V is I_{DSS} = 191.4 mA/mm, and the threshold voltage is –0.79 V. The peak transconductance (g_m = 330 mS/mm) occurs at V_{DS} = 1.2 V and V_{GS} = 0.06 V. The output conductance g_o = 41.1 mS/mm at this bias point and the drain-gate breakdown voltage BV_{off} is 12.6 V.

ii. DC Characteristics

The same DC characterization performed on the Al gate device was also done on the buried WSi gate devices. Within an error of 1%, the V_T for all five devices under study was –0.79 V. Although BV_{off} initially increases as L_{RD} increases from 0.4 to 1 um, it was found to decrease as L_{RD} is increased further to 2.2 um (Fig. A-1). The reason for this anomalous behavior is not understood. Similar to the Al gate devices, a larger L_{RD} is correlated to a larger R_D (Fig. A-1). In addition, with increasing L_{RD}, a decrease in g_m and an increase in g_{ds} are observed (Fig. A-2).

In the output characteristics, there is an increasing presence of NDR as L_{RD} is increased from 0.6 to 2.2 um when the gate is forward biased (Fig. A-3). Note that the collapse in I_D is more dramatic for high values of L_{RD}. In Fig. A-4, the longest WSi gate device shows a slight increase in I_G with a decrease in I_D.

The fact that the NDR becomes stronger with small changes in V_{GS} is consistent with the theory of real space transfer (RST) because a positive V_{GS} applied on the gate will incur an enhanced injection of electrons from the 2DEG within the InGaAs channel into the AlGaAs subspacer. If we
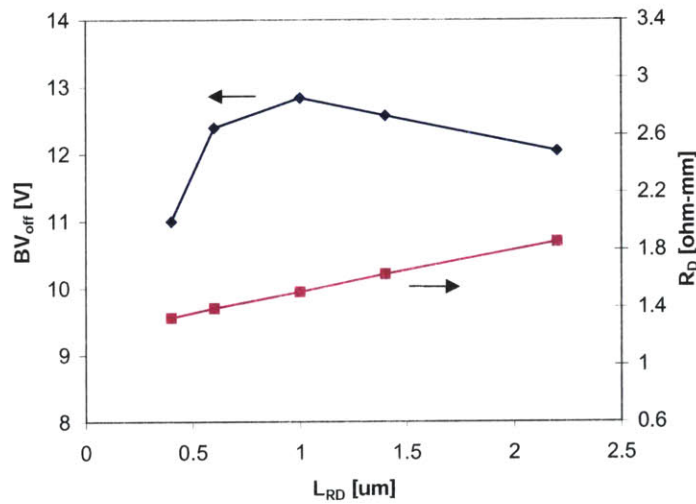
Fig. A-1: BV_{off} and R_D for WSi devices with L_{RD} = 0.4, 0.6, 1.0, 1.4, 2.2 um.
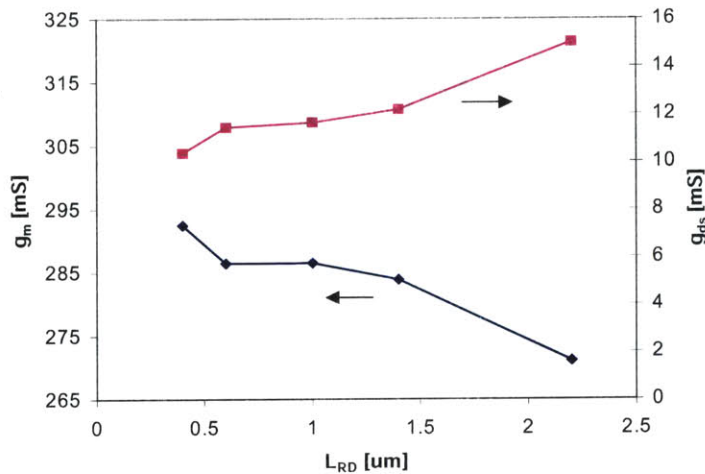
Fig. A-2: g_m and g_{ds} versus L_{RD} for WSi devices with L_{RD} = 0.4, 0.6, 1.0, 1.4, 2.2 um.

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consider the conduction-to-valence band split ratio between $Al_{0.24}Ga_{0.76}As$ and $In_{0.15}Ga_{0.85}As$ to be 60:40 [54], the conduction band discontinuity ΔE_C is approximately 0.32 eV. To estimate the energy necessary for momentum transfer between the Γ point and the next lowest conduction valley in the $In_{0.15}Ga_{0.85}As$ channel, we can linearly interpolate between 1.16 and 0.31 eV for GaAs and InGaAs, respectively. This analysis yields a separation energy $\Delta E_{\Gamma L}$ of approximately 0.44 eV. Since $\Delta E_{\Gamma L}$ is greater than ΔE_C, it is more likely that the hot electrons will experience real space transfer from $In_{0.15}Ga_{0.85}As$ to $Al_{0.24}Ga_{0.76}As$ before momentum space transfer between neighboring conduction valleys within the $In_{0.15}Ga_{0.85}As$ channel and lends supporting evidence that real space transfer is a possible cause of NDR.
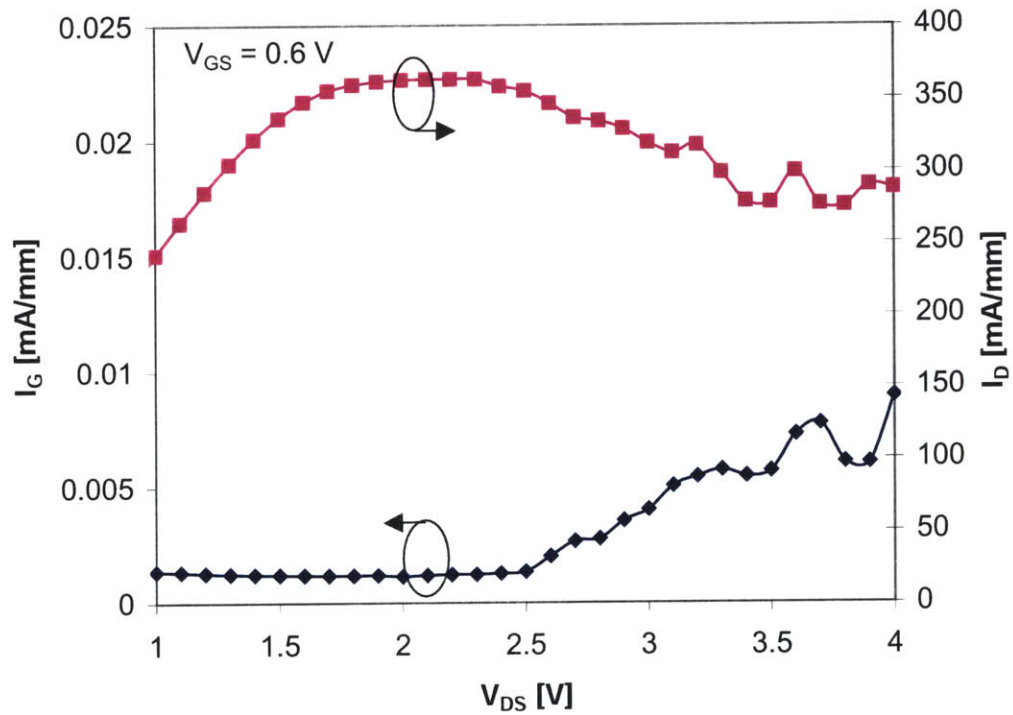
Fig. A-3: Output characteristics of WSi gate devices with varying L_{RD}. V_{GS} = -0.8 to 0.6 V in 0.2 V increments.
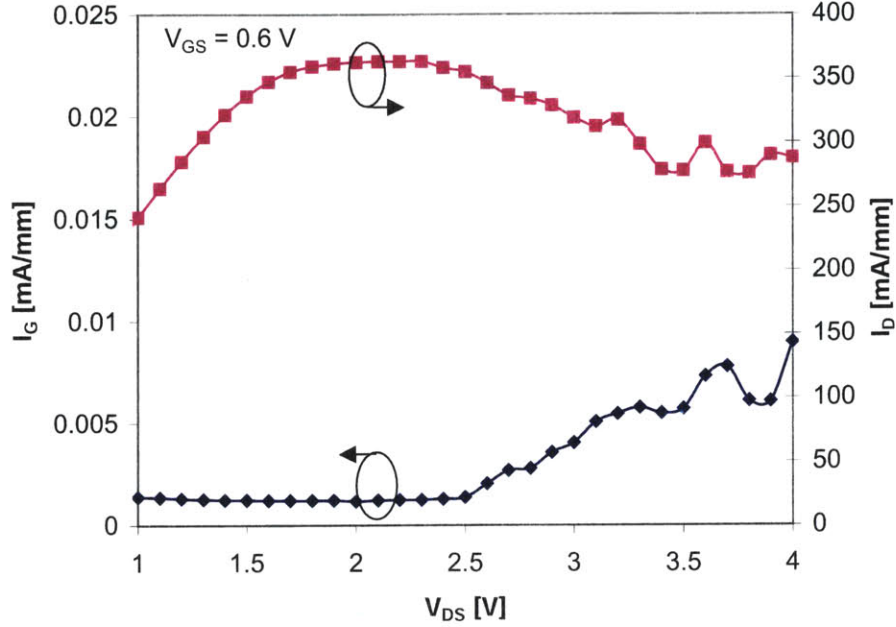
Fig. A-4: I_G and I_D vs. V_{DS} for the L_{RD} = 2.2 um gate device at V_{GS} = 0.6 V.

iii. Large Signal Measurements

We now extend our large signal analysis to the 600 um (6 fingers X 100 um) buried WSi gate PHEMTs with three different L_{RD} (0.6, 1.4, 2.2 um). The devices were tuned for peak PAE at the 3-dB compression point without any restriction on the small signal gain at various drain voltages and I_D = 100 mA/mm. We have performed load-pull measurements at 8, 12, and 16 GHz.

a. Across L_{RD}

At 8 GHz, the gain of the L_{RD} = 0.6 um compresses later than the L_{RD} = 1.4 and 2.2 um devices and the PAE of the L_{RD} = 0.6 and 1.4 um devices approach 60% (Fig. A-5). Although the small signal gains of the devices are different, the longer L_{RD} is, the sooner the device compresses at 12 GHz (Fig. A-6). In addition, the PAE at the 3-dB compression decreases slightly as L_{RD} is increased. At 16 GHz, $P_{OUT,3\text{-}dB}$ is virtually the same for all three devices at 21.9 dBm (Fig. A-7).

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Likewise, the PAE at the 3-dB compression for the three devices are practically identical. At the three frequencies examined, it is difficult to observe trends across L_{RD} simply by analyzing the gain compression and PAE behavior at this particular drain voltage.
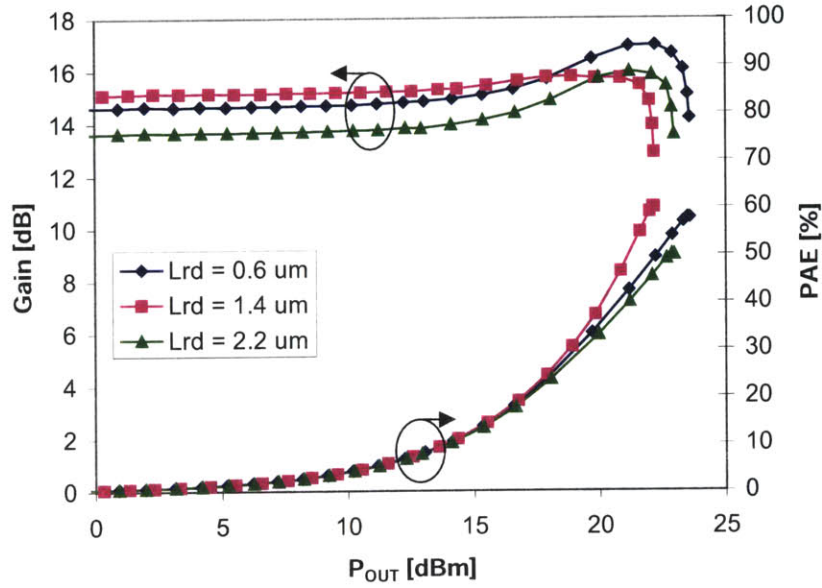
Fig. A-5: Gain and PAE versus P_{OUT} for devices with varying L_{RD} at 8 GHz and $V_{DS} = 4$ V, $I_D = 100$ mA/mm.
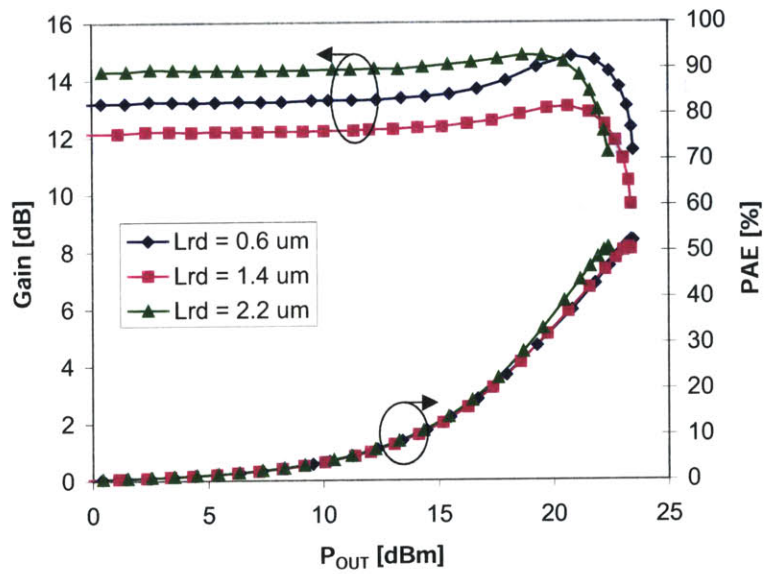
Fig. A-6: Gain and PAE versus P_{OUT} for devices with varying L_{RD} at 12 GHz and $V_{DS} = 4$ V, $I_D = 100$ mA/mm.
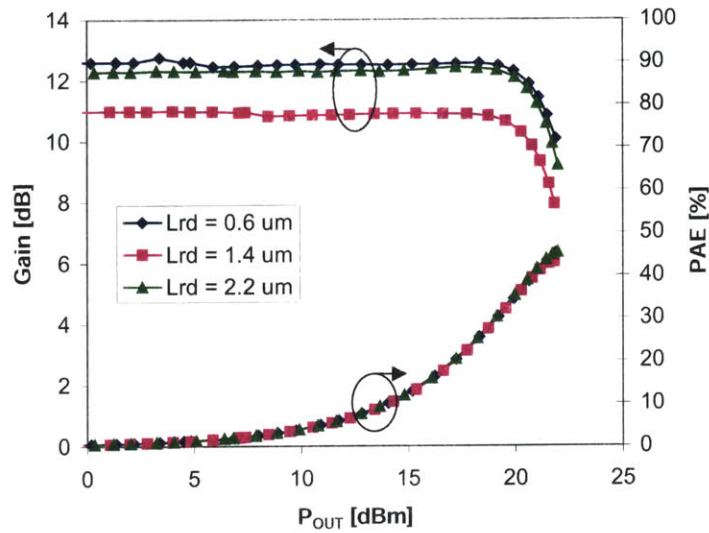
Fig. A-7: Gain and PAE versus P_{OUT} for devices with varying L_{RD} at 16 GHz and V_{DS} = 4 V, I_D = 100 mA/mm.

If we consider the RF induced I_G and I_D, the three different L_{RD} devices all experience a large degree of I_G as the devices are driven into compression. Similar to the biasing behavior of the Al gate devices, the longer L_{RD} devices experienced a sharp increase in I_G at 8 GHz (Fig. A-8). The L_{RD} = 1.4 um devices has a much smaller degree of self-biasing as compared to the other devices, which may possibly be attributed to the selection of non-optimal impedances due to a poor optimization (Fig. A-8). At 12 GHz, only the L_{RD} = 0.6 and 1.4 um devices experience a large increase in I_G while the I_G of the L_{RD} = 2.2 device barely increases at compression (Fig. A-9). In addition, the amount of self-bias goes up the smaller L_{RD} becomes, which is behavior that is also characteristic of the Al gate devices. Lastly, at 16 GHz, there is no significant increase in I_G for any of the devices as they enter compression and the amount of self-bias is reduced from the levels seen at 8 and 12 GHz (Fig. A-10).

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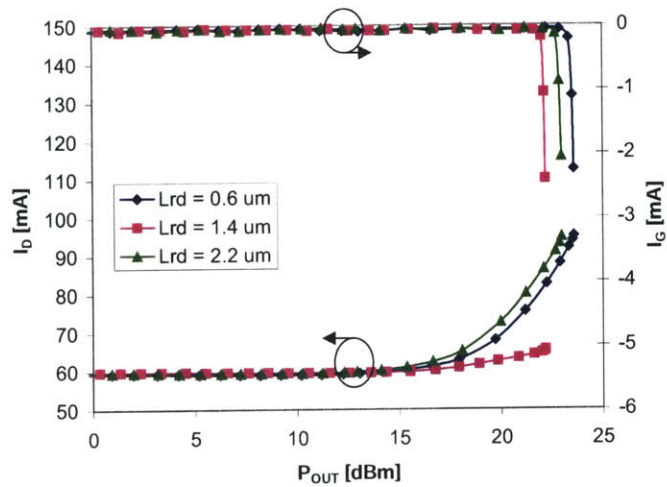
Fig. A-8: I_D and I_G versus P_{OUT} for devices with varying L_{RD} at 8 GHz and V_{DS} = 4 V.
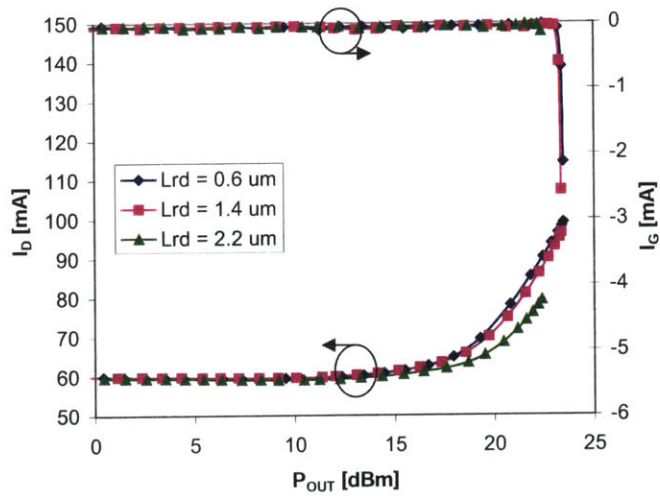
Fig. A-9: I_D and I_G versus P_{OUT} for devices with varying L_{RD} at 12 GHz and V_{DS} = 4 V.
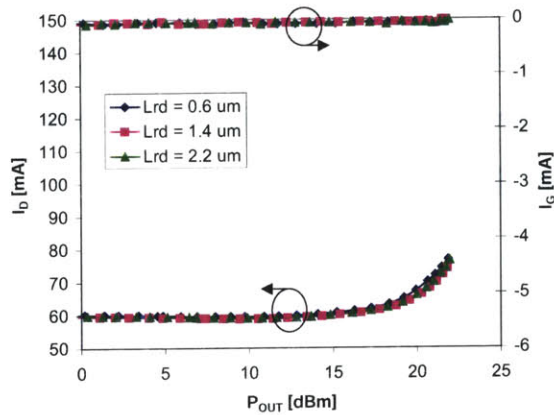
Fig. A-10: I_D and I_G versus P_{OUT} for devices with varying L_{RD} at 16 GHz and V_{DS} = 4 V.
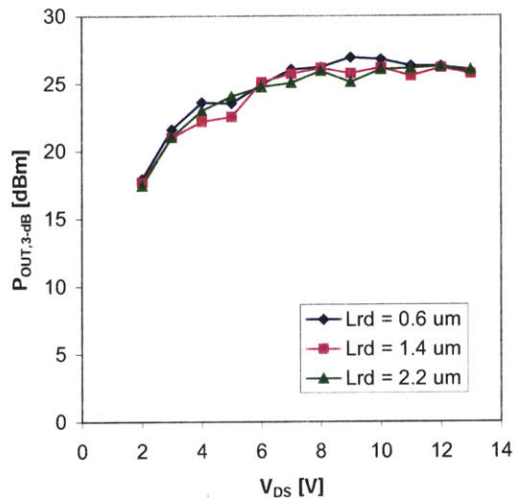
Fig. A-11: $P_{OUT,3\text{-dB}}$ versus V_{DS} for different L_{RD} devices at 8 GHz and I_D = 100 mA/mm.
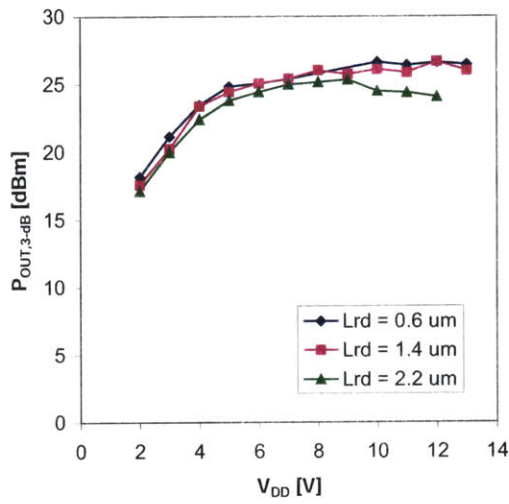
Fig. A-12: $P_{OUT,3\text{-dB}}$ versus V_{DD} for different L_{RD} devices at 12 GHz and I_D = 100 mA/mm.
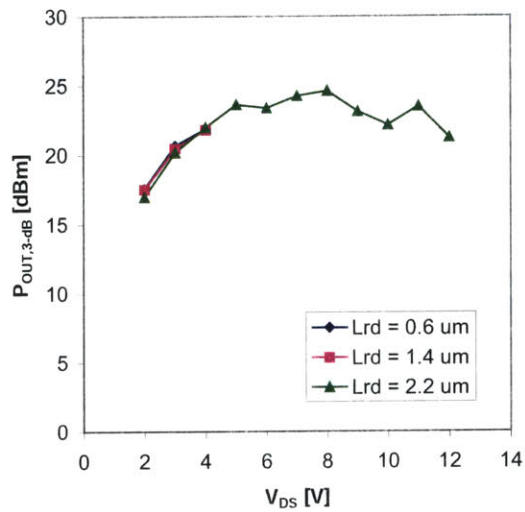
Fig. A-13: $P_{OUT,3\text{-dB}}$ versus V_{DD} for different L_{RD} devices at 16 GHz and I_D = 100 mA/mm.

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b. Across V_{DS}

In this section, we will compare the gain, PAE, and RF induced currents of the shortest L_{RD} (0.6 um) and longest L_{RD} (2.2 um) buried WSi gate PHEMT. For the characteristics shown for the L_{RD} = 0.6 um device at V_{DS} = 6 and 8 V and 8 GHz, the large jump in gain and PAE may indicate RF induced oscillations. Beyond V_{DS} = 4 V, the PAE at the 3-dB compression point drops off sharply (Fig. A-14). Similar behavior is also observed for the L_{RD} = 2.2 um device; the compression behavior varies dramatically depending on V_{DS} (Fig. A-15). At 12 GHz, the power sweeps at V_{DS} = 10 and 12 V for the L_{RD} = 0.6 um device are limited by their sudden increase in positive gate current (Fig. A-16). For the L_{RD} = 2.2 GHz device at 12 GHz, gain compression actually occurs earlier at V_{DS} = 10 and 12 V than it does at V_{DS} = 8 V (Fig. A-17). Under these conditions, these devices are also accompanied by a sharp increase in positive I_G, which we shall show later on in the section. We only have the gain and PAE characteristics for the L_{RD} = 0.6 um device at 16 GHz and they appear normal (Fig. A-18). For the L_{RD} = 2.2 um device at 16 GHz, gain compression actually occurs earlier when the device is biased beyond V_{DS} = 8 V (Fig. A-19).
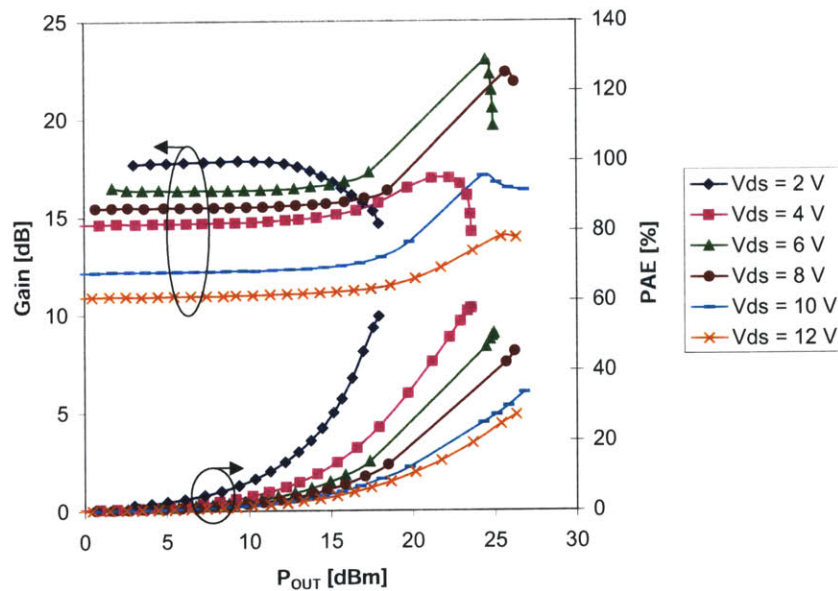
Fig. A-14: Gain and PAE versus P_{OUT} for device with L_{RD} = 0.6 um for varying V_{DS} and I_D = 100 mA/mm at 8 GHz.

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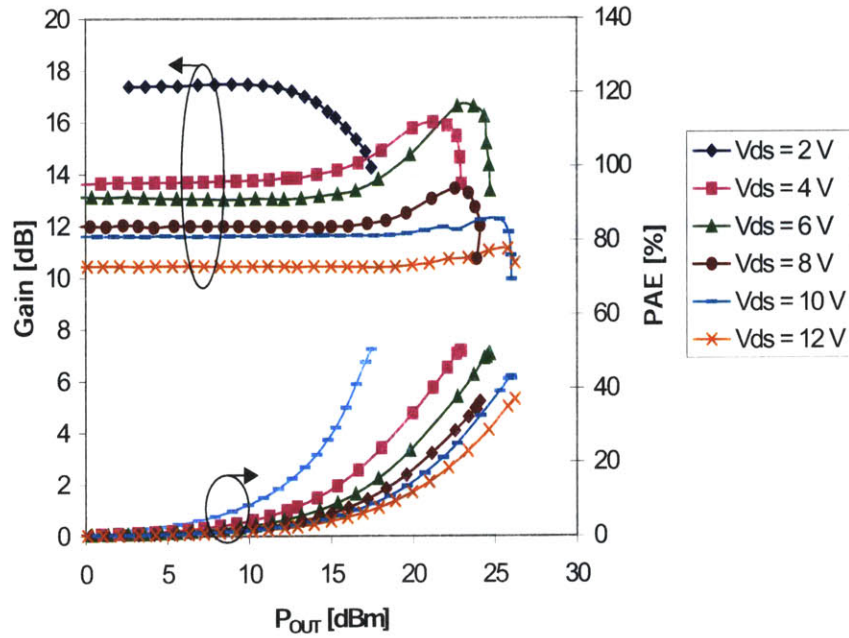
Fig. A-15: Gain and PAE versus P_{OUT} for device with L_{RD} = 2.2 um for varying V_{DS} and I_D = 100 mA/mm at 8 GHz.
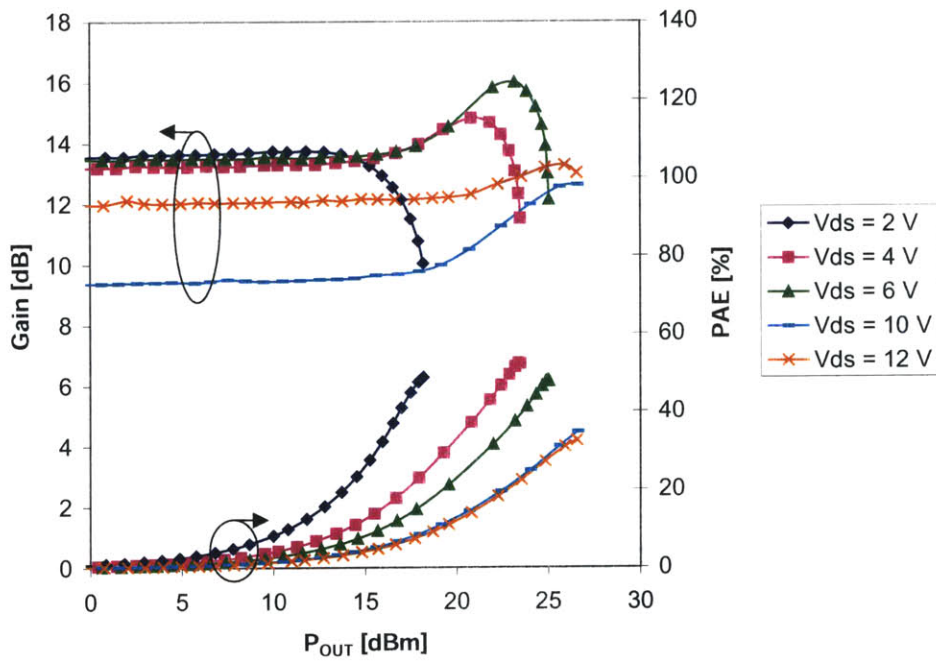
Fig. A-16: Gain and PAE versus P_{OUT} for device with L_{RD} = 0.6 um for varying V_{DS} and I_D = 100 mA/mm at 12 GHz.
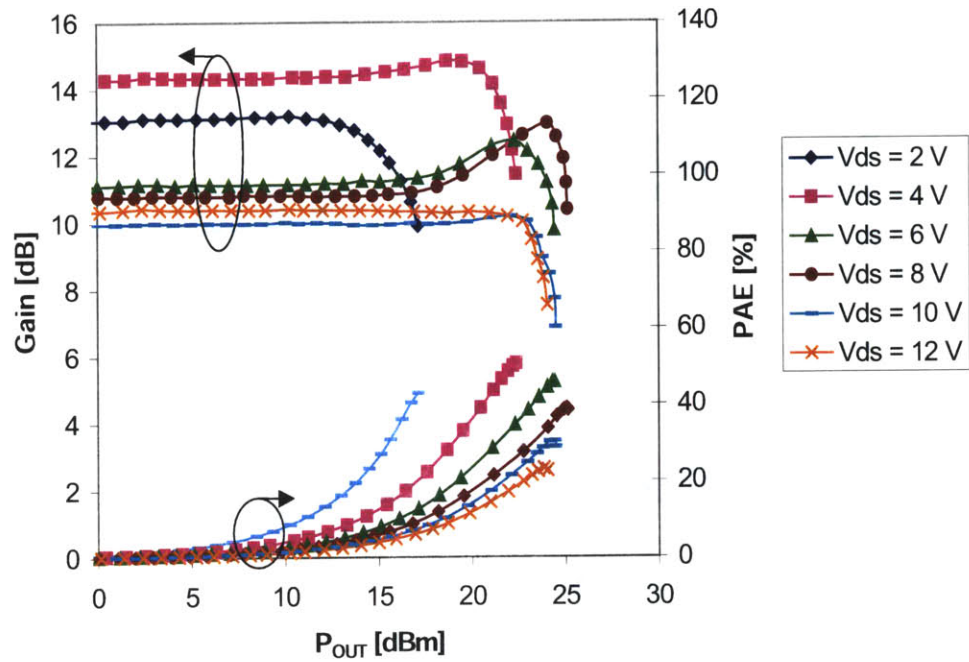
Fig. A-17: Gain and PAE versus P_{OUT} for device with L_{RD} = 2.2 um for varying V_{DS} and I_D = 100 mA/mm at 12 GHz.
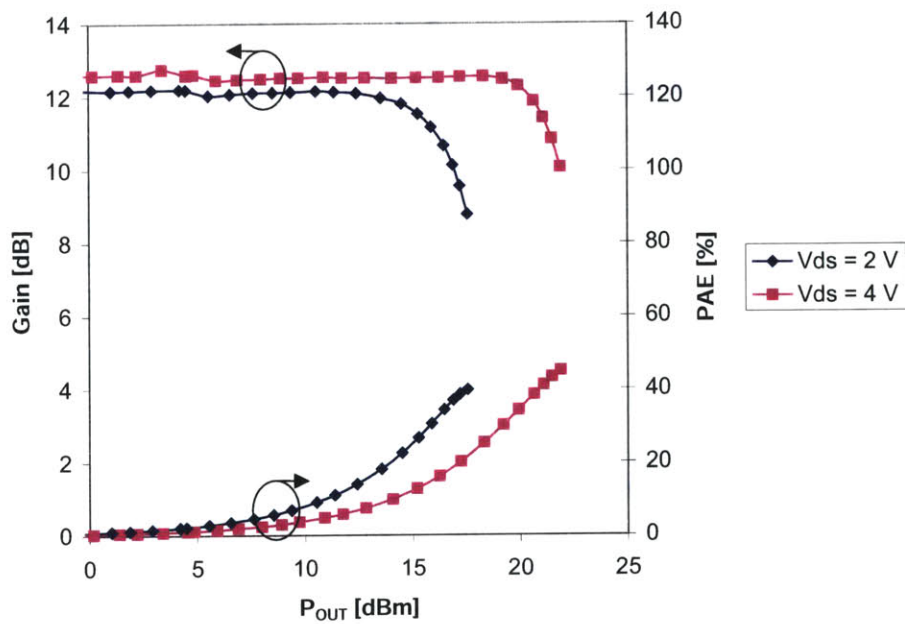
Fig. A-18: Gain and PAE versus P_{OUT} for device with L_{RD} = 0.6 um for varying V_{DS} and I_D = 100 mA/mm at 16 GHz.
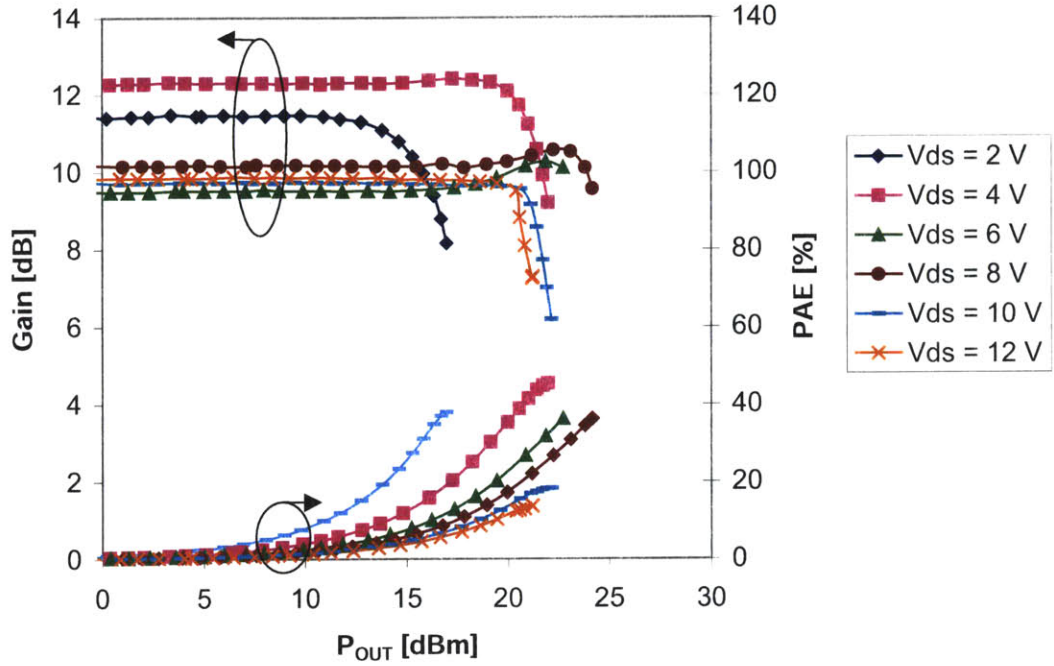
Fig. A-19: Gain and PAE versus P_{OUT} for device with L_{RD} = 2.2 um for varying V_{DS} and I_D = 100 mA/mm at 16 GHz.
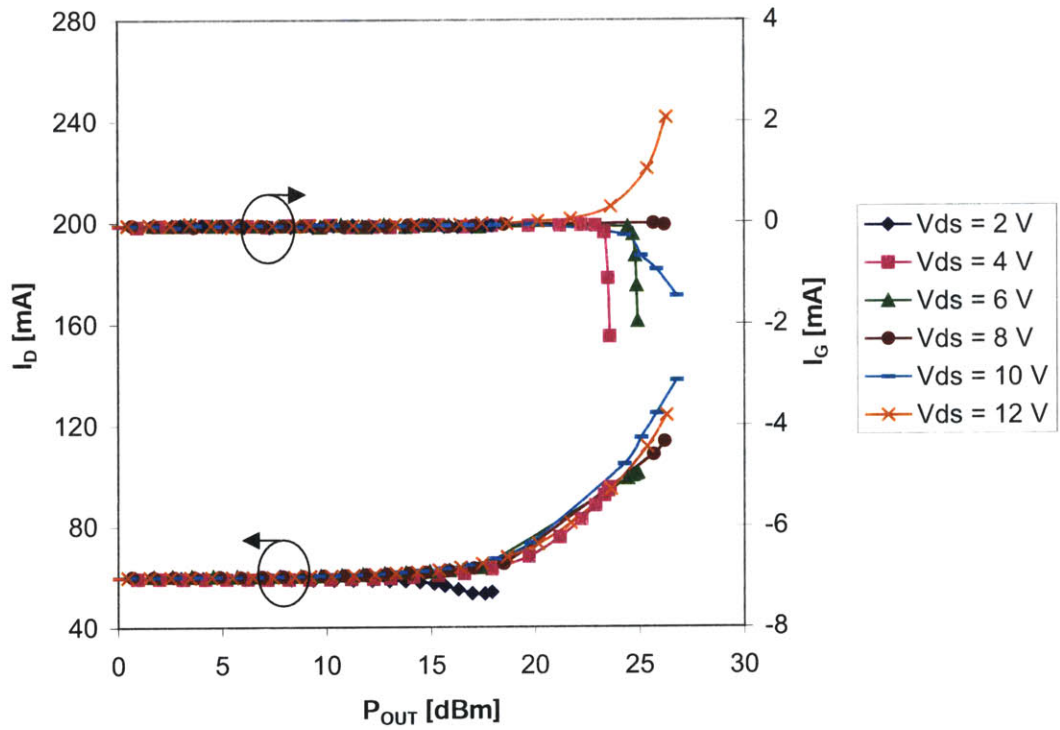
Fig. A-20: Drain and gate current versus P_{OUT} for device with L_{RD} = 0.6 um for varying V_{DS} and I_D = 100 mA/mm at 8 GHz. The resolution of the gate current is 1 mA.

At 8 GHz, the L_{RD} = 0.6 um device experiences a higher degree of self-bias than the L_{RD} = 2.2 um device across V_{DS} (Figs. A-20 to A-21). At V_{DS} = 12 V, I_G initially turns positive and then becomes sharply negative at compression. The initial upswing in positive I_G is observed for the L_{RD} = 2.2 um device at V_{DS} = 8, 10, and 12 V appears to accompany reduced self-bias as compared to the performance at V_{DS} = 6 V (Fig. A-21). At 12 GHz, positive I_G is observed at V_{DS} = 10 and 12 V for the L_{RD} = 0.6 um device (Fig. A-22) and V_{DS} = 6 – 12 V for the L_{RD} = 2.2 um device (Fig. A-23).

Again, reduced self-bias is observed for the L_{RD} = 2.2 um device when compared the L_{RD} = 0.6 um device at 12 GHz. At 16 GHz, there is no fluctuation in I_G and only a slight amount of self-bias for the L_{RD} = 0.6 um device (Fig. A-24). However, for the L_{RD} = 2.2 um device, I_G turns sharply positive and stays positive at higher V_{DS} at 16 GHz (Fig. A-25).
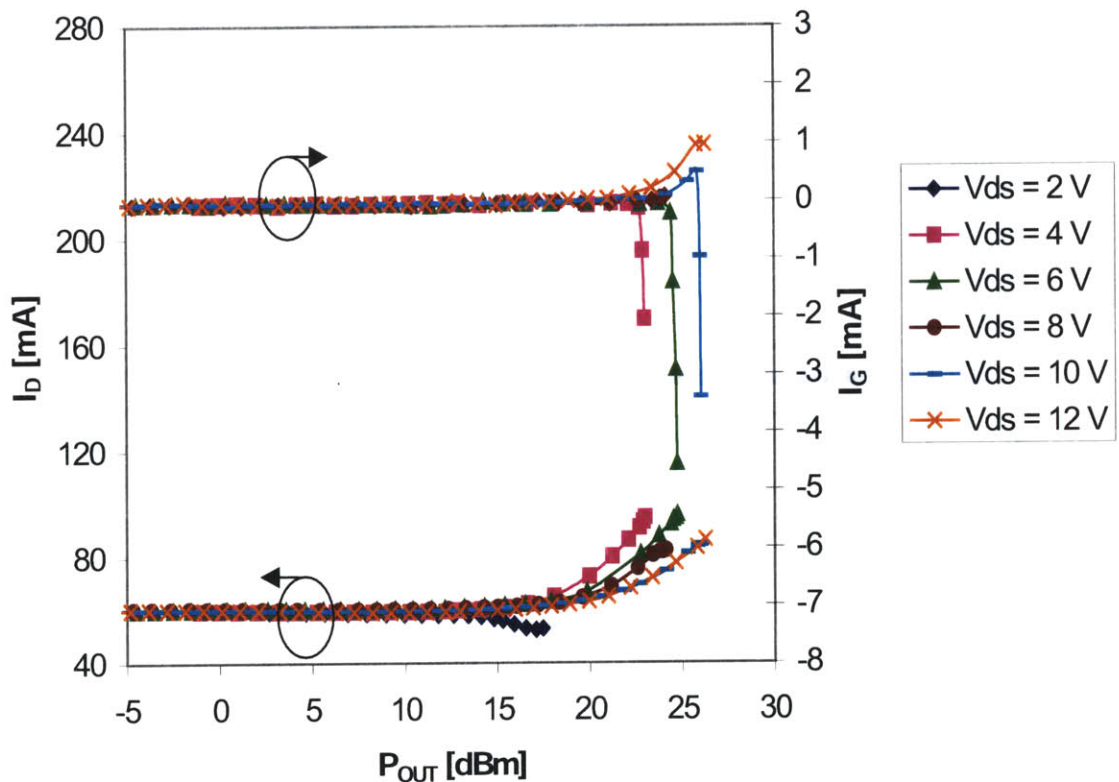
Fig. A-21: Drain and gate current versus P_{OUT} for device with L_{RD} = 2.2 um for varying V_{DS} and I_D = 100 mA/mm at 8 GHz. The resolution of the gate current is 1 mA.

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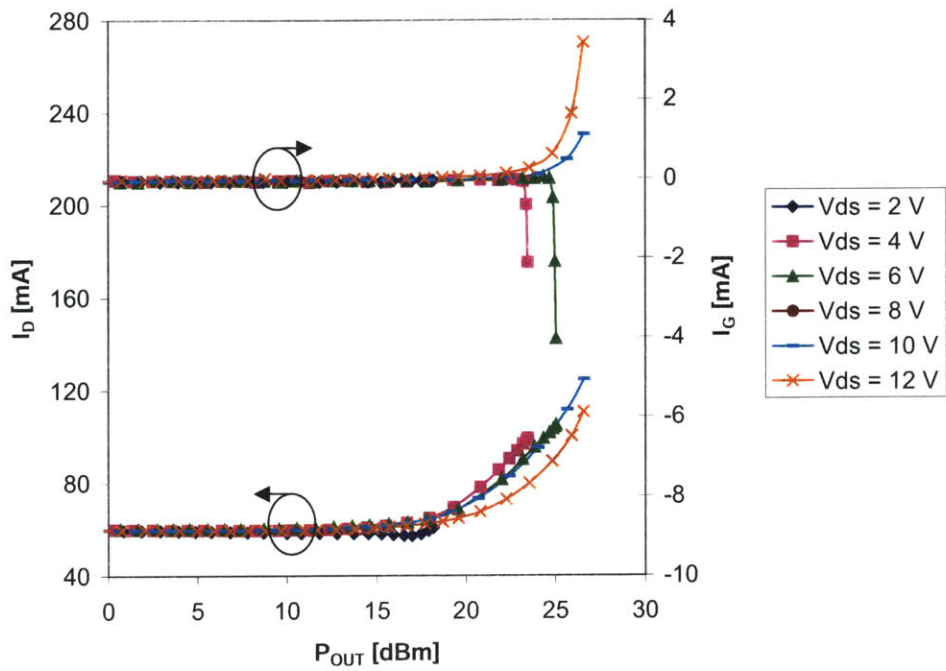
Fig. A-22: Drain and gate current versus P_{OUT} for device with L_{RD} = 0.6 um for varying V_{DS} and I_D = 100 mA/mm at 12 GHz. The resolution of the gate current is 1 mA.
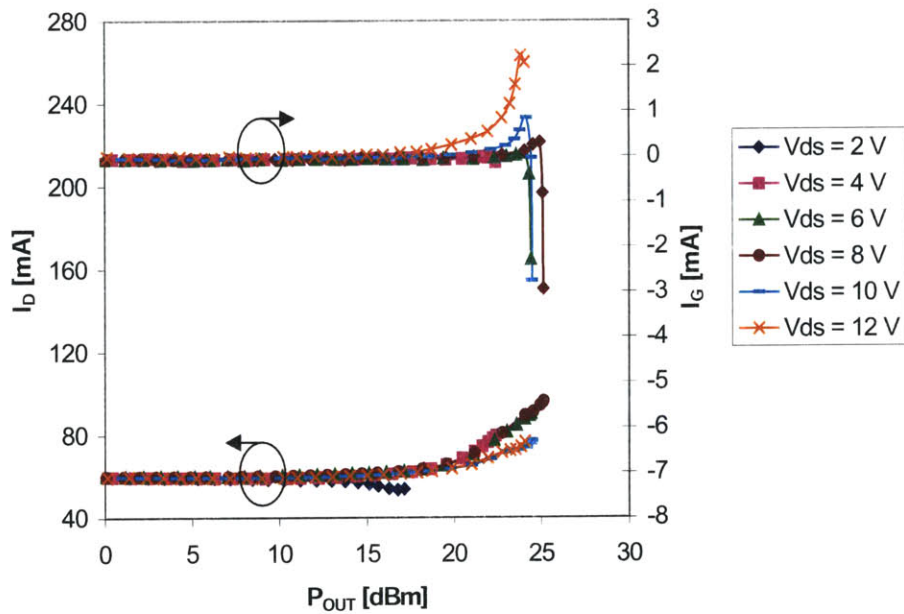
Fig. A-23: Drain and gate current versus P_{OUT} for device with L_{RD} = 2.2 um for varying V_{DS} and I_D = 100 mA/mm at 12 GHz. The resolution of the gate current is 1 mA.
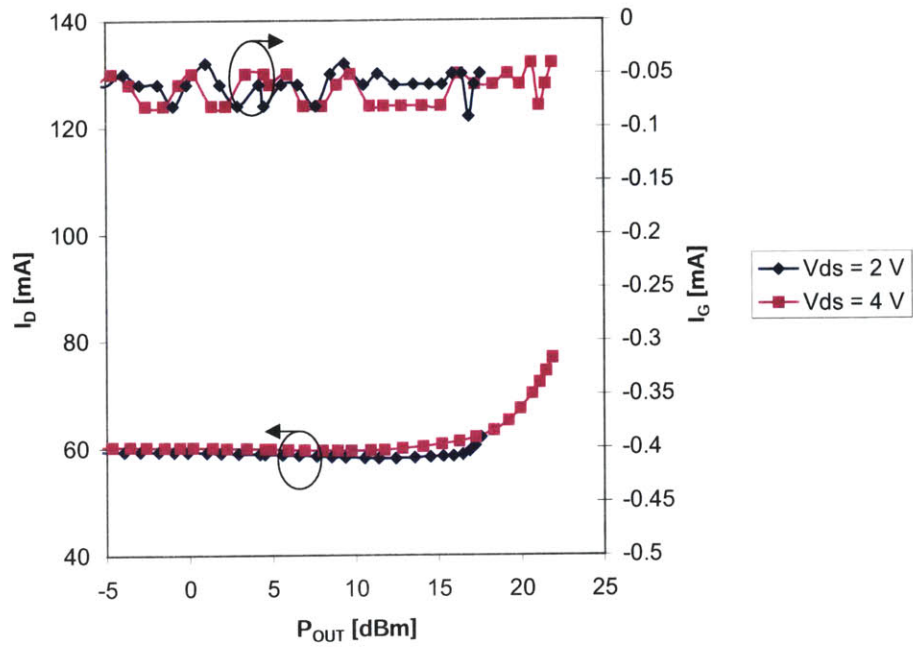
Fig. A-24: Drain and gate current versus P_{OUT} for device with $L_{RD} = 0.6$ um for varying V_{DS} and $I_D = 100$ mA/mm at 16 GHz. The resolution of the gate current is 1 mA.
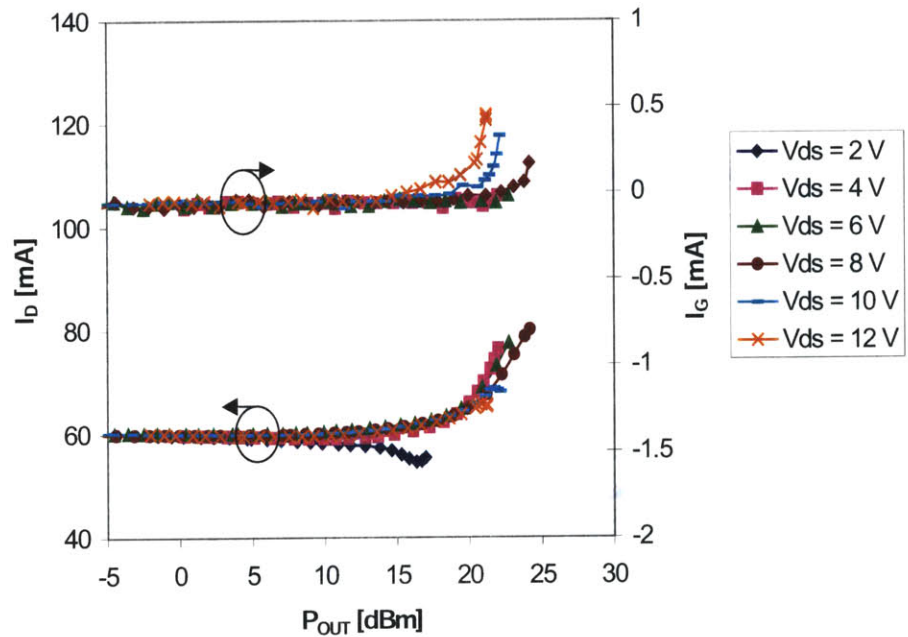
Fig. A-25: Drain and gate current versus P_{OUT} for device with $L_{RD} = 2.2$ um for varying V_{DS} and $I_D = 100$ mA/mm at 16 GHz. The resolution of the gate current is 1 mA.

c. Across Frequency

Unlike the Al gate devices, the buried WSi devices do not exhibit obviously different trends in $P_{OUT,3\text{-}dB}$ when measured up to 16 GHz (Fig. A-26). In order for the devices to manifest different trends with frequency, it is necessary to measure their large signal characteristics at higher frequencies and/or drain voltages. Due to the limitations of the measurement equipment, it was not possible to test under these conditions.
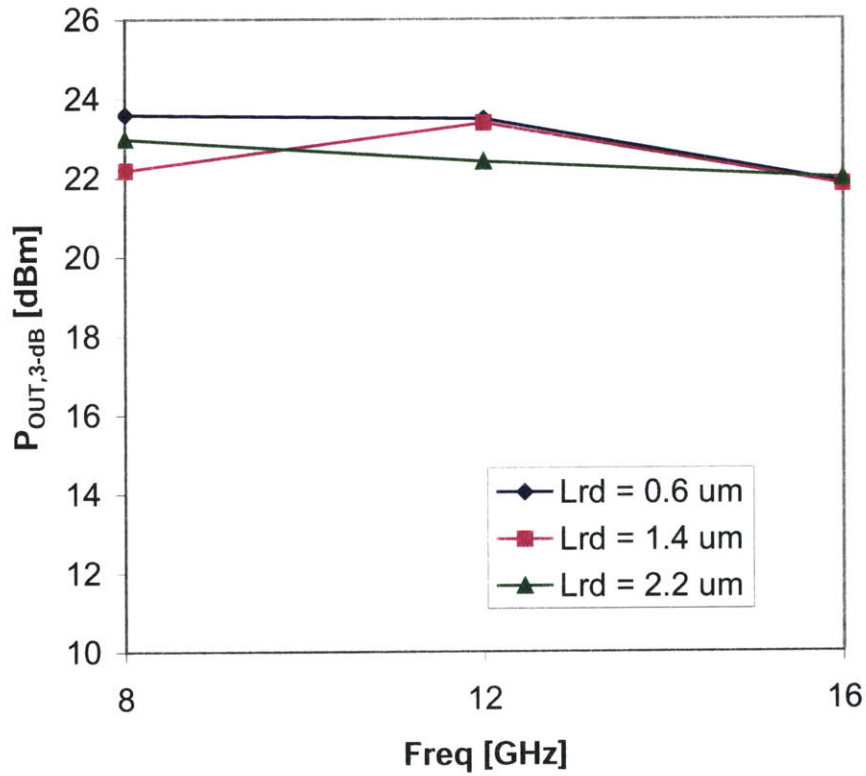
Fig. A-26: $P_{OUT,3\text{-}dB}$ versus frequency at small signal bias of V_{DS} = 4 V and I_D = 60 mA.

d. Reliability Study

Load pull measurements were performed with test plans that began at 2 V and ramped up to 13 V in 1 V increments. To track the degree of degradation at 8 GHz, verification measurements were performed at a benign V_{DS} = 2 V under the same conditions after each subsequent measurement at higher V_{DS}. A comparison of the V_{GS} required to maintain I_D = 60 mA at V_{DS} = 2 V reveals that all three devices experience slight shifts in V_T as a result of measurements taken at high V_{DS} (Fig. A-27). The degradation measurements reveal that the L_{RD} = 0.6 and 1.4 um devices are very robust; the $P_{OUT,3-dB}$, gain, and PAE barely fluctuate from their initial levels up to V_{DS} = 13 V. On the other hand, the L_{RD} = 2.2 um device degrades very rapidly with increasing drain voltage; $P_{OUT,3-dB}$ and the gain drop by 5 dBm and 5 dB, respectively, and PAE is reduced by about 40% as the drain voltage is increased to 13 V (Figs. A-28 to A-29). It is clear that the longest L_{RD} device is not as robust as the shorter L_{RD} devices.
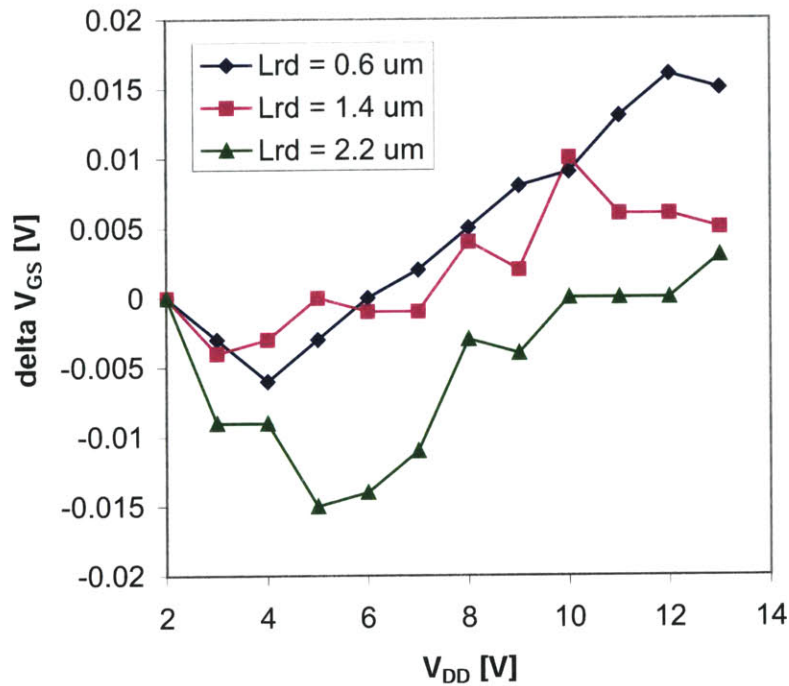
Fig. A-27: Difference between initial V_{GS} verification measurement at 2 V necessary to maintain I_D = 60 mA under smalls signal conditions and subsequent V_{GS} measurements at higher V_{DD}.

128
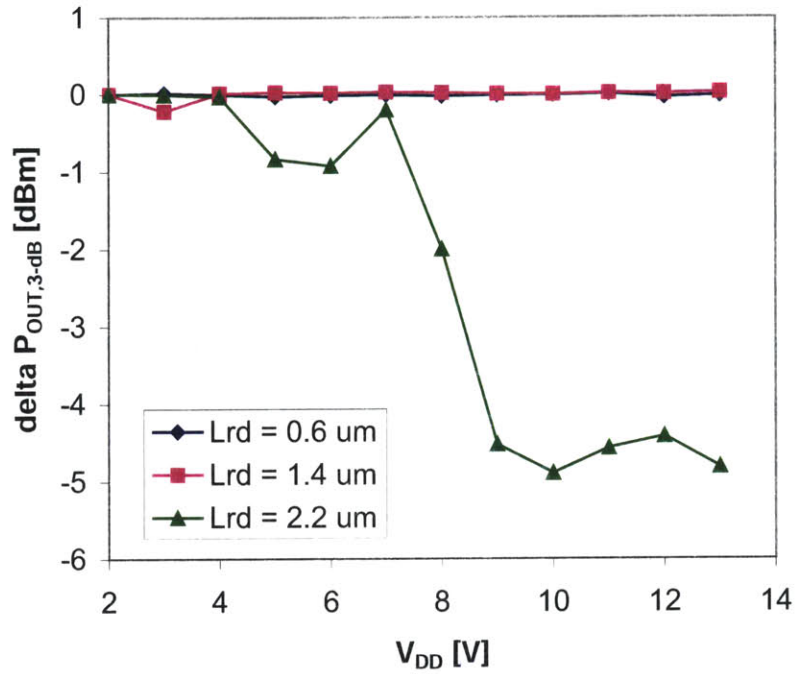
Fig. A-28: Difference between initial $P_{OUT,3-dB}$ verification measurement at 2 V and subsequent $P_{OUT,3-dB}$ measurements at higher V_{DD}.
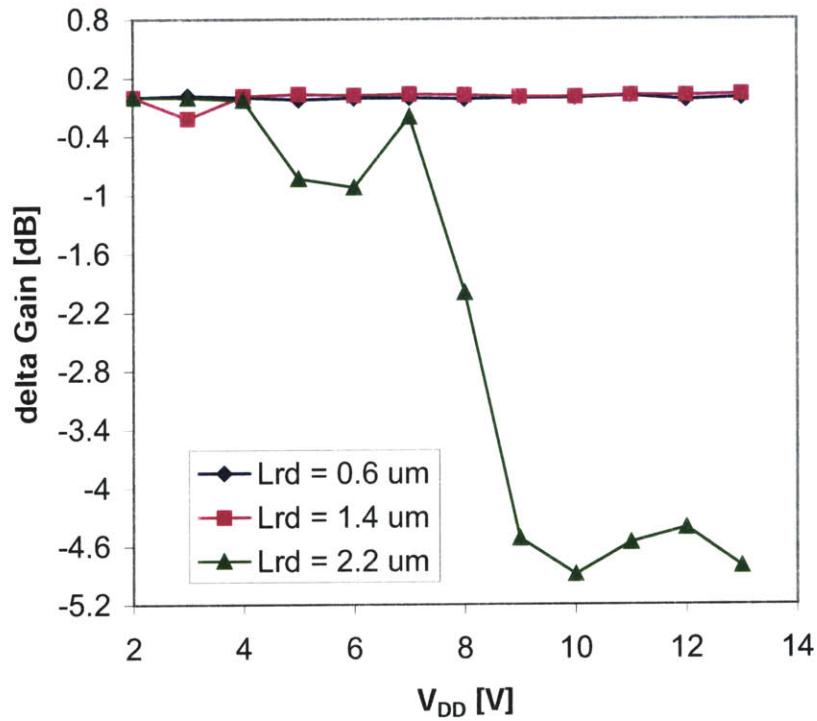
Fig. A-29: Difference between initial tranducer gain verification measurement at 2 V and subsequent gain measurements at higher V_{DD}.

iv. Load Line Analysis

Similar to the procedure described in section 5.2, we have carried out load line analysis for the L_{RD} = 0.6 and 2.2 um devices as a function of L_{RD} and V_{DS}. Using the optimized load impedance to extract R_L and the position of the load line, we can compare the different load lines at V_{DS} = 6 V, I_{D0} = 60 mA. In Figs. A-30 through A-32, the L_{RD} = 2.2 um clearly maintains a higher load resistance than the L_{RD} = 0.6 um device and is consequently unable to maximize the IV plane to achieve maximum power at 8, 12, and 16 GHz.

The evolution of the load lines with respect to drain bias is also similar to the results seen with the Al gate devices. At 12 GHz, the L_{RD} = 0.6 um device exhibits load lines that allow the bias point to be balanced between the forward and reverse conduction regions (Fig. A-33). On the other hand, the load lines for the L_{RD} = 2.2 um device show increasing R_L with increasing V_{DS} as they approach the NDR region in the output characteristics (Fig. A-34). The optimum load lines ended up positioning themselves to avoid the NDR region, which are known to exhibit high frequency instabilities.
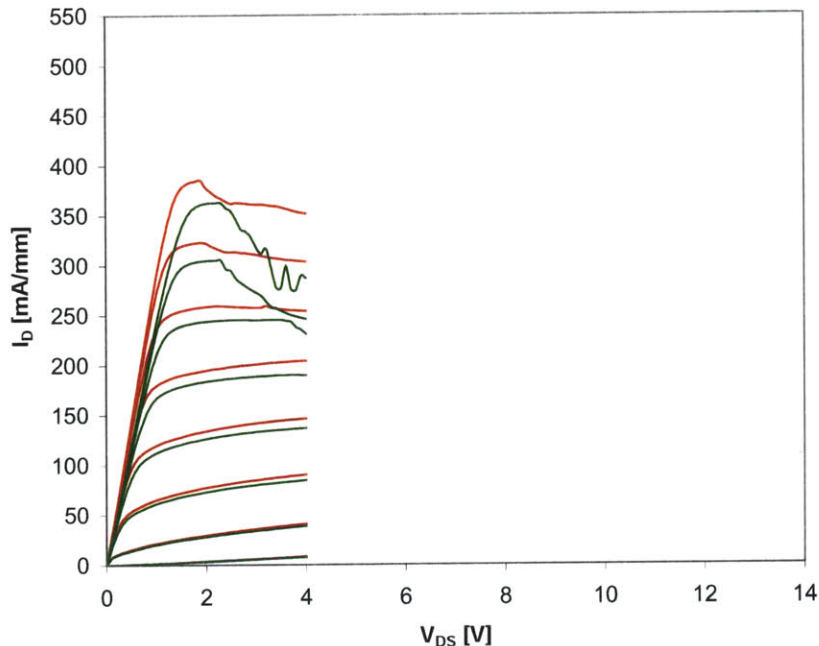
Fig. A-30: Load lines at 8 GHz and V_{DSQ} = 6 V and I_{D0} = 100 mA/mm.

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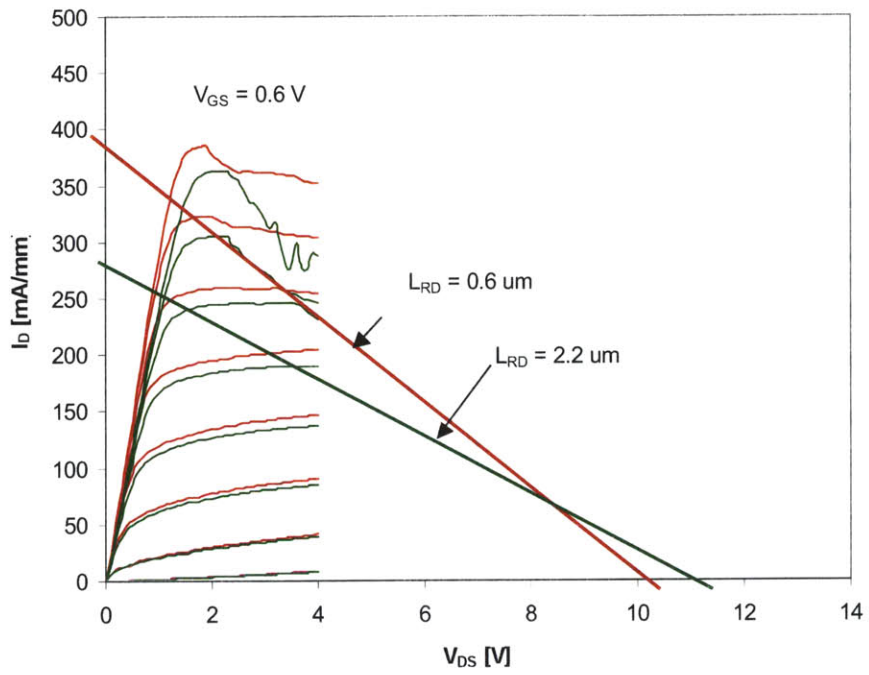
Fig. A-31: Load lines at 12 GHz and V_{DSQ} = 6 V and I_{D0} = 100 mA/mm.
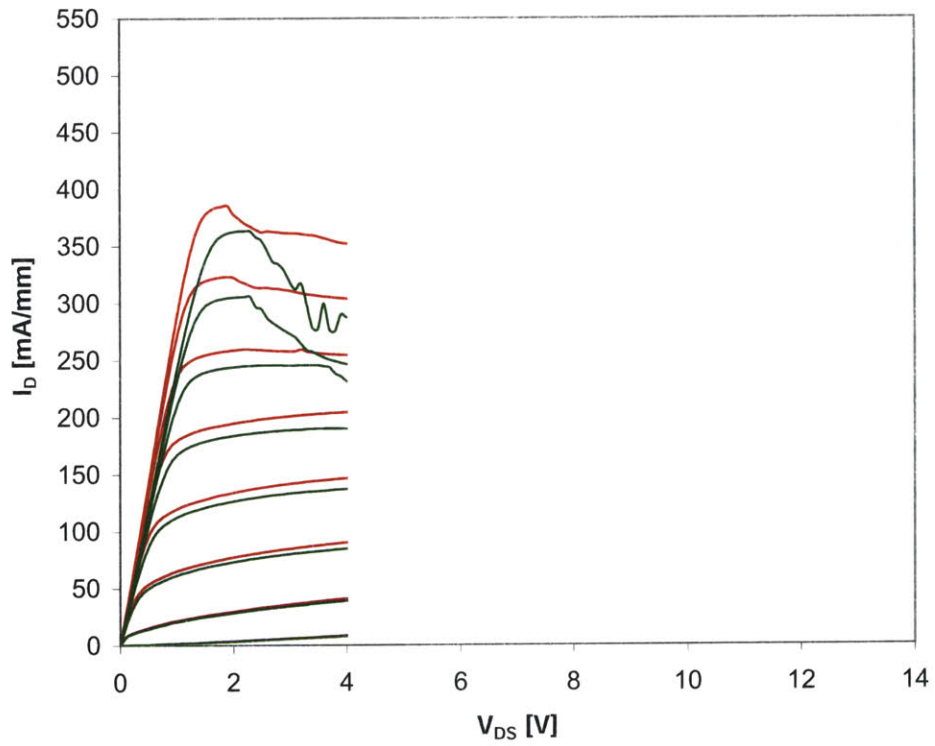
Fig. A-32: Load lines at 16 GHz and V_{DSQ} = 6 V and I_{D0} = 100 mA/mm.

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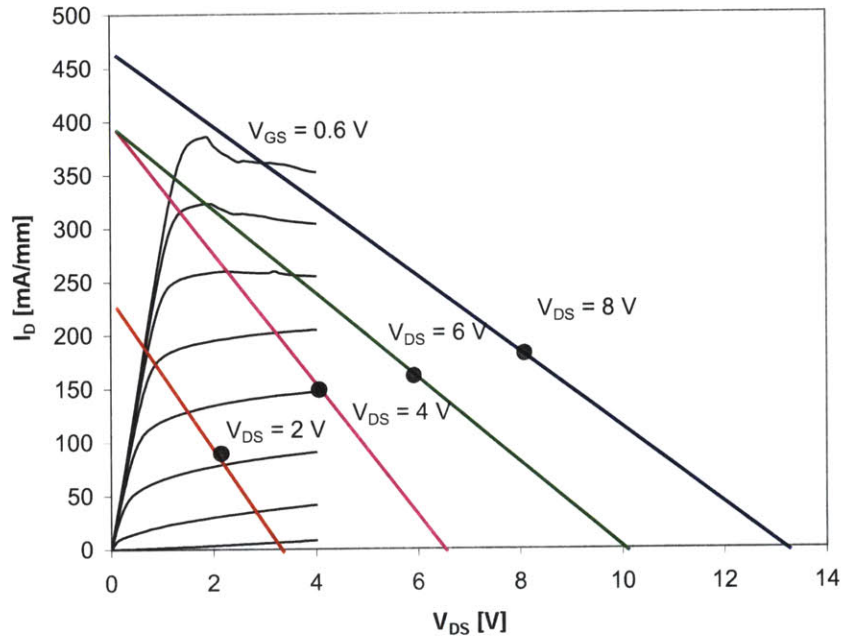
Fig. A-33: Load lines at 12 GHz and varying V_{DSQ} and I_{D0} = 100 mA/mm for the L_{RD} = 0.6 um device.
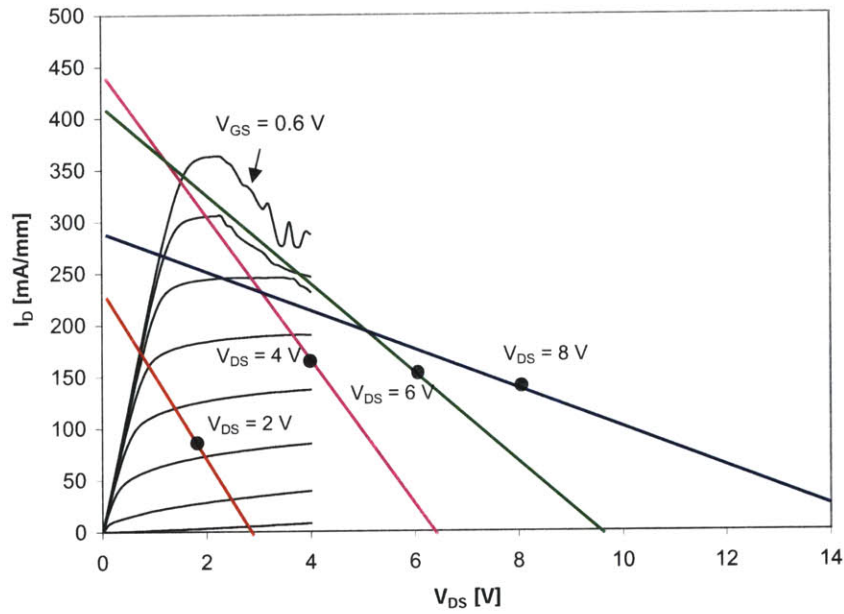
Fig. A-34: Load lines at 12 GHz and varying V_{DSQ} and I_{D0} = 100 mA/mm for the L_{RD} = 2.2 um device.

v. Conclusion

Due to their similar epitaxial structure, the Al gate and WSi gate PHEMTs bear many similarities. The presence of NDR in the output characteristics of the buried WSi PHEMT strengthens with increasing L_{RD}. The large signal measurements have shown that the longer L_{RD} is, the less $P_{OUT,3\text{-}dB}$ the device can deliver. Unfortunately, this could not be shown across a range of frequencies due to the limitations of the measurement setup. Verification measurements have shown that the L_{RD} = 2.2 um device is not as robust as the L_{RD} = 0.6 and 1.4 um devices as they undergo the load pull optimization procedure. We have also shown that the decrease in $P_{OUT,3\text{-}dB}$ is related to the position of the load lines. In general, for long L_{RD} devices, R_L is higher and the load lines appear to avoid the NDR region.

References

[1]   K. Hosogi, N. Nakano, H. Minami, T. Katoh, K. Nishitani, and M. Otsuo, "Photo/EB hybrid exposure process for T-shaped gate super low-noise HEMTs," *Electronics Letters*, vol. 27, pp. 2011-2012, 1991.

[2]   J. H. Lee, H. S. Yoon, C. S. Park, and H. M. Park, "Ultra low noise characteristics of AlGaAs/InGaAs/GaAs pseudomorphic HEMTs with wide head T-shaped gate," *IEEE Electron Device Letters*, vol. 16, pp. 271-273, 1995.

[3]   W. Marsetz, A. Hulsmann, T. Kleindienst, S. Fisher, M. Demmler, W. Bronner, T. Fink, K. Kohler, and M. Schlechtweg, "High Performance Double Recessed $Al_{0.2}Ga_{0.8}As/In_{0.25}Ga_{0.75}As$ PHEMTs for Microwave Power Applications," *27th European Microwave Conference and Exhibition*, vol. 2, pp. 1030-1034, 1997.

[4]   J. C. Huang, W. Boulais, A. Platzker, T. Kazior, L. Aucoin, S. Shanfield, A. Bertrand, M. Vafiades, and M. Niedzwiecki, "The Effect of Channel Dimensions on the Millimeter-Wave Performance of a Pseudomorphic HEMT," *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, pp. 177-180, 1993.

[5]   J. C. Huang, G. S. Jackson, S. Shanfield, A. Platzker, P. K. Saledas, and C. Weichert, "An AlGaAs/InGaAs pseudomorphic high electron mobility transistor with improved breakdown voltage for X- and Ku-band power applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, pp. 752-759, 1993.

[6]   T. Satoh, A. Betti-Berutto, C. Poledrelli, C. Khandavalli, J. Nikaido, S. Kuroda, T. Yokoyama, and J. Fukaya, "A 68% P.A.E. Power pHEMT for K-Band Satellite Communication System," *IEEE Transactions on Microwave Theory and Techniques*, vol. 3, pp. 963-966, 1999.

[7]   M. Zaknoune, M. Ardouin, Y. Cordier, S. Bollaert, B. Bonte, and D. Theron, "60-GHz High Power Performance $In_{0.35}Al_{0.65}As-In_{0.35}Ga_{0.65}As$ Metamorphic HEMTs on GaAs," *IEEE Electron Device Letters*, vol. 24, pp. 724-726, 2003.

[8]   A. Inoue. Cambridge, MA, 2004.

[9]   J. Laskar, A. A. Ketterson, J. N. Baillargeon, T. Brock, I. Adesida, K. Y. Cheng, and J. Kolodzey, "Gate-Controlled Negative Differential Resistance in Drain Current Characteristics of AlGaAs/InGaAs/GaAs Pseudomorphic MODFET's," *IEEE Electron Device Letters*, vol. 10, pp. 528-530, 1989.

[10]   K. Y. Hur, R. A. McTaggart, P. J. Lemonias, and W. E. Hoke, "Development of Double Recessed AlInAs/GaInAs/InP HEMTs for Millimeter Wave Power Applications," *Solid-State Electronics*, vol. 41, pp. 1581-1585, 1996.

[11]   J. C. Huang, P. K. Saledas, J. Wendler, A. Platzker, W. Boulais, S. Shanfield, B. Hoke, and P. Lyman, "A Double-Recessed AlGaAs/InGaAs Pseudomorphic HEMT for Ka- and Q-Band Power Applications," *IEEE Electron Device Letters*, vol. 14, pp. 456-458, 1993.

[12]   D. Teeter, C. Whelan, A. Platzker, S. Bouthillette, S. Nash, G. Chu, B. Hoke, P. Marsh, and T. Kazior, "Recent Advances in High Efficiency PHEMT Devices and Power Amplifiers," presented at Compound Semiconductor Power Transistors II and State-of-the-Art Program on Compound Semiconductors XXXII, Toronto, Canada, 2000.

[13]   P. R. de la Houssaye, D. R. Allee, Y. Pao, D. G. Schlom, J. S. Harris, and R. F. W. Pease, "Electron saturation velocity variation in InGaAs and GaAs channel MODFETs for gate length to 550 A," *IEEE Electron Device Letters*, vol. 9, pp. 148-150, 1988.

[14]   D. H. Zhang, "Metal Contacts to n-type AlGaAs grown by molecular beam epitaxy," *Materials Science and Engineering B (Solid-State Materials for Advanced Technology)*, vol. B60, pp. 189-93, 1999.

[15]   L. D. Nguyen, P. J. Tasker, and W. J. Schaff, "Comments on 'A new low-noise AlGaAs/GaAs 2DEG FET with surface undoped layer,'" *IEEE Transactions on Electron Devices*, vol. 34, pp. 1187, 1987.

[16]   B. Hughes and P. J. Tasker, "Bias Dependence of the MODFET Intrinsic Model Elements Values at Microwave Frequencies," *IEEE Transactions on Electron Devices*, vol. 36, pp. 2267-2273, 1989.

[17] T. Suemitsu, "An Intrinsic Delay Extraction Method for Schottky Gate Field Effect Transistors," *IEEE Electron Device Letters*, vol. 25, pp. 669-671, 2004.

[18] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, pp. 1151-1159, 1988.

[19] A. Caddemi, N. Donato, and G. Crupi, "A robust approach for the direct extraction of HEMT circuit elements vs. bias and temperature," presented at 6th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Service, 2003.

[20] P. M. White and R. M. Healy, "Improved Equivalent Circuit for Determination of MESFET and HEMT Parasitic Capacitances from "Coldfet" Measurements," *IEEE Microwave and Guided Wave Letters*, vol. 3, 1993.

[21] N. Moll, M. R. Hueschen, and A. Fischer-Colbrie, "Pulse-Doped AlGaAs/InGaAs Pseudomorphic MODFET's," *IEEE Transactions on Electron Devices*, vol. 35, pp. 879-887, 1988.

[22] S. C. Cripps, *RF power amplifiers for wireless communications*: Artech House, 1999.

[23] T. A. Winslow and R. J. Trew, "Principles of large-signal MESFET operation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, pp. 935-942, 1994.

[24] R. Vetury, Y.-F. Wu, P. T. Fini, G. Parish, S. Keller, S. DenBaars, and U. K. Mishra, "Direct measurement of gate depletion in high breakdown (405 V) AlGaN/GaN heterstructure field effect transistors," presented at IEDM '98 Technical Digest, International Electron Devices Meeting, San Francisco, CA, 1998.

[25] B. Green, V. Tilak, V. Kaper, J. Smart, J. R. Shealy, and L. F. Eastman, "Microwave Power Limits of AlGaN/GaN HEMTs Under Pulsed-Bias Conditions," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, pp. 618-623, 2003.

[26] D. G. Ballegeer, I. Adesida, C. Caneau, and R. Bhat, "Physics and behavior of asymmetrically recessed InP-based MODFET's fabricated with an electron beam resist process," presented at Sixth International Conference on Indium Phosphide and Related Materials, Santa Barbara, CA, 1994.

[27] C. S. Wu, C.-K. Pao, W. Yau, H. Kanber, M. Hu, S. X. Bar, A. Kurdoghlian, Z. Bardai, D. Bosch, C. Seashore, and M. Gawronski, "Pseudomorphic HEMT Manufacturing Technology for Multifunctional Ka-Band MMIC Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, pp. 257-267, 1995.

[28] J. M. Lopez, T. Gonzalez, D. Pardo, S. Bollaert, T. Parenty, and A. Cappy, "Design optimization of AlInAs-GaInAs HEMTs for high-frequency applications," *IEEE Transactions on Electron Devices*, vol. 51, pp. 521-528, 2004.

[29] T. Suemitsu, K. Shiojima, T. Makimura, and N. Shigekawa, "Intrinsic Transit Delay and Effective Electron Velocity of AlGaN/GaN High Electron Mobility Transistors," *Japanese Journal of Applied Physics*, vol. 44, 2005.

[30] Y. W. Chen, W. C. Hsu, H. M. Shieh, Y. J. Chen, Y. S. Lin, Y. J. Li, and T. B. Wang, "High Breakdown Characteristic delta-doped InGaP/InGaAs/AlGaAs Tunneling Real-Space Transfer HEMT," *IEEE Transactions on Electron Devices*, vol. 49, pp. 221-225, 2002.

[31] Y. A. Tkachenko, Y. Lan, D. S. Whitefiled, C. J. Wei, J. C. M. Hwang, T. D. Harris, R. D. Grober, D. M. Hwang, L. Aucoin, and S. Shanfield, "Hot-electron-induced degradation of metal-semiconductor field-effect transistors," presented at GaAs IC Symposium, 1994.

[32] Y. K. Chen, D. C. Radulescu, G. W. Wang, F. E. Najjar, and L. F. Eastman, "Observation of High-Frequency High-Field Instability in GaAs/InGaAs/AlGaAs DH-MODFET's at K Band," *IEEE Electron Device Letters*, vol. 9, pp. 1-3, 1988.

[33] W. Kruppa and J. Boos, "Observation of DC and microwave negative differential resistance in InAlAs/InGaAs/InP HEMTs," *Electronics Letters*, vol. 28, pp. 267-269, 1992.

[34] J. Laskar, J. M. Bigelow, J. P. Leburton, and J. Kolodzey, "Experimental and theoretical investigation of the DC and high-frequency characteristics of the negative differential resistance in pseudomorphic AlGaAs/InGaAs/GaAs MODFET's," *IEEE Electron Device Letters*, vol. 39, pp. 257-263, 1992.

[35]   K. Fobelets, G. Borghs, and J. Hegarty, "Experimental drain current drop-back in GaAs MESFETs," *Electronics Letters*, vol. 31, pp. 2042-2044, 1995.

[36]   S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.

[37]   J. Huang, P. J. Tasker, G. W. Wang, Y. K. Chen, L. F. Eastman, O. A. Aina, H. Hier, and A. Fathimulla, "Kink effect in submicrometer-gate MBE-grown InAlAs/InGaAs/InAlAs heterojunction MESFETs," *IEEE Electron Device Letters*, vol. 9, pp. 630-632, 1988.

[38]   D. Frickey, "Conversions Between S, Z, Y, h, ABCD, and T Parameters which are Valid for Complex Source and Load Impedances," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, pp. 205-212, 1994.

[39]   G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. New Jersey: Prentice Hall, 1997.

[40]   M. H. Somerville, R. Blanchard, J. A. del Alamo, K. G. Duh, and P. C. Chao, "On-state breakdown in power HEMTs: measurements and modeling," *IEEE Transactions on Electron Devices*, vol. 46, pp. 1087-1093, 1999.

[41]   C. S. Putnam, M. H. Somerville, J. A. del Alamo, P. C. Chao, and K. G. Duh, "Temperature dependence of breakdown voltage in InAlAs/InGaAs HEMTS: Theory and experiments," presented at Proc. 7th Int. Conf. InP and Rel. Mat., 1997.

[42]   S. R. Bahl and J. A. del Alamo, "Breakdown voltage enhancement from channel quantization in InAlAs/n+ -InGaAs HFET's," *IEEE Electron Device Letters*, vol. 13, pp. 123-125, 1992.

[43]   H. Rohdin, C.-Y. Su, N. Moll, A. Wakita, A. Nagy, V. Robbins, and M. Kauffmana, "Semi-anlytical analysis for optimization of 0.1-um InGaAs-channel MODFETs with emphasis on on-state breakdown and reliability," presented at International Conference on Indium Phosphide and Related Materials, Cape Cod, MA, 1997.

[44]   C. P. Baylis and L. P. Dunleavy, "Understanding pulsed IV measurement waveforms," presented at 11th IEEE International Symposium on Electron Devices for Microwave and Optoelectronic Applications, 2003.

[45]   R. Vetury, N. Zhang, S. Keller, and U. K. Mishra, "The Impact of Surface States on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Electron Device Letters*, vol. 48, pp. 560-566, 2001.

[46]   R. Menozzi, M. Borgarino, K. Van der Zanden, and D. Schreurs, "On the Correlation Between Drain-Gate Breakdown Voltage and Hot-Electron Reliability in InP HEMT's," *IEEE Electron Device Letters*, vol. 20, 1999.

[47]   C. Lee, H. Tserng, L. Witkowski, P. Saunier, S. Guo, B. Albert, R. Birkhahn, and G. Munns, "Effects of RF stress on power and pulsed IV characteristics of AlGaN/GaN HEMTs with field-plate gates," *Electronics Letters*, vol. 40, pp. 1547-1548, 2004.

[48]   A. A. Villanueva, "Electrical Reliability of RF Power GaAs PHEMTs," in *Department of Electrical Engineering and Computer Science*. Cambridge: Massachusetts Institute of Technology, 2003, pp. 82.

[49]   R. Mosca, E. Gombia, A. Passaseo, V. Tasco, M. Peroni, and P. Romanini, "DLTS characterization of silicon nitride passivated AlGaN/GaN heterostructures," *Superlattices and Microstructures*, vol. 36, pp. 4-6, 2004.

[50]   H. Brech, T. Grave, and S. Selberherr, "Development of Global Calibration for Accurate GaAs-PHEMT Simulation," *IEEE Transactions on Electron Devices*, vol. 47, pp. 1957-1965, 2000.

[51]   H. Brech, T. Grave, T. Simlinger, and S. Selberherr, "Optimization of Pseudomorphic HEMT's Supported by Numerical Simulations," *IEEE Electron Device Letters*, vol. 44, pp. 1822-1828, 1997.

[52]   H. Brech, T. Grave, A. Werthof, H. J. Siweris, T. Simlinger, and S. Selberherr, "Influence of backside doping on the nonlinear capacitances of a PHEMT affects the VCO frequency characteristics," presented at 1997 IEEE International Symposium on Compound Semiconductors, San Diego, CA USA, 1997.

[53]   G. M. Dunn, A. Phillips, and P. J. Topham, "Current Instability in power HEMTs," *Semiconductor Science and Technology*, vol. 16, pp. 562-566, 2001.

[54]   S. Giugni and T. L. Tansley, "Comment on the compositional dependence of bandgap in AlGaAs and band-edge discontinuities in AlGaAs-GaAs heterostructures," *Semiconductor Science and Technology*, vol. 7, pp. 1113-1116, 1992.