PRODUCT STRATEGY IN RESPONSE TO TECHNOLOGICAL INNOVATION IN THE SEMICONDUCTOR TEST INDUSTRY

by

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Bachelor of Science in Mechanical Engineering
Massachusetts Institute of Technology, 2000
Submitted to the Sloan School of Management and the
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Partial Fulfillment of the Requirements for the Degrees of

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and
Master of Science in Management

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ABSTRACT

After the market boom of 2000 in the semiconductor industry changed significantly. The changes included stricter limits on capital cost spending, and the increased propensity of the industry to outsource the manufacturing of semiconductors. Thus, the semiconductor industry demanded greater cost of test economics in semiconductor test equipment. In response to the changes in the industry and the customer demands, the semiconductor test industry segmented itself into two broad strategies. Typically, the large semiconductor test equipment manufacturers employed a broad platform strategy, while the smaller semiconductor test equipment manufacturers employed a niche platform strategy.

This thesis confirms the underlying changes in the semiconductor test industry by looking at the entire semiconductor value chain. It also looks at the root causes of the changes in order to determine the future effects of the changes in the semiconductor test industry. This thesis also analyzes the two distinct market strategies, developing a systematic method to compare and evaluate each strategy. In addition, it explores the intangible risks associated with the adoption of each strategy. After understanding the trends in the semiconductor test industry, this thesis also presents a unified model to discuss the future direction of the semiconductor test industry. Looking at this direction, this project develops specific recommendations for businesses to compete effectively given the impending market conditions.

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Chapter 1: Project Background and Description

1.1 Background

The subject of the Leaders for Manufacturing (LFM) thesis is determined jointly from the sponsor company, Teradyne Incorporated located in Boston Massachusetts, and the LFM student. Much of the product and market information comes directly, or indirectly from the sponsor company.

1.2 History of Semiconductor Testing before the 1960s

The modern concept of building test equipment began in the early 1960s. At the time, Hewlett-Packard, General Radio, and Textronix dominated the testing business with a paradigm of measurement in the test industry. It consisted of viewing the test equipment as a measurement device.

This, in effect, was a true comment. The test equipment would generate a signal input to the semiconductor device. The test equipment would then measure the output. Then the test equipment would compare the measured output to the "expected" output for the semiconductor devices. If the signal measurements matched, the semiconductor device passed the test. If the measured output from the semiconductor did not match the "expected" output response, the semiconductor did not pass the test.

The business models that viewed the test equipment as a measurement device differed substantially than the later business models of viewing the test equipment as a piece of production equipment. However, the former view sparked the beginning of the semiconductor industry. The devices were extremely technologically challenging. The devices were also notoriously unreliable. The semiconductor designers did not always know where the failure would occur, so the test equipment measured almost every conceivable process that the semiconductor needed to accomplish. Because of the low volume requirements of the industry, the semiconductor industry demanded technological performance to measure the technologically challenging devices. It did not worry about the throughput speed of the test equipment. Even more, customers did not keep manufacturing performance metrics for the tester such as utilization or downtime because it viewed the test equipment as measurement equipment.

1.3 Changing the Test Strategy in the 1960s

As the semiconductor revolution progressed in the late 1960s, the diodes and transistors made from companies like Transitron began to build volume. The semiconductors came off the production line in the volume of thousands per hour. Manufacturers needed more throughput capacity in the test equipment. Therefore, the test equipment paradigm shifted from measurement to production equipment. In other words, in a high volume environment, the ideal tester would determine whether the chip was good or bad. In the process, it would make measurements, but hopefully, the measurements would be invisible to the operator. The shift in paradigm began the concept of the modern production tester.

As the product floor changed from low volume vacuum tubes to high volume semiconductors, the idea of the production tester continued to gain acceptance. The idea came from the belief that the true cost of production equipment lay, "not in the capital cost of the tester, but in the penalty paid for unreliable testing and in the 'down-time' required for calibration and maintenance."[62] Furthermore, as the semiconductors became increasingly complex, the tester innovated to keep up with the increasing performance of the semiconductor devices. From the sixties until the 1990s, the idea of utilization, downtime reduction, and technological performance drove the paradigm of production testing, and the development of test equipment in the semiconductor test industry.[1]

1.4 New Trends in the Semiconductor Test Industry

In the booming 1990s, the semiconductor test industry experienced large amounts of growth. The test equipment industry for semiconductors followed the same level of growth. However, the new millennium brought new challenges in the semiconductor test equipment industry.

Macroeconomic Conditions

As the economy went into recession, the semiconductor test industry also began to stumble. Figure 1.4.1 shows the average sales, gross profit, net income, and R&D spending for all the large semiconductor test equipment manufacturers. In the year 2000, the industry grew at a large percentage. The test industry understood that it could not continue at its rapid pace. However, it expected a slowdown in growth. In the years following 2000, the test industry experienced a free fall in sales, gross profit, and net income. By 2002, the customers of the test industry began to demand "a different type of test equipment".

[1] Van Veen writes a substantial history on Teradyne.

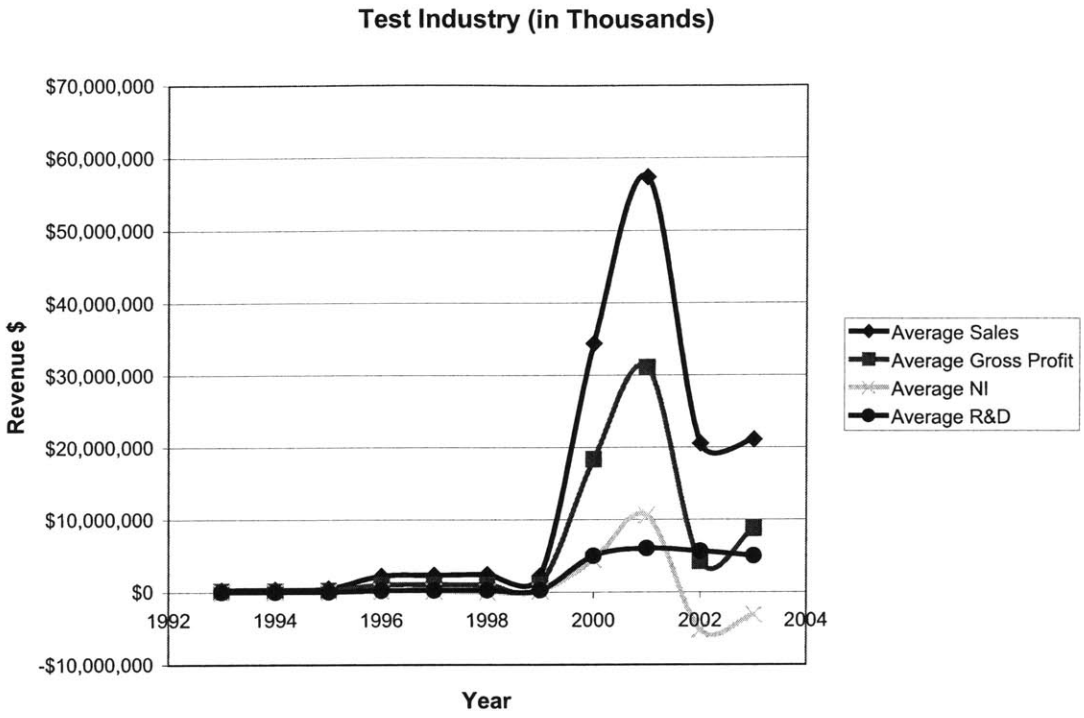


Figure 1.4.1 Financials of the Semiconductor Test Industry

Because of the drop in demand from the year 2000 to the present, most of the semiconductor manufacturers had lots of overcapacity in the manufacturing equipment, including test equipment. In looking for new test equipment purchases, the semiconductor manufacturers began to look for flexible semiconductor test equipment, rather than dedicated semiconductor test equipment. In addition to the traditional measure of utilization, throughput, and downtime, the semiconductor manufacturers wanted more capability of instruments to test multiple devices. The semiconductor manufacturers also wanted upgrade and downgrade capability. The customers of the test industry became wary of dedicated test equipment in the case of demand fluctuation as in the late 1990s to the early 2000s. In case of decrease demand, they wanted equipment that they can easily downgrade, or upgrade to test multiple families of devices rather than equipment that could only test one specific family of devices.

Capital Cost Limits

As the cost of equipment for semiconductor manufacturing increased, the customers of the semiconductor test equipment makers no longer simply relied on the traditional cost of test per device measurements in determining cost for semiconductor test equipment. In the past, semiconductor test equipment got bigger and faster. The semiconductor manufacturers measured the cost for the devices by the cost of test per device. Therefore, as long as the capital equipment costs resulted in throughput advances driving down the cost of test per device, the customers were happy.

Especially after the year 2000, the semiconductor industry began to face limitations on capital to purchase the expensive test equipment. This resulted in considerations of the absolute capital cost of the equipment in addition to the cost of test per semiconductor device.

Outsourcing Strategy
In the past much of the semiconductor test business came from the integrated device manufacturers (IDMs) such as Intel, Motorola, and Texas Instruments. These integrated device manufacturers bought a majority of the semiconductor test equipment. In addition, the IDM controlled the purchase of test equipment by the test and assembly contract manufacturers. For instance, the IDMs designed a semiconductor device. The IDMs also designed the test program using a specific tester. The semiconductor manufacturers outsource the testing of the devices to the subcontractors, dictating the type of tester for the subcontractors to purchase.

Especially with the contraction of free capital after the year 2000, the trend of outsourcing the testing of semiconductors increased. In addition, many companies developed business models on designing semiconductor devices, outsourcing both the fabrication of the chips, and the assembly and testing of the semiconductor devices. These companies possessed very limited capital equipment property, but a great deal of intellectual property.

As companies develop greater links and dependencies between the contract manufacturer, the foundries, and the semiconductor design firms, the power of the IDMs to dictate equipment purchases changed. This thesis analyzes these trends.

1.5 Vertical and Horizontal[2] Strategy Description

In response to the changes in the industry and the customer demands, the semiconductor test industry segmented itself into two broad strategies. Typically, the large semiconductor test equipment manufacturers employed a broad platform strategy, while the smaller semiconductor test equipment manufacturers employed a horizontal or niche platform strategy.

Horizontal Strategy
The semiconductor market encompasses a wide range of products. Each segment requires different test capabilities. Therefore, in theory, a purely horizontal strategy focuses different, independent test platform solutions targeting a specific segment of the market. For instance, many of the smaller semiconductor test equipment vendors focus on testing in the low-speed digital segment, offering better cost of test economics per device with less performance per pin. Looking at this generally, one can view the horizontal strategy as a niche strategy. The test equipment maker focuses its products on small, specific segments in order to better serve the customer in that segment.

[2] Until Chapter 4, the thesis uses the terms vertical, flexible, and broad almost synonymously. The thesis also uses the terms horizontal, focused, and niche almost synonymously.

Vertical Strategy

The wide range of products in the semiconductor test market ranges can be stacked into one large vertical column. The extremely complex semiconductor devices stack on the very top of the column, while the low complexity devices stack on the low end of the column. The vertical strategy offers one test equipment platform to test the entire column of semiconductor test products. The pure vertical strategy involves using a modular platform with upgrades and downgrades to fulfill test requirements in each market segment. Looking at it generally, one can view the vertical strategy similarly to the broad market strategies. The test equipment maker leverages the flexibility of the modular platform and standardization to beat the niche competition.

Market View

Agilent was the 1st mover in the vertical strategy for large ATE companies by developing the 93000 series tester in the late 1990s. Agilent advertised that "the Agilent 93000 SOC Series Solution gives you the ability to test your most complex devices with the highest throughput for the most economical price. Agilent's SOC Solution offers a true Single Scalable Platform that delivers uncompromising flexibility and scalability, ensuring the broadest application coverage at the lowest cost of test." [1] Corresponding to the introduction of the vertical strategy, Agilent began to display market strength. Therefore, many in the semiconductor industry attributed Agilent's market strength to it vertical strategy. Figure 1.5.1 shows the market share increase between Teradyne and Agilent. The right axis is the total ATE total available market (TAM), while the left axis is market share.

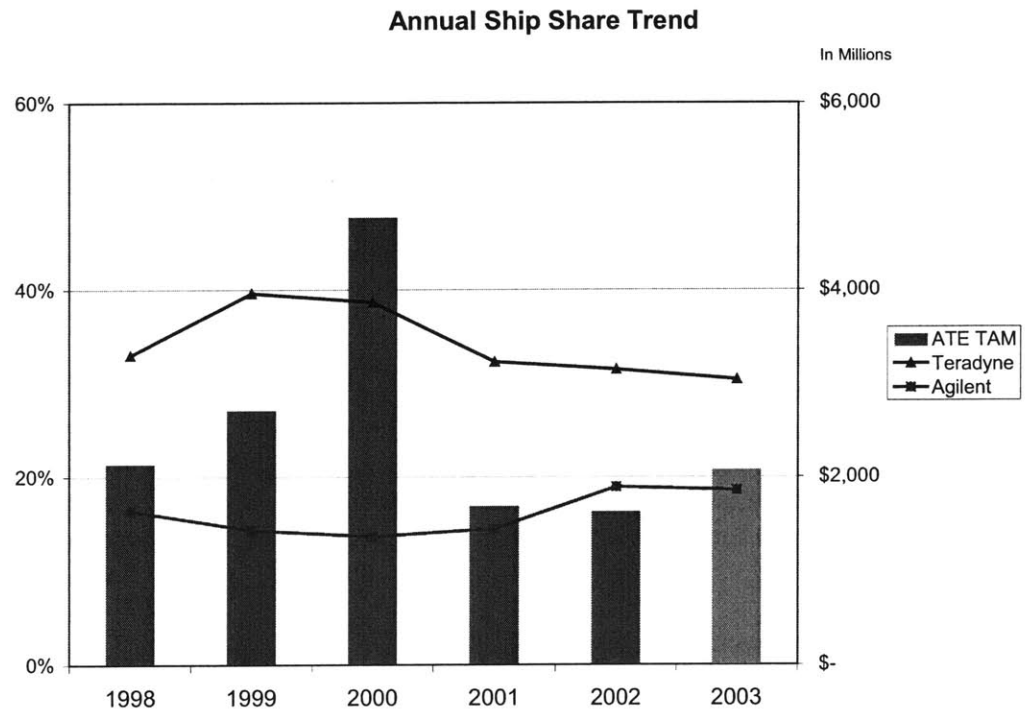


Figure 1.5.1 Annual Ship Market Share Trend [37]

1.6 Questions in the Determination of the New Market Strategy

The market for the semiconductor test equipment is changing. In following the voice of the customer, the semiconductor test industry changed its product development methodology. Typically, large companies followed the vertical strategy, and smaller companies followed the horizontal strategy. However, the industry recently navigated through a period of uncertainty due to the macroeconomic conditions from the recession after the year 2000. In the future, much about semiconductor industry remains unclear. The test industry must answer numerous questions in order to determine the best strategy to move forward in product development.

It must answer the following questions:
How real and lasting are the changes?
Will an economic recovery shift customer demand back toward the traditional production paradigm again?
How does each one of the changes affect the future product strategy?
Should Terdyne follow either the vertical or horizontal strategy?
Will the changes in the market result in disruptive or incremental business changes?
How should the industry best react to the changes?

1.7 Goals of the Project

In determining the product strategy for the semiconductor test industry, the thesis set three tangible goals.

1. Confirm the underlying changes in the semiconductor test industry. This project studies all the changes in the semiconductor test industry by looking at the entire semiconductor value chain. It also looks at the root causes of the changes in the semiconductor test industry in order to determine the future effects of the changes in the semiconductor test industry.

2. Analyze the vertical and the horizontal market strategies. Because of the semiconductor test industry's emphasis on the horizontal or vertical market strategy, this project develops a systematic method to compare and value each strategy.

3. Develop specific considerations in product strategy in response to the future changes in the semiconductor test industry. After understanding the trends in the semiconductor test industry, this thesis presents a unified model to discuss the future direction of the industry. Looking at this direction, this project develops specific recommendations to compete effectively in the future semiconductor test industry.

1.8 Project Methodology and Conclusions

This thesis began with an introduction of the specific project. It also discusses the current semiconductor testing business model, and the current trends and changes in the test industry in the framework of the changes in each step of the entire semiconductor value

chain. This thesis also discusses the current strategies (horizontal and vertical) employed by the semiconductor test industry, developing a model to understand and tangibly value the tradeoffs in each strategy. It concludes that in the long-term, the current strategies are not sufficient to meet the future needs of the semiconductor test industry.

Chapter 2: Introduction to Semiconductor Test

2.1 Introduction

This chapter starts with an introduction to Teradyne and a general description of the industry in which Teradyne participates. It also gives a brief introduction to the need for semiconductor test equipment, as well as the semiconductor test technology.

2.2 Origins of Teradyne, Inc.

In 1960, Nick DeWolf and Alex d'Arbeloff devised the plan to start Teradyne. The business plan for Teradyne, it stated that "electronics equipment for industry requires a high order of reliability and dependability. The high cost of down-time for maintenance and repeated calibration is sufficient to warrant more care in the design of such equipment and the use therein of higher quality components than in the production of consumer goods. The penalties to the user of undetected improperly functioning equipment may be many times the original cost of the equipment."[62]

In the 1960s, Teradyne's equipment tested mostly capacitors, transistors, resistors, and diodes. Teradyne's equipment also tested the integrated circuit to a limited extent. In the 1970s Teradyne began to diversify, grow, and extend its business. By the 1980s it possessed a similar structure to the current Teradyne.

2.3 Organization of Teradyne, Inc.

As shown in Figure 2.3.1, the Teradyne of the 21st century consists of five major divisions. This thesis consists of data from the semiconductor test market, which encompasses about 46% of Teradyne's annual revenue. The Connection Systems Division provides test solutions for the telecommunications and networking markets. It accounts for 32% of Teradyne's revenue. The Circuit Board Test and Inspection Division accounts for 14% of revenue. Diagnostic Solutions Division, which provides for solutions in automotive electronics testing, accounts for 5%. Teradyne's smallest division provides solutions to test broadband service within the telecommunications industry. It accounts for only 3% of revenue.

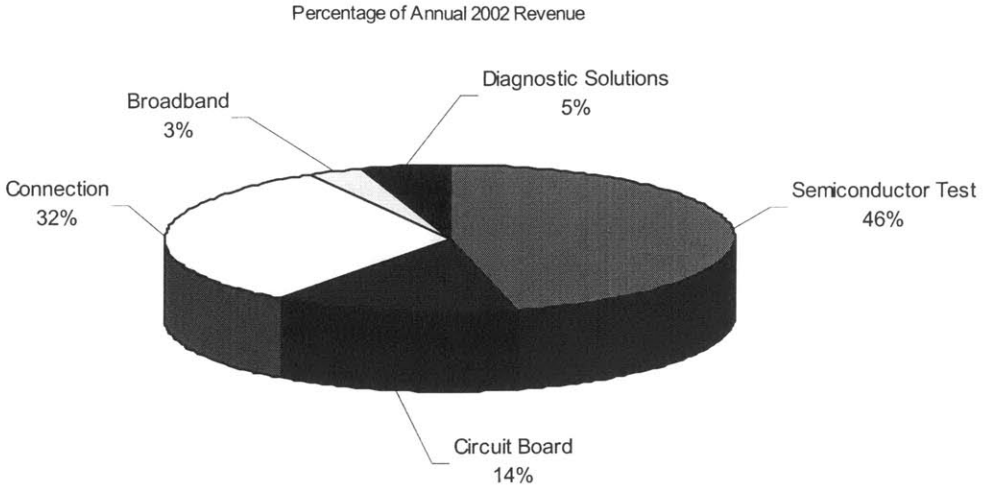


Figure 2.3.1 Percentage of Annual Revenue for the Divisions at Teradyne[1]

2.4 Summary of the Teradyne, Inc. Financials to Present

As with the economy of the booming 1990s, the semiconductor industry, semiconductor test industry, and Teradyne enjoyed continued rising profits until the economic recession of 2000. The years subsequent to 2000 were challenging for Teradyne as well as most of the semiconductor industries. Figure 2.4.1 shows the net income and the revenue of Teradyne. It shows the increasing revenue growth of the 1990s with the peak at the year 2000. After 2000, both the revenue as well as the net income dropped sharply for Teradyne.

Specifically, in the Teradyne's Semiconductor Test Division, revenues mirrored the general Teradyne trend. The early 1990s showed large growths in revenues, but the industry suffered since the peaking of revenues in 2000.

[1] Graph presented from the financials numbers from [55].

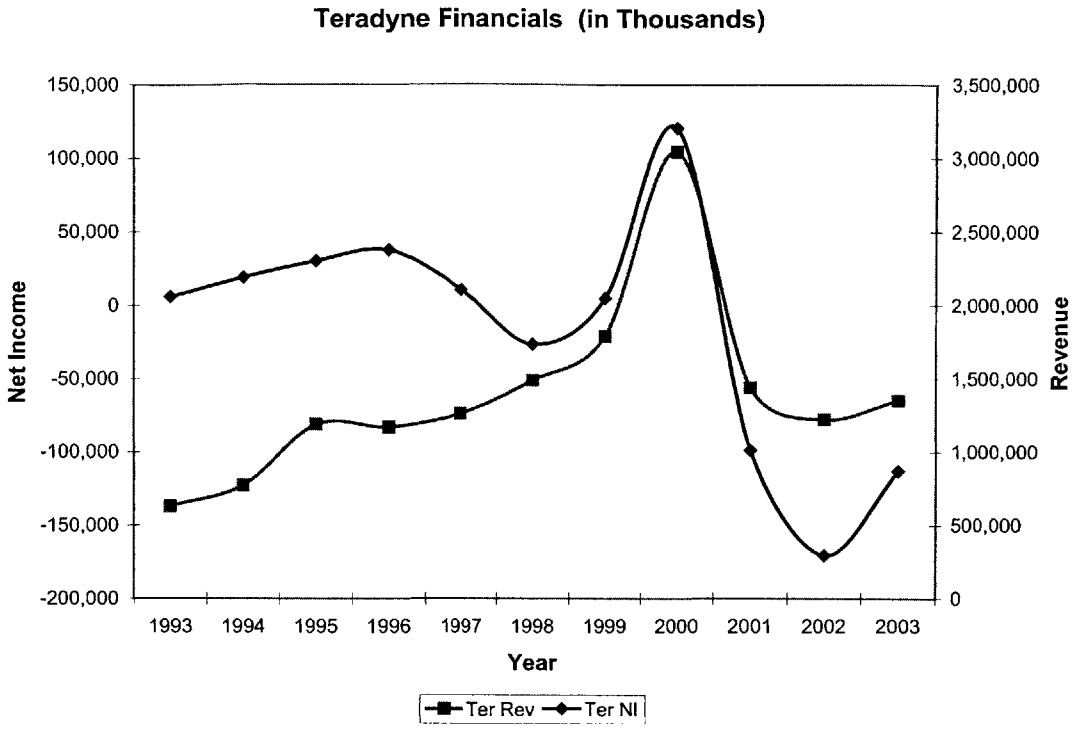


Figure 2.4.1 Selected Financial Data of Teradyne[2]

2.5 General Divisions of Marketing in Semiconductor Testing

Teradyne fulfills the market with four major business units. The computing market encompasses all the high-speed digital devices such as the microprocessors, chip sets, and network processors. The mass storage data communications market includes high-speed SOC (Systems on Chip) devices, as well as high-speed data transmission devices such as SERDES (Serializers/Deserializers). The wireless market consists of the cordless phone devices, Wireless LAN (Local Area Network), and Bluetooth devices. The consumer markets consists of the low-speed digital devices such as micro-controllers, smart cards, automotive, and consumer electronics devices. The subsequent chapters describe the alignment of the Teradyne product offerings to each market segment.

2.6 Test Objectives

In the most basic sense, the automated test equipment (ATE) simulates the function of the chip by driving an electrical signal through the chip. The chip processes the input signal and responses with an output. The ATE captures the output, compares it to the expected output of the chip, and determines whether the chip is good or bad.

The primary objective of testing is to insure that the device will perform all of its designed functions in the worst-case environment as defined by the device

[2] Graphs presented from the financials numbers from [3].

specifications.[3] The test equipment uses different techniques to accomplish the test objective depending on the goals of the tester. To this effect, testing is divided into four different categories.[4]

1. Characterization Test:
Characterization testing encompasses the most comprehensive sort of test. Often named characterization and design verification testing, the purpose of this type of test is to verify the correctness of the design and determine the devices characteristics. In this type of testing, the test accuracy far exceeds the demands for test speed because of the developmental nature of characterization testing. Furthermore, from the characterization test, the test engineer writes the production test.

2. Production Test
Because of the rigorous nature of characterization test, it is not practical to use the characterization test program in production. The test engineer prepares a "dumber" version of the characterization test in the production test program. Production testing ensures that the device meets its specifications and functions correctly in its specified mode of operation. However, the production test must also consider the minimization of the test time, and the maximization of the cost effectiveness for testing. Much of the test revenue in the semiconductor test business comes from production test because of the volume of devices that require production testing.

3. Burn-in and Incoming Inspection Test
Test engineers use burn-in testing to insure that the device will function correctly for a specified number of years. Engineers make correlations between the life span at room temperature and life span at elevated temperatures. The basic idea comes from putting a device in the furnace for a certain length of time at specified temperatures. Based on the temperature and time in the furnace, the engineer can determine the expected life of the devices.

In complex and costly systems, where the semiconductor devices represent only a small portion of the cost, the system manufacturers use incoming inspection testing. This testing insures that all devices used in their systems function correctly according to specification. In most cases, the incoming inspection test is not as comprehensive as the characterization test, but is more comprehensive than the production test.

This paper addresses the issues of production testing in the non-memory ATE market, which generates most of the ATE revenue because of the volume of devices as well as the level of technological differentiation.

2.7 Automated Test Equipment (ATE)

Most automated test equipment for production consists of the workstation, the main cabinet, and the head. As shown in Figure 2.7.1, the workstation (1) serves as the user interface for the ATE. The test engineers interface with the software tools to debug test

[3] Similar views of the generally accepted objectives of test comes in [31] used for training, as well as [10].
[4] Characterization as proposed by [31] used internally for training at Teradyne.

programs, manage daily production operations, and controls the tester through software on the workstation.

The main cabinet (2), sometimes called the mainframe, consists of compartments for the power supply, measurement instruments, and computers that control the instruments. For those ATE with liquid cooling to regulate the test head as compared with those with fan cooling, the main cabinet also contains the refrigeration unit or fan unit. A plenum (3) carries either the cooling air or the liquid from the main cabinet to the test head.

The test head (4) contains the most sensitive measurement electronics. Due to measurement sensitivity, these circuits in the test head requires close proximity with the device being tested or device under test (DUT). For example, the tester shown below tests high-speed broadband devices. The high-speed devices benefit from short electrical paths between the tester's digital drivers and the pins of the DUT. Therefore, in the tester below, the instruments slide into the slots in the test head allowing for a short path between the DUT and the tester.

The Device Interface Board (DIB) (5) provides the electrical interface between the tester and the device. The mechanical manipulator (6) holds and positions the test head.

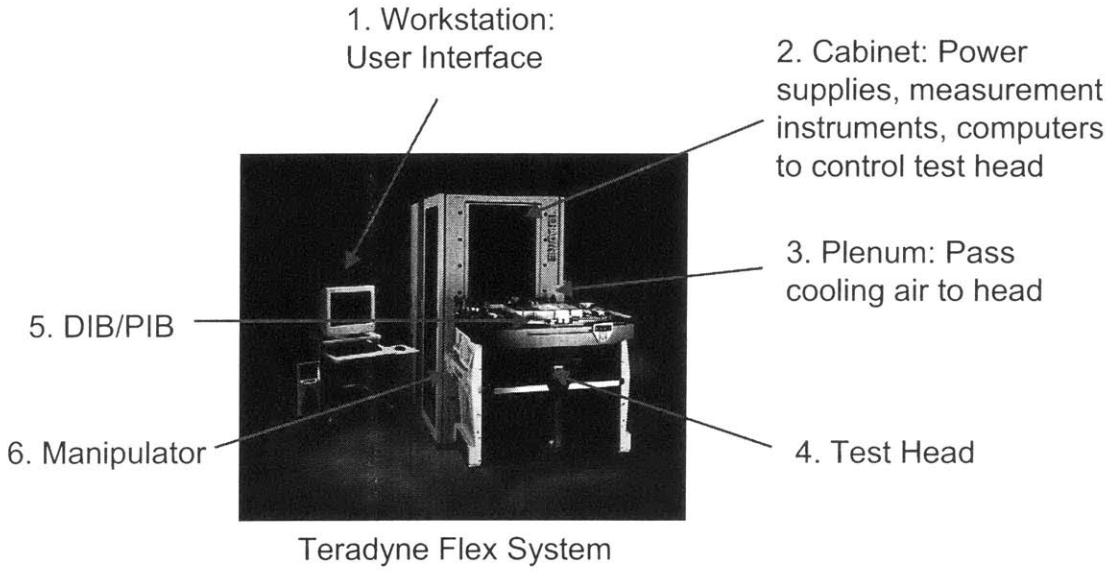


Figure 2.7.1 FLEX ATE Tester from Teradyne[5]

2.8 Interfacing with the ATE

As mentioned in section 2.7, in addition to the ATE, the Probe Interface Board (PIB) or Device Interface Board (DIB) provides the electrical interface between the ATE tester and the wafer or the DUT. As shown in Figure 2.8.1 [10], the DUT attaches to the socket, which attaches to the DIB. The DIB interfaces with pins, often referred to as the

[5] Teradyne product photograph introduced on [56]

pogo pins, from the pin card electronics. The pin card electronics contains the instrumentation to test the DUT, and is contained in the test head.

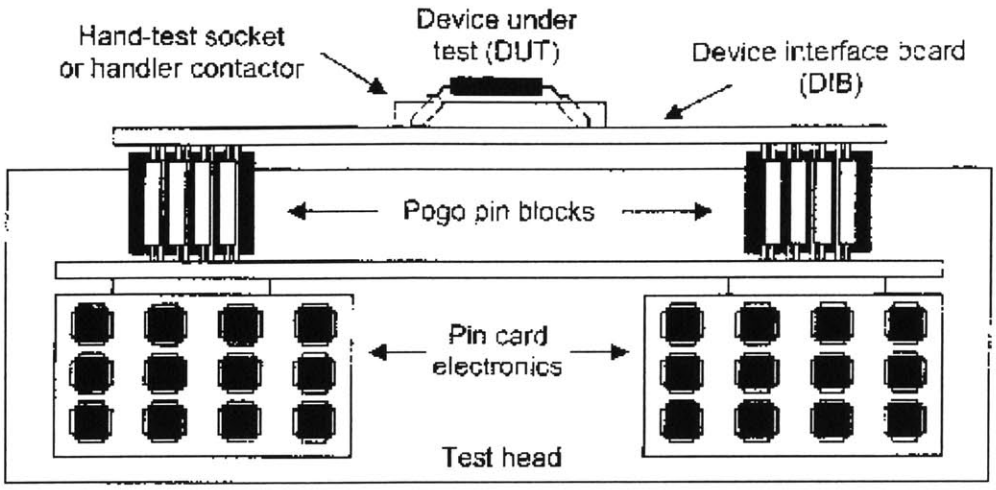


Figure 2.8.1 ATE Test Interface[10]

2.9 Wafer Test

Customers employ the ATE tester in multiple steps along the value chain. After the fabrication of the wafer, the wafer manufacturer usually tests the individual dies on those wafers. In this test, called the wafer test, the wafer probers manipulate wafers for the ATE equipment to test the individual dies. Figure 2.9.1 shows the probe card. The probe card attaches electronically to the PIB, providing a connection between the probe card and the PIB. The PIB provides the electrical connection to the test instrumentation. The prober (handler for the semiconductor wafers) moves the wafer underneath the probe card. The probe card contains sets of small electrical probes that touch down on the individual dies, establishing electrical connections to the dies in order to test them.

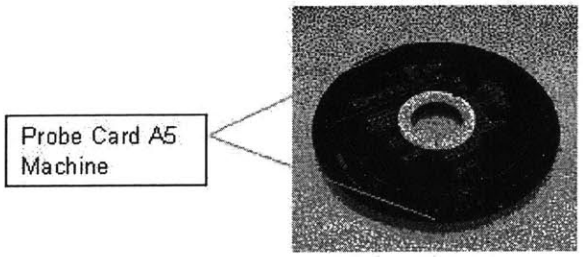


Figure 2.9.1 Probe Card[6]

[6] Picture obtained from Teradyne [56]

2.10 Device Test

After the packaging of the individual semiconductor chips to create semiconductor devices, the semiconductor devices is tested again as the final quality gate. In this test, the DIB, as shown in figure 2.10.1, contains sockets that the handler fills with device packages. The devices are tested in the sockets. The handler removes the semiconductor devices from the sockets and inserts another set of devices to be tested.

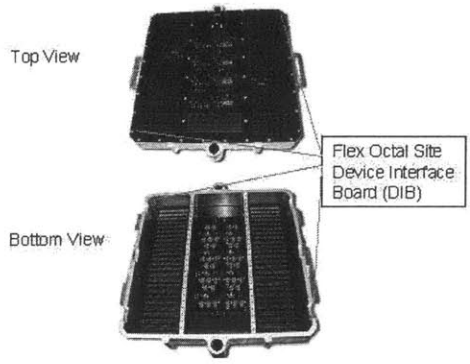


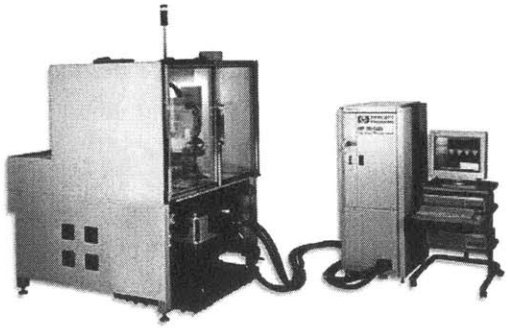
Figure 2.10.1 Device Interface Board (DIB)[7]

The handlers for the devices manipulate packaged devices in much the same way as the probers for the wafers. Handlers typically fall under two categories, the gravity-fed and the robotic. Robotic handlers are also known as the pick-and-place handlers. The robotic handlers act as a robot hand. It picks up the semiconductor device, and then it inserts the devices into the DIB sockets. The gravity fed handlers use gravity to drop a device into the socket.

The handler manipulates the devices to establish a temporary electrical connection between the DUT and the DIB board. Figure 2.10.2 shows examples of both gravity-fed and robotic handlers. In addition to feeding the devices in and out of the DIB sockets, the handlers also sort the good devices from the bad.

[7] Picture obtained from Teradyne [56]

MCT Gravity-Fed Handler



SSI Robotics Handler

Figure 2.10.2 Handlers[8]

2.11 Test Layout

In the Figure 2.11.1, the Teradyne Catalyst cabinet (2) sits at the left back of the room. The workstation (1) sits at the back right. The manipulator (3) controls the test head, which interacts with the wafer. The prober (4) holds and handles the wafers for testing. In this case, the inverted test head (5) carries a PIB with a probe card that touches down on the individual dies to test the whether the dies meet specifications.

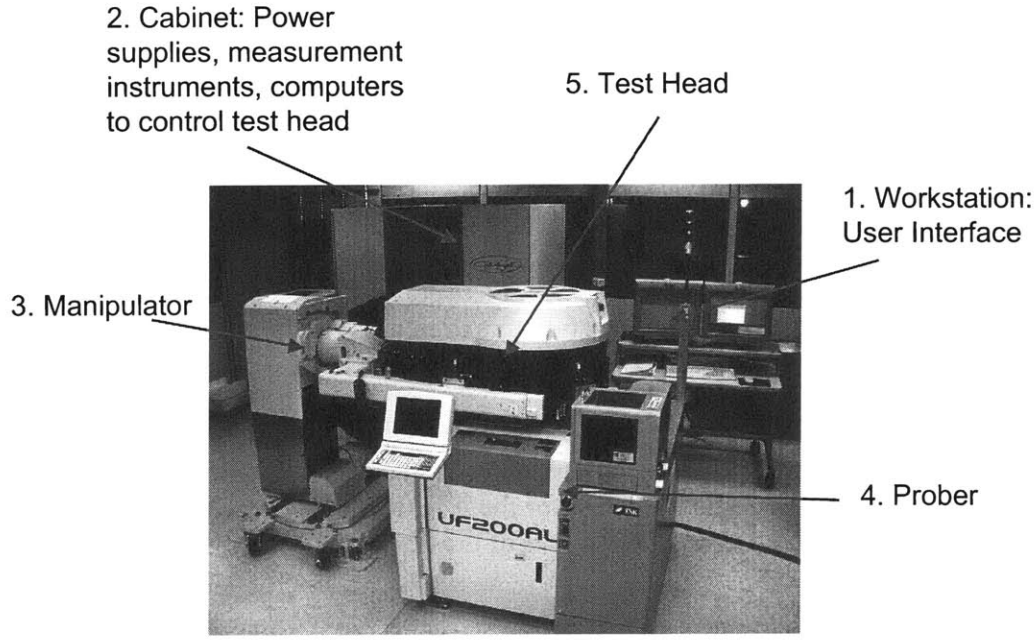


Figure 2.11.1 Test Floor Layout[9]

[8] Handler picture obtained from product photographs in [39] for gravity fed and [53] for robotic.
[9] Picture courtesy of Teradyne, Inc.

2.12 Device Introduction

The market for test devices encompasses a wide array of digital, analog, and mixed-signal devices. To understand some of the details behind the market, it is important to understand the fundamental definition for devices before explaining the market for such devices.

1. Digital Circuits

"Digital describes electronic technology that generates, stores, and processes data in terms of two states: positive and non-positive. Positive is expressed or represented by the number 1 and non-positive by the number 0. Thus, data transmitted or stored with digital technology is expressed as a string of 0's and 1's. Each of these state digits is referred to as a bit (and a string of bits that a computer can address individually as a group is a byte)." [19]

On the application level, purely digital circuits are those that only process the ones and zeros. For instance, an Intel Pentium II microprocessor is a purely digital device. It takes digital inputs, computes those inputs, and provides the output in digital format.

2. Analog and Mixed-Signal Circuits

Analog circuits, also known as the linear circuits, include operational amplifiers, active or passive filters, comparators, and other functions. By definition, a mixed-signal circuit consists of both digital and analog elements. For instance, an analog-to-digital converter (ADC) is a common mixed signal circuit. The circuit takes in the analog signal and converts it into a digital signal.

On the application level, most of the devices in the market today consist of both analog and digital circuits because of the complexity of the devices. For instance, a cellular telephone consists of many analog, digital, and mixed signal circuits working together in a very complex fashion. For instance, "the control microprocessor selects the incoming and outgoing transmission frequencies by sending control signals to the frequency synthesizer. The synthesizer...controls the mixers in the radio frequency (RF) section of the cellular telephone. The mixers convert the relatively low-frequency signals of the base-band interface to extremely high frequencies that can be transmitted from the cellular telephone's radio antenna." [10]

The digital microprocessor circuit, the analog conversion to high frequencies, and the analog to digital conversions in the cellular phone all contribute to the mixed-signal capabilities of the device. The challenge for the ATE tester comes from testing the digital, analog, and mixed signal capabilities of the devices with cost and speed of test constraints.

2.13 Common Tests

In order to give some basic concept of testing, this thesis includes a few common tests. It only gives a brief introduction, not attempting to rigorously broach the complexities of testing semiconductor devices.

One can divide testing into three basic categories: functional, DC parametric, and AC parametric. "Functional tests insure that the device operates as it is supposed to. They verify that the truthtable is correct....DC parametric tests insure that the device will operate in its specified environment. They measure the current consumption of the device and its ability to operate at the proper voltage levels. AC parametric tests are concerned with timing." [31]

On an applications level, perhaps the most common test is the direct current (DC) continuity test. It insures that the DUT connects correctly to the ATE using the test fixture such as a DIB. Another test called the leakage current test measures the small amounts of leakage into or out of the pin. Excessive leakage is caused by physical defect, and poor processing that causes infant mortality. In addition, it affects the operation of the device. The power supply current test is one of the best ways to detect catastrophic defects. This test measures the amount of the current drawn from each of its power supplies. It is also performed on most devices.[10]

2.14 Chapter Summary

The economic conditions following the peak demand year of 2000 led to large declines in revenue for the semiconductor test industry. While many predicted a drop in revenue, the length and the extent of the declines led to worry in the semiconductor test industry. Even though the sponsor company consists of five different segments, namely, broadband, diagnostic solutions, connections, circuit board, and semiconductor test, most of the revenue comes from the semiconductor test business. Subsequently, the company sponsored a project to understand the changing market conditions in the industry.

This thesis focuses on the production testing markets. Because of the volume of devices in production testing, this market provides the greatest revenue for the test industry. The testing of semiconductors occurs in two separate steps in semiconductor manufacturing production. First, after wafer fabrication, the individual dies must be tested. Secondly, the testing of the packaged devices acts as the final device quality gate.

The test technology consists of software, electrical, and mechanical component. The software library runs the routines to test the semiconductor wafers and devices. The electrical instruments boards as well as the internal "guts" of the ATE carries out the software instructions. The mechanical controls and support cabinetry houses manipulates, cools, and houses the instruments.

In order to understand the market models to fulfill the project objectives, it is valuable to understand semiconductor test and semiconductor test technology. This knowledge will be later incorporated in understanding the semiconductor industry strategy.

[10] Burns and Roberts provide a good introduction to ATE testing.

Chapter 3: Market Trends in the Semiconductor Industry

3.1 Semiconductor Value Chain Trends

This chapter discusses the observed trends of outsourcing, and capital limitations as recognized by Teradyne. However, it discusses these trends systematically in the framework of the entire value chain for semiconductor manufacturing. This chapter fulfills the projects first goal of confirming the changes in the semiconductor test industry. In addition, it goes further to look at changes beyond those specified initially in the project description.

Figure 3.1.1 shows the decomposition in the semiconductor value chain. The stars in the figure indicate the steps in the chain where semiconductor testing occurs. The flow starts with the creation of software and hardware design tools to develop complex ICs. Using the design tools, the IC designers create circuit designs. The IC designers transfer those designs to the foundry for fabrication of the ICs. After the fabrication of the wafers, the wafers are tested (probe test). The wafers are transferred to assembly. At this step, the circuits are packaged and tested. The testing of the devices is the final quality gate before distribution for use. Finally, the packages are distributed to the customers.

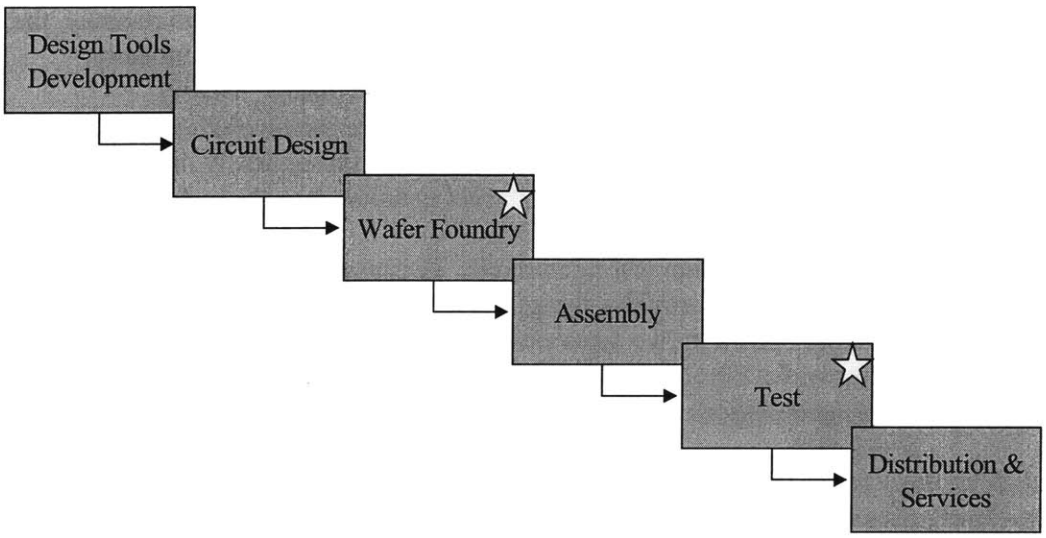


Figure 3.1.1 Semiconductor Value Chain[1]

1. Design

Historically, semiconductor companies developed their own set of rules and techniques to match their manufacturing capability. As the complexity of ICs increased, two significant trends arose in design of semiconductors.

1. The design rules began to become standardized across companies as technology became more similar.

[1] Breakdown and description of the value chain described in detail from Klein [33] and [34].

2. The scale and specialization levels required to develop design tools became so great that even the largest companies decided to involve third party specialists to develop a new generation of design tools.

With all the papers written about Moore's Law (the exponential growth in the number of transistors per integrated circuited), this thesis will go not debate its merits except to say it drives the complexity of chip designs in the semiconductor industry as shown in Figure 3.1.2 from Intel. Later sections in this thesis will discuss its effects on the semiconductor test industry.

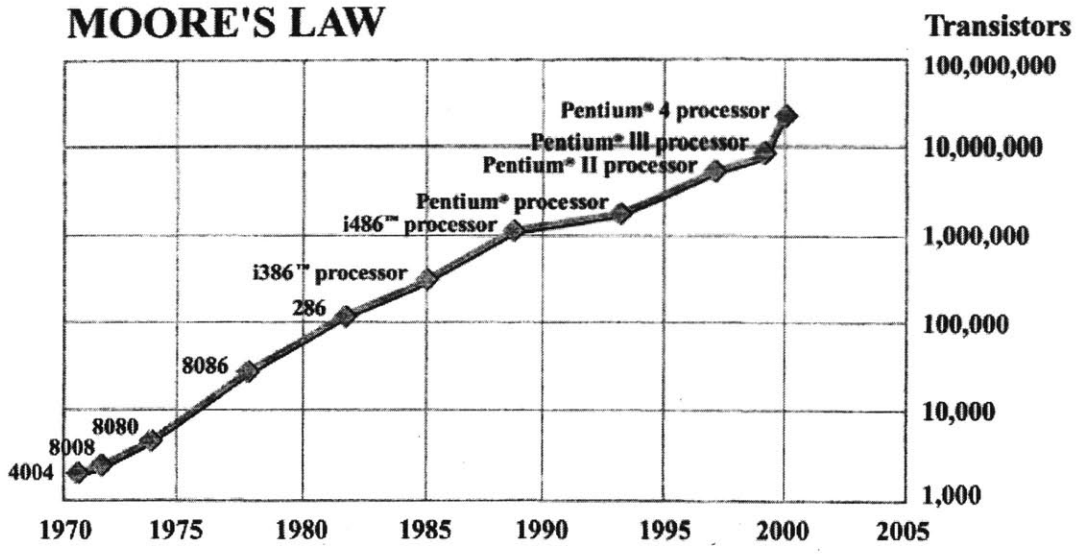


Figure 3.1.2 Moore's Law from Intel [40]

Because of the rapid growth in the complexity of the chip, it outpaces the advancement of design tools. The IC designs still rely heavily on the ability of the skills and expertise of the engineers. This, along with the development of independent foundries, has led the industry towards the disintegration of the value chain. In the past, vertically integrated manufacturers dominated the industry. Today, many firms simply focus on design tools, IC design, or manufacturing. Section 3.3 will describe the specific dynamics in the industry.

2. Wafer Fabrication

Two major trends appear in the fabrication of semiconductors. First, as shown in Figure 3.1.3, the increased complexity of semiconductors resulted in an exponential boom in capital costs for the manufacturing of semiconductors. "Motorola's MOS2 fab cost $4 million in 1974 while Motorola's newest fab cost $1.7 billion." [33]

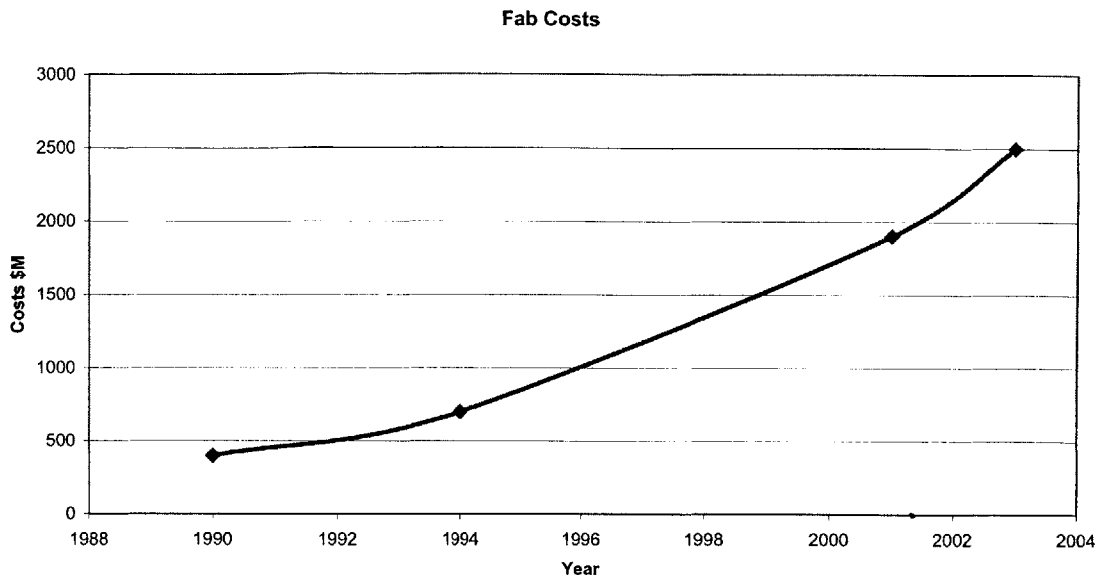


Figure 3.1.3 Estimated Cost of Semiconductor Fabs[2]

Secondly, the standardization in the industry around Complementary Metal Oxide Semiconductor (CMOS) came due to its combination of high performance, low cost, and low power consumption. This provided opportunities for expanded economies of scale around fabrication of CMOS semiconductors.

Both of these trends resulted in the creation of specialists in the fabrication of semiconductors. These companies often called pure-play foundries such as Taiwan Semiconductor Manufacturing Company (TSMC), and United Manufacturing Company (UMC) build successful businesses around this model.

3. Assembly and Test

After the wafer production, the wafer is sawn into "chips" and assembled into packages that protect the circuits and provide the electrical interface to the rest of the system. Three major trends drive this assembly and test industry. First, the proliferation of the semiconductor market led to the increase in the variety of packages and requirements. Second, because of the historical labor-intensive process of semiconductor packaging, many of the IC firms established assembly and test facilities in the Far East low cost regions such as Korea, Taiwan, and Malaysia. Today, much of the packaging expertise still resides in these regions. Third, the semiconductor industry views the assembly technology as a commodity space. They perceive little value-add in the package, and with few exceptions, the package adds little competitive advantage. This makes IC manufacturers more willing to outsource the assembly and test steps in the value chain.

On the test side, companies need reliable testers. They also look for an inexpensive work force to operate the relatively high capital cost ATE, maximizing the utilization rate of

[2] The figures come from estimates from [50]

the specialized equipment. The three trends in assembly as well as the need for a relatively inexpensive work force leads many firms to outsource the assembly and test operations to firms called the subcontractors. ASE Group, Amkor, and STATS provide successful business models in assembly and test that take advantage of the trends.

3.2 Semiconductor Development Trends

As a general statement, the test technology development must correspond with device technology development. In the four major categories of device characteristics, it appears that the chip testing requirements will continue to increase. The fundamental issues in the test industry come in four major categories.[3]

1. Pin Count

With the increase complexity and shrinking geometries of the IC, the amount of integration on the circuit continues to increase. As a result of the integration, the complexity of circuitry on the IC increased the pin count on the semiconductor devices. The increase in complexity and subsequently pin count results in greater required ATE performance in the case of functional test, as well as challenges in throughput performance due to the number of pins on the device. These all serve to increase the cost of testing.

2. Speed

As devices become more complex, and the number of transistors per chip continues to increase, it becomes possible to run them at increasingly fast rates. In the testing environment, the ATE must locate its instruments close to the devices in order to solve the problems that come from establishing temporary high frequency connections between the device and the tester. In addition, the faster devices require faster instruments to satisfy the increase speed of the devices.

3. Power

As the device density increases, the devices require more power to operate, resulting in greater power consumption during the testing process. The large power requirement results in challenges during testing such as heat dissipation, and signal path carrying capacities. Heat issues result in solutions that require liquid to cool the test head increasing the complexity and cost of design for the ATE.

4. Systems on a Chip

As the systems-on-chips (SOC) becomes increasingly prevalent due to the shrinking geometries, and the decreasing manufacturing costs of CMOS, it introduces additional complexities to testing. For example, the SOC devices inherit all problems described in the above subsections. However, it adds the problems of limited access to the individual subcomponents and individual systems on the chip.

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[3] Ochoa and Porter provide the categories of devices characteristic development [43].

3.3 Industry Capital Equipment Trends

Traditionally, the Integrated Device Manufacturers dominated the value chain, buying all the capital equipment. These companies include Intel, Motorola, Texas Instruments, and ST Microelectronics. From design tools to assembly and test, these companies vertically integrated everything. However, the outsourcing of design tools to 3rd parties started the disintegration of the value chain. The electronic design automation companies such as Mentor Graphics, and Cadence built successful business models.

On the capital equipment side, a wide variety of strategies of outsourcing exist. For instance, Intel does not outsource much of its manufacturing operations, buying the capital equipment to manufacture semiconductor devices in-house. Motorola, and Advance Micro Devices clearly stated their intentions towards the Asset-Lite model, incorporating pure-play foundries as well as subcontractors into their manufacturing decisions, while still planning to build fabrication facilities. On the other end of the spectrum, companies such as NVIDIA, Broadcom, and Qualcomm (fabless) developed business models on design of ICs rather than the manufacturing. Deciding to take advantage of per-unit pricing offered by independent foundries and subcontractors, these companies invest their money on research and development rather than capital expenditures.

Today, the IDM's, fabless companies, pure-play foundries, and subcontractors hold complex relationships. Often, the IDM's keep the fabrication of their bleeding-edge (devices that follow Moore's Law) devices in-house. They outsource their trailing-edge (devices at the end of their lifecycles) devices to the pure-play foundries. The outsourced devices typically employ independent assembly and test subcontractors for packing and testing the devices. However, the typical scenario also includes many permutations. For instance, IDM's may choose to design in-house, outsource to foundries, and bring the assembly and test back in-house. More often, IDM's will choose to design in-house, manufacture the wafers in-house, and outsource for assembly and test.

In most cases, the pure-play foundries charge for manufacturing of semiconductors by the wafer. These foundries do not charge fees for the capital equipment for manufacturing the semiconductors. Instead, these foundries add overhead and capital cost to the prices of each batch of semiconductors (per-unit manufacturing pricing). The availability of per-unit manufacturing costs, due to the rise of the pure-play foundries, led to an increase in the number of fabless, or independent design house. The fabless companies typically employ a pure-play foundry to manufacture their designs, and outsource the assembly and test of the devices to independent subcontractors as well. However, complex relationships exist where the fabless companies outsource to the IDM to manufacture the device. The IDM's might outsource the fabless design to pure-play foundries, and independent subcontractors.

As Figure 3.3.1 shows, in any stage of the process, companies can outsource to each other to fulfill the necessary functions in the development of the semiconductor devices.

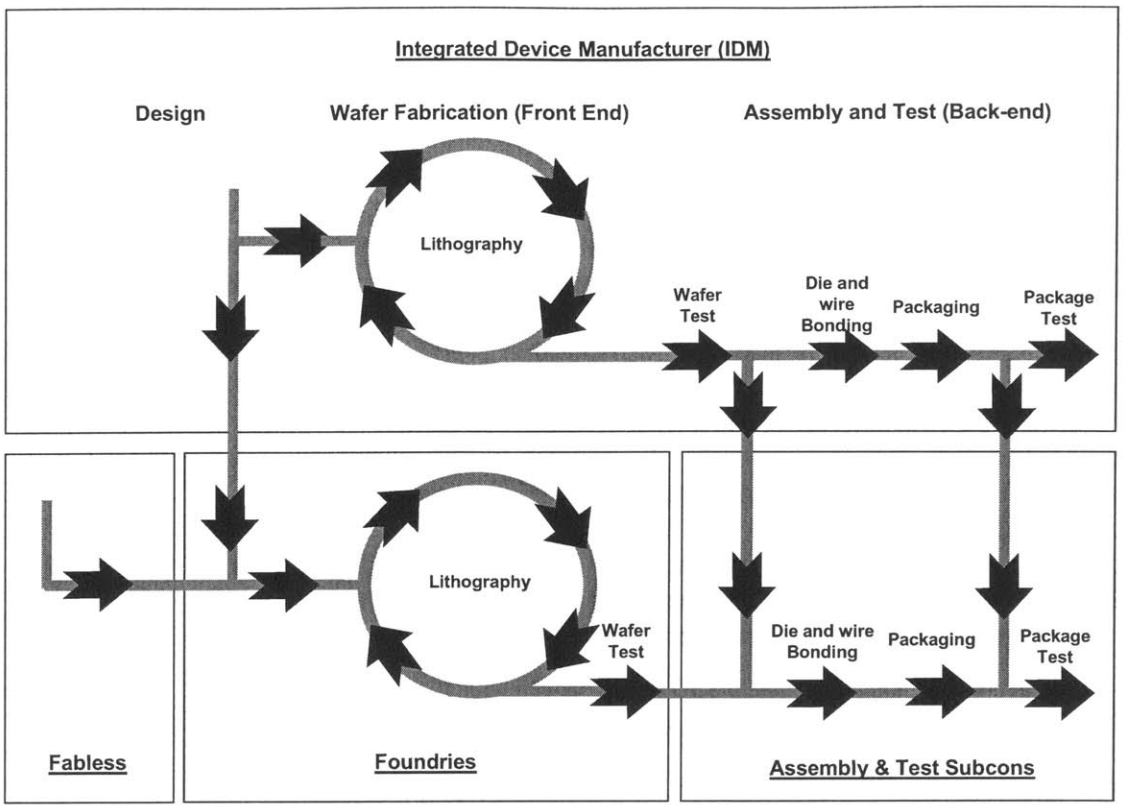


Figure 3.3.1 Interactions of IDM, Fabless, Foundries, and Subcons[4]

3.4 Outsourcing Strategy Considerations

Strategically, from the side of the Fabless companies, outsourcing solves problems with the limitation on capital and overcomes the initial high barriers to entry due to the large (and continually rising) capital equipment costs. In addition, the rise of the independent pure-play foundries solved the concerns with the theft of Intellectual Property when outsourcing to the IDMs, who often offered competitive products. On the IDM side, the outsourcing of semiconductor manufacturing eases the problems with demand fluctuation. In addition, the falling of transfer prices from moving the circuit design towards manufacturing, as discussed in section 3.1, also makes outsourcing cost competitive.[5]

On the other hand, concerns for quality with the outsource partner creates incentives for IDM to keep everything inside. In addition, IDM often keep operations inside to have greater control over their capacity. This way they can expedite orders, reprioritize products as needed without having to negotiate with an outsource vendor.

[4] Picture format taken from Teradyne, Inc.

[5] Dhayagude, Tushar et al. gives a good picture of the initial environment for IDM, Fabless, and Subcon competition.

3.5 Outsourcing Strategy Trends

Looking at the financials of the large IDMs[6], the financials show an increasing trend towards the fabless model. The initial analysis included the large IDM Intel, as well as some smaller IDMs. Because the monopoly nature of Intel, and its distinct in-house strategy, it appears an anomaly from the majority of the industry. Furthermore, the squeeze on capital assets since 2000 skewed the capital assets allocations of smaller IDMs with less resource for large capital equipment purchases. For these reasons, the data presented comes from the list of the chosen companies in the footnotes.

Figure 3.5.1 shows the average R&D expenditure, average capital expenditures, and average net income (NI) as a percentage of sales. The early 1990's marked an increase in both R&D and capital expenditures as percentages of sales. This strategy correlated with the continued decline in net income. Even before the peak of 2000, IDMs appeared to move their investment emphasis towards the higher margin R&D instead of the continuing to invest heavily in capital expenditures. The net income correspondingly increased with the shift of investment. The term "Asset Lite" means that the firm invests less on plant, property, and equipment (PPE). Instead, the firm utilizes more outsourcing in the manufacturing of semiconductors.

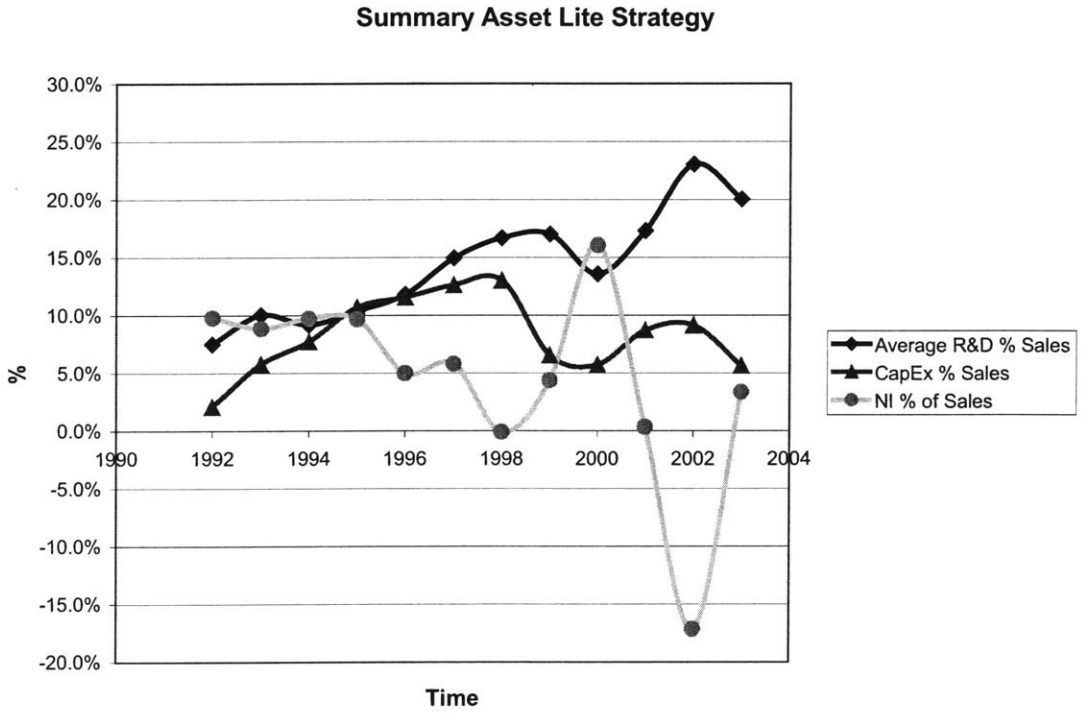


Figure 3.5.1 Financial Ratios Summarizing the "Asset Lite" Strategy

[6] Financials obtained from Thompson Financial Database for companies Motorola, ADI, and AMD.

At the same time, as shown in Figure 3.5.2, the financial statements of the Fabless design companies showed healthier gross margins, indicating a higher return on investment from the research and development as compared with manufacturing.

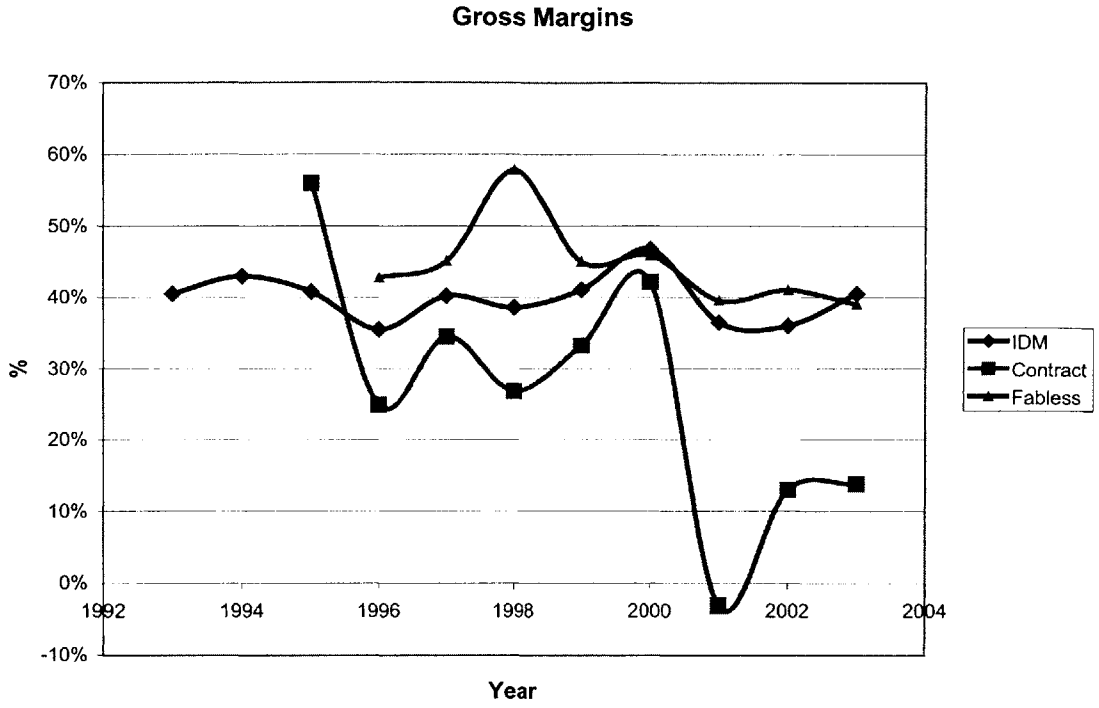


Figure 3.5.2 Semiconductor Industry Gross Margins[7]

In fact, the data for the growth of the subcontractor and foundry segments also shows the trend of IDM investment towards research and development, and the increase in IDM outsourcing. The rate of growth in the contract manufacturing exceeds the growth of the semiconductor industry, meaning that the subcontractors gained market share. Correspondingly, since 1998, the subcon Non-Memory Automated Test Equipment market (NM ATE market) has grown faster than the total Non-Memory Automated Test Equipment (NM ATE) market. This indicates that the subcons have been gaining share in ATE purchases.[8]

3.6 Chapter Summary

The semiconductor value chain is comprised of design tools development, IC design, fabrication, assembly, test, and distribution. The trends in the industry arose due to the complexity of the semiconductor devices that drove outsourcing of the EDA tools. Currently, three factors drive the continued disintegration of the value chain. First, the cost of semiconductor capital equipment and the economies of scale around CMOS technologies result in specialized wafer foundries. Second, companies outsource

[7] Financials of Fabless companies obtained from Thompson Financial Database.
[8] Data from Teradyne Internal, unpublished.

semiconductor assembly and testing because of the specialization in the East Asian region. Also, IC design specialty, as well as the rise of per-unit cost manufacturing drives the development of fabless companies.

In addition, three specific trends affect the semiconductor test industry. First, the disintegration of the value chain results in outsourcing. This shifts the customer structure of the semiconductor test industry. Second, the complexity of the semiconductor devices drives the complexity of the semiconductor test technology. Also, the constraints in capital costs leads to limitations on the absolute capital customer are willing to pay for the tester. However, the customer still demands low cost of test as measured per device.

Chapter 4: Semiconductor Industry Test Strategies

4.1 Introduction

After understanding the changes in the semiconductor test industry, this chapter discusses the details of the vertical and horizontal strategy. It begins with a brief introduction of test requirements. It also discusses the semiconductor device markets because the markets served by the test platform define the test strategies. It also clarifies the definitions of vertical, horizontal, broad, niche, flexible, and focused.

4.2 Review of Testing

As discussed in Chapter 3, semiconductor testing occurs in two steps of the value chain. Testing occurs after the fabrication of the semiconductor wafer, and also as a final quality gate in semiconductor testing. In this section, the semiconductor test market is further segmented in different devices from complex microprocessors to small micro-controllers embedded onto a credit card. The following sections provide two different methods to divide the device segment market. The first comes from the end-function view, and the second comes from the view of the semiconductor test industry.

4.3 Device Market Overview

Difficulties arise in the definition and segmentation of the device market. In much of the market studies, the device breakdowns come from end function devices. For instance, the data processing electronic device segment includes all the devices for processing data as an end function. This segment includes the very fast microprocessor devices as well as some very slow digital devices such as smart cards (an example includes those devices found in your American Express Blue Card). Table 4.3.1 describes the breakdown of some of the devices by end function.

Data Processing Electronics	Consumer Electronics	Communications Electronics	Automotive Electronics
DAS/FAS Storage	Analog Camcorder	Cable Modem	Airbags
Desktop PC (CPU & Memory)	Analog Set Top Box	System Cores	Antilock Braking System
Desktop PC Motherboards	Appliances	Digital Cellular	Auto Stereo
Disk Drive	CD Player	Digital Cordless	Climate Control Unit
Flash Cards	Color TV	DSL	Dashboard Instrument Cluster
Graphics/Audio Cards	Consumer Display	LAN	Engine Control Units
Handheld Computers	Digital Audio Players	Legacy Phone	GPS Navigation Systems
Mainframe/Super Computers	Digital Camcorder	Mobile Infrastructure	Remote/Keyless Entry
Memory Cards	Digital Set Top Box	Public Infrastructure	
Memory Modules	Digital Still Camera	RAS/RAC	
Monitor	Digital TV, CRT	Routers	
Notebook	DVD	SONET/SDH	
Printer	Mini-Disc Player		
Server	VCR		
Smart Cards	Video Game Devices		
Storage Network			
Tape Storage			
Workstation			

Table 4.3.1 Method of Market Segmentation Used in Market Data Presented in Thesis[2]

4.4 Semiconductor Test Market

The semiconductor test industry groups each market segments by device performance rather than by end-function. For instance, the FPGAs (field programmable gate arrays), smart cards, and low-end microcontrollers all require low-speed, low-cost digital test

[2] Market segmentation by end function comes from Gartner Database [27].

capabilities. Even though the end functions of each device differ, the semiconductor test industry groups these together. All these low-speed digital devices require low capital cost, and low-speed digital pins in the test platform.

As shown in Figure 4.4.1, Teradyne divides the market segments according to platform strategy. The Tiger platform covers the microprocessors, network processors, chipset, and other high-speed digital semiconductor devices. The Catalyst platform covers the mixed-signal business including the wireless, set top box, and other baseband devices. The J750 covers the low-speed digital devices such as the micro-controllers and the smart cards.

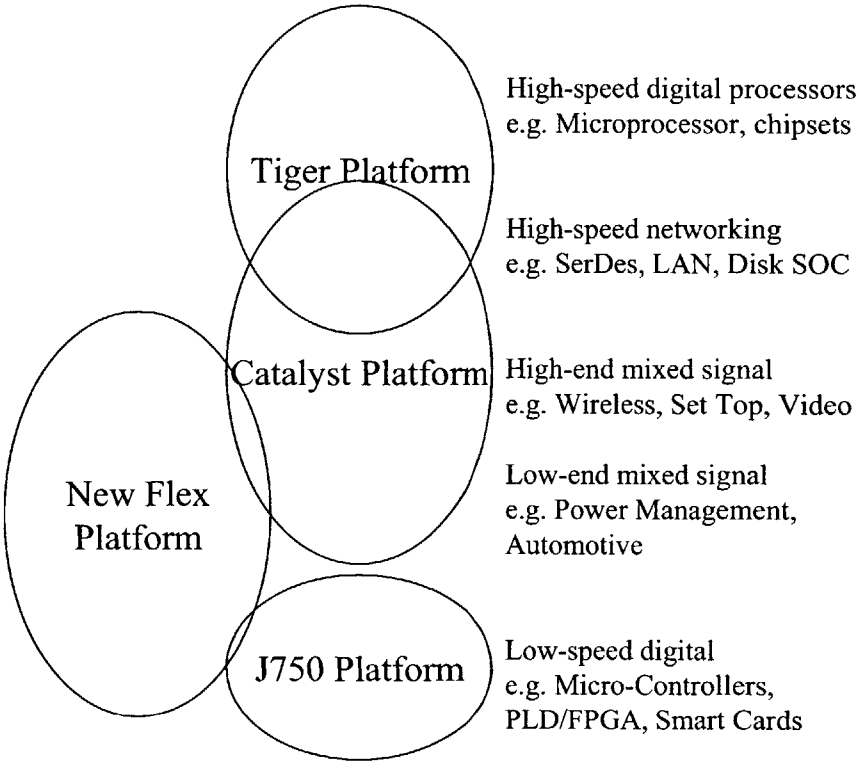


Figure 4.4.1 Teradyne's Semiconductor Test Platform Market Segmentation[3]

Overall, the semiconductor test market consists of six major competitor: Teradyne, Agilent, Advantest, NPTest, Credence, and LTX. These companies build large ATE in many of the segments in the semiconductor test industry. Although each company possesses strengths and weakness in the market, the large ATE companies compete in most of the device markets.[4]

Recently, several small competitors began competing for market share in specific niche segments. These companies include Eagle Test Systems, and Nextest. Eagle Test

[3] Picture used to some extent content from internal Teradyne document.
[4] Studies in market competition taken from conversations with company representative of the test industry as well as public research from [1], [16], [21], [36], [41], [42], and [47].

Systems focuses on the low-end mixed signal market, while Nextest focuses on the low-end digital market.

4.5 Test Industry Direction

In order to understand the direction of the industry, an interview was done with five of the six major semiconductor test equipment manufacturers, as well as two of the smaller makers of manufacturing equipment. In the interviews, questions were asked about their perception of the vertical and horizontal strategy.

- Two of the five large manufacturers interviewed acknowledged that their future ATE platform development was moving towards commonality between all their product platforms.

- Two major manufacturers claimed their product platform could test the entire market meaning that the one platform was flexible enough to test high-end digital devices, mixed signal devices, and low-end digital devices.

- One major manufacturer acknowledged the need for a vertical platform strategy, but realized that their diverse product portfolio made it very difficult in the near future.

- Of the two small manufacturers, both were satisfied with the horizontal market strategy. They felt no pressure to move towards a more vertical strategy.

4.6 Definitions

Until this point, this thesis used vertical, flexible, and broad almost interchangeably. It also used the terms horizontal, focused, and niche together. Furthermore, the thesis discussed the semiconductor test markets, and the semiconductor test industry strategies. In order to evaluate the tradeoffs in each strategy, this thesis must narrowly define the terms.

Due to the shortened lifecycles of semiconductor products, semiconductor manufacturers continually develop new products with greater integration, capability, and pin count that exceed the capabilities of current ATE. Furthermore, the manufacturing floor of the customer also changes its technology from its installed base due to unexpected volume changes.

In the course of these changes, the customer must consider the cost to switch from one tester platform to another. ***The vertical strategy allows the semiconductor manufacturers to use the same test platform, and make minor upgrades or downgrades in order to test a new device.*** Whether the test equipment needs to test a new device because of demand fluctuations of a new product introduction, the vertical strategy allows this change to occur easily. In order to make the vertical strategy a reality, the architecture of the semiconductor test platform must be flexible. ***Flexibility of the test platform means that the platform can be reconfigured easily in order test a new device.*** In order to make the vertical strategy possible, ***the test equipment platform must test a***

broad spectrum of semiconductor devices. From the high-end digital devices, to the low-end digital devices, the vertical strategy requires the platform to test multiple device segments.

On the other side, the horizontal strategy does not allow the semiconductor manufacturers to use the same test platform to test new devices. In the case of a new product introduction, or demand fluctuations, the manufacturer must purchase a new test platform. The solution on the horizontal strategy test is very focused to the semiconductor device being tested. It relies on a niche market strategy by driving down cost, and delivering equal or more performance than the broad market strategy.

4.7 Manufacturing Floor

In the past, much of the arguments for the value of the vertical strategy centered on the increase utilization of the semiconductor test equipment due to the capabilities reconfiguring the tester from one device to another.

In interview with the two subcontractors, it became clear that due to the cost of downtime, and the capital cost of the semiconductor test equipment, semiconductor manufacturers do **NOT** "swap machines around" on a regular basis. The manufacturers plan semiconductor production test capacity, and only change the production test plan usually because of two conditions.

1. Substantial changes in volume. In the case the demand volume drops for the foreseeable future, manufacturers change the capacity planning. They swap the testers from one device to another semiconductor device. The manufacturers do not change test production planning daily, or hourly. If the demand increases for the foreseeable future, the floor will add production capability for the device. The manufacturer will attempt to reconfigure another tester with less capacity, or buy a new tester.

2. New product introduction. In the case that a new product gets introduced, the performance enhancements of the new semiconductor device drive the need for a new test platform. The performance enhancements are typical due to the effects of Moore's Law. In this case, the manufacturer must upgrade an old tester, or purchase a new tester in the case that the old tester can not be upgraded.

4.8 Scenario Analysis of Switching Costs

The scenario analysis is described to help understand the concept of switching costs. In the scenario as shown in figure 4.8.1, the manufacturer possesses no installed base. The manufacturer must make a decision between a flexible or focused platform solution. In other words, they must chose between the vertical and horizontal strategy. The value of the horizontal strategy comes from the focused solution for testing a specific device, translating into lower cost of testing. However, the vertical strategy offers decreased future switching costs if the capacity plan changes, or a new product introduction requires the test equipment to upgrade.

The second tier of the tree represents the second purchasing decision due to either a new device introduction or device volume fluctuation. Assuming the semiconductor manufacturer decided on the horizontal strategy in the first decision, the second decision once again mirrors the first decision.

However, assuming the semiconductor manufacturer decided on the vertical strategy in the first decision, the vertical installed base plays a significant role in the second decision. Because of the lower costs of switching of the flexible platform compared with the horizontal platform, the flexible installed base influences the manufacturer towards upgrading or changing the platform in connection with the vertical platform strategy.

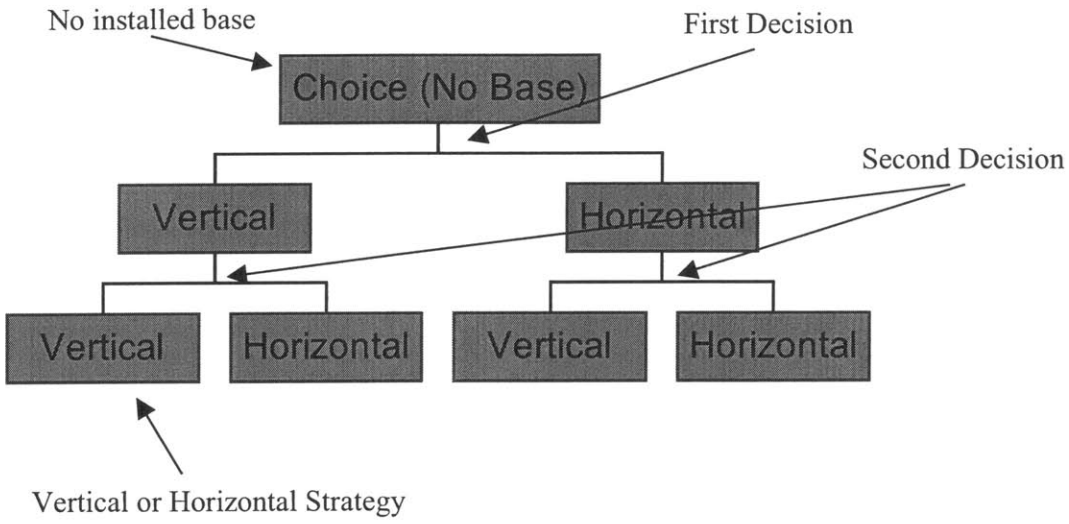


Figure 4.8.1 Decision Analysis to Value the Vertical and Horizontal Strategy[5]

In all cases, the vertical strategy decreases switching costs, while the horizontal strategy offers focused solutions to device testing, not affecting the future decision of the ATE purchases. The value of the vertical strategy comes from decreasing the switching cost for manufacturer when their tester needs change. The thesis provides a framework understand the customer's valuation of the flexible and focused solution.

4.9 Assumptions to Valuation

Section 4.8 proposed a method to think about the value of the vertical and horizontal strategies. As proposed in the previous section, the value of the horizontal strategy comes from the cost of test savings from a focus solution. It is easily calculated from a cost of test model.

The value the vertical strategy comes from the savings associated from switching. However, it is more difficult to determine the value associated with switching. In order to do so, this thesis makes several assumptions.

[5] The foundation of the scenario analysis comes from the test industry customer perspective.

The first assumption comes from ignoring competition within the semiconductor test industry. For instance, the model will compare only the horizontal and vertical strategies in the test industry. It will ignore competition between two companies using the vertical strategy. In addition, in order to value the solutions, this theory assumes parity in the platform offerings of each competitor, customer relationship strength, and company reputation. In chapter 6, we will relax this assumption and discuss test industry competition's effects on market strategy.

To begin, the *Price Premium of the ATE Product = the Perception of Product Differentiation from its Competitors + the Value of the Flexible Platform.*

In this case, looking at the horizontal and vertical strategy, the perception of the product differentiation comes from comparing the costs of the focused solution against the flexible solution for test equipment. In most cases, the horizontal strategy will offer better cost of test savings. The vertical strategy will offer better value in the case it becomes necessary to change the test production floor.

As mentioned previously, the horizontal cost savings will translate from simple cost of test calculations. The complexity comes from isolating the value of flexibility. In order to do so, the theory assumes that the value of flexibility comes from the savings in switching costs.

Therefore, the *Value of Flexibility = Switching Costs (Vertical to Horizontal) – Switching Costs (Vertical to Vertical).*

This thesis acknowledges that customers could switch from a vertical platform to another vertical platform from another manufacturer. However, assuming parity in performance, customer reputation, and customer relations, there would be no incentive for customers to do so. On the other hand, customer may feel that they can utilize the equipment without change for the entire depreciation life. In these cases, the customer might want to return to the focused solutions that offer direct cost of test savings without regard for future flexibility.

Using these equations for the value of flexibility, the proceeding chapters build a model to value flexibility based on defining and assessing the switching costs. The model is limited because it does not develop a framework to evaluate the cost to develop horizontal and vertical strategies. However, looking at it from a marketing lens, the differences in cost of the initial vertical and horizontal platform must not exceed the value obtained from the flexible strategy as describe in Chapter 5.

4.10 Chapter Summary

This chapter describes the horizontal and the vertical strategy. In theory, a purely horizontal strategy provides an independent platform solution targeting a specific segment of the market. For instance, many of the smaller ATE vendors such as Nextest focus on testing in the low-speed digital segment, offering better cost of test economics

per devices with less performance per pin. On the other hand, Agilent became the first large industry play to differentiate itself using the single platform or vertical strategy. It advertised itself as the "last platform you will ever need." [1]

Since manufacturing planning changes only in the case of sustained volume change or new product introduction, the main advantage of the vertical strategy comes from the decrease in switching cost from reconfiguring the tester as opposed to buying a new test platform. On the other side, the horizontal strategy offers a focused solution with better economics than the vertical strategy. The proceeding chapter describe a model to value the switching cost based on the equation that:

Value of Flexibility = Switching Costs (Vertical to Horizontal) – Switching Costs (Vertical to Vertical).

Chapter 5: Value of the Vertical and Horizontal Strategy

5.1 Introduction

This chapter discusses the valuation of the vertical and horizontal strategy using the switching cost analysis proposed in chapter 4. It divides the categories of switching cost into four main categories in order to break down the cost saving from switching for a vertical strategy. It also describes strategic threats to the vertical strategy, and uses game theory to determine the best strategy.

5.2 Value of Flexibility Model

An EXCEL model was created to determine the value of flexibility. The model divides the value flexibility into four broad categories: time to market, equipment and hardware, engineering, and production. Each subsection describes the categories.[1]

1. Time-to-market

The semiconductor manufacturer must plan for changing in production testing. Whether introducing a new semiconductor test device onto the new test platform or shifting device volume to another tester as mentioned in Chapter 4, the semiconductor manufacturer must develop a schedule to ramp the semiconductor production testing. The first category of cost from switching comes in this production-planning phase labeled time-to-market. Perhaps, it would be better to use the term "time to ramp manufacturing production".

Aggressive Production Ramp

When looking at the vertical strategy, because the test equipment is reconfigured rather than brand new, the semiconductor manufacturer can ramp production faster due to the familiarity. Teradyne uses a rule-of-thumb of 10% improvement in the manufacturing schedule because of the familiarity. Figure 5.2.1 shows a typical manufacturing ramp schedule, with a 10% improvement in ramping the manufacturing because of the familiarity. In the figure, the independent x-variable indicates the days to ramp. The y-variable indicates the percentage of throughput from the final production plan. The difference in throughput between the two ramp scenarios represents the opportunity costs for the production planning.

[1] Base costs for model calculations from customer perspective [4].

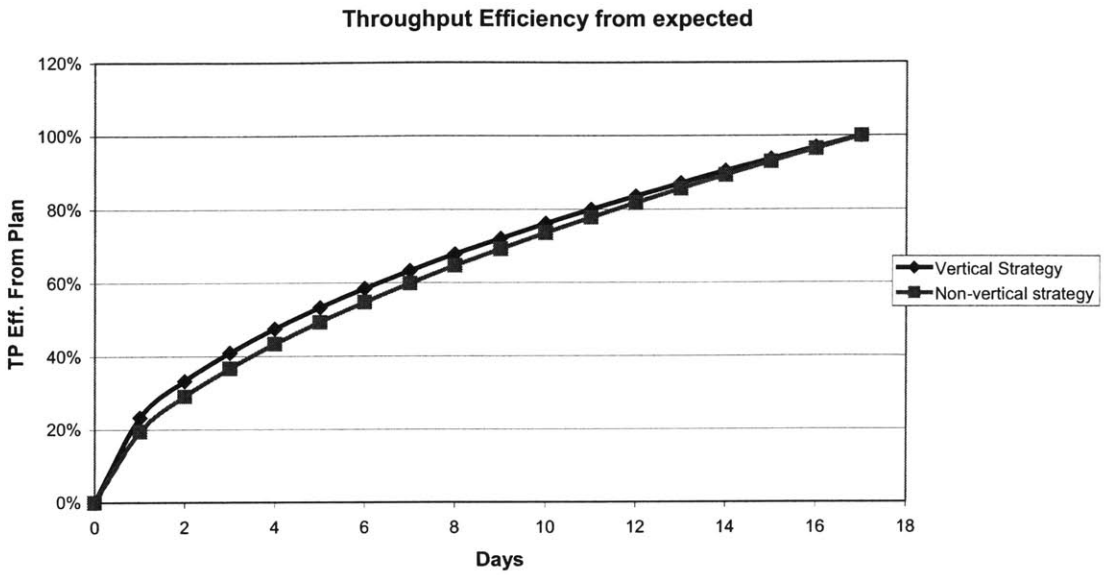


Figure 5.2.1 Production schedule ramp between horizontal and vertical strategy

As the manufacturing schedule ramps toward 100% of planned capacity, the two curves come closer. However, in the first 10 days, the learning curve for the vertical strategy results in greater throughput than the horizontal strategy. The greater throughput translates into opportunity costs for the devices. The model assumes the average selling price (ASP) of the semiconductor device as the opportunity costs.

Production Risk

In talking with semiconductor customers, it became apparent that upgrading a test configuration from a flexible platform is considerably less risky than buying a brand new unfamiliar platform. However, it was difficult to rate this intangible risk. In order to overcome this difficulty, the model translates all the risk of test production into risks for production slippage. In the case that things do not work out with the tester, the production schedule slips, and the consequences comes from the production slippage rather than from the complications of the test platform. In this way, the model values production risk.

The model assumes a linear risk profile, meaning that the risk of production slippage increases linearly with time. In the case of a flexible platform from a vertical strategy, the mitigation of risk is also estimate at 10% as in the production ramp improvement.

2. Equipment and Hardware

The equipment and hardware category encompasses all the costs from leveraging the installed hardware and equipment between flexible platforms, thus decreasing switching costs.

Maintenance and Spares

From the customer's perspective, the cost savings can come from leveraging current parts and maintenance training in flexible platforms in two ways. First, the common parts from the old platform and the flexible new platform results in lower inventory for spares. Second, it also results in lower costs for training maintenance workers. The value created for the customer depends on parts similarity between the flexible platforms. One must also consider the part similarities between the focused platforms. The switching cost savings comes from the greater parts commonality between flexible platforms.

Docking and Handling

Another aspect of savings comes in the form of docking and handling equipment. This model did not take into account switching cost savings associated with docking and handling for two reasons.

First, in many cases, companies hold one to one ratios of docking and handling equipment to testers. In the case of any volume growth, the semiconductor test industry customers must buy new docking and handling equipment. Therefore, in the case of volume growth, flexibility in platforms does not decrease switching costs.

Secondly, docking and handling equipment comes from 3rd party vendors. In most cases, the equipment is very flexible. They work with multiple testers. Therefore, the customer can already reconfigures the docker and handler to work with flexible as well as focused platforms. The universality of the docking and handling equipment means that flexible platforms provides no benefits above horizontal platforms in terms of switching.

3. Engineering

The engineering costs contain all the costs for extra engineering effort due to switching from one platform to another. The vertical strategy allows for cost savings associated with less engineering effort in order to switch from one platform to another.

Engineering Training

The first subcategory in engineering costs comes in the form of training. It is expensive to train engineers at the customer site. The model evaluates the costs savings associated with the accelerated training programs due to the engineer's pervious familiarity with the tester platform in the vertical strategy. In the past, platforms with common software language and library typical in vertical platform strategies cut training times by 50%.

Test Program Development

The typical test program development for semiconductor devices ranges from one to three months. The vertical strategy could decrease the time due to leveraging the knowledge from one platform to another, especially when reconfiguring the test floor for volume fluctuations. In the past, program developers cut test development time by10% to 50% depending on the complexity of the device. The model uses the 10% conservative value in the estimations.

Non-Recurring Engineering Costs (NRE)
The typical non-recurring engineering costs for DIB designs vary from $5,000 to $20,000. Common DIBs between tester platforms could save all the switching cost from one platform to another. On the probe side, the NRE for PIBs vary between $5,000 to $15,000. In addition, the probe card costs between $5,000 to $50,000 depending on the complexity of the wafer. However, more likely, the DIB/PIB design would show improvement rather than eliminate the entire costs of DIB/PIB development.

Mostly on the digital side, engineers must configure the new test platform to the Automated Test Pattern Generator (ATPG) or other Computer Aided Engineering (CAE) software. The conversion requires varying levels of effort depending on the complexity of the semiconductor chips. Less frequently, companies license conversion tools for pattern conversion costing between $5,000 to $20,000 annually for each user. These costs also vary depending on the design and functional complexity. The decreased NRE costs decrease with familiarity with test platforms by 10% to 15%.

4. Production Monitoring
Semiconductor manufacturers also incur costs during the production process.

Production Interface
In many cases, the semiconductor manufacturers have multiple pieces of test equipment from multiple vendors. The manufactures standardize the test floor by building an operational interface for the test equipment. Thus, the operator only need to understand one interface. Most often, the semiconductor manufacturers build this production operations interface for the tester. The software costs are small, and flexible platforms with standard software language and libraries usually present a 5% advantage over focused solutions.

Data Control Links
In addition, manufacturers must develop the data control links that interface the new platforms with the current production monitoring equipment. This along with the data analysis pack does have small software development costs, but usually present no advantage over competitors in switching costs.

Test Automation Tools
Also, semiconductor test companies often charge up to $20,000 to develop the automation tools to control the test floor. Companies can develop these tools themselves as well. Any software flexibility that allows easier development of the automation tools results in lowering development costs that can be passes onto the customer to lower switching costs.

5.3 Analysis of Results

The model provides enough flexibility to deal with varying device complexity, company charges, and ATE manufacturers. For each device and company, the model for the valuation of provides a unique solution. The solution determines the price premium that the customer is willing to pay for flexibility. The particular solution for the analysis in

the following sections comes from a specific company testing a high-speed data processing device. The model predicts a 20% premium for flexibility. This correlates with the 20% premium rule-of-thumb that many people quote in semiconductor industry.

Figure 5.3.1 shows allocation of the flexibility price premium of 20%. A vast majority of the premium for the vertical strategy comes from the time-to-market category. The opportunity cost of ramping the production faster provides the most cost savings in the vertical strategy. However, this value changes significantly with the change in complexity and subsequently the ASP of the semiconductor chip. The engineering costs cover approximately 19% of the switching costs premium, with Hardware and Equipment at 5%, and finally production monitoring at 2%.

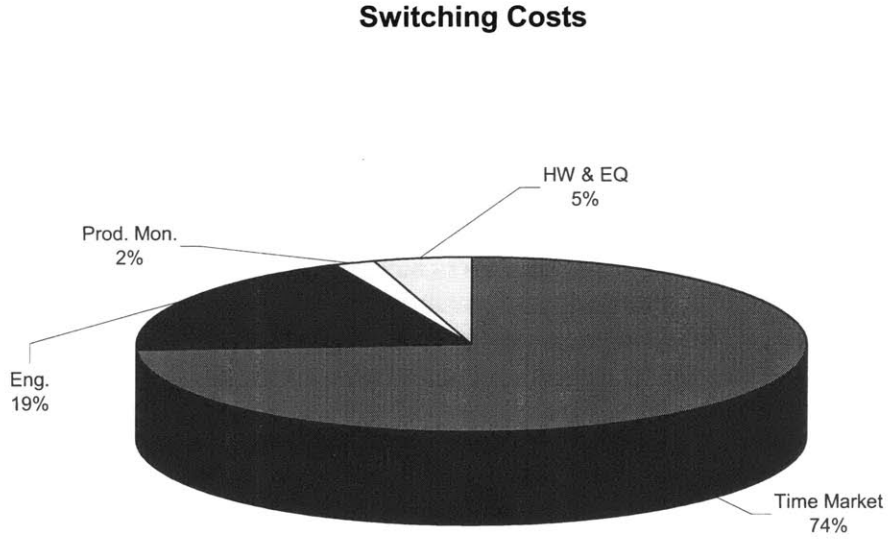


Figure 5.3.1 Switching Costs Savings Category Allocation

Figure 5.3.2 provides the sensitivity study for the flexibility valuation model. It describes the percentage change in the price premium for flexibility against a 1% change in the each major assumption in the model.

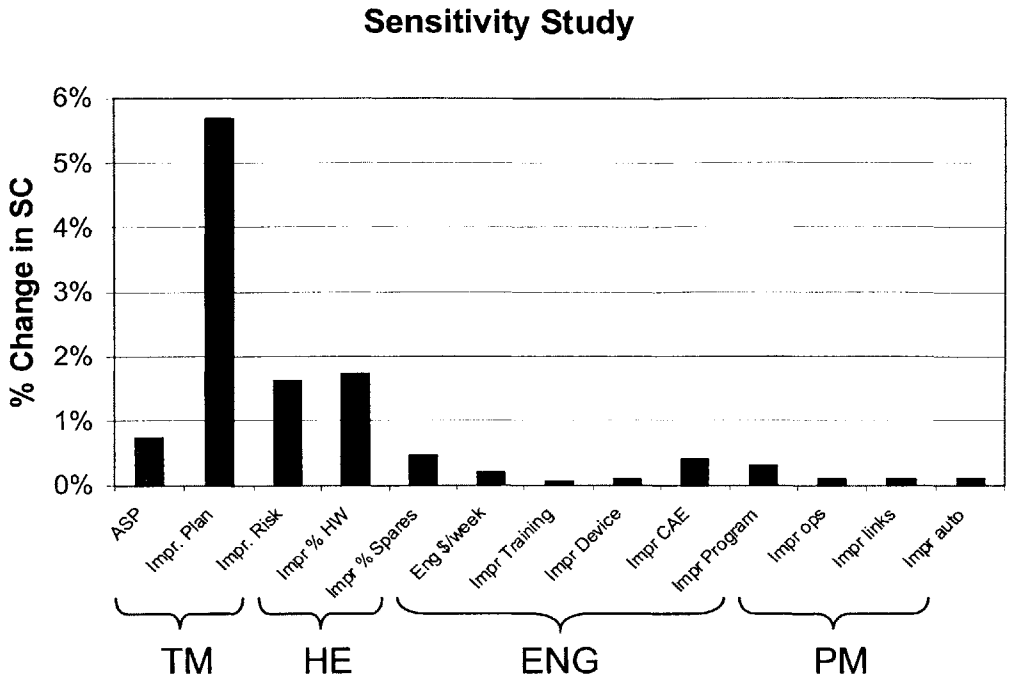


Figure 5.3.2 Sensitivity Study for Model to Value Switching Costs in Flexibility

In grouping the categories, the time-to-market (TM) category provides the greatest changes in the value of flexibility. The Hardware and Equipment (HE) categories provides nominal changes to the valuation of flexibility, while the engineering (ENG) and the production monitoring (PM) provides the least changes to the valuation of flexibility. In analyzing figure 5.3.2, changes in the improvement plan, improvement risk, and improvement percentage in hardware and equipment changes the switching cost savings of flexibility the most.

Sensitivity for Time to Market

The main assumption comes from the opportunity costs associated with faster production ramp. The sensitivity analysis shows that a 1% improvement in the production ramp plan increases the switching cost saving by over 5.5%. A 1% improvement in production risk improves the switching costs saving by over 1.5%.

Sensitivity for Hardware and Equipment

The main assumption that varies the sensitivity analysis comes from the improvement in flexibility from one competitor to another, and the costs of the handling and docking equipment. The study shows a 1.5% change in switching costs for 1% improvement in leveraging docking and handling flexibility. Other less sensitive assumptions comes from the annual charges on maintenance.

Sensitivity for Engineering

The main assumptions come from the time savings for training engineers in the flexible platforms compared with focused platforms, the complexity of the semiconductor devices to test, and the improvement assumptions. However, 1% improvement in any categories translates into less than 1% improvement in switching cost savings.

Sensitivity for Production Monitoring

The main assumption in the category lies the time to develop production operations interface, control data link, and tester automation tooling as well as the improvement in development time for flexible platforms. The model is not sensitive to these costs translating in less than 0.5% improvement with 1% improvement in flexibility.

5.4 Test Industry Application

Looking at it from the direction of the semiconductor test industry, this model provides a good guideline for the development of the vertical strategy. Due to the different definitions of the vertical strategy, using the model, the semiconductor test industry can evaluate important parameters in the vertical strategy. For instance, the greatest value for flexibility comes from the time-to-market segment. The priority in the product development strategy in the semiconductor test industry should focus on improving the production ramp speed, as well as mitigating the production slippage risks for the customers.

5.5 Game Theory for Customers of the Semiconductor Test Industry

In looking at the competition, this decision can be expressed in game theory. From the customer perspective, the advantage of a choosing a focused platform is the savings associated with the cost of test. The disadvantage of choosing a focused platform is that the customer needs to buy a new platform in the case that the test floor needs to change. The advantages of the flexible platform in the vertical strategy are the future cost saving associated with purchasing a flexible platform. The disadvantages are the greater cost for the flexible platform.

1. Game with no Change of Production Test Plans

The semiconductor device manufacturers look at the vertical and horizontal strategy using separate scenarios. Figure 5.5.1 shows the game when the manufacturers will never need to reconfigure the production test. They depreciate the test for its full life without reconfiguring the tester. In addition, the new devices introduced require so much new technology to test that the manufacturer must buy a new platform to test the device.

As with most game theory results, the left column represents the decisions of the semiconductor manufacturer, the top row represents the decisions of the competition in the semiconductor industry. The matrix represents the gains and losses for the semiconductor manufacturer and the competition with each decision.

No Change in production test plan

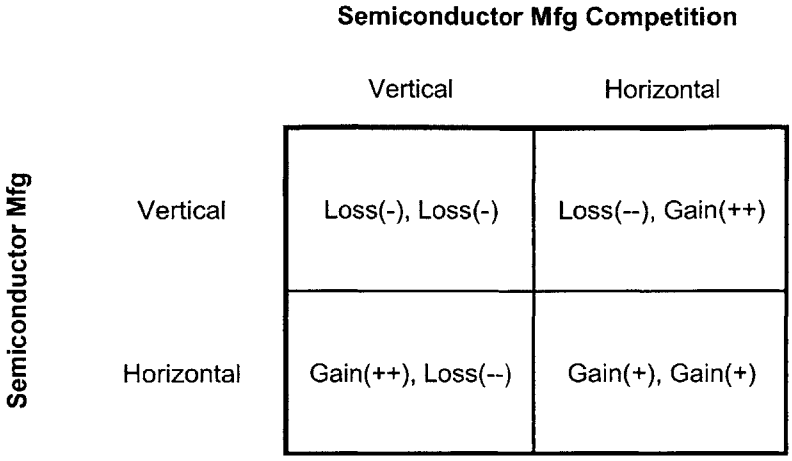


Figure 5.5.1 Game Results with no Change in Production Test Plan

In the event that there is no change in the production test plan for the life of the tester, the semiconductor manufacturer should choose the horizontal strategy. Since it will never switch testers, the manufacturer will never benefit from the savings in switching costs from the vertical strategy. It would gain (++) if the competition decides to buy test machines with the vertical strategy, because if would gain a test cost advantage over its competitors who paid for the benefits of reduced switching costs. In effect the competition bought an option to decrease test costs in case switching occurred, but had no opportunity to exercise the option.

2. Game with Changes of Production Test Plans
Figure 5.5.2 shows the game when the manufacturers will need to reconfigure the production test plan.

Change in production test plan

Semiconductor Mfg		Semiconductor Mfg Competition: Vertical	Semiconductor Mfg Competition: Horizontal
	Vertical	Gain(+), Gain(+)	Gain(++), Loss(--)
	Horizontal	Loss(--), Gain(++)	Loss(-), Loss(-)

Figure 5.5.2 Game Results with Change in Production Test Plan

In the event that there is a change in the production test plan, the semiconductor manufacturer should choose the vertical strategy. Since it will switch testers, the manufacturer will benefit from the savings in switching costs from the vertical strategy. It would gain (++) if the competition decides to buy test machines with the horizontal strategy, because if would gain a test cost advantage over its competitors who did not pay for the benefits of reduced switching costs, and needed to switch. In effect the customer bought and exercised an option to decrease test costs in case switching occurred.

5.6 Probability of Changes in Production Test Planning

In valuing the gains and losses, one should use the proposed model in the beginning of this chapter. The current macroeconomic climate resulted in uncertainty of the production volume and production test planning. Therefore, the industry is moving towards the vertical test strategy. However, will this trend continue in the event that the economy recovers in the near future?

1. Re-examination of Moore's Law

Looking back at section 3.1, much of the semiconductor complexity is driven by Moore's Law. In addition to driving the pace of innovation of microprocessors, the pace of technological innovation in all segments of the semiconductor test industry feels this pressure to innovate. The relative high clock speed of the industry as described by Fine (1998) continually develops higher performance technologies. These new semiconductor technologies will require new tester capabilities, forcing the manufacturer to upgrade the production tester.

2. Volume Fluctuation

It's difficult to imagine a time when the semiconductor industry will once again feel confident in its volume predictions. In talking with the major semiconductor manufacturers, without exception, they concluded that it would be valuable to have an

option to reconfigure the tester rather than buy a brand new test platform for changing demands.

5.7 Test Strategy Recommendations

Customers who want flexibility are still concerned with cost. It becomes difficult to judge which is more important. The model presents a method to value flexibility for the semiconductor test customer. So long as the cost of the flexible platform solution does not exceed the price premium for that solution, the game theory holds. Further analysis is required to determine whether the product development costs allows for Teradyne to build and offer products within the price premium.

As described above, because of the inevitable need to change the test floor, as well as the customer value in purchasing the option to reconfigure the tester in the vertical strategy, the large ATE manufacturers would gain the most by employing the vertical strategy. In addition, it allows the large ATE manufacturers to gain a larger price premium for their products compensating for the larger fixed costs of large ATE manufacturers as compared with the smaller ATE vendors. The next chapter further discusses the implication of fixed costs for large ATE vendors.

5.8 Product Mix Limitations

Even with the valuation of flexibility, and a clear understanding of the tradeoffs that occur in the product development process, a closer examination of the vertical strategy belies some strategic risks, especially in the area of product innovation.

For example, Agilent made a conscious decision to de-emphasize the low-speed digital markets such as the smart cards, and micro-controller markets with their flexible 93000 series tester. Because of certain fixed designed-in costs of the 93000, and limitations of the scalable architecture such as the water-cooled design, the Agilent does not compete well in the economics sensitive low-speed digital semiconductor device segments. Figure 5.8.1 shows the positioning of the Agilent products.

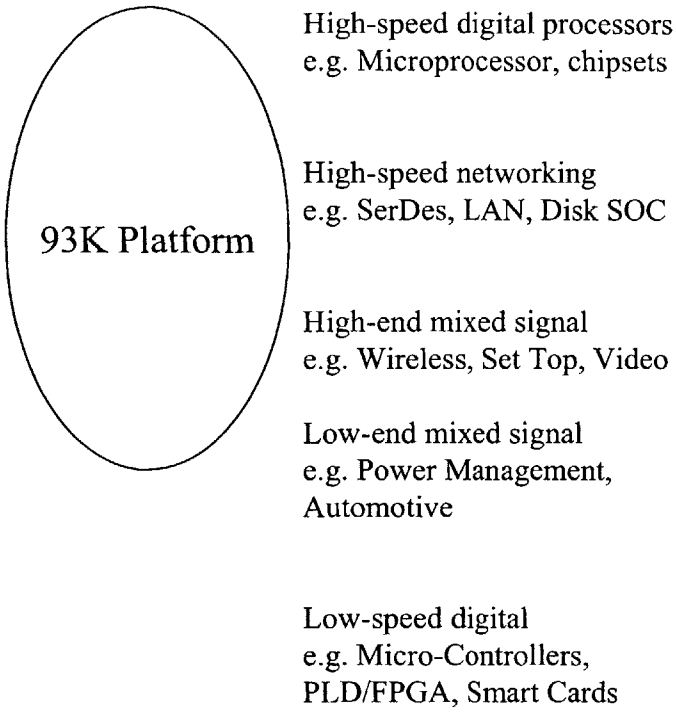


Figure 5.8.1 Agilent Market Position

5.9 Chapter Summary

One of the biggest challenges for all the large-scale manufacturers of ATE is to compromise the economic sensitive segments with the fixed designed-in costs of a single platform. On one hand, the vertical strategy presents some challenges to fill the low-end economically sensitive segments. On the other hand, the vertical strategy allows the large ATE companies to get a premium for their products due to the decreased switching costs, allowing them to better compete with the smaller, more cost effective ATE solutions. This chapter provides a model to value that vertical strategy.

Chapter 6: Other Considerations for the Vertical and Horizontal Strategy

6.1 Introduction

Much of Chapter 5 discusses the price premium that ATE vendors could charge for a flexible ATE platform that provides solutions for the entire market segment in a very tangible framework. Beyond the costing concerns, this chapter discusses the strategic risks and rewards in the vertical and horizontal strategy. The intangible nature of these risks and rewards does not lend itself to building a tangible model, but rather a discussion of the possibilities that Teradyne should consider in formulating its product strategy.

6.2 Understanding the "Attacker's Advantage"

The term "attacker's advantage" as coined by Foster (1986) comes from the inherent weakness of the firm in limiting the dynamics of technical development as described in 6.3, and organization weakness as described in 6.4. Although Christensen (2000) extends the theory by using these examples to illustrate disruptive technologies, this thesis only argues that technological development in respects to the technological S-Curve gives rise to inherent weakness that competitors can exploit. The concept of possible disruptive technologies on the semiconductor test industry goes beyond the scope of this thesis.

1. History

In much of the literature involved in technical innovation, and the study of the companies that win and lose, Foster (1986) first described the notion that established firms in the technology industry bore inherent strategic weaknesses as compared with smaller firms, dubbing it as the "attacker's advantage". In further studies, Henderson and Clark (1990) as well as Henderson's architectural innovation paper (1993) used examples in the photolithography industry to explain the technological development limitations to established firm. Later Christensen and Bower (1996) continued to examine the inherent organizational weaknesses in established firms. The changes in the semiconductor industry parallel the empirical examples given from both these studies. In all these cases, the "attacker's advantage" resulted in significant market share loss to the established firms.

2. Technology S-Curve

Many of the empirical studies in technology industries chart a technological development trend towards greater performance capability. For instance, Christensen and Bower (1996) studied the disk drive industry to determine that as time progressed, companies such as Seagate Technologies developed disk drives with more and more capabilities. Smother (1990) also documented the trend towards greater performance of American Automotive Manufacturers. For instance, GM in the 1970s and 1980s built bigger, and faster cars. Many writers including Foster (1986), later echoed by Christensen (1992), described this effect as the technological S-Curve, as shown in Figure 5.9.1, meaning as technology develops, the product performance gets better, and the engineering effort to develop the product gets greater.

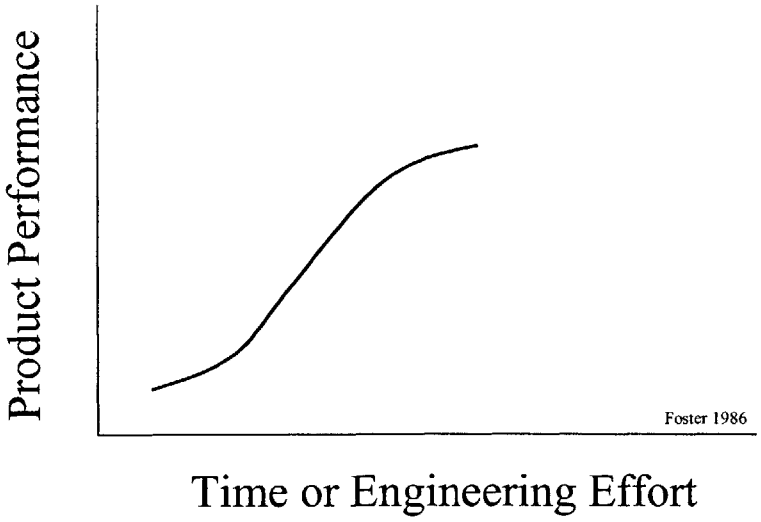


Figure 6.2.1 The Technology S-Curve

In much of the same way, technological performance in the semiconductor test industry continues to increase rapidly. Figure 5.9.2 shows the increasing number of pins in the test head (pin count) of digital ATE with each product innovation as time progressed. Because the complexity of the semiconductor devices drives the number of pins for those devices, in order for the ATE to test the semiconductors, the ATE manufacturer designs a greater number of pins in the test head in order to accommodate the semiconductor pins. Chapter 3 discussed the issues in semiconductor chips, especially the significance of the number of pins on the test head (pin count) in complexity, that mark technical development in the semiconductor ATE.

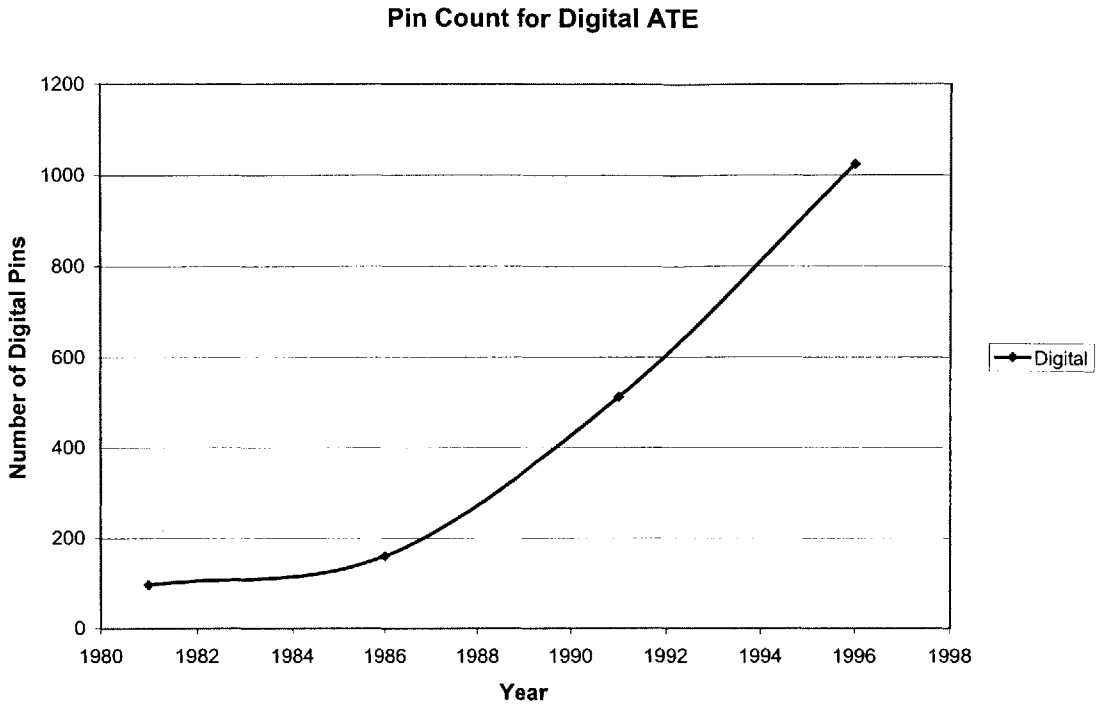


Figure 6.2.2 Digital Pin Count for ATE

6.3 Limitations in the Dynamics of Technical Development

Henderson and Clark (1990) proposed that the establishment of a technical paradigm moves the technological development towards incremental and modular improvements that specifically drive performance and cost efficiency. Using the example of the photolithography aligners industry, Henderson (1993) determined that engineers within a specific technology paradigm mirrored the technology itself. These engineers, and the organizational structure to which they belonged facilitated improvements on the component level as well as the refinements in the interactions between the components. With each shift in the photolithography aligner technology, established firms failed to develop new architectures successfully. In fact, engineers could not see beyond their established technological paradigm or understand the difference and superiority of the new technology architecture. Ultimately, the new technology architecture became dominant in the industry driving the old technology out of business. Christensen and Rosenbloom (1995) also documented empirical examples in the VCR industry with the failure of RCA and Ampex to successfully compete, and the failure of firms to change technology paradigms as disk drives became smaller in the disk drive industry.

6.4 Organizational Weakness

Bower (1972) observed that resource allocation, especially the funding for projects, comes from the middle levels of the organization. The theory states that industry ideas do not usually come from the tops of the organizations. The middle managers make decisions for their resource allocation. These decision filter up in the organization.

Bower noted that managers receive career advancements with successful projects, and career derailments for unsuccessful projects. Although in some cases managers do not get penalized for projects that fail due to problems with technological delivery, project that fail because of little or no market demand does lead to dire consequences for most managers.

In looking at the allocation of resources, the high-end segments typically require greater technology performance, possess less competitive pressure because of the high barriers to entry, and expected profits are higher because customer typically demand greater performance. Therefore, a middle manager usually chooses projects in these segments. Christensen (2000) proposed a conversation, in which the middle manager sees the high-end market, and rightfully decides on these markets because of the risks associated with competing in the lower-end or emerging markets. Because of this resource allocation process, organizations develop products with greater performance, and engineering effort.

Furthermore, the movement towards greater complexity for the technical product continues to add cost into the organizational structure, inherently adding more overhead costs to the products. In fact, because of the economic pressures in the low-end segments, these costs make it difficult for firms to move their performance downwards in order to compete with entrants that possess less technological advantage, but lower costs structures.

In the event that the attackers with low cost structure develop products to compete with larger firms, the attackers possess an inherent cost advantage because of the lower fixed costs in the organizational structure.

6.5 Strategic Risk Examples

Christensen (2000) gives several studies on the "attacker's advantage" with examples from the disk drive, steel, copier, computer, and many other industries. Smothers (1990) also documented these risks from the attackers in the automotive industry with the Japanese firms gaining market hold with cheap, fuel efficient cars. In all these cases, established companies concentrated on technological performance, leaving neglected markets for emerging competitors to gain foothold in the industry. Ultimately, the competitors that gain foothold eventually developed better products that resulted in taking market share away from the larger, more established firms.

The semiconductor test industry, namely the printed circuit board test industry, underwent this similar phenomenon in the 1970s. At that time, the functional test of the printed circuit board mimicked the natural input/output of the board. As the products developed with speed and performance, the spending for the test equipment went up exponentially. The ATE test instruments usually took from 6 to 9 months to develop. Teradyne' engineering expertise made it a leader in the functional testing of printed circuit boards. However, as the push for economical testing became apparent, the industry began to develop pattern generators. Teradyne led this drive because of its compatibility with the functional testing paradigm.

However, in the 1980's, the push for economics especially in the lower-end segments such as the consumer segment led to the propagation of in-circuit testing in consumer segment. The specification conscious industries such as the automotive industry, the defense industry, and the telecommunications industry still focused on functional test. Teradyne followed its primary customers developing it functional test capabilities because of the profits in the higher-end market segments, while leaving in-circuit testing to smaller companies.

In the 1990's the high density of the boards resulted in too many solder joints on the board to test functionally. In-circuit test technology became more reliable, and function testing became infeasible. The telecommunications, automotive, and defense industries began to design their boards like the consumer segment. Teradyne began to lose market share and lost much of the business to other competitors because of its dedication to functional testing.[3]

6.6 Evaluation of Competition in the Semiconductor Test Industry

Table 6.6.1 provides a summary of the player, concerns, and the development strategies in the semiconductor test industry. The large ATE competitors focus on customer needs and developing the vertical strategy, while the small ATE competitors focus on decreasing the cost of testing and developing the horizontal strategy. The term competition refers to all the competitors in the ATE industry, while the attackers refer to the small ATE companies that are attacking the large ATE companies.

Company	Size	Primary Concern	Development Strategy
Agilent	Large	Customer Needs	Vertical
Advantest	Large	Customer Needs	Vertical
Credence	Large	Customer Needs	Vertical/Horizontal
Eagle	Small	Cost of Test	Horizontal
LTX	Large	Customer Needs	Vertical
Nextest	Small	Cost of Test	Horizontal
NPTest	Large	Customer Needs	Vertical
Teradyne	Large	Customer Needs	Vertical

*Customer needs is a combination of performance and cost of test

Table 6.6.1 Competition in the Semiconductor Test Industry

In analyzing the risks and rewards of the vertical and horizontal strategy, it is important to once again look at the first mover on the vertical strategy Agilent. The end of Chapter 5 discussed some limitations to the product strategy of Agilent. The high fixed-costs of the flexible platform made it difficult for Agilent to compete in the low-end cost sensitive markets. The second mover Teradyne is trying to examine the cost efficacy of including the low-end market in its vertical strategy. In addition, I imagine that as the other large ATE manufacturers begin to implement the vertical strategy, they feel the same types of pressure. On the other hand, the smaller competitors such as Eagle and Nextest focus on

[3] Account taken from [64].

niche solutions that target specific market segments in the low-end. They focus on providing lower cost solutions that the larger ATE companies.

In many ways, the semiconductor test industry follows the same phenomenon as the industries that became susceptible and eventually lost market share because of the "attacker's advantage". As you recall from the first "attacker's advantage" as described in section 6.3 (Limitations in the Dynamics of Technical Development), the establishment of a technical paradigm moves the technological development towards incremental and modular improvements that specifically drive performance and cost efficiency. This technical paradigm hinders the dynamics of product innovation in other technical paradigms. In this case, the development of the single flexible platform sets the technical paradigm for Teradyne beyond the horizontal strategy. Because of the greater investment in the one platform, most of the investment will go toward incremental and modular improvements to drive performance and cost efficiency. Although this occurs with the horizontal strategy, the diversified platforms to cover each specific segments of the market, as well as the lower platform investments allows for easier introduction of new platforms and technologies.

The second advantage, as describe in section 6.4, established firms develop a cycle of investment in high-performance products that leads to high-cost structures that leads again to the development of greater technical performance in the products to get greater margins. In much of the same way, large ATE manufacturers are developing higher-performance products to respond to the lower-cost niche competitors. In the end, the low-end competitors develop their capabilities and threaten the larger companies.

6.7 Game Theory for the Semiconductor Test Equipment Manufacturer

In looking at the semiconductor test equipment competition, this decision can also be expressed in game theory. From Teradyne's perspective, the move towards vertical strategy makes it susceptible to niche and horizontal market player that could develop strong market power. The advantage of the vertical strategy is the demand of the customer, as well as the price premium for the product.

1. Development of Sustaining Technology

In this first scenario, this paper assumes that the current methods of testing will continue. The customer will test the semiconductor devices functionally. Technology development will drive the complexity of the test equipment, and the current technology will incrementally improve to test new semiconductor devices. Customers will not change the design paradigm of functional testing. Also, competition in the semiconductor test industry will not change the functional testing paradigm. The left hand column of the game represents the decisions of Teradyne, the top row represents the decisions of the competition in the semiconductor test industry.

Figure 6.7.1 shows the results of the game played under these circumstances in the semiconductor test industry. In this case, there is no fear from the attacker's advantage. Although smaller competitors still possess a cost advantage, the premium charged for flexible platforms using the vertical strategy can negate the smaller competitors cost

advantages because customer want the "real option" of reconfiguring the test equipment that the vertical strategy enables. In this case, Teradyne would choose the vertical strategy. In addition, if the competition chooses the horizontal strategy, Teradyne would gain even more.

Development of sustaining technologies

		Competition	
		Vertical	Horizontal
Teradyne	Vertical	Gain(+), Gain(+)	Gain(++), Loss(--)
	Horizontal	Loss(--), Gain(++)	Loss(-), Loss(-)

Figure 6.7.1 Game Results Assuming Development of Sustaining Technologies

2. Development of New Technologies (Radical Innovation)
In the second scenario, this paper assumes that the current methods of testing will not continue. Technology development in the semiconductor test industry will create new methods to test semiconductor devices changing the test technology. This paper used the new technology and radical innovation synonymously.

Figure 6.7.2 shows the results of the game played under these circumstances in the semiconductor test industry. In this case, the attacker's advantage will exhibit itself. The vertical strategy will dedicate the investment and resources of Teradyne into the single vertical platform, making it less able to adapt to new technologies. In this case, choosing the vertical strategy will result in future losses. On the other hand, the horizontal strategy will allow a firm to focus on niche and emerging segments making it less susceptible to the "attackers advantage" from new technologies.

Development of new technology

Competition

Teradyne		Vertical	Horizontal
	Vertical	Loss(-), Loss(-)	Loss(--), Gain(++)
	Horizontal	Gain(++), Loss(--)	Gain(+), Gain(+)

Figure 6.7.2 Game Results Assuming Development of New Technologies

6.8 Probability of Development of New Technology

In valuing the gains and losses associated with the game within the semiconductor test industry, one cannot tangibly model them like the game with the semiconductor manufacturers. However the risks are very real, and one must decide without fully understanding the tangible risks involved. Because of the intangible aspect of these risks, one must examine the likelihood of the development of new technologies.

1. Inevitability of Radical Innovation

Although the clock speed of an industry varies depending on the technology, I cannot think of an industry where the technology developed incrementally forever. All the examples previously mentioned (e.g. automotive, motorcycle, printed circuit board) experienced new technology innovation more radical than incremental improvement on existing technologies. In fact, Christensen (2000) argues that these radical innovations are inevitable. The next chapter describes the market dynamics showing the inevitability of radical innovation in the semiconductor test industry as well.

2. Time Frame for Innovation

The game from section 5.5 yielded the recommendation for the vertical strategy. However, the game from 6.7 yields the recommendation for the horizontal strategy because of the inevitability of new technology development. While on the surface they conflict, the game played in section 5.5 is being played right now. For instance, customers of the test equipment must decide today on the flexible or focused platform. This thesis uses short-term to describe the decision between the vertical and horizontal strategy from the side of the customer of the semiconductor test industry.

On the other hand, the game played in section 6.7 among the semiconductor test industry itself has a larger time span. It takes time for the industry to accept the radical innovations. It also takes time for the radical innovation to gain market advantage.

6.9 Recommendations to React to Competition in the Test Industry

The recommendations come from the review of the games played, and the probability of each game.

1. Use the vertical strategy to command a price premium over the niche players

The focused platforms are built with lower cost of test partially due to the lower cost structure of small ATE firms, and their focus on cost of test reduction rather than serving customer needs, which the small competitors (attackers) view as a competitive advantage. In order to compete effectively in the short-term, the large test manufacturers should developed flexible platforms solutions. Thus, the large manufacturers can command a price premium for flexible platforms within the vertical strategy to support their fixed costs. This premium is especially important to overcome the cost advantages for the economically sensitive low-end segment.

2. Enable the flexible platforms to test low-end products

While Agilent abandoned the low-end segment and Teradyne is considering the cost efficacy of the low-end segment, it is important to evaluate the risks from the "attacker's advantage". I understand the cost difficulties associated with using the building a flexible platform that competes effectively in the cost sensitive low-end segments. However, because of the risks from the attackers, it is especially important for Teradyne not to completely abandon the low-end segments.

3. Competition in the low-end segments will diminish the risks from the attackers

The three reasons for participating in these segments comes from the lessons learned in the printed circuit board industry. (1) In participating in niche and low-end market segments, companies become familiar with new technologies and understanding emerging and niche markets. It allows established companies to respond faster to market threats. (2) Established companies that look to participate in niche markets have a better vision of the market development and niche possibilities. Teradyne designers can look at the test industry from an economics rather than performance paradigm. (3) Participating in the niche or low-end segments develops cost effective design discipline in developing test products. It allows Teradyne to slow the high performance, high cost structure cycle.

4. Teradyne should look beyond the horizontal and vertical strategy

While the initial project description only asks to evaluate the advantages and risks of the two product strategies (which was done in Chapter 5 and 6), the research determined that the current framework, which compares the horizontal and vertical strategy, is insufficient to help make a determination for the long-term strategy in the semiconductor test industry. The test industry should respond in the long-term without the constraints of making the decision to either employ the horizontal or vertical strategy. The next chapter discusses the market dynamics beyond looking at

the horizontal and vertical strategies. It will discuss changes in business strategy to minimize the "attacker's advantage" in the long-term, while employing the vertical strategy in the short-term.

6.10 Chapter Summary

This chapter describes the strategic challenges posed by the industry move towards the vertical strategy. It explain the issues posed by the "attacker's advantage" as proposed by Foster (1986) in which companies abandon the low-end segments allowing competitors to survive, grow, and increase in market share. In this case, the large semiconductor test manufacturers exhibit the tendency of all the incumbent firms before they lost market share to smaller attackers. The move towards a vertical strategy will make large test equipment manufacturers even more susceptible to the "attacker's advantage". Thus far, the thesis focused primarily on the question of horizontal and vertical strategy as applied to test equipment platforms, describing either the focused or the flexible platform. The following chapter breaks out of the constrictive horizontal and vertical thinking in examining the market dynamics and product strategy.

Chapter 7: Assessment of Market Dynamics in the Semiconductor Test Industry

7.1 Perspectives in the Semiconductor Industry

This chapter uses systems dynamics to understand the effects of these trends described in chapter 3 on the future of the semiconductor test markets. The dynamics analyzes three segments of the value chain that drives the semiconductor test industry.

1. End customers: the demands of the end customers for application such as computer, PDAs, cable modem services, or cable televisions ultimately drives the demand for semiconductors, which affects the semiconductor test industry.

2. Semiconductor manufacturers: the semiconductor manufacturers are the customers of the semiconductor test industry. The semiconductor test industry sells most of its equipment to these manufacturers. They will dictate much of the dynamics in the semiconductor test industry.

3. Semiconductor test industry: the competition in the semiconductor test industry will also drive the future market dynamics of semiconductor testing.

7.2 End Customer Perspective

Figure 7.2.1 shows the customer's expectations for price and performance, and its relation to the semiconductor test industry. The end customer's willingness to buy the product, containing the semiconductor device, influences the average selling price (ASP) of the semiconductors. The ASP pressures the manufacturers to meet the cost and performance requirements. The manufacturers pressure the semiconductor test industry. The pressure affects the cost of testing and also the cost of manufacturing the semiconductors. The cost of manufacturing the semiconductor devices influences the customer expectations.

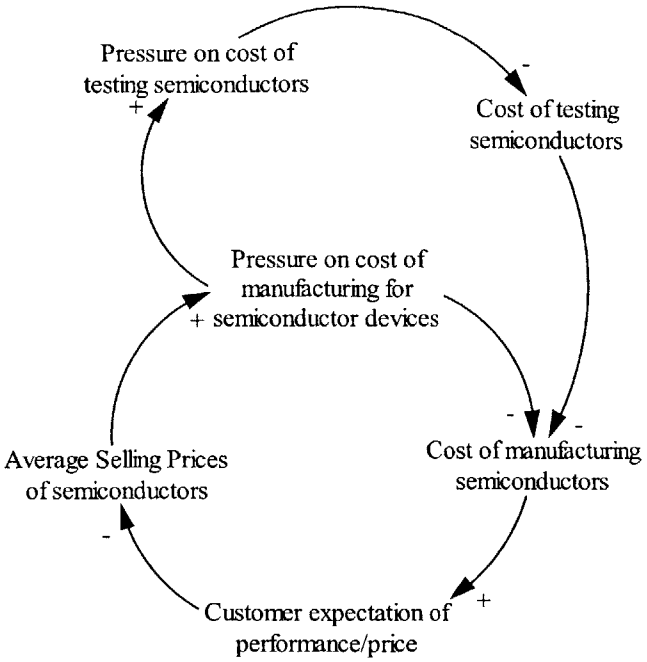
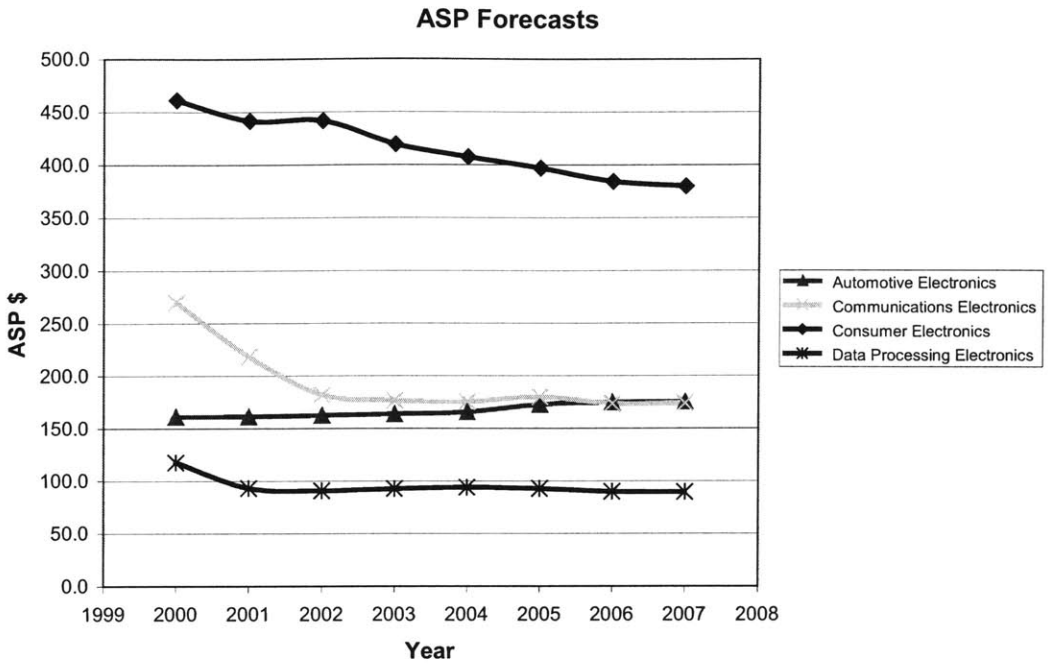


Figure 7.2.1 Systems Dynamics Model of End Customer Effects on Test Industry

1. Price trends
Since the late 1990s, average selling price (ASP) of semiconductor devices decreased by almost 40%. The dropping ASP squeezes the profits for semiconductor manufacturers resulting in pressure to reduce the cost of manufacturing. In the future, the continued standardization and economies of scale around CMOS processes in the semiconductor industry will continue to drive the cost of semiconductor chips down.

In addition, the estimate future ASP of the devices as shown in Figure 7.2.2 continues to drop putting continued pressure on the manufacturing industry to drive cost out of semiconductor manufacturing and production.



7.2.1 Average Selling Price (ASP) Forecasts[1]

2. Manufacturing Costs

The market pressures to reduce semiconductor costs translated in the continued drop in the manufacturing costs per transistor. However, the cost of testing semiconductor devices does not mirror the economies of scale and cost reduction as the manufacturing. In response to the reduction in manufacturing costs, and the subsequent rise in test costs in semiconductor production, the semiconductor industry pushes towards improvements in the cost of testing semiconductors as shown in Figure 7.2.3.

[1] Market data from [27].

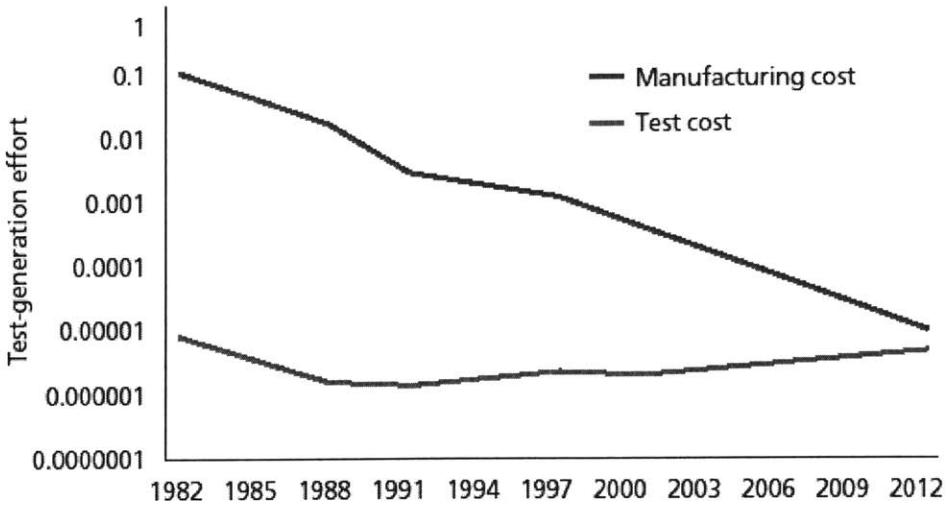


Figure 7.2.3 Test and Manufacturing Costs for Semiconductor Production [25]

7.3 Semiconductor Manufacturing Perspective

Figure 7.3.1 shows the systems dynamics for the semiconductor manufacturing industry. As in chapter 2, we discussed the disintegration of the value chain and the move of the industry towards the outsourcing model. With this rise, the barriers to entry for the production of semiconductor devices will decrease because semiconductor designers no longer need the large capital required to build foundries to produce devices. Therefore, the per-unit cost for devices will intensify competition in the semiconductor industry. As this occurs, it will increase the cost of test pressure for the industry with the same intensity as the eroding average selling prices.

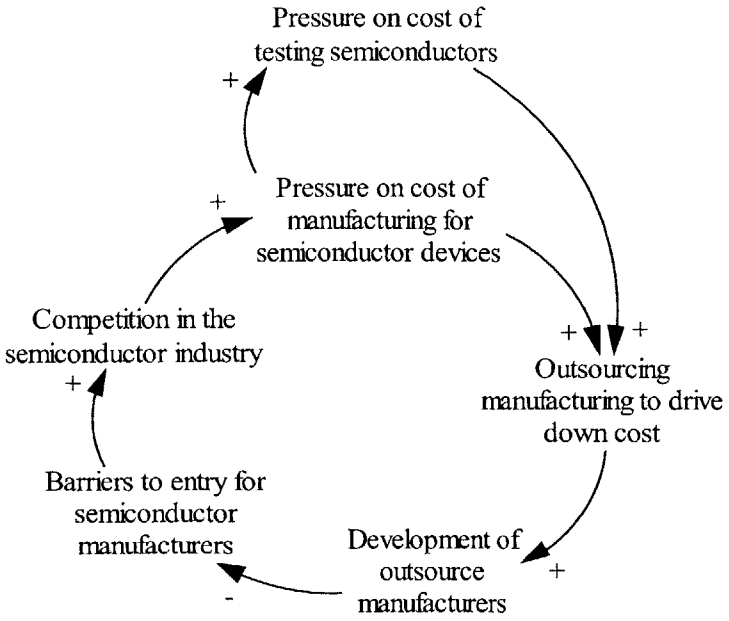


Figure 7.3.1 Model of Semiconductor Manufacturer's Effects on Test Industry

7.4 Test industry Perspective

Figure 7.4.1 shows the dynamics of the semiconductor test industry in competition with itself to reduce the cost of testing semiconductors. The manufacturer of semiconductor can decrease pressure for the cost of test in two ways.

1. Pressure the semiconductor test industry to decrease the cost of testing the devices.

2. Design the cost of testing out of the semiconductor devices using techniques such as built in self-test (BIST), scan (commonly used), and other design for test techniques.

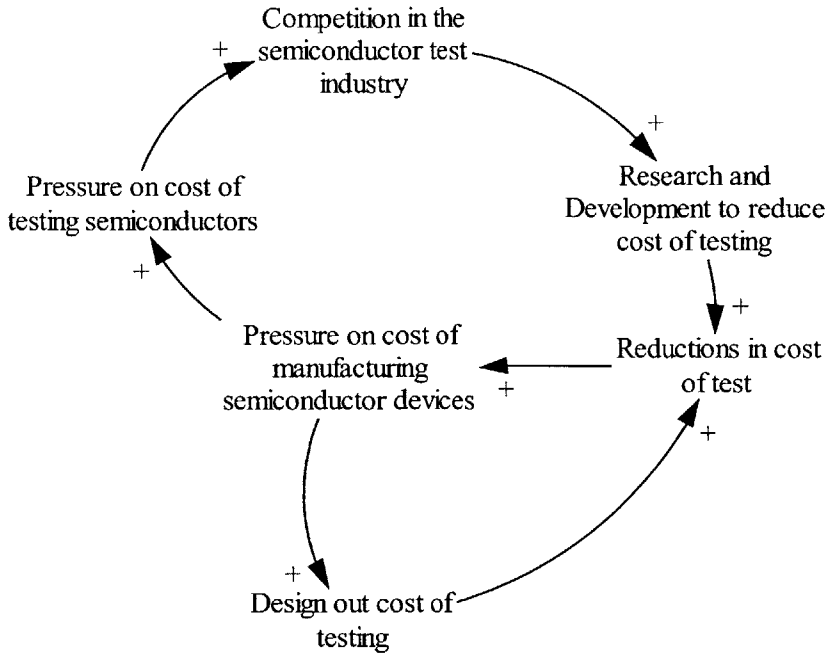


Figure 7.4.1 Model of the Semiconductor Test Industry Competition

Figure 7.4.2 shows the financial summary of the semiconductor test industry. It shows the average gross margins, average net income as a percentage of sales, and average research and development as a percentage of sales spending for all publicly traded semiconductor test manufacturing companies. As shown in Figure 7.4.2, the pace of research and development as a percentage of sales continues at its tremendous pace even as net income as a percentage of sales and gross margins decline substantially after the year 2000.

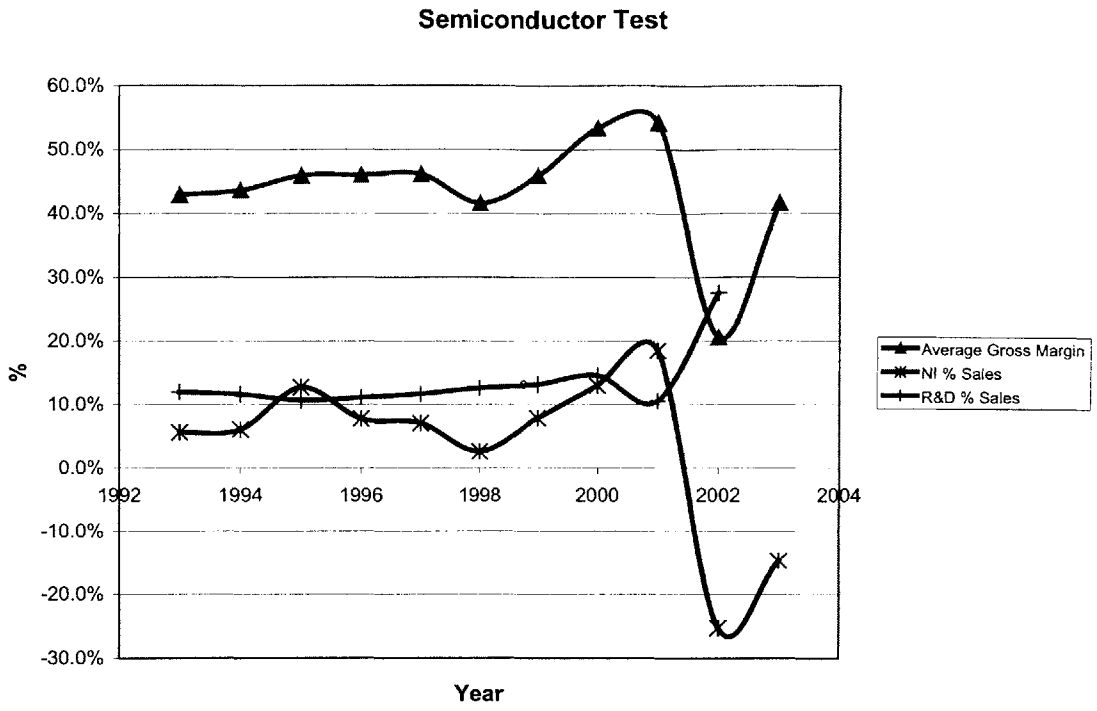


Figure 7.4.2 Financials of the Semiconductor Test Industry[2]

7.5 Dynamic Model of the Semiconductor Test Market

An EXCEL model of the market was created to predict the future market revenue for semiconductor test equipment. It unites the systems dynamics from the end-customer, semiconductor manufacturer, and test industry perspectives in predicting the future market demand for semiconductor capital equipment.

Figure 7.5.1 shows abbreviated interactions (without all the loops as in the models above) of all three perspectives into the semiconductor industry and semiconductor test industry. The pressure from cost of testing comes ultimately from the end customer, and the competition in the semiconductor industry. The semiconductor manufacturer reduces the cost of test by designing cost out of the semiconductor device, or it pressure the semiconductor industry to decrease costs.

[2] Data retrieved from Thompson's Financial Database.

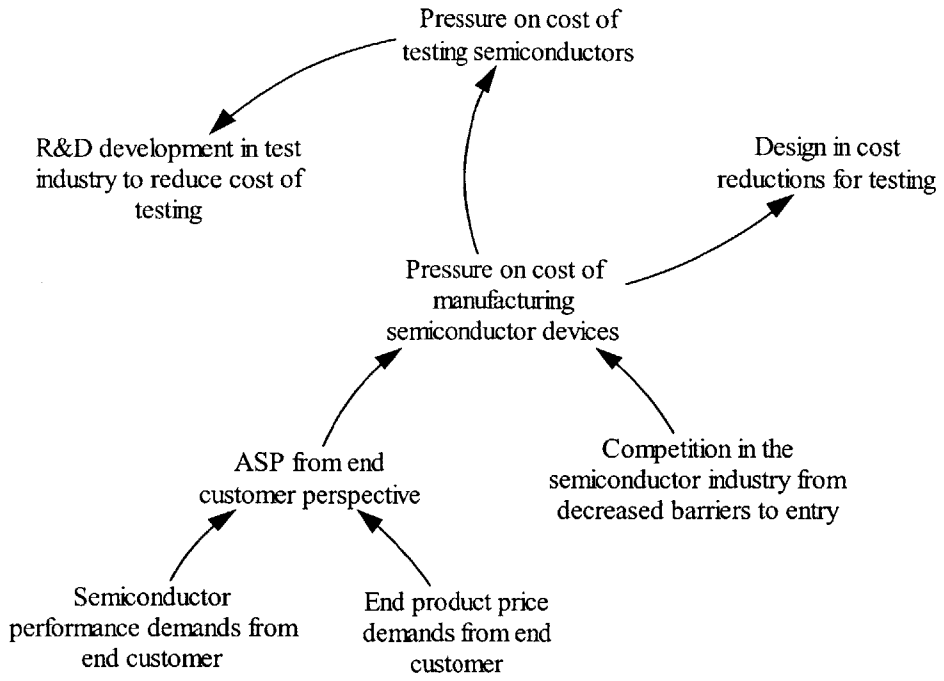


Figure 7.5.1 Interactions Affecting the Semiconductor Market Revenue

7.6 Translating the Interactions to Models

The following sections describe translating the market dynamics into tangible models to value the semiconductor market.

1. Assumptions

The dynamics affecting the semiconductor test market resulted in the four basic assumptions that drive the market mode.

1. Underlying model: The semiconductor test industry will compete to drive down the cost of testing. Realizing that the semiconductor industry feels pressure to reduce testing costs, the test industry will invest in R&D in order to keep the semiconductor test industry from focusing on designing out the test costs because of unresponsiveness from the semiconductor industry.

2. Throughput assumption: The capital cost pressure drove the industry to outsource. In addition, the test industry will focus its investments in R&D. As shown from the semiconductor manufacturing perspective, outsourcing drives the competition in the industry. The competition in the semiconductor industry feeds more outsourcing. The semiconductor manufacturing industry will consolidate in that only those companies with large economies of scale from volume will fabricate semiconductors. Those with lower volume will outsource. The test

industry will respond by increase the throughput of its test equipment. As shown in recent history, the introduction of a new test product results in step functions improvements in throughput and cost of test economics.

3. Test platform cost erosion assumption: The limitations of capital because of the pressure to reduce manufacturing costs will result in limits on the absolute value of capital equipment to test semiconductors. There is a limit to the absolute value manufacturers are willing to pay for capital equipment in addition to concerns about the cost of test for each device. While in the past, throughput increase offset capital cost increase, this will not happen in the future.

4. Volume assumption: The model used market projections for the number of devices that require testing. The test costs for each devices comes from current and historical averages and estimates. The model uses the volume assumptions with the cost of test per device assumptions to determine semiconductor test industry revenue.

2. Model description

With three major assumptions of volume, capital cost erosion, and continued investment in technical innovation to increase throughput, the model predicts cost of test improvements that erode the semiconductor test market. The base assumptions to the model as well as the model sensitivity and conclusion come in the subsequent sections.

7.7 Modeling of the Semiconductor Test Industry Markets

The foundation of the model uses system dynamics to explain the interactions of the market forces described at the beginning of Chapter 7. However, the model describes these market forces on the expected revenue of the semiconductor test market.

1. Volume Assumptions

The first assumption of the market dynamics model comes from device volume. As the volume of devices to test increases, it will drive the demand for testers, easing the pressures to reduce cost of test. Figure 7.7.1 shows the device volume assumptions that go into the model.

Dataquest predicts the unit volume of growth for the all device applications at round 6.2% CAGR (Compounded Annual Growth Rate) from 2001. Most of the volume occurs in the communications market with CAGR of 7.8%, closely followed by the consumer segment at 7.4%. The automotive segment grows moderately at 4.9% with the data processing segment growing at 5.6%. On the other hand, the data processing segment continues to lead the volume of devices followed by the communications segment, the consumer segment, and finally the automotive segment.

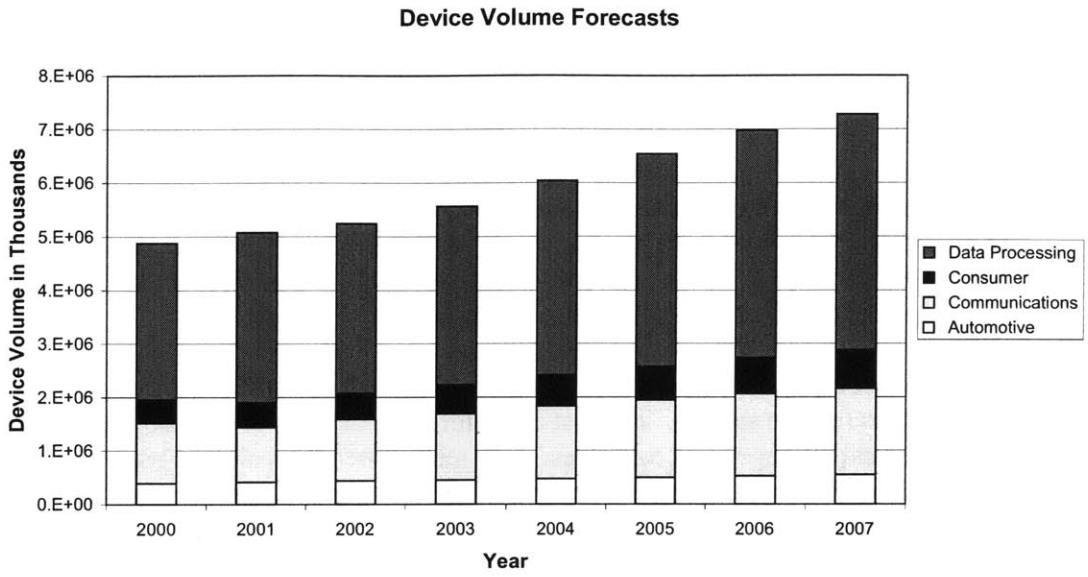


Figure 7.7.1 Device Volume Forecasts

2. Capital Price Assumption

The second assumption to the model deals with the erosion of capital costs after the introduction of the product platform. Looking historically, the capital price of ATE platforms erode with time. Figure 7.7.2 shows the average erosion rate for a capital platform with 100% as the price of the platform at introduction obtained from the historical erosion of four test platforms, and subsequent drop in capital prices in the product lifecycle. The model assumes an average erosion rate, with sensitivity on the aggressive as well as moderate rates.

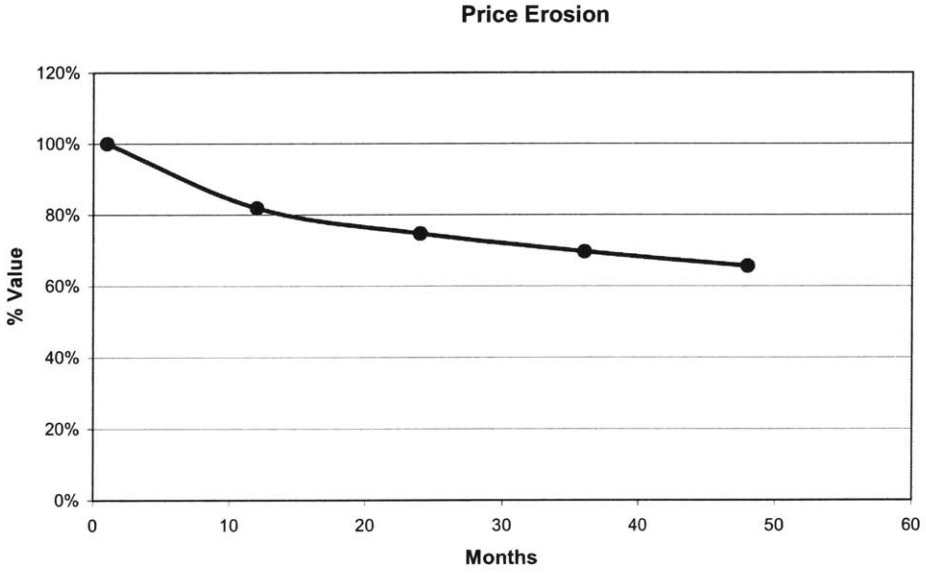


Figure 7.7.2 Average Capital Price Erosion Rate

The model assumes that the introduction of new ATE platforms initially results in a rise in pricing. Historically, the new platform results in an increase of 25% from the base price of the previous platform. However, as time progresses, the capital prices erode.

Figure 7.7.3 shows the model sensitivity to the capital cost assumptions in the consumer devices market segment. The points on the graph reflect the right y-axis showing the test platform cost erosion assumption. The solid lines on the graph correspond to the left y-axis showing the anticipated market revenue for ATE equipment. The stars on the graph represent high, and low test cost erosion assumptions. The high test cost erosion comes from the most aggressive erosion of the four platforms graphed, while the low test cost erosion comes from the slowest erosion of the four platforms graphed.

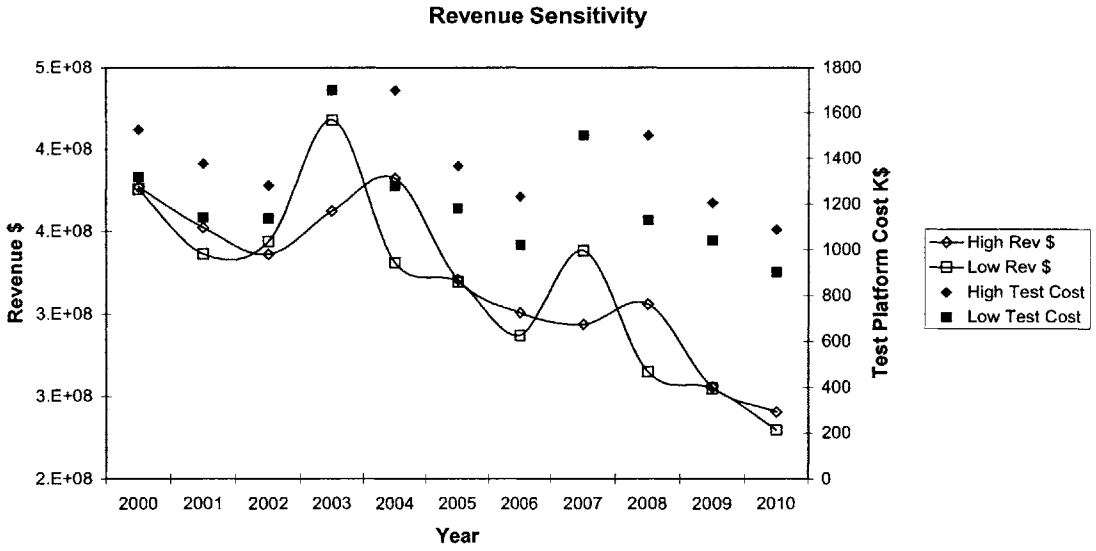


Figure 7.7.3 Capital Price Sensitivity

Looking at the sensitivity analysis, three major factors affect the revenue of the ATE market. The first comes from the rate of price erosion of the test platform. The second comes from the price rise with the introductory platform price, which the model assumed an historical increase of 25%. However, the sensitivity shows that large increases in prices at the initial introduction do not affect the results. The major factor comes from the erosion of test platform costs with time. The third, which the model does not vary, comes from the amount of time between new platform introductions.[3]

The high cost of capital points on the graph shows an example of aggressive capital cost erosion. Using this as the base assumption, the model shows large decreases in revenue. Furthermore, the model also predicts large drops in market revenue even with the

[3] Historical as well as industry plans point to new product introductions every 4-5 years. This model takes the conservative estimate of product development at every 5 years.

assumptions of mild capital cost erosion. All capital cost assumptions lead to the erosion of the test market revenue.

3. Throughput Increase

The most important issue in looking at the dynamic model comes from the throughput assumptions. Much of the previous market dynamics as described at the beginning of Chapter 7 discusses the cost pressure in the semiconductor test industry stemming from the customer as well as the industry perspective. Recently, in the semiconductor test industry, the cost of test reductions manifests themselves in controlling the capital costs while increase the throughput of the ATE platform. This results in decreasing the per device cost of test.

On one hand, increases in volume inherently increase the semiconductor test market. On the other hand, the capital cost erosion, and more importantly, the increase in throughput decreases the semiconductor test market.

The model breaks down two different categories for throughput sensitivity. The first comes from incremental improvements of throughput due to the increased speed of the ATE computer. For instance, Intel develops the newest microprocessor speeding up the computing capabilities of the ATE computer, and the tester. These improvements come from between 2% to 5% annually for Intel processors, and 5% to 7% improvement per 1.5 years for Unix processors typically from Sun Microsystems.[4]

The second category of throughput increases comes from step function improvements in speed from the introduction of the new test platform. The new products introduced in recent history show the 25% step function improvement in throughput over the industry standard.

In Figure 7.7.4, the distinct points reference the percentage of throughput improvement of platforms in the consumer device segment. The solid lines correspond to the revenue of the semiconductor test industry as a result of throughput improvements with the other major assumptions kept fixed. Figure 7.8.1 shows that without step function throughput improvements in the test industry, the semiconductor test revenue grows moderately. However, factoring in the expected step function improvements in throughput the market revenue declines substantially. Although these step function improvements in throughput only appear in recent history, and there is no long-term history to show this trend, the systems dynamics model predicts that these step function improvements will continue.

[4] Predictions of expected throughput increase from [7].

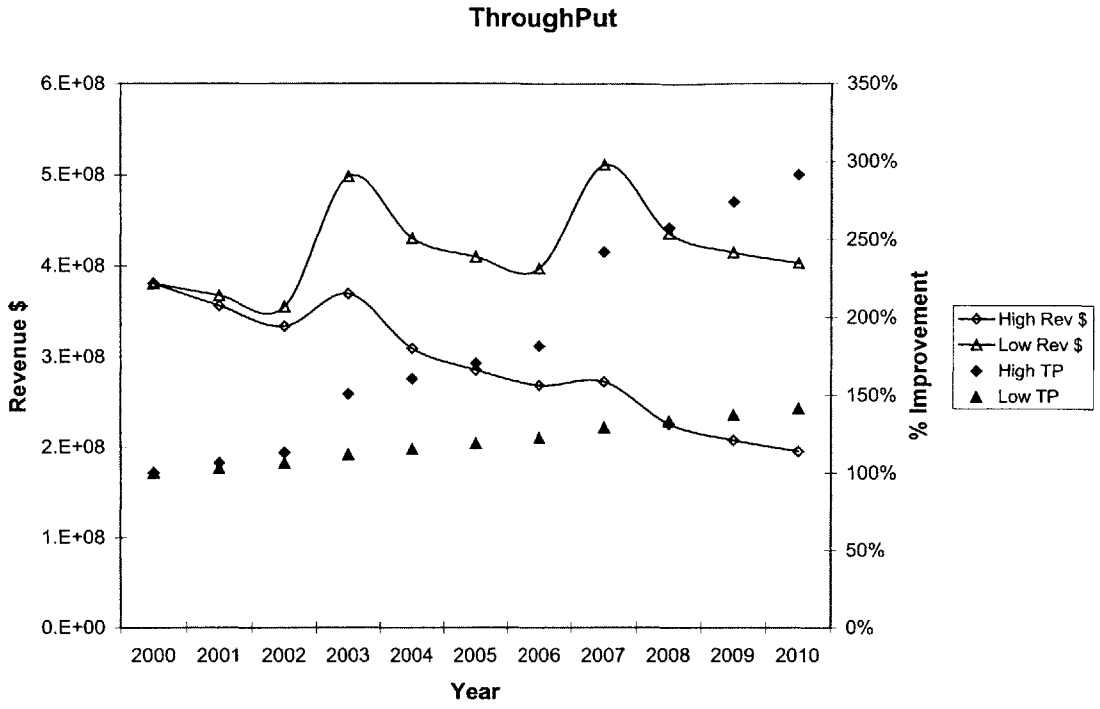


Figure 7.7.4 Throughput Assumption Sensitivity Analysis

7.8 Market Shrinkage as Model Results

The model predicts heavy cost of test erosions in the semiconductor test industry. The resulting erosions outpace the increases in volume, which drives down the revenue in the semiconductor test industry.

Data Processing

The market for each segment behaves differently. While the consumer and communications segments experiences similar results, the data processing segment differs slightly from the consumer segments in that the industry experiences no substantial or step function throughput increase from the historical context. Usually, this segment follows closely with Moore's Law because of the high complexity of devices. This drives the capital cost erosion of the industry with each new test platform development for two reasons. First, the complexity of the chips requires greater technical complexity in new test platforms. This results in a focus on performance rather than increasing throughput in new test platforms. Second, the increasing complexity of chips results in high semiconductor fabrication capital costs. Therefore, these manufacturers feel the greatest capital pressures. The manufacturers place great limits on test equipment capital spending rather then decreasing the cost of test per device.

However, the predicted capital cost erosion of ATE platforms in the semiconductor segments results in a similar market scenario as the model analysis above. Figure 7.8.1 shows the market model for the data processing segment. The points show the capital

cost erosion assumptions specific to the data processing segment, and the solid lines shows the corresponding model output exhibiting market erosion.

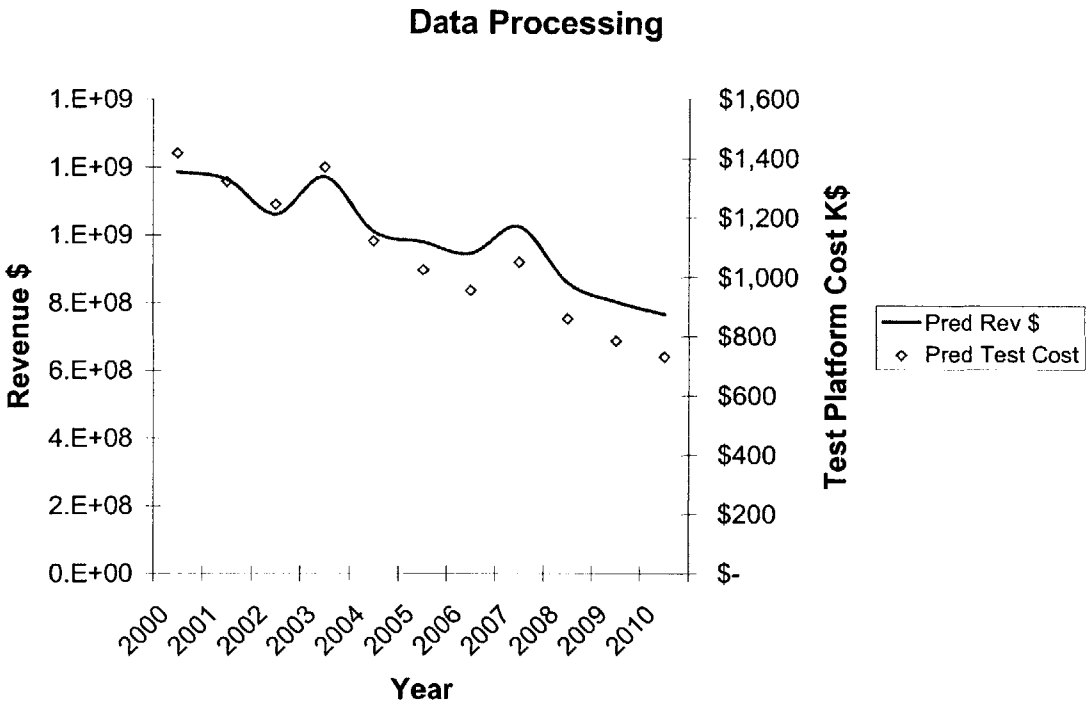


Figure 7.8.1 Data Processing Segment

7.9 Industry Maturity

Utterback (1996) proposed that the introduction of new products results in an exciting time for technical innovations. Because of the uncertainty in the market, the customers and companies explore for the best solutions. Characteristics such as reliability and consistency are less relevant because of the uncertainty in the customer expectations for a product. Utterback (1996) uses the example of the initial market exploration of the typewriter keyboard. The uncertain market requirements led to differences in the placement of the alphabet keys. Also, people were satisfied to get a typewriter, not worrying about the placement of the alphabet keys. Consistency of the placement of the keys seemed less important than the invention of the typing machine.

As the product matures, customers begin to understand their requirements. In this example, customers wanted more reliability and consistency in the typewriter. The novel idea of buying a typewriter was no longer enough to induce market demand. The industry responded with the emergence of a dominant architecture. Manufacturers begin to standardize around the QWERTY system.

At the end of the maturation process, the product development begins to focus on process rather than product innovation to drive efficiency in making the product. As the technology matures, the product becomes more of a commodity. The manufacturers

compete more on cost, rather then new product capabilities. In order to drive down cost, the manufacturer streamlines their product development and manufacturing process. Therefore, much of the innovation occurs not on the product itself, but the way they make the product. In many cases, the process innovation leads to modular architectures. Because of the process improvements involved in modularity as described by Utterback (1996), product maturity drives many industries towards modular architectures to cope with market maturity.

Figure 7.9.1 shows the how the product S-Curve relates to the technology S-Curve as described by Utterback (1996). In this figure, as time progress, the rate of growth in the industry declines. In fully mature markets, no growth exists. The new product introduction possesses the ability to improve the technology through product development and technological innovation. As the product matures, the level of technological growth begins to move towards process development rather than product development for product innovation.

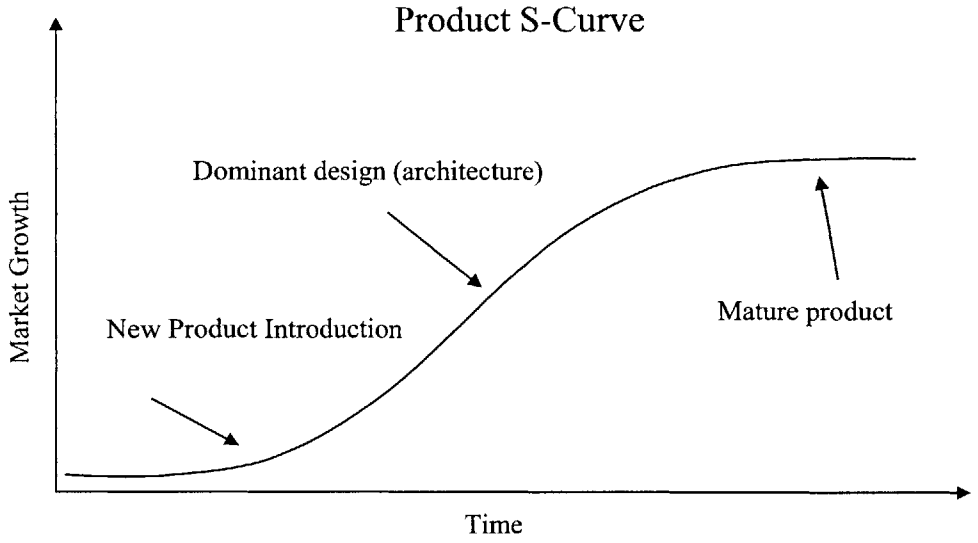


Figure 7.9.1 Industry S-Curve[5]

7.10 Application of Maturity to the Semiconductor Test Industry

It seems like a universal axiom of business theory that only in hindsight, can one fully and understand and predict industry change. However, the dynamics that led to the market shrinkage, as well as four other industry phenomena indicates that the semiconductor test industry is maturing.

1. Market Shrinkage

The first indication that the market is maturing comes from the low predicted growth rates in the semiconductor test industry. Although many reasons may exist for low growth rates in the market, the three phenomena, as described in the proceeding subsections, indicates that the market maturity is the cause of the low revenue growth. In

[5] Format of the picture provided by Professor Dan Whitney with ideas from [11], and [61].

most cases, the market maturity leads to a leveling off of growth in the market. However, in this case, the additional effect of market shrinkage is a result of pressures in the semiconductor test industry. It must be considered in addition to the market maturity.

2. Semiconductor Test Performance

Gartner reports that "if you look at the International Technology Roadmap for Semiconductors (ITRS) and compare the leading-edge companies' two year timelines for pilot line production with the ITRS timeline, by 2007, a technology gap begins to appear. In 2007, almost a three-year gap is evident between the ITRS and the leading-edge companies for when pilot line production is introduced to the market." [24] The lengthening of production timelines signals a lag in the incorporation of bleeding-edge technologies for semiconductors. Even though the complexity of bleeding-edge chips follows Moore's Law, the complexity for the majority of chips does not keep pace with Moore's law. In fact, the technology for a vast majority of semiconductor devices falls further and further behind bleeding edge devices.[5]

In the past, the pace of technological development in the semiconductor industry led the pace of development in the semiconductor test industry. The semiconductor testers needed to test the newest devices, driving product innovation. In fact, Moore's law prevented the semiconductor test industry from maturing. As a majority of devices lags behind Moore's Law, it reduces the pressures for product innovation. Furthermore, in the event that the industry no longer follows Moore's Law, it will speed the maturity of the markets and shorten the timeline for the decline of the market as predicted in the dynamics model.

3. Customer Expectations

The semiconductor industry is obsessed with the reduction of test costs. Initially, the pace of technology development kept the focus of test equipment on fulfilling the technical needs of testing. Today, Intel, AMD, and other major manufacturers proclaim the use of design for test (DFT) techniques to eliminate the difficult challenges in testing performance semiconductor chips. In fact, the use of built-in-self-test (BIST) by Intel resulted in huge market declines for the semiconductor test industry. In addition, most roadmaps from both the customers and test industry manufacturers show the proliferation of DFT. The rise of DFT resulted in slowing down the pace of product innovation in the semiconductor test industry as well.

In another example, ST Microelectronics stated that "partnering with Synopsys is a key part of the ST strategy to attack test challenges with a disciplined, unified approach, tightly linking design with manufacturing test. We see this as a long-term solution to reduce the risk of unacceptable growth in test costs." [54] It seems clear that the customer of the test industry know what they want.

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[5] Gartner defines bleeding edge devices are the newest devices developed with the newest technologies that follow Moore's Law. The leading edge devices are devices that incorporate older technologies than the bleeding edge devices, and the lagging edge devices are devices developed with older technologies.

4. Industry Response to the Expectations

As previously mentioned in Chapter 3, all the large players in the semiconductor test industry understand the importance of the vertical strategy. In addition, the customers see the value in a flexible architecture. The flexible architecture consists of one platform that the customer can reconfigure to test multiple market segments. In order to achieve flexibility, most of the large ATE manufacturers propose a modular architecture that allows customer to upgrade and downgrade the test platform. In effect, the modular, flexible architecture is the dominant architecture. Also, the move towards modularity mirrors that of many of other mature industries as described by Utterback (1996).

Another dynamic in the industry consists of the Open Architecture Initiative (OAI). Currently, all the large ATE manufacturers possess their own software platforms for their testers. In fact, Teradyne itself possesses two (one in UNIX, one in Visual Basic). OAI attempts to unify and standardize all the software platforms. This initiative also indicates the markets movement towards standardization and maturity.

5. Overview

Originally, the test platforms in the industry possessed no standard. The innovation of the product focused on keeping pace with the technological complexity of the semiconductor devices. The customers understand their needs for cost reductions in test, flexibility in platforms, and adequate performance. On the test industry side, the ATE manufacturers understand that they must drive down the cost of test, create flexible ATE platforms, and deliver adequate performance. As this understanding of market requirements crystallizes, the industry's move towards the vertical strategy begins to looks like the dominant architecture as explained by Utterback (1996).

7.11 Recommendations for the Long-Term

The result for the market model shows market erosion in the semiconductor test equipment industry. In addition, the semiconductor test industry must deal with market maturity. In the long term, Teradyne must implement a strategy to overcome both phenomena.

1. Market erosion

Since the year 2000, the semiconductor test industry has not slowed its pace of research and development even in the face of shrinking revenue and income. The semiconductor test industry should quicken the pace of product development and maintain strong investments in R&D in order to cope with shrinking markets. As the markets shrink, less revenue is available for all the competitors in the market. Two major scenarios can happen with less revenue in the market. Either every competitor gets less, or some competitors get squeezed out preserving revenues for the remaining players in the market. A combination between these two possibilities also exists.

1. Every Competitor Gets Less

   The semiconductor test industry has small and large players. As competition get more intense for revenue dollars because of the shrinking market, gross margins will erode. One can look at the Airline Industry in recent history to observe this event.

The players with the lowest cost structure and more efficient operations will benefit most from this model. In the case of the airline industry, all the large Airlines lost money. Only the small airlines (Southwest, Jet Blue) remained profitable.

2. Squeeze out Competition

When every competitor gets less, the large ATE manufacturers will suffer because of gross margin erosion. The smaller ATE companies can best cope with these shrinking margins. Therefore, in order to maintain revenue, and gross margins, the large ATE companies must squeeze out competition. The disk drive industry provides an example of consolidation in shrinking markets. As the markets shrank, the large disk drive makers aggressively developed new product offerings for their customers. The smaller companies were unable to keep pace with the heavy investments in R&D, and lost market share. Figure 7.11.1 shows a graph of the financials of the disk drive industry, the disk drive industry continued in its pace of R&D in response to shrinking markets. The three main manufacturers drove other companies out of business preserving its gross margins.

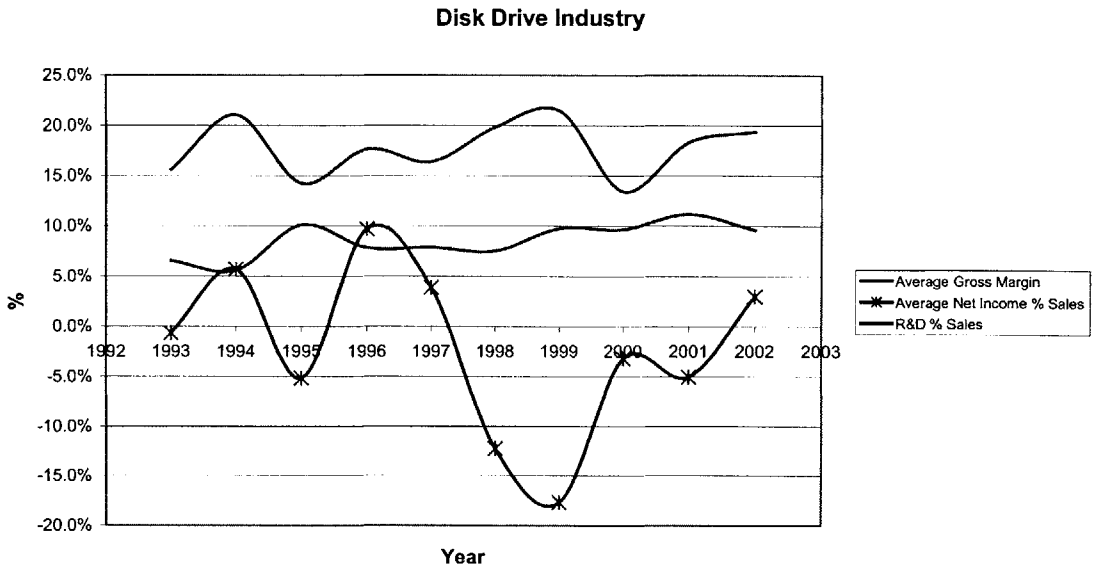

Figure 7.11.1 Financial averages from the Disk Drive Industry

In application for the semiconductor test industry, it must continue to invest in R&D, and speed the pace of product development in an effort to squeeze out the smaller niche competitors, others with less resources, and other with less product development capabilities.

2. Market Maturity

The industry will continue to mature and develop a flexible platform for testing multiple segments of semiconductors. In order to compete in maturing markets, the semiconductor test industry must make the adjustment towards process innovation as described by Utterback (1996).

In the past, much of the ATE products were driven by the performance requirements of the semiconductor devices. As the market matures, the platforms will be driven by continuous improvements on the flexible architecture, and innovations in the development and manufacturing process for semiconductor test equipment. The industry must trim costs and even more aggressively pursue the implementation of the principles of lean manufacturing and design.

3. Finding New Markets

In order to cope with both eroding and maturing markets, it is important to invest in new market opportunities.

1. Understand Core Capabilities and Markets

   The test industry must examine its core capabilities and markets, in order to apply competencies in new market, or develop other competencies for the core markets of semiconductor testing. For instance, on one hand, it could apply its product development capabilities to test MEMS devices. On the other hand, it could also offer test services in its core test markets. However, the first step is to understand it core capabilities and its core markets.

2. Create New Capabilities

   It is often difficult to find other markets to apply core competencies. In most cases, companies tend to create capabilities within an organization to cope with changing markets. In this way, the company can utilize its understanding of the industry in order to gain more opportunities. In this case, the semiconductor test industry must develop other capabilities along the value chain for the semiconductor industry. Christensen (2000) suggests that companies can create capabilities through acquisition, internal development, and spinning off organizations. It is beyond to scope of this thesis to examine this strategy beyond this point.

7.12 Chapter Summary

The model presented in this chapter predicts market erosion in the semiconductor test industry. In addition, the observed trends in the industry are consistent with the maturing of the semiconductor test market. In order to deal with these long-term effects, large manufacturers of test equipment should continue it quicken the pace of development. In order to deal with the effects of industry maturity, it should focus on process innovation, and participate in niche and emerging markets. Ultimately, in order to overcome both effects, large ATE manufacturers need to find new markets, and develop new capabilities in order to expand its revenue.

Chapter 8: Conclusion

8.1 Thesis Results

The economic conditions following the peak demand year of 2000 led to large declines in revenue for the semiconductor test industry. While many predicted a drop in revenue, the length and the extent of the declines led to worry in the semiconductor test industry. In the subsequent years after the peak in demand, the customers of the semiconductor test industry began to experience stricter limits on capital cost spending, greater propensity to outsource, and better test economics. The semiconductor test industry segmented itself into two broad strategies in order deal with these changes. Typically, the large semiconductor test equipment manufacturers employed a vertical strategy, while the smaller semiconductor test equipment manufacturers employed a horizontal strategy.

8.2 Confirmation of General Trends

This thesis confirmed the underlying fundamental trends in the semiconductor test industry by examining the changes in the semiconductor value chain and its effect on the semiconductor test industry. The thesis identified three main factors that drive the continued disintegration of the value chain. First, the increasing complexity of chips drives specialization in the industry as it attempts to follow Moore's Law. Second, the cost of semiconductor capital equipment and the economies of scale around CMOS technologies result in specialized wafer foundries. Third, companies outsource semiconductor assembly and testing because of the specialization in the East Asian region. Also, IC design specialty, as well as the rise of per-unit cost manufacturing drives the development of fabless companies.

The trends in the semiconductor value chain affect the semiconductor test industry in three ways. First, the disintegration of the value chain results in outsourcing. This shifts the customer structure of the semiconductor test industry. Second, the complexity of the semiconductor devices drives the complexity of the semiconductor test technology. Also, the constraints in capital costs leads to limitations on the absolute capital customers are willing to pay for the tester. However, the customer still demands low cost of test as measured per device.

8.3 Evaluation of Horizontal and Vertical Strategies

This thesis analyzed the rewards and risks of the horizontal and vertical market strategies. In theory, a purely horizontal strategy provides an independent platform solution targeting a specific segment of the market. The purely vertical market strategy provides one flexible platform with the test capabilities to test all semiconductor devices.

In evaluating the rewards, this thesis presented a model to value the price premium for the flexible strategy. It assumes that since manufacturing planning changes only in the case of sustained volume change or new product introduction, the main advantage of the vertical strategy comes from the decrease in switching cost from reconfiguring the tester as opposed to buying a new test platform. Chapter 5 introduced the flexibility valuation equation as the *Value of Flexibility = Switching Costs (Vertical to Horizontal) – Switching Costs (Vertical to Vertical).*

This thesis also described the intangible risks posed by the vertical strategy as compared with the horizontal strategy. It explain the issues posed by the "attacker's advantage" as proposed by Foster (1986) in which companies abandon the low-end market segments allowing competitors to survive, grow, and increase in market share. The move towards a vertical strategy will make large test equipment manufacturers even more susceptible to the "attacker's advantage". It also provided recommendations to diminish the risks from attackers, while maximizing profits by employing the vertical strategy.

8.4 Future Market Strategies

In Chapter 7, the thesis proposed a model for market erosion in the semiconductor test industry. In addition, the thesis concludes that the observed trends in the industry are consistent with the maturing of the semiconductor test market. It provides recommendations to deal with the shrinking and maturing semiconductor test market.

8.5 Opportunities for Further Analysis

This thesis addressed the problems in the semiconductor test industry from a customer perspective. One of the areas of further study is to evaluate the semiconductor industry from the product development perspective. This thesis made no attempt to quantify the product development costs associated with developing a single flexible platform in the vertical strategy. Furthermore, it is valuable to determine the cost comparisons between a flexible and focused product solution.

Secondly, much of the thesis examined the market conditions assuming the increased complexity of semiconductor devices. A great deal of controversy exists over the continuation of Moore's Law. Further study needs to be done in the case that Moore's Law does not continue.

Third, this thesis did not quantify the risks associated with the vertical strategies. It stated them intangibly warning of the dangers of the "attacker's advantage". In order to develop a true risk/benefit analysis, one must determine the probability of the risk and quantify the value in terms of lost revenue. Another area of study is to develop a complete cost/benefit analysis.

Also, it was beyond the scope of the thesis to develop alternative business models in the face of shrinking and maturing markets. Although the thesis recommends evaluating alternative business models, it does not build on any of these models.

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