Discrete Superconducting Vortex Flow Transistors

by

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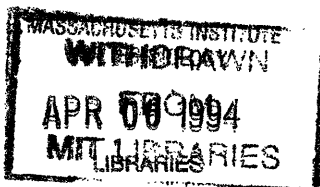
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Abstract

In this thesis, two versions of a Discrete Superconducting Vortex Flow Transistor (DVFT) are studied. Both overdamped and underdamped versions are fabricated with low T_c Niobium Josephson junctions. We present analytical models for the operation of the DVFTs that agree with the experimental data. In addition to the operational model of the DVFT, we also present an example of a circuit implementation of the DVFT.

Measurements on the overdamped version of the DVFT indicate a current gain of 1.2 when the gate current is injected parallel to the array of junctions. With this manner of gate current injection, the gain is linear in the number of junctions and can be made much greater than 1. Measurements on the underdamped version of the DVFT indicate a transresistance of 2.8Ω with parallel gate current injection.

The overdamped DVFT is better suited for circuit implementation than the underdamped version because its operation is nonlatching and is therefore less sensitive to noise.

The conclusion of this thesis is that the DVFT is a viable superconducting transistor. The DVFT can be used as a building block to construct complex logic circuitry or as an interface between current based electronics, such as RSFQ logic and voltage based circuits, such as CMOS memory devices.

Thesis Supervisor: Terry P. Orlando
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I would also like to thank my family and my friends for their support.

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Chapter 1

Introduction

1.1 Superconductivity

The field of semiconductor microelectronics has seen great achievements since its conception, but it is generally agreed that it is reaching some fundamental limits in terms of the response time of the transistors and the power consumption caused by the demand for increasing component density. Superconductors offer a potential solution to these problems. The basic element in superconductor microelectronics, the Josephson junction, has an intrinsic switching response time on the order of a picosecond [1].

There are still some unsolved problems in superconductor-based microelectronics. Up to now, this technology does not have a feasible three-terminal component, or a switch, which is a necessity for the simplicity of logic circuits. In the absence of such a switch, even simple logic operations have required complex engineering solutions [2, 3].

There are two main material technologies in superconductor electronics. The major distinction among them is the transition temperature (T_c) of the materials. T_c is the temperature below which the material becomes superconducting. The T_c of any material is much lower than room temperature, thus refrigeration is needed in order to observe superconducting phenomena. Normally, either liquid helium or liquid nitrogen are used to achieve the necessary temperatures. Helium liquifies at 4.2

K and nitrogen liquifies at 77 K, thus low T_c materials have transition temperatures in the range of 4 K and are measured with liquid helium, and high T_c materials can be measured with liquid nitrogen. Currently, the most commonly used low T_c material is niobium, which has a transition temperature of 9.3 K. Niobium technology is well characterized and controlled. Nevertheless, one would eventually like to operate at the temperature of liquid nitrogen, which is much cheaper than liquid helium. Currently, there is much research in developing a technology that would operate at the higher temperatures. The main material being considered is $YBa_2Cu_3O_{7-x}$, which has a T_c of 92 K. High T_c technology is in the developmental stage and is much less controlled than low T_c fabrication technology.

The basic building block of most low T_c superconducting electronics is the Josephson junction. The counterpart of the Josephson junction in high T_c electronics is the weak link. A Josephson junction or a weak link can be modeled as an ideal element, exhibiting the DC (equation 1.1) and AC (equation 1.2) Josephson effects, shunted by a parallel combination of a resistor and a capacitor.

$$i = i_o \sin \theta \tag{1.1}$$

$$v = \frac{\Phi_o}{2\pi} \frac{d\theta}{dt} \tag{1.2}$$

A figure of merit describing this parallel combination is the damping parameter, β_c, which is equal to the Q of the equivalent parallel circuit.

1.2 Vortex Flow Transistors

There have been some previous attempts at constructing a superconducting three-terminal transistor. The most promising results have been demonstrated by using the magnetic flux of a current to control the characteristics of a Josephson system [4, 5, 6, 7]. These systems are commonly referred to as Vortex Flow Transistors (VFTs). VFTs have been made both in low T_c and high T_c material technologies.

1.2.1 Low T_c

Up to now, the low T_c VFTs have been made using long continuous Josephson junctions. There are two versions of low T_c VFTs; one is a device with overdamped junctions (the McCumber parameter $\beta_c < 1$) and the other is made with underdamped junctions ($\beta_c > 1$).

The most prominent characteristic of overdamped VFTs is a nonhysteretic I-V relationship which can be modulated by an external magnetic flux imposed on the Josephson junction by a gate current. Overdamped VFTs based on long Josephson junctions, which are made in low T_c materials, have demonstrated [7] current gains of 10 and transresistances of 0.2 Ω. The disadvantage of the long-junction-based overdamped VFTs is the large size, necessary for high gains (750 μm in length), low output voltage (< 1 mV), and low output resistance ($<< 1\ \Omega$). Moreover, it is difficult to manipulate the parameters and improve the response time of the device.

In contrast with the overdamped VFTs, underdamped VFTs, which are made only in low T_c technology, demonstrate a hysteretic I-V curve with a magnetic field induced voltage peak in the subgap region. This feature is referred to as the Eck peak [8]. The operation of the underdamped VFTs is based on the modulation of the voltage position of the Eck peak with the magnetic field of a gate current. Underdamped VFTs with long Josephson junctions have demonstrated [9] output voltages of 0.17 mV, output resistances of 1 Ω and transresistances of about 2 mV. The disadvantages of these devices are similar to their overdamped counterparts: large size (800 μm in length), low output voltage, and difficulty in manipulating the parameters of the device.

1.2.2 High T_c

The VFTs fabricated using high T_c material technology are similar to the low T_c overdamped VFTs in that they both have nonhysteretic I-V traces and use gate currents to modulate these I-Vs. The high T_c VFTs utilize parallel arrays of weak links, rather than Josephson junctions. These VFTs have shown some promising

results [10]. Maximum output voltages of 20 mV and transresistances of the order of 10 Ω were obtained. The discrete lattice of weak links permits the high T_c VFTs to have more efficient magnetic flux coupling, so the device can be made small in size (80 μm). The disadvantage of the high T_c devices is that the fabrication technology is not yet fully developed and that the factors determining the performance of these devices are not completely understood.

1.2.3 Discrete VFTs

The high T_c weak link transistors have good current gain and output voltage range, but there is no analytical model that governs the operation of these devices. Therefore, the improvement of the performance of the high T_c devices becomes very hard. The low T_c technology is very well controlled, and the dynamics of vortex motion is better understood [11]. Therefore, it is possible to construct a model to explain the operation of a vortex flow transistor in low T_c technology. We can also build a device that is made with low T_c technology, with the magnetic coupling advantage of the high T_c devices. With an understanding of the low T_c devices we hope to improve our understanding of the operation of the technologically important high T_c devices. The analog of the high T_c weak link devices in the low T_c technology is a device based on a parallel array of Josephson junctions. We refer to such devices as Discrete Vortex Flow Transistors (DVFTs).

DVFTs are three terminal devices: a gate current regulates the number of vortices in the device; and a bias current causes the vortices to move which leads to a voltage proportional to the number of the vortices. A DVFT consists of a parallel array of Josephson junctions which are coupled to each other by superconducting wires. Each junction is separated from its neighbor by the lattice constant p of the cell. An important parameter in discrete 1D arrays is the penetration depth Λ_J, in units of p, which is a measure of the discreteness of the system. For $\Lambda_J < 1$, vortices are well localized objects; whereas, for $\Lambda_J >> 1$ vortices are spread out over several cells. The

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penetration depth Λ_J is defined as

$$\Lambda_J = \sqrt{\frac{L_J}{L_s}}.$$ (1.3)

Here, L_s is the self-inductance of a cell in the array and L_J is the Josephson inductance, $L_J = \Phi_o/(2\pi I_c)$, where Φ_o is the flux quantum and I_c is the critical current of a single junction. From measurements of Fiske modes in underdamped arrays, we have determined that in our DVFT geometry, $L_s = 1.1\ \mu_0 p$ [12].

In this thesis, we describe the operation of two versions of Discrete Vortex Flow Transistors. The overdamped DVFT has externally shunted junctions, such that $\beta_c \approx 1$. There is also an underdamped version of the DVFT with $\beta_c = 120$. The analysis of both versions shows that the underdamped DVFT is more susceptible to fluctuations of the critical current, so the overdamped DVFT is better suited for circuit implementation. We also describe in detail an inverter implementation of the DVFT and show the implications of various parameters introduced in the chapter on the overdamped DVFT. We also show an oscillator based on the DVFT inverter. This oscillator can be used not only to generate clock signals, but to measure delay times through transmission lines and the inductance per unit length of superconducting lines.

Chapter 2

Overdamped Vortex Flow Transistors

2.1 Introduction

In this chapter we discuss discrete overdamped vortex flow transistors (DVFTs) made of short niobium Josephson tunnel junctions connected in parallel. The results of our DVFT are compared with the high T_c devices and the long continuous Josephson junctions. We also present model calculations on our DVFT which are in good agreement with our experimental results. We calculate the current gain, transresistance, the output voltage and output resistance and discuss how one can improve the operation of an overdamped DVFT and what its limitations are. Our model is also applicable to other 1D discrete systems and can also be used to model long Josephson junctions. Our analysis shows that when disregarding the lower temperatures and voltage levels in low T_c materials, DVFTs made of niobium tunnel junctions can perform at the level comparable to the present high T_c flux flow devices.

2.2 Experimental results

Our DVFTs are fabricated with the dual dielectric selective niobium anodization process (DSNAP) technology developed at Lincoln Laboratory. A layout of the device

is shown in Fig. 2-1. A schematic drawing of the device is given in Fig. 2-2. The DVFT consists of an array of $N = 9$ underdamped Josephson junctions, each shunted with an external resistor R_s. The transport current i_t is injected through a resistor of about $1\,\Omega$ connected to each node so that the current is uniformly injected along our 1D array. The gate current i_g can be applied in two ways; in a loop near the edge of the array or through a line parallel to the array. In this section on the experimental results we will show results with the parallel gate current injection except for the measurement of the gain, where we show the results for both modes of injection.

Each Nb-Al$_2$O$_x$-Nb junction has a lithographically defined area of $3 \times 3\,\mu\mathrm{m}^2$. At $4.2\,\mathrm{K}$ the total array critical current in zero magnetic field, i_{co}, is $0.37\,\mathrm{mA}$ so that I_c is $0.04\,\mathrm{mA}$. Thus, the critical current density, J_c, is estimated to be $450\,\mathrm{A/cm^2}$. Because the $I_c R_n = 1.75\,\mathrm{mV}$ for these junctions at $4.2\,\mathrm{K}$, the junction normal-state resistance, R_n can be estimated as $43\,\Omega$. The shunt resistance R_s is $5.0\,\Omega$, and the capacitance C is $405\,\mathrm{fF}$. The characteristic parameters of our 1D array are the lattice spacing $p = 10\,\mu\mathrm{m}$ and $L_s = 14\,\mathrm{pH}$. The McCumber parameter is $\beta_c = 2\pi R_{eq}^2 C I_c/(\Phi_o)$ where R_{eq} is the parallel combination the junction resistance R_j and R_s [1]. The externally shunted junctions are critically damped with $\beta_c \approx 1$.

We have measured the array voltage v_a as a function of i_t at $4.2\,\mathrm{K}$ for several values of i_g as illustrated in Fig. 2-3. The array critical current, i_c, is the point of the highest zero voltage current in the i_t-v_a characteristic. By increasing i_g, i_c is suppressed. This is the key point for the operation of the DVFT. In the absence of an applied magnetic field the highest i_c occurs for $i_g = 0$ and is denoted in this paper as i_{co}. For uniform current injection $i_{co} = NI_c$. (Note capital letters denote junction parameters and small letters denote parameters of the full discrete 1D arrays.)

Suppose the array is biased just below i_{co}, as shown in Fig. 2-3 by the dotted line at $i_t = 0.36$ mA. For a zero gate current, the voltage is 0, but when i_g is increased, the operating point moves along the horizontal dotted line (for a non-loaded device), shown in Figure 2-3. As a result, the array voltage, v_a, increases. If a load is present

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[1] R_j should be taken as the subgap resistance for junctions operating below the gap voltage and R_n for higher voltages. However, for our samples the shunt resistance is much less than R_n, so that the shunt resistance is the equivalent resistance.
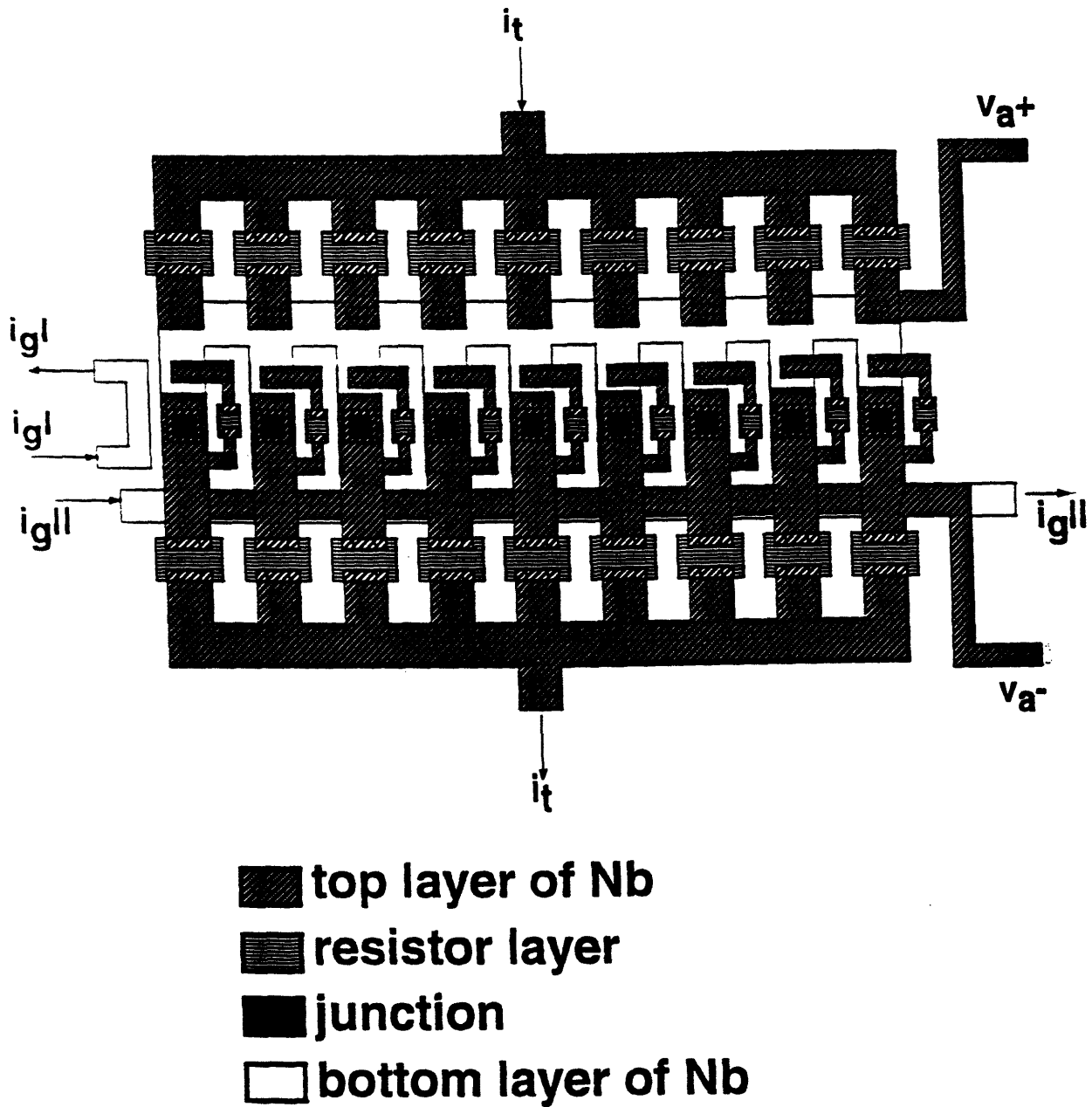
Figure 2-1: A layout of the overdamped DVFT showing two possible ways of injecting the gate current.
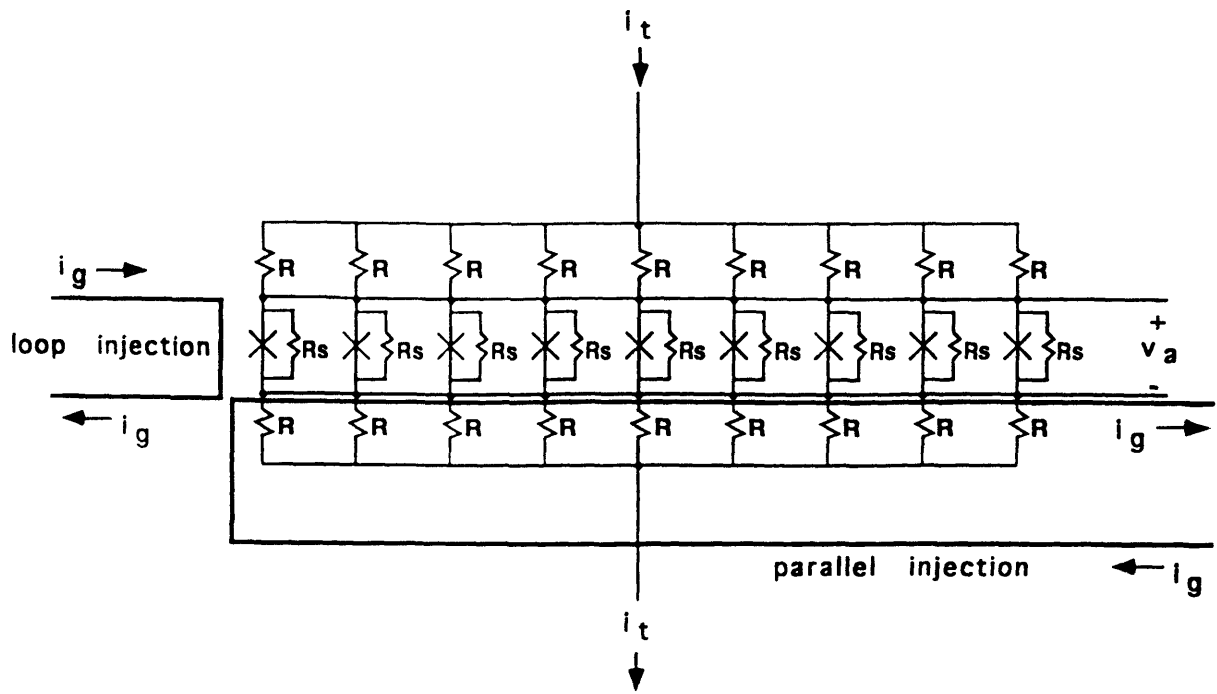
Figure 2-2: A schematic drawing of the overdamped DVFT with junctions externally shunted with a resistance R_s and resistors R connecting to each node to uniformly inject the transport current into the array.
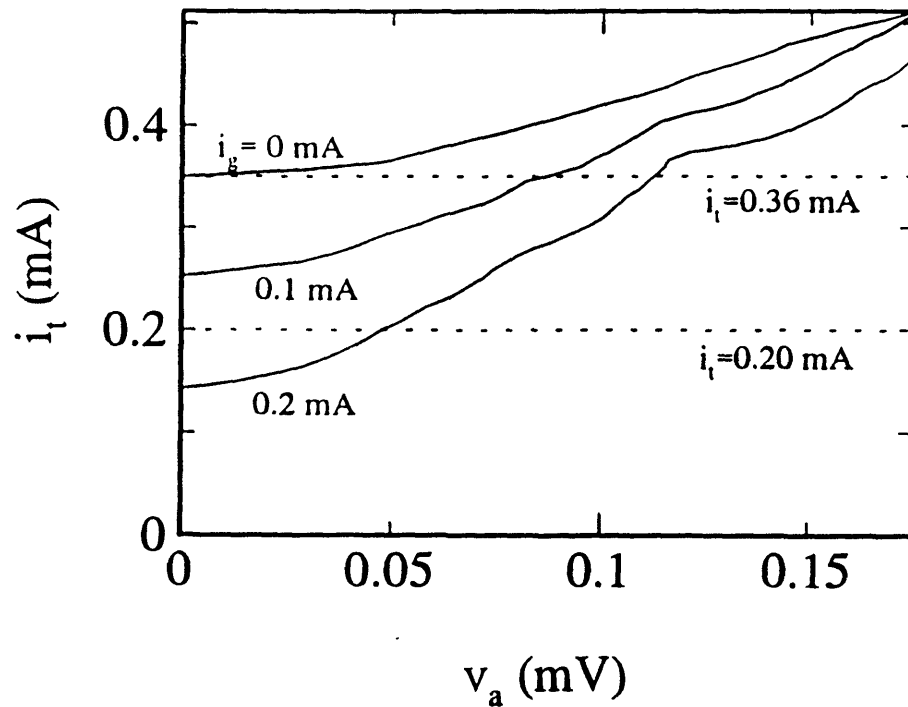
Figure 2-3: The array voltage as a function of the array transport current for three different gate currents. The gate current is injected parallel to the array.
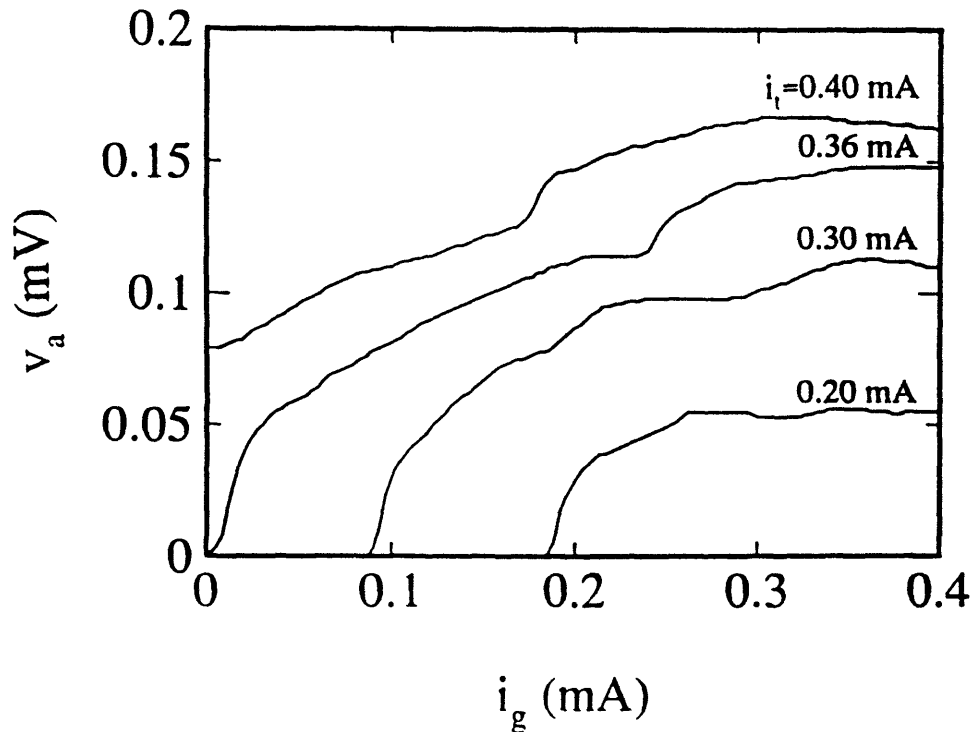
Figure 2-4: The input (gate current) - output (array voltage) characteristic of the DVFT for four different transport currents through the array. The gate current is injected parallel to the array.

at the output of the DVFT, the operating point will move along a load line, the slope of which is equal to $-1/R_L$, where R_L is the load resistance.

Fig. 2-4 shows the input-output relation of the DVFT. It shows the array voltage, v_a, as a function of i_g for several bias values of i_t when the array is not loaded. For practical applications, the range of the output voltage needs to be as high as possible. Bias currents much lower than i_{co} result in a degradation of the output voltage. To keep the voltage levels high, it is desirable to bias i_t near i_{co}. There is also an upper limit to the bias of i_t, beyond which, v_a will not go down to 0 volts. Thus, for usual operating conditions, the maximum array output voltage in Fig. 2-4 is about 0.15 mV.

The coupling between i_g and v_a is described by the transresistance r_m, defined as $\Delta v_a / \Delta i_g$, which can be obtained from Fig. 2-4. Since these curves resemble more a square root behavior than a straight line, the differential, r_m, ranges from 2 Ω for $0 < i_g < 0.025$ mA, to 0.33 Ω for $0.025\,\text{mA} < i_g < 0.25$ mA. As an estimate of r_m, we use the difference between the endpoint values at $v_a = 0$ ($i_g = 0$) and $v_a = v_{amax}$

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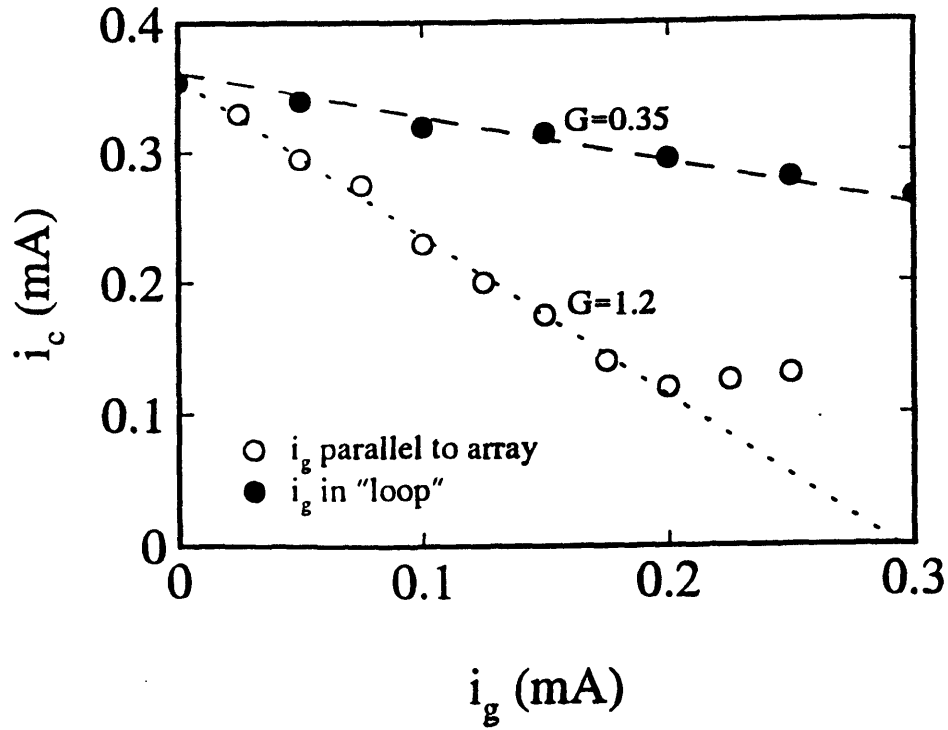
Figure 2-5: The suppression of the array critical current by the gate current for loop injection and parallel injection. The dashed lines define the current gain of the DVFT.

(i_g = 0.35 mA), i.e. r_m = 0.15/0.35 = 0.43 Ω. It is desirable to have r_m as high as possible, since this factor is proportional to the gain of the device (see next section).

Another measure characterizing the performance of the DVFT is $G = \Delta i_c / \Delta i_g$, the amount of suppression of i_c by i_g, which is a measure of the current gain of the device. Fig. 2-5 shows i_c as a function of i_g for the two cases of gate current flowing parallel to the DVFT and flowing through a loop near the DVFT edge. For small i_g, the relationship approaches a straight line, the slope of which is equal to G. For the sample of Fig. 2-5, $G = 1.2$ for parallel gate currents and $G = 0.35$ for gate currents through the loop. Estimates of G, its dependence on N, and the method of flux coupling will be modeled in the next section. We will show that r_m depends on G, which in turn depends on the gate current injection.

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2.3 DVFT Analysis

2.3.1 RSJ model

We have found that the i_t-v_a relationship of our arrays can be approximated by an equivalent RSJ model

$$v_a = r_{eq}i_c(i_g)\sqrt{\left(\frac{i_t}{i_c(i_g)}\right)^2 - 1}. \tag{2.1}$$

where $r_{eq} = (R_s \| R_j)/N$ is the equivalent resistance. For our samples, $r_{eq} \approx R_s/N$. The array critical current i_c in Eq. 2.1 depends on the induced magnetic field and does not follow the single-junction magnetic field dependence of the critical current. In general, i_c depends on the number of junctions, the penetration depth and the way i_g is injected. Eq. 2.1 works well for high temperatures where $\beta_c << 1$, but at 4.2 K where $\beta_c \approx 1$, deviations are found. (β_c is temperature dependent through I_c.) We have shown that in underdamped 1D arrays there exist resonances which are associated with standing modes of small amplitude phase oscillations [12]. In Fig. 2-3, the effects of resonances are superimposed on the RSJ-like behavior.

A possible explanation for the RSJ-like behavior is given in Ref. [11]. In that paper, the equation of motion for a single, independent vortex in a 1D array is calculated. This equation of motion along the 1D array is equivalent to the equation of motion for the phase difference across a single RSJ junction, indicating that the vortex dynamics in 1D arrays is equivalent to single junction dynamics and hence qualitatively similar current-voltage characteristics are expected. However, this assumes that vortex flow is the only dynamics in the array. When other dynamics occur, such as Fiske modes, then the simple model presented here must be modified. For $\beta_c < 1$ we expect this simple model to be valid. In further analysis we will use the RSJ-like dependence of Eq. 2.1 and calculate the characteristic properties of DVFTs using typical numbers for niobium technology at 4.2 K. We will assume the I_cR_n(4.2 K)-product of 1.75 mV and the specific capacitance C' of 45 fF/ μm^2 to be independent of J_c.

Eq. 2.1 shows that to have the output voltage levels as high as possible, $r_{eq}i_c$ must be at the highest level possible. For i_t biased close to i_{co} and for $i_c(i_g)$ suppressed by

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the gate current well below i_{co}, then Eq. 2.1 shows that the maximum voltage can be written as

$$v_{amax} \approx r_{eq} i_{co} = \left(\frac{R_{eq}}{R_n} \right) * 1.75\,\text{mV} . \tag{2.2}$$

For our sample we expect v_{amax} to be $0.2\,\text{mV}$, which is close to the measured value of $0.15\,\text{mV}$. To increase v_{amax} one would like to have $R_{eq} = R_n$, indicating intrinsically overdamped junctions. In this respect it is helpful to write the McCumber parameter in terms of the critical current density. For unshunted niobium junctions at 4.2 K, we find

$$\beta_c \approx \frac{C'}{J_c} \tag{2.3}$$

when C' is expressed in $\text{fF}/\mu\text{m}^2$ and J_c in kA/cm^2. For the junctions to be intrinsically overdamped J_c must be at least $45 \frac{\text{kA}}{\text{cm}^2}$. Such high-$J_c$ junctions are also needed for SFQ circuits [3] and have been fabricated [13]. Probably, J_c must even be higher, because the specific capacitance is expected to be larger for these high-J_c junctions.

The expression for the output resistance in the RSJ model can be derived by taking a derivative of Eq. 2.1

$$r_o = \frac{\partial v_a}{\partial i_t} = \frac{r_{eq} i_t}{\sqrt{i_t^2 - i_c^2}} . \tag{2.4}$$

For transport currents much higher than i_c, r_o can be approximated by:

$$r_o \approx r_{eq} \tag{2.5}$$

which is $R_s/N = 0.55\ \Omega$ for our shunted DVFT. From the DC standpoint, it is desirable to have the output resistance as small as possible, but since this device would probably be required to drive transmission lines, r_o must be matched in order to reduce reflections. Resistances of the order of a few ohms are desirable for many superconducting circuits.

The transresistance, r_m, is defined as

$$r_m = \frac{\partial v_a}{\partial i_g} = \frac{\partial v_a}{\partial i_c}\frac{\partial i_c}{\partial i_g}. \tag{2.6}$$

The term $\left(-\frac{\partial i_c}{\partial i_g}\right)$ will be denoted by G, the current gain. For bias currents close to i_{co}, Eq. 2.6 can be written as

$$r_m = \frac{r_{eq}Gi_c}{\sqrt{i_t^2 - i_c^2}} \approx \frac{r_{eq}Gi_c}{\sqrt{i_{co}^2 - i_c^2}}. \tag{2.7}$$

indicating that r_m depends on the gate current through i_c and on the manner of its injection through G. As an estimate of r_m, we do not take the differential, but instead the large signal resistance between the endpoints at $v_a = 0$ and $v_a = v_{amax}$. If $\Lambda_J < 1$, then i_c is some fraction of i_{co} (see calculations next section) so that

$$r_m \approx \alpha r_{eq}G \approx \alpha r_o G \tag{2.8}$$

and α is a parameter depending on i_g and $\alpha < 1$. For our sample, the measured gain is 1.2, and this estimate gives with $\alpha = 0.5$ that $r_m \approx 0.6r_{eq} = 0.33\,\Omega$, in agreement with our experimental value of $0.43\,\Omega$. In order to make r_m as high as possible, G and r_{eq} must be as high as possible.

As an estimate of the response time of our arrays, we can multiply the single junction response time [14] by the number of junctions, N, and the cell-to-cell propagation time by the number of cells, $N - 1$, which gives

$$\tau_R \approx N2R_{eq}C + (N - 1)\sqrt{L_s C}. \tag{2.9}$$

For our DVFT, we can estimate that $\tau_R = 56\,\text{ps}$. It is convenient to write the expression for the response time in terms of J_c for $\beta_c \approx 1$ and $\Lambda_J \approx 1$,

$$\tau_R = R_{eq}C\,(3N - 1) = \frac{8\,\text{ps}}{J_c}\frac{R_{eq}}{R_n}\,(3N - 1) \tag{2.10}$$

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with J_c in units of kA/cm². If $J_c = 45\frac{\text{kA}}{\text{cm}^2}$ so that the junctions are intrinsically overdamped with $R_{eq} = R_n$, then τ_R is expected to be about 5 ps for an array with 9 junctions.

2.3.2 Current gain

The current gain G is defined as

$$G = -\frac{\Delta i_c}{\Delta i_g} = \left(-\frac{\left(\frac{\Delta i_c}{NI_c}\right)}{\Delta i_g}\right) NI_c = \left(\frac{\left(-\frac{\Delta i_c}{i_{co}}\right)}{\Delta i_g}\right) \frac{N\Phi_o}{L_J 2\pi} \qquad (2.11)$$

To get more insight in the factors determining G, we will write the suppression of the array critical current by i_g as a suppression by a perpendicular magnetic field and then we can calculate the critical current suppression numerically as a function of Λ_J and N.

Thus, the first step is to write i_g in terms of a magnetic field. If i_g is supplied through a filamentary wire as in the discrete device shown in Fig. 2-1, then the magnetic field is $B = \mu_0 i_g/2\pi r$, where r is the distance from the center of the wire. We integrate the magnetic field over the area of the array to get the total applied magnetic flux linkage and then divide by $N - 1$ to get the average flux Φ_{app} in a unit cell of the array. Therefore, $\Phi_{app} = i_g M/2\pi(N-1)$, where M is the mutual inductive coupling which depends on the size of the array and the manner of injection of gate current with respect to the Josephson junction array. As shown in Fig. 2-1, the gate current, i_g, can be injected parallel to the length of the array, or into a "loop" located at one side of the array.

It is convenient to define

$$f = \frac{\Phi_{app}}{\Phi_0} = \frac{i_g M}{2\pi \Phi_o(N-1)}, \qquad (2.12)$$

which is known as the frustration and measures the number of flux quanta in a unit

cell. Therefore, the gain can be written as

$$G = D\left(\frac{M}{L_J}\right)\frac{N}{N-1}\frac{1}{(2\pi)^2},$$ (2.13)

where $D = -(\frac{\Delta i_c}{i_{co}})/\Delta f$. Consequently, the problem of estimating G has been reduced to finding two separate terms: M which is a property of the method of inductive coupling, and D which is a property of the array in a magnetic field.

For injection of i_g into the loop, M_ℓ is given as

$$M_\ell = \mu_o \int_0^w \int_d^{l+d} \frac{1}{x}dxdy = \mu_o w \ln \frac{l+d}{d}$$ (2.14)

Here l is the length of the array which is $(N-1)p = 80\,\mu m$ in our samples; w is the width of the array which is about $p = 10\,\mu m$; and d is the distance of the loop from the array which is about $1\,\mu m$. Therefore, M_ℓ can be approximated by $M_\ell \approx 4.4\mu_o p = 4L_s$.

If i_g is injected parallel to the length of the array, $M_\|$ is

$$M_\| = \mu_o \int_0^l \int_{d'}^{w+d'} \frac{1}{y}dydx = \mu_o l \ln \frac{w+d'}{d'}$$ (2.15)

Here, d' is the distance of the control line from the array, $d' = 1\mu m$, so we can approximate $M_\|$ by $M_\| \approx 2.4(N-1)\mu_o p = 2.2(N-1)L_s$. With this manner of gate current injection, we get about a factor of $0.55N$ increase in G. For current injection parallel to the array,

$$G_\| \approx \frac{1.1}{2\pi^2}\frac{ND}{\Lambda_J^2}$$ (2.16)

and current injection by a loop is

$$G_\ell \approx \frac{1}{\pi^2}\frac{D}{\Lambda_J^2}.$$ (2.17)

The problem of finding G has now been reduced to determining D, the suppression of i_c by f. For penetration depths $\Lambda_J >> 1$, the critical current i_c of an array of N

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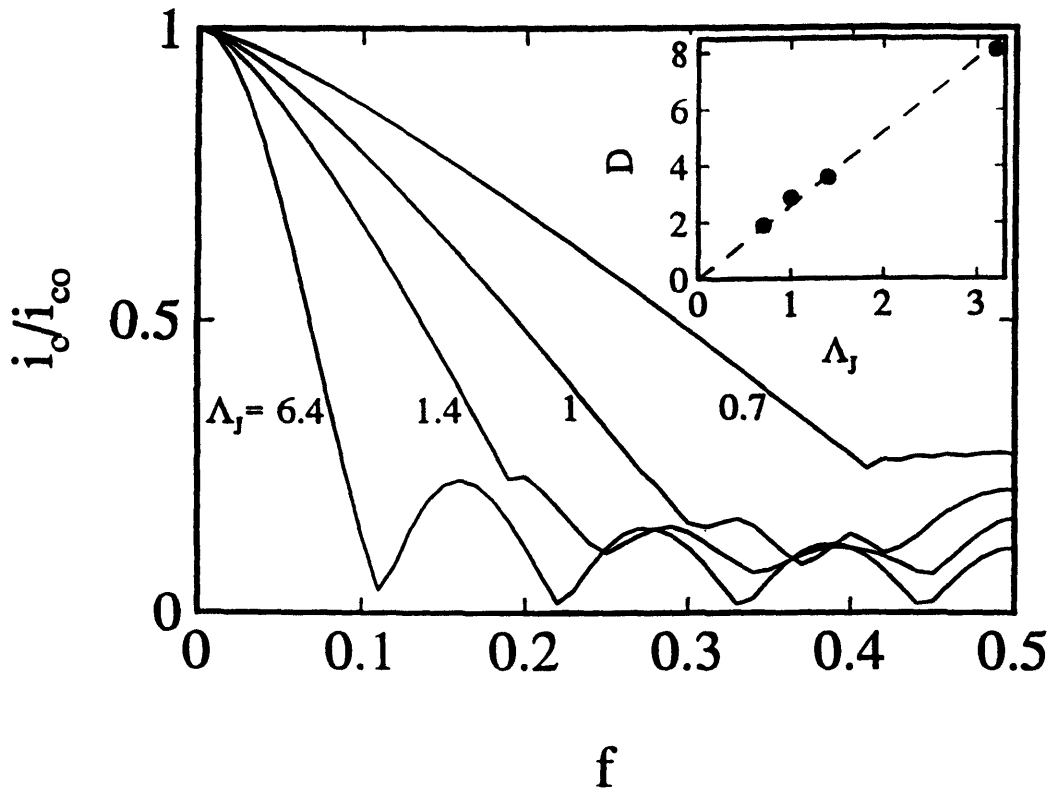
Figure 2-6: The array critical current as a function of the frustration for four different values of Λ_J. The plot is a result of a numerical sumulation on an array with 9 junctions and uniform current injection when considering self-inductances only. The inset shows the linear dependence of D on Λ_J for an $N = 9$ array.

junctions depends on the external magnetic flux [15] as

$$i_c(f) = I_c \left| \frac{\sin N\pi f}{\sin \pi f} \right| \tag{2.18}$$

so that $D \approx N$. Therefore, G can be made larger by decreasing Λ_J. As Λ_J is decreased below N, self-induced fields by the supercurrents in the DVFT become important and the dependence of i_c on f must be calculated numerically [16]. The suppression of i_c depends on the manner of injection of current into the array; the current can be injected uniformly, in the middle of the array, or at one or both edges of the array. In Fig. 2-6, we show the result of numerical calculations for uniform current injection in an array with $N = 9$. The curves in this plot are obtained from calculations with the self-inductance of the loops only. (Inclusion of all the inductances of the array and different ways of current injection can be accounted for in our simulations [16].)

With Fig. 2-6 and similar curves for various N, we have found D as a function of Λ_J for $\Lambda_J < N$. The result is shown in the inset of Fig. 2-6. We note that for uniform

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current injection and $\Lambda_J < N$, then $D \approx 2.6\Lambda_J$, independent of N. Therefore, for $\Lambda_J < N$,

$$G_{\parallel} \approx 0.15\frac{N}{\Lambda_J} \qquad (2.19)$$

and

$$G_\ell \approx 0.26\frac{1}{\Lambda_J}\,. \qquad (2.20)$$

In our sample with $\Lambda_J = 0.76$ and for parallel injection of i_g, we expect $G_{\parallel} \approx 1.8$ which agrees with my measurement of $G_{\parallel} = 1.2$. Likewise, for loop injection we expect $G_\ell \approx 0.34$, which agrees well with the experimental value of 0.35. Hence, we conclude that our model provides good estimates for the gain.

From Eqs. 2.19 and 2.20, we see that the highest gains are found for low Λ_J values. However, it is difficult to make arrays with Λ_J much less than 0.1 without making the cells too big. We also see that gains of 10 or higher are difficult to obtain for an array with 9 junctions. One could increase N, in order to increase $G_{\parallel}$; however, this will lead to a longer response time and smaller output resistances. Better magnetic coupling, such as with the ground plane [2], also increases G. We also expect that including mutual inductance effects [16], will not significantly change the value of the gain.

It is also interesting to compare the gain of an array to that of a two junction SQUID, which is an array with $N = 2$. The gain of the SQUID, G_{SQ} is still given by Eq. 2.13. Also the magnetic coupling M of the SQUID is given by Eqs. 2.14 and 2.15 with $w = \ell = p$ and $d = d'$, since for a square cell, "loop" and "parallel" current injection are the same. Finally, the estimate of D can be derived noting that for $\Lambda_J < 1$, the change of a 1/2 flux quantum of applied field, decreases the critical current of the SQUID from $i_{co} = 2I_c$ to $i(1/2) = I_{\min}$. From Fig. 12.20 of Ref. [14] which shows $I_{\min}$ as a function of Λ_J^2, we find that for the SQUID $D = 1.6\Lambda_J$. For

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[2]Another possible method of control is to have i_g flow uniformly through a thin ground plane of width W placed directly over or under the array. A constant magnetic flux density $B = \mu_0 i_g/2W$ then passes through the array, and the current gain is then $G_{\text{gp}} = D\frac{N}{4.4\pi}\frac{L_t}{L_J}\frac{p}{W}$ The width W could be of the order of p, which means that $G_{\text{gp}} > G_{\parallel}$. Hence, this method provides a better coupling than the methods using filamentary conductors.

$p = 10\,\mu\text{m}$, $d = 1\,\mu\text{m}$, and $M = 2.4\mu_o p \approx 2.2 L_s$, then

$$G_{\text{SQ}} \approx 0.18 \frac{1}{\Lambda_J} \qquad\qquad (2.21)$$

for $\Lambda_J < 1$. Moreover, as Λ_J approaches zero, $I_{min}/(2I_c) = 1 - \pi\Lambda_J^2$ [14] and $D = 2\pi\Lambda_J^2$ indicating that the current gain saturates at about 0.7 for the numbers given above. Consequently, we see that it is difficult to get gains greater than one with this manner of magnetic coupling. We note that G_{SQ} is about 50% lower than G_ℓ, as to be expected from the increased magnetic coupling from all the cells in the array. Moreover, for parallel coupling, G_{SQ} is N times smaller than the array. In both cases the array provides a larger gain than a single two junction SQUID.

There are better ways to couple flux in the SQUID loop (e.g. by using pick-up coils), but there is a trade off. One would like the inductances L_{cl} of the wires used to couple the flux in the loop to be as small as possible. When several loops with control lines are connected together, the L_{cl}/r_o constant must be kept below the response time of the SQUID, which is τ_R. For τ_R of the order of 10 ps and with $r_o = 5\,\Omega$, L_{cl} must be smaller than 50 pH. This might in particular be a problem for high-T_c-devices.

In conclusion, to obtain output voltages of the order of the $I_c R_n$-product (1.75 mV for niobium at 4.2 K) one needs intrinsically shunted junctions so that J_c must be higher than 45,000 A/cm^2. To get the highest gains, Λ_J must be kept smaller than 1. However, higher gains can also be obtained by increasing the number of junctions but longer arrays will increase the response time and decrease the output resistance.

2.4   Comparison to low-T_c LJJ and High-T_c-devices

The low-T_c (niobium) long Josephson junction Current Injection Transistor (CIT) [7], like the junctions in our samples, is shunted by a parallel resistor to make the device overdamped. The transport current-voltage characteristics of this device follow the RSJ model, thus its operation is similar to our devices with one major exception that the control current is actually injected into the body of the device. Therefore, in the

CIT, there is no isolation between the input and the output which can be a problem in circuit designs. The current gain for this device has been shown to be $G \approx \ell/2\lambda_J$, where ℓ is the length of the device and λ_J is the Josephson penetration depth [7]. For a long junction made of electrodes with penetration depth λ and thickness greater than λ, then $\lambda_J^2 = \Phi_o/2\pi\mu_o J_c h$, where $h = 2\lambda + t_{\text{ox}}$ and t_{ox} is the oxide thickness of the junction.

To make a closer comparison between the DVFT and the CIT, we model the CIT as a DVFT with a rectangular unit cell: the lattice spacing along the direction of the device is given by λ_J, and the lattice spacing perpendicular to the device is h. The self inductance L_s is modeled as the inductance of a transmission line of length λ_J so that $L_s = \mu_o h \lambda_J / W_J$; where W_J is the width of the junction. The "junction" inductance is modeled as $L_J = \Phi_o/2\pi J_c W_J \lambda_J$. Consequently, the corresponding $\Lambda_J = 1$, as to be expected since the penetration depth is the lattice spacing along the array. The equivalent number of junctions is $N \approx \ell/\lambda_J$, assuming $N \gg 1$. Likewise, the corresponding resistances and capacitances are N times larger and smaller respectively than the total resistance and capacitance. Therefore, β_c remains the same for each cell as for the whole continuous junction. In the upper part of table 2.1, the parameters for the "discrete model" of the CIT are given in brackets. From these parameters we calculated the output parameters using the formulas for the DVFT. These output parameters are listed in the lower part of table 2.1 in brackets next to the experimentally measured values. The two sets of numbers agree reasonably well, suggesting the usefulness of our "discrete model." For our "discrete model" of the CIT, a gain of $\ell/2\lambda_J$ translates into $G = N/2$. This is the same dependence as Eq. 2.19 for $G_{\parallel}$ and $\Lambda_J = 1$, except for a numerical factor of order unity reflecting the different magnetic coupling used in the CIT.

An analogous "discrete model" for high-temperature superconductors was not done because the mechanism of vortex motion is probably not the same as in a Josephson junction or array. However, if the current-phase relation for high-T_c-devices is sinusoidal, one could still use our estimate of the gain. For the high-T_c-device of Ref. [10], we predict a gain of 2.2 for loop injection in reasonable agreement with the

parameter	DVFT	CIT [7]	HTc [10]	DVFT with high J_c
$J_c(A/cm^2)$	450	1000	4000	45,000
$A_j(\mu m^2)$	9	[75]	20	0.22
$I_c(mA)$	0.04	[0.75]	0.8	0.1
$i_c(mA)$	0.37	22.5	4	0.9
$R_s(\Omega)$	5	[0.8]	-	-
$R_n(\Omega)$	43	[2.7]		17.5
$C(fF)$	405	[640]	-	10
N	9	[30]	5	9
$p(\mu m)$	10	[25]	20	10
$l(\mu m)$	80	750	80	80
Λ_J	0.77	[1]	0.12	0.5
$L_s(pH)$	14	[0.44]	28	14
$L_J(pH)$	8	[0.44]	0.4	3.3
β_c	1.3	1	<1	1
$r_m(\Omega)$	0.43 (0.49)	0.2 [0.06]	10-20	2.7
G_l	0.35 (0.34)		1.1 (2.2)	0.52
$G_\parallel$	1.2 (1.77)	10 [4.5]		2.8
V_{amax} (mV)	0.15 (0.2)	0.2 [0.47]	23	1.75
r_o (Ω)	0.55 (0.55)	0.025 [0.028]	12.8	2
τ_R (ps)	- (55)	100 [42]	60	5

Table 2.1: Summary of the vital characteristics of three non hysteretic superconducting transistor technologies.
The parameters for the low-T_c-devices are taken at 4.2 K, and the ones for the high-T_c device at 77 K. The DVFT is the measured array of Figures 2-1 through 2-6. In parentheses, we quote the numbers expected from our model calculation. The high-J_c DVFT is a proposed devices based on high critical current density junctions. The CIT is the continuous junction of Ref. [7]; the bracketed numbers refer to the discrete model of the continuous devices as discussed in the text. The high-T_c device is the high-temperature superconducting flux flow transistor of Ref. [10].

experimental value of 1.1. In addition, our relation $r_m \approx r_o G$ also seems to hold for this high-T_c-device as can be seen in table 2.1.

In table 2.1, we summarize the characteristics of our measured DVFT, the CIT of Ref. [7] and the high-T_c flux flow transistor of Ref. [10]. The response times of the measured three devices are comparable, so it is hard to make a distinction among them in this respect. The CIT has the largest gain; but this is due to it having the largest effective N. If the other devices were as long, they would have comparable gains. Furthermore, the CIT would be difficult to use in complex circuit designs, because of the problem of the input not being isolated from the output and the low output voltages and resistances. The separate control over the resistances, self inductance, and lattice spacing, as well as using the same fabrication technology as other low-T_c devices also gives the DVFT a strong advantage over the CIT. The high-T_c devices have the advantage over the low-T_c devices, in that the voltage scale is increased by a factor of 100.

In table 2.1 we also list the calculated properties of a DVFT made with niobium technology similar to our measured device, but with intrinsically shunted junctions requiring critical current densities larger than $45,000 \, \text{A/cm}^2$. In our calculations, we have taken a junction critical current of $0.1 \, \text{mA}$, which is about the critical current used in the single-flux-quantum (SFQ) technology [3]. With $J_c = 45,000 \, \text{A/cm}^2$, the junctions are $0.5 \times 0.5 \, \mu\text{m}^2$, which should be possible with present technology. For $N = 9$, gains of about 3, response times around 5 ps, and voltage levels of 1.75 mV are possible. In addition, r_o and $r_{m\|}$ will be about 2-3 Ω. By making the junctions a factor 6.25 smaller (0.2 by $0.2 \, \mu\text{m}^2$), the gain will still be larger than 1, but r_o, and $r_{m\|}$ will be about 10 Ω. The response time and the voltage levels would remain the same. Except for the voltage levels, the performance of such DVFT would be the same as or better than that of the present high-T_c devices.

One of the possible applications for the DVFT is to act as an interface between the current based SFQ logic and the voltage based CMOS memory. For this application, the DVFT must have output voltage levels that are high enough to surpass the threshold levels of the CMOS gates. Output voltages on the order of 0.1 volt

are desirable. The low-T_c technology will be limited by the $I_c R_n$ product, which is 1.75 mV for Nb at 4.2 K. Therefore, to obtain higher voltage outputs one needs several DVFTs connected in series or stacked on top of each other. The high-T_c materials have an advantage in this area because the characteristic voltage scale can be much higher, although the present value of 0.02 V still seems to be too small. For other applications at 4.2 K where the output voltage is not as important, DVFTs made in niobium technology are expected to have a comparable or better performance with the advantage of using a reliable technology.

2.5 Conclusions

We have fabricated, measured, and modeled discrete overdamped vortex flow transistors made of low-temperature Josephson junctions connected in parallel. The DVFT compares in performance with the high-temperature superconducting DVFTs except that the output voltage is lower. The DVFT has advantages over the continuous LJJ in that more freedom can be exercised over the parameters, which is useful in designing specific devices. Our modeling of these devices shows that overdamped submicron junctions with high critical current densities would be the near optimal design for DVFTs. It should be possible to stack DVFTs or connect them in series, by which both the output voltage and the output resistance increase. With 100 DVFTs in series, we project output voltages greater than 0.1 V and resistances of the order of 100 Ω. However, these devices require longer control lines for injecting the gate currents and the inductances L_{cl} associated with these lines must be kept small so that the bandwidth of the circuit is not dominated by the L_{cl}/r_o time constant.

Chapter 3

Underdamped Vortex Flow Transistors

3.1 Experimental results

The underdamped DVFTs are fabricated with a four mask selective-niobium-anodization process (SNAP) technology at Lincoln Laboratory and AT&T. A schematic drawing of the array is shown in Fig. 3-1. Our underdamped DVFT consists of an array of 54 unshunted Josephson junctions with a lithographically defined area of $1.5 \times 1.5 \, \mu\text{m}^2$. At $4.2 \, \text{K}$, $\beta_c(R_n) \approx 100$. The transport current is injected into the array at the middle of the sample and the voltage across the array is measured with a pair of leads at the edge of the array. The gate current is injected from one edge to the other edge of the array through the superconducting wire connecting all junctions in parallel. We have measured three underdamped DVFTs and we will show here the results of the array with the highest Λ_J.

We have measured the $i_t - v_a$ characteristic at 4.2 K for several values of i_g as shown in Fig. 3-2. The i_t-v_a characteristic is hysteretic, which is a consequence of the low damping in the Josephson system. In the absence of an induced magnetic field, the i_t-v_a characteristic shows a critical current; and above the critical current the device directly switches to the niobium gap. By applying a gate current, i_g, we impose a magnetic flux on the array of Josephson junctions which gives rise to a

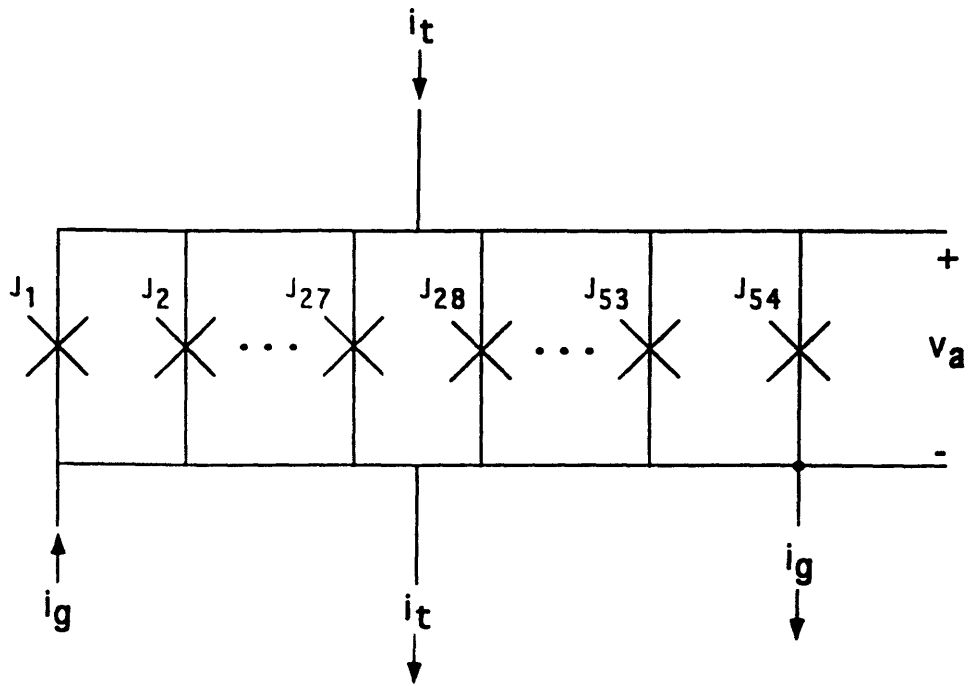Figure 3-1: A schematic drawing of the underdamped DVFT in which the transport current is injected into the middle of the array.
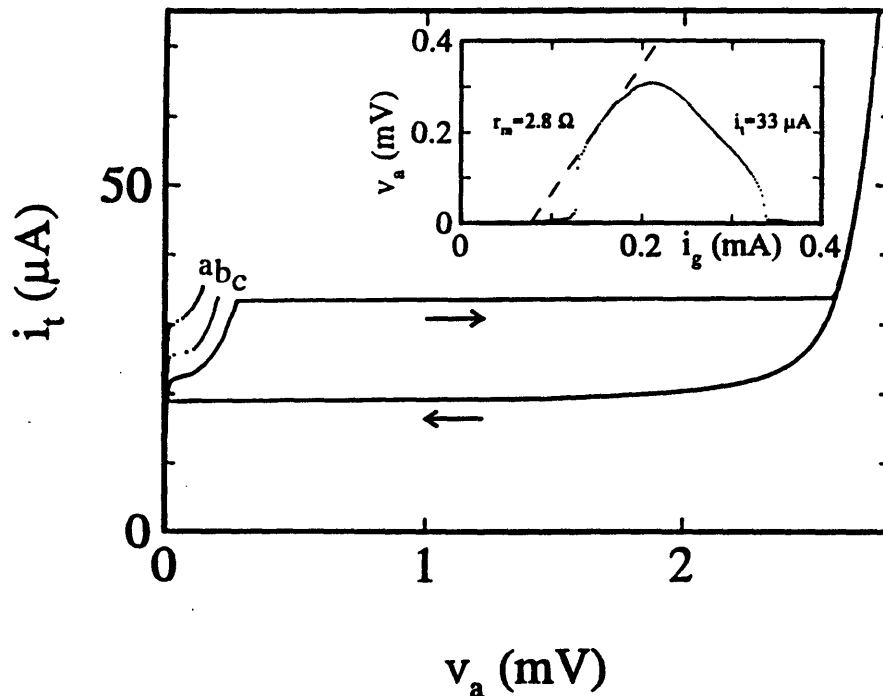

Figure 3-2: The array voltage as a function of the transport current for three different gate currents. The inset shows the input-output relation of this underdamped DVFT for a transport current of $i_t = 33\mu$A. The slope of the dashed line is the transresistance r_m.

peak in the i_t-v_a within the gap region. This peak is known as the Eck peak. As i_g is increased, the voltage position of the Eck peak increases, and its current height decreases slightly.

Because of the hysteresis in the i_t-v_a, the choice for the bias of i_t is very important. As soon as the current position of the operating point surpasses the height of the Eck peak, the voltage switches to the superconducting gap. If this happens, it is necessary to bring i_t down to 0, in order to reset the Josephson array into the superconducting state. This effect is referred to as the "latching" of the Josephson system. Thus, in order to avoid "latching", it is necessary to bias i_t below the lowest height of the Eck peak, as is shown in Fig. 3-2. But, since the Eck peak also has a finite slope, the choice of the bias of i_t also determines the range for the output voltage. Decreasing the bias of i_t would decrease the voltage range. The output resistance, r_o, is the reciprocal of the slope of the Eck peak in the i_t-v_a. The value of r_o in our samples is about $2.7\,\Omega$.

The inset of Fig. 3-2 shows the dependence of v_a on i_g for $i_t = 33\ \mu$A. There is a threshold current i_{th}, for i_g, below which there is no output voltage. This quantity represents the amount of magnetic flux required for a vortex to enter the system. The transresistance, r_m, is a function of the voltage position of the operating point. We find r_m to be of the order of $2.8\ \Omega$ as illustrated in the inset of Fig. 3-2.

3.2 DVFT Analysis

In underdamped 1D Josephson systems, resonances occur in the i_t-v_a characteristic. In a small system, there are standing modes of small amplitude phase oscillations which are called Fiske modes [17]. In the $i_t v_a$, these Fiske modes show up as current steps occurring at certain voltages. For a sufficiently long system, damping can destroy the standing wave condition and the Fiske peaks merge into one current step which is called the Eck peak [8]. The Eck peak can also be explained in terms of vortex motion. The magnetic field introduces vortices in the array which are accelerated by the transport current to velocities close to the speed of light in the array. The number

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of vortices leaving the array per unit time determines the voltage. The higher the magnetic field, the more vortices are introduced and the higher the voltage. In fact, a linear dependence of the voltage on the applied magnetic field has been observed in long Josephson junctions [8]. There have been no previous reports on measurements of Eck peaks in underdamped DVFTs.

In a long Josephson junction of length ℓ and Josephson penetration depth λ_J, a magnetic field causes an array of vortices to enter with periodicity λ_J/f. Here, $f = \frac{Bh\lambda_J}{\Phi_0}$, where B is the external magnetic flux density penetrating the junction and $h = t_{ox} + 2\lambda_J$. Here, t_{ox} is the thickness of the insulating barrier in the Josephson junction. However, for vortices to enter, the f must be larger than f_{c1}, the lower critical field. For $f > f_{c1}$, the phase of the array of vortices can be approximated as a sinusoidal wave with wavenumber $k = 2\pi f/\lambda_J$. Since the vortices of an Eck peak move at the speed of light $\bar{c}$, the corresponding angular frequency for the wave is $\omega(k) = \bar{c}k$. Note that $\omega(k)$ is the dispersion relation of the transmission line without the Josephson tunneling channel. The voltage of the Eck peak is given by the Josephson voltage-phase relation,

$$v_E = \frac{\Phi_o}{2\pi}\omega(k)\,. \tag{3.1}$$

Using the dispersion relation, one finds the known relation $v_E = \Phi_o \bar{c} f/\lambda_J$, which is linear in the magnetic field [8].

We have performed an analysis for the Eck peak in discrete systems similar to that for long continuous junctions [18]. For $f > f_{c1}$, the phase of the vortices in the discrete array for $\Lambda_J \gg 1$ can be approximated again by a sinusoidal wave with wavenumber $k = 2\pi f/p$. We find that for a general f the voltage at the Eck peak is still given by Eq 3.1. However, $\omega(k)$ is the dispersion relation of the discrete array without the Josephson channel; that is, the dispersion relation of a ladder network of inductances and capacitors. If only the self inductance L_s is considered, we find that

$\omega(k) = (2\bar{c}/p)|\sin kp/2|$. This gives the voltage at the Eck peak of

$$v_E = \frac{\Phi_o}{\pi\sqrt{L_s C}} |\sin(\pi f)| \ . \tag{3.2}$$

For small f we obtain the result for the continuous junction, $v_E = \Phi_o \bar{c} f / \lambda_J$ where $\bar{c} = p/\sqrt{L_s C}$ for a discrete transmission line. Because of the discreteness, v_E is periodic in f with period $f = 1$ and $v_E(f)$ bends at the first Brillouin zone edge at $f = 0.5$. The periodic nature of v_E is an extra factor that must be taken into account in the operation of the underdamped DVFT. In general one needs to keep $f < 0.5$.

In the experiment we have observed sine-like behavior in the input-output relation above an entry field f_{c1} of 0.2. The measured maximum voltage is $0.3\,\mathrm{mV}$ which is in good agreement with the expected value of $\Phi_o/(\pi\sqrt{L_s C})$. Table 3.1 contains the values of the parameters for the underdamped DVFT. To increase the maximum voltage one could decrease the cell size (decrease L_s) and/or decrease the junction area (decrease C). A reduction of L_s can also be obtained by using a superconducting groundplane. Of course, the output voltage is limited by the $I_c R_n$ product.

The transresistance r_m is can be found by noting that

$$r_m = \frac{\partial v_E}{\partial i_g} = \frac{\partial v_E}{\partial f}\frac{\partial f}{\partial i_g} \ . \tag{3.3}$$

Using Eqs. 2.12 and 3.2 along with the definitions for M from Eqs. 2.14 and 2.15, we find that for loop injection of i_g

$$(r_m)_\ell = \frac{2}{\pi(N-1)}\sqrt{\frac{L_s}{C}} \cos\pi f \tag{3.4}$$

and for i_g injected parallel to the array

$$(r_m)_{\parallel} = \frac{1.1}{\pi}\sqrt{\frac{L_s}{C}} \cos\pi f \ . \tag{3.5}$$

Since these formulae are only valid for $f > f_{c1}$, we must choose a value of f to compare with our data. From the inset of Fig. 3-2 we see that the value of r_m was

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chosen is near $f \approx 3/8$. For this f and with the parameters listed in Table 3.1, we estimate that $(r_m)_{\parallel}$ is $1.4\,\Omega$ which agrees well with the measured value of $2.8\,\Omega$.

Although there is no expression for the current-voltage characteristic of the Eck peak, we assume that the vortex velocity u is the same as found for a single vortex driven by a current in the absence of an applied magnetic field. From Ref. [19], this velocity in a long Josephson junction is given by $u = \bar{c}(1 + 16i_c^2/\pi^2 i^2 \beta_c)^{-1/2}$. By assuming now that each vortex in an applied field moves with this same velocity, we find that the voltage is $v_E = \Phi_o u f / p$. Hence,

$$v_a(i_t) = \frac{\Phi_o f \bar{c}}{p\sqrt{1 + \frac{16 i_c^2}{\pi^2 i_t^2 \beta_c}}} .$$

(3.6)

Therefore, for $\beta_c \gg 1$, $i_t \approx i_c$ and $\bar{c}/p = 1/\sqrt{L_s C}$, then

$$r_o \approx \frac{16 \Lambda_J^2 f}{\pi \beta_c} \sqrt{\frac{L_s}{C}}$$

(3.7)

Using the parameters listed in Table 3.1 and setting $f = 3/8$, we get an estimate of r_o of about $1\,\Omega$ which compares with the measured value of $2.7\,\Omega$.

We can estimate the response time as the transit time for a vortex to travel across the array. The maximum vortex velocity is $p/\sqrt{L_s C}$, so that the expected transit time τ_t is $(N-1)\sqrt{L_s C}$. For our underdamped DVFT, we find $\tau_t = 60\,\text{ps}$. Again, a decrease of the response time is obtained by decreasing L_s and C.

When comparing two samples with three different Λ_J's, we have seen a better performance for the sample with the higher Λ_J value. In that sample the Eck peak is also more pronounced leading to a smaller output resistance. This indicates that one would like to have $\Lambda_J > 1$, which is the assumption we made in our analysis. In that respect, our design with $\Lambda_J = 1.3$ is far from optimal. Improvements could be obtained by decreasing L_s and C yielding higher output voltages, higher speed and higher Λ_J values. We expect that for higher Λ_J values the Eck peak becomes more pronounced so that the output resistance would also be smaller.

3.3 Comparison to LJJ

The operation of the vortex flow transistor in the underdamped region has been studied using long Josephson junctions [20, 21, 22]. Because the magnetic coupling into the LLJs is different, a direct comparison of the transresistance is not possible. The value of r_m that appears in the literature is inversely proportional to the control line width, W_s. An experimental expression for r_m for NbN/Pb-alloy junctions has been determined [21] to be: $r_m = \frac{375m\Omega-\mu m}{W}$. This dependence on W follows from calculating r_m with the plane method of magnetic coupling described earlier. This gives $r_m = \sqrt{(\mu_o ht/\epsilon)}/2W$, which for typical parameters and dielectric constant ϵ gives $r_m W$ to be a few hundred $m\Omega$-μm. In practical devices W can be as small as $5\mu m$. The transresistance also can be slightly increased by reducing the control line thickness, thus further increasing the inductance of the control line.

The maximum output voltage can not exceed the superconducting gap of the material. So, the maximum output voltage of the Nb-Aℓ_2O$_x$-Nb junctions is never greater than 1.75 mV. The NbN/Pb-alloy junctions have output voltages as high as 3 mV [20].

The output resistance reflects the slope of the Eck peak. Ideally, the Eck peak should be as vertical as possible, yielding in an infinitesimal output resistance. Output resistances have been reported as low as 0.1 mΩ [21] in long junctions.

The speed of the long Josephson junction-based VFTs depends on the length of the device. Amplifiers based on the long junction VFT have been shown to have reasonable gain up to 100 GHz [22]. This value implied delay times on the order of 10 ps.

In Table 3.1 we compare the results for the LLJ [9] with those of the underdamped DVFT. We see that the DVFT is better in most regards to the LJJ. However, both of these devices are inferior in performance to the overdamped junctions.

parameter	DVFT	LJJ [9]
J_c (A/cm^2)	670	350
A_j (μm^2)	2.25	[920]
I_c (mA)	0.012	[3.2]
R_n (Ω)	145.8	[0.6]
C (pF)	0.15	[7.8]
N	54	[35]
p (μm)	12	[23]
l (μm)	636	800
Λ_J	1.3	[1]
L_s (pH)	16.6	[0.1]
L_J (pH)	27.7	[0.1]
β_c	120	[28]
$r_{m\parallel}$ (Ω)	2.8 (1.4)	0.002 [0.015]
i_{th} (mA)	0.125 (-)	48 [-]
V_{amax} (mV)	0.31 (0.42)	0.17 [0.75]
r_o (Ω)	2.7 (0.3)	1 [0.008]
τ_R (ps)	- (84)	100 [30]

Table 3.1: Summary of the vital characteristics of two hysteretic superconducting transistor technologies.

The DVFT is the measured array of Figures 3-1 and 3-2 and LJJ is the continuous junction of Ref. [9]. In parentheses, we quote the numbers expected from our model calculation for the DVFT and the bracketed numbers refer to the discrete model of the continuous devices as discussed in the text. A_j is the defined junction area; the actual junction area of the DVFT is 1.8 μm^2. The capacitance of these junctions is higher than expected due to parasitic contributions [12].

3.4 Conclusions

We have fabricated, measured and modeled discrete underdamped vortex flow transistors made of low temperature Josephson junctions connected in parallel. We have also constructed a discrete model to the published data on the underdamped vortex flow transistors based on long Josephson junctions. In comparison with these long junction based transistors, the underdamped DVFT performs better. In comparison with the overdamped DVFT, the underdamped DVFT has the disadvantage of having a hysteretic i_t-v_a relationship. This hysteresis makes the underdamped DVFT much more sensitive to the fluctuations in i_c caused by noise or any other factors.

Chapter 4

Implementation of the DVFT

4.1 Introduction

In the preceding chapters, the fundamentals of the operation of the overdamped and underdamped vortex flow transistors have been introduced. This chapter discusses the role that these fundamentals play in the implementation of the Discrete Vortex Flow Transistor in circuits. The underdamped DVFT is much harder to implement than its overdamped counterpart, because of its hysteretic $i_t - v_a$ relationship, so we will concentrate on the overdamped DVFT.

We attempted to use SPICE to simulate DVFT circuits, in order to determine the effects of the individual characteristics of the DVFT on its performance in simple circuits, such as an inverter, memory cell, or an oscillator. We were successful in programming an approximate model of the overdamped DVFT into SPICE, but attempts to embed this model into more complex circuitry ran into computational problems. Nevertheless, we can still gain some important information from hand calculations of the performance of a simple inverter.

4.2 Inverter

Consider an inverter shown in Fig. 4-1. The bias current i_b can be thought of as a supply current. The gate current i_g is assumed to be fed by other DVFT circuits. If i_b
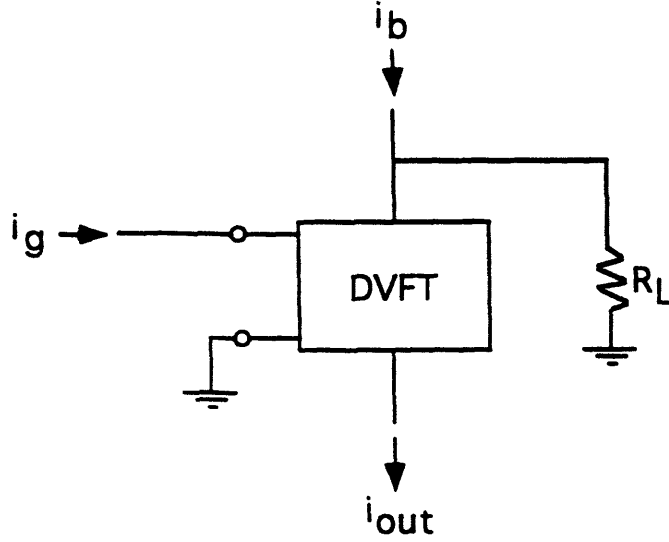
Figure 4-1: A schematic drawing of a DVFT based inverter.

is biased below i_{co} of the DVFT, then for a zero i_g, the i_c of the DVFT is unsupressed and remains at i_{co}. In this case, the entire bias current i_b is flowing through the DVFT, resulting in a zero voltage across the resistor. Therefore, there is an output current, $i_{out} = i_b$, for a zero gate current. Thus, a logic "1" on the output corresponds to a logic "0" on the input.

Now, suppose there is a gate current corresponding to a logic "1" that suppresses the i_c of the DVFT. Since the bias current exceeds the critical current of the DVFT, the bias current will flow through both the DVFT and the load resistor, R_L. Since there is a finite current flowing through the resistor, there is a voltage across the parallel combination of the DVFT and R_L. Therefore, the DVFT must be in the resistive state. We can solve this problem either graphically by combining the i_t-v_a relationship of the DVFT and the load line of the resistor, or by simultaneously solving the system of equations for the output current i_t:

$$v_a = r_{eq}\sqrt{i_t^2 - i_c^2} \qquad (4.1)$$

$$v_a = R_L (i_b - i_t) \qquad (4.2)$$

The solution of this system of equations is:

$$i_t = \frac{-i_b R_L^2 \pm r_{eq}\sqrt{i_c\left(r_{eq}^2 - R_L^2\right) + i_b^2 R_L^2}}{r_{eq}^2 - R_L^2} \tag{4.3}$$

Consider the limit of $i_c = 0$. The expression for i_t reduces to:

$$i_t = \pm i_b \frac{R_L}{r_{eq} \pm R_L} \tag{4.4}$$

In this, expression, the upper sign is the only physically realizable situation, since the lower sign would give us a current opposite in sense to i_b, unless $r_{eq} < R_L$, in which case we get a current that is larger than i_b, which is impossible. Thus, if we are able to conceive a situation where i_c is suppressed to zero, the expression for i_t simplifies to a simple current divider relation:

$$i_t = i_b \frac{R_L}{r_{eq} + R_L} \tag{4.5}$$

Ideally, we would like i_t, which is the output current, to be zero in this case, since we are trying to invert an input of logic "1". Thus, from the above argument, it is evident that for this particular implementation it is necessary not only to be able to suppress i_c to zero, but make $R_L \ll r_{eq}$.

From the simulations shown in Fig. 2-6, we know that i_c does not go to zero for small Λ_J. In order to divert current from the output, i_t has to be greater than i_c. If the minimum level of i_c increases, then the amount of current diverted from the output decreases. Thus, the logic "0" output current is increased, which is a very undesirable effect. In other implementations, that do not use a shunting resistor, the maximum suppression of i_c still remains a critical problem that must be solved, because the degradation of output logic "0" can potentially create errors, since a nonzero current can be interpreted as a logic "1" by the subsequent stages. There are several possible solutions to this problem.

From the earlier discussion on the gain of overdamped DVFTs, we know that

the gain is: $G = 0.15\frac{N}{\Lambda_J}$. This suggests that to get large gain with relatively small transistors, it is necessary to have small Λ_J. On the other hand, from Fig. 2-6, we see that as Λ_J is decreased, the minimum value of i_c, i_{cmin}, increases. Thus, from the above discussion, we see that the only way to have low levels of i_{cmin} and have large gain would be to have large N and large Λ_J. Figure 2-6 also shows that for large Λ_J there are nonlinear "ripples" in the dependence of i_c on i_g. This is an undesirable artifact, and there are several possible solutions to this problem.

In the literature dealing with Josephson junctions [15], there have been some successful attempts at reducing the "ripple" effect in the i_c behavior in the magnetic field. Instead of being uniform in shape along its length, the Josephson junction can be shaped such that the critical current I_c is greater in the middle and smaller along the length of the junction towards the ends. The dual of this would be to arrange a parallel combination of short junctions such that the Josephson junctions with larger areas would be in the middle of the array and decrease the junction area along the length of the array away from the middle.

It is important to remember that $\Lambda_J = \sqrt{\frac{\Phi_o}{2\pi I_c L_s}}$. Thus, Λ_J can be increased by decreasing the junction critical current, or decreasing the self-inductance of the loops by making them small or including a ground plane underneath the entire transistor, which decreases L_s by a factor of 5.

Factors such as the nonzero logic "0" output of the DVFT inverter and the presence of noise suggest that we need a threshold level for the operation of DVFT circuits. This threshold can be accomplished in a variety of ways. We can bias the DVFT below the maximum critical current, i_{co}, which is shown in Fig. 2-4. As the bias of i_t is decreased, the threshold for the "turn-on" of the DVFT is increased.

Another way of introducing the threshold level is to inject the bias current into the DVFT in the middle of the array, rather than using uniform injection. The behavior of i_c in magnetic field for middle current injection is shown in Fig. 4-2. This figure closely resembles the ideal inverter transfer characteristics. Current injection in the middle of the array also helps to reduce the power consumption, because this would eliminate the bias resistors that are used to achieve uniform current injection. The disadvantage
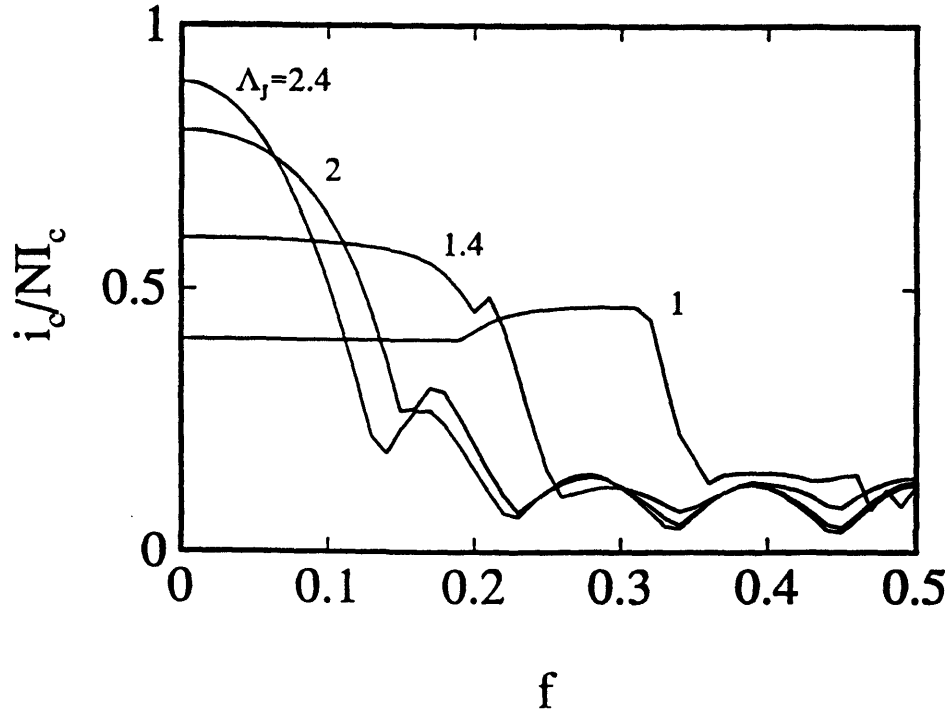
Figure 4-2: The array critical current as a function of the frustration. The plot is a result of a numerical simulation on an array with 9 junctions and current injection in the middle when considering only the self-inductances.

of using middle bias current injection is the fact that i_{co} is strongly sensitive to the penetration depth in the array, which in turn, is a function of the critical current density of the Josephson junctions. Thus, to use middle bias current injection, the fabrication process must have tight controls that allow good reproducibility of the target critical current density. Current low-T_c processes can achieve J_c within 10% -15% of the target.

4.3 Oscillator

A DVFT based oscillator can be realized by feeding the output of the inverter shown in Fig. 4-1 back to the input of the same inverter. This creates a feedback loop that results in the oscillation of i_{out}. This method is similar to the clock oscillators used in many CMOS integrated circuits. The period of the oscillations is approximately

	$J_c = 450\ \mathrm{A/cm^2}$	$J_c = 12\ \mathrm{kA/cm^2}$	$J_c = 45\ \mathrm{kA/cm^2}$
frequency (GHz)	3.7	5.6	5.9

Table 4.1: Oscillation frequency for a single stage DVFT inverter based oscillator

equal to twice the response time of the inverter. Thus, the oscillation period is:

$$T = 2\left(\tau_R + \frac{L_L}{R_L}\right) \qquad (4.6)$$

Here, τ_R is the DVFT response time defined in equation 2.10, and L_L is the inductance of the line connecting the DVFT with the load. We can monitor the oscillations by directly observing the transitions with a current to voltage converting DVFT, magnetically picking up the signal, or indirectly by measuring the voltage across a series connected Josephson junction. Assuming $L_L = 40\mathrm{pH}$, and $R_L = 0.5\Omega$, table 4.1 shows the expected frequency for different J_c. In table 4.1, the only parameter that is changed is J_c, and the delay through the DVFT becomes negligible as the junctions in the array become intrinsically shunted, thus it becomes possible to measure delay times arising from propagation along superconducting lines. Thus, it is possible to precisely measure inductances of superconducting lines.

Chapter 5

Conclusion

5.1 Summary

In this thesis, we have described the operation of two versions of a Discrete Vortex Flow Transistor. We have included analytical models that describe the operation of the transistors. When compared with experimental data, the models were in good agreement. Therefore, we can conclude that the models presented here are valid.

From the analysis of the overdamped DVFT, we saw that we can construct an equivalent RSJ model to describe the entire array of Josephson junctions as a single entity. The maximum output voltage is $v_{amax} = \left(\frac{R_{eq}}{R_n}\right) * 1.75mV$. Here, $R_{eq} < R_s$ in the case of externally shunted junctions. We also saw that the current gain of the overdamped DVFT with parallel gate current injection is proportional to the number of junctions in the array, N, and inversely proportional to the penetration depth in the array, Λ_J.

We compared both the underdamped and overdamped versions of the DVFT with the long junction based devices and the DVFT showed better performance. In comparing the two versions of the DVFT, the underdamped version has a disadvantage. The underdamped DVFT has a hysteretic $i_t - v_a$ relationship which causes it to switch to the superconducting gap voltage when i_t surpasses i_c. This is the "latching" effect that is seen in underdamped superconducting systems. This effect causes the underdamped DVFT to be much more sensitive to fluctuations of i_c due to noise or other

factors.

Of course, the future direction for the DVFT points toward using high T_c technology. Circuits made with high T_c materials take advantage of the low cost of liquid nitrogen cooling opposed to cooling with liquid helium. Before it is possible to construct circuits with high T_c transistors, it is necessary to have a model that describes the operation of the devices. Such a model does not exist currently for the high T_c transistors.

As an example of a circuit implementation of the DVFT, we have also used the analytical model for the overdamped DVFT to analyze a DVFT based inverter. We have seen that its operation is crucially linked to the behavior of i_c in the magnetic field.

5.2 Suggestions for Future Work

The understanding of the operation of the VFT in high T_c technology is very important for future applications. Thus, it is very important to continuously improve the reproducibility of the high T_c fabrication technology and to find a successful model to describe the operation of the VFT is this technology.

The improvement of the operation of the low T_c based devices is also very important. There is a large number of research possibilities that remain to be explored in this area.

- In the analysis of the overdamped DVFT, we saw the importance of having overdamped Josephson junctions without the use of external shunting resistors. This can be achieved with high critical current density junctions. Critical current densities as high as 45,000 kA/cm^2 are needed to get $\beta_c = 1$. It is important to fabricate DVFTs utilizing these junctions and verify the operation of the DVFT under these conditions.

- It is also important to explore the possibility of improved magnetic coupling of the gate current to the Josephson array. It is possible to arrange the gate wire to form a complete loop over the entire array, if another layer of metal is available

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in the fabrication process. This method would double the coupling efficiency of the parallel method shown earlier. Thus, G would double on the account of better coupling. Of course, the gate wire can be looped many times over the array, improving the coupling even further, but increasing the length of the gate wire increases the input inductance which would slow down the response time of the device.

- If we can improve the magnetic coupling, then we can afford to reduce the surface area of the DVFT by reducing the number of junctions, N, without decreasing G. This opens up the possibility of having uniform current injection without using resistors to achieve this. This may be possible because the size of the array becomes comparable to the penetration depth, so the current would be distributed over a greater percentage of the array, so i_{co} should be more insensitive to the penetration depth. This is definitely true in the case of the penetration depth being larger than the size of the array.

- In the analysis of the DVFT based inverter we saw the importance of the behavior of i_c in the magnetic field. It is very important that i_c goes down to 0 and that i_{co} is insensitive to J_c. This would take some engineering of the array. As discussed in the previous chapter, it may be possible to vary the area of the junctions along the array, such that the larger junctions are in the middle of the array, and the area of the junctions decreases toward the ends of the array. This method may help to reduce the "ripple" effect that is seen in the behavior of i_c in the magnetic field.

- With a model describing the operation of the DVFT, we can now use the DVFT to design circuits. We saw an analysis of a simple example of a circuit implementation of the DVFT - the inverter. More complex circuits would be much harder to analyze, that is why a computer simulation tool such as SPICE is needed.

- In our model, we proposed a theoretical approximation for the response time of

the DVFT. It is important to make experimental measurements to determine the validity of our model for the response time.

- In our model, we did not include any effects of disorder in the Josephson system, which may be caused by an uncontrolled spatial variation of the critical current density. The effects of disorder can be easily included in the simulations of the behavior of i_c in the magnetic field.

- It would also be interesting to study the effects of noise in the system. There are many sources of noise, and it is an important aspect of electronic circuit design.

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