A Clamped Folded Cascode Amplifier for Analog-to-Digital Converter Applications

by

Allison Margaret Marino

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degrees of

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and

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Abstract

The performance demands on analog-to-digital converters for high speed, high accuracy, low power, and small die area are continuously increasing. Overdrive recovery time of the comparator is a speed-limiting factor in high bit accuracy successive approximation analog-to-digital converters. The bottleneck is most severe when a large input is followed by a small input of the opposite polarity. Output clamping is one way of improving overdrive recovery time. A single stage, folded cascode amplifier with clamping and auto-zeroing is presented. Active clamping is explored in detail and an auto-zeroing scheme is presented for a 12 bit analog-to-digital converter in a 0.8 micron technology. The optimized clamped folded cascode amplifier is then compared with existing comparator gain stages.

MIT Thesis Advisor: James K. Roberge

Company Supervisor: William T. Mayweather, III

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Chapter 1

Introduction

1.1 Motivation

Applications for high speed comparators in analog-to-digital converters (ADC's) range from High Definition Television to ultrasound imaging. Because the world is inherently analog, there will always be a need for faster and better ADC's to keep pace with the newest digital processing circuitry.

At the heart of analog to digital conversion is the comparator. The comparator is frequently the speed limiting factor in high bit accuracy ADC's. Overdrive recovery time is often the cause of speed loss. For example, in a 12 bit converter with a 2V input range, the comparator must be able to sense and amplify voltages ranging from under 0.49mV (an LSB) to a full scale 2V. Without careful comparator design, overdrive will inevitably occur and prevent accuracy at a high sampling rate.

The issue of overdrive recovery has not been thoroughly examined for folded cascode amplifiers with respect to clamping. Improving the overdrive performance for a folded cascode amplifier, using a non-cascoded amplifier as a reference, is an interesting and challenging technical problem.

1.2 Background

1.2.1 Sequential Successive Approximation ADC Architecture

In the sequential successive approximation (SSA) architecture, the ADC input voltage is successively compared to binary weighted voltages. The value compared to the input signal in each successive cycle is based on the outcome of the previous cycle. For an N bit converter, the digital output will be available after N clock cycles. Because the SSA architecture requires only one comparator, it is efficient in terms of die area consumption. For reference, an N bit flash type ADC requires 2^N comparators. A flash architecture works by simultaneously comparing each possible input level to the actual input voltage. For high bit accuracy converters, a full flash structure is impractical, while an SSA type remains perfectly reasonable. For more general information on ADC's, refer to [15] or [8].

To increase the throughput of an SSA converter, the comparator may be duplicated. If N comparators are used, the converter can simultaneously process N inputs,resulting in an N cycle latency and a throughput of 1 output per cycle. Additional cycles for autozeroing or error-correction may increase the latency.

1.2.2 The Comparator

A comparator is comprised of a gain stage and a latch (usually regenerative) for converting the output of the amplifier to a digital level. The amplifier explored in this thesis is designed for an existing latch used in other ADC designs at the David Sarnoff Research Center. This latch has a worst case input offset voltage of 50mV. This offset voltage is large because input accuracy has been traded for lower power consumption. The Sarnoff latch consumes approximately 1mW of power and converts an input of 50mV to a digital level in approximately 1.5ns.

Because the comparator is destined for large digital integrated circuits, a fully differential design is required to satisfy noise immunity constraints. Ease of manufacture

is also important; consequently it is assumed that no laser trimming or specialized devices, such as Schottky or high frequency diodes, are available.

1.3 Simulation Environment

To verify and improve the theoretical comparator design, Mentor Graphics Falcon Framework, Design Architect schematic editor, and Accusim simulator were used for simulations. The technology simulated was a 0.8 micron, 5V, double metal, N-well process. The SPICE modelfile was developed from measurements taken on previously fabricated chips from the vendor. Representative SPICE models are included in Appendix A.

1.4 Outline

Chapter 2 clarifies the fundamentals of the folded cascode, such as gain, parasitic output capacitance, and biasing. The MOS device models used are also included.

Chapter 3 examines passive and active clamping for the folded cascode amplifier. Clamping theory is developed, and related problems are addressed.

Chapter 4 explains the autozeroing circuitry. This circuitry is important because a large input referred offset due to sizing mismatch or threshold variations is anticipated.

Chapter 5 compares David Sarnoff's existing 12 bit non-cascoded multistage amplifier with the clamped folded cascode. The evaluation metric is speed. Conclusions and suggestions are presented.

Chapter 2

The Non-Clamped Folded Cascode

2.1 Introduction

A folded cascode architecture has the potential for very high gain, with more output swing than a non-folded cascode. As a result, the folded cascode is useful not only in the 5V technology being used for the simulations in this thesis, but also in 3V processes. An additional benefit of a cascoded design is the small back coupling from the outputs to the inputs.

In the following sections, the theoretical gain, capacitive loading, unclamped overdrive recovery time, transient response, and biasing of the folded cascode amplifier are explained. Equations are developed to enable easy modification of the folded cascode's characteristics via device sizing.

2.2 Device Modeling

The low frequency small signal transistor model used to characterize the folded cascode is shown in Figure 2-1. Equations defining the transconductance, source-drain resistance, and quiescent current are as follows:

$$g_m = \sqrt{2I_D\mu C_{ox}\frac{W}{L}}$$

$r_o = \frac{1}{\lambda I_D} = \frac{1}{g_o}$

where $I_D =$

$$\frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_t)^2, \text{ when } V_{DS} > V_{GS} - V_t > 0;$$

$$\mu C_{ox}\frac{W}{L}[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2] \text{ when } (V_{GS} - V_t) > V_{DS} > 0;$$

$$0, \text{ when } V_{GS} < V_t.$$

Appendix B explains the variables in the equations and models, and relates them to the SPICE model parameters in Appendix A.

A complete MOS device model is shown in Figure 2-2. The capacitances were considered open circuits for the gain calculations. The backgate transconductance, g_{mb}, did not have a large impact on the gain (at most a few percent) and was thus ignored for the gain calculation.

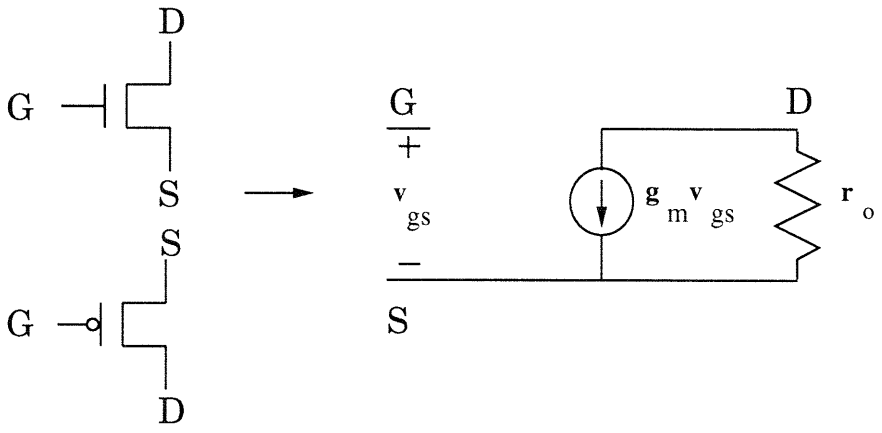


Figure 2-1: Low Frequency Small Signal Model

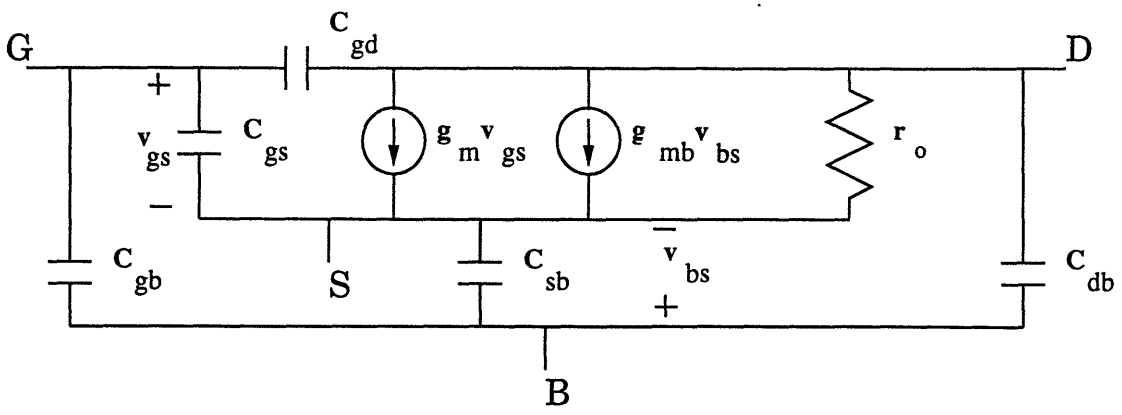


Figure 2-2: Complete Small Signal Model

2.3 Folded Cascode Gain

The fully differential folded cascode circuit is shown in Figure 2-3. A half circuit, shown in Figure 2-4, is used to calculate the small signal gain. In the half circuit, the resistances of M1 and M3 have been represented by r_{in}, which equals $r_{o1}||r_{o2}$.

Assuming no mismatch, the complete differential gain is equal to the half circuit gain. The impact of mismatch on circuit performance is addressed in more detail in Chapter 4.

The common node is grounded in the half circuit because any change in voltage on that node would be reflected as common mode gain, and thus would have no impact on the differential gain. For further discussion on the common node virtual grounding approach, refer to [14, pages 255-257].

A Norton equivalent circuit approach is used to calculate the gain of the half circuit. In a Norton equivalent circuit, shown in 2-5, the behavior of a more topologically complex circuit is exactly modelled as a current source and resistor in parallel.

Figure 2-6 shows the circuit used to determine the short circuit current. Figure 2-7 shows the circuit used to calculate the equivalent resistance.

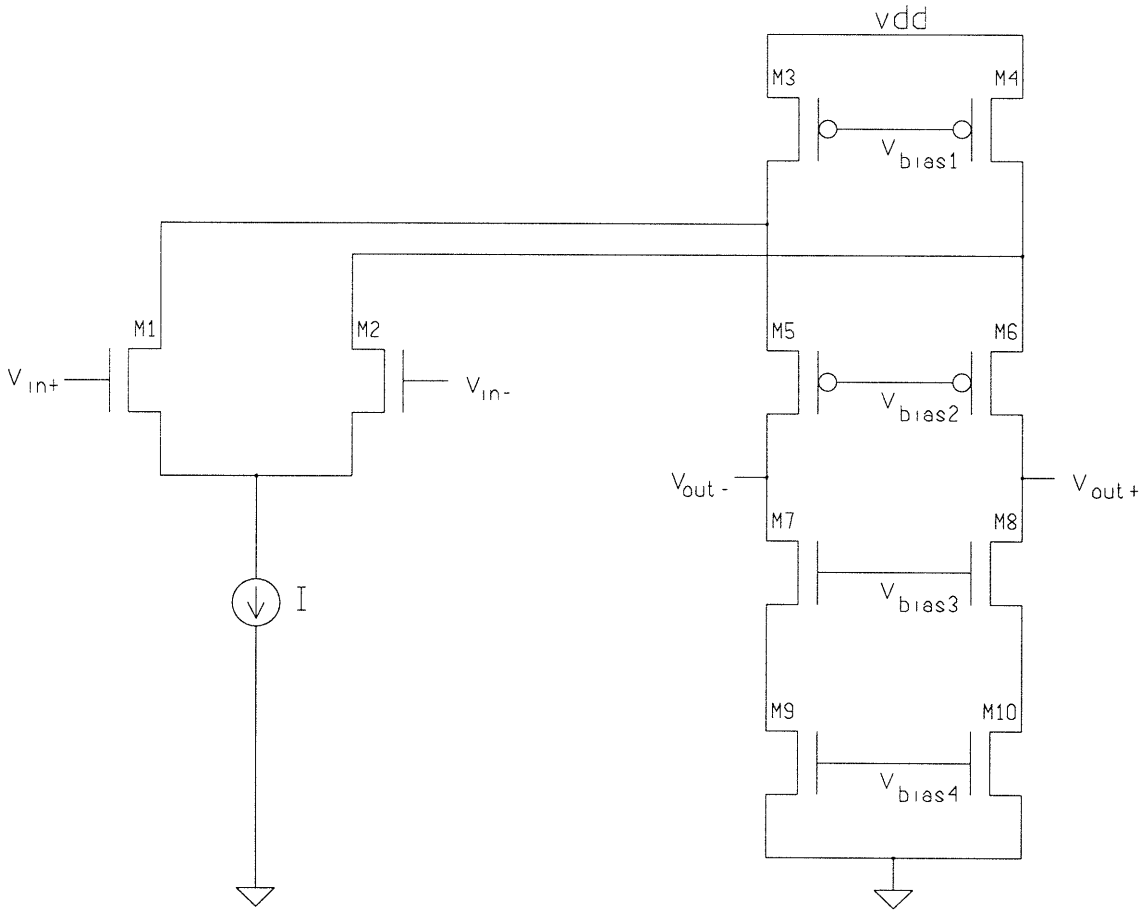


Figure 2-3: Fully Differential Folded Cascode Circuit

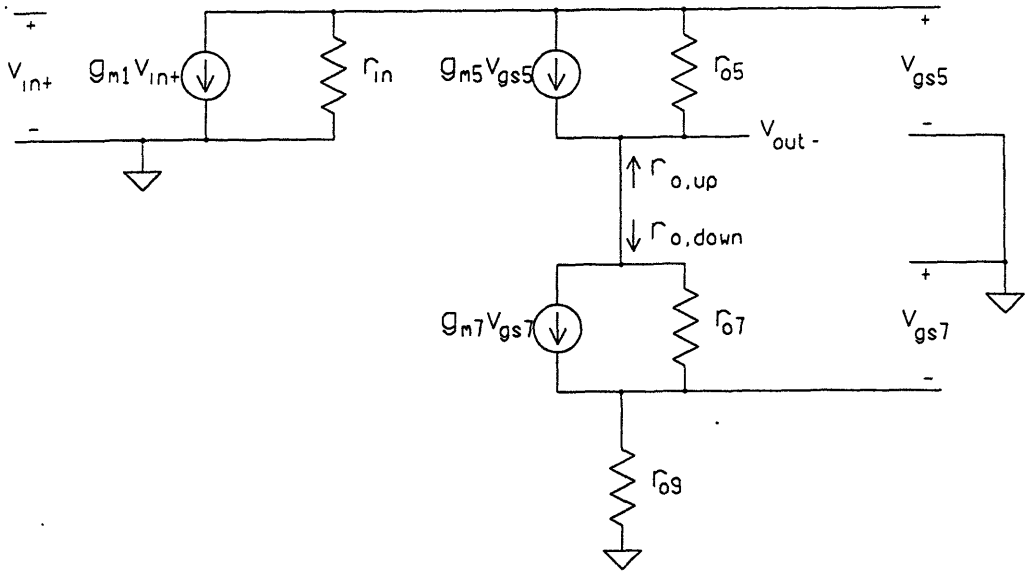


Figure 2-4: Half Circuit for Small-Signal Gain Calculation

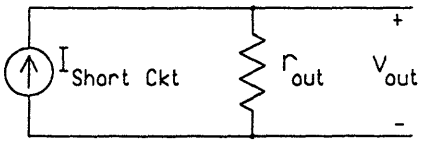


Figure 2-5: Norton Equivalent Circuit

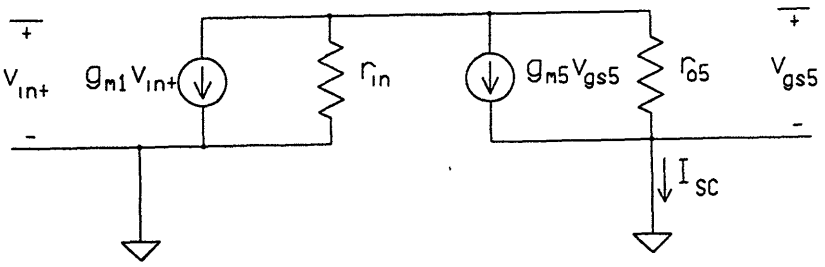


Figure 2-6: Circuit for $I_{ShortCkt}$ Calculation

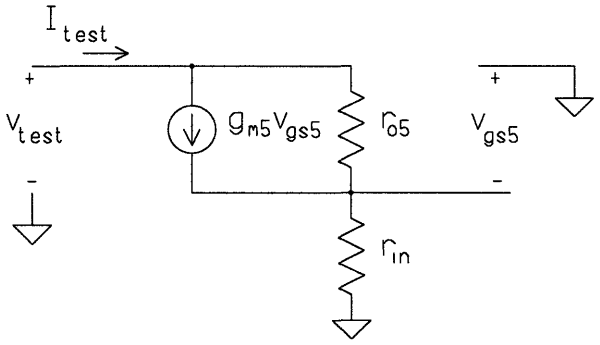


Figure 2-7: Circuit for $R_{o,up}$ Calculation

The short circuit current is calculated as follows:

$I_{SC} = g_{m5}v_{gs5} + v_{gs5}/r_{o5} = -g_{m1}v_{in} - v_{gs5}/r_{in}$

$v_{gs5} = \frac{-v_{in}g_{m1}}{g_{m5}+g_{o5}+g_{o,in}}$

$I_{SC} = v_{in}(\frac{g_{m1}g_{o,in}}{(g_{m5}+g_{o5}+g_{o,in})} - g_{m1})$

In order to calculate R_{out}, $R_{o,up}$ and $R_{o,down}$ must also be calculated. The g_m's and r_o's specified in Figure 2-7 are for $R_{o,up}$ as noted in Figure 2-4. $R_{o,up}$ is calculated as follows:

$I_{test} = g_{m5}v_{gs5} + \frac{v_{test}+v_{gs5}}{r_{o5}} = -v_{gs5}/r_{in}$

$v_{gs5}(g_{m5} + g_{o5} + g_{o,in}) = -V_{test}g_{o5}$

$I_{test} = \frac{V_{test}g_{o5}g_{o,in}}{(g_{m5}+g_{o5}+g_{o,in})}$

$R_{o,up} = V_{test}/I_{test} = \frac{(g_{m5}+g_{o5}+g_{o,in})}{g_{o5}g_{o,in}}$

Since $R_{o,down}$ has an identical topology:

$R_{o,down} = \frac{(g_{m7}+g_{o9}+g_{o7})}{g_{o7}g_{o9}}$

Thus,

$R_{out} = R_{o,down}||R_{o,up}$

If the transistors are in the saturation region (when $V_{ds} > (V_{gs} - V_t)$), then it can be assumed that $g_o << g_m$, such that the expressions for $I_{ShortCkt}$ and R_{out} simplify to:

$I_{SC} = -v_{in}g_{m1}$

$R_{out} = (\frac{g_{m5}}{g_{o5}g_{o,in}})||(\frac{g_{m7}}{g_{o7}g_{o9}})$

Putting the two results together, the total gain is

$\frac{vout^+ - vout^-}{vin^+ - vin^-} = g_{m1}[(\frac{g_{m5}}{g_{o5}g_{o,in}})||(\frac{g_{m7}}{g_{o7}g_{o9}})]$.

For the circuit shown in Schematic A, the simulated DC gain is 880. For a 12 bit converter, in dc operation such a gain will amplify half an LSB (.24mV) to 4 times the latch offset voltage.

Transistors M9A and M10A in Schematic A are used in the autozeroing circuitry and can be temporarily ignored for the gain calculation. The device sizing shown results in quiescent currents of approximately 100μA in each transistor, which yields a transconductance value of:

$g_{m1} = .92mS$

Drain-source conductance is difficult to accurately hand-calculate, so the simulator was used to determine the exact gain. Working backwards from the calculated g_{m1} and the simulated gain gives a value of $R_{out} = 0.96M\Omega$. Appendix C contains dc operating points for the folded cascode, and Appendix B contains the equations used to generate g_{m1}. It is important to have a estimate of R_{out} for speed considerations because the dominant time constant for a folded cascode amplifier is due to the output loading.

2.4 Output Capacitance

Just as an accurate output resistance value is important, an output capacitance value is necessary to predict the circuit's behavior. The following equation models the capacitive loading at the negative output terminal:

If M5 and M7 are in saturation:

$C_{load} = C_{db,5} + C_{gd,5} + C_{db,7} + C_{gd,7} + C_{misc.}$

Appendix B gives equations for drain-to-bulk and gate-to-drain capacitances. C_{misc} represents the miscellaneous loading due to any following stages and the unmodeled parasitic capacitance from the wiring.

It is important to note that the drain-to-bulk and gate-to-drain capacitances vary proportionally with W. To avoid unnecessary loading, the width of devices M5, M6,

M7, and M8 should be kept as small as possible. At equilibrium (when $V_{out-} = V_{out+} = 2.5V$), for the device sizes shown in Schematic A,

$C_{gd,7} = 0.47fF$

$C_{db,7} = 3.4fF$

$C_{gd,5} = .84fF$

$C_{db,5} = 6.8fF$

With an estimated value of 10fF for C_{misc}, this gives a value of $C_{load} = 21.5fF$.

2.5 Transient Analysis

The worst case overdrive recovery time occurs when a large input is followed by an LSB input of the opposite polarity. Assuming temporarily that the output equilibrium occurs at $V_{out-} = V_{out+} = 0V$, $V_{out-}(t)$ can be modeled as follows for a positive LSB following a negative MSB:

$V_{out-,0s} \approx -2.5$ volts

$V_{out-}(t) = [-2.5e^{\frac{-t}{\tau}} + 0.22(1 - e^{\frac{-t}{\tau}})]$ volts, $t > 0$

The first term of V_{out-} is a decaying exponential due to the state created by the negative MSB; this term exists until V_{out-} passes through 0 volts. The second term is a rising exponential caused by the new input. The 0.22V final voltage is the result of multiplying the gain (880) by half of an LSB (0.24mV for an input voltage swing of 2V). The value of half of an LSB is used because the circuit is fully differential, and the other half of the circuit is operating in exactly the same way, but with the opposite polarity. The dominant time constant is due to the output load, where $\tau = R_{out}C_{load} = (960K\Omega)(21.5fF) = 21ns$ for the circuit shown in Schematic A.

By solving for t when $V_{out-} = 25mV$, the time it takes to reach the latch offset of 50mV (assuming V_{out+} is undergoing similar changes in the opposite direction), the maximum comparison time necessary to trigger the latch can be found. For the values mentioned above, it theoretically takes 52ns to reach a differential output of 0V and 2.5ns more to reach a 50mV differential output. The total theoretical comparison time is thus 54.5ns. Simulation A shows the actual unclamped folded cascode transient

response for this case. The simulated time from the new input to the 50mV necessary for latching was measured as 57ns, just 2.5ns off of the predicted value. The extra delay is probably due to the changing gate-to-drain and drain-to-bulk capacitances, but could also be the result of a slight error in the estimate of R_{out}.

2.6 Biasing

The biasing scheme, consisting of transistors M12, M13, M14, and M15 as shown in Schematic A, consists of 4 diode connected transistors. It was chosen for its simplicity and lack of fixed voltage requirements. The current in the bias leg of the transistor is approximately 10 μA. This current is mirrored and scaled up to $\approx 100\mu A$ in all transistors except M9A, M10A, M3, M4, and M11. Transistors M9A and M10A have smaller currents than the other devices because they are for output level adjustment only; M9 and M10 carry most of the current in the parallel combination. M3, M4, and M11 have currents of approximately 200 μA. I_{M7} and I_{M8} were set slightly larger than I_{M1} and I_{M2} to avoid a situation where there is not enough current to meet the demands of the input transistors.

Chapter 3

The Clamped Folded Cascode

3.1 Introduction

The goal of clamping the outputs of an amplifier is to limit the differential output voltage as quickly as possible. The unclamped 12 bit overdrive recovery time discussed in Chapter 2 is unacceptable for high frequency applications. This chapter explores how to most effectively clamp a folded cascode amplifier to drive a regenerative latch with a 50mV worst case input offset.

MOS devices are used as the clamping devices because Schottky diodes and good high frequency diodes are not available.

3.1.1 Passive Clamping

Passive clamping is accomplished by connecting the outputs of an amplifier to the source and drain of a MOSFET (or the terminals of a complementary pair of MOSFETS's). The gate of the MOS device is tied to a fixed voltage.

Passive clamping is easier to implement than active clamping in that it requires minimal layout complexity and is not subject to any clock feedthrough. A viable passive clamp is shown in Figure 3-1, where V_{dc} is a fixed voltage (5V in most applications).

Passive clamping improves the overdrive recovery time of an amplifier, but the

speed improvements are difficult to predict because MOS thresholds and saturation V_{ds} are not sharply defined. A MOSFET threshold voltage is dependent on the terminal voltages and doping, which can vary widely on a single chip.

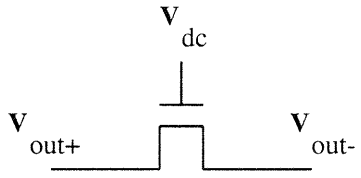


Figure 3-1: Passive Clamp

3.1.2 Active Clamping

In active clamping, the clamp gate voltage is driven by a clock, and can be with reference to a fixed voltage, as shown in Figure 3-2. However, the clamp does not have to be referenced to anything; it can simply connect two active nodes directly, as in the passive clamp Figure 3-1. If the swing on each output node is very large, a fixed voltage reference is preferable so that a charge equilibrium is reached not far from the nominal output equilibrium value. For a circuit with a large output swing, complementary transmission gates are needed to effectively clamp at both the positive and negative rails. Additionally, complementary transmission gates also partially cancel clock feedthrough.

Active clamping is more effective than passive clamping because the active clock ensures the clamp will be turned on at a certain time. The remainder of this chapter focuses on modeling and optimizing active clamping. The most challenging issues involve clock feedthrough and input timing with reference to the clamp.

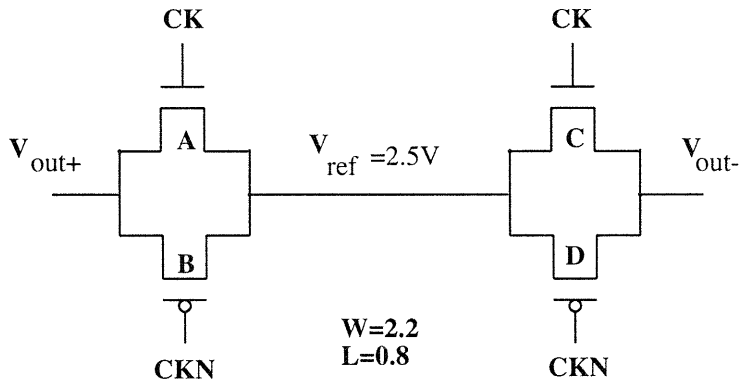


Figure 3-2: Referenced Active Clamp

3.2 Active Clamping Simulation Implementation

Due to the limitations of the SPICE model, the clamping scheme shown in Schematic B had to be used. The clamp network consists of 4 transmission gates (devices MC1-MC8) referenced to 2.5V (labelled V_{fix}). While only two transmission gates would be needed in a physical implementation, a software bug necessitated simulating with 4 to get accurate drain and source modeling. (Otherwise, the simulator yielded different results depending on the nominal location of the drain in the schematic.) This fix caused the parasitic capacitance to be non-symmetric for the devices and threw off the capacitive coupling by an unrealistic amount. By placing two devices of half the nominal width of $2.2\mu m$ in parallel with opposite drain locations, the simulator limitations were overcome. The only major problem caused by the alternate simulation implementation was an increase in the source-to-bulk and drain-to-bulk capacitances due to apparent sidewall and junction parasitic capacitances. This error is compounded by the fact that a software designer implemented the default sidewall capacitance to

be proportional to $2W + 2L_d$, not $W + 2L_d$ as is correct and as shown in Appendix B. The net effect is extra capacitive loading at the output, and slightly more clock feedthrough. Though the simulation correlation to the physical design is non-ideal, the result is tolerable because the additional capacitance (at most a few fF) effectively substitutes for the parasitic capacitance due to wiring that was not included in the simulation model. For clarity of discussion, the rest of the sections in this chapter reference the clamping scheme shown in Figure 3-2. Predicted capacitance values will be based on the device sizes shown in Figure 3-2, but the values corresponding to the actual implementation will be indicated when there is a noticeable discrepancy.

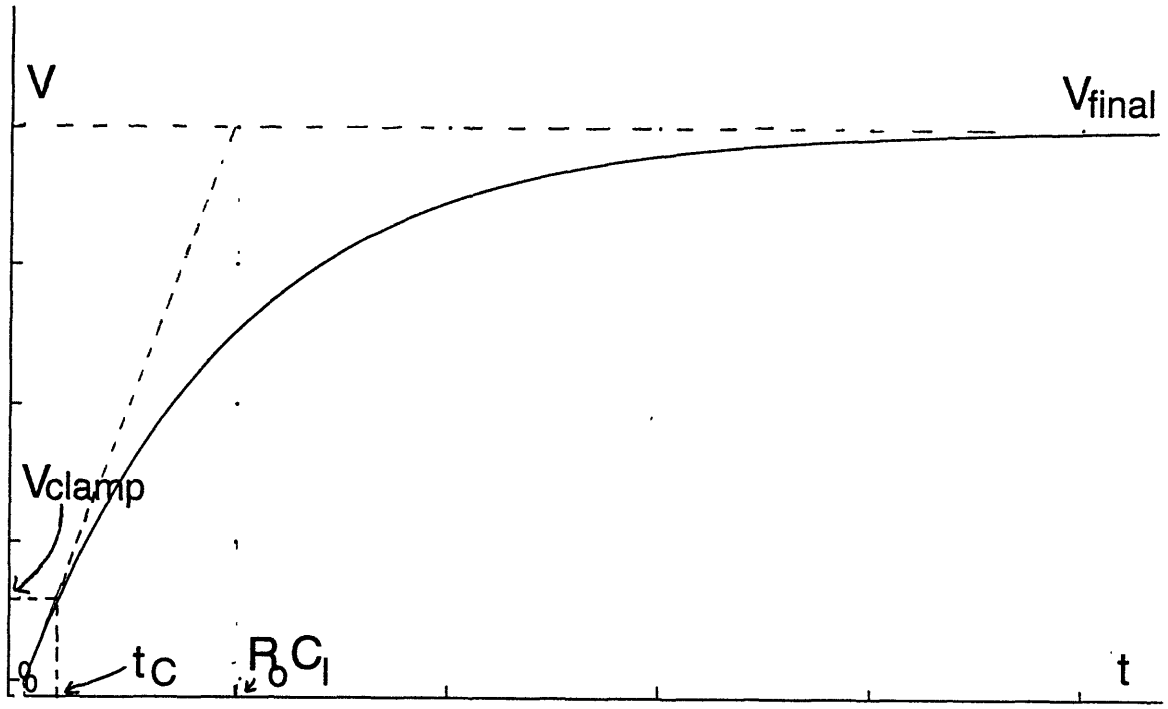


Figure 3-3: Single Stage High Gain Clamped Amplifier Transient

3.3 Clamping and Gain

In Figure 3-3, t_C represents the time from zero seconds to the time the output has moved enough to be latched, and is thus ready to be clamped. The dominant time constant R_oC_l is due to the output loading. Voltage V_{final} is the product of the

smallest input that must be recognized and the gain of the amplifier. Voltage V_C is the minimum value necessary to trigger the latch correctly. If it is assumed that:

$V_C << V_{final}$

t_C reduces to $\frac{V_C}{V_f/\tau}$

Substituting $\tau = R_L C_l$ and $V_f = g_m R_L V_{min}$ yields:

$t_C = \frac{V_C C_l}{g_m V_{min}}$

Thus, to minimize t_C, g_m should be increased. This is the sensible result, since increasing power usually increases speed. The result indicates that the specific gain of the clamped folded cascode does not matter, as long as it is high enough such that $V_C << V_{final}$. Figure 3-3 assumes an ideal clamp and does not account for clock feedthrough.

Substituting $C_l = 32fF$ (calculated in the next section), $V_C = 50mV$, $g_m = .92mS$, and $V_{min} = 0.49mV$ results in $t_C = 3.5ns$. Simulation B shows (from top to bottom) a plot of the clamp, the differential input voltage, and the differential output voltage. From the time the clamp releases, it takes 5ns for the output to reach V_C when driven by an LSB after an MSB of the opposite polarity. Part of the 1.5ns discrepancy between theoretical and measured time delay can be attributed to the $g_m 1$ calculation in Chapter 2. An alternate way of calculating g_{m1} is to work backwards from the 3dB point of the clamped folded cascode and the output load, assuming a single dominant pole. The corresponding output resistance for $f_{3dB} = 4.67MHz$ (from simulation data) and $C_l = 32fF$ (theoretical) is 1.07MΩ. Working backward from the theoretical gain of $g_{m1}R_{out}$, the simulated gain of 880, and the new value of $1.07M\Omega$ for R_{out} yields a g_{m1} of 0.83mS. Substituting this g_m into the t_C equation yields a delay of 4ns, closer to the simulated value. The remaining discrepancy can be partially accounted for by the extra capacitance introduced by the artificial 8 transistor clamp implementation.

3.4 Effect of Clamping on Output Capacitance

Adding MOS clamps to the outputs of the amplifier increases the total capacitive load. Assuming $V_{out-} << 2.5V$, the following additional capacitive components will be present at output node V_{out-} when the clamp is turned on:

$C_{gdB} + C_{dbB} + C_{gsA} + C_{sbA}$

At V_{out+}:

$C_{gdD} + C_{dbD} + C_{gsC} + C_{sbC}$

Referring to Appendices A and B, and using bias points of $V_{db} = 2.5V, V_{sb} = 2.5V$, with sizing of $W = 2.2$, $L_{nmos} = .645$, and $L_{pmos} = .674$

$\triangle C_{load-} = 10.5fF$

$\triangle C_{load+} = 10.3fF$

$C_{load} = C_{load,unclamped} + \triangle C_{load} \approx 32fF$

The actual simulation transistors result in equal $\triangle C$ loads of 13.2fF, which slow down the circuit a little.

3.5 Discharge Current

Discharge current (the current going through the clamp) determines how quickly the clamp can minimize the difference in the outputs. When determining how long the clamp should be on, a model is helpful. It is possible to model the clamp as a resistor, but the value of the resistor changes so unpredictably that the model is only helpful for general trends or when focusing on an operating point.

At any given time the clamp is on, both devices are operating in the linear region, one with a fixed gate-source voltage, and one with a gate-source voltage that varies with the output voltage. If the output is greater than 2.5V (the voltage the clamp is referenced to), the N device has a fixed gate-source drive. If the output is less than 2.5V, it is the P device that has a fixed drive.

3.5.1 Resistance of the Clamp

If the $\frac{1}{2}V_{DS}^2$ term is dropped from the following linear region equation:

$I_D = \mu C_{ox}\frac{W}{L}[(V_{gs} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2]$

The fixed drive device can be modelled as a resistor of value

$R_C = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{gs}-V_t)}$.

Mobility μ is dependent on V_{ds}, such that the value of this R_{C1} decreases nonlinearly with V_{ds}.

The non-fixed drive device behaves according to the linear region equation noted for the fixed drive device, but the resistance of the non-fixed drive device increases nonlinearly with V_{DS}. This is because the net effect of the gate-source voltage decreasing outweighs the changing mobility.

The total clamp resistance is equal to the parallel combination of the resistances of the two devices.

3.5.2 Clamp Time Constant

Considering the clamp to be a variable valued resistor, the entire circuit can be approximated by the circuit shown in Figure 3-4.

The following equation shows the transient response:

$V_{out} = V_{in}(\frac{R_L}{R_C+R_L})(1 - e^{\frac{-t(1/R_C+1/R_L)}{C_L}})$

Simulation C shows the change in outputs in response to the clamp turning on. Within the first 2ns the clamp is on, the outputs are drawn from a full differential output to within 0.3V of each other. After that, the clamping dramatically slows down. The clamp transient response equation is difficult to match up to the simulations and of questionable value. Nonetheless, the resistive modeling aspect of the transient equation (the final dc response) is important to note.

The equation does reveal that because the load is not purely capacitive, the final value due to clamping alone is not equal to the reference voltage, but a large fraction of it. It is also important to recognize what an input drive does to the output voltage. Such an input drive could be due to mismatch within the circuit or to an actual signal

at the input of the amplifier. For the model shown in Figure 3-5, where $\triangle i = g_{m1} V_{in}$, the final value output voltage is

$V_{out} = \triangle i R_C + V_{in}$,

assuming $R_L >> R_C$

Simulation D illustrates this effect. Though the clamp turns on at 42ns, 0.5V is maintained across the outputs until the drive on the input is removed. The input is removed at 45ns, at which point the differential voltage starts to decay.

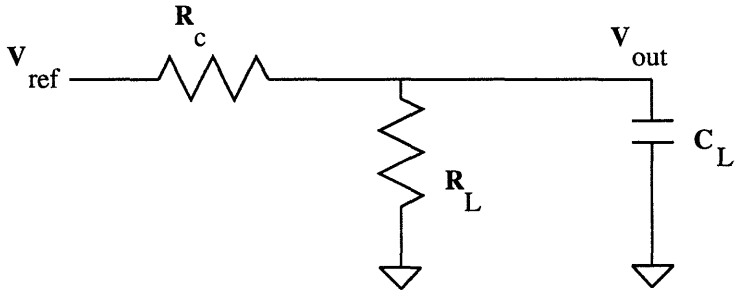


Figure 3-4: Clamping Circuit Representation

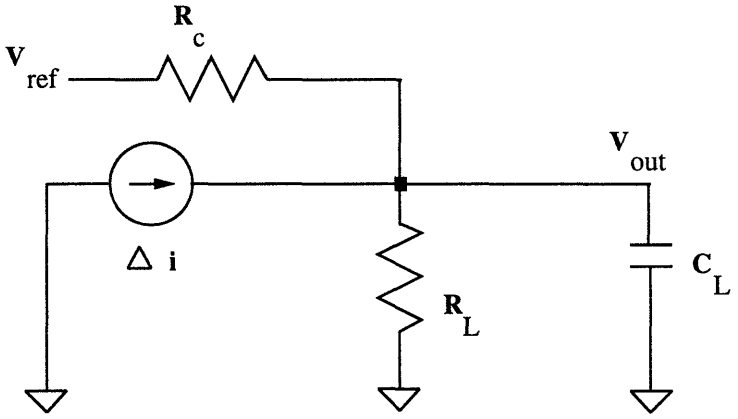


Figure 3-5: Clamping Circuit Representation with Differential Drive

3.6 Clock Feedthrough

The output voltages are directly affected by the clock transitions via coupling to the clock, or feedthrough, as shown in Figure 3-6. The complementary devices partially cancel each other out, but not entirely; complete cancellation can never be depended on because process variations inevitably create some mismatch among coupling capacitors.

If the output voltage is less than 2.5V, then the NMOS device will couple to the output via C_{gs} and the PMOS device will couple to the output via C_{gd}. For the clamp sizing shown in Figure 3-2, $C_{gsA} = 2.46fF$ and $C_{gdB} = 1.83fF$. The following equation characterizes the coupling effect:

$$V_{out-} = \frac{V_{ckn}C_{gd}}{C_{gd}+C_{load}} + \frac{V_{ck}C_{gs}}{C_{gs}+C_{load}} = 98mV$$

For V_{out+}, which has slightly different loading conditions, the net clock coupling results in approximately 84mV. Thus the differential coupling effect comes to about 14mV.

Simulation C shows both outputs after being clamped for 20ns. No new input is applied after an MSB input the cycle before. Both outputs drop by approximately 110mV, on the order of the predicted 98mV and 84mV. In the waveform at the bottom of the page in Simulation E, it is possible to see the differential coupling effect when the clamp is released at 54ns. With no new input, the differential output jumps approximately 12mV when the clamp is released and can be seen to decay thereafter.

Simulation F shows a close-up of what happens when the outputs do not reach the reference voltage. The PMOS and NMOS gate-to-drain and source-to-drain capacitances are not as well matched and the common mode coupling doesn't cancel as well as in Simulation E, resulting in a common mode output drop of 0.35V. It can be inferred that if the two output voltages are not close to each other they will not couple uniformly, which could result in a large differential voltage change. Clamp input timing is important in preventing such a situation.

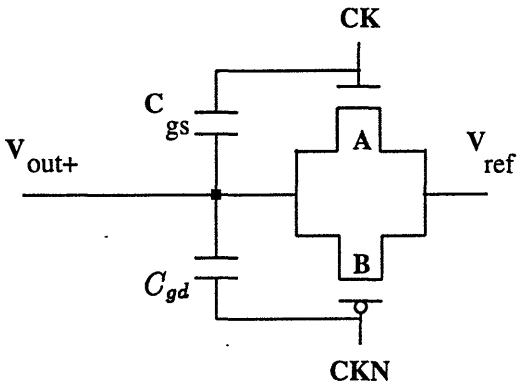


Figure 3-6: Clock Feedthrough Circuit

3.7 Clamp and Input Timing

The only major input timing constraint is that the last output be removed before the clamp turns on or very soon after it turns on. This is crucial for the case of a large input followed by a small input of the opposite polarity, as is evident from Simulation D. The large input prevents the outputs from getting close to each other. If the differential output is not lowered before the clamp ends, an LSB of the opposite polarity will not be strong enough to discharge the outputs quickly.

Introducing the new input while the clamp was still on yielded the lowest time from input turning on to output reaching the latch offset voltage. This time, shown in Simulation B was 7.5 ns. The input was applied for 2.5ns before the clamp was released. It took 5ns to reach the valid latch voltage after that. When the new input was not turned on until after the clamp was off, the time delay was approximately 1ns longer to reach a valid output.

3.8 Clamp Sizing

Both the P and N clamping devices need to be sized equally so that clock feedthrough will be minimized. Larger $\frac{W}{L}$ ratios decrease the clamp resistance, but increase the capacitive loading. Whether increasing the clamp size has a positive or negative effect on the speed of the circuit depends on the SPICE parameters and the default layout parameters. For the SPICE model used in this thesis, increasing the clamp size was not effective. Doubling the clamp width to 4.4 μm resulted in a 3 ns increase in the time for the outputs to reach 50mV.

Chapter 4

Autozeroing

4.1 Introduction

Autozeroing, or autobalancing, is the cancelling of any dc offset on the output nodes, such that the input referred offset is very small. There are two basic approaches that can be taken to cancel these offsets. One is to feedback via a switched capacitor network a fraction of the output such that each output is compensated independently, but with respect to the same fixed voltage. Another technique is to cancel the common mode and differential mode with two separate feedback loops. The former approach was chosen because it allowed for hysteresis and non-correlation between the two legs of the cascode, without the need for aggressive sizing techniques.

4.2 Approach

4.2.1 Background

Figure 4-1 shows the basic feedback concept, consisting of a switched capacitor low pass filter and a single ended differential amplifier for each output. If process inaccuracies cause an output to be too high, a high voltage is fed back to the parallel feedback device, causing its resistance to drop and thus the output voltage to drop also. The single ended differential amplifier, consisting of devices M16-M20, is refer-

enced to 2.5V; and its equilibrium output is centered at 2.5V. The nominal feedback voltage to M9A and M10A is centered at 2.5V to produce the nominal folded cascode output of 2.5V. The actual feedback circuit implementation is shown in Schematic C.

4.2.2 Referred Input Offset

To avoid large output swings due to the feedback circuitry, the change in output voltage due to the maximum possible change in feedback voltage per cycle must be limited to much less than the change in output due to an LSB.

The gain from $V_{g,M9A}$ to V_{out-} is, based on the same calculation methods used for the folded cascode gain equation in Chapter 2:

$\frac{V_out-}{V_{g,M9A}} = \frac{-g_{m9A}}{g_{in}g_{o5}/g_{m5}+g_{o7}g_{o9}/g_{m7}} = 13$, as measured in simulation.

To prevent the output from switching too rapidly, C_{L2} and C_{R2} are each 10pF, to be implemented with depletion NMOS devices. C_{L1} and C_{R1} are each approximately 4.4fF. With these capacitance values, the maximum feedback voltage swing is $\frac{4VC_{L1}}{C_{L2}+C_{L1}} = 1.8mV$. Amplified by the feedback gain, this results in a maximum voltage change of 21mV. A 21mV change referred back to the input of the amplifier corresponds to an input of $24\mu V$, less than one twentieth of an LSB .

The feedback is powerful enough to compensate for large input offsets, but not in one cycle. The scaling down of the feedback capacitors makes the system stable and allows the feedback to work slowly over several cycles.

4.3 Simulation Results

4.3.1 Normal Operation

Simulation G shows the autozeroing circuitry functioning with no mismatch and a default initial condition on V_{g9A} and V_{g10A} of $2.5V$. The key waveform in the Simulation is V_{out-}, the fourth waveform from the top of the page. It gradually settles to the nominal 2.5V. The intermediate waveforms are shown above V_{out-} and can be examined more closely by referring to the node names shown in Schematic C,

if desired. The bottom two waveforms show the two stage feedback clocking. The nominal overal period was set at 40ns, though in an actual 12-bit implementation, the total period would be longer because the autozeroing would only occur once per overall ADC timing cycle.

4.3.2 Mismatch Operation

To verify the effectiveness of the autozeroing, various simulations were run with sensitive gate lengths changed. The success of the autozeroing circuitry depended heavily on how the feedback timing related to the clamp timing. Simulation H shows the result when both input devices have a nominal gate lenght of 0.85 μm instead of $0.8\mu m$. The format of the Simulation H plot is just like that of Simulation G. The autozeroing circuitry eventually centers the output around 2.5V.

4.4 Autozeroing Summary

The autozeroing circuitry was pursued to determine if there existed a fundamental problem associated with autozeroing a high gain clamped stage. While no inherent problem was found, it is important to note that this particular autozeroing scheme is not crucial to the clamp's operation, and hasn't been optimized to work with the clamping. Autozeroing issues not discussed at length here include the time constant of the feedback, its interaction with the clamping of the amplifier, and potential feedthrough-related problems.

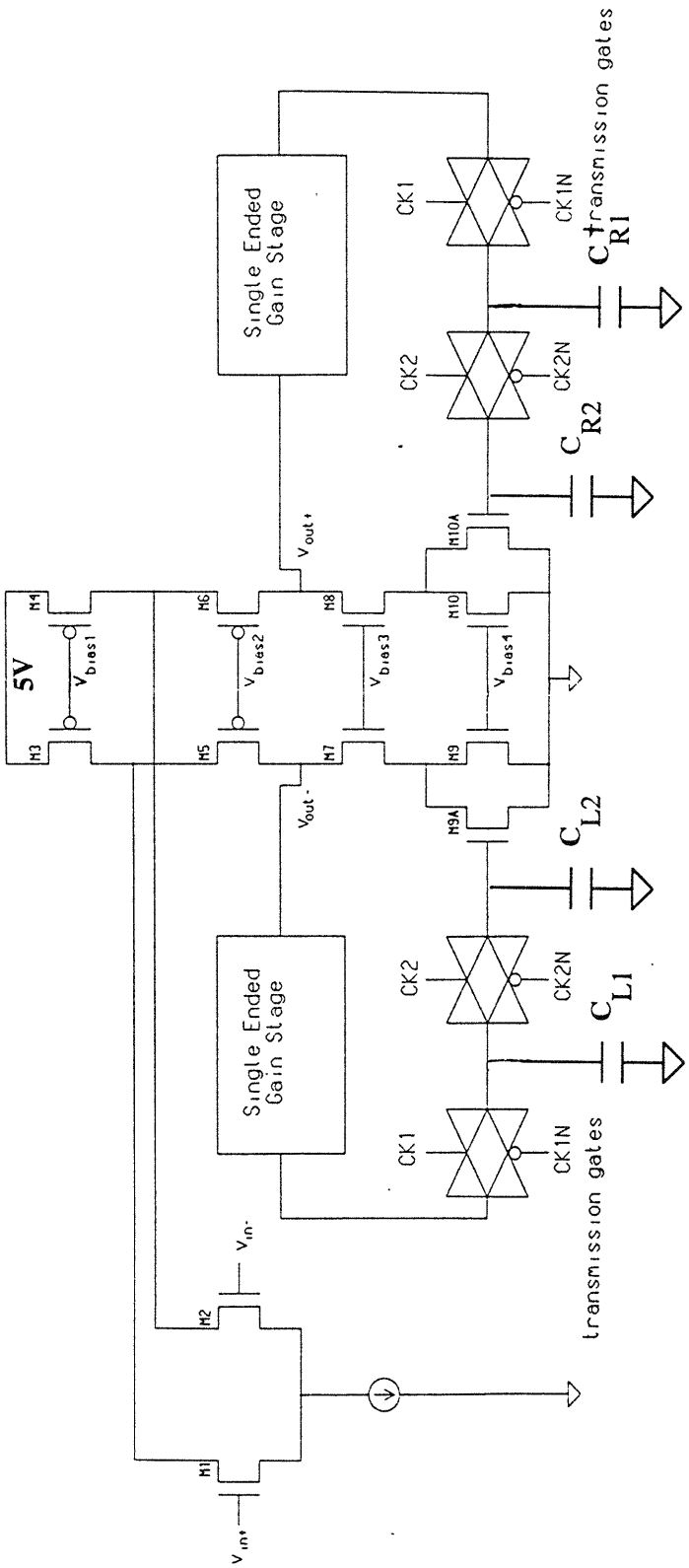


Figure 4-1: Autozeroing Technique

Chapter 5

Comparison and Conclusions

5.1 Review

The goal of this project was not to produce the fastest 12 bit ADC possible, but to push the limits of affordable, low-power technology by speeding up one of the critical paths in high bit-accuracy ADC's. The amplifier itself consumes 2.5mW of power (not counting auto-zeroing circuitry), and the rest of the ADC circuitry would consume an estimated 300mW, based on present Sarnoff designs. When compared to amplifiers of this power and technology (CMOS), the clamped folded cascode outperforms them all. However, before making a comparison, it is necessary to relate the clamped time response to the worst case series of inputs to the potential sampling rate of the ADC in which the amplifier will be implemented.

5.2 Impact of Improved Overdrive Recovery Time on Sampling Rate

As mentioned in chapter one, a pipelined SSA ADC has a fundamental internal clocking frequency that may also be the sampling rate. While the total period of the multiple phase clock depends on the autozeroing and error correction schemes, the fundamental period is foremost limited by the comparison time, and the delay around

the decoding and subsequent digital-to-analog(DA) conversion for the next cycle comparison. It would be difficult to run the internal clock any faster than the frequency limit of the comparator-DA loop because the loading of so many comparators on the voltage reference lines would become unmanageable. This means that the overdrive recovery time can directly limit the sampling rate of a high bit accuracy ADC. For a different Sarnoff ADC implemented in $1\mu m$ CMOS, the delay from the output of the latch to a new valid comparator input is approximately 12ns. With the $0.8\mu m$ technology simulated in this thesis, that time would probably reduce to 10ns without any major topology changes. Thus, the fundamental period limit for the simulated amplifier would be 17.5ns, based on a worst case delay of 7.5ns from valid amplifier input to valid latch input plus a delay of 10ns from latching to valid DAC output. This converts to an admirable 57MHz sampling rate limit.

5.3 Comparison to Multistage Amplifier

The single stage clamped folded cascode beat an existing 12-bit Sarnoff ADC amplifier under worst case input voltage conditions by approximately 5ns. This two stage clamped amplifier was implemented in $1\mu m$ CMOS and was clocked (the whole ADC) at a maximum sampling rate of 40MHz. The multistage amplifier drew 4mW of power, more than the clamped folded cascode.

The multistage amplifier, though used for a 12-bit ADC with a 2V input swing, only had to sense a minimum input voltage of 1mV, not the 0.49mV the folded cascode was tested at, because of clever input circuitry and amplification prior to the signal's entrance to the comparator. If the clamped folded cascode only needed to sense 2LSB, it could potentially be clocked at 67MHz. However, this would not include much margin for error, just as the 40 MHz sampling rate is pushing the limits of the multistage Sarnoff comparator. It is safe to say that with similar input amplification circuitry, the clamped folded cascode could effectively and reliably perform at 60MHz.

Razavi and Wooley [13] report a 12-bit 5-Msample/s converter implemented in $1\mu m$ CMOS, based on a two-step flash architecture. They too employ clamping, but

require 100ns for input sampling, and an additional 100ns for subsequent conversion. The total power dissipated in both the coarse and fine comparators is 2.25mW, and the overall ADC power consumption is 200mW. While this amplifier consumes slightly less power than the clamped folded cascode, it suffers an order of magnitude decrease in sampling rate limit.

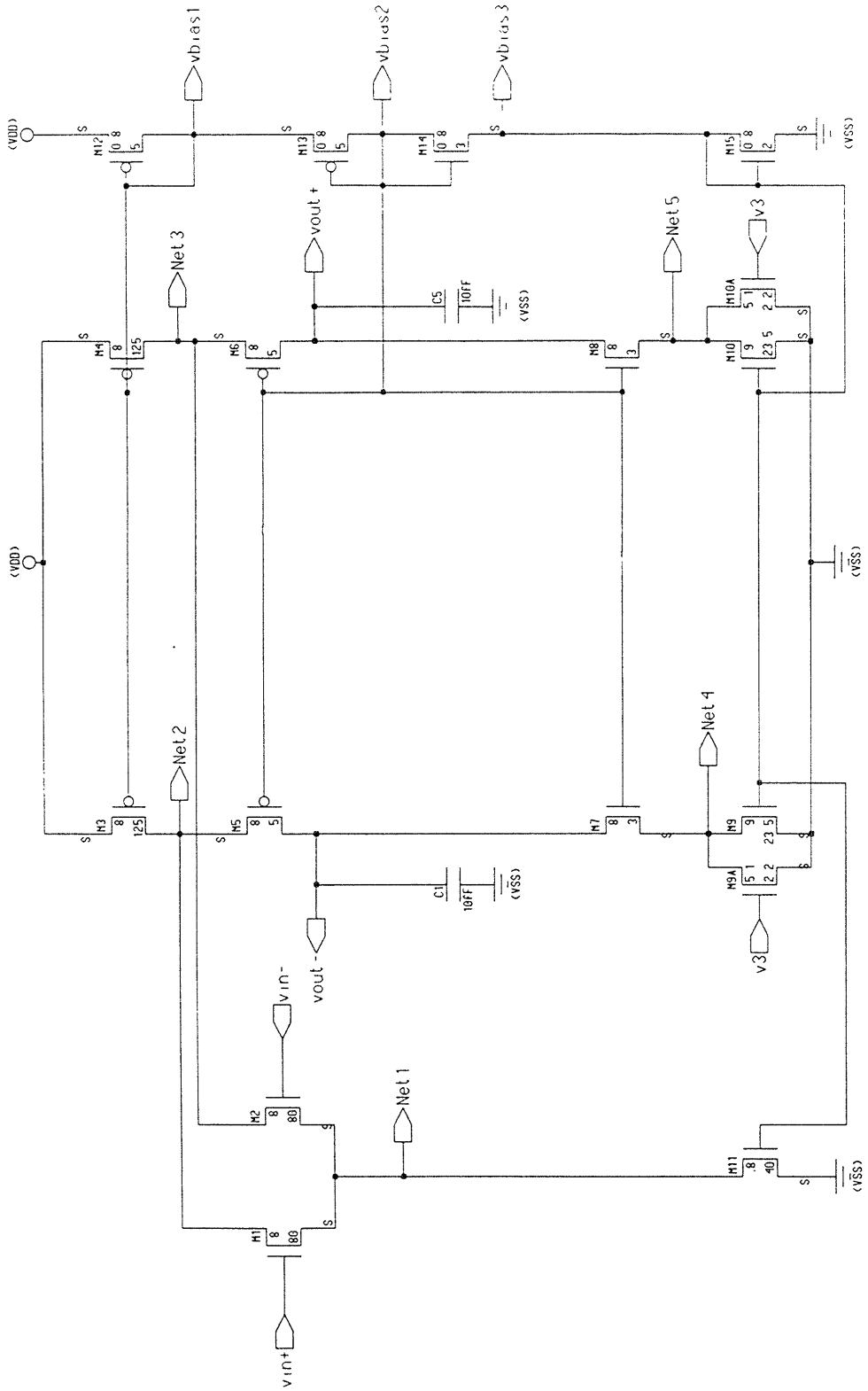
The main delay due to comparison time occurs in the fine comparator, which is a combined amplifier and latch within a folded cascode topology. While some of the sampling rate limit is due to DAC conversion time and logic, a large part of the delay could be elimated if the fine comparator were a clamped amplifier and separate latch.

5.4 Conclusion: Single Stage Versus Multistage Comparators

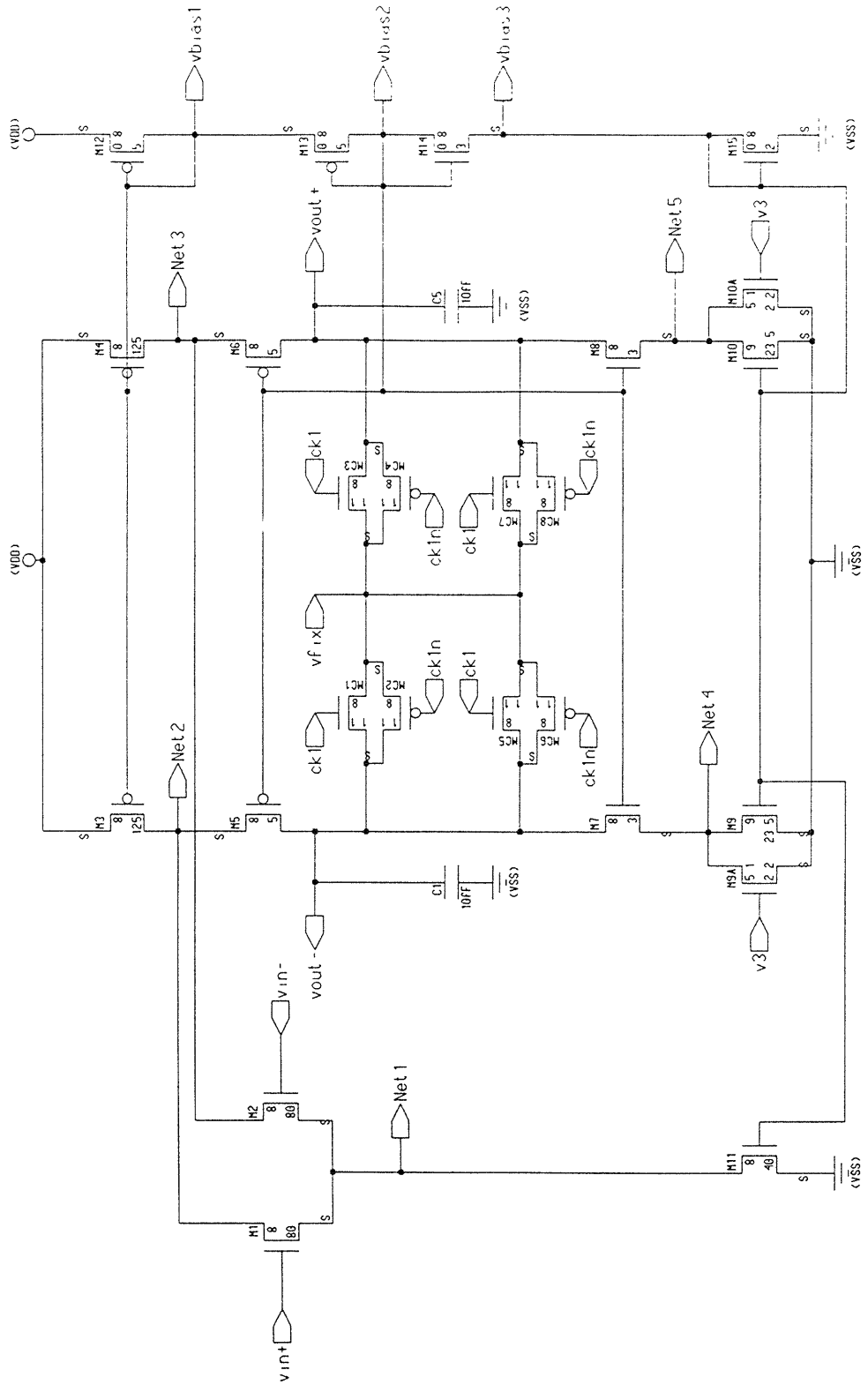
Multiple stage unclamped gain stages outperform single stage high gain amplifiers without clamping. This statement is supported theoretically in the standard derivation of the optimal gain per stage of e, as outlined in [4], as well as supported by the reported performance of unclamped multiple stage amplifiers at Sarnoff compared to the unclamped folded cascode. However, it has been shown in this thesis that a clamped single stage high gain amplifier can outperform a clamped multiple stage amplifier. The nonlinearities of clamping and the extra loading due to the actual clamps decrease the potential sampling rate as more stages are added.

The success of the clamped folded cascode amplifier does not have to stop at a 12 bit application. The folded cascode topology has enough gain potential to perform superbly for a 14 bit design as well.

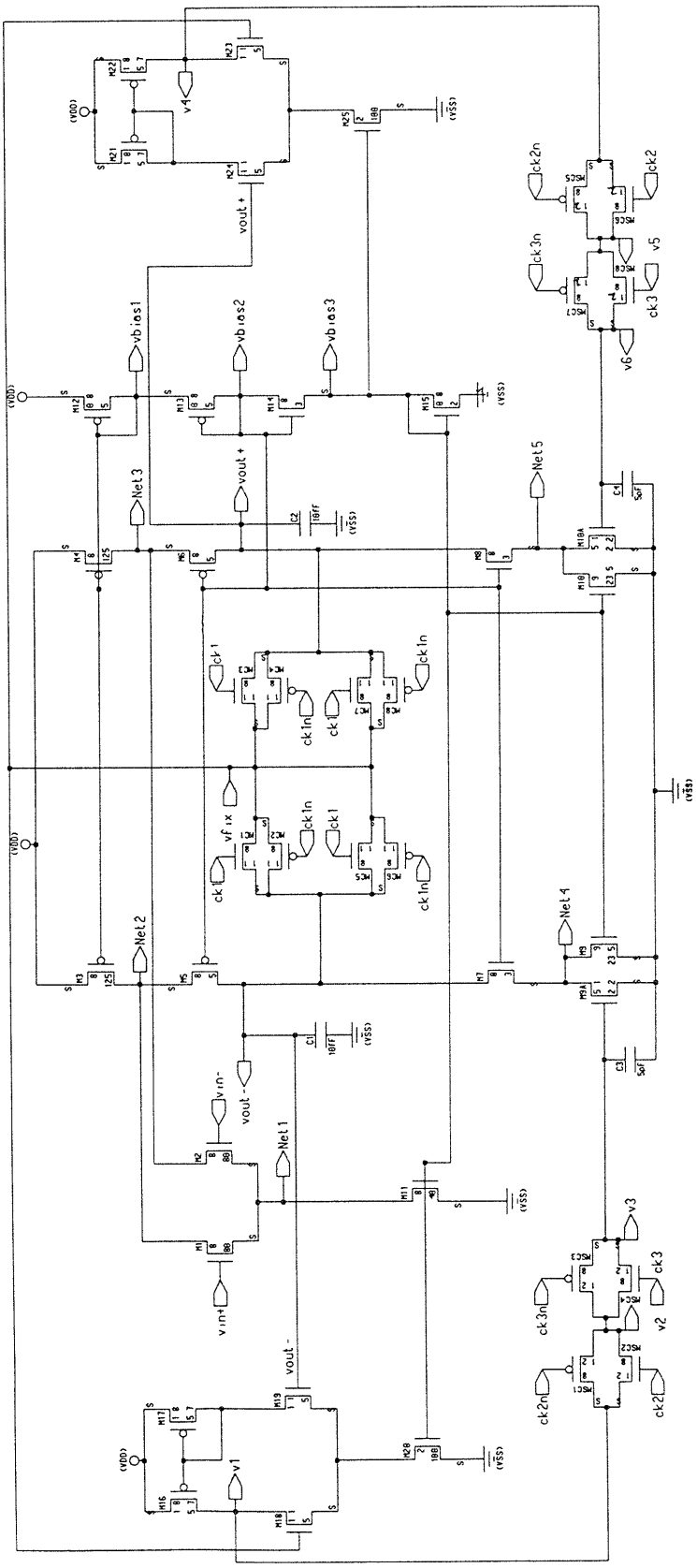
Schematics



Schematic A: Unclamped Folded Cascode Amplifier

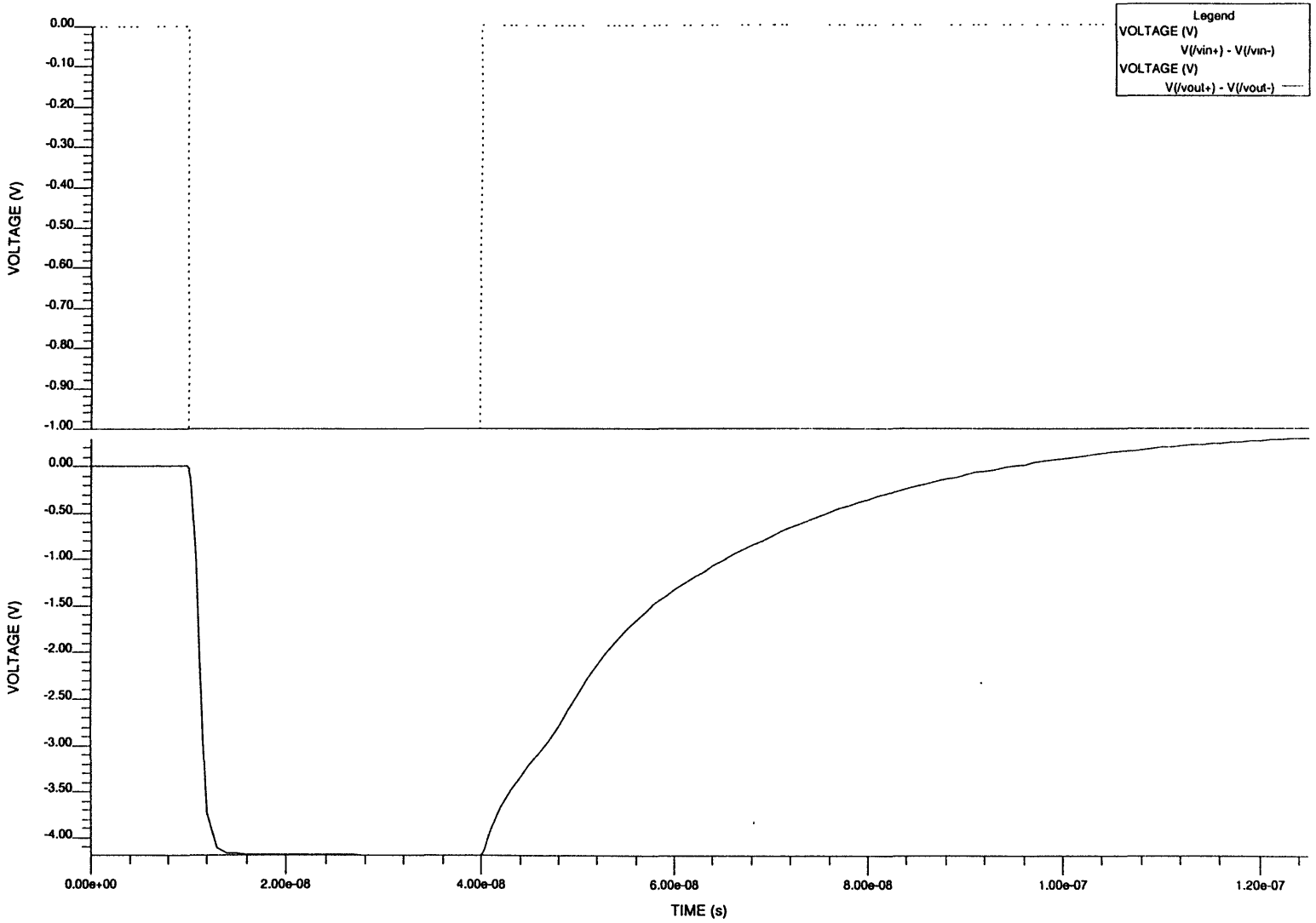


Schematic B: Clamped Folded Cascode Amplifier

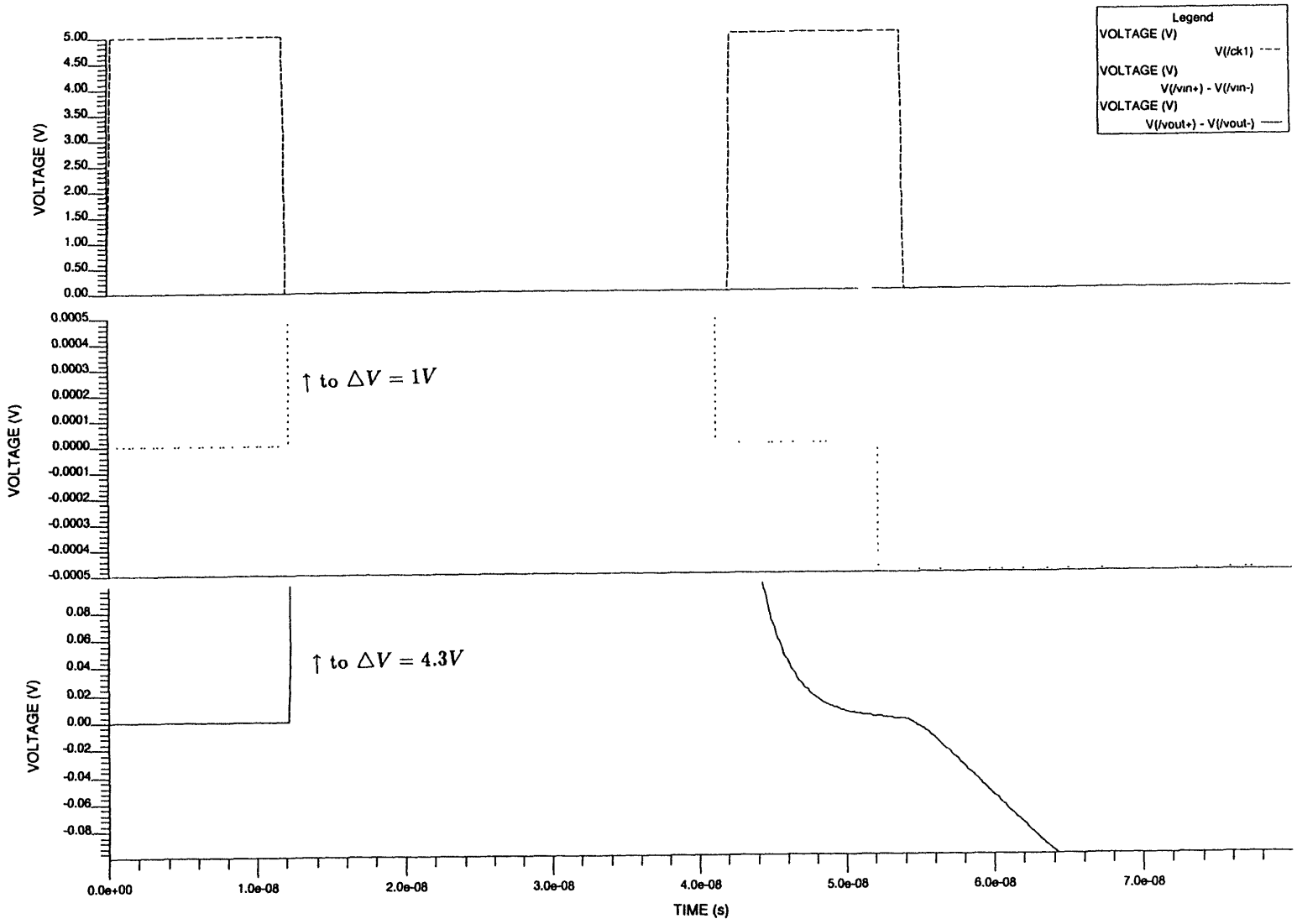


Schematic C: Autozeroed, Clamped Folded Cascode Amplifier

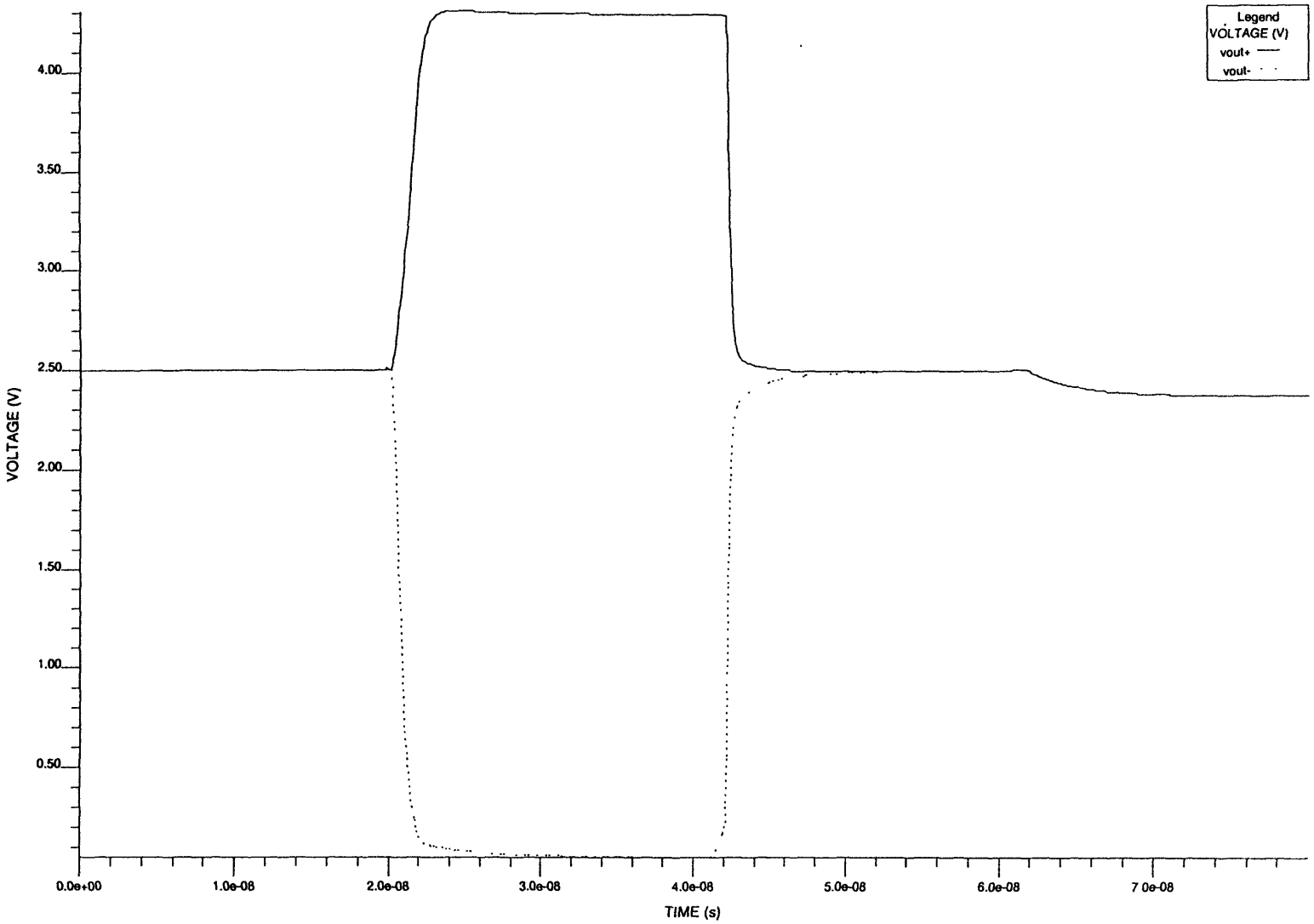
Simulations



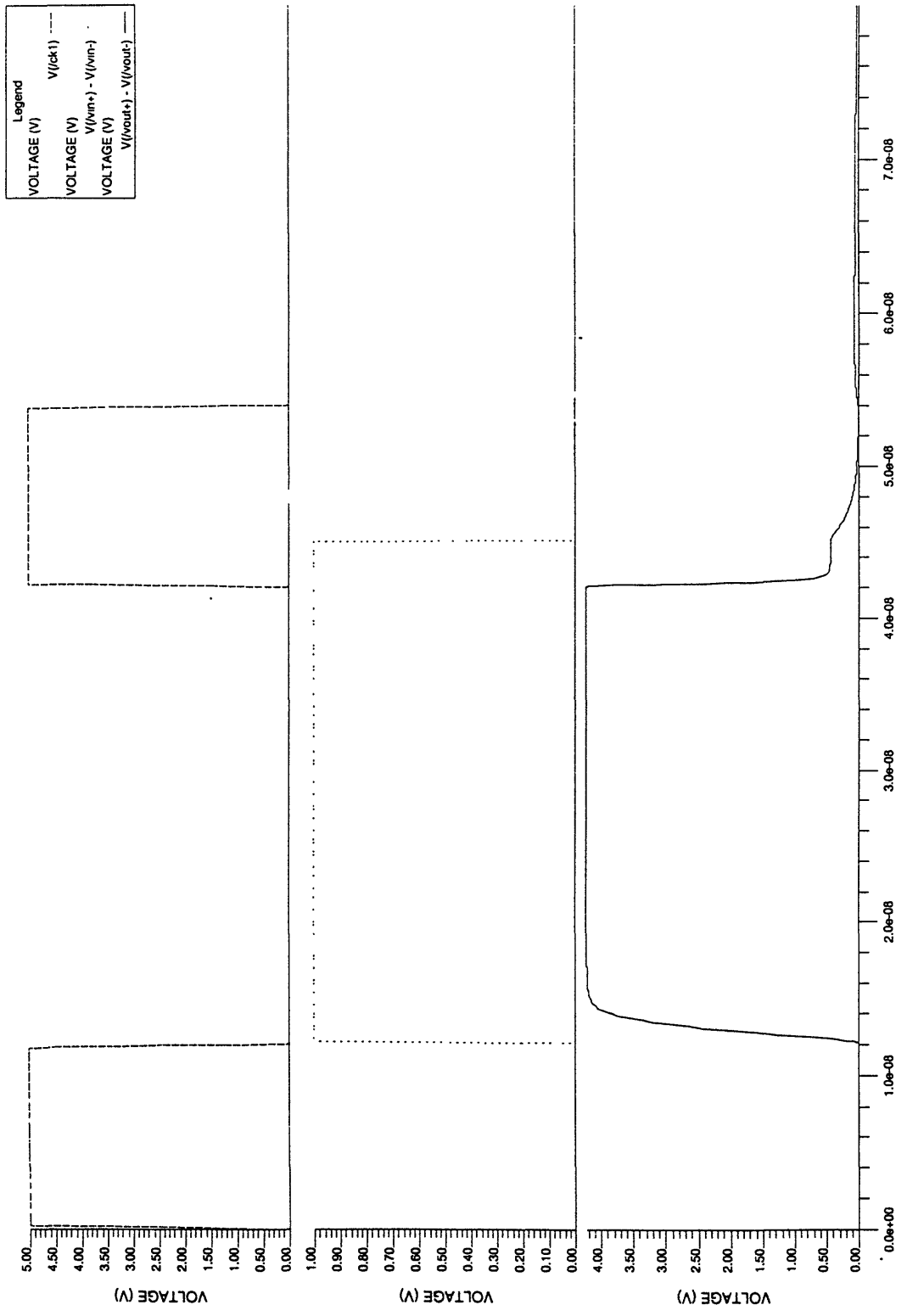
Simulation A: Unclamped Folded Cascode Transient



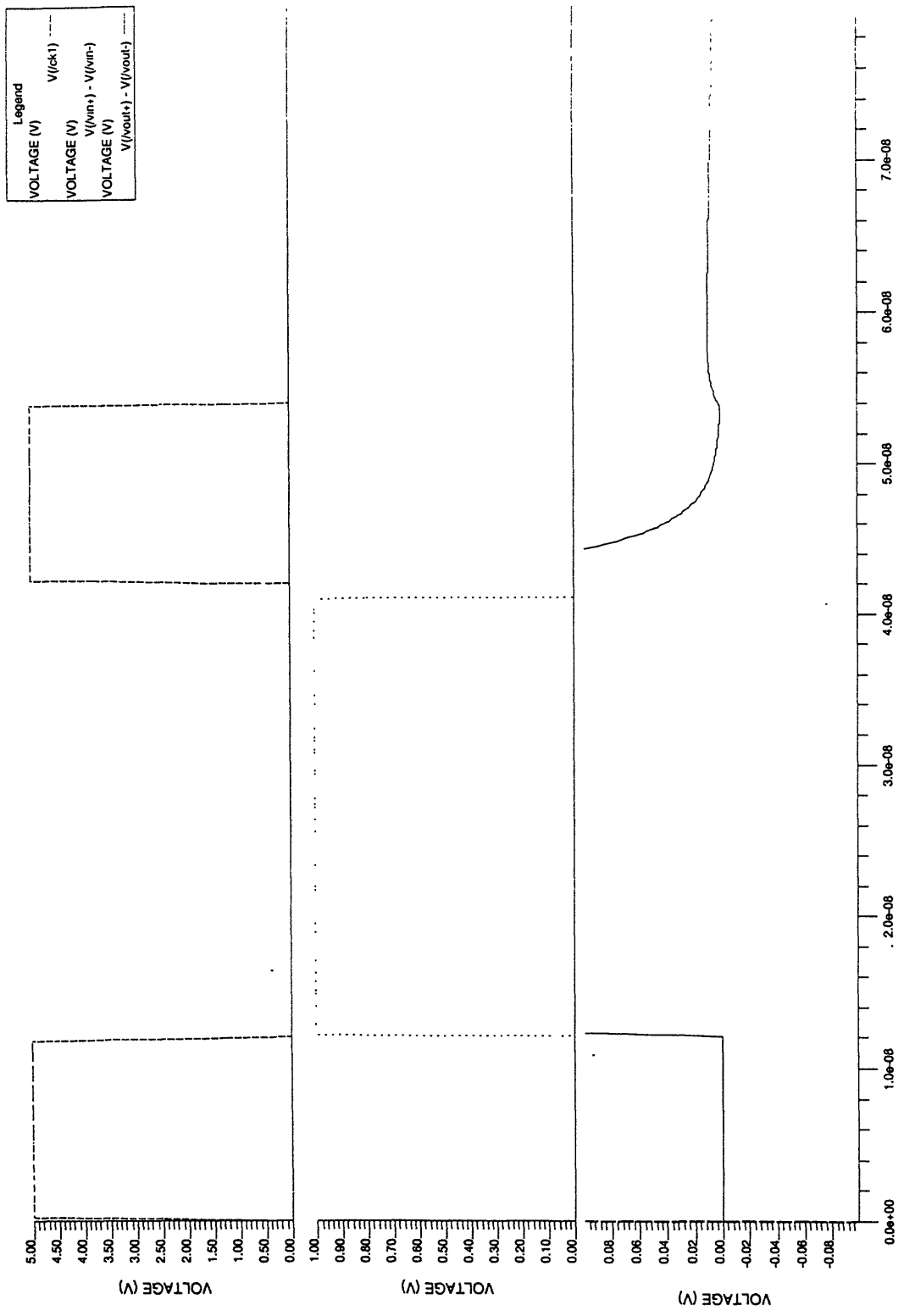
Simulation B: Clamped Folded Cascode Transient



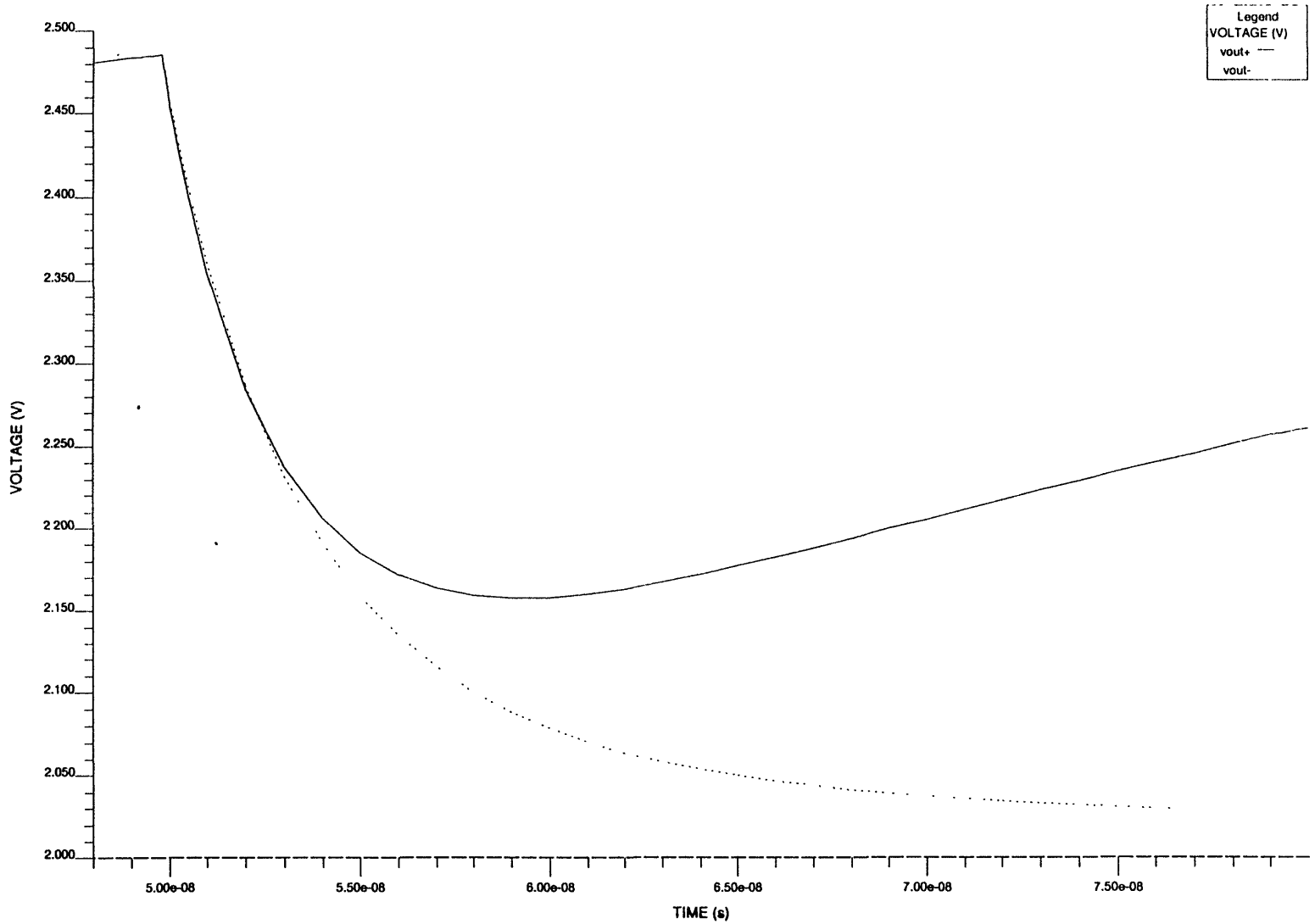
Simulation C: Clamping Time Constant



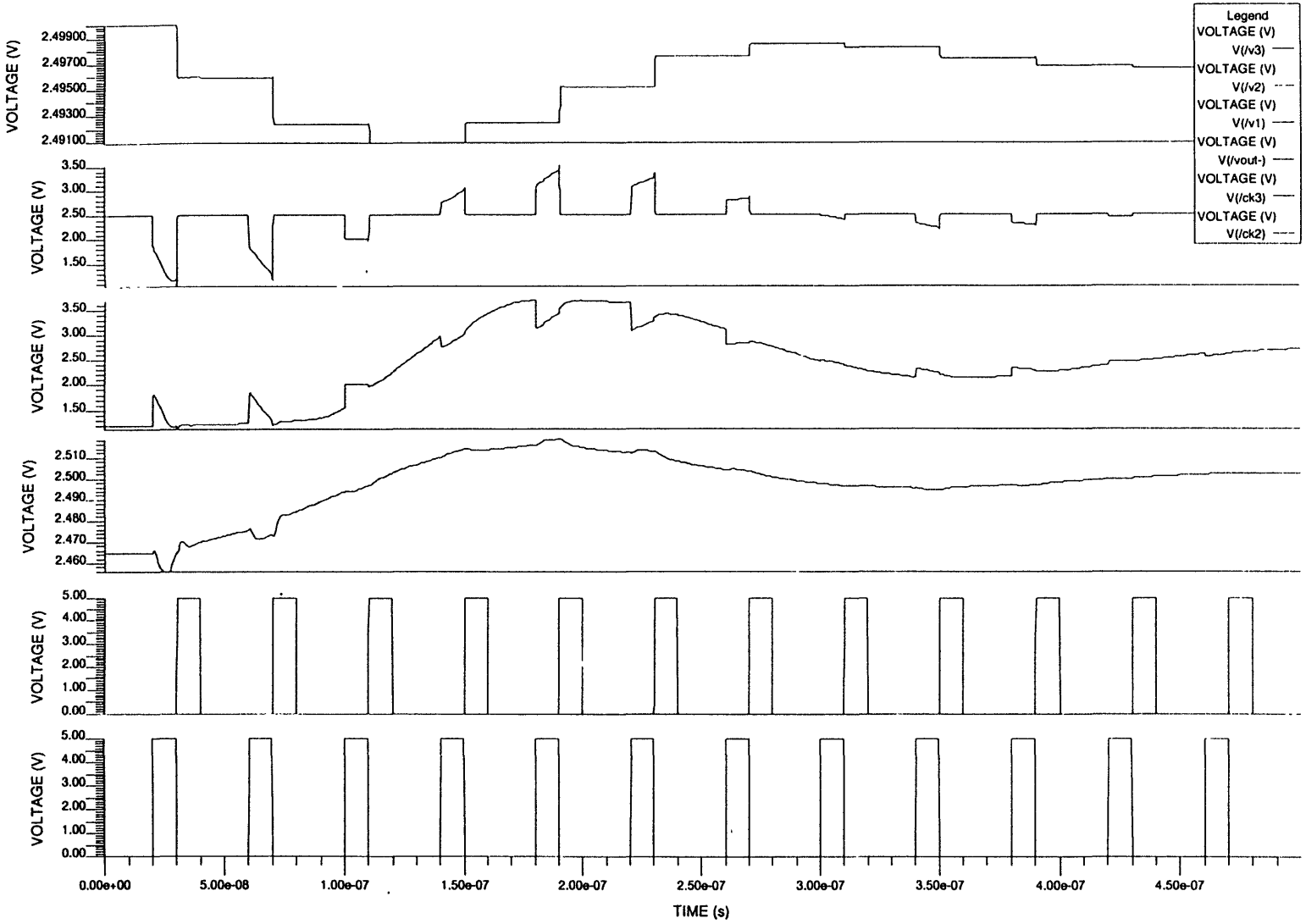
Simulation D: Effect of Input Timing on Output



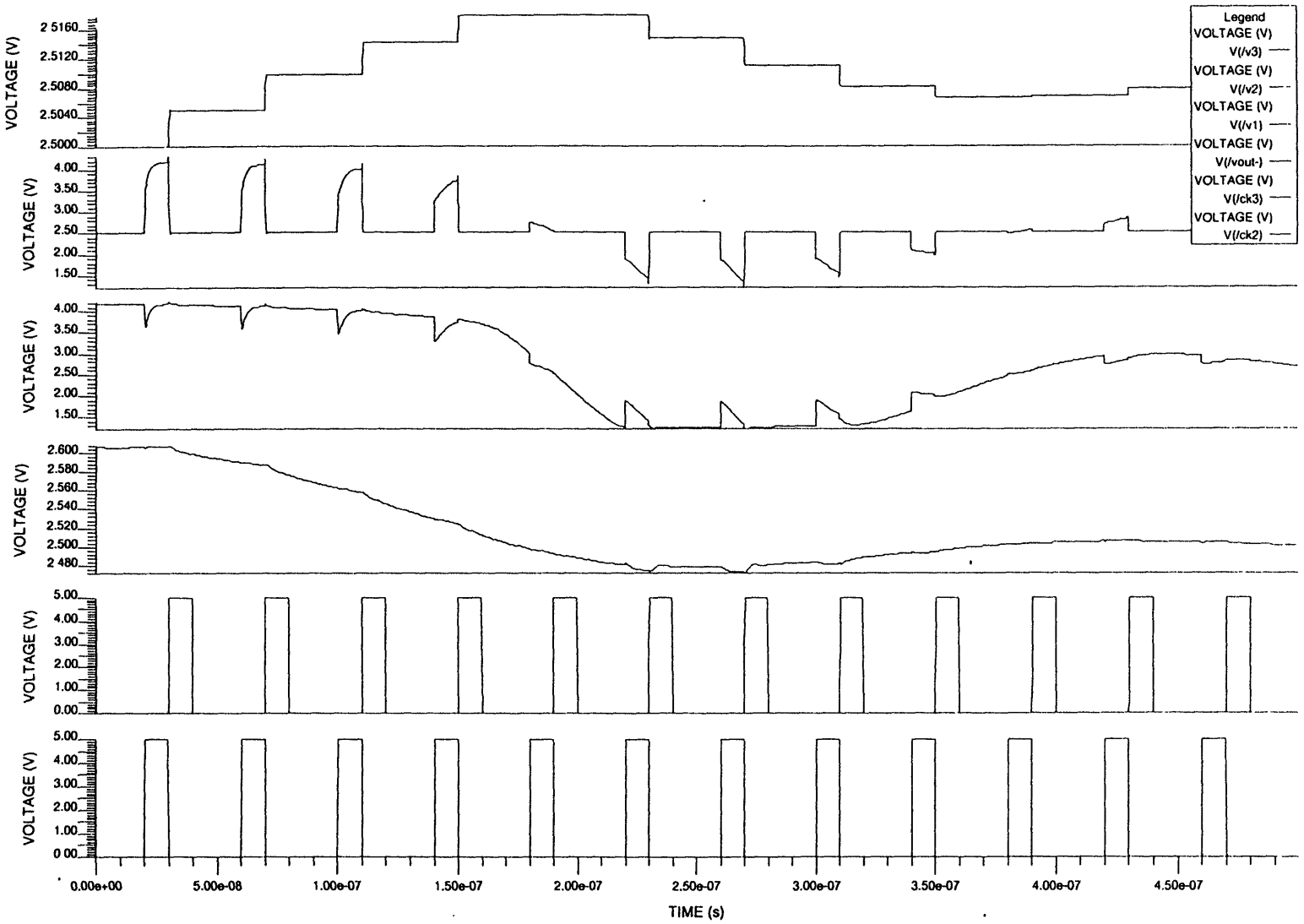
Simulation E: Differential Clock Feedthrough



Simulation F: Pronounced Clock Feedthrough



Simulation G: Autozero Functioning without Mismatch



Simulation H: Autozero Functioning with Mismatch

Appendix A: SPICE Modelfile

SPICE MODELFILE

```
* NMOS L=0.8uM
* PMOS L=0.8uM


.MODEL NE NMOS(LEVEL=3 VTO=0.7821 TOX=1.75E-8 RSH=62.5
+  NSUB=4.0121E+16 LD=7.7667E-08 UO=480.0
+ VMAX=1.3625E+05 THETA=3.9505E-02 ETA=9.9859E-03 KAPPA=0.1094
+  TPG=1 DELTA=0.7667
+ CGSO=4.740E-10 CGDO=1.561E-10 CJ=2.4E-4  CJSW=4.9E-10
+ MJ= 0.44 MJSW=0.35  )


.MODEL PE PMOS(LEVEL=3 VTO=-0.9247 TOX=1.7500E-08 RSH=138
+  NSUB=4.0116E+15 LD=6.3184E-08 UO=153.4
+ VMAX=1.5801E+05 THETA=8.2588E-02 ETA=3.1827E-03 KAPPA=1.952
+  TPG=-1 DELTA=0.5856
+ CGSO=3.718E-10 CGDO=1.6865E-10 CJ=7.1E-4  CJSW=1.87E-10
+ MJ= 0.55 MJSW=0.38 )
```

Appendix B: SPICE Parameter Explanation

References [5], [1], and [6] contain the equations found in the appendix and can be referred to for further clarification. Variables are listed roughly according to their order of appearance in the text.

$\mu_o(\frac{cm^2}{V \cdot s})$: Channel Mobility

$$\mu_{eff} = \frac{\mu_s}{1+(\mu_s V_{ds})/(V_{max} L_{eff})}$$
$$\mu_s = \frac{\mu_o}{1+\theta(V_{gs}-V_{TH})}$$

Nominal value is given as UO in SPICE model.

$C_{ox}(\frac{pF}{\mu m^2})$: Gate oxide capacitance

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

Oxide thickness t_{ox} is TOX in SPICE. ϵ_{ox} is for silicon.

$W(\mu m)$: Channel Width

Nominal channel width is the same as the actual channel width, to a first order approximation.

$L(\mu m)$: Channel Length

$$L = L_{nom} - 2L_d$$

On Schematics, the L shown is the nominal gate length. In all equations, L refers to the effective gate length. Length L_d (LD in SPICE) is the overlap due to diffusion on both the drain and source sides of the device.

$V_t(V)$: Threshold Voltage

Nominal value is VTO in SPICE modelfile. The actual threshold varies with doping and terminal voltages.

$\lambda(V^{-1})$: Channel Length Modulation

Difficult to calculate; depends on device current and gate length.

$C_{gs}(fF)$: Gate-to-Source Capacitance

In Saturation and Cutoff Regions: $C_{gs} = \frac{2}{3}WLC_{ox} + CGSO \cdot W$
In Linear Region: $C_{gs} = CGSO \cdot W + \frac{1}{2}WLC_{ox}$

The units for the SPICE gate-to-source overlap capacitance CGSO are $\frac{fF}{\mu m^2}$.

$C_{gd}(fF)$: Gate-to-Drain Capacitance

In Saturation and Cutoff Regions: $C_{gd} = CGDO \cdot W$
In Linear Region: $C_{gd} = CGDO \cdot W + \frac{1}{2}WLC_{ox}$

The units for the SPICE gate-to-drain overlap capacitance CGDO are $\frac{fF}{\mu m^2}$.

$C_{sb}(fF)$: Source-to-Bulk Capacitance

Under Zero Bias Conditions: $C_{sbo} = CJSW \cdot (W + 2L_{sd}) + CJ \cdot (WL_{sd})$
Biased Conditions: $C_{sb} = \frac{C_{sbo}}{\sqrt{(1+V_{sb}/\psi)}}$

The SPICE sidewall capacitance CJSW is in units of $fF/\mu m$. The SPICE bottom junction capacitance is in units of $fF/\mu m^2$. Length L_{sd} represents the source diffusion extension beyond the transistor gate. The default SPICE value for ψ is 0.5V.

$C_{db}(fF)$: Drain-to-Bulk Capacitance

Under Zero Bias Conditions: $C_{dbo} = CJSW \cdot (W + 2L_{dd}) + CJ \cdot (WL_{dd})$
Biased Conditions: $C_{db} = \frac{C_{dbo}}{\sqrt{(1+V_{db}/\psi)}}$

Length L_{dd} represents the drain diffusion extension beyond the transistor gate.

$C_{gb}(fF)$: Gate-to-Bulk Capacitance

The gate-to-bulk capacitance depends on the extension of the gate area beyond the active channel region, CJSW, and CJ. Area and perimeter values are smaller than for C_{sb} and C_{db} so this capcitance was left out of theoretical calculations.

$g_{mb}(mS)$: Back-gate Transconductance

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f + V_{sb}}} g_m$$
$$\gamma = \frac{1}{C_{ox}} \sqrt{2q\epsilon N_S}$$

The backgate transconductance was ignored for all calculations. The error it introduced was on the order of 2.5 percent. Substrate doping N_S is represented in SPICE by NSUB and measured in units of atoms/cm^2. For silicon, ϵ = 1.04e-12F/m. Charge q = 1.6e-19C.

Appendix C: DC Operating Point

Line	Net/Pin	Voltage/Current
0	//GND:v	0
1	//VDD:v	5
2	/C1/NEG:i	0
3	/C1/POS:i	0
4	/C2/NEG:i	0
5	/C2/POS:i	0
6	/C3/NEG:i	0
7	/C3/POS:i	0
8	/C4/NEG:i	0
9	/C4/POS:i	0
10	/ck1:v	0
11	/ck1n:v	5
12	/ck2:v	0
13	/ck2n:v	5
14	/ck3:v	0
15	/ck3n:v	5
16	/M1/E0:i	0
17	/M1/MN/B:i	-5.534e-12
18	/M1/MN/D:i	0.000111
19	/M1/MN/G:i	0
20	/M1/MN/S:i	-0.000111
21	/M1/T0:i	-0.000111
22	/M1/T1:i	0.000111
23	/M10/E0:i	0
24	/M10/MN/B:i	-4.842e-13
25	/M10/MN/D:i	0.000108
26	/M10/MN/G:i	0
27	/M10/MN/S:i	-0.000108
28	/M10/T0:i	-0.000108
29	/M10/T1:i	0.000108
30	/M10A/E0:i	0
31	/M10A/MN/B:i	-4.848e-13
32	/M10A/MN/D:i	2.528e-05
33	/M10A/MN/G:i	0
34	/M10A/MN/S:i	-2.528e-05
35	/M10A/T0:i	-2.528e-05
36	/M10A/T1:i	2.528e-05
37	/M11/E0:i	0
38	/M11/MN/B:i	-8.953e-13
39	/M11/MN/D:i	0.0002218
40	/M11/MN/G:i	0
41	/M11/MN/S:i	-0.0002218
42	/M11/T0:i	-0.0002218
43	/M11/T1:i	0.0002218
44	/M12/MP/B:i	1.248e-12
45	/M12/MP/D:i	-9.639e-06
46	/M12/MP/G:i	0
47	/M12/MP/S:i	9.639e-06
48	/M12/P0:i	0
49	/M12/T0:i	9.639e-06
50	/M12/T1:i	-9.639e-06
51	/M13/MP/B:i	3.846e-12
52	/M13/MP/D:i	-9.639e-06
53	/M13/MP/G:i	0
54	/M13/MP/S:i	9.639e-06

```
 55 /M13/P0:i                          0
 56 /M13/T0:i                   9.639e-06
 57 /M13/T1:i                  -9.639e-06
 58 /M14/E0:i                          0
 59 /M14/MN/B:i                -3.522e-12
 60 /M14/MN/D:i                 9.638e-06
 61 /M14/MN/G:i                        0
 62 /M14/MN/S:i                -9.638e-06
 63 /M14/T0:i                  -9.638e-06
 64 /M14/T1:i                   9.638e-06
 65 /M15/E0:i                          0
 66 /M15/MN/B:i                -1.101e-12
 67 /M15/MN/D:i                 9.639e-06
 68 /M15/MN/G:i                        0
 69 /M15/MN/S:i                -9.639e-06
 70 /M15/T0:i                  -9.639e-06
 71 /M15/T1:i                   9.639e-06
 72 /M16/MP/B:i                 3.067e-12
 73 /M16/MP/D:i                 -9.82e-05
 74 /M16/MP/G:i                        0
 75 /M16/MP/S:i                  9.82e-05
 76 /M16/P0:i                          0
 77 /M16/T0:i                    9.82e-05
 78 /M16/T1:i                   -9.82e-05
 79 /M17/MP/B:i                 2.513e-12
 80 /M17/MP/D:i                -9.781e-05
 81 /M17/MP/G:i                        0
 82 /M17/MP/S:i                 9.781e-05
 83 /M17/P0:i                          0
 84 /M17/T0:i                   9.781e-05
 85 /M17/T1:i                  -9.781e-05
 86 /M18/E0:i                          0
 87 /M18/MN/B:i                -2.711e-12
 88 /M18/MN/D:i                 9.819e-05
 89 /M18/MN/G:i                        0
 90 /M18/MN/S:i                -9.819e-05
 91 /M18/T0:i                  -9.819e-05
 92 /M18/T1:i                   9.819e-05
 93 /M19/E0:i                          0
 94 /M19/MN/B:i                -3.265e-12
 95 /M19/MN/D:i                 9.781e-05
 96 /M19/MN/G:i                        0
 97 /M19/MN/S:i                -9.781e-05
 98 /M19/T0:i                  -9.781e-05
 99 /M19/T1:i                   9.781e-05
100 /M2/E0:i                           0
101 /M2/MN/B:i                 -5.534e-12
102 /M2/MN/D:i                   0.000111
103 /M2/MN/G:i                         0
104 /M2/MN/S:i                  -0.000111
105 /M2/T0:i                    -0.000111
106 /M2/T1:i                     0.000111
107 /M20/E0:i                          0
108 /M20/MN/B:i                -7.551e-13
109 /M20/MN/D:i                  0.000196
110 /M20/MN/G:i                        0
```

111	/M20/MN/S:i	-0.000196
112	/M20/T0:i	-0.000196
113	/M20/T1:i	0.000196
114	/M21/MP/B:i	2.513e-12
115	/M21/MP/D:i	-9.781e-05
116	/M21/MP/G:i	0
117	/M21/MP/S:i	9.781e-05
118	/M21/P0:i	0
119	/M21/T0:i	9.781e-05
120	/M21/T1:i	-9.781e-05
121	/M22/MP/B:i	3.067e-12
122	/M22/MP/D:i	-9.82e-05
123	/M22/MP/G:i	0
124	/M22/MP/S:i	9.82e-05
125	/M22/P0:i	0
126	/M22/T0:i	9.82e-05
127	/M22/T1:i	-9.82e-05
128	/M23/E0:i	0
129	/M23/MN/B:i	-2.711e-12
130	/M23/MN/D:i	9.819e-05
131	/M23/MN/G:i	0
132	/M23/MN/S:i	-9.819e-05
133	/M23/T0:i	-9.819e-05
134	/M23/T1:i	9.819e-05
135	/M24/E0:i	0
136	/M24/MN/B:i	-3.265e-12
137	/M24/MN/D:i	9.781e-05
138	/M24/MN/G:i	0
139	/M24/MN/S:i	-9.781e-05
140	/M24/T0:i	-9.781e-05
141	/M24/T1:i	9.781e-05
142	/M25/E0:i	0
143	/M25/MN/B:i	-7.551e-13
144	/M25/MN/D:i	0.000196
145	/M25/MN/G:i	0
146	/M25/MN/S:i	-0.000196
147	/M25/T0:i	-0.000196
148	/M25/T1:i	0.000196
149	/M3/MP/B:i	3.813e-13
150	/M3/MP/D:i	-0.0002442
151	/M3/MP/G:i	0
152	/M3/MP/S:i	0.0002442
153	/M3/P0:i	0
154	/M3/T0:i	0.0002442
155	/M3/T1:i	-0.0002442
156	/M4/MP/B:i	3.813e-13
157	/M4/MP/D:i	-0.0002442
158	/M4/MP/G:i	0
159	/M4/MP/S:i	0.0002442
160	/M4/P0:i	0
161	/M4/T0:i	0.0002442
162	/M4/T1:i	-0.0002442
163	/M5/MP/B:i	2.897e-12
164	/M5/MP/D:i	-0.0001333
165	/M5/MP/G:i	0
166	/M5/MP/S:i	0.0001333

167	/M5/P0:i	0
168	/M5/T0:i	0.0001333
169	/M5/T1:i	-0.0001333
170	/M6/MP/B:i	2.897e-12
171	/M6/MP/D:i	-0.0001333
172	/M6/MP/G:i	0
173	/M6/MP/S:i	0.0001333
174	/M6/P0:i	0
175	/M6/T0:i	0.0001333
176	/M6/T1:i	-0.0001333
177	/M7/E0:i	0
178	/M7/MN/B:i	-2.988e-12
179	/M7/MN/D:i	0.0001333
180	/M7/MN/G:i	0
181	/M7/MN/S:i	-0.0001333
182	/M7/T0:i	-0.0001333
183	/M7/T1:i	0.0001333
184	/M8/E0:i	0
185	/M8/MN/B:i	-2.988e-12
186	/M8/MN/D:i	0.0001333
187	/M8/MN/G:i	0
188	/M8/MN/S:i	-0.0001333
189	/M8/T0:i	-0.0001333
190	/M8/T1:i	0.0001333
191	/M9/E0:i	0
192	/M9/MN/B:i	-4.842e-13
193	/M9/MN/D:i	0.000108
194	/M9/MN/G:i	0
195	/M9/MN/S:i	-0.000108
196	/M9/T0:i	-0.000108
197	/M9/T1:i	0.000108
198	/M9A/E0:i	0
199	/M9A/MN/B:i	-4.848e-13
200	/M9A/MN/D:i	2.528e-05
201	/M9A/MN/G:i	0
202	/M9A/MN/S:i	-2.528e-05
203	/M9A/T0:i	-2.528e-05
204	/M9A/T1:i	2.528e-05
205	/MC1/E0:i	0
206	/MC1/MN/B:i	-5.014e-12
207	/MC1/MN/D:i	2.51e-12
208	/MC1/MN/G:i	0
209	/MC1/MN/S:i	2.504e-12
210	/MC1/T0:i	2.504e-12
211	/MC1/T1:i	2.51e-12
212	/MC2/MP/B:i	5.026e-12
213	/MC2/MP/D:i	-2.516e-12
214	/MC2/MP/G:i	0
215	/MC2/MP/S:i	-2.51e-12
216	/MC2/P0:i	0
217	/MC2/T0:i	-2.51e-12
218	/MC2/T1:i	-2.516e-12
219	/MC3/E0:i	0
220	/MC3/MN/B:i	-5.014e-12
221	/MC3/MN/D:i	2.504e-12
222	/MC3/MN/G:i	0

223	/MC3/MN/S:i	2.51e-12
224	/MC3/T0:i	2.51e-12
225	/MC3/T1:i	2.504e-12
226	/MC4/MP/B:i	5.026e-12
227	/MC4/MP/D:i	-2.51e-12
228	/MC4/MP/G:i	0
229	/MC4/MP/S:i	-2.516e-12
230	/MC4/P0:i	0
231	/MC4/T0:i	-2.516e-12
232	/MC4/T1:i	-2.51e-12
233	/MC5/E0:i	0
234	/MC5/MN/B:i	-5.014e-12
235	/MC5/MN/D:i	2.504e-12
236	/MC5/MN/G:i	0
237	/MC5/MN/S:i	2.51e-12
238	/MC5/T0:i	2.51e-12
239	/MC5/T1:i	2.504e-12
240	/MC6/MP/B:i	5.026e-12
241	/MC6/MP/D:i	-2.51e-12
242	/MC6/MP/G:i	0
243	/MC6/MP/S:i	-2.516e-12
244	/MC6/P0:i	0
245	/MC6/T0:i	-2.516e-12
246	/MC6/T1:i	-2.51e-12
247	/MC7/E0:i	0
248	/MC7/MN/B:i	-5.014e-12
249	/MC7/MN/D:i	2.51e-12
250	/MC7/MN/G:i	0
251	/MC7/MN/S:i	2.504e-12
252	/MC7/T0:i	2.504e-12
253	/MC7/T1:i	2.51e-12
254	/MC8/MP/B:i	5.026e-12
255	/MC8/MP/D:i	-2.516e-12
256	/MC8/MP/G:i	0
257	/MC8/MP/S:i	-2.51e-12
258	/MC8/P0:i	0
259	/MC8/T0:i	-2.51e-12
260	/MC8/T1:i	-2.516e-12
261	/MSC1/MP/B:i	5.574e-12
262	/MSC1/MP/D:i	-2.51e-12
263	/MSC1/MP/G:i	0
264	/MSC1/MP/S:i	-3.063e-12
265	/MSC1/P0:i	0
266	/MSC1/T0:i	-3.063e-12
267	/MSC1/T1:i	-2.51e-12
268	/MSC2/E0:i	0
269	/MSC2/MN/B:i	-4.467e-12
270	/MSC2/MN/D:i	2.51e-12
271	/MSC2/MN/G:i	0
272	/MSC2/MN/S:i	1.957e-12
273	/MSC2/T0:i	1.957e-12
274	/MSC2/T1:i	2.51e-12
275	/MSC3/MP/B:i	5.022e-12
276	/MSC3/MP/D:i	-2.51e-12
277	/MSC3/MP/G:i	0
278	/MSC3/MP/S:i	-2.512e-12

279	/MSC3/P0:i	0
280	/MSC3/T0:i	-2.512e-12
281	/MSC3/T1:i	-2.51e-12
282	/MSC4/E0:i	0
283	/MSC4/MN/B:i	-5.018e-12
284	/MSC4/MN/D:i	2.51e-12
285	/MSC4/MN/G:i	0
286	/MSC4/MN/S:i	2.508e-12
287	/MSC4/T0:i	2.508e-12
288	/MSC4/T1:i	2.51e-12
289	/MSC5/MP/B:i	5.574e-12
290	/MSC5/MP/D:i	-2.51e-12
291	/MSC5/MP/G:i	0
292	/MSC5/MP/S:i	-3.063e-12
293	/MSC5/P0:i	0
294	/MSC5/T0:i	-3.063e-12
295	/MSC5/T1:i	-2.51e-12
296	/MSC6/E0:i	0
297	/MSC6/MN/B:i	-4.467e-12
298	/MSC6/MN/D:i	2.51e-12
299	/MSC6/MN/G:i	0
300	/MSC6/MN/S:i	1.957e-12
301	/MSC6/T0:i	1.957e-12
302	/MSC6/T1:i	2.51e-12
303	/MSC7/MP/B:i	5.022e-12
304	/MSC7/MP/D:i	-2.51e-12
305	/MSC7/MP/G:i	0
306	/MSC7/MP/S:i	-2.512e-12
307	/MSC7/P0:i	0
308	/MSC7/T0:i	-2.512e-12
309	/MSC7/T1:i	-2.51e-12
310	/MSC8/E0:i	0
311	/MSC8/MN/B:i	-5.018e-12
312	/MSC8/MN/D:i	2.51e-12
313	/MSC8/MN/G:i	0
314	/MSC8/MN/S:i	2.508e-12
315	/MSC8/T0:i	2.508e-12
316	/MSC8/T1:i	2.51e-12
317	/N$23:v	2.5
318	/N$274:v	0.7446
319	/N$41:v	2.5
320	/N$44:v	0.7446
321	/Net1:v	0.8848
322	/Net2:v	4.629
323	/Net3:v	4.629
324	/Net4:v	0.4737
325	/Net5:v	0.4737
326	/v1:v	1.948
327	/v2:v	2.5
328	/v3:v	2.498
329	/v4:v	1.948
330	/v5:v	2.5
331	/v6:v	2.498
332	/vbias1:v	3.762
333	/vbias2:v	2.411
334	/vbias3:v	1.09

335	/vfix:v	2.5
336	/vin+:v	2
337	/vin-:v	2
338	/vout+:v	2.494
339	/vout-:v	2.494

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