Design and Fabrication of Polycrystalline Material Thin-Film Transistors for Active Matrix Liquid-Crystal Display and Static Random Access Memory Applications

by

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ABSTRACT

Polycrystalline silicon germanium (poly-$Si_{1-x}Ge_x$) thin-film transistors have been designed and fabricated for applications in the areas of active matrix liquid-crystal display (AMLCD) and static random access memory (SRAM). This project has been completed in four phases: design, fabrication, testing, and device/process modification.

First, the design phase includes device design, unit process development, and process integration. A top-gate TFT is chosen for process and testing simplicity. Unit process development includes active layer film deposition, grain size enhancement, gate dielectric considerations, and gate/source/drain doping and activation. The film deposition investigation is composed of plasma-enhanced low-pressure chemical vapor deposition (PELPCVD) and low-pressure chemical vapor deposition (LPCVD) of polycrystalline and amorphous films. Further, electrical characterization is done on poly-$Si_{1-x}Ge_x$ using Hall-Effect test structures, and results show higher mobility and lower sheet resistance were possible when the Ge content is optimized. Grain size enhancement techniques explored include amorphous deposition followed by solid-phase crystallization (SPC), polycrystalline deposition, and poly deposition followed by Si implant amorphization and SPC. Gate dielectric considerations include thermal oxide and low-temperature oxide (LTO). LTO annealing duration and gate/source/drain dopant activation are also optimized.

Second, the fabrication involves a low-temperature(< 625°C) 0.8 μm self-aligned NMOS/PMOS Si process with four levels of device-definition masks plus two implant split masks. Device separation was done by mesa island isolation of the active layer. Fabricated device sizes range from 0.5 μm to 60 μm drawn gate length and width.

Third, device testing includes typical I_{DS} vs. V_{DS} transfer curves, I_{DS} vs. V_{GS} transfer characteristics, and activation energy determination. Mobility, threshold voltage,

subthreshold slope, and leakage current are measured using I_{DS} vs. V_{GS} curves. Further, temperature-dependent I_{DS} vs. V_{GS} curves are used to measure the activation energy.

Finally, a poly-Si-capped poly-$Si_{1-x}Ge_x$ TFT structure is designed to improve the gate oxide interfacial quality of poly-$Si_{1-x}Ge_x$ TFTs. Fabrication of poly-Si-capped poly-$Si_{1-x}Ge_x$ TFTs requires only a 10% modification of the conventional process.

The major contribution of this project to the polycrystalline material TFT research can be summarized by the results of high-temperature ($\leq$ 1000°C) processed and low-temperature ($\leq$ 625°C) processed TFTs. High-temperature processed poly-Si-capped poly-$Si_{0.9}Ge_{0.1}$ TFTs with thermal oxide were found to have the highest mobility reported-to-date, for poly-$Si_{1-x}Ge_x$, of 51 cm^2/V-sec for p-channel devices and 41 cm^2/V-sec for n-channel devices. This is compared to the hole mobility of 27 cm^2/V-sec and the electron mobility of 45 cm^2/V-sec for similarly processed poly-Si TFTs. Low-temperature processed poly-$Si_{0.88}Ge_{0.12}$ TFTs were also measured to have the highest mobility reported-to-date, for poly-$Si_{1-x}Ge_x$, of 35 cm^2/V-sec for hole and 28 cm^2/V-sec for electrons. This is compared to the hole mobility of 26 cm^2/V-sec and the electron mobility of 29 cm^2/V-sec for similarly processed poly-Si TFTs.

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Acknowledgments: The single most read page in a thesis[0]

I thank my parents for everything they have done for me to get me this far. They have sacrificed much of what they had yesterday to make me much of what I am today.

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[0] Julie A. Tsai, private communication.

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Chapter 1

Introduction

Thin-film transistors (TFTs) [1] (Figure 1.1) belong to a novel class of transistors that have a similar structure to metal-oxide-semiconductor field-effect transistors (MOSFETs), devices that are the basic building blocks of virtually all integrated circuits. Although the conventional MOSFET technology is far more mature and advanced than the TFT technology, there are many applications where it is impossible to use the conventional MOSFET technology. These applications usually involve transistors being constructed on an amorphous substrate such as glass or silicon dioxide. These areas first became the niche for TFTs, then they emerge as markets of its own class. Some of the most important TFT applications include liquid crystal displays (LCDs) [2-3], static random access memories (SRAMs)[4,5], and image sensors [6,7].

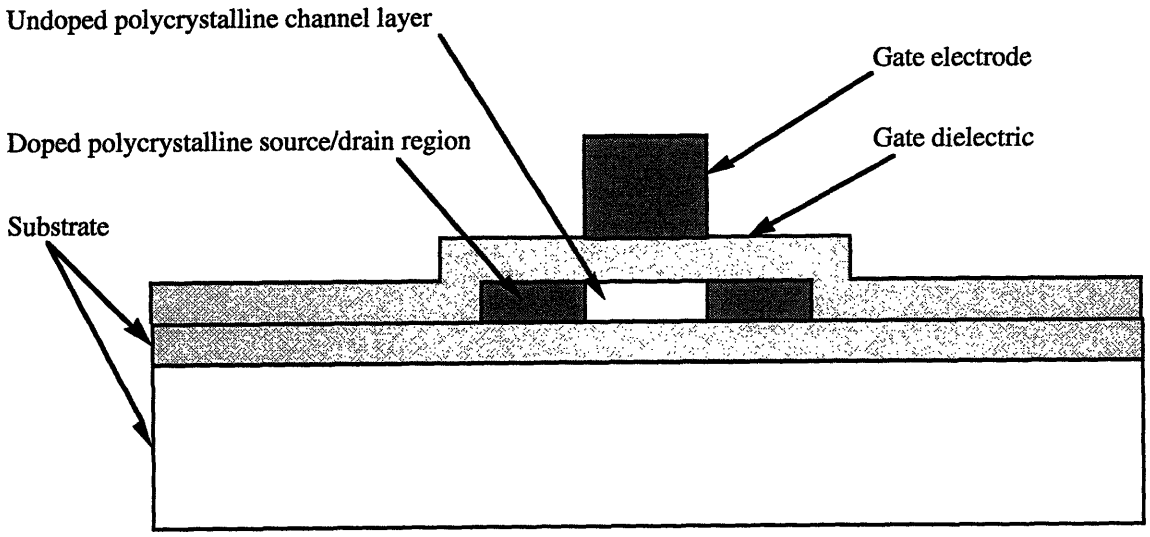


Fig. 1.1: A typical TFT structure.

1.1 Applications of TFTs:

LCDs

LCD is a type of display that relies pixel control on liquid crystals, voltage-controlled light filters. The most important part of building a LCD is the formation of the voltage

controllers which are usually made by transistor switches. Since LCDs require transparent substrates to house both the transistor switches and the liquid crystals, an ideal choice for the substrate is glass. Because glass is amorphous, conventional MOSFET technology is not applicable; therefore, TFTs are the ideal candidates for such applications.

Another part of an LCD is the peripheral circuit element. Peripheral circuit elements of an LCD usually include shift registers, drivers, and combinational logic circuits. These peripheral elements are usually done by employing application specific integrated circuits (ASICs) using conventional MOSFET technology[3]. However, it will be far more economical to build ASICs on the same glass substrate along with the transistor switches [2,3]; furthermore, with a totally integrated system , signals from the peripheral circuits are better transmitted and received since they are not required to go off-chip.

Amorphous Si was first used in the TFT technology for its process simplicity and low leakage current[2], and are suitable for the transistor switches. However, because of its lower mobility, amorphous Si TFTs do not qualify to be used as the peripheral circuit elements. Therefore, the latest trend calls for a high-mobility material, polycrystalline Si (poly-Si) [2], to serve as pixel controllers as well as the peripheral circuit elements[3].

SRAMs

An SRAM cell consists of two access transistors controlled by the word line[5] and a flip flop which is made up of two Complimentary Metal Oxide Semiconductor (CMOS) inverters. Furthermore, a CMOS inverter consists a pull-up and a pull-down transistor. Finally, a pull-down transistor is defined as a transistor that provides a current sink to the electrical ground when the transistor is turned on; on the other hand, a pull-up transistor is a transistor which provides a current path to the power supply (Vdd) when the transistor is turned on.

The earliest CMOS SRAM cell is called the 6-T cell which consists of six conventional MOSFETs; later, the 6-T cell evolved into the 4-T+2-R cell with four MOSFETs plus two

polycrystalline resistors serving as the pull-up devices; as of today, the SRAM cell has matured to an elegant split-word-line (SWL) SRAM cell (Fig. 2) which employs four MOSFETs plus two pull-up TFTs[4,5]. The SWL TFT SRAM cell has the advantage of compactness over the 6-T cell and the advantage of higher on/off current ratio over the 4-T+2R design[5].

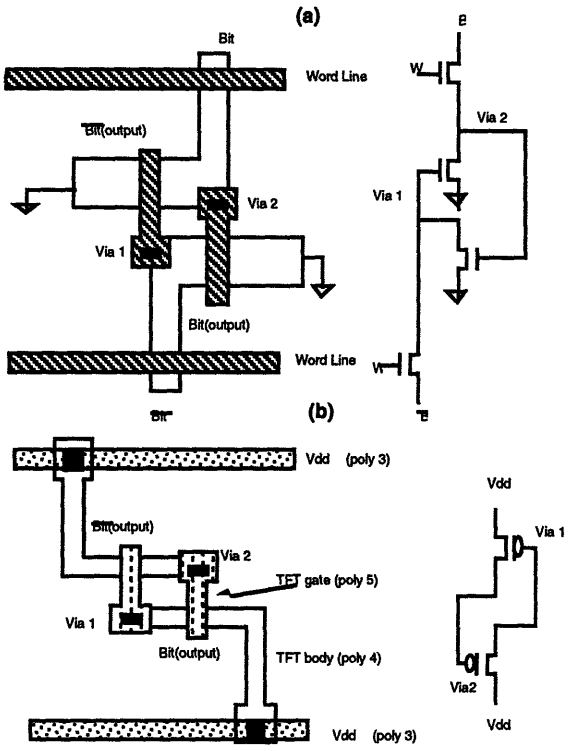


Fig. 1.2: A typical SWL SRAM cell with TFT pull-up transistors. a) Two single crystalline access transistors and two pull-down transistors. b) Two TFT pull-up transistors [6].

Image Sensors

Contact-type linear image sensors are commonly used in facsimiles and optical scanners because of their compactness and the cost-advantage due to the minimum requirements for optical components [6,7]. Each pixel of these sensors consists of a detector based on amorphous Si TFT and an analog switch. Signal is read out from each pixel by turning on its switch and transferring the charge stored in the detector to an external amplifier. Similar

to the development of LCDs, it is very important to integrate the amorphous Si sensors, the analog switch, and the external amplifier. Consequently, a material with higher mobility is required to ensure enough circuit speed and current drive for such an integration[10].

1.2 Motivation for using polycrystalline silicon germanium alloy thin film transistors

Current drive of TFTs is directly proportional to the average grain size of the TFT channel layer. As a result, numerous grain-size enhancement techniques were proposed, and the two major techniques are solid phase crystallization (SPC) [8-13] and Excimer laser annealing (ELA) [14].

T.-J. King et. al. have approached this problem by using poly-$Si_{1-x}Ge_x$ as a replacement for poly-Si in the active layer of the TFT structure without changing any other process parameters[15-17]. Poly-$Si_{1-x}Ge_x$ offers higher mobility and lower processing temperatures than poly-Si[18-20]. Higher mobilities provide higher circuit speed, and lower processing temperatures allow the flexibility of using cheaper substrates. The design and fabrication of poly-$Si_{1-x}Ge_x$ TFTs are covered in Chapter 3. But first, the fundamental device physics are reviewed in Chapter 2 because they are the prerequisites for the device and process design in Chapter 3.

Chapter 2

A Brief Review of Semiconductor Device Physics

2.1 Metal-Oxide-Semiconductor (MOS)

An ideal MOS capacitor can be characterized by several device parameters: threshold voltage (V_{th}), interface trap density (Q_i), breakdown voltage(V_{Br}), and leakage current (I_L) [21]. V_{th} can be well controlled by doping levels and device dimensions; on the other hand, V_{th}, Q_i, and I_L are mainly controlled by the choice of gate dielectric as well as the history of the thermal treatment. Some of the most important governing equations for MOS capacitors are listed below:

$$\text{Flat band voltage} = V_{FB} = \psi_{ms} - \frac{Q_i}{C_{ox}} \tag{2.1.1}$$

$$\text{Threshold volatage} = V_{th} = V_{FB} - \frac{Q_d}{C_{ox}} + 2\phi_f \tag{2.1.2}$$

$$\psi_{ms} = \psi_m - \psi_s \tag{2.1.3}$$

$$Q_i = \text{int}\,erface \text{ traps density} \tag{2.1.4}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.1.5}$$

$$Q_d = 2\sqrt{q\varepsilon_s N_A \phi_f} \tag{2.1.6}$$

$$\phi_f = \frac{KT}{q}\ln\frac{N_A}{n_i} \tag{2.1.7}$$

Since LTO is commonly used as the gate dielectric of a low-temperature processed TFT, V_{Br} and I_L are the two figures of merit we monitor. Optimization of the gate dielectric and dielectric densification will be covered in Section 3.3.

2.2 Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

MOSFET is a three-terminal voltage-controlled current source [21], as seen in figure 2.1. The gate voltage (V_{GS}) serves as the switch to the current source between the source and drain terminals. Similar to the MOS structure, the switch is turned on after the gate voltage exceeds the threshold voltage.

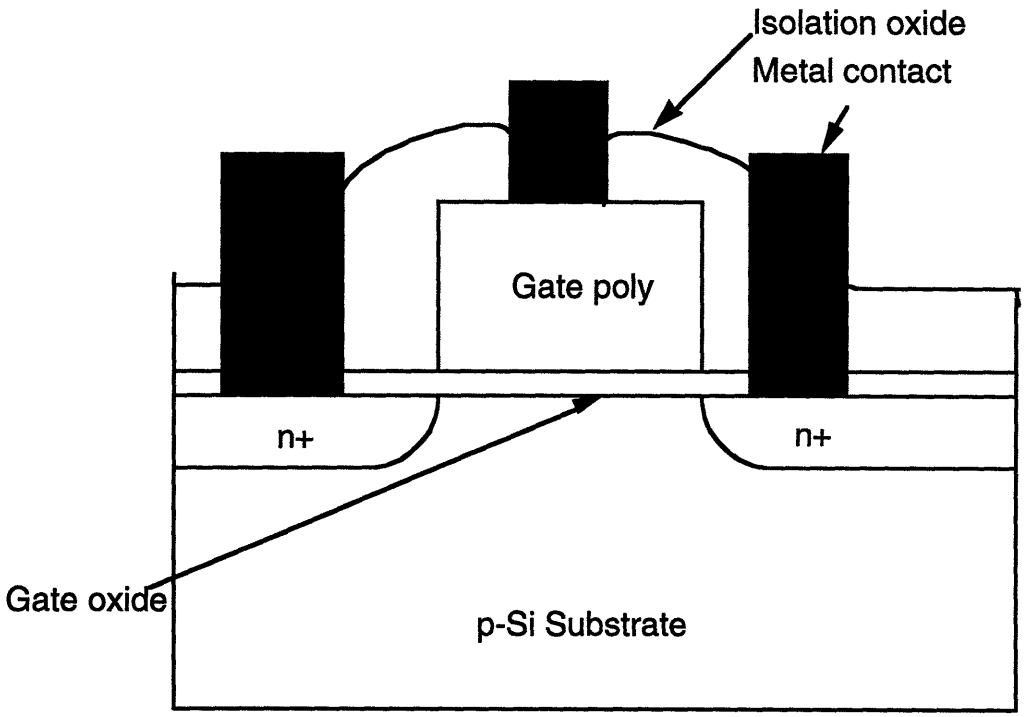


Figure 2.1 A typical self-aligned n-channel MOSFET

There are three distinctive regions in the operation of a MOSFET: cutoff, linear, and saturation. First, the cutoff region is defined as the off state of the device when $V_{GS} < V_{th}$. Next, the linear region is defined as the region where $V_{GS} > V_{th}$ and also $V_{GD} > V_{th}$. Finally, the saturation is defined as the region where V_{DS} is high enough that

V_{GD} is no longer effective enough to invert the entire channel, or the occurrence of pinch-off at the drain end. This region is characterized by $V_{GS}>V_{th}$ and $V_{GD}<V_{th}$.

Some figures of merit of MOSFET are V_{th}, field-effect mobility, subthreshold slope, and leakage current. Some of the governing equations in MOSFETs are derived in this section [21]. (2.2.1) through (2.2.10) are shown on the next page with C_G being the gate capacitance, Q_E being the inversion charge density, E being the electric field in the channel, T being the channel transit time, V_{DSsat} being the effective V_{DS} in the saturation regime, and SS being the subthreshold slope. (2.2.1) through (2.2.5) are from the fundamental physics of solid, and (2.2.6) was obtained by the substitution of V_{GS} with $(V_{GS}-V_{DS}/2)$ into (2.2.5). In the linear region, the voltage at the center of the channel can be approximated as $V_{DS}/2$; thus the effective gate voltage is $V_{GS}-V_{DS}/2$ instead of just V_{GS}, as used in (2.2.5). In the saturation regime, I_{DS} reaches a saturated value when V_{DS} is increase to V_{DSsat}. At that point, I_{DS} is determined by drift velocity of carriers across the pinch-off depletion region at the drain end. In this region V_{DS} is replaced by the effective V_{DS}, or V_{DSsat}. Results are shown in (2.2.7). Finally, subthreshold swing, which defines how sharp transistors turn on, is shown in (2.2.10) and (2.2.11).

Derivation of I_{DS}:

$$C_G = \frac{\varepsilon \cdot W \cdot L}{t_{ox}} \tag{2.2.1}$$

$$Q_E = (V_{GS} - V_{th}) \cdot C_G \tag{2.2.2}$$

$$E = \frac{V_{DS}}{L} \tag{2.2.3}$$

$$\tau = \frac{L}{V_{el}} = \frac{L}{\mu E} = \frac{L^2}{\mu V_{DS}} \tag{2.2.4}$$

$$I_{DS} = \frac{Q_E}{\tau} = \frac{(V_{GS} - V_{th}) \cdot C_G}{\frac{L^2}{\mu V_{DS}}} \tag{2.2.5}$$

Linear Regime:

$$I_{DS} = \frac{\varepsilon_{ox} W \mu}{t_{ox} L}[(V_{GS} - V_{th}) \cdot V_{DS} - \frac{(V_{DS})^2}{2}] \tag{2.2.6}$$

Saturation Regime:

$$I_{DS} = \frac{\varepsilon_{ox} W \mu}{t_{ox} L}[(V_{GS} - V_{th}) \cdot V_{DSsat} - \frac{(V_{DSsat})^2}{2}] \tag{2.2.7}$$

$$V_{DSsat} = V_{GS} - V_{th} \tag{2.2.8}$$

$$I_{DS} = \frac{\varepsilon_{ox} W \mu}{t_{ox} L}[\frac{(V_{GS} - V_{th})^2}{2}] \tag{2.2.9}$$

Definition of Subthreshold Slope:

$$SS = \ln(10) \cdot {dV_G}/{d(\ln I_{DS})} \tag{2.2.10}$$

$$SS \approx \frac{KT}{q} \ln 10 \cdot (1 + \frac{C_d}{C_{ox}}) \tag{2.2.11}$$

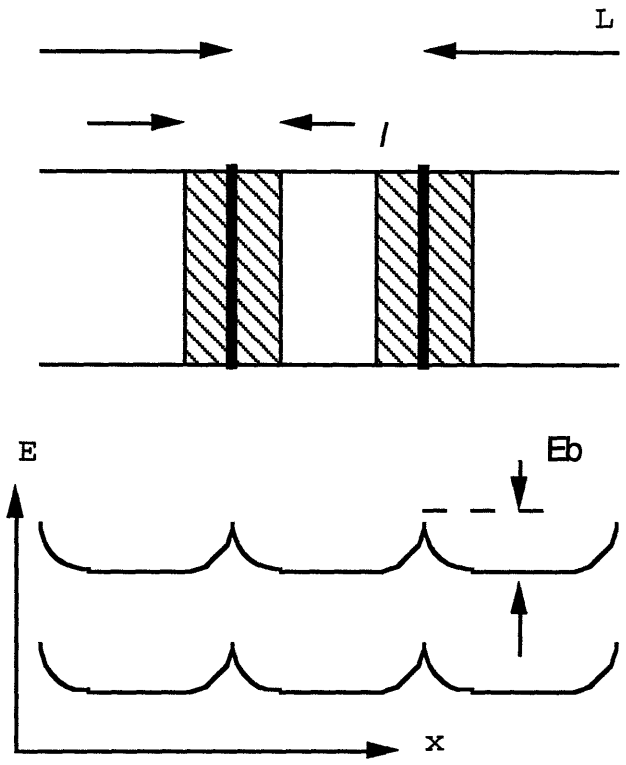


Figure 2.2 Seto's grain boundary model

2.3 Thin-Film Transistor (TFT)

TFTs can be considered as a special type of silicon on insulator (SOI) with the exception of the active layer of the transistor, which is made of polycrystalline material. The ideal current equations [21] derived for MOSFET will be modified according to Seto's grain boundary carrier hopping theory[22]. Seto proposed to model polycrystalline films as a collection of single crystalline regions (see figure 2.2) separated by sheet charge of grain boundary traps, N_T. The grain boundary traps also create a depletion region which serves as a potential hill to carriers. The equations that describe this theory are summarized in (2.4.1) and (2.4.2). V_b is defined as the grain boundary height carriers must surmount in

order to participate in conduction. Modified device parameters and current equations with the effects of N_T are shown in (2.4.3) through (2.4.6).

Bulk properties:

$$V_b = \frac{qN_T^2}{8\varepsilon_o\varepsilon_s N_A} \tag{2.4.1}$$

and

$$\mu = \frac{q \cdot L}{2\pi \cdot kT \cdot m_e^*} \cdot e^{(\frac{-eV_b}{kT})} \tag{2.4.2}$$

TFT device parameters and current-voltage relations:

$$V_{th} = V_{FB} - \frac{Q_d}{C_{ox}} + 2\phi_f + \frac{N_T}{C_{ox}} \tag{2.4.3}$$

$$I_{DS} = \mu_o \cdot C_i \cdot (W/L) \cdot (V_{GS} - V_{th}) \cdot V_{DS} \cdot e^{-(E_a/KT)} \tag{2.4.4}$$

$$\mu_{FE} = \mu_o \cdot e^{-(E_a/KT)} \tag{2.4.5}$$

$$SS \approx \frac{kT}{q} \ln 10 \cdot (1 + \frac{C_d}{C_{ox}} + \frac{q \cdot d \cdot N_T}{C_{ox}}) \tag{2.4.6}$$

where C_d is the depletion capacitance, C_{ox} is the gate capacitance, m^* is the carrier effective mass, N_A is the dopant concentration, and E_a is the activation energy for field-effect mobility.

2.4 The Hall effect

If a magnetic field is applied perpendicular to the direction in which holes drift in a p-type semiconductor, the path of the holes tends to be deflected (Fig. 2.3). This phenomenon is known as the Hall effect [21].

Known parameters:
Bz,Ix

Measured parameters:
$Vy=V_{AB}, Vx=V_{CD}$

Calculated parameters:
p, rho, and mu

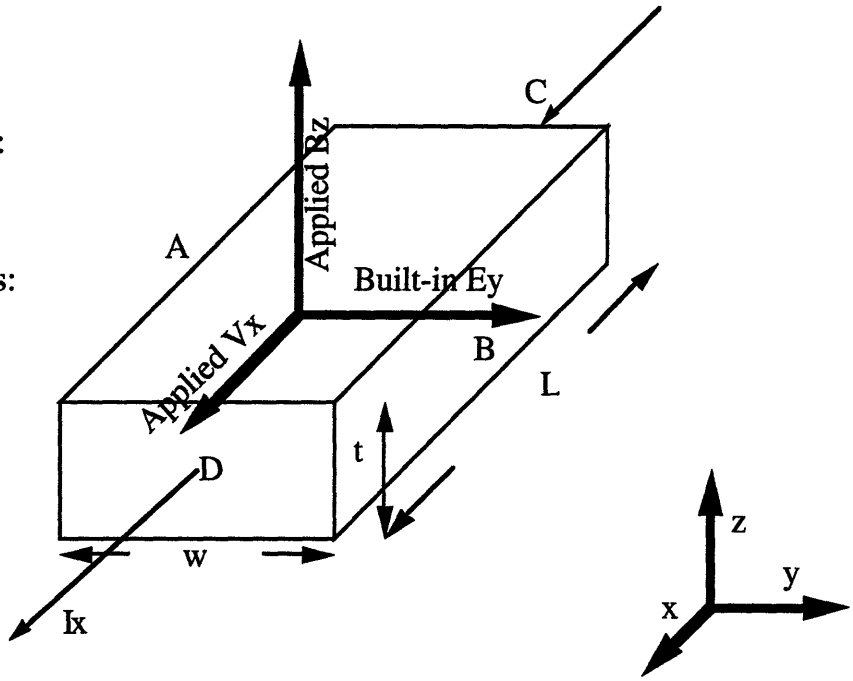


Figure 2.3 Depiction of Hall effect

The total force exerted on the hole is shown in (2.5.1):

$$F_y = q(E_y - v_x \times B_z)$$
$$E_y = v_x B_z \qquad (2.5.1)$$

Since we know that the holes are not accelerating in the y-direction, Fy must be balanced or zero. This calls for a built-in electric field, Ey, that counterbalances the force generated by

the cross product of the magnetic field and the velocity in the x-direction. Also, the saturation velocity, v_x, can be expressed in terms of charge, concentration, and current density. This is summarized in (2.5.2) below:

$$E_y = \frac{J_x}{qp_o} B_z = R_H J_x B_z \qquad (2.5.2)$$

Further, we can solve for the active carrier concentration by rearranging (2.5.2). Carrier concentration is then shown in (2.5.3):

$$p_o = \frac{J_x \cdot B_z}{qE_y} = \frac{I_x \cdot B_z}{qtV_{AB}} \qquad (2.5.3)$$

Resistivity can be solved without using the external magnetic field; however, Hall mobility determination requires both the resistivity and the Hall coefficient which is obtained under a external magnetic field. Resulting equations are shown below:

$$\rho = \frac{Rwt}{L} = \frac{V_{CD}/I_x}{L/wt} \qquad (2.5.4)$$

$$\mu = \frac{\sigma}{qp_o} = \frac{R_H}{\rho} \qquad (2.5.6)$$

Chapter 3

Process and Device Design of Polycrystalline Material TFTs

TFTs are usually fabricated on an amorphous medium which can be either glass or interlevel dielectric. The TFT process begins with the active layer film deposition and grain enhancement. Then, gate dielectric and gate electrode definition take place, followed by source/drain/gate dopant implantation and activation. Next, isolation oxide is deposited and contact cuts are made. Finally, Al is sputtered and patterned to serve as electrical contacts and plasma hydrogenation is performed.

3.1 Active layer design

We are interested in two main types of materials: silicon and silicon germanium. In addition, we have looked at the different options of deposition technology: low pressure chemical vapor deposition (LPCVD) and plasma-enhanced LPCVD (PELPCVD). Finally, we have also explored the option of amorphous Si and $Si_{1-x}Ge_x$ deposition.

3.1.1 Trade-offs between the use of $Si_{1-x}Ge_x$ and Si films by Hall-Effect test structures

To find out the trade-offs between $Si_{1-x}Ge_x$ and Si films , electrical characterization of resistivity and mobility as a function of Ge content is obtained using Hall-effect test structures shown in figure 3.1 [18,19] (See Appendix B). Si substrate is used as the starting material, then a 5000Å of thermal oxide is grown. Next, about 1000Å of poly-$Si_{1-x}Ge_x$ is deposited on the samples. One light blanket implant is used as the doping of the film while a heavy contact implant is done in the contact area to form ohmic contacts. For electrical isolation, 3000Å of LTO is deposited, then contact holes are formed and Al-1%Si is sputter-deposited and patterned. Finally, sintering in H_2/N_2 is done before the Hall measurements.

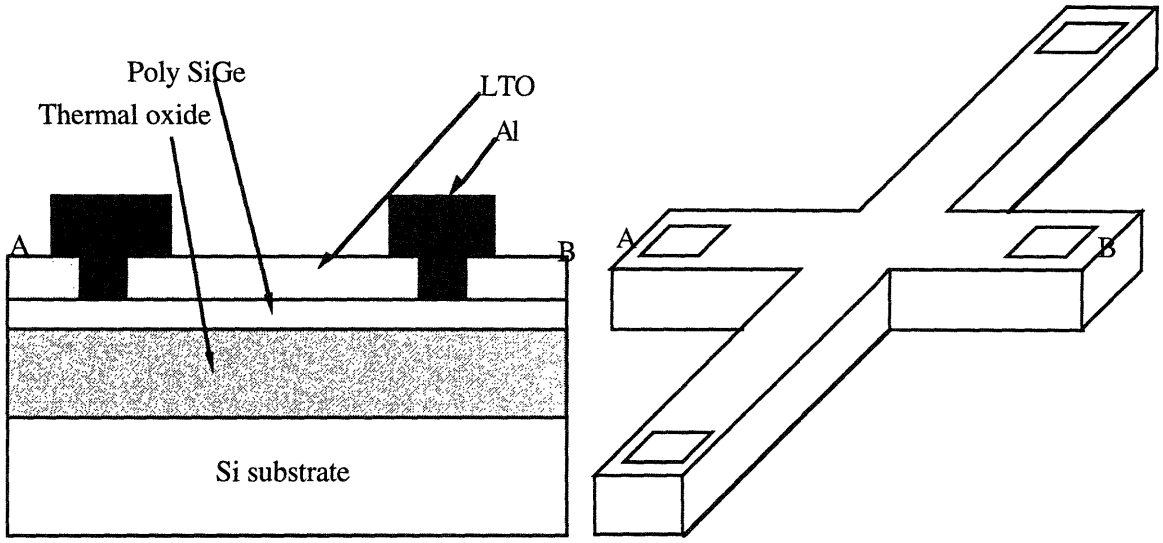


Figure 3.1 Hall-effect test structure

The results of the Hall-effect experiment are shown below in Fig. 3.2a and Fig. 3.2b. From the figures, hole mobility increases with the increase in Ge content until a critical Ge content is reached; on the other hand, electron mobility increases monotonically for all the Ge content attempted in this experiment. Finally, the resistivity seemed to be lowered as more Ge is alloyed with poly-Si, and the trend seems to continue for Ge content of up to 32%.

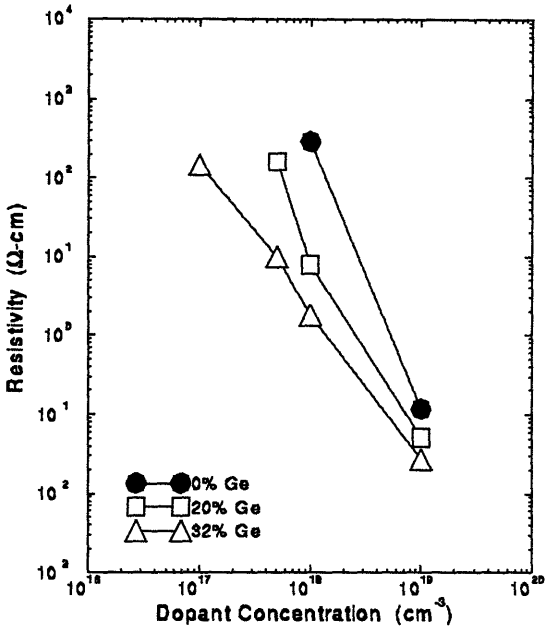


Figure 3.2a Resistivity as a function of Ge content

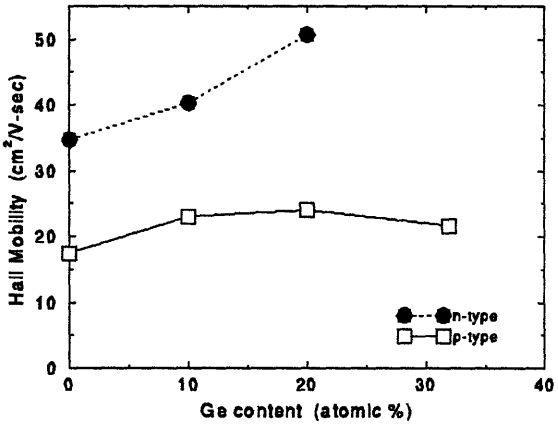


Figure 3.2b Hall mobility as a function of Ge content.

3.1.2 Trade-offs between the use of Poly and amorphous films

With regard to the choice between polycrystalline and amorphous materials, polycrystalline materials provide higher mobility while the amorphous materials provide lower leakage, better surface morphology, better uniformity, and lower thermal budget. Nevertheless, polycrystalline films can be formed from amorphous films, and they generally have higher mobility, larger grains, and lower leakage currents than the as-deposited polycrystalline films. The two major deposition systems, LPCVD and PELPCVD, are also compared for the applications of poly-Si and poly-$Si_{1-x}Ge_x$. Since GeO is volatile, PELPCVD is preferred for the poly-$Si_{1-x}Ge_x$ deposition for its higher Ge sticking coefficient on oxide; further, PELPCVD provides higher deposition rate and thereby increases throughput. PELPCVD also offers stronger textured grains which reduces misalignment angle between grains. Although PELPCVD provides many attractive features to the film deposition, LPCVD films are still widely used due to its simplicity and availability.

The different types of films available are summarized in Table 3.1 with the pros and cons associated with each method.

Film types	**Advantages**	**Disadvantage**
Si	simplicity	mobility and thermal budget
$Si_{1-x}Ge_x$	mobility and thermal budget	oxide interface
As-deposited poly	mobility, simplicity	uniformity
Amorphous to poly	mobility	complexity
Amorphous	morphology, uniformity	mobility
LPCVD	simplicity, grain size	growth rate, contamination
PELPCVD	sticking coefficient, growth rate, contamination, texture	grain sizes, damage

Table 3.1 Trade-offs between different types of films

3.2 Grain enhancement techniques

Equation (2.4.2) is rewritten below, and it governs the transport mechanism in poly films. It is easy to see that the mobility is linearly related to the grain size L. Therefore, it is very important that the grain size be maximized using various type of amorphization and subsequent annealing techniques.

$$\mu = \frac{q \cdot L}{2\pi \cdot kT \cdot m_e^*} \cdot e^{(\frac{-eV_b}{kT})} \qquad (3.2.1)$$

3.2.1 Amorphization

The amorphization techniques that will be discussed here consist of amorphous deposition and polycrystalline deposition with Si implant [8-10]. Amorphous deposition is accomplished by simply carrying out the normal deposition at a temperature lower than the polycrystalline/amorphous transition temperature (Table 3.2) [18]; however, the growth rate may be very low at such temperatures and plasma deposition is required to enhance the deposition rate. Another amorphization technique is the option of polycrystalline deposition with subsequent Si implantation [10]. This technique is more costly than the former and also more complicated; however, Si implantation provides a more thorough amorphization and therefore yields larger grains (figure 3.3). We have also found the optimized dose of Si for amorphization, and the results are summarized in Table 3.3.

Deposition temperature	Mode	Si	Si_xGe_{1-x}
600°C	thermal	poly	poly
500°C	thermal	amorphous	poly
500°C	plasma	amorphous	poly
450°C	plasma	amorphous	amorphous
400°C	plasma	amorphous	amorphous

Table 3.2 Poly to amorphous transition temperatures

Ge content/Si implant dose	1e14 cm^{-2}	5e14 cm^{-2}	1e15 cm^{-2}
0%	poly	poly	amorph
10%	poly	NA	amorph
25%	poly	amorph	amorph
43%	poly	amorph	amorph

Table 3.3 Si implant optimization

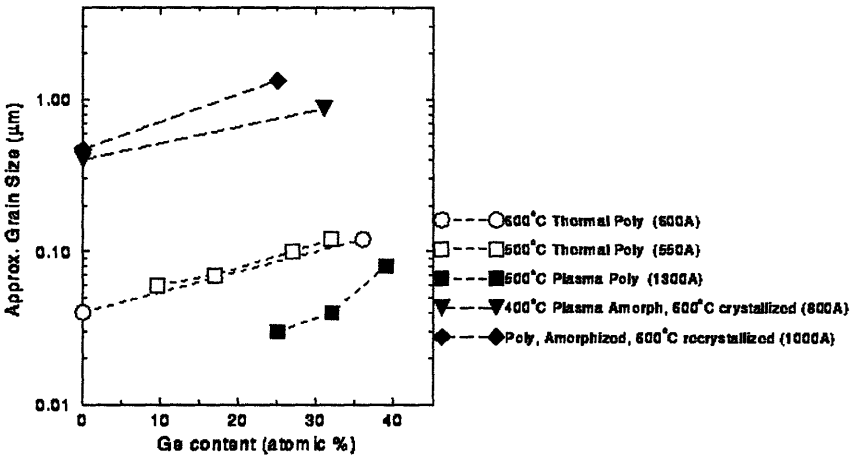


Figure 3.3 Grain size as a function of Ge content and active layer formation method.

3.2.2 (Re)crystallization

After an amorphous film is obtained, several annealing techniques have been proposed and used to recrystallize the amorphous film. First, solid phase crystallization (SPC) provides the traditional furnace annealing which lasts from 20 hours to 60 hours usually at low temperatures (~600°C) [8,10-13]. SPC suffers from the low throughput and ineffective annealing of intragranular defects; however, SPC is capable of producing the largest grains among all other techniques because of its slower process. Excimer laser annealing (ELA) has become more attractive recently because of the improving stability of lasers. In general, ELA-processed samples produces films with smaller but uniform grains; more importantly, ELA-processed TFTs are usually the highest performance devices [14]. Finally, we have briefly examined rapid thermal annealed TFTs which yield reasonably good performance, but its effect on the underlying glass substrate is still to be investigated. Table 3.4 summarizes the different (re)crystallization techniques.

Amorphization	Annealing	Advantage	Disadvantage
Amorphous as deposited	SPC	Surface morphology	Smaller grain
Si implant	SPC	Larger grain	Process complexity
Si implant	ELA	High mobility, higher throughput	Process complexity
Si implant	RTA	Process simplicity, high mobility	Deformation of glass substrate.
Amorphous as deposited	RTA	High mobility	Smaller grain

Table 3.4 Various (re)crystallization techniques

3.3 Gate dielectric considerations

The process parameters regarding gate dielectric annealing and dopant activation are optimized in a single experiment using LTO capacitors. P-type Si substrates are used and 1000Å of LTO is deposited. Next, samples are annealed in nitrogen at 600°C for either 0,12,24, or 36 hours before 3500Å of poly-Si is deposited at 625°C. Then, either a single implant or a double implant scheme is used to dope the poly-Si top plate of the LTO capacitor. The single implant is designed to have a dose of 2e15/cm^2 B at 30 KeV; on the other hand, the double implant composes of an 1e15 B/cm^2 blanket implant at 65 KeV and a 2e15 B/cm^2 implant at 30 KeV. Dopant activation is carried out in N_2 at 600°C for either 0.5 or 2 hours. Fowler-Nordheim measurements are done, and voltage operation range was defined as the gate voltage range for which leakage current is less than 10 nA. Arbitrary resistance measurements are also done by simple V/I evaluation of the heavily

doped poly-Si gate. The exact process traveler is in Appendix A. An LTO test structure is shown in Figure 3.4 and results are summarized in Table 3.5.

24-hour LTO densification was chosen according to the measured break-down voltage and leakage current. For the G/S/D doping, a single self-aligned G/S/D B implant was chosen over the double implant because of throughput and process simplicity considerations. Sheet resistance improvement of only 50% is achieved using the more complicated double implant scheme. Further, a 30-minute implant anneal in nitrogen at 600°C was chosen because any additional annealing in the same ambient does not enhance the sheet resistance much further.

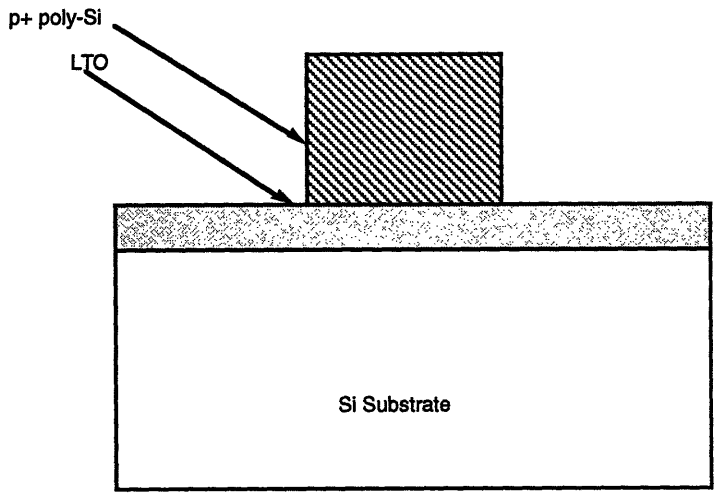


Figure 3.4 A LTO capacitor test structure

Densification duration (hrs)	Implant split	Dopant activation(hrs.)	Voltage operation range (V)	Resistance (arbitrary units)
0	double	2	0	
12	double	0.5	5	59
12	double	2	50	
12	single	0.5	10	59
12	single	2	25	
24	double	0.5	50	58
24	double	2	50	58
24	***single***	***0.5***	***60***	***110***
24	single	2	55	110
36	double	0.5	50	
36	double	2	70	55
36	single	0.5	40	100
36	single	2	45	106

Table 3.5 Results of the LTO experiment: optimized split is high-lighted

Other gate dielectrics have also been explored: thermal oxide and rapid thermal oxide. The results of TFT performance with other dielectrics are covered in Chapter 5.

3.4 Gate electrode, source, and drain doping control and activation

P^+ gate electrode is optimized using the LTO experiment. 2e15 B/cm^2 is chosen for a self-aligned implant. SUPREM simulation is performed to target the peak of the implant profile at the center of the source, drain, at gate electrode. Since the gate electrode is usually much thicker than the source or drain, compromise is made when choosing the implant energy. B is annealed for 0.5 to 2 hours while P is annealed for 60 hours, both at 600°C in

nitrogen ambient. Sheet resistance of source/drain area of a TFT is measured and shown in figure 3.5.

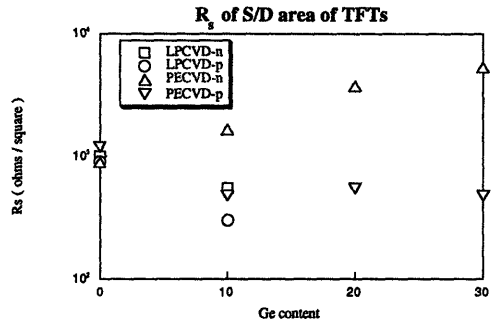


Figure 3.5 R_s of S/D area of TFTs as a function of Ge content

Chapter 4

Measured Current-Voltage Transfer Characteristics for Poly-$Si_{0.88}Ge_{0.12}$ TFTs

4.1 Fabrication process

We have fabricated poly-$Si_{1-x}Ge_x$ TFTs with a top-gate structure as shown in Figure 4.1 (See Appendix C). First, 5000Å of thermal oxide is grown on bare 4-inch silicon substrates, then approximately 1000Å of poly-$Si_{1-x}Ge_x$ is deposited and patterned to serve as the active layer of the device. A Si implant with a dose of $2x10^{15}$ /cm^2 and with the implant peak at the center of the film is done to amorphize the film; subsequently, a 60-hour solid phase crystallization anneal is performed at 600°C in nitrogen (N_2) gas. Following channel definition, 1000Å of low-temperature oxide is deposited as the gate dielectric and 3000Å of polycrystalline silicon (poly-Si) is then deposited at 625°C as the gate electrode. Once the gate is defined, the source/drain/gate doping is achieved using a single self-aligned implant with a $2x10^{15}$ cm^{-2} dose of boron for p-type doping or phosphorus for n-type doping. Further, 3000Å of low-temperature oxide is deposited as the passivation layer, and dopant activation is performed in N_2 at 600°C. After the dopant activation, 1 μm of Al-1% Si is sputtered and patterned for use as electrical contacts. Finally, devices are sintered at 400°C in a N_2/H_2 mixture. The performance of devices is evaluated both before and after hydrogenation which is performed in a parallel-plate plasma reactor at 350°C.

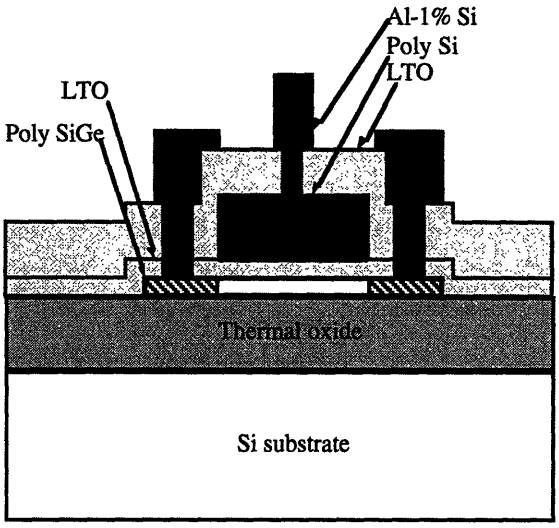
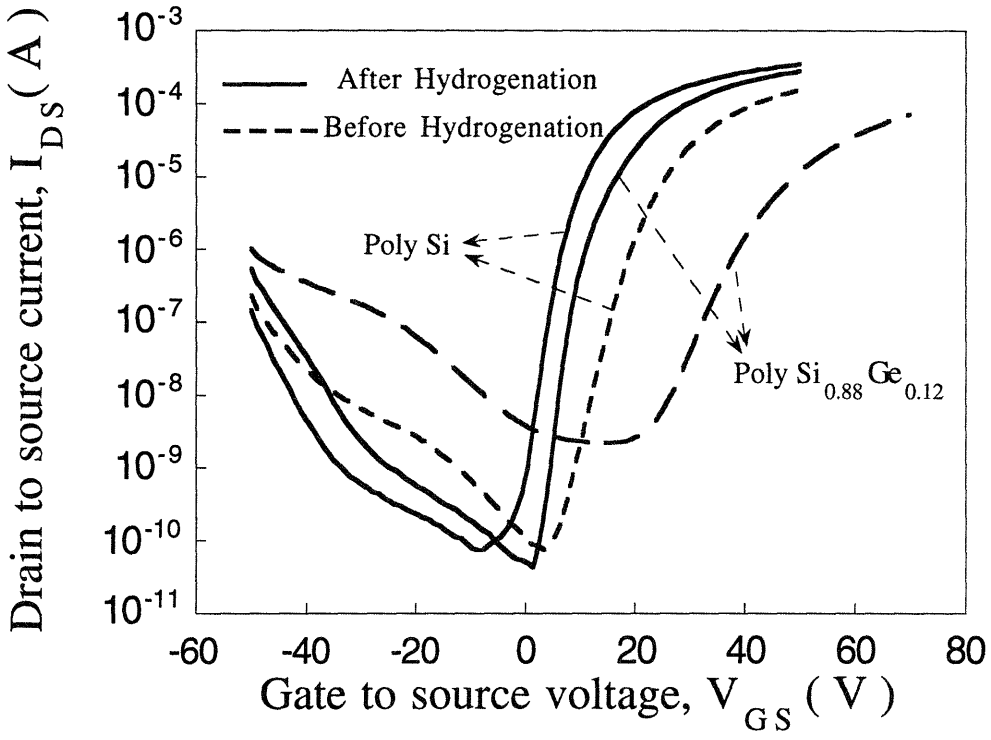


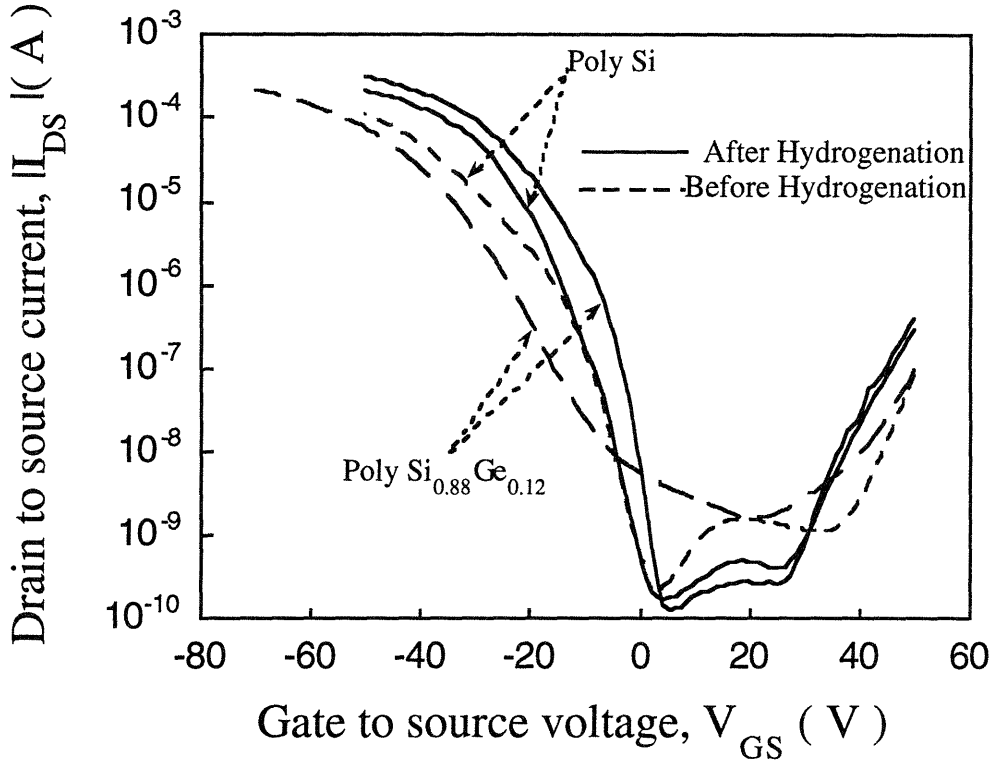
Figure 4.1. Structure of a top-gate TFT.

4.2 Results and discussion

Typical I_{DS} vs. V_{GS} transfer characteristics for poly-$Si_{1-x}Ge_x$ TFTs before and after hydrogenation are shown in Figure 4.2(a) for n-channel devices and in Figure 4.2(b) for p-channel devices. Device parameters such as effective field-effect mobilities (μ_{FE}), threshold voltages (V_{th}), subthreshold slopes, and leakage currents are derived and summarized in Table 4.1. μ_{FE} is measured at $|V_{DS}|= 0.1$ V while V_{th} is defined as the V_{GS} at which I_{DS} reaches 100 nA with $|V_{DS}| = 10$ V. Further, with $|V_{DS}|= 10$ V, the subthreshold slope is read from the I_{DS} vs. V_{GS} curve while the leakage current is defined as the minimum stable off-state current.


Drain to source current, I_{DS} (A)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
After Hydrogenation
Before Hydrogenation
Poly Si
Poly $Si_{0.88}$ $Ge_{0.12}$
-60
-40
-20
0
20
40
60
80
Gate to source voltage, V_{GS} (V)

(a)



(b)

Figure 4.2. Typical I_{DS} vs. V_{GS} transfer characteristics for devices with W=L=5 μm at $|V_{DS}|$=10 V. (a) n-channel; (b) p-channel.

Device Types	n-channel		p-channel	
TFT Channel Material	Si	$Si_{0.88}Ge_{0.12}$	Si	$Si_{0.88}Ge_{0.12}$
Field-Effect Mobility (cm2/V-Sec)	21	12	18	22
Threshold Voltage (V)	15	32	-9	-15
Subthreshold Slope (V/dec)	3.0	4.9	3.3	7.1
Leakage Current (pA)	100	1000	1000	1000

(a)

Device Types	n-channel		p-channel	
TFT Channel Material	Si	$Si_{0.88}Ge_{0.12}$	Si	$Si_{0.88}Ge_{0.12}$
Field-Effect Mobility (cm2/V-Sec)	29	28	26	35
Threshold Voltage (V)	4	8	-8	-3
Subthreshold Slope (V/dec)	1.8	1.6	2.9	1.8
Leakage Current (pA)	100	150	100	100

(b)

Table 4.1. Electrical characteristics for poly-$Si_{1-x}Ge_x$ and poly-Si TFTs with W=L=5 μm and $|V_{DS}|$=10 V. (a) before hydrogenation; (b) after hydrogenation.

From Table 4.1, post-hydrogenation improvement in μ_{FE} and V_{th} shows that the hydrogenation process is very efficient and essential for defect passivation in the poly-$Si_{0.88}Ge_{0.12}$ TFTs. As a result, higher μ_{FE}, lower threshold voltage, and steeper subthreshold swing were achieved after hydrogenation. Also from Table 4.1, poly-$Si_{0.88}Ge_{0.12}$ TFTs have comparable leakage currents as poly-Si devices despite the narrower bandgap of poly-$Si_{1-x}Ge_x$. This is because the leakage current arises from trap-to-band tunneling and thermionic emission [23], rather than band-to-band tunneling.

From Table 4.1, p-channel poly-$Si_{0.88}Ge_{0.12}$ devices have greater values of μ_{FE} than n-channel poly-$Si_{0.88}Ge_{0.12}$ devices. Although grain boundaries in poly-Si can trap either electrons or holes, grain boundaries in poly-$Si_{0.88}Ge_{0.12}$ are more efficient at trapping electrons than holes; this model is consistent with the reported behavior of poly-Ge grain boundaries which trap mainly electrons [24]. To further investigate the hole mobility of poly- $Si_{0.88}Ge_{0.12}$, we can look at the thermionic emission model. According to this model, I_{DS} in the linear region, where V_{DS} is small and the quadratic V_{DS} term is disregarded, can be expressed as:

$$I_{DS} = \mu_o \cdot C_i \cdot (W/L) \cdot (V_{GS} - V_{th}) \cdot V_{DS} \cdot e^{-(E_a/KT)} \tag{4.2.1}$$

and

$$\mu_{FE} = \mu_o \cdot e^{-(E_a/KT)} \tag{4.2.2}$$

where E_a is the activation energy, C_i is the gate capacitance, and μ_o is the intragranular carrier mobility [25]. For the determination of E_a, I_{DS} vs. V_{GS} curves were recorded at temperatures 30°C, 50°C, 75°C, and 100°C with $|V_{DS}|$=0.1 V. (4.2.1) is used to calculated E_a from the slope of the straight-line Arrhenius plot of log I_{DS} versus $1/kT$ for each V_{GS}. In figure 4.3, E_a is plotted as a function of V_{GS} for both poly-Si and poly-$Si_{0.88}Ge_{0.12}$. Despite the higher activation energy, μ_{FE} of p-channel poly-$Si_{0.88}Ge_{0.12}$ devices is enhanced over that of p-channel poly-Si devices by more than 30%, from Table 4.1. The higher intrinsic mobility values of poly-$Si_{0.88}Ge_{0.12}$ [18,19] can cause the overall μ_{FE} to be superior since (4.2.2) indicates that μ_{FE} depends on both intragranular mobility and activation energy.

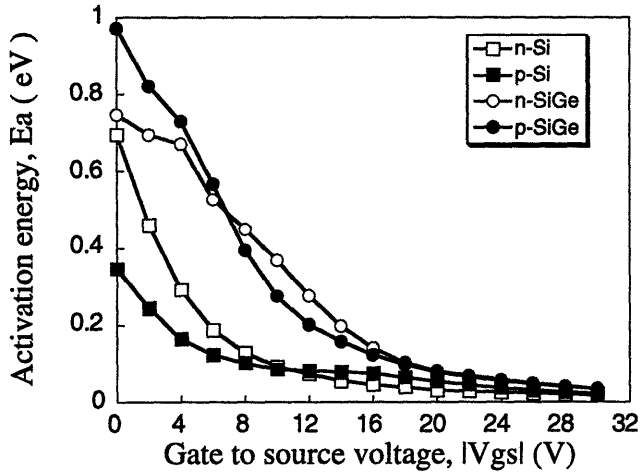


Figure 4.3 (a) E_a as a function of V_{GS} at $|V_{DS}|$=0.1 V for devices with W=L=5 μm.

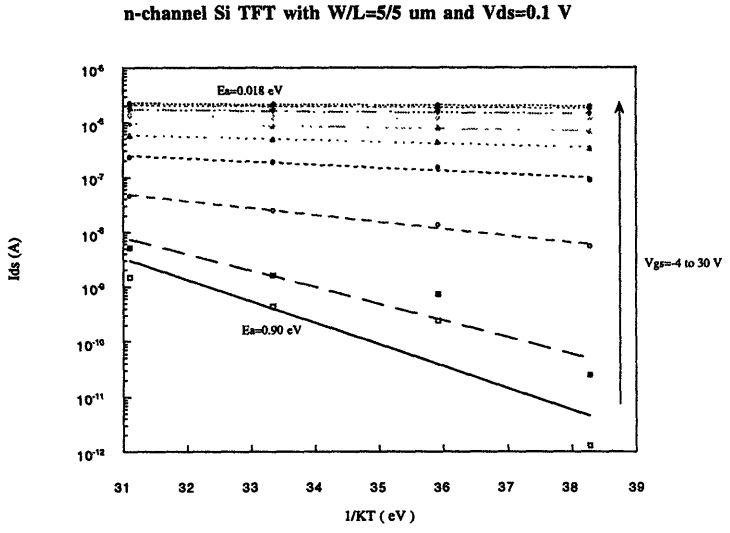


Figure 4.3 (b) Arrhenius plot of I_{DS} vs. $1/KT$ with $|V_{DS}|$=0.1V and n-channel poly-Si TFT W=L=5 μm at various V_{GS} for the determination of Ea.

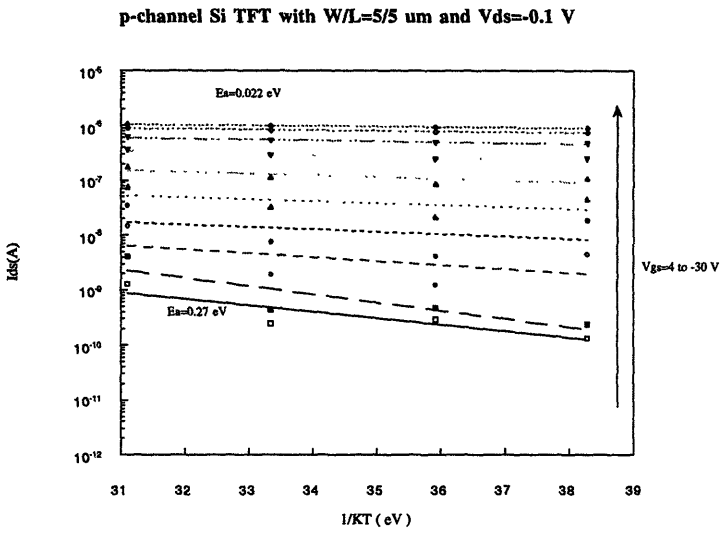


Figure 4.3 (c) Arrhenius plot of I_{DS} vs. $1/KT$ with $|V_{DS}|$=0.1V and p-channel poly-Si TFT W=L=5 μm at various V_{GS} for the determination of Ea.

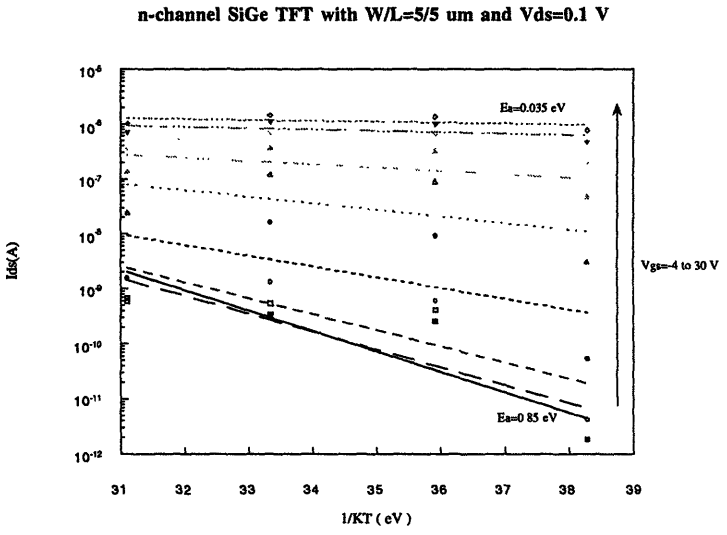


Figure 4.3 (d) Arrhenius plot of I_{DS} vs. $1/KT$ with $|V_{DS}|$=0.1V and n-channel poly-$Si_{0.88}Ge_{0.12}$ TFT W=L=5 μm at various V_{GS} for the determination of Ea.

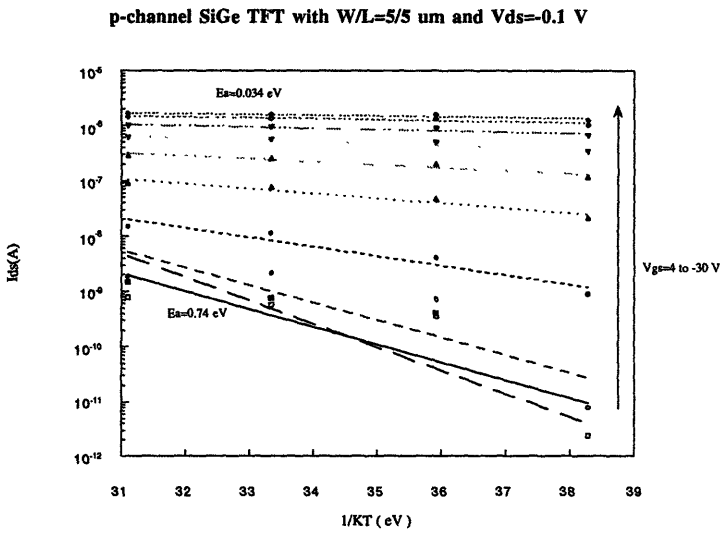


Figure 4.3 (e) Arrhenius plot of I_{DS} vs. $1/KT$ with $|V_{DS}|$=0.1V and n-channel poly-$Si_{0.88}Ge_{0.12}$ TFT W=L=5 μm at various V_{GS} for the determination of Ea.

Chapter 5

Poly-Si-Capped Poly-$Si_{1-x}Ge_x$ TFTs

5.1 Motivation

From Chapter 4, we have observed the higher performance of p-channel poly-$Si_{1-x}Ge_x$ TFTs relative to the poly-Si TFTs; however, both the n-channel poly-$Si_{1-x}Ge_x$ TFTs and the pre-hydrogenation p-channel poly-$Si_{1-x}Ge_x$ TFTs suffer from high V_{th} and high subthreshold swings. Although interface trap measurements were not done on poly-$Si_{1-x}Ge_x$ TFTs, poly-$Si_{1-x}Ge_x$ is known to have an inferior oxide interfacial quality as compared to poly-Si. As a result, we have proposed a poly-Si capped poly-$Si_{1-x}Ge_x$ TFT structure [26] to utilize both the good oxide interfacial quality of poly-Si and the superior field-effect mobility observed in the poly-$Si_{1-x}Ge_x$ TFTs.

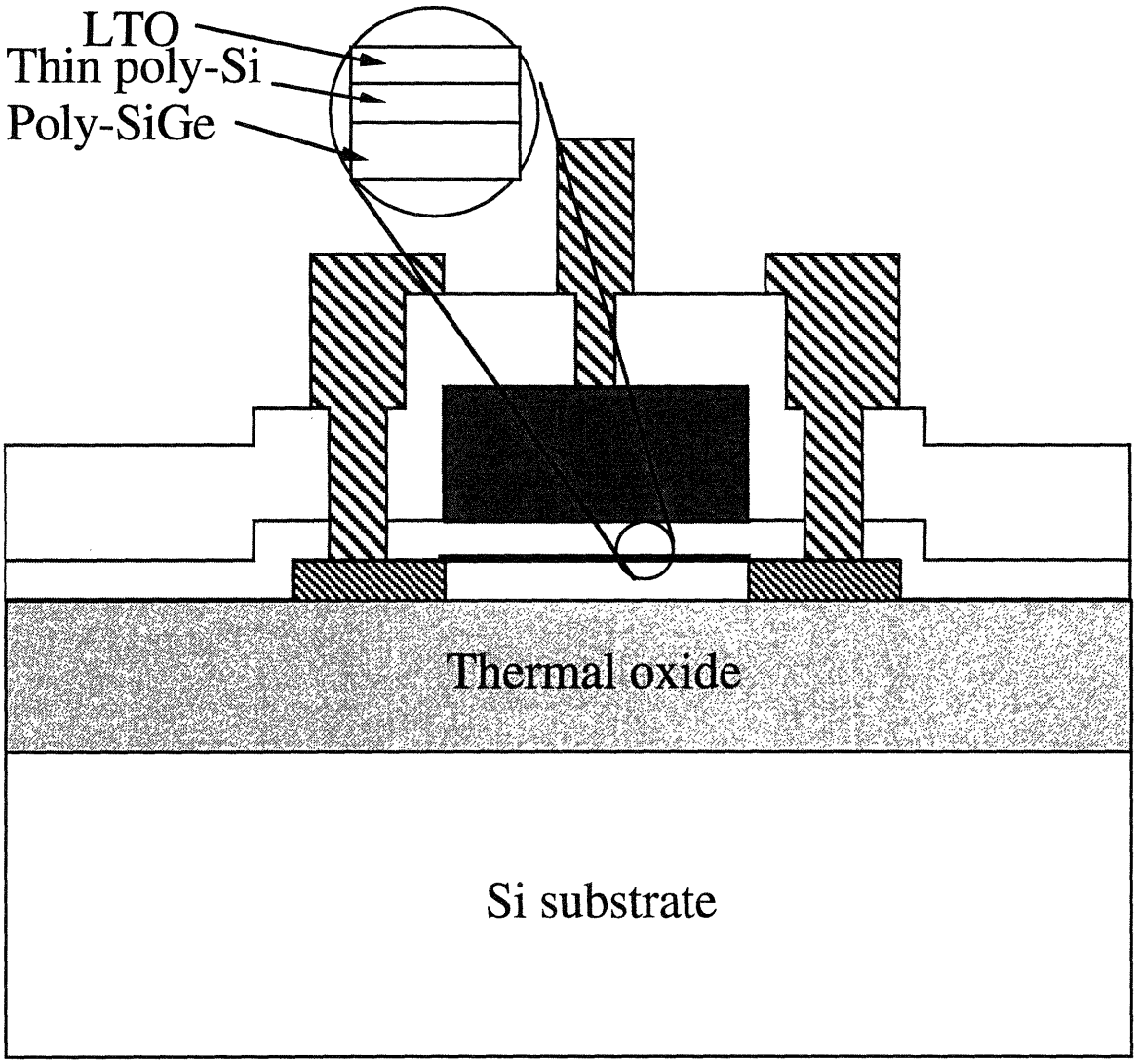


Figure 5.1 A modified TFT structure: Si-capped TFT

5.2 Experimental design and fabrication

We have designed four different TFT processes in addition to one control process (see Appendix D), as built in TFT2. This experiment involves the use of RTA, RTO, poly-Si cap, and the use of thermal oxide as the ultimate TFT performance limit. A few parameters among all splits are fixed to simplify the experiment, and these parameters are: 5000Å isolation oxide, 1000Å active layer, 250Å gate dielectric, 3000Å poly-Si gate, S/D annealing in N_2 at 600°C for 60 hours for n-channel and 2 hours for p-channel devices.

For the control TFTs, the process outline is identical to TFT2 (see Chapter 4). For the Si-cap split, the active layer has been modified to a sandwich structure of 30Å poly-Si on poly-$Si_{1-x}Ge_x$ to utilize poly-Si/oxide interface. For the RTA split, the process is modified from the Si-cap split by adding an extra RTA in N_2 for 30 sec at 1000°C following the SPC. Next, for the RTO split, the process is further modified from the RTA split by adding ,after the gate LTO deposition, a RTA step in O_2 ambient at 1000°C for 15 sec. Finally, to observe the ultimate performance ceiling of poly TFTs, the thermal split employs a 250Å thermal oxide grown on the 140Å poly-Si/ poly-$Si_{1-x}Ge_x$ active layer at 1000°C. The process and structure experimental split is summarized in Table 5.2. The thermal oxide thickness is calculated from poly-Si consumption on the test wafers.

steps/split	control	Si-cap	RTA	RTO	Thermal
Active layer	Poly-$Si_{1-x}Ge_x$	30Å poly-Si/ poly-$Si_{1-x}Ge_x$	30Å poly-Si/ poly-$Si_{1-x}Ge_x$	30Å poly-Si/ poly-$Si_{1-x}Ge_x$	140Å poly-Si/ poly-$Si_{1-x}Ge_x$
Crystallization	SPC	SPC	SPC+RTA	SPC+RTA	SPC
oxide formation	LTO	LTO	LTO	LTO	250Å at 1000°C
LTO densification	O_2 and N_2 at 600°C	O_2 and N_2 at 600°C	O_2 and N_2 at 600°C	O_2 and N_2 at 600°C	None
interface annealing	None	None	None	1000°C in O_2 for 15 sec	None
Remaining processes	Same as TFT2 from Chapter 4	Same as TFT2 from Chapter 4	Same as TFT2 from Chapter 4	Same as TFT2 from Chapter 4	Same as TFT2 from Chapter 4

Table 5.1 Experimental split chart of TFT3

5.3 Measured TFT results before hydrogenation

Device parameters such as effective field-effect mobilities (μ_{FE}), threshold voltages (V_{th}), subthreshold slopes, and leakage currents are derived and summarized in Table 5.2. μ_{FE} is measured at $|V_{DS}|$= 0.1 V while V_{th} is defined as the V_{GS} at which I_{DS} reaches 100 nA with $|V_{DS}|$ = 3 V. Further, with $|V_{DS}|$= 3 V, the subthreshold slope is read from the I_{DS} vs. V_{GS} curve while the leakage current is defined as the minimum stable off-state current.

	PE-CVD 0%	PE-CVD 0%	PE-CVD 10%	PE-CVD 10%	LP-CVD 0%	LP-CVD 0%	LP-CVD 10%	LP-CVD 10%	LP-CVD 0%	LP-CVD 0%
split: Control										
wafer	t13	t13	t14	t14	ss3	ss3	ss13	ss13	m2	m2
Device type	n	p	n	p	n	p	n	p	n	p
FE mobility (cm2/V-S)	6.57	3.98	3.14	3.04	52.43	23.46	3.16	7.20	25	20.19
SS (V/dec)	0.63	0.56	0.89	1.50	0.56	0.50	1.30	1.25	0.23	0.60
Threshold Voltage (V)	2	-3	4.5	-4	0.5	-1.5	6	-3.5	0	-2
Leakage current (e-10 A)	5	5	5	7	50	50	10	10	5	7
split: Si cap										
wafer			t19	t19	ss1	ss1	ss11	ss11		
Device type			n	p	n	p	n	p		
FE mobility (cm2/V-S)			11.61	6.72	17.65	15.78	2.06	5.32		
SS (V/dec)			NA	1.70	0.64	0.75	1.50	2.00		
Threshold Voltage (V)			NA	-2.5	2	-3.5	6	-0.5		
Leakage current (e-10 A)			100000	50	5	5	50	100		
split: RTA										
wafer	t15	t15	t16	t16	ss2	ss2	ss12	ss12	m5	m5
Device type	n	p	n	p	n	p	n	p	n	p
FE mobility (cm2/V-S)	27.29	18.43	scrap	scrap	42.26	23.59	0.75	1.52	35.31	40.68
SS (V/dec)	0.31	0.33			0.50	0.50	1.40	2.40	0.38	1.10
Threshold Voltage (V)	-0.4	-1.25			0	-2.5	7.5	-4	0.5	1
Leakage current (e-10 A)	7	2			10	2	50	10	10	100

split: RTO										
wafer	t17	t17	t18	t18			ss21	ss21	m7	m7
Device type	n	p	n	p			scrap	scrap	n	p
FE mobility (cm2/V-S)	27.73	18.61	1.21	3.07					28.11	46.77
SS (V/dec)	0.83	0.64	1.10	2.10					0.38	0.47
Threshold Voltage (V)	-1.5	-0.5	7	0					0	-2
Leakage current (e-10 A)	5	12	1000	100					10	8
split Thermal										
wafer	t20	t20	t21	t21			ss22	ss22	m9	m9
Device type	n	p	n	p			scrap	scrap	n	p
FE mobility (cm2/V-S)	42.50	32.17	41.25	21.35					78.52	39.60
SS (V/dec)	0.31	0.33	0.47	1.25					0.29	0.38
Threshold Voltage (V)	-0.3	-1.5	2.5	-0.6					0	-0.5
Leakage current (e-10 A)	5	2	8	50					5	8

Table 5.2 Measured TFT performance before hydrogenation for L=W=0.5 μm devices

	PE-CVD 0%	PE-CVD 0%	PE-CVD 10%	PE-CVD 10%	LP-CVD 0%	LP-CVD 0%	LP-CVD 10%	LP-CVD 10%	LP-CVD 0%	LP-CVD 0%
Split: control										
wafer	t13	t13	t14	t14	ss3	ss3	ss13	ss13	m2	m2
Device type	n	p	n	p	n	p	n	p	n	p
FE mobility (cm2/V-S)	16.58	8.08	4.06	1.80						
SS (V/dec)	0.55	0.70	0.88	0.85						
Threshold Voltage (V)	2	-3.5	4.5	-3.3						
Leakage current (e-10 A)	2	2	2	10						
split: Si cap										
wafer			t19	t19	ss1	ss1	ss11	ss11		
Device type			n	p	n	p	n	p		
FE mobility (cm2/V-S)			16.4	3.6						
SS (V/dec)			0.35	1.70						
Threshold Voltage (V)			~4	-5						
Leakage current (e-10 A)			5 to 10	10						

Table 5.3 Measured TFT performance before hydrogenation for L=W=0.75 μm devices

n-channel	t13	t14	t19	t20	t21
mobility	10	9	NA	45	41
leakage	10	40	NA	20	40
V_{th}	2.1	6.3	NA	0.2	2.9
SS	.46	.95	NA	.43	.51

Table 5.4a Measured poly-Si-capped poly-$Si_{0.9}Ge_{0.1}$ TFT with thermal oxide performance after 4 hours of hydrogenation for L=W=3 μm n-channel devices.

p-channel	t13	t14	t19	t20	t21
mobility	10	9	1.5	27	51
leakage	7	20	20	20	40
V_{th}	-3.5	-5.1	-5	-2.1	-2.7
SS	.38	.91	.54	.38	.63

Table 5.4b Measured poly-Si-capped poly-$Si_{0.9}Ge_{0.1}$ TFT with thermal oxide performance after 4 hours of hydrogenation for L=W=3 μm p-channel devices.

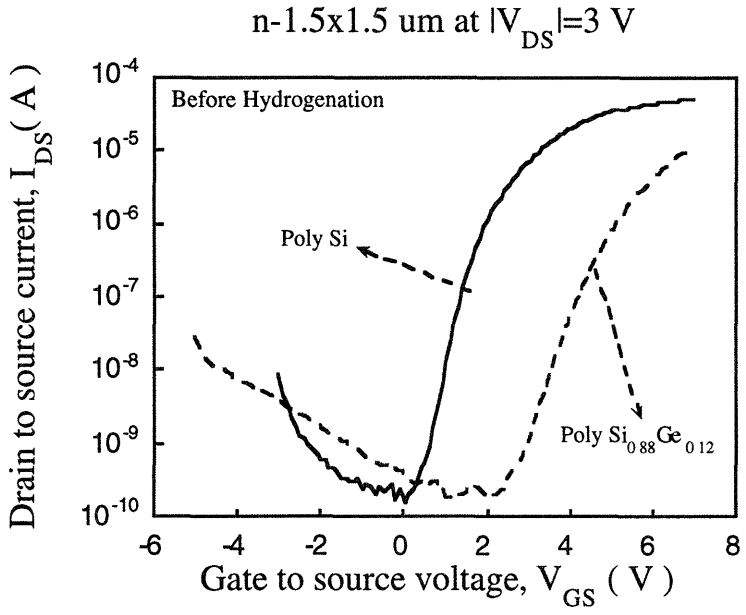


Figure 5.2a Pre-hydrogenation I-V characteristics for poly-Si-capped poly-$Si_{1-x}Ge_x$ TFTs with thermal oxide .

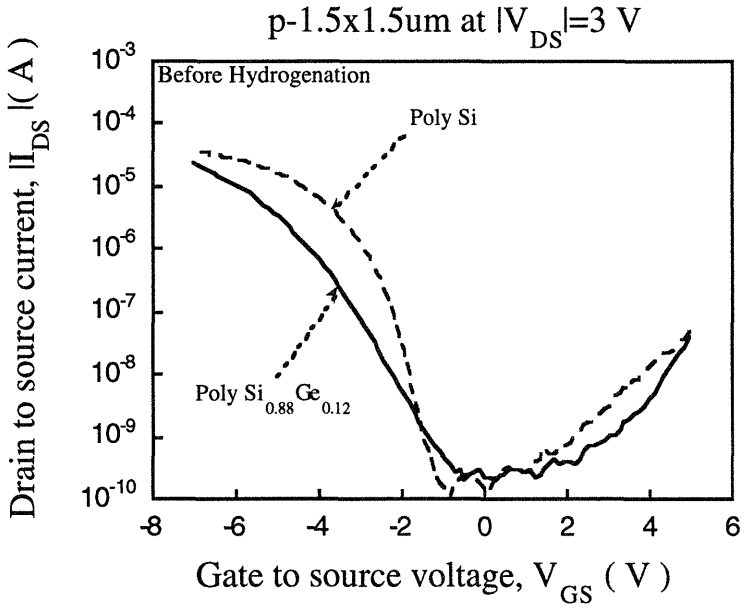


Figure 5.2b Pre-hydrogenation I-V characteristics for poly-Si-capped poly-$Si_{1-x}Ge_x$ TFTs with thermal oxide .

From Fig. 5.2 and Table 5.3, the performance of poly-Si-capped poly-$Si_{1-x}Ge_x$ TFTs is not as good as anticipated, but the slightly inferior device characteristics are due to the rather high threshold voltage. It is very possible that, if these devices are hydrogenated for a longer duration, the threshold voltage will allow the observation higher field-effect mobility.

From Table 5.4, the thermal oxide split yields the best poly-$Si_{1-x}Ge_x$ device performance. Similar to the findings from TFT2, hole mobility in poly-$Si_{1-x}Ge_x$ TFTs are much higher than the poly-Si counterpart; in fact, poly-$Si_{1-x}Ge_x$ TFTs with thermal oxide have almost a two-fold increase from the poly-Si TFTs while the low-temperature processed poly-$Si_{1-x}Ge_x$ TFTs have a 30% improvement from the conventional poly-Si TFTs (See Chapter 4). Poly-$Si_{1-x}Ge_x$ TFTs with thermal oxide show the immense potential of poly-$Si_{1-x}Ge_x$ as a possible replacement for poly-Si.

Chapter 6

Conclusions and Future Work

Poly-$Si_{1-x}Ge_x$ TFTs were designed and fabricated in a self-aligned 0.8μm CMOS line. Film deposition, grain-enhancement techniques, gate dielectric choice, and dopant activation were optimized for poly-$Si_{0.88}Ge_{0.12}$ TFTs.

The major contribution of this project to the polycrystalline material TFT research can be summarized by the results of high-temperature (≤ 1000°C) processed and low-temperature (≤ 625°C) processed TFTs. High-temperature processed poly-Si-capped poly-$Si_{0.9}Ge_{0.1}$ TFTs with thermal oxide were found to have the highest mobility reported-to-date, for poly-$Si_{1-x}Ge_x$, of 51 cm^2/V-sec for p-channel devices and 41 cm^2/V-sec for n-channel devices. This is compared to the hole mobility of 27 cm^2/V-sec and the electron mobility of 45 cm^2/V-sec for similarly processed poly-Si TFTs. Low-temperature processed poly-$Si_{0.88}Ge_{0.12}$ TFTs were also measured to have the highest mobility reported-to-date, for poly-$Si_{1-x}Ge_x$, of 35 cm^2/V-sec for hole and 28 cm^2/V-sec for electrons. It is compared to the hole mobility of 26 cm^2/V-sec and the electron mobility of 29 cm^2/V-sec for similarly processed poly-Si TFTs.

A successful research area usually has two major components that benefit and support each other: the experimental team and the theoretical counterpart. In the context of poly-$Si_{1-x}Ge_x$ TFT research, there is still room for improvement in the experimental research. The two most important areas are device design and defect passivation. The single most important criterion for a new poly-$Si_{1-x}Ge_x$ TFT is the requirement of the performance of the new device not dependent on the quality of the poly-$Si_{1-x}Ge_x$ /oxide interface; otherwise, means of passivating the poly-$Si_{1-x}Ge_x$/oxide interface must be fully optimized. Further, defect passivations (intragranular traps, grain-boundary traps, and interfacial traps) in poly-$Si_{1-x}Ge_x$ TFT need to be fully optimized. RTA should be further investigated for intragranular defect passivation; on the other hand, RTO is likely to improve the interfacial quality of TFTs. Finally, plasma hydrogenation remains the most effective passivation method for all three types of defects. Therefore, a combination of the three should be used depending on the situation.

In terms of theoretical work of poly-$Si_{1-x}Ge_x$ TFTs, little has been done as of today; therefore, more effort should be focused on the fundamental or theoretical device improvement ceiling when Ge is alloyed with poly-Si. Also, models (e.g. MEDICI) should be developed to fit the device characteristics that have already been fabricated previously [18-20]. Finally, as mentioned in the previous paragraph, passivation is very important in poly-$Si_{1-x}Ge_x$ TFTs, so hydrogenation as well as the fundamental materials properties of poly-$Si_{1-x}Ge_x$:H must be modeled and checked with existing experimental results [18-20]. With a balance in theoretical and experimental work, poly-$Si_{1-x}Ge_x$ TFT research will continue the kind of rapid growth that has been achieved in the past five years.

APPENDICES

Appendix A

LTO capacitor experiment

Process Traveler

---

0. starting materials

diameter 99.5/100.5
Rho 10/20
Thickness 500/550
orientation 100
type P - boron
lot number MEMC 541193

---

1. RCA

---

2. LTO 1000A
   Tube A7
   RECIPE#436

---

3. Densification@600 N2
   12 hours
   24 hours
   36 hours

---

4. Gate poly 3500A
   Tube A6
   Recipe# 428
   modified dep time from 31 to 36.5

---

5. Implant
   B 1e15 @65

---

6. Pattern

---

7 BOE
Poly etch: Etcher 1
recip 10
oxide etch: Etcher2
recipe 23

---

8. asher

---

9. 2nd implant (SD implant)

2 splits:
B 2e15 @30 or B 2e15 @65
double implant 65/30

---

10. Implant Anneal
600C in nitrogen in B2 TRL
0.5 hours or 2 hours

---

11. Testing
Resistivity of
gate electrode

Breakdown voltage
of oxide

---

end of process

Appendix B

Hall-Effect Structures

Process Traveler

---

1 PRELIMINARY

1a p-type Si substrates (10-20 ohm-cm)

1b RCA Clean (ICL)

1c 1K Oxide Growth (ICL)
rec. 100, Tube A2

or

5K Oxide Growth (ICL)
rec. , Tube B2

---

2 FILM DEPOSITION: 1000A Si or SiGe

2a RCA Clean and HF dip procedure (TRL)

2b Si or SiGe film deposition using PE-VLPCVD
(TRL group equipment)

---

3 SOLID-PHASE CRYSTALLIZATION ANNEAL

3a RCA Clean (TRL) (short)

3b Anneal in N2 (80% flow) at 600C (TRL) for 65 hours
Manual recipe, Tube B2

---

4 IMPLANT FILMS FOR CONDUCTIVITY

4A Pattern films for 1st 1/4-wafer splits (TRL)

4Ab-n Film Implantation I (ICL)

Implant	Element	P
	Dose	1e12 cm-2
	Energy	55 KeV (aim peak >mid film)

4Ab-p Film Implantation I (ICL) Wafers:

Implant	Element	B
	Dose	1e12 cm-2
	Energy	30 KeV (aim peak >mid film)

4Ac Strip Resist

4Ba Pattern films for 2nd 1/4-wafer splits (TRL)

4Bb-n Film Implantation II (ICL)

Implant	Element	P
	Dose	1e13 cm-2
	Energy	55 KeV (aim peak at mid film)

4Bb-p Film Implantation II (ICL)

Implant	Element	B
	Dose	1e13 cm-2
	Energy	30 KeV (aim peak at mid film)

4Bc Strip Resist

4Ca Pattern films for 3rd 1/4-wafer splits (TRL)

4Cb-n Film Implantation III (ICL)

Implant	Element	P

	Dose	1e14 cm-2
	Energy	55 KeV (aim peak at mid film)

4Cb-p Film Implantation III (ICL)

Implant	Element	B
	Dose	1e14 cm-2
	Energy	30 KeV (aim peak at mid film)

4Cc Strip Resist

4Da Pattern films for 4th 1/4-wafer splits (TRL)

4Db-n Film Implantation I (ICL)

Implant	Element	P
	Dose	1e15 cm-2
	Energy	55 KeV (aim peak at mid film)

4Db-p Film Implantation I (ICL)

Implant	Element	B
	Dose	1e15 cm-2
	Energy	30 KeV (aim peak at mid film)

4Dc Strip Resist

---

5 DOPANT ACTIVATION ANNEALING

5a RCA Clean (TRL) (short)

5b-n Anneal in N2 (80% flow) at 600C (TRL)
Manual recipe, Tube B2
30 hours, P-doped wafers

5b-p Anneal in N2 (80% flow) at 600C (TRL)
Manual recipe, Tube B2
3 hours, B-doped wafers

---

6 CROSS-SHAPED MESA FORMATION

6a Pattern cross-shaped Hall structures (TRL)

6b Plasma etch poly-SiGe film (ICL)

Acid Used	7:1 BOE	
Etch Time	1 min. 0 sec	0 hrs 20 min.
Etcher #	1	
Recipe #	10	

6c Strip Resist

---

7 DIELECTRIC DEPOSITION AND CONTACT PATTERNING

7a LTO deposition
3K
Recipe # 976
Tube A7

7b Contact Hole Pattern (TRL)

7c Contact Hole Plasma Etch

Etcher #	2
Recipe #	24
BOE	1.5 minutes

7d-n Ohmic Contact Implantation (ICL)

	Implant	Element	P
		Dose	2e15 cm-2
		Energy	55 KeV

7d-p Ohmic Contact Implantation (ICL)

	Implant	Element	B
		Dose	2e15 cm-2
		Energy	30 KeV

7c Strip Resist

7d Contact Implant Annealing

7d-n Anneal in N2 (80% flow) at 600C (TRL)
Manual recipe, Tube B2

7d-p Anneal in N2 (80% flow) at 600C (TRL)
Manual recipe, Tube B2
2 hours, B-doped wafers

7d-RTA Anneal in N2, 900C, 30 sec.

---

8 METAL

8a (Varian sputterer, 1um)
1um Al-1%Si Metal Deposition

8b Pattern Al metal pads (TRL)
(3" dark-field contact mask;
requires image reversal process)

8c Plasma etch Al metal (ICL)
Etcher-3
Recipe32

8d Strip Resist

8e Al sintering at 400C (ICL)

---

9 HALL MEASUREMENT

Appendix C

TFT2

Process Traveler

Film deposition

---

p-type Si substrates (0.5-2 ohm-cm)

RCA

1K Oxide Growth

Amorphous SiGe deposition	LPCVD deposition
Machine Julie's reactor	Machine Stanford

RCA

SPC
annealing 55 hours @590 to 600 C in 80% N2
Tube B2

Poly-Si Active Area Pattern (mask ND)

Island etch
Hardbake
BOE
Poly etch

Etcher 1
Recipe 10

PR ashing
asher twice

Inspection
nano spec
island thickness:
oxide thickness

RCA: pre-gate cleaning

Gate oxide deposition

Recipe 436, 25 min.
1000A gate LTO (ICL)
Tube A7
Recipe 436
oxide thickness on poly

Gate Poly deposition
Recipe. 428
3K LPCVD Poly-Si
Tube A6

Gate Patterning

Gate etch
Pre-Etch BOE 5 sec
Poly Etch
Etcher 1
Recipe 10

PR ashing

RCA -

LTO annealing

SD implant block
stepper rows 1,3,5,7 open up for implant,

SD IMPLANT (1)

N+ implant P 2e15

PR ashing

Asher/piranha

RCA
2 hrs

LTO densification, and Phosphorus activation
60 hours , N2, 600 C, TRL B2

SD implant block
stepper rows 2,4,6,8 open for implant

SD IMPLANT2

P+ implant boron 2e15@45

PR ashing

RCA

LTO passivation
3K LTO deposition
Tube A7
Recipe: 976

SD annealing
3 hrs, TRL B2, 80% N2
600C to be decided

Contact Hole Pattern (mask NC)

Contact LTO etching
Etcher2
Recipe24
30 sec BOE

---

30 sec BOE wet etch for contact holes

PR ashing

---

pre-metal clean

Al deposition
1um Al-1%Si Metal Deposition

Metal Pattern
Metal Pattern (mask NM)

Hardbake

Metal Etch
Etcher 3
Recipe 32

PR ashing

Sintering
Tube B8
recipe 710

Device complete
measurement

Hydrogenation done at the Xerox PARC by Dr. Tsu-Jae King

Appendix D

TFT3

Process traveler

---

p-type Si substrates (0.5-2 ohm-cm)

RCA

5K Oxide Growth

FILM DEPOSITION

Amorphous SiGe deposition	LPCVD deposition
Machine Julie's reactor	Machine Stanford

RCA

Si cap

split 1
1:00 dep

split 2
1:30 dep (about 250A? by nanospec)

Si implant 2e15 @40 KeV

only LPCVD wafers

RCA (5/10/10)

SPC

Annealing 65 hours @590 to 600 C in 80% N2
Machine TRL B2

Wafer split
RTA (30 sec @ 1000C)

Poly-Si Active Area Pattern (mask ND)

Island etch
BOE 15 sec
Poly etch
Etcher 1
Recipe 10

PR ashing

Active layer island dek tak measurement

RCA (5/10/10)

Gate oxide deposition

**********Split one**********
~200A gate dry ox
Tube b5
Recipe 221 for 5 min. @1000C , projected at 230A
Oxide thickness measured on poly dummies:

**********Split two**********
270A gate LTO done at Lincoln Lab by Bob Mountain
Tube C1, temp=320C , time=2:00 , RECIPE=C1_LTOnd.9

LTO annealing

SPLIT ONE
****
RCA
8 hrs in oxygen
16 hr. in nitrogen

SPLIT TWO
****

RTA in oxygen
15 sec in oxygen @ 1000C

RCA

Gate Poly deposition
Recipe. 428
3K LPCVD Poly-Si (gate material)
Tube A6

Gate Patterning
Poly-Si Pattern (mask NP)

Gate etch
BOE 5 sec
Poly Etch
Etcher 1
Recipe 10

PR ashing

SD implant block
wafers: all
stepper rows 1,3,5,7 open up for implant,

SD IMPLANT (1)
N+ implant P 2e15 @ 75 KeV

PR ashing

RCA

Phosphorus activation
60 hours , N2, 600 C, TRL B2

SD implant block
stepper rows 2,4,6,8 open for implant

SD IMPLANT2
P+ implant boron 2e15@45

PR ashing

RCA
2/0/5

Boron annealing
TRL B2, 80% N2

SD implant anneal
600C to be decided

RCA

LTO passivation
3K LTO deposition
Tube A7
Recipe: 976

Contact Pattern
Contact Hole Pattern (mask NC)

Contact LTO etching
Etcher2
Recipe24

---

40 sec BOE wet etch for contact holes

PR ashing

Pre-metal clean

Al deposition
1um Al-1%Si Metal Deposition

Metal Pattern
Metal Pattern (mask NM)

Hardbake

Metal Etch
Etcher 3
Recipe 32 (timed etch 1:20 plus 65% OE)

PR ashing

Sintering
Tube B8
recipe 710

Device complete
measurement

Plasma Hydrogenation done at the Xerox PARC by Dr. Tsu-Jae King

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