HOT-CARRIER RELIABILITY EVALUATION FOR CMOS DEVICES AND CIRCUITS

by

VEI-HAN CHAN

B.S. Elec. Eng., National Taiwan University (1986)

S.M. Elec. Eng., Massachusetts Institute of Technology (1991)

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy in Electrical Engineering

at the

Massachusetts Institute of Technology, February 1995

Signature of Author _____

Department of Electrical Engineering and Computer Science

Jan. 20, 1995

Certified by _____

James E. Chung, Thesis Supervisor

Assistant Professor of Electrical Engineering

Accepted by _____

Frederic R. Morgenthaler

Chairman, Committee on Graduate Students

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ABSTRACT

As CMOS scaling continues, the traditional DC device-level hot-carrier reliability criteria becomes difficult to meet for newer generations of technology. In order to satisfy hot-carrier reliability requirements by using AC circuit-level criteria, issues of AC device degradation under circuit operation and impact of device degradation on circuit performance need to be examined.

In order to satisfy the wide range of bias conditions in AC circuit environments, NMOSFET hot-carrier degradation models are investigated in detail. Accurate calibration of these models to a particular technology is shown to require accounting for the asymptotic and variable power-law time dependence of hot-carrier degradation associated with the LDD structure, and the impact of the local oxide electric field on the critical energy for interface damage. In addition, statistical analysis is used to determine the prediction intervals within which hot-carrier lifetime can be estimated, and to offer insight into developing more efficient and precise testing methodologies.

Evaluation of hot-carrier degradation for basic digital and analog subcircuits is conducted with experimental verification using circuit test structures. The AC device degradation mechanisms due to hot carriers are studied under high-frequency digital circuit operation. Two new degradation phenomena are observed at these high frequencies. First, voltage overshoot, due to internal MOSFET parasitic capacitances, causes enhanced hot-carrier degradation. Second, the quasi-static approximation is found to be invalid at high frequencies. For NMOSFETs, fast voltage transitions are found to induce different degradation dynamics; for PMOSFETs, donor-type interface-state generation and electron detrapping both become significant.

The impact of NMOSFET hot-carrier-induced degradation on CMOS analog subcircuit performance is evaluated. Because of circuit design requirements, most NMOSFETs used for analog applications are biased in the saturation region with a low gate-to-source voltage. Under such operating conditions, hole trapping is the dominant

mechanism to affect analog NMOSFET device performance. The hot-carrier-induced degradation of analog subcircuit performance is also found to be quite sensitive to the particular circuit design and operating conditions. Circuit performance and reliability tradeoffs are examined.

Thesis Supervisor: Dr. James E. Chung

Title: Assistant Professor of Electrical Engineering

Acknowledgements

I would like to express my gratitude to Prof. James E. Chung, my thesis advisor. He has worked hard and provided leadership to establish this research program. He not only gave me important guidance, but also allowed me to explore various approaches and topics freely during various stages of this project. This thesis will not be completed without his enthusiasm and encouragement along the way.

I am indebted to Prof. Dimitri Antoniadias and Prof. Hae-Sung Lee to spend their valuable time in serving in my thesis committee and reviewing my manuscript. Prof. Syh-Chern Lee of National Taiwan University and Prof. Jason Woo of UCLA who led me into the interesting area of solid-state electronics and CMOS device physics are appreciated greatly. Thanks go also to Prof. Terry P. Orlando who provided me an opportunity to work with him as a teaching assistant. This experience broadened my education at M.I.T..

Industrial collaborations are important elements of this research projects. I am grateful to Dr. Brad Scharf and Mr. Mike Delaus of Analog Devices, Inc., Mr. Thomas Kopley, Mr. Paul Marcoux, and Dr. Wayne Green of Hewlett-Packard Company, Dr. Shyh-Chyi Wang, Mr. Chia-Shine Chen, and Mr. Shun-Liang Hsu of Taiwan Semiconductor Manufacturing Company, and Chung-Lin Liang of INTEL Corp.. They have provided great help on this project.

I owes my appreciation toward several students - David Yuan, Eric Shen, Jeff Kim, and Huy Le who have worked with me during various periods of this research. I am grateful to Dr. Hwa-Fang Wei, Dr. Quan Xiong, Dr. Hao Fang and other group members who maintain a stimulating and yet comfortable environment for me to work. I also would like to thank my close friends at Microsystems Technology Laboratories - Dr. Lung-Han Peng, Dr. Zhen-Hong Zhou, Dr. Syun-Ming Jang, Ken Liao, Paul Yu, and Charles Hsu who make my M.I.T. experience more pleasant and enjoyable.

Finally, without the constant support of my parents and my wife - Chia-Lin Wang during my study at M.I.T., I would not be able to finish this thesis. I thank for their patience and love.

This research project has been supported by Advanced Research Projects Agency and National Science Foundation.

Biography

Vei-Han Chan was born on 28th of November, 1964 in Taipei, Taiwan, Republic of China. He earned his bachelor of Science degree from the Department of Electrical Engineering at National Taiwan University in 1986. After graduation, he joined the ROC Navy. From 1986 to 1988, he served as an ensign in Chinese Naval Weapon School in Kaohsiung, Taiwan to work on ship-based fire control systems. Before coming to M.I.T., he studied at Univ. of California, Los Angeles for one years.

His research interest is in solid-state applications. For his master degree, he has studied the interaction between transition-metal ions and crystal fields based on tetrahedral sites as potential near infrared tunable solid-state laser applications. Since 1991, he has worked as a research assistant in Microsystems Technology Laboratories at M.I.T.. His doctoral work focuses on examination of hot-carrier degradation in CMOS devices and circuits.

On his spare time, he enjoys travel, camping, and family life.

To My Family

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Chapter 1

Introduction

The rapid growth of the semiconductor industry for the past two decades has been propelled by the continuation of CMOS device scaling. The shrinking of devices has provided more current-carrying capabilities per device width, less power consumption per device, and higher device density per area. The rising cost of fabrication has been compensated by the use of a large wafer size and a continuation of yield improvement.

Historical trends have indicated that a new generation of technology has been developed every three years. For every two generations, the device size has been reduced half and the speed of the device operation has increased twice. Through continuing innovation, the advance of technology does not show any slowdown. It is projected that before the end of this decade, 0.25μm technology will go into production and yield DRAM circuits with 256Mb capacities and microprocessors operating in the +500MHz range.

However, the continuation of device scaling is not without some technology constraints [1.1]: short-channel lengths have induced short-channel effects (V_T roll-off and drain-source punch-through); high electric field in the device has produced impact ionization (hot carriers), gate-induced drain leakage (GIDL), and oxide dielectric breakdown; higher current density has created electromigration in both interconnects and vias. These performance and reliability issues must be addressed before the scaling of CMOS devices is able to continue.

This thesis will address the issues of hot-carrier degradation. The device degradation and the impact on the performance of circuits will be evaluated in detail.

1.1. Review of Hot-Carrier Degradation

As CMOS device scaling continues without adjusting the power-supply voltage proportionally, hot-carrier degradation presents a major problem for long-term device reliability. When devices are operated in the saturation region, a large lateral electric field is created in the pinch-off region. This large electric field accelerates charged carriers and subsequently induces impact ionization. The resulting hot electrons and holes, when possessing enough energy to overcome the oxide energy barrier, can inject themselves into the oxide area and damage the gate oxide by creating either interface states or oxide traps. The hot-carrier-induced damage is able to change the device characteristics and, as a result, degrade circuit operations [1.2], [1.3].

In this section, the current NMOSFET and PMOSFET transistor DC degradation models and their application to hot-carrier circuit reliability simulation will be reviewed.

1.1.1. NMOSFET Device Degradation

There are three different hot-carrier degradation mechanisms for NMOSFETs. Each occurs during different voltage stress regions. For the low gate-voltage stress ($V_G \sim V_T$, peak gate hole-current region), device I-V characteristics are affected by hole traps generated inside the oxide [1.4]. The positive trapped charge lowers the local threshold voltage near the drain. Thus, the channel portion below the trapped holes, which will be turned on earlier than other parts of the channel, acts as an extension of the drain. This "channel shortening" effects will increase the drain current [1.5]. Currently, the degradation model of hole traps has not yet been developed due to the common belief of its limited influence on the performance of digital circuits. However, it remains to be

determined whether it will affect the device performance in CMOS analog circuits [1.3].

Neutral electron traps are also generated during this low gate-voltage stress [1.4]. They can be converted to interface states after subsequent electron injection. It is reported that this mechanism is responsible for the observed enhanced AC hot-carrier degradation [1.6]. When the voltage waveform traverses both low gate- and high gate-voltage regions as in certain circuit operation, additional interface states are generated. The device degradation due to this mechanism can be modelled as [1.4]

$$\Delta = [\frac{1}{A} \cdot (\frac{I_D}{W}) \cdot (\frac{I_{SUB}}{I_D})^i \cdot t]^j \qquad (1.1)$$

where A, i and j are degradation model parameters obtained by fitting the experimental data; Δ, which is the degradation monitor, can be ΔV_T, $\Delta g_m/g_{m0}$, or $\Delta I_D/I_{D0}$.

For the medium gate-voltage stress ($V_G \sim V_D/2$, peak substrate-current region), acceptor-type interface state generation is the most important degradation mechanism [1.7]. The acceptor-type interface states, when occupied, are negatively charged. These negative charges increase the threshold voltage, increase the series resistance in the LDD structures [1.8], and decrease the carrier mobility. Therefore, the drain current decreases. The hot-carrier degradation due to interface states can be modelled by either substrate current

$$\Delta = (\frac{1}{H} \cdot I_{SUB}^m \cdot t)^n \qquad (1.2)$$

or drain electric field ($E \sim I_{SUB}/I_D$)

$$\Delta = [\frac{1}{H} \cdot (\frac{I_D}{W}) \cdot (\frac{I_{SUB}}{I_D})^m \cdot t]^n \qquad (1.3)$$

where H, m, n are degradation model parameters. This interface-state generation is commonly believed to be the dominant degradation mechanism to affect NMOSFET device and CMOS digital circuit performance [1.9].

For the high gate-voltage stress ($V_G \sim V_D$, peak gate electron-current region), the electron trapping mechanism affects the device most [1.10]. These electron traps, whose occupancy is insensitive to the bias voltage, will have similar effects as the acceptor-type interface states. The transistor degradation can be expressed as [1.10]

$$\Delta = [\frac{1}{B} \cdot (\frac{I_D}{W}) \cdot (\frac{I_G}{I_D})^k \cdot t]^l \tag{1.4}$$

where B, k and l are degradation model parameters.

1.1.2. PMOSFET Device Degradation

Because the inversion-layer hole mobility is less than one half of the inversion-layer electron mobility and the oxide barrier for holes is 1eV higher than the barrier for electrons, hot-carrier degradation is less a problem for PMOSFETs than for NMOSFETs. However, PMOSFET hot-carrier reliability is reported to be very important with the punchthrough voltage reduction for device lengths below 0.5μm [1.11].

The dominant degradation mechanism for PMOSFETs is found to be electron traps in the oxide. These electron traps can induce the same "channel-shortening effect" as hole traps in NMOSFETs [1.5]. As a result, drain current increases. Reduction of punchthrough voltage and increase of static-power dissipation due to the channel-shortening effect are two primary reliability concerns. The degradation can be modelled by either the gate-current-induced damage model [1.12]

$$\Delta = [\frac{1}{H} \cdot (\frac{I_G}{W})^m \cdot t]^n \tag{1.5}$$

or trap-charge filling model [1.13]

$$\Delta = A \cdot \ln(\frac{\tau_0}{\tau}) \cdot \ln(\frac{t}{\tau}) \tag{1.6}$$

where H, m, n, A, τ, and τ_0 are all degradation model parameters which can be extracted by individual device stress measurements.

1.1.3. Circuit-Level Degradation Simulation

Because circuit and system performance degradation should be the real criteria for evaluating hot-carrier reliability, how to simulate circuit degradation has attracted a great deal of attention recently [1.14]-[1.19]. Almost all existing simulation programs use the empirical power relation based on DC device degradation [1.20].

$$\Delta = A t^n \tag{1.7}$$

where Δ, which is the degradation monitor, can be ΔV_T, $\Delta g_m/g_{m0}$, or $\Delta I_D/I_{D0}$. This equation forms the basis to calculate the device lifetime under different operating voltages.

In the real circuit environment, drain and gate voltage are time-varying functions. In order to accommodate the AC waveforms, the degradation of NMOSFETs can be rearranged in the following form from (1.3)

$$\Delta = \left(\int \frac{I_D(t)^{1-m} \cdot I_{SUB}(t)^m}{W \cdot H} \cdot dt\right)^n \tag{1.8}$$

Based on (1.8), the total degradation can be obtained by integrating the degradation over various time periods. The drain and gate voltage can be acquired by using SPICE simulation. This information, in turn, can give the drain and substrate currents that can be used in (1.8). All the degradation model parameters (n, m and H) need to be obtained by separate DC device stress experiments. Note, that an important "quasi-static approximation" is made in the above calculations. It states that the device degradation under AC conditions can be approximated by dividing time into small periods and applying DC (static) degradation models.

The PMOSFET degradation can be expressed for the reliability simulations similarly from (1.5)

$$\Delta = (\int \frac{1}{H} \cdot (\frac{I_G(t)}{W})^m \cdot dt)^n \qquad (1.9)$$

The total degradation can be obtained by integration (1.9).

Once the device degradation of every transistor in the circuit is known, degraded device I-V SPICE model parameters can be used in the SPICE program to simulate the degradation of circuit performance due to hot-carriers effects.

1.2. Motivation

As device scaling continues, the traditional device-level DC hot-carrier reliability criteria becomes more difficult to meet. Either AC-type or circuit-level criteria become necessary for newer generations of technology. Although fairly good understanding of the device-level hot-carrier degradation under DC stress conditions has been achieved [1.4]-[1.7], device degradation under AC stress conditions and its influence on the circuit performance are still not yet fully understood.

Earlier efforts to verify the AC device degradation models mostly suffered from unrealistic circuit operating conditions [1.21], excessive experiment-setup-inductive noise [1.22], or lack of enough experimental validations [1.23]. These effects coupled with possible inaccuracies of parameter extraction and substrate/gate current modeling, thus, gave some conflicting results.

As for circuit-level reliability evaluation, The traditional DC device-type reliability criteria such as 10% change in current drive or 10mV threshold voltage shift do not necessarily reflect how the circuit performance degrades [1.24]. Circuit-level criteria such

as a 10% change in access time or a 10mV offset voltage are necessary to evaluate the impact of hot-carrier degradation on circuit performance.

Due to lack of understanding of AC device degradation and its impact on circuit performance, extremely conservative circuit design and technology development are currently adopted. Circuit and system performance are often sacrificed. Take drain engineering as an example. The lightly-doped drain (LDD) structure is commonly used to improve submicrometer device hot-carrier reliability [1.25]. However, the lightly-doped drain region often introduces parasitic drain/source series resistance components (R_D, R_S). Thus, the overall performance of the circuit is sacrificed. A typical plot (Fig. 1.1) of NMOSFET LDD n^- doping-induced resistivity versus the device delay (which represents device performance) and substrate current (which represents device reliability) illustrates the tradeoff between reliability and performance [1.25]. Without a clear understanding of hot-carrier degradation, it is very difficult to formulate the precise reliability criteria and thus optimize the reliability-performance tradeoff. And with the continuation of device scaling , it will become more difficult to optimize and integrate these novel device structures for the next generation of technology [1.26].

In the past, reducing the power supply voltage is another common method to combat hot-carrier degradation. However, for high speed microprocessor operation, a higher power supply voltage to achieve faster computation speed is often desired [1.27]. Fig. 1.2 shows that the speed of CMOS devices slows down as the power supply voltage reduces [1.28]. It is projected that the performance of microprocessors for the future 0.25μm process will degrade 15-20% from a 3.3V power supply to a 2.5V power supply. Also the performance of BiCMOS logic circuits is severely degraded below 3.3V.

Therefore, the reliability of the devices and circuits needs to be examined carefully. By understanding the device degradation under AC operating conditions and the circuit hot-carrier reliability, the tradeoff between reliability and performance can be optimized.

1.3. Methodology

This thesis will concentrate on device and circuit degradation due to hot-carrier effects. Through analytical modeling, experimental verification, and reliability simulation, the research will try to evaluate systematically the hot-carrier reliability for devices, digital circuits, and analog circuits. The device degradation under both DC and AC stress conditions will be evaluated and compared. The impact of device degradation on circuit performance will be analyzed.

Current hot-carrier device degradation models will be improved for lifetime estimation and circuit reliability simulation purposes. The time and voltage dependence of hot-carrier degradation will be evaluated for a wide range of stress conditions. The issues of statistical data collection and degradation model parameter extraction will be examined.

For circuit-level reliability evaluation, this thesis will concentrate on the experimental results from subcircuit test structure measurements for the following reasons:

(1) existence of multiple degradation mechanisms: Both oxide traps and interface states are generated during hot-carrier stress for NMOSFET [1.4], [1.10] and PMOSFET devices [1.29], [1.30]. The impact of different mechanisms has not been fully tested in a real circuit environment under AC operating conditions. As a result, the models based on DC device stress may not be valid for AC purposes. The relative importance of different degradation mechanisms will heavily depend on the particular operating voltage waveform (which affects the level of hot-carrier damage) and circuit operating condition (which dictates how the damage affects the device) [1.3].

(2) lack of verifications in current simulation tools: Because hot-carrier degradation is very sensitive to applied voltage waveforms, capacitance coupling due to device parasitics [1.31] and interconnects [1.32] often contribute significantly. Therefore, correct modeling of the device and parasitics is needed for the accuracy of current

reliability simulation programs. Duty-cycle calculation based on the quasi-static approximation (1.8) is widely used by current reliability simulation programs [1.33]. However, whether the quasi-static approximation can be used needs further experiment verification.

Through degradation experiments based on subcircuits, realistic results can be obtained and compared directly to simulation results. Therefore, these controversial simulation issues can be addressed. The circuit test structures will be designed to reflect realistic circuit operation conditions. All the high frequency input/output will be probed by picoprobes to avoid test setup loading effects. Special circuit structures, which enable the testing of devices embedded inside the circuits, will be used. The experimentally measured device degradation in a real circuit environment can then be compared directly to the simulation prediction. Model and simulation program validations can be accomplished. Besides the model verification, the correlations between device and circuit degradation can be established in this way. This result will be used to choose the hot-carrier reliability criteria based on the circuit performance requirements instead of individual device specifications.

1.4. Overview of the Thesis

Although there have been numerous studies to model the hot-carrier degradation, the circuit-level study requires a valid model over a wide range of bias conditions and device technologies. In order to satisfy these stringent requirements, Chapter 2 will examine the two most important parameters in existing NMOSFET hot-carrier degradation models: (1) the time acceleration factor which is related to the time dependence of hot-carrier degradation; and (2) the voltage acceleration factor which is related to the voltage dependence of hot-carrier lifetime. The bias-voltage dependence and its impact on lifetime estimation will be assessed. Hot-carrier degradation was often treated as a deterministic process in the past. Not, until recently has the statistical nature of hot-carrier reliability been studied in more detail [1.34]. Chapter 2 has incorporated this

statistical uncertainty into the lifetime estimation and reliability simulation. By using statistical analysis, the prediction intervals of lifetime estimation are determined and incorporated into lifetime estimation. Also, efficient parameter extraction procedures, which can minimize the statistical uncertainly, stress time and the number of measurements, are derived for rapid and accurate process calibration.

Chapter 3 will discuss the time dependence of modern submicrometer LDD NMOSFET hot-carrier degradation in detail. Takeda [1.20] has empirically shown the degradation follows the $A \cdot t^n$ relation (1.7). Later Hu [1.7] formulated a physical model for it. However, non $A \cdot t^n$ relations are commonly observed in LDD NMOSFET [1.35] device degradation. These phenomena can be attributed to "spacer induced damage" for non fully overlapped device structures [1.8]. The physical causes which lead to this behavior will be investigated by I-V measurement, charge pumping measurement, and device-level simulation. How the non-constant rate coefficients affect the hot-carrier lifetime estimation and reliability simulation will be examined. In addition, model modifications will be proposed.

Evaluation of hot-carrier degradation for basic subcircuits will be conducted in this thesis based on an existing digital/analog circuit classification scheme which connects device and technology parameters to specific circuit applications [1.36]. Chapter 4 uses simple digital logic circuits which constitute the high-density logic circuits commonly found in the data path, control, and processing sections of integrated circuits to study high-frequency AC hot-carrier degradation. The degradation characteristics of NMOSFET, PMOSFET, and digital circuits will be examined. Their degradation time dependence under high-frequency circuit operations will be evaluated and compared to DC stress data. Also a new enhanced AC degradation mechanism will be explained by using the charge feedforward phenomenon found in short voltage transient conditions.

Chapter 5 utilizes differential amplifiers and current mirrors which constitute the main building blocks for many analog circuits to study how NMOSFET degradation affects circuit performance. Due to the low gate-to-source operating bias conditions, the

analog NMOSFET performance is identified to be mostly affected by hole traps. Key performance parameters which include open circuit voltage gain and input offset voltage will be monitored. The tradeoff between performance and reliability will be evaluated.

Chapter 6 will summarize the research results in this thesis. Possible future studies are suggested.

Finally, Appendix will discuss the issues of test structures design for hot-carrier reliability evaluation purposes and the associated testing configurations.

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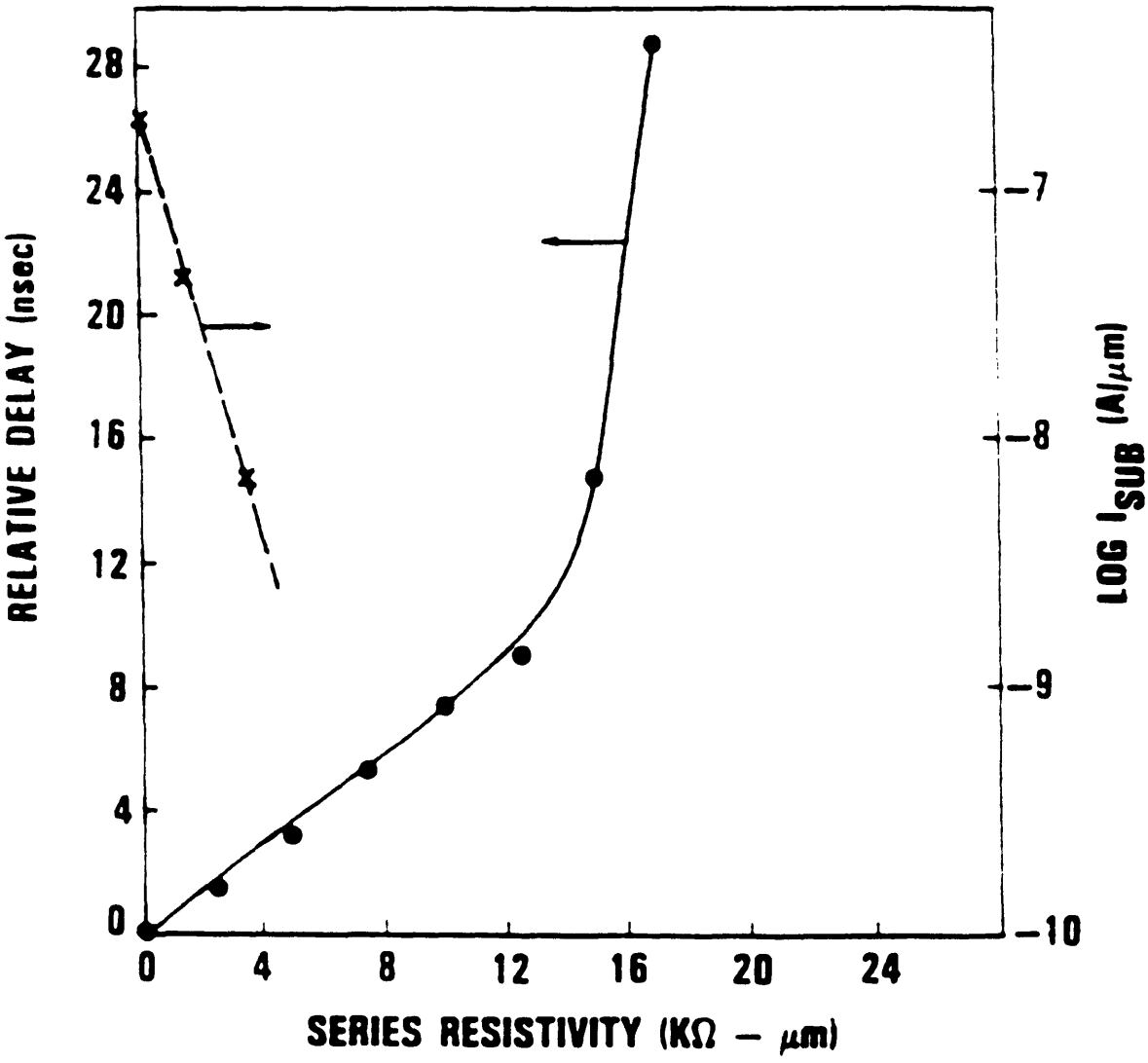

Fig. 1.1 NMOSFET LDD n^- doping induced resistivity versus device performance (relative delay time) and reliability (substrate current I_{SUB}). W/L=20/2μm, T_{OX}=25nm.

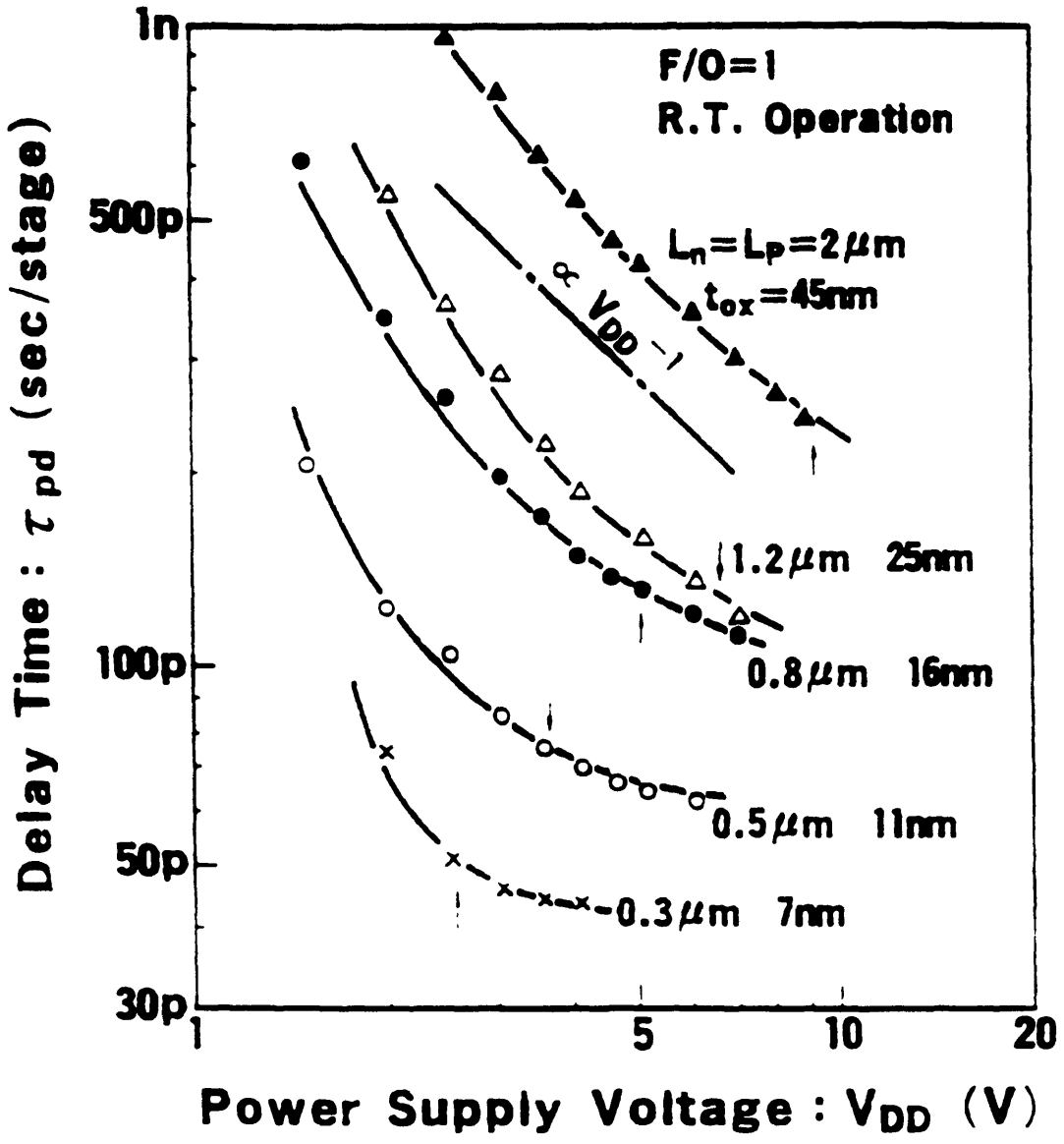

Fig. 1.2 CMOS inverter propagation delay time (t_{pd}) measured from ring oscillators with fanout 1 versus power supply voltage at each design generation.

Chapter 2

Parameter Extraction for NMOSFET Hot-Carrier Degradation Models

2.1. Introduction

As VLSI scaling continues toward smaller geometry, hot-carrier degradation constitutes a major threat to long term device reliability. Hot electrons and holes are generated when devices are operated in saturation region where a large lateral electric field is created. These hot electrons and holes subsequently damage gate oxide either by creating interface states or oxide traps. These damages which change device characteristics will slow down the circuit operation [2.1] or induce device parameter mismatches in the circuits [2.2], [2.3].

Several degradation models have been proposed [2.4]-[2.6] to explain hot-carrier degradation. SPICE level or timing level simulation programs that can evaluate hot-carrier-induced device degradation and its effects on circuit performance such as BERT [2.7] and RELY[2.8] have also been developed. However, the appropriate procedures to calibrate these tools to a particular process have been so far largely unaddressed. Without careful calibrations, these simulation tools would not be very accurate, thus limiting their overall impacts and usefulness.

In this chapter, I will examine the NMOSFET parameter extraction for lifetime

extrapolation and circuit-level hot-carrier reliability simulations in detail. General parameter extraction guidelines accounting for the asymptotic and variable power-law time dependence of hot-carrier degradation, the dependence of the critical energy for interface damage on the local oxide electric field are presented. Finally, I will present the statistical analysis of lifetime extrapolation from which extraction procedures can be developed to optimize the stress time, the number of measured devices, and the lifetime prediction intervals.

2.2. Degradation Model and Extraction Procedure Review

Depending on the operating voltage range, the degradation of NMOSFETs is due to three different mechanisms. Acceptor-type interface states generate over all the voltage range [2.4]. Hole traps generate during low gate-voltage (V_G~V_T) operation [2.6] and electron traps generate during high gate-voltage (V_G~V_D) operation [2.5]. It is believed that the acceptor-type interface-state generation is the dominant mechanism for hot-carrier degradation of digital circuits [2.1]-[2.4]. Therefore, I will only consider the interface-state generation mechanism in this chapter. The importance of hole and electron traps in evaluating the degradation of analog circuit performance will be discussed in Chapter 5.

Present simulation tools all use similar hot-carrier degradation models based on the drain current and lateral electric field (~I_{SUB}/I_D). The degradation can be represented by the quantity

$$AGE = \frac{I_D}{W \cdot H} \cdot \left(\frac{I_{SUB}}{I_D}\right)^m \cdot t_{STRESS} \qquad (2.1)$$

for NMOSFETs, where hot-carrier-induced interface damage is dominated and modeled as [2.7]

$$\Delta N_{it}=(AGE)^n \tag{2.2}$$

The parameter n is the degradation rate coefficient which reflects either the reaction-limited or transport-limited regimes of the interface state generation mechanism [2.4]; m equals φ_{it}/φ_i, where φ_{it} and φ_i are the critical energies for interface damage and impact ionization respectively; H is a technology dependent parameter; W is the device width.

The change of interface state density as well as various device parameters [2.9] (such as ΔV_T or $\Delta I_D/I_{D0}$) shown by (2.2) follow the $A \cdot t^n$ relation. By plotting the amount of degradation versus time in a log-log scale, the data form a straight line where the rate coefficient n is the slope. The device lifetime τ due to hot-carrier degradation can be extrapolated accordingly.

The degradation model (2.1) can be further rearranged as

$$\frac{\tau \cdot I_D}{W}=H \cdot A^{\frac{1}{n}} \cdot \left(\frac{I_{SUB}}{I_D}\right)^{-m} \tag{2.3}$$

where A is the lifetime definition chosen in (2.2) such as $\Delta I_D/I_{D0}=0.1$ or $\Delta I_{CP}=100$pA/m/Hz and τ is the device lifetime. Based on (2.3), parameter m and H can be extracted from the lifetime correlation plot of $\tau \cdot I_D/W$ versus I_{SUB}/I_D in a log-log scale. By stressing devices with different I_{SUB}/I_D ratios, the data can be fitted to the model (2.3). Parameter m and log(H) can be derived respectively from the slope and y-intercept of the fitted line.

2.3. Experimental Methodology

The NMOSFET devices used in this study were fabricated using a 0.8μm double-level poly, double-level metal CMOS technology with an oxide spacer LDD structure (minimum $L_{EFF}=0.45\mu m$, $T_{OX}=16.5$nm). The transistors were stressed with DC voltages. The reduction in forward-linear current drive ($\Delta I_D/I_{D0}$ measured at $V_D=0.05V$, $V_G=3.0V$)

as a function of stress time was chosen as the principal degradation monitor because of its direct relation to the hot-carrier-generated interface state density [2.10] and ease of measurements. All the data were measured at room temperature on wafer level.

2.4. Degradation Rate Coefficient

Fig. 2.1 shows the typical reduction of forward-linear current as a function of stress time for different stress voltages. The rate coefficient n from Fig. 2.1 exhibits a large range of values. It seems to suggest that the rate coefficient n depends on the particular stress voltage. The lifetime τ is calculated for different lifetime definitions and the resulting lifetime correlations are plotted (Fig. 2.2). The different m coefficients obtained from Fig. 2.2 as a result of variation in rate coefficients indicate that the lifetime correlation exhibits a strong dependence on the particular lifetime criterion chosen. This is clearly incorrect as the critical energy for interface state generation should not depend on some external parameters. Therefore, a consistent lifetime correlation can not be obtained based on the current degradation model.

However, this behavior is an artifact which arises from not properly accounting for the degradation-rate saturation behavior in the hot-carrier degradation's time dependence, a common observation in submicrometer LDD devices [2.11], [2.12]. Fig. 2.3 shows the data from the same devices displayed in Fig. 2.1 stressed for such a long duration that the degradation rate reaches its final asymptotic value. Using the asymptotic value for the parameter n, a consistent relation between lifetime and I_{SUB}/I_D can be obtained independent of the particular lifetime criterion (Fig. 2.4). The same asymptotic phenomenon is also observed in charge-pumping experiments which directly measure the interface-state density [2.12]. This demonstrates the increasing rate of interface states being asymptotic, not the interface states effect on linear-current reduction. Thus, $A \cdot t^n$ power relation of linear current reduction is still valid and applicable for lifetime extrapolation and circuit-level hot-carrier degradation simulations as long as the asymptotic behavior is taken into account. Without considering the degradation-rate

saturation behavior, the wrong lifetime value will be extrapolated and consequently results in the wrong lifetime correlation with power-supply voltage.

2.5. Critical Energy for Hot-Carrier Damage

The critical energy for interface state generation φ_{it} has been demonstrated to depend on the oxide electric field near the drain during stress [2.13]. It is suspected that this oxide-field dependence is associated with either the injection mechanisms or the interface-state damage generation [2.14]. In order to be suitable for evaluation of hot-carrier degradation in AC conditions, the model must be applicable over a wide range of operating voltage. Therefore, it is necessary to account for this local oxide-field dependence in extracting the degradation model parameters. Fig. 2.5 displays lifetime correlation data obtained under constant oxide field stress conditions $E_{OX} \approx (V_G - V_D)/T_{OX}$. The V_{GD} dependence of parameters m and log(H) displayed in Fig. 2.6 can be empirically fitted and used in circuit-level hot-carrier degradation simulation programs.

For comparison purposes, Fig. 2.5 also displays lifetime data obtained under peak substrate-current stress conditions with resulting constant m and H coefficients. Peak substrate current stress conditions are achieved by adjusting gate voltage for a given drain voltage to get maximum substrate current. As a result of this, peak substrate stress conditions traverse different V_{GD} bias region and ignore φ_{it} bias dependence. Fig. 2.7 compares different extrapolated lifetimes obtained using constant (either peak I_{SUB} only or peak $I_D \cdot (I_{SUB}/I_D)^m$) and V_{GD}-dependent (constant oxide field) values for the parameters m and H. Measuring peak I_{SUB} alone while neglecting the V_{GD}-dependence of the coefficient m results in significantly overestimated lifetime values. Note that this overestimation of hot-carrier lifetime worsens as the power supply voltage is reduced (since more extrapolation is required). Therefore, it is necessary to consider the V_{GD} bias-dependent m and H to get a realistic lifetime estimates.

2.6. Estimating Lifetime under AC Operating Conditions

For a typical circuit operation, bias voltage experienced by devices usually traverses different voltage ranges. Therefore, the oxide electric-field dependence of φ_{it} and m can significantly impact estimates of the hot-carrier lifetime in AC operation. Fig. 2.8 illustrates how the bias conditions experienced by an NMOSFET during the discharge phase of a CMOS inverter depend on a particular load capacitance. The different predictions of AC degradation that result from using both constant (peak I_{SUB}) and V_{GD}-dependent (constant oxide field) values of the parameter are illustrated in Fig. 2.9. Without considering V_{GD} dependence, the extrapolation using constant m and H fails to show the output capacitance dependence of the degradation. For more accurate AC degradation predictions, the V_{GD} dependent parameters should be used.

Under AC operating conditions, variability of the degradation rate coefficient n can also significantly impact hot-carrier lifetime estimates. Fig. 2.10 considers an example of a simple periodic stress waveform with two different voltages which occur during the time intervals t_1 and t_2. A single device stressed for N cycles by this waveform will have only two stress conditions (AGE1 and AGE2) along with two corresponding rate coefficients (n1 & n2). If n1 equals n2, then the total cumulative hot-electron damage that occurs over the device's entire operational lifetime can be estimated using [2.7]

$$\Delta N_{it}=[N(AGE1+AGE2)]^n \tag{2.4}$$

Note that hot-carrier degradation simulation only needs to be performed for a single waveform cycle. However, for variable rate coefficients ($n1 \neq n2$) this simple extrapolation is no longer applicable. The cumulative degradation occurring through t_1 is

$$\Delta N_{it}=AGE1^{\,n1} \tag{2.5}$$

The cumulative degradation through t_2 is

$$\Delta N_{it}=(AGE1^{n1/n2}+AGE2)^{n2} \tag{2.6}$$

Simulating hot-carrier degradation for all N cycles by iterating (2.6) is required. Fig. 2.10 shows that significant differences can exist between the approximate (averaged n is used) and exact lifetime calculations. For a typical clock-frequency 50MHz circuit operating for 10 years, 10^{15} cycles extrapolation is required. Apparently, significant errors can be introduced. A generalized version of this problem exists for the case of a continuously-time-varying waveform. For accurate degradation assessments, the variability of the rate coefficient need to be modeled and incorporated into existing lifetime models and simulation programs.

2.7. Statistical Parameter Extraction Issues

In the past, hot-carrier degradation has been treated as a deterministic process. However, due to die-to-die device variation, hot-carrier degradation and all other reliability problems in today's CMOS VLSI circuits are statistical process. In order to take this variation into account, statistical analysis should be used to evaluate the worst-case hot-carrier degradation. Fig. 2.11 displays the statistical variability of hot-carrier degradation measurements for a typical set of data. The prediction contours of the data can be calculated by the following formula [2.15]

$$S_y=S_e\sqrt{1+\frac{1}{N}+\frac{(x-\frac{1}{N}\sum_i x_i)^2}{\sum_i x_i^2-\frac{1}{N}(\sum_i x_i)^2}} \tag{2.7}$$

$$S_e=\sqrt{\frac{\sum_i (y_i-(-mx_i+logH))^2}{N-2}} \tag{2.8}$$

where S_y is the standard error of y; S_e is an estimate of standard deviation of the scatter of the data points around the regression line; m and H are degradation parameters; N is the number of measurements; x_i and y_i corresponding to $\log(I_{SUB}/I_D)_i$ and $\log(\tau \cdot I_D/W)_i$ are data points. Based on (2.3), (2.7) and (2.8), the lifetime with 99% prediction intervals for the operating voltage can be extrapolated to be

$$\tau = \frac{W \cdot H \cdot A^{\frac{1}{n}}}{I_D} \cdot \left(\frac{I_{SUB}}{I_D}\right)^{-m} \cdot 10^{\pm t_{n-2} \cdot S_y} \qquad (2.9)$$

where t_{n-2} is the critical value of t distribution for a two-tailed test to account for limited number of data points; I_{SUB} and I_D are the substrate current and drain current under operating voltage.

Fig. 2.12 shows the resulting lifetime with both 95% and 99% prediction intervals derived from Fig. 2.11. As the extrapolated lifetime is further away from the measured data points, the prediction intervals become larger. The widening of the prediction intervals is a result of statistical uncertainty in both the parameters m and H by using the linear regression method and is reflected in the estimated lifetime values for a particular power supply voltage.

Fig. 2.12 suggests that in order to minimize the prediction intervals, maximum stress voltage range should be used to reduce the extrapolation. However, the stress voltage range is limited by several constraints: the upper limit voltage should not turn on the parasitic source-bulk-drain bipolar transistor [2.16], and the lower limit voltage is set such that (1) stress time should be long enough to attain final asymptotic behavior; (2) the final degradation value should be at least one half of the degradation value of lifetime definition to minimize the lifetime extrapolation errors [2.17].

Based on these criteria, the prediction interval versus number of measurements is calculated as shown in Fig. 2.13, where the total testing time (number of measurements multiplies the individual device stress time) is a constant. For long individual device

stress time, the large prediction interval is due to the uncertainty associated with the small number of measurements. For small individual device stress time, the large prediction limit results from the large extrapolation range. A minimum prediction interval is achieved by balancing the stress voltage range and uncertainty associated with a small number of data points. Based on this analysis, an optimal extraction procedure which minimizes the extrapolation errors can be designed and performed.

2.8. Parameter Extraction Guidelines

This chapter presented NMOSFET general parameter extraction guidelines for DC lifetime extrapolation and circuit-level hot-carrier reliability simulations. It shows that the following procedures need to be adopted for process calibration:

(1) Devices need to be stressed long enough to attain the final asymptotic behavior and to minimize lifetime extraction errors;

(2) The local oxide field (V_{GD}) dependence of critical energy for interface damage must be taken into account;

(3) The variations of rate coefficient n need to be considered for AC operating conditions;

(4) Optimal extraction requires maximizing stress voltage range and number of measurements under time and parasitic bipolar effect constraints.

Following these guidelines have been shown to have several orders of magnitude impact on lifetime extrapolation.

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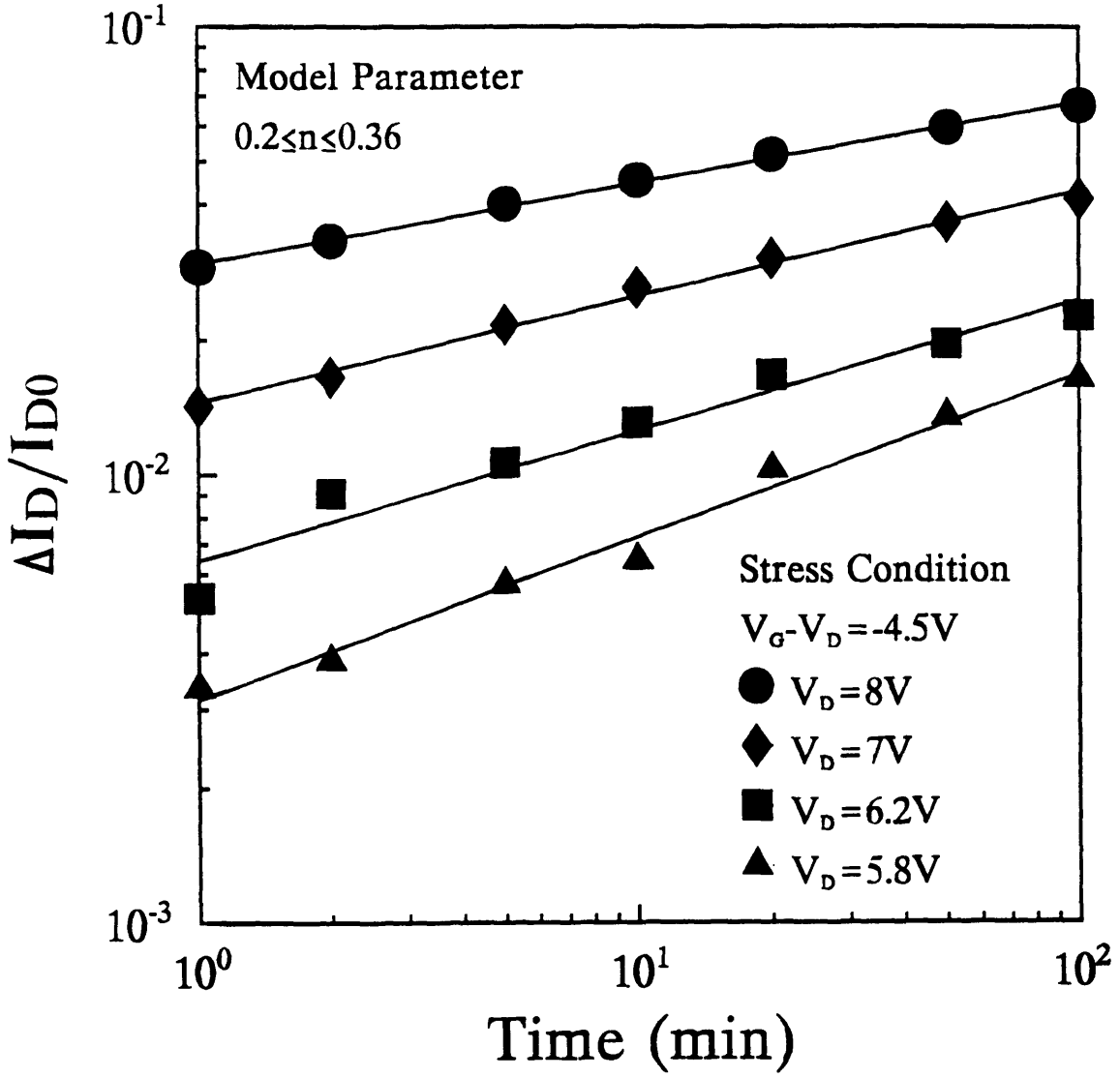

Fig. 2.1 Time dependence of NMOS hot-carrier degradation. The linear regression lines are shown.

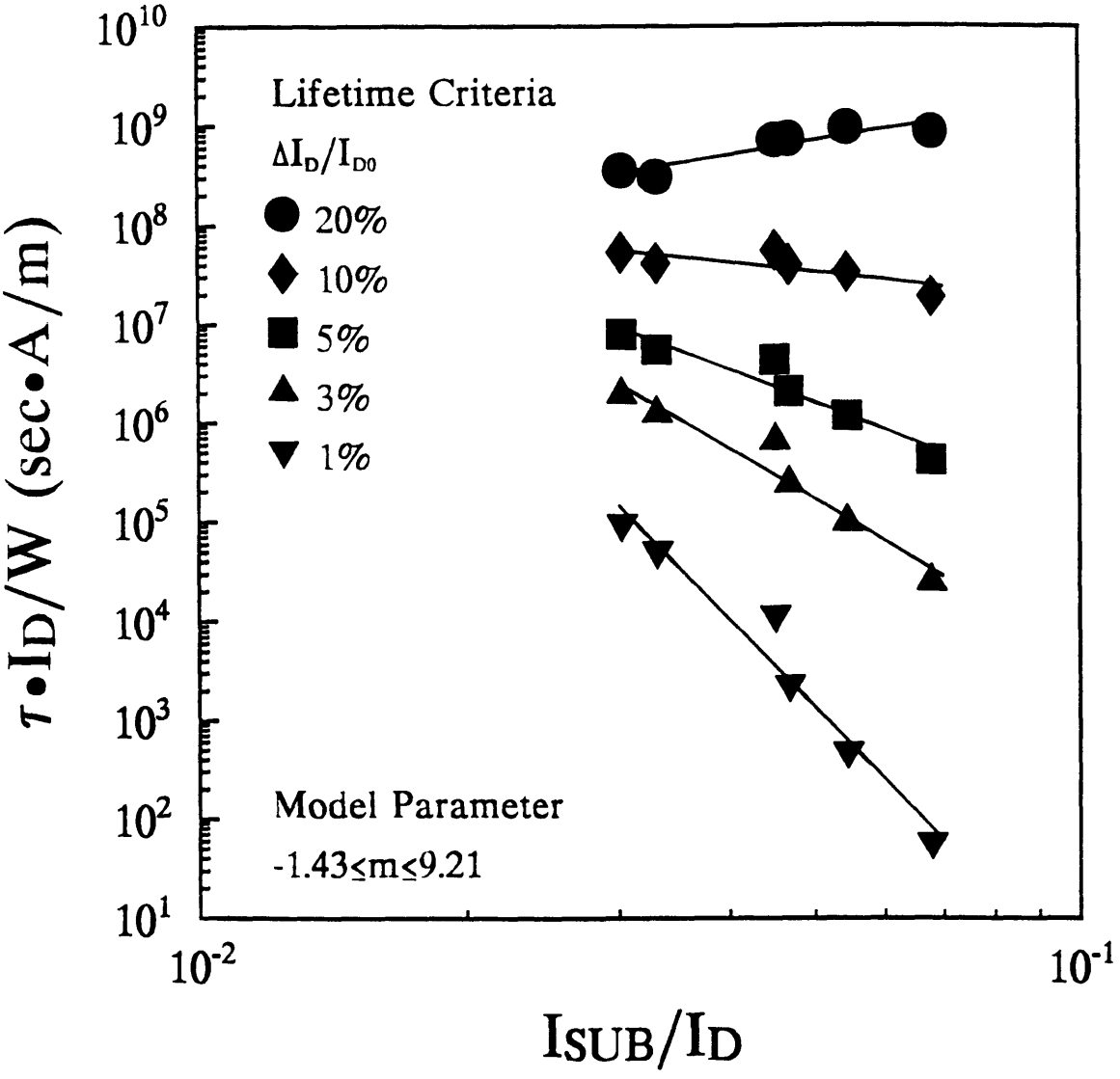

Fig. 2.2 Lifetime correlation plot. Lifetime values are calculated from Fig. 2.1.

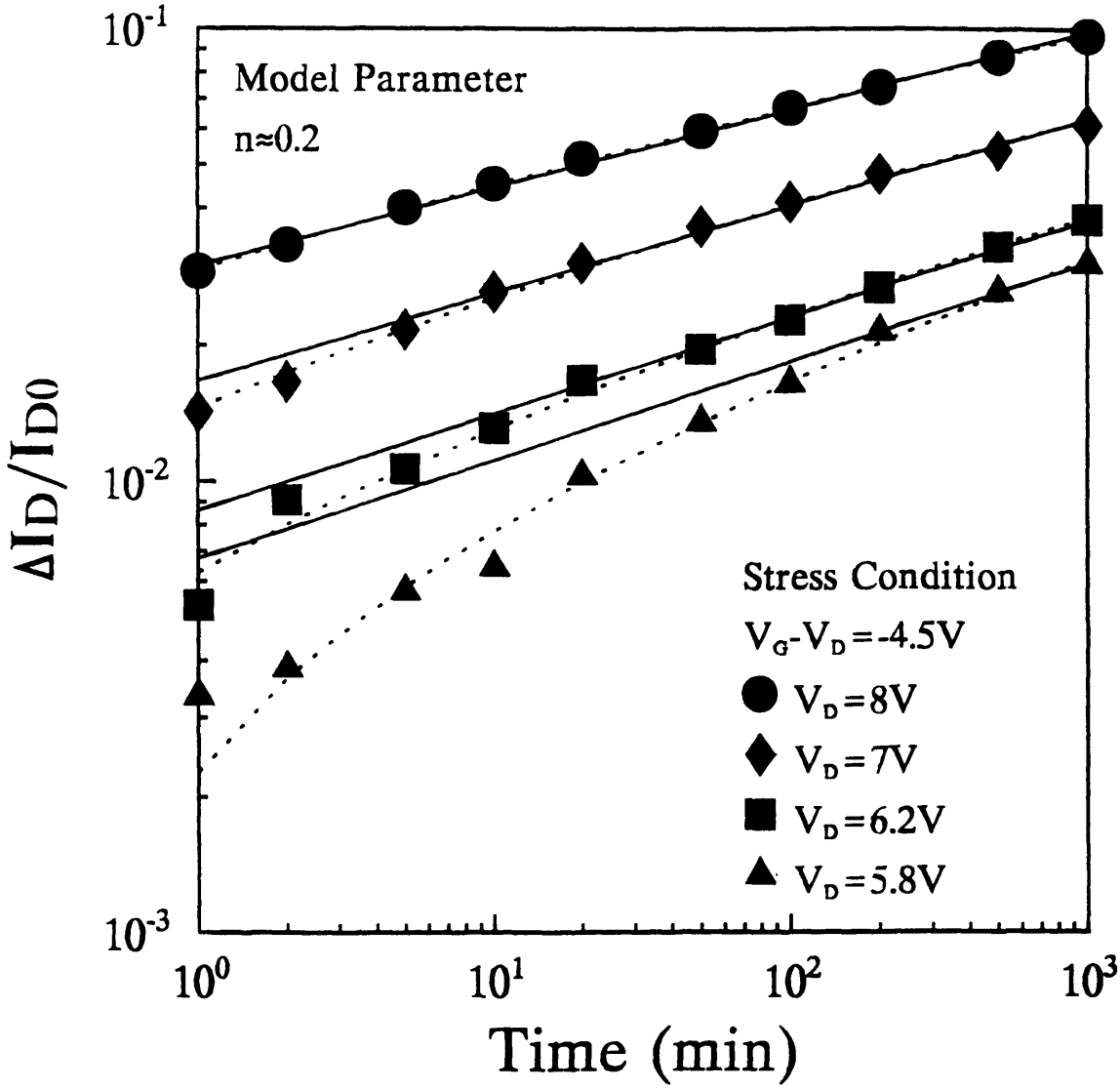

Fig. 2.3 Time dependence of NMOS hot-carrier degradation. The solid lines are asymptotes of the final slopes. The dotted curves are fitted including all the data points.

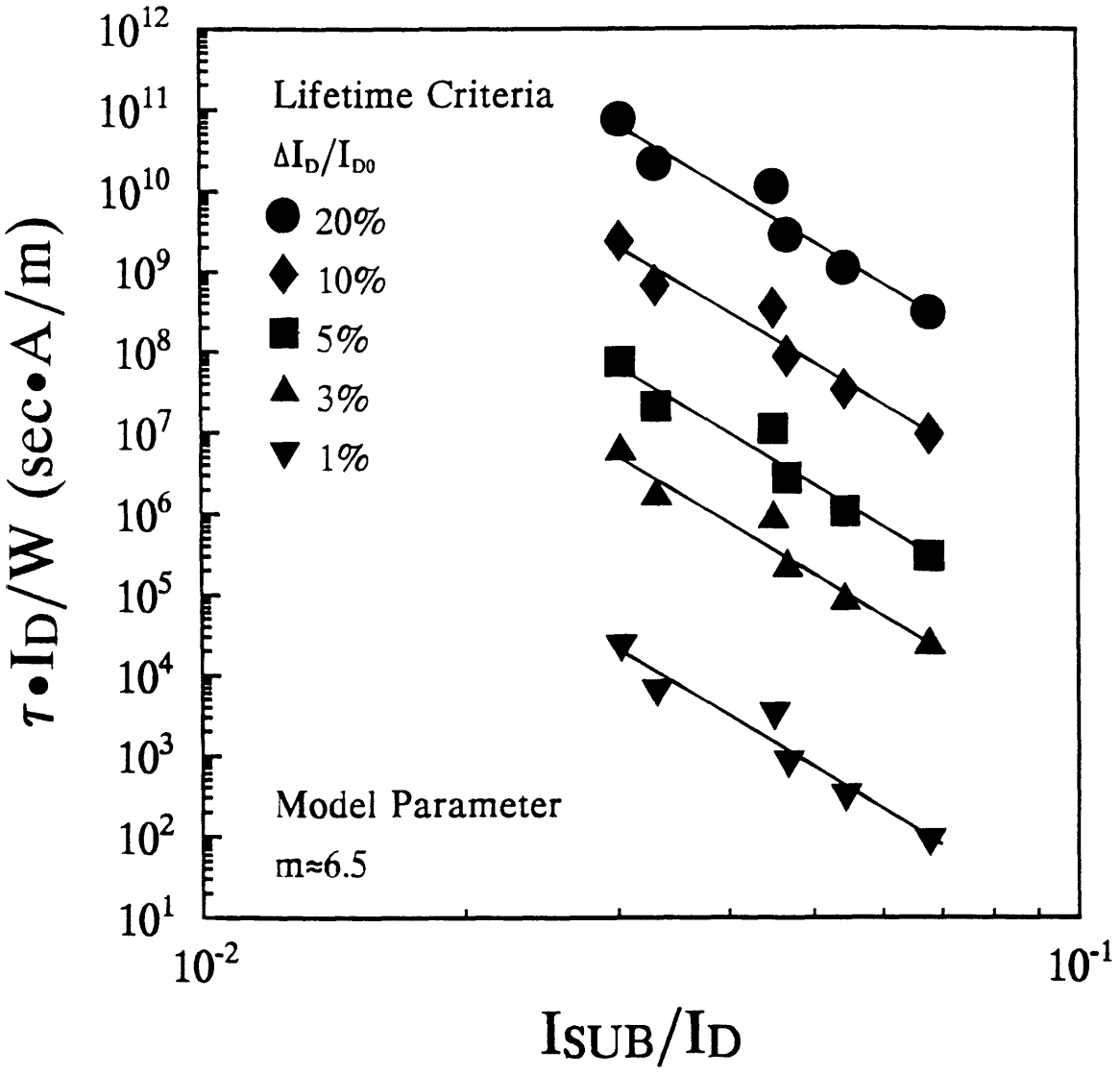

Fig. 2.4 Lifetime correlation plot. Lifetime values are calculated by using the asymptotes from Fig. 2.3.

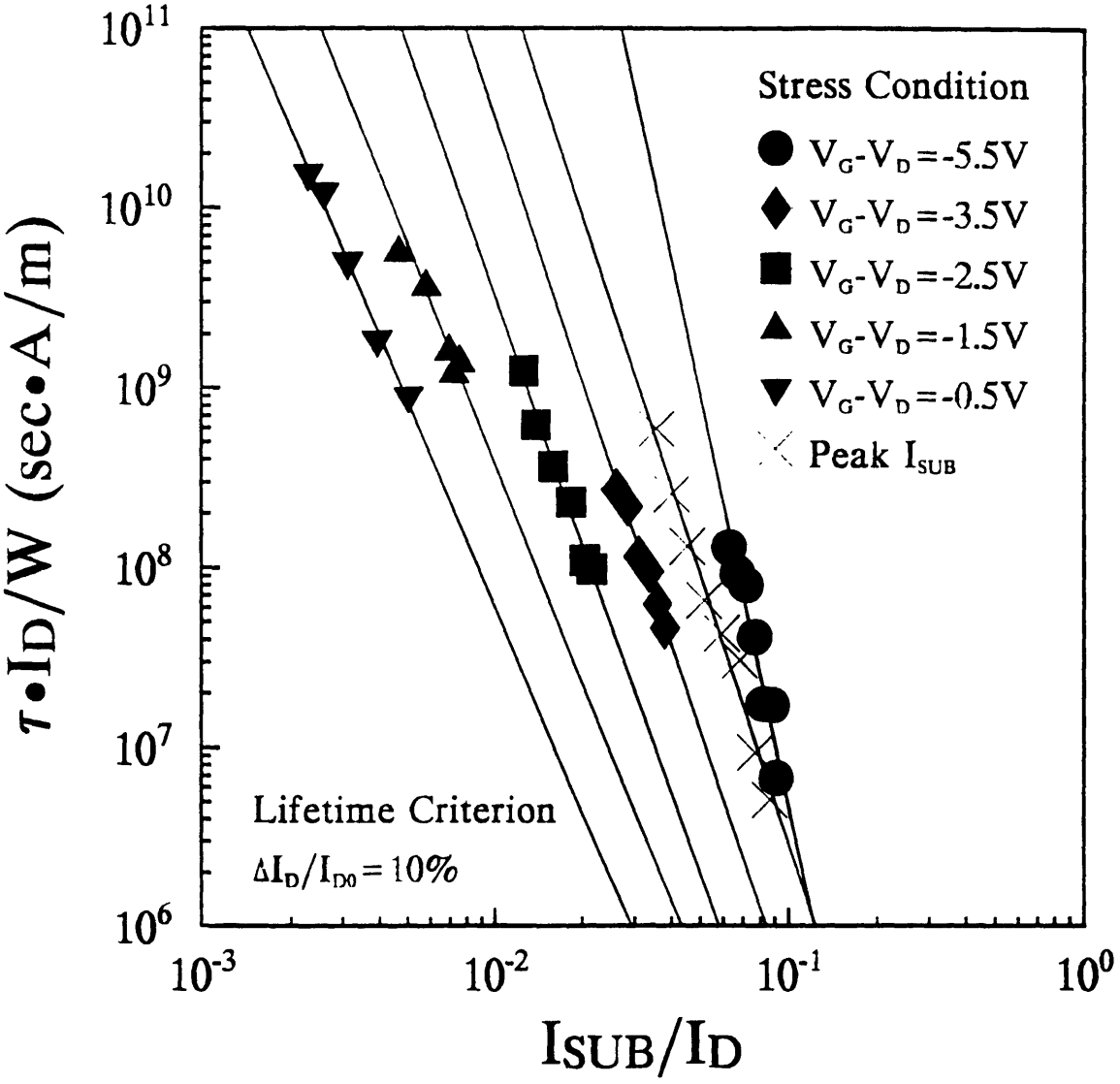

Fig. 2.5 Lifetime correlation plot with both fixed V_{GD} and peak I_{SUB} stress data.

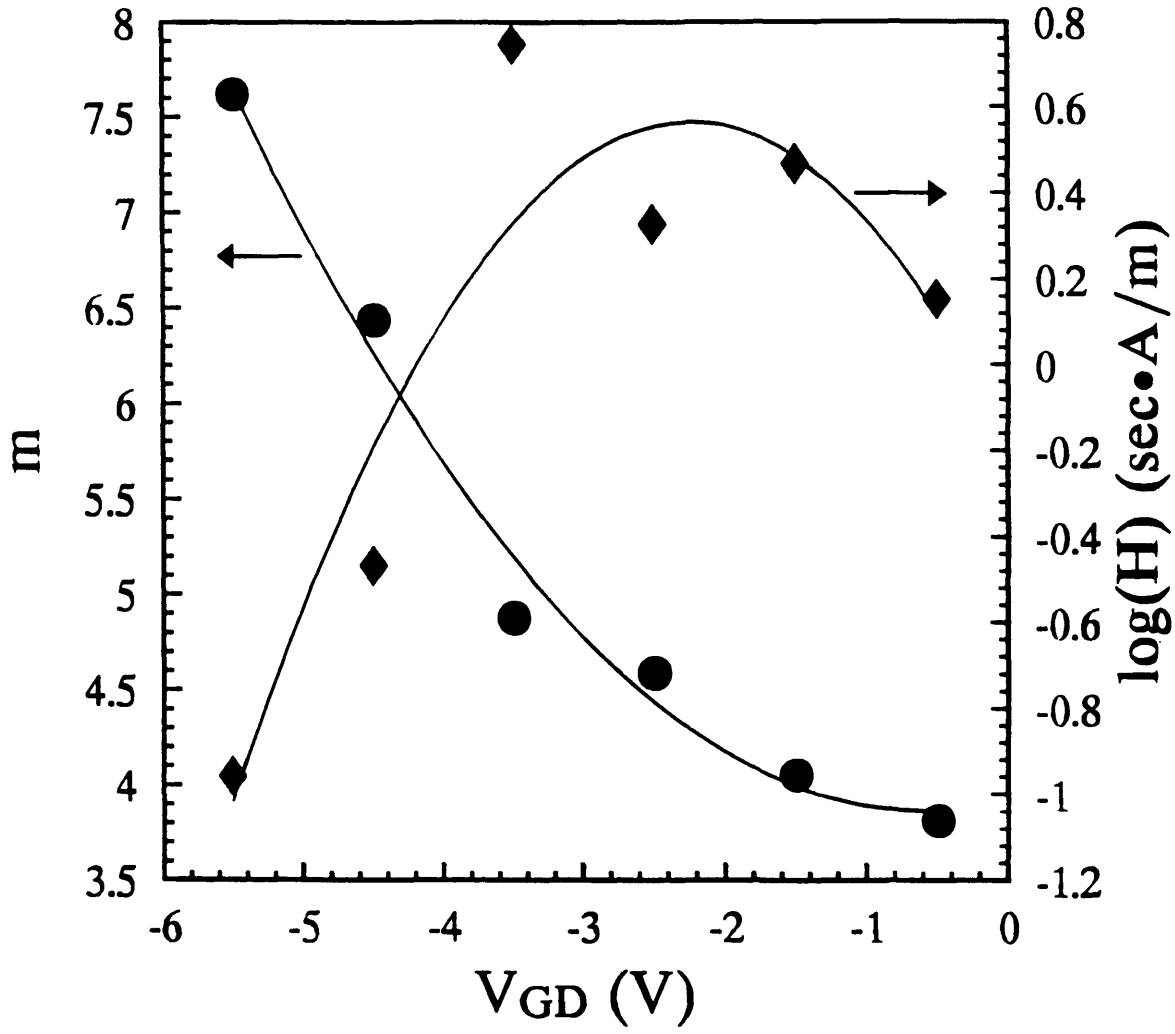

Fig. 2.6 Dependence of m and log(H) on V_{GD}. Data are extracted from Fig. 2.5.

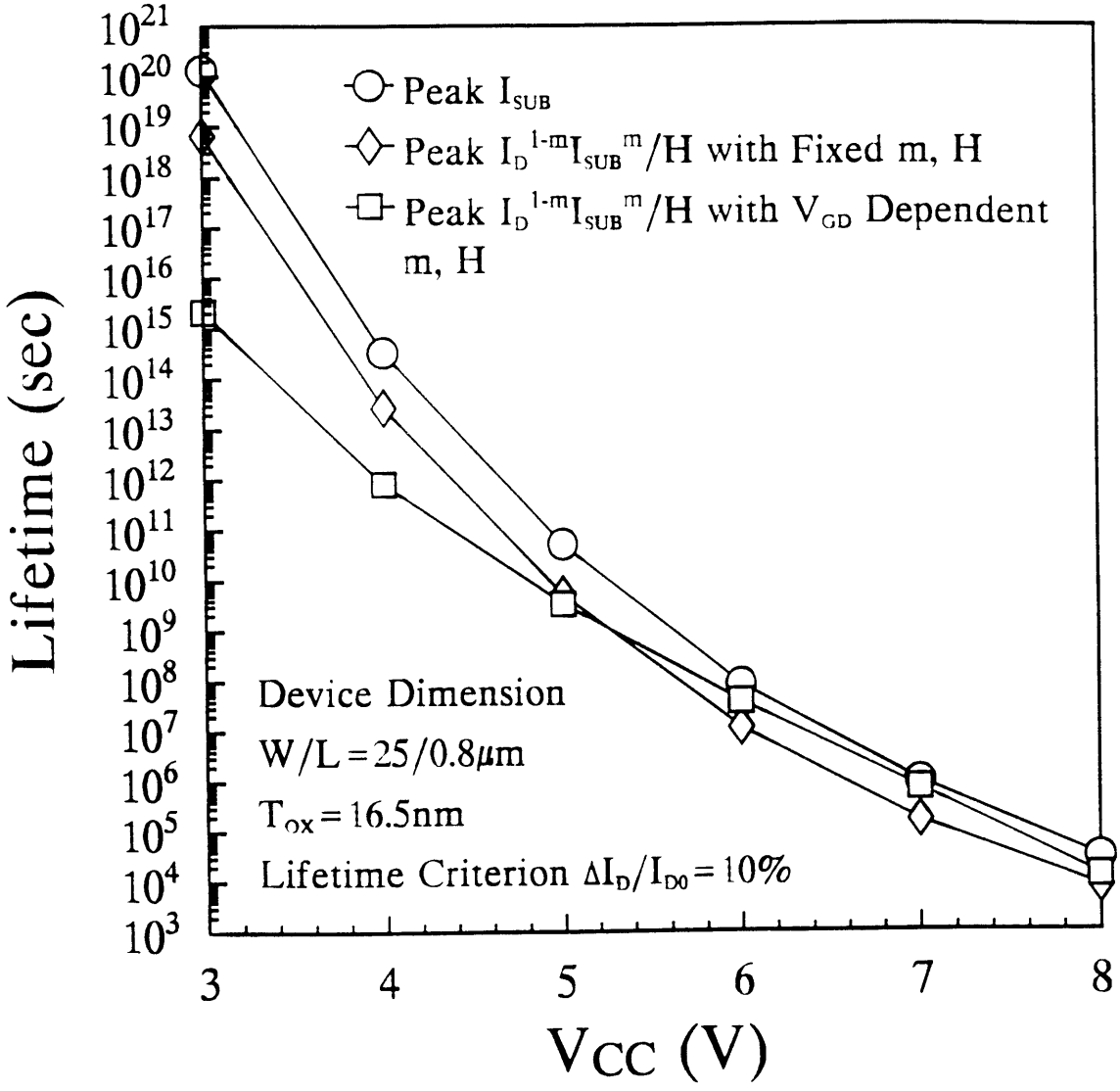

Fig. 2.7 Lifetime versus V_{CC} plot using three extrapolation techniques.

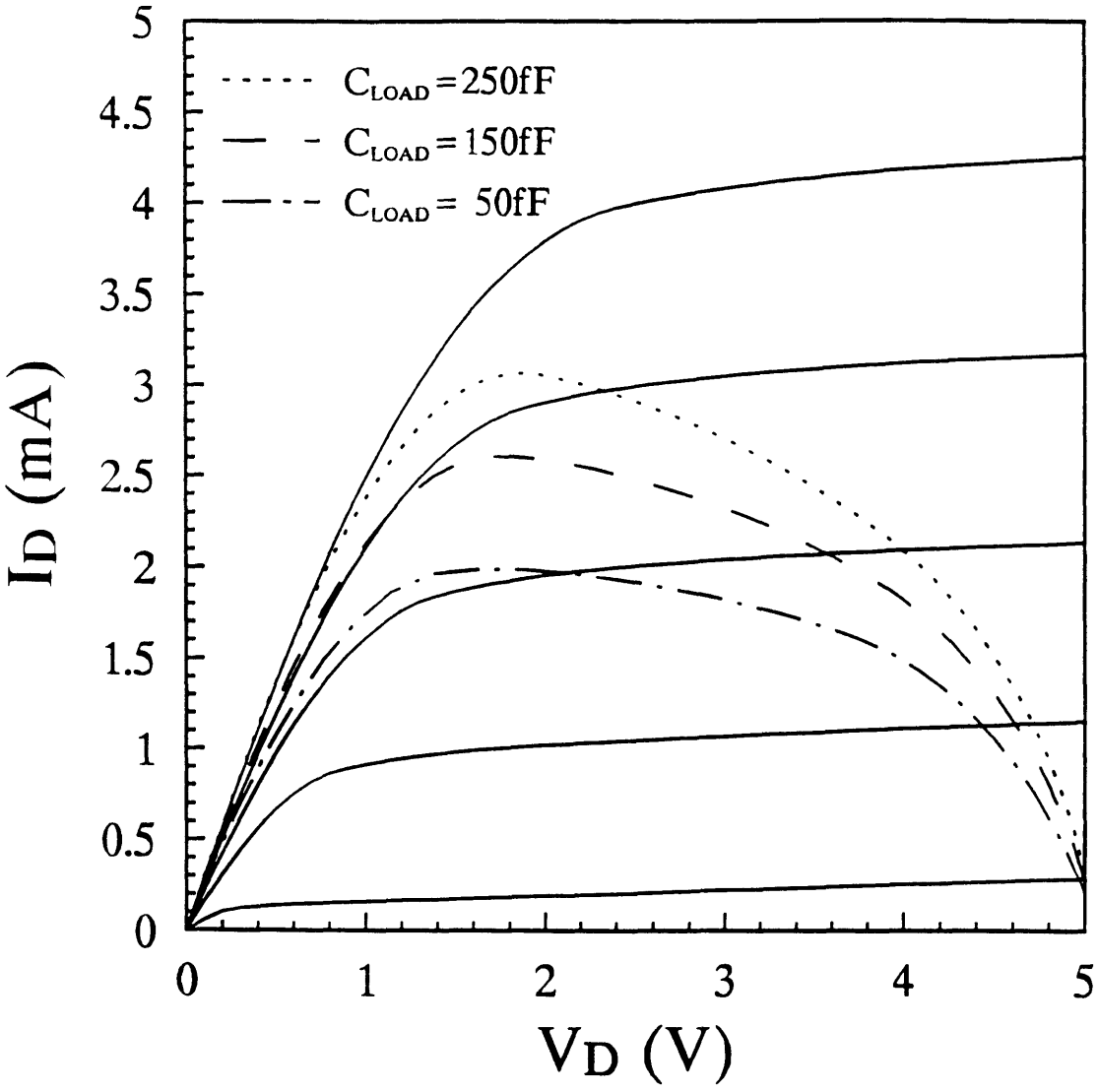

Fig. 2.8 Locus of I_D versus V_D for different C_{LOAD} conditions during NMOSFET discharge phase. The device has L_{EFF}=0.42μm, W=10μm. The solid curves are the device characteristics.

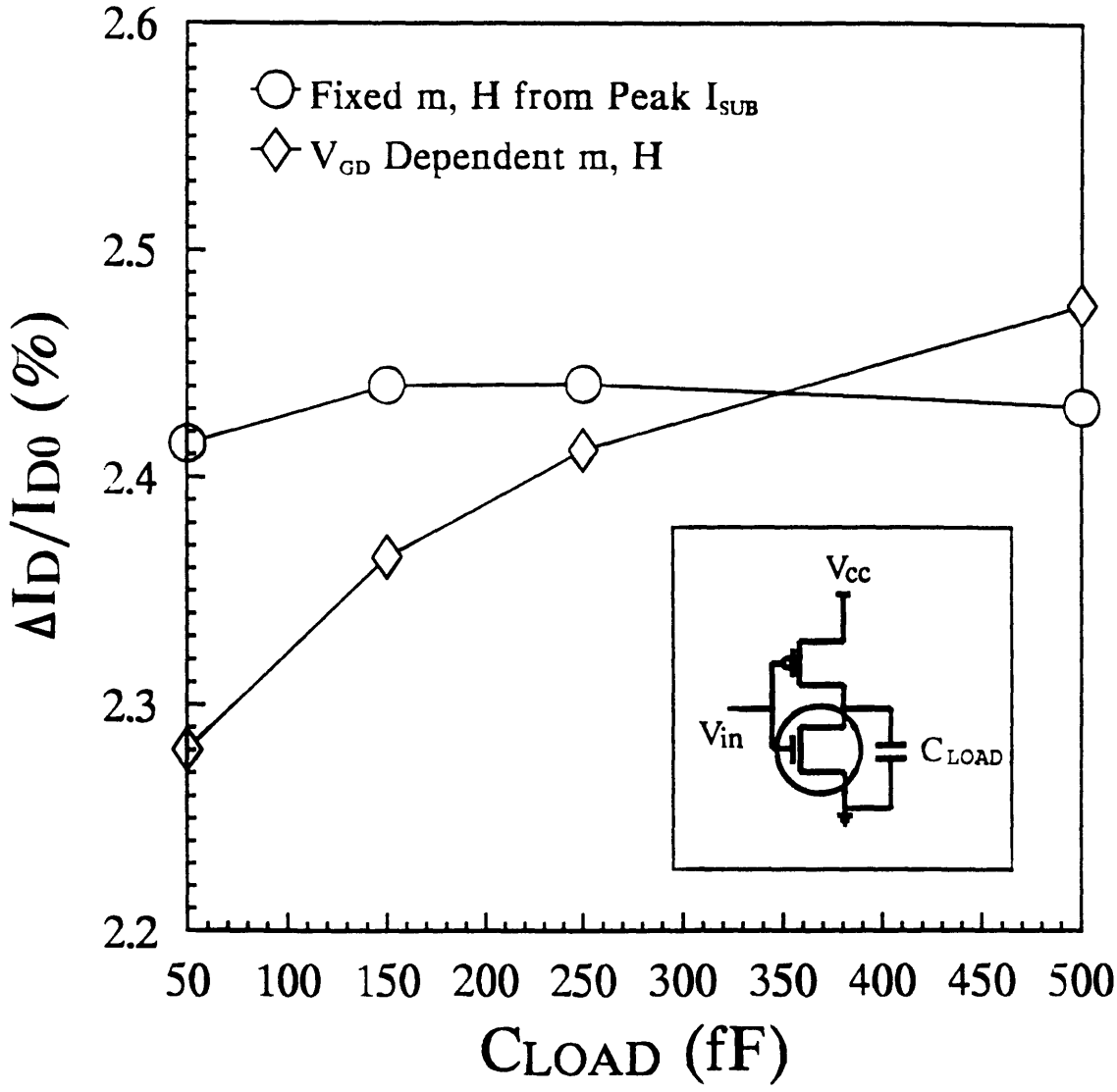

Fig. 2.9 Degradation induced in NMOSFET after 10 years with 100MHz signal. Degradation is calculated by using constant and V_{GD} dependent m and H coefficients.

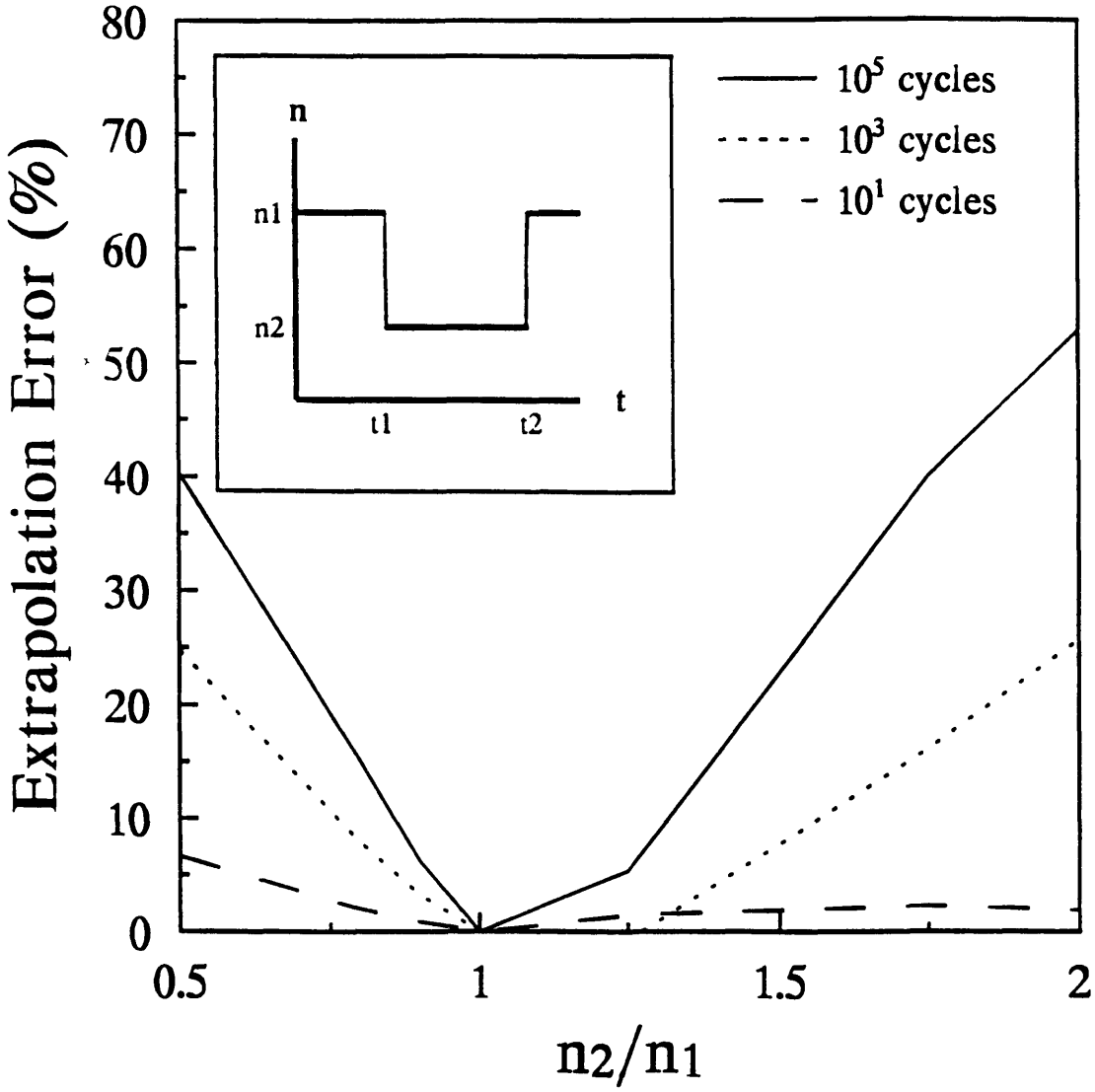

Fig. 2.10 Error due to constant n approximation for different cycles as a function of n2/n1. Insert illustrates the two-step assumption used in this calculation.

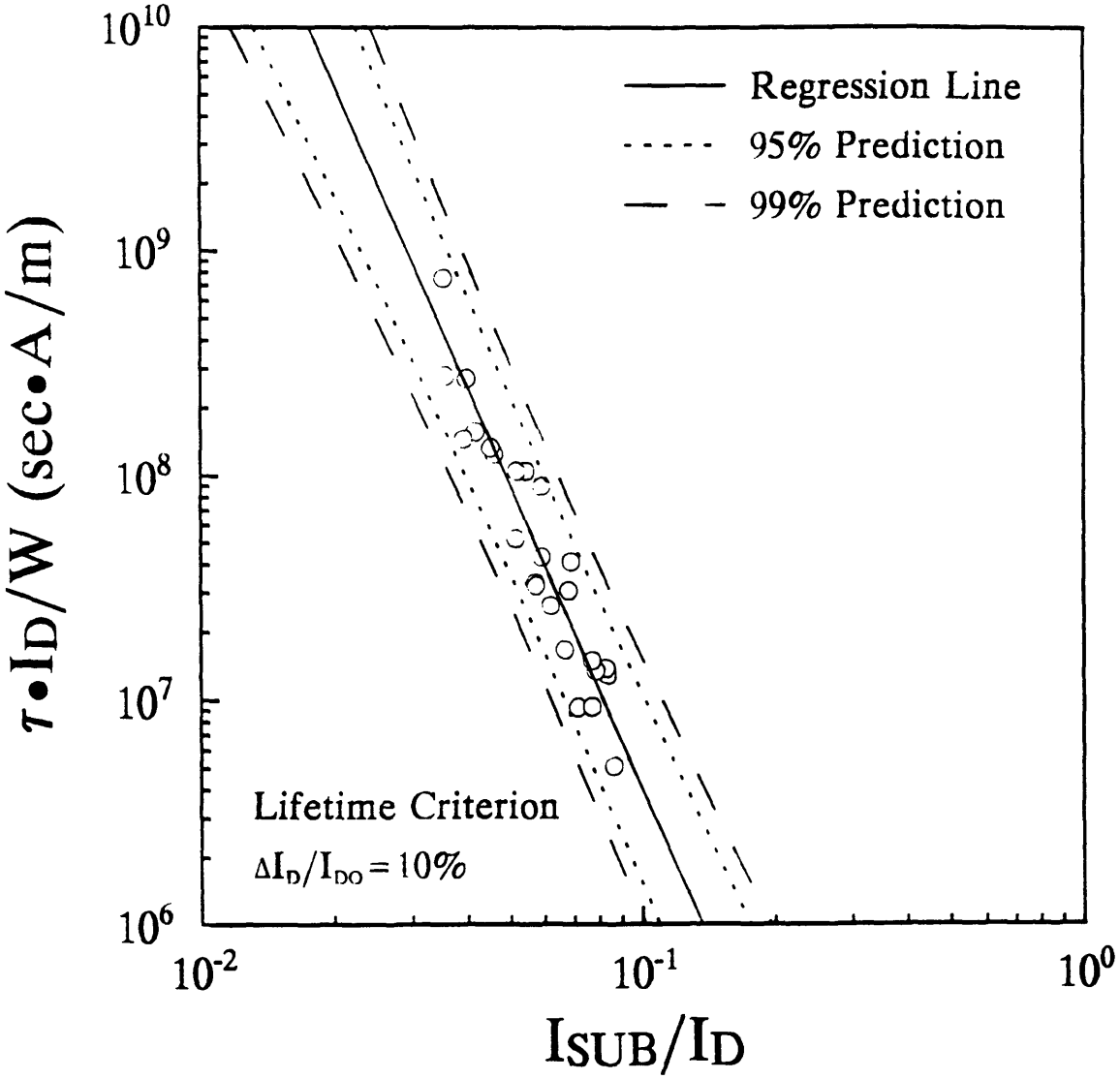

Fig. 2.11 Lifetime correlation plot with 95% and 99% prediction intervals.

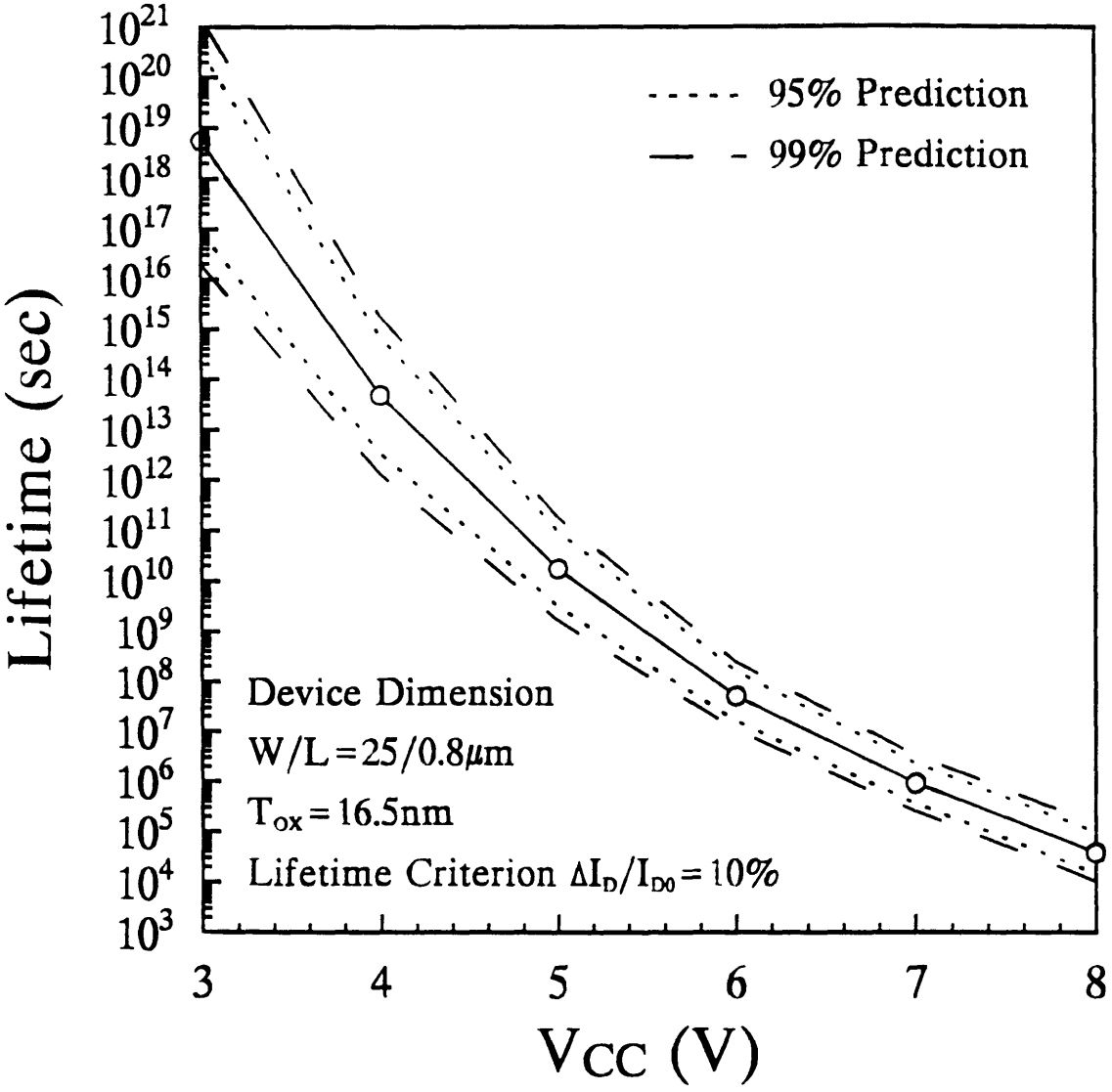

Fig. 2.12 Lifetime versus V_{CC} plot with 95% and 99% prediction intervals.

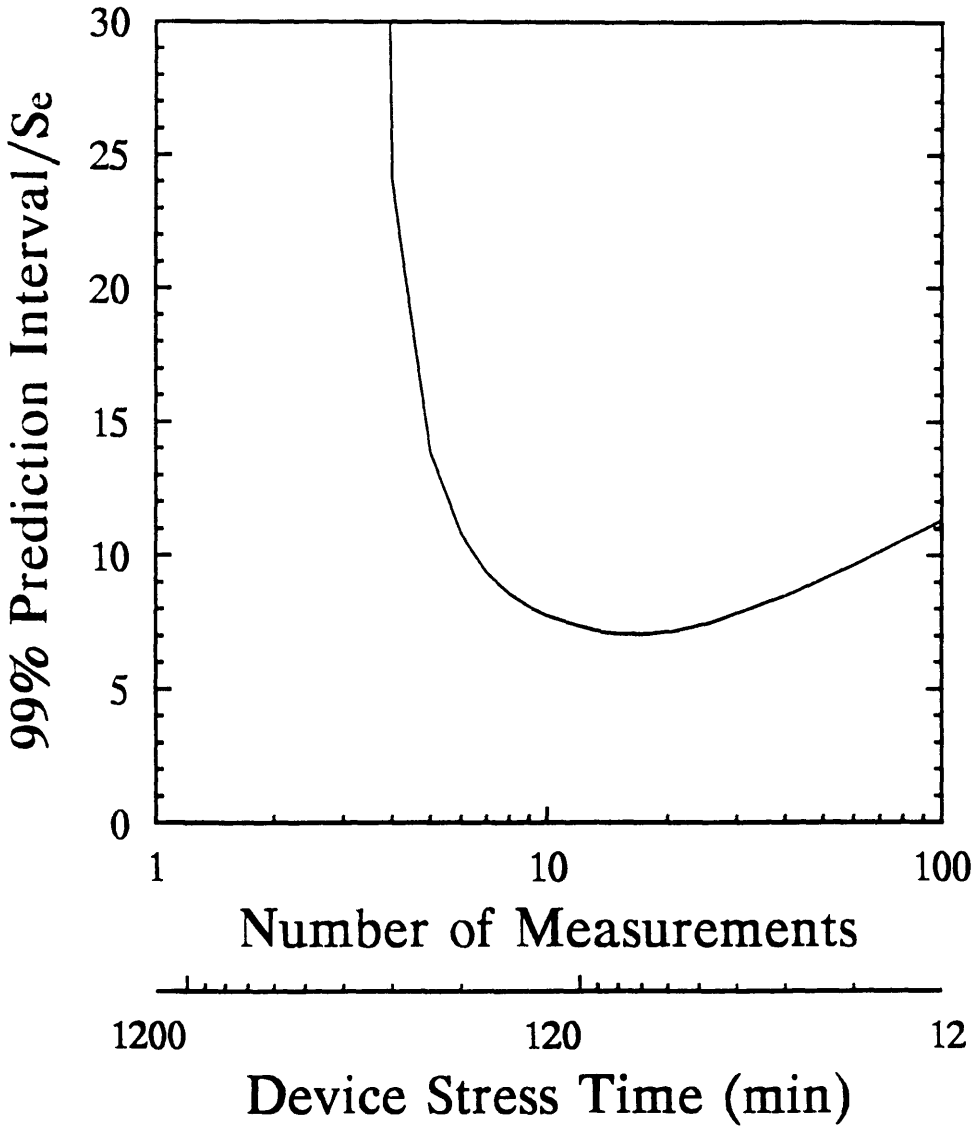

Fig. 2.13 Prediction interval versus number of measurements.

Chapter 3

Two-Stage Hot-Carrier Degradation in LDD NMOSFETs

3.1. Introduction

Lightly-doped drain (LDD) structures using oxide spacers are commonly used to reduce hot-carrier degradation for submicrometer NMOSFET devices [3.1]. However, it has been recognized that such LDD structures often introduce additional degradation mechanisms associated with the oxide spacers [3.2], where trapped electrons can increase the parasitic drain series resistance. As a result, the device I-V degradation characteristics often show different attributes, as compared to conventional single-drain devices [3.3]. One significant difference is that the linear-current degradation characteristic exhibits a saturating time dependence [3.4] which results in a stress-voltage-dependent degradation rate coefficient [3.5]. These saturating characteristics make the usual $A \cdot t^n$ time-dependence extrapolation technique inconsistent and inaccurate [3.6]. Therefore, the particular degradation mechanisms and time dependence of oxide-spacer LDD NMOSFET devices need to be understood in order to extract correctly the device lifetime.

Past studies have attributed this saturation behavior either to an increase in the potential barrier for hot-carrier injection [3.7], a shift in location of the damage region [3.8], or a saturation of mobility degradation [3.9]. However, these theories cannot fully explain additional degradation phenomena associated with oxide-spacer LDD NMOSFETs

such as substrate current variation during stress and degradation dependence on measurement gate voltage [3.10].

In this chapter, a two-stage degradation mechanism for oxide-spacer LDD NMOSFET devices is identified. The device degradation is due to a combination of an increase in the series resistance underneath the LDD spacer region, and a reduction of carrier mobility in the subdiffusion and channel regions. This two-stage degradation mechanism can fully explain the hot-carrier degradation characteristics of a oxide-spacer LDD NMOSFET. By taking the saturation of the series-resistance increase into account and by using an asymptotic degradation rate coefficient, a more accurate and consistent value of the device lifetime can be extracted.

3.2. Experimental Methodology

The NMOSFET devices used in this study were fabricated using a 0.8μm double-level metal, CMOS process with conventional oxide-spacer LDD structures. The spacer length is approximately 0.22-0.25μm with a peak n^- concentration of $3 \cdot 10^{18} cm^{-3}$. The NMOSFET dimensions are T_{ox}=19nm, L_{EFF}=0.59μm, and W=20μm for all measurements in this study. DC stress was performed by using constant-voltage stress conditions. Linear-current degradation (measured at V_D=0.05V and V_G=3V) and charge-pumping current (measured by applying a 100KHz, 8V peak-to-peak square wave to the gate) are the two primary degradation monitors.

3.3. Two-Stage Hot-Carrier Degradation

3.3.1. Degradation Characteristics

Fig. 3.1 and Fig. 3.2 show typical time dependence plots of the linear-current degradation and the corresponding increase in charge-pumping current, which is directly

proportional to the number of hot-carrier-induced interface states [3.11], [3.12]. Note that the degradation rate (slope of the time-dependence plots) in both figures decreases for increasing stress time (i.e. the degradation saturates) [3.4]. In addition, the value of the degradation rate coefficient also depends on the value of the particular applied stress voltage as has been previously observed in [3.5]. Both of these degradation characteristics are commonly observed in submicrometer oxide-spacer LDD NMOSFET devices [3.4]-[3.6], [3.8]-[3.10], but not typically in conventional devices [3.11], [3.13].

Because rate coefficients vary for different stress voltages (see Fig. 3.1), the choice of the lifetime criterion is critical if the conventional $A \cdot t^n$ time-dependence extrapolation is used [3.6]. Different criteria can result in different lifetime correlations as shown in Fig. 3.3. This result can not be physically accurate, because the slope of the lifetime correlation plot, which is proportional to the critical energy for interface-state generation [3.13], should not depend on the particular chosen definition for device lifetime. Clearly, the current hot-carrier degradation model can not be directly applied to LDD NMOSFET devices. The detailed degradation mechanisms need to be investigated in order to construct a correct lifetime extraction procedure.

3.3.2. A Two-Stage Degradation Process

The observed phenomena in Fig. 3.1 and Fig. 3.2 can be attributed by a two-stage degradation process in LDD NMOSFETs. This two-stage degradation is evident from the correlation plot between linear-current degradation and charge-pumping current. In conventional single-drain devices, the typically observed linear relationship between $\Delta I_D/I_D$ and ΔI_{CP} indicates a single degradation mechanism which is mobility reduction [3.11]. For oxide-spacer LDD devices, the correlation exhibits two distinct regions as shown in Fig. 3.4. In region I, the linear-current degradation will be shown to be dominated by the increase in parasitic drain resistance underneath the spacer region. In region II, the degradation will be shown to be mostly due to mobility reduction, as in the case of conventional devices.

This two-stage degradation process can also explain how the linear-current degradation depends on the particular measurement gate voltage as shown in Fig. 3.5. At first, the dominant degradation mechanism is the increase in drain series resistance. For larger measurement V_{GS}, the channel resistance becomes smaller and the device is affected more by an increase in the series resistance. As a result, the liner-current degradation worsens as the measurement gate voltage increases. However, as the stress proceeds further, the dominant degradation mechanism changes to mobility reduction. For a larger measurement V_{GS}, the vertical electric field becomes stronger and the mobility is less affected by stress-induced interface states, as is observed in conventional devices [3.11]. Therefore, the current degradation now decreases as the measurement gate voltage increases.

During the stress, the observed changes of substrate current (Fig. 3.6) are also a result of the two-stage degradation process. The substrate current only increases during hot-carrier stress for conventional single-drain devices. However, for LDD devices, substrate current first decreases, then increases. This variation is a result of the changes in the channel electric field near the drain [3.14].

$$E_D \sim \frac{V_{DS}-V_{DSAT}}{l_C} \sim \frac{V_{DS}-V_{GS}+V_T}{l_C} \qquad (3.1)$$

In the beginning of the stress, because of the increase in drain series resistance, the effective drain voltage (V_D-I_D·R_D) is reduced, and thus the channel electric field decreases (see (3.1)). As a result, the substrate current at first decreases. As the stress proceeds, however, the substrate current eventually increases due to the stress-induced increase in the threshold voltage which now results in a larger lateral electric field as shown in (3.1).

3.4. Physical Mechanisms

In order to understand this two-stage degradation process, interface states have

been spatially profiled by charge-pumping experiments [3.15], and their extracted lateral spatial distribution has been incorporated into PISCES-IIB [3.16] to simulate the device current characteristics. The technique of spatial charge pumping is illustrated in Fig. 3.7. The drain/source reverse bias is used to control the depletion width below the gate which, in turn, regulates the effective charge-pumping region. By varying the reverse-bias voltage, and thus modulating the effective charge-pumping region, the lateral spatial distribution of interface states can be obtained. A critical hole concentration ($P_s^{CRIT.}$) at the surface, which allows all the electrons trapped in interface states to recombine, demarcates the effective charge-pumping region. Based on a previous study [3.12], the critical hole concentration is calculated to be $10^{14}cm^{-3}$ for a 100KHz symmetrical square-wave gate pulse. The actual surface hole concentration in the device was determined by PISCES-IIB device simulation.

The extracted lateral profile of acceptor-type interface states is shown in Fig. 3.8. It shows that the peak interface-state damage occurs inside of the LDD region which is consistent with reported experimental [3.17] and simulation [3.18] results. This result is expected since peak electric field exists inside the LDD region. Because this damage is located outside of the immediate region of gate-electrode control, V_T and subthreshold slope shifts for LDD NMOSFET devices due to hot carriers are usually much smaller in the beginning than that for conventional devices. Non-negligible interface-state generations also occurs in subdiffusion and channel regions as shown in Fig. 3.8. Therefore, as stress proceeds and more negative charge accumulates outside the LDD region, threshold voltage will start to increase.

The impact of interface charge within the different device regions (Fig. 3.9) is simulated by placing negative charges along SiO_2-Si interface in PISCES-IIB. The damage in the LDD region, which creates a depletion region, increases the drain series resistance [3.2]. Damage in the subdiffusion and channel region (which is under gate electrode control), induces Coulombic scattering, reducing the carrier mobility as in the case of conventional devices [3.11]. The increase in series resistance eventually saturates [3.4] as shown in Fig. 3.9, as enough negative charge is trapped to induce surface

inversion which limits any further growth of the depletion width. However, the degradation mechanism of mobility reduction continues to exist and is approximately linearly-dependent on the amount of interface charge outside of the LDD region. The combination of these two mechanisms creates the saturation effects observed in the experimental degradation data (Fig. 3.1 and 3.2). By comparison, damage inside the heavily-doped drain in conventional devices produces very little current degradation (Fig. 3.10), although the characteristics of current degradation due to interface states in the subdiffusion and channel regions are quite similar. Note, that saturation of drain series resistance depends on critically on the drain donor concentration as shown in Fig. 3.9 and 3.10.

3.5. Impact on Lifetime Prediction

By combining the effects of series-resistance increase and mobility reduction, the linear-current degradation for LDD NMOSFETs can be expressed as

$$\frac{\Delta I_D}{I_D}(t) = f(R_D(t)) + \left[\frac{I_D}{W \cdot H} \cdot \left(\frac{I_{SUB}}{I_D} \right)^m \cdot t \right]^n \qquad (3.2)$$

where W is the device width; n is the degradation rate coefficient; m and H are technology-related parameters. The first term represents the current reduction due to the increase in drain series resistance, and the second term represents the contribution of mobility reduction which follows the same model as in conventional devices [3.11]. The exact functional form of $f(R_D(t))$ is unknown. However, it is not important in lifetime extrapolation, as $f(R_D(t))$ will eventually saturate as shown in Fig. 3.9 and this saturation value is usually much lower than typical lifetime criterion. By using the asymptotic value of the degradation rate coefficient n, as suggested in (3.2), existing NMOS degradation models [3.13] can still be employed to project the device lifetime for oxide-spacer LDD NMOSFETs.

By subtracting the degradation due to the saturated increase in series resistance and by using the asymptotic degradation rate coefficient, the hot-carrier lifetime correlation can then be expressed as

$$\frac{\tau \cdot I_D}{W} = H \cdot \left[\left. \frac{\Delta I_D}{I_D} \right|_{lifetime\ criterion} - f(R_D(\infty)) \right]^{\frac{1}{n}} \cdot \left(\frac{I_{SUB}}{I_D} \right)^{-m} \qquad (3.3)$$

where $f(R_D(\infty))$ is the maximum amount of current reduction due to the saturated series resistance increase (shown in Fig. 3.11) and is about 3% for our devices. Fig. 3.11 illustrates how to use the asymptotic value of the rate coefficients to extract the correct lifetime. Note that, the slopes of the asymptotes are now independent of the stress voltages (compare Fig. 3.1 and 3.11). Fig. 3.12 shows that the ideal $A \cdot t^n$ time dependence, using the asymptotic rate coefficient, is still maintained even for a device which was stressed for times as long as 10^5 mins with degradation level as high as a 30% $\Delta I_D/I_D$ reduction. This suggests that the new proposed technique will be suitable for most lifetime extraction purposes. As shown in Fig. 3.13, with the series resistance correction, the lifetime correlation plots based on (3.3) can be obtained consistently, independent of the particular lifetime definition chosen.

3.6. Conclusions

In this chapter, I have shown that the degradation of oxide-spacer LDD NMOSFET devices is due to a combination of the series-resistance increase in the LDD region, and the carrier-mobility reduction in other regions. As a result, the time dependence of hot-carrier degradation exhibits strong saturating characteristics. Thus, in order to extract a more accurate and consistent lifetime value, the device must be stressed long enough for the increase in series resistance to saturate. Then, the lifetime of LDD devices can be extracted by using asymptotic rate coefficients based on the usual extrapolation method.

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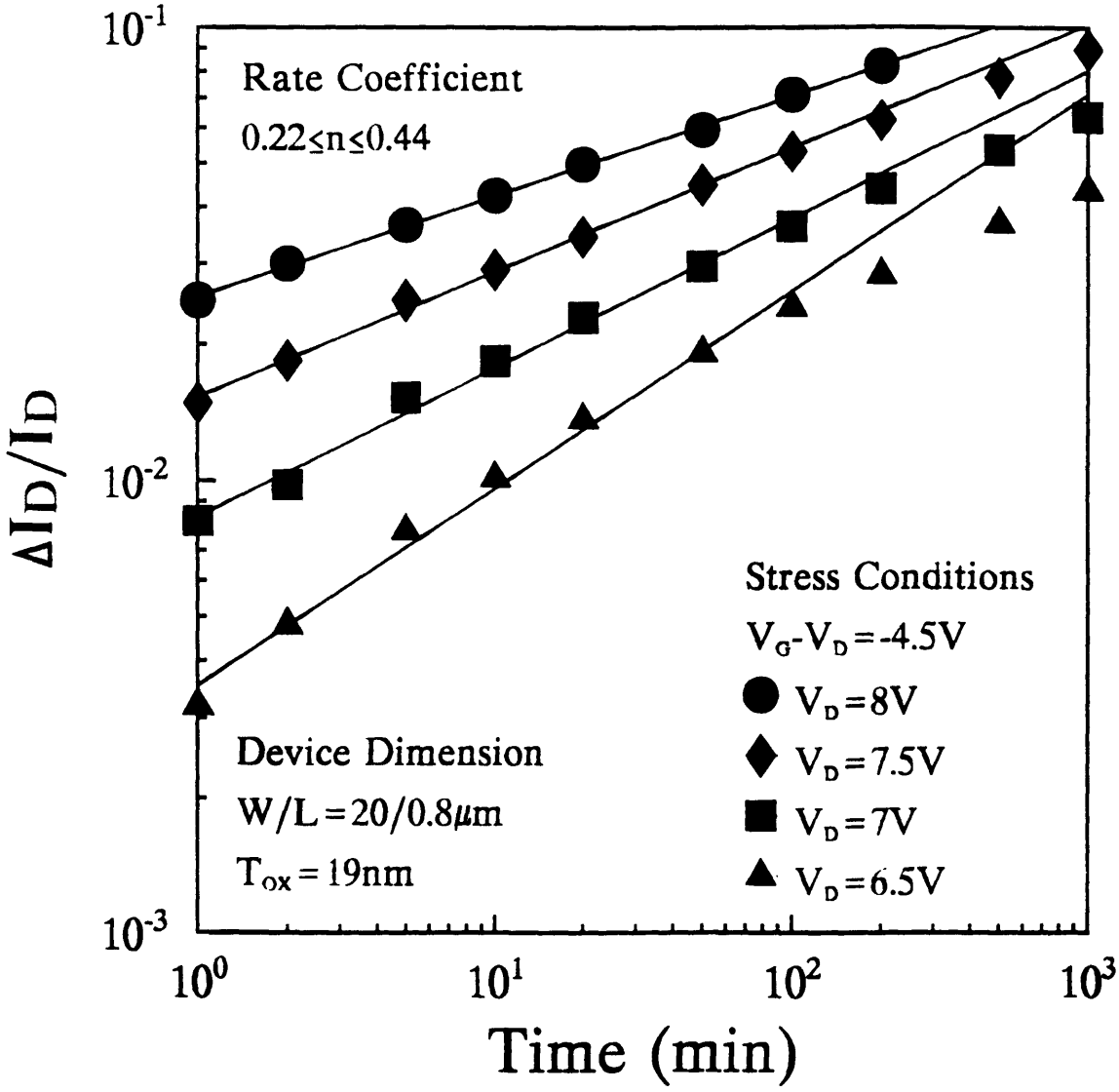

Fig. 3.1 Time dependence of the linear-current degradation. I_D was measured at V_D=0.05V and V_G=3V. Linear regression lines which were used to fit the initial slopes are also shown.

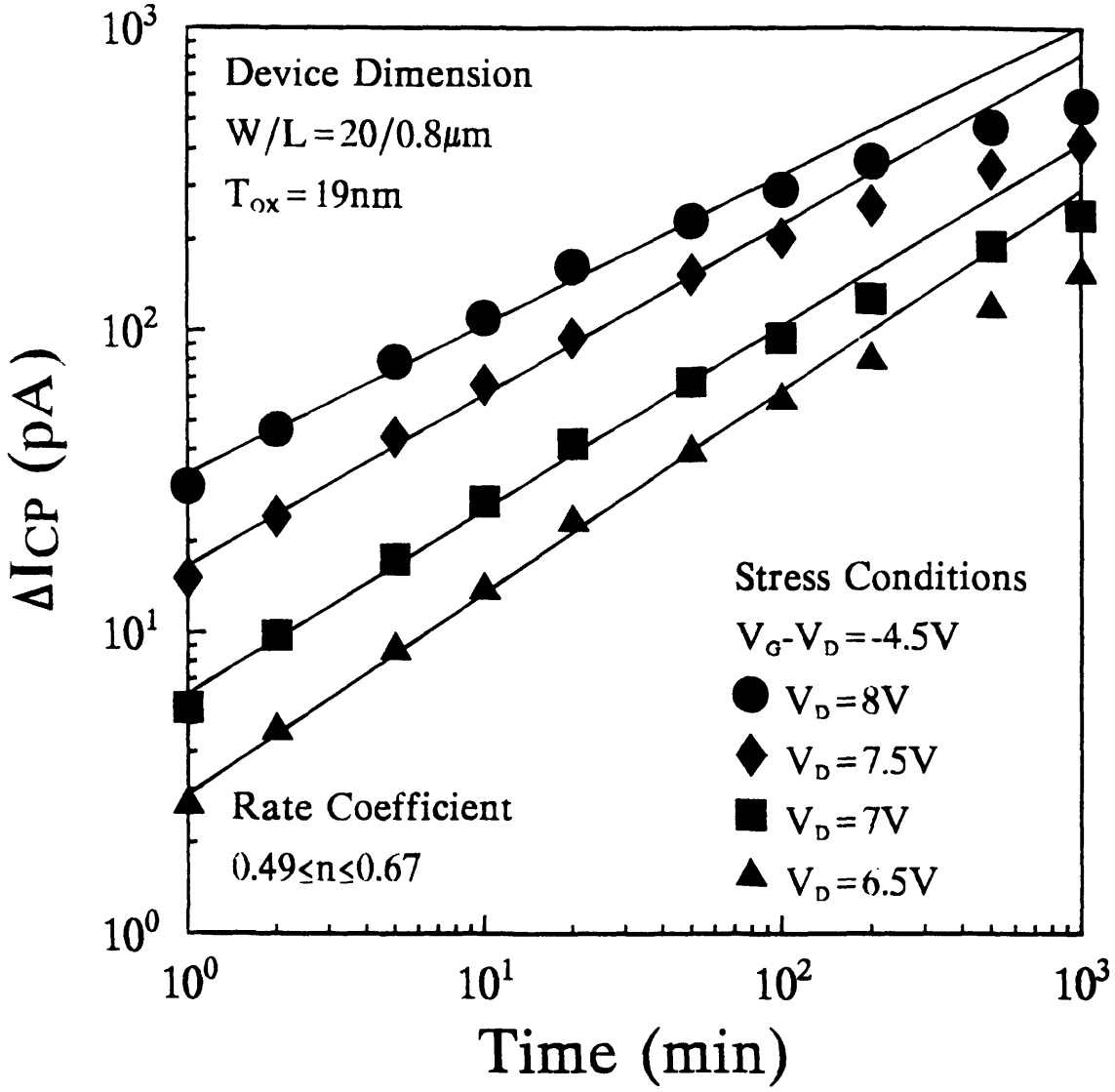

Fig. 3.2 Increase of charge-pumping current which was measured at f=100KHz and ΔV=8V after hot-carrier stress. The linear regression lines are also shown.

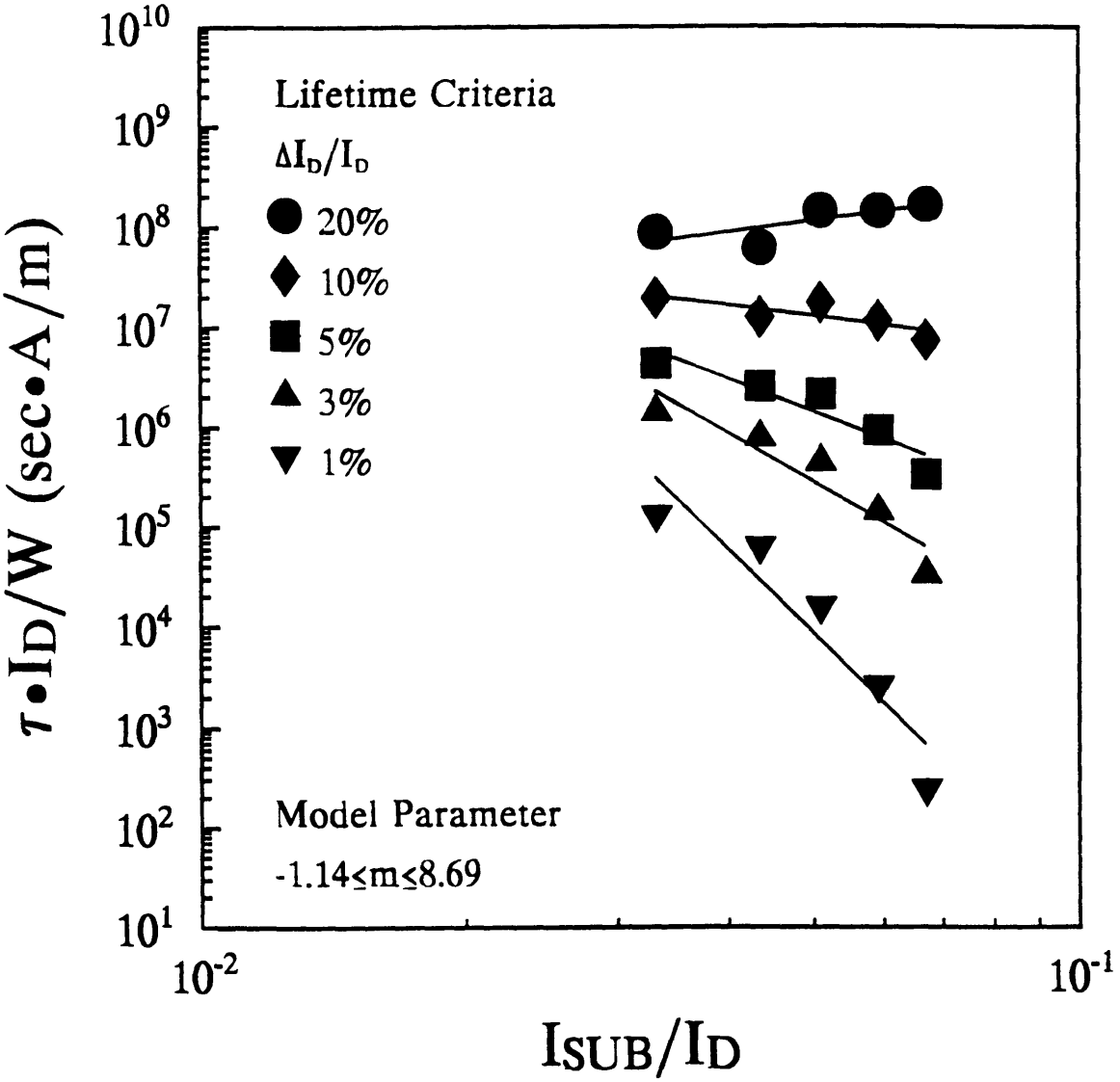

Fig. 3.3 Lifetime correlation of oxide-spacer LDD NMOS transistors for fixed V_{GD}=-4.5V stress using conventional lifetime extrapolation techniques.

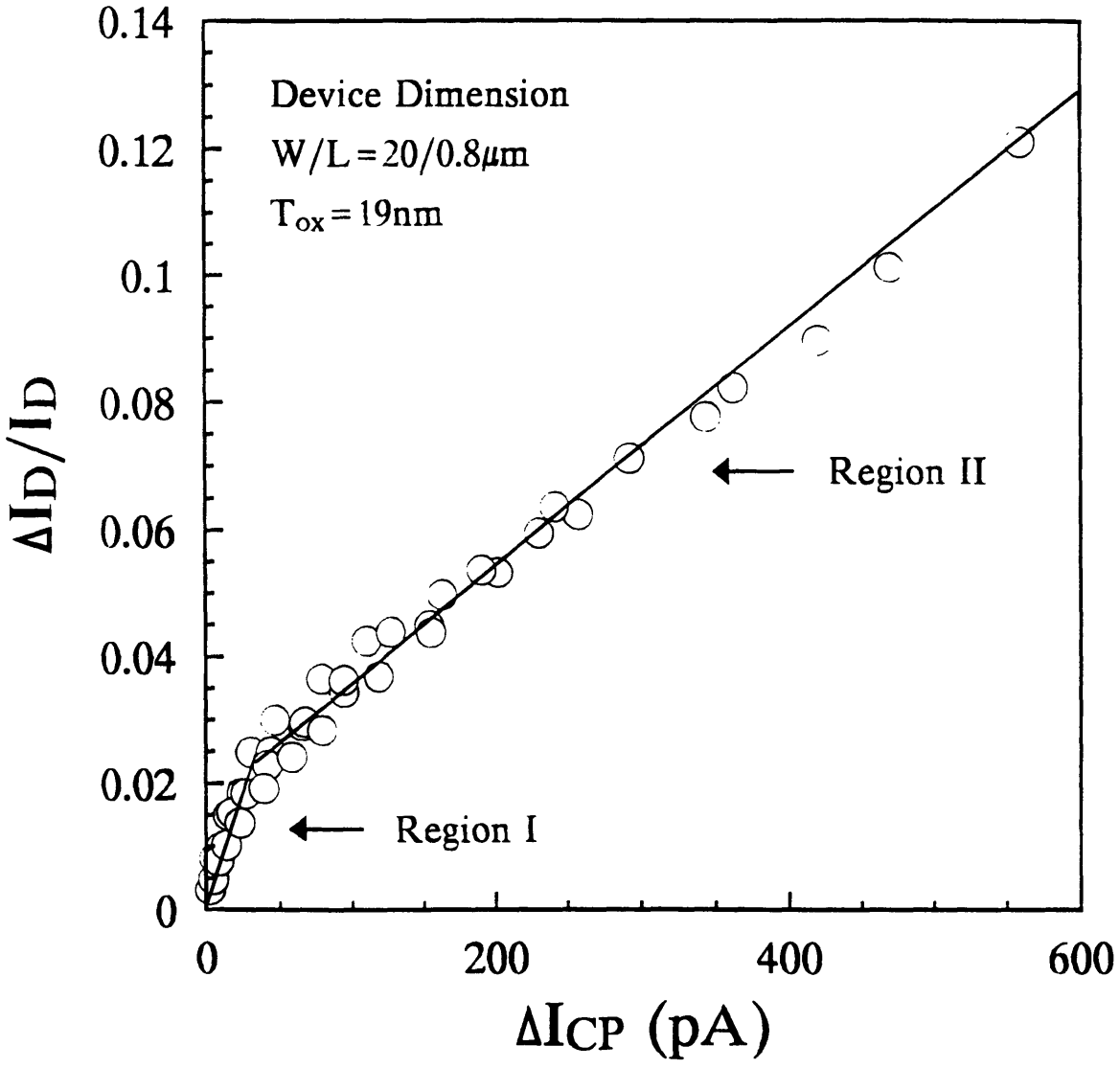

Fig. 3.4 Relation between the linear-current degradation and charge-pumping current for several stressed devices.

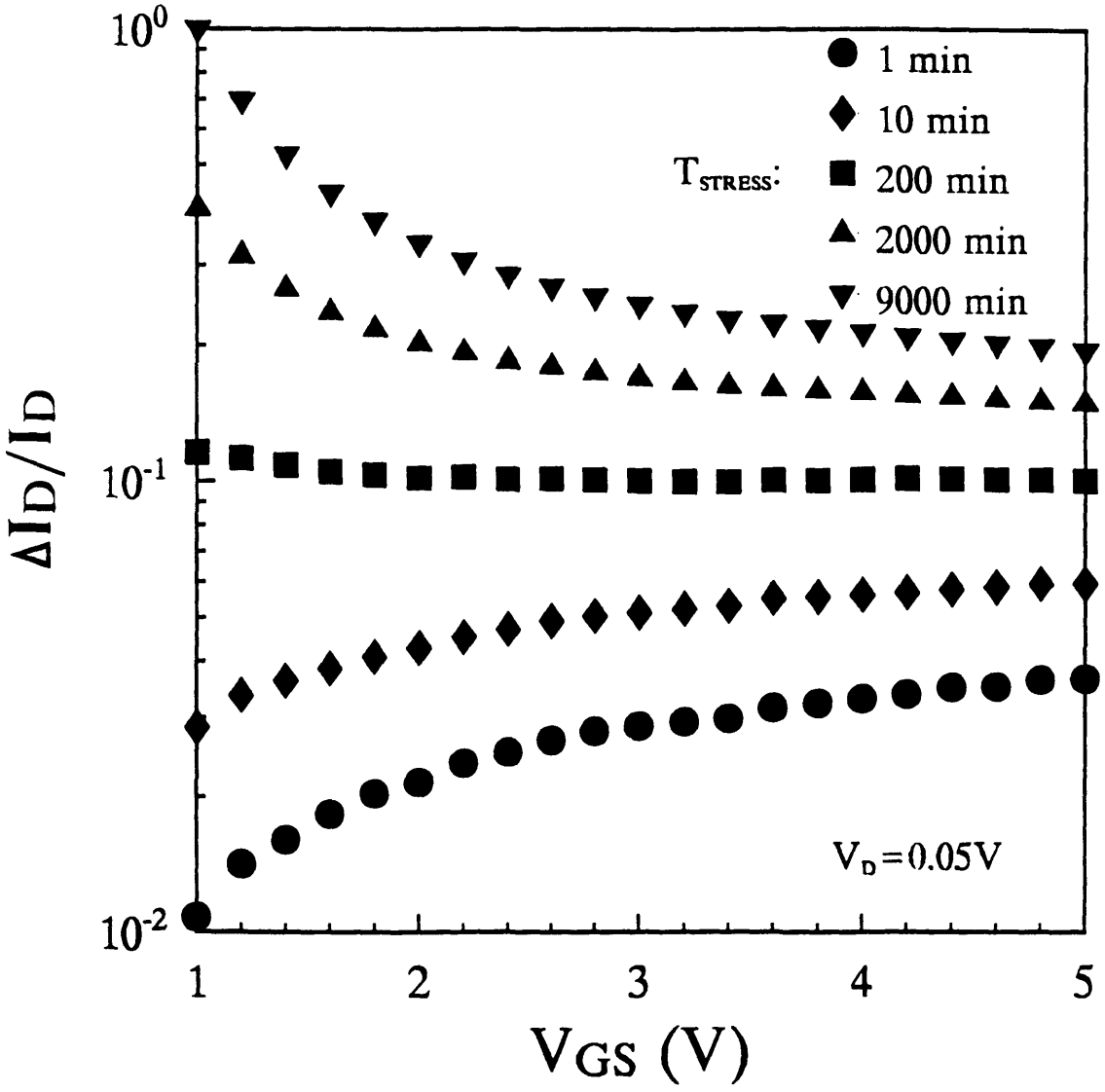

Fig. 3.5 Measurement voltage dependence of the linear-current degradation. Stress condition: V_D=8.3V and V_G=3.8V.

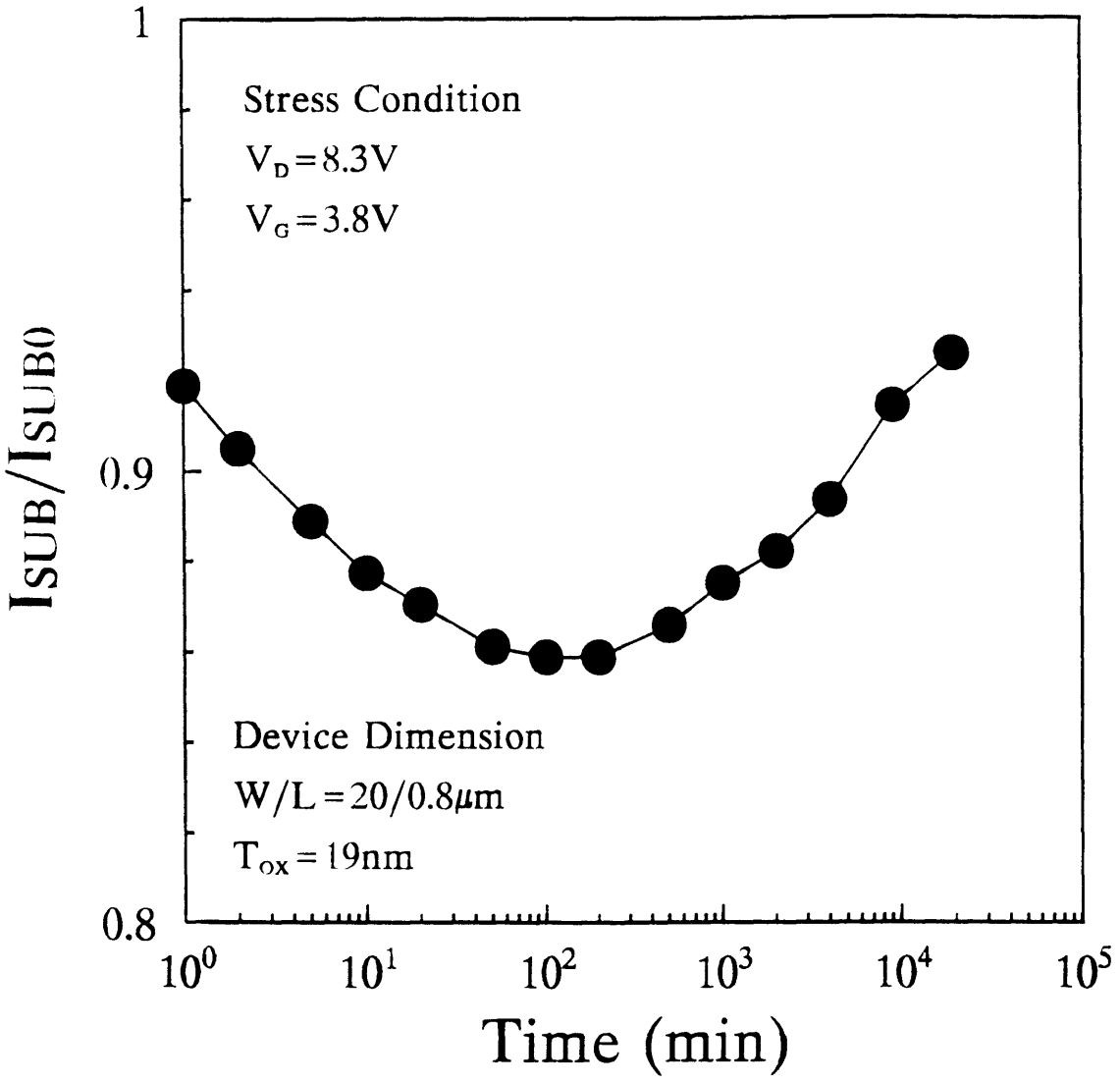

Fig. 3.6 Substrate current variation during the hot-carrier stress.

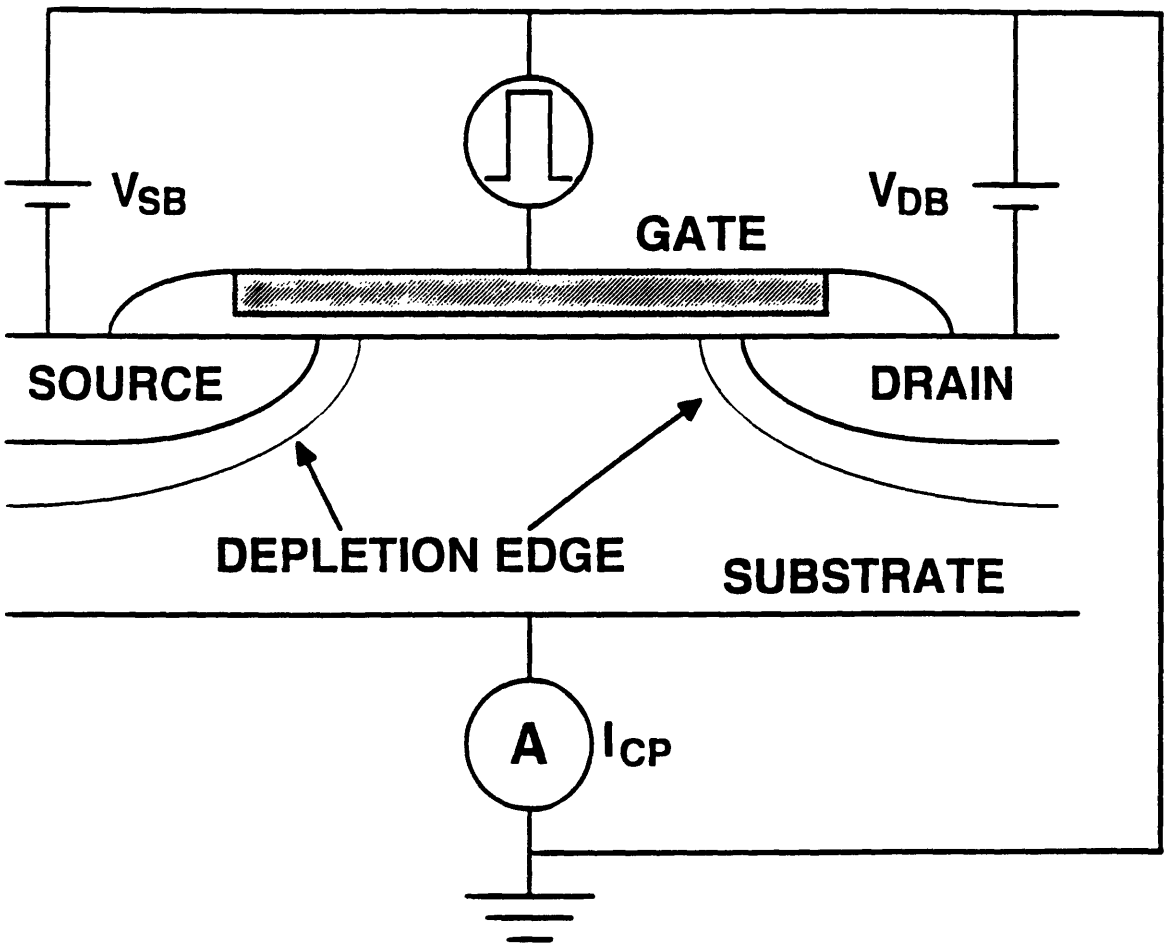

Fig. 3.7 Schematics of spatial charge-pumping experiment.

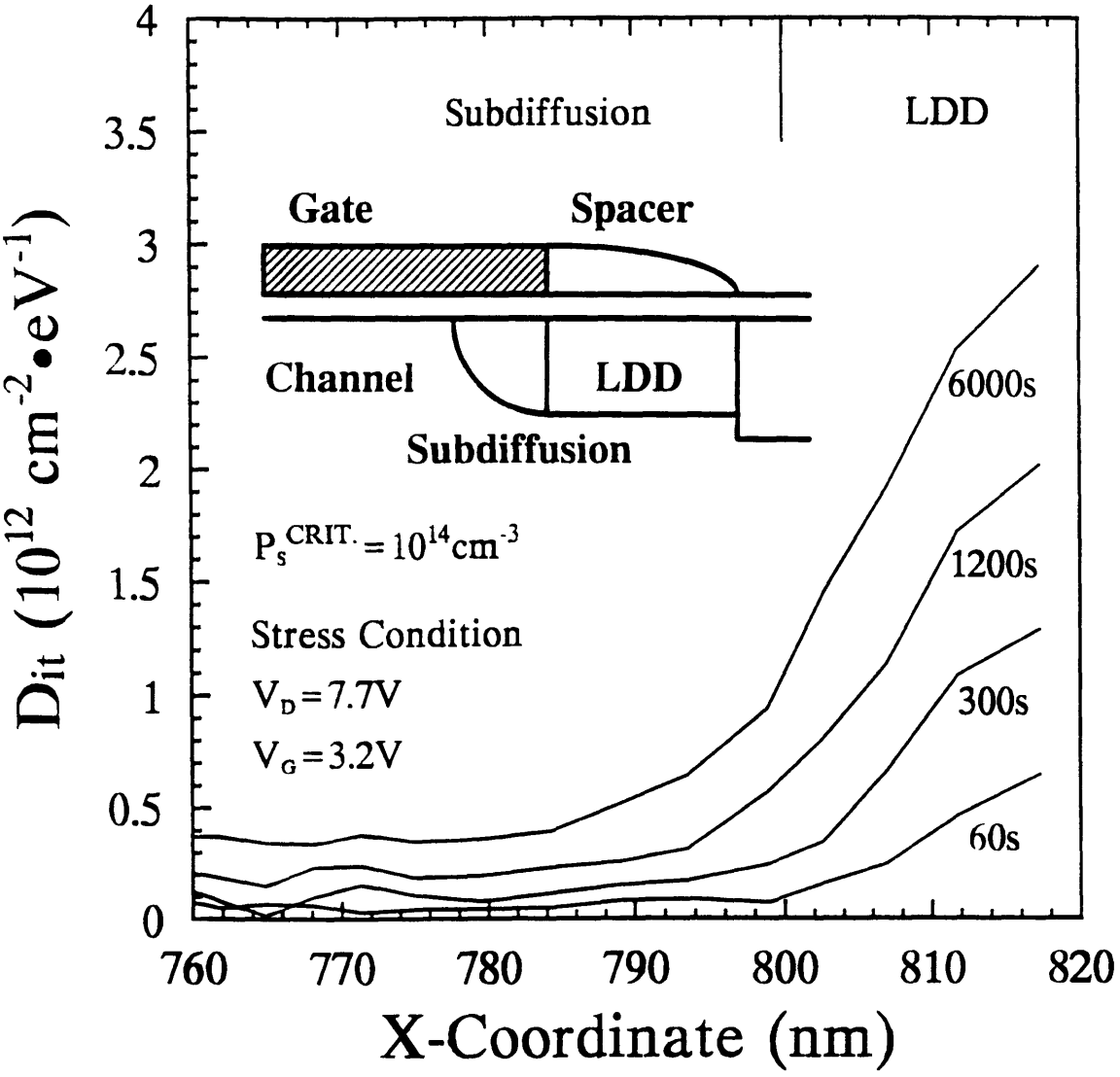

Fig. 3.8 Extracted lateral interface-state distribution along the transistor. The critical hole concentration $P_S^{CRIT.}$ determines the effective charge-pumping region.

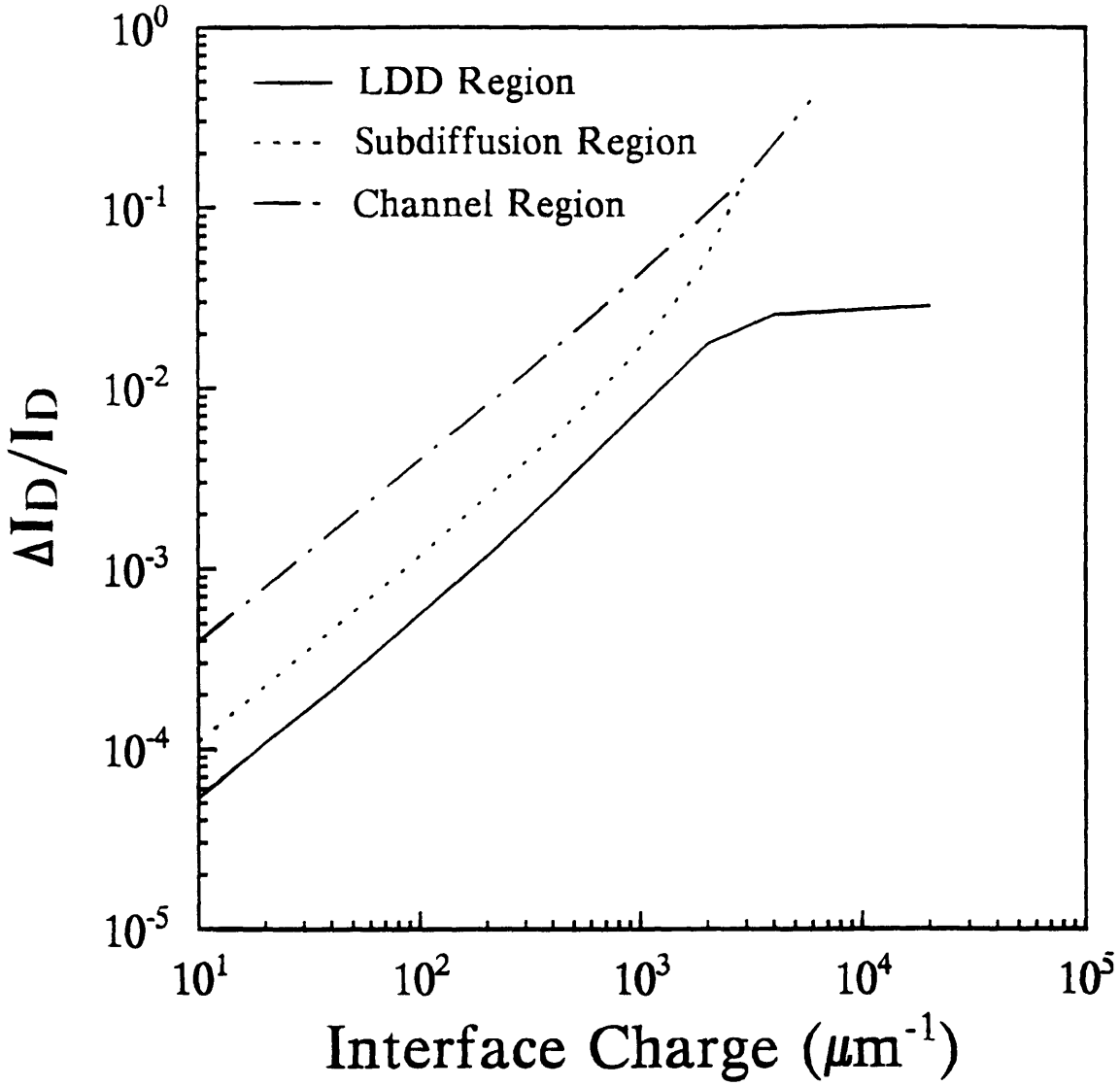

Fig. 3.9 Linear-current degradation simulated at V_D=0.05V and V_G=3V versus interface charges in different regions for oxide-spacer LDD NMOSFETs.

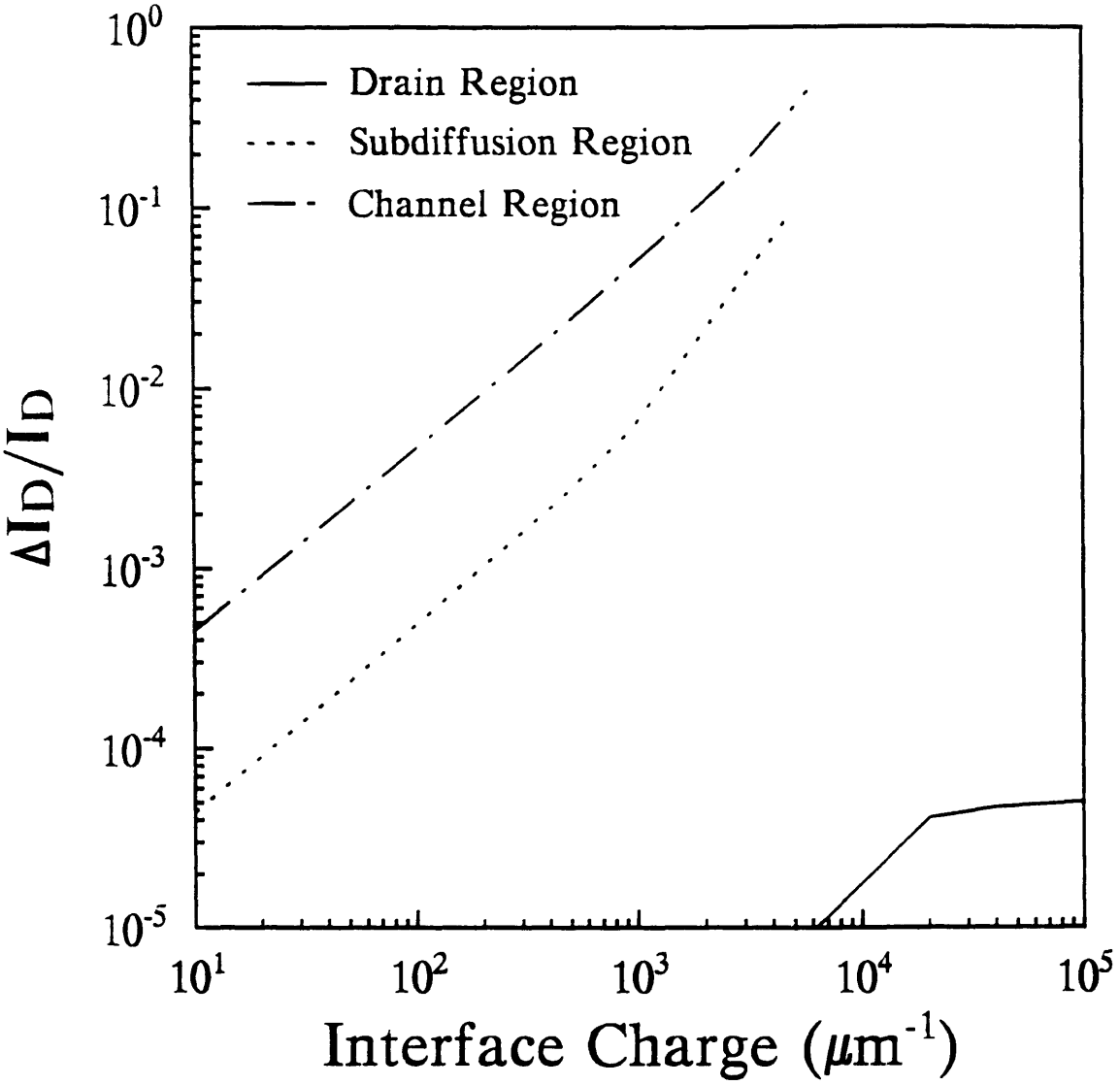

Fig. 3.10 Linear-current degradation simulated at V_D=0.05V and V_G=3V versus interface charges in different regions for conventional NMOSFETs.

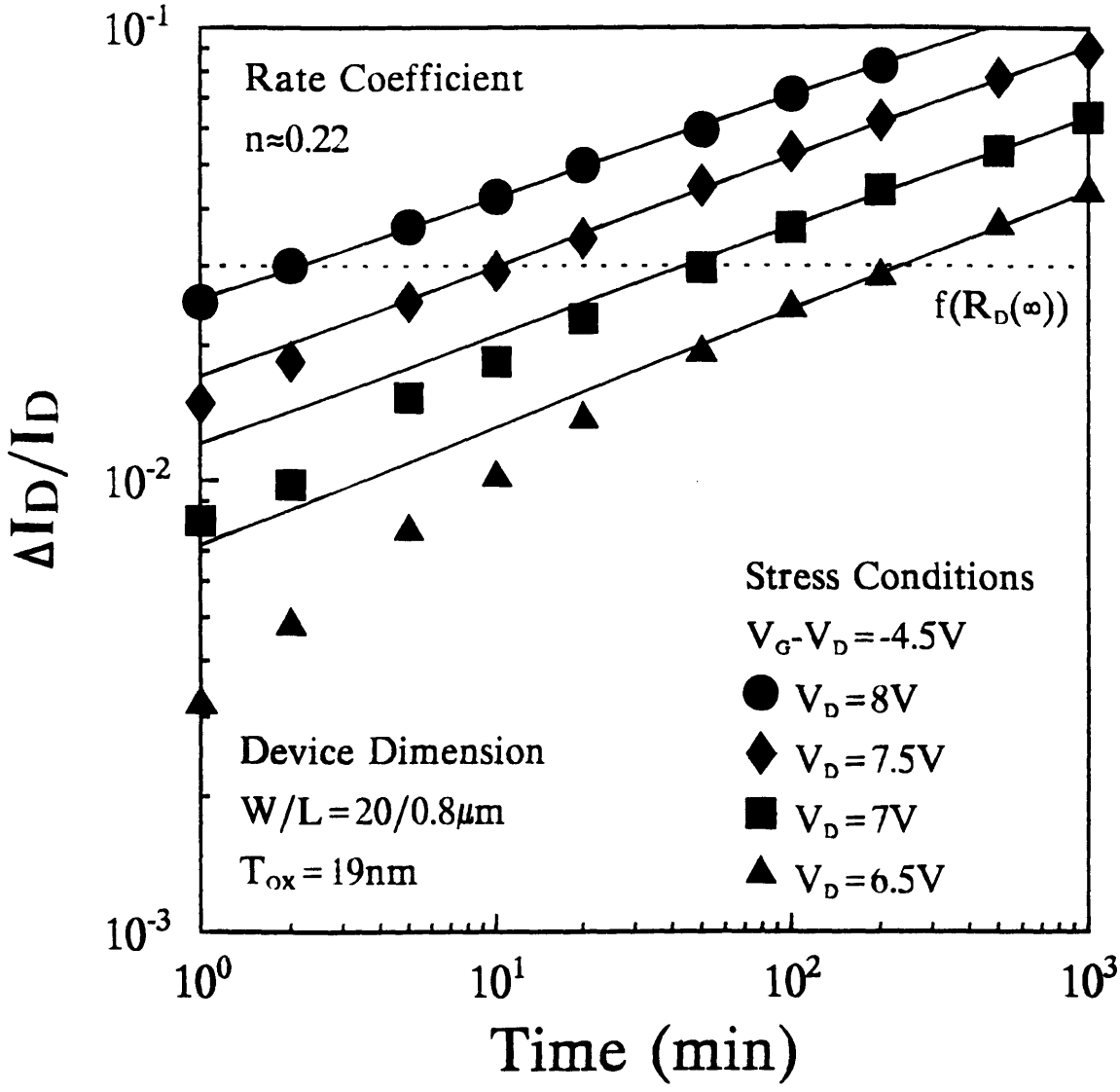

Fig. 3.11 Time dependence of the linear-current degradation as in Fig. 1. The solid lines are asymptotes of the degradation time dependence.

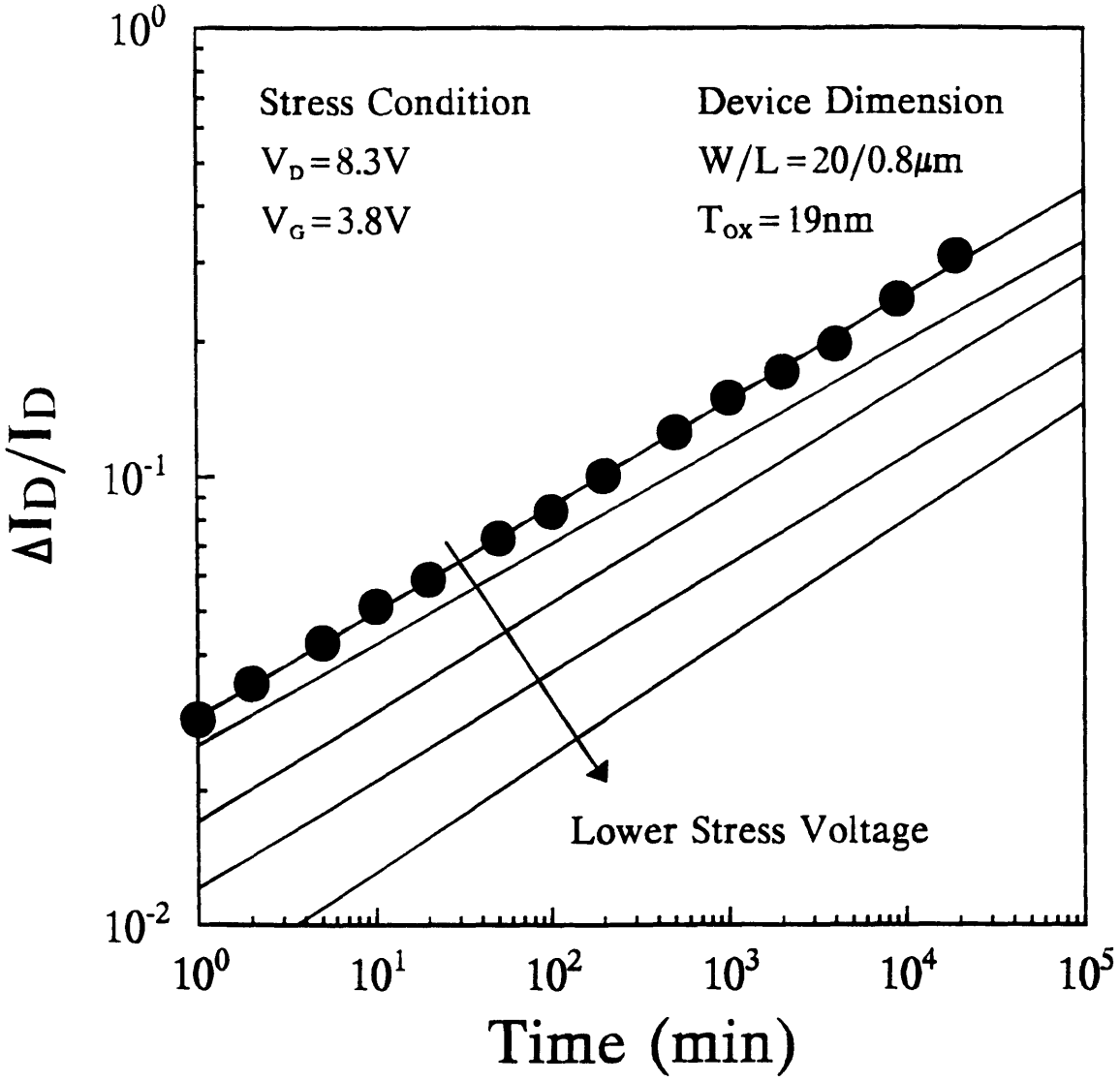

Fig. 3.12 $A \cdot t^n$ time dependence for a LDD NMOS transistor up to 30% $\Delta I_D/I_D$ degradation. Several extrapolated degradation from Fig. 11 are also shown.

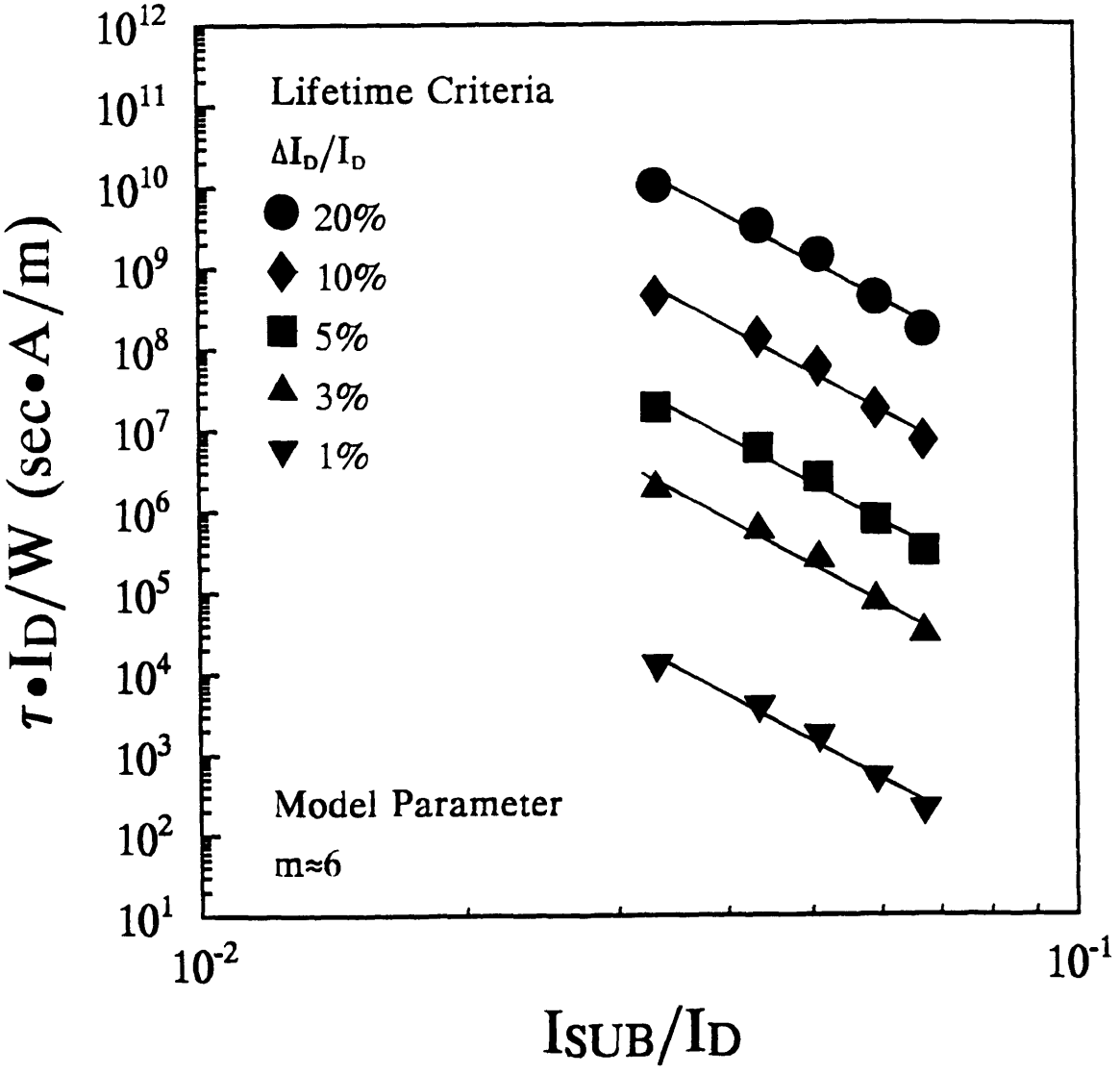

Fig. 3.13 Lifetime correlation of oxide-spacer LDD NMOS transistors for fixed V_{GD}=-4.5V stress with series resistance correction.

Chapter 4

Digital Circuit Degradation

4.1. Introduction

As switching frequencies continue to increase, greater concern exists about the validity of existing quasi-static device-level hot-carrier reliability criteria under very short voltage transient conditions [4.1]-[4.9]. Because hot-carrier degradation is extremely sensitive to the applied voltage waveforms, different test configurations employed in past studies produced different results. The common problems associated with these past experiments are: (1) excessive inductive noise is generated by the test setup in short-transient pulsed AC device measurements; (2) the hot-carrier stress is conducted using artificial operating conditions with either very long voltage transients or unrealistic voltage waveforms; and (3) the degradation of devices and circuits is not directly measured and compared. As a result, whether DC degradation models can be applied to circuit operation conditions is not fully tested and resolved.

In this chapter, on-chip circuit-level test structures will be used to remedy these problems. High-frequency operation and short voltage transients are achieved by using state-of-the-art submicrometer CMOS digital static-logic circuits to reflect realistic circuit operations and to avoid the setup-induced-inductive noise present in the typical pulsed device stress experiments [4.3], [4.8]. Direct measurements of device- and circuit-level hot-carrier degradation are made through these structures to examine the various degradation mechanisms and their characteristics for both NMOSFET and PMOSFET

devices. The AC and DC device degradation results are compared directly. The result will be used to evaluate the validity of the quasi-static approximation. The impact of device degradation on stage delay time of CMOS static logic circuits will be examined.

4.2. Hot-Carrier Reliability Test Circuits

In order to study high-frequency AC hot-carrier degradation free from measurement-induced artifacts [4.3], [4.8], on-chip ring-oscillator test circuits with different stage numbers, output fanout factors, and logic elements were implemented. Fig. 4.1 shows a basic structure of the inverter ring oscillator. The number of stages is chosen to be a small odd prime number to increase the oscillation frequency and suppress high-order harmonics [4.10]. A two-to-one ratio between PMOSFET-to-NMOSFET width is adopted to compensate the mobility difference. Also shown in Fig. 4.1, both the NMOSFET and PMOSFET devices in one stage of each ring oscillator are configured to be accessible through pass transistors [4.5]. During AC stress, the pass transistors are switched off in order to isolate the circuit from pad capacitances and, as a result, avoid slowdown of circuit operations. During device measurements, the operation of circuits is halted and devices can be measured by turning on the pass transistors. These test circuits allow direct correlation between not only device and circuit degradation under realistic high-frequency and short-transient circuit operating conditions, but also the device degradation under AC and DC conditions.

The devices and circuits used in the study were fabricated using a 0.6μm triple-level metal, CMOS process with scaled-down gate dimensions. The NMOSFETs have oxide-spacer LDD structures; the PMOSFETs have conventional single-drain structures. The NMOSFETs have an effective channel length of 0.26μm; the PMOSFETs, 0.43μm. The oxide thickness is 10.5nm. The oscillation frequency of the CMOS inverter structures, ranges from 280MHz to 440MHz with rise/fall times between 100ps and 500ps. Note, that such a short transient condition is very difficult to achieve in typical device experiments. Details of the experimental conditions are listed in Table 4.1 for

references.

4.3. Degradation Characteristics under AC Circuit Stress

Fig. 4.2 shows a typical test-circuit inverter degradation characteristic. The shift of the DC transfer curve is due to simultaneous degradation of both NMOSFET and PMOSFET devices. The device I-V measurements show the corresponding NMOSFET and PMOSFET characteristics before and after AC circuit stress in Fig. 4.3. From changes in the I-V characteristics, the NMOSFET oxide damage, which is similar to damage generated by DC voltage stress, appears to be acceptor-type interface states [4.11]. For PMOSFETs, the saturation-current increase after stress indicates the usual electron trapping mechanism observed in DC stress conditions [4.12]. However, the decrease of linear current after stress points to a degradation mechanism which is different from the mechanism in the saturation region. It is believed that this additional mechanism is due to donor-type interface states as reported in other studies [4.6], [4.7].

Fig. 4.4 compares the time dependence of CMOS device and circuit degradation. The NMOSFET linear- and saturation-current degradation rates exhibit different time dependence. This behavior is only observed in LDD-type transistors due to non fully overlapped drain structures [4.13]. The damage (acceptor-type interface states) under the oxide spacer increases the drain series resistance and damage under the gate-controlled region reduces carrier mobility. While the linear current is affected by both mechanisms, the saturation current which, in the first order, is independent of the drain voltage is influenced mostly by mobility reduction only. As a result, the linear- and saturation-current degradation show different time dependence behaviors.

For PMOSFETs, because competing donor-type interface-state (positive charge) and oxide electron-trap (negative charge) generation mechanisms are both present, different time-dependence behaviors are observed for the linear- and saturation-current degradation characteristics as well. The degradation of linear current which is affected

by both mobility reduction due to interface states and channel-shorting effect due to electron trapping [4.14] shows a saturating characteristic with a maximum degradation value of 3 percent in our devices [4.15]. The degradation of saturation current is mostly affected by electron-trap-induced channel shortening effect because most of the interface states are empty and, as a result, have not effects.

Both NMOSFET and PMOSFET devices show the existence of multiple degradation mechanisms. The different mechanisms can be differentiated by properly observing the difference between the linear- and saturation-current degradation. Although only results from the inverter test structure with fanout of 1 are shown in this section, that the results from other test structures with different configurations show exactly the same characteristics indicates the generality of these device degradation behaviors.

The degradation of inverter stage-delay time as a result of device degradation is shown in Fig. 4.4. This circuit degradation due to only NMOSFET or PMOSFET device degradation can be distinguished by measurements of rise and fall time components. However, that is beyond the capabilities of test circuits used in this study. Another method to separate out the individual contribution will be discussed in Section 4.6.. The overall degradation of stage-delay time reflects the partial cancellation between the decrease of NMOSFET and increase of PMOSFET current-drive capabilities [4.2].

4.4. Enhanced Degradation due to Intrinsic MOSFET Voltage Overshoot

Voltage overshoot due to device-to-interconnect coupling has been shown to cause enhanced hot-carrier degradation [4.16]. However, Fig. 4.5 shows another, more intrinsic, coupling mechanism where charge feedforward from the MOSFET overlap capacitance C_{GD} to the output capacitance arises during rapid voltage transitions. This charge feedforward results in voltage overshoots that can dominate the amount of hot-carrier degradation (due to the exponential dependence of degradation on the applied voltage [4.17]).

The observed non-monotonic dependence of degradation on fanout/node-capacitance shown in Fig. 4.6 contradicts those model predictions based solely on transition-time (rise/fall time) calculations [4.2], [4.18]. This voltage overshoot due to charge feedforward can be modeled as [4.19]

$$\Delta V = \frac{C_{GD}}{C_{GD}+C_{OUT}} V_{CC} \tag{4.1}$$

where C_{OUT} is the output capacitance and V_{CC} is the power-supply voltage. For a smaller fan-out (output capacitance), although the transition time is shorter, voltage overshoot (4.1) becomes larger and contributes to the observed enhanced degradation as shown in Fig. 4.7. By properly accounting for both voltage-overshoot and transition-time effects, the observed tradeoff between fanout and degradation can be correctly explained (Fig. 4.7).

This result indicates the important contribution of device parasitic as well as interconnect capacitance. In order to accurately predict hot-carrier degradation in a circuit environment, accurate modeling of these components must be taken into account.

4.5. Validity of Quasi-Static Approximation (DC vs. AC Degradation)

Whether the quasi-static approximation is applicable is critically important for the circuit-level hot-carrier reliability evaluation. This study provides a direct experimental approach to test this assumption. Due to the structures of test circuits used in this study, it is possible to compare DC and AC NMOSFET degradation results directly as shown in Fig. 4.8. The AC device degradation is obtained from direct test-circuit measurements. The DC device degradation is obtained from a peak substrate current DC stress and a duty-cycle-corrected DC results obtained using the quasi-static approximation is also shown [4.2], [4.5], [4.18]. An obvious difference between the degradation time dependence of AC and DC (or duty-cycle-corrected DC) linear and saturation current is

observed. The different degradation rates which are specially evident in saturation-regime characteristics (about 0.5 for DC and 0.3 for AC device degradation) strongly suggest that the quasi-static approximation is inaccurate for circuit-level hot-carrier reliability evaluation.

As for further confirmations, individual device stress was performed using sinusoidal and triangular gate-voltage waveforms (rather than the usual pulse stress [4.3]) in order to accentuate the amount of transition-induced degradation (Fig. 4.9). A 0-to-2V gate waveform is chosen to simulate the gate voltage conditions under maximum drain voltage encountered in circuit test structures (Fig. 4.5). This condition also can avoid the observed enhanced degradation due to additional interface-state generation by alternate hot hole and electron injections [4.9]. The observed change in the degradation rate/slope with increasing frequency suggests the onset of different non-quasi-static degradation dynamics. As a result, quasi-static approximation is inaccurate at higher frequencies. Based on data shown in Fig. 4.8, the impact of this non-quasi-static degradation dynamic on lifetime extrapolation can be estimated as shown in Fig. 4.10. Because these two degradation curves cross each other in Fig. 4.8, the device lifetime depends on the particular lifetime criterion chosen. Without understanding of this high-frequency phenomenon, one can mistakenly overestimate or underestimate the device reliability based on quasi-static approximation. So it is very important to extract the correct AC degradation time dependence experimentally by using circuit test structures as shown in Fig. 4.1 and procedures described in Section 4.2..

Fig. 4.11 shows that the quasi-static approximation is inaccurate at high-frequencies for PMOSFETs as well. As shown in Fig. 4.12, the PMOSFET voltage waveforms in circuit operating conditions traverse both the peak gate- and substrate-current stress regions during AC stress. As a result, both electron traps (which occur during the peak gate-current region) and donor-type interface states (which occur during the peak substrate-current region) are generated. The combination of these two mechanisms results in the observed sign difference between the linear- and saturation-current degradation under AC stress. In addition, the changing PMOSFET bias conditions

result in electron detrapping during AC stress [4.12]. Therefore, the AC device degradation due to electron traps is much smaller than DC (and duty-cycle-corrected DC) degradation as shown in Fig. 4.11.

4.6. Impact of AC Device Degradation on Circuits

In order to separate out the contribution of NMOSFET and PMOSFET device degradation, DC stress is performed on devices embedded in one stage of circuit test structures. The degradation of circuit delay time as a result of the individual NMOSFET device degradation is measured as shown in Fig. 4.13. The correlation between linear- and saturation-current degradation is also plotted to facilitate the use of different degradation monitors. The result indicates that for the same device degradation, circuits with the highest output capacitance (such as I/O buffers and bus interface circuits) are the most susceptible to hot-carrier degradation.

By establishing the correlation between device and circuit degradation, the reliability criteria can be redefined based on AC circuit requirements. The result is plotted in Fig. 4.14. By switching from a DC device criterion (10% linear current degradation) to a AC device criterion (10% linear current degradation), significant lifetime improvement can be achieved. This is because devices degrade only during voltage transition in AC operation. If we go a step further by using a AC circuit criterion (such as 5 ps delay-time degradation per stage in inverter ring oscillators with fanout of 1 which corresponds to 20% linear current degradation or 5% saturation current degradation), additional lifetime improvement is obtained. This figure demonstrates that reliability can be improved greatly by using AC circuit-level evaluation without resorting to complex technologies.

For PMOSFETs, the AC device degradation with both donor-type interface states and electron traps can not be duplicated by simple DC stress experiments. As a result, the interaction between these two degradation mechanisms and their power-supply voltage

dependence needs to be understood first before their impact on circuit degradation can be evaluated.

4.7. Conclusions

In this chapter, I have used circuit test structures to study hot-carrier degradation under high-frequency circuit operation. It is found that device parasitics, which induce voltage overshoot under short voltage transients, produce enhanced degradation. As a result, analytic models based on purely transition-time calculations may underestimate the degradation. Correct modeling of device parasitic and interconnect capacitance is necessary.

The applicability of the quasi-static approximation is also in question at high frequencies. Circuit and device measurements indicated that NMOSFETs have different acceptor-type interface-state generation dynamics under short voltage transients. The different degradation rates have significant effects on lifetime extrapolation. For PMOSFETs, the AC operating waveform also induces additional donor-type interface states and electron detrapping which are different from DC stress results. Due to large electron detrapping, electron trap generation is unlikely a reliability concern for digital circuit operation.

Finally, the impact of NMOSFET device degradation on CMOS logic circuits is analyzed. The resulting correlation between device and circuit degradation is established. It is demonstrated that the current DC device reliability criterion is very conservative in digital circuits. By switching to AC reliability criteria based on circuit performance constraints, one can relax the device reliability requirements significantly.

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Table 4.1 Experimental conditions of inverter ring oscillators. Stress voltage is 5.8V for all structures.

Fanout	Stage	Frequency (MHz)	delay time (ps)
1	23	385	56
2	13	440	87
4	13	278	138

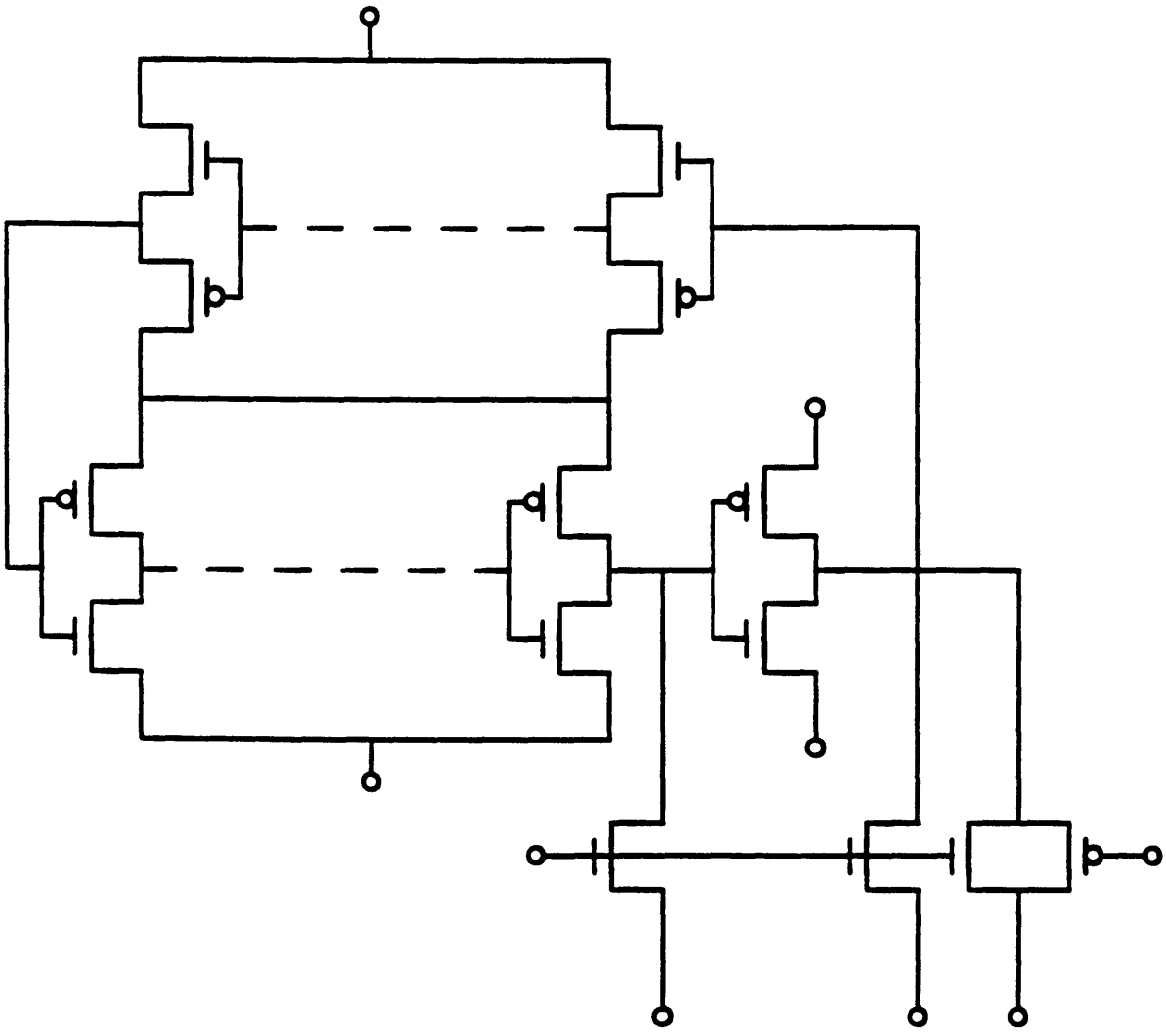

Fig. 4.1 Simplified circuit schematic used in high-frequency AC stress.

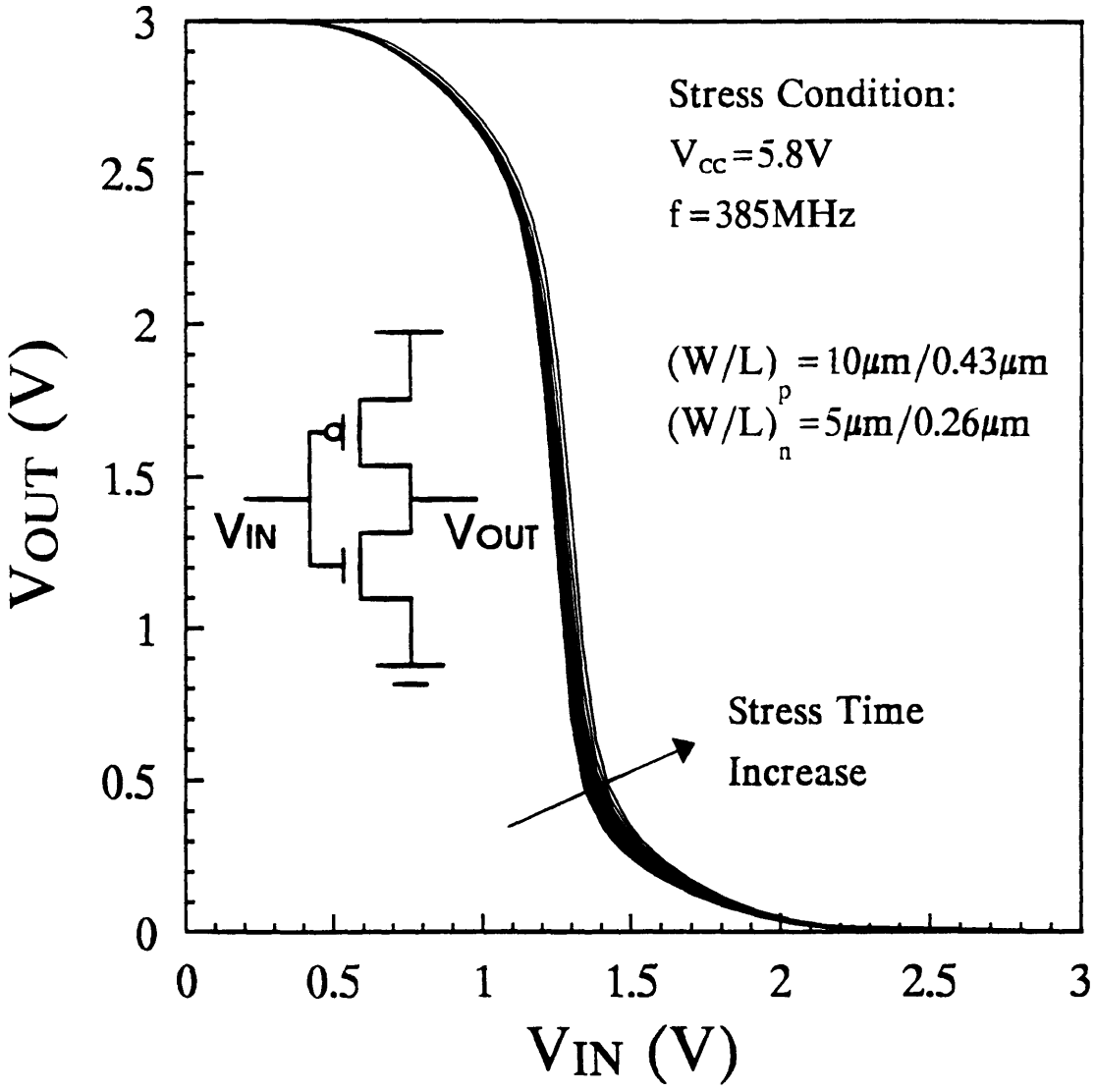

Fig. 4.2 DC transfer curves of a CMOS static inverter after AC stress in a CMOS ring oscillator with fanout of 1.

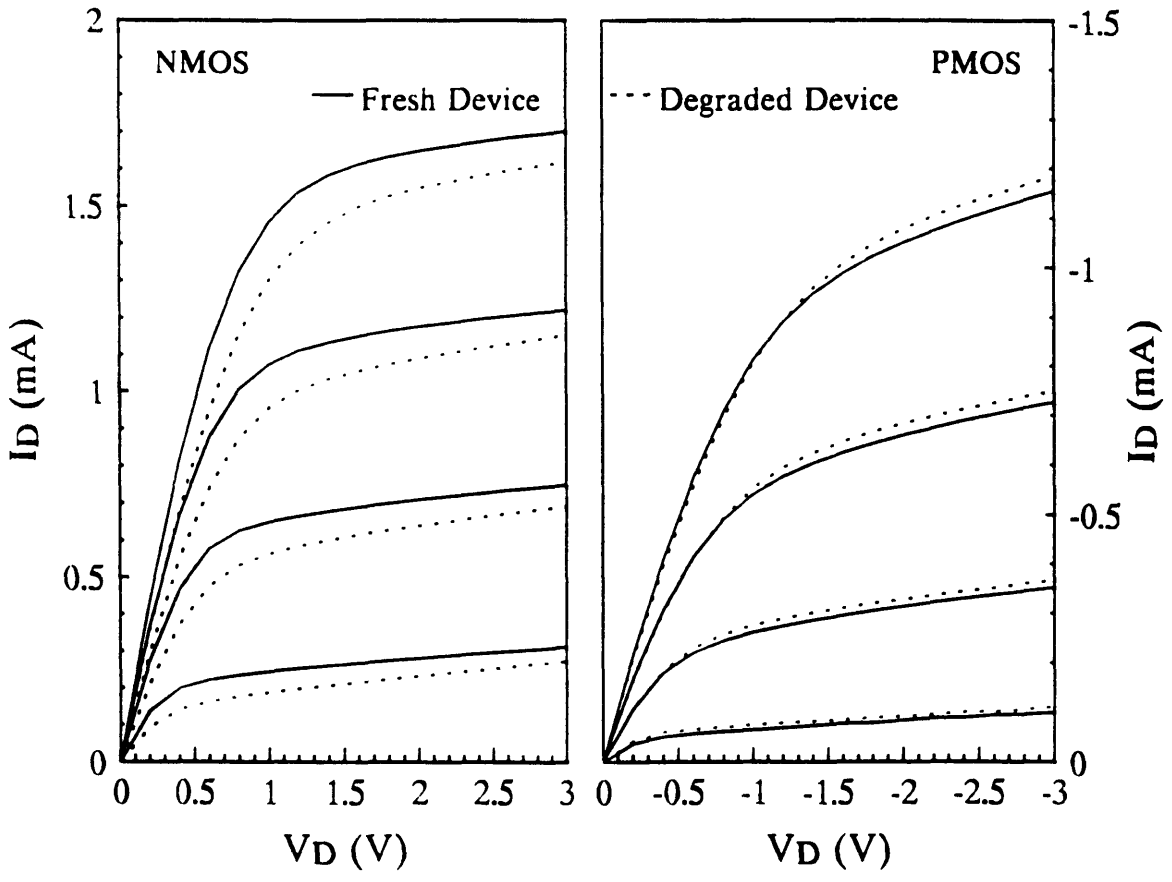

Fig. 4.3 AC device degradation after 500 hours in a CMOS inverter ring oscillator with fanout of 1.

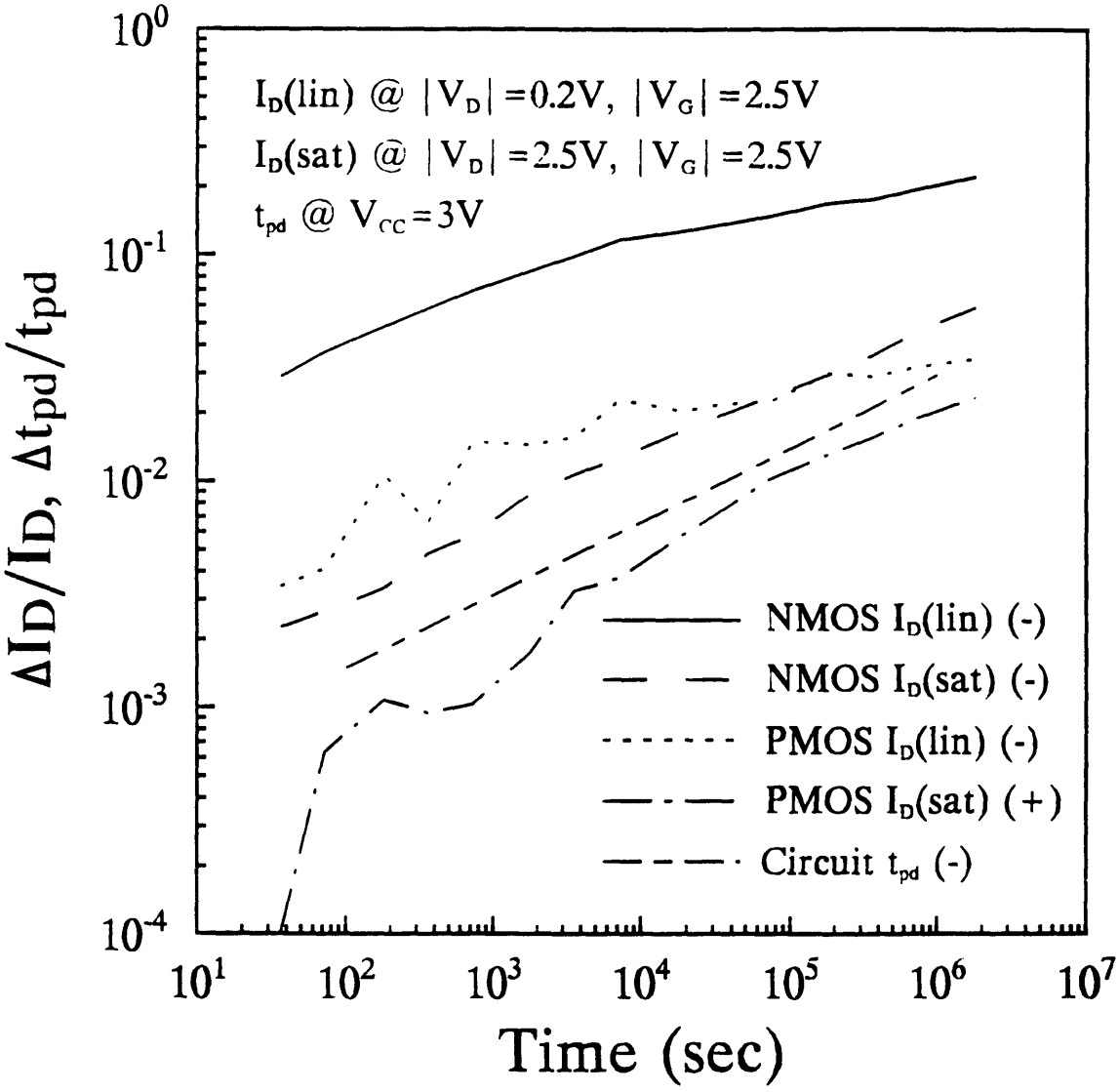

Fig. 4.4 Time dependence of various device/circuit degradation monitors for a CMOS inverter ring oscillator with fanout of 1.

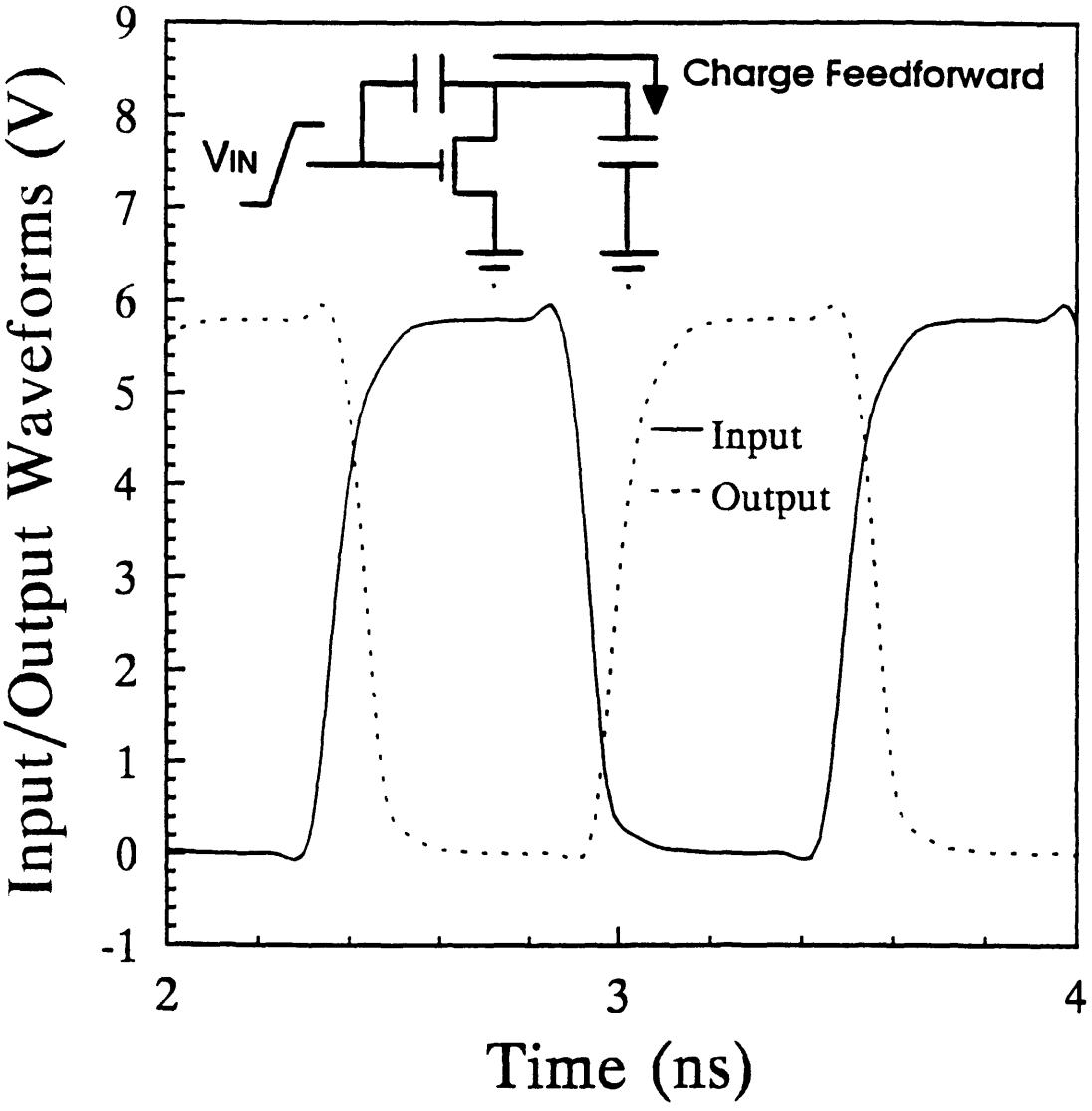

Fig. 4.5 Simulated inverter voltage waveforms in the ring oscillator with fanout of 1.

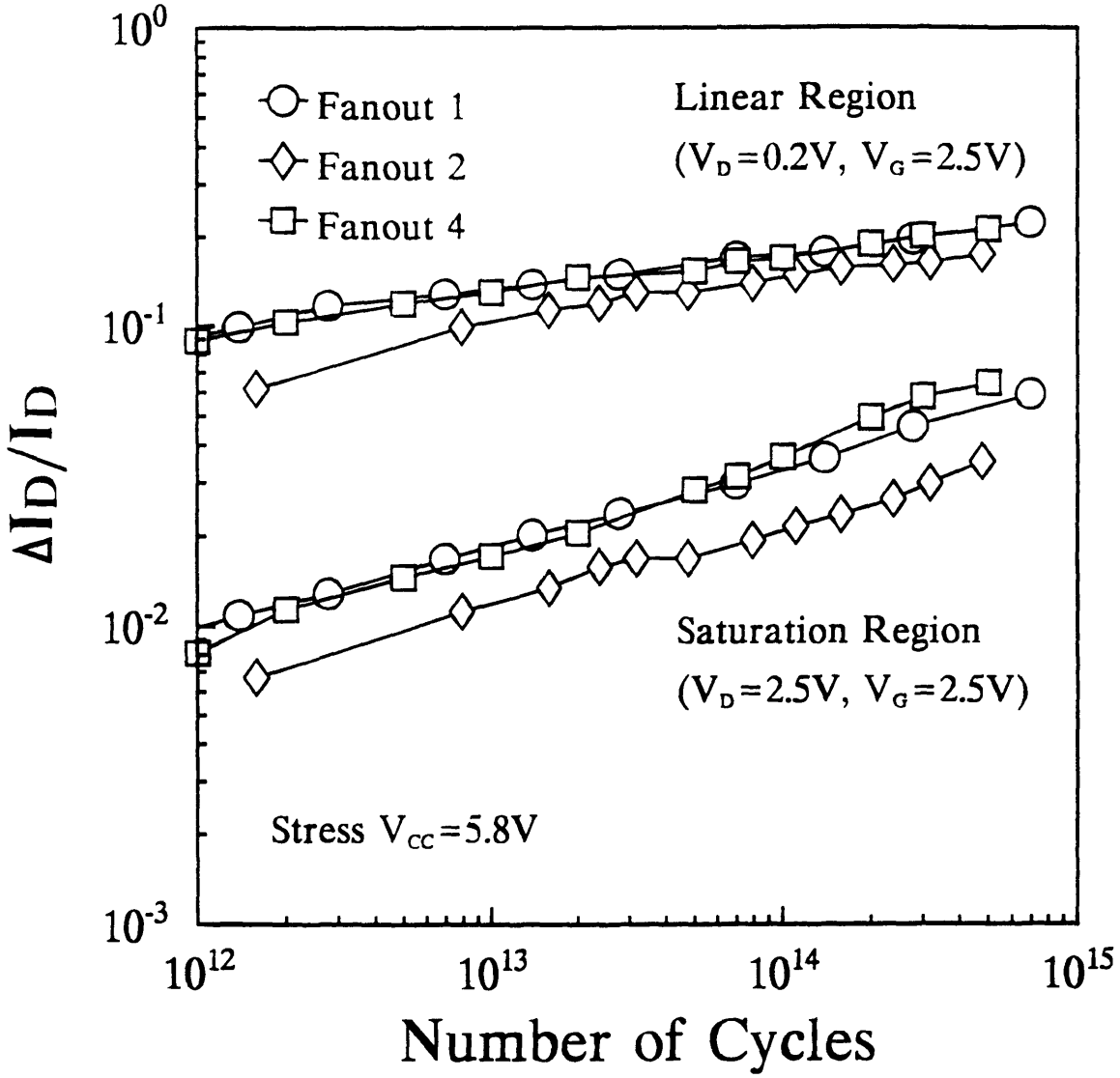

Fig. 4.6 Linear- and saturation-current degradation of NMOSFETs in ring-oscillator circuits with different fanouts.

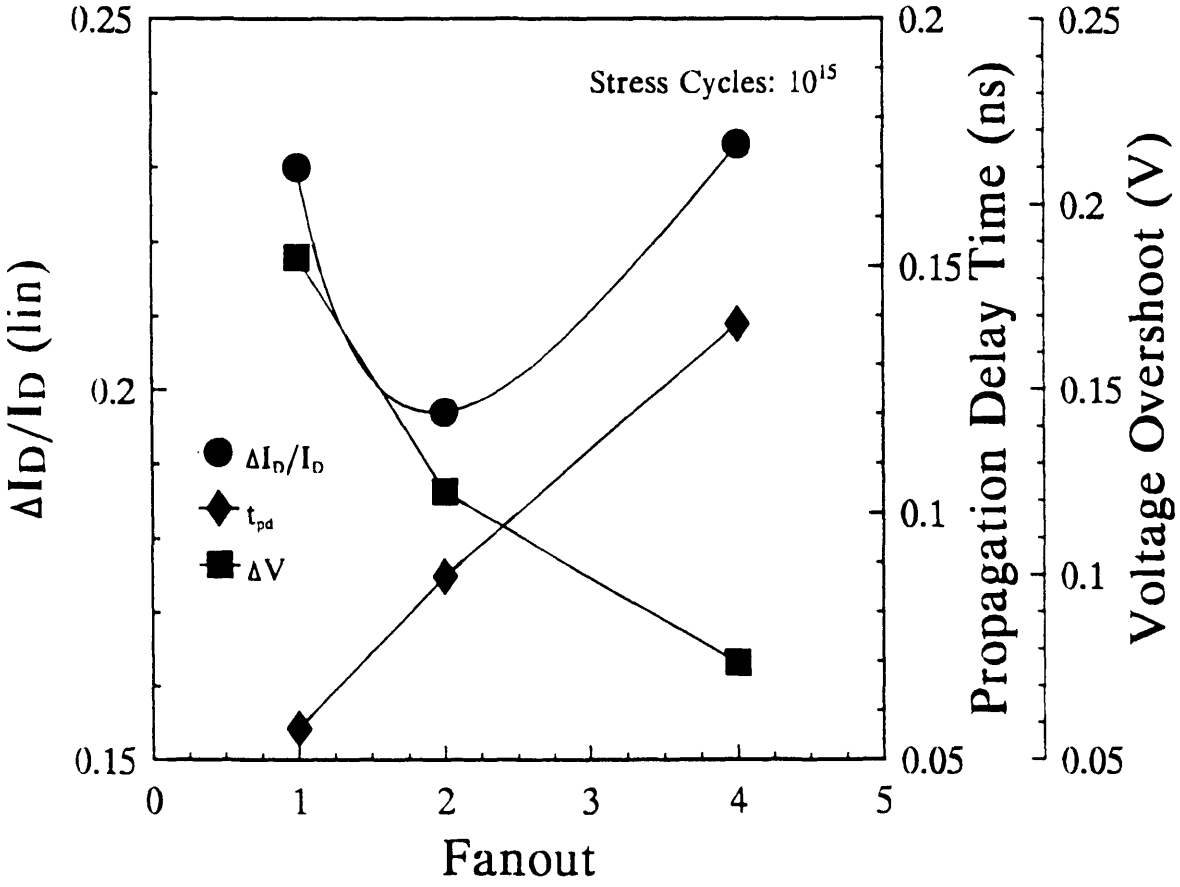

Fig. 4.7 Impact of voltage overshoot and propagation delay time on device degradation.

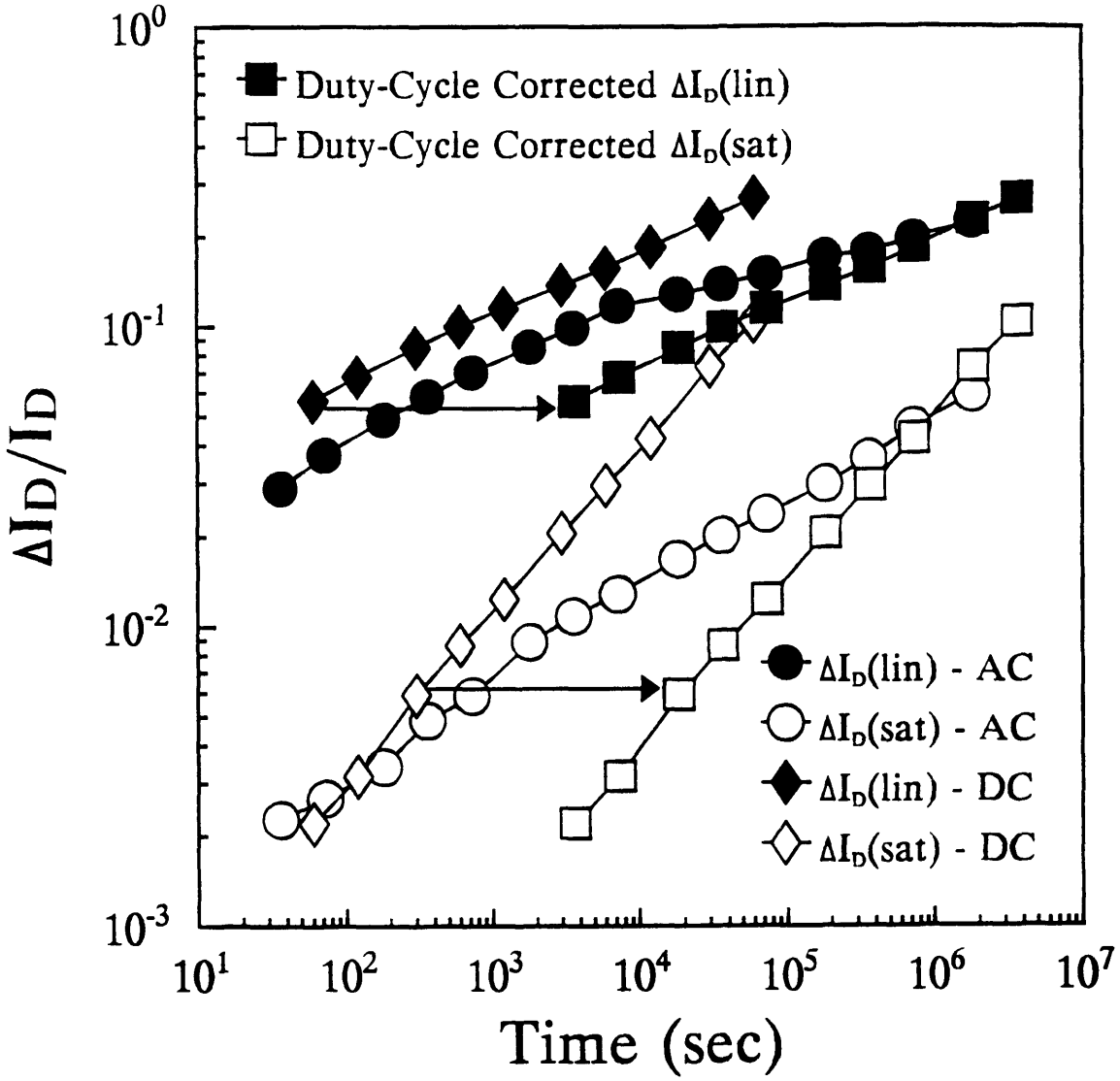

Fig. 4.8 Comparison of DC and AC NMOSFET current degradation. DC stress condition: V_D=5.8V, V_G=1.9V; AC: V_{CC}=5.8V, f=385MHz.

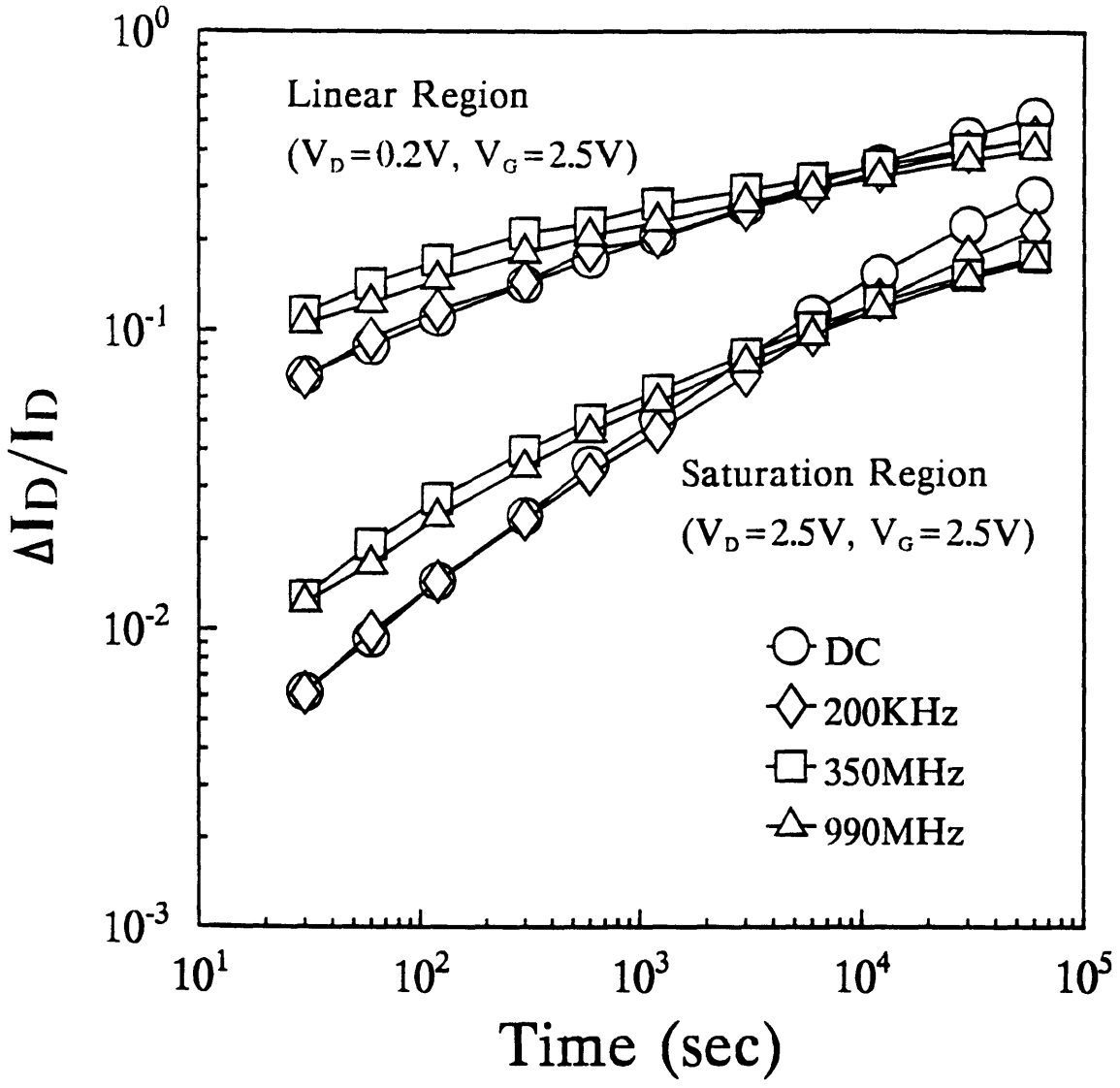

Fig. 4.9 The NMOSFET current degradation for different stress frequencies under a 0-to-2V sine gate voltage waveform. The stress V_D is a constant 5.8V. V_G is 1.9V for DC stress.

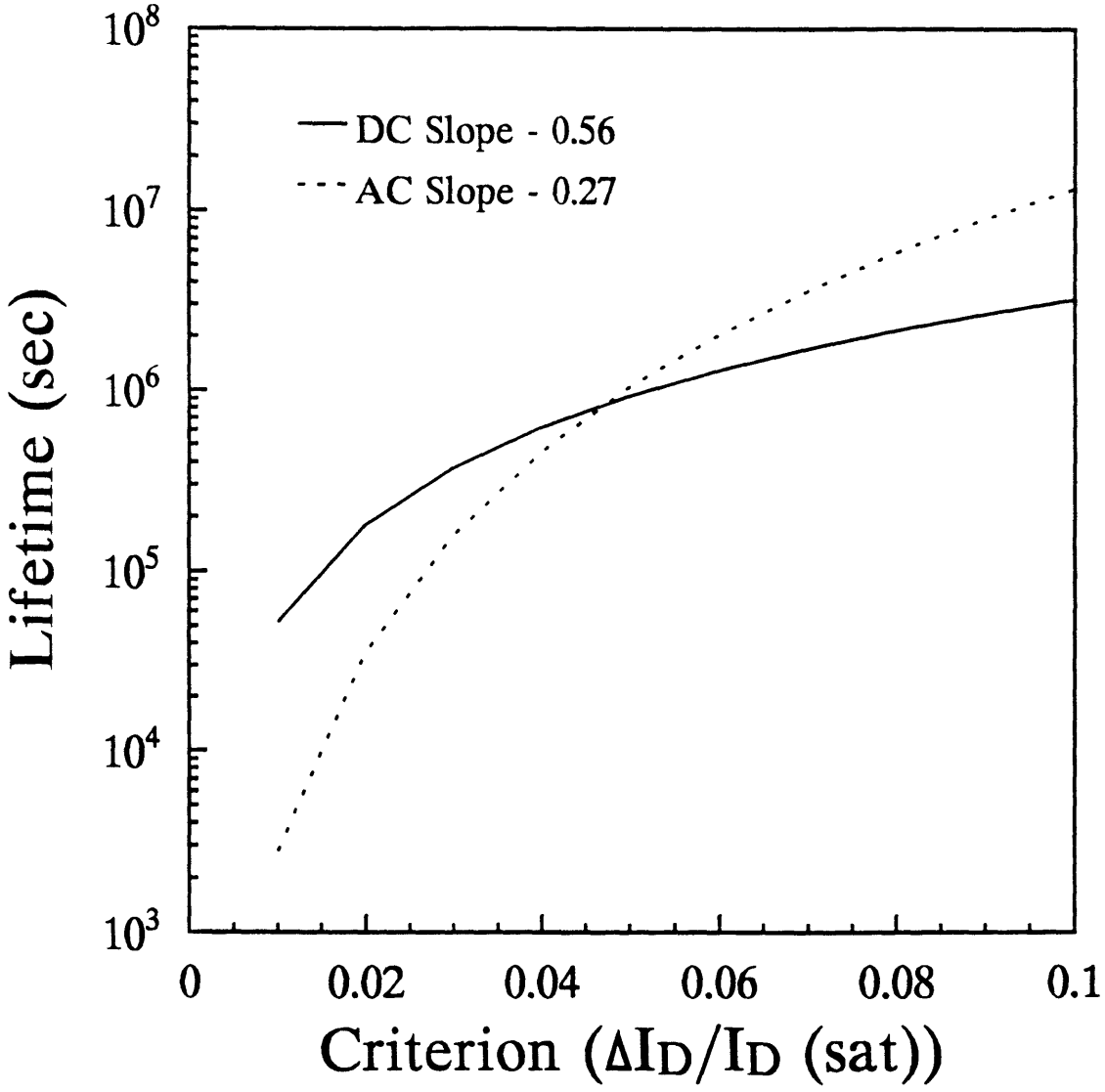

Fig. 4.10 Lifetime extrapolation based on quasi-static approximation (DC) and actual experimental data (AC, non-quasi static degradation) with different reliability criteria.

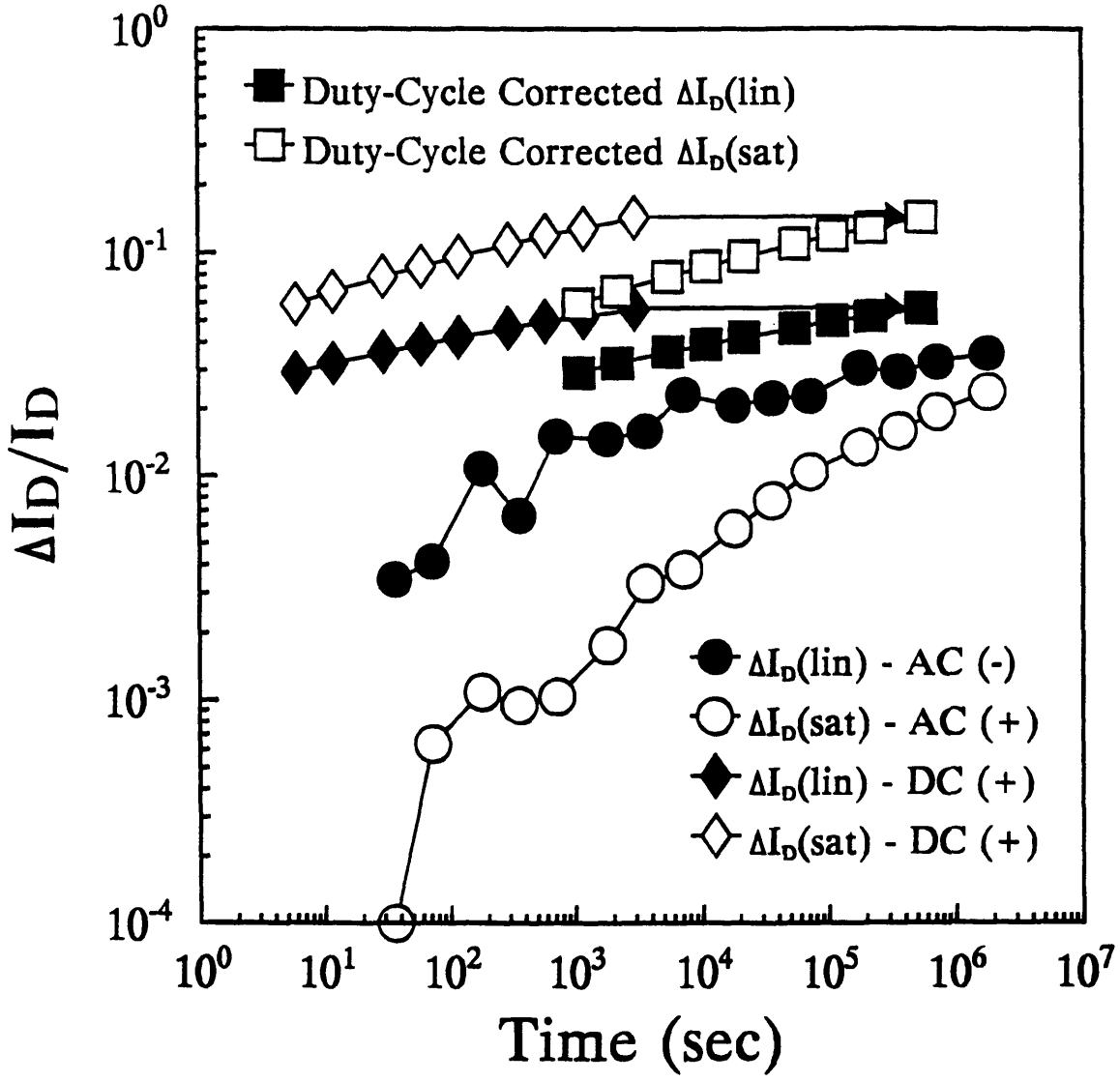

Fig. 4.11 Comparison of DC and AC PMOSFET current degradation. DC stress condition: V_D=-5.8V, V_G=-1.2V; AC: V_{CC}=5.8V, f=385MHz.

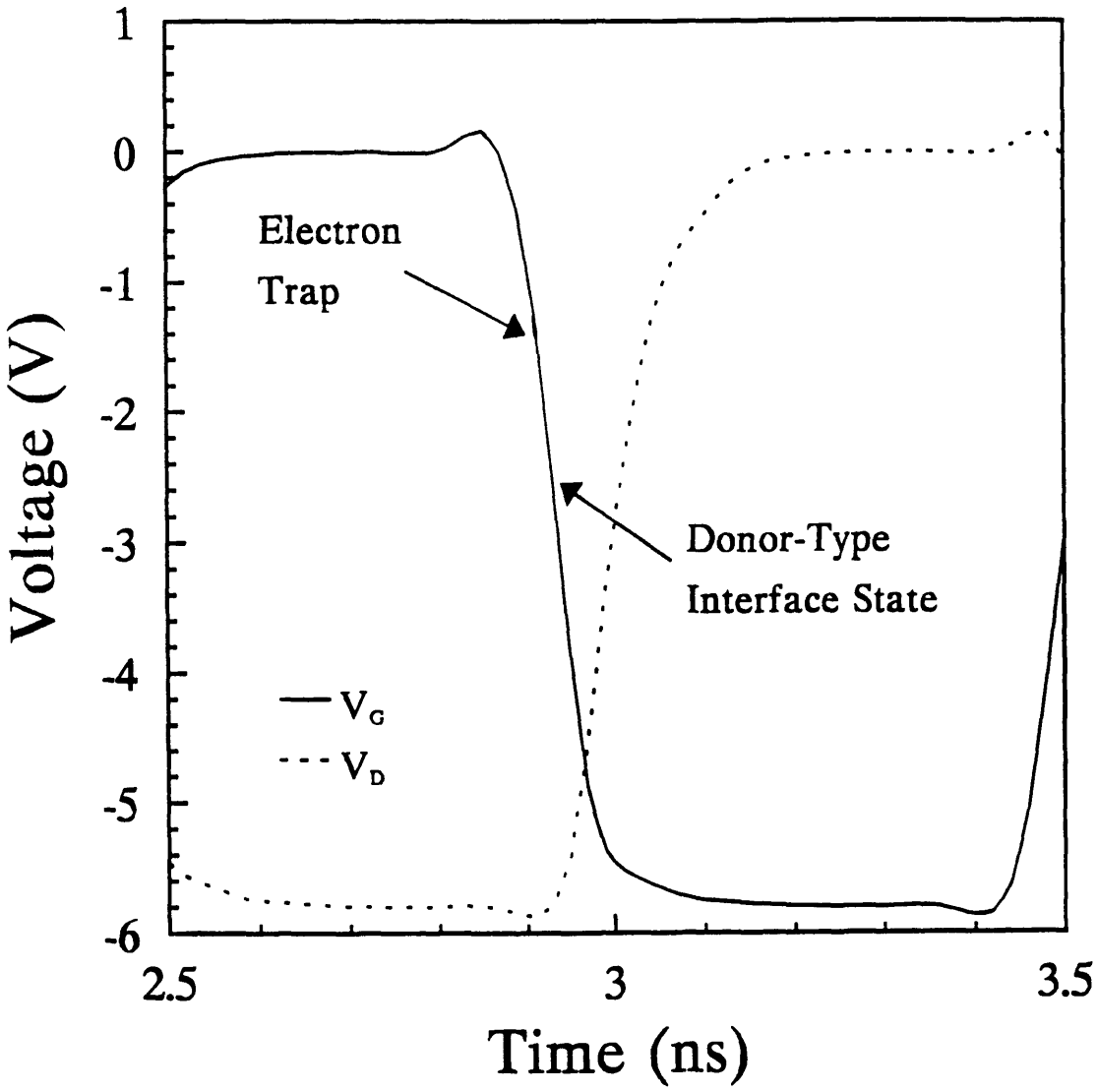

Fig. 4.12 PMOSFET operating waveforms and degradation mechanisms.

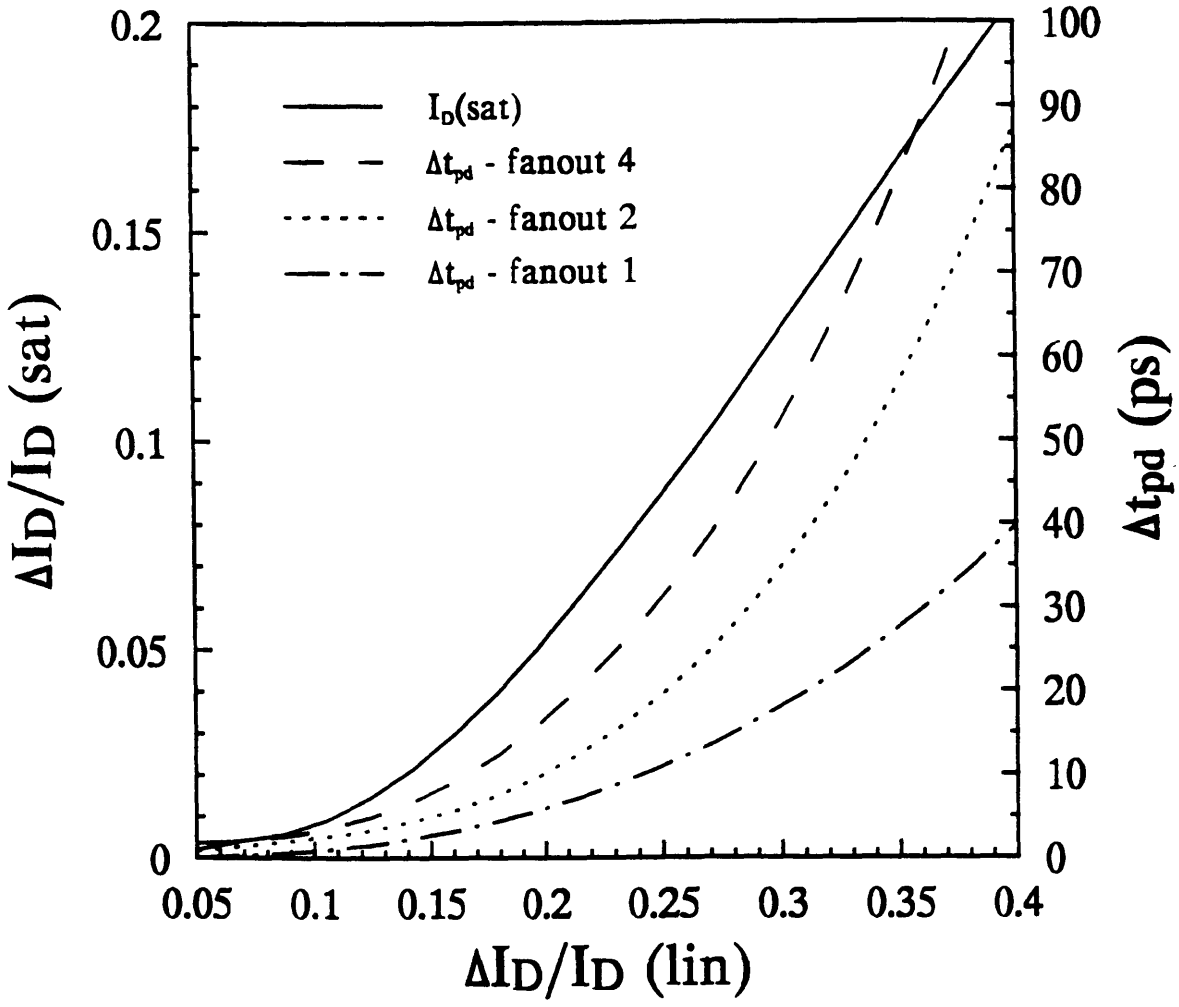

Fig. 4.13 Degradation correlation between NMOSFET current and inverter stage delay for different fanouts.

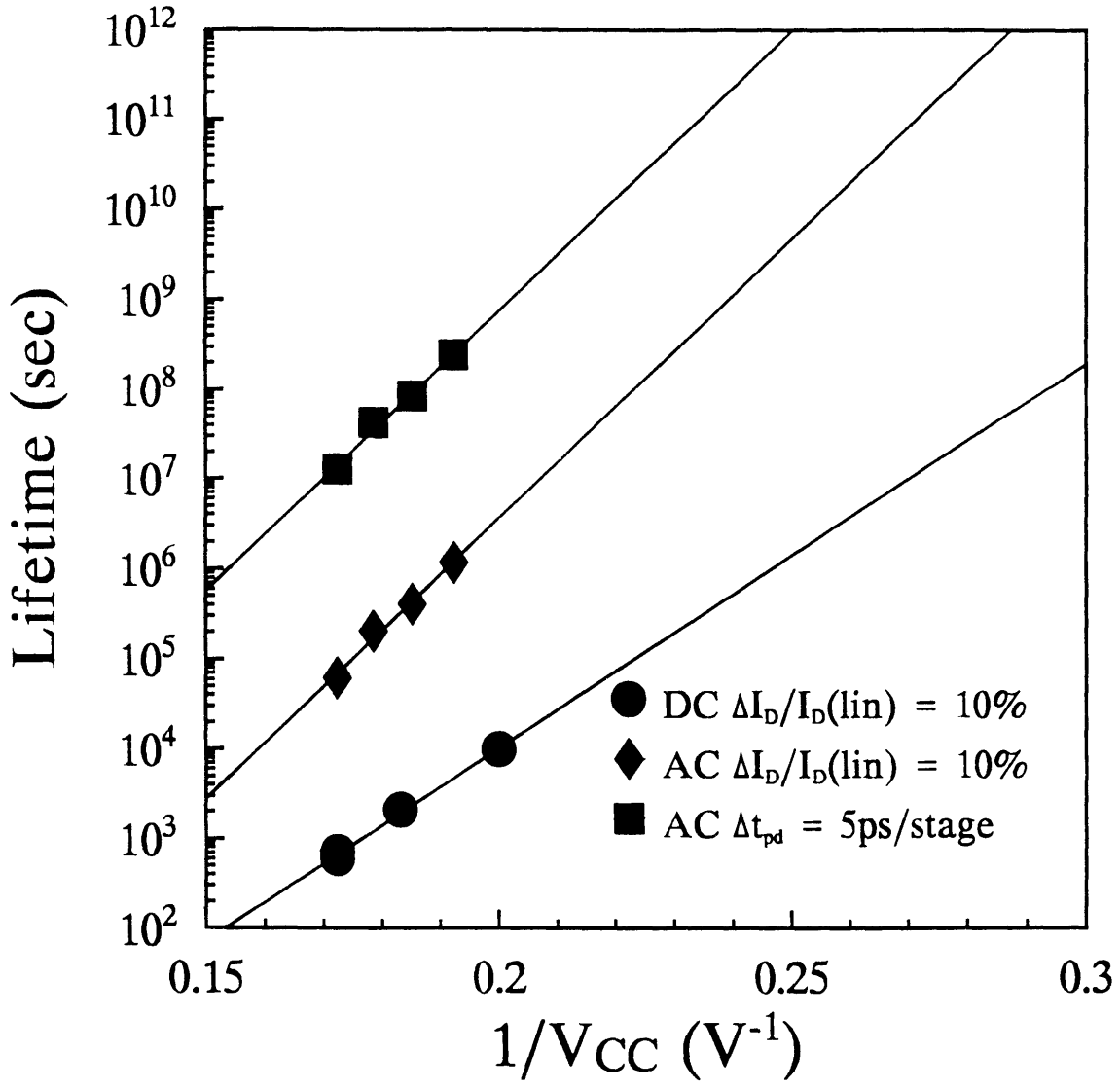

Fig. 4.14 Device lifetime estimation by using DC device-based, AC device-based, and AC circuit-based reliability criteria. The circuit criteria are applied to a inverter ring oscillator with fanout of 1 operating in 100MHz.

Chapter 5

Analog Circuit Degradation

5.1. Introduction

Hot-carrier degradation has long been identified as a VLSI reliability concern. Its fundamental device-level degradation mechanisms have been extensively characterized and modeled [5.1]-[5.3]. However, in recent years, it has become recognized that circuit performance degradation due to hot carriers is very sensitive to the particular circuit topology and operating conditions [5.4], [5.5]. Thus, the real criteria for hot-carrier reliability should be based on circuit and system performance requirements. There have been a few efforts to study how hot-carrier-induced damage affects circuit performance. They have examined the impact of hot-carrier degradation on SRAM [5.6], DRAM [5.7], and CMOS logic circuit [5.8] performance. Because analog circuits used to use long-channel devices due to device-matching constraints, the influence of hot-carrier effects on analog circuit performance has been believed to be minimal and, as a result, has been mostly overlooked. However, because power supply scaling for analog circuits will not likely be as aggressive as for digital circuits, because submicrometer devices are necessary for high speed applications (such as for video applications [5.9]), and because the operation of analog circuits is sensitive to device parameter variations [5.10], [5.11], the impact of hot-carrier degradation on the performance of CMOS analog circuits needs to be clearly understood [5.12].

This chapter presents some of the first experimental data on actual CMOS analog

subcircuit performance degradation due to hot-carrier effects. It is found that, compared to the performance degradation of digital circuits which is dominated by interface-state generation in NMOSFETs [5.4]-[5.8], the performance degradation of analog circuits is found to be more sensitive to hole trapping in NMOSFETs. The exact amount of performance degradation depends heavily on the particular circuit design and operating conditions. Tradeoffs between circuit performance and reliability are also illustrated.

The devices and circuits used in this study were fabricated using a 1.5μm LOCOS-isolated, double-level metal, BiCMOS process with conventional drain/source junctions. The MOSFET dimensions are T_{ox}=35nm, L_{EFF}=1.5μm-12μm. All the measurements were performed at room temperature and at the wafer level.

5.2. Degradation of Analog NMOSFET Device Parameters

There are two principal ways in which hot-carrier degradation can affect analog device characteristics. It can affect device matching characteristics and it can degrade device performance [5.10].

5.2.1. Analog Device Matching Degradation

The design of most analog subcircuits, such as differential amplifiers and current mirrors, critically depends on device matching properties. Basic concepts about the impact of device mismatching can be illustrated by examining the following simple analytical models. For NMOSFETs, the device mismatch of drain current for the same applied voltage can be modeled as [5.13]

$$\frac{\Delta I_D}{I_D} = \frac{\Delta \beta_n}{\beta_n} - \left(\frac{g_m}{I_D}\right) \cdot \Delta V_T \qquad (5.1)$$

or the mismatch of gate voltage for the same drain current can be modeled as

$$\Delta V_G = \Delta V_T - \left(\frac{I_D}{g_m}\right) \cdot \frac{\Delta \beta_n}{\beta_n} \qquad (5.2)$$

where $\beta_n = \mu_n C_{ox} W_{EFF}/L_{EFF}$ is the device transconductance and V_T is the threshold voltage. Note, that the current and voltage mismatch differ only by the proportional $(-I_D/g_m)$ factor. Both threshold voltage and device transconductance have been shown by previous studies [5.1]-[5.3] to change after hot-carrier stress. Thus, it is reasonable to expect that analog device matching properties will also be affected by the hot-carrier-induced damage.

Typical characteristics of NMOSFET current mismatch ($\Delta I_D/I_D$) after hot-carrier stress are shown in Fig. 5.1 for different stress gate voltages. The linear-current mismatch (indicated by the diamond symbols) can be divided into three distinct regions, each of which corresponds to a different degradation mechanism. For a low-gate-voltage stress condition ($V_G \sim V_T$), the observed increase of drain current is believed to be due to hole trapping [5.3]. For a high-gate-voltage stress condition ($V_G \sim V_D$), electron trapping, which causes the observed decrease of drain current, is believed to be dominant [5.2]. For a mid-gate-voltage stress condition ($V_G \sim V_D/2$), the observed reduction of drain current is due to the generation of acceptor-type interface states [5.1]. The corresponding linear-region NMOSFET voltage mismatch (ΔV_G) characteristics are shown in Fig. 5.2. Note, that they exhibit similar characteristics as those of the current mismatch because only a simple $(-I_D/g_m)$ proportionality-factor difference exists between the two quantities (see (5.1) and (5.2)). Hence, the voltage mismatch also shows the same three distinct degradation regions.

When the device is biased in the saturation region, as in most analog circuits, acceptor-type interface states are mostly unoccupied (and hence neutral) because of the lowered electron quasi-fermi level near the drain. As a result, oxide traps (both hole and electron traps) will have a larger relative effect on device characteristics. Fig. 5.1 shows that the current mismatch in the saturation region (indicated by the circular symbols) gradually changes from a positive value, due to hole traps, to a negative value, due to electron traps, as the stress gate voltage increases. A similar phenomenon is also

observed for the saturation-region voltage mismatch shown in Fig. 5.2. Note, for a mid-gate-stress-voltage condition, the peak in the mismatch (for both $\Delta I_D/I_D$ and ΔV_G) observed in the linear region disappears in the saturation region, as a result of unoccupied acceptor-type interface states. Thus, because most NMOSFETs used for analog applications are biased in the saturation region with a low gate-to-source voltage, hole trapping is expected to have a larger impact than acceptor-type interface state generation on long-term device reliability.

Fig. 5.3 and Fig. 5.4 show how the impact on device performance of a given amount of NMOSFET hot-carrier-induced damage depends on the particular device biasing conditions in a circuit. The device in these two figures was stressed under a certain low V_{GS} and high V_{DS} condition (V_{GS}=1.3V, V_{DS}=9.3V). This stress condition corresponds to a dominant hole-trapping degradation mechanism, although some interface states are also generated (see Figs. 5.1 and 5.2). When measured in the saturation region, $\Delta I_D/I_D$ is positive due primarily to the "channel shortening" effect induced by the positive hole traps in the oxide near the drain [5.14]. When measured in the linear region, the acceptor-type interface states are now occupied, increasing the number of scattering sites. $\Delta I_D/I_D$ now changes sign to the negative due to the reduction in inversion-layer mobility [5.15].

Note, in (5.1) and (5.2), the I_D/g_m term can be shown to be proportional to $(V_{GS}-V_T)/2$ or $(I_D/2\beta_n)^{1/2}$ in the saturation (quadratic) region. Thus, near the subthreshold region, where I_D/g_m is small, the current mismatch is expected to be the most severe for current-mirror applications and the gate-voltage mismatch can be minimized for differential-amplifier applications. Both of these trends can be observed in Figs. 5.3 and 5.4. These characteristics of hot-carrier-induced device mismatch are quite similar to the characteristics of intrinsic mismatch which arise due to process non-uniformity. The main difference is that the hot-carrier-induced $\Delta\beta_n$ and ΔV_T are strongly bias-dependent and will change over time.

5.2.2. Analog Device Performance Degradation

Hot-carrier degradation also affects analog device performance parameters such as the transconductance (g_m) and output resistance (r_o). These parameters, in turn, can affect circuit performance parameters such as open-circuit voltage gain and output signal swing over which a large open-circuit voltage gain is available [5.16]. Fig. 5.5 illustrates how g_m and r_o degrade for different operational bias conditions. From Fig. 5.5, it is clear that most of the observed voltage gain degradation ($A_V=g_m \cdot r_o$) is due to a reduction of output resistance rather than a reduction of transconductance. Note, that hot-carrier degradation can significantly alter r_o even with very little visible change in the I-V characteristics [5.10]. Whereas, for digital applications, current degradation is the most useful hot-carrier degradation parameter, for analog applications, monitoring current degradation alone is not necessarily sufficient to evaluate hot-carrier reliability.

5.3. Differential Amplifier Degradation

From the device DC degradation data, it is evident that the operating conditions of analog circuits, not only affect the level of hot-carrier stress (and hence, the amount of generated damage), but also influence how the hot-carrier-induced damage impacts the device parameters. Therefore, in order to obtain meaningful results about the impact of hot-carrier-induced damage on circuit performance, it is necessary to base the study on actual circuit operation under realistic conditions.

This section focussed on the analysis of the single-ended differential amplifier, a basic analog subcircuit. Fig. 5.6 displays the basic schematic. On-chip MOS switches (not shown) were utilized in order to characterize each individual device without affecting the circuit loading conditions during normal operation. In order to optimize the gain and speed tradeoff [5.13], [5.17], the input NMOSFETs are biased at a $I_D/g_m \sim (V_{GS}-V_T)/2$ condition in the 100-500mV range. This corresponds to a V_{GS} operating voltage of 0.7V-1.5V. A 1MHz square wave with a 33ns rise/fall time and an amplitude of 1V is used

as the input stress waveform. This waveform creates large voltage swing at the output node as commonly observed in latch circuits. The SPICE-simulated input and output waveforms are shown in Fig. 5.6. When V_{IN2} is reduced, the impedance of M_{N2} increases. Thus, less current flows through M_{N2} than through M_{N1}. As a result, V_{OUT2} increases, approaching V_{CC}. For transistor M_{N2}, this high drain voltage, combined with a non-zero drain current, produces a condition of maximum hot-carrier stress. Significant degradation occurs only during voltage transitions because, during the period of maximum drain voltage (when V_{IN2}=-1V), no drain current flows through transistor M_{N2} and no hot carriers are generated. In order to insure observable circuit degradation within a reasonable time limit, an 11V power supply voltage was chosen to accelerate the hot-carrier degradation. This power supply voltage produces a maximum V_{DS} of 9V across the input NMOSFET device (M_{N2}).

5.3.1. Degradation Characteristics

Under stress, the experimentally measured DC transfer curve of the differential amplifier changes with time as shown in Fig. 5.7. The shift of the transfer curves creates an offset voltage and the slope change of the transfer curves changes the amplifier voltage gain. The offset voltage is defined as the input voltage difference between V_{IN1} and V_{IN2} required to achieve the same output voltage (V_{OUT1}=V_{OUT2}). The voltage gain is measured as the slope of the V_{OUT2} curves at the bias point of V_{OUT1} equal V_{OUT2}. The time dependence of the offset voltage shift (ΔV_{OFFSET}) and gain degradation ($\Delta A_V/A_V$) is plotted in Fig. 5.8.

After each hot-carrier stress interval, every device in the test circuit was individually measured in order to identify which particular devices were responsible for the observed circuit degradation. As is suggested from SPICE simulation (Fig. 5.6), it is found that almost all of the hot-carrier-induced degradation occurred in transistor M_{N2}. After stress, the gate-to-source voltage of transistor M_{N2} required to sustain the same drain current is observed to decrease. This is believed to be due to hole trapping because of

the low gate-to-source voltage seen during stress. The gate-voltage mismatch of transistor M_{N2} under circuit operating conditions (ΔV_G(AC)) versus time is plotted in Fig. 5.8. Its mismatch closely follows the differential amplifier's offset voltage. This confirms that most of the V_{OFFSET} circuit degradation indeed is due to the ΔV_G mismatch in transistor M_{N2}.

The change of voltage gain due to device performance degradation can be understood by examining the analytic formulas for voltage gain [5.17]

$$A_V = g_{m(M_{N2})} \cdot (r_{o(M_{N2})} // r_{o(M_{P2})}) \tag{5.3}$$

The change of transconductance in transistor M_{N2} is very small (see Section 5.2.2.). As a result, most of the gain degradation in this differential amplifier is due to the degradation of r_o in transistor M_{N2}. The correlation is shown in Fig. 5.9. Because r_o in PMOSFET M_{P2} does not degrade in this case, (5.3) indicates that the degradation of overall voltage gain is effectively reduced as compared to r_o degradation of transistor M_{N2}.

DC stressing of an NMOSFET device was also performed to compare the degradation in both DC and AC environments. The DC stress voltages were chosen to match the maximum stress voltage experienced by the M_{N2} device in the differential amplifier circuit as determined from the circuit measurements. The DC result (ΔV_G(DC)) is plotted in Fig. 5.8 and exhibits good correlation with the AC stress data (especially when properly correcting for duty-cycle differences [5.4]).

5.3.2. Circuit Design Tradeoff

The offset voltage and voltage-gain degradation of the differential amplifier versus a wide range of operational bias currents are shown in Fig. 5.10. Note, that the same bias current is used for both stress and measurement phases. As the bias current is increased, the amount of hot-carrier-induced damage (and hence, the degradation of both circuit

parameters) also increases because of the following two reasons: (1) with increasing I_{BIAS}, the V_{GS} across transistor M_{N2} increases, which leads to greater hole current injection into the gate oxide under normal differential amplifier operating conditions; (2) with increasing I_{BIAS}, M_{N2} conducts more drain current and noticeable stress starts to occur, not only during voltage transitions, but also during the entire period of high drain voltage [5.10]. As a result of these two mechanisms, the performance degradation increases with increasing bias current.

In order to study the effects of a different input waveform, a 1MHz sinusoidal input signal with an amplitude of 0.1V was applied to the differential amplifier circuit. This small input signal is commonly observed in amplifier circuits. With such a small input signal, the gate voltage of the input NMOSFET (M_{N2} in Fig. 5.6) is now held almost constant. Thus, the resulting stress conditions are very similar to the case of DC stress. The NMOSFET hot-carrier degradation now mostly depends on the DC bias level of the drain voltage which is controlled by the load PMOSFET transistor width. For the test structures (with fixed PMOSFET width) used in this study, a small bias current which causes a smaller V_{DS} drop across the PMOSFET load can produce a larger DC drain voltage on NMOSFETs and thus larger degradation. Thus, for this particular small-signal waveform, the hot-carrier degradation generally becomes worse, as the bias current becomes smaller as shown in Fig. 5.11. This trend is opposite to that observed in Fig. 5.10.

5.4. Current Mirror Degradation

For current mirror operations, the optimization of W/L requires a compromise between a small saturation voltage ($V_{DSAT} \sim V_{GS}-V_T$) for large signal swing and a large V_{GS} for a small current mismatch (see (5.1)) [5.13]. For typical W/L ratios, the V_{GS} will have a bias voltage between 1 to 2V. Thus, it is expected that hole trapping will again be the dominant degradation mechanism. The gate voltage of devices in current mirrors is held constant throughout operation. This is similar to differential amplifier operation under a

small signal input. Therefore, degradation will be mostly dependent on the drain voltage of the output device. In order to study the worst-case degradation, a constant DC voltage stress was applied to the output node of a current mirror.

The measured current mismatch, as a function of stress time, is shown in Fig. 5.12 and approximately follows an empirical $A \cdot t^n$ relation [5.18]. The current-mirror degradation as a function of the design parameter I_{BIAS}/W is shown in Fig. 5.13. The observed bell-shaped dependence is due to interaction between the supply of hot carriers and the influence of the vertical electric field. As the bias current during stress increases, at first, the damage increases as more hot holes are generated. However, as the bias current during stress increases further, the gate-to-drain vertical electric field becomes less favorable for hot hole injection into the gate oxide, and thus, the amount of degradation decreases.

If this current mirror is used as a load device for a PMOSFET-input differential amplifier, it will typically be biased into the deep saturation region in order to reduce its noise and offset contribution [5.17]. Mismatch in current mirrors will generate a differential amplifier offset voltage (ΔI_D(NMOSFET)/g_m(PMOSFET)) which has a functional form of $\Delta I_D/I_D^{1/2}$. This resulting offset voltage as a function of bias current is shown in Fig. 5.13.

5.5. Conclusions

This chapter has provided some of the first experimental evidence of NMOSFET hot-carrier degradation in CMOS analog circuits. Both DC device and AC circuit experimental data show that the dominant mechanism for NMOSFET degradation in analog subcircuits is hole trapping rather than interface state generation. Unless the hole-trapping mechanism is incorporated, present device degradation models and circuit reliability simulation programs will be unable to predict accurately analog device and circuit degradation. Thus, it is necessary to reexamine present hot-carrier degradation

models in order to predict the correct device lifetime and to evaluate circuit reliability for analog applications [5.19].

This chapter also has demonstrated that hot-carrier-induced circuit performance degradation is very sensitive to the particular circuit operating conditions and circuit design. The design curves shown in Figs. 5.10, 5.11, and 5.13 which illustrate the different trade-offs between analog subcircuit performance and hot-carrier reliability, can be used to provide insight into design-for- reliability. By taking hot-carrier degradation into account in the circuit design phase [5.4], [5.5], acceptable hot-carrier reliability may be achieved without resorting to complex and costly device structures and/or technologies.

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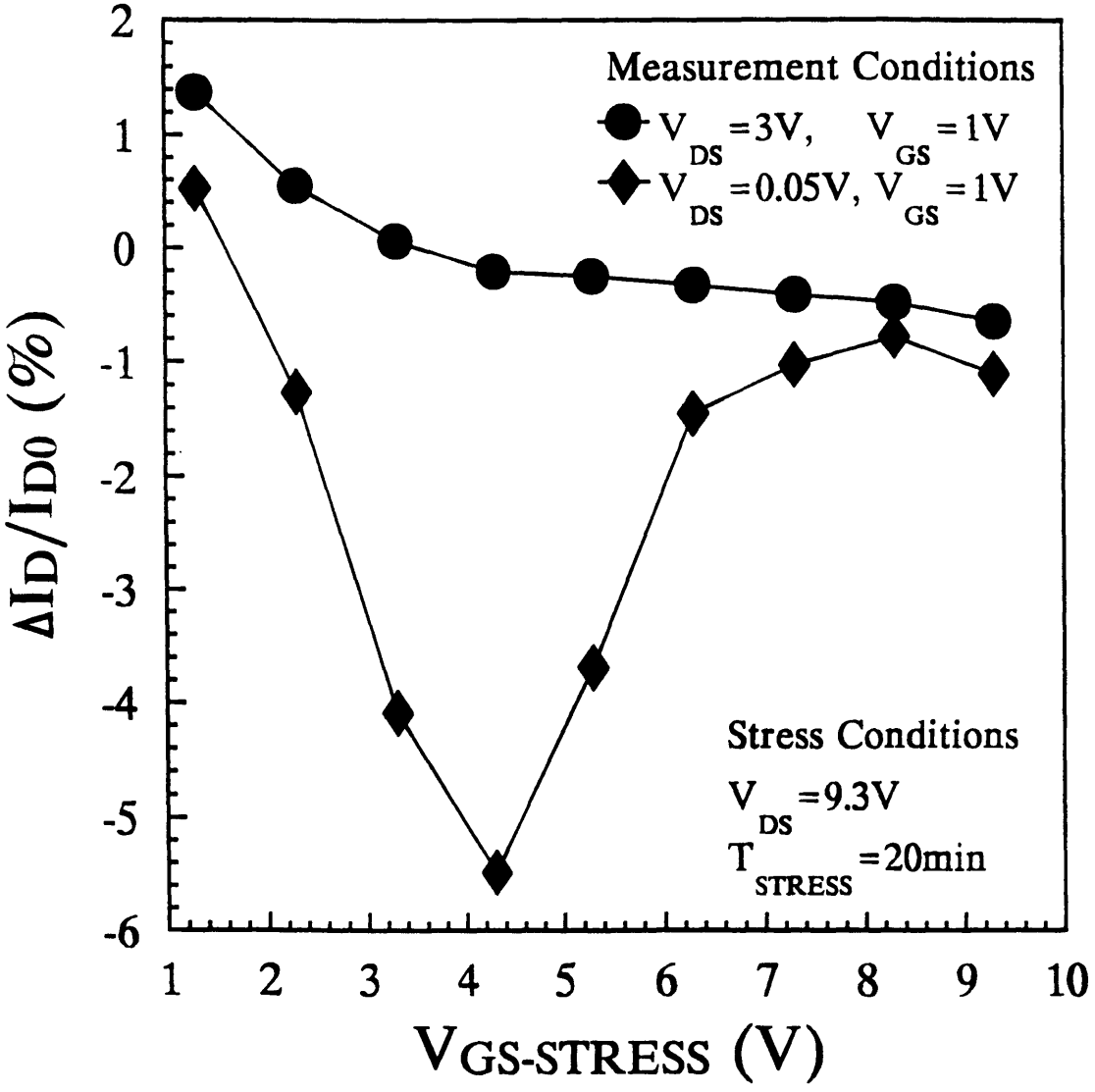

Fig. 5.1 NMOSFET current mismatch versus stress gate voltage. L=3μm, W=20μm, T_{ox}=35nm, V_T=0.8V.

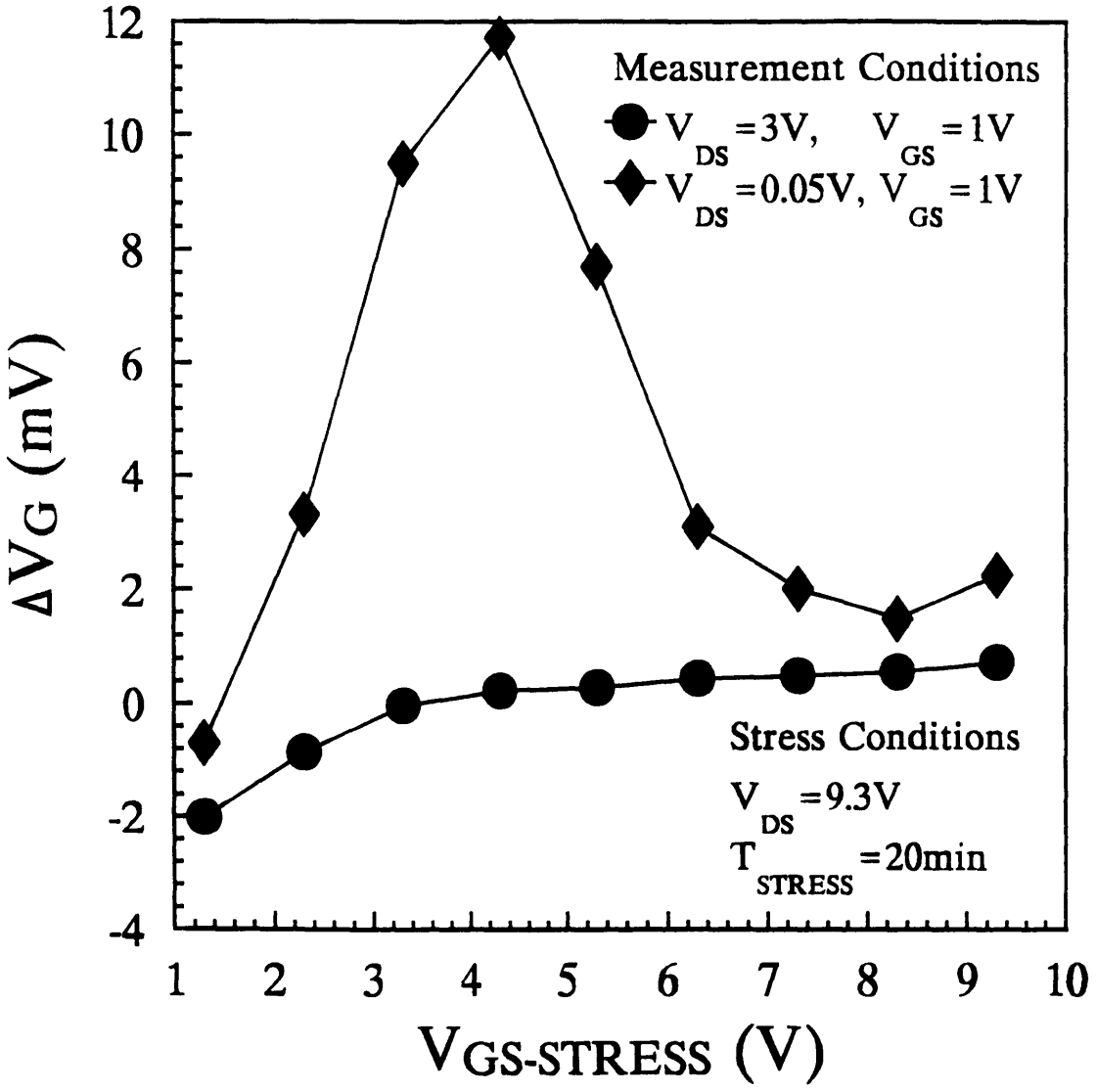

Fig. 5.2 NMOSFET gate voltage mismatch versus stress gate voltage. L=3μm, W=20μm, T_{OX}=35nm, V_T=0.8V.

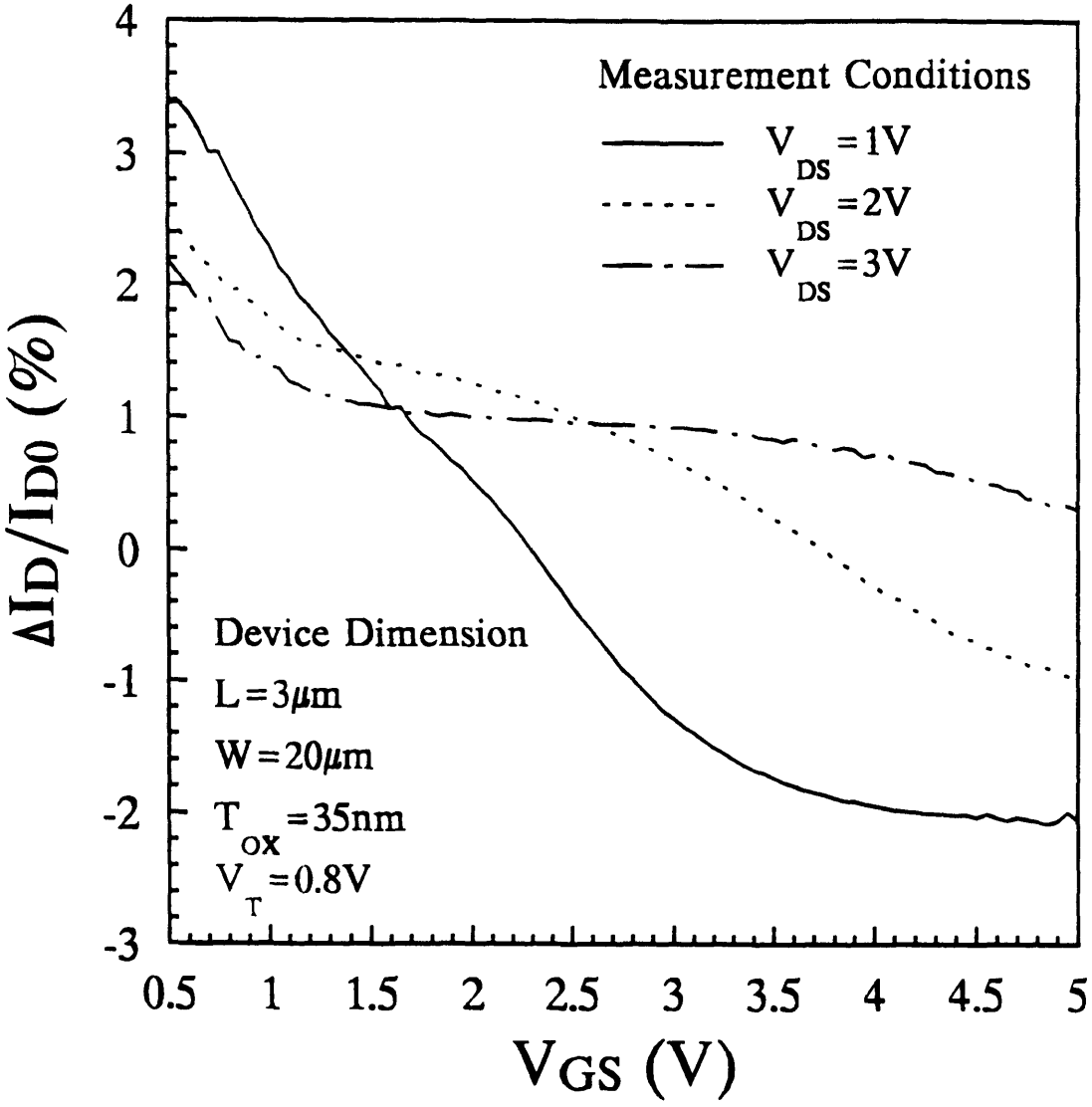

Fig. 5.3 NMOSFET current mismatch at different bias conditions. Stress condition: V_{DS}=9.3V, V_{GS}=1.3V, T_{STRESS}=20min.

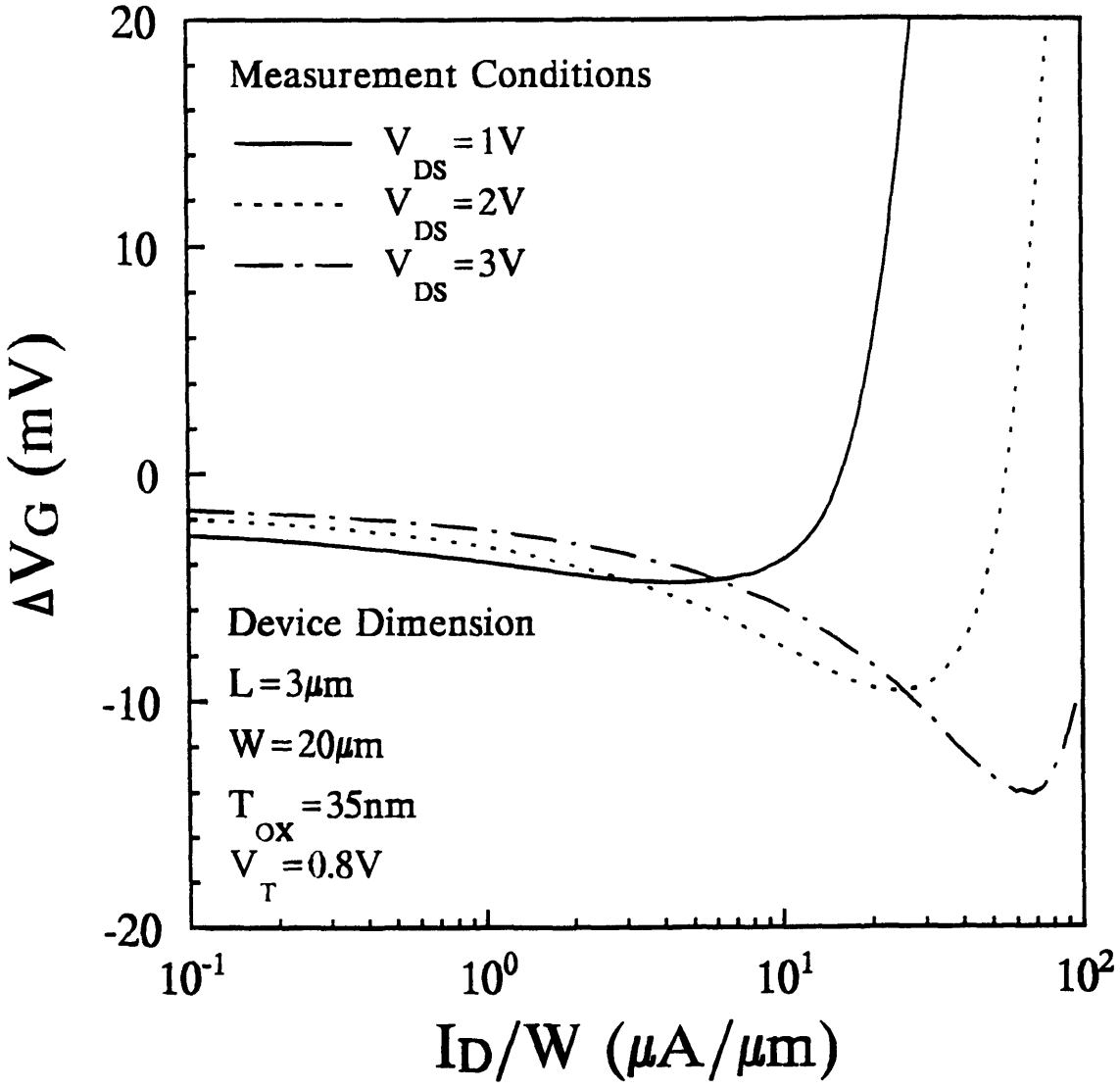

Fig. 5.4 NMOSFET gate-voltage mismatch at different bias conditions. Stress condition: V_{DS}=9.3V, V_{GS}=1.3V, T_{STRESS}=20min.

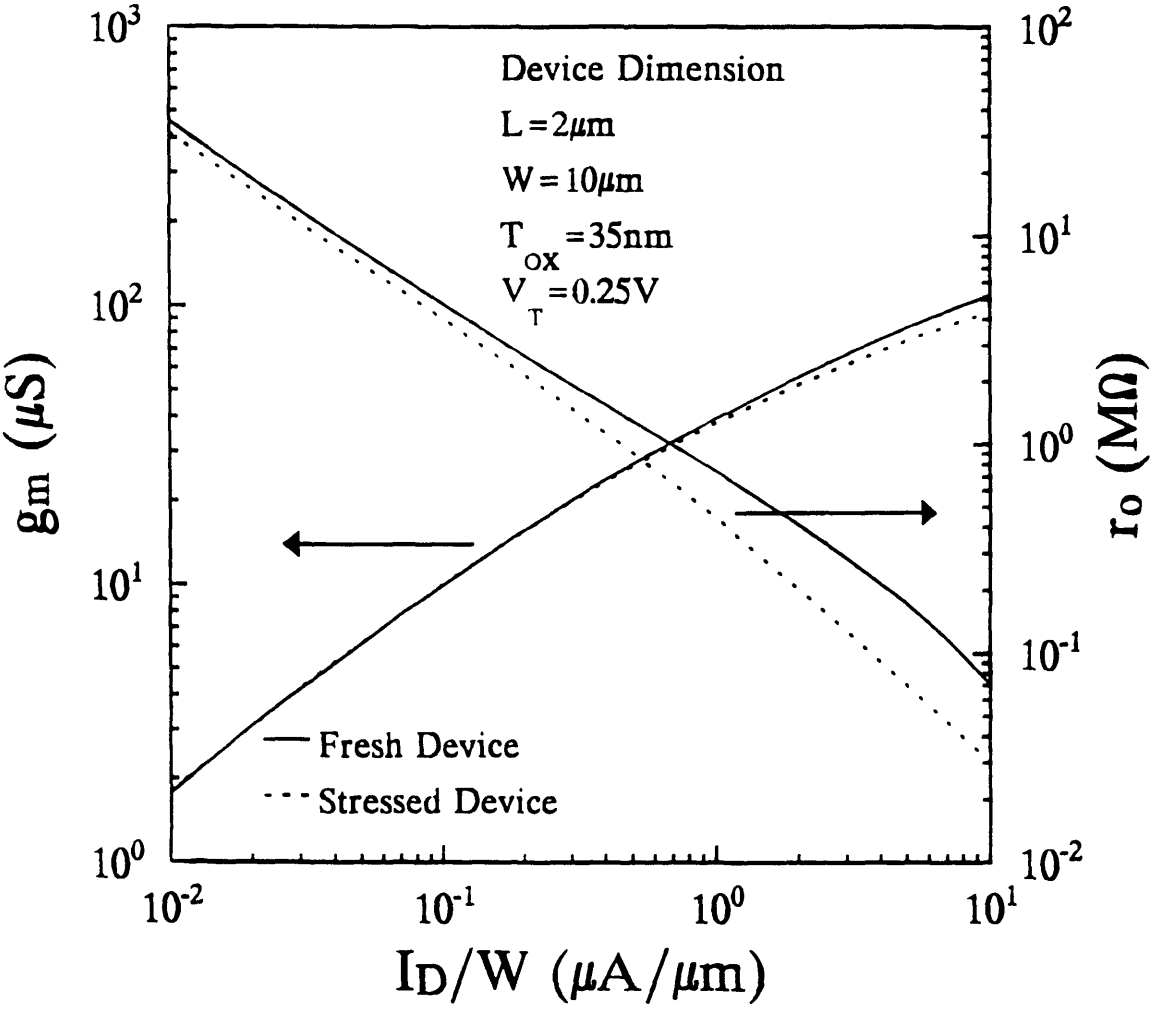

Fig. 5.5 NMOSFET transconductance and output resistance degradation as a function of drain current I_D. Stress condition: V_{DS}=9V, V_{GS}=1V, V_{BS}=-2V, T_{STRESS}=1000min. r_o and g_m were measured at V_{DS}=1V.

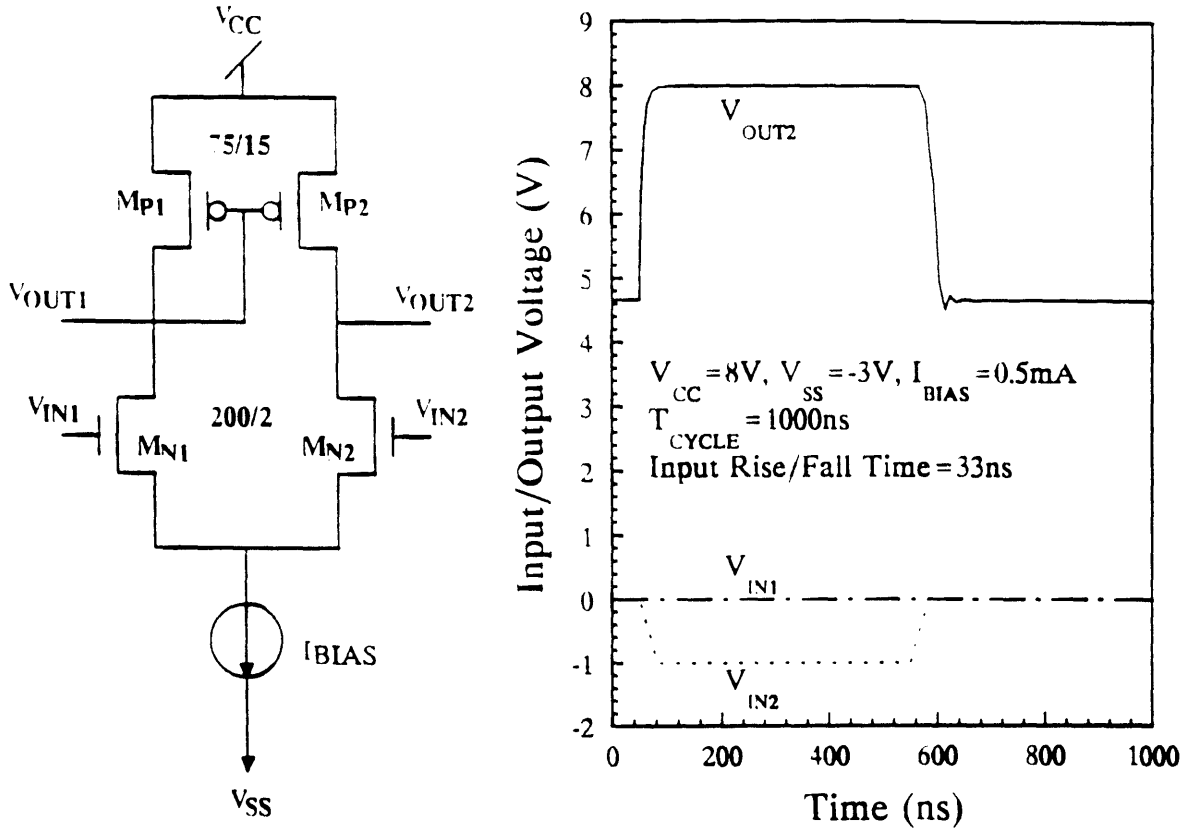

Fig. 5.6 Schematics of the differential amplifier test structure and SPICE-simulated stress input/output waveforms.

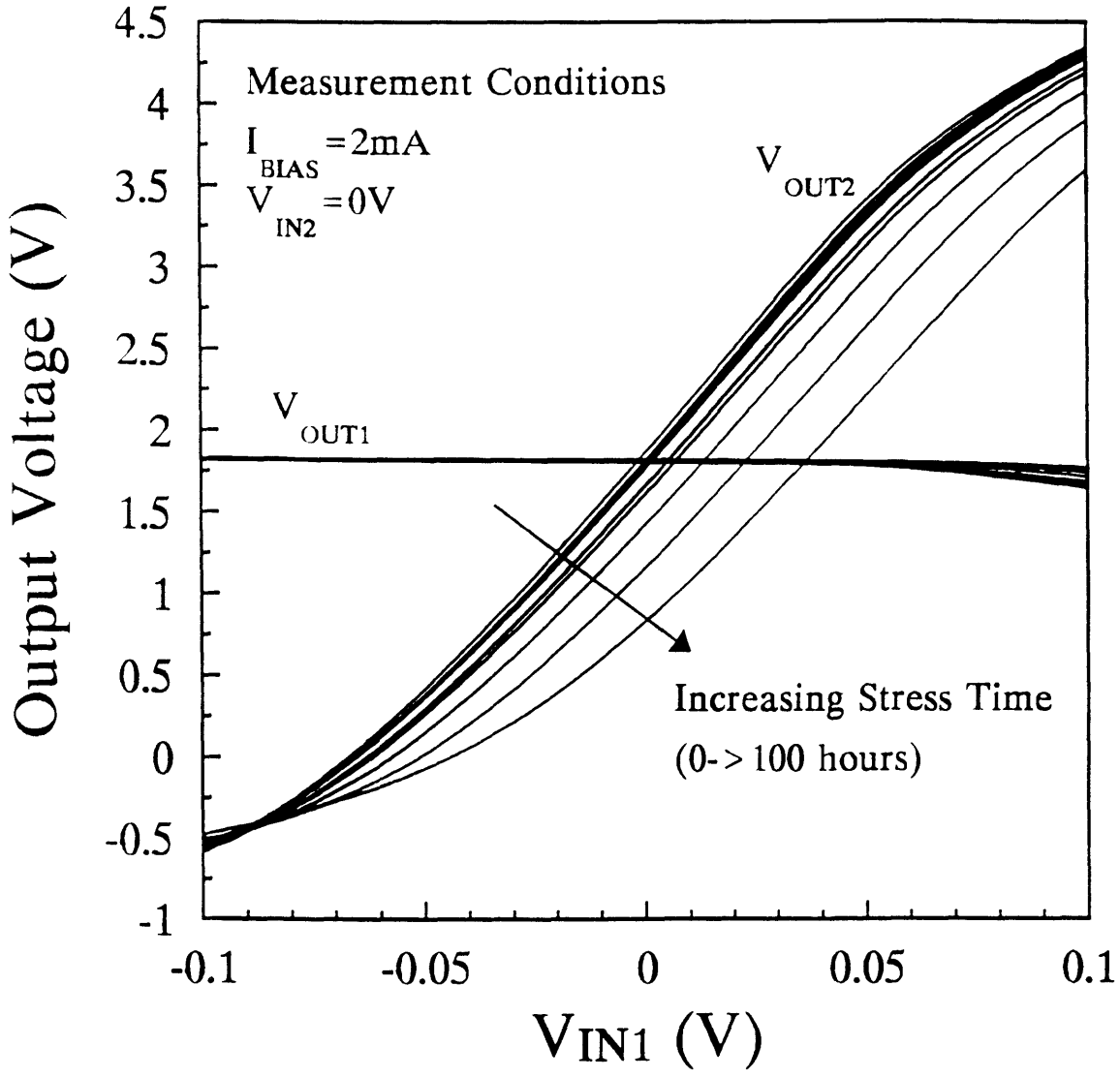

Fig. 5.7 Changes in DC transfer curves of the differential amplifier during stress.

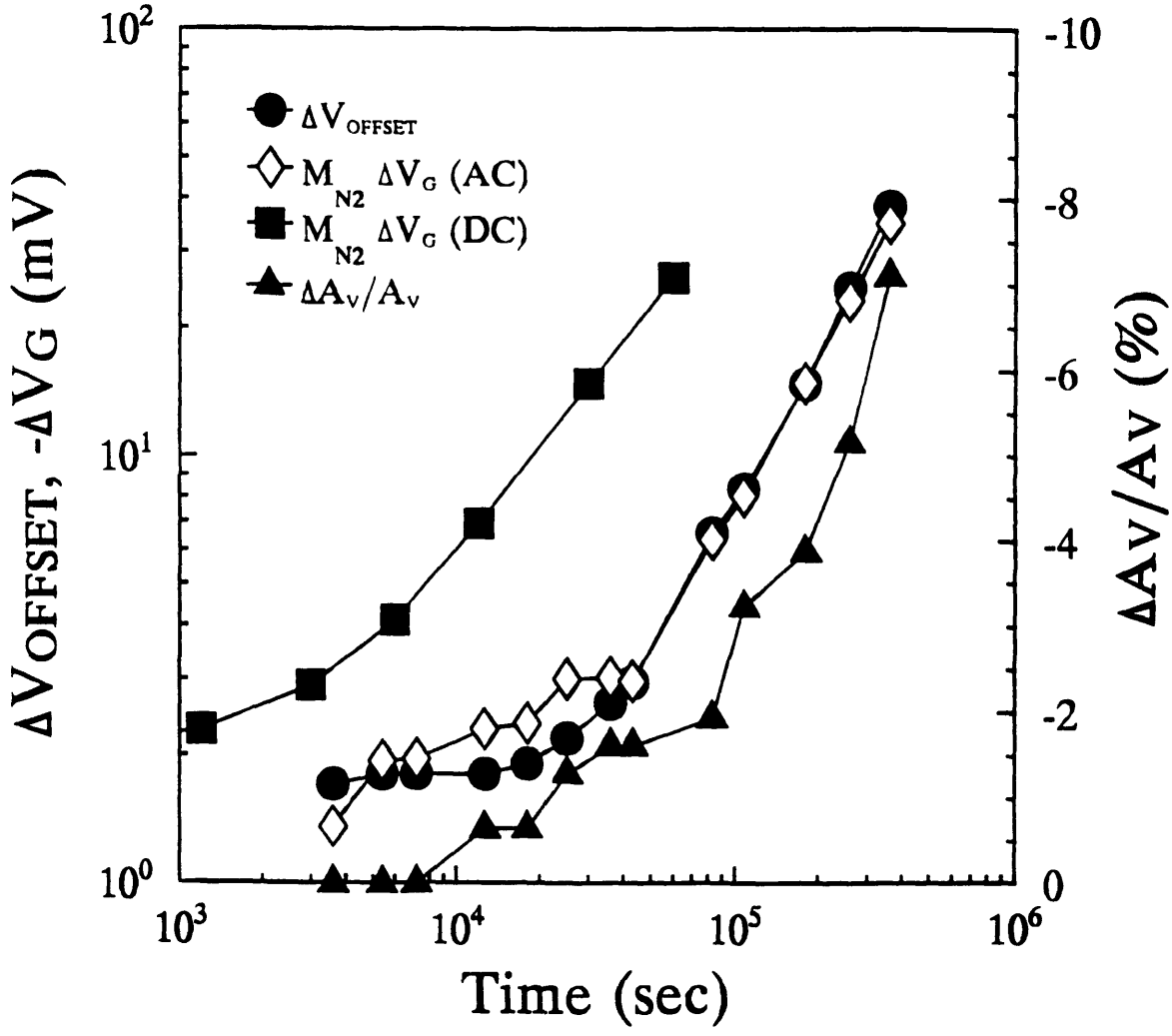

Fig. 5.8 Time dependence of circuit degradation parameters and the device gate-voltage mismatch. DC device stress condition: V_{DS}=9V, V_{GS}=1V, V_{BS}=-2V; measurement condition: I_D=5μA/μm, V_{DS}=3V, V_{BS}=-2V.

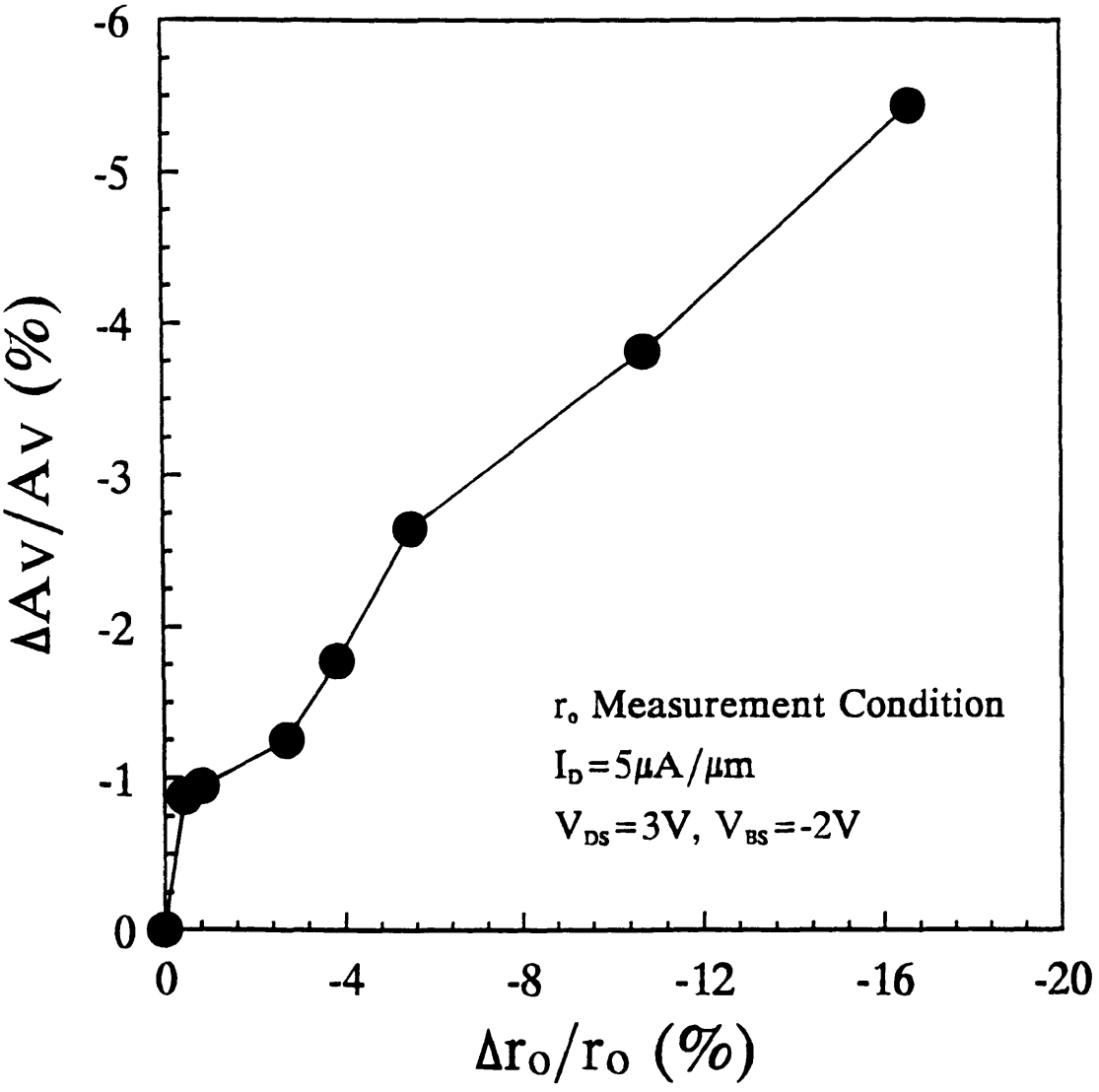

Fig. 5.9 Correlation between gain degradation in the differential amplifier circuit and r_o degradation in the NMOSFET M_{N2}.

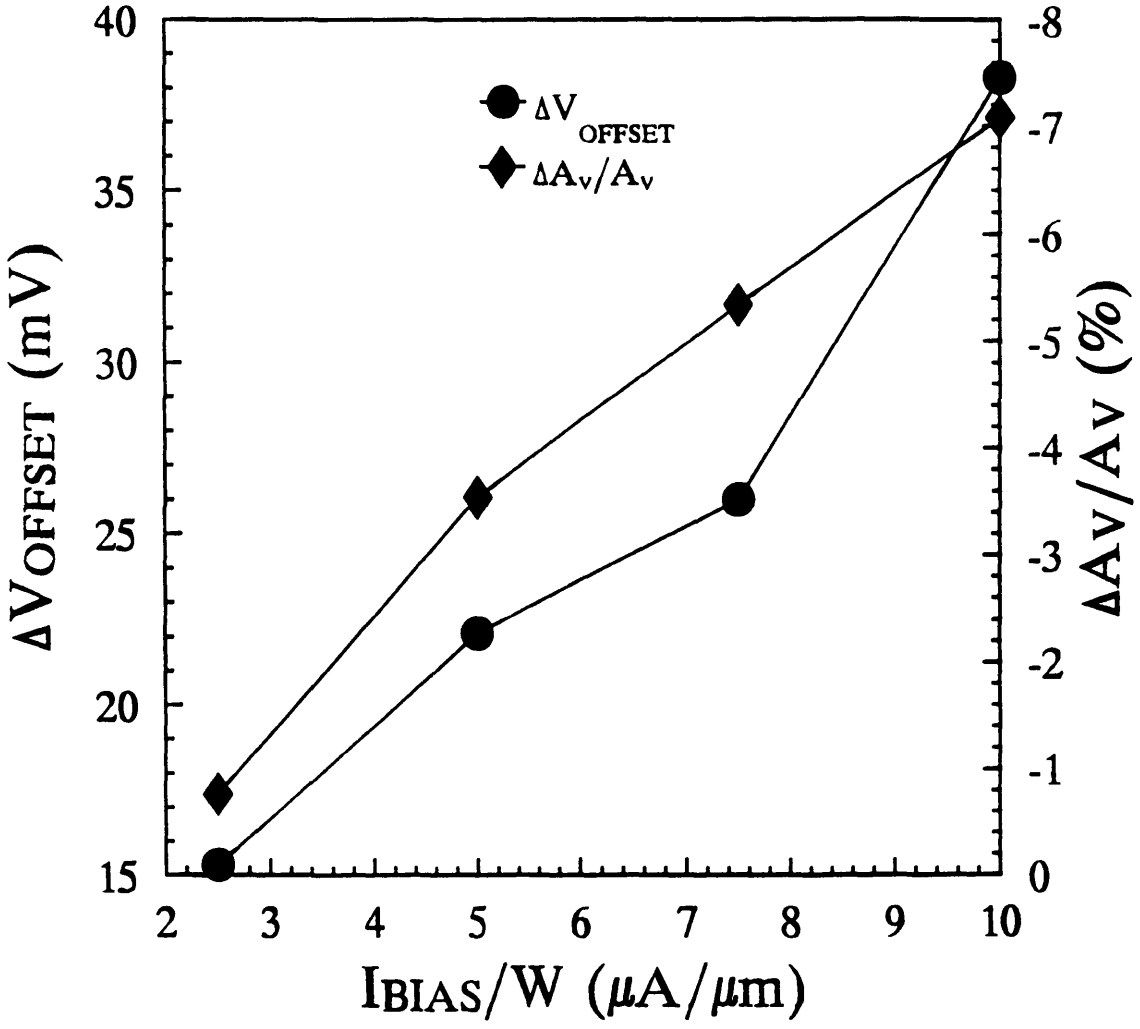

Fig. 5.10 Differential amplifier offset voltage and gain degradation for different operating bias current after 100-hour stress by using a 1MHz, 1V square wave input.

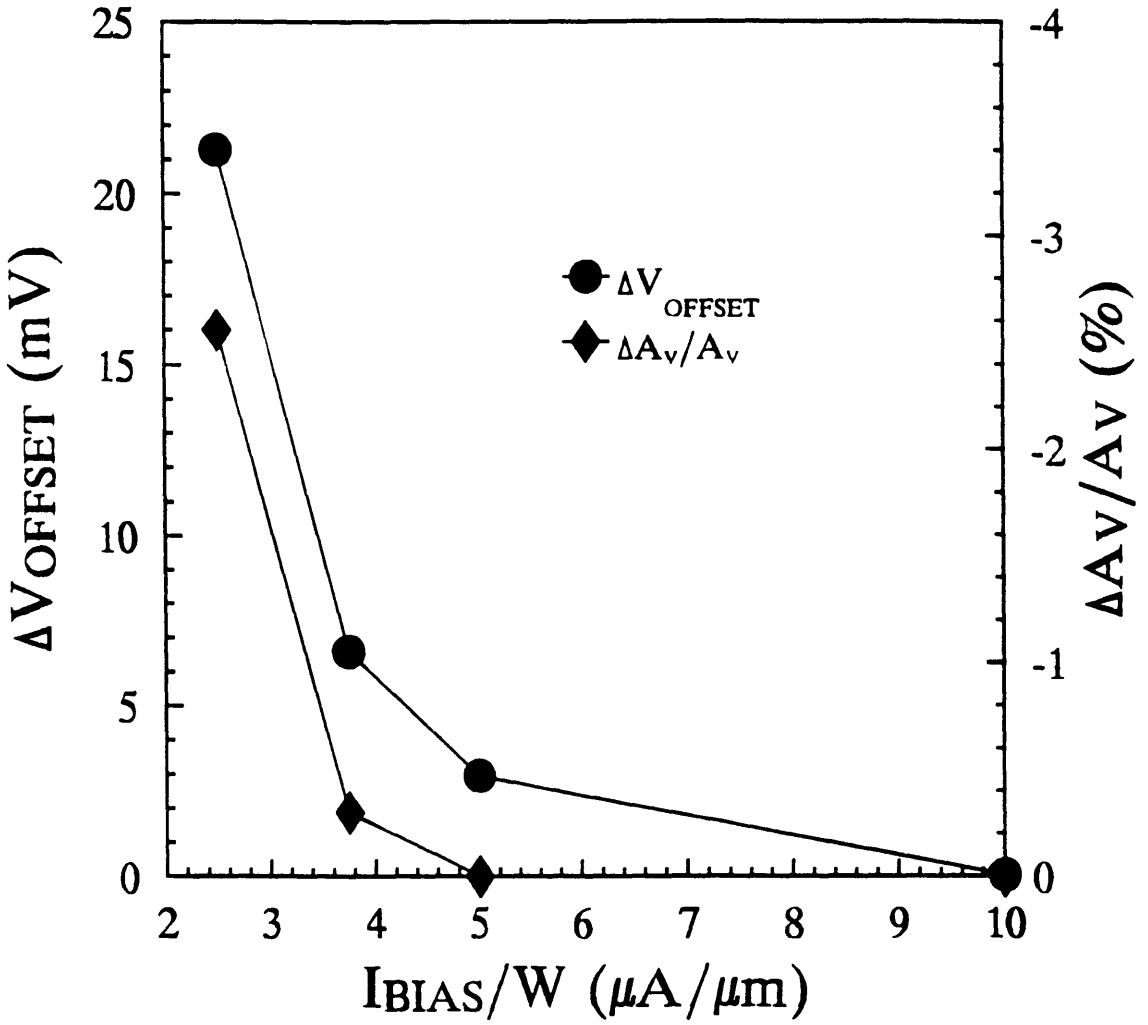

Fig. 5.11 Differential amplifier offset voltage and gain degradation for different operating bias current after 100-hour stress by using a 1MHz, 0.1V sinusoidal wave input.

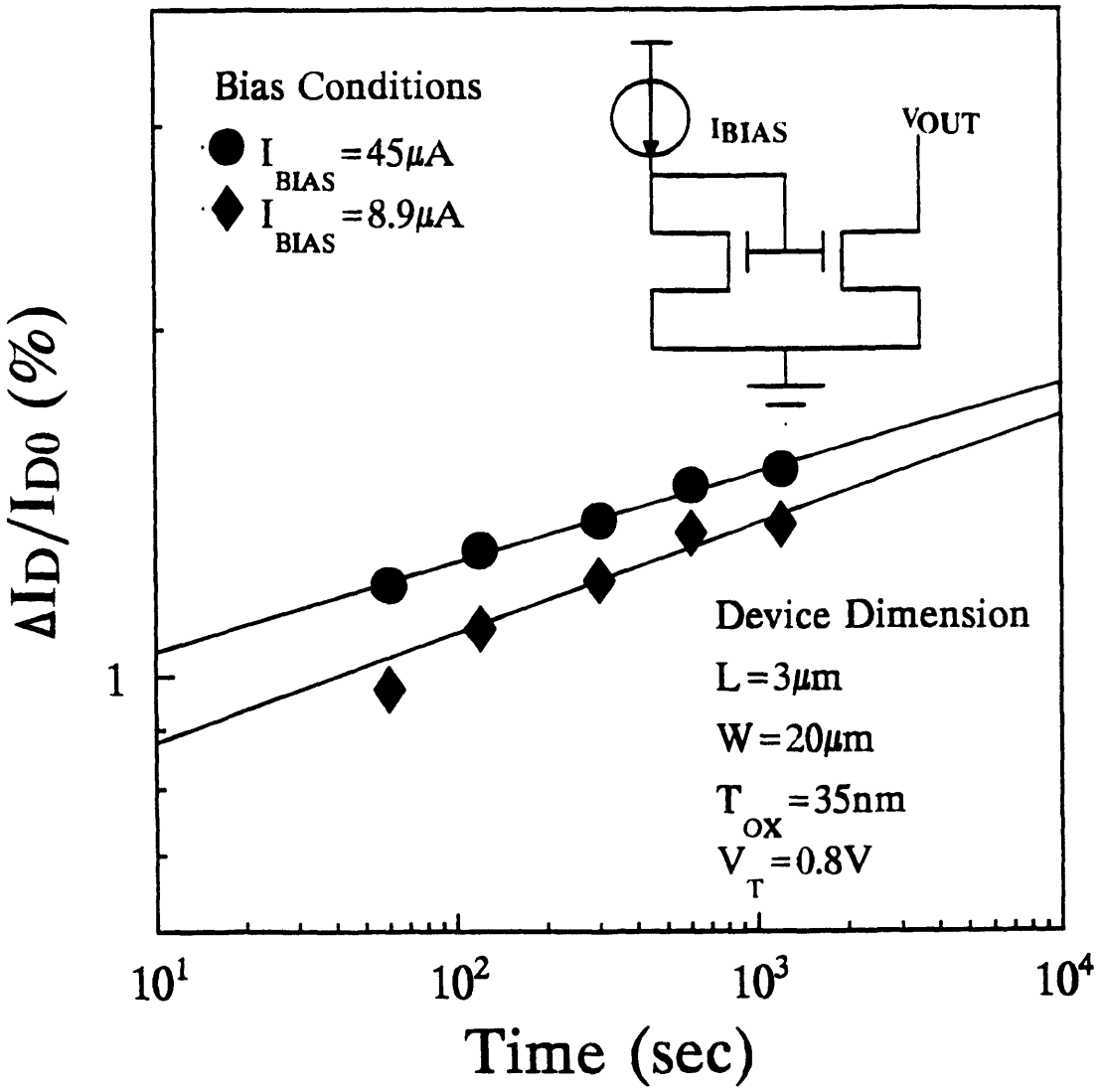

Fig. 5.12 Time dependence of current mismatch for NMOSFET current mirrors. Stress condition: V_{DS}=9.3V, T_{STRESS}=20min. I_D was measured at V_{DS}=2V.

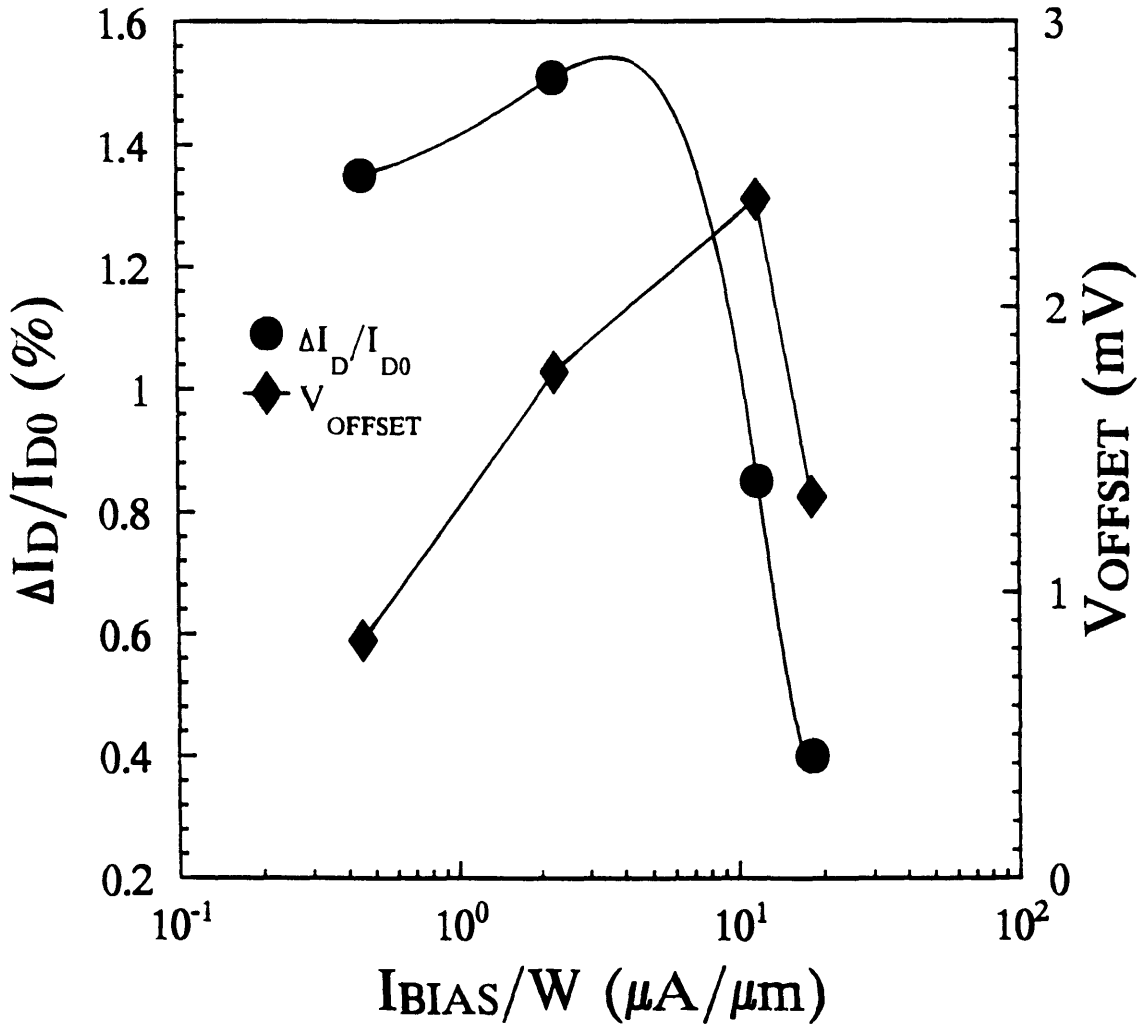

Fig. 5.13 Current mismatch and corresponding offset voltage of current mirrors versus bias current. Offset voltage was calculated assuming on input PMOSFET device with L=3μm, W=200μm, T_{OX}=35nm. Stress condition: V_{DS}=9.3V, T_{STRESS}=20min. I_D was measured at V_{DS}=2V.

Chapter 6

Conclusions

6.1. Summary

Due to reliability concerns imposed by hot carriers for the continuation of device scaling, this thesis has examined issues of hot-carrier degradation for CMOS devices and circuits. The primary purpose of this study is to investigate how devices degrade under AC circuit operation and the effects of device degradation on circuit performance. The results of this research help the transition from the traditional DC device-level reliability criteria to a more relevant AC circuit-level reliability criteria.

The structure of this thesis can be divided into two parts. The first part of this research concentrated on the understanding of device degradation behavior:

This research has evaluated NMOSFET hot-carrier reliability and proposed universal guidelines which are applicable to a wide range of bias conditions found in circuit operations. The degradation time dependence has been observed to follow an asymptotic behavior due to the non fully-overlapped source/drain structures such as LDD. The voltage dependence of interface-state generation is affected by the local oxide electric field near the drain ($E_{OX} \sim (V_G - V_D)/T_{OX}$). Also device nonuniformity can affect the statistical variation of hot-carrier lifetime. All three effects need to be taken into account and can have significant impact on lifetime evaluation. Discussions about the limits of stress conditions (stress voltage and time) were made to develop efficient and relevant

projections of hot-carrier reliability.

The asymptotic time dependence of NMOSFET was further investigated in detail. It was found out that the linear-current degradation of LDD NMOSFET results from mobility reduction due to damage (acceptor-type interface states) under the gate region and series-resistance increase due to damage under the LDD oxide spacer. As a result, the degradation time dependence exhibits two different regions which correspond to these two different degradation mechanisms. At first, the current degradation is due to series-resistance increase because most of the damage is generated in the LDD region. However, as enough negative charge accumulates under the oxide-spacer region, an inversion region is formed and, thus, limits the depletion width and increase in series resistance. Therefore, the current reduction in the latter stage of degradation is due to mobility reduction. An asymptotic slope which represents the reduction of carrier mobility is present and can be used for realistic lifetime evaluation purposes. This result also points out that a compact device model which includes both resistance and mobility effects is needed for accurate simulation of circuit degradation.

The second part of this thesis emphasized the evaluation of CMOS circuit degradation. Both digital and analog circuit test structures have been built and used to verify the quasi-static approximation and to determine the device degradation mechanisms under circuit operations. These circuit test structures have provided the benefits of realistic circuit operating waveforms, reduced inductive noise generation, and direct comparisons of device and circuit degradation.

For the evaluation of digital circuit reliability, ring-oscillator type test circuits with different fanouts and logic elements were implemented. Voltage overshoot due to capacitance coupling between output capacitance and overlap capacitance has been shown to induce enhanced degradation. The comparison between AC and DC device degradation indicated that the applicability of quasi-static approximation is in question. The degradation of NMOSFET devices in high-frequency digital circuits displayed different damage (acceptor-type interface states) generation rates. Separate AC device experiments

also exhibited this frequency-dependent generation rate. For PMOSFETs, besides electron trapping, the device degradation also showed additional donor-type interface state generation and significant electron detrapping which are not observable in typical DC device stress experiments. These novel phenomena are believed to be due to the large voltage swings in digital circuits. As the gate voltage traverses various regions, both hot hole and electron injection occur in a short time. As a result, interaction between different mechanisms is possible under high-frequency, short-transient digital circuit operating conditions.

For the evaluation of analog circuit reliability, differential amplifiers and current mirrors were used. The particular operating conditions have different impact on hot-carrier reliability. Because the gate-to-source voltage in typical analog circuits is only 100-500mV beyond threshold voltage, this voltage range results in a dominant oxide trapping mechanism (hole traps in NMOSFETs and electron traps in PMOSFETs). Also, because the gate voltage swing in analog circuits is typically much smaller as compared to digital circuits, devices under circuit stress are very similar to devices under DC stress. Therefore, DC degradation models with appropriate duty-cycle correction (quasi-static approximation) can be used to accurately estimate the device degradation under AC circuit operations.

In conclusion, the dominant device degradation mechanisms relevant to circuit operation were identified in this thesis. The different operating conditions between digital and analog circuits have major effects on how the devices degrade. The large gate voltage swing in digital circuits induces the presence of multiple degradation mechanisms and, as a result, invalidates the direct application of the quasi-static approximation. In NMOSFETs, the interface-state generation rate is different. However, the voltage dependence, which is related to the critical energy for damage generation, in my opinion, will not change. In PMOSFETs, significant detrapping in AC conditions makes the oxide traps less a reliability problem. On contrary, the small signal nature of analog circuits induces DC-like device degradation which makes the quasi-static approximation applicable. Also the small DC gate bias voltage (near V_T) in analog circuits makes the

oxide trapping mechanism more important than interface states.

6.2. Future Research Topics

1. It has been shown in Chapter 2 that the damage generation in NMOSFET depends on the local oxide electric field. This dependence will have a large effect on both device lifetime [6.1], [6.2] and circuit-level reliability evaluations where various bias conditions are used [6.3]. Possible explanations about this effect are the effect of field-dependent damage generation [6.4] and field-dependent hot-carrier injection into the oxide [6.1]. In order to have degradation models which are applicable to various bias conditions and technologies, the physical mechanism needs to be understood and a suitable model needs to be developed.

2. Both circuit and device experiments have shown different NMOSFET damage generation rates under high-frequency, short-transient gate waveforms (Chapter 4). The understanding of this phenomenon is crucial for the evaluation of AC NMOSFET device degradation. The physical mechanisms, voltage dependence, and appropriate degradation models need to be developed.

3. Results in this thesis (Chapter 4) have indicated that the electron trapping mechanism in PMOSFETs is unlikely a reliability concern for digital circuits due to significant detrapping in AC circuit operation. However, as the channel length of PMOSFET devices becomes shorter, hot-hole injection induces additional degradation mechanisms - donor-type interface state and positive oxide charge generation [6.5]-[6.7]. The importance of these new mechanisms in digital circuit reliability is unclear. Proper modeling of the time dependence, voltage dependence, and effects on device characteristics is needed for evaluation of their impact on circuit performance.

4. Because the gate-to-source bias voltage in analog circuits is very small (near V_T), the oxide trapping mechanism is observed to have a more significant impact on analog circuit

performance than interface-state generations. The primary effect of these oxide traps (hole traps in NMOSFETs and electron traps in PMOSFETs) is the channel-shortening effect. In order to predict and simulate the impact of channel-shortening effect on the performance of analog circuits, further works are needed to model the bias dependence and examine the effects on device characteristics.

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Appendix

Test Structures for Circuit-Level Hot-Carrier Reliability Evaluation

A.1. Introduction

While DC device-level reliability testing has been used extensively by the semiconductor industry, the use of circuit test structures becomes necessary as the determination of hot-carrier reliability shifts from DC device-type evaluation to AC circuit-type evaluation. This migration is fueled by recognizing the impact of device degradation on circuit performance: (1) It has been identified that hot-carrier reliability criteria based on device-level performance constraints such as threshold voltage (V_T) or transconductance (g_m) do not necessarily reflect the degradation of circuits and systems which use a different set of performance monitors such as propagation delay time (t_{pd}) for digital circuits and amplifier gain (A_V) for analog circuits. In order to choose a more relevant reliability criterion, the link between the device and circuit degradation must be established; (2) As scaling of CMOS devices continues aggressively, the application of traditional device-level criteria becomes harder to meet for today's deep submicrometer dimensions. Therefore, the use of AC-type circuit reliability criteria not only are more appropriate for circuit operations, but also are necessary to meet today's reliability requirements.

In order to answer this challenge, a lot of effort has been spent on developing

simulation tools to predict accurately hot-carrier degradation based on AC circuit operation and to evaluate the impact of device degradation on circuit degradation. These reliability programs either use SPICE [A.1], [A.2] or timing simulators [A.3], [A.4] to generate accurately AC voltage waveforms. Then, the total device degradation can be obtained by summing up degradation in small time slices, based on quasi-static approximation (see (1.7) and (1.8)). As a result, the overall circuit degradation can be simulated by using degraded device models through empirically fitting [A.1] or theoretical calculations [A.5] in SPICE or timing simulators.

However, these approaches have no or little experimental verification and exhibit severe limitations: (1) Precise voltage-waveform modeling is necessary for calculating device hot-carrier degradation because of the exponential dependence of degradation on the applied voltage waveforms. Thus, macromodels or timing simulation may not be sufficient to deal with problems such as capacitance coupling through either device parasitics and interconnect [A.6]; (2) The applicability of the quasi-static approximation is never fully verified in AC circuit environments. As a result, the models used in today's reliability simulators may not be accurate and applicable for circuit-level reliability simulation [A.6], [A.7].

Also in the past, several studies have used pulsed AC device experiments to study AC device degradation. The use of different pulse waveforms often produces different results [A.8]-[A.10]. One common problem associated with the pulsed device experiments is the large inductive noise generation at device nodes when a short-transient current is induced by short-transient gate waveforms. This experiment artifact has been shown to result in the observed enhanced degradation. Other problems for this technique are the use of unrealistic waveforms and the lack of correlation between degradation of devices and circuits.

Due to these limitations, circuit test structures are necessary to provide not only verification vehicles for reliability simulations, but also early failure analysis in technology development stages.

A.2. The Requirements for Circuit Test Structures

In order to accomplish the goals of verifying the AC degradation mechanisms and its impact on circuit performance, circuit test structures must comply with the following requirements to avoid the problems commonly occurred in simulation and pulsed AC device studies.

(1) The test structures must reflect the actual operation in real circuit environments. For digital circuits, this means that the circuits need to operate at +100MHz with rise/fall times in the range of 100-500ps to mimic today's advanced 0.35μm-0.5μm CMOS logic circuits operation such as microprocessors using submicrometer dimensions. For analog circuits, suitable DC bias voltages and appropriate high frequency input/output waveforms should be used.

(2) Correlation between the device and circuit needs to be established. It means that the characteristics of circuits (for example, stage delay time for digital circuits and voltage gain for analog circuits) and devices (for example, device current characteristics for digital circuits and output resistance for analog circuits) embedded in circuits need to be directly measured. This will facilitate the direct comparison between device and circuit degradation without using questionable extrapolation and simulation techniques.

(3) The circuits need to be designed for easy reliability testing without interfering with the circuit operation. Buffering or high-frequency probes such as Picoprobes® are necessary for high-frequency input and output signals. Pass transistors should be placed to isolate the effects of pad capacitance. Also appropriate multiplexing to accomplish parallel testing can be used to reduce drastically reliability testing time.

By satisfying these requirements, device degradation mechanisms relevant to circuit operation can be studied and the effects of device degradation on circuit performance can be evaluated. The following sections will explain the detailed digital and analog circuit test structures for hot-carrier reliability evaluation.

A.3. Test Structures - Digital Circuits

The test structures for digital circuits are combinations of typical digital benchmark circuits which provide a yardstick for a particular CMOS technology and some unique reliability testing features which facilitate testing of both circuit and device degradation. The most commonly used benchmark circuits for CMOS technologies are ring oscillators [A.11] and chain structures [A.12].

A.3.1. Ring Oscillators Structures

Fig. A.1 illustrates a schematic for a typical ring oscillator circuit. This circuit is operated by a DC supply voltage. An odd number of logic elements such as inverter, NOR, and NAND gates are connected in a closed loop. The oscillation frequency can be calculated by

$$f_{osc} = \frac{1}{2 \cdot N \cdot t_{pd}} \qquad \textbf{(A.1)}$$

where N is the total number of logic elements and t_{pd} is the average propagation delay time. The advantages of such structures are: (1) the circuit is self-actuating and thus, no external signal is required; (2) the performance of the circuit can be easily tested by measuring oscillation frequency.

Based on (A.1), larger number of stages makes the measurement easier to accomplish. However, smaller odd and prime number of stages is used to not only alleviate harmonic generation of the fundamental frequency [A.13], but also increase the usage of individual logic gates to reduce the testing time. The stage delay time versus power supply voltage is shown in Fig. A.2 for inverter ring oscillators used in Chapter 4.

A special structure was implemented to allow for individual device probing in a

ring oscillator as shown in Fig. A.3 without using complex and expensive equipments such as electron beam probing [A.14]. During normal circuit operation, the pass transistors are switched off to prevent interference from the probing pads. Without using these pass transistors, the rise and fall time of logic operation would slow down greatly. Thus, the employment of these pass transistors insures that the logic gate retains its fast transient characteristics. During device measurements, these pass transistors allow direct access to both the NMOSFET and PMOSFET devices in the logic gate. Vddrive node is used to apply voltage and supply drain current through the transmission gate. Because of the voltage drop due to on-resistance of the T-gates, a separate pad (Vdsense) and a pass transistor are used to measure the actual voltage at the device drain node.

The ring oscillator allows us to measure circuit degradation

$$\frac{\Delta f_{osc}}{f_{osc}} = -\frac{\Delta t_{pd}}{t_{pd}} \qquad \textbf{(A.2)}$$

which can be directly compared to $\Delta I_D/I_D$ of both NMOSFET and PMOSFET devices under AC circuit stress. Also direct comparison between DC and AC device degradation can be accomplished by using this structure (Section 4.5).

Another advantage of this structure is that the circuit degradation due to NMOSFET and PMOSFET can be decoupled and examined individually by DC stress of NMOSFET or PMOSFET devices embedded inside the circuit (Section 4.6).

These structures have been successfully implemented and built by Hewlett-Packard ICBD TDC facility at Palo Alto, CA. A layout plot is shown in Fig. A.4. Detailed analysis of the result can be found in Chapter 4. Because digital circuits are less sensitive to individual device degradation, the minimal stress time to observe a reasonable value of degradation is long. As a result, the output signals of eight circuits are multiplexed to accomplish parallel testing to drastically reduce reliability testing time.

The main limitation for ring oscillators is that it is only applied for static-logic

circuits which do not need external input signals. Dynamic logic circuits which are often preferred for their fast operations and smaller sizes can not be implemented in ring oscillator structures.

A.3.2. Chain Structures

For circuits which require external signals (such as clock signals), chain structures are more suitable. Fig. A.5 shows a typical example of chain structures. The main difference to ring oscillators is that the operating loop is open and thus, external input signals are needed. To measure the circuit delay time across the chain structures, two identical structures are constructed with different stages numbers. Only differential signals are measured to ensure the evaluation of the true stage delay time. As a result, the delay time associated with input and output buffers can be completely canceled.

$$t_{pd}=\frac{\Delta t}{\Delta N} \qquad \text{(A.3)}$$

where the Δt is the time delay between the two chains; ΔN the stage difference.

In order to perform on-chip stress to avoid the measurement-setup-induced noise contribution to hot-carrier degradation, an internal clock signal is used. The internal clock signal is generated by on-chip voltage controlled oscillators (VCO). A simple realization of a VCO is shown in Fig. A.6 [A.15]. The transmission gates between stages of this ring oscillators serves as voltage controlled resistors. By varying the voltage VCOcntl1 and VCOcontl2 and thus, the resistance of the transmission gates, the user can control the RC time constant of the ring oscillator.

Domino logic circuits are ideal candidates for the chain structures. A latched domino logic inverter is shown in Fig. A.7. When these domino logic gates are connected, a precharge phase is initiated by the global clock signal supplied by VCO. The evaluation of the logic gate will be initiated by the input signal from the previous

stage [A.11].

This structure has been implemented using MIT baseline CMOS process and currently in fabrication. Detailed information about the whole test chip can be referred to reference A.16.

A.4. Test Structures - Analog Circuits

In this study, fundamental building blocks - differential amplifiers and current mirrors for analog circuits are chosen as the bases for the evaluation of hot-carrier degradation.

A schematic of the single-ended differential amplifier test structure is shown in Fig. A.8. The input and output nodes where high frequency signals over 1MHz may pass through need special attention in structure design and test configurations. For input nodes where there exists an infinite resistance, a passive high frequency coaxial probe such as Model 10 Picoprobe® can be used [A.17]. These kind of probes, which typically have frequency bandwidth up to several GHz, should be enough for testing of analog circuits. A terminating 50 ohm resistor needs to be used at the end of probe tip (supplied by the probe-tip manufacturer) or on the test wafer (designed by the test-structure designer) to maintain a constant impedance along the signal path and reduce the signal reflection.

The output nodes which are high impedance nodes for voltage gain purposes are able to drive capacitance loads. So the output voltage can be measured by using an active Picoprobe® with input impedance smaller than 1 pico farad. Another way to measure is to route the signal through a source follower with low impedance output. However, direct access of device nodes is then blocked.

An additional pad is put on the source node of this source-coupled pair. The additional pad enables us to measure the device characteristics directly. Because the

source node in the differential amplifier is a low-impedance node, the contribution of this additional pad and probe capacitance should have very limited impact on the circuit operation especially for fully differential operation where the source node is AC grounded.

Current mirror test structures can be implemented directly as shown in Fig. 5.12. The gate voltage is set by the external current source (I_{BIAS}) and remains constant throughout the circuit operation. The output voltage waveform (V_{OUT}) can be set externally to simulate various circuit operation. The circuit sensitivity to hot-carrier degradation can be studied by varying I_{BIAS} and V_{OUT} for different experiments.

These structures have been successfully implemented and built by Analog Devices, Inc. at Wilmington, MA. A layout plot is shown in Fig. A.9. Detailed analysis of the result can be found in Chapter 5.

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Picoprobe is a trademark of GGB Industries, Inc.

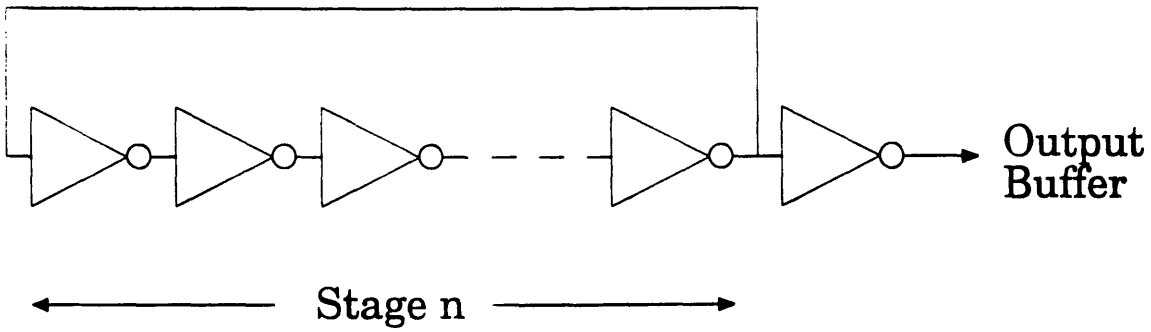

Fig. A.1 Schematic of the ring oscillator structure for digital static-logic circuit reliability testing.

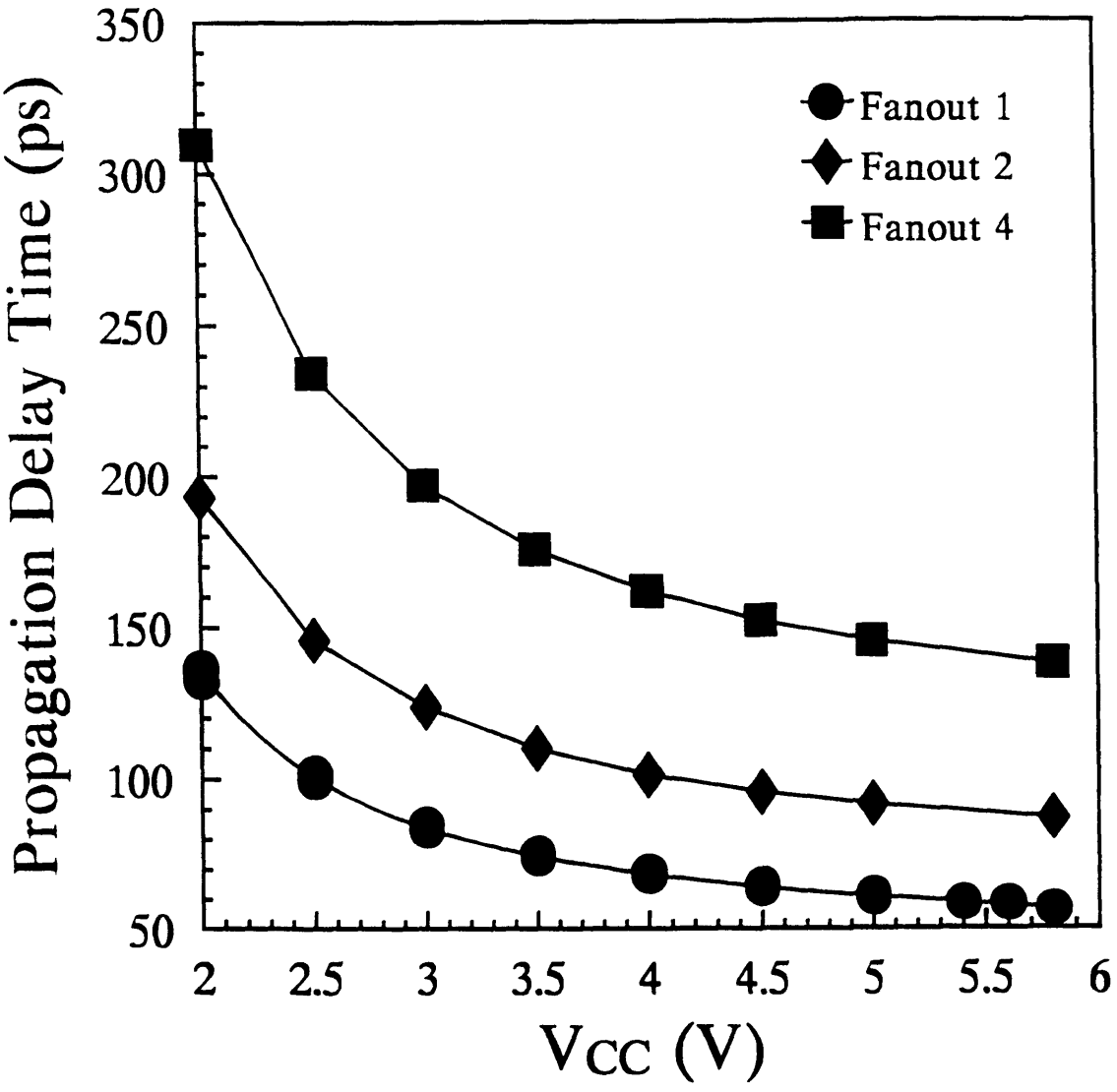

Fig. A.2 Stage propagation delay time versus power supply voltage for inverters with different fanout factors.

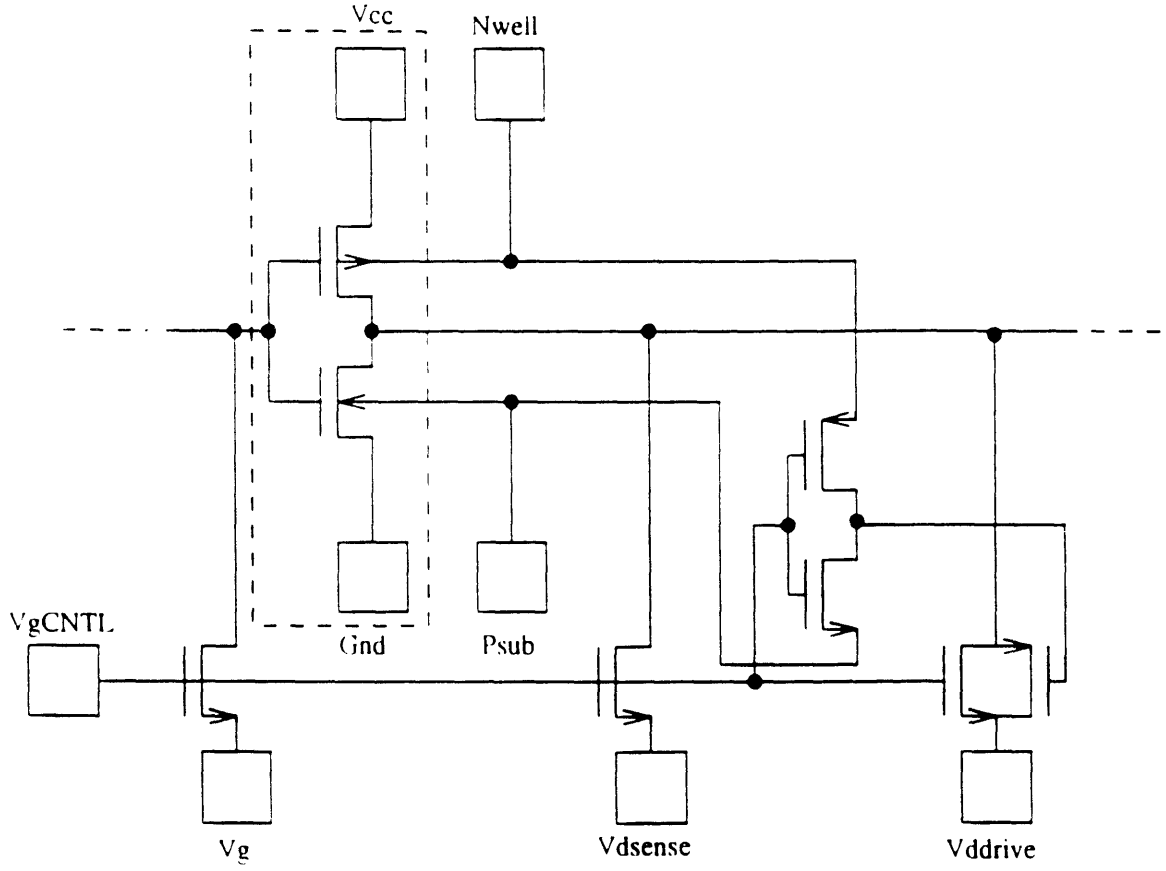

Fig. A.3 Special structures to allow individual device probing.

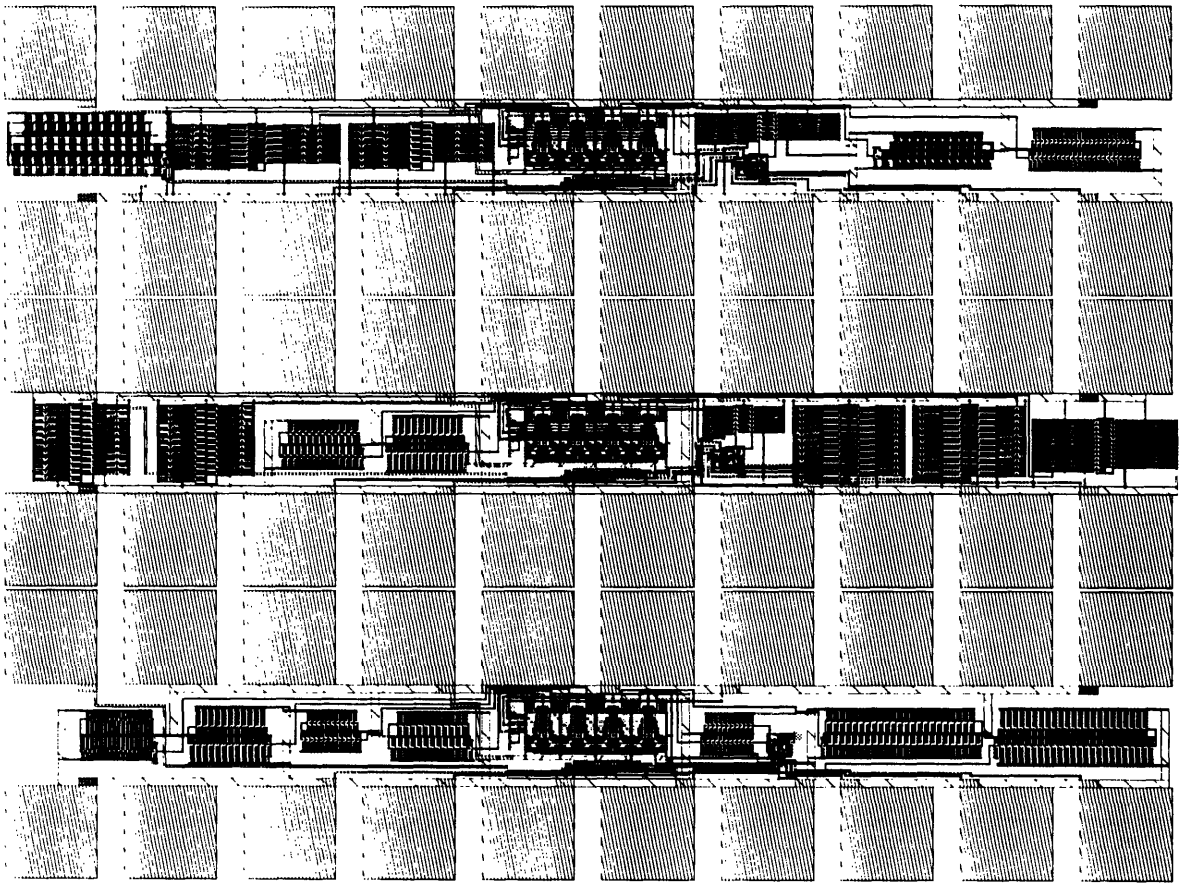

Fig. A.4 Layout plot for implementation of ring-oscillator test structures.

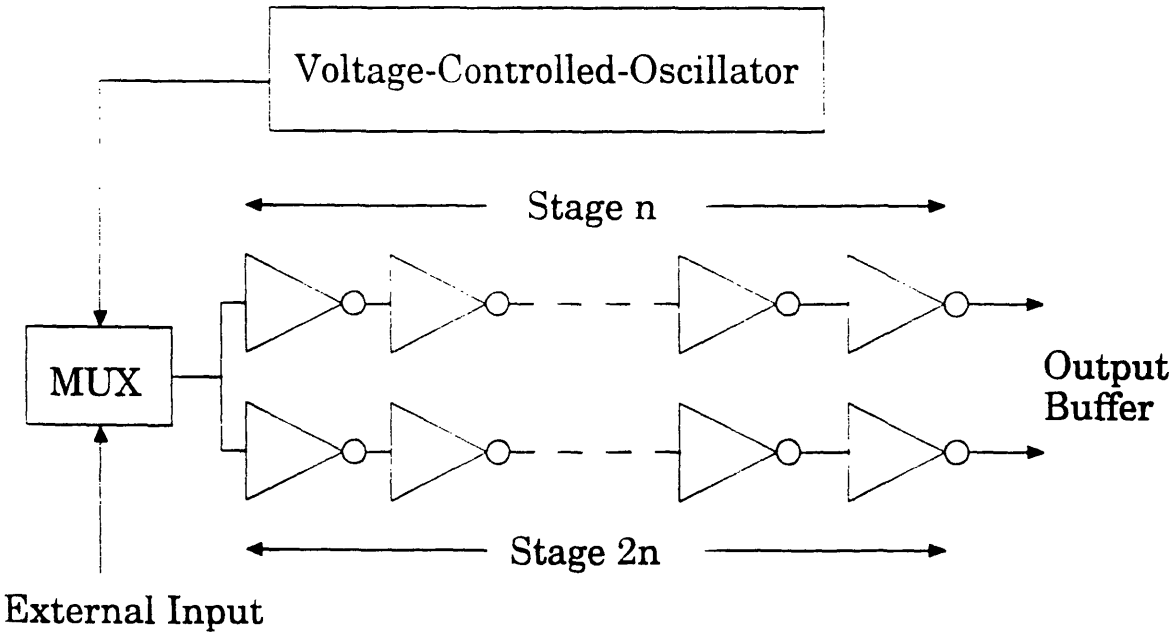

Fig. A.5 Schematic of the chain structures for digital circuit reliability testing.

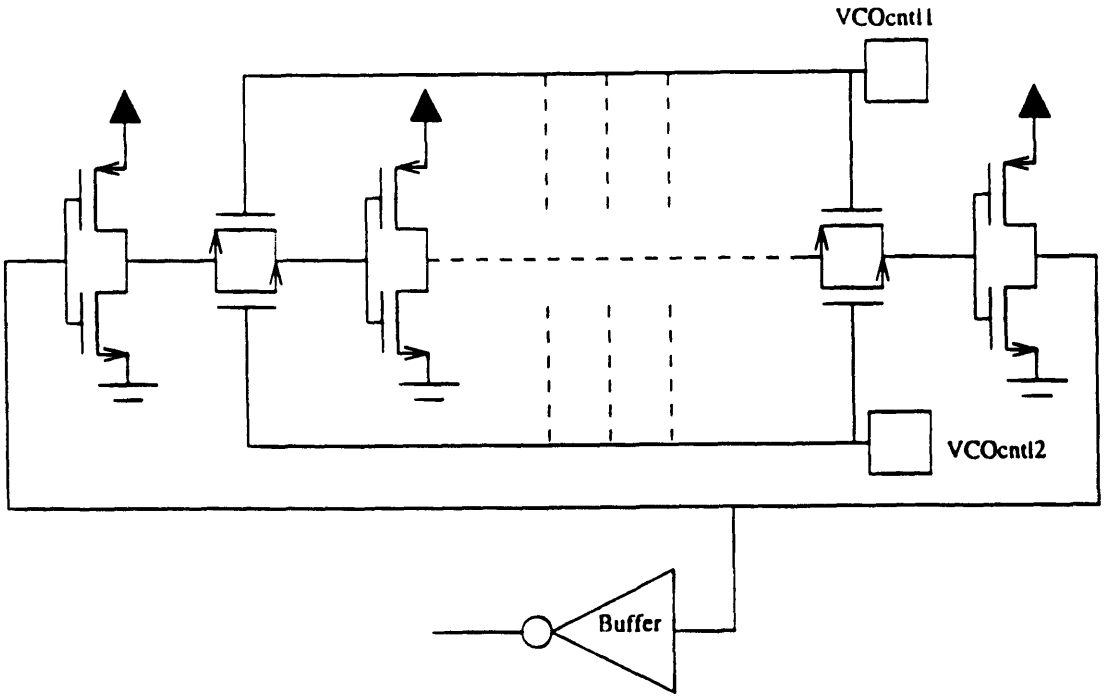

Fig. A.6 An implementation of voltage-controlled oscillators for on-chip clock signal generation.

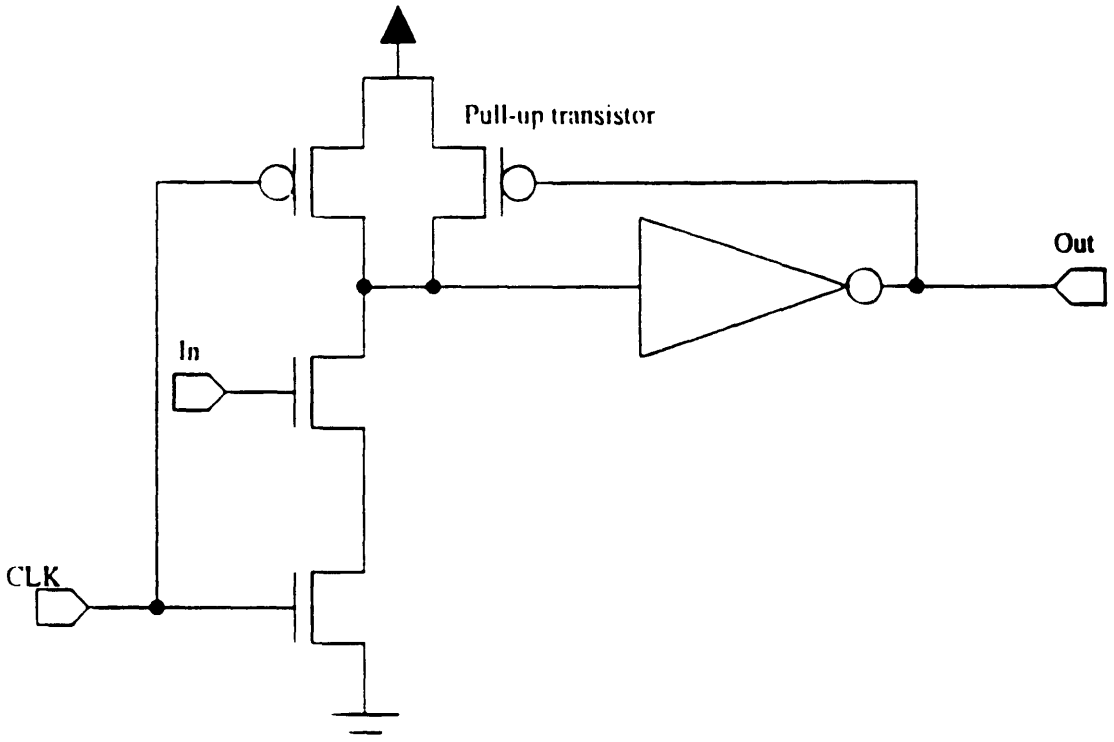

Fig. A.7 Schematic for an dynamic domino logic inverter.

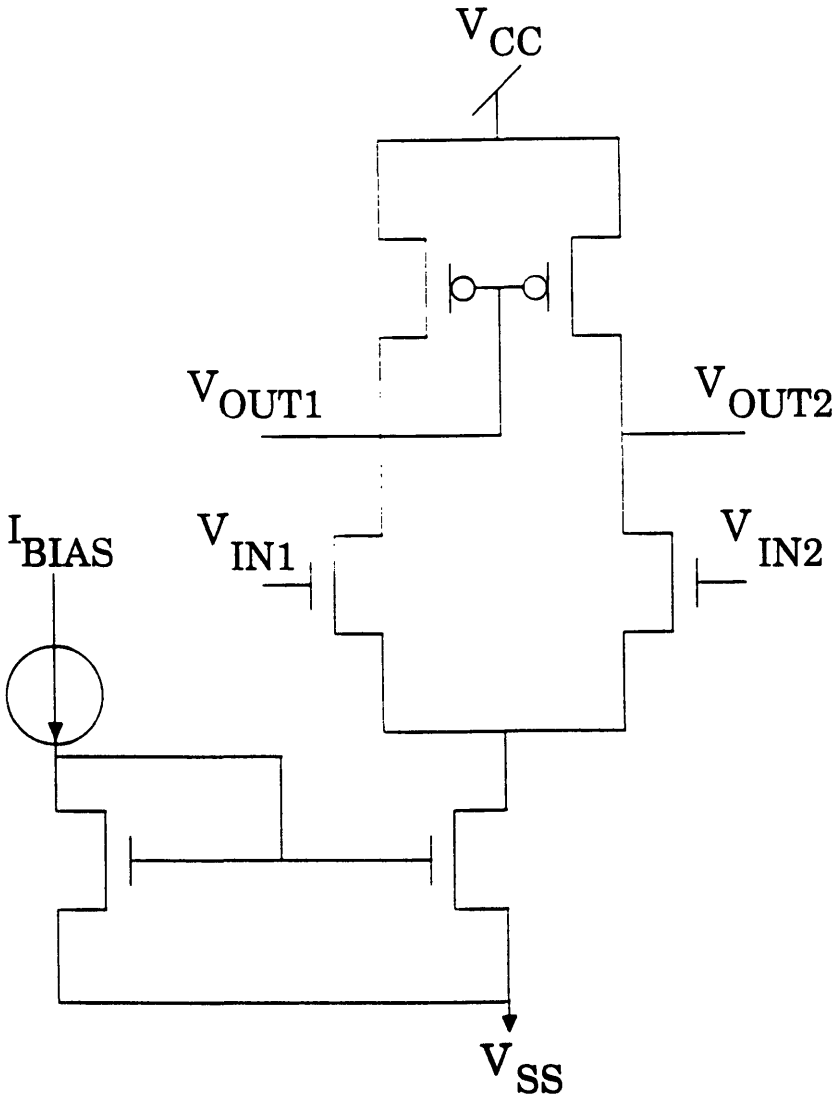

Fig. A.8 Schematic for the differential amplifier test structures.

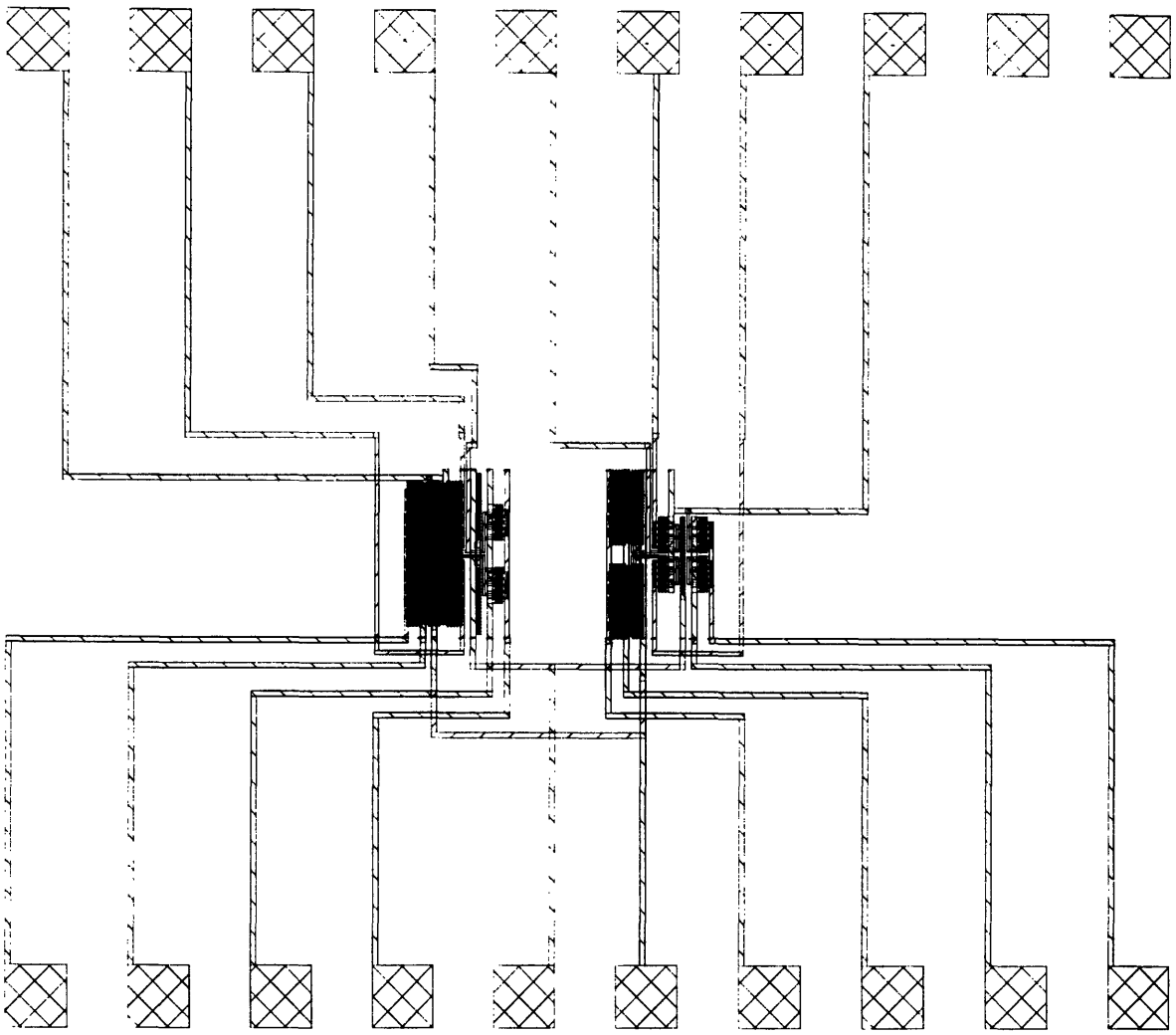

Fig. A.9 Layout plot for implementation of differential amplifiers.