A High-Speed General-Purpose Externally Compensated Operational Amplifier

by

Sandro Herrera

Submitted to the Department of Electrical Engineering and Computer Science
In Partial Fulfillment of the Requirements for the Degree of
Master of Engineering in Electrical Engineering

at the

Massachusetts Institute of Technology

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Abstract

Although most modern monolithic solid state operational amplifiers (op-amps) are internally compensated, externally compensated units provide an invaluable degree of freedom to analog designers. As a result, these op-amps offer true 'general purposeness,' since allowing the user to choose the amplifier's compensation can drastically improve performance in many applications. This thesis proposes a design of a high speed, general purpose externally compensated operational amplifier using a modern complementary bipolar process.

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Finally, I would like to thank my wife Wendy Matos, the lady I want to spend the rest of my life with.

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1. Introduction

An externally compensated operational amplifier is an op amp that allows the user to tailor its open-loop transfer characteristics by means of an external network. The objective of this thesis is the design of a high-speed, general-purpose, externally compensated operational amplifier using a modern complementary bipolar process.

1.1 Background

Since their appearance in 1964 with the introduction of Fairchild Semiconductor's μA702, operational amplifiers (op-amps) are still the most widely used linear integrated circuit [1]. They are found in thousands of applications which include signal amplification, filtering, analog computers, nonlinear function generators, buffers, etc. Their versatility allows them to be incorporated in independent cells, which can be put together to form a system.

The first integrated models that appeared on the IC market, Fairchild's μA702 and μA709, and National's LM101, employed external compensation. It was not until the introduction of the μA741 by Fairchild Semiconductor in 1968, that the compensation network was brought on chip. After its release, the sales of this kind of operational amplifier increased dramatically while the sales of the externally compensated models decreased [2].

After these pioneering designs, many integrated op-amps have showed up on the semiconductor market in order to fulfill the many applications in which they are needed. Among these designs we can find rail-to-rail amplifiers, low power, high precision, high

speed, high output current, high slew rate, low noise, etc. An interesting feature though, is that almost all include internal compensation. In the next section we will see the reasons for this choice.

1.2 Motivation

Although internally compensated operational amplifiers are easier to use and understand than externally compensated models, they are not more versatile. Fixed compensation makes the op amp have an optimum open-loop transfer function for a very small number of applications. This is one of the reasons for the large variety of internally compensated operational amplifiers in the market, where each one is tailored to fulfill a specific set of applications.

Even though the number of different integrated op-amps is constantly growing, it is frequently impossible to find one that is optimally compensated for the closed-loop configuration in which it will be used (amplifier, filter, etc.). This is not only due to the vast range of applications in which an op amp is found, but due to the fact that some are too specific to have an IC op amp manufactured for, i.e. the op amp would not be general purpose and thus not profitable. A couple of examples would be internally compensated op-amps that can follow an input ramp with no steady state error, or that can drive very big capacitors without traces of instability[1].

As a result, the only way to obtain the optimum open-loop transfer function characteristic for a specific application is to allow the user to compensate the operational

[1] An op amp that can drive a big capacitor or that can follow a ramp with no steady state error requires a specialized compensation scheme. As a result, the op amp will not be stable under all conditions.

amplifier. This fact is asserted by Professor James K. Roberge in his book *Operational Amplifiers: Theory and Practice.*

> If compensation can be intelligently selected as a function of the specific application, the ultimate performance possible from a given amplifier can be achieved in all applications. Furthermore, the compensation terminals make available additional internal circuit nodes, and at times it is possible to exploit this availability in ways that even the manufacturer has not considered. The creative designer working with linear integrated circuits soon learns to give up such degrees of freedom only grudgingly. [3]

Given the many reasons to prefer externally compensated operational amplifiers, internally compensated models greatly outsell them. The following are some reasons provided by op amp users:

> (a) The manufacturers' compensation is optimum in my circuit. (This is only true in about 1% of the applications).
>
> (b) It's cheaper to use an internally compensated operational amplifier since components and labor associated with compensation are eliminated...
>
> (c) Operational amplifiers can be destroyed from the compensation terminals. (Operational amplifiers can be destroyed from any terminal).
>
> (d) The compensating terminals are susceptible to noise pickup since they connect to low signal level nodes. (This reason is occasionally valid. For example, high-speed logic can interact with an adjacent operational amplifier through the compensating terminals, although inadequate power supply by-passing is a far more frequent cause of such coupling.)
>
> After sufficient exposure to this type of rationalization, it is difficult to escape the conclusion that the main reason for the popularity of internally compensated amplifiers is the inability of many users to either determine appropriate open-loop transfer functions for various applications or to implement once they have been determined. [3]

1.3 Externally Compensated Operational Amplifiers

There are two classes of externally compensated op-amps, single-stage and two-stage. Single-stage types have a single gain stage and therefore have one high-impedance node to which a passive network is connected to define their open-loop transfer function. In these units, the compensation network is connected from the high-impedance node to signal ground. Figure 1 shows a simplified diagram of a single-stage externally compensated op amp.

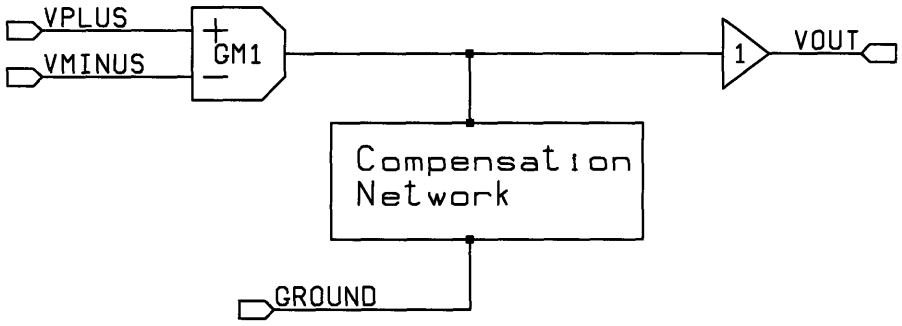

Figure 1. Simplified diagram of a single-stage externally compensated op-amp.

Two-stage externally compensated operational amplifiers are composed of two gain stages and thus they possess two high-impedance nodes. The compensation network is connected between these two nodes forming a minor feedback loop within the op amp. Figure 2 shows a simplified diagram of a two-stage externally compensated op amp with the compensation network around the second gain stage. In the case where a single capacitor is used as a compensation network, these op-amps are known as Miller multiplied or Miller compensated operational amplifiers. This name is a misleading since

the Miller effect is simply a special case of minor loop feedback. Figure 3 shows the block diagram of the compensated operational amplifier depicting the minor loop within the amp. This loop feeds back a current proportional to the admittance of the compensation network and the op amp's output voltage to the input of the second stage. Feedforward effects through the compensation network have not been included on the diagram; it will be argued later why this is the case. Since this op amp has a high gain in the forward path of the minor loop, the open-loop transfer characteristic is set by the compensation network over a wide frequency range.

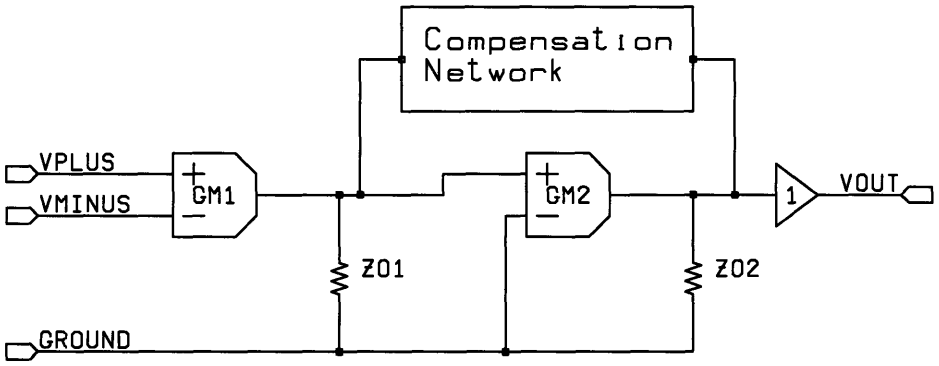

Figure 2. Simplified diagram of a two-stage externally compensated op-amp.

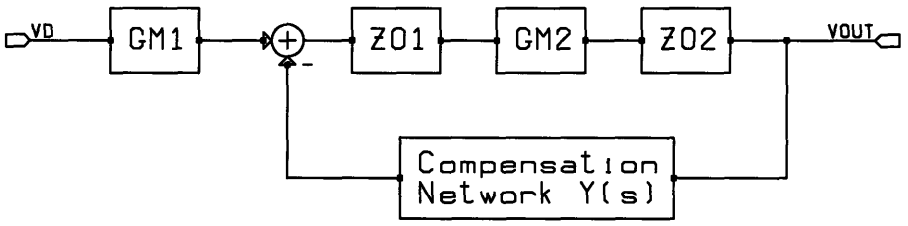

Figure 3. Block diagram of a two-stage externally compensated op-amp.

The presented operational amplifier belongs to the second class and it presents several advantages over single-stage and internally compensated units. In order to achieve good stability over a large range of closed-loop gains, internally compensated op-amps use a dominant pole compensation scheme and as a result suffer from constant gain-bandwidth product, which reduces the closed-loop bandwidth as the closed-loop gain increases. Also, these amps have trouble driving heavy capacitive loads since the loading capacitor forms a pole with the output impedance. This pole appears in the major loop of the op amp and can cause stability problems. Finally, the user of these units is stuck with the dynamics offered by a single pole roll-off transfer function, in the sense that it will only provide zero steady-state error to a step input but not to a ramp.

Single-stage externally compensated operational amplifiers are more flexible than internally compensated units because they do not suffer from constant gain-bandwidth product limitations. If the op amp is configured to provide certain gain, the compensation network can be chosen to optimize the bandwidth at that gain. Also, they allow the introduction of zeros in their major loop transfer function (using a series RC compensation network) such that the op amp can drive heavy capacitive loads. However, one problem with these amps though is that a roll-off slope steeper than -20dB per decade in the open-loop transfer function is not possible because the compensation network is connected to signal ground. Thus, compensation schemes like two-pole compensation are unachievable.

Two-stage externally compensated op-amps can implement almost any open-loop transfer function. Thus, they can be compensated to excel in performance under any conditions. This flexibility is due to the minor loop in their architecture where the open-

loop transfer function of the op amp will follow the inverse of the transfer function of the minor loop's feedback path (1/Y(s) in figure 3) as long as the minor loop's loop-gain is greater than one. The major disadvantage of these op-amps is that since they posses an inner loop, the user has to make sure that both major and minor loop are stable when the op amp is connected in a feedback configuration.

1.4 Problems at Large

Although externally compensated op-amps have plenty of advantages to offer, they have two inherent problems that limit their performance. The first one has to do with the availability of passive components used in the compensation network. For example, for a two-stage operational amplifier, such as shown in figure 2, with an input-stage transconductance (G_{M1}) of one millimho, to achieve a unity-gain (A_{CL}=1) bandwidth of 150MHz ($2\pi\omega_c$), equation one states that the optimum compensation capacitor would be 1pF (assuming capacitive dominant pole compensation is used).

$$C_c = \frac{Gm_1}{A_{CL} 2\pi \cdot \omega_c} \tag{1.4.1}$$

If a closed-loop gain of ten (A_{CL}=10) is desired, the optimum compensation would be achieved using a 0.1 picofarad capacitor (equation one determines C_c such that the closed-loop bandwidth of the op amp is kept constant, thus the gain-bandwidth product is increased as A_{CL} increases). As the desired closed-loop gain-bandwidth product increases, the size of the passive components that form the compensation

network shrink drastically. This is a big problem, since in today's market, good small-sized passive components may not only be hard to find, but can be very expensive (even more than the op amp itself).

The second problem has to do with the parasitics encountered when taking critical parts of an integrated circuit off-chip, in our case the compensation network. These parasitics include the capacitance of the bond pads and the inductance of the bond wires (these connect the die to the package leads), the self and mutual inductance of the leads, the capacitance between the leads, the transmission line effects of the PCB board traces and capacitance of the soldering pads (figure 4). All of these appear in the compensation path and as a result affect the behavior of the op amp. A typical value for the sum of all these parasitics is about 0.5pF of capacitance and about 5nH of inductance. From our discussion above we can see that their size is quite comparable to the components used in the external compensation network.

These two problems are addressed by the amplifier presented in this thesis.

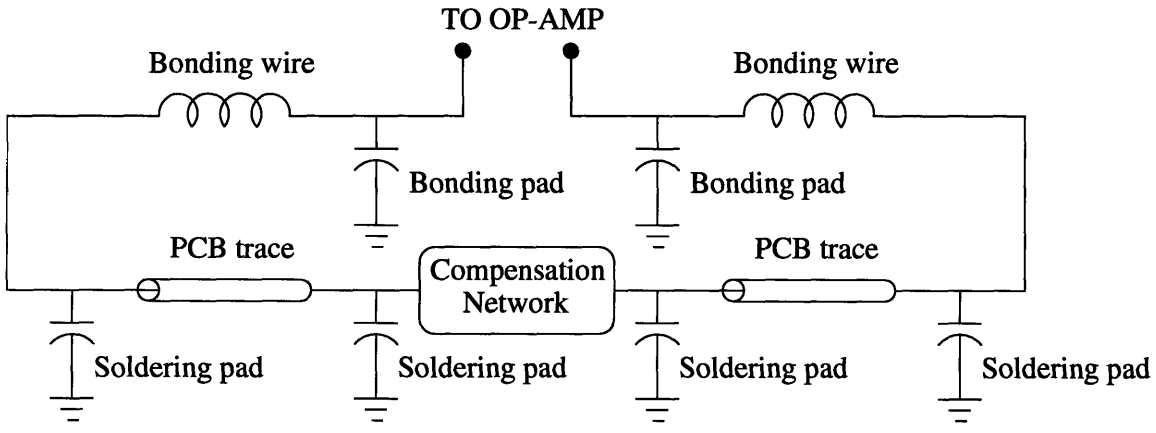

Figure 4. Parasitics in series with the op-amp's compensation network.

1.5 Prior Art and Targeted Specifications

Since the introduction of the μA741, not much work has been done in the area of externally compensated operational amplifiers. Some single-stage models have appeared in the market but due their limited flexibility they are mainly used in applications that need constant gain-bandwidth products. Thus, single stage units are commonly known as 'de-comp' operational amplifiers, since they can be de-compensated to keep the overall bandwidth constant as the closed-loop gain is increased.

	PROPOSED	LM101A	AD8021	AD8041
DC SPECIFICATIONS				
• Input offset voltage	< 1 mV	0.7 mV	0.4 mV	2 mV
• Input offset current	< 0.1 μA	1.5 nA	0.1 μA	0.2 μA
• Input bias current	< 3 μA	30 nA	7.5 μA	1.5 μA
• Open-loop gain	> 50,000	160,000	20,000	50,000
DYNAMIC SPECIFICATIONS				
• Maximum closed-loop Bandwidth	100 MHz	1 MHz	490 MHz	160 MHz
• Slew rate, G = +1	> 100 V/μs	0.7 V/μs	120 V/μs	160 V/μs
INPUT CHARACTERISTICS				
• Input resistance	> 1 MΩ	4 MΩ	10 MΩ	160 kΩ
• Input common mode range	At least 1 V from the positive rail and the negative rail.	Up to positive rail, 2 V from negative rail	0.4 V from positive rail and 0.9 V from negative rail	1 V from the positive rail and 0.2 beyond negative rail.
OUTPUT CHARACTERISTICS				
• Short circuit current	> 80 mA	n/a	75 mA	90 mA
• Output range	At least 1.25 V from supply rails.	2 V from positive and negative supplies	1.5 V from positive and negative supplies	0.1 V from positive and negative supplies
COMMON MODE REJECTION RATIO	> 70 dB	96 dB	98 dB	80 dB
POWER SUPPLY REJECTION RATIO	> 70 dB	96 dB	95 dB	80 dB
POWER SUPPLY				
• Supply current	< 10 mA	1.2 mA	7.7 mA	6.5 mA

Table 1. Comparison table between proposed operational amplifier and other commercial units.

A commercial example of this kind of op amp is the AD8021 high speed, low noise operational amplifier. This amp boasts a typical small signal bandwidth of 490MHz for a gain of +1 with a single 10pF compensation capacitor. [4]

Regarding two-stage externally compensated operational amplifiers, there are currently no modern designs available. Therefore, Robert Widlar's LM101 and LM101A are the only commercial representatives of this kind of op-amps. These amplifiers were designed in the late 1960s and thus their dynamic performance is quite unacceptable by today's standards. The LM101A has a typical maximum bandwidth of approximately 1MHz in optimally compensated applications [5], beyond that the phase lag is too large for proper use of the amplifier.

Table 1 shows a comparison of the specifications of the mentioned amplifiers along with the proposed specifications for the presented op-amp. Also, the specifications of the AD8041 have been included for reference even though it is an internally compensated unit. The proposed specifications are fairly typical for a general purpose amplifier and are adequate for most applications.

Given the external compensation feature of the proposed amplifier, it should be a unique part in class with no rivals in the market.

1.6 Process Discussion

The operational amplifier discussed in this thesis was designed using Analog Devices proprietary process XFCB 1.5. This is a modern high voltage complementary bipolar process with ideal attributes for a high speed amplifier design.

XFCB 1.5 is a silicon on insulator (SOI) process in which the active devices are electrically and thermally isolated via a layer of silicon dioxide and side wall trenches. In addition to individual devices, complete circuit sections may be trenched to provide further isolation.

The process includes very fast vertical NPN and PNP bipolar transistors with highly doped polysilicon emitters and very small minimum geometries. As mentioned above, transistors are dielectrically isolated from other devices via trenches and a bonded SOI layer. This isolation results in a very small collector to substrate capacitance, a major bandwidth limiter in standard junction isolated processes. Also, device junction capacitances are quite small, which coupled with the small collector to substrate capacitance, leads to excellent high frequency characteristics.

The NPN transistor peak f_T is about 8 GHz while the PNP transistor peak f_T is about 5 GHz. For the NPN, the nominal β is 100 and the nominal Early voltage is 75V. For the PNP, the nominal is β is 65 and the nominal Early Voltage is 20V. The latter is a somewhat low, which suggests that cascoding the PNP's where possible might be a good idea.

Complementing the bipolar transistors, the XFCB 1.5 process also includes trimmable and non-trimmable thin-filmed resistors, diffused resistors, shottky diodes, Metal-Oxide-Metal (MOM) capacitors and a buried Zener diode. Also, two metal layers are available for interconnects. The provided MOM capacitors and thin filmed resistors posses quite good matching characteristics with very small parasitic capacitances.

Overall, the process is ideally suited for high-speed design and represents one of the best silicon bipolar processes currently available in the market.

2. The Proposed Operational Amplifier

As discussed in chapter 1, the presented operational amplifier belongs to the two-stage externally compensated class. The amplifier possesses two gain stages, each composed of a transconductor cell (G_M) and an output impedance (Z_O). G_{M1} denotes to the transconductance of the first stage and G_{M2} to the transconductance of the second stage. Accordingly, Z_{O1} denotes the overall impedance at the output node of the first stage and Z_{O2} the overall impedance at the output node of the second stage. The amplifier also includes a voltage buffer between the two gain stages and between the second stage and the overall output. The first one is included to prevent inter-stage loading effects while the second reduces the open-loop output resistance of the amplifier and enhances its output current handling. Finally, an interface circuit has been included between the second compensation terminal and the output of the first stage. The interface is modeled as an attenuator with finite bandwidth. The detailed block diagram model of the amplifier is shown in figure 5.

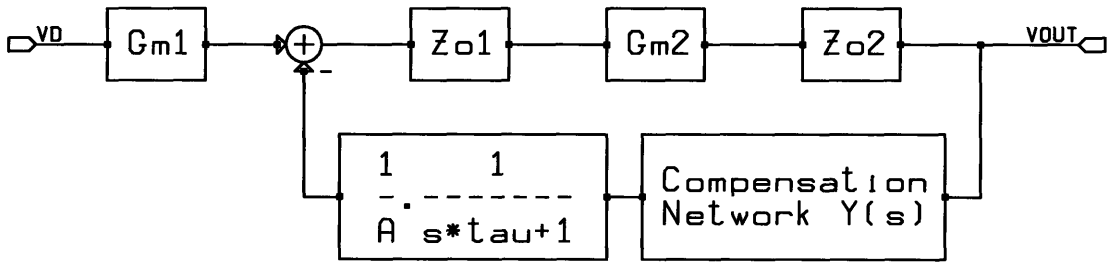

Figure 5. Block diagram for the proposed operational amplifier.

The structure shown in the model for the proposed of op amp is quite standard with the exception of the interface circuit block. The main purpose of this interface is to

reduce the effects of parasitics in the compensation network and to enable the user to use reasonably sized components. The two main problems of externally compensated amplifiers are addressed by using an 'enlarged' external compensation network (bigger admittance) and making it look 'small' to the operational amplifier by attenuating the current signal fed back by the compensation network. This is achieved by means of the interface block as shown in figure 5.

The inclusion of the interface moves the limits in performance of the op amp from the availability of external network components and surrounding parasitics to the achievable performance of the interface. The interface circuit is included within the minor loop of the amplifier and any singularities it introduces (poles and zeros) will affect the behavior of this loop. As the model shows, the interface has a finite bandwidth which introduces a pole within the loop. The circuit also has finite input impedance which will create a pole with any capacitance attached to the interface input. These two poles severely degrade the stability of the minor loop and can drive it to instability. Therefore, the figures of merit of the interface will dictate the overall performance of the amplifier.

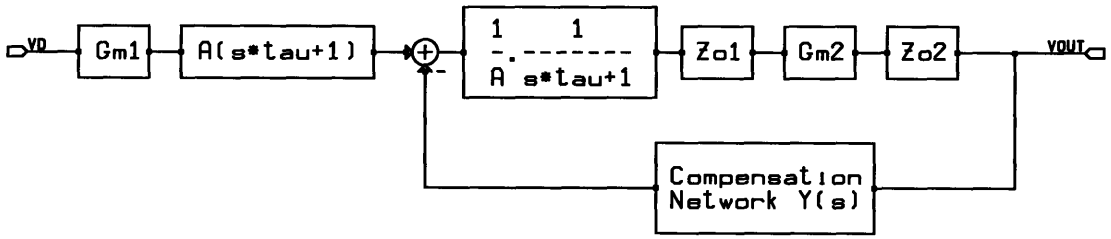

Figure 6. Equivalent block diagram for the proposed operational amplifier.

Although the introduced interface solves the problems of external parasitics and component availability, it is important to keep in mind how it affects the op-amp user. Via simple block diagram manipulations, the diagram in figure 6 is obtained from the one in figure 5. Even though the model in figure 6 is not physically accurate, both diagrams are mathematically equivalent leading to an important result. As long as the singularities in the interface are sufficiently beyond the amplifiers cross-over frequency, to the user the interface just amplifies the transconductance of the first stage. Therefore, he can use all the compensation techniques described in chapter 3 with the assumption that the effective input stage transconductance (G_{Meff}) is AG_{M1}, where A is the interface's attenuation factor.

The presented model neglects any feed-forward effects (from the output of the input stage to the output of the second stage) via the compensation network. This is due to the fact that the interface circuit is unilateral and thus it blocks any signals from propagating in the feed forward direction. This avoids unwanted effects like the right half plane zero in purely capacitive Miller compensation.

Although the models in figures 5 and 6 describe the presented amplifier in detail, they have a few shortcomings. First, it does not show large signal currents. Since the current signal injected into the output of the first stage (I_{FB}) is attenuated by the interface to allow the admittance of the compensation network to be enlarged (bigger compensation capacitor in the case of purely capacitive compensation), the current that has to be provided by the second stage is vastly increased. For example, a 10 pF compensation capacitor with an attenuation of ten in the interface creates an effective capacitance of 1 pF. If the input stage outputs 100 uA of current into the 'effective

compensation capacitor' during a slew condition, the op amp's output will rise at a rate of 100V/us (SR=I/C) as long as the second stage provides 1 mA of current, ten times more current than the input stage. This problem arises from the fact that the admittance of the compensation network is reduced only on one side, i.e. to the output of the input stage but not to the output of the second stage. As shown later in this chapter, to overcome this problem, a current on demand second stage is used.

Also, the model does not show how the forward path of the op amp is affected by the compensation network. In the input stage, this shortcoming can be neglected since the output capacitance of the interface is quite low (less than 0.1 pF) and output impedance of the interface is quite high. On the other hand, since the compensation network is connected directly from the output of the second stage to the input of the interface (a small signal ground), the second stage is considerably loaded. This loading is particular to the compensation network in use and this effect has to be taken into consideration when compensating the amplifier.

2.1 Simplified Circuit

As mentioned in the previous section, the amplifier is divided into five sections, the input trans-conductors, the inter-stage buffers, the second stage trans-conductors, the output buffer and the interface circuit. Figure 7 shows the top-level diagram of the amplifier.

The chosen architecture consists of two differential input trans-conductors that form two in-phase high impedance nodes, 'HIZ1P' and 'HIZ1N'. These nodes drive the second stage trans-conductors via the inter-stage buffers. The output currents of the

second stage trans-conductors are added at the second stage high impedance node, 'CC1', which in turn is buffered from the output node by the output buffer. The input of the interface circuit is connected to external compensation terminal 'CC2', and its outputs are connected to high impedance nodes 'HIZ1P' and 'HIZ1N', i.e. the output nodes of the input stage.

This parallel path architecture was chosen since it provides an easy way to implement the current on demand function required by the amplifier's second stage. As it will be described in section 2.3, the second stage uses a class-AB feedback architecture that needs two in-phase voltage inputs.

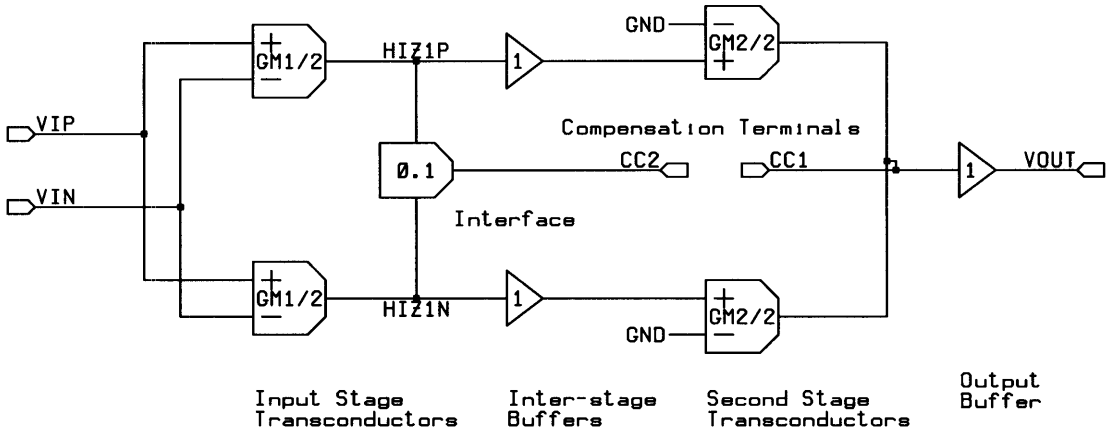

Figure 7. Top-level diagram of the amplifier.

2.2 Input Stage

As it names suggests, the 'input stage' in an operational amplifier refers to the input differential gain stage. Its functions are summarized below:

1. Provides high gain to input differential signals and ideally no gain to common mode signals. The extent to which the input stage achieves this function is

measured by the op-amp's common rejection ratio or CMRR (refer to chapter 4 for details).

2. Allows a wide range of input common-mode signals without degradation of the differential gain and without increasing the common mode-gain.
3. In most op-amps, it converts the input differential signal into a single ended signal. In the presented op-amp, this function is extended such that the input stage generates two in-phase single ended signals.

The performance and functionality requirements of the input stage set the architectural, device sizing, power and design complexity trade-offs. The requirements set for the input stage in the presented design are:

1. Generate two in-phase high impedance output nodes, 'HIZ1P' and 'HIZ1N'. The former will be at an output level of two V_{BE}'s below the positive supply rail while the latter at two V_{BE}'s above the negative supply rail.
2. The input common mode should extend up to the negative rail.

The first requirement is dictated by the architecture of the second stage which is described in the next section. The second requirement allows the amplifier to operate effectively in a single-supply system since it will be able to accept input signals whose common-mode extend to ground.

The first requirement was met by using two trans-conductors in parallel as shown in figure 7. This way, each transconductor can be optimized separately for the required output level. To satisfy the second requirement both trans-conductors use the resistively loaded PNP folded-cascode architecture.

The basic resistively loaded PNP folded-cascode trans-conductor cell is shown in figure 8. PNP transistors Q1 and Q2 with their respective emitter resistors RE1 and RE2

form a degenerated differential pair that drives NPN cascode transistors Q3 and Q4. The latter convey the differential pair's output current signal to the cell's output node. Resistors RL1 and RL2 set the bias current for the folded cascode structure and load the input differential pair. Transistor Q5 and resistor R5 form the tail current source of the differential pair. The current mirror loading the folded cascode transistors provides differential to single ended conversion and high output impedance. Also, it forces current balance between transistors Q3 and Q4. In figure 8, the current mirror is shown as an ideal mirror since its architecture depends on the desired output signal level.

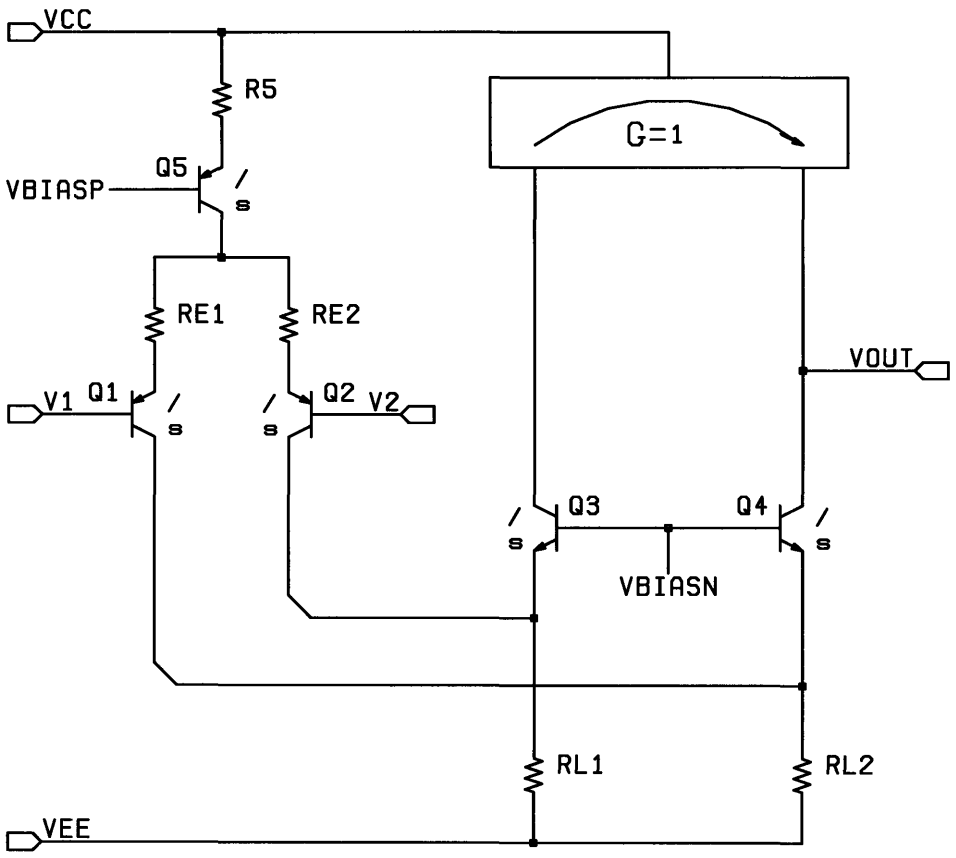

Figure 8. Resistively loaded, PNP input folded-cascode trans-conductance cell

When analyzing differential stages, it is useful to decompose the input voltage signals V1 and V2 into their differential and common-mode components. These are defined as follows:

$$V_D = \frac{V1 - V2}{2} \tag{2.2.1}$$

$$V_{CM} = \frac{V1 + V2}{2} \tag{2.2.2}$$

The differential gain of the cell is given by

$$A_{VD1} = \frac{V_{OUT}}{V_D} = G_{M1}\left(\frac{\frac{1}{gm_4}}{RL_2 + \frac{1}{gm_4}}\right)\left(R_{OM} \parallel r_{o4}(1 + g_{m4} \cdot RL2)\right) \tag{2.2.3}$$

where g_{m4} and r_{o4} are the transconductance and output resistance of transistor Q4, R_{OM} is the output resistance of the current mirror and G_{M1} is the transconductance of the input differential pair. The latter is given by

$$G_{M1} = \frac{1}{\frac{1}{g_{m1}} + RE1} = \frac{1}{\frac{kT}{qI_{C1}} + RE1} \tag{2.2.4}$$

where I_{C1} is the collector current of transistor Q1, q is the charge of an electron, k is Boltzmann's constant and T is the device temperature in Kelvin.

The purpose of degeneration resistors RE1 and RE2 is to allow the choice of G_{M1} be independent of Q1's collector current, I_{C1}. This way I_{C1} can be chosen to optimize performance metrics including slew rate, input referred noise, bandwidth and input bias current independently of the value of G_{M1}. Also, by means of local voltage feedback, RE1 and RE2 improve the linearity of the stage.

The second factor in equation (2.2.3) is the loading effect of resistors RL1 and RL2 on the input differential pair. These resistors partially shunt the differential pair's output current signal to the negative rail degrading the stage's total trans-conductance. In practice, these resistors are much greater than $1/g_{m4}$ and therefore the loading imposed on the input differential pair is negligible.

The input common mode range of the stage is defined as the range of V_{CM} for which the stage does not show any significant degradation in differential gain and common mode gain. The same definition applies for the output voltage range but with the consideration of V_{OUT} signals instead. Typically, common mode voltage ranges are limited by transistors entering the saturation regime and thus degrading performance.

For the stage shown in figure 8, the input common mode range is bounded on the low side by

$$V_{CM\,\min} = V_{CEsat} + V_{RL} - V_{BE} \tag{2.2.5}$$

where V_{RL} is the voltage across resistors RL1 and RL2. Beyond this minimum V_{CM}, transistors Q1 and Q2 saturate. For XFCB 1.5, typical V_{CEsat}'s range from about 400mV at low temperatures to about 200mV at high temperatures, while typical V_{BE}'s are about 800mV. If V_{RL} is set to approximately 200mV, the worst case minimum input common mode voltage is about 0.2V below the negative rail. This satisfies the second requirement of the input stage.

On the high side, the input common mode range is bounded by

$$V_{CM\,\max} = V_{CC} - V_{R5} - V_{CEsat} - V_{RE} - V_{BE} \tag{2.2.6}$$

where V_{R5} and V_{RE} are the voltages across resistors R5 and RE1. Beyond this maximum V_{CM}, current source transistor Q5 saturates. Using the process' typical values and

150mV for V_{R5} and V_{RE}, the maximum input common mode voltage is 1.5V from the positive supply. This value is actually conservative since the circuit can tolerate some saturation in the tail current source transistor.

The output voltage range is bounded by

$$V_{OUT\max} = V_{CC} - V_{OM} \tag{2.2.7}$$

$$V_{OUT\min} = V_{RL} + V_{CEsat} \tag{2.2.8}$$

where is V_{OM} is the minimum voltage required across the current mirror output and its common terminal. If V_{OM} is designed to be small, the stage will have a very wide output voltage range. Due to the architecture of the second stage, node 'HIZ1P', the output of the first input trans-conductor, will be at a quiescent voltage of two V_{BE}'s from the positive rail while 'HIZ1N', the output of the second input trans-conductor, will be at two V_{BE}'s from the negative rail. Equations 2.2.7 and 2.2.8 show that these quiescent output voltages are well within the capabilities of the folded cascode structure.

In order to keep the amplifier's input offset voltage low, it is important to keep the differential structures of the input stage electrically balanced. Simply put, this means that the quiescent operating voltages and currents for each transistor on both sides of the stage's differential half circuits should be matched. If the balance is broken, any asymmetries will have to be compensated by the input differential pair in the form of offset voltage. Also, asymmetries will cause input bias current offsets.

In the folded cascode trans-conductor, electrical balance is achieved by the appropriate choice of the current mirror. By nature of the cell, the V_{CE} of transistors Q1 and Q2 will be equal, but the matching of the Q3 and Q4's V_{CE} depends on the quiescent output voltage of the cell and the quiescent input voltage of the mirror.

For the first transconductor, the emitter follower enhanced (EFE) current mirror was selected (figure 9). In this circuit, the quiescent input voltage of the mirror sits at approximately two V_{BE}'s below the positive rail which matches its quiescent output voltage and thus keeps the V_{CE} of Q3 and Q4 roughly equal. This way, the mirror achieves voltage balance. Although not shown in the diagram, the inter-stage buffer injects a PNP base current into the mirror's output node, 'HIZ1P' ('Iout' figure 9). This current is balanced by Q3's base current which is injected into the input of the mirror.

Degeneration resistors RE1 and RE2 serve the dual role of boosting the output impedance of the circuit while providing thermal stability between transistors Q1 and Q2. Capacitor C1 provides compensation to the mirror preventing any high frequency oscillations. Transistor QCL acts as a voltage clamp for output node 'IOUT', such that the minimum possible V_{CE} for Q2 is one V_{BE} and thus never enters the saturation regime. Clamp transistors like QCL are very important for overdrive recovery.

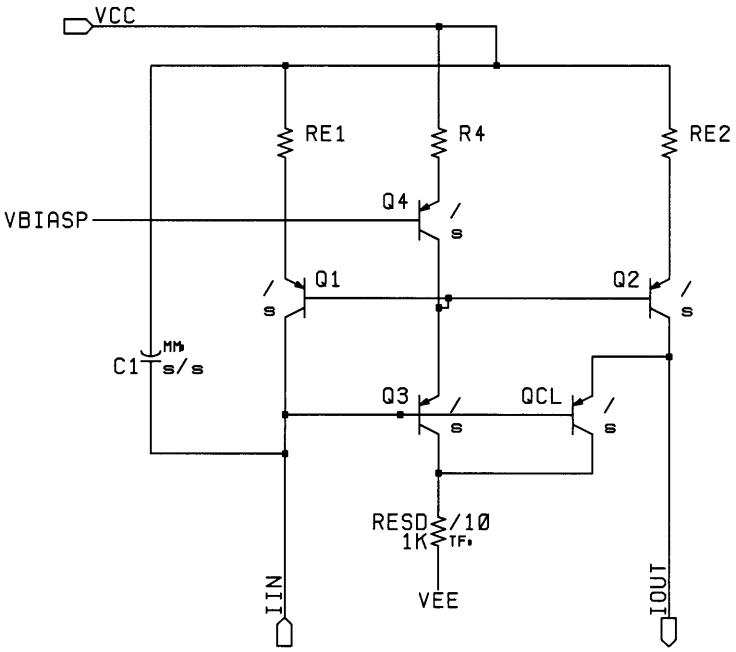

Figure 9. Emitter Follower Enhanced (EFE) current mirror.

The second transconductor uses a current mirror with common-mode feedback. By means of a reference and a simple feedback loop, these mirrors allow a wide selection of input quiescent voltages. Figure 10 shows the implemented mirror for the second transconductor.

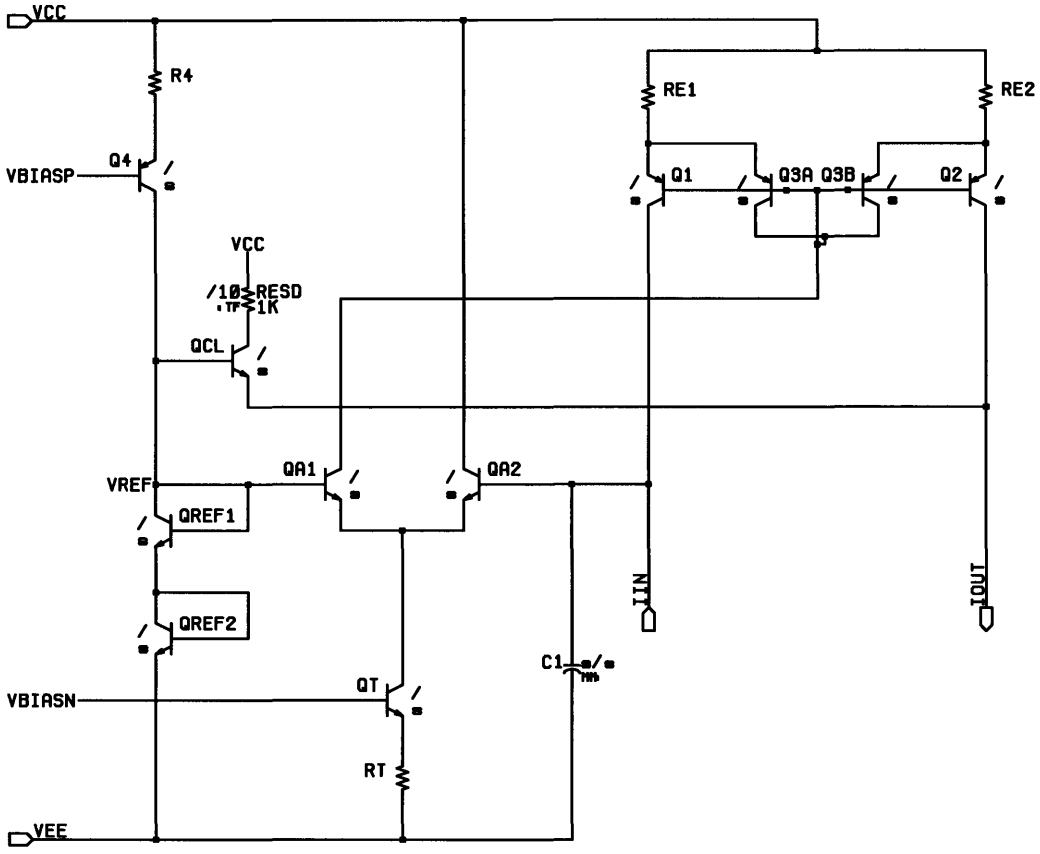

Figure 10. Current mirror with common mode feedback.

In this circuit, the quiescent input voltage of the mirror is set by reference node 'VREF' and by the differential amplifier QA1, QA2, Q1, Q3A, Q3B and QT. The feedback provided by the differential amplifier sets QA2's base voltage, and therefore the mirror's input voltage, to match 'VREF' by driving Q1's base until its collector current matches the mirror's input current (current at node 'IIN'). By construction, the amplifier

also drives Q2's base such that its collector current also matches the mirror's input current, thus achieving the current mirror function. By setting 'VREF' and thus the mirror's input voltage to two V_{BE}'s above the negative rail, the mirror achieves voltage balance since the output voltage is also at set at two V_{BE}'s above the negative rail. The input bias current drawn by the common mode feedback amplifier, i.e. QA2's base current, is balanced by the current drawn by the inter-stage buffer (not shown). In order to assure stability, the common mode feedback loop is compensated with capacitor C1. Finally, QCL is a clamp transistor that helps for overdrive recovery since it prevents the saturation of Q4 in figure 8.

2.3 The Second Stage

In a two-stage operational amplifier, the second stage serves the purpose of gaining up the input stage's output signal. Also, it allows the use of minor loop feedback to tailor the amplifier's open-loop characteristics i.e. it allows the use of minor loop compensation.

The main requirements for the second stage are high input impedance, high gain and wide bandwidth. The first requisite is to avoid loading down the input stage and thus avert gain degradation. The second and third are to ensure that the dynamics set by the compensation network hold over a wide frequency range. In addition, due to the increased conductance of the compensation network, the second stage of the presented amplifier is also required to output large dynamic currents.

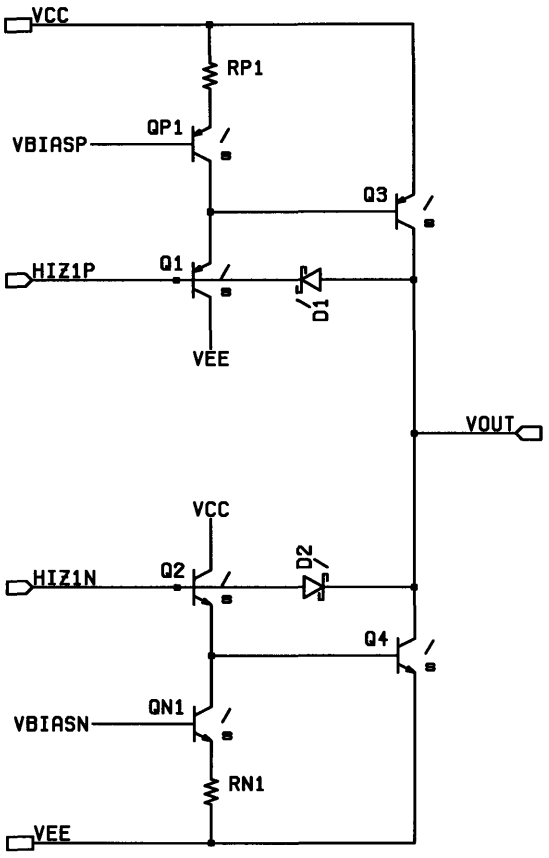

Figure 11. Class AB second stage.

As shown in the figure 7, the second stage consists of two parts, the inter-stage buffers and the second stage transconductors. The buffers fulfill the high input impedance requirement while the transconductors provide high voltage gain. Figure 11 shows the schematic of the implemented second stage.

The chosen second stage is a Class AB or Push-Pull gain stage formed by the complementary cascade of emitter followers Q1 and Q2, and common emitters Q3 and Q4. The main advantage of this architecture is that when inputs 'HIZ1P' and 'HIZ1N' are driven with two in-phase voltages, the structure can sink and source very large currents via the NPN (Q4) and the PNP (Q3) output devices, thus meeting the fourth requirement for the second stage. It is very important to re-iterate that the input signals

must be two in-phase voltages, otherwise the output currents will partially cancel each other. If the stage is driven differentially, the net output current will be zero, and only the stage's standing current would be affected.

Besides the large dynamic output current capability, another advantage of the Class AB gain stage is their rail-to-rail output range which reaches up to a V_{CEsat} from each supply. Also, the power efficiency is quite good since their maximum output current is independent of their quiescent bias current, and thus the latter can be set to be quite small. The maximum output current is limited by the transistors betas and the input stage's tail current source.

$$Iout_{\max} = \beta^2 I_{TAIL} \tag{2.3.1}$$

The inter-stage buffers are implemented with emitter follower transistors Q1 and Q2. These provide adequate buffering and set the second stage's input resistances to

$$R_{INP} \approx r_{\pi 1} + (1+\beta) r_{\pi 3} \tag{2.3.2}$$

$$R_{INN} \approx r_{\pi 2} + (1+\beta) r_{\pi 4}. \tag{2.3.3}$$

Also, they level shift the quiescent voltages at input nodes 'HIZ1P' and 'HIZ1N' such that they respectively sit at two V_{BE}'s from the positive and negative supply rails. As described in the previous section, this condition partially set the choice for the folded cascode mirrors in order to obtain low input offset voltage.

Another advantage of the Class AB stage is its inherent G_M doubling property. Ignoring the voltage attenuation due to the inter-stage buffers, the second stage's transconductance is given by

$$G_{M2} = G_{MP} + G_{MN} = 2 g_{m3} = 2 \frac{q I_{BIAS}}{kT} \tag{2.3.4}$$

assuming equal I_{BIAS}. Thus, for a given bias current I_{BIAS} and degeneration resistor RE, the effective transconductance of the stage is twice the transconductance of a degenerated common emitter stage. The intuition behind this result lies in the parallel drive applied to the two complementary common emitters in the Class AB. Since their output current signals are added at the output node, they both contribute towards the overall transconductance of the stage. Notice though, this is only true for in-phase input signals.

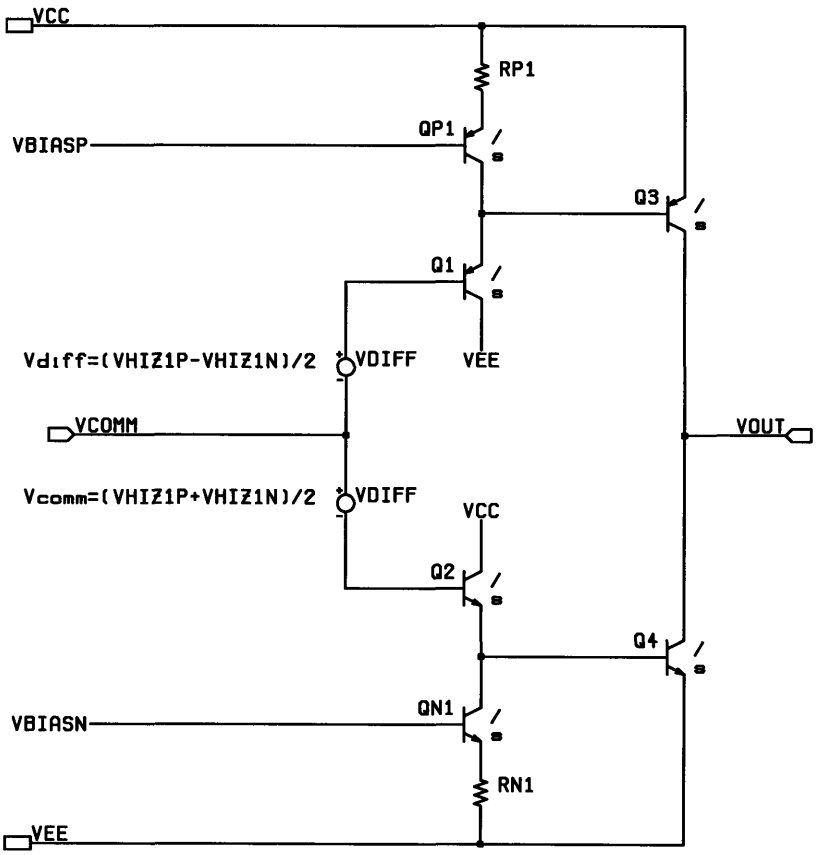

Figure 12. Class AB second stage with input voltage decomposition.

Even though, Class AB gain stages possess many advantages, one major disadvantage is their complexity. First, they normally require two in-phase input voltages which typically sit at different quiescent voltages. As seen in the previous section, this

doubled the complexity of the input stage. Second, while the stage's output current is controlled by the common-mode of the input voltages (i.e. by their in-phase component), the output transistors bias current is controlled by their differential-mode (see figure 12). Since the input stage can only generate in-phase output signals, it can only change the common mode of V_{HIZ1P} and V_{HIZ1N} and thus, the op-amp's major feedback loop is unable to precisely set the second stage's bias current. To solve this problem, a separate internal control circuit is required. This auxiliary circuit is known as the Class AB bias control loop.

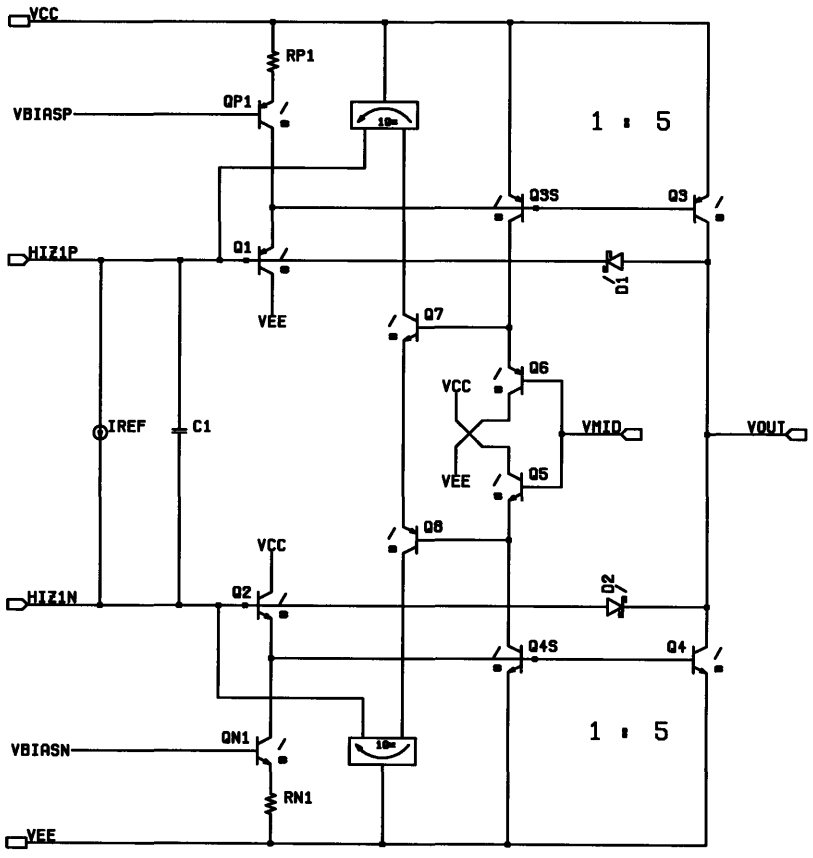

Figure 13. Class AB gain stage with Class AB biasing.

Figure 13 shows the complete class AB second stage. The class AB bias circuit is composed by floating reference current source I_{REF}, sample transistors Q3s and Q4s, and the geometric mean circuit, Q5-Q8. By means of negative feedback, the circuit establishes the bias current of the output transistors to be five times the reference current, I_{REF}. The circuit's operation is as follows, the reference current is injected into the inputs of the second stage which gains it up by a factor of β^2. The amplified currents (the common emitter collector currents) are then sampled and attenuated by the emitter area ratio of the sample and common emitter transistors, in this case by a factor of five. Finally, the attenuated sampled currents are driven into a circuit that takes their geometric mean and feeds the result back into the input of the second stage. Capacitor C1 compensates the feedback loop to prevent high frequency oscillations. Figure 14 shows the block diagram of the Class AB bias circuit.

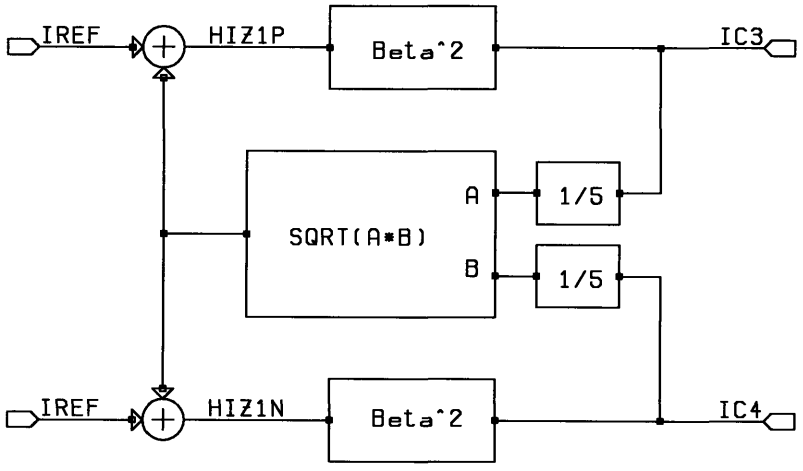

Figure 14. Class AB feedback block diagram.

For $\beta^2 >> 5$, the closed-loop transfer function is

$$I_{C3}I_{C4} = (5I_{REF})^2. \tag{2.3.5}$$

Therefore, when I_{C3} and I_{C4} are equal, i.e. when the output current is zero, the output devices bias current is $5I_{REF}$. Due to the form of (2.3.5), the presented class AB bias strategy is known as 'Constant Product Class AB Control'. Defining the output current as $I_{OUT} = I_{C3} - I_{C4}$, then the collector currents of Q3 and Q4 are given by

$$I_{C3} = \frac{I_{OUT}}{2} + \frac{\sqrt{I_{OUT}^2 + 4K}}{2} \tag{2.3.4}$$

$$I_{C4} = \frac{I_{OUT}}{2} - \frac{\sqrt{I_{OUT}^2 + 4K}}{2} \tag{2.3.5}$$

where K is

$$K = (5I_{REF})^2. \tag{2.3.6}$$

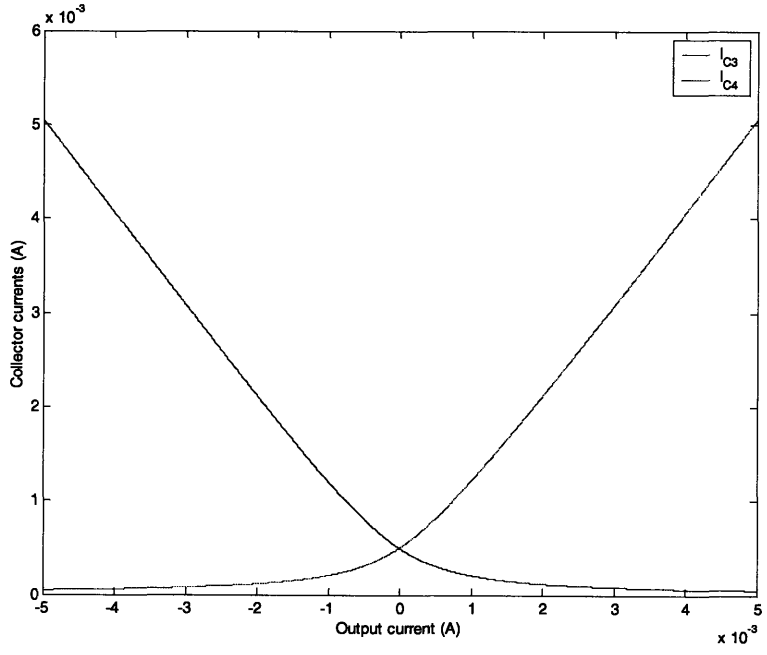

Figure 15. Second stage output transistors collector current.

Figure 15 shows the output devices collector currents versus the output current. Even when the stage is sinking or sourcing hard, the output transistors never turn off (their collector current never reaches zero). This is a property of constant product Class AB biasing which is highly valued since transistors switching-off usually causes unwanted delays and other undesirable effects.

The final components of the second stage are clamp shottky diodes D1 and D2. These prevent the common emitter transistors from saturating when the amplifier is overdriven. Shottky diodes are employed instead of PN diodes since they have no charge storage and thus recover much faster.

2.4 Output Stage

The output stage of the presented op-amp is voltage buffer that provides isolation between the output node (and thus the amp's load) and the second high impedance node 'CC1'. Also, the stage lowers the amplifier's output impedance and increases the maximum output current into a load.

Since the presented op-amp belongs to the general purpose family, the challenge set for the stage's design was to make it able to drive 50 Ω loads. This type of load is fairly typical in high speed applications which frequently use 50 Ω terminated coaxial cables. In terms of output current, for an output swing of +/-4 V, the requirement translates to I_{OUT} = +/-80 mA.

A fairly popular stage used in most high output current op-amps is shown in figure 16. This stage is commonly referred as the 'Complementary diamond voltage

buffer' or 'Diamond buffer' for short due to the shape formed by the emitters of the four core transistors, Q1-Q4. The main advantage of this cell is its ability to sink and source very high output current levels independently of the output transistors' quiescent current. In other words, the bias current of the diamond buffer stage can be set to a relatively small fraction of the peak output current. As a result, the stage can be designed to be very power efficient. Another nice feature of the diamond buffer is the approximate equality between the input voltage 'VIN' and the output voltage 'VOUT'.

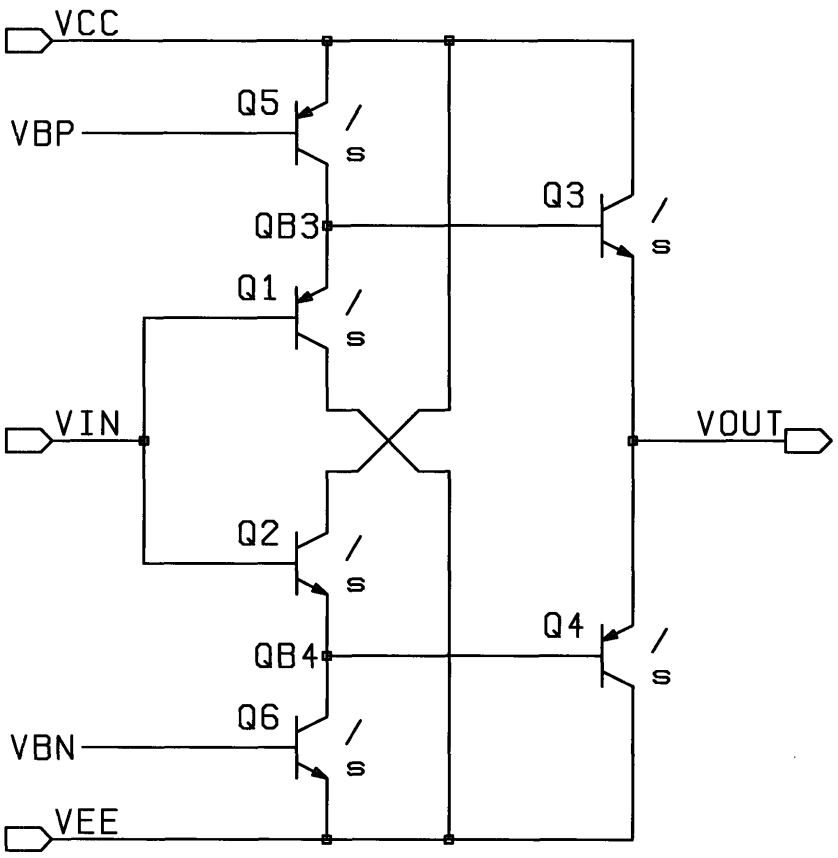

Figure 16. Complementary diamond voltage buffer output stage.

The input and output voltage range for the diamond buffer is bounded by

$$V_{IN\_MAX} = V_{OUT\_MAX} = V_{CC} - V_{CESAT} - V_{BE} \tag{2.4.1}$$

$$V_{IN\_MIN} = V_{OUT\_MIN} = V_{EE} + V_{CESAT} + V_{BE} \tag{2.4.2}$$

which can reach up to ~1.25V from the supply rails. Again, this value is conservative. The maximum output current that the cell can sink and source is limited by the base current of the output devices Q3 and Q4 such that

$$I_{E3}\_\max = \beta_{Q3} * I_{C5} \tag{2.4.3}$$

$$I_{E4}\_\max = \beta_{Q4} * I_{C6} \tag{2.4.4}$$

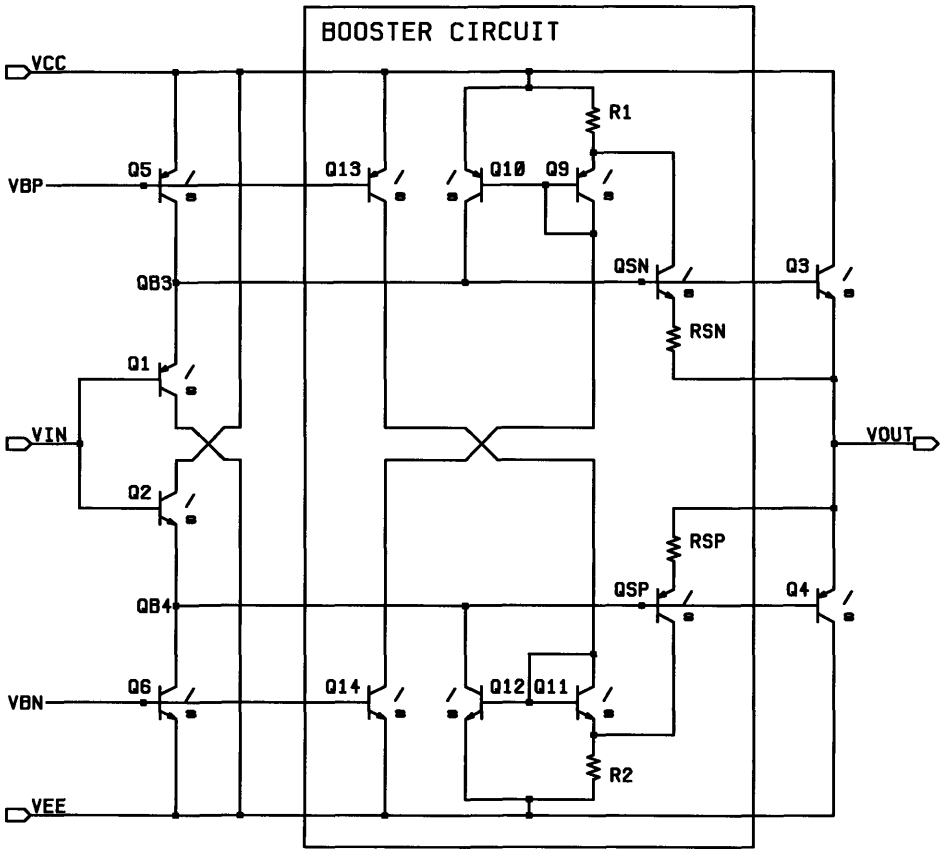

Figure 17. Boosted complementary diamond voltage buffer output stage.

At high output currents, the base currents of the output devices are quite large, requiring bias currents I_{C5} and I_{C6} to be large too. For example, if I_{E6} is 80 mA and β_{Q6} is 50 (a good worst case approximation for a PNP) then I_{B6} is 1.6mA, and thus I_{C6} has to be at least 1.6mA to support the output current. The problem though, is that when the circuit is not sinking or sourcing large currents, it is power inefficient to have such large bias currents in the pre-drivers.

A simple approach to improve the efficiency of the cell while still being able to drive heavy loads (small load resistors), is to dynamically increase the pre-drivers' bias currents. This is achieved with the inclusion of a booster circuit as shown in figure 17.

The booster's operation is quite simple. When the output transistors start to source or sink considerable current, the collector current of sense transistors QSN or QSP increases. This increases the collector current of Q10 and Q12 thus boosting the maximum available base current drive for the output devices. The purpose of resistors RSN and RSP is to limit the sense transistor's collector current at high output currents therefore preventing thermal runaway.

A consequence of the addition of the booster circuit is that the impedance looking into the base of the output transistors becomes negative due the positive feedback nature of the technique. Luckily, this negative impedance shows up in parallel with the incremental emitter impedance of the pre-driver transistors Q1 and Q2 which dominates and hence keeps the circuit stable. In other words, the loop gain of the positive feedback loop is much less than one.

The maximum slew rate of the cell is limited by the slew rate of internal nodes QB3 and QB4. These are

$$SR_{QB3} = \frac{I_{C5}}{C_{NODE}} \tag{2.4.3}$$

$$SR_{QB4} = \frac{I_{C6}}{C_{NODE}} \tag{2.4.4}$$

where C_{NODE} represents the total capacitance at nodes 'QB3' and 'QB4'. Since the output devices are quite large due to their current handling requirements, their collector to base capacitance is substantial and hence C_{NODE} can be a relatively large. Therefore, I_{C5} and I_{C6}, should be chosen such that the output buffer does not limit the slew rate of the amplifier. For the presented amplifier, these were chosen to be 900 uA.

Finally, the current isolation provided by the diamond buffer is approximately β^2 which is quite adequate for most applications.

2.5 The Interface

As mentioned before, the purpose of the interface circuit is to attenuate the current signal fed back by the compensation network into high impedance nodes 'HIZ1P' and 'HIZ1N'. To the amplifier, this results in an apparent decrease in the admittance of the compensation network. To the user, this results in an apparent boost in the input stage's transconductance, G_{M1}. The interface's circuit implementation is shown in figure 18.

The interface circuit is an attenuating complementary common base current buffer. The input current signal at node 'IIN' divides between transistors Q5 and Q7, and between Q6 and Q8 in a 1:A ratio due to the sizing of their emitter areas. The portion of the input current signal that flows into transistors Q5 and Q6, i.e. 1/A of the input current signal, is conveyed to output nodes 'IOP' and 'ION' which are connected to high

impedance nodes 'HIZ1P' and 'HIZ1N'. The current signal that flows into transistors Q7 and Q8, i.e. the other portion of the input current, is thrown away to the supply rails. This way, the interface achieves the desired current attenuation.

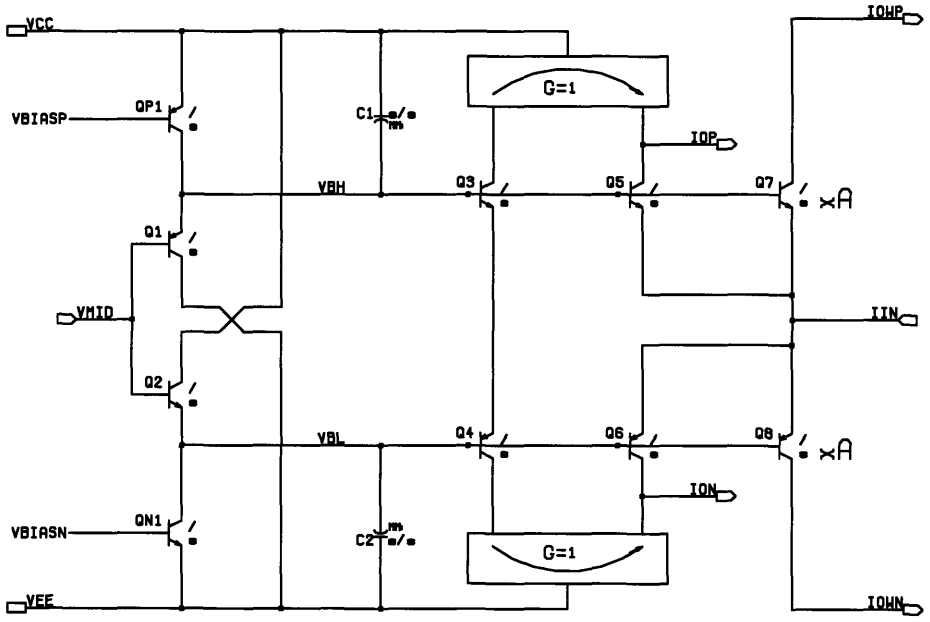

Figure 18. Interface circuit.

The bandwidth of the interface is extremely high since only common base transistors Q5 and Q6 are in the signal paths. The -3dB point of the circuit is estimated by setting the current gain of the common base stage, α_F, equal to 1/sqrt(2). Therefore, it can be shown that

$$Interface\_Bandwidth \approx \frac{f_T}{1+\sqrt{2}} \approx 0.4 f_T \qquad (2.5.1)$$

which evaluates to about 2 GHz for the process in use.

The function of the other components in the circuit is as follows. Transistors Q3 and Q4 and the two current mirrors remove the DC component of the signal at nodes

'IOP' and 'ION'. Transistors Q1, Q2 set the bias voltage at nodes 'VBH' and 'VBL' to one V_{BE} above and below mid-supply node 'VMID'. Also, in conjunction with current source transistors QP1 and QN1, they set the quiescent bias current of transistors Q3 through Q8 via a translinear loop. The collector bias currents are given by

$$I_{C3} = I_{C4} = I_{C5} = I_{C6} = \frac{A_{E3}}{A_{E1}}\sqrt{I_{C1}I_{C2}} \tag{2.5.2}$$

$$I_{C7} = I_{C8} = A\frac{A_{E3}}{A_{E1}}\sqrt{I_{C1}I_{C2}} \tag{2.5.3}$$

assuming $A_{E1}=A_{E2}$ and $A_{E3}=A_{E4}$.

For improved matching, transistors Q7 and Q8 are implemented as several unit transistors identical to Q5 and Q6. Also, their collector voltage sits at the same voltage as Q5's and Q6's collector. This avoids errors due to finite Early voltage in the transistors.

It is interesting to point out that even though the interface circuit is the main innovation of the amplifier, the actual circuit implementation is quite simple.

2.6 Current Distribution Circuit

The current distribution circuit for the presented op-amp is shown in figure 19. Its purpose is to replicate and scale the current from master current source 'IBIAS' to the different stages of the amplifier. For this design, an ideal temperature stable 'IBIAS' is used.

The circuit is composed of four mirrors, two PNP's and two NPN's, and a floating current source 'IREF' with output terminals 'IREFP' and 'IREFN'. As shown in the picture, the first set of current mirrors provides bias currents to the input and second stage

while second set of mirrors provides bias currents to the output stage. The floating current source sets the reference current for the class AB feedback circuit in the second stage.

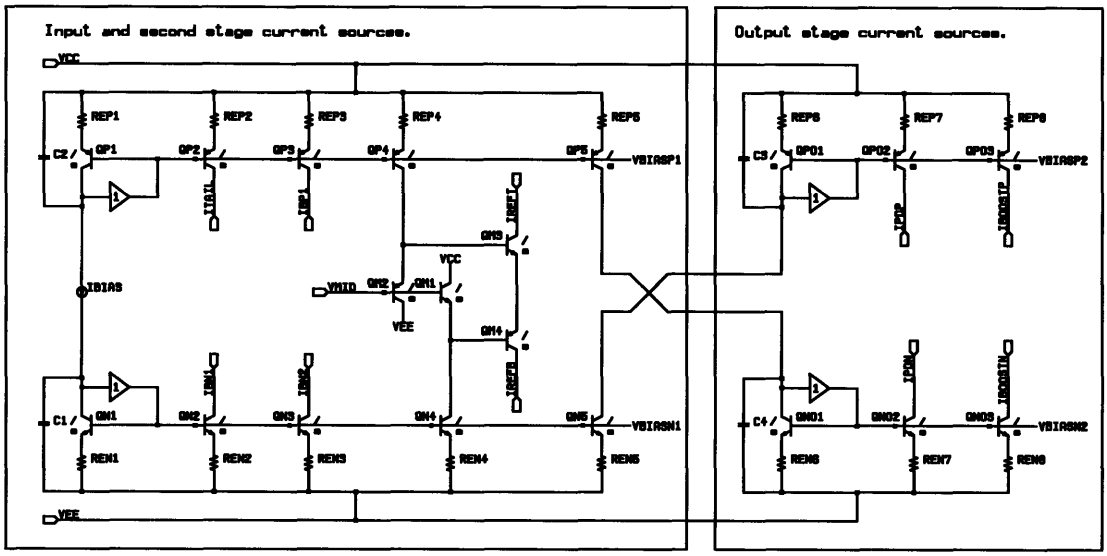

Figure 19. Amplifier's current distribution circuit.

The current sources in the output stage are isolated from the current sources on other stages by means local mirrors. This prevents disturbances in base rails 'VBIASP2' and 'VBIASN2' from coupling into sensitive nodes in the op-amp's signal chain. Sources of these disturbances are capacitive coupling of the output signal through the current source transistors' C_μ and saturation base currents due to over-ranging the amplifier.

In order to improve the op-amp's input/output over-range recovery time, the base rails of all the current sources are driven with a diamond buffer as shown in figures 19 and 20. The advantage of using such a buffer is that it can provide the base rail with very high bi-directional currents, a property that becomes quite beneficial in situations where a

current source saturates. For example, pretend that the input differential pair is taken above the allowed input common-mode and current source 'ITAIL' deeply saturates. This condition will degrade the output impedance of the current source and will lower the magnitude of its output current. Also, the base of the current source transistor will get flooded with unwanted charge due to the forward biasing of its base-collector junction. When the input common-mode returns to the allowed range, the diamond buffer will actively discharge this excess base charge via its NPN output transistor (Q3 in figure 20). This minimizes the current source transition time from the saturation to the forward active regime and thus also minimizes the amplifier's input over-range recovery time.

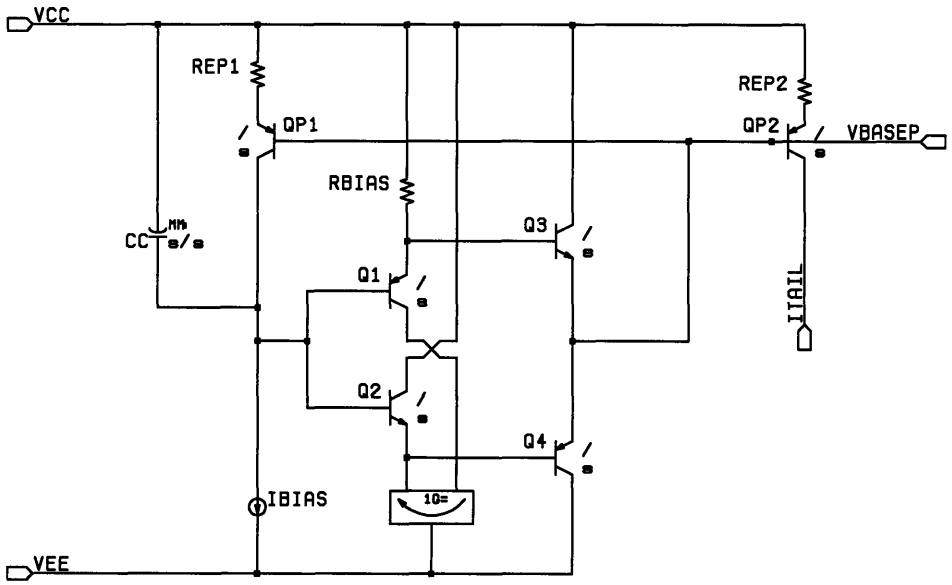

Figure 20. Diamond buffers drive the current source base rails.

As seen in figure 19, all the current sources have been resistively degenerated. This boosts their output impedance and reduces mismatches between them due to different output voltages. The current sources' output impedance is

$$R_{OUT} = R_E + (1 + g_m(r_\pi \parallel R_E)) \cdot ro \approx (1 + \frac{V_{R_E}}{V_{th}}) \cdot r_o \tag{2.6.1}$$

for RE << r_π and $V_{RE} = I_E R_E$, the degeneration voltage. For all current sources, the degeneration voltage is approximately 150 mV, thus their output impedances get boosted by about seven at 27°C.

The floating current source is implemented using the same geometric mean calculator circuit as the one used in the second stage's class-AB biasing loop. This way, reference currents 'IREFP' and 'IREFN' are pre-distorted to cancel out errors due to inaccuracies in the feedback path of the loop (errors in the geometric mean calculator circuit). Looking more closely at figure 13, the current fed back to node 'HIZ1P', I_{C7}, does not equal the current fed back to node 'HIZ1N', I_{C8}. In fact, the relation between them is

$$I_{C7} = I_{C8} + I_{B8} - I_{B7} \tag{2.6.2}$$

which leads to,

$$\frac{I_{C7}}{I_{C8}} = \frac{\beta_N(1+\beta_P)}{\beta_P(1+\beta_N)}. \tag{2.6.3}$$

Therefore, if currents 'IREFN' and 'IREFP' were identical, there will be an unwanted error current at nodes 'HIZ1P' and 'HIZ1N' that has to be compensated by the input stage's transconductors. This leads to input offset voltage. Therefore, by using the same geometric mean calculator circuit to create the floating current source, the error current is added to reference currents 'IREFN' and 'IREFP', and thus it does not need to be provided by the input stage. As a result, no offset input offset voltage is generated.

3. Operational Amplifier Compensation

As the name suggests, externally compensated operational amplifiers require an external compensation network to establish their frequency response and to ensure closed-loop stability and satisfactory transient performance [7]. This chapter describes how to choose this network for several applications using the minor loop feedback approach. This approach is not only simpler than the network-theory compensation method [8, 9] but provides the circuit designer with valuable intuition and insight allowing him to compensate the amplifier over a wide range of applications [7].

In this chapter, we define A(s) as the open-loop gain transfer function of the op-amp such that

$$V_{out}(s) = A(s)(V_p - V_m) = A(s)V_D \tag{3.1}$$

This parameters of this relation are represented in the following figure.

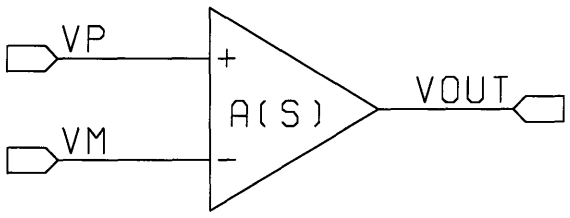

Figure 21. Open-loop operational amplifier.

3.1 Minor Loop Feedback Compensation

As mentioned in chapter one, when a compensation network is connected from the output of the op-amp's second stage to the output of the op-amp's first stage, a minor loop is formed within the amplifier. In this loop, the admittance of the compensation network, Y(s), feeds back a current signal from the output of the second stage to the

output of the input stage as shown in the block diagram of figure 3. Rearrangement of this block diagram results in the block diagram of figure 22, where the input stage's transconductance has been pushed inside the loop.

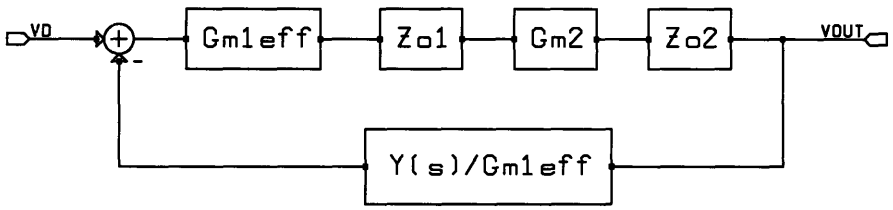

Figure 22. Equivalent block diagram for minor loop compensation.

The minor loop compensation approach is interested in the case where the loop transmission of the minor loop is large such that the amplifier's open-loop transfer function is approximated by

$$A(s) \approx \frac{G_{M1}}{Y(s)} \tag{3.1.1}$$

Thus, by choosing the compensation network, i.e. setting Y(s), the shape of A(s) can be tailored to optimize the amplifier's performance for a given application.

As mentioned in chapter two, any feedforward signals through the compensation network are blocked by the interface circuit and thus are not considered. Also, due to the interface circuit, the effective transconductance of the input stage is

$$G_{M1eff} = A \cdot G_{M1} \tag{3.1.2}$$

where 1/A is the interface's current gain and G_{M1} is the input stage's transconductance.

The next sub-sections describe different compensation schemes using the minor loop feedback compensation approach. The op-amp model shown in figure 7 is used to obtain the ideal responses for each one of them.

3.2 Dominant Pole Compensation

The simplest compensation strategy for an op-amp is the dominant pole scheme which guarantees a -20dB/dec roll-off in A(s) over a wide frequency range. Thus, A(s) is approximated by

$$A(s) = \frac{A_o}{\tau s + 1} \tag{3.2.1}$$

where A_o represents the DC open-loop gain of the amplifier. Figure 23 shows a typical magnitude Bode plot of A(s) for dominant pole compensation. [7]

One way to implement the dominant pole is to use a single capacitor, C_C, as the compensation network. Figure 24 shows the simplified model of the connection. The resulting block diagram is shown in figure 25 where $Y(s) = sC_C$ is the admittance of the compensation capacitor.

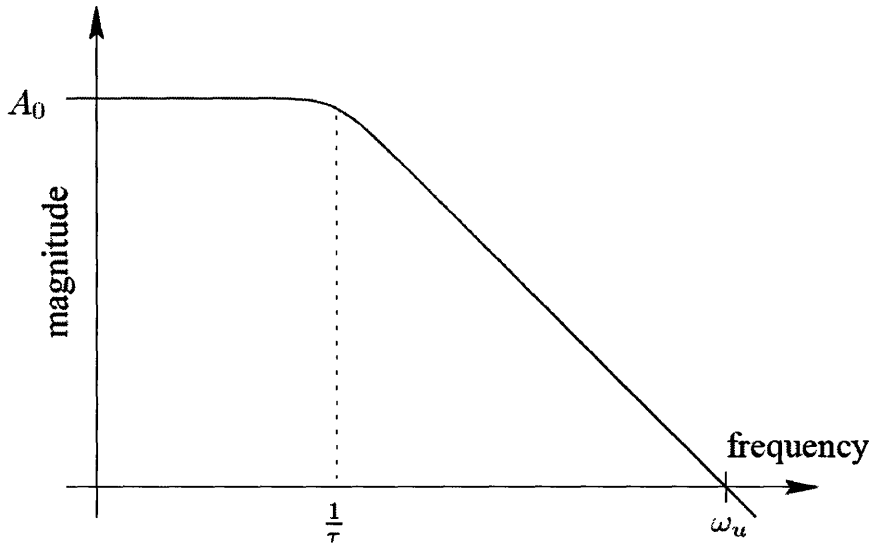

Figure 23. Open-loop gain for dominant pole compensation.

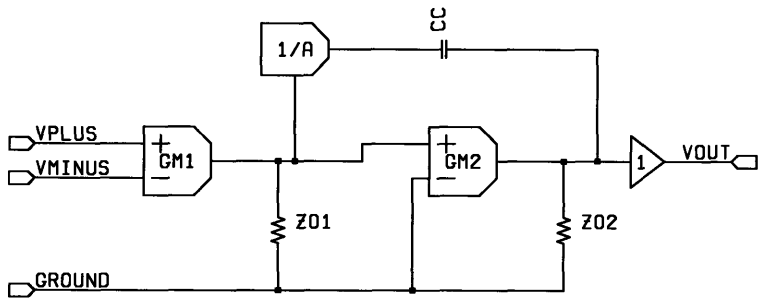

Figure 24. Simplified two stage model op-amp with capacitive compensation.

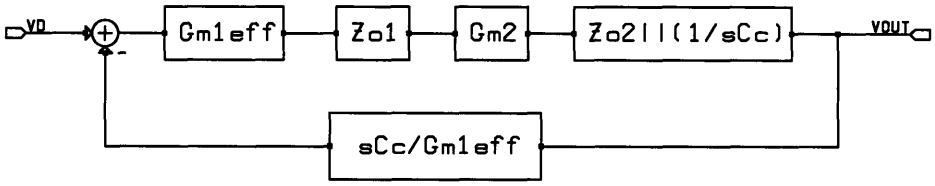

Figure 25. Block diagrams of a two stage op-amp with capacitive compensation.

The above block diagram shows that the addition of the compensation capacitor modifies the amplifier model shown in figures 5 and 6 since it loads the second stage's output node. The loading effect on the input stage's output node is neglected since it is buffered by the interface circuit. Also, it is assumed that the singularities introduced by the interface are at a much higher frequency than any range of interest. Using this model, the forward path of the amplifier is

$$G(s) = G_{M1eff} Z_{O1} G_{M2} (Z_{O2} \parallel Z_C) = G_{M1eff} \left(\frac{R_{O1}}{R_{O1} C_{P1} s + 1} \right) G_{M2} \left(\frac{R_{O2}}{R_{O2} (C_{P1} + C_C) s + 1} \right) \qquad (3.2.2)$$

where

$$Z_C = \frac{1}{sC_C} \qquad (3.2.3)$$

$$Z_{O1} = \left(\frac{R_{O1}}{R_{O1} C_{P1} s + 1} \right) \qquad (3.2.4)$$

$$Z_{O2} \| Z_C = \left(\frac{R_{O2}}{R_{O2}(C_{P2} + C_C)s + 1} \right) \tag{3.2.5}$$

In these equations, C_{P1} and C_{P2} represent the total internal capacitances at the output nodes of the first and second gain stages. The minor loop's feedback path is

$$H(s) = \frac{Y_C(s)}{AG_{M1}} = \frac{sC_C}{G_{M1eff}}. \tag{3.2.6}$$

Using Black's formula [10], the open-loop transfer function of the op-amp is

$$A(s) = \frac{G(s)}{1 + G(s)H(s)} = \frac{G(s)/H(s)}{1/H(s) + G(s)} \tag{3.2.7}$$

Looking at (3.2.7), an interesting result is obtained by noting that when G(s) >> 1/H(s), A(s) ≈ 1/H(s), and when G(s) << 1/H(s), A(s) ≈ G(s). Thus, if G(s) and 1/H(s) are plotted on the same Bode plot, A(s) can be approximated by tracing the lower curve of the two. Remember that the case where G(s) >> 1/H(s) is the one of interest for minor loop compensation, since A(s) ≈ 1/H(s) = G_{M1eff}/Y(s). Figure 26 shows a Bode plot of the forward path G(s), the inverse of the feedback path 1/H(s), and the compensated open-loop gain A(s) for a compensation capacitor C_C of 10 pF.

The location of the compensated poles and open-loop unity frequency, ω_U, can be obtained from the intersection of the plotted curves. The location of the dominant pole, ω_1, is at the low frequency intersection of G(s) and 1/H(s). Since this intersection happens before the poles of G(s), then

$$G_{M1eff} R_{o1} G_{M2} R_{o2} = \frac{G_{M1eff}}{\omega_1 C_C} \tag{3.2.8}$$

and thus

$$\omega_1 = \frac{1}{R_{o1} G_{M2} R_{o2} C_C}. \tag{3.2.9}$$

The high frequency pole, ω_2, happens at the high frequency intersection of G(s) and 1/H(s). Since this intersection happens after the poles of G(s), then

$$\frac{G_{M1eff} G_{M2}}{\omega_2^2 C_{P1}(C_{P2} + C_C)} = \frac{G_{M1eff}}{\omega_2 C_C} \tag{3.2.10}$$

and thus

$$\omega_2 = \frac{G_{M2} C_C}{C_{P1}(C_{P2} + C_C)} \tag{3.2.11}$$

Finally, the unity gain frequency, ω_U, happens at the intersection of 1/H(s) and 1. Therefore,

$$\omega_U = \frac{G_{M1}}{C_C} \tag{3.2.12}$$

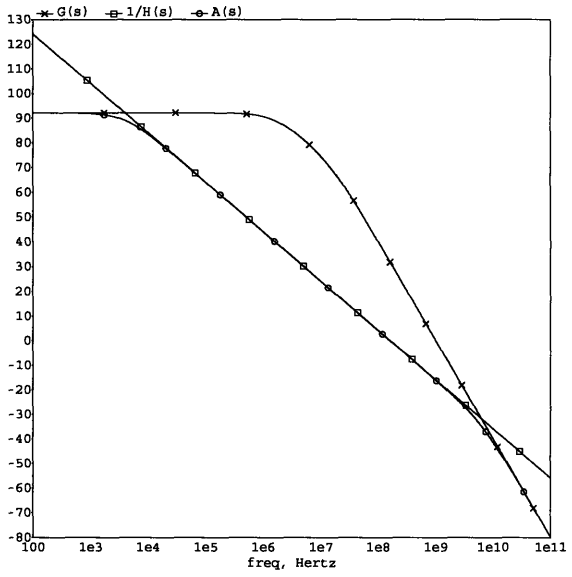

Figure 26. Forward Path G(s), Inverse Feedback Path 1/H(s) and Open-loop gain A(s).

If the high frequency pole is designed to be at a higher frequency than ω_U, then the open-loop gain A(s) obtained approximates quite well the ideal transfer function shown in equation (3.2.1).

3.3 Defeating the Gain-Bandwidth Product

Capacitive dominant pole compensation is the most used compensation scheme in internally compensated op-amps due to the guaranteed stability that the arrangement provides as long as any high frequency poles are located past ω_U. Thus, the op-amp can be used as a buffer, integrator, amplifier, etc, with an adequate transient response. Once the compensation capacitor is chosen, the op-amp's open-loop dynamics are set i.e. ω_1, ω_2 and ω_U are fixed.

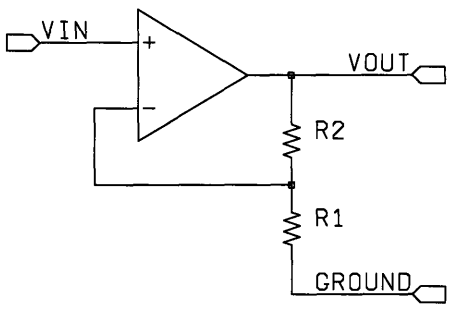

Figure 27. Schematic of a non-inverting amplifier.

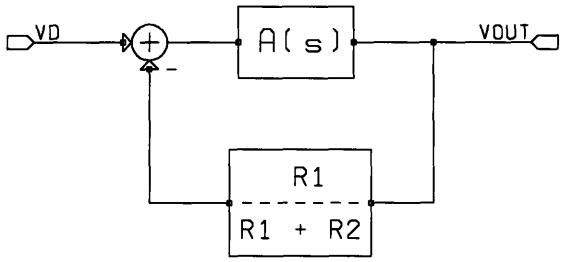

Figure 28. Non-inverting amplifier block diagram

The simple amplifier configuration is one example where having a fixed open-loop gain transfer function affects performance. Figure 27 shows the non-inverting amplifier op-amp configuration. The DC closed-loop gain and feedback factor for the configuration are given by

$$A_{CL} = \frac{V_o}{V_i} = \frac{R_1 + R_2}{R_1} = \frac{1}{F} \tag{3.3.1}$$

$$F = \frac{R_1}{R_1 + R_2} \tag{3.3.2}$$

The block diagram of the non-inverting amplifier is shown in figure 28. The circuit's loop gain is

$$L(s) = A(s)\frac{R_1}{R_1 + R_2} = A(s)F\,. \tag{3.3.3}$$

Using Black's formula, the closed-loop transfer function of the circuit is

$$\frac{V_o}{V_i}(s) = \frac{A(s)}{1 + A(s)F}\,. \tag{3.3.4}$$

Substituting the ideal dominant pole open-loop gain from (3.2.1) into (3.3.4), it can be found that

$$\frac{V_o}{V_i}(s) = \frac{1}{F}\frac{1}{\frac{\varpi s}{A_O F} + \frac{1}{A_O F} + 1} \approx \frac{1}{F}\frac{1}{\frac{\varpi s}{A_O F} + 1} \tag{3.3.5}$$

for $A_O F >> 1$. Rewriting,

$$\frac{V_o}{V_i}(s) \approx A_{CL}\frac{1}{\frac{\varpi s}{A_O F} + 1} \tag{3.3.6}$$

The closed-loop bandwidth for the connection in radians per second is

$$BW = \frac{A_O F}{\tau}. \tag{3.3.7}$$

Equations (3.2.1) and (3.2.7) show that as the feedback factor F is reduced to increase the closed-loop gain, the closed-loop bandwidth decreases. Even more important, if the closed-loop gain and closed-loop bandwidth are multiplied, then

$$GBW = A_{CL}BW = \frac{A_O}{\tau}. \tag{3.3.8}$$

The gain–bandwidth product of the configuration is a constant dependent on A_0 and τ, parameters set by technology limitations and the compensation of the op-amp.

The constant gain-bandwidth product result obtained in (3.3.8), can also be shown graphically by using the observation made on Black's formula in the previous section. Recapping, by Black's formula the closed-loop gain of the amplifier is

$$A_{CL}(s) = \frac{V_o}{V_i}(s) = \frac{G(s)}{1+G(s)H(s)} = \frac{A(s)}{1+A(s)F}. \tag{3.3.9}$$

where the forward path of the configuration is G(s) = A(s) and the feedback path H(s) = F. Thus, in the frequency range where G(s) >> 1/H(s), A(s) ≈ 1/H(s), and where G(s) << 1/H(s), A(s) ≈ G(s). As a result, if G(s) and 1/H(s) are plotted on the same Bode plot, $A_{CL}(s)$ can be approximated by tracing the lower curve of the two.

Figure 29 clearly shows in a graphical way how the closed-loop bandwidth decreases when the closed-loop gain increases as a direct consequence of the shape of A(s).

Even though dominant pole compensation is not optimal for almost all op-amp applications, it is by far the most widely used compensation scheme. This is because as long as frequency independent feedback components are used, the amplifier will be stable

for all closed loop gains above a specified minimum (normally one, but greater than one for de-compensated op-amps like the OP-37).

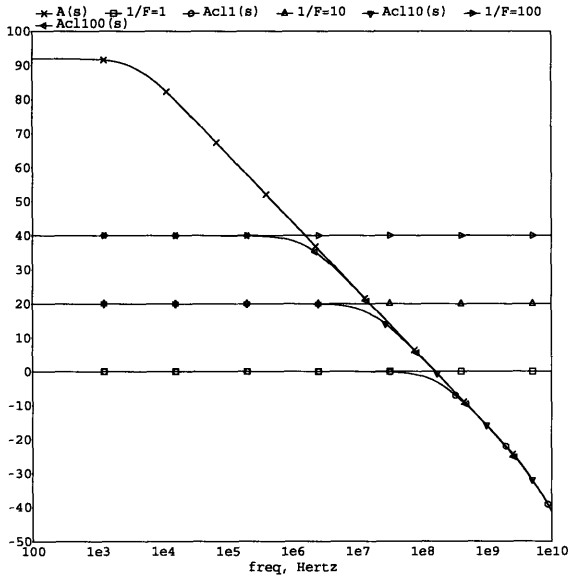

Figure 29. Bode plots of A(s), 1/F and $A_{CL}(s)$ for F=1, 10, 100.

In the case of externally compensated amplifiers, the compensation constraints are different. Now, what matters is the phase-margin of the loop gain L(s) in a given application. For the non-inverting amplifier, the loop gain is

$$L(s) = A(s)\frac{R_1}{R_1 + R_2} = A(s)F\,.$$

When capacitive dominant pole compensation is used in the amplifier, at frequencies past the dominant pole ω_1, the open-loop gain of the op-amp is about

$$A(s) \approx \frac{G_{M1}}{sC_C} \tag{3.3.10}$$

and thus the loop gain for the non-inverting amplifier is

$$L(s) = A(s)F \approx \frac{G_{M1}}{sC_C} F \,. \tag{3.3.11}$$

For closed-loop gains greater than one, i.e. feedback factors, F, less than one, the compensation capacitor can be reduced to keep L(s) unchanged and thus keep the closed-loop bandwidth constant. Figure 30 shows the loop gains Bode plots, L(s), and closed-loop gain, $A_{CL}(s)$, for a non-inverting amplifier with closed-loop gains of 1, 10 and 100 (i.e. F=1, 0.1 and 0.01) with scaled compensation capacitor. It can be observed how the closed-loop bandwidth remains roughly constant for all three values of F.

By adapting the compensation network to the application, externally compensated op-amps defeat the gain-bandwidth product issue.

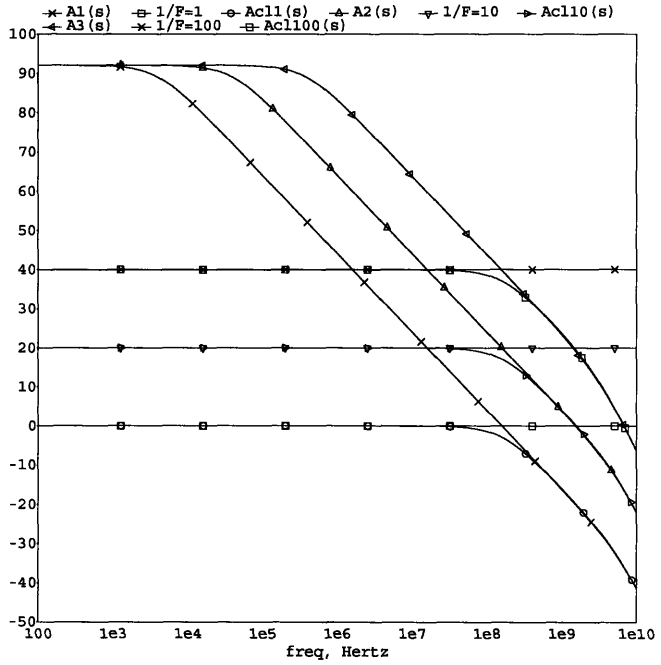

Figure 30. Bode plot of L(s), 1/F and $A_{CL}(s)$ for F=1, 10, 100.

3.4 Two-pole Compensation

One important closed-loop system specification is steady-state error. In the case of closed-loop operational amplifier circuits, the concern is the dynamic tracking to a step and a ramp input signals. As mentioned before, most internally compensated operational amplifiers use capacitive dominant pole compensation which implements an open-loop gain transfer function of the form

$$A(s) = \frac{A_o}{\tau s + 1} \tag{3.4.1}$$

This A(s) can be approximated as

$$A(s) \approx \frac{A_o}{\tau s} \tag{3.4.2}$$

at frequencies above the dominant pole. Therefore, it is expected that the closed-loop operational amplifier will have no steady-state error to an input step signal since A(s) looks like an integrator.

In the case where zero steady-state error to a ramp is desired, dominant pole compensation would fail since two integrations are required in A(s). Two-pole compensation is the implementation of the special-purpose transfer function that allows the amplifier to follow a ramp with no steady-state error.

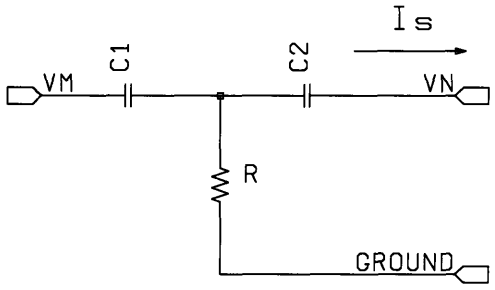

Figure 31. Two-pole compensation network.

Figure 31 shows a compensation network that will achieve two-pole compensation. The short-circuited transfer admittance of the network is

$$Y(s) = \frac{I_S}{V_M}(s) = \frac{RC_1C_2s^2}{R(C_1 + C_2)s + 1} \tag{3.4.3}$$

When the network is used in the amplifier, the compensation minor loop feedback path is

$$H(s) = \frac{Y(s)}{AG_{M1}} = \frac{1}{G_{M1eff}} \frac{RC_1C_2s^2}{R(C_1 + C_2)s + 1} \tag{3.4.4}$$

and the approximate open-loop transfer function (when G(s) is high) is

$$A(s) = \frac{G(s)}{1 + G(s)H(s)} \approx \frac{1}{H(s)} = G_{M1eff} \frac{R(C_1 + C_2)s + 1}{RC_1C_2s^2} \tag{3.3.5}$$

As equation (3.3.5) shows, the two-pole compensation network implements the two integrations required in A(s) for zero steady-state error to a ramp.

Figure 32 shows the Bode plot of the forward path G(s), the inverse of the feedback path 1/H(s), and the compensated open-loop gain A(s) for two-pole compensation. It can be observed that the open-loop gain of the amplifier behaves like a double integrator for most of the frequency range of interest ($\omega < \omega u$).

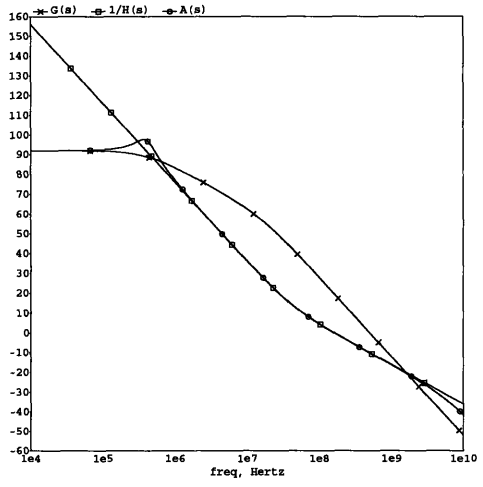

Figure 32. Bode plot of A(s), G(s) and 1/H(s) for two-pole compensation.

The zero introduced in A(s) by the network at a $\omega < \omega_C$ is for phase recovery. The phase advance provided by the zero, allows the amplifier to 'cross-over' with positive phase margin and thus be stable.

The superior tracking to an input ramp offered by two-pole compensation is observed in figure 34. The graph plots the error signal of an inverting amplifier (V_{Error} = V_{Plus} - V_{Minus}) using dominant pole and two-pole compensation when driven with a 1 V/μs input ramp. As expected, the error signal in the dominant pole compensated op-amp reaches a constant value while the error signal of the two-pole compensated one goes to zero.

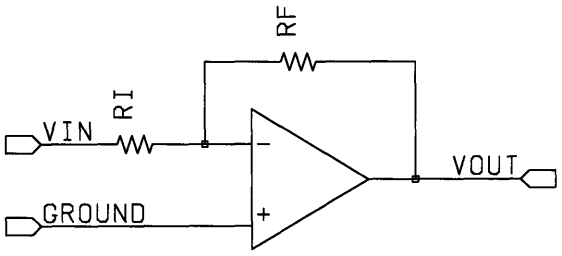

Figure 33. Schematic of a simple inverting amplifier.

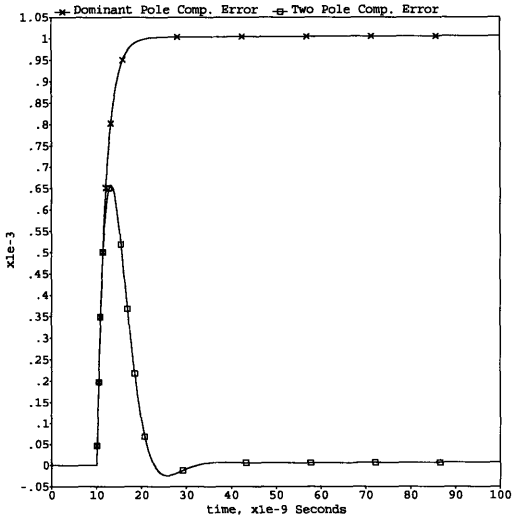

Figure 34. Steady state error to a ramp for dominant pole and two-pole compensation.

3.5 Compensation that Introduces a Zero

For most modern high-speed op-amps, the most dreaded load is the purely capacitive one. In most applications, a high-speed amplifier will become unstable with a load capacitor of a few tens of picofarads. Therefore, what can be done if for example the load capacitance is 10 nF.

Consider the case where an op-amp is connected as a unity gain buffer with a purely capacitive load as shown in figure 35. This connection is typically used in sample and hold circuits where large capacitors are used to prevent voltage droop.

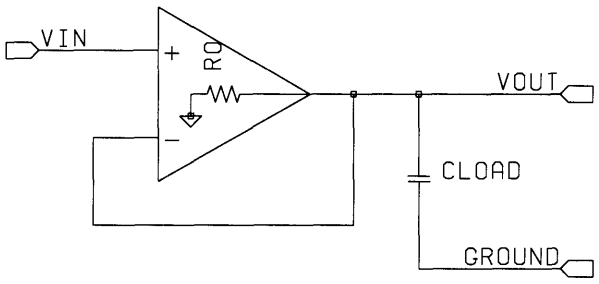

Figure 35. Unity-gain buffer with purely capacitive load.

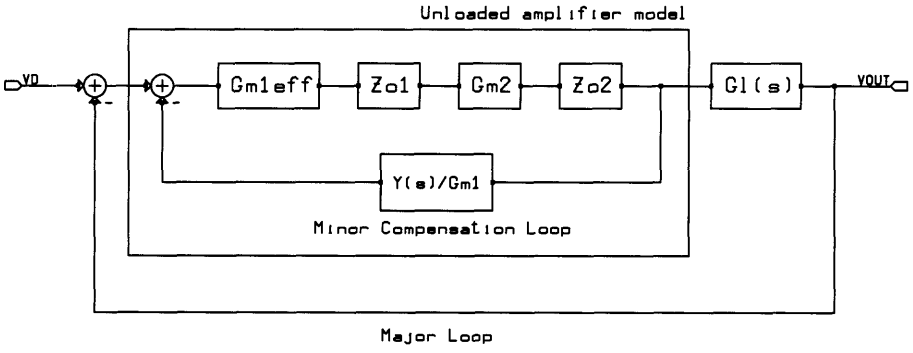

Figure 36. Block diagram for unity gain buffer with capacitive load.

Due the output resistance of the amplifier and the location of the major loop sampling point (node V_{OUT}), the pole created by R_O and C_{LOAD} falls inside the forward path of the amplifier's major loop. Figure 36 shows the block diagram of the circuit where the pole due to C_{LOAD} is modeled by $G_L(s)$. The transfer function of $G_L(s)$ is

$$G_L(s) = \frac{1}{R_O C_{LOAD} s + 1}. \tag{3.5.1}$$

If dominant pole compensation is used, then the op-amp's open-loop gain transfer function is approximately

$$A(s) \approx \frac{G_{M1eff}}{Y(s)} = \frac{G_{M1eff}}{sC_C} \tag{3.5.2}$$

and the major loop gain of the buffer connection is

$$L(s) \approx A(s)G_L(s) = \frac{G_{M1eff}}{sC_C} \frac{1}{R_O C_{LOAD} s + 1}. \tag{3.5.3}$$

A typical modern high-speed non-rail-to-rail op-amp, will have an open-loop output impedance of about 10 ohms. Therefore the time constant $R_O C_{LOAD}$ is about 100ns and the frequency of the output pole is 1×10^7 radians per seconds (1.6 MHz). Also, a typical cross-over frequency for a modern amplifier is 1×10^9 radians per second (~160 MHz). Using these numbers, the major loop gain is given by

$$L(s) \approx \frac{10^9}{s} \frac{1}{10^{-7} s + 1}. \tag{3.5.4}$$

Figure 37 shows the Bode plot of L(s). The output pole has introduced enough phase lag to drop the phase margin of the connection to about 6 degrees which is pretty unacceptable for most applications. This degrade in stability is also reflected by the vastly under-damped step response of the loaded connection.

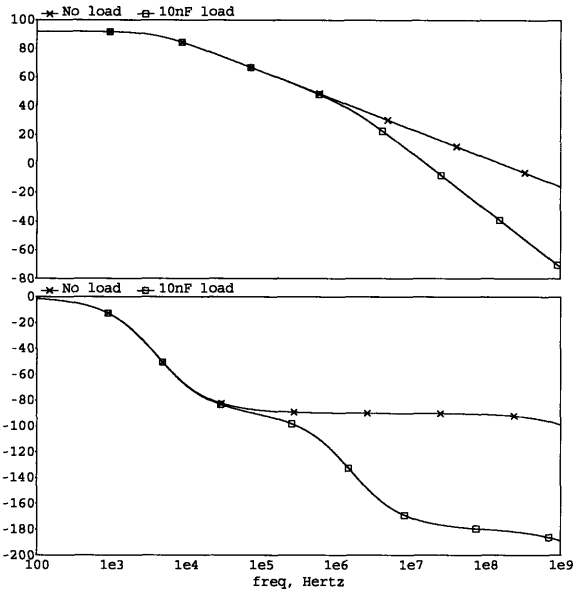

Figure 37. Bode plot of L(s) with and without capacitive load using dominant pole compensation.

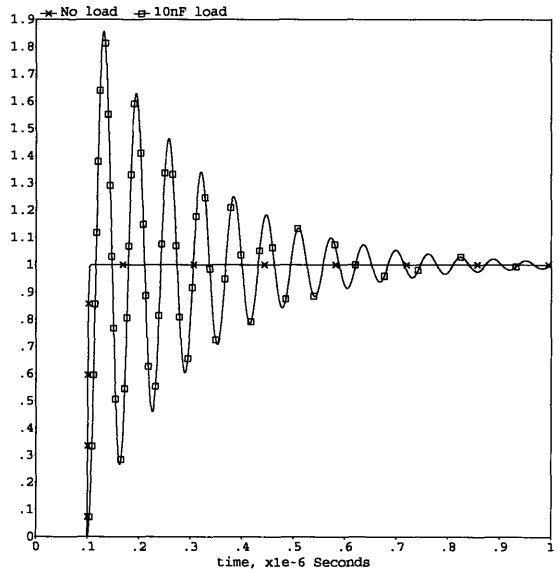

Figure 38. Buffer step response, C_{LOAD} = 0 and 10 nF.

One way to improve the stability of the buffer is to introduce a zero in A(s) such that the phase lost due to output pole is partially recovered before the cross-over frequency of L(s). This way the circuit's phase margin is restored.

The proposed zero can be introduced with an RC compensation network like the one shown in figure 39.

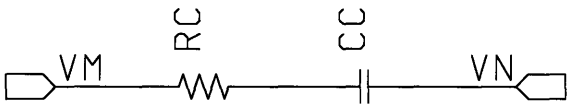

Figure 39. RC compensation network.

The short-circuited transfer admittance of the network is

$$Y(s) = \frac{C_C s}{R_C C_C s + 1} \tag{3.5.5}$$

and thus the open-loop gain of the amplifier is approximately

$$A(s) \approx \frac{G_{M1eff}}{Y(s)} = \frac{G_{M1eff}(R_C C_C s + 1)}{sC_C}. \tag{3.5.6}$$

The new major loop gain is

$$L(s) = A(s)G_L(s) \approx \frac{G_{M1eff}(R_C C_C s + 1)}{sC_C} \frac{1}{R_O C_{LOAD} s + 1}. \tag{3.5.7}$$

If R_C and C_C are chosen such that the introduced zero is at the same frequency as the output pole, the resulting loop gain (using the previously assumed values) is approximately

$$L(s) \approx \frac{10^9}{s}. \tag{3.5.8}$$

Figure 40 shows the loaded and unloaded Bode plot of L(s) with the new the RC compensation network. The phase margin has improved to almost 90 degrees due to the phase restoring effects of the introduced zero. Sadly, a resonance has appeared in L(s) at a frequency past cross-over indicating the possibility of an internal instability.

It can be shown [1, 6] that the stability of the minor loop is compromised when a simple RC network is used to implement the proposed zero. One way to stabilize the minor loop is to connect a small capacitor $C_M << C_C$ across the network as shown in figure 41.

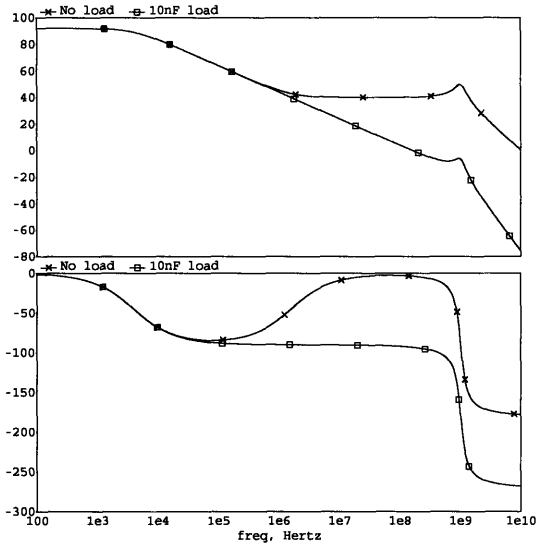

Figure 40. Bode plot of L(s) with RC compensation.

The Bode plot of L(s) with the improved RC compensation network is shown in figure 42. The introduction of capacitor C_M has vastly reduced the resonance suggesting improved stability in the minor loop. However, it has also reduced the phase margin due to the introduction of an extra pole in A(s). This extra pole is located at approximately

$$p_M \approx \frac{1}{R_C C_M} \tag{3.5.9}$$

for $C_M << C_C$.

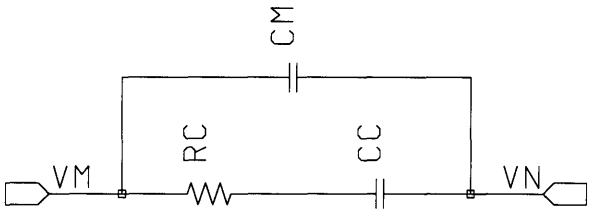

Figure 41. Improved RC compensation network.

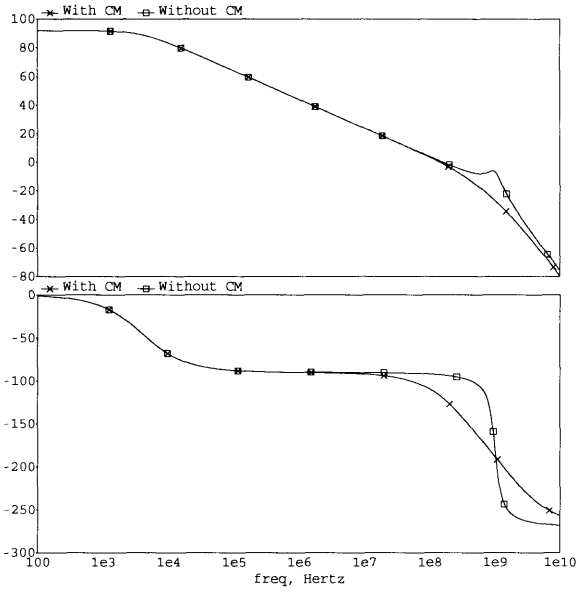

Figure 42. Bode plot of L(s) with improved RC compensation.

Figure 43 shows the step response of the op-amp buffer with the 10 nF load capacitor and the improved RC compensation network. Compared to the step response in figure 38, the stability improvement is evident. It is important to remember that this compensation scheme was implemented to stabilize the operational amplifier when driving a 10nF load. Therefore, adequate performance should not be expected from the op-amp when the load is removed.

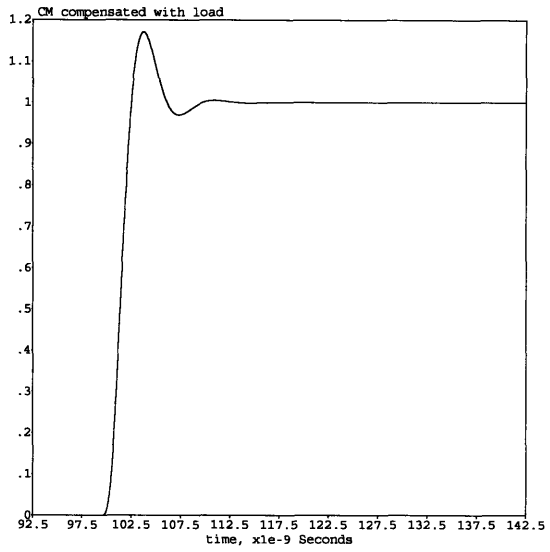

Figure 43. Loaded buffer step response with special purpose compensation.

As the previous sections also revealed, yet again, having external compensation allows the amplifier achieve levels of performance that their internally compensated counterparts can't. In this case, the amplifier can drive very heavy capacitive loads that would render any internally compensated unit unstable.

4. Simulated Results

In a general purpose amplifier, many specifications are considered when describing its overall performance. Since the thesis is mainly concerned with the external compensation capability of the amplifier, only the most important will be covered.

The overall amplifier was simulated using Adice 5, Analog Devices' proprietary simulation tool. Also, the most current models for the process were used.

4.1 Compensation Independent Performance

Since the amplifier's compensation is external, its dynamics can be optimized by the user for a given application. As a result, it makes sense to first look at the op-amp's performance metrics which are independent of the compensation employed. These metrics are mainly 'static' or DC metrics, i.e. they measure the response of the amplifier to either DC or very slow stimuli. Among them we have

- Input offset voltage: The DC voltage that must be applied between the input terminals to force the quiescent DC output voltage to zero or mid-supply. This voltage is specified as the maximum over the operating temperature range.
- Input bias current: The average of the currents into the two input terminals with the output at zero or mid-supply. Notice, that a negative input bias current implies that current is coming out of the input terminals.
- Input offset current: The difference between the currents into the two input terminals with the output at zero or mid-supply.

- Differential open-loop gain: The ratio of the change in output voltage due to the change in differential input voltage with the amplifier in an open-loop configuration.
- Slew Rate: The closed-loop amplifier's output voltage rate of change for an input step signal. Typically, this metric is very dependant on the compensation network, so the quoted slew rate corresponds to the unity gain buffer case (G = +1) with simple capacitive compensation.
- Input resistance: The resistance to ground at the input of a unity gain buffer configuration.
- Input common-mode range: The range of input common-mode voltage that if exceeded will cause the operational amplifier to cease functioning properly. Typically, the output signal will cease to respond to input signals with common-mode voltages outside this range.
- Short circuit output current: The maximum output current that the amplifier can supply with its output shorted to ground or mid-supply. This metric is correlated to the minimum resistance that the amplifier can drive.
- Output Voltage range: The maximum positive and negative voltages that the amplifier's output can reach without waveform 'clipping'.
- Common-mode rejection ratio: The ratio of differential voltage amplification to common-mode voltage amplification. This metric quantifies how the input common-mode voltage affects the output voltage with respect to the input differential voltage.

- Power supply rejection ratio: The ratio of the change in input offset voltage due to a change in power supply voltage. This metric quantifies the amplifier's sensitivity to signals in the power supply rails.
- Power supply current: The maximum current provided by the power supply to operational amplifier over the operating temperature range.

Table 2 shows that all the proposed specifications have been exceeded. All of these were achieved via careful design.

	PROPOSED	SIMULATION RESULT
DC SPECIFICATIONS		
• Input offset voltage (systematic[2])	< 1 mV	0.1 mV
• Input offset current	< 10 nA	2.3 nA
• Input bias current	< 3 μA	2.95 μA
• Open-loop gain	> 50,000	56,000
DYNAMIC SPECIFICATIONS		
• Maximum closed-loop Bandwidth	100 MHz	185 MHz (PM = 60°)
• Slew rate, G = +1	> 100 V/μs	160 V/μs
INPUT CHARACTERISTICS		
• Input resistance	> 1 MΩ	6.3 MΩ
• Input common mode range	At least 1 V from the positive rail and the negative rail.	0.9 V from positive rail, 0.1V beyond negative rail
OUTPUT CHARACTERISTICS		
• Short circuit current	> 80 mA	Source: 147 mA Sink: 149 mA
• Output range	At least 1.25 V from supply rails.	0.95 V from positive and negative supplies
COMMON MODE REJECTION RATIO	> 70 dB	107 dB
POWER SUPPLY REJECTION RATIO	> 70 dB for both supplies	Positive Supply: 97 dB Negative Supply: 92 dB
POWER SUPPLY		
• Supply current	< 10 mA	9.66 mA

Table 2: Comparison table between proposed specifications and simulated results.

[2] Systematic input offset voltage refers to the offset voltage generated by circuit imbalances. It does not consider the random mismatches in the input devices.

4.2 Dynamic Performance

Chapter 3 described the minor loop op-amp compensation approach and detailed the dominant pole, the two-pole, and the zero introducing compensation schemes. In this section, these schemes will be employed in the proposed operational amplifier.

In order to appropriately compensate the presented op-amp, the user needs to know its small signal characteristics. These are summarized in table 3 and figure 45. The latter shows that the bandwidth of the interface is about 4 GHz, about twenty times higher than the maximum closed-loop bandwidth of the amplifier. Therefore, the assumption that ignored the minor loop pole due to the interface's finite bandwidth holds quite well. The magnitude of the interface's output current signals is 26 dB below the magnitude of the input signal, which demonstrates the fixed current attenuation factor of 10 (attenuation of 20 to each high impedance node). The input impedance of the interface remains flat over frequency up to about 2 GHz at a magnitude of 14.1 Ω. After this frequency, it begins to increase showing an inductive behavior. This behavior will be mitigated by the capacitance to ground of the bonding pad.

Small Signal Parameter	Description	Value
G_{M1}	Input stage transconductance	$1x10^{-3}$ mho
G_{M2}	Second stage transconductance	$40x10^{-3}$ mho
Ro	Amplifier open-loop output resistance	8 Ω
A	Interface attenuation factor	10
τ	Interface bandwidth associated time-constant	40 ps
R_{IN}	Interface input resistance	14.1 Ω

Table 3. Summary of op-amp's small signal parameters.

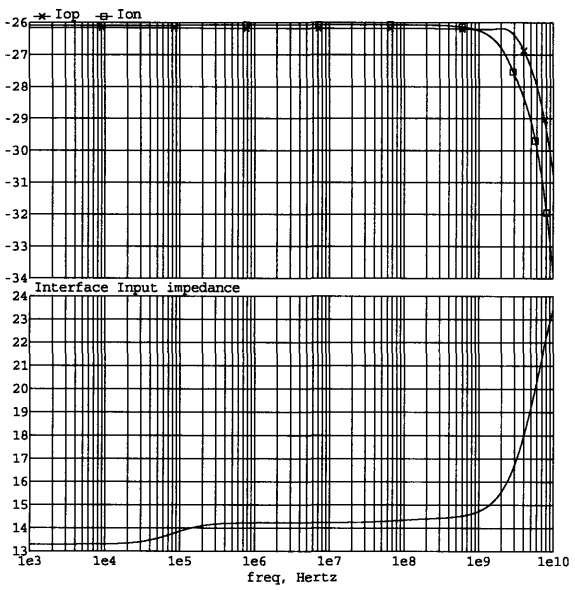

Figure 44. Interface transfer characteristics and input impedance.

4.2.1 Gain-Bandwidth Optimized Dominant Pole Compensation

The discussion section 3.3 showed that when the op-amp is used in a non-inverting gain configuration and compensated with capacitive dominant pole (a single compensation capacitor), the closed-loop bandwidth of the connection decreases as the close loop gain increases. Also, it was shown that this behavior can be defeated by proportionally reducing the compensation capacitor as the closed-loop gain is increased. This behavior also applies to the inverting amplifier connection.

Figure 46 shows the loop gain for a non-inverting amplifier with close-loop gains of 1, 10, and 100 using capacitive dominant pole compensation. The compensation capacitors are 10pF, 1pF and 0pF respectively. These values optimize the bandwidth for closed-loop gains of 1, 10 and 100. The unity gain frequencies for these closed-loop gains are 160MHz, 120MHz and 60MHz with phase margins of 61°, 54° and 60°. The drastic loss in bandwidth for the gain of 100 case is due to an internal Miller capacitance

that sets the dynamics of the amplifier when the compensation terminals are left unconnected (C_C = 0pF). This capacitance comes from the reverse biased shottky diodes across the input and output terminals of the second stage (figure 11).

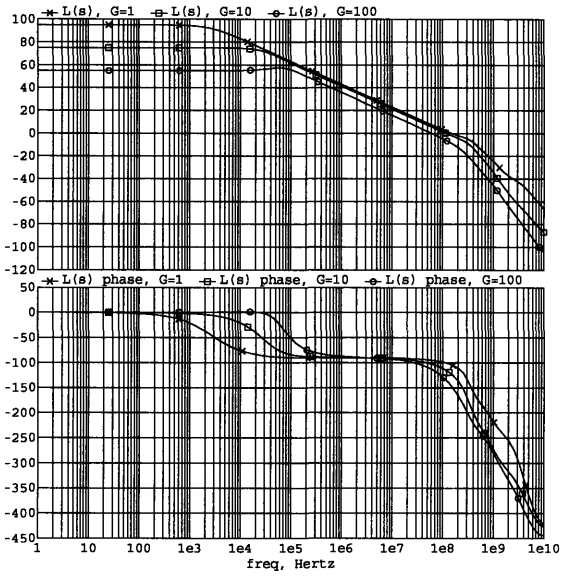

Figure 45. Non-inverting amplifier L(s) (G=1, 10,100) with bandwidth optimized compensation

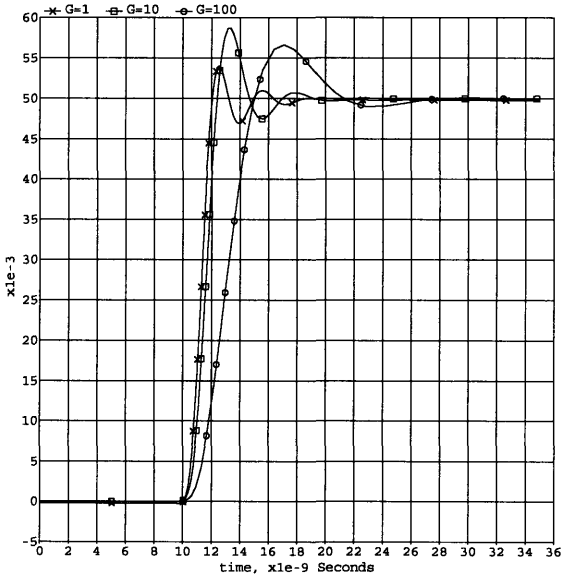

Figure 46. Non-inverting amplifier step responses (G=1, 10, 100) with bandwidth optimized compensation.

Figure 47, shows the step response for these three closed-loop gains (normalized amplitudes). As predicted by the configuration's bandwidth loss, the rise time for the closed-loop gain of 100 (circles) is significantly lower than for the other closed-loop gains.

4.2.2 Two-pole Compensation

As mentioned in section 3.4, to have zero steady-state error to an input ramp, the op-amp requires two-pole compensation. This compensation method implements two integrations in the op-amp's open-loop loop gain A(s) by means of a T network like the one shown in figure 31.

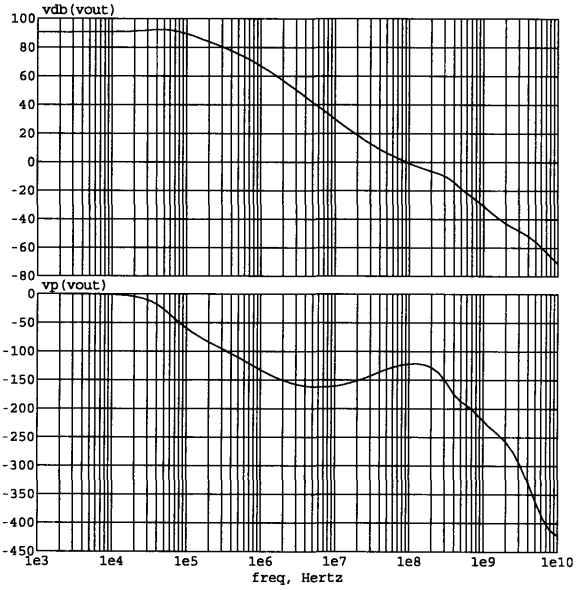

Figure 47. Amplifier's open-loop gain with two-pole compensation.

Figure 48 shows the open-loop gain of the amplifier with two-pole compensation. The employed compensation network component values are CC = 40pF and RC = 50Ω. This places the two-pole compensation zero at 40 MHz and cross-over at 90MHz. Figure 49 shows the error signal of an inverting unity gain amplifier (G = -1) to a 1 V/μs input ramp using single-pole and two-pole compensation. As expected, the two-pole compensation scheme greatly reduces the steady state error while single-pole compensation does not.

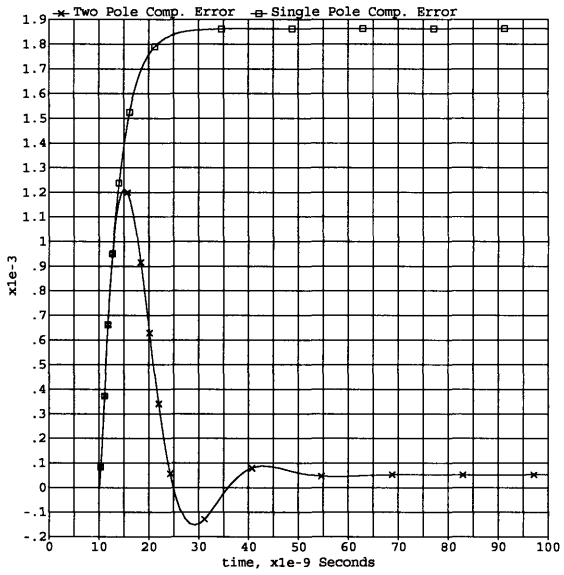

Figure 48. Error signal to an input ramp using two-pole and single-pole compensation.

4.2.3 Compensation that Introduces a Zero

Section 3.5 explored a specialized compensation scheme that introduced a zero in the open-loop gain of the amplifier. This scheme turned out to be very useful when the op-amp is driving a heavy capacitive load. In this situation, the amplifier's output impedance and the load capacitor form a pole which appears in the op-amp's open-loop

transfer function. Therefore, the introduced zero can be used to cancel out the detrimental effects introduced by this pole.

Figure 50 shows the open-loop gain of the loaded and unloaded amplifier compensated with a 10 pF compensation capacitor. The load capacitance is 10 nF. The load capacitor introduces a pole at approximately 2 MHz and lowers the amplifier's phase margin to 2 degrees. Figure 51 shows the amplifier compensated with an RC network using a 50pF compensation capacitor and a 2KΩ resistor. The network introduces a zero at 1.6 MHz which renders the effects of the output pole to insignificance. Figure 52 shows the step response for the amplifier in a non-inverting unity gain configuration driving a 10 nF capacitive load.

In this amplifier, capacitor C_M is not required since there is an internal parasitic capacitance (as mentioned in 4.2.1) that accomplishes the same effect as the former.

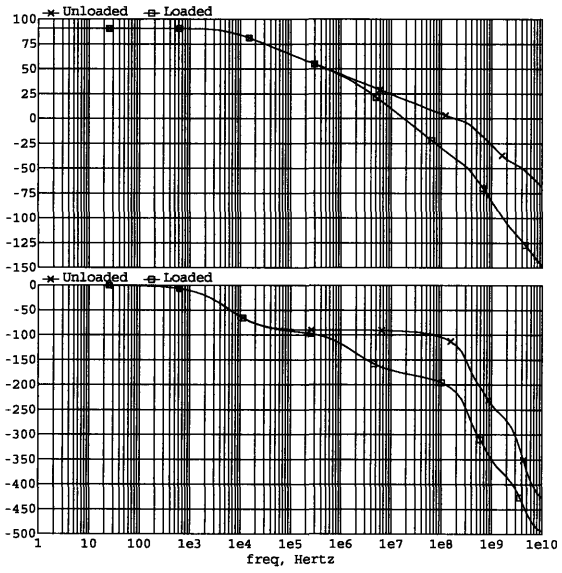

Figure 49. Amplifier's open-loop gain with and without 10nF load (C_C=10pF).

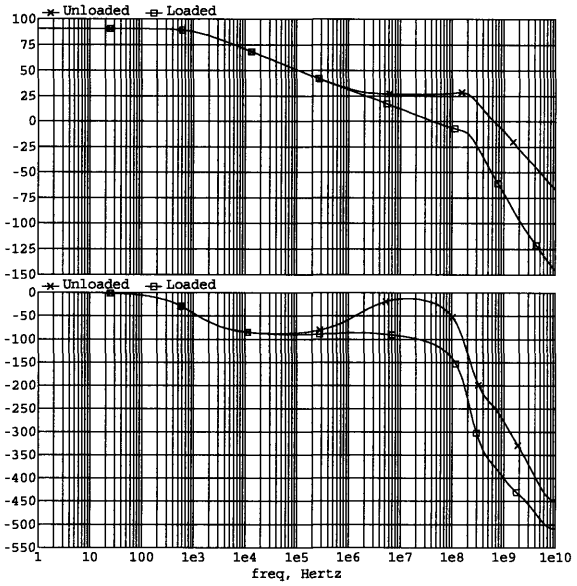

Figure 50. Amplifier's open-loop gain with RC compensation, with and without 10nF load.

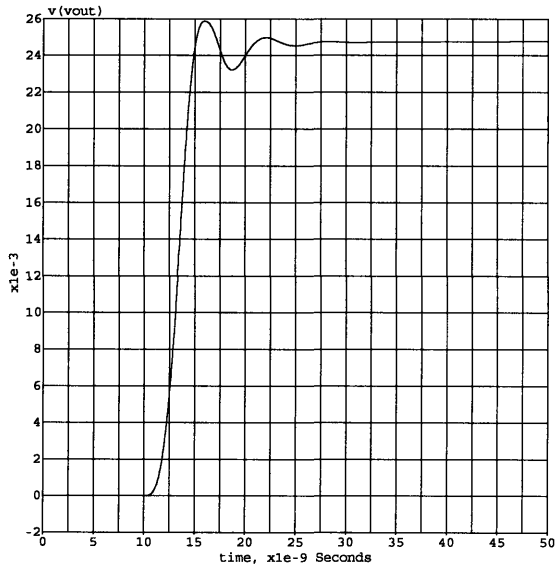

Figure 51. Unity gain buffer step response with RC compensation and a 10nF load capacitor.

4.3 Representative Figures

In all the graphs except where indicated, the following conditions were used: V_{CC}=+4V, V_{EE}=-4V, C_C=10pF, R_L=1kΩ, T_A=27°C, T_{A_MIN}=-40°C and T_{A_MAX}=125°C.

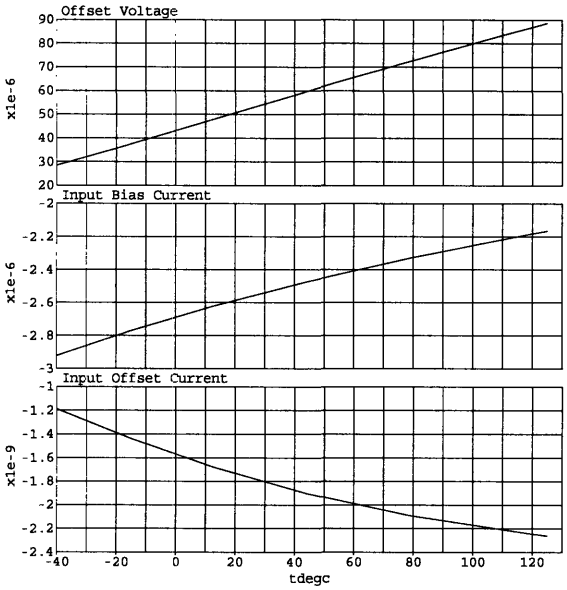

Figure 52. Input offset voltage, input bias current and input offset current vs. Temperature.

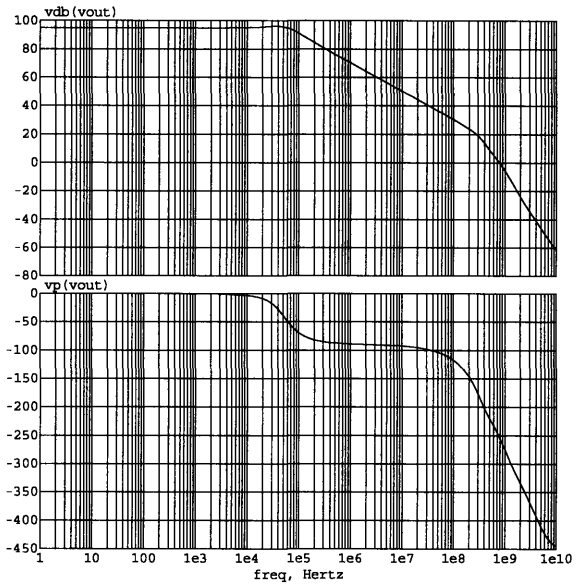

Figure 53. Uncompensated open-loop gain A(s).

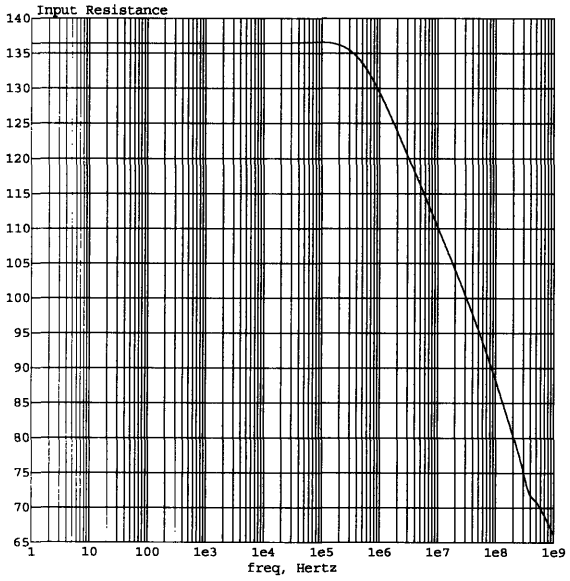

Figure 54. Input impedance vs. Frequency.

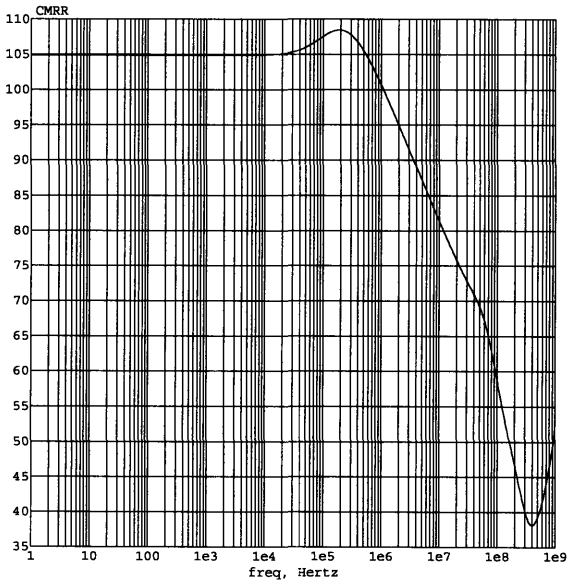

Figure 55. CMRR vs. Frequency.

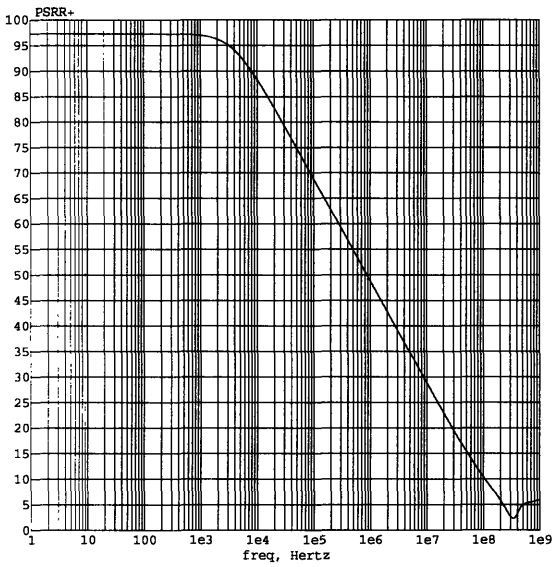

Figure 56. Positive supply PSRR vs. Frequency.

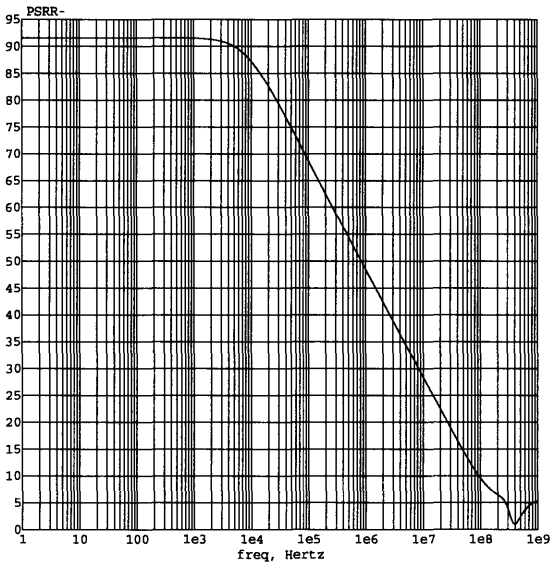

Figure 57. Negative supply PSRR vs. Frequency.

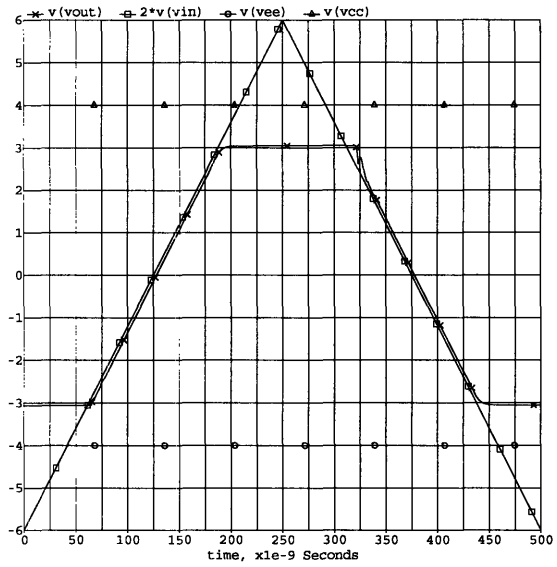

Figure 58. Output voltage range and over-drive recovery.

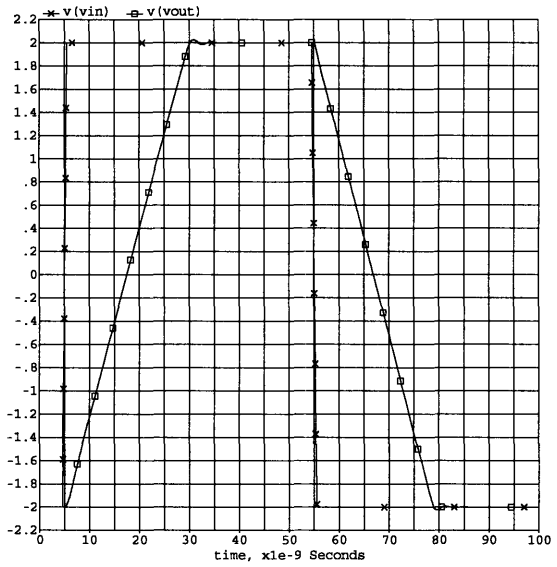

Figure 59. Large signal transient, op-amp in slew mode.

5. Schematics

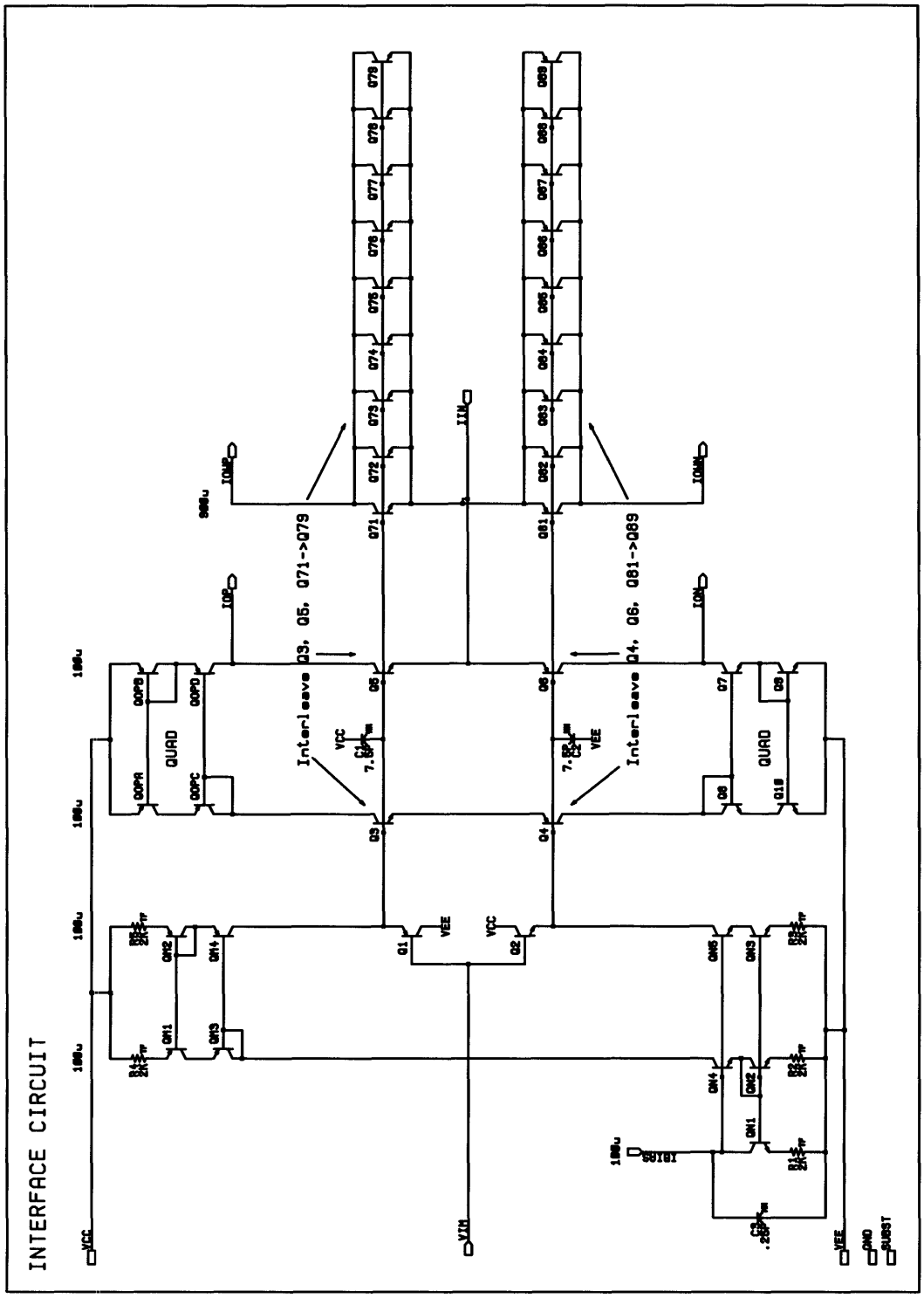

Figure 60. Schematic of the interface circuit.

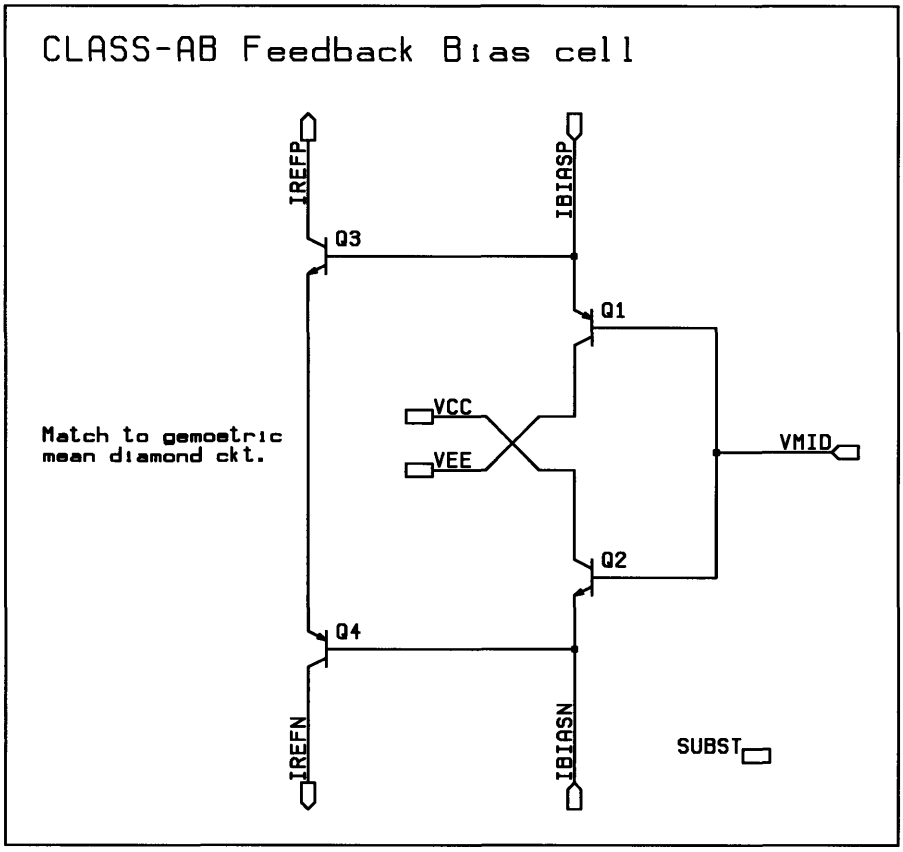

Figure 61. Schematic of the class AB reference floating current source.

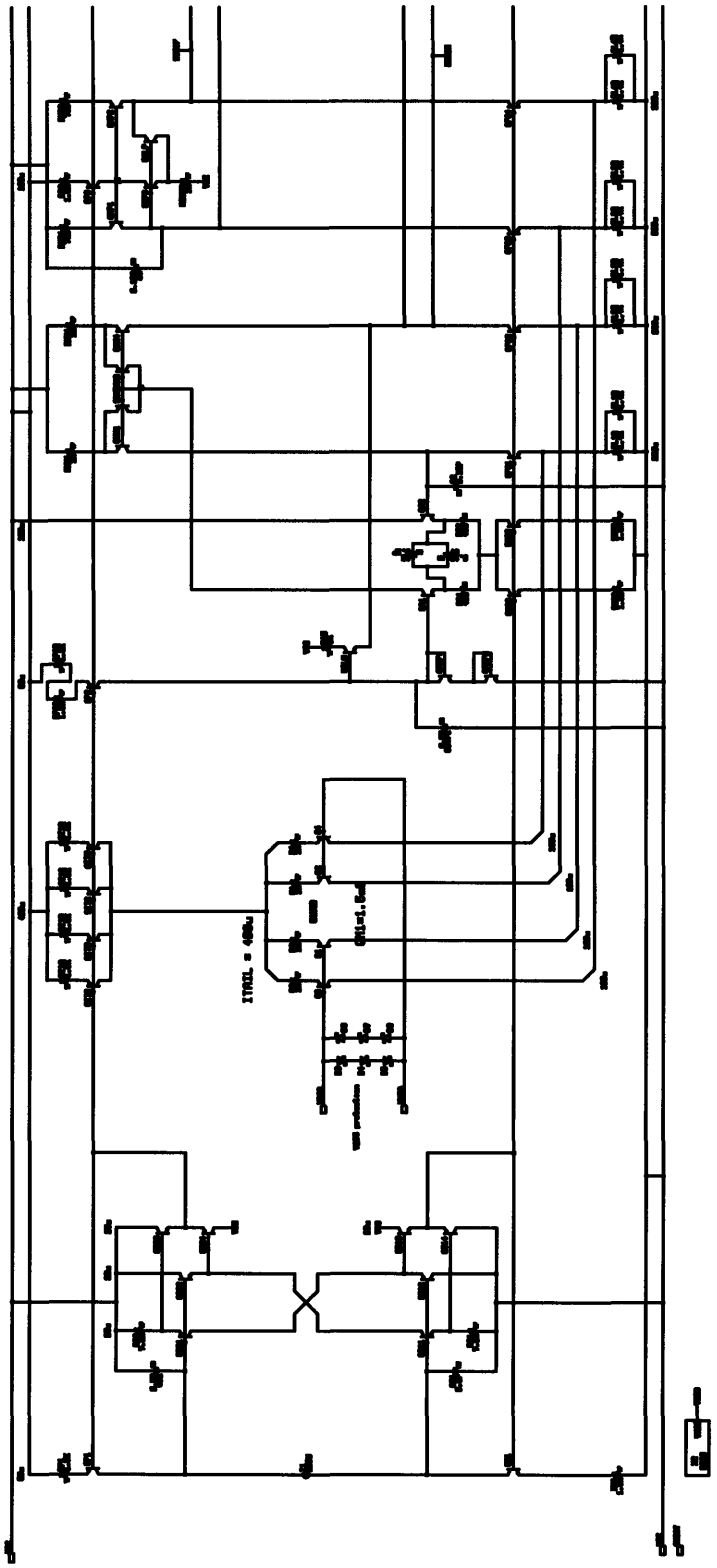

Figure 62. Left half schematic of the amplifier.

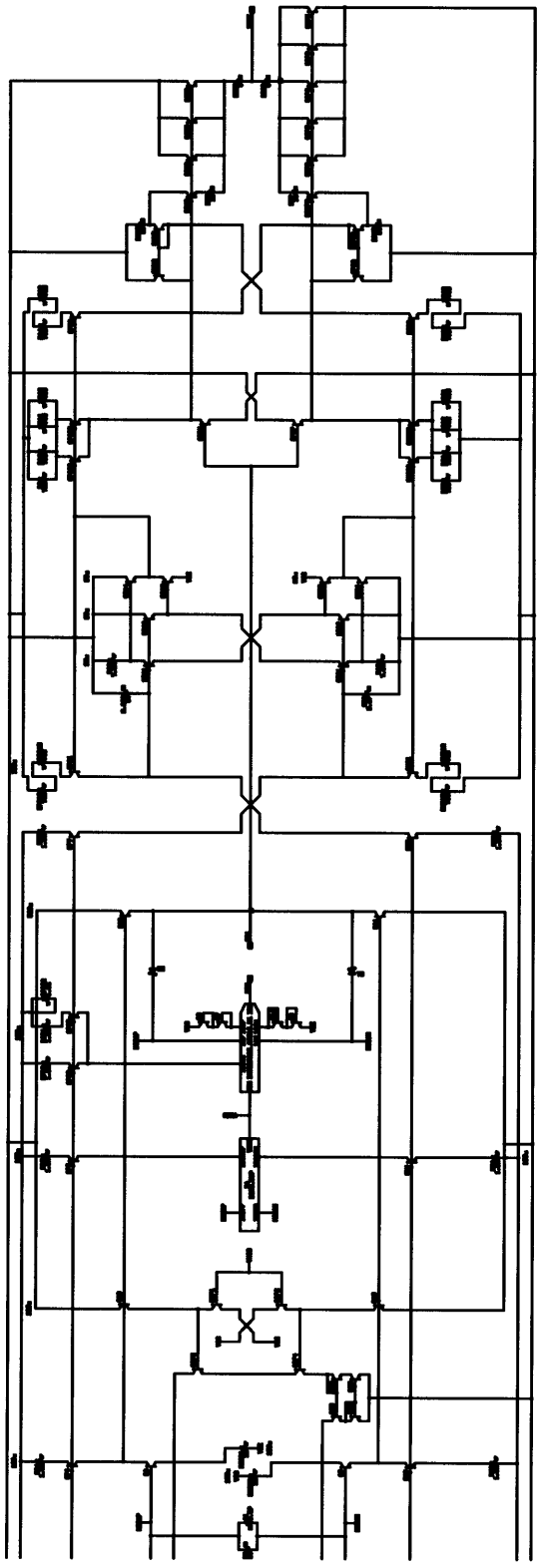

Figure 63. Right half schematic of the amplifier.

6. Conclusion

A high-speed, general purpose externally compensated operational amplifier has been designed and simulated. Its static performance is quite comparable to commercial units, while its dynamic performance is far superior. The latter is due to the external compensation capability that the op-amp possesses allowing the user to optimize the amplifier's dynamics to a given application.

The proposed amplifier includes a novel interface circuit which moves the limitations in performance from compensation component availability and board parasitics to the performance of the interface itself. Since a current mode stage is used to implement the interface, a very high-bandwidth is achieved in this block.

Future work will include designing the bias circuit and laying out the entire amplifier. After that, it will hopefully be fabricated at Analog Devices' Wilmington foundry.

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