A Silicon Current Sensing Amplifier and Organic Imager for an Optical Feedback OLED Display

by
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B.S., Massachusetts Institute of Technology (2004)

Submitted to the
Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of
Master of Engineering in Electrical Engineering and Computer Science
at the
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
February 2006

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Abstract

Organic LEDs (OLEDs) have the potential to be used to build thin, flexible cost-effective displays. Currently, the primary drawback to their usage lies in the difficulty of producing OLEDs that emit light at a constant and predictable brightness over their lifetime. This leads to a non-uniform brightness and a limited effective lifetime in an OLED display. The solution presented herein uses organic photodetectors on a per-pixel basis using a column-parallel architecture for optical feedback to control the desired luminosity. The integrated silicon control chip and organic imager array, together with the OLED array, form a stable display. In particular, this thesis focuses on the design and fabrication of the Current Sensing Amplifier circuits for the organic imager array in an optical feedback OLED display. The results demonstrate functionality of the high gain Current Sensing Amplifier with a measured transimpedance gain of 496 MΩ using a clock frequency of 20kHz, 50% duty cycle, and a Programmable Gain setting of 5$\times$.

Thesis Supervisor: Charles G. Sodini
Title: Professor

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Acknowledgments

First, I would like to thank my project advisors Prof. Charles G. Sodini and Prof. Vladimir Bulović for their support, guidance, and direction, without which this work would be impossible.

Next, I would like to thank my academic advisor Prof. Dennis Freeman for his advice through the years.

I would also like to thank Peter Holloway and National Semiconductor for their help in realizing our silicon chip design.

In addition, I thank Ioannis Kymissis, Kevin Ryu, and Jennifer Yu for their help and cooperation in my organic investigations.

Furthermore, much gratitude go to my parents, Quincy and Kathy Lin, and my sister, Janice Lin, for their continued encouragement and support.

Finally, I thank my friends and the people of the Sodini group and Lee group who have also helped me a great deal along the way, and made my experience most enjoyable.

This work was funded in part by C2S2, the MARCO Focus Center for Circuit & System Solution (C2S2), under MARCO contract 2003-CT-888.

Contents

List of Figures

Chapter 1

Introduction

Electronics, small or large, have shown a steady evolutionary trend - the integration of ever more features and more complex functions onto a single device. As devices are packed with functionality, the display becomes an absolutely essential part of all modern electronics. It is one of the most intuitive and user-friendly interfaces for navigating through features, and communicating and soliciting information. Already, many electronics are beginning to use multiple, high-resolution, color displays; and devices previously without displays are now finding them a must-have feature.

In the near future, displays of various sizes, resolutions, and purposes will be found in all aspects of our daily lives; displays will be pervasive and ubiquitous. Not only will our electronics be equipped with displays, but our environments will also be complemented by displays. Billboards will change from static posters to dynamic, flashy displays; and wall paintings will transform from oil and canvas to ever-changing digital scenery and photographs. Displays will be omnipresent, in many different shapes and forms, serving many different purposes. Thus, only a versatile display suitable for a multitude of applications can facilitate and aid the coming of the Display Era.

OLED displays are the versatile display of choice by many research institutions and corporations[1]. OLED display technology has been given much attention as a promising alternative to modern displays, since it has the potential to scale across a

wide range of dimensions, deliver supreme resolution and color, and achieve very high power efficiencies[2, 3]. In addition, unlike liquid-crystal displays (LCDs), plasma displays, and cathode-ray tube displays (CRTs), OLED displays can be made paper-thin and paper-light, and cost-effectively fabricated. Thus, OLED displays are emerging as the fittest in the evolution of displays.

However, current processes find it hard to produce accurate, or even precise, OLED light-output vs. current characteristics. In other words, a specific light-output vs. current characteristic, or even a consistent light-output vs. current characteristic, is hard to achieve from batch to batch, device to device. In addition, OLED light-output vs. current characteristics degrade over time and use, and are dependent on too many external parameters to be reliably predictable[4]. Thus, these two issues of non-uniformity and degradation must first be overcome before OLEDs and OLED displays can be widely commercialized.

1.1 Thesis Objectives and Motivation

This thesis proposes the design of an optical feedback OLED display. The optical feedback solution aims to solve the two greatest flaws in OLED display technology, addressing the problems of OLED device non-uniformity and performance degradation. The work of Eko Lisuwandi and Matthew Powell is furthered in this thesis by the design of an integrated, all-organic display panel and an integrated silicon feedback control chip[5, 3]. The integrated organic display will consist of both light emitting (OLED) and light sensing (organic photodetector) devices. The integrated silicon chip will use the organic photodetector output as a feedback signal to better control the OLEDs despite non-idealities in the OLED light-output vs. current characteristics.

The optical feedback solution presented in this thesis aims to further OLED displays as an appealing display candidate of the future. By overcoming the problems intrinsic to the organics in a robust manner, the proposed optical feedback solu-

tion fundamentally solves many pixel-level and display-level problems to deliver unprecedented performance and catalyze the widespread commercialization of OLED displays.

1.2 Thesis Organization

The thesis is organized generally according to the signal pathway of the optical feedback OLED display. First, Chapter 2 provides a background discussion of OLEDs and OLED displays, and their advantages and disadvantages. Chapter 3 introduces the optical feedback solution and analyzes it from the system level. Chapter 4 describes the organics and explores a suitable design for the organic photodetector array. Chapter 5 continues to discuss the silicon current sensing amplifier, which processes the organic outputs, and its detailed circuit design. The entire silicon chip is overviewed in Chapter 6; and Chapter 7 presents simulation and measurement results. Finally, the thesis concludes in Chapter 8 and suggests other potential applications of the developed solution.

This thesis focuses on the silicon current sensing amplifier for the organic imager, and discusses potential organic imager array designs. The silicon summing junction and compensator for the optical feedback OLED display is discussed in Lamba's thesis[6].

Chapter 2

Background

2.1 OLEDs and OLED Displays

Research on organic optoelectronics over the past two decades has advanced OLEDs significantly to render them suitable for a display technology. Power efficiencies have increased from 0.1-1 lm/W to 10-100 lm/W[7]. And new topologies, techniques, and organic materials have allowed OLEDs to become much more stable. Already, there are a few big corporations that have begun to commercialize the OLED display technology[1].

OLED display technology has a lot to offer. Instead of filtering light like LCDs, OLEDs emit light. Due to this fundamental difference, OLED display technology offers increased contrast, faster response times, much greater power efficiencies, and significantly lower power consumption[7]. In addition, as an emissive technology, OLED displays do not need a backlight, making them light weight, smaller and thinner[3, 8]. Lastly, OLEDs can be deposited on plastics, allowing cheap, scalable fabrication and even flexible displays[8, 4]. These advantages and features are just a small subset of the whole. Unfortunately, OLED technology is still in its relative infancy, and two main problems limit OLED performance.

2.2 Problem Statement

First, OLED light output characteristics are non-linear and hard to match from OLED to OLED[2, 8]. This means that OLEDs in an OLED display will shine at different brightness even though they are driven by the same current. Such non-uniformity in OLED characteristics causes non-uniformity in brightness on the OLED display, resulting in poor visual performance and a low manufacturability yield.

Second, OLEDs degrade over time and use, meaning the quantum efficiency decreases and brightness decreases for a given drive current[7, 9, 8, 4]. Since the OLEDs degrade at varying rates dependent upon use and environment, the OLED display will have an unacceptably non-uniform brightness after an initial period of use. In addition, OLEDs degrading will cause the aggregate display to grow dimmer and dimmer with time. Text and images may become harder to see as contrast is also lost. Thus, these problems will render the display useless. This problem of degradation severely limits the useful lifetime of the OLED display. For example, the human eye is highly sensitive to differences in brightness and contrast as little as 1%[8]. Setting a degradation tolerance of 5%, an $Ir(ppy)_3$ OLED display can operate for approximately 2000 hours driven with constant current. The initial intensity is 200 cd/m^2, and after only 2000 hours, the intensity degrades to only 190cd/m^2 (see Figure 2-1)[10]. After 2000 hours, the light intensity drops below the threshold and the display is considered unacceptable.

Since both these issues deal with non-ideal brightness (non-uniform and degrading), a single solution is possible to fix both these problems. By employing integrated optical feedback for an OLED display, the optical feedback can compensate for any inaccuracies in brightness, whether it's non-uniformity in fabrication or degradation in efficiency. The optical feedback OLED display will have integrated photodetectors in the organic display and a silicon control chip for feedback functions.

As long as the photodetector is uniform in fabrication and doesn't degrade significantly, the optical feedback will cause the OLED display to produce images of

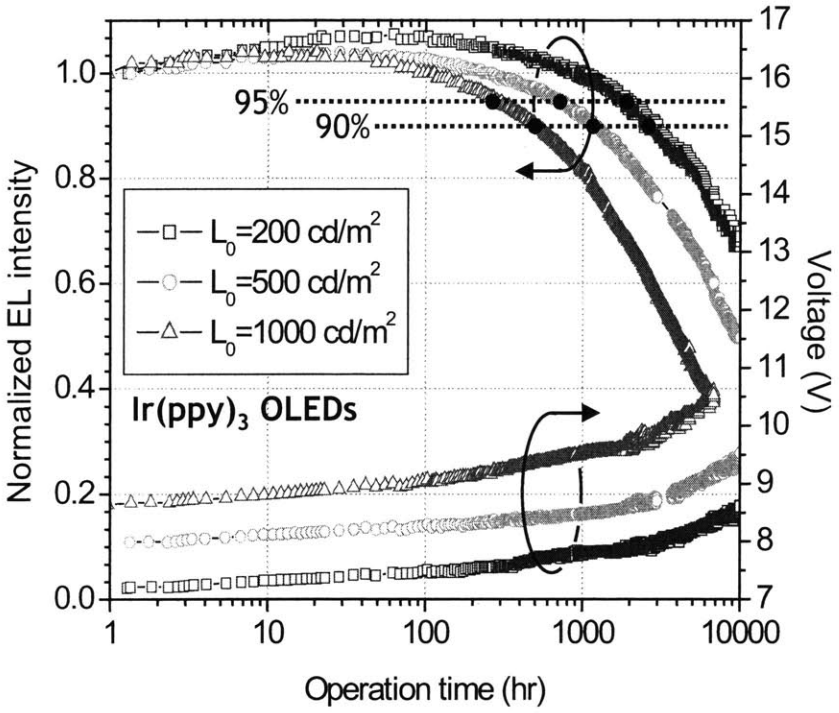


Figure 2-1: OLED EL Efficiency Over Time. The OLEDs are $Ir(ppy)_3$ phosphorescent OLEDs. The top curves show curves driven at constant current with normalized EL intensities (left axis). The bottom curves show the increase in voltage in order to drive the OLEDs at constant brightness (right axis).

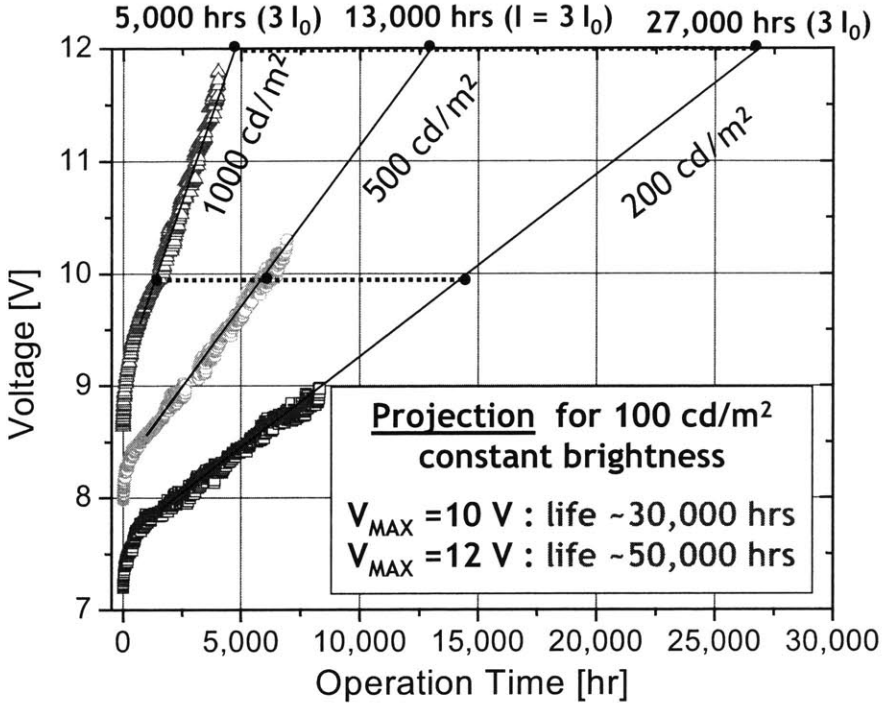


Figure 2-2: Voltage Increase Over Time for Constant Brightness.

the desired brightness without distortions in contrast. The photodetector design is discussed in Chapter 4. Figure 2-2 shows the projected increase in display lifetime by compensating for decreasing efficiency (by increasing voltage). Looking at the 200 cd/m^2 curve and assuming the display can sustain a maximum voltage of 10V, optical feedback has the potential to run constant brightness OLEDs up to 14,000 hours. This is a lifetime increase by 600%[4].

To summarize, OLEDs have two problems. First, there is non-uniformity in fabrication. Second, there is degradation that is inconsistent and unpredictable. This results in two distinct, yet related, problems from the user perspective. First, the user will observe $non-uniform\ brightness$ in the display due to non-uniformity in fabrication and degradation that varies from pixel to pixel. Second, the user will observe a *gradual dimming* in the overall display brightness due to degradation. These problems severely limit the performance and useful lifetime of the OLED display and are a major obstacle in the widespread commercialization of OLED displays. As these

problems are closely related, they can be solved via a single, well-designed robust solution - the optical feedback OLED display.

2.3 Prior Work

Eko Lisuwandi of MIT first began the optical feedback solution design in his Master's thesis. His research explored and confirmed the feasibility of an optical feedback solution to stabilize the brightness of an OLED display. Lisuwandi built a discrete version of the feedback circuitry for a 5 by 5 LED array. An external camera was used as a photo imager for the optical feedback. His results proved that the optical feedback design is a promising solution for OLED displays[5].

Matthew R. Powell continued Lisuwandi's work in designing and revising an integrated version of the circuit. The design was an all-silicon design except for the OLEDs, which were deposited on the silicon chip in a separate organic process. The photodetectors (silicon photodiodes) and the feedback circuits were integrated with the addressing and driver circuits on a single chip. The chip features a 128 by 16 pixel array in a column-parallel architecture (1 feedback loop per column)[3]. However, this approach fundamentally limits the OLED display size to the silicon die size, which is usually only a few millimeters on each side.

As a next step, this thesis will investigate an all-organic OLED display working with an integrated silicon control chip. The all-organic display will contain both light-emitting OLEDs and light-sensing photodetectors; the silicon control chip will then perform the feedback functions to properly drive the display. This calls for a new organic display design and organic photodetector design (see Chapter 4) and a new silicon chip design for signal processing, feedback, and compensation (see Chapter 3 and Chapter 5).

Chapter 3

Optical Feedback OLED Display

The optical feedback solution proposed herein aims to solve the two main problems limiting the performance and lifetime of OLED displays: 1) non-uniform OLED brightness across the display, and 2) gradual dimming across the overall display. As mentioned previously in Chapter 2, these two problems are caused by the non-uniformity of OLED fabrication and the inherent degradation of the individual OLED pixels over use. These display problems can be overcome using optical feedback as a means of correcting and compensating the OLED non-idealities[5].

3.1 Optical Feedback System Overview

Figure 3-1 shows one complete feedback loop. The OLED Pixel block takes in a drive voltage, and the OLED outputs light at varying intensities. The Organic Photodetector senses the OLED brightness and outputs a signal current representative of the detected intensity. The Current Sensing Amplifier converts and amplifies the signal current to an appropriate voltage, which is then compared to the desired brightness, represented as a voltage from a display adaptor. Lastly, the Compensator offers stability compensation by introducing a dominant pole in the overall system. And thus, using feedback, the actual brightness can be adjusted to match the desired brightness for each pixel, regardless of the uncertainty in the degraded OLED characteristics.

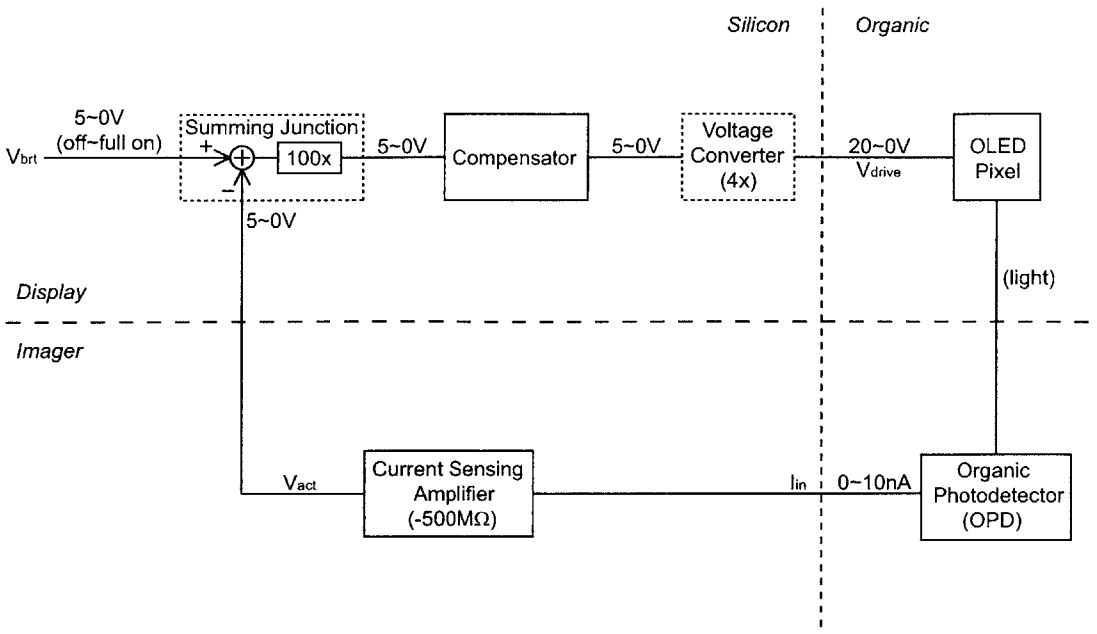


Figure 3-1: Feedback Block Diagram for an Optical Feedback OLED Display.

Of course, for this optical feedback solution to work, the organic photodetector must be uniform and resistant to the degradation effects that plague the OLED. Organic photoconductors are already commonly used in photocopier drums and are relatively stable[2]; thus they were chosen over photodiodes for use in the organic photodetector.

The optical feedback solution can be split into left and right halves (see Figure 3-1). The left half is all fabricated in integrated silicon, while the right half can be fabricated in integrated organics. The silicon chip uses column parallel architecture (see Figure 3-2), meaning there is only one feedback loop per column. For a display with m columns and n rows, there are only m silicon circuits, which are time-shared by the n rows. As each row in the organics is selected, the m pixels in that row are connected to the m circuits in the silicon to perform the feedback. Then another row is selected to be connected to the silicon circuits for feedback, and so forth. A column parallel architecture (as opposed to per-pixel feedback circuitry) significantly reduces circuit area as well as power consumption. Another benefit is that the silicon and

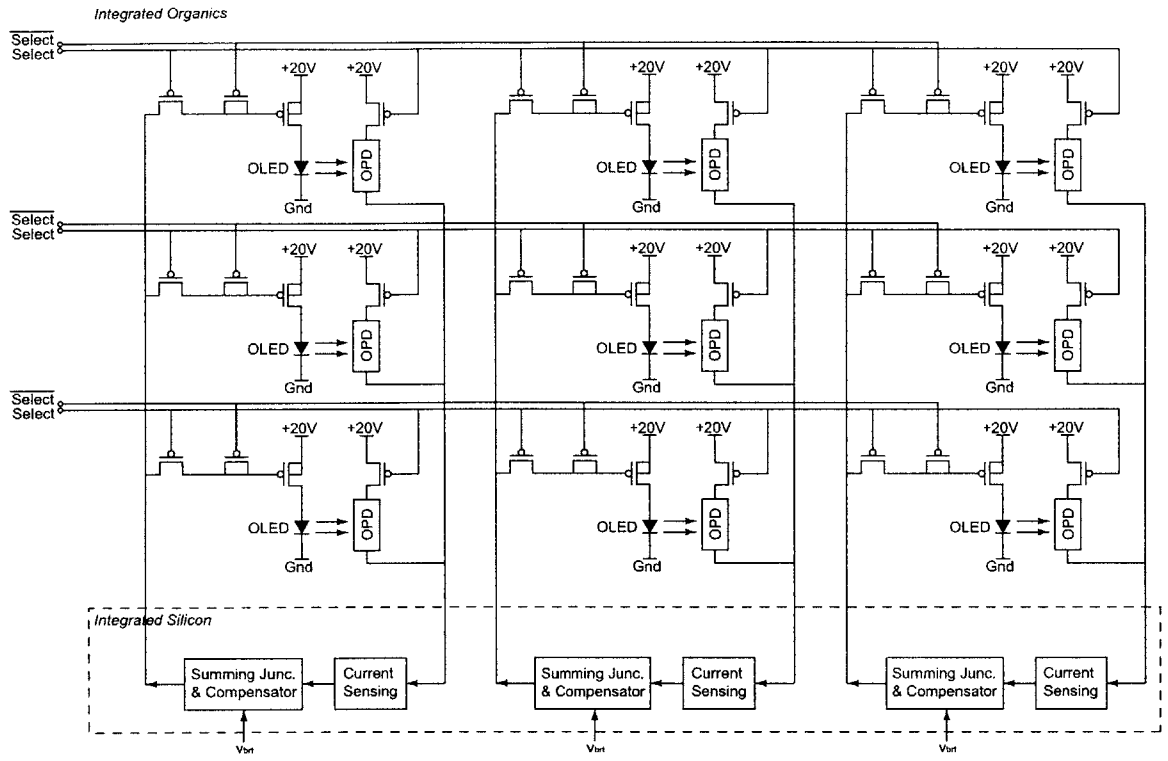


Figure 3-2: Sample Display Illustrating the Column Parallel Architecture.

organics can be completely separated, which allows for display scalability and easier, cheaper fabrication.

Additionally, the system can be split into top and bottom halves (see Figure 3-1). The top half is essentially a display, consisting of the pixel driver and the pixel. The bottom half is essentially an imager, consisting of the image sensor and its signal processing circuitry. An advantage of such symmetry is that the solution can be divided into two independent devices (display and imager) for independent application in other systems. This chapter proceeds to discuss the feedback system and its components. The next few chapters focus on the imager half of the system, beginning with a discussion of the organic imager array and then the Current Sensing Amplifier. For more details on the display half, please refer Kartik Lamba's thesis[6].

3.2 System Specifications

3.2.1 Feedback Specifications

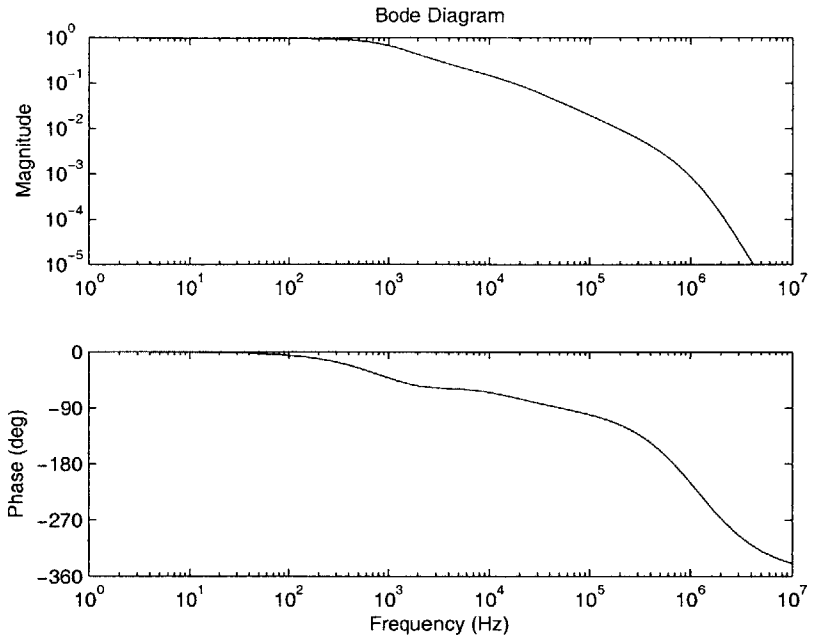
To determine the basic specifications, the system must be analyzed using feedback theory. The starting specifications of the overall system are as follows:

1. The system must be stable, with a closed-loop dominant pole at 1kHz and 60 degrees of phase margin.

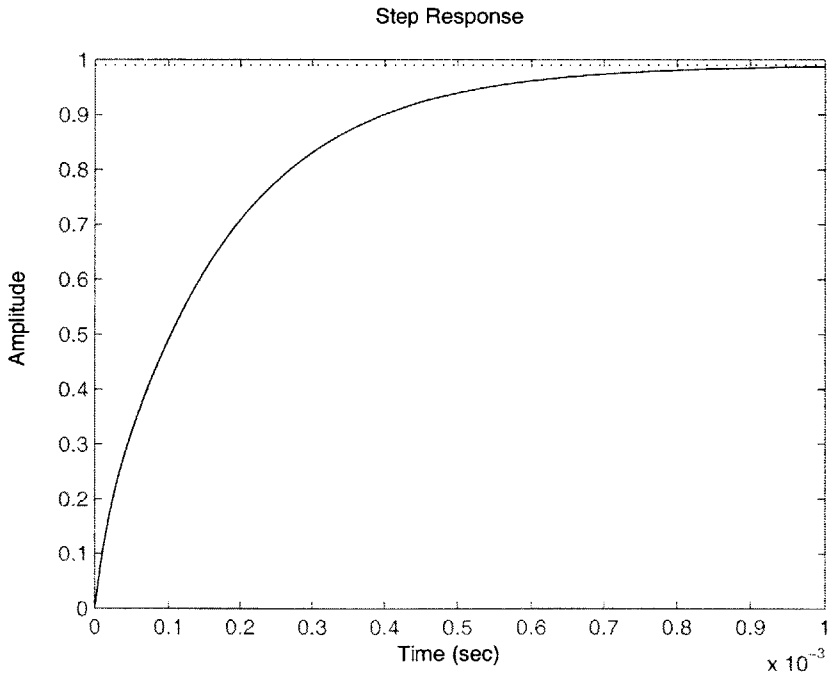
2. The dc system error (desired brightness - actual brightness) must be no greater than 1%.

Using Black's formula [11] and a few other feedback concepts, it can be shown that a loop gain of 100 is necessary to obtain a dc error of 1%, and that the compensation pole must be implemented at 10Hz to obtain an overall system dominant pole at 1kHz (refer to Lamba's thesis for more details on pole implementation). In addition, the compensator pole must be placed in the forward path; if placed in the feedback path, a zero is introduced as well, which can cause instability by decreasing the phase margin. Furthermore, all non-dominant poles (i.e. the dominant poles of all the other blocks) must be set above 1MHz to guarantee the desired degree of stability. Lastly, negative feedback requires that there must be a net negation as the signal traverses the entire loop, and minor loop stability requires that each block is itself stable.

Figure 3-3 shows the simulation results of the feedback system. The model accounts for the 10Hz pole of the Compensator block, the 100× Summing Junction gain, and the 10kHz OLED Pixel dominant pole (see Sections 3.2.2 & 3.2.3 for more details). The pole contributions from the rest of the system are lumped together as 3 higher-order poles located at 1MHz, 1.2MHz, and 1.4MHz. Lastly, the silicon circuits are implemented as switch capacitor circuits with a 20kHz switching frequency, which introduces a zero at 5kHz. This model was simulated in MatLab to determine system stability. From Figure 3-3, the system is quite stable showing no ringing in the step



a)



b)

Figure 3-3: Feedback System Concept Closed Loop Simulation in MatLab. a) Closed Loop Bode Diagram. Dominant pole occurs at 1kHz. b) Closed Loop Step Response. 10% to 90% rise time is 0.37ms; settling time to within 1% of final value is 0.78ms.

response. The step response also identifies the dc system error of 1% mentioned in above.

Next, the high-level specifications for each of the blocks in Figure 3-1 are defined.

3.2.2 Organic Specifications

Most of the specifications of the organics are given, and do not need to be set. An understanding of the specifications of the organic blocks will aid in the design of the interacting silicon blocks. Thus this section briefly describes the organic characteristics.

There is much uncertainty in the organic components as research is currently in progress to fine-tune the many organic processes. This implies that there must be a degree of flexibility built into the silicon design to tolerate an ever-evolving, uncertain organic counterpart. As a first-order estimate, expected numbers (as set forth in the work of Ioannis Kymissis and Kevin Ryu and Jennifer Yu) are presented[2, 8, 4].

The OLED Pixel block consists of the OLED and OFET current drivers (refer to Ryu's thesis)[8]. Given an input voltage (OFET V_G) between 0V (V_{SG} = 20V = full on) and 20V (V_{SG} = 0V = off), the OLED will shine at varying intensities. Note that there is an intrinsic negative relationship between the drive voltage and brightness in the OLED Pixel design; and this will require a negation in the silicon to cancel its effect on the feedback system (see Section 3.2.3). Currently, a 20V power supply is required for the OFET driver to provide sufficient current ($\sim 30\mu$A) to the OLED[3, 4]. However, as OFET technology matures, the carrier mobility will improve, allowing the OFET to deliver more current. A 5V V_{SG} will be able to supply enough current to drive the OLED, and a 5V power supply (instead of a 20V supply) will be sufficient. Until then, an external, tunable voltage converter is used to convert the silicon's 5V drive voltage to a 20V scale. This block is a 4× linear gain block, which can be removed once organic technology has matured to allow for a 5V supply. In terms of frequency, an estimated OLED Pixel pole occurs at 10kHz due to the large gate capacitance of the driving OFET. But the precise location of this pole will

depend on the final design of the OLED Pixel (also see Ryu's thesis)[8].

The Organic Photodetector (OPD) senses the OLED brightness, and outputs a current signal between 0A (no light) and 10nA (full brightness). 10nA (the maximum output signal) is an estimate and may change depending on the final Organic Photodetector design as well as the organic processing, and will likely fall between 5nA and 20nA. This block is extremely fast, and its pole is negligible compared to the others.

3.2.3 Silicon Specifications

With the input-output characteristics of the organics understood, the specifications of the silicon can be set.

The Current Sensing Amplifier (CSA), the signal processing circuitry for the Organic Photodetector, takes the signal current from the OPD and amplifies it to a 0-5V range. A negation is required in the Current Sensing Amplifier to achieve an overall negation in the feedback loop (see Figure 3-4). There is a negation in the Summing Junction (so it implements a subtraction) and there is an intrinsic negation in the organics (see Section 3.2.2 and Figure 3-4); thus, a third negation is necessary to cancel out the organic negation, which is implemented in the CSA. Hence, for an input of 0nA, the CSA output is 5V; and for an input of 10nA, the output is 0V. In summary, the Current Sensing Amplifier has an inverting gain of 500 MΩ.

The Summing Junction must subtract the actual brightness, V_{act}, from the desired brightness, V_{brt}. V_{brt} will be supplied by a computer or a display adaptor, and ranges from 0-5V. To be consistent with the organics, 5V signifies "pixel off" while 0V signifies "pixel full on". Additionally, there must be a gain of 100, the required loop gain mentioned previously.

Next the Compensator block takes in 0-5V (5V=off) and outputs 0-5V (gain of 1). A dominant pole is implemented at 10Hz, as required by the feedback system specifications (see Section 3.2.1). The output of this block is then passed into the voltage converter, which then provides the necessary 20V range voltage drive for the

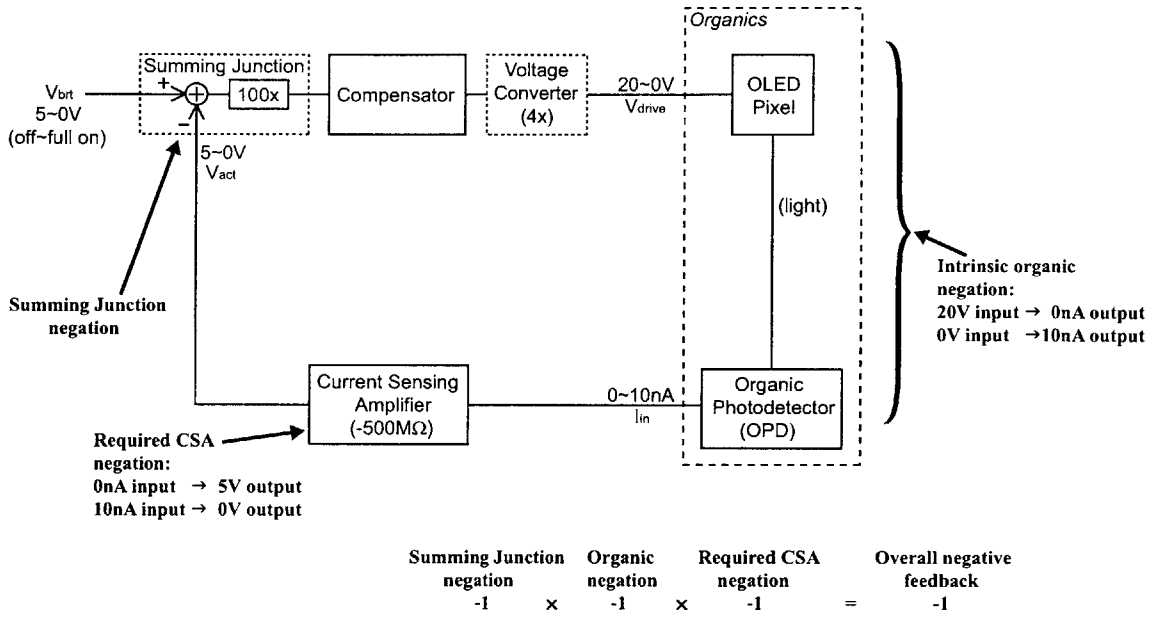


Figure 3-4: Illustration of Inversions in the Optical Feedback OLED Display System.

OLED pixel. When the OFET mobility is sufficiently improved, the converter will be removed, and the Compensator block will directly drive the OLED Pixel (see Section 3.2.2).

Due to leakage currents in the organic photodetectors, the organics can only provide current-sensing accuracy to about 1%[2]. As such, the organics are the limiting factor in the overall system accuracy. Thus, the silicon circuits need only be accurate to 1% as well.

In addition, feedback does not require linear blocks. Though linearity is not a requirement in the silicon blocks, it is preferred because it helps guarantee that the dc system error is no more than 1% for any input. If the blocks are non-linear, the error is no more than 1% for some inputs, but not necessarily all inputs, and the feedback system will perform poorly in certain regions known as low gain regions. Thus we make linearity a requirement for all silicon blocks.

Since there is uncertainty in the output range of the OPD, a hardwired, precise gain in the silicon blocks is inappropriate. The silicon power rails limit the voltages

to 0-5V, so too much gain will cause the signal to be truncated at 0V and 5V. This reduces the dynamic range of the system. On the other hand, too little gain does not reduce the dynamic range of the system, but reduces the resolution of the output. And thus what is required is a continuously, tunable gain in the feedback path that can accommodate any range of OPD signal currents to produce a precise 0-5V output from the CSA to the Summing Junction. Such a tunable gain is implemented in the first stage of the Current Sensing Amplifier and described in Section 5.1.1.

3.2.4 Summary of Specifications

Figure 3-5 summarizes the feedback system, organic, silicon, and external voltage converter specifications discussed in this chapter.

Feedback System Specs

DC Error	≤1%
Loop Gain	100
Stability	Stable; ≥ 60° phase margin; All minor loops stable
3db Frequency	1kHz (closed loop)

Organic Specs (Given)

Input Range	0-20V
Output Range	0-10nA
Gain	Roughly 5×10^{-10} Siemens
Accuracy	Limited to ~1%
3db Frequency	10kHz
Negation	Intrinsic signal inversion

External Voltage Converter Specs

Input Range	0-5V
Output Range	0-20V
Gain	4
Linearity	1% linearity for inputs from 0-5V

Silicon Specs

Current Sensing Amplifier	
Input Range	0-10nA
Output Range	0-5V
Gain	500 million Ohms, tunable
Accuracy	~1%
3db Frequency	≥1MHz
Negation	Inversion required
Linearity	1% linearity for inputs from 0-10nA
Summing Junction	
Input Range	0-5V, both inputs
Output Range	0-5V
Gain	100
Accuracy	~1%
3db Frequency	≥1MHz
Negation	Feedback signal inversion
Linearity	1% linearity for entire input range
Compensator	
Input Range	0-5V
Output Range	0-5V
Gain	1
Accuracy	~1%
3db Frequency	10Hz open loop
Negation	none
Linearity	1% linearity for inputs from 0-5V

Figure 3-5: Table of System Specifications.

Chapter 4

Organic Imager Array Design

The organic imager array design is still very much subject to change, as organic technology continues to mature. This chapter details the original array design, some observed problems, and a proposed new design to solve these issues.

4.1 Original Design

The original prototype imager array design consists of a column-parallel 64×64 array of organic photodetectors (OPD), which are photoconductors with organic FET switches (see Figure 3-2 and Figure 4-1). Competing designs use an organic photodiode instead of an organic photoconductor. However, organic photodiodes suffer from the same degradation effects that severely affect OLEDs[12]. On the other hand, organic photoconductors made from titanyl pthalalocyanine have already been widely used in photocopier drums without degrading over use or time[2]. Furthermore, the low nA current levels through the photoconductor (compared to μAs through a photodiode) significantly decrease any degradation effects resulting from use. Thus, the titanyl pthalalocyanine photoconductor was chosen over a photodiode for this design.

The photoconductor modulates the output current signal depending on the OLED brightness, and the OFET switches select which row of sensors will be used for feedback in the silicon circuits. For optimal performance, the OFETs should act as ideal

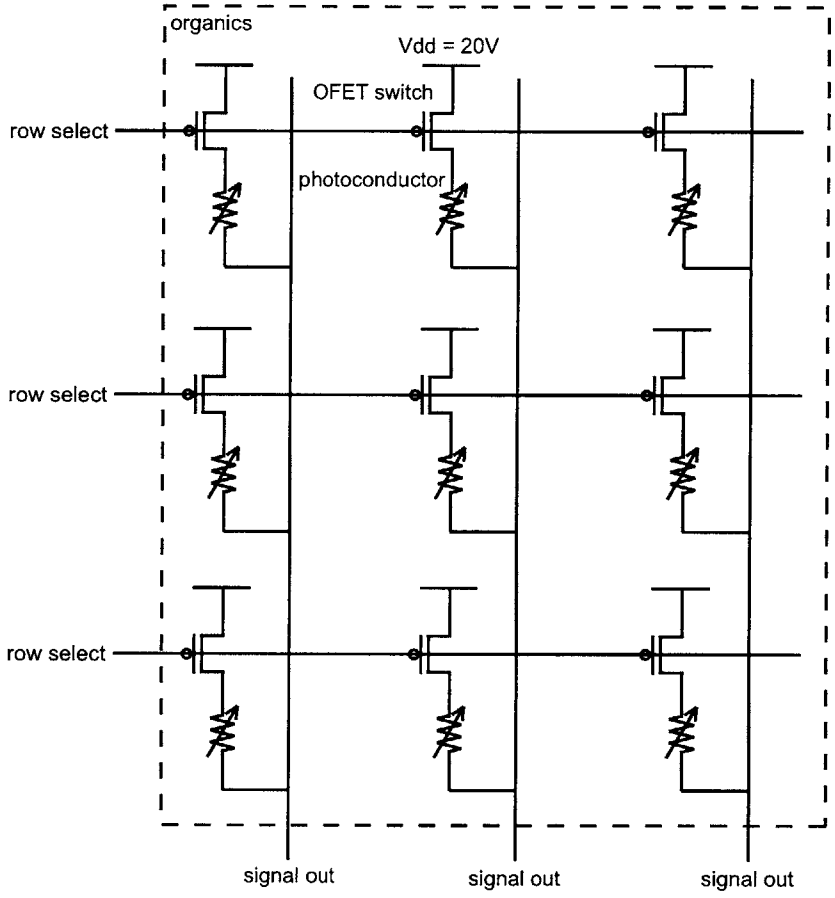


Figure 4-1: Original Organic Photodetector Array Design.

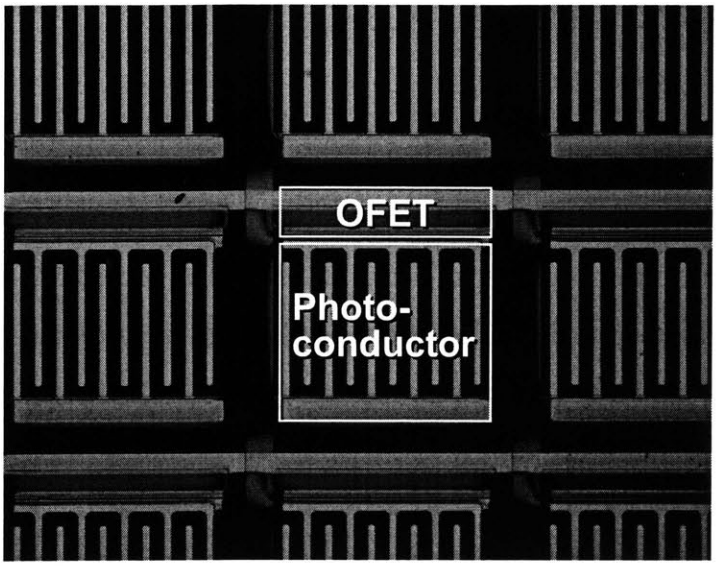


Figure 4-2: Die Photo of Current Organic Photodetector Structure.

switches. Due to the limited performance of the OFETs, the switch approximation is only valid if the following condition is met:

$$R_{photoconductor} \gg R_{OFET,on} \tag{4.1}$$

Condition 4.1 makes the OFET switch transparent to the photoconductor when the row is selected so that the photoconductor can properly modulate the output current. For the same reason, the input impedance of the next stage (Current Sensing Amplifier, see Figure 3-1) must also be small, several orders of magnitude less than the photoconductor resistance.

Currently, the photoconductor resistance is designed to range from about 2GΩ $\sim$ 20GΩ [2], and the OFET is designed to have an on-resistance of 2MΩ. This corresponds to a $\frac{W}{L}$ of $\frac{1000\mu m}{10\mu m}$ in our current organic technology.

4.2 Leakage Current Issues

The original design was tested and a large leakage current relative to the signal range was observed; and the signal was barely discernible from the background leakage. Thus, a good metric to measure the performance of the organic photodetector array is the "signal-to-leakage ratio". The "signal-to-leakage ratio" is the ratio of the maximum signal current to the maximum leakage current. This metric is unitless; and the larger it is, the more accurately the output represents the signal of interest.

With a small signal-to-leakage ratio, the leakage can easily swamp the output and make the signal indiscernible. The contributing factors to the observed low ratio are both a small signal and large leakage. The photoconductor material intrinsically has a large resistance, on the order of several gigaOhms; this implies a very small signal current (nAs). The resistance can be adjusted by changing the width and/or length of the device, or by using another device structure; however, wafer size constraints limit each photoconductor size to 0.15mm^2 on our prototype test panel. The largest signal (least resistance) is obtained in a horizontal device with a comb (finger) structure (see Figure 4-2)[2]. This method has already been employed and only creates a signal of up to 10nA. In order to increase the signal-to-leakage ratio substantially, the leakage must be suppressed.

Figure 4-3 illustrates the dominant leakage paths in the original Organic Photodetector array design. The third row has been selected and its output signals are the signals of interest. However, all the other non-selected rows are leaking onto the *signal out* column lines as well. The leakage is dominated by the off currents through the OFETs. Modeling the OFET leakage as a current source, the leakage current through photodetector unit in column m and row n ($n \neq$ selected row) is then

$$i_{leakage}(m,n) = OFET_{off\ current}. \tag{4.2}$$

The total leakage on column line m is then the sum of all the row contributions

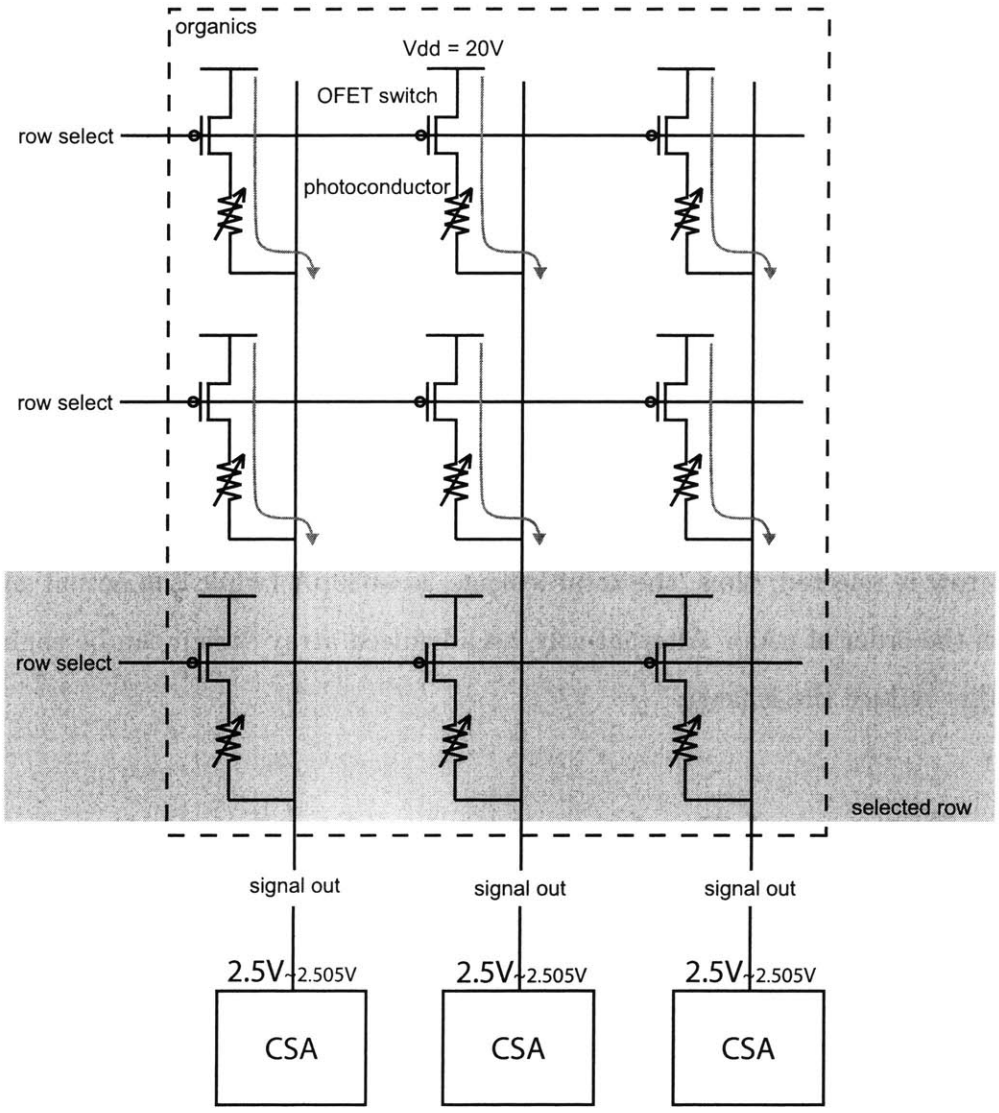


Figure 4-3: Dominant Leakage Paths in the Original Organic Photodetector Array Design. The leakage is determined mainly by the OFET switch off current and the effects of the photoconductor are negligible. The CSA forces its input voltage to 2.5~2.505V; the numbers in larger font are the numbers used for worst-case leakage current estimation.

(excluding the selected row):

$$i_{leakage}(m) = \sum_{\substack{k=0 \\ k \neq selected\ row}}^{k=n_{rows}} i_{leakage}(m,k) \approx n_{rows} \times OFET_{off\ current} \quad (4.3)$$

The power supply (V_{dd}) is 20V, and the Current Sensing Amplifier (CSA) forces the voltage of the *signal out* line to between 2.5V-2.505V [1]; thus, the worst-case OFET V_{SD} is approximated to be 17.5V (the voltage drop across the photoconductor is negligible).

In this case, the OFET off current (with $\frac{W}{L}=\frac{1000\mu m}{10\mu m}$, V_{SG}=0V, and V_{SD}=17.5V) is about 10pA, and the leakage through a single photodetector device can be as large as 10pA. Since there are 64 rows in this array, 63 rows are each leaking 10pA while only 1 row is selected; thus, the total leakage is ~630pA (while the actual signal is only on the order of nAs). Alternatively, an advanced array design can be engineered to further reduce the leakage.

4.3 Proposed Designs

Several organic imager array designs were explored to help reduce the leakage currents.

4.3.1 Improved Switches

One way to decrease the leakage is to use better switches with substantially lower off currents; perhaps these switches can be done in silicon. Figure 4-4 shows such a design. The switches in each photodetector unit are pulled out and implemented in silicon because silicon switches provide better isolation from the power rail, thereby reducing leakage through the FET switch by an estimated factor of 10,000. But

[1]The Current Sensing Amplifier has a closed loop op amp in the input stage. This op amp will coerce the *signal out* line (*Iin* in Figure 3-1, *signal out* in Figure 4-3) to a voltage of V_{CM}=2.5V. However, due to op amp input offsets, this voltage may actually range over 5mV (say from 2.5V~2.505V) from CSA to CSA, and will not be exactly at 2.5V. See Section 5.1.

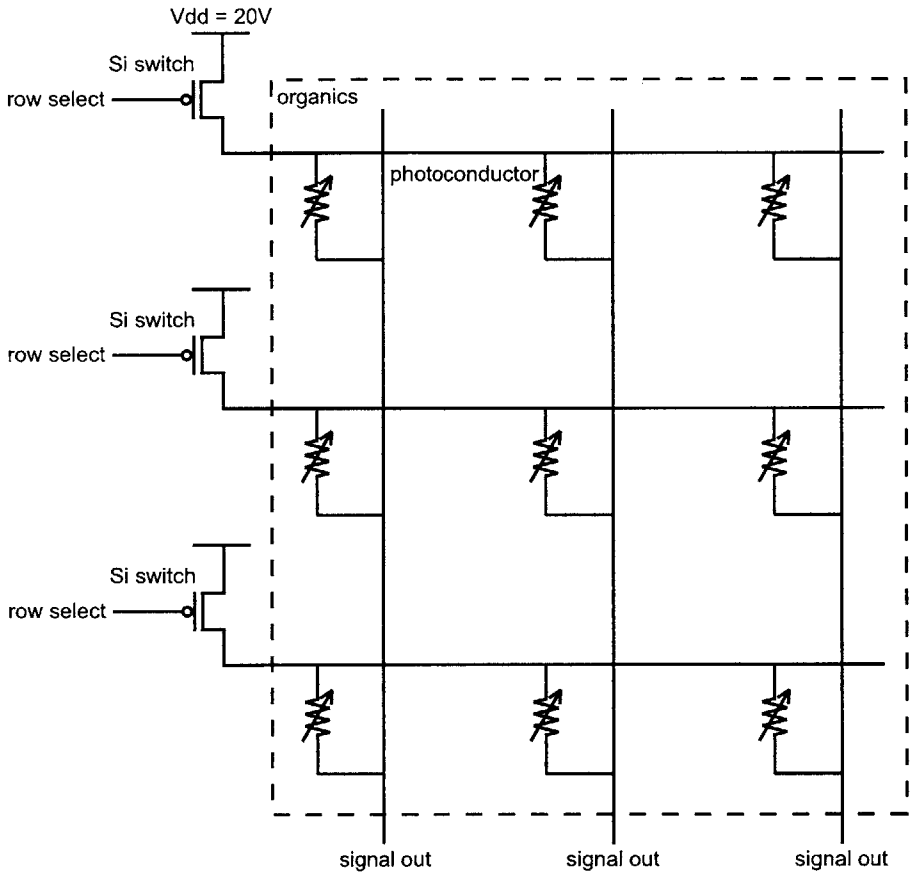


Figure 4-4: An Organic Photodetector Array Design with Silicon Switches.

this design also introduces a new type of leakage - column coupled leakage. In this design, all photodetectors in the same row are coupled together. This means that although the row is off, current can back flow from the silicon chip, back through a photoconductor, and then down through another photoconductor (see Figure 4-5). A quick analysis will identify the leakage contribution by the column coupling effect.

In Figure 4-5, leakage through the silicon switches can be considered negligible. Instead, the dominant leakage path is now leakage from one column (or several columns) to another (see Figure 4-5). As previously noted in Section 4.2, the CSA forces the

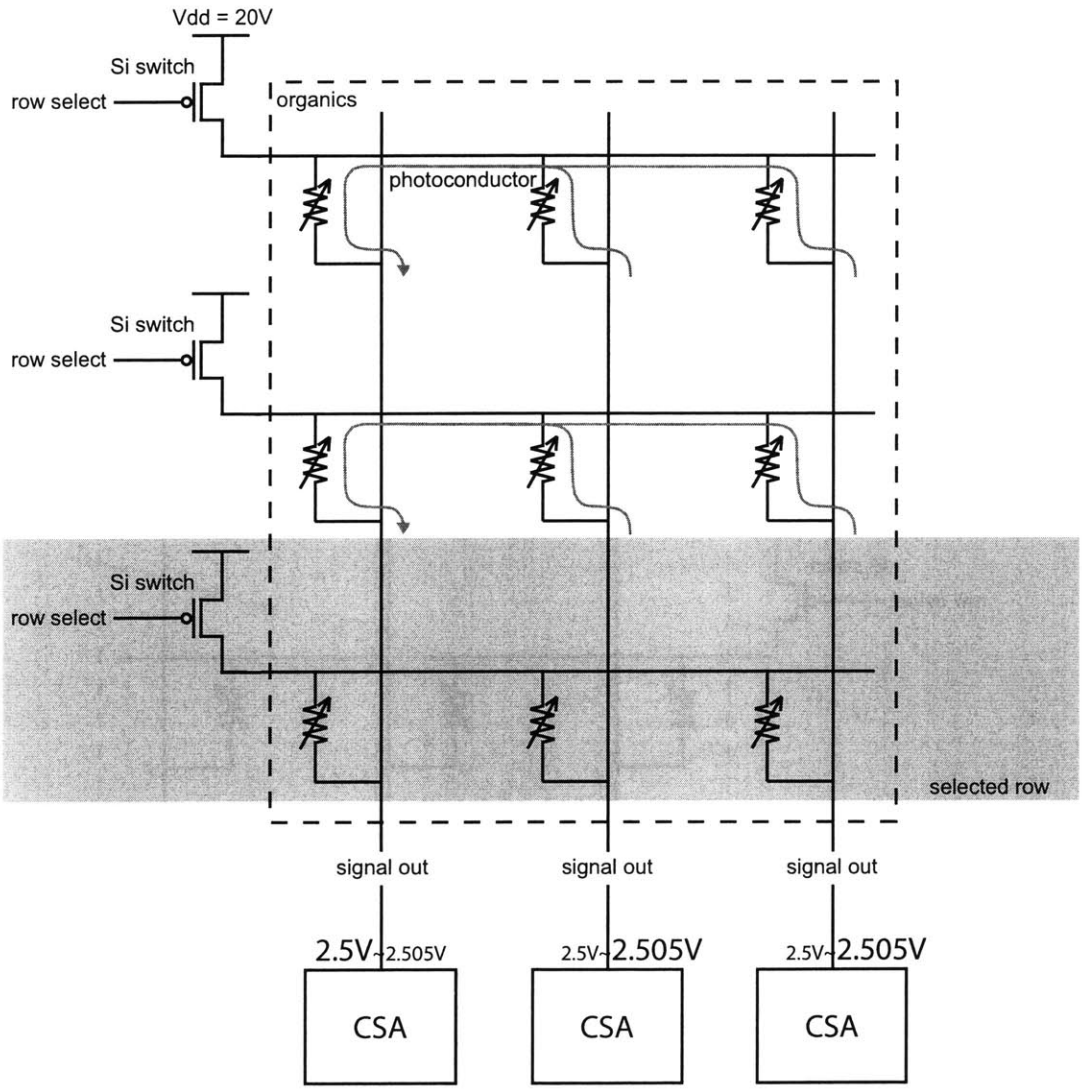


Figure 4-5: Dominant Leakage Paths in an Organic Photodetector Array Design with Silicon Switches. The leakage is determined mainly by the worst-case photoconductor resistance and the CSA input voltage. The CSA forces its input voltage to 2.5~2.505V; the numbers in larger font are the numbers used for worst-case leakage current estimation.

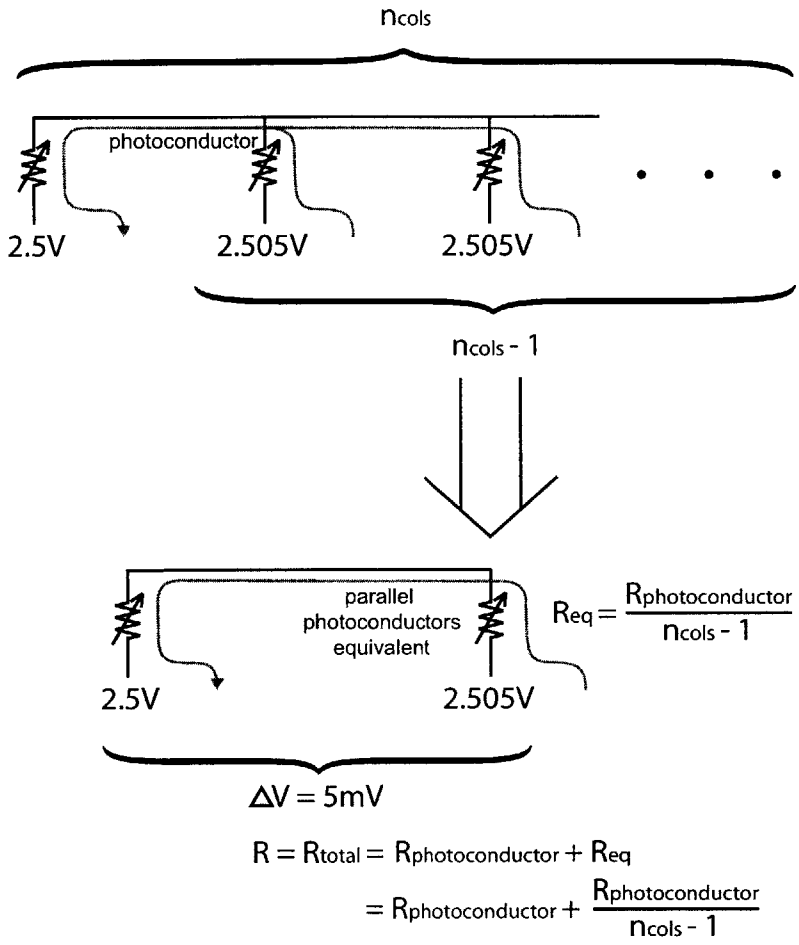


Figure 4-6: Illustration of the Derivation of Leakage Analysis Variables ΔV and R for the Organic Photodetector Array Design with Silicon Switches.

signal out line to 2.5V~2.505V, and the exact voltage may differ from CSA to CSA. This voltage difference from one *signal out* column line to another causes leakage from a column to another. The worst-case leakage occurs when 63 columns are collectively leaking onto one column. This scenario is illustrated in Figure 4-5 (note that an equally bad leakage scenario is when one column is leaking onto 63 other columns; which produces the same worst-case leakage current, but opposite in sign).

This worst-case leakage occurs when one CSA forces the *signal out* line to 2.5V, while the 63 others force their voltages to 2.505V (see Figure 4-5). For a given row, all "leakage-contributing" columns have the same voltage on the *signal out* line (the worst-case assumes they are all forced to 2.505V). And thus, all the photoconductors in the "leakage-contributing" columns can be considered parallel conductors (or resistors). The total resistance between the voltage difference is then the parallel resistance of 63 photoconductors that is then in series with another photoconductor resistance (See Figure 4-6). The leakage through one photodetector (from column-coupled leakage) is

$$i_{leakage,single\ photodetector} = \frac{\Delta V}{R}. \tag{4.4}$$

By argument of symmetry (since the rows are not coupled), all non-selected rows have the same leakage component. Thus, the general expression of the leakage on a single *signal out* column line is described by:

$$\begin{aligned} i_{leakage} &= \left[(n_{rows}-1)\times\frac{\Delta V}{R}\right] \\ &= \left[(n_{rows}-1)\times\frac{\Delta V}{R_{photoconductor}+\frac{R_{photoconductor}}{n_{cols}-1}}\right] \\ &\approx \left[n_{rows}\times\frac{\Delta V}{R_{photoconductor}+\frac{R_{photoconductor}}{n_{cols}}}\right] \\ &\approx \left[n_{rows}\times\frac{\Delta V}{R_{photoconductor}}\right] \end{aligned} \tag{4.5}$$

The final two approximations are only valid if the number of columns is large, for example greater than 10. ΔV is the worst case voltage difference between the CSAs,

which is 2.505V-2.5V = 5mV, and the worst case $R_{photoconductor}$ is 2GΩ. Thus, the worst case leakage on a single column is calculated to be ~160pA, a factor of about 4 improvement from the original design in Section 4.1. Since the columns are coupled, the argument for symmetry among the columns does not hold. Instead, one column will experience the worst case leakage of 160pA, while the other 63 will experience only $\frac{1}{63}$ that value, but in the opposite direction (since they are "supplying" leakage).

This "Improved Switches" Organic Photodetector array design is not very robust, as the leakage on a single column is dependent upon the number of columns, and the columns are coupled together. An improved design can decouple the columns, as well as further reduce leakage.

4.3.2 Power Supply Switching

Figure 4-7 shows an alternative architecture that completely eliminates the column coupling effects in Section 4.3.1. Instead of using power-cutoff switches, power lines are switched between an "off voltage" such as 2.5V (to turn off a row) to an "on voltage" such as 20V (to turn on a row) as each row is selected. To turn on a row, the power line for that row is set to the "on voltage" (20V) while all the other rows' power lines are set to the "off voltage" (such as 2.5V). The voltage power supply, having an extremely low input impedance, decouples the columns. Any current back flowing through the photodetectors will drain out through the voltage source, as opposed to entering down another column.

Since there is no power isolation switch, the power supply must be switched to the correct "off voltage" in order to properly turn off a row. The "off voltage" must be such that the voltage drop across the photodetector is zero, resulting in zero signal current. If the voltage is slightly off, there will be leakage through the photodetector device. Given the range of possible voltages for the *signal out* line (2.5V~2.505V as forced by the CSA, see Section 4.2), the voltage drop across all photodetectors in the same row cannot all be set to zero, and leakage is unavoidable (see Figure 4-8). However, the worst-case leakage can be minimized.

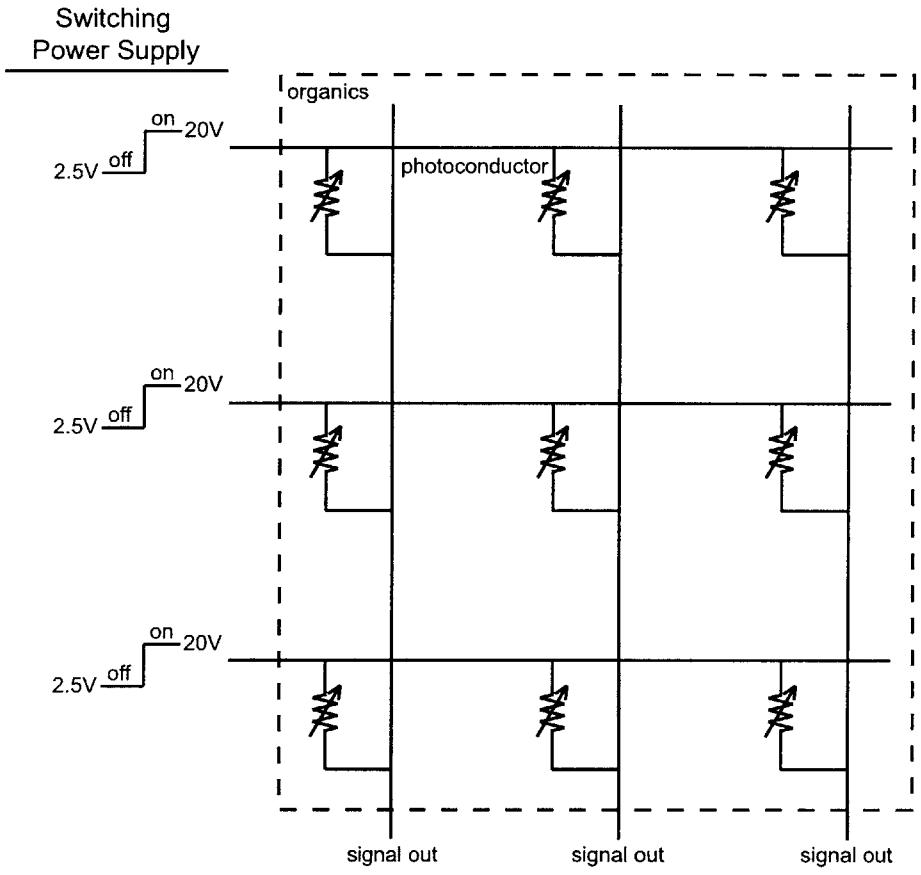


Figure 4-7: An Organic Photodetector Array Design with Power Supply Switching.

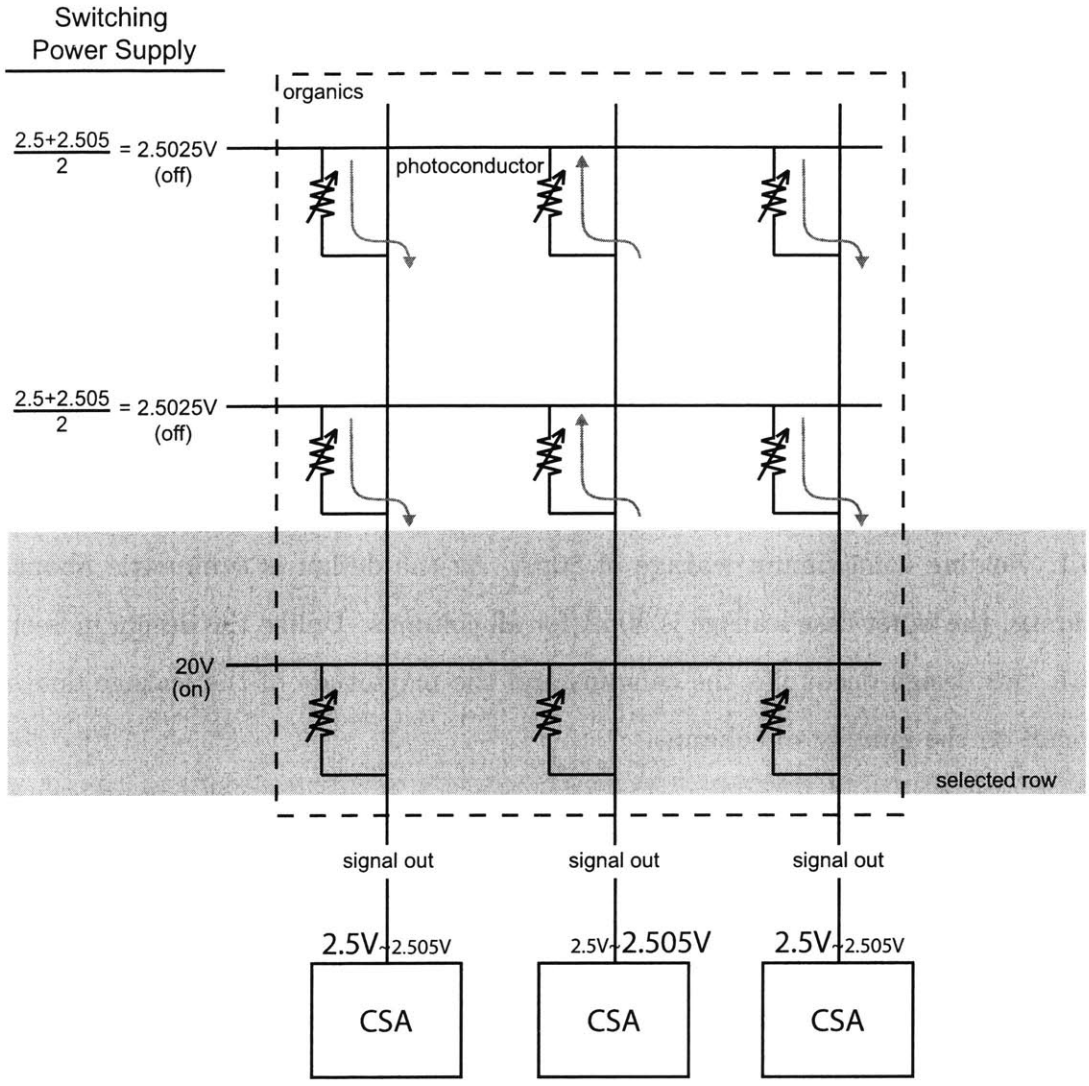


Figure 4-8: Dominant Leakage Paths in an Organic Photodetector Array Design with Power Supply Switching. The optimal "off voltage" to minimize leakage is the median of the CSA input voltage range; in this case, the "off voltage" is chosen to be 2.5025V. With the optimal "off voltage", leakage is determined mainly by the worst-case photoconductor resistance and the CSA input voltage range. The CSA forces its input voltage to 2.5~2.505V; the numbers in larger font are the numbers used for worst-case leakage current estimation.

The leakage current analysis is similar to that in Section 4.3.1:

$$i_{leakage} = \left[(n_{rows} - 1) \times \frac{\Delta V}{R}\right] \approx \left[n_{rows} \times \frac{\Delta V}{R_{photoconductor}}\right] \tag{4.6}$$

R is the resistance of the path, which is the resistance of the photoconductor. ΔV is the voltage drop across the photoconductor, which is the voltage difference between the power line "off voltage" and the CSA input voltage. Thus, the worst-case leakage can be minimized by choosing the voltage range median as the "off voltage". In this case, the *signal out* line ranges from 2.5V to 2.505V, then choose the "off voltage" to be 2.5025V. Thus, regardless of what voltage *signal out* is, $\Delta V \leq$ 2.5mV. The worst-case ΔV here is then 2.5mV, compared to 5mV in Section 4.3.1 & Equation 4.5. Thus, this design effectively halves the worst case leakage calculated in Section 4.3.1, yielding a maximum leakage of 80pA. As the design is symmetric about all columns, the worst-case leakage is 80pA for all columns. Unlike the design in Section 4.3.1, this design decouples the columns and the magnitude of the leakage does not depend on the number of columns.

4.3.3 Combining Features

Further improvements can be achieved by a combination of the above designs for better performance. Figure 4-9 shows a combination of the silicon switches with the OFET switches. Its dominant leakage paths (shown in Figure 4-10) are analogous to those shown in Figure 4-5.

For a conservative estimate, the effect of the photoconductor resistance is assumed negligible. In reality, the photoconductor resistance will help lower the leakage current through the OFET. Now, notice that the 63 OFETs in the "leakage-contributing" columns are transistors in parallel. This is equivalent to a single OFET 63 times wider. This equivalent 63× OFET is then in series with the 1× OFET in the "leakage-sinking" OPD unit (see Figure 4-11). A second simplification, also a conservative approximation, is to assume that the equivalent 63× OFET has little impact, i.e. the

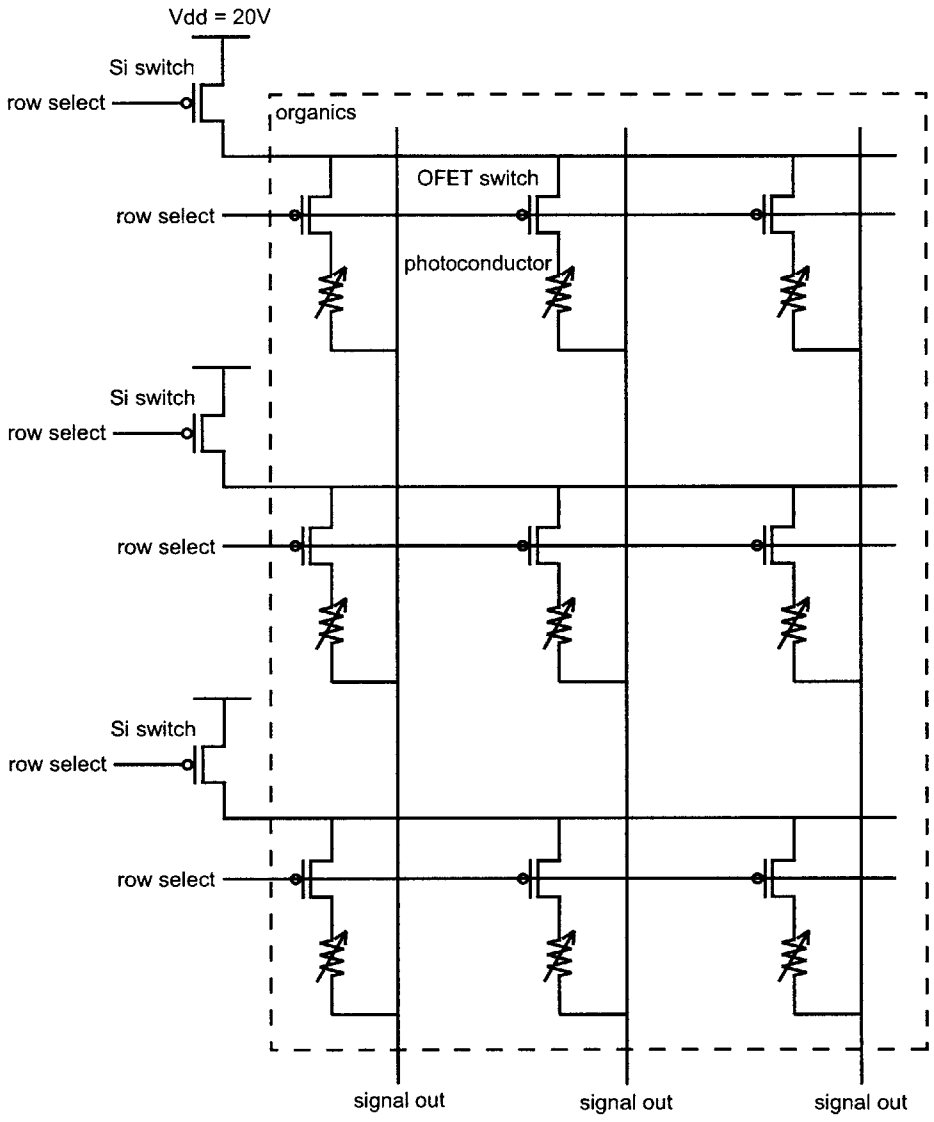


Figure 4-9: An Organic Photodetector Array Design Implementing Both Silicon and Organic Switches.

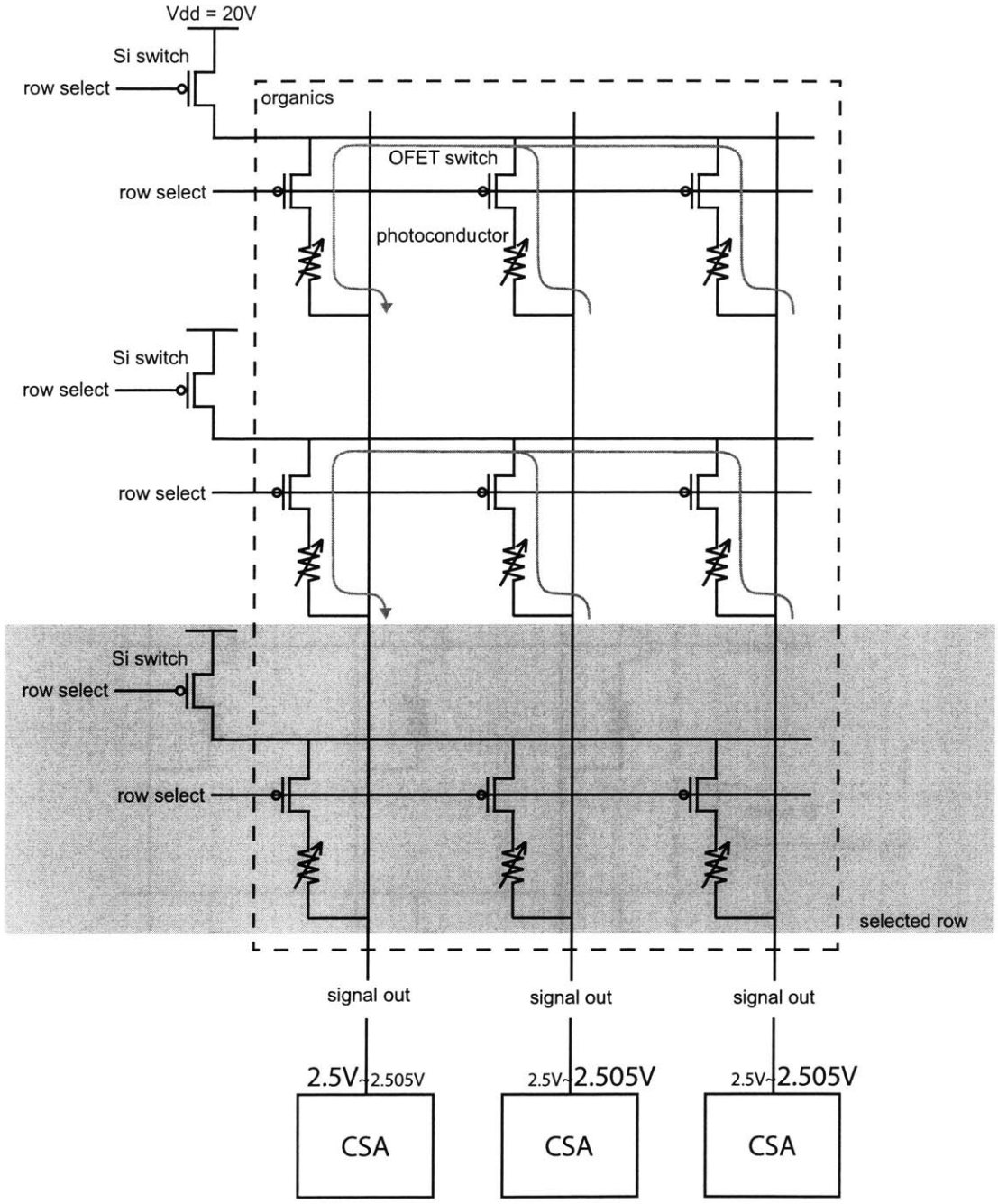


Figure 4-10: Dominant Leakage Paths in an Organic Photodetector Array Design Implementing Both Silicon and Organic Switches. The leakage is determined mainly by the OFET switch off current and the CSA input voltage. The CSA forces its input voltage to 2.5~2.505V; the numbers in larger font are the numbers used for worst-case leakage current estimation.

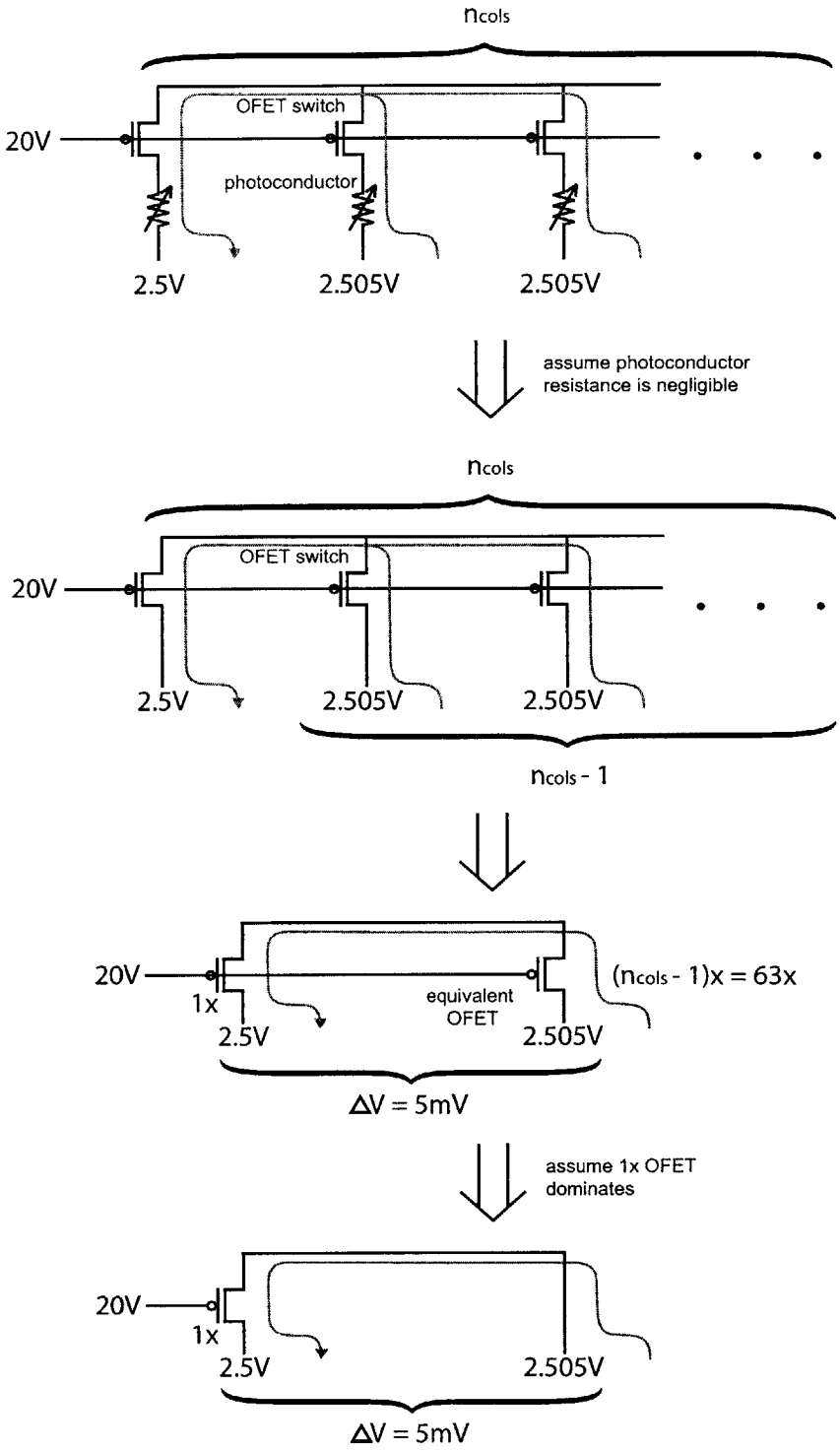


Figure 4-11: Illustration of the Leakage Current Analysis for the Organic Photodetector Array Design Implementing Both Silicon and Organic Switches.

majority of the voltage drops across the 1× OFET in the "leakage-sinking" OPD unit (see Figure 4-11). Thus, the worst-case leakage is the OFET off current with a V_{SG} of -17.495V and a V_{SD} of 5mV (V_G=20V, V_S=2.505V, and V_D=2.5V).

The OFET off current is estimated to be ~360fA for V_{SG}=-17.495V and V_{SD}=5mV ($\frac{W}{L}=\frac{1000\mu m}{10\mu m}$). Referring back to equation 4.3, this results in a total leakage of 22.7pA on a single column line. Since the columns are coupled, one column will experience this worst case leakage, while the other 63 columns will experience $\frac{1}{63}$ of this value.

Figure 4-12 shows another array architecture combining power supply switching with OFET switches. The nature of the leakage is the same as the design in Figure 4-1. thus the dominant, worst-case leakage is similarly derived (see Figure 4-13 and Equation 4.3).

Again, for a conservative estimate, the effect of the photoconductor resistance is assumed negligible. With this simplification, the worst-case OFET V_{SD} in this case is reduced to 2.5mV. The OFET off current with $\frac{W}{L}=\frac{1000\mu m}{10\mu m}$, V_{SG}~-17.4975V, and V_{SD}=2.5mV (V_G=20V, V_S=2.5025V, and V_D=2.5V) is 280fA. This yields a total leakage of 17.6pA on a single column line.

Table 4-14 compares and summarizes all the designs. The final proposed design is the one shown in Figure 4-12, with the least amount of leakage. Since the OPD imager array will be done in integrated organics along with the OLED array, the organic fabrication and testing of the proposed imager array design falls beyond the scope of this thesis. But should the leakage still prove to be too large, this chapter has established many design architectures to serve as a basis for exploration and expansion to further reduce leakage.

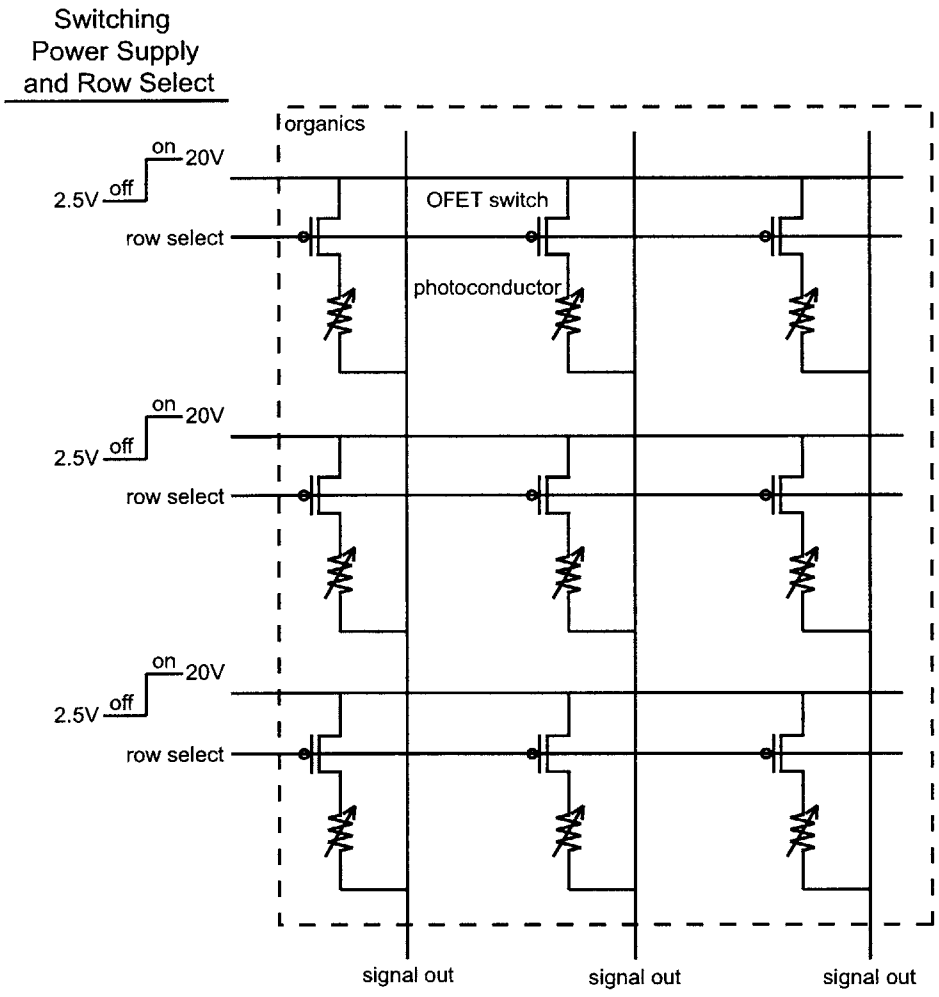


Figure 4-12: An Organic Photodetector Array Design Implementing Both Power Supply Switching and Organic Switches.

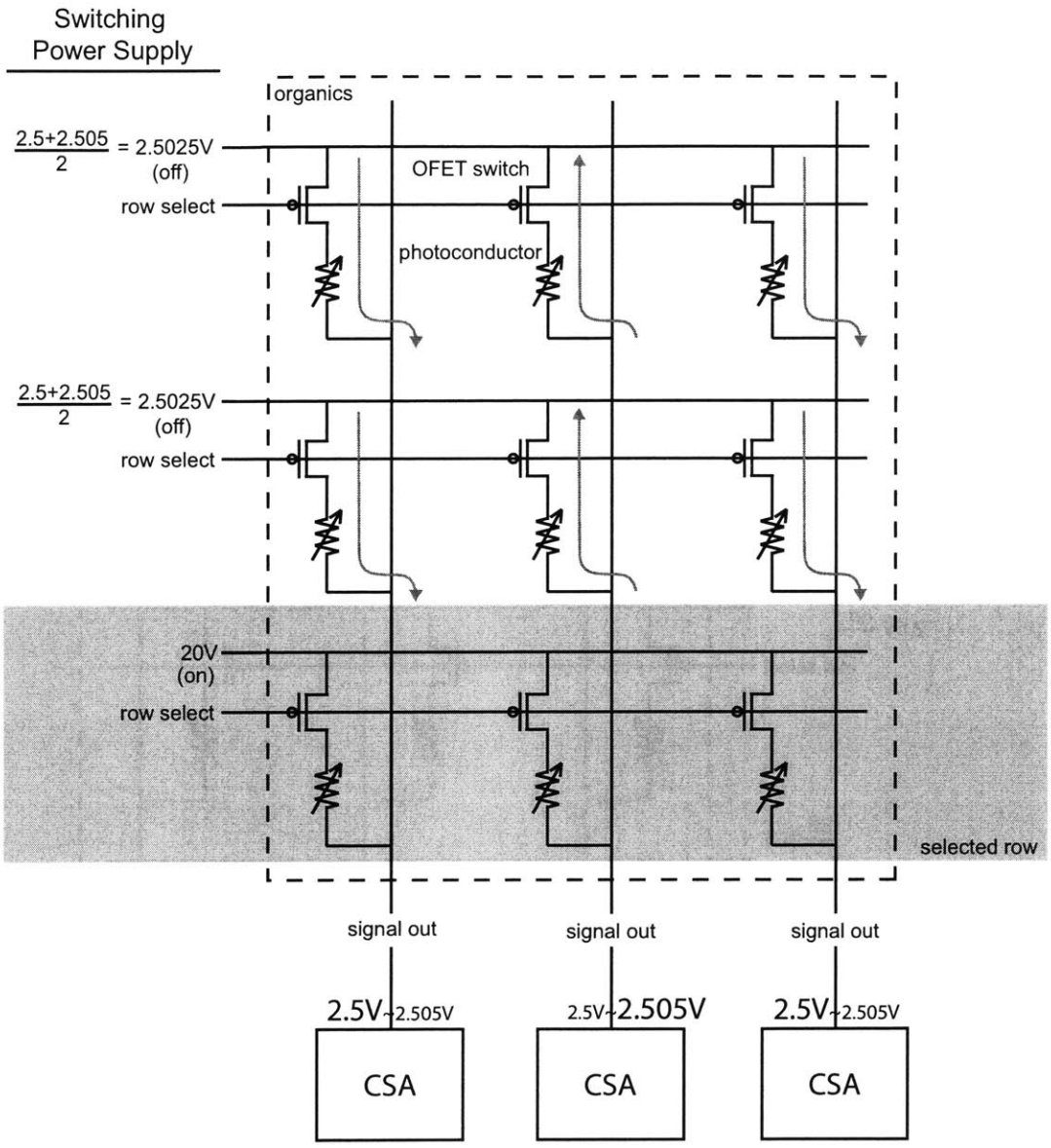


Figure 4-13: Dominant Leakage Paths in an Organic Photodetector Array Design Implementing Both Power Supply Switching and Organic Switches. The optimal "off voltage" to minimize leakage is the median of the CSA input voltage range; in this case, the "off power voltage" is chosen to be 2.5025V. With the optimal "off voltage", leakage is determined mainly by the OFET switch off current and the CSA input voltage. The CSA forces its input voltage to 2.5~2.505V; the numbers in larger font are the numbers used for worst-case leakage current estimation.

Organic Photodetector Array Designs

Design	Figures	Features			Worst-case Leakage on a Single Column Line	Comments
		OFET Switches	Improved (Silicon) Switches	Power Supply Switching		
Original Design	Figures 4-1 & 4-3	✓			630pA	Large leakage and small signal-to-leakage ratio
Improved Switches Design	Figures 4-4 & 4-5		✓		160pA	Column coupling & dependency on number of columns
Power Supply Switching Design	Figures 4-7 & 4-8			✓	80pA	-
OFET Switches and Improved Switches Design	Figures 4-9 & 4-10	✓	✓		22.7pA	-
OFET Switches and Power Supply Switching Design	Figures 4-12 & 4-13	✓		✓	17.6pA	Least leakage; other leakage paths may come into play

Figure 4-14: Table Summarizing the Five Organic Photodetector Array Designs.

Chapter 5

Current Sensing Amplifier

The Current Sensing Amplifier (CSA) is essentially a high-gain transimpedance amplifier. It must be able to sense low currents in the 0-10nA range and amplify it up to a 0-5V range. The gain of 500 MΩ must be inverting and linear as mentioned in Section 3.2.3.

Its gain must also be continuously tunable over a wide range due to the great uncertainty in the OPD design (which causes uncertainty in the range of I_{in}). It is estimated that the OPD output range will most likely fall between 0-5nA and 0-20nA. However, there is also a non-negligible possibility that the OPD range is as small as 0-2nA or as large as 0-50nA. And thus, the Current Sensing Amplifier implements a transimpedance gain of 500 MΩ, continuously tunable from 62.5 MΩ to 4 GΩ. To achieve these specifications, the Current Sensing Amplifier is implemented as a cascade of four stages (see Figure 5-1):

1. Transimpedance Stage
2. Gain Stage
3. Differential to Single-ended Conversion Stage
4. Sample and Hold Stage

Each of these stages is discussed in detail in the following sections.

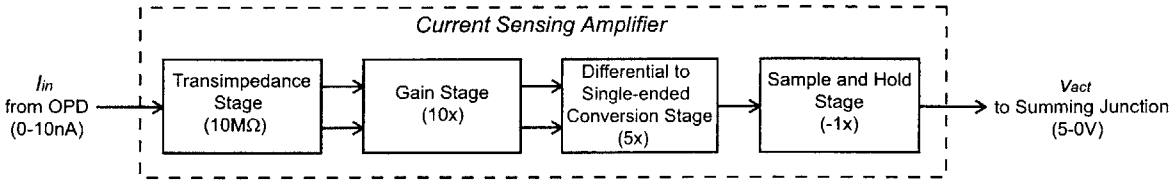


Figure 5-1: Block Diagram of the Current Sensing Amplifier.

5.1 Transimpedance Stage

The Transimpedance Stage is implemented as a closed-loop switch capacitor circuit (see Figure 5-2). It is a two-phase system with a 20kHz switching frequency. In one phase (gain phase), it converts current into voltage by integrating current on a capacitor, according to the relation

$$\int I dt = CV. \tag{5.1}$$

Approximating I to be a constant current in the short integration window[1], this simplifies to

$$It = CV. \tag{5.2}$$

Since this phase lasts for 25μs and C is 2.5pF, the Transimpedance Stage has a transimpedance of 10 MΩ. In the other 25μs phase (reset phase), the system is reset and any input offsets are sampled for input offset cancellation. The circuit also employs charge injection cancellation to decrease error (see Figure 5-2).

By changing the length of the integrating window, a continuous range of transimpedance gains can be obtained. A reasonable range for the integrating window is 12.5μs-50μs (10kHz-40kHz, with a center frequency of 20kHz). Thus, this stage implements a typical transimpedance gain of 10 MΩ, with the ability to tune to any

[1]The switch capacitor nature of the silicon circuits requires a sample and hold at the Compensator output (see Figure 5-1 & Section 5.4), which is the OLED drive voltage. Since the drive voltage is constant, the OLED brightness and OPD output current will mostly be constant. Furthermore, the switch capacitor frequency is much faster than the signal frequencies of interest. Thus this approximation is appropriate.

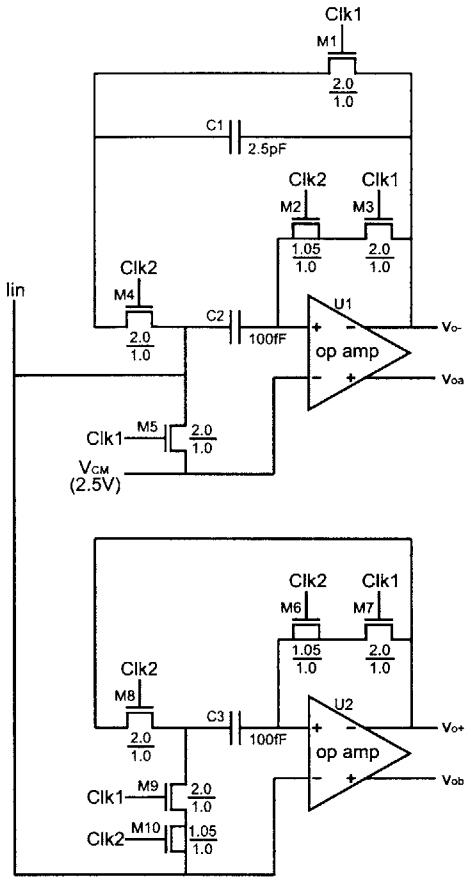


Figure 5-2: Switch Capacitor Transimpedance Stage Circuit Diagram. Clk1 and Clk2 are non-overlapping clocks corresponding to the reset phase and gain phase respectively; V_{CM} is supplied externally.

gain in the 5-20 MΩ range.

Implementing the Transimpedance Stage with a closed loop op amp allows for an ultra low input impedance. Low input resistance is critical for the Transimpedance Stage as an input stage, since a non-trivial input impedance will alter the input current signal upon "sensing" it. The feedback loop forces the input voltage to stay at a constant value (~2.5V) over the entire range of possible input currents, deviating by a maximum of only 80μV, which prevents distortion of the input signal. See Section 5.1.4 for detailed R_{in} calculations.

The positive and negative output signals are taken from across the integrating capacitor $C1$ and buffered appropriately. As mentioned before, one end of the capacitor

(the input) is held at 2.5V; thus the differential output is only semi-differential. v_{o-} is the output signal that varies over a 100mV range and v_{o+} is the constant reference voltage. This semi-differential voltage is converted to a fully differential voltage in the next stage (see Section 5.2).

Since the input signal is at most 10nA, the input signal cannot be used to directly drive the next stage. Instead, a buffer is required to drive the switch capacitor loads of the next stage. The closed-loop op amp acts as an output buffer for v_{o-}. A separate unity gain closed-loop op amp is used to buffer v_{o+} (see Figure 5-2). From the figure, there are four outputs, though only two convey the signal (v_{o+} and v_{o-}). The other two (v_{oa} and v_{ob}) are passed to the next stage because they must be presented with the same load as the two signal outputs. Otherwise, the mismatched capacitive loads may cause all outputs to ring, or even oscillate. This is best understood by considering the effects of the common-mode feedback within the op amps.

Both op amps in Figure 5-2 include common-mode feedback (CMFB). The CMFB adjusts op amp internal bias conditions such that the op amp output common-mode is at 2.5V, i.e. if $\frac{v_{o+}+v_{o-}}{2} > 2.5V$, CMFB forces both outputs to decrease, and vice versa, until the outputs have a common-mode of 2.5V. The common-mode feedback is a feedback loop and is capacitively compensated. It can be considered to be just as fast as the unloaded op amp.

The ringing arises from the interactions between a very fast CMFB and its two

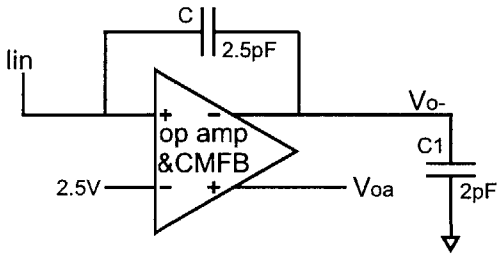


Figure 5-3: Simplified Closed-loop Op Amp Circuit with Mismatched Capacitive Loads. v_{o+}=v_{oa} has no capacitor load; v_{o-} has a 2pF + 2.5pF capacitor load. The CMFB forces the output common-mode voltage to 2.5V. See Figure 5-4 for simulation results.

dependent signals. One of the signals, v_{oa}, adjusts very fast, as it has no capacitive load. The other signal, v_{o-}, adjusts very slowly due to a large capacitive load. Figure 5-3 shows a simplified equivalent of the circuit in question. A manual step-by-step simulation follows.

1. The op amp starts at steady state with both outputs at 2.5V (zero differential output).

2. A change in inputs causes the op amp to increase the differential output to a new voltage, say 1V. In steady state, the op amp will settle to $v_{oa} = 3$V, and $v_{o-} = 2$V.

3. But in the short run, v_{oa} settles to 3V extremely fast, while v_{o-} has not moved much from 2.5V due to its large capacitive load. Say the outputs are now at $v_{oa} = 3$V and $v_{o-} = 2.49$V.

4. The CMFB detects an increase in the output common-mode ($\sim$2.75V) and adjusts the internal bias voltage immediately to restore the common-mode to 2.5V.

5. This causes v_{oa} to move instantly to 2.51V. Since the op amp is trying to output a differential output voltage of 1V, v_{o-} is now being driven to 1.51V (though slowly).

6. This eventually causes v_{o-} to overshoot its steady state value of 2V.

7. Now less than 2V, this value of v_{o-} gets fed back around the whole op amp through the feedback capacitor (see Figure 5-3) to the op amp positive input. This decrease in the positive op amp input causes the op amp to decrease its differential output.

8. The process above is then reversed, with the op amp trying to drive v_{o-} higher back towards a smaller differential output. This causes ringing (if the magnitude decays) or oscillation (if the magnitude increases).

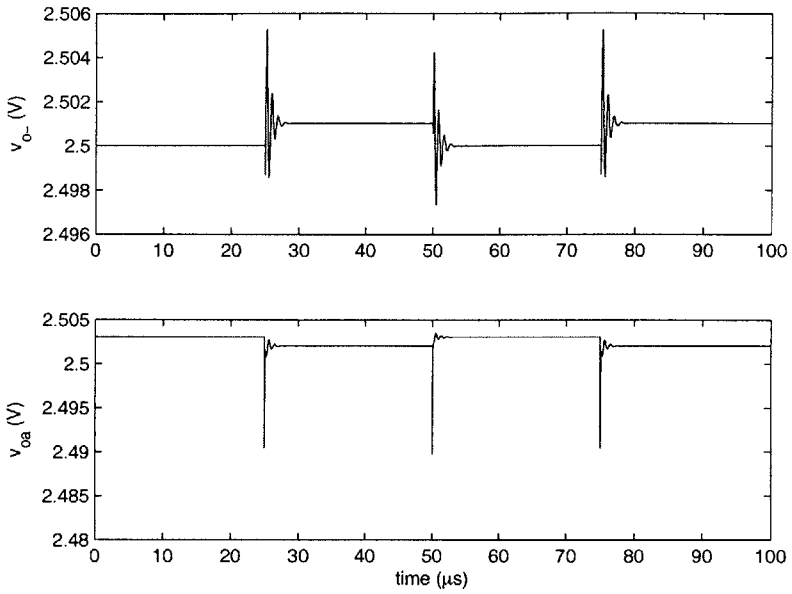


Figure 5-4: Cadence Simulation of Op Amp Circuit in Figure 5-3. Mismatched capacitive loads resulted in ringing.

Figure 5-4 shows Cadence simulation results which support the analysis above. Ringing is observed when v_{o-} is capacitively loaded but v_{oa} is not.

The analysis is tailored to the top op amp circuit in Figure 5-2. However, a similar analysis will show that the bottom op amp (in Figure 5-2) will ring as well if presented with mismatched capacitive loads. Thus, the next stage must provide switched dummy load capacitors to the two unwanted signals (v_{oa} and v_{ob}) to reduce ringing.

Several important design decisions were made in the process of designing the Transimpedance Stage; the following sections discuss some of the most important design decisions. The last section, Section 5.1.4, describes the op amp design that allows it to properly sink the 10nA signal current and source the driving current.

5.1.1 Sensing Current or Sensing Charge; Resistor or Capacitor

One of the most important design decisions was whether to sense the instantaneous current, or to sense charge, i.e. an integrated value of current. Sensing current is best done with a resistor, and integrating current is best done with a capacitor.

Sensing current looks at the instantaneous value of the OPD output, which improves the speed of the overall system. Integrating current factors in past values in addition to the current value, which decreases the response to a step change. On the other hand, integrating current acts like a low pass filter and prevents glitches or transients from propagating errors through the system.

Converting instantaneous current into a voltage using a resistor follows the relationship

$$V = IR. \tag{5.3}$$

The resistance R is the transimpedance gain. To achieve a transimpedance gain of 10 MΩ, R must be 10MΩ. However, such a resistor would require too much area; and thus a more reasonable value for R is 1MΩ. In this case, an additional 10× gain stage is required to provide the missing gain (see Figure 5-5). Overall, the resistor implementation will require much more area. On the other hand, integrating current into a voltage by forcing the current onto a capacitor is described by Equation 5.2. The transimpedance gain is $\frac{t}{C}$. Thus, with an appropriate choice of t (25μs), only a small C (2.5pF) is required to achieve a gain of 10 MΩ (circuit shown in Figure 5-2). Thus the capacitor implementation uses area much more efficiently.

In terms of complexity, the resistor option has a less complex circuit as it does not require clocking or switching; the capacitor option requires a switch capacitor implementation with two phases, one for integrating and the other for resetting the integrating capacitor. In addition, the switch capacitor circuit introduces errors from charge injection, as transistor switches are turned on and off to clear the capacitor. Hence additional charge cancellation transistors are required.

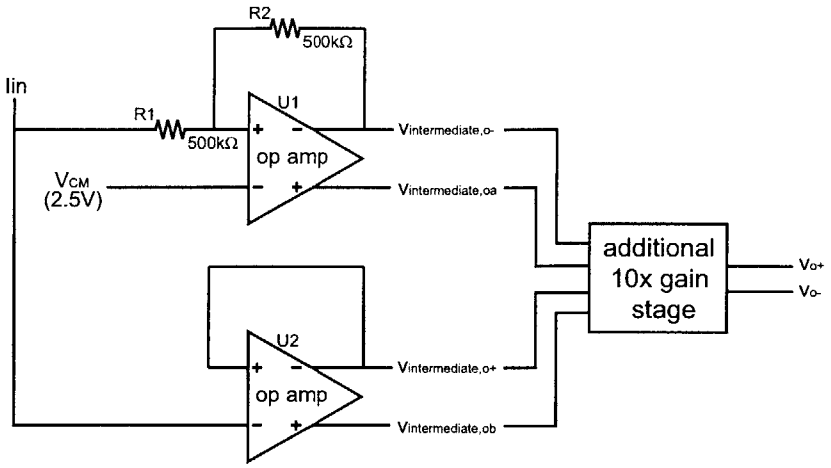


Figure 5-5: Resistor Option Transimpedance Stage Circuit Diagram. The two 500kΩ resistors yield a 1MΩ transimpedance.

Furthermore, resistors and capacitors introduce different root mean square noise values, which impose limits in the attainable accuracy. For a resistor, the root mean square voltage noise [13] is

$$E_n = \sqrt{4kTR\Delta f}. \tag{5.4}$$

For a resistor value of 1MΩ and a frequency bandwidth of 20kHz, E_n is ~18μV. But this is for a transimpedance of 1MΩ; there is an additional 10× gain stage to increase the gain to 10 MΩ. Thus the effective output noise $E_{n,output}$ is 180μV. Alternatively, the noise can be expressed as input-referred noise, which would be $I_{n,input-referred}$ = 18pA. A capacitor, however, has a root mean square noise [13] of

$$E_n = \sqrt{\frac{kT}{C}}. \tag{5.5}$$

For a capacitor of 2.5pF, E_n is 41μV. Since no additional gain stage is necessary, $E_{n,output}$ = 41μV and $I_{n,input-referred}$ = 4.1pA. In comparison, using these component values, the capacitor implementation introduces less noise, permitting 2 more bits of resolution over the resistor implementation.

A capacitor implementation offers several other advantages as well, including ac-

Comparison of Sensing Current and Integrating Current

Parameter	Sensing Current With a Resistor	Integrating Current Over a Capacitor
Transimpedance Gain (Ω)	R	$\frac{t}{C}$
Speed	Fast	Slow
Circuit Complexity and Area	Simpler; however larger area	Requires more circuitry; smaller area
Power Consumption	Less	More
Root Mean Square Output Voltage Noise (μV)	$E_{n,output} = 180$	$E_{n,output} = 41$
Tolerance to Transients	No	Yes
Continuously Tunable Gain	No	Yes, Intrinsic to design
Fabrication Accuracy and Uniformity	Low (within 1-5% error)	High (within 0.1% error)

Figure 5-6: Table Summarizing the Resistive Sensing Current and Capacitive Integrating Current Designs.

curacy and uniformity in fabrication. But perhaps most importantly, it allows for a continuously tunable gain. As seen in Equation 5.2, the transimpedance is given by $\frac{t}{C}$. With a fixed C, the transimpedance can be adjusted over a continuous range by adjusting the external clock frequency. If the clock frequency is decreased, the period and integrating window are increased, thereby increasing the transimpedance, and vice versa. Note that the switch capacitor approximations hold only if the switch capacitor frequency is much faster than the signal frequencies of interest. This sets a minimum switching frequency of 10kHz. Similarly, the slew rate of the op amp imposes a maximum switching frequency of 40kHz. Thus the capacitor implementation allows a continuously tunable transimpedance gain of 5-20 MΩ. For a broader range, a Programmable Capacitor Array is used (see Section 5.3).

Each technique and design offers its own advantages and disadvantages; but in the end, integrating current over a capacitor proved to be most appropriate for this

application. Figure 5-6 summarizes and compares the two options of sensing current with a resistor or integrating current with a capacitor.

5.1.2 Open Loop or Closed Loop

Several open-loop designs were tested as well. Open loop designs do not have the problem of op amp input offsets, and require less circuitry and hence less power. They also possess the potential to reach incredibly high transimpedance gains of 50-200 MΩ in a single stage. Unfortunately, test results show that open loop designs are subject to mismatch errors. Slight mismatches in the MOSFET thresholds can result in mismatches from channel to channel on the same die. With an open loop transimpedance gain of 10 MΩ or higher, such mismatches can easily cause outputs to rail. Some channels will permanently rail high, while others rail low. The remaining few will operate at unpredictable common mode voltages, likely in low-gain or non-linear regions of the amplifier. In any case, test circuits of open loop transimpedance amplifiers have demonstrated that closed-loop feedback control is a must for such high-gain applications. As such, all of the silicon stages in the Current Sensing Amplifier are individual closed-loop stages. The Transimpedance Stage is no exception, implementing a closed-loop integrating capacitor with a modest transimpedance gain of 10 MΩ.

5.1.3 Single-Ended, Semi-Differential, or Fully Differential

The benefit of a differential circuit is its immunity to systematic noise that identically affects both differential signals. In a single-ended signal, data is conveyed in the absolute value of the signal. Thus, noise can easily alter the data by contaminating the absolute value of the single-ended signal. However, in a differential signal, data is conveyed in the difference of the two signals. If a systematic noise source affects both signals identically, the difference and data are preserved. Hence a differential implementation is chosen for this application.

The decision is then whether to use a semi-differential or a fully differential Transimpedance Stage. A semi-differential signal has one varying signal, while the other is held constant as a reference voltage. A fully differential signal has both signals varying, usually keeping a constant common mode voltage. For most circuits, a varying common mode voltage usually varies the operating point of the current and downstream stages, and can introduce a signal dependent error. Thus, a fully differential implementation is preferred as it maintains a constant common mode voltage. However, as an input stage, the Transimpedance Stage must have a low input resistance, but a fully differential design with a low input resistance is not feasbile. The remainder of this section explains why a semi-differential design was chosen.

The voltage across the integrating capacitor is exactly representative of the average current into the capacitor, as given in Equation 5.2. Thus, for the highest level of current-to-voltage conversion accuracy, the Transimpedance Stage differential outputs must be taken across the integrating capacitor. Figure 5-7a illustrates such a fully-differential design. However, this design has a substantial input impedance (low input impedance is a requirement, see Section 4.1). The input impedance (as seen from the previous stage) can be approximated as the change in voltage due to a small change in input current:

$$R_{in} = \frac{\partial v_{in}}{\partial I_{in}} \tag{5.6}$$

Assuming a large op amp gain, the positive op amp input voltage will equal the constant 2.5V at the negative op amp input (see Figure 5-7a). v_{o+} will then increase in voltage as the current I_{in} is forced into the integrating capacitors. The relationship between v_{in} and I_{in} is

$$v_{in} = v_{o+} = 2.5 + \frac{I_{in}t}{C}. \tag{5.7}$$

The input impedance is then

$$R_{in} = \frac{t}{C} \approx 10M\Omega \tag{5.8}$$

in the worst case scenario (t = duration of gain phase = 25μs). With such a large input impedance, the signal current from the Organic Photodetector can be distorted, introducing a signal-dependent error.

Another fully differential alternative is to take the outputs from the differential outputs of the differential op amp (Figure 5-7b). This design does not have the large input impedance problem seen in the previous design (Figure 5-7a). Instead, its input impedance is very small assuming a large op amp gain. In Figure 5-7b, the input node is the same as the positive op amp input terminal. With sufficient op amp gain, this node is forced to the same voltage as the negative op amp input terminal, which is a constant 2.5V. Thus, no matter the input current, the input voltage is always forced to a constant 2.5V. This is the definition of zero input impedance (like an ideal voltage source).

However, this design (Figure 5-7b) requires the assumption that the op amp differential output obeys

$$v_{o,d} = a_d v_{i,d}, \tag{5.9}$$

implying it has absolutely no input offset - it must have a 0V differential output when the differential input is 0V. Otherwise, with an op amp input offset, there will be an error in the outputs. In the light of potential transistor mismatches, op amp input offsets are not uncommon and this assumption cannot be made. Figure 5-7b also illustrates three possible output characteristics of the form

$$v_{o,d} = a_d v_{i,d} + k. \tag{5.10}$$

The top characteristic illustrates a positive k. In this case, the differential output voltage is higher than it should be for all inputs. The middle characteristic is the ideal case where k=0, and the differential output voltage is exactly representative of the input current. However, a case of no op amp offset is extremely rare and cannot be assumed. The bottom characteristic illustrates a negative k, where the differential output voltage is lower than it should be for all inputs. Due to op amp offsets, this

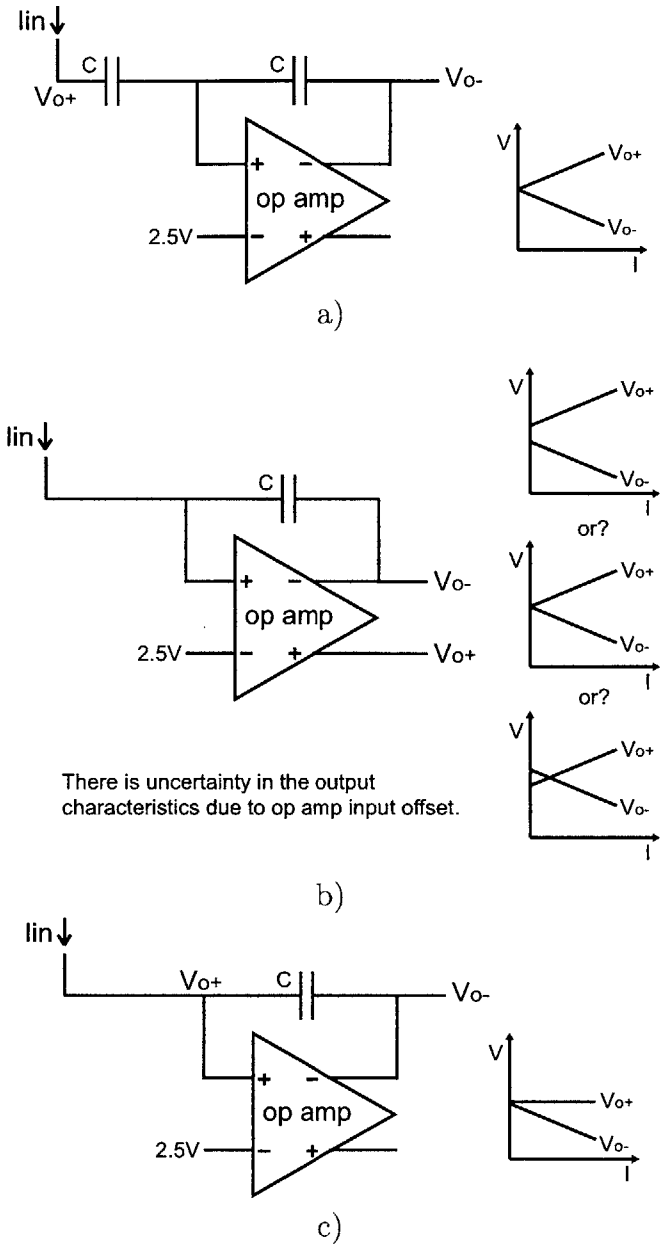


Figure 5-7: Differential Output Design Options. a) Fully differential design with outputs taken across the capacitors. V_{o+} is the voltage measured at the input node. b) Fully differential design with outputs taken from the op amp. The op amp outputs are fully differential because it has CMFB to ensure the output common-mode is always at 2.5V. However, due to op amp input offset, there is some uncertainty in the output characteristics. c) Semi-differential design with outputs taken across the capacitor. V_{o+} is the voltage measured at the input node.

Comparison of Various Differential Output Designs for the Transimpedance Stage

Differential Output Design Option	Transimpedance Gain (Ω)	Offset Problem	Approximate Input Impedance (assume large op amp gain)
1. Figure 5-7a	$\frac{2t}{C}$	No	$\approx \frac{t}{C}$; worst case $\approx 10M\Omega$
2. Figure 5-7b	$\frac{2t}{C}$	Yes	Very small; Negligible
3. Figure 5-7c	$\frac{t}{C}$	No	Very small; Negligible

Figure 5-8: Table of the Transimpedance Stage Differential Output Design Options.

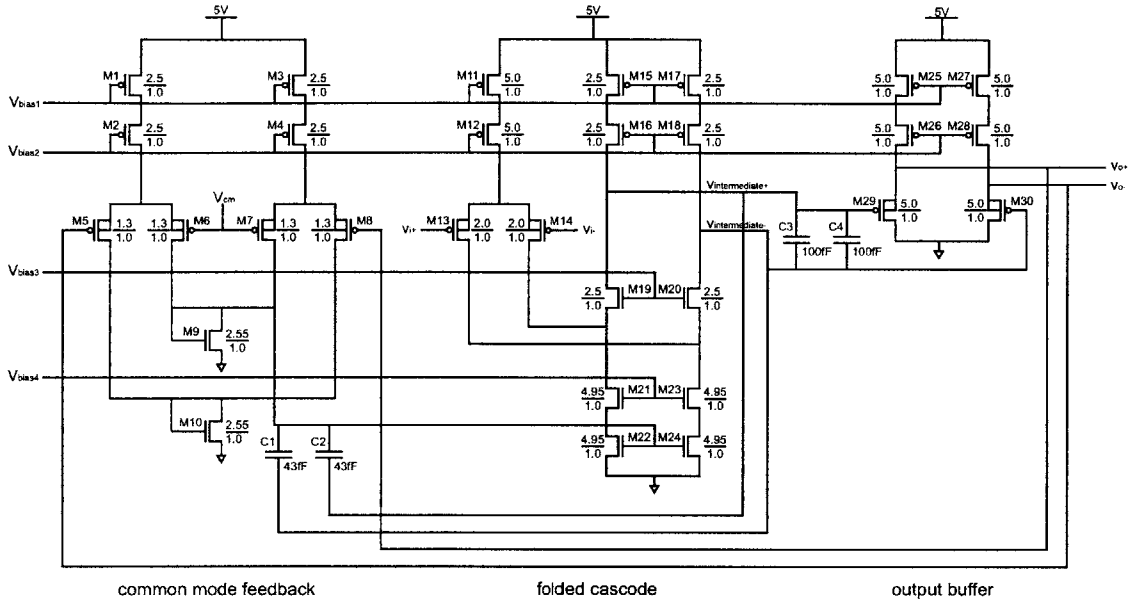
design will likely introduce errors.

The third design (Figure 5-7c) is a semi-differential design that is a combination of the above two designs. Like the first design, the outputs are taken from across the integrating capacitor to avoid the offset problem and ensure the highest level of accuracy. And like the second design, the input node is the same as the positive op amp input, allowing a very small input impedance. This semi-differential design is a compromise between the benefits of a fully differential circuit, and the requirements that minimize error. This semi-differential output is easily adjusted to a fully differential signal in the next stage (see Section 5.2).

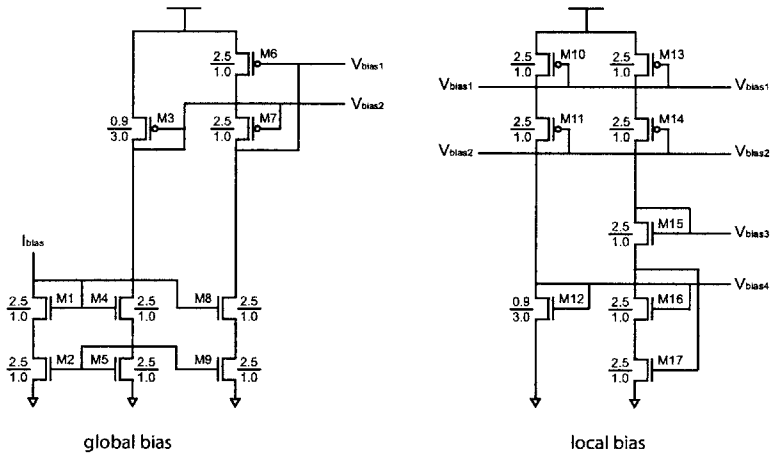
Figure 5-8 summarizes the three designs discussed in this section.

5.1.4 Op Amp Design

The op amp for the Transimpedance Stage requires high gain, an output buffer, and common mode feedback. The open loop gain of 2,500 is achieved using a single gain stage, folded-cascode topology. The input pair and the top cascode yields a transimpedance gain of $g_m^2 r_o^2$, and is biased to optimize the transistors' g_m and r_o (shown in Figure 5-9). The high gain is required for a small Transimpedance Stage input impedance (as mentioned in Section 4.1 and Section 5.1.3). In Section 5.1.3, the input impedance was estimated to be zero in comparison to the gigaohms of the



a)



b)

Figure 5-9: a) Op Amp for the Transimpedance Stage. b) Bias Circuitry. V_{CM} is supplied externally.

OPD output resistance. The following derives a more exact answer as a function of the op amp gain. The input impedance is approximated as the change in voltage due to a small change in input current (like Equation 5.6).

$$R_{in} = \frac{\partial v_{in}}{\partial I_{in}} = \frac{\partial v_{opamp,i+}}{\partial I_{in}} \tag{5.11}$$

In the Transimpedance Stage (see Figure 5-2, a simplified diagram is shown in Figure 5-7c), note that the node voltage v_{in} is the same as $v_{opamp,i+}$. The relationship between the op amp output voltages ($v_{opamp,o+}$ and $v_{opamp,o-}$) and the input current is:

$$v_{opamp,o+}(I_{in}, t) \approx 2.5 + \frac{I_{in}t}{C} \tag{5.12}$$

$$v_{opamp,o-}(I_{in}, t) \approx 2.5 - \frac{I_{in}t}{C} \tag{5.13}$$

The relationship between the op amp input voltages ($v_{opamp,i+}$ and $v_{opamp,i-}$) and the input current can then be derived.

$$\begin{aligned} A v_{opamp,i_{diff}} &= v_{opamp,o_{diff}} \\ A(v_{opamp,i+} - v_{opamp,i-}) &= v_{opamp,o+} - v_{opamp,o-} \\ v_{opamp,i+} &= \frac{2}{A}\frac{I_{in}t}{C} + v_{opamp,i-} \end{aligned} \tag{5.14}$$

Finally,

$$R_{in} = \frac{2}{A}\frac{t}{C} \tag{5.15}$$

where A is the op amp dc gain. Thus, with high gain, the input impedance will be low. In this case, the worst case input impedance (t=duration of the gain phase=25μs) is 8kΩ, which for this application is relatively small (for the small range of input currents I_{in} = 0-10nA, v_{in} only varies over 80μV). This means that the Transimpedance Stage (and hence the Current Sensing Amplifier) input resistance does not significantly affect the signal current from the organic photodetector ($R_{out,OPD}$ = ~2GΩ $\gg$ 8kΩ = $R_{in,CSA}$).

The output buffer in the op amp is necessary for a low output impedance. The negative op amp output node must sink the constant input current in steady state (see Figure 5-2 & 5-7). Without a low output impedance, the output voltage of the op amp will be distorted by the steady state current flowing into the positive output node. With a folded cascode topology, the output impedance without a buffer will be extremely high, 10-100MΩ; thus even a 1nA current going into the op amp will result in a 10-100mV change in voltage. A common drain output buffer is implemented to ameliorate this effect.

Due to a low output impedance, the feedback and load capacitors no longer act as compensation capacitors. Since the Transimpedance Stage is a closed-loop feedback system in itself, it must be stabilized by dominant pole compensation in the op amp. Thus, compensation capacitors are added between $v_{intermediate+}$ and $v_{intermediate-}$. This node is a high impedance node; furthermore, these capacitors are Miller multiplied by a factor of 2. This allows the dominant pole to be implemented easily with small capacitors. The op amp is compensated with a 3dB frequency of 2.4kHz (yielding a 3dB point at 6MHz under unity gain configuration).

Lastly, the op amp also has common mode feedback to control the output common mode at 2.5V, as the subsequent stages are optimized for such a common mode. Since common mode feedback is again feedback, the loop must be stable. Thus, compensation capacitors are again inserted to stabilize the minor loop (see Figure 5-9).

5.2 Gain Stage

The 10× gain stage is implemented as a straight forward switch capacitor circuit using a closed-loop op amp. The design is shown in Figure 5-10. It is a fully differential circuit with several measures to decrease error. Input offset cancellation is important in this design as it can otherwise result in an output error equal to the input offset multiplied by the gain. During one phase, the circuit performs the voltage gain with

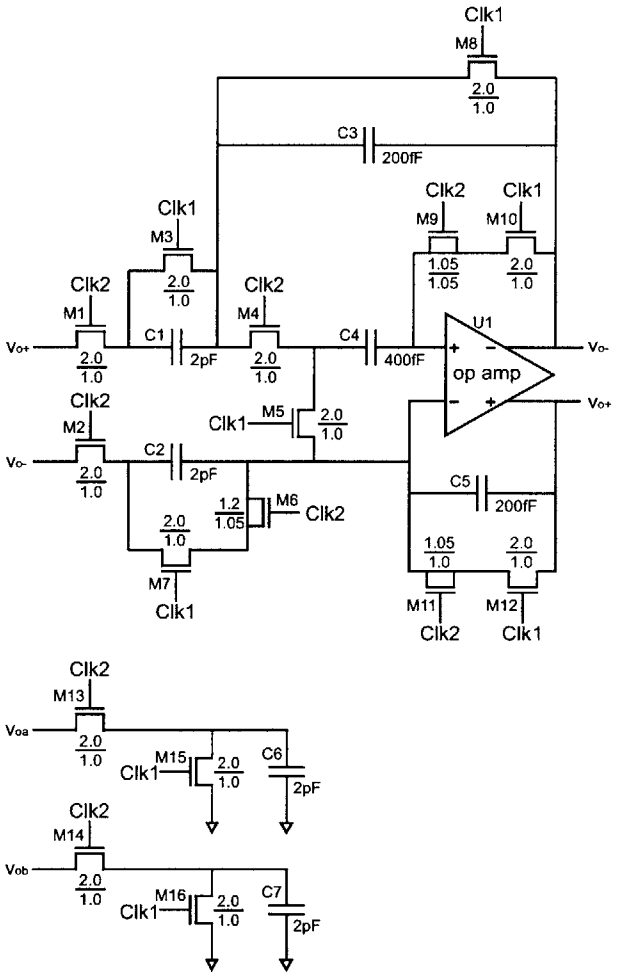


Figure 5-10: Gain Stage Circuit Diagram. Clk1 and Clk2 are non-overlapping clocks corresponding to the reset phase and gain phase respectively.

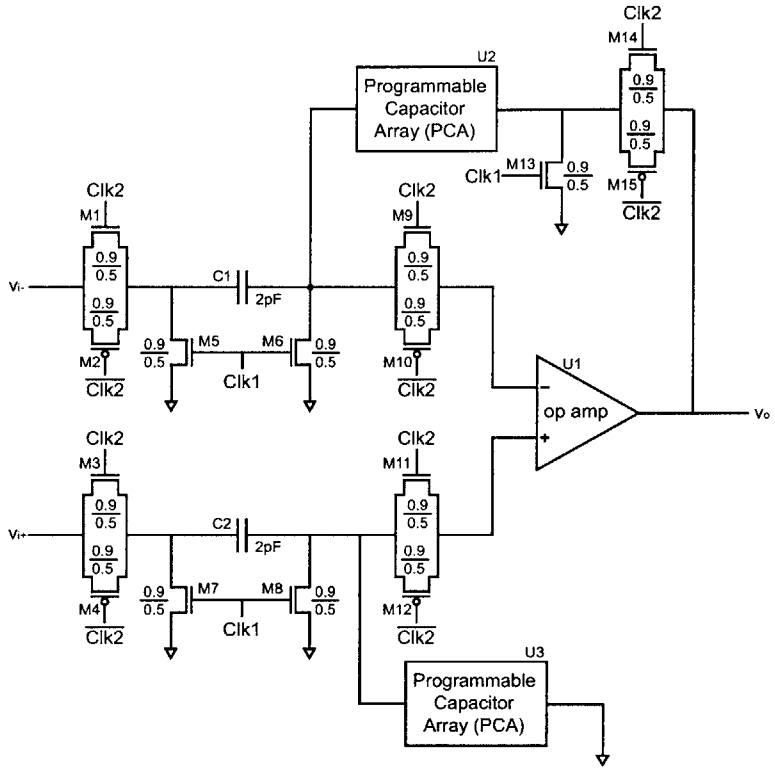
input offset cancellation. During the other phase, the capacitors are reset and the input offset is sampled for input offset cancellation. Charge injection could also create significant error in the output. To decrease this effect, capacitor sizes were chosen as large as possible within reasonable area considerations. And transistors M6, M9, and M11 were inserted to "sink/source" the problematic gate charges. Lastly, when a semi-differential signal is passed into the input, the common-mode feedback within the op amp forces the output to become fully differential. A fully differential output holds the common mode constant, eliminating a potential signal dependent error in the next stage.

Note that the output of the Transimpedance Stage has 4 terminals (see Section 5.1). Even though two of these signals are later discarded, the Gain Stage must present matched capacitive loads for stability reasons. Figure 5-10 also shows these circuits.

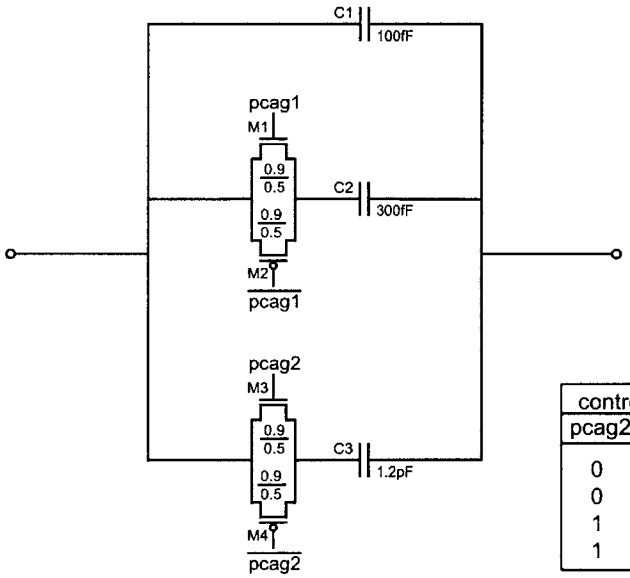
The op amp design for the Gain Stage requires high gain and common mode feedback; however, it does not require an output buffer. For this circuit in steady state, the op amp does not have to sink any current. Thus, low output impedance, and hence an output buffer, is not necessary. With the buffer removed, the feedback capacitors are sufficient to serve as compensation capacitors to provide a dominant pole for the op amp. The op amps for the Gain Stage and the Transimpedance Stage were similarly designed for easier implementation. The op amp circuit is the same as Figure 5-9, but without the output buffer; common mode feedback is also done using the outputs directly from the cascode ($v_{intermediate+}$ and $v_{intermediate-}$ in Figure 5-9). Refer to Section 5.1.4 for more details on the other parts of the op amp.

5.3 Differential to Single-ended Conversion Stage

This conversion stage is necessary for easy comparison in the Summing Junction Block. The Summing Junction only takes in two inputs, one of which is the desired brightness v_{brt}, leaving only one input for the actual brightness level v_{act}. In addition



a)



control lines		feedback	gain
pcag2	pcag1	capacitance	value
0	0	100fF	20x
0	1	400fF	5x
1	0	1.3pF	2/1.3x
1	1	1.6pF	1.25x

b)

Figure 5-11: a) Differential to Single-ended Conversion Stage Circuit Diagram. b) Programmable Capacitor Array. Clk1 and Clk2 are non-overlapping clocks corresponding to the reset phase and conversion phase respectively.

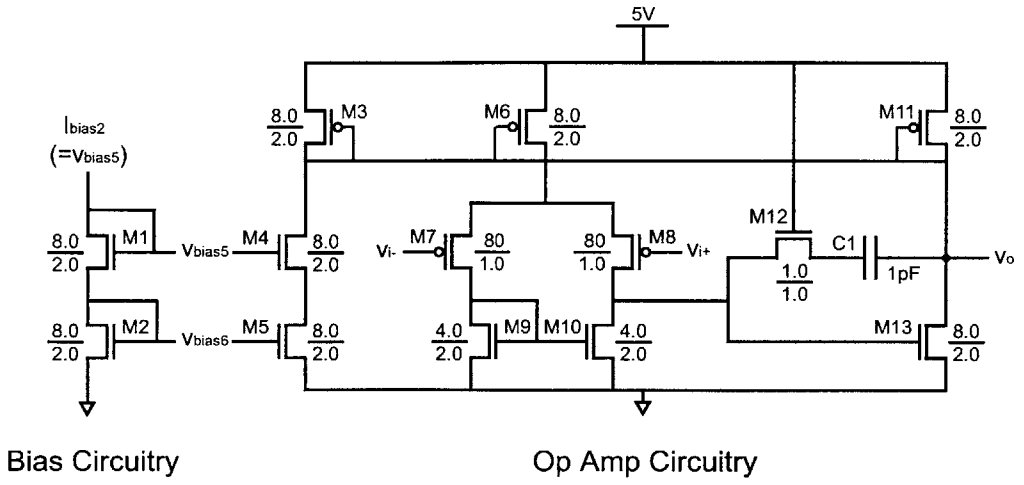


Figure 5-12: Op Amp for the Differential to Single-ended Conversion Stage. This op amp is also used in the Sample and Hold Stage.

to the conversion, this stage also incorporates a 5× gain (see Figure 5-11a). The differential input signal has a 1V swing; v_{i+} ranges from 2.5-3.0V and v_{i-} ranges from 2.5-2.0V. Thus, a gain of 5 will amplify the signal to the desired 5V output swing. The gain for this stage will be set to a default of 5×. Should the OPD prove to require a different gain from the CSA, the Programmable Capacitor Array (see Figure 5-11b) can be used to adjust the gain of this stage among four discrete values. Using two control lines, switches can connect various feedback capacitors to obtain gains of 1.25×, $\frac{2}{1.3}$×, 5×, or 20×. Couple this gain programmability with the continuously tunable gain of the Transimpedance Stage, the Current Sensing Amplifier can now attain a gain anywhere between 62.5 MΩ $\sim$ 4 GΩ.

A completely different op amp (from that in the Transimpedance Stage and Gain Stage) is required for the Differential to Single-ended Conversion Stage. The outputs of the prior stages only need to swing at most 1V. For this stage however, 0-5V rail-to-rail output swing is required. In addition, this op amp only needs to be single-ended, which greatly reduces the circuit complexity since it eliminates the need for common mode feedback. Figure 5-12 shows the op amp design, which consists of a differential input stage followed by a common source gain stage. An output buffer is

not necessary and thus omitted.

5.4 Sample and Hold Stage

The Sample and Hold Stage (shown in Figure 5-13) is necessary for output sampling. The signals in the previous stages are constantly changing and only reach the correct value at the end of the gain phase (ϕ_2), and the reset phase (ϕ_1) conveys no data. Thus, the output must be sampled at an instantaneous point at the end of ϕ_1 (see Figure 5-13). The Sample and Hold samples at the end of $\phi 2$ and holds for $\phi 1$; and thus supplies an entire window (the duration of $\phi 1$) for the application to sample the CSA output signal. With a constant input to the next stage, it also allows more time for the downstream stages in the Summing Junction and Compensator to settle to the correct values. Figure 5-14 shows sample waveforms for the signals before and after the Sample and Hold.

The Sample and Hold Stage must be able to accept inputs from 0-5V. With a closed-loop op amp implementation, the design must keep both inputs to the op amp in the high gain region. With inputs to the op amp too high or too low, the transistors leave the saturation regime and the op amp characteristics plateau. The design shown in Figure 5-13 prevents this by keeping the op amp inputs near 2.5V, the center of the high gain region. A necessary, and desirable, result of this design is that the signal becomes inverted. The inversion is used to cancel the inversion in the organics, as explained in Section 3.2.2.

The op amp design for the Sample and Hold Stage is the same as the op amp design for the Differential to Single-ended Conversion Stage as the specifications are identical. See Section 5.3 and Figure 5-12 for details on op amp design.

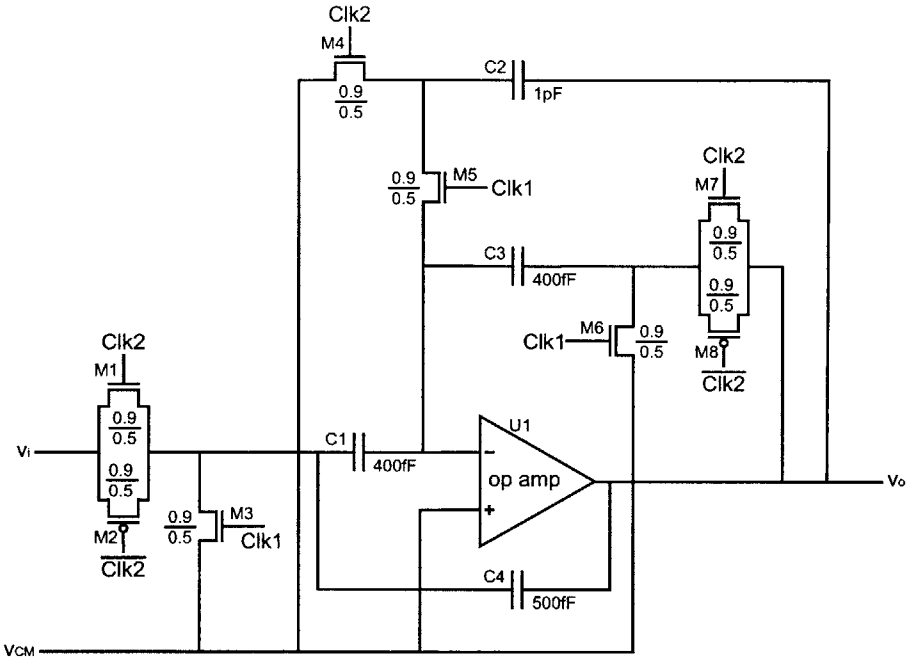


Figure 5-13: Sample and Hold Stage Circuit Diagram. Clk1 and Clk2 are non-overlapping clocks corresponding to the hold phase and sample phase respectively; V_{CM} is supplied externally.

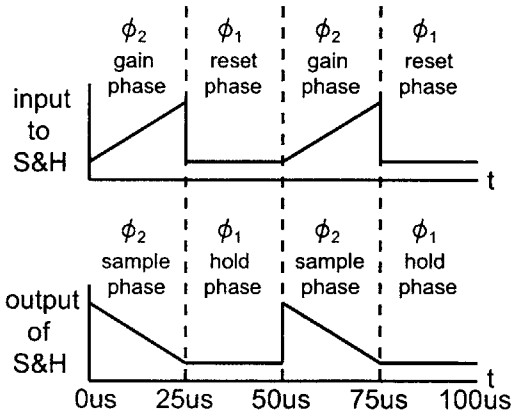


Figure 5-14: Typical Waveforms for the Inputs and Outputs of the Sample and Hold Stage.

Chapter 6

Integrated Silicon Chip Overview

This chapter briefly describes the fabricated chip, which consists in part of the Current Sensing Amplifier.

6.1 Channel Array

The Current Sensing Amplifier (CSA) combined with the Summing Junction and the Compensator forms a single channel (see Figure 3-1 and 6-1). The channel starts with the input I_{in} from the OPD, and ends with the output v_{drive} to the OLED Pixel (see Figure 6-1). A variable gain in the CSA allows fine tune adjustments to the gain. And a variable pole in the Compensator provides a tunable time-domain response. The CSA is described in detail in Chapter 5. The Summing Junction and Compensator are discussed in Lamba's thesis[6].

The integrated silicon chip contains 16 of these channels so that it can perform feedback for 16 columns of the display simultaneously (see Figure 6-2). For a larger

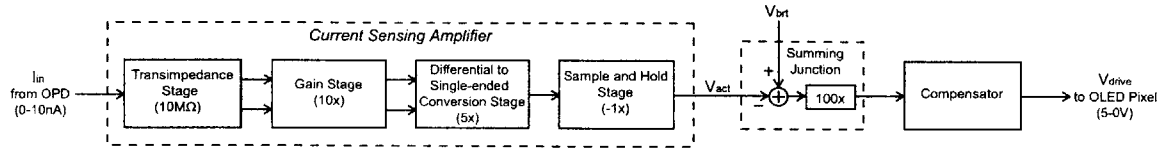


Figure 6-1: Block Diagram of a Single Feedback Channel.

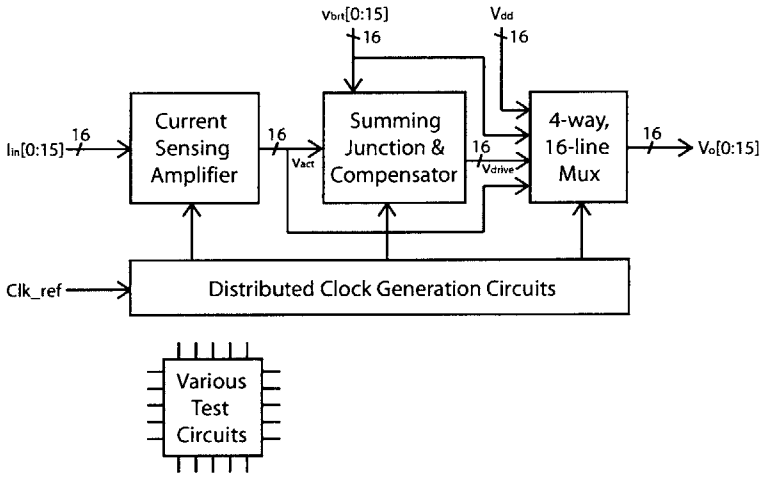


Figure 6-2: Summary Diagram of Entire Silicon Chip. Main signal paths are shown; control lines are omitted.

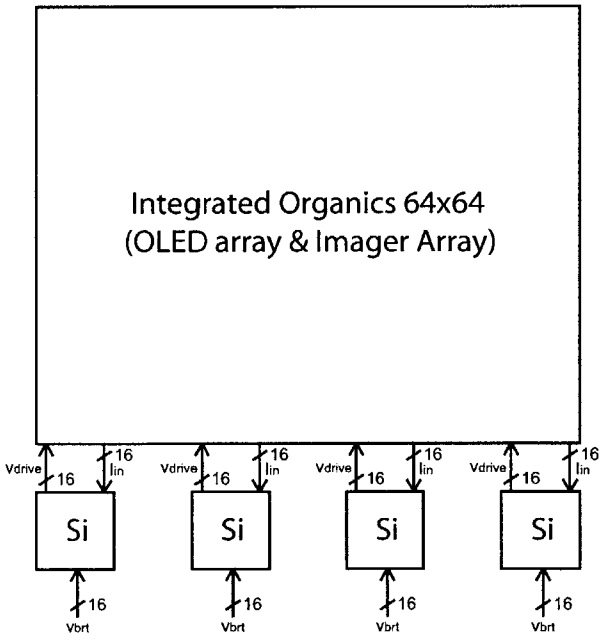


Figure 6-3: Overall System Architecture Illustrating a Silicon Chip for Every 16 Columns. Other I/O lines, voltage converters, and details omitted.

64 × 64 display, several chips can be used as shown in Figure 6-3. This architecture allows for display scalability; there are no fundamental design limitations to how many rows or columns the display can have. Note that the same architecture and benefits are applicable to a stand-alone organic imager (see Section 6.2 for imager mode operation of the silicon chips).

6.2 Multi-mode Operation

In addition to the basic channel array, the chip features a muxing array for multi-mode operation. A multiplexing (mux) array chooses between four sets of signals for output from the chip (see Figure 3-1 & 6-2):

1. V_{dd}, the power rail
2. v_{brt}, the adaptor input
3. v_{drive}, the feedback output
4. v_{act}, the CSA output

Figure 6-2 also shows these muxing circuits. Figure 6-4 tabulates the control signals for mode selection.

Mode	Control Lines		Output Signal	Operation Mode
	Mux0	Mux1		
1	0	0	V_{dd}	Display Off
2	0	1	V_{brt}	Adaptor Feedthrough; Feedback Off
3	1	0	V_{drive}	Feedback Control
4	1	1	V_{act}	Imager

Figure 6-4: Table of Silicon Chip Modes of Operation.

Mode 1 sets all outputs to V_{dd} (5V), which will force the display to turn off despite controls from the display adaptor. Mode 2 turns off the optical feedback by allowing

the display adaptor to directly control the display. For an OLED display suffering degradation, direct adaptor control yields poor, non-uniform results. Thus; Mode 2 allows an assessment of the improvement the optical feedback solution offers. Mode 3 performs the feedback necessary for the optical feedback OLED display described throughout this thesis (shown in Figure 3-1). Mode 4 allows an application to use the chip to process the outputs of an imaging or sensor array. With just the silicon chips and organic imager array described in Chapter 4, they together serve as a standalone imager.

6.3 Additional On-chip Circuits

Lastly, the chip also contains clock generation circuitry for the four required switch capacitor clock signals and several test circuitry to allow debugging of individual blocks and sub-blocks. The die photo is shown in Figure 6-5.

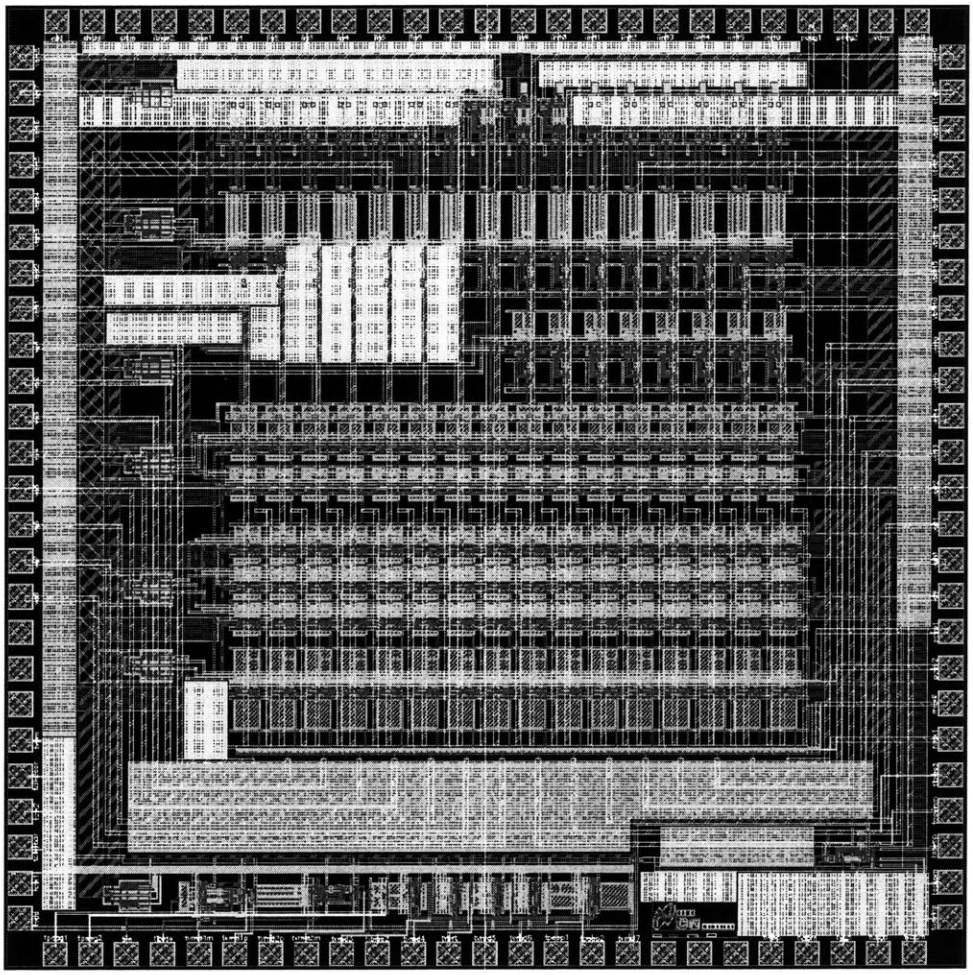


Figure 6-5: Silicon Chip Die Photo. The die size is 4mm $\times$ 4mm.

Chapter 7

Results

7.1 Simulation Results

The Current Sensing Amplifier design was thoroughly tested in Cadence using the Spectre simulator. The process used for design and testing was the National Semiconductor CMOS7_5V 0.35μm 5V process. The results are detailed below.

7.1.1 Typical Waveforms

In these tests, the input-output characteristics of the overall Current Sensing Amplifier system were simulated. As illustrated in Figure 5-1, I_{in} is the input current and is varied as a parameter over a suitable range. The output V_{out} (also known as V_{act}) was then recorded for each input.

Figure 7-1 illustrates typical V_{out} waveforms for I_{in} of 0nA, 5nA, and 10nA. Also shown is the reference clock (Clk_{in}). During phase $\phi 1$, the Transimpedance Stage, Gain Stage, and Differential to Single-ended Conversion Stage are all in reset mode, during phase $\phi 2$, they are in gain mode. It is also during $\phi 2$ when the Sample and Hold Stage samples the value. Once sampled, the value is then held in $\phi 1$. Thus, for the application to read the correct value, it should sample V_{out} in phase $\phi 1$, which corresponds to the low level of the input reference clock.

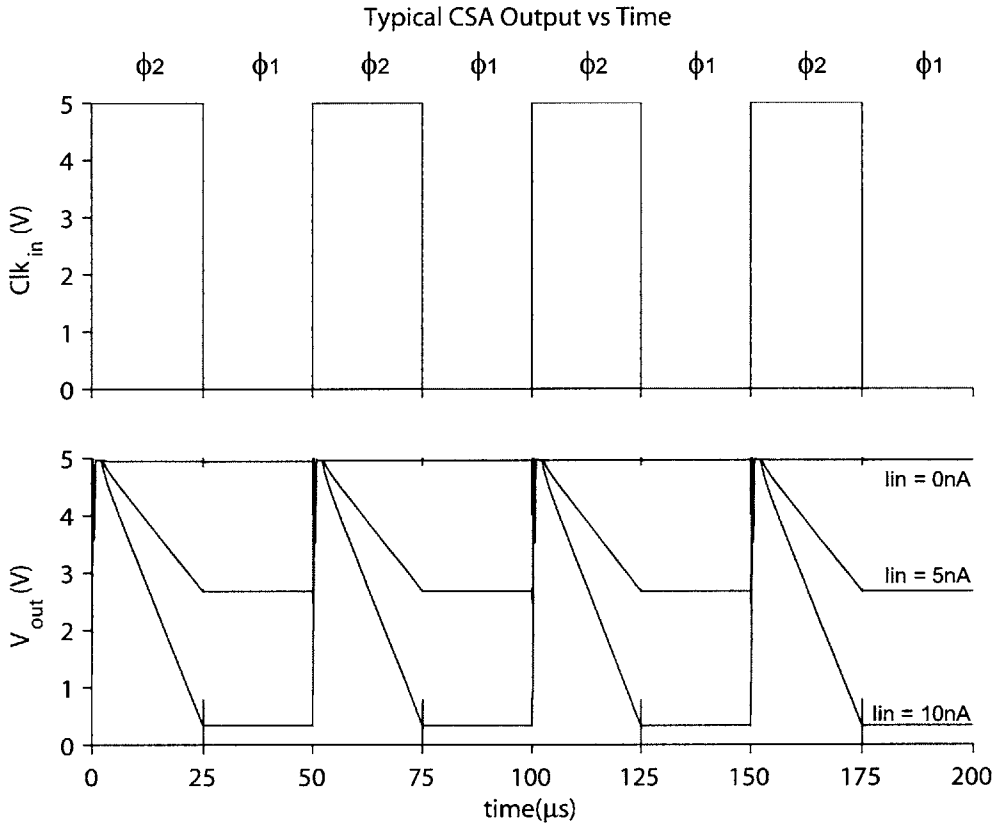


Figure 7-1: Typical Simulation Output Waveforms for the Current Sensing Amplifier. Clock period was set to 50μs, with a 50% duty cycle; and the gain mode in the Differential to Single-ended Conversion Stage was set at $5\times$. The top plot shows the reference clock, Clk_{in}. The bottom plot shows three output waveforms corresponding to an I_{in} of 0nA, 5nA, and 10nA.

7.1.2 Varying Gain Modes

As discussed in Section 5.3, the Differential to Single-ended Conversion Stage has 4 gain modes - 1.25×, 1.54×, 5×, and 20×. These modes can be toggled by adjusting two control inputs, $pcag1$ and $pcag2$. Figure 7-2 shows the simulated CSA characteristics for the different gain modes.

When the Programmable Gain in the Differential to Single-ended Conversion Stage is set to 1.25×, the CSA should have an ideal overall transimpedance gain of 125 MΩ. The simulation data shows a linear gain of 114 MΩ. Again, when the Programmable Gain is set to 1.54×, 5×, and 20×, the ideal CSA gains should be 154 MΩ, 500 MΩ, and 2 GΩ, respectively. The simulation data shows corresponding gains of 142 MΩ, 469 MΩ, and 1.85 GΩ. These results are summarized in Figure 7-3.

The discrepancy between the simulated gain and the ideal gain mainly arises from an "integration duration offset". In the Transimpedance Stage, the gain is proportional to the integration time, i.e. the duration of $\phi 2$ when the input current i_{in} is being integrated over the feedback capacitor. In these tests, Clk_{in} was set such that $\phi 1 = \phi 2 = \frac{T_{clk}}{2} = 25\mu s$ (50% duty cycle). However, due to non-idealities and settling times, the input current I_{in} is actually only being integrated for approximately $\frac{T_{clk}}{2}$ - $1.5\mu s$. Notice, in Figure 7-1, the slight delay after the clock edge before current integration onto the integration capacitor actually begins. Thus, the simulated gains are slightly lower than the ideal gains under ideal conditions. Figure 7-3 also shows the calculated CSA gain with the "integration duration offset" taken into account. These values match the simulated results much better.

This offset effect illustrates the benefit of the proposed design. This CSA has a continuously tunable gain (see Section 5.1) across 8× above and below the center gain of 500 MΩ. Thus, by adjusting the period of the reference clock the exact desired gain can be obtained. The next section illustrates how adjusting the clock period can adjust the overall CSA gain.

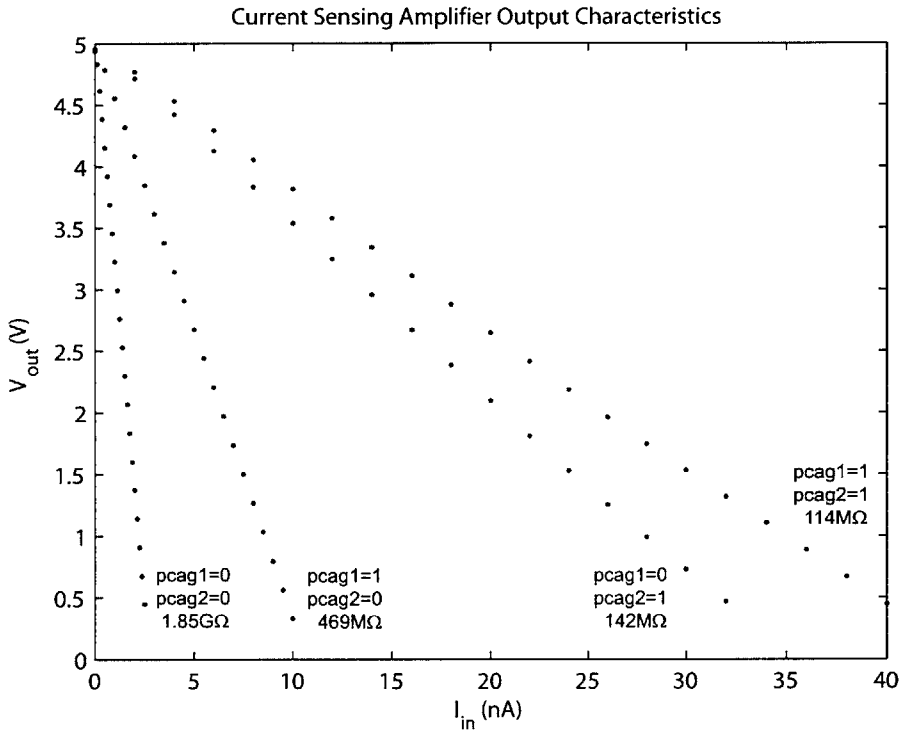


Figure 7-2: Simulated CSA Characteristics with Varying Gain Modes. The Programmable Gain in the Differential to Single-ended Conversion Stage was varied over the four possible values of 1.25×, 1.54×, 5×, and 20×. The clock period was set to 50μs with a 50% duty cycle. Shown next to each trace are the Programmable Gain settings and the overall CSA transimpedance gain.

Summary of Simulation Results for Various CSA Operating Configurations

Programmable Gain			T_{clk} (μs)	Ideal CSA Gain (MΩ)	Observed CSA Gain (MΩ)	Theoretical Gain Considering "Integration Duration Offset" Effect (MΩ)
gain	pcag1	pcag2				
1.25x	1	1	50	125	114	117
1.54x	0	1	50	154	142	145
5x	1	0	50	500	469	470
20x	0	0	50	2000	1850	1880
5x	1	0	25	250	225	220
5x	1	0	100	1000	957	970

Figure 7-3: Table Summarizing the CSA Simulation Results.

7.1.3 Varying Clock Period

Section 5.1 describes how the Transimpedance Stage can tune to *any* gain in the 5-20 MΩ range by adjusting the clock period. This design provides the CSA with its feature of continuous gain configurability. Typically, the period of the clock is set to 50μs (50% duty cycle, 25μs integration time) to achieve a gain of 500 MΩ. However, the clock period can be adjusted (recommended range is a factor of 2 above and below 50μs) to increase the gain up to double or decrease the gain down to half. Figure 7-4 shows the simulation results of adjusting the Clk_{in} period.

For a Clk_{in} period of 25μs, 50μs, and 100μs (and the Programmable Gain of the Differential to Single-ended Conversion Stage set to the center value of 5×), the CSA should have an ideal transimpedance gain of 250 MΩ, 500 MΩ, and 1 GΩ, respectively. The corresponding simulated gains were 225 MΩ, 469 MΩ, and 957 MΩ. These results are summarized in Figure 7-3.

As mentioned in the previous section, there are slight discrepancies between the ideal gain and the simulated gain, which are caused by the "integration time offset". Figure 7-3 also shows the calculated CSA gain with the "integration duration offset" taken into account. These values match the results much better. The next section shows how to overcome these slight inaccuracies to tune to a specific desired overall CSA gain.

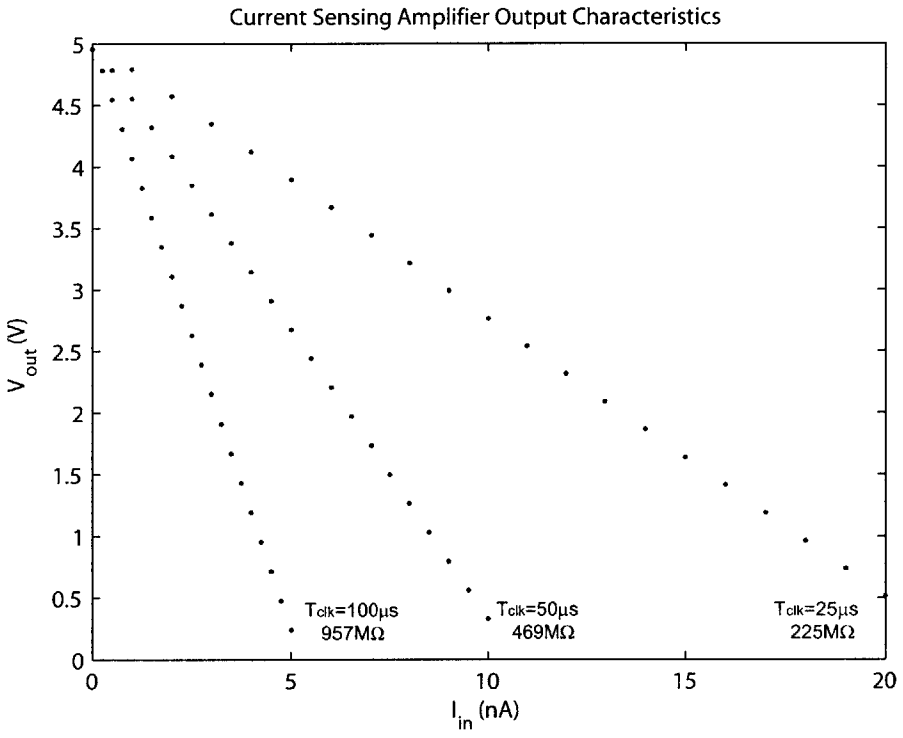


Figure 7-4: Simulated CSA Characteristics with Varying Clock Period. The periods shown are 25μs, 50μs, and 100μs with a 50% duty cycle. The period can be chosen to be anything within the 25$\sim$100μs range, limited only by the accuracy of the signal generator. Shown next to each trace are the clock period (with 50% duty cycle) and CSA transimpedance gain in Ω.

7.1.4 Arbitrarily Tunable Gain

By using both adjustment techniques described previously, the CSA can tune to any gain in the 62.5 MΩ to 4 GΩ range. As an illustration, three precise gains were chosen for CSA configuration. First, the required gain of 500 MΩ for the Optical Feedback OLED Display was chosen, then two other values were chosen arbitrarily - 1.2 GΩ to test the higher end of the gain range and 375 MΩ to test the lower end of the gain range). To achieve these gains, the Programmable Gain and the clock period were chosen appropriately with the following in mind (assuming 50% duty cycle):

1. The only options for the Programmable Gain are 1.25×, 1.54×, 5×, and 20×.
2. T_{clk} can be anything in the range of 25μs$\sim$100μs.
3. The overall CSA gain is 2 million × T_{clk}(in μs) × Programmable Gain.
4. The actual Clk_{in} period will have to be compensated for the "integration duration offset" effect by adding 1.5μs×2=3μs to the desired T_{clk}.

Figure 7-5 shows the simulation results. All results are within 1% of the desired value with an average input-referred offset of 48pA. In theory, there is no limit to the accuracy of the CSA gain with respect to the desired gain. However, in reality, signal generators have limited accuracy in generating a clock of a certain period. In these tests, it was assumed that the signal generator does not have arbitrarily large accuracy, but rather an accuracy of only up to 3 significant figures. If, on the other hand, a signal generator of higher accuracy were used, the results will improve to match the desired gain more closely.

In summary, the simulation results demonstrate a fully functional, high-gain, continuously tunable Current Sensing Amplifier with great accuracy as specified.

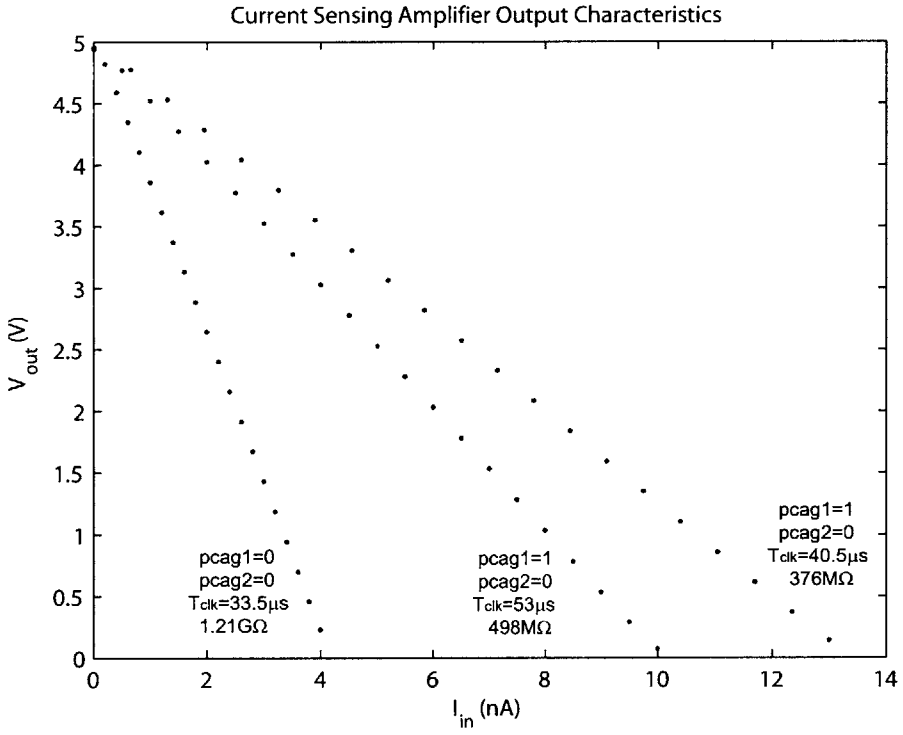


Figure 7-5: Simulated CSA Characteristics for Three Desired Gains. The Programmable Gain and the clock period were adjusted to configure the CSA to have exact gains of 1.2 GΩ, 500 MΩ, and 375 MΩ. All periods were chosen to 3 significant figures. All actual gains were within 1% of the desired gain (accuracy limited only by the accuracy of the clock period as generated by the signal source). Shown next to each trace are the Programmable Gain settings, the clock period (with a 50% duty cycle), and the overall CSA gain.

7.2 Measurement Results

The Current Sensing Amplifier design was fabricated (as detailed in the chip design in Chapter 6) using the National Semiconductor CMOS7_5V 0.35μm 5V process. The measurement results are detailed below.

7.2.1 Testing the Main Channels

The fabricated chip contains 16 main channels (see Chapter 6); the measurement results from these channels are documented in this section. The chip was configured to operate in Imager Mode (see Chapter 6) and the Programmable Gain was set to 5×. The output always railed to around 0V despite varying the input current I_{in}. Railing to 0V corresponds to a large positive offset (output-referred). Typical curves are shown in Figure 7-6. To understand the source of the offset, the shape of the waveform is analyzed (see Figure 7-6).

The spike in the beginning of the sample phase conveys a lot of information regarding the operations of the stages in the CSA. Figure 7-7 illustrates why the spike results. The top graph shows the input V_{in} to the last stage of the CSA, which is the Sample and Hold Stage. This input comes from the Differential to Single-ended Conversion Stage and the V_{in} signal rails high at 5V. The middle graph shows the

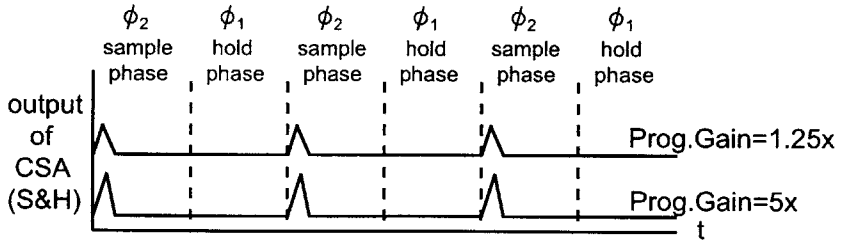


Figure 7-6: Typical Waveforms Observed in the Main Channel CSA in Measurement Tests. The main channel was configured for Imager Mode with a Programmable Gain of 5× to measure the results of the CSA in the main channel. The results showed that despite the input current I_{in}, the output always railed to ~0V, implying a large offset. By analyzing the waveform shape, and by adjusting the Programmable Gain, the offset source was isolated to the first two stages of the CSA.

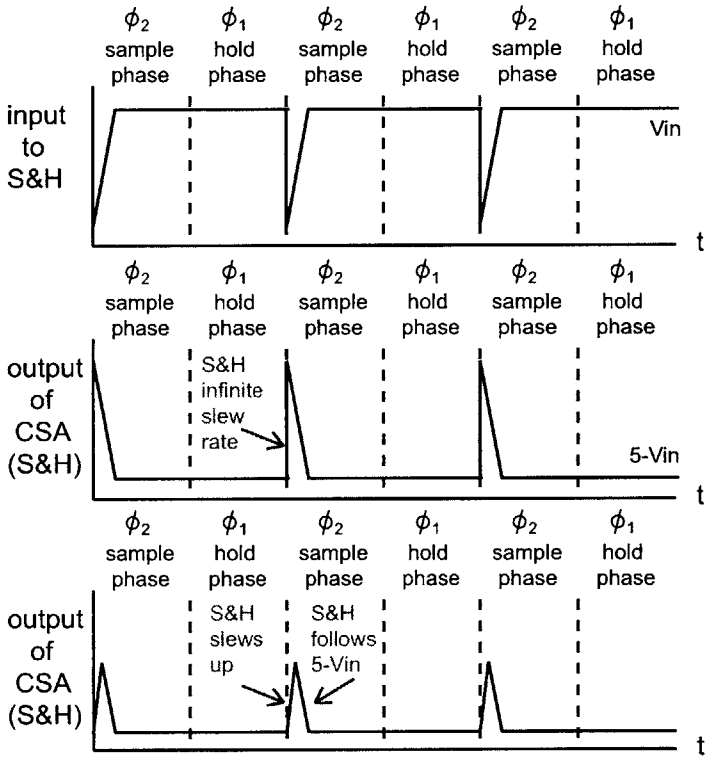


Figure 7-7: Illustration of Spike Occurrence. The top graph shows the input to the Sample and Hold. The middle graph shows the output perfectly following $5 - V_{in}$, the designed output, if the Sample and Hold Stage had infinite slew rate. The bottom graph shows the Sample and Hold output with a finite slew rate, which results in the characteristic spike observed.

output of the CSA with an ideal Sample and Hold of infinite slew rate. The Sample and Hold computes $5 - V_{in}$ and holds it. So during the sample phase, the Sample and Hold follows the input perfectly well (it actually follows $5 - V_{in}$). The bottom graph shows the Sample and Hold with a finite slew rate. First, the sample and hold slews up from 0V (the previously held value) to meet the $5 - V_{in}$ curve, which it then follows back down to rail at 0V again. Thus, the occurrence of the spike is natural and expected.

The spike implies that the Sample and Hold Stage is functioning correctly and is not the stage causing the large offset (sampling function is following correctly, and hold function is holding correctly). Furthermore, when the Programmable Gain is switched to 1.25× in the Differential to Single-ended Conversion Stage, a large offset is still observed (see Figure 7-6). This hints that the large offset is caused by a stage upstream of the Differential to Single-ended Conversion Stage, either the Transimpedance Stage or the Gain Stage, and then amplified in the downstream stages to cause railing. By examining the test channel, more can be learned.

7.2.2 Testing the Test Channel

The chip also contains a test channel, which includes a CSA with all intermediate nodes between stages pulled to pads. This allows each stage to be examined individually. The measurement results from each stage follow.

A typical waveform from the Transimpedance Stage is shown in Figure 7-8. The Transimpedance Stage has a large offset, which can range from 0.1V to 0.7V (output-

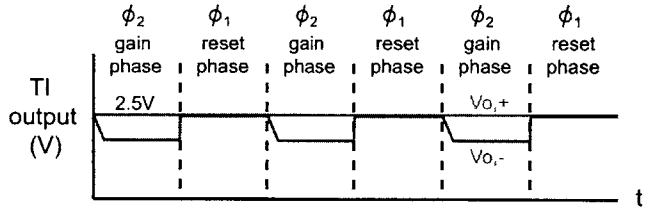


Figure 7-8: Typical Waveforms from the Transimpedance Stage Showing a Large Output Offset.

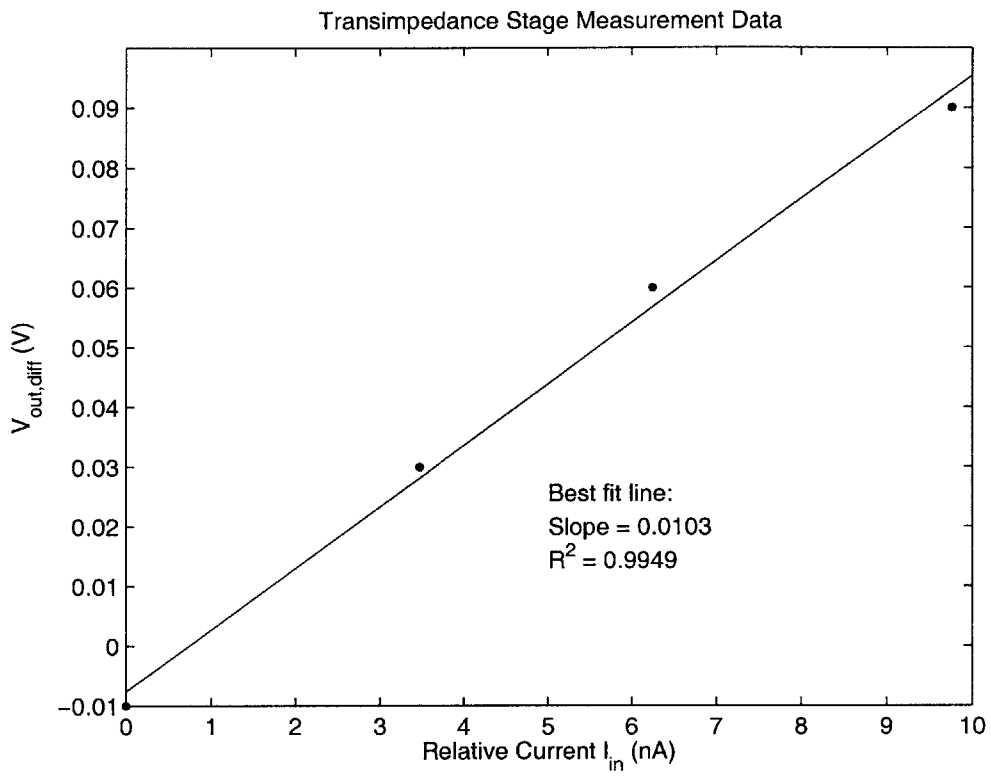


Figure 7-9: Measurement Results from the Transimpedance Stage in the Test Channel. The results demonstrate functionality and accurate gain despite a large offset. To best illustrate the functionality despite offset, the measurement data is plotted as the change in output voltage for a change in input current.

referred) over different chips. The large positive offset seen before in the main channel can now be ascribed to the Transimpedance Stage. Even though the stage has a large offset, it has functionality. Figure 7-9 shows measurement data illustrating the transimpedance gain of the Transimpedance Stage, while ignoring the offset (by plotting the differential output as a function of the differential input). The measured gain is 10.3 MΩ, which is quite close to the desired gain of 10 MΩ (Figure 7-13 summarizes these results). Thus, the Transimpedance Stage has functionality and the correct gain, but has a large offset that causes subsequent stages to rail.

Figure 7-10 shows measurement data from the Gain Stage. The measured input-output characteristic shows the Gain Stage operating quite well according to specifi-

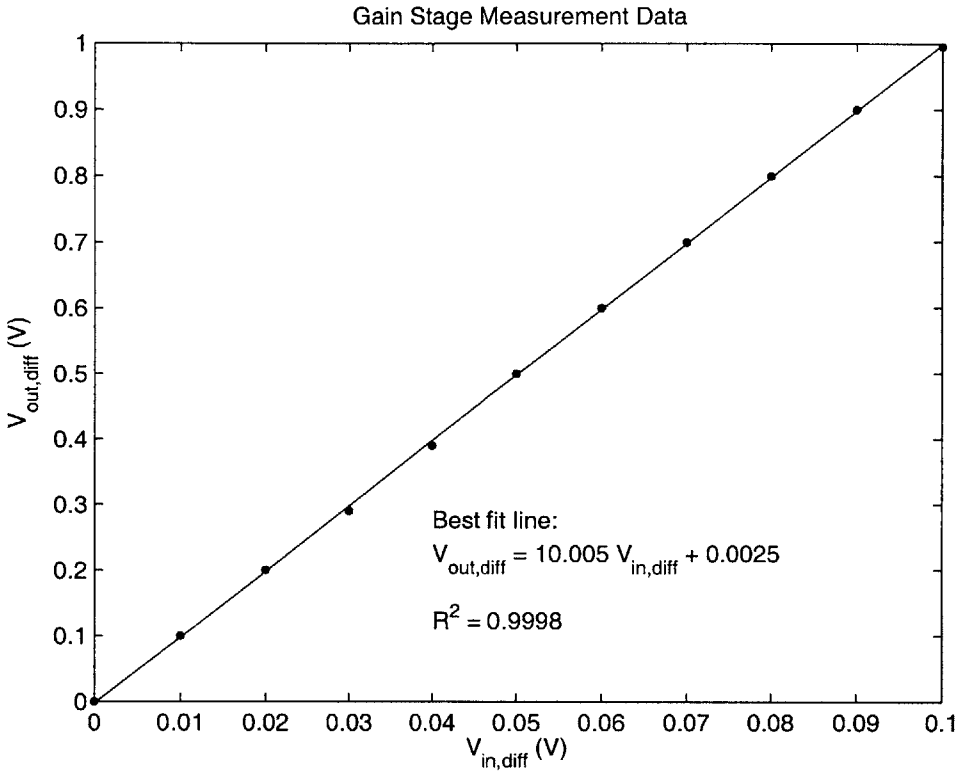


Figure 7-10: Measurement Results from the Gain Stage in the Test Channel. The results verify the functionality and performance of the Gain Stage.

cations. The characteristic is very linear with a gain of 10.005× and an input referred offset of -0.25mV. The results are summarized in Figure 7-13.

Next, Figure 7-11 illustrates the measured characteristics of the Differential to Single-ended Conversion Stage with the Programmable Gain set to 5×. The stage ideally should have rail-to-rail swing with a linear gain of 5×. The measurment data shows a very linear gain, but only at 4.777×. In addition, the stage has an output range from 0.18V to 4.92V and an input offset of -40mV. The reason for the gain inaccuracy is detailed in Section 7.2.3. The results of this stage are summarized in Figure 7-13.

The Sample and Hold Stage was designed to have an inverting unity gain, meaning $V_{out} = 5 - V_{in}$. Figure 7-12 shows data measured from the Sample and Hold Stage in the test channel. The results show a linear gain of -1.002× and an input-referred

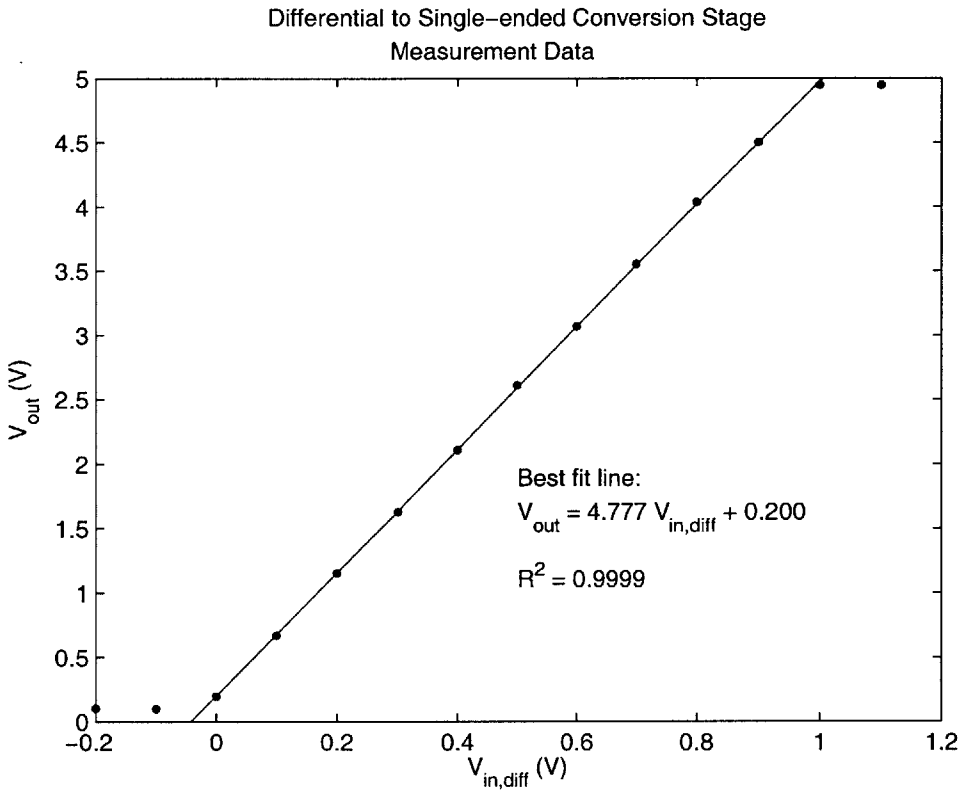


Figure 7-11: Measurement Results from the Differential to Single-ended Conversion Stage in the Test Channel. The results show functionality with a small gain error and offset.

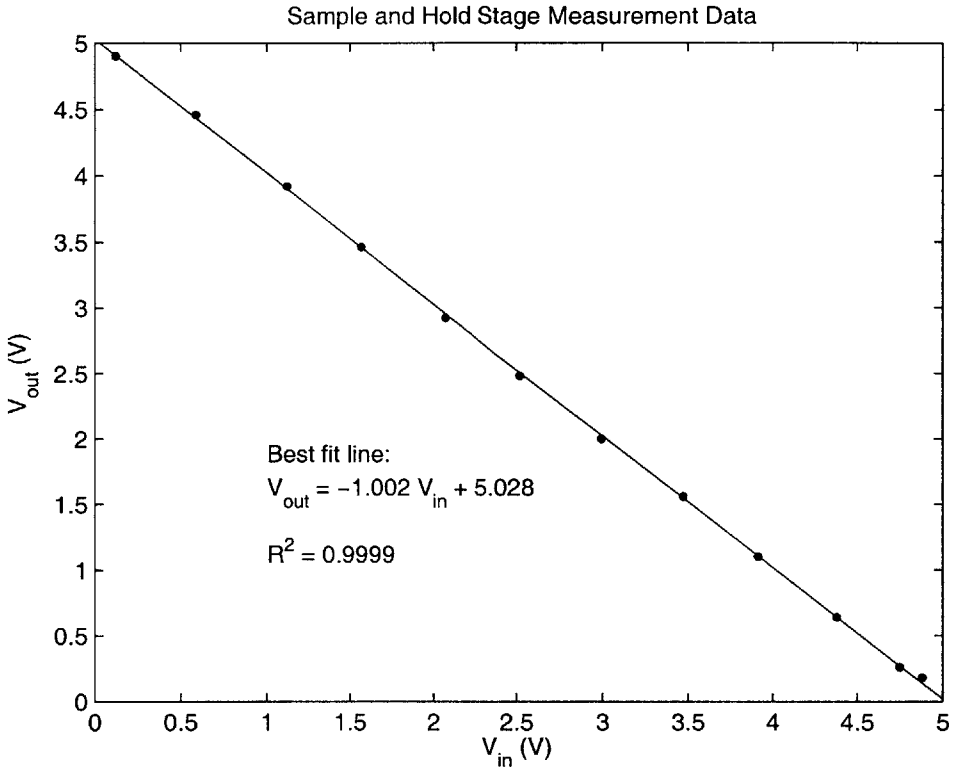


Figure 7-12: Measurement Results from the Sample and Hold Stage in the Test Channel. The results verify the functionality and performance of the Sample and Hold Stage.

Summary of Measurement Results from the Test Channel

CSA Stage	Ideal Gain	Measured Gain	Measured Offset	Measured Linearity
Transimpedance Stage	10 MΩ (V/A)	10.3 MΩ (V/A)	0.1V~0.7V output referred	Very $R^2 = 0.9949$
Gain Stage	10×	10.005×	-0.25mV input referred	Very $R^2 = 0.9998$
Differential to Single-ended Conversion Stage	5×	4.777×	-40mV input referred	Very $R^2 = 0.9999$
Sample and Hold Stage	-1×	-1.002×	28mV input referred	Very $R^2 = 0.9999$

Figure 7-13: Table Summarizing the Measurement Results in the Test Channel.

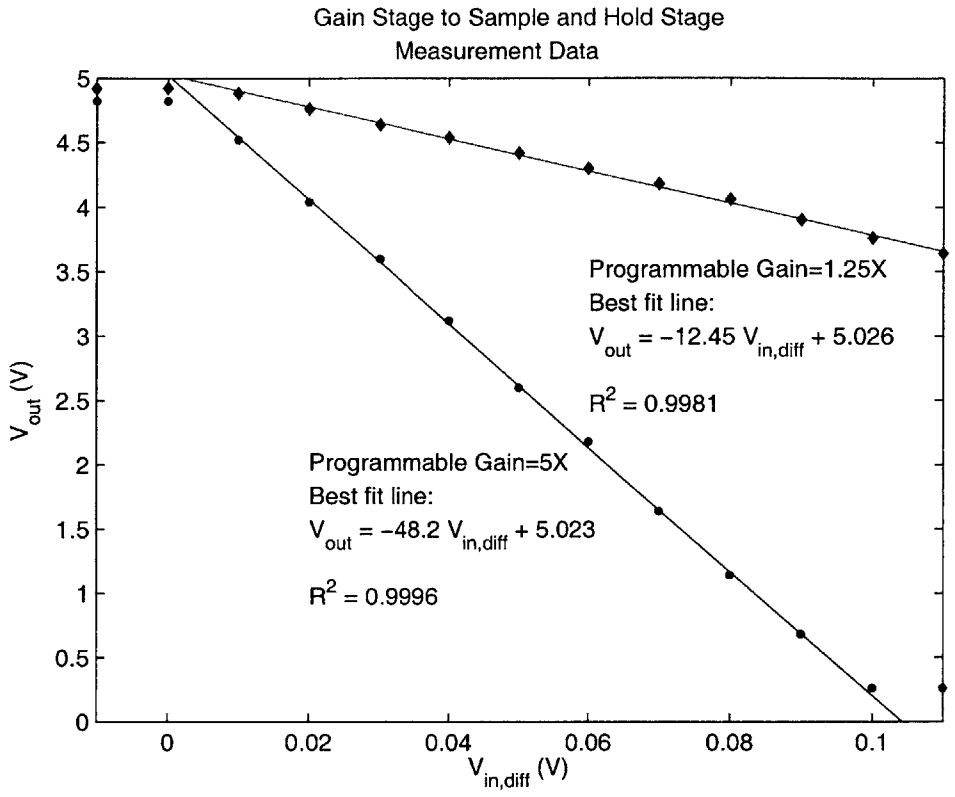


Figure 7-14: Measurement Results Looking that the Gain Stage, Differential to Single-ended Conversion Stage, and Sample and Hold Stage in Operation Together. The two traces show characteristics for a Programmable Gain (set in the Differential to Single-ended Conversion Stage) of 1.25× and 5×. The results verify the functionality and performance of these three stages as a whole.

offset of 28mV. This matches pretty well with the design specifications; these results are summarized in Figure 7-13.

Lastly, Figure 7-14 shows the characteristics measured across the last three CSA stages - Gain Stage, Differential to Single-ended Conversion Stage, to Sample and Hold Stage. By by-passing the Transimpedance Stage with the large offset, the following stages should not rail. The characteristics for the 1.25× and 5× gain settings are shown. Both curves show good functionality, linear gain, and little offset.

The main channel and test channel measurement results demonstrate functionality in all the stages. This verifies the design and theory of the circuits. However, practical issues have severely limited the performance of the stages, causing a large offset in the

Transimpedance Stage and inaccuracies in the Differential to Single-ended Conversion Stage. Section 7.2.3 describes these issues and how they are caused.

7.2.3 Issues Influencing Performance

The two main issues affecting the performance of the Transimpedance Stage and the Differential to Single-ended Conversion Stage are respectively:

1. transient ground spikes caused by the digital clock generation circuits, and
2. floating op amp inputs during the reset phase in the Differential to Single-ended Conversion Stage.

Ground Spikes

Because there are both digital and analog circuits on this chip, the digital circuits can cause ground spikes that affect the performance of the analog circuits. Most notably, the ground spikes up several hundred millivolts on the clock transitions. The chip features 7 clock generation (ClkGen) circuits that each generate four clocks - $clk1$, $\overline{clk1}$, $clk2$, and $\overline{clk2}$. On the transitions of these clocks, the 7 clock generation circuits switching simultaneously can cause large current spikes through the ground trace. Considering the small but significant resistance of the ground traces, this could lead to a voltage spike. Figure 7-15 (Left) shows the clock generation circuits, the ground pad, and the ground traces that connect them on the fabricated chip. For clarity, the same diagram is shown again on the right without the die photo background. Figure 7-16 shows the equivalent circuit schematic taking into account the resistances of the ground traces.

From simulation (shown in Figure 7-17 1st curve), a single clock generation block can contribute current spikes as high as ~32mA on the clock transitions. Hand calculations were used to estimate the peak voltage spike at each node in Figure 7-16 if these current spikes from all 7 clock generation blocks occurred simultaneously. Since they are all clocked by the same Clk_{in} signal, the spikes should all occur roughly

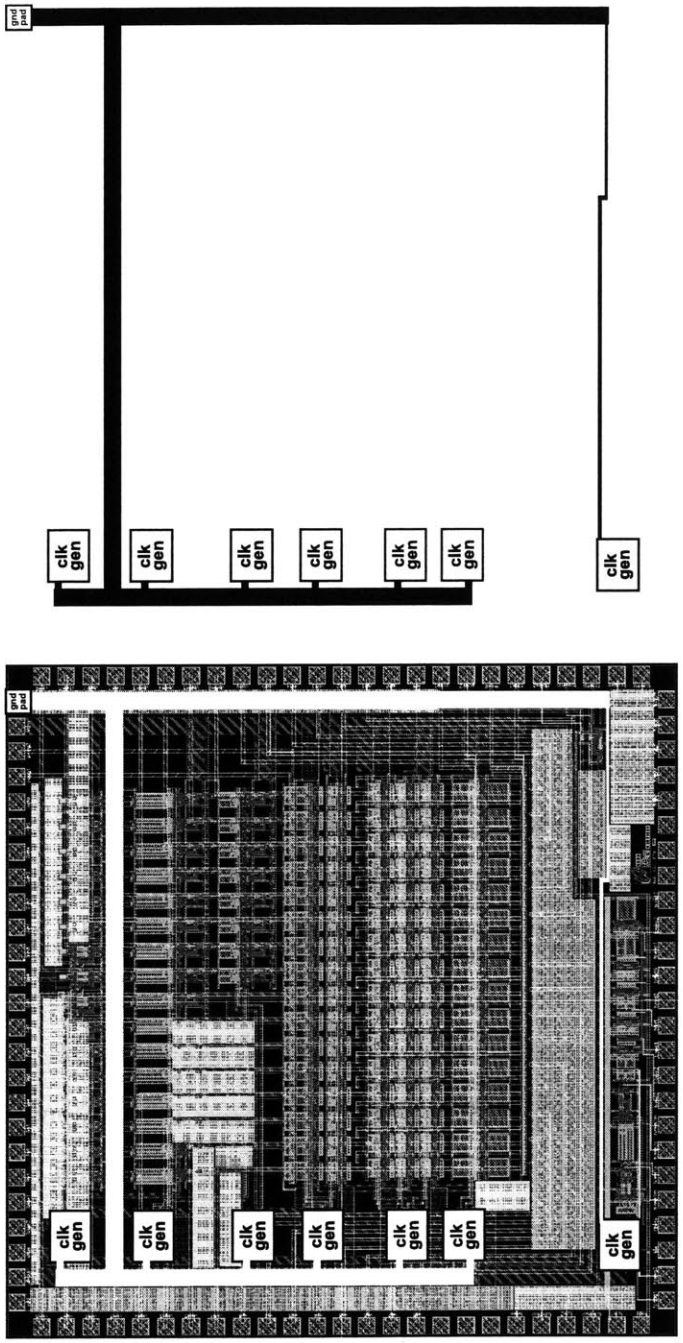


Figure 7-15: Clock Generation Circuits and Ground Wires on the Die. (Left) The 7 clock generation (ClkGen) circuits are on the left side of the die. The ground pad is on the top right. Ground wires connecting these ClkGen circuits to the ground pad are shown in white. (Right) For clarity, the same ClkGen and ground wire diagram is shown in black and without the die photo background.

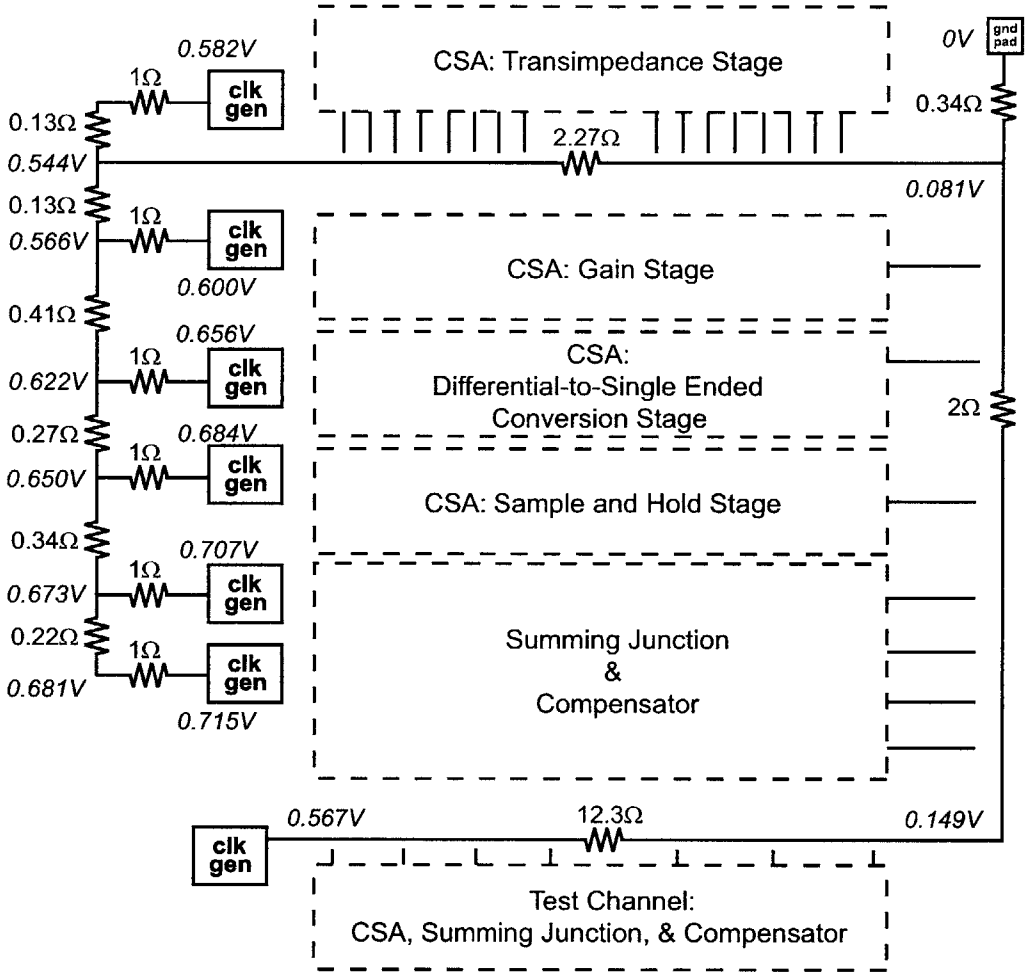


Figure 7-16: Model of the Ground Network Serving the Clock Generation Circuits. Not all ground traces are shown, only those that connect the clock generation circuits to the ground pad. Resistors modeling the metal trace resistances are shown. Also shown are the predicted peak voltage spikes at each node given that each clock generation block sends a current spike of 32mA to its local ground. Other modules are shown in large boxes with short wire segments indicating roughly where the modules tap into the ground network.

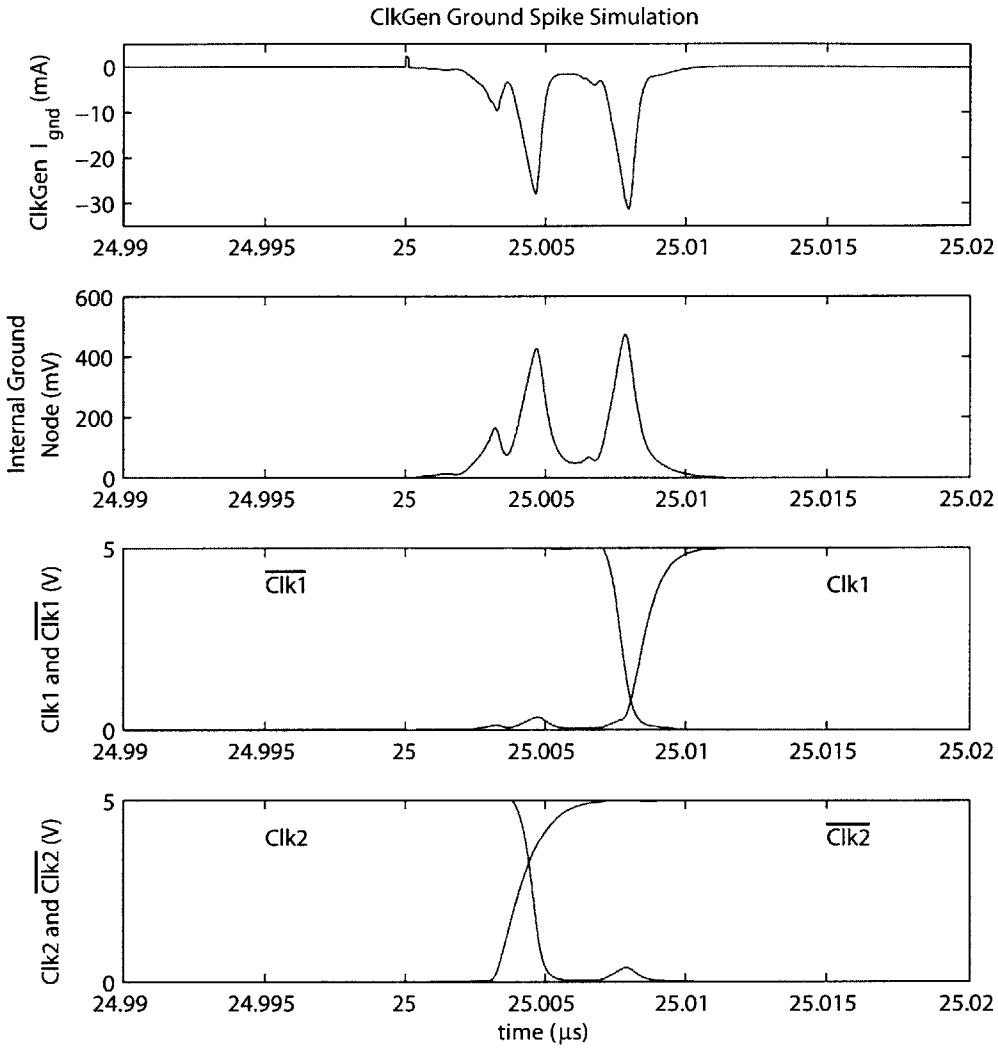


Figure 7-17: Cadence Simulation of Clock Generation Circuits and Resistive Ground Networks. The first curve shows the current spikes sent into the ground node by a single clock generation circuit. From the graph, each clock generation circuit contributes about 32mA of current spike. The second graph shows the voltage of a ground node located in the test channel near its clock generation circuit. The voltage spike of about 500mV shows the combined effect of all the clock generation circuits switching simultaneously. The last two plots show the clock transitions. The simulation data shows the spikes coinciding with the clock transitions.

at the same time. Calculations predict ground spikes of as high as 0.5V, 0.6V and 0.7V to occur all across various sections of the die. The second curve in Figure 7-17 shows the simulation of the clock generation circuits and ground network alone. The voltage plotted is taken from a ground node located in the test channel, near the test channel's dedicated clock generation circuit (lower left in Figure 7-15 (Left)). The simulation shows spikes of about 500mV occurring at the clock transitions (see Figure 7-17), verifying that very high spikes of 0.5V, 0.6V, and 0.7V are possible and likely to occur in various corners of the die.

Ground spikes caused by the digital circuits are likely to affect the Transimpedance Stage the most. As shown in Figure 7-16, the Transimpedance Stages of the main channel tap into ground along a long horizontal trace. Some Transimpedance Stages tap into ground near the ground pad on the right, where spikes of only 0.081V are predicted. On the other hand, some Transimpedance Stages tap into ground on the left, where spikes of up to 0.544V are predicted, which can significantly affect the performance of the stage. As for the other stages in the main channel, they all tap into ground on the vertical trace on the right, where ground spikes only peak up to $\sim$0.11V at the end of the CSA (Sample and Hold Stage), thus affecting these stages much less.

For the test channel, ground is drawn from the horizontal trace above it. Upstream stages, like the Transimpedance Stage, are located closer to the clock generation circuit on the bottom left of Figure 7-15 (Left), and are thus more subject to the effects of the ground spike (up to 0.567V). All other stages are downstream of the Transimpedance Stage, and experience decreasing ground spikes towards the right. Thus, in both the main channels and the test channel, the Transimpedance Stage is most affected by the ground spikes.

The ground spike can cause a large transient current through the Transimpedance Stage. The following steps propose how this mechanism affects the results in the Transimpedance Stage:

1. The ground voltage spikes, causing transient currents to flow through the inte-

grating capacitor (see Figure 5-2).

2. The transient current dumps charge into the capacitor; the integrating capacitor now has more charge than it should.

3. At the peak of the spike, the clocks transition, causing the switched-capacitor switches to flip.

4. Now that the circuit topology has changed mid-way due to the clock transitions; charge cannot flow back the way it came. (If it could, the capacitor could very possibly be reset back to its original state, resulting in no errors.)

5. The charges that were deposited onto the capacitors are not completely removed due to the change in the circuit topology mid-way. As a result, some capacitors now have the incorrect amount of charged stored on them as they enter the gain phase. This leads to an offset in the Transimpedance Stage.

Thus, the ground spike effect causes the large offset in the Transimpedance Stage, which then causes the downstream stages to rail.

Floating Op Amp Inputs

The ground spike effect could also explain the error and offset seen in the Differential to Single-ended Conversion Stage. But most likely another effect is at work as well. The Differential to Single-ended Conversion Stage in the reset phase leaves the op amp inputs floating (see Figure 5-11) for the entire duration of the phase (25μs). In an ideal scenario, this should not cause any problems. However, in practice, the op amp inputs will float and may go to any voltage as a result of leakage, charge injection, or other effects.

When this happens, the op amp output will change or even rail. Since the inputs are left floating for 25μs, it is hard to predict the op amp output, but it is almost certainly signal-dependent. Certain input signal levels to the Differential to Single-ended Conversion Stage could incline the op amp inputs to float in one direction and

magnitude more likely than others. Sometimes the op amp output will go to 5V, sometimes 0V, and yet sometimes 2.5V, or any other voltage.

At the onset of the gain phase, the switches M14 and M15 in Figure 5-11 connect the op amp output to a node that was previously discharged by M13 to 0V in the reset phase. By connecting two nodes of different voltages, this causes a transient current that equilibrates the two voltages levels. The transient current will flow through the feedback capacitors, dumping (or removing) a certain amount of charge onto them.

Since the op amp output voltage in the reset phase is unpredictable and likely signal dependent due to floating inputs, the transient current on the onset of the gain phase will also be unpredictable and signal-dependent. The signal-dependent component will manifest itself as a gain error as the capacitors are given varying, signal-dependent amounts of charge. The DC component of the transient current will manifest itself as an offset, delivering the same charge dump onto the capacitors regardless of the input.

Thus, this issue of floating op amp inputs in the reset phase causes the Differential to Single-ended Conversion Stage to have a gain error as well as an offset, which is exactly what was observed (see Section 7.2.2).

The Ground Spike Effect and Floating Op Amp Inputs account for the large offset observed in the Transimpedance Stage and the inaccuracies in the Differential to Single-ended Stage. These issues can be addressed for example by isolating the digital and analog grounds and driving the otherwise floating inputs, respectively.

Other minor issues observed included noise on the I_{in} lines and crosstalk between channels and closely routed signals. Both these effects can be eliminated by "ground-shielding," in which ground traces are laid out alongside the sensitive signal lines to reduce noise and crosstalk.

7.2.4 Summary

In summary, the simulation and measurement results demonstrate a functional Current Sensing Amplifier limited in performance by the ground spike effect and floating

op amp inputs effect. Once those two main issues are address as outlined above, the CSA should perform well and accurately, as the measurement data from other stages suggests.

Chapter 8

Conclusion

A high gain Current Sensing Amplifier (CSA) with a continuously tunable gain across a wide 62.5 MΩ $\sim$ 4 GΩ range was designed and tested. The simulation results were positive, showing high accuracy in gain and little offset, and verified the design. The measurement results from the fabricated chip demonstrated full functionality in the Gain Stage and Sample and Hold Stage. The Transimpedance Stage has functionality but with a large offset, and the Differential to Single-ended Conversion Stage has functionality but with some gain error. Overall, the CSA design was verified by the results, while some changes will further improve the performance.

The CSA is a general purpose Current Sensing Amplifier, which was tailored for the Optical Feedback OLED Display application. However, it can be used in any other application which requires measuring low current levels. In addition, the features included in the design allow precise adjustments of the gain. Such versatility allows the CSA to handle many different applications, or compensate for unexpected circumstances and inaccuracies in both the application and the CSA.

In addition, various Organic Imager Array designs were investigated given the organic process and technology and a final design proposed. The design was optimized to reduce leakage current levels to facilitate the organic photodetector signal detection. The Organic Imager Array will utilize the CSA proposed in this thesis for current amplification of the sensor signal. The Organic Imager Array together with the

CSA constitute a complete general-purpose imager, which can be used in the Optical Feedback OLED Display to complete the feedback path.

Future work may include the construction of an Optical Feedback OLED Display prototype to demonstrate the effects of OLED degradation and how optical feedback can compensate for such effects. Other extension possibilities also include applying such "User Interface Feedback Technology" to other display technologies, or even beyond displays to other user interfaces, for example to audio systems or force feedback systems.

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