Massachusetts Institute of Technology

POLY GATE MOSCAP PROCESS SUMMARY

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   Determine bulk dopant concentration.
   Determine fixed interface charge.
T.2 Sheet resistance measurement: Van der Pauw structure
MOSCAP LAB SESSION 1
Gate Oxidation, Polysilicon Deposition and Anneal

Location: ICL (2nd floor, Building 39)

Overview of Lab Session:
This first session will start with an introduction to the Integrated Circuits Lab (ICL) lab environment, as well as proper and safe working practices. The fabrication sequence will begin with a rigorous cleaning procedure that eliminates sources of wafer contamination and preserves the clean integrity of the furnaces. A ~500 Å gate oxide will be grown using a dry oxidation process. Immediately following the oxidation, the doped polysilicon gate layer will be deposited by chemical vapor deposition (LPCVD) to a target thickness of 2500 Å. The deposited polysilicon layer will be annealed to enhance an even distribution of dopants.

Lab Objectives:
- Review of lab safety and administrative procedures
- Introduction to cleanroom gowning and wafer-handling practices to avoid contamination
- Characterize basic physical and electrical characteristics of the starting n-type silicon substrates
- Complete growth and characterization of the gate oxide
- Complete growth of the gate polysilicon
- Instruction on the following major pieces of lab equipment:
  - Semifab RCA Cleaning Station
  - Thermco Atmospheric Furnace (5D-FieldOx)
  - Thermco Low Pressure Furnace (6A-Poly)
  - Thermco Atmospheric Furnace (5B-anneal)

Before attending this lab session, make sure to read the Standard Operating Procedures for the above equipment. SOPs can be accessed at: 

Lab Procedures:
1. Lab Safety and Cleanroom Orientation
   Read the sections on lab safety and code of conduct before attending lab session.

2. RCA Wafer Clean
   Follow the SOP for the Semifab RCA Cleaning Station.

3. Gate Oxidation
   Note: This step must be immediately preceded by RCA clean!
   Approximately 500 Å will be grown using a dry oxidation process at 1000 C. Follow the SOP for the Thermco Atmospheric Furnace (5D-FieldOx) using recipe "6.152 GATEOX 500A" with an interval time of 1 hour for the step of dry oxidation.

4. Doped Polysilicon Deposition
   Note: this step must immediately follow the gate oxidation.
   About 2500 Å of phosphorus-doped polysilicon will be deposited by LPCVD in the Thermco Furnace (6A-Poly). The deposition rate is fixed at ~30 A/min.

5. Anneal
   The deposited polysilicon gate layer will be annealed at 950°C for 12 minutes in a nitrogen ambient to enhance an even distribution of phosphorus dopants. Follow the SOP for the Thermco Atmospheric Furnace (5B-anneal).
Pre-Lab Questions:

1. What contaminants does the RCA clean remove? What is the purpose of the HF dip in the RCA clean?

2. Why is dry oxidation used to grow the gate oxide?

3. From the oxide growth chart in the Appendix, predict the gate oxide thickness after the oxidation.

4. From the oxide color chart in the Appendix, what color would one expect the gate oxide to appear?

5. What are the advantages of using polysilicon rather than aluminum for the gate electrode?

6. What is the by-product of the polysilicon deposition? What controls the deposition rate (transfer of SiH4, reaction at the surface of the substrate, or removal of the by-product)?

7. Sketch a cross section of the wafer after this lab session.
MOSCAP LAB SESSION 2
Back-side Strip
Location: ICL (2nd floor, Building 39)

Overview of Lab Session:
The first step of this lab session will be to characterize the oxide and polysilicon films deposited in
lab session 1. The main processing taking place in this lab session will be the removal of the
oxide and polysilicon layers from the back side of the wafers. This will allow electrical contact to
the back side of the wafer. The wafers will be coated with a photoresist solution using an
automatic coating system which has several modules operating in a pipelined fashion. The first
module treats each wafer with Hexamethyldisilazane (HMDS) vapor, an adhesion promoter. Next,
a photoresist solution is dispensed onto the wafer and evenly distributed by a spin-on technique.
Finally, the wafer is baked to expel solvents from the photoresist. Since the wafers will not be
patterned photolithographically, the wafers will be post-baked directly (rather than pre-baked,
exposed, and then post-baked) to harden the resist into a protective masking layer. The back
sides of the wafers will be etched dry-etched in He/Cl₂ plasma. Next, the oxide will be wet-etched
in buffered oxide etch (BOE), a solution of hydrofluoric acid. Finally, the photoresist will be
stripped by oxygen plasma etch.

Lab Objectives:
• Complete characterization of Oxide and Polysilicon films grown in Lab Session 1.
• Remove oxide and polysilicon films from back side of wafers.
• Instruction on the following pieces of lab equipment
  • KLA Tencor UV1280 Film Thickness Measurement System
  • SSI Coater Track
  • LAM 490B Plasma Etcher
  • Oxide Etch Sink
  • Matrix 106 System One Stripper

Before attending this lab session, make sure to read the Standard Operating Procedures
for the above equipment. SOPs can be accessed at:

Lab Procedures:
1. Characterize Oxide and Polysilicon deposited in Lab session 1.
   Measure the oxide and polysilicon thickness using the UV1280.
   Note: An oxide color chart is enclosed in the Appendix. The color chart assumes
   perpendicular illumination and viewing of wafer surface under white fluorescent lighting.

2. Etch oxide in BOE.
   (Oxide etch sink)
   Using the Oxide Etch Sink, etch the native oxide on the polysilicon surface of the wafer in
   Buffered-Oxide-Etch (BOE). The etch rate for BOE is about 1000 Å/min. The thickness of
   the native oxide is around 200 Å so estimate the approximate etch time required. When the
   BOE etch is complete, the BOE should ‘de-wet’ or bead up off the wafer. After completing
   etch, rinse thoroughly with DI water and spin dry.

   Overall reaction for etching SiO₂ with BOE:
   SiO₂ + 6HF ==> H₂ + SiF₆ + 2H₂O
   where a buffering agent, ammonium fluoride (NH₄F), is added to maintain HF concentration and to
   control pH (to minimize photoresist attack):
   NH₄F <=> NH₃ + HF.
3. Coat frontside of wafers with blanket photoresist and bake. Follow the SOP for the SSI Coater Track, using the following three modules
   • HMDS module: treatment promotes adhesion of photoresist
   • coating module: photoresist will be dispensed and spun on for ~1 micron thickness
   • bake module: at 95 C for 60 s on hot plate

4. Dry-etch backside polysilicon in He/Cl₂ plasma. Use the LAM 490B with recipe "BACKSIDE POLY (5KA)" to etch the exposed polysilicon on the backside of the wafer. The wafers will be loaded into the machine upside down. Take care handling the wafers to avoid marring the front side. Based on your previous measurements of polysilicon thickness, estimate the appropriate etch time required.

5. Etch backside gate oxide in BOE until de-wet. (Oxide etch sink) Using the Oxide Etch Sink, etch the exposed oxide on the back side of the wafer in Buffered-Oxide-Etch (BOE). The etch rate for BOE is about 1000 Å/min. Based on your previous measurements of oxide thickness, estimate the approximate etch time required. When the BOE etch is complete, the BOE should 'de-wet' or bead up off the wafer. After completing etch, rinse thoroughly with DI water and spin dry.

   NOTE: BOE contains a high concentration of hydrofluoric acid (HF). Be aware of the dangers of handling HF!

6. Strip photoresist with the Matrix System One Stripper (Asher) This is an oxygen plasma etch.

Pre-lab questions:
1. Why is HMDS applied to the wafers before photoresist application?
2. Why is BOE particularly dangerous? How should one be gowned when handling BOE?
3. What is the purpose of NH₄F in BOE?
4. Sketch a cross-section of the wafer after the processing in this session.
MOSCAP LAB SESSION 3
Photolithography and Gate Patterning
Location: ICL (2nd floor, Building 39)

Overview of Lab Session:
In this lab session, photolithography will be used to transfer an image from a mask to the wafer. Wafers will be coated with photoresist on the SSI track, similar to the photoresist application step in Lab Session 2, except that wafers will be pre-baked. The pattern will be transferred from a mask to the wafer using the Nikon NSR2005i9 Wafer Stepper (i-stepper), a projection aligner. The photoresist in the clear fields of the mask is exposed to UV light, and resist in these areas is removed when the wafer is developed. Finally, the wafer is post-baked to improve adhesion. Using the photoresist as an etch mask, the polysilicon will be dry-etched using He/Cl₂ plasma. After this step, the photoresist will be ashed, and the process is completed.

Lab Objectives:
- Introduction to photolithographic process and procedures.
- Patterning of polysilicon gate electrode.
- Instruction on the following pieces of equipment:
  - SSI Coater Track
  - Nikon NSR2005i9 Wafer Stepper (i-stepper)
  - LAM 490B Plasma Etcher
  - Matrix 106 System One Stripper
  - Optical Microscope

Before attending this lab session, make sure to read the Standard Operating Procedures for the above equipment. SOPs can be accessed at: [http://www-mtl.mit.edu/mlt/home/3Mfab/sop.html](http://www-mtl.mit.edu/mlt/home/3Mfab/sop.html)

Lab Procedures:
1. HMDS, photoresist deposition, and pre-bake.
   Follow the SOP for the SSI Coater Track, using the following modules:
   - In-line HMDS treatment
   - Spin-on module: standard dispense for ~1 micron thickness
   - Pre-bake module: 95 C on hot plate.

2. Exposure, development and inspection
   Refer to Appendix for mask schematics.
   Use the i-stepper to transfer mask pattern to wafers.
   - Use control wafer to make a ‘focus-expo’ grid --- a matrix of various focal lengths and exposure times.
   - Develop this wafer using the following modules of the SSI Coater Track:
     - Post-exposure bake
     - Develop
     - Post-bake
   - Inspect developed control wafer with optical microscope and determine optimal focal length and exposure time.
   - Use these settings for exposure of device wafers.
   - Develop device wafers using the following modules of the SSI Coater Track:
     - Post-exposure bake
     - Develop
     - Postbake
   - Inspect wafers visually with optical microscope
3. Dry-etch polysilicon in He/Cl₂ plasma.
   • Use the LAM490B to etch exposed gate polysilicon that is not protected by photoresist. Use recipe "POLY EP"; This recipe features automatic endpoint detection. From the etch time, calculate the average etch rate.
   • Inspect wafers visually with optical microscope.

4. Strip photoresist with the Matrix System One Stripper (Asher)

Pre-lab questions:

1. Describe the various alignment marks on the reticle.

2. Explain the difference between isotropic and anisotropic etch characteristics.

3. What chemical is used to etch the polysilicon? Is this an isotropic or anisotropic etch?

4. Sketch the cross-section taken through the gate of a device.

MOSCAP Testing

Location: ICL, EML (5th floor, Building 39)

Overview of Lab Session:
This lab session will take place in the Exploratory Materials Laboratory (EML). Electrical testing will be performed to characterize materials and device performance.

Lab Objectives:
• Introduce electrical testing instruments and procedures
• Characterize device performance and materials
• Relate device characteristics to fabrication process

Lab Procedures:
1. Device Characterization: MOS Capacitor

The following devices will be measured:
   1) 500 x 500 µm² cap, with anneal
   2) 200 x 200 µm² cap, with anneal

Follow instructions (in SOP for test station) for use of HP-4061A system to perform C-V measurement (see appendix) on MOS capacitor. The gate electrode is probed, along with the backside of the substrate.

At high frequency (100 kHz), the result should be similar to this CV curve for an aluminum gate MOS structure.
A. Oxide Capacitance: $C_{ox}$

All capacitance values with * are area normalized capacitances; e.g. $C_{ox}^* = \frac{C_{ox}}{A}$ and $C_{ox} = \frac{C_{ox}^*}{A}$.

From the accumulation capacitance:

$$C_{acc} = A C_{ox}^*$$

$$C_{ox}^* = \frac{C_{ox}}{t_{ox}}$$

Calculate $t_{ox}$ and compare with measured values from UV1280 of gate oxide thickness taken in Lab Session 2.

B. Bulk Dopant Concentration: $N_D$

From the high-frequency inversion capacitance, the bulk dopant concentration can be calculated.
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\[ C_{\text{min}}^* = \frac{(C_{ox}^* C_S^*)}{C_{ox}^* + C_S^*} \]

where \( C_s \) = semiconductor capacitance:

\[ C_S^* = \sqrt{\frac{q \varepsilon_s N_D}{2(2|\Phi_f|)}} \]

and

\[ \Phi_f = \left( \frac{kT}{q} \right) \ln \left( \frac{N_D}{n_i} \right) \]

### C. Fixed Interface Charge: \( Q_F \)

Calculate the capacitance at flatband voltage (The condition where the surface concentration of electrons is equal to that in the bulk.).

\[ C_{FB}^* = \frac{1}{\frac{1}{C_{ox}^*} + \sqrt{\frac{kT}{q^2 \varepsilon_s N_D}}} \]

Find the flatband voltage \( V_{FB} \) corresponding to \( C_{FB} \) from the C-V curve.

Calculate approximately the fixed charge at the Si/SiO\(_2\) interface from the theoretical expression for flatband voltage.

\[ V_{FB} = \Phi_{MS} - \left( \frac{Q_F}{C_{ox}^*} \right) \]

\[ \Phi_{MS} = \left( \frac{kT}{q} \right) \ln \left( \frac{N_D}{n_i} \right) - \left( \frac{kT}{q} \right) \ln \left( \frac{N_C}{n_i} \right) \]

\[ = \left( \frac{kT}{q} \right) \ln \left( \frac{N_D}{N_C} \right) \]

### 2. Sheet Resistance: Van der Pauw Structure

The Van der Pauw structure is used to measure sheet resistance. The structure consists of an area of material, contacted at each corner.

\[ R_{\text{square}} = \frac{(\pi \ln 2)}{(V/\text{l})} \text{Ohms/square} \]

Van der Pauw further showed that by taking voltage measurements from adjacent leads when current is forced through the other 2 leads, then rotating the lead positions by 90\(^\circ\), any asymmetry in the structure could be corrected for by using a mathematical
function. The structures to be tested on the mask are symmetrical by design, so do not need to be corrected. Still, the average of the two measurements yields a better estimate of the sheet resistance of the underlying material.

$$R_{\text{square}} = \frac{4.53}{2} [(V_{\text{CD}}/I_{\text{AB}}) + (V_{\text{BC}}/I_{\text{AD}})] \text{ Ohms/square}.$$ 

To measure the sheet resistance using the Van der Pauw structure, use program **PPOLYVDP**. Setup of leads for both are as follows:

- SMU 1 -- Current Source -- [7]
- SMU 2 -- Ground -- [15]
- VM 1 -- Voltage Tap -- [21]
- VM 2 -- Voltage Tap -- [5]

Average resistivity can then be determined simply by multiplying the measured sheet resistance by the thickness of the polysilicon layer.

Physical Constants:

- \(e_s = 1.05 \times 10^{-12} \text{ (F/cm)}\)
- \(e_{ox} = 3.45 \times 10^{-13} \text{ (F/cm)}\)

- \(q = 1.6 \times 10^{-19} \text{ C}\)
- \(kT/q = .026 \text{ V}\)

- \(N_c = 2.86 \times 10^{19} \#/\text{cm}^3\)
- \(n_i = 10^{10} \#/\text{cm}^3\)

<<Appendices>>
Features to check exposure. All lines and spaces should be exposed. Corners should touch, but not overlap on abutting squares.

Wafer Alignment Marks - Wx: for global alignment of wafer to stage.

Fine Alignment marks LSAx: Used to align each exposure position to the wafer; used to register to previous mask steps.

Wafer Alignment Marks - Wy: for global alignment of wafer to stage.

Fine Alignment marks LSAy: Used to align each exposure position to the wafer; used to register to previous mask steps.
Probe card pinout

Van der Pauw test structure. Arms should align to pins 7, 5, 21, and 15.

Poly-gate MOS Capacitors. Side length indicated.