Characterization and Modeling of Plasma Etch Pattern Dependencies in Integrated Circuits

By

Kwaku O. Abrokwah

Submitted to the Department of Electrical Engineering and Computer Science

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ABSTRACT

A quantitative model capturing pattern dependent effects in plasma etching of integrated circuits (ICs) is presented. Plasma etching is a key process for pattern formation in IC manufacturing. Unfortunately, pattern dependent non-uniformities arise in plasma etching due to microloading and RIE lag. This thesis contributes a semi-empirical methodology for capturing and modeling microloading, RIE lag, and related pattern dependent effects. We apply this methodology to the study of interconnect trench etching, and show that an integrated model is able to predict both pattern density and feature size dependent non-uniformities in trench depth.

Previous studies of variation in plasma etching have characterized microloading (due to pattern density), and RIE lag (aspect ratio dependent etching or ARDE) as distinct causes of etch non-uniformity for individual features. In contrast to these previous works, we present here a characterization and computational methodology for predicting IC etch variation on a chip scale that integrates both layout pattern density and feature scale or ARDE dependencies. The proposed integrated model performs well in predicting etch variation as compared to a pattern density *only* or feature scale *only* model.

Thesis Supervisor: Duane S. Boning
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Chapter 1

Introduction and Motivation for Research

This thesis presents the motivation for studying variation in plasma etching of integrated circuit (IC) interlayer dielectrics (ILD) due to pattern dependencies. We also motivate the need for accurate prediction and modeling. After describing the physical processes involved in plasma etch, previous work in the field is presented. This thesis attempts to capture IC dielectric etch variation through an integrated pattern density and aspect ratio based model that can simulate within and across die variation in etch depth for all feature sizes.

1.1 Motivation and Overview

As integrated circuits follow a path of shrinking technology scale, the percentage of performance variation due to back end of the line processes has increased to the point whereby it is comparable to that of transistor variations [1]. Plasma etching of interlayer dielectrics (ILD) for metal contacts, vias, and lines is a significant contributor to chip-scale circuit performance variations. These performance variations manifest themselves in terms of varying resistance and capacitance across the chip and lead to circuit signal delays and skews [1].

This thesis has three goals. The first is to develop a computationally efficient chip scale pattern density model based on the physical process of plasma etching. The second is to develop a chip scale feature-level or aspect ratio dependent etch (ARDE) model based on plasma etchant transport dynamics. Lastly, this thesis will integrate the pattern density and feature level models into a combined model, and show how the combined model provides superior prediction to the individual models.

Chapter 2 will describe in detail the theories behind the causes of plasma etch variations at the wafer, die, and feature levels. Chapter 3 describes the mask layout of the test chip used to obtain empirical data for our model development and for characterizing variations seen in plasma etch of ICs. Next, Chapter 4 describes the etch experiment conducted using the test mask. Chapter 5 presents the metrology taken on the test wafers and Chapter 6 and Chapter 7 develop the two etch models: a pattern density model and a feature based (aspect ratio dependent etch) model. Chapter 8 presents the integrated model that combines the pattern density and feature based models, and demonstrates the ability of the integrated model to effectively predict chip scale etch variations. Lastly, Chapter 9 concludes the thesis.

1.2 Overview of Plasma Etching

Plasma etching is a key process for pattern formation in IC manufacturing. Plasma etching allows for anisotropic and selective etching of material layers in both front end and back end IC process steps. In the front end processes of transistor formation, plasma etching is used to etch shallow trench isolation (STI) structures, and form the polysilicon gate. In the back end processes, plasma etching is used for contacts, vias, and trench line formation.

Figure 1.1 illustrates a schematic of an inductively coupled plasma etcher. The etching process occurs in a vacuum chamber regulated by an automatic pressure controller (APC). The top of the chamber has an inlet and showerhead where the feed gas such as carbon tetraflouride (CF_4) enters and is ignited into the etching plasma. This ignition is induced and maintained by the radio frequency (RF) coils that wrap around the chamber and typically operate at 2 MHz with RF power between 0 and 1000 watts. The

substrate holder or chuck is RF biased at 13.56 MHz with power between 0 and 1000 watts. The chuck also has a helium cooling gas inlet that cools the backside of the wafer and regulates the wafer temperature.

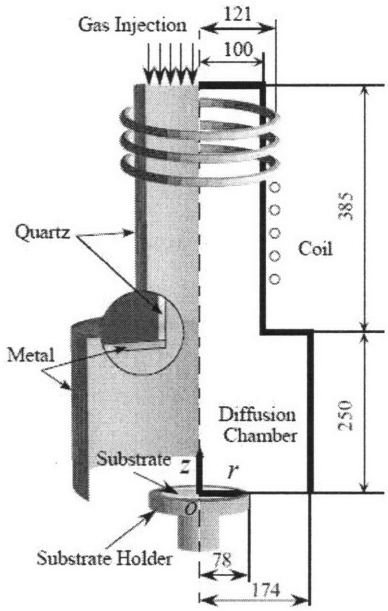

Figure 1-1 – Schematic of inductively coupled plasma etching chamber [2].

1.2.1 Physical and Chemical Process in Plasma Etching

Plasma etching involves the ionization of chemical gas into ion and neutral plasma. For oxide (SiO_2) etching, the initial gas is usually a carbon fluorine molecule such as carbon tetraflouride (CF_4). The ionized plasma within the chamber is accelerated towards the wafer holding chuck through the RF bias on the chuck which creates a strong electric field with the plasma. The space between the plasma and the wafer is called the sheath. The ions pick up most of their energy when they enter the sheath and are accelerated by the electric field. The neutral plasma diffuses from the plasma through the sheath and towards the wafer. The method of diffusion is highly debated within the semiconductor industry and academia [3].

Although some isotropic diffusion of the neutrals takes place, there is evidence that collisions between neutrals, ions, and electrons create fast neutrals that do not behave isotropically [4]. These fast neutrals, along with other causes of non-uniform distributions of neutrals within the etch chamber, are discussed in Chapter 2. The interaction of ions and neutrals once they reach the wafer surface is discussed in Chapter 6 and Chapter 7.

1.3 Previous Work

Previous works in modeling non-uniformities in plasma etch have generally focused on three areas that correspond to three length scales. The first area where non-uniform etch rate was encountered is across wafer or wafer-to-wafer etch variation. This variation, termed macroloading, is the longest length scale where non-uniform etching occurs. Industry engineers and academic scientists first noticed macroloading when the etch rate of one wafer varied from the etch rate of another wafer due to the amount of exposed area being etched [5]. Macroloading was also noticed within the wafer whereby different regions of the wafer, having differing amounts of open area, etch at different rates [5].

The next area of non-uniformity corresponds to the length scale of within die and between die. This length scale of variation is termed microloading because it corresponds to localized variation in reactant depletion that cause etch rate non-uniformity. Areas within the die with more exposed surface area etch more slowly than areas with less exposed surface area. Microloading differs from macroloading both in their length scales and their effect on the etch rate. While macroloading increase the reactant loss rate throughout the reactor and *loads* down the reactant concentration, near the reactive surfaces, the reactant concentration is depleted further due to microloading [4].

Microloading causes and effects are described in Chapter 2 and form the basis of our modeling work in this thesis, along with aspect ratio dependent etching.

The third area of non-uniformity corresponds to the length scale of individual features. Variations at this length scale are termed aspect ratio dependent etching. The mechanisms of ARDE act independently of macroloading and microloading. Industry engineers and academic researchers have focused on transport of ions and neutrals within a microstructure as the mechanism by which ARDE occurs [4][6]. The cause and effects of ARDE are discussed in Chapter 2.

1.4 Summary

Layout induced etch variation within integrated circuit manufacturing becomes more pronounced as the industry technology evolves. This thesis is devoted to first understanding the sources of etch rate non-uniformity, and then presenting a methodology for effectively capturing etch rate variation at the chip scale based on layout pattern dependencies. The following chapters present the theories underpinning our methodology and the development of pattern density and feature level models from the methodology.

Chapter 2

Theory of the Causes of Plasma Etching Non-uniformity

In this chapter the spatial and physical sources of plasma etch non-uniformity are described, along with models that explain the interactions between the physical processes and the spatial variations. The physical processes include the chemistry of the plasma and the characteristics of the chamber generating the plasma. Much of the chemistry involved in plasma etching was described in Chapter 1. The spatial variations depend on the size and arrangement of features on the wafer and the evolution of these features throughout the etch process. The trench evolution is dictated by the interactions of the plasma species with the substrate being etched.

Although this section will review most of the causes and effects of plasma etch non-uniformity, this thesis primarily focuses on microloading and ARDE which are caused by transport of chemical etch species. In Section 2.1 the common terminology used to describe pattern dependent effects in RIE are defined and categorized. Next, Section 2.2 discusses the sources of variations seen in the etch rates and profiles of structures. Section 2.3 expands on one of two sources of variations, chamber induced non-uniformity. Section 2.4 describes the second source of variation, pattern induced non-uniformity. Section 2.5 focuses on the most commonly encountered RIE effects. Finally the conclusion in Section 2.6 revisits all the causes and effects of variations seen in plasma etch.

2.1 Vocabulary

Non-uniformities in plasma etch processes have been studied continuously over the past 30 years. As a result, terminology has emerged for describing these variations.

Specifically, microloading, reactive ion etch lag (RIE-lag), aspect ratio dependent etching (ARDE), ion shadowing, and neutral shadowing merit discussion. These term arose to describe the causes and effects of etch rate non-uniformity. Often many terms overlap such as RIE-lag and ARDE.

Microloading describes competition for and depletion of reactive etching agents when exposed to loading across a chip, and results from similar mechanisms to those that cause macroloading [4]. Microloading should only be used to refer to a local dependence on pattern density for identical features. Section 2.4 further describes the causes and effects of microloading.

RIE-lag and ARDE describe non-uniformity arising from the aspect ratio of individual features. Aspect ratio is defined as the ratio between the depth of a microstructure and its width. Ion and neutral shadowing are one of many means by which RIE lag and ARDE occurs. Gottscho describes RIE lag as resulting from microscopic transport phenomena within a single feature. It is possible to have RIE-lag without microloading and vice versa [4]. In the subsequent sections of this chapter, we describe both the physical, descriptive, and analytical models that have been used to study RIE-lag.

Although used interchangeably, RIE-lag is a manifestation of ARDE, which is synonymous with aperture or proximity effect [4]. The term was coined by researchers at IBM to describe the common observation that smaller diameter trenches and holes etch more slowly than larger diameter trenches and holes [4]. This effect is also evident in the etching of post structures, where the etch rate near the post can be less than the etch rate in the open area between the posts [4]. RIE lag refers to the dependence of etch rate on aspect ratio (depth/width). Unlike microloading, RIE-lag is characteristic of individual

microstructures. It does not depend on absolute feature size but only on aspect ratio. Therefore, because aspect ratio continually increases during the etching process, etch rates are necessarily time dependent [4].

Etch rate and profile deviations depend on the interactions of microstructures and etchant species [4]. Ion and neutral transport encompass the majority of the causes of etch rate and profile variations [4][7]. The cause and effect of microloading and ARDE are shown in Table 2-1. The three causes of RIE-lag are transport of reactive species, ion shadowing and neutral shadowing (Table 2-1). In most cases of RIE-lag, there is a decrease in etch rate with increasing aspect ratio. This is often called "positive" or "ordinary" RIE lag and is mostly caused by diminishing probability of reactants reaching the bottom of the etching structure [6]. But when RIE-lag is caused by shadowing of reactants, there can be acceleration in reaction rate with increasing aspect ratio. This phenomenon is called "reverse" or "negative" RIE lag [4][7].

Table 2-1 – Causes and effects of ARDE and microloading.

	Cause	Effect
ARDE		
	Knudsen Transport of neutrals	RIE lag
	ion shadowing	RIE lag, microtrenching, slopped sidewall, profile shape
	neutral shadowing	RIE lag, slopped sidewall, profile shape
	differential charging	RIE lag, notching, bowing, microtrenching, retrograde sidewalls
Microloading		
	depletion of chemical etch species	Underetching

2.2 Sources of Non-uniformity

In studying microscopic uniformity in plasma etching of interlayer dielectrics, it is important to study the causes and effects of non-uniformity in etch rate and the final etch profile. The causes can be divided into those induced by the plasma species and those from the patterns on the wafer. The effects result from the interaction of the plasma

species with the patterns on the wafer. We consider the causes and effects of microscopic non-uniformity categorized by Rangelow into three groups (Figure 2-1) [7].

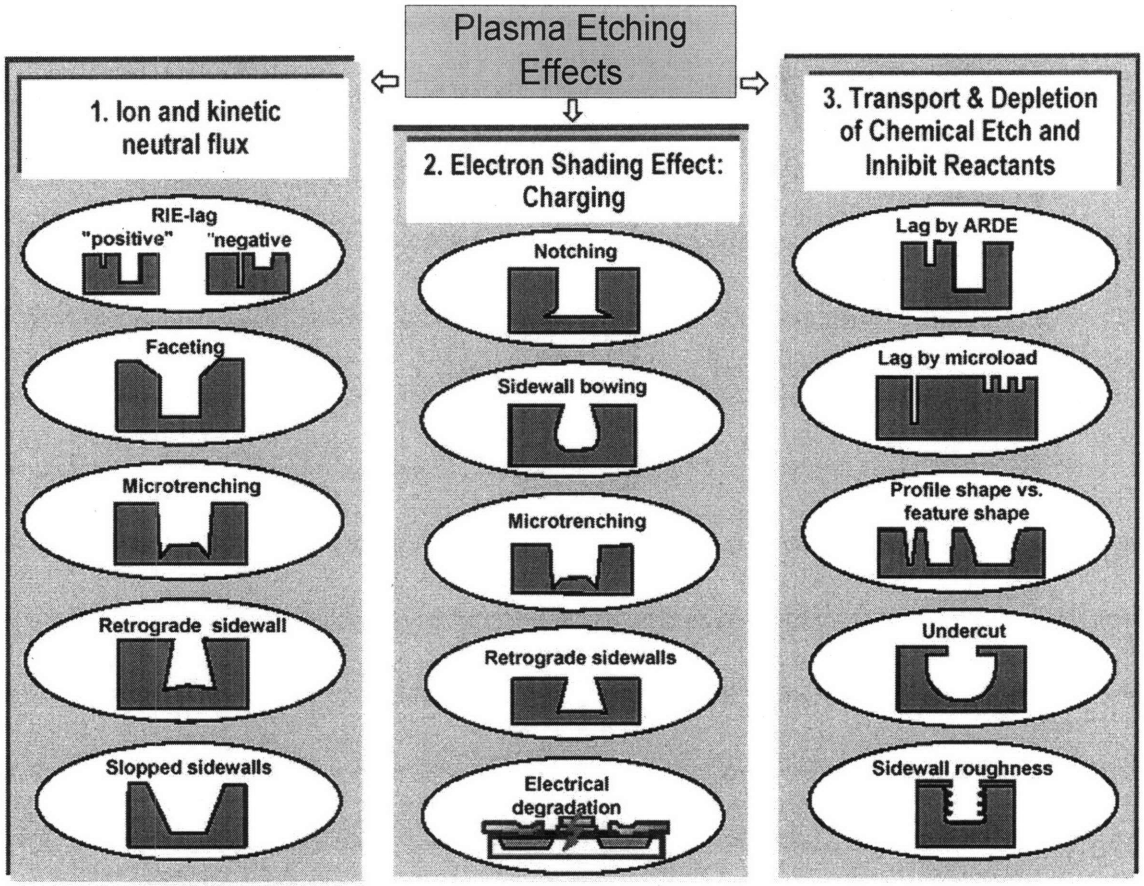

Figure 2-1 – Profile of plasma etching non-uniformity causes and effects [7].

The first group is composed of etch rate and profile deviations that are caused by kinetic ion and neutral fluxes. Non-uniformity in ion and neutral flux distribution is described later in Section 2.3. Angular dispersion of ions and neutrals due to collisions within the sheath, and ion and neutral interaction with sidewalls result in positive RIE-lag, negative RIE-lag, faceting, microtrenching, retrograde sidewall, and sloped sidewalls [7]. The left column of Figure 2-1 shows the effects resulting from ion and neutral kinetics.

The second group is composed of etch profile deviations from design that are induced by electron charging of the wafer substrate. The electron charging alters the trajectory of

high energy ions while they are in transit through the microstructure. This electron shading effect is caused by non-uniform charging of the etching feature; upper parts of the feature and its sidewalls are locally charged and can deflect the flight of the ions reaching the bottom of the microstructure. Electron charging reduces the number of the etching species reaching the bottom surface [7]. Pattern dependent charging originates in the directionality differences between ions and electrons as they cross the plasma sheath and interact with both conducting and insulating microstructures [7]. The results of surface charging are "notching," sidewall "bowing," microtrenching, and electrical degradation or plasma damage as illustrated in the second column of Figure 2-1.

The third group is composed of microscopic non-uniformities due to transport and depletion of chemical etch and inhibitor reactants. Ion and neutral transport and depletion cause both etch rate and profile deviations, and are significant and dominant factors in microscopic non-uniformity, RIE-lag, and microloading [4]. Furthermore, transport and depletion of chemical etching and inhibitor reactants under conditions of high reaction probability at the wafer surface, along with deposition of material produced in discharge within the microstructure, result in RIE-lag, microloading, irregular feature shape, undercutting, and sidewall roughness as shown in column three of Figure 2-1.

The sources of etch non-uniformity result from both the design and operational settings of the etch chamber and the patterned structures being etched into the wafer. Chamber non-uniformities manifest themselves in the uneven generation or transport of the plasma species. Pattern-induced non-uniformity is caused by the perturbation of the etch reactants at the wafer surface. Figure 2-2 shows how non-uniformities can be categorized into chamber and pattern induced effects.

Furthermore, the interaction between the two categories of non-uniformity occurs at the interface of the generated plasma species and the wafer patterns. This interface, and the evolution of the interface as the patterns are etched, ultimately determines the overall etch process. The consumption of etchant species and the kinetics of the ions and neutrals within the microstructure have feedback effects by depleting and changing the kinetics of the species outside of the microstructure. Therefore the arriving species and the evolution of the microstructure influence each other.

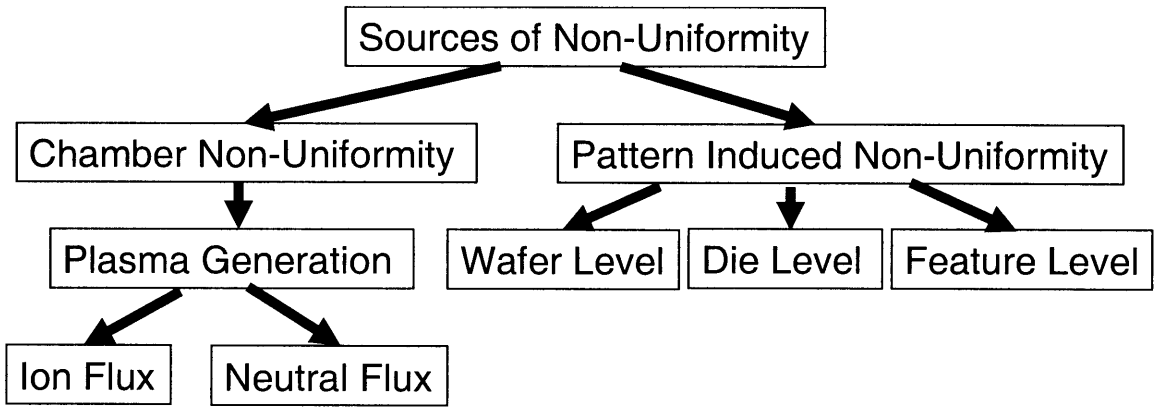

Figure 2-2 – Sources of non-uniformity in plasma etch.

2.3 Chamber Induced Non-uniformity

Chamber non-uniformity is caused by the physical structure of the inductively coupled plasma etcher. Asymmetry in the coils of the chamber can causes asymmetric generation of plasma above the wafer and lead to non-uniform distribution and generation of etchant species across the wafer. The asymmetry of the plasma over the wafer can also occur if the wafer is placed in an offset position from the center of the reactor. Any asymmetry in the design of the inflow and outflow of gasses may cause non-uniform concentration and distribution of etchant species in the chamber (Figure 2-3). Lastly, although not considered in this master's thesis, the dimension and volume of the chamber

along with the power and pressure at which the ICP is operating also contribute to non-uniformities.

A quantitative and qualitative description of the etching mechanisms requires: (i) identification of the species generated in the plasma, and characteristic parameters of the species, like angle and energy distribution; (ii) knowledge of the elementary species-surface interactions such as adsorption, reflection, and surface coverage; and (iii) recognition of the reaction products [7]. In the rest of this section, these mechanisms are considered along with their influence on etch profile and etch rate.

2.3.1 Plasma Generation

The generation of plasma in an inductively coupled plasma etcher occurs with the breakup of the feed gas into ion and neutral elements. This process is subject to asymmetry that can be caused by the feed gas flowing from the showerhead into the chamber (Figure 2-3). The asymmetric gas flow causes non-uniform plasma generation in the chamber. Most modern ICP used in microelectronics fabrication have symmetric gas flow into the chamber.

Nonetheless non-uniform plasma generation occurs because of other factors involved in the generation of plasma. Asymmetric RF coils that break the feed gas into its ion and neutral components can also contribute to non-uniform plasma generation. If a single-turn coil is used to power ICP plasma, the power may be deposited off-axis [8]. As a result of the heating of the plasma being away from the center, it is sometimes possible to get an off-axis plasma density peak [8].

The second source of off-axis density peak is the shape of the reactor. If the reactor is a squat cylinder with a height much less than its radius, then there is a hollowing of the

plasma at its center due to faster loss of ions at the center than at the perimeter. In some circumstances, the wafer sits on a holder that is not directly above the center of plasma but at a slight offset (Figure 2-3). This can also cause asymmetric distribution of the plasma over the surface of the wafer.

The functional settings of the etch chamber indirectly influence uniformity through the breakdown of the feed gas into plasma, the strength of the electric field across the sheath, and the pressure within the chamber. The density of the plasma depends on the power applied to the coils to ignite and sustain the plasma, along with the pressure maintained within the chamber and the RF bias applied to the cathode. The chamber pressure increases collisions of electrons with neutrals which increases the ionization of neutral species. The strength of the electric field across the sheath depends on both the bias applied to the wafer chuck and the rate at which electrons leave the plasma. This flow of electrons generates variations in the electron distribution of the plasma. The non-uniform electric field distribution contributes to variation in ion acceleration and distribution across the wafer.

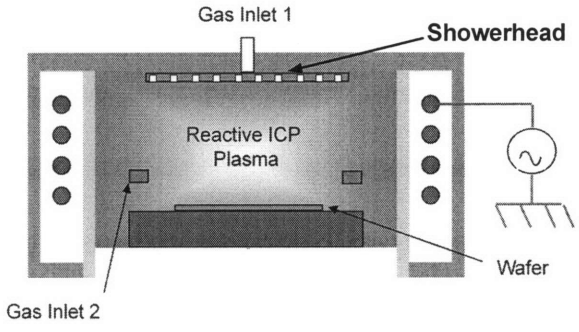

Figure 2-3 – Asymmetric gas flow and chamber design [9].

2.3.2 Etch Species, Temperature, and By-products

The influence of etch species on uniformity is largely based on gas phase transport of ions and neutrals. These ions and neutrals are generated from the feed gas and are influenced by chamber dimensions, temperature, and pressure. The specific etch species used depends on the material substrate being etched. Various studies suggest that gas-phase transport of ions and neutrals is an important factor in ARDE. Fugiwara et al. showed that RIE-lag of Si trenches is more severe in Cl_2 than in HCl, HBr, or HI ECR plasma (Figure 2-4) [10].

Pressure is importance in determining the relative influence of mechanisms such as Knudsen transport, ion shadowing, neutral shadowing, and differential charging on ARDE. The dependence of etch rate and RIE-lag on pressure has been demonstrated for various chemistries and substrates [4]. A high pressure "plasma etching" system operating at 270 Pa has worse RIE-lag than a lower pressure "RIE" system operating at 6.5 Pa (Figure 2-4) [4]. A "microwave plasma etching" system operating at 0.4 Pa has the least RIE-lag (Figure 2-4) [4]. Although it may be tempting to conclude that lower pressure can ameliorate RIE-lag, Gottscho and Jurgensen point out that, when a reactor's geometry is altered, the change in pressure alone may be inadequate to account for the improvement in RIE-lag [4].

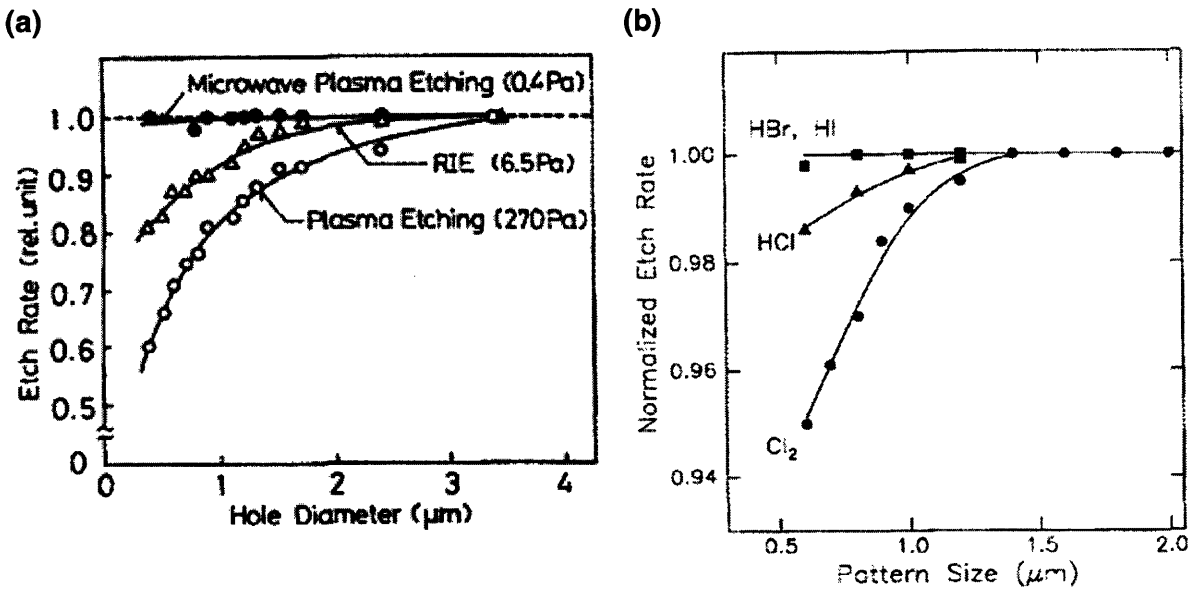

Figure 2-4 – (a) Effect of pressure on etch rate [4] and (b) effect of chemistry on etch rate [4].

Inhibitors can be by-products that adsorb on the microstructure bottom or sidewall in many RIE etch processes. Other RIE etch processes such as deep reactive ion etch deliberately introduce passivant precursors such as CHF_3 and CH_4 into the chamber that form inhibitors. The generation of inhibitors from diffusing by-products and the transport kinetics of inhibitors can reduce the etch rate at the bottom of a microstructure and protect the sidewalls from undercutting. The transport kinetics of inhibitors is influenced by the substrate temperature. In the case of DRIE, lower substrate temperature lowers the volatility of SiF_xO_y etch products such that they are absorbed on the sidewalls. The inhibitors on the sidewall aid the anisotropic etching process by protecting the sidewalls from ion bombardment, while the inhibitors at the trench bottom are eroded. But if inhibitors dominate in the etching/deposition balance, "black silicon" islands can form and the etching progress dissipates while further exacerbating non-uniformity [7].

2.3.3 Ion Flux Distribution

Ions exiting the plasma undergo acceleration and collisions as they enter the sheath. The acceleration and collisions provide the ions with energy and angular distribution (directionality) as they impart on the wafer. In an ICP chamber, the flux and concentration of the ions at different locations along the wafer depend on both the generation of the species from the plasma and the collisions of the species within the sheath. For typical plasma chambers the angular distribution can be modeled as a cosine function, depending on how the ions are generated. The ionization process in the plasma is influenced by inelastic collisions of electrons with neutrals. Collisions within the plasma and during acceleration in the sheath result in a flux profile that is not perfectly directional. Figure 2-5 shows both an ideal and a real ion flux angular and energy distribution.

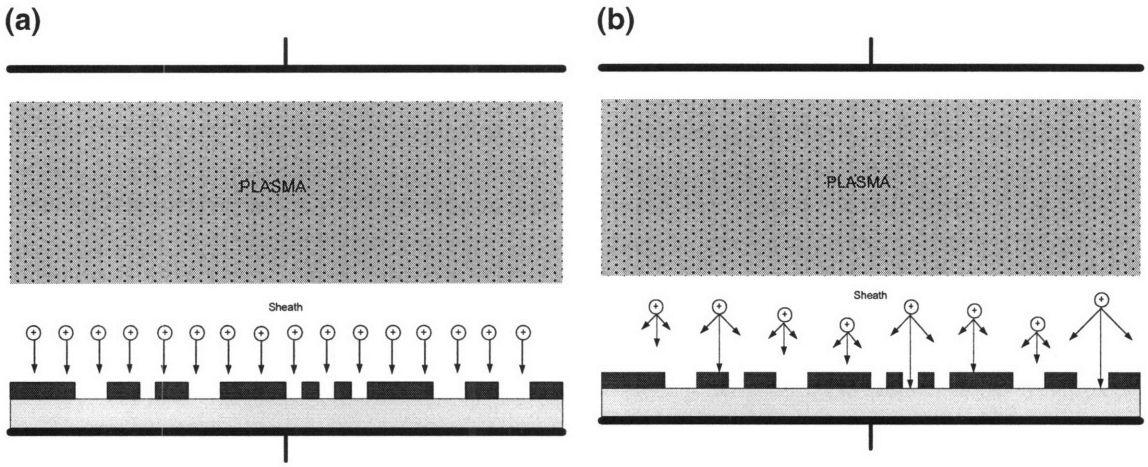

Figure 2-5 – (a) Schematic of ideal ion flux versus (b) real ion flux with distribution of energies (velocities) and angles.

2.3.4 Neutral Flux Distribution

Neutral flux distribution is often modeled as isotropic. But due to collisions within the plasma, the neutral species will have an angular distribution as they enter the sheath. The

neutrals may also undergo elastic collisions within the sheath, depending on the sheath thickness and the mean free path of the neutral species. These elastic collisions contribute to neutral angular flux distribution [8]. Any asymmetries in the plasma will propagate into the neutral flux out of the plasma.

Nonetheless, the neutral flux distribution is often considered to be isotropic with equal arrival at all points on the wafer surface [7]. In modeling the behavior of neutral species as isotropic, we exclude fast neutrals created by charge-exchange reactions with ions [4]. In great abundance, these fast neutrals may significantly and non-uniformly affect the etching rate, depending on their profile. Fast neutrals may etch away the substrate faster than low energy neutrals because their higher energy accelerates their adsorption and reaction with the substrate. Uneven etching rates across the wafer may result from a large proportion of fast neutrals within the overall neutral flux. Figure 2-6 shows the ideal and real neutral flux distribution.

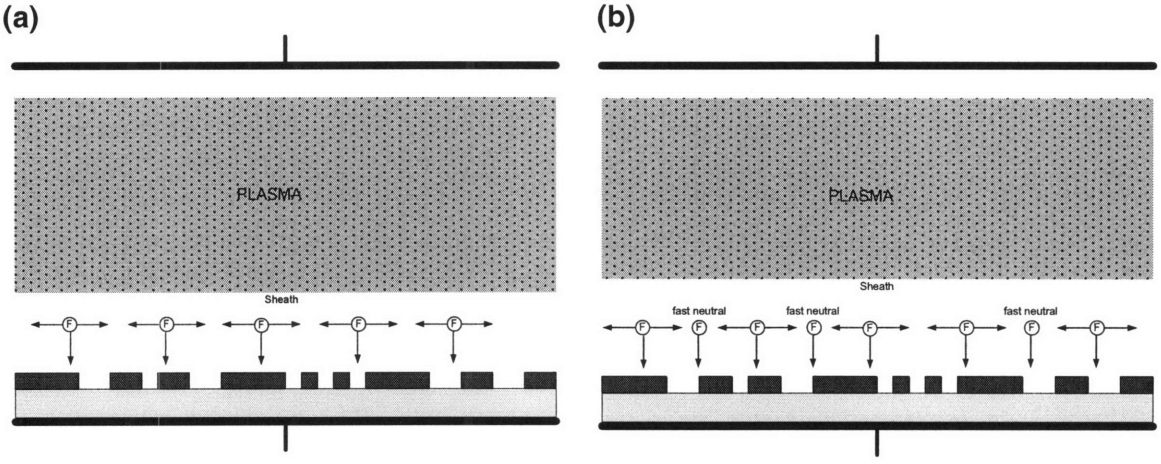

Figure 2-6 – (a) Schematic of ideal neutral flux versus (b) real neutral flux.

2.3.5 Ion Neutral Synergism

Ion neutral synergism, as described by Gottscho and Jurgensen, models etch rate as a function of ion flux, neutral flux, and surface coverage. The etch rate is given in terms of ion flux as

$$R = k\Theta E_i J_i \tag{2-1}$$

where k is the volume removed per unit bombardment energy (cm^3/eV) for a saturated surface, Θ is the fraction of surface with adsorbed neutral species (surface coverage), E_i is the average ion energy in electron volts (eV), and J_i is the ion flux ($cm^{-2}s^{-1}$) to the surface of the wafer [4]. The etch rate is also given in terms of the neutral flux as

$$R = vS_o(1-\Theta)J_n \tag{2-2}$$

where v is the volume removed per reacting neutral (cm^3), S_0 is the reactive sticking probability on a bare surface (unitless), and J_n is the neutral flux ($cm^{-2}s^{-1}$) to the surface [4]. In the case of etch rate as determined by neutral flux, we assume that the reactive sticking probability of neutrals is proportional to the number of bare sites on the surface, (1- Θ). We obtain an expression (Equation 2-3) for the surface coverage as a function of ion energy flux to neutral flux ratio by equating expression (Equations 2-1 and 2-2).

$$\Theta = \frac{1}{1+\frac{kE_iJ_i}{vS_oJ_n}} \tag{2-3}$$

By substituting Equation 2-3 into Equation 2-1, we obtain the expression for etch rate as a function of the ion and neutral flux as follows:

$$R = \frac{kE_i J_i}{1 + \frac{kE_i J_i}{vS_o J_n}} \tag{2-4}$$

There is a clear synergism between the fluxes of ions and neutrals. With negligible neutral flux, $vS_o J_n = 0$, the etch rate vanishes, except for ion sputtering [4]. Similarly, with negligible ion flux, $kE_i J_i = 0$, the etch rate vanishes, except for thermally activated neutral etching. The total etch rate is greater with both ions and neutrals than with either alone [4].

Furthermore, Equation 2-4 presents two interesting limiting cases. For $vS_o J_n >> kE_i J_i$, the surface is saturated with neutrals and the etch rate, $R = kE_i J_i$, becomes independent of neutral flux [4]. When $vS_o J_n << kE_i J_i$, the surface is starved of neutrals and the etch rate, $R = vS_o J_n$, is proportional to the neutral flux [4]. Thus Equation 2-4 predicts that at constant ion energy flux, the etch rate will initially increase in proportion to the neutral flux and then saturate as the neutral flux continues to increase [4].

Sun et al. observed this ion neutral synergism in their experiment to determine the effect of wafer level loading on etch rate [11]. Through experiments where they etched wafers of increasing loading, from 0.03 to 17.6 percent, they were able to determine the time averaged ion and neutral distributions across the wafer (Figure 2-7) [11][12].

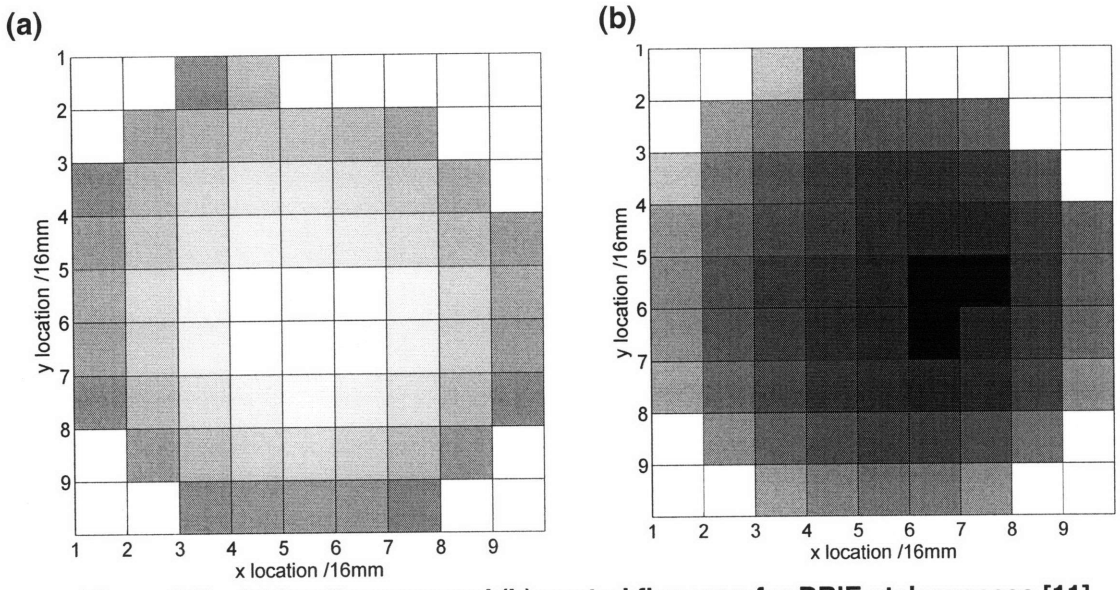

Figure 2-7 – (a) Ion flux map and (b) neutral flux map for DRIE etch process [11].

2.4 Pattern Induced Non-uniformity

Non-uniformity can also be caused by the structures on the wafer. These patterned microstructures affect overall etch uniformity at different levels. In aggregate, all the unmasked structures on the wafer contribute to loading or macroloading that reduces the etch rate for all structures on the wafer. Loading refers to surface area or open area of a wafer that is unmasked and is being etched, divided by the total surface area of the wafer.

Wafer level pattern induced non-uniformity is also influenced by the overall generation and flux of etch species as described in Section 2.3. At the chip or die level, open area microstructures load down reactant species in competition with other parts of the die and between dies. This is the die-level pattern induced non-uniformity. At the microstructure or feature level, reactant transport to the bottom of the trench is the limiting factor in overall etch uniformity. The three forms of loading dependent non-uniformity are described next.

2.4.1 Wafer Level Non-uniformity

Wafer level loading or macroloading contributes to overall etch rate non-uniformity by loading down etchant species and thus reducing the overall amount of available species at all parts of the wafer. Macroloading is effectively an aggregate or averaged reduction in reactant species. For a given set of etching conditions, the loading effect is characterized by a decrease in etch rate as the quantity of material to be etched is increased [5]. Loading is therefore proportional to the inverse of etch rate ($1/ER$) (Equation 2-5) [5]. The etching conditions include gas pressure, gas flow rate, RF power density, and the temperature of the substrate. Most of these conditions were addressed in Section 2.3. This means that the etch rate will decrease as a function of the percentage of open area on the wafer.

$$1/ER \propto loading \tag{2-5}$$

Although the overall etch rate for the wafer decreases as loading increases, the decrease in etch rate is non-uniform across the wafer surface. Parts of the wafer etch more quickly than other parts. In DRIE experiments on an STS ICP etcher at MIT's Microsystems Technology Laboratories by Sun et al., the percentage of overall loading affected the profile of etch rate across the wafer [12]. Figure 2-8 shows the experiment for four levels of loading: 0.03 and 17.6 percent, respectively. For low loading, 0.06%, there is a "hot spot" or fast etch rate region that forms, and a gradient from the area of fast etching to the area of slow etching (Figure 2-8). As the loading increases to 17.6%, a "cold spot" or slow etching region forms, and there is a gradient of etch rates from the area of slow etching to the area of fast etching (Figure 2-8). This experiment shows that

both the overall wafer etch rate and spatial uniformity of the etch rate are affected by loading.

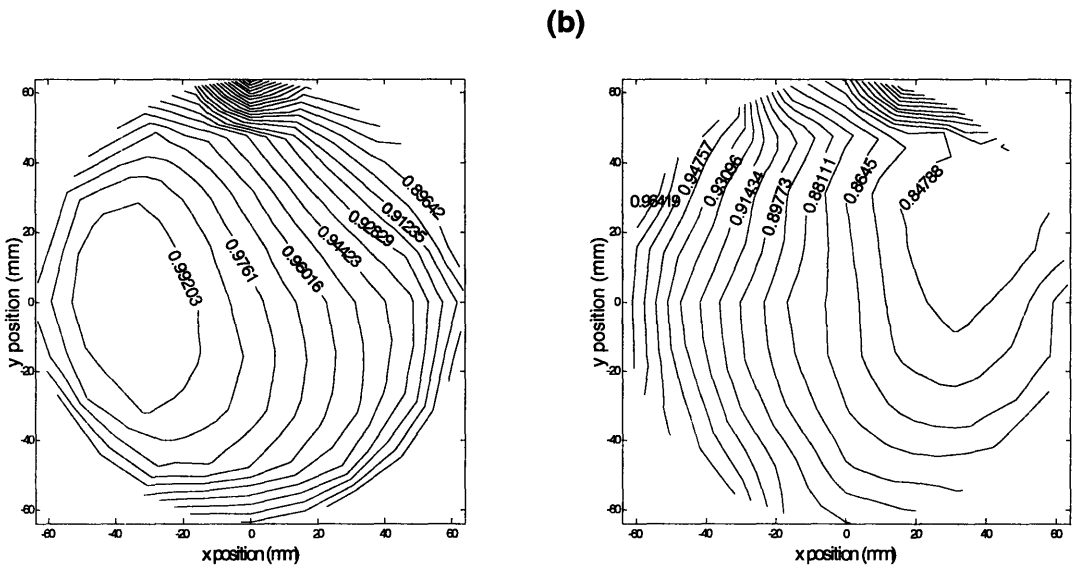

Figure 2-8 – (a) Global etch map for 0.06% loading, which features a hot spot at the middle left part of the wafer [12]. (b) Global etch map for 17.6% loading, featuring a cold spot at the upper right region of the wafer [12].

Sun et al. made several observations about how global loading interacts with ion neutral synergism theory as described in Section 2.3.5 [12]. For low pattern densities, ion transport is the dominant factor in determining uniformity since neutrals are in abundance [12]. As a result, layouts with low loading (<10%) generally exhibit a "hot spot" with a higher than average etch rate. Since neutrals are depleted as pattern density increases (>10%), the behavior is governed by neutral transport and results in a "cold spot" with lower etch rate (Figure 2-8).

2.4.2 Die Level Non-uniformity

Variations at the die level refer to spatial differences in etch rates within and between dies. These variations are not for differences between specific features within or between dies, but rather indicate differences between and within regions of dies. This means that

die level variations are the averaging effects of neighboring structures within and across dies. Variations are primarily due to microloading, which refers to the localized reduction in etch rate as the amount of local open area increases. The local open area, which we defined as pattern density, is the ratio of unmasked area to mask area within any unit area across dies. Pattern density can vary depending on the size of the unit area chosen.

We define die-level variation as a local dependence of etch rate on pattern density. Qualitatively, dies or regions in a die that are surrounded by highly loaded areas will etch more slowly, since they encounter more competition for reactants [13]. This phenomenon is analogous to the microloading effect.

Microloading is the reduction in local etch rate due to competition for reactive species. In areas of high local loading, there is a depression in the available reactive species leading to slower etch rates. Another effect of microloading is to create a concentration gradient between areas of high loading having depleted reactant species, and areas of low loading having abundant reactant species. This leads to the diffusion of reactant species from areas of low loading to areas of higher loading (Figure 2-9).

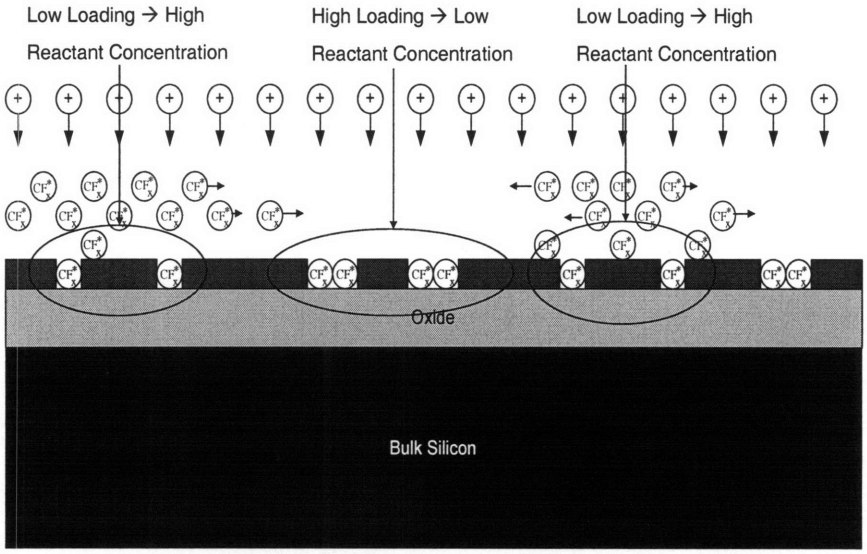

Figure 2-9 – Schematic of the depletion of reactants due to microloading.

2.4.3 Feature Level Non-uniformity

Feature-level variation refers to differences in etch rate due to differences in aspect ratio (Figure 2-10). The differences in etch rate for individual features primarily depends on the transport of reactants within the microstructure as their aspect ratio evolves. A thorough discussion of transport kinetics in ARDE is given in Section 2.5. The transport kinetics of reactants within a trench is used as the theoretical foundation of our ARDE model described in Chapter 7.

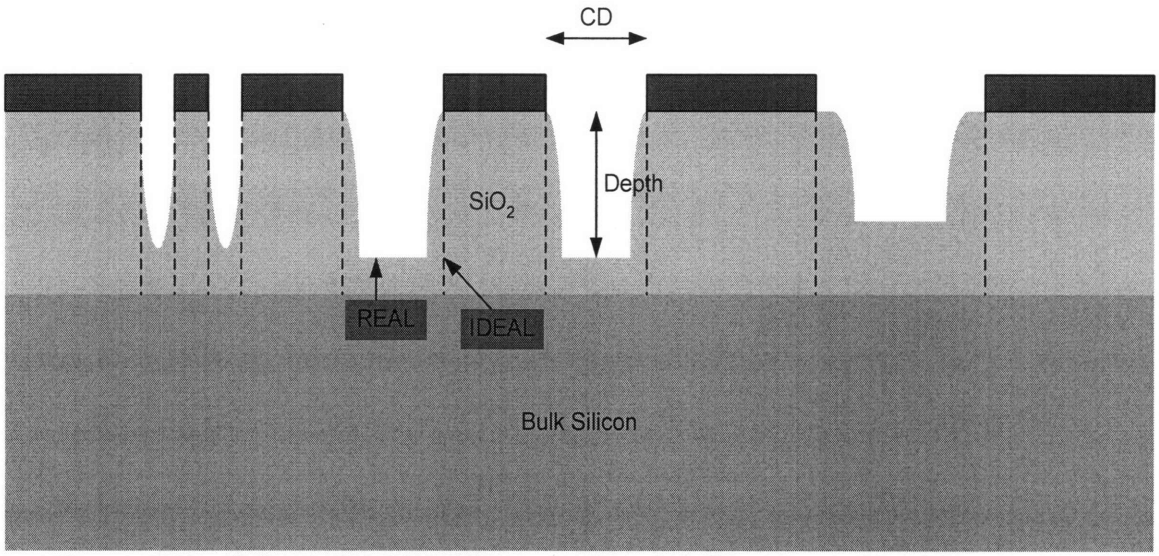

Figure 2-10 – Schematic of feature non-uniformity. Structures with different critical dimension (CD) etch at different rates due to ARDE effects.

2.5 Aspect Ratio Dependent

Aspect ratio dependent etching refers to etch rate and profile dependence on the time and interface evolution in the dimensions of the microstructure being etched. In this thesis, we focus exclusively on the etch rate dependence on time evolution of the feature and ignore the profile dependences. Rangelow, Gottscho, and Shaqfeh have fully characterized profile dependence on aspect ratio [4][7][14]. There are three physical mechanisms by which etch rate depends on aspect ratio: ion shadowing, neutral

shadowing, and Knudsen diffusion. All three mechanisms involve the transport kinetics of etch species within the dimension of the etching microstructure and are discussed next.

2.5.1 Ion Shadowing

Ion shadowing is the dependence of the etch rate on the ion flux. The amount of ion flux reaching the bottom of the microstructure depends on ion angular distribution. Ions that undergo collisions in the sheath will arrive at the wafer surface with hyperthermal energies and off-normal angles of incidence [4]. For hyperthermal energies beyond the relative sputtering threshold, ion-enhanced etching will occur on the sidewall as well as on the bottom surface. Gottscho et al. point out that under these conditions, the number of ions able to impact the bottom surface relative to the number impacting the sidewalls will decrease as the aspect ratio increases [4]. This is the qualitative basis for RIE-lag and such profile phenomena as sidewall bowing [4].

Models for ion angular distribution are critical for simulating etch profiles. Zarowin has noted the importance of off-normal ion incidence in determining reactive ion etched profiles [15]. Jurgensen presented a simple angular distribution model that is qualitatively consistent with the shape of etching profiles and magnitude of RIE-lag effect, and scales with pressure [14]. Other models assume an ion angular distribution that is Gaussian or modified Gaussian. Ion shadowing is most critical in the regime, $\nu S_o J_n >> kE_i J_i$, where the surface is saturated with neutrals and the etch rate becomes independent of the neutral flux.

Geometric analysis can be used to understand ion and neutral shadowing. Figure 2-11 shows a schematic of a microstructure undergoing an etch process. As the trench etches

deeper over time, the angular spread of the ions and neutrals that can reach the bottom becomes smaller and smaller. As a result, the etch rate decreases.

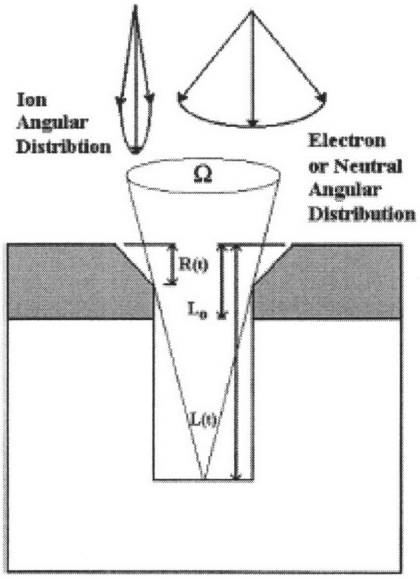

Figure 2-11 – Illustration of shadowing effect [16].

2.5.2 Neutral Shadowing

Neutral shadowing is the dependence of the etch rate on the neutral flux. ARDE can be induced by neutral shadowing when the reaction is neutral limited, i.e. $vS_oJ_n << kE_iJ_i$. Under neutral limited etching, the transport of neutral reactants dominates the RIE lag effect. The first assumption for neutral shadowing is that we exclude fast neutrals created by charge-exchange reactions with ions [4]. This results in the neutral angular distribution being nearly isotropic and the energy distribution being nearly Maxwellian [4]. In an idealized scenario suggested by Gottscho and Jurgensen, we can ignore particles scattered from the sidewalls and consider only reactants that have line-of-sight from the plasma in calculating the etch rate at the center of the bottom of a microstructure [4].

2.5.3 Knudsen Transport

Knudsen transport is the movement of an incident molecule through an orifice without reacting with the side-wall of the orifice. Take a two chamber system connected by an orifice as shown in Figure 2-12. The diffusion of a molecule in chamber 1 with pressure 1 through the orifice into chamber 2 with pressure 2 depends on the pressure and the geometry of the orifice. Knudsen transport states that there is a probability coefficient K that a molecule will start in chamber 1 and diffuse to chamber 2.

The probability coefficient K completely depends on the geometry of the tube that the molecule transits. The molecule reflects off the sidewall of the tube following a cosine law and there is no sticking on the tube sidewall. In application to plasma etch, K is the molecular transmission probability or likelihood that an incident molecule will reach the trench bottom by diffusion. K is dependent on aspect ratio, and has been empirically tabulated in the literature [17][18]. Figure 2-13 plots the transmission coefficient K as a function of aspect ratio. This model, or variants of this model, will be used in the proposed non-uniformity model discussed in Chapter 7.

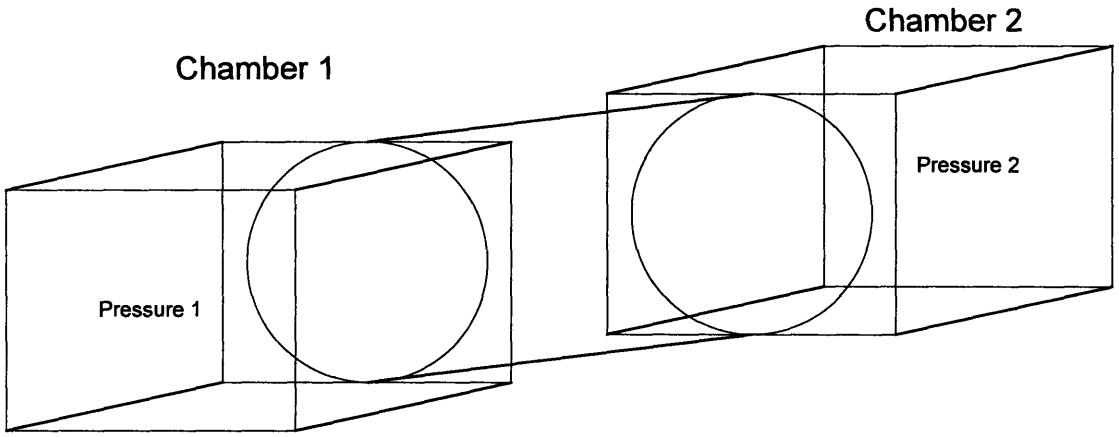

Figure 2-12 – Schematic of Knudsen transport between two chambers.

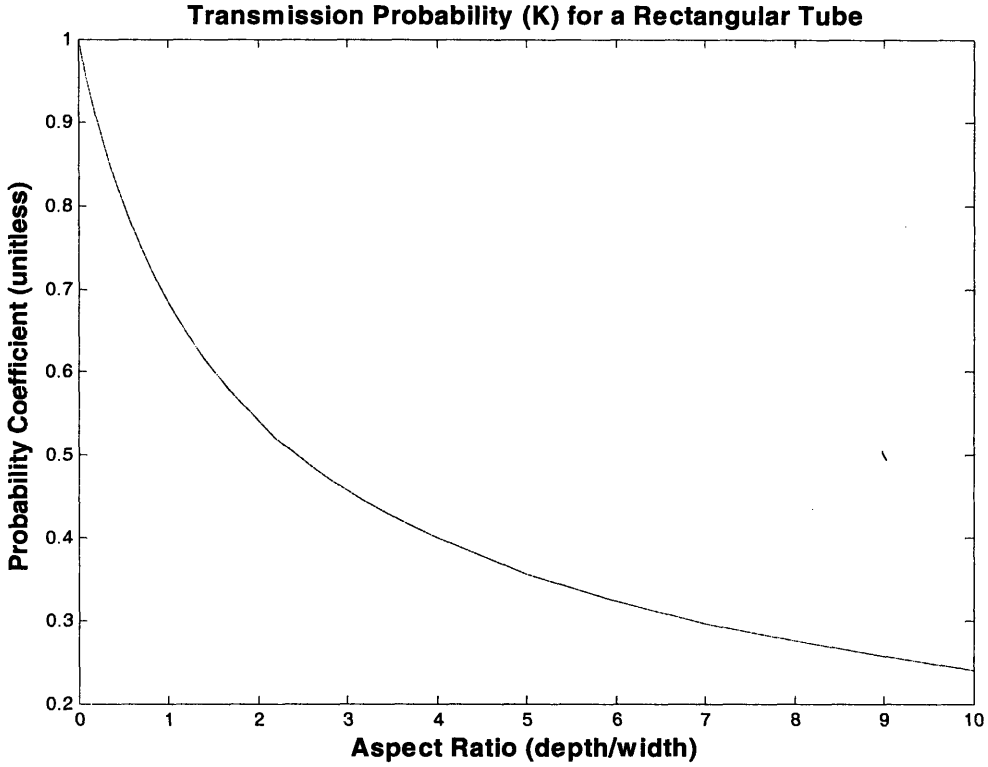

Figure 2-13 – Plot of Knudsen transmission probability, K.

2.6 Summary

This chapter reviews the relevant theories, terminologies and models used to describe plasma etch non-uniformities, and discusses each of them in terms of wafer-, die-, and feature-level scales which have been designated for our pattern density and aspect ratio dependent based prediction models.

Chapter 3

Mask Description

A test mask is used in this work to understand and characterize pattern dependent variations in plasma etching. The mask pattern was originally designed to study electro-copper deposition (ECD) and chemical mechanical polishing (CMP) pattern dependencies, using a wide range of feature and density structures. The mask has structures that allow for characterization of the effects of aspect ratio and pattern density on the etch rate of trench lines. The mask further allows for the modeling of the plasma etch process, improving ECD and CMP models, and integrating plasma etch, ECD, and CMP models.

In this chapter, the mask floor plan and layout is presented in Section 3.1. We then present two set of structures that are used in generating a data set for this thesis. Section 3.2 describes the capacitance structures, while Section 3.3 describes the line width and space structures. Finally, Section 3.4 concludes the chapter.

3.1 Mask Floor Plan

The test mask is 15.1x22.3 millimeters in size and has a floor plan consisting of seven regions: (1) capacitance/comb structures, (2) line width and space (LWS) structures, (3) variable array structures, (4) variable line length structures, (5) dummy fill structures, (6) slotting structures, and (7) near neighbor structures. These structures correspond to the labels listed in Table 3-1.

Table 3-1 – Definition of block names for the Copper Mask.

No.	Structure Name	Structure Definition
1	Cap_Total	capacitance/comb structures
2	CuLineArrayBlock	line width and space structures
3	Var_Array_Total	variable array structures
4	ISO_var_Length_Total	variable line length structures
5	DummyBlock	dummy fill structures
6	SlotBlock	slotting structures
7	Iso_Line_$_Boxsand_Total	near neighbor structures

The nomenclature for line width and space structures and capacitance structures are as shown in Table 3-2. The line width and space structures, along with the capacitance structures, are the most relevant in our research to determine pattern dependent effects caused by plasma etching. The other structures are useful for verification and extension of our etch model and models (ECD and CMP) that predict copper metallization variations.

Table 3-2 – Nomenclature for individual Capacitance and Line Width and Space blocks.

Structure Name	Structure Definition
BlockLinelw0_1ls0_27	Line Width/Space of 0.1 and 0.27 micron, respectively
BlockLinelw3ls1	Line Width/Space of 3 and 1 micron, respectively
Cap_Combo$LW_0_1LS_6$LW_5LS_5	Two Capacitance Structures: Line Width/Space of 0.1/6 and 5/5 microns
Cap_Combo$LW_6LS_0_8$LW_0_5LS_1	Two Capacitance Structures: Line Width/Space of 6/0.8 and 0.5/1 microns

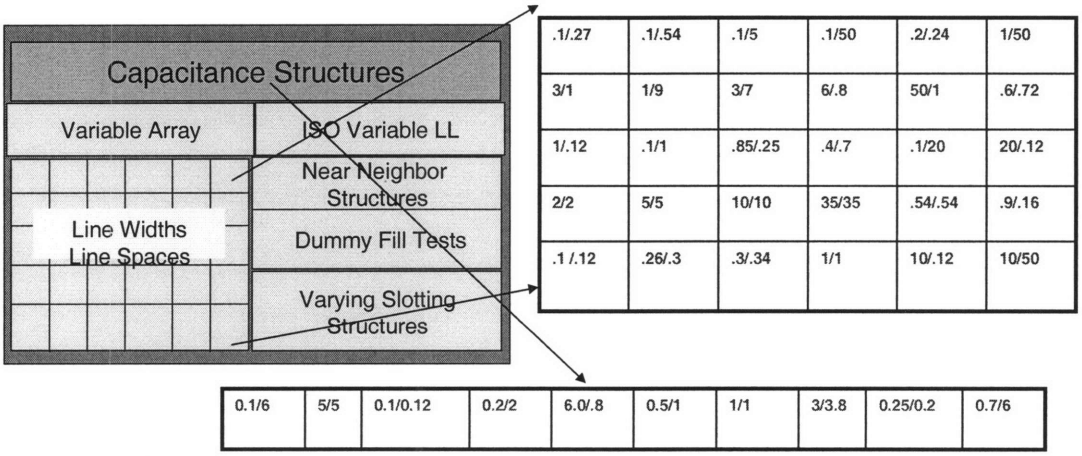

Figure 3-1 – Schematic of copper mask along with line widths and line spaces for each capacitance and line width and space structure (in μm).

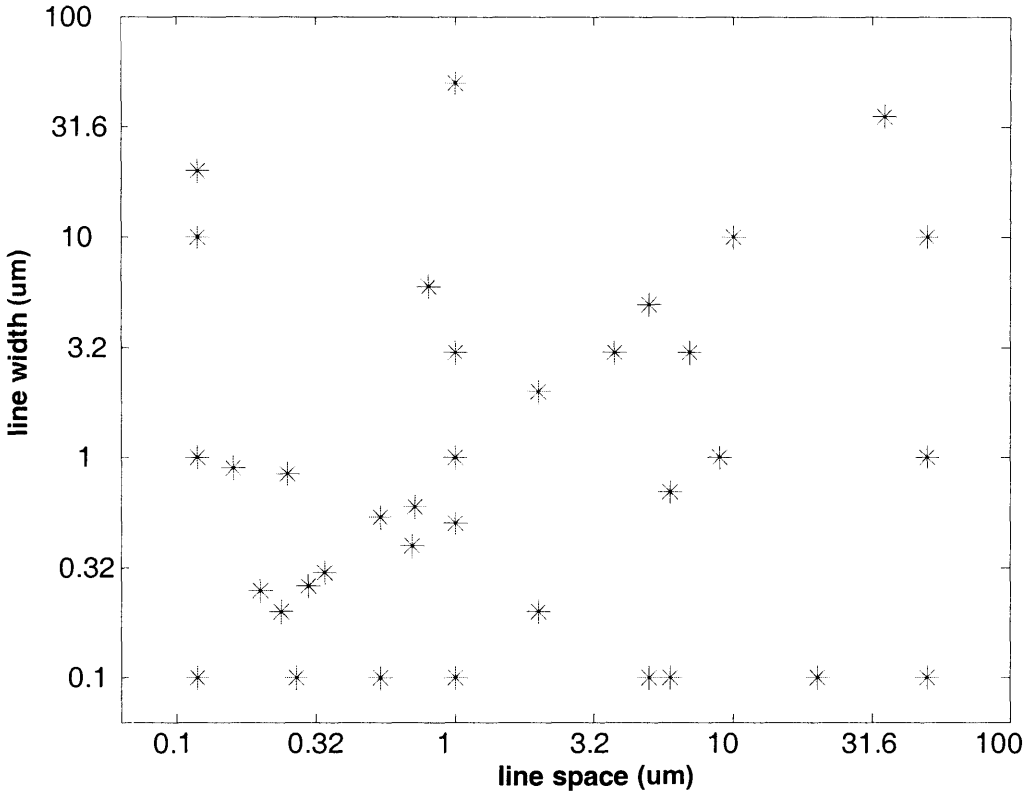

Figure 3-2 – The design space of line widths and spaces encompassed by the capacitance and line width and space structures.

The various line width and line space combinations for the capacitance and line width and space structures are shown in Figure 3-1. The layout design space spanned by the two regions is mapped in Figure 3-2. Figure 3-3 illustrates the layout of the capacitance and line width and space structures on test mask.

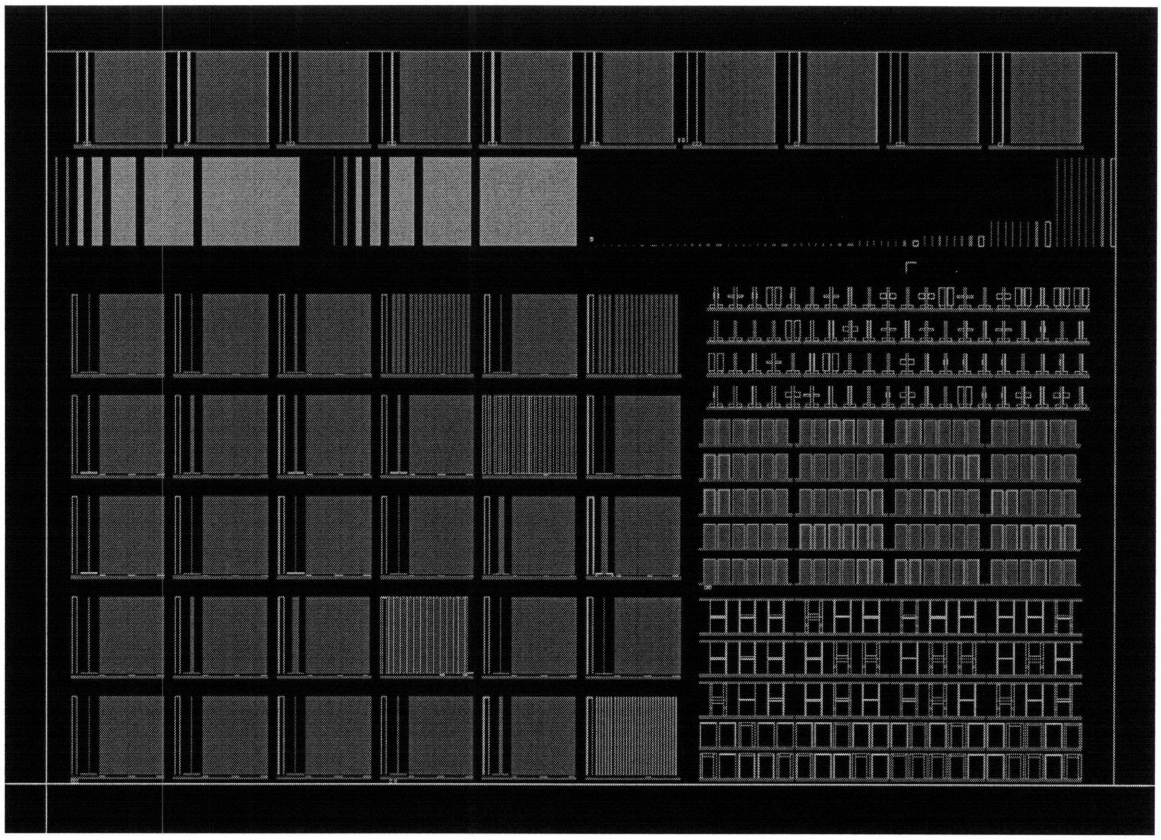

Figure 3-3 – Test mask layout.

3.2 Capacitance/Comb Structures

Capacitance or comb structures are designed for post-metallization electrical measurements for the study of ECD and CMP process induced variations. For our etch variation studies, these capacitance structures also provide post-etch measurement data for studying etch process non-uniformity. Capacitance structures form arrays of trench lines as illustrated in Figure 3-4. Capacitance structures are indexed from CA1 to CA10, left to right, as shown in Figure 3-4.

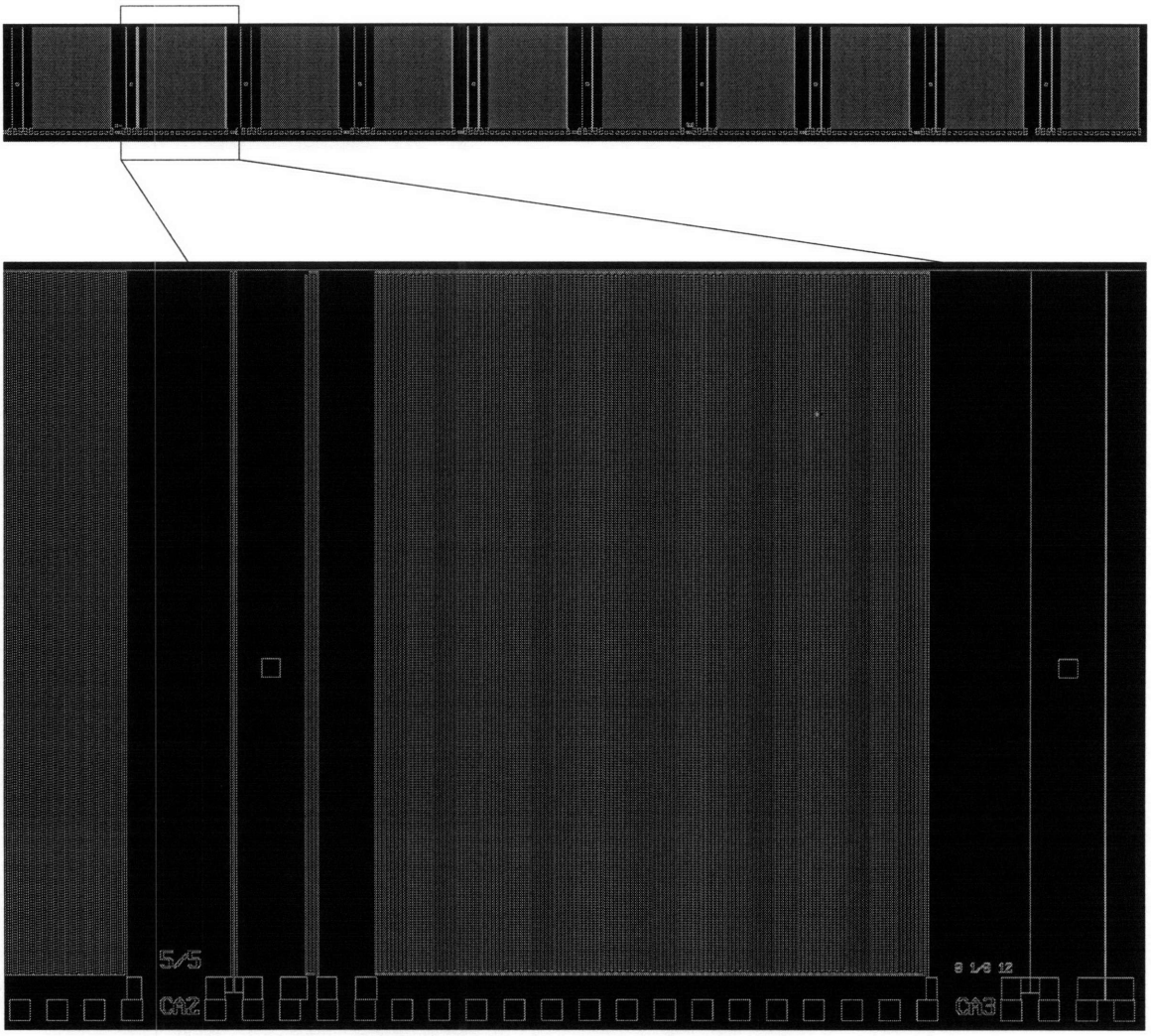

Figure 3-4 – Capacitance structures.

3.3 Line Width Line Space Structures

There are thirty LW/LS structures arranged in an asymmetric assortment of pattern densities and pitches. These structures, along with the capacitance structures, are used to characterize the dependence of etch rate, depth, critical dimension, and line space on density and pitch.

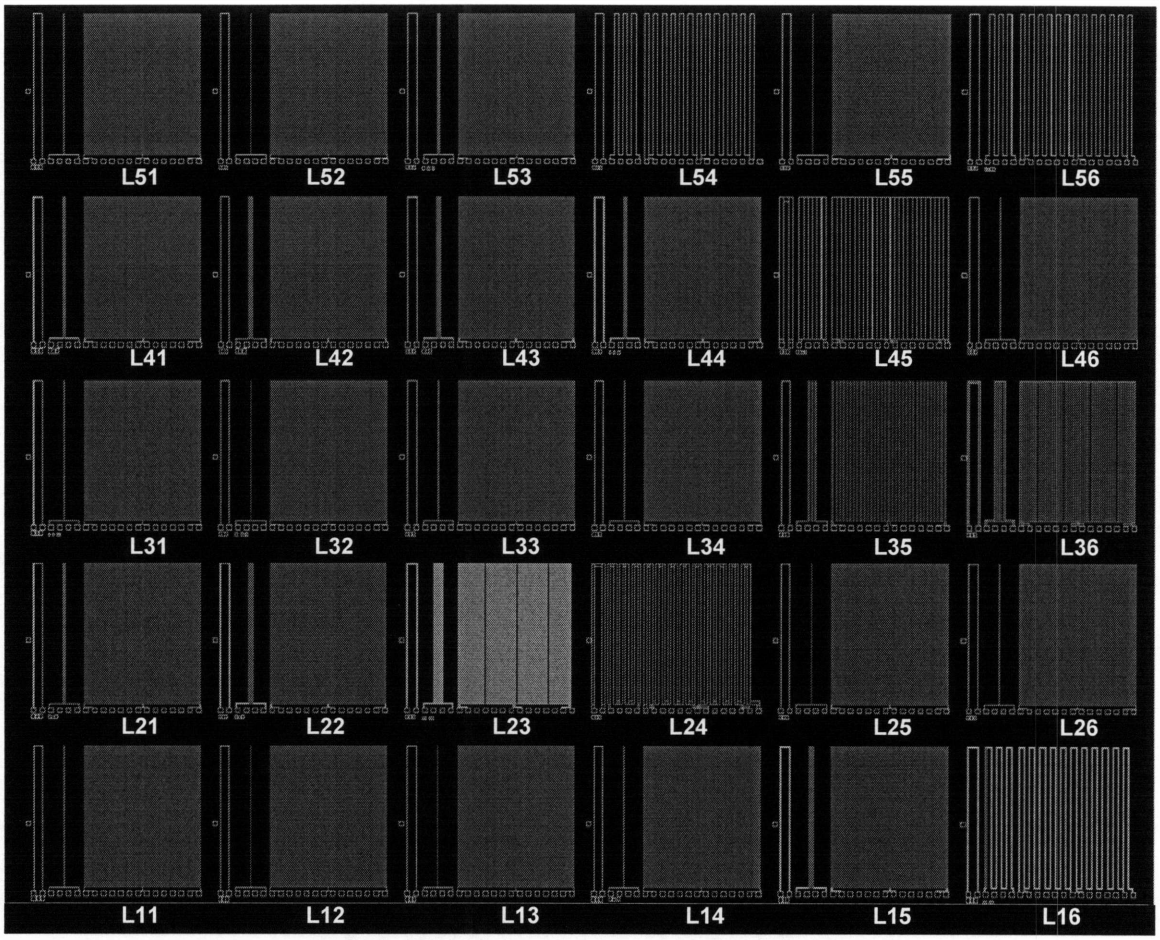

Figure 3-5 – Line width and space structures.

These LWS structures are also used in modeling etch rate and CD profile. They are in a row and column arrangement with each structure given identified with an L, followed by the row and column numbers as shown in Figure 3-5. The asymmetric arrangement of the structures allows for the interaction of neighboring structures with different pattern densities. This interaction affects the microloading of individual trenches which are in competition for reactants as explained in Chapter 6. We are also able to examine and understand the transition from a high density region to a low density region by examining trench lines of adjacent structures with high and low densities, respectively.

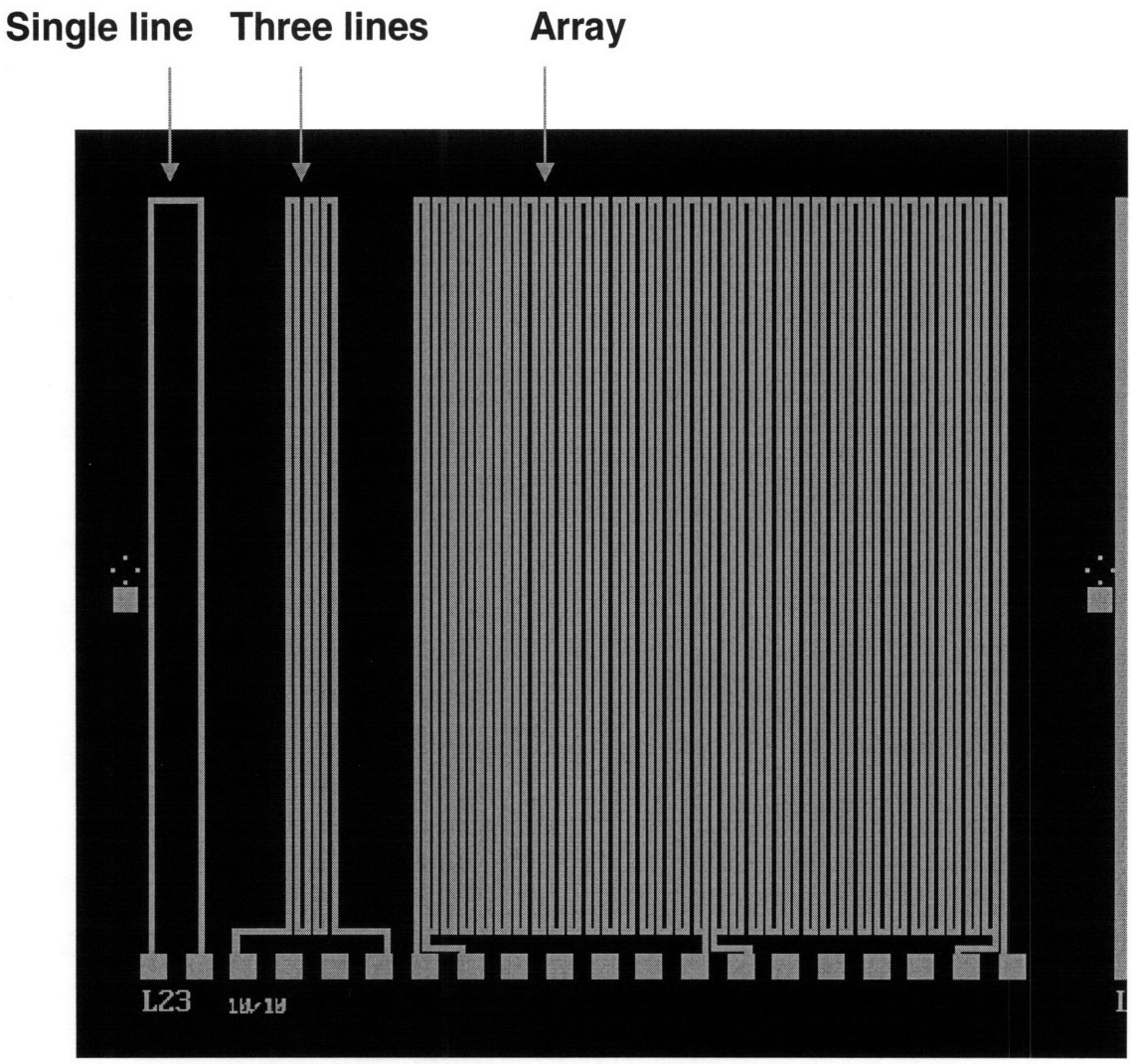

Figure 3-6 – Close up view of a line width and space module with line width and line space of 10 μm and density of 50%.

Each module consists of (1) an isolated line, (2) an isolated serpentine line, and (3) an array of serpentine lines (Figure 3-6). The isolated line is a single line that goes up and bends back down. The isolated serpentine line is also a single line that goes up and bends down three times. The array is composed of many trench lines that are connected as shown in Figure 3-6. For each LWS module, all three parts of the module fit in a 1919 μm x 1702 μm region. Table 3-3 gives the specification for all the modules, including the

local pattern density, the targeted etch depth, and the resulting targeted feature level aspect ratio.

Table 3-3 – Specifications for each line width and space structure.

Module Name	Line Width (in μm)	Line Space (in μm)	Pitch (in μm)	Line Length (in μm)	Density	Targeted Depth (in μm)	Targeted Aspect Ratio
L51	0.1	0.27	0.37	1604	0.27027027	0.27	2.7
L52	0.1	0.54	0.64	1604	0.15625	0.27	2.7
L53	0.1	5	5.1	1604	0.01960784	0.27	2.7
L54	0.1	50	50.1	1604	0.00199601	0.27	2.7
L55	0.2	0.24	0.44	1604	0.45454545	0.27	1.35
L56	1	50	51	1604	0.01960784	0.27	0.27
L41	3	1	4	1604	0.75	0.27	0.09
L42	1	9	10	1604	0.1	0.27	0.27
L43	3	7	10	1604	0.3	0.27	0.09
L44	6	0.8	6.8	1604	0.88235294	0.27	0.045
L45	50	1	51	1604	0.98039216	0.27	0.0054
L46	0.6	0.72	1.32	1604	0.45454545	0.27	0.45
L31	1	0.12	1.12	1604	0.89285714	0.27	0.27
L32	0.1	1	1.1	1604	0.09090909	0.27	2.7
L33	0.85	0.25	1.1	1604	0.77272727	0.27	0.317647059
L34	0.4	0.7	1.1	1604	0.36363636	0.27	0.675
L35	0.1	20	20.1	1604	0.00497512	0.27	2.7
L36	20	0.12	20.12	1604	0.99403579	0.27	0.0135
L21	2	2	4	1604	0.5	0.27	0.135
L22	5	5	10	1604	0.5	0.27	0.054
L23	10	10	20	1604	0.5	0.27	0.027
L24	35	35	70	1604	0.5	0.27	0.007714286
L25	0.54	0.54	1.08	1604	0.5	0.27	0.5
L26	0.9	0.16	1.06	1604	0.8490566	0.27	0.3
L11	0.1	0.12	0.22	1604	0.45454545	0.27	2.7
L12	0.26	0.3	0.56	1604	0.46428571	0.27	1.038461538
L13	0.3	0.34	0.64	1604	0.46875	0.27	0.9
L14	1	1	2	1604	0.5	0.27	0.27
L15	10	0.12	10.12	1604	0.98814229	0.27	0.027
L16	10	50	60	1604	0.16666667	0.27	0.027

3.4 Summary

The copper mask is used to characterize and model the effect of line width and pattern density on etch rate. The capacitance and line width and space structures allow for characterizing and modeling etch rates, while the rest of the structures can be used to verify and extend the model.

Chapter 4

Experiment in Non-uniformity of Dielectric Plasma Etch

In this chapter, we present an experiment for determining the extent of etch uniformity dependence on pattern density and aspect ratio. Our methodological approach is to conduct two etch experiments using a standard 90 nanometer fixed etch process in collaboration with Texas Instruments Inc. The fabrication and measurements were performed in a level one environment at Texas Instrument's Kilby Research Fabrication in Dallas, Texas. The experiment fabricates the structures on the test mask described in Chapter 3. We take depth and width measurements of the fabricated structures to characterize pattern dependent etch variations and to calibrate models that predict these etch variations. The measurements form a data set which we use first in systematic models as a sampling of the variations that occur in the chosen fixed etch process. Once calibrated with the data set, our systematic models can give a prediction of depth variation in structures etched using the fixed 90 nm etch process.

The first experiment, which we will call our critical dimension (CD) experiment, allows for the study and modeling of CD variations in the case of an etch-stop based process. The second experiment, which we will call our depth experiment, allows for the characterization and modeling of depth variance in a timed (as opposed to etch-stopped) process. Although both experiments are discussed in this chapter, the depth experiment is the focus of the thesis work.

Section 4.1 presents the motivation and purpose of our experiments. Section 4.2 presents the process flow of the CD experiment to be used to determine critical dimension profile non-uniformity. Section 4.3 presents the process flow of the depth

experiment used to determine pattern density and aspect ratio dependent etching. Section 4.4 reviews how optical proximity correction (OPC) and the photolithographic process are used to match the printed structure on the wafer to the physical design. Section 4.5 reviews the interaction of etch variation with lithographic and OPC variation. Section 4.6 concludes the chapter.

4.1 Motivation

We are interested in understanding IC dual damascene trench etch variation for critical submicron technological nodes. In order to understand etch bias at submicron length scale, we design experiments for the 90 nanometer critical dimension node with minimum feature size of 100 nanometers. Our experiments mirror the production line interlayer dielectric trench etches seen in IC back end of the line (BEOL) processes; with the exception that experimental etch processes are not part of a production chip process and thus, are not preceded by a contact or via layer. This deviation may result in unforeseen differences between the models generated from our experiment and real metal trench depth and thickness variations seen in production chips.

Test wafers with varying feature sizes are fabricated in order to characterize and understand: (1) the dependence of feature dimensions such as line width, line space, and pitch on each other; (2) the dependence of etch rate on feature dimension and pattern density; and (3) the variation of feature dimension from design. After characterizing etch pattern variations, models are developed based on both empirical results along with physical understanding the etch process. These models are presented in Chapter 6 and Chapter 7. When generating our models, we take into account as much of the process

conditions and steps as needed to achieve an accurate prediction of the empirical results seen in our experiment.

The experiment and characterization is one of the steps in our layout prediction based model. Because each process condition is unique, an experiment must be performed for each process condition in order to calibrate the model. The test mask would be the same in all environments.

4.2 Critical Dimension Process Flow

The CD process flow creates a stack of dielectric materials on a bulk silicon substrate. The dielectric has an etch barrier (etch stop) layer. The etch stop layer prevents the downward etching of the dielectric during the etch process and allows for uniform depth across all structures on the wafer. The CD process is used to characterize etch profile non-uniformities and not depth or vertical etch rate variations. Any variations due to the etch process will manifest themselves in terms of profile deviations such as feature width, sidewall bowing, faceting, and slopped sidewall, which are described in Chapter 2. Therefore, the CD process is useful in studying trench width and space variations induced by plasma etch.

The layers of material on the stack are illustrated in Figure 4-1. The first material, Phosphorus Silicon Glass (PSG), is deposited through low pressure chemical vapor deposition (LPCVD). Then silicon nitride (SiN) followed by low temperature oxide (TEOS) is deposited by LPCVD. Silicon Carbide (SiC), a hard white or colorless crystalline material that is heat resistant, is deposited by chemical vapor deposition (CVD). This hard compound acts as the etch barrier because of its high selectivity (low etch rate) compared to oxide with respect to the etch chemistry. RIE lag and

microloading are overcome through over-etching after the barrier layer is reached, allowing for uniform depth across all microstructures, but at the cost of CD and feature shape non-uniformity.

After the etch barrier is deposited, phosphorus doped low temperature oxide (PTEOS) or cap TEOS is deposited by LPCVD. Then low dielectric constant (low-k) organic silicate glass (OSG) or CORAL is deposited via CVD. This is the primary dielectric material of the ILD stack. The low-k property of this material reduces capacitance between metal lines. PTEOS and SiN are deposited on top of the low-k OSG by LPCVD. The process flow is diagramed in Figure 4-1.

Three wafers go through the CD process flow. Following the deposition of the dielectric stack, the wafers undergo the 90 nanometer photolithographic process where the structures on our test mask are patterned on the dielectric. All three wafers have the CD stack and the test mask structures patterned on the stack. Two of the three wafers undergo a baseline oxide etch process using a carbon tetraflouride (CF_4) etch chemistry.

The etching of the dielectric stack consists of three etching steps. First the silicon nitride cap, along with the PTEOS, is etched off for 30 seconds. Then the OSG low-k CORAL is etched for 25 seconds. Finally, the cap TEOS (PTEOS) is etched for 20 seconds. The final etched stack profile is shown in Figure 4-2. The targeted depth of the metal one etch step is 2400 angstroms.

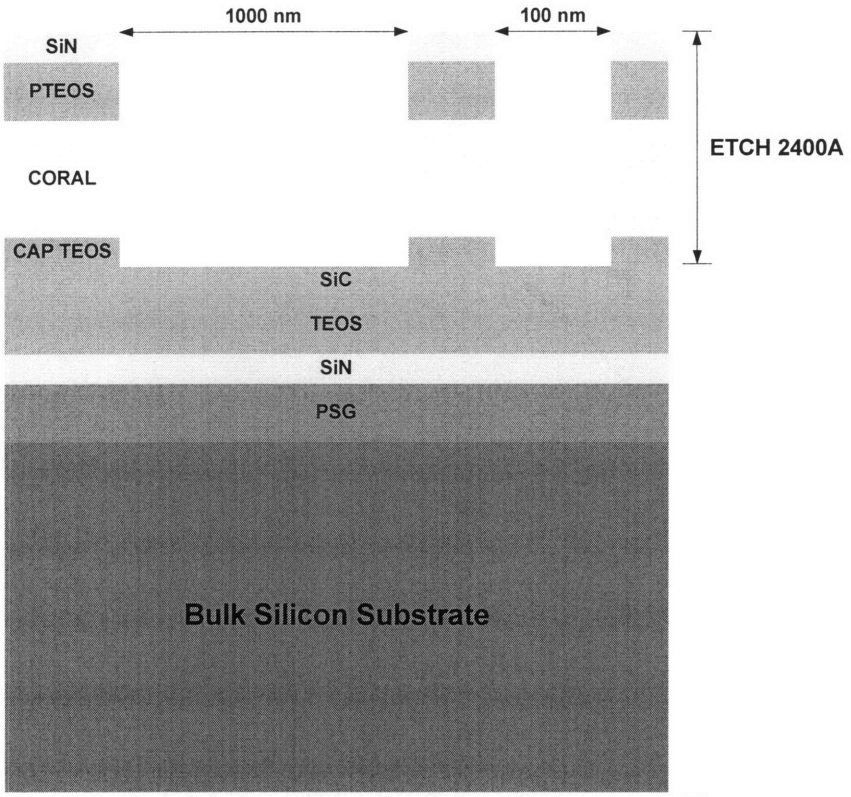

Figure 4-1 – CD process post-etch stack profile.

4.3 Depth Process Flow

The depth process flow is similar to the CD process but has a timed etching step instead of an over-etching step. The depth process is used to characterize etch depth and etch rate variations. The timed etch process into the dielectric stack allows for microloading and RIE lag to influence the etch rates of all the microstructures on our test chip. Therefore variations in the etch process will manifest themselves in terms of microloading and ARDE, as well as profile deviations such as sidewall bowing, faceting, and slopped sidewall. The etch rate non-uniformities are described in Chapter 2.

The initial material of the stack consists of PSG, which is deposited through LPCVD. Then silicon nitride, followed by TEOS, is deposited by LPCVD. Silicon Carbide is then deposited by CVD. Unlike the CD process, the silicon carbide is not used as an etch

barrier in the depth. Instead of using the SiC as an etch barrier, phosphorus doped low temperature oxide, PTEOS, is deposited by LPCVD. Then low-k organic silicate glass is deposited via CVD. By depositing a thick layer of CORAL, we are able to conduct a timed etch into the dielectric without overetching up to the etch barrier. Finally, PTEOS, followed by silicon nitride, is deposited by LPCVD. The depth process flow is diagramed in Figure 4-2.

As with the CD process, three wafers undergo the depth process. The deposition of the dielectric stack is followed by a 90 nanometer photolithography process. Two of the three wafers undergo a timed oxide etch process using a carbon tetrafluoride etch chemistry. The dielectric stack is etched for 75 seconds. The final etched stack profile is shown in Figure 4-2. The targeted depth is 2600 angstroms.

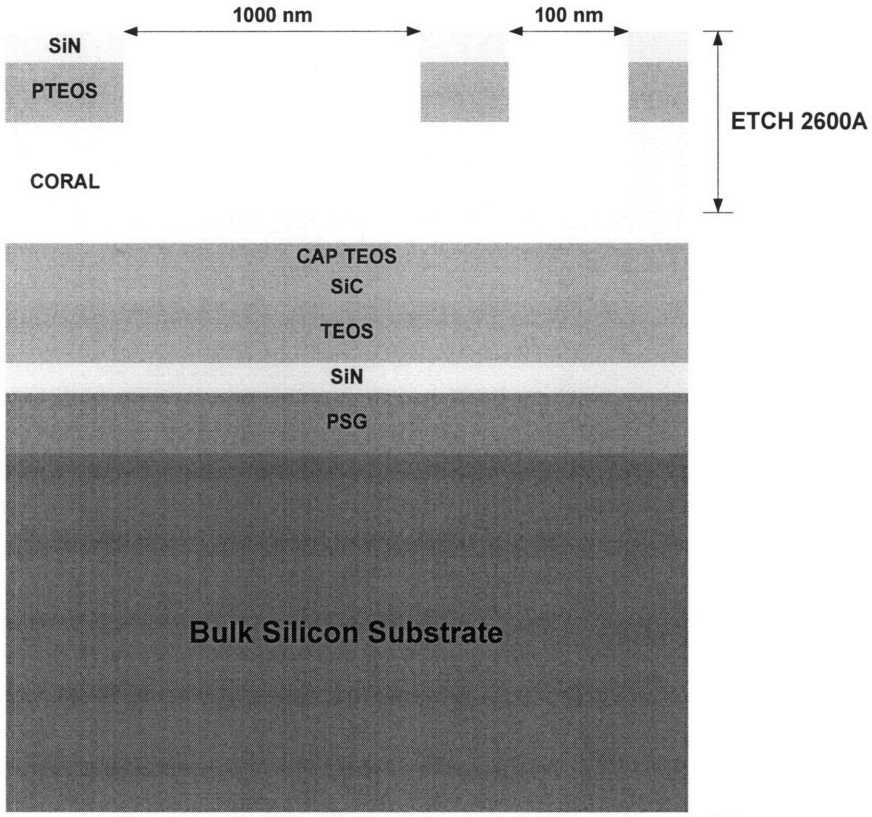

Figure 4-2 – Depth process post-etch stack profile.

4.4 OPC and Lithography

In modern submicron semiconductor integrated circuit production, mask alterations are routinely performed in order to enhance the printing of structures from a mask onto a wafer via photolithography [19]. Several techniques are currently in use such as optical proximity correction (OPC) and other reticle enhancement techniques (RET) [19]. OPC was first extensively used in the 0.18 micron node. OPC corrections may include modification of microstructures on the mask or the addition of auxiliary structures on the mask that enhance the microstructure but do not print on the wafer. These features are sometimes smaller than the exposure wavelength.

Two kinds of OPC corrections are currently used in the IC industry. The first is rule-based OPC where rectangles are added by a post-processor to features that meet design specifications [19]. The second is model based OPC where a simulation of the actual exposure of a feature on the resist is used to modify the mask in order to make the simulated feature match the physical design [19]. For our experimental test mask, rule-based OPC was performed so that the physical design will match what is printed on the wafer. Figure 4-3 shows a pre-OPC linewidth/linespace structure, which has a line width and space of 35 microns. Figure 4-4 shows the OPC corrected structure. The OPC mask has added line breaks in the long trench lines and line adjustments at bends and line ends along the trench lines.

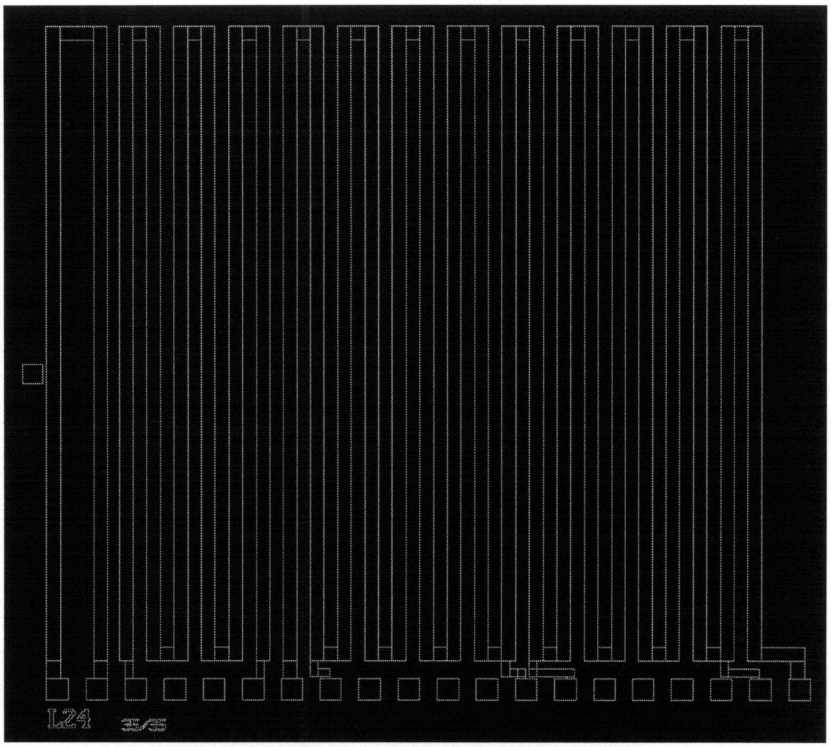

Figure 4-3 – Designed structure L24.

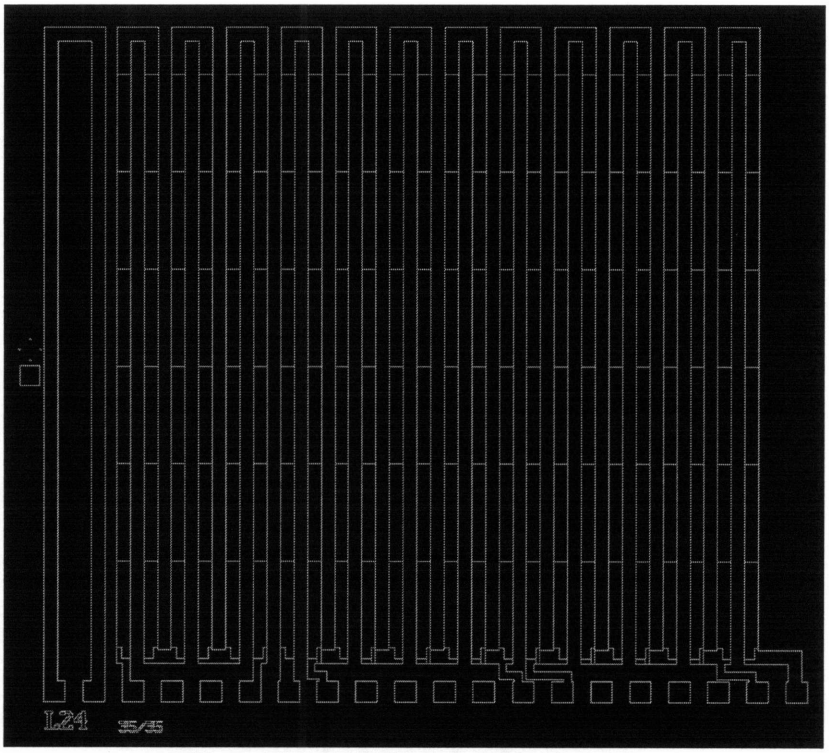

Figure 4-4 – OPC correction on L24.

4.5 Progression of Variations

Variations in back end of the line processes often propagate from one process step to the next. In the processes leading to trench etching, non-uniform surface topography before the ILD stack is deposited leads to varying surface topography in the field oxide thickness after deposition. Furthermore, even with OPC alterations, the photolithographic process introduces variations from the printing of the mask design into resist on the wafer. The roughness of the developed resist leads to roughness in the critical dimension of the etched microstructure. Figure 4-5 shows a schematic of the variations introduced by the processes leading to plasma etching.

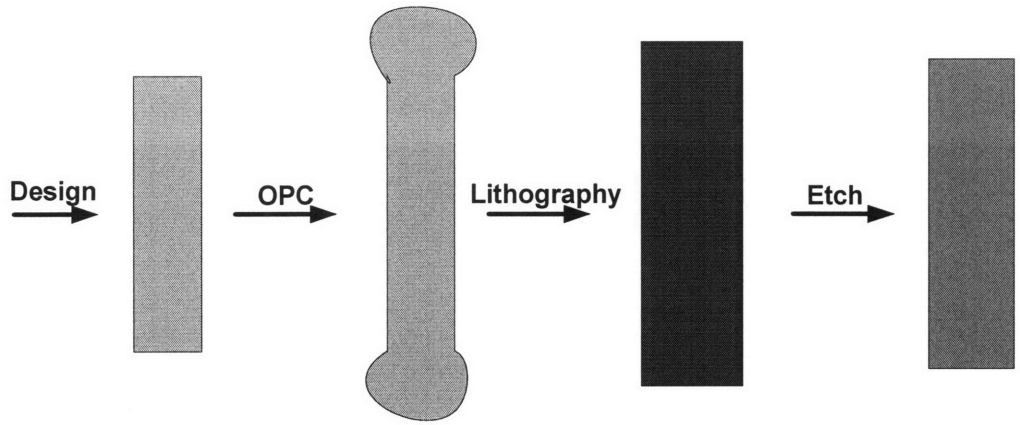

Figure 4-5 – Variations introduced in the OPC, lithography, and etch processes.

In this thesis, we define variation at each process step as including previous variations. Cai et al. have demonstrated how topographic non-uniformity caused by the metal one metallization and CMP process induces topographic variations in the metal two metallization process [20]. We define the variations seen after the etch process as the summation of design, OPC, lithography, and etch variations. Consequently, in order to extract the critical dimension variation that is induced purely by the etch process, we

must be able to subtract the variations added by design, OPC and lithography. By taking measurements after the etch process and subtracting them from measurement taken after the lithographic process, we obtain the change in critical dimension that is purely caused by the etch process.

4.6 Summary

This chapter presented the details of our experiment to characterize non-uniformity in plasma etching of interlayer dielectrics. The experiment showed that the etch process is but one of many sources of variations within the back end of the line processes. The next chapter presents the metrology and characterization of structures on the test wafers.

Chapter 5

Metrology and Characterization

In this chapter the metrology and characterization of our experimental test wafers are presented. We first present the measurement plan and results from measuring the capacitance and line width/space structures described in Chapter 3. We next characterize how parameters of interest such as critical dimension, line space, and depth vary with respect to designed line width, density, and pitch.

The Applied Materials VeritySEM tool is a scanning electron microscope (SEM) that can be used for both overhead and side-angle measurement of structures on a wafer. The SEM tool measures depth, critical dimension (CD), and sidewall profile of microstructures on our test wafers with submicron resolution of small features. Section 5.1 presents the CD measurement plan and result while Section 5.2 presents the depth measurement plan and result. Variational trends seen in the depth measurements are discussed in Section 5.3. Lastly Section 5.4 concludes the chapter.

5.1 Critical Dimension Scanning Electron Microscopy

The SEM tool was used to measure the critical dimension of most of the structures on our test wafers. For the CD measurements, the SEM tool is set at a normal angle to the top of the microstructure in measurement. This normal angle provides a top-down view of each microstructure. The tool, called a CDSEM, measures critical dimension and line space of structures on the wafer using a perpendicular electron beam. The maximum field of view of the VeritySEM tool is four microns and the maximum precision is three angstroms.

5.1.1 CDSEM Measurement Plan

The CDSEM tool can measure features that are smaller than two microns. This field of view limits the measurement plan to structures with line width or line space that are less than two microns (Figure 5-1). Figure 5-1 shows structures in dark gray which have both line width and space that are less than or equal to two microns, while structures in light gray have either their line width or space less than two microns. The structures in dark gray have both their line width and space measured, while the structure in light gray have either their line width or space measured. The total number of structures measured is thirty seven, shown in the measurement map (Figure 5-1).

The measurement map graphs the data points for several pitch and density structures along with constant density structures that are characterized in Section 5.3. The CDSEM tool measures all six wafers that comprise the CD and depth experiments. For each wafer, the tool measures four dies in order to characterize wafer level variations (Figure 5-2). In all of the four dies, the CDSEM tool measures each array structure at nine quadrants shown in Figure 5-2. By measuring at these nine quadrants we can ascertain the influence of neighboring structures on both lithography and etch rate uniformity. Neighboring structures affect each other as because of the pattern density or microloading effect whereby structures near highly loaded areas etch more slowly, due to reactant depletion, than structures neighboring less loaded areas. Chapter 2 gives the theory behind the microloading effect which we use to generate the pattern density model in Chapter 6.

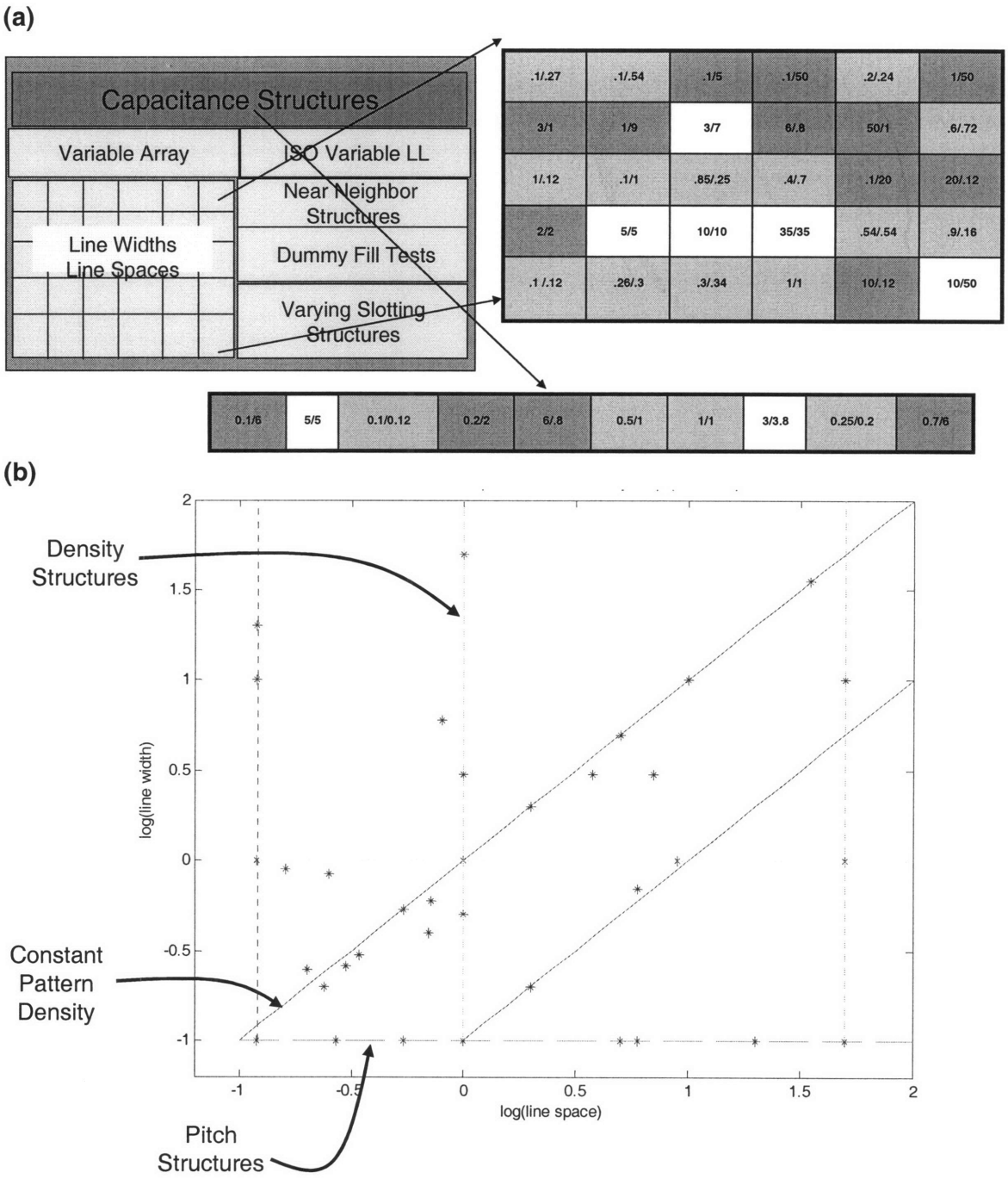

Figure 5-1 – (a) Structures of interest on the test mask. (b) Map of line width and line space of all structures.

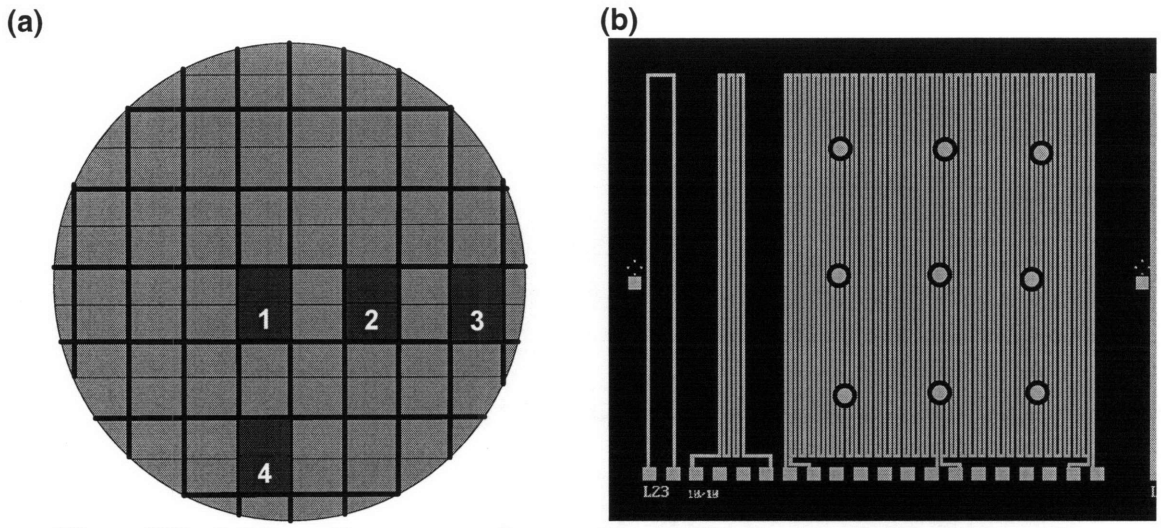

Figure 5-2 – (a) Four dies measured per wafer and (b) nine quadrants measured per structure.

5.1.2 CDSEM Measurement Results

Figure 5-3 shows post-lithographic and etch SEM pictures for the depth experiment. From Figure 5-3, which is a SEM of structure CA3, we can observe that resist edge roughness translates into post-etch roughness. This propagation of variation from one process layer to the next presents a challenge in isolating variations to only include the etch process. Variation propagation is not a significant concern in our etch rate modeling which we present in Chapter 6 and Chapter 7. But as discussed in Chapter 4, variation propagation is important in understanding and modeling CD and profile non-uniformity.

The post-lithographic SEM shows that the trench width is 16 nanometers wider than the designed width of 250 nanometers. We can observe from Figure 5-3 that there is a significant sidewall or whitish area at the edge of the line space. This expanded sidewall is most likely caused by the ion and kinetic neutral flux described in Chapter 2. As described in Chapter 4, overetching in the CD process is used to achieve depth uniformity. As a consequence of this overetching the sidewalls become wider and the width of the

trench bottom is much smaller than the width at the top. The magnitude of the sidewall slope and width is illustrated in Section 5.2.

Furthermore, the SEM shows resist and edge roughness (Figure 5-3). Again, the resist roughness propagates to the post-etch roughness. The side-effect of overetching is that the trench spaces shrink and the width of the trench wall enlargens.

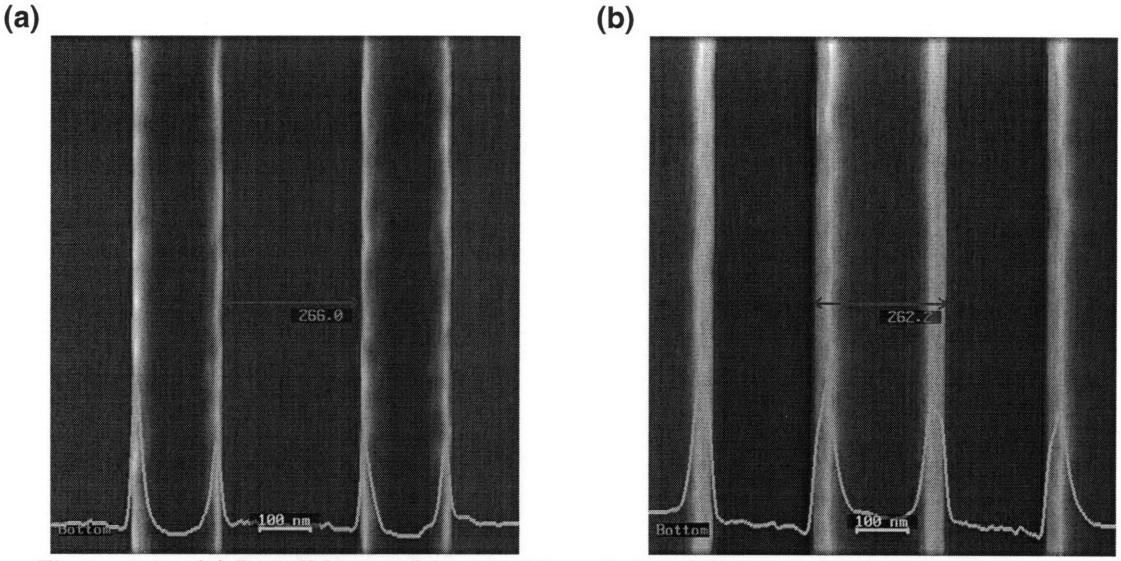

Figure 5-3 – (a) Post lithographic and (b) post etch SEM of capacitance structure, CA3.

Summary statistics for the CDSEM metrology are given in Table 5-1. The table provides critical dimension averages at the top and bottom of each microstructure and measurements for all four dies on the four post-etch wafers. The table shows that the sidewall thickness is a significant part of the overall width of each microstructure. The average sidewall thickness for all feature widths across all dies range from 35.4, 35.1, 39.9, and 38.9 nanometers to 70.7, 56.5, 59.2, and 59.0 nanometers with a standard deviation per feature of 3.6, 3.6, 4.0, and 4.3 nanometers for each post-etch wafer, respectively. As given in Table 5-1, the sidewall is a significant percentage of the line width of many features sizes particularly the 100 nanometer trench width features.

Table 5-1 – Summary statistics for CDSEM measurements.

Structure	CD_TD1	CD_TD2	CD_TD3	CD_TD4	CD_AVG	CD_TSTD	WALL1	WALL2	WALL3	WALL4	WALL_AVG	WALL_STD	pitch	design	density
CA1	155.111	159.833	161.489	161.83	159.567	2.68122	39.578	43.966	54.411	52.866	47.70525	7.1094915	6100	100	0.0164
CA3	694.722	691.211	675.144	687.69	687.192	7.38661	49.478	49.878	54.077	50.489	50.9805	2.1057775	6700	700	0.1045
CA4	117.056	118.867	115.311	114.56	116.447	1.6653	34.5	36.934	38.722	36.5	36.66415	1.7336324	220	100	0.4545
CA6	197.511	197.644	189.5	194.87	194.881	3.29809	42.844	44.5	47.767	46.667	45.4445	2.2017563	2200	200	0.0909
CA9	500.7	498.456	483.811	492.59	493.889	6.52873	48.144	49.1	54.867	49.889	50.5	2.9974848	1500	500	0.3333
CA10	242.211	241.389	232.089	237.92	238.403	3.98486	45.011	46.145	51.033	45.555	46.936	2.7703114	450	250	0.5556
L11	116.289	117.144	113.422	111.49	114.586	2.25787	34.322	34.9	36.455	36.1	35.444325	1.0012953	220	100	0.4545
L12	294.8	297.667	293.356	294.06	294.969	1.63887	58.889	65.256	61.278	62.912	62.08375	2.6835815	560	260	0.4643
L13	330.067	354.267	366.189	365.86	354.094	14.6796	41.756	78.611	79.956	82.512	70.70875	19.369526	640	300	0.4688
L26	843.389	837.344	824.167	825.42	832.581	8.08625	47.8	51.277	53.678	53.855	51.6525	2.8246777	10600	900	0.0849
L31	938.456	936.156	929.722	926.63	932.742	4.76267	51.145	54.589	55.922	57.177	54.70825	2.5999286	1120	1000	0.8929
L32	161.378	163.444	160.778	159.5	161.275	1.42433	46.067	48.255	53.989	53.1	50.35275	3.8095452	1100	100	0.0909
L33	827.111	829.933	818.744	818.69	823.619	5.00332	53.255	51.811	55.177	54.856	53.77475	1.5558343	1100	850	0.7727
L34	402.644	403.689	394.267	395.33	398.983	4.2165	50.2	49.089	53.323	50.522	50.7835	1.8008558	1100	400	0.3636
L35	159.111	160.789	154.278	156.17	157.586	2.52702	45.7	49.667	52.822	52.178	50.09175	3.2287554	20100	100	0.005
L42	995.733	994.167	983.7	982.9	989.125	5.85811	51.566	52.2	56.133	59.233	54.783	3.5891493	10000	1000	0.1
L51	167.578	169.044	164.867	164.7	166.547	1.83947	49.811	51.455	54.9	54.467	52.65825	2.4393758	370	100	0.2703
L52	166.744	167.078	164.067	163.36	165.311	1.62391	48.355	49.045	55.034	52.612	51.2615	3.1313587	640	100	0.1563
L53	160.312	162.089	158.2	158.8	159.85	1.50429	46.562	49.8	54.825	53.367	51.1385	3.7100058	5100	100	0.0196
L54	160.911	162.422	156.6	157.71	159.411	2.35102	47.533	51.844	54.833	53.289	51.87475	3.1412887	50100	100	0.002
L55	198.056	200.6	190.533	196.1	196.322	3.70353	42.078	47.611	48.933	47.767	46.59725	3.0700354	440	200	0.4545
L56	988.889	987.544	973.078	982.98	983.122	6.19924	55.122	55.144	60.345	53.445	56.014	2.9949895	51000	1000	0.0196
CA1	163.111	165.444	161.467	165.16	163.794	1.61714	46.333	48.666	53.956	54.312	50.81675	3.9497427	6100	100	0.0164
CA3	694.6	687.767	673.522	695.08	687.742	8.70414	51.256	54.156	53.322	48.522	51.814	2.5104884	6700	700	0.1045
CA4	118.367	119.167	113.933	116.49	116.989	2.01416	34.834	36.356	37.444	37.433	36.516775	1.2327145	220	100	0.4545
CA6	199.722	197.778	189.4	196.62	195.881	3.9021	42.789	43.522	47.422	45.8	44.88325	2.1232496	2200	200	0.0909
CA9	501.1	508.233	483.122	503.21	498.917	9.4799	51.567	45.255	51.822	47.289	48.98325	3.2406068	1500	500	0.3333
CA10	245.189	239.878	231.522	243.01	239.9	5.19228	44.911	46.311	49.066	45.478	46.4415	1.8417196	450	250	0.5556
L11	116.744	117.967	112.689	112.97	115.092	2.30685	34.011	34.667	35.567	36.489	35.183425	1.0791978	220	100	0.4545
L12	290.2	298.6	285.622	289.47	290.972	4.73467	51.856	64.889	49.955	59.545	56.56125	6.9290716	560	260	0.4643
L13	332.167	330.033	335.311	362.97	340.119	13.3238	41.7	49.377	55.067	77.556	55.925	15.425771	640	300	0.4688
L26	855.856	840.078	825.389	830.68	838	11.5736	46.612	50.067	57.567	52.756	51.7505	4.6217261	10600	900	0.0849
L31	936.611	940.4	928.644	930.56	934.053	4.69875	53.355	52.9	54.988	58.7	54.98575	2.6334614	1120	1000	0.8929
L32	163.144	163.056	160.467	162.66	162.331	1.09176	45.944	46.812	53.767	54.078	50.15025	4.3720534	1100	100	0.0909
L33	829.567	834.833	829.933	819.84	828.544	5.43631	53.423	51.2	50.244	56.855	52.9305	2.9357662	1100	850	0.7727
L34	406.556	409.944	396.4	399.58	403.119	5.38706	48.767	48.411	49.344	49.3	48.9555	0.4478188	1100	400	0.3636
L35	161.367	161.067	153.878	159.72	159.008	3.02617	46.823	49.067	52.189	54.789	50.717	3.4944577	20100	100	0.005
L42	992.322	995.789	983.622	982.96	988.672	5.52612	55.066	54.633	54.489	59.678	55.9665	2.486454	10000	1000	0.1
L51	168.667	168.689	164.978	167.52	167.464	1.51091	49.845	49.378	54.9	55.889	52.503	3.3685404	370	100	0.2703
L52	167.222	166.844	163.789	167.78	166.408	1.54834	47.5	47.611	54.422	55.2	51.18325	4.2012333	640	100	0.1563
L53	161.425	163.056	157.522	160.66	160.665	2.01057	46.637	49.478	54.3	53.256	50.91775	3.5263167	5100	100	0.0196
L54	159.944	160.344	155.578	160.33	159.05	2.01115	45.411	47.844	53.845	53.644	50.186	4.2281451	50100	100	0.002
L55	199	199.089	194.6	196.08	197.192	1.92529	41.9	44.611	52.1	47.356	46.49175	4.3520411	440	200	0.4545
L56	989.789	989.878	976.722	984.12	985.128	5.38407	53.656	53.889	53.033	55.266	53.961	0.9420577	51000	1000	0.0196
CA1	145.689	148.5	147.956	145.38	146.881	1.36534	38.745	41.367	52.645	47.778	45.133725	6.2826206	6100	100	0.0164
CA3	733.833	720.656	722.078	718.26	723.706	6.00472	38.466	39.723	42.689	41.167	40.51125	1.82364	6700	700	0.1045
CA4	113.544	113.067	110.611	110.37	111.897	1.42106	40.711	40.989	47.522	45.667	43.72225	3.4039148	220	100	0.4545
CA6	199.722	206.089	202.789	206.94	203.886	2.86127	40.666	46.122	59.567	54.188	50.13575	8.389588	2200	200	0.0909
CA9	520.067	558.178	518.067	543.93	535.061	16.7835	39.034	41.889	44.623	43.344	42.2225	2.4012439	1500	500	0.3333
CA10	258.867	259.211	258.111	258.63	258.706	0.400039	51.423	57.111	64.922	61.944	58.85	5.9055474	450	250	0.5556
L11	112.178	113.078	111.822	114.03	112.778	0.857249	39.878	40.445	42.089	38.2	40.152775	1.6044759	220	100	0.4545
L12	267.711	271.578	293.9	292.4	281.397	11.8439	54.944	54.222	59.167	57.622	56.48875	2.3080791	560	260	0.4643
L13	354.233	347.589	340.822	338.02	345.167	6.28468	41.255	42.611	49.478	46.844	45.047	3.7936935	640	300	0.4688
L26	915.567	886.656	865.811	876.62	886.164	18.5071	38.578	41.312	44.1	43.778	41.942	2.5652327	10600	900	0.0849
L31	975.733	976.267	967.111	957.38	969.122	7.69296	40.555	40.489	44.289	43.789	42.2805	2.040953	1120	1000	0.8929
L32	152.567	152.389	150.633	148.76	151.086	1.54319	44.445	44.733	55.066	53.289	49.3834	5.5846642	1100	100	0.0909
L33	879.4	872.967	856.967	859.76	867.272	9.24952	40.878	41.8	45.223	44.278	43.04475	2.0420485	1100	850	0.7727
L34	450.478	445.222	424.144	435	438.711	10.0848	40.311	41.544	48.022	44.244	43.53025	3.4153583	1100	400	0.3636
L35	141.1	141.478	141.778	139.18	140.883	1.01357	39.5	41.478	52.911	48.756	45.661275	6.2609916	20100	100	0.005
L42	1016.04	1022.03	1003.54	1000.8	1010.59	8.76283	36.669	37.741	43.318	42.15	39.9695	3.2571227	10000	1000	0.1
L51	159.789	160.211	156.822	155.57	158.097	1.95957	51.889	52.389	60.522	58.823	55.90565	4.409066	370	100	0.2703
L52	157.678	158.344	156.433	155.06	156.878	1.2559	45.645	47.011	57.244	54.934	51.208525	5.7410613	640	100	0.1563
L53	144.322	144.722	142.211	141.43	143.172	1.38496	41.511	43.478	52.6	49.855	46.861025	5.2270896	5100	100	0.0196
L54	142.7	140.678	140.556	138.71	140.661	1.41165	40.267	41.378	52.767	48.055	45.616875	5.8782465	50100	100	0.002
L55	208.956	208.244	203.9	205.58	206.669	2.03522	54.056	55.744	64.867	62.222	59.22225	5.1526713	440	200	0.4545
L56	1008.26	1026.62	993.533	1015.9	1011.08	12.0506	36.971	38.809	42.7	41.987	40.11675	2.6942512	51000	1000	0.0196
CA1	147.911	149.233	146.522	146.89	147.639	1.05188	39.944	43.066	53.333	48.622	46.24135	5.935804	6100	100	0.0164
CA3	738.2	718.733	700.975	732.48	722.597	14.3485	39.522	40.855	46.7	42.278	42.33875	3.1176801	6700	700	0.1045
CA4	114.356	113.022	108.756	111.62	111.939	2.07652	40.823	41.333	47.2	45.366	43.68065	3.1042585	220	100	0.4545
CA6	198.044	200	197.622	202.59	199.564	1.96339	39.866	44.344	60.889	52.289	49.347	9.2518917	2200	200	0.0909
CA9	520.8	542.778	505.511	537.96	526.761	14.7389	39.489	42.067	45.144	43.767	42.61675	2.435509	1500	500	0.3333
CA10	256.522	261.022	253.556	261.74	258.211	3.35087	48.978	58.689	65.678	62.277	58.9055	7.2073087	450	250	0.5556
L11	112.667	112.944	113.378	114.49	113.369	0.694217	39.7	40.077	37.978	37.867	38.9056	1.1465857	220	100	0.4545
L12	267.8	275.967	294.211	282.89	280.217	9.68532	55.867	55.178	60.6	59.289	57.7335	2.6236619	560	260	0.4643
L13	353.067	341.333	334.711	344.93	343.511	6.62409	40.623	42.044	54.644	48.155	46.3665	6.4132035	640	300	0.4688
L26	899.689	875.5	859.656	860.44	873.822	16.2139	41.056	41.744	45.145	44.788	43.18325	2.0832922	10600	900	0.0849
L31	975.778	975.111	955.8	956.4	965.772	9.67742	41.367	41.222	43.667	44.033	42.57225	1.4841463	1120	1000	0.8929
L32	154.133	153.344	149.189	149.62	151.572	2.18991	44.444	45.844	55.645	53.711	49.910875	5.589931	1100	100	0.0909
L33	860.922	866.411	849.556	855.22	858.028	6.29102	40.711	41.744	46.423	45.022	43.475	2.690723	1100	850	0.7727
L34	432.156	436.833	420.811	422.44	428.061	6.66757	39.689	41.433	48.555	44.688	43.59125	3.9041547	1100	400	0.3636
L35	143	141.833	139.967	141.14	141.486	1.09976	39.411	41.511	53.189	49.977	46.022125	6.6097805	20100	100	0.005
L42	1009.47	1024.4	999.4	1005.6	1009.72	9.2047	37.453	38.167	44.383	42.253	40.564	3.3096532	10000	1000	0.1
L51	161.811	160.8	155.622	157.14	158.844	2.54451	52.522	52.756	60.711	59.733	56.43045	4.3971958	370	100	0.2703
L52	159.922	159.044	154.533	156.86	157.589	2.0879	46.455	47.944	57.4	55.712	51.877675	5.4794772	640	100	0.1563
L53	146.456	145.356	140.767	142.94	143.881	2.20107	42.778	44.389	53.911	50.9	47.9945	5.2808085	5100	100	0.0196
L54	145.167	142.367	138.644	140.49	141.667	2.41148	41.956	43.145	53.355	49.778	47.05845	5.428163	50100	100	0.002
L55	207.7	207.9	202.922	207.94	206.617	2.13497	51.944	55.789	65.744	62.833	59.0775	6.3310625	440	200	0.4545
L56	1012.96	1035.17	1010.26	1015.4	1018.44	9.82455	37.06	40.414	43.227	42.7	40.85025	2.8063514	51000	1000	0.0196

5.2 Profile Scanning Electron Microscope

We used the Applied Materials VeritySEM to measure trench depth and sidewall angle. The VeritySEM tool is configured to scan the surface of a trench with the angle of incidence of the electron beam tilted by fifteen degrees from the normal axis (Figure 5-4). Each measurement scan was made on a side wall surface (Figure 5-4). The depth corresponds to the distance from the top to the bottom of the sidewall and does not refer to the bottom center of the trench. Also, the slope of the sidewall is measured in degrees from the horizontal plane.

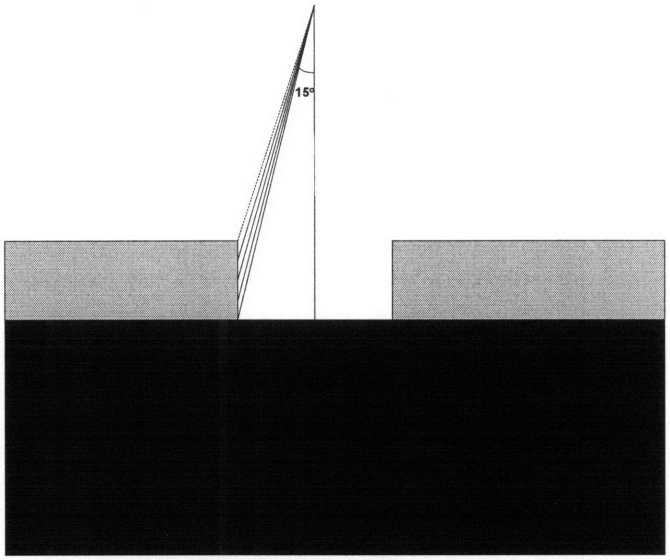

Figure 5-4 – Setup of VeritySEM tool for profile measurements.

The VeritySEM tool first tilts its electron beam at a high angle of 15 degrees from the normal axis, to scan a user specified area of the trench shown as the red box at the top left of Figure 5-5. Then the tool uses signal processing detection software to identify the top, bottom, wall, and edge boundaries of the trench sidewall as shown in the middle of Figure 5-5. Next, the feature match software identifies the top and bottom of the trench, and measures the trench depth while profiling the sidewall. Finally, the tool tilts its

electron beam back to the normal angle position, and scans the same user specified area of the trench shown as the red box at the top right of Figure 5-5. Using the signal processing and feature match software the tool measures the width of the trench sidewall as shown in the bottom of Figure 5-5.

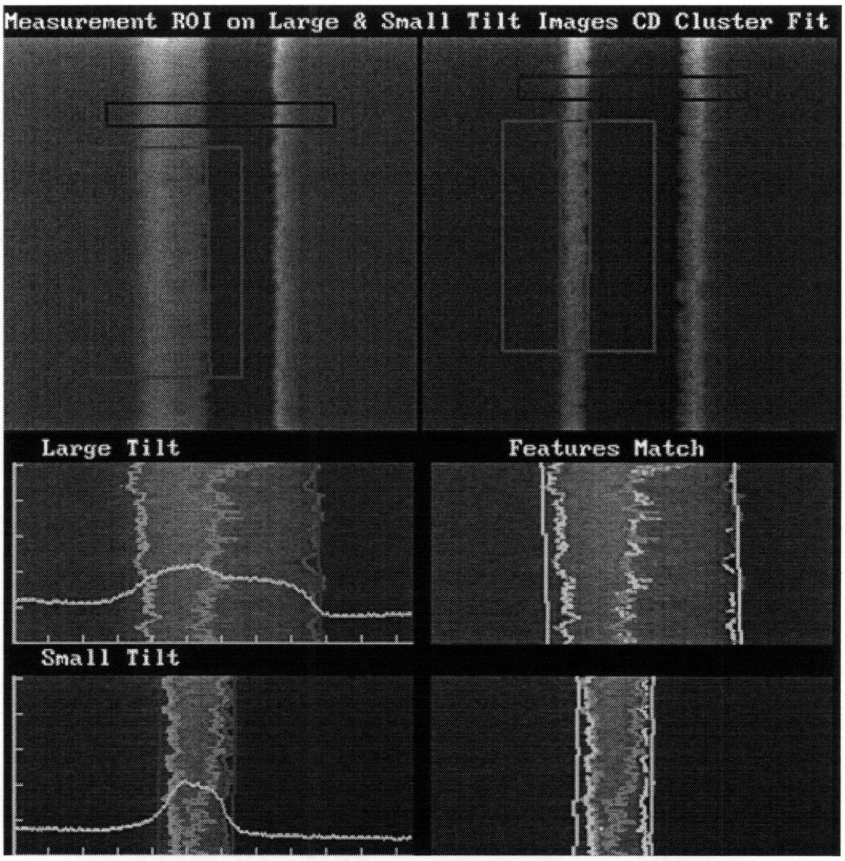

Figure 5-5 – Measurement process of VeritySEM tool.

5.2.1 Measurement Plan

The measurement plan shows the 33 microstructures on four dies that are measured for each of the two wafers from the depth experiments (Figure 5-6). These 33 structures overlap with most of the line width measurements described in Section 5.1 and are used in the feature level modeling described in Chapter 7. Figure 5-7 shows the locations of the four dies on both wafers and the measurement points at three locations across each microstructure. By measuring multiple locations across each structure, we are again able

to quantify the effect of neighboring interaction on depth uniformity as described in Chapter 6.

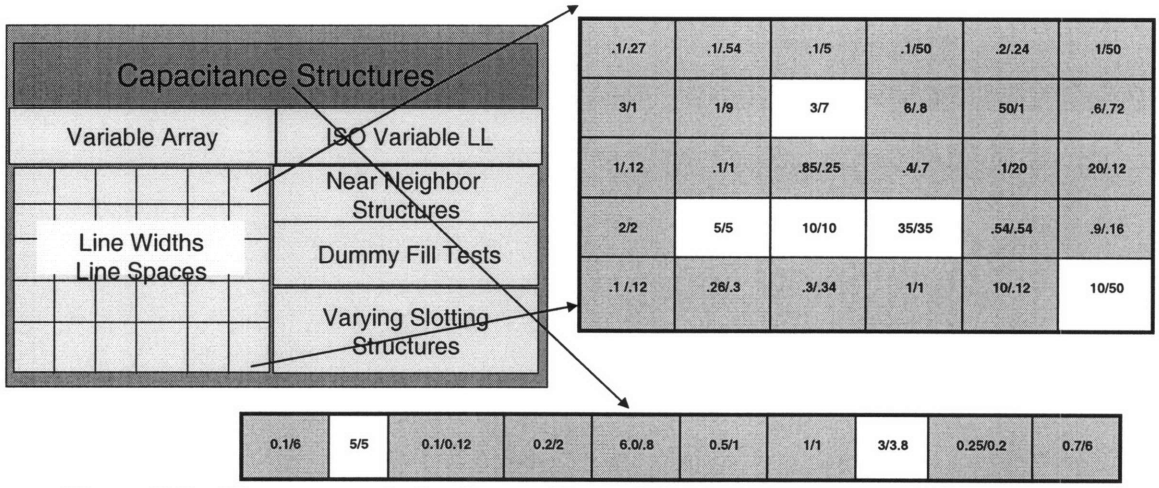

Figure 5-6 – Measurement plan for profile and depth measurements of structures.

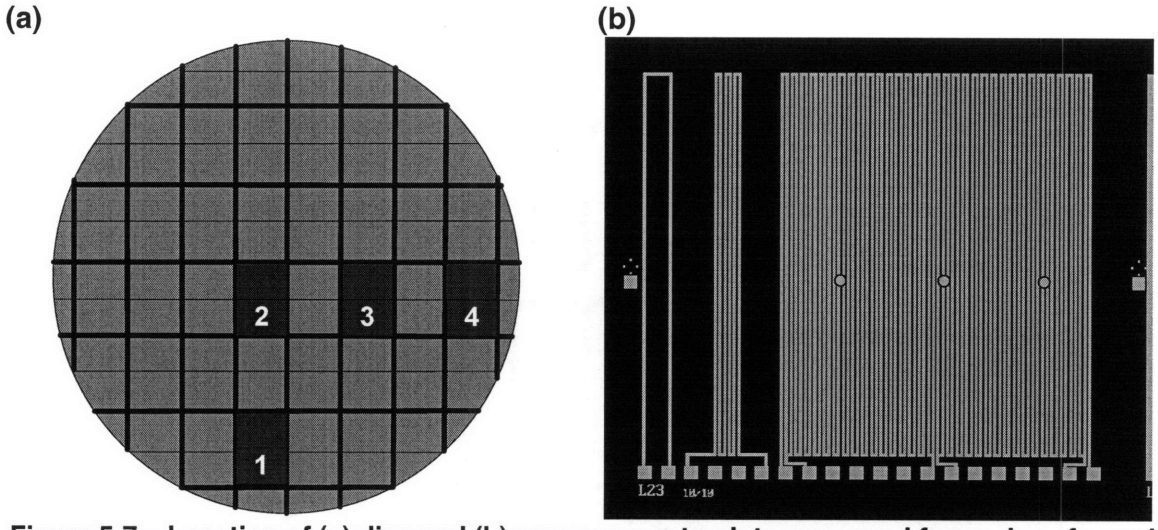

Figure 5-7 – Location of (a) dies and (b) measurement points measured for each wafer and structure, respectively.

5.2.2 Measurement Results

In Chapter 2 we discuss the causes and effects of non-uniformity in etch rate and profile. Specifically, we categorize the causes and effects into three groups that are caused by the interaction of the plasma species with the patterns on the wafer. Our experimental result lends support to our hypothesis that depletion of chemical etch and

inhibitor reactants along with ion and neutral flux has direct effect on overall etch profile. The profile measurements show faceting, line edge roughness, and sloped sidewalls. These results suggest that the influence of etch species on uniformity is largely based on gas phase transport of ions and neutrals.

The first effect, as observed in Figure 5-8, is line edge and sidewall roughness. This effect also lends support to our hypothesis that smaller line widths have rougher line edge and sidewall profile than larger line widths because of the variability in reactant transport within the two different sized trenches.

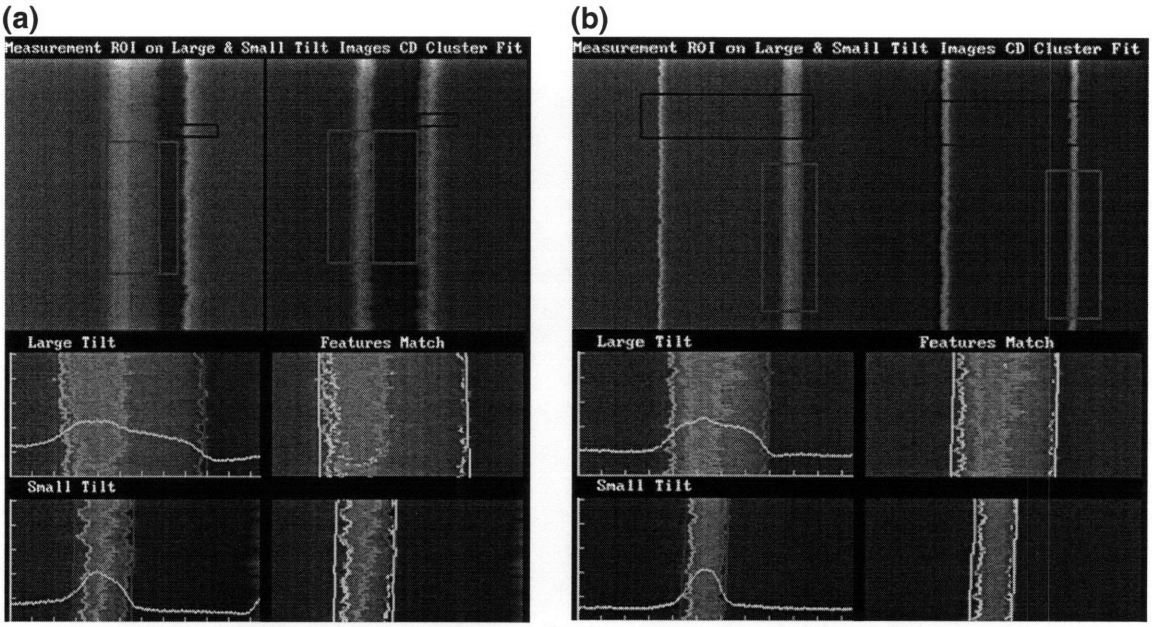

Figure 5-8 – Profile measurement results for (a) 0.1 μm and (b) 6 μm capacitance structures showing line and edge roughness.

Moreover, Figures 5-9 and 5-10 show different degrees of faceting and slopping of sidewalls for two trenches profiles: two capacitance structures with 0.1 μm and 6 μm trench widths, respectively. We again hypothesis that the faceting and slopped sidewalls seen in the trench profiles result from the reactant transport within each trench feature. Both figures show the sidewall profile to be sloped at a roughly eighty degree angle. The

width of the 0.1 μm structure's sidewall represents a larger fraction of its line width than the faction of the line width that is taken up by the sidewall width of the 6 μm structure (Figures 5-9 and 5-10). For small line widths such as the 0.1 micron structure the average sidewall width is 40 nanometers as shown in Figure 5-9. The average sidewall width of large line widths such as the 6 micron structure is 50 nanometers as shown in Figure 5-10. For the 0.1 micron structure, a 40 percent decrease in width from the top of the trench to the bottom will affect reactant transport within the trench. This effect on reactant is less severe for the 6 micron structure which has a 0.17 percent decrease in width.

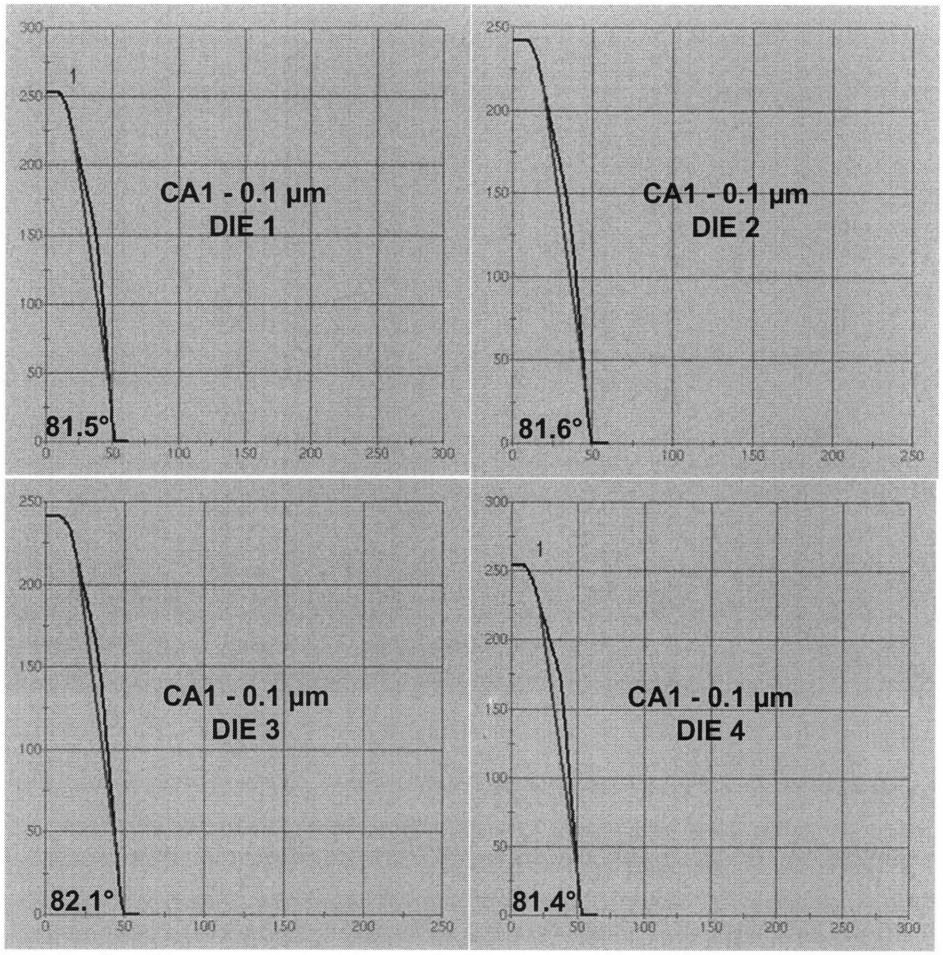

Figure 5-9 – Profile measurement results for 0.1 μm capacitance structure showing faceting and slopped sidewall.

Furthermore, faceting is more severe for smaller line width structures than for larger line width structures. Figure 5-9 shows a 0.1 micron structure that has more faceting than the 6 micron structure shown in Figure 5-10. Also, for both features, faceting and sloping of the sidewalls vary from the inner dies to the outer dies. Figures 5-9 and 5-10 show the profiles of dies 1 through 4 corresponding to Figure 5-7. There is both variation in faceting and sloping within structures and across dies.

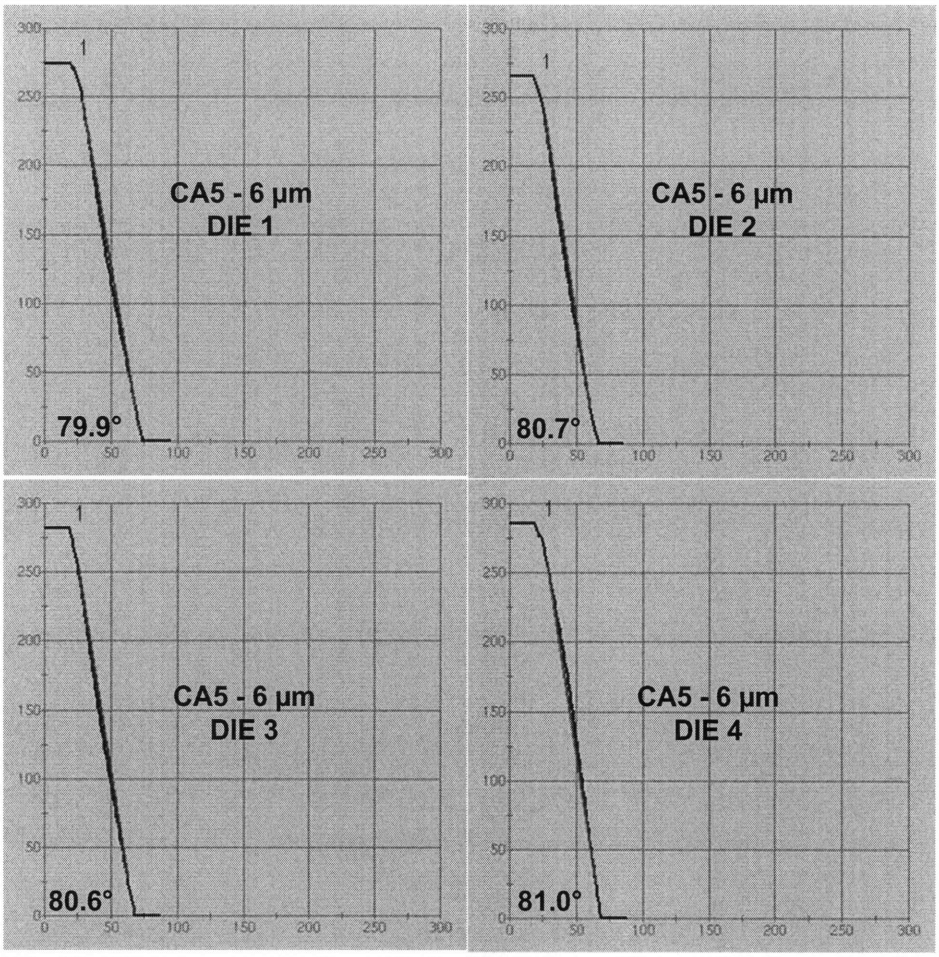

Figure 5-10 – Profile measurement results for 6 μm capacitance structure showing faceting and slopped sidwall.

5.3 Depth Trends

In this section we characterize the variation of our experimental depth data with design parameters such as pitch, line width, and density. We also use an analysis of

variance (ANOVA) decomposition of depth variations to characterize die and feature specific contributions to variations in depth.

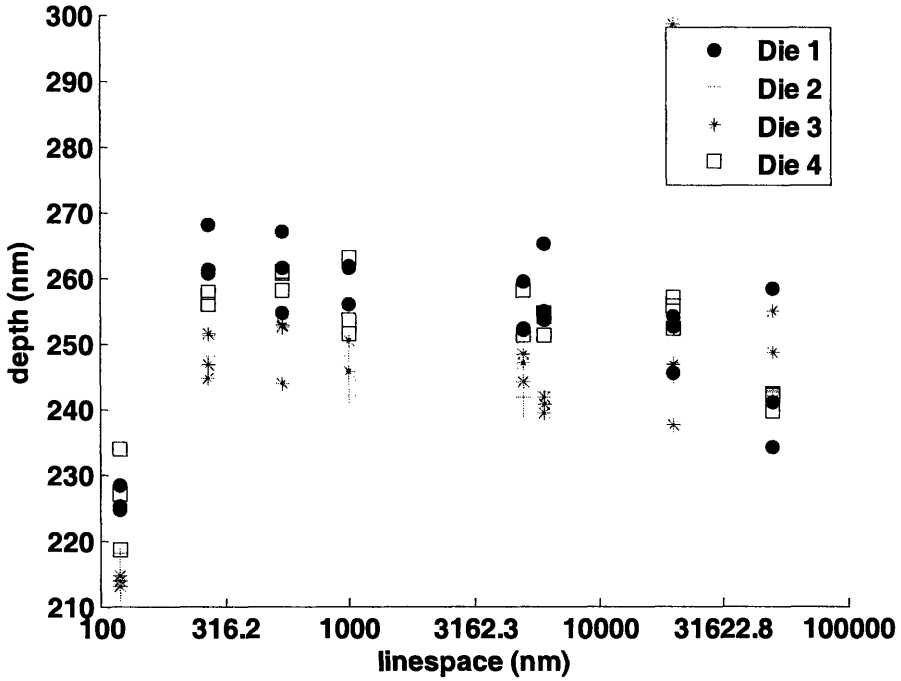

Figure 5-11 – Measured depth for fixed line width of 0.1 μm.

5.3.1 Depth Trends

We observe from Figures 5-11, 5-12, 5-13, and 5-14 that the measured depth varies non-uniformly with parameters such as pitch, design width, and density. First, Figure 5-11 shows that for a fixed line width of 0.1 microns, there is an increase in etch rate for increasing line space (or pitch) followed by a decrease in etch rate for larger pitches. This effect is consistent across all four measured dies shown in Figure 5-7. The two center dies have reduced etch rates when compared to the two outer dies. This difference in etch rate follows our hypothesis that competition for reagents is more severe at the center of the wafer than at the outer edges and that the increase in competition for reactants leads to reduced etch rates.

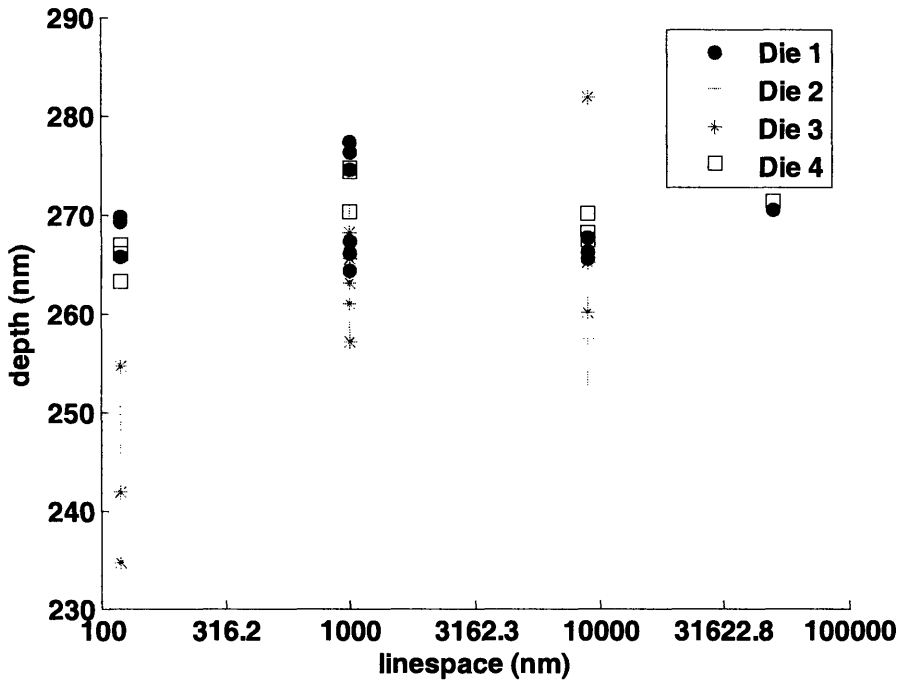

Figure 5-12 – Measured depth for a fixed line width of 1 μm.

Similarly, we observe the same phenomena when the feature line width is 1 micron as seen in Figure 5-12. There is an initial increase in depth followed by a gradual decrease as the line space (or pitch) increases. Additionally, the center dies have reduced etch rates than the outer dies due to the aforementioned competition for reagents at the center of the wafer.

Figure 5-13 shows the effect of both pattern density and ARDE on etch rates, explained in Chapter 2 and modeled in Chapter 6 and Chapter 7. We observe that for a fixed line space of 1 micron, depth initially increases for increasing line width, but then decreases for very large line width. This is because initially, with increasing line width, there is a decrease in aspect ratio that increases the etch rate and counteracts the effect of increasing pattern density which slows etch rate. But with very large line width, the decrease in etch rate caused by increasing pattern density overwhelms the increase in etch

rate due to decreasing aspect ratio. Again, we observe that the center dies etch slower than the outer dies. We will further explore and model the relationship between and coupling of pattern density and aspect ratio in Chapter 8.

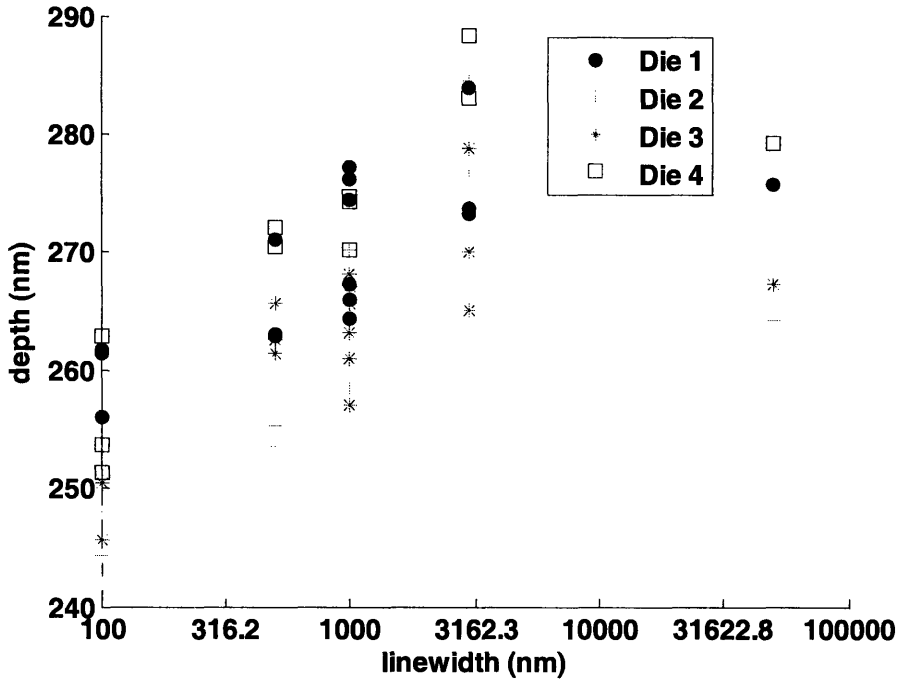

Figure 5-13 – Measured depth for a fixed line space of 1 μm.

Figure 5-14 shows the effect of density on etch rate for a fixed pitch between 1 and 1.2 microns. We observe two simultaneous effects occurring. With fixed pitch, density increases with increasing line width. But increasing line width decreases aspect ratio and increases etch rates. This explains why there is an initial increase in depth for increasing density. As density further increases and dominates the aspect ratio effect, we observe that the etch rate decreases.

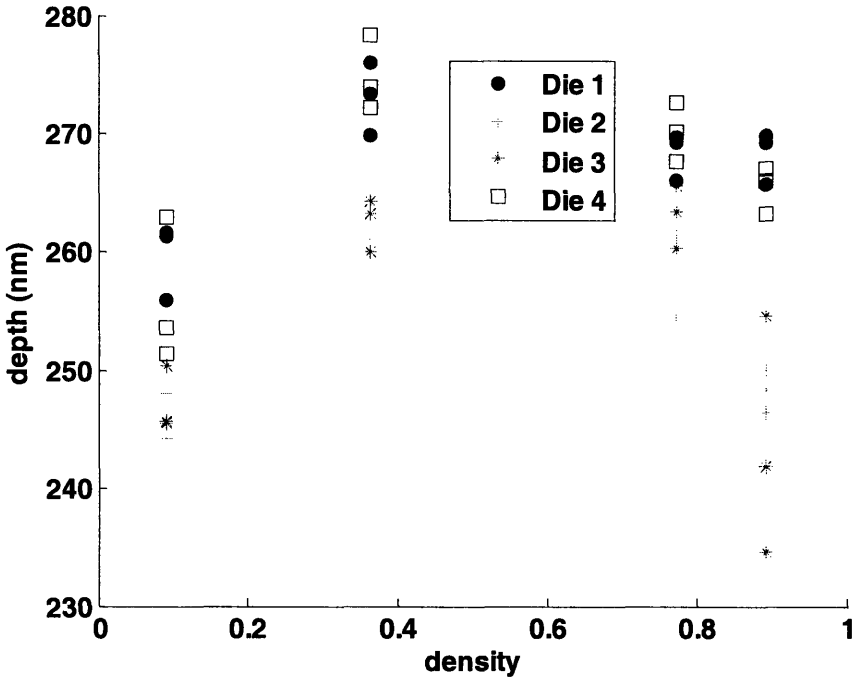

Figure 5-14 – Measured depth for a fixed pitch between 1 and 1.2 μm.

5.3.2 Analysis of Variance

We use an analysis of variance (ANOVA) computation to show the percentage of variations that can be attributed to feature, die, and wafer levels described in Chapter 2. First we group our depth measurements by the individual microstructures measured in accordance with the measurement plan (Figure 5-6). There are 33 groupings corresponding to the 33 microstructures and each microstructure is measured three times (Figure 5-7) on four dies giving a total of 396 data points for the ANOVA analysis. The ANOVA analysis compares the means of the 33 groupings of our depth measurements and returns a p-value for the null-hypothesis that the means of the groupings are equal. Figure 5-15 graphs the means and one-standard deviation bars for each grouping. We observe that the null-hypothesis (no difference in means) is false because the means of

each grouping, while are around the targeted 260 nm depth, deviate by significant amounts compared to the within group standard deviation.

Next, we perform the same ANOVA analysis with our measurement data grouped by the die in which the microstructure was measured. The data is grouped into four dies with a total of 396 data points. Figure 5-7 shows the spatial location of the dies groupings. The ANOVA analysis compares the means of the 4 groupings of our depth measurements and returns a p-value for the null-hypothesis that the means of the groupings are equal. Figure 5-16 graphs the means and one-standard deviation bars for each grouping. We observe that the means of the dies are not equal. In fact, the two center dies have a slower etch rate than the two outer dies, which confirms our observation in the previous section, where the depth trends show that the center dies etch slower than the outer dies. There is also considerable variation in the standard deviation in our die groupings.

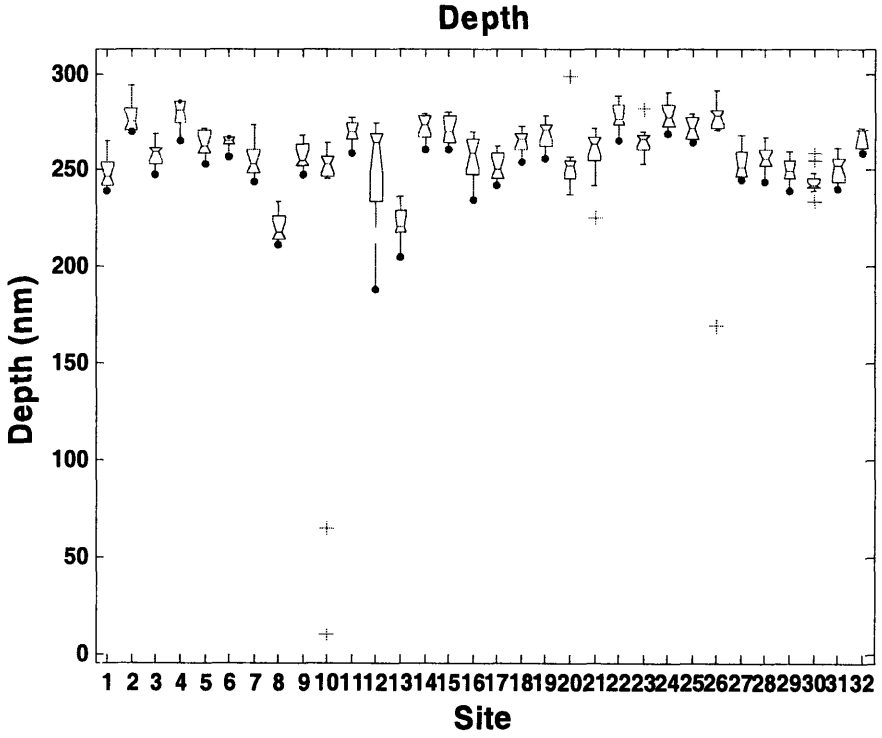

Figure 5-15 – Mean and one standard deviation depth grouped by feature.

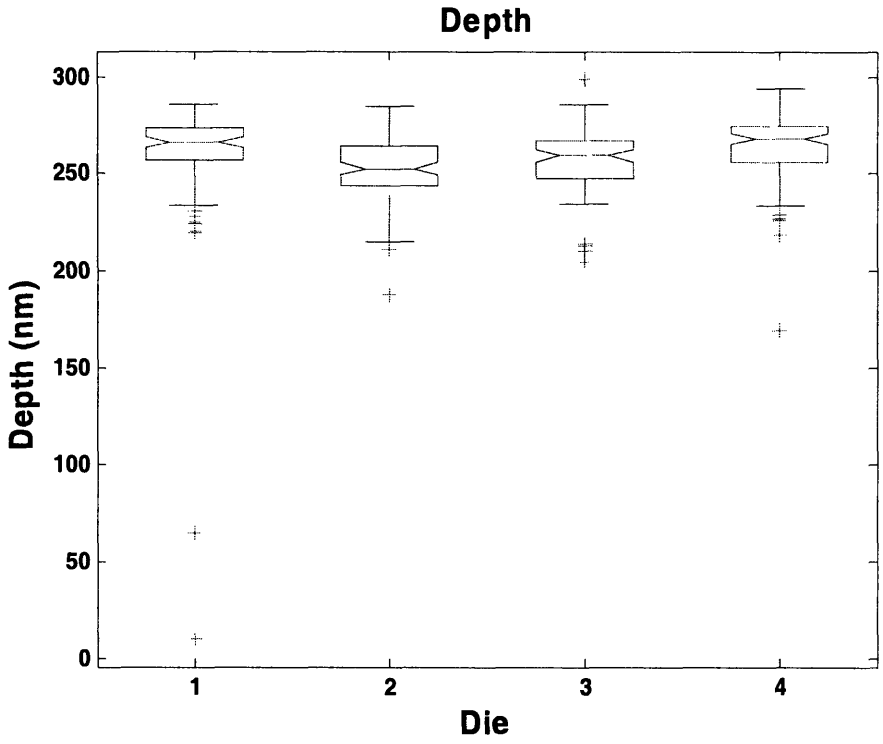

Figure 5-16 – Mean and one standard deviation depth grouped by die.

Lastly, we perform a two-way ANOVA analysis with two sets of groupings according to our feature and die groups. The ANOVA analysis returns the sum of squares (SS) for the main fixed effects of each grouping variable (i.e. feature and die) along with the sum of squares for the combined variables (i.e. model). We also obtain the degree of freedom (df) and f-statistic, which gives the statistical significance of all our variables. With both the sum of squares and degrees of freedom, we are able to calculate the percentage of the observed variations in our depth measurements that can be accounted for by our variables. We find that all our variables are significant and that the model variable accounts for 45.9 percent of the observed variations. The feature and die variables account for 42 and 3.7 percent of the observed variation, respectively. The feature variation encompasses both ARDE and pattern density effects. Die variation is primarily caused by macroloading or wafer level effects. The model variable combines the feature and die variations and thus

represents ARDE, pattern density, and macroloading effects. Table 5-2 lists the results from the ANOVA analysis.

Table 5-2 – ANOVA analysis results.

Total Analysis of Variance for Depth and Critical Dimension
Depth Wafer 22 Only

Source	SS	df	MS	F	Prob>F	% of Variations
MODEL	95152.9894	34	2798.61734	8.01	0	45.91237939
SITE	88019.265	31	2839.33113	8.13	0	42.16097382
DIE	7831.79161	3	2610.5972	7.48	0	3.75140557
ERROR	112096.103	321	349.209043			54.0876208
TOTAL	207249.092	355	583.80026			100.0000002

5.4 Summary

This chapter present the metrology and characterization of our etch experiment. The metrology consists of the CDSEM tool to measure both CD and depth of features on our chip. The data set for our etch modeling in Chapter 6, Chapter 7 and Chapter 8 is composed of the depth data set for etched feature depth. The observed profile and depth trends, along with an ANOVA analysis, match our qualitative understanding of the effect of reactant gas and pattern features on overall depth variations. In the next chapter, we develop a quantitative predictive model relating etch depth to only pattern density.

Chapter 6

A Pattern Density Based Etch Prediction Model

We present a quantitative model capturing plasma etch pattern density effects for integrated circuits. This layout pattern density model expands and extends the concepts of pattern density as a model for microloading. We see that this model captures key effects and trends in the observed etch data. However, we also find that pattern density alone is insufficient for good etch prediction. This leads us to a feature only model presented in Chapter 7. However, although the feature only model capture key effects such as ARDE, it is also not able to capture all etch variations and is insufficient for good etch prediction. As we will see in Chapter 8, by coupling the feature and pattern density models, an effective methodology for modeling pattern dependent etch variations is achieved.

This chapter introduces new concepts in modeling reactant consumption: an effective pattern density using a three dimensional filter is used to model reactant concentration gradient. We present etch rate as a mathematical function of effective pattern density. We use data from our experimental test mask, TI-Praesagus-x1916, to calibrate and demonstrate the model. A comparison between the model and the experimental data is presented for various parameters. Finally, limitations in the current model and directions for future work are summarized.

6.1 Description of Model

Our methodology for modeling microloading in the ILD etch process uses pattern density as the parameter of variation. We define pattern density as the fraction of exposed surface on a wafer that is not blocked by etch mask. This definition of pattern density has a direct relationship with microloading because they both represent how the open area in

an etch process leads to variations in reactant species consumption. Pattern density is proposed as the basis for approximation of microloading effects. Microloading depends upon the amount of exposed area, while pattern density represents the amount of exposed area as a fraction of total area. Thus we model how design or layout specific variations across a chip or wafer result in pattern density variations; these in turn lead to etch rate and depth variations due to microloading across a chip or wafer.

We model a unit of pattern density as causing a depletion or perturbation of reactant species. This implies that reactant concentration has an impulse response-like behavior to a unit of pattern density in its localized area. Our etch model convolves an etch "impulse response" with a local pattern density map for any device layout in order to predict the perturbations or depressions of reactant species due to that device design. Using this convolved etch mask, which we term "effective pattern density," we model etch rate and depth variations assuming a mathematical function with effective pattern density as the independent variable. Within die and between die pattern density based interactions are captured.

A pictorial schematic of the components and approach of our model is illustrated in Figure 6-1. Our model has three components: a wafer level model, a die level (pattern density) based model, and a feature level (aspect ratio) based model. We believe that there is a coupling of wafer level, die level, and feature level non-uniformity in a manner that is non-linear and non-additive. This chapter develops the die level model. Chapter 7 focuses on the feature level model while Chapter 8 presents the integration of the die and feature level models. The wafer level model is left for discussion and future work in the summary chapter (Chapter 9).

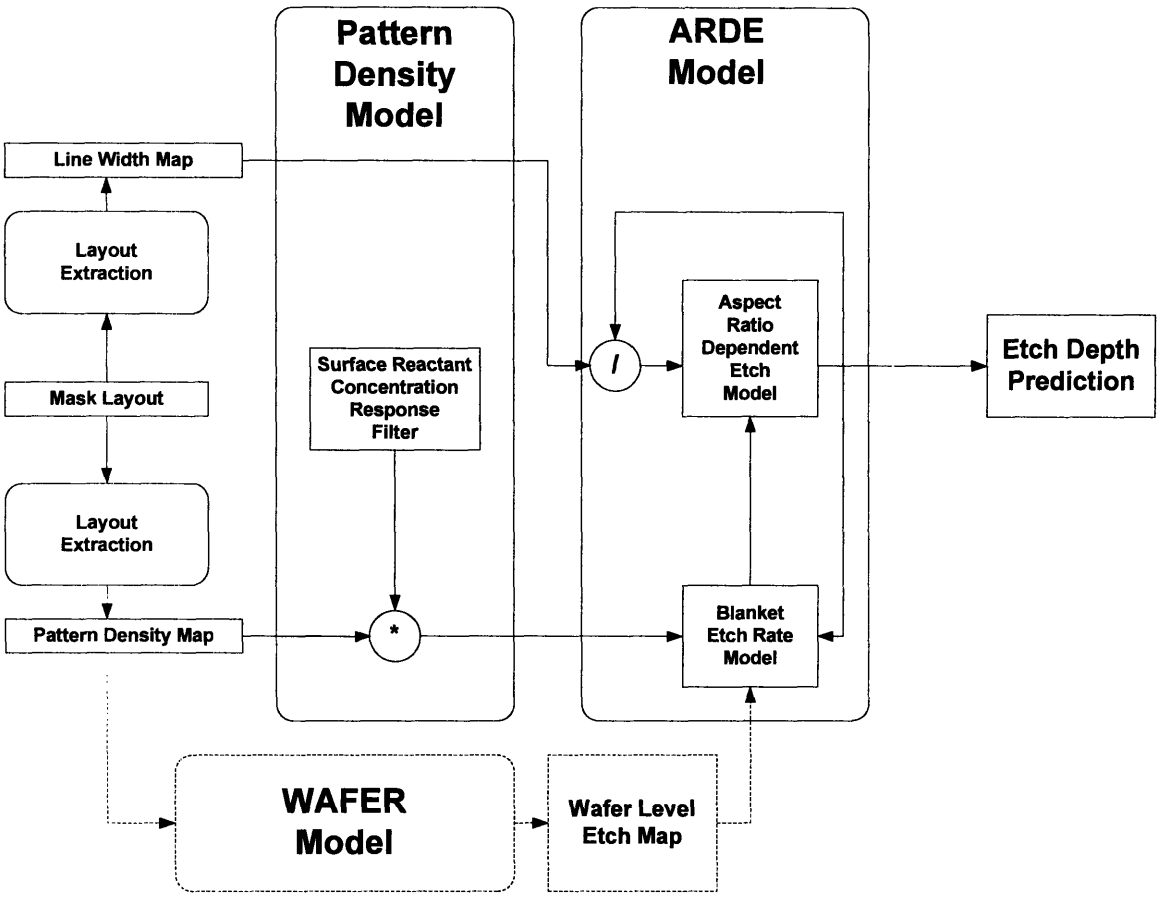

Figure 6-1 – Overall plasma etch model architecture.

6.2 Pattern Density Model

The physical rationale behind the pattern density model is described next. Then the model derivation and implementation is presented. The sources of etch non-uniformity result from both the design and operational settings of the etch chamber and the pattern structures being etched into the wafer.

6.2.1 Physical Motivation for Pattern Density Effect

Plasma etching involves the interaction of two chemical and physical mechanisms. The first mechanism is ion bombardment to activate the surface of the wafer by removing the inhibitor layer and to impart energy onto adsorbed species thereby accelerating surface reactions [19]. The second mechanism is the chemical reaction of adsorbed

species with the wafer surface [19]. During the etch process, we assume that the limiting factor is the availability of chemical species that react with the wafer surface. This is a simplification of the plasma etch process as described in Chapter 2, where the etch process is a synergistic interaction between ions and neutral chemical species leading to accelerated anisotropic etching. Representative etch reactions include the following:

$$CF_4 + e^- \rightarrow CF_3 + F + e^- \quad (6\text{-}1)$$

$$CF_4 + e^- \rightarrow CF_4^* + e^- \quad (6\text{-}2)$$

$$CF_4 + e^- \rightarrow CF_3^+ + F + 2e^- \quad (6\text{-}3)$$

$$CF_3 + e^- \rightarrow CF_3^+ + 2e^- \quad (6\text{-}4)$$

$$SiO_2\,(s) + 4F\,(g) \rightarrow SiF_4\,(g) + O_2\,(g) \quad (6\text{-}5)$$

$$SiO_2\,(s) + CF_x^*\,(g) \rightarrow SiF_4\,(g) + CO\,(g) \quad (6\text{-}6)$$

Equations 6-1, 6-2, 6-3, and 6-4 represent the dissociation, excitation, dissociative ionization, and ionization of carbon tetraflouride (CF_4) into reactive neutral fluorine and flourocarbon free radicals (F, CF_3) and ions [19]. The fluorine and fluorocarbon radicals diffuse onto the wafer surface where they etch away the dielectric. Our base assumption is that the localized variation in concentration of the free radicals creates spatial variations in etch rates. Pattern density dependencies result from localized consumption differences of free radical reactants across the wafer where different locations have different open area. Depressions in concentration result from areas of high density which act as sinks for reactant concentration. Thus pattern density dependencies provide both a qualitative and quantitative measure of microloading, where features and dies that are surrounded by highly loaded areas will etch more slowly because they encounter more competition for reactants. We note that some etch processes might be limited by removal

of product species rather than supply of reactants; a similar model development is possible in these cases.

6.2.2 Effective Pattern Density

We model die level interactions using an etch impulse response filter in a methodology similar to that used by Hill et al. [13]. This idea is analogous to a filter-based inter-layer dielectric (ILD) thickness prediction scheme for CMP described by Ouma et al. [21]. If *f[x,y]* represents the spatial response to an impulse of pattern density, and *d[x,y]* is a function describing the local spatial pattern density of a layout, then the die-level variation *z[x,y]* is given by a convolution operation [13]:

$$z[x,y] = f[x,y] \otimes d[x,y] \tag{6-7}$$

The etch impulse response filter is based on a diffusion equation with inverse distance ($1/r$) dependence for a spherical coordinate system [13]. A mathematical expression for the filter function is given by the reduction of reactant concentration at a radius, r, from an arbitrarily loaded point on the wafer surface as described below.

6.2.3 Filter Description

The filter represents the effect of a unit of loading on surrounding etchant concentration. We arrive at the mathematical representation of the filter by solving for the diffusion equation (Equation 6-8). Equation 6-8 is the diffusion equation in spherical coordinates and represents a constant reaction rate at the surface of a wafer as a function of the diffusion coefficient and the change in reactant concentration with respect to distance. We consider diffusion in the hemisphere above the wafer and assume that the reactants diffuse isotropically. An expression for the concentration of reactants at an etching site (Equation 6-9) is obtained by integrating Equation 6-8 and rearranging terms.

Figure 6-2 illustrates the diffusion assumptions we use in our model. First, we assume that there is a constant supply of reactants, ($C=C_o$), being generated from the plasma source above the wafer. This creates a constant concentration of reactants at the boundary of the hemispherical sheath. Second, the concentration of reactants at the surface of an open area site (i.e unit of pattern density) is zero ($C=0$). Reactants adsorbing to the open surface area are used to etch away the oxide. Third, the concentration of reactants, $C(r)$, and the flux of reactants, $V(r)$, through a hemisphere r distance away from the open area is a function of the distance.

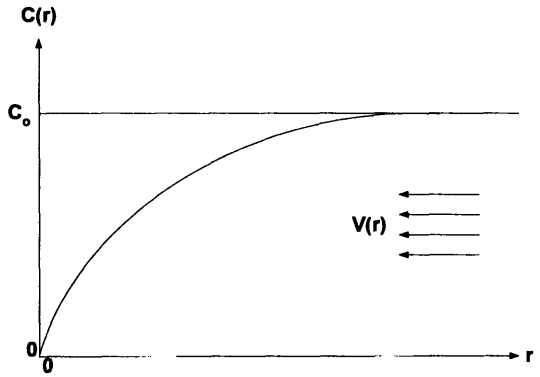

Figure 6-2 – Reactant concentration as a function of distance from etching feature.

$$2\pi r^2 D\frac{\partial C}{\partial r} = \Phi \tag{6-8}$$

$$C = C_o - \frac{\Phi}{D}\frac{1}{2\pi r} \tag{6-9}$$

In Equation 6-9, there are two important parameters: the reaction rate Φ and the diffusion coefficient D, which represent the consumption rate of oxide and transport rate of etchant to the wafer surface, respectively [13]. Equation 6-9 gives the negative impact on background reactant concentration as a function of distance away from each area of exposed oxide, consistent with a pattern density (loading) effect. The initial concentration, C_o, is depressed as a function of radial distance, r. The further the distance, r, from the

etching feature, the less depressed is the initial reactant concentration. Equation 6-9 leads to the impulse response filter given by Equation 6-10 that can be convolved with a representation of the open area or local pattern density across the wafer shown in Figure 6-3. This gives us an "effective" pattern density map that incorporates the location specific depression in reactant concentration. The empirical constant coefficient α in Equation 6-10 is added to scale the filter with respect to wafer-level effects [13]. Loading seen by reactant concentration at a given point *[x,y]* on the wafer surface is the weighted average of surrounding open surface areas.

$$f = -\alpha\left(\frac{k}{D}\right)\frac{1}{2\pi r} \tag{6-10}$$

$$f_1 = \frac{a}{(r+c)^b} \tag{6-11}$$

Furthermore, we see in Equation 6-10 that the filter is an inverse function of distance of the form $(1/r)$. This physical derivation suggests that a family of model forms that are also inverse or decreasing functions of distance may be useful as filters in our semi-empirical modeling approach. Other filters that are not derived from the diffusion equation are elliptical filters and Gaussian filters, shown along with the inverse filter in Figure 6-3. In particular, Equation 6-11 gives a generalized filter f_1 which allows for an arbitrarily fitted set of parameters a, b, and c that can be calibrated using empirical data. The coefficient a represents the diffusion equation parameters and can be tuned for many etch processes. The exponent b captures the slope of decrease in the filter; the slope of the filter becomes sharper with an increase in the value of b. Lastly, the denominator parameter c represents the filter's length or diameter at which the value of the filter

declines appreciably. By setting the value of c, we can express the spatial range over which regions on the chip interact.

Moreover, the set of possible filters need not be generated by assumptions of spherical geometric symmetry. A more exact derivation of the boundary conditions of the chamber may yield other spatial geometries. More formally, if we look at the sheath directly above the wafer and consider the diffusion of reactants as being limited to the sheath geometry, we can model the diffusion of reactants as being bounded by a region more easily described in a cylindrical coordinate system. This gives rise to *ln(r)* dependence.

(a) **(b)** **(c)**

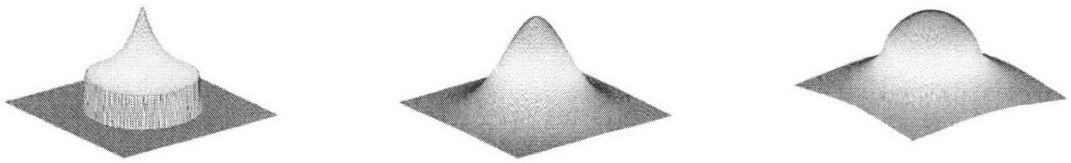

Figure 6-3 – (a) Inverse, (b) Gaussian, and (c) Elliptical filter shapes [21].

Figure 6-4 shows an illustrative example of an effective pattern density map which is obtained by convolving a local layout pattern density map (discretized) with the pattern density response function or filter that describes diffusion of etchant species (Equation 5). The local discretized pattern density (Figure 6-4) is extracted from a GDS layout of our test mask using a pattern density processing tool (courtesy of Praesagus, Inc.). The convolution is efficiently implemented using fast Fourier transform (FFT) approaches (Equation 6-12).

$$z[x,y] = ifft\{fft(f[x,y]) \times fft(d[x,y])\} \tag{6-12}$$

As is observed in Figure 6-4, the effective pattern density is simply a weighted average of neighboring pattern densities at each position on the die. This is where we get the term "effective" pattern density. The 2D filter acts as an "averager" that takes a weighted average of the pattern density for a localized area on the die. The weights are the shape of the filter which results from the parameters used to fit the filter. The filter is normalized such that the area under the filter is one.

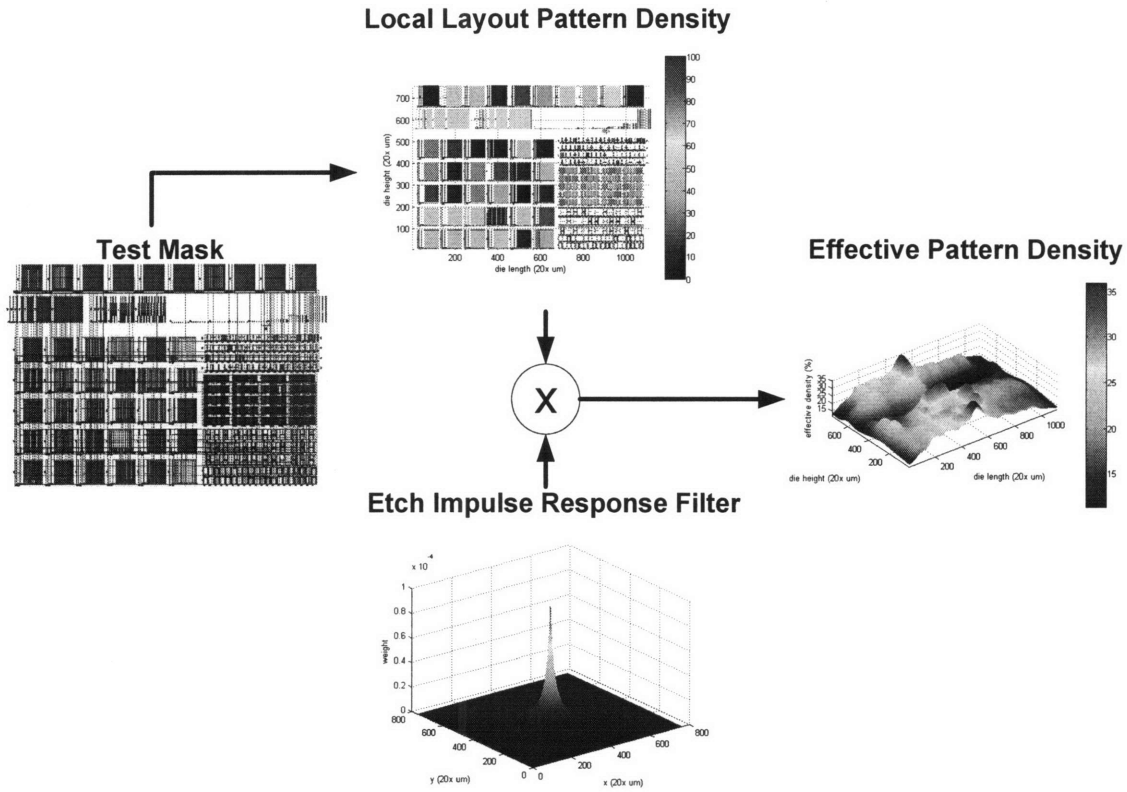

Figure 6-4 – Local layout pattern density, extracted from a mask layout on a discretized grid across the chip, is convolved with an etch impulse response or averaging filter. The result is the effective pattern density across the chip. The vertical axis of the effective pattern density is in percentage.

6.2.4 Pattern Density Model Implementation

Using the effective pattern density function, $\rho_{eff}[x,y]$, we propose an empirical relationship as given by Equation 6-13 to capture the effect of microloading on etch rate. Here, the etch rate R is a negative exponential function of effective pattern density,

$\rho_{eff}[x,y]$, where x and y denote the spatial location on the chip, and parameters R_0, α, and β are fitted using our experimental data. The parameter R_0 represents the global time averaged etch rate that is optimized to fit the model. The coefficient α represents the diffusion equation parameters given in Equation 6-10 and represented by a in Equation 6-11. By optimizing α, the etch equation can be tuned to wafer level effects for many etch processes. The exponent β captures strong local pattern density effects that may result from the slowdown of downward etchant diffusion caused by increased byproduct generation in high density areas. We note that other functional forms besides Equation 6-13 may be reasonable, and some (such as polynomial dependencies) could be generated by Taylor series expansion of Equation 6-13.

$$R = R_0 \cdot e^{-\alpha \cdot \rho_{eff}[x,y]^{\beta}} \tag{6-13}$$

$$z = t \cdot R_0 \cdot e^{-\alpha \cdot \rho_{eff}[x,y]^{\beta}} \tag{6-14}$$

The pattern density model is extracted or generated by fitting the etch rate equation to the empirically measured depth for each structure on the test mask using MATLAB optimization. Since the predicted etch rate R in Equation 6-13 is the time averaged etch rate, we use the empirical time of etch, t, to determine the simulated depth z given in Equation 6-14.

6.3 Model Prediction

We first compare the Gaussian and the inverse ($1/r$) filter and demonstrate how filter shapes vary with the type of filter used; changing the filter parameters can greatly alter the shape of the filter. Then we show how well the pattern density model predicts etch variation when compared to empirical data.

6.3.1 Filter Comparison

Figure 6-5a shows a local pattern density extraction of our test die with locations on the die where depth measurements were taken for use in calibrating our etch model. The spatial locations of the measurements span most of the die and provide areas of different pattern densities. Figure 6-5b shows the locations of all the measurement points, while Figures 6-5c and 6-5d shows the location of structures with critical dimension of 0.1 μm and 3 μm, respectively.

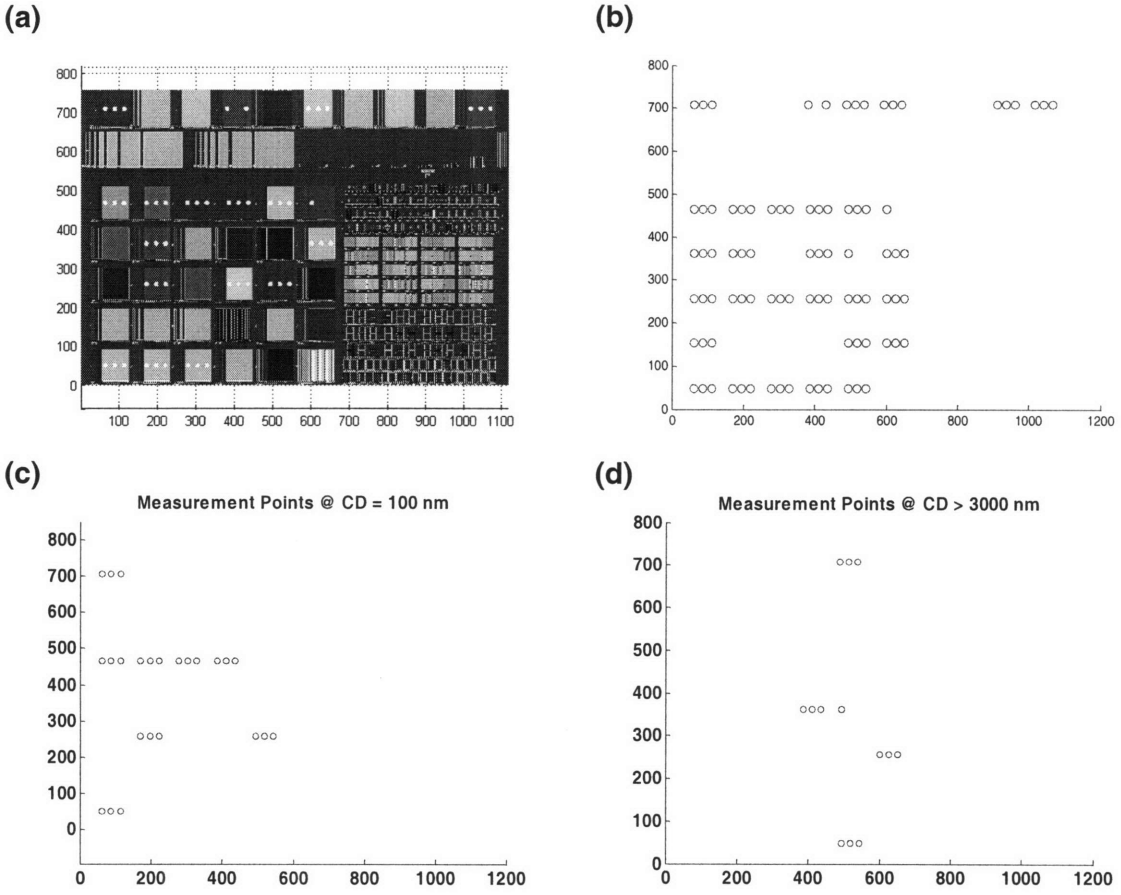

Figure 6-5 – Spatial location on test die of depth measurements; the coordinates indicate the spatial location of structures and measurement points on the chip (in 20x μm). (a) Local layout pattern density with (b) locations of measurements. (c) Location of 100 nm (0.1 μm) line width structures. (d) Location of structures with line widths greater than 3000 nm (3 μm).

The effective pattern density at the measurement locations depends on the filter chosen. Figures 6-6 and 6-7 illustrate the Gaussian and inverse (Equation 6-11) filter types and their corresponding effect on effective pattern density. Both filters are normalized to unit area. The filter data structure is a square matrix with length equal to the minimum extent of the local pattern density data structure. The Gaussian impulse response filter, shown in Figure 6-6 for various widths, is more conical than the inverse filter, shown in Figure 6-7, which is sharply pointed and quickly decreasing. The Gaussian filter has a cone like shape that quickly goes to zero, while the inverse filter has a needle head and a wide bottom. The difference in shapes results in the Gaussian filter averaging over a much more localized area, while the inverse filter (Equation 6-11) averages over a wider area.

The primary parameter in determining the filter shape is the width. The filter width sets the area of pattern density interaction: the filter width determines how quickly the filter decreases, and therefore determines the localized area where pattern density influences reactant concentration.

In the case of the Gaussian filter, the standard deviation of the Gaussian function represents the width or spread of a Gaussian curve. Figure 6-6 shows the Gaussian filter for three widths (standard deviations): 20, 600, and 2000 microns. The effective pattern densities in the first column of Figure 6-6 show that the Gaussian filter averages the pattern density for a localized area of the die. For a filter width of 20 and 600 μm, the distinct features on the die are clearly visible with averaged densities. Even for a wide filter width of 2000 μm, the features are locally averaged due to the sharp cutoff of the Gaussian filter.

In the case of the inverse filter, the width is defined as the distance at which the magnitude of the filter is halved and is represented by the parameter c in Equation 6-11. Figure 6-7 shows the inverse filter for three widths: 20, 600, and 2000 microns. The first filter in row one is the inverse ($1/r$) filter generated by the solution to the diffusion equation. It has a sharp point at its center and a wide bottom. In fact, the inverse distance filter has a magnitude that is mostly concentrated at its center. This arises from the diffusion equation assumptions by which the local reactant concentration at each location on the die depends on neighboring pattern density that provides competition for reactants. The inverse ($1/r$) filter assumes that the entire wafer is providing competition for reactants at each point. Long range averaging occurs for filter widths of 600 and 2000 μm.

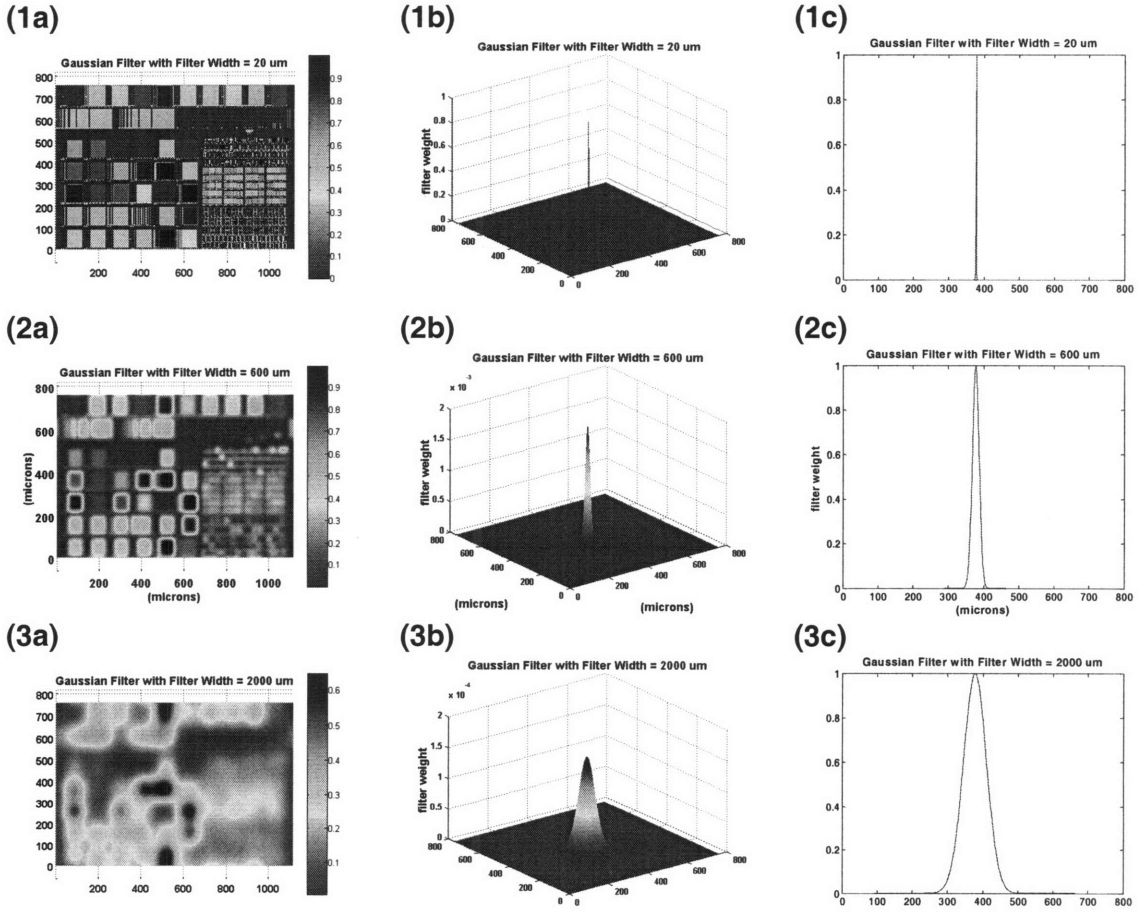

Figure 6-6 – (Top row) Effective pattern density using gaussian filter with filter width of 20 μm, (middle row) filter width of 600 μm, (bottom row) filter width of 2000 μm.

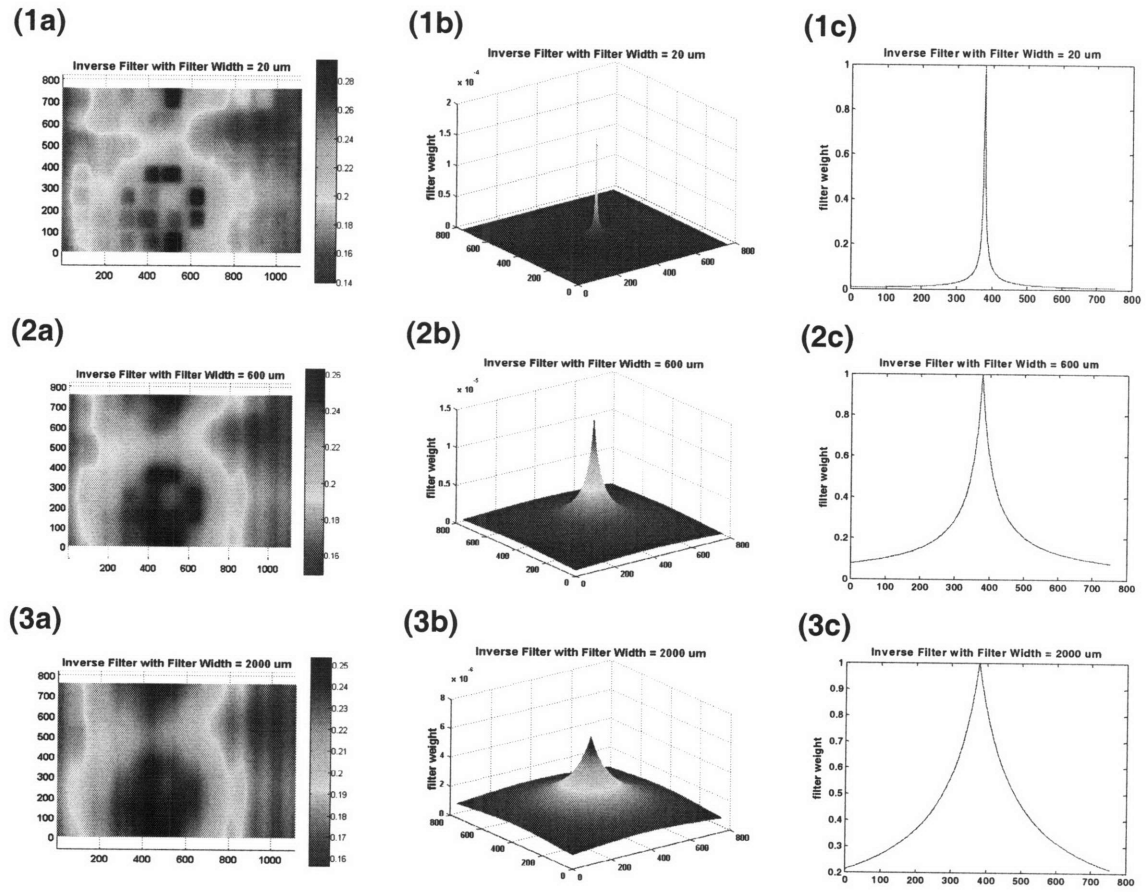

Figure 6-7 – (Top row) Effective pattern density using inverse distance filter with filter width of 20 μm, (middle row) filter width of 600 μm, (bottom row) filter width of 2000 μm.

6.3.2 Model Results

To test the model including only pattern density effects as described above, we fit the model to our experimental data set using MATLAB optimization. Figure 6-8 shows the resulting effective pattern density map for the test chip using a pattern density filter given by Equation 6-11, and Figure 6-9 illustrates the chip-scale prediction for etch depth based on the fitted model. Figure 6-10 shows the empirical and simulated depth for 0.1 μm structures at various densities with an overall root mean square (rms) error of 4.5%. We see that the simulated results appear to be consistent with a pattern density trend in the empirical data.

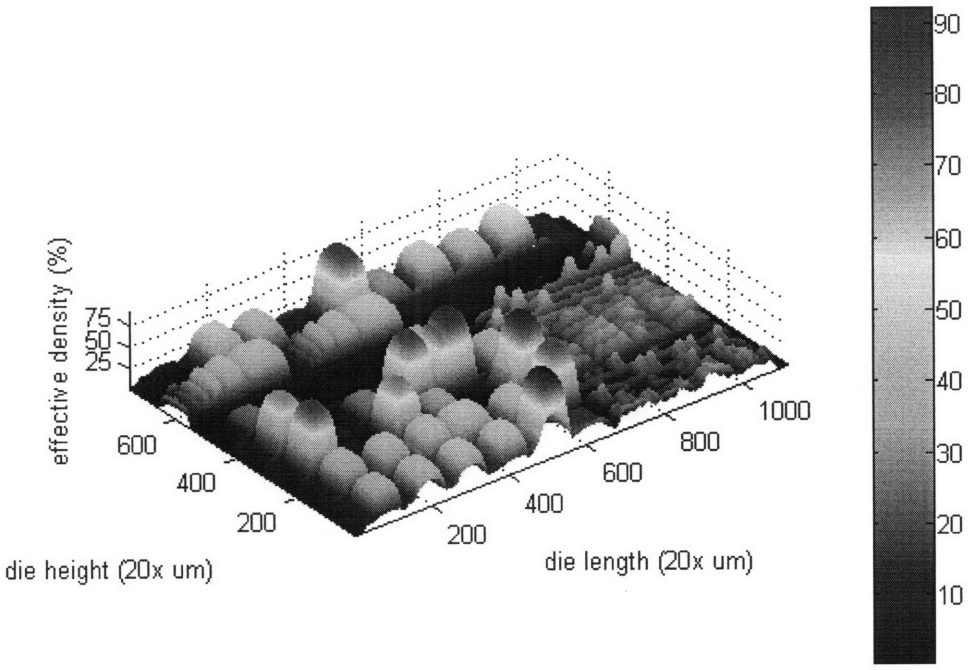

Figure 6-8 – 3D view of effective pattern density, as extracted using the pattern density only model.

The fitted model parameters for this experimental data are shown in Table 6-1. The extracted value for b indicates that the "best-fit" filter for the pattern-density only model is sharply sloped and declines quickly. Along with a narrow filter length, c, we see that the model based only on pattern-density uses a fairly localized effective pattern density, and does not appear to depend strongly on neighboring structures. Similarly, Figure 6-8 shows that the effective pattern density closely mirrors the local pattern density with little spatial averaging. This primarily local dependence on the layout suggests that local feature dependencies may be highly important in determining etch depth. In the next chapter, we attempt an alternative model based only on feature size. We will see that this model also suffers from poor prediction, leading us to the integrated pattern density and feature size model we present later in the Chapter 8.

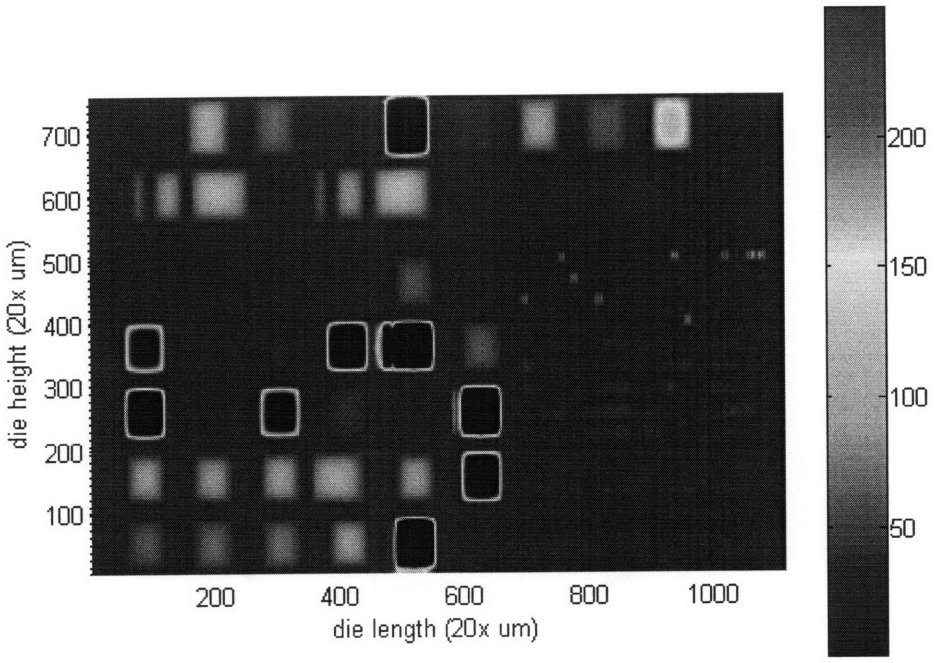

Figure 6-9 – Chip-scale simulation of etch depth (in nm) using the pattern density only model.

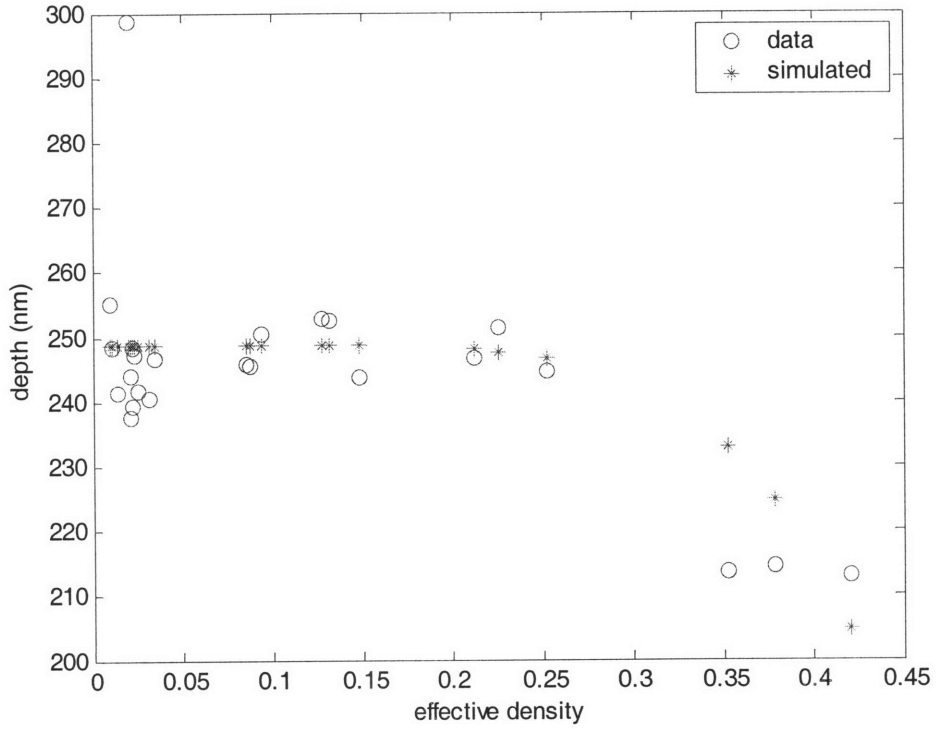

Figure 6-10 – Simulated and experimental etch depth. Simulations are based on the pattern density only model for 0.1 μm features. The rms error is 4.5%.

Table 6-1 – Extracted pattern density-only parameters.

t (sec)	r (μm/sec)	$\alpha = a$	β	b	c
75	3.3	35	6	4.3	214.6

6.4 Limitations of Model

The limitations of using pattern density alone as an etch prediction tool is that we are only able to predict general trends affecting all features on a chip. We are not able to predict well individual feature depth. As mentioned earlier, pattern density is an averaging phenomenon whereby etch rates are determined for localized areas by localized competition for reactants. Because the etch rate is for a localized area and not for specific features within the localized area, there is an averaging effect whereby the predicted depth is the weighted average of the depths of all features. In order to get better prediction for individual features, we introduce the feature level (ARDE) model in the next chapter.

6.5 Summary

This chapter presented the pattern density model as a derivation of the microloading effect seen at the die level, where variations in open area lead to competition for reactants. This competition for reactants leads to variations in reactant concentration over the wafer, and results in variations in etch depth. We model the perturbation in reactant concentration by deriving the diffusion equation and using it as an impulse response filter that describes the depletion of reactants due to the presence of a unit of pattern density. The filter is shown to be of an inverse ($1/r$) shape, and we described how other filter shapes, such as Gaussian, can be fitted using empirical data from our experiment. We further noted that the critical determinant of the filter shape is its width, and showed how varying the filter type and width can give different reactant concentration profiles on the

die (e.g. effective pattern density). Lastly, we showed that the pattern density model used alone did well in capturing the overall pattern density effect, but did poorly in predicting individual feature dependencies.

Chapter 7

A Feature Based Etch Prediction Model

We present a feature based model for determining etch depth for individual structures across an integrated circuit chip. In Chapter 6 we presented a quantitative model capturing plasma etch pattern density effects for Integrated Circuits and showed how it captured long scale microloading effects caused by reactant depletion but failed to predict shorter scale depth variations across individual features. The feature based model attempts to capture etch variations that are due to differences in line width of various features on the die, also referred to as aspect ratio dependent etching or RIE lag. The feature based model is a complement to the pattern density based model in that the feature based model captures short scale depth variations but fails to capture long scale depth variations. As we will see in Chapter 8, the integrated pattern density and feature based model is capable of capture both long and short scale depth variations.

Transport kinetics of ions and reactive neutrals are the primary physical cause of RIE lag [4][6]. Variations in reactant transport within individual features (trenches) are due to differences in the ability of reactant species to enter features of different size. We gave the theoretical underpinning of ARDE in Chapter 2 where we showed that transport kinetics of ions and reactive neutrals are the primary physical cause of RIE-Lag. This chapter focuses on reactive neutral transport within the trench, although ion transport has a similar effect on RIE-Lag.

Section 7.1 presents the Coburn and Winters feature based model. Section 7.2 presents the results of the Coburn and Winters feature based model. Section 7.3 presents our summary.

7.1 Coburn and Winters Model

Our feature level model implements the Coburn and Winters (CW) model [6], which applies the theory of Knudsen transport to the etch process. This model relates the flux of reactants at the top of the feature to the flux at the closed bottom, and sets the ratio of the fluxes equal to the etch rate of the trench. If there is no consumption at the bottom (i.e. etching), then the fluxes will be identical [6]. The CW model uses conservation of gas flow to express etchant gas fluxes into and out of the closed feature [6]. The difference in the fluxes is equated to the etching reaction rate (Equation 7-1) [6].

7.1.1 Model Description

Figure 7-1 illustrates the CW model and Equations 7-1 and 7-2 quantify the model. The first term in Equation 7-1 is a randomly directed (isotropic) incident flux (v_t) that enters the trench. The second term is the fraction of the incident flux that is reflected back out of the feature without reaching the bottom surface. This fraction is one minus the Knudsen coefficient, which is the probability that the incident flux reaches the bottom surface. The third term is the reactant flux which reaches the bottom surface but does not react and eventually escape through the open end. The right hand term represents the consumed reactant species. The s term in the equation is the probability that the reactant species adsorbs and reacts with the bottom surface of the feature. Therefore, the CW model sets the net flux into the trench equal to the consumed reactant species flux at the bottom surface [6].

$$v_t - (1-k)v_t - k(1-s)v_b = sv_b \tag{7-1}$$

$$\frac{R(z/d)}{R(0)} \equiv \frac{v_b}{v_t} = \frac{k}{k+(1-k)s} \tag{7-2}$$

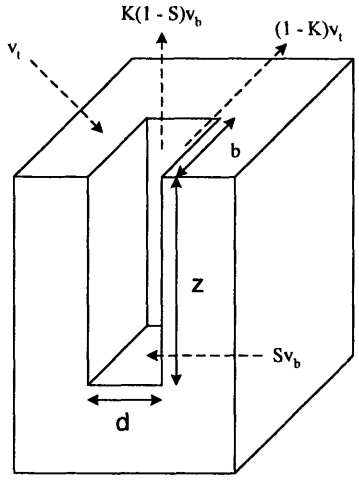

Figure 7-1 – Schematic of etchant flux in narrow trench feature.

Furthermore, the CW model makes the assumption that etch rates will be proportional to the flux of etching species [4][6]. Equation 7-1 sets the net flux into the trench equal to the consumed reactant species flux at the bottom surface. Equation 7-2 gives the ratio of the etch rate at the bottom of a feature of depth z and width d, $R(z/d)$, to the etch rate at the top of the feature $R(0)$. The s term in the equations is the probability that the reactant species adsorbs and reacts with the bottom surface of the feature. With a known or empirically fitted etch rate at the top, we can calculate the etch rate at the bottom using Equation 7-2. The equation is composed of the Knudsen coefficient (k) and the reaction probability (s). The reaction probability can be empirically fit such that the rms error between the simulated depth and the actual depth is minimized.

The CW model allows for the modeling of aspect ratio dependence in etch variations seen by individual features. In order to estimate the reaction probability that allows for the best prediction of etch depth with the smallest rms error, we use a MATLAB optimization loop that performs a scalar bounded nonlinear minimization.

7.2 Model Results

To test the model, we fit this feature based model against our experimental data. We obtain a reaction probability of 0.397 with an rms error of 7.3% from the optimization loop. Figure 7-2 shows the comparisons between the model fit and experimental data, as a function of feature size. Figure 7-3 shows the chip-scale simulation of etch depth using this model. As in the pattern-density only model, we find that the feature-scale only model captures some trends, but results in an even weaker model fit (with larger rms error). This motivates us to explore an integrated model incorporating both effects as described in the next chapter.

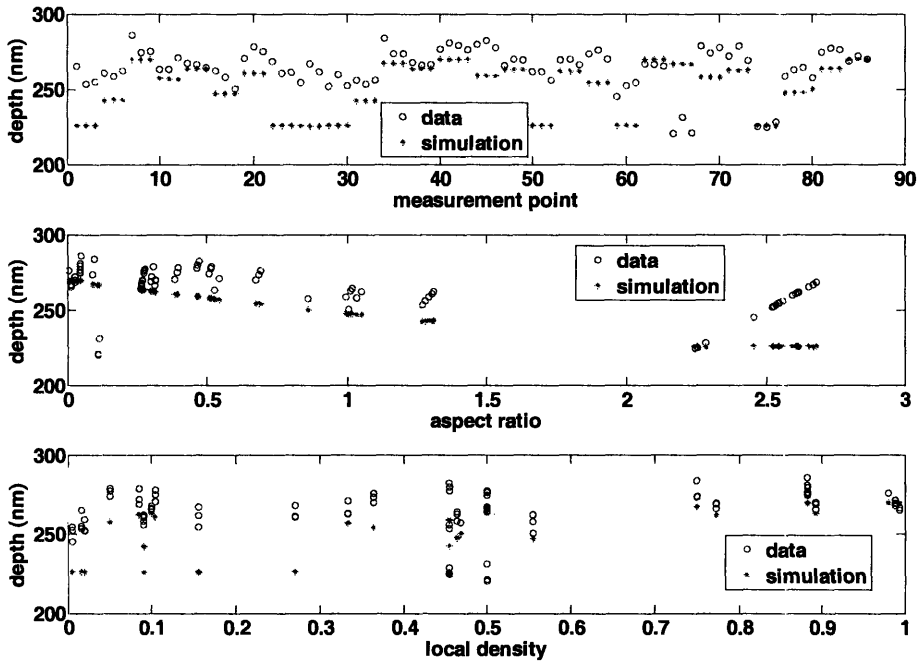

Figure 7-2 – Feature based model comparison to measurement data. Overall fit has 7.3% rms error.

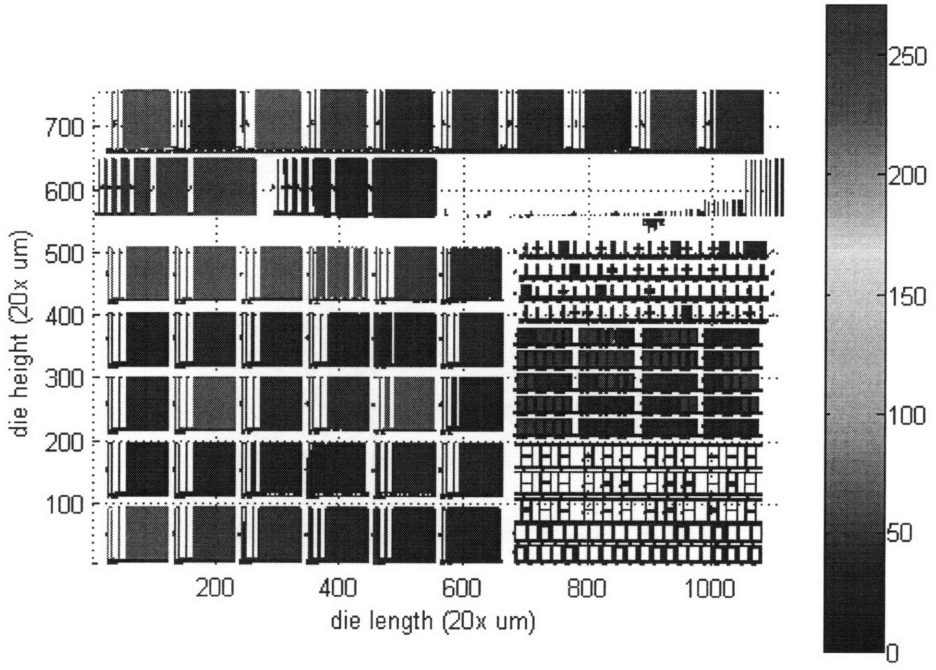

Figure 7-3 – Chip-scale simulation using the feature based only model. The scale indicates the predicted etch depth (in nm).

7.3 Summary

This chapter presented the feature level model. The feature level model captures variations resulting from differences in individual feature size and can be used to model the RIE-lag effect in plasma etching. The model fails to predict any interactions between and among different features that leads to etch rate non-uniformity. The next chapter presents the integrated model that can both capture individual feature variation and long range interactions among structures.

Chapter 8

An Integrated Etch Prediction Model

The pattern density and feature level models predict etch variations due to pattern dependencies. But they both suffer from different deficiencies. The pattern density model predicts etch variations on a long length scale across many features, while the feature level model predicts etch rate for individual features. This chapter presents an integrated model that achieves better overall prediction and combines the variations caused by individual attributes of each feature along with the near neighbor interactions among many features.

Section 8.1 presents the model description and Section 8.2 presents the model results. Section 8.3 concludes the chapter.

8.1 Model Description

The combined pattern density and feature level model captures localized variations in etch rate due to pattern density along with feature specific aspect ratio dependencies. Equation 8-1 summarizes the combined model, where the reactant flux at the top of the feature is set by the reactant concentration as determined by our pattern density model. The first part of Equation 8-1 represents the pattern density model. In the context of the combined etch model, the empirical time averaged etch rate R_0 represents the global etch rate for the entire wafer. Effective pattern density represents the microloading process that perturbs the uniform etch rate across the chip due to reactant consumption and diffusion.

$$R(z/d) = \left[r \cdot e^{-\alpha \cdot \rho_{eff}(x,y)^{\beta}}\right]\left[\frac{k}{k+(1-k)s}\right] \tag{8-1}$$

Furthermore, the model integrates the two mechanisms that govern microloading and RIE lag: diffusion and transport of reactants. The diffusion occurs at the top surface of the wafer while the transport occurs into the etching structures. Our integrated model first determines the time averaged diffusion profile of reactants, which we termed effective pattern density. Then we use the time evolution of etch rates due to aspect ratio in the CW model to determine how fast each feature size is etching. Aspect ratio determines the transport rate of species reaching the bottom of the etching feature. As aspect ratio evolves over the lifetime of the etch process, the etch rate also evolves for each feature size. Diffusion modifies the amount of reactants able to be transported into the etching structure. By simultaneously optimizing for both the diffusion coefficients and transport coefficients, we merge the two etch mechanisms and achieve an overall improved predictive model.

8.2 Model Results

The integrated model is fit to our empirical data, resulting in an overall 2% rms error, substantially better than either the pattern density only or feature size only models. Figure 8-1 illustrates the effective pattern density across the test chip, as determined by the best-fit filter function for the integrated model. Figure 8-2 illustrates the chip scale prediction of the etch depth for all regions on the test chip, and Table 8-1 gives the extracted parameters of our model fit for this experimental data.

Table 8-1 – Extracted parameters of the integrated model.

r (μm/s)	$\alpha = a$	β	b	c (μm)	s
3.65	2.6	7.7	2	197.7	0.124

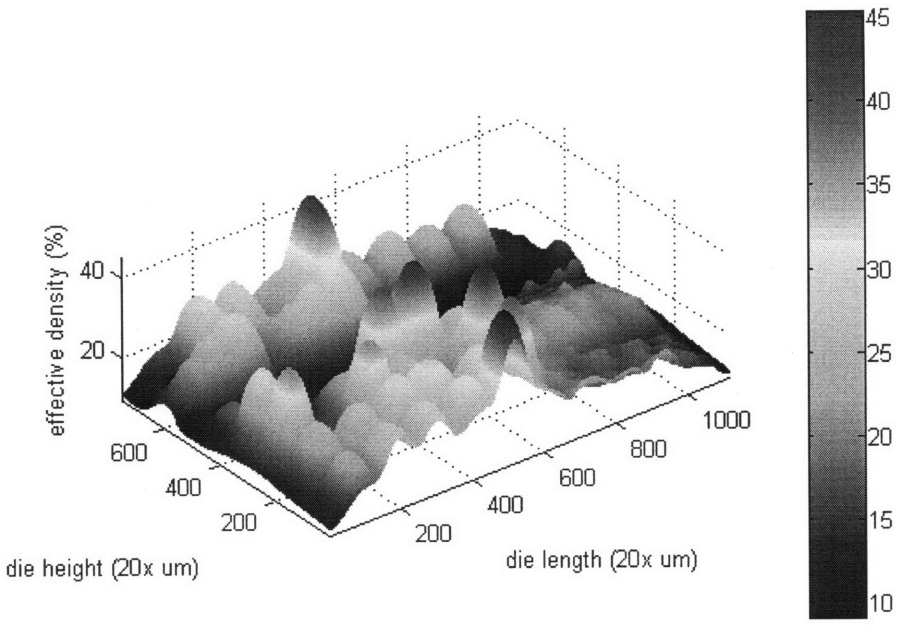

Figure 8-1 – 3D view of effective pattern density for integrated etch model.

Comparisons between measurement and simulation for our measured structures are shown in Figure 8-3. The top plot of Figure 8-3 gives the data and corresponding predicted result of our model for all features across the die. The second plot shows our measured and predicted depth as a function of aspect ratio. We observe that there is a visible aspect ratio trend (RIE lag) in the data and that our model tracks this trend. The third plot shows the data and predicted depth as a function of effective pattern density. We observe that any trend in pattern density alone is difficult to discern. This is because the measured structures also have different aspect ratios, so the two trends of pattern density and feature size are coupled. Referring again to the top plot in Figure 8-3, we see that the integrated model is able to combine the feature size and pattern density dependencies in order to accurately predict the etch depth for each structure on the test chip.

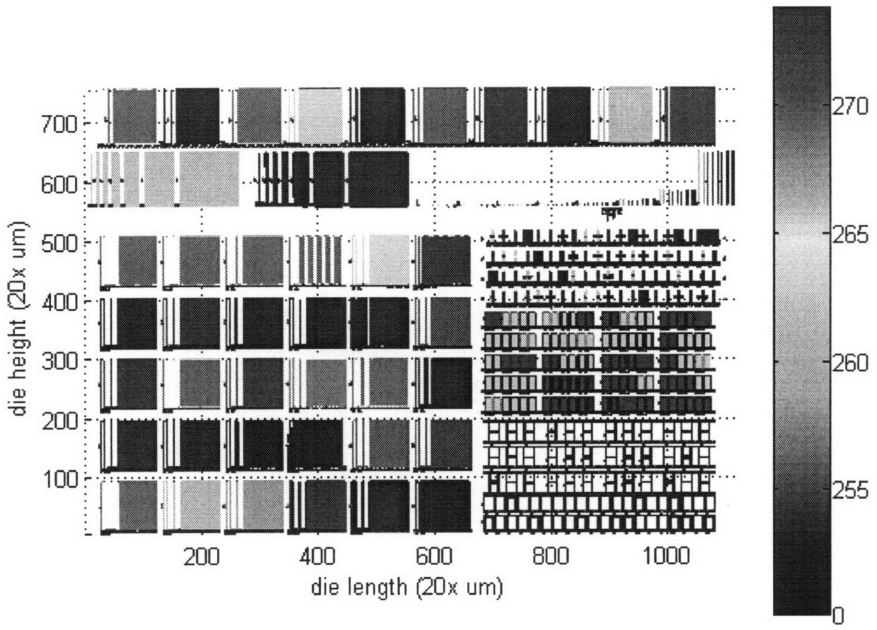

Figure 8-2 – Chip-scale simulation of etch depth using the integrated model. The scale indicates the predicted depth (in nm) based on both pattern density and aspect ratio.

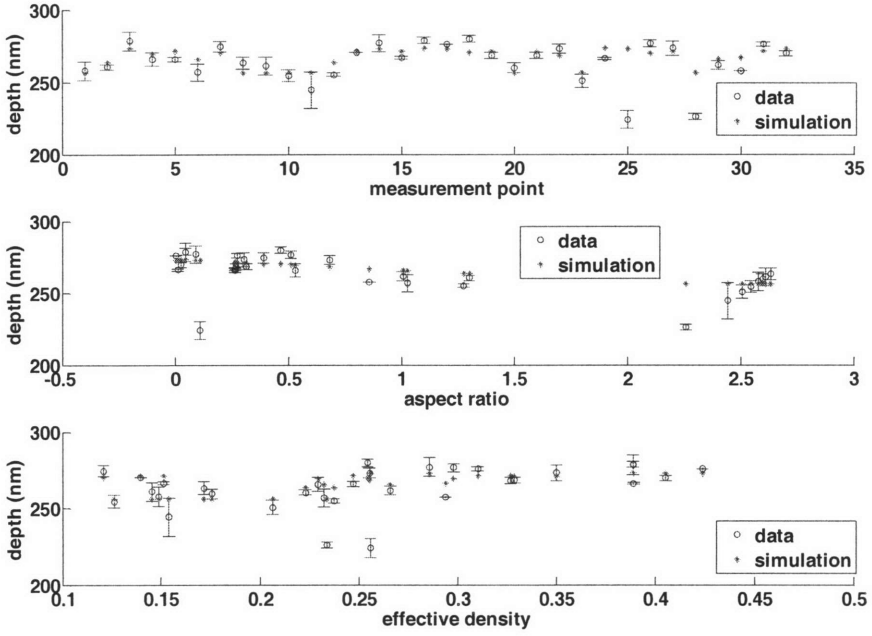

Figure 8-3 – Comparison of integrated model prediction and measurement data (top); as function of line width (middle); as function of pattern density (bottom).

8.3 Summary

This chapter presented the integrated pattern density and feature level model as an interaction between reactant diffusion that leads to microloading, and reactant transport that leads to RIE-Lag. We showed that etch non-uniformity is governed by both competition for reactants due to pattern density, and aspect ratio dependencies due to feature width and the evolution in feature depth. We combined our two previous two etch models. The first models the perturbation in reactant concentration by deriving the diffusion equation and using it as an impulse response filter that describes the reactant depletion. The second models transport of the reactants down to the etching interface. Combined, the integrated model provides a good chip scale prediction of etch variation across many reticle structures.

Chapter 9

Conclusion and Future Work

This thesis attempts to characterize and model etch rate variations resulting from plasma etching of interlayer dielectric in integrated circuit manufacturing. The thesis focuses on understanding the theoretical causes and effects of non-uniformity and then generating a model based on our theoretical understanding. We then implement two models using the microloading and aspect ratio dependent etching effects, which result from reactant diffusion and transport dynamics explained in Chapter 2. The first of the two models is the pattern density model. The second of the two models is the feature based model. We found that neither model alone was able to capture all etch rate variations. Therefore, we combine the pattern density and feature based models into the integrated model, which is able to predict etch rate variations.

Section 9.1 comments on the pattern density only model and suggests future paths to improving the model. Section 9.2 focuses on the feature based model and suggests future improvements to the model. Section 9.3 examines the integrated model and suggests future improvements to the integration of pattern density and feature level variation modeling. Section 9.4 discusses the possible addition of a wafer level model. Lastly, Section 9.5 concludes the thesis.

9.1 Pattern Density Model Conclusion and Future Work

The pattern density model alone is able to model microloading trends. As discussed in Chapter 6, the pattern density model alone is not able to model feature level trends such as aspect ratio dependence. This leads us to explore possible improvements to the ability of the pattern density model to predict microloading trends.

The key capability of the pattern density model is the generation of the effective pattern density through convolution of a diffusion filter with the local pattern density of a chip. The current pattern density model uses a time averaged effective pattern density calculation. A future improvement of the pattern density model will incorporate a time evolving change in the effective pattern density similar to the time evolution in the feature level model. By calculating the change in effective pattern density as the etch process evolves, we can capture how the change in reactant concentration over time affects etch rate uniformity.

9.2 Feature Based Model Conclusion and Future Work

The feature based model is able to model RIE-lag trends. As discussed in Chapter 7, the feature based model alone is not able to capture microloading or other long scale trends. This leads us to explore improvements to ability of the feature level model to predict aspect ratio dependencies.

As discussed in Chapter 2, there are alternative models that can predict RIE-lag trends. The neutral shadowing model given by Gottscho et al. can be used to predict aspect ratio dependencies and add to the Coburn and Winters model for greater predictive accuracy [4]. Also, the Coburn and Winters feature based model equates the etching rate ratio to the neutral flux ratio by making the assumption that the neutral reaction probability is independent of the neutral flux [4]. This assumption only holds when the neutral flux is relatively much smaller than the ion flux [4]. In general, the neutral reaction probability depends on the neutral flux, thus the etching rate ratio cannot be equated to the neutral flux ratio. Gottscho et al. propose an improvement to the Coburn and Winters model that can be explored in future iterations of the feature level model [4].

9.3 Integrated Model Conclusion and Future Work

The integrated model captured both pattern density and aspect ratio dependencies. In order to improve the integrated model, we must explore the interaction of the causes of ARDE and microloading. In the case of ARDE, the reduction in reactant transport for high aspect ratio structures versus low aspect ratio structures explains many of the observed variations. Microloading is caused by reactant depletion in areas of high loading. Therefore, we must explore how the possibility that reduced reactant transport into a high aspect ratio structure may increase the available reactant concentration above the structure and thus moderate reactant depletion caused by microloading. Other interactions can also be explored such as incorporating a wafer level component into the integrated model.

9.4 Wafer Level Model

Our pattern density, feature based, and integrated models assumed a constant global etch rate. This assumption is not entirely appropriate. Wafer level variations induced by the plasma formation in the etching chamber can generate non-uniform global etch rates across a wafer. We considered some of the causes of wafer level variations in Chapter 2. An incorporation of a wafer level model into our integrated model framework would enable the model to predict wafer-scale etch variations along with chip-scale variations.

9.5 Summary

This thesis attempts an initial modeling approach to capture etch rate variations that can be attributed to microloading and aspect ratio effects. Our results show that an integrated model can captures both pattern density and feature level effects and yields a

superior prediction of etch rate variations as compared to a feature based or pattern density model alone.

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