Design of Micropower Operational Amplifiers

by

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Abstract

The operational amplifier is a fundamental building block for electronic devices and systems. The advancement of modern electronic technology has been setting more performance demand on the underlying integrated circuits including the operational amplifier. Reduction in power consumption and improvement in speed are some of the most important requirements. To address these concerns, this thesis presents a design of micropower Class AB operational amplifiers which has the ratio of gain bandwidth product to supply current higher than that of an existing IC. The design is in a 0.6μm CMOS process. The input stage of the design has the folded-cascode architecture that allows the input common-mode range down to negative supply voltage. The Class AB output stage swings rail-to-rail and has the ratio of maximum current to quiescent current greater than 100. The bias cell of the operational amplifier is designed to consume only 6% of the total supply current. The thesis concludes the operational amplifier design with two frequency compensation options. The one with simple Miller compensation has a unity gain frequency of 360kHz with 61.5 degrees of phase margin at 100pF load while consuming 20μA supply current. The other with the hybrid of simple Miller compensation and cascode compensation offers an improved unity gain frequency of 590kHz at the same loading and power condition.

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Chapter 1 Introduction

The operational amplifier is a fundamental building block in electronics. It is employed in a wide range of applications including monitoring circuitry, cellular phones, portable devices, medical instrumentation, and solar-powered systems [1], [2]. Linear Technology Corporation launched *LTC1541 Micropower Op Amp/Comparator/Reference* in February 1998. The IC has been incorporated in many consumer products such as smoke detectors, infrared receivers, battery-powered systems, and portable phones [1].

1.1 Overview of Micropower Op Amp in *LTC1541*

The micropower op amp, which is part of *LTC1541*, was fabricated in a 4.0μm CMOS process. It has a unity-gain frequency of 12kHz while consuming a typical supply current of 1.5μA. Electrical characteristics of *LTC1541* with 3V supply voltage at 25 °C from [1] are summarized in Table 1-1.

Specifications are at 25°C. V_{DD} = 3.0V and V_{SS} = 0V.							
Primary Characteristics							
Symbol	**Parameter**		**Condition**	**Value**			**Unit**
				Min	**Typical**	**Max**	
GBW[1]	**Gain Bandwidth Product**		C_L = 0pF R_L = 100kΩ	-	**12**	-	**kHz**
A_{VOL}	**Large-Signal Voltage Gain (DC Open-Loop Gain)**		C_L = 0pF R_L = 100kΩ	**93**	**114**	-	**dB**
I_S	**Supply Current**		No load	-	**1.5**	-	**μA**
V_{INCM}	Input Common-Mode Range		-	V_{SS}	-	V_{DD} - 1.3V	V
V_{OS}	Input Offset Voltage		V_{INCM} = 1.5V	-	-	0.7	mV
V_{OUT}	V_{OUTH}	Output High Voltage	R_L = 100kΩ to V_{SS}	V_{DD} - 0.07V	-	-	V

[1] Implying the gain bandwidth product per supply current GBW/ I_S = 8 MHz/mA @ C_L = 0pF

	V_{OUTL}	Output Low Voltage	R_L = 100kΩ to V_{DD}	-	-	V_{SS} + 0.05V	V
I_{SOURCE}	Output Source Current		-	0.6	0.95	-	mA
I_{SINK}	Output Sink Current		-	1.2	1.8	-	mA
Secondary Characteristics							
Symbol	**Parameter**		**Condition**	**Value**			**Unit**
				Min	**Typical**	**Max**	
SR	Slew Rate		A_V = 1V/V, 1V Step	-	0.008	-	V/μs
CMRR	Common Mode Rejection Ratio		@ DC V_{INCM} = V_{SS} to V_{DD} -1.3	63	-	-	dB
PSRR	Power Supply Rejection Ratio		@ DC	74	-	-	dB
e_n	Input Noise Voltage		f = 0.1 to 10Hz	-	3	-	μV_{P-P}

Table 1-1: Electrical Characteristics of *LTC1541* [1]

1.2 *LTC1541* Limitations and Problem Definition

The standard of electronic equipment and systems has been constantly developing for the past years. This condition has imposed more demanding performance requirements on the supporting semiconductor products, particularly lower power consumption and higher speed. As a result, these foundational integrated circuits including op amps have to continually improve to meet the need.

Currently, there are a few general-purpose low-power op amp ICs in the market. One of them is *MAX9914 1MHz, 20μA, Rail-to-Rail I/O Op Amps with Shutdown* by Maxim Integrated Products. It has a 1MHz gain-bandwidth product at 15pF load with 45 degrees of phase margin [3]. Another well-known one is *MIC861 Teeny™ Ultra Low Power Op Amp* by Micrel, Inc. With static supply current of 4.6μA, *MIC861* offers a 225kHz gain-bandwidth product at 50pF load with approximately 45 degrees of phase margin[2] [4].

Although the *Micropower Op Amp* in *LTC1541* consumes an extremely low supply current, its speed is far too low to accommodate the need of modern technologies such as medical instrumentation [5] and portable devices. This thesis seeks to identify

[2] The phase margin is not given in [4]. It is estimated from the datasheet that the IC has 2-3 periods of decayed oscillation in the small-signal pulse response at 50pF load.

the fundamental limit of speed versus power consumption and propose an improved general-purpose micropower op amp whose speed to supply current ratio is higher than that of *LTC1541*. Other crucial performance specifications are large DC gain and wide input common-mode range that includes the negative supply voltage. In addition, op amp characteristics such as stability, input offset voltage, output swing, and output drive capability have to be considered as well. Some target applications of the new general-purpose low-power op amp include battery-powered systems, portable electronic devices, and safety sensors.

1.3 Thesis Goal

This thesis aims to design a two-stage operational amplifier that satisfies the performance specifications in Table 1-2 and can operate between supply voltages of 2.5V up to 6.0V. The specifications are defined at supply voltage of 2.5V, and they are ordered by their relative importance in the descending order. The first three parameters: unity gain frequency, DC open-loop gain, and supply current, are central in the design process. The other requirements on the primary list must be met, unless their sacrifice exceptionally enhances one of the first three characteristics. The design should also satisfy all the secondary specifications.

Specifications are at 25°C. V_{DD} = 2.5V and V_{SS} = 0V.				
Primary Specifications				
Symbol	**Parameter**	**Condition**	**Value**	**Unit**
GBW[3]	**Gain Bandwidth Product**	C_L = 100pF R_L = 100kΩ	**> 0.3**	**MHz**
A_{VOL}	**Large-Signal Voltage Gain (DC Open-Loop Gain)**	C_L = 100pF R_L = 100kΩ	**> 100**	**dB**
I_S	**Supply Current**	No Load	**< 21**	**µA**
V_{INCM}	Input Common-Mode Range	-	> V_{DD} - 1.25V And must include negative supply voltage	V

[3] Implying the gain bandwidth product per supply current GBW/ I_S > 14.3 MHz/mA @ C_L = 100pF. Note that GBW/ I_S @ C_L = 0pF is going to be higher than that @ C_L = 100pF.

V_{OS}	(Untrimmed) Input Offset Voltage		V_{INCM} = 0.65V	< 5	mV
V_{OUT}	V_{OUTH}	High Output Voltage	I_{SOURCE} = 1.0mA	> V_{DD} - 0.3V	V
	V_{OUTL}	Low Output Voltage	I_{SINK} = 1.0mA	< V_{SS} + 0.3V	V
I_{SOURCE}	Output Source Current		C_L = 100pF R_L = 100kΩ	> 1.0	mA
I_{SINK}	Output Sink Current		C_L = 100pF R_L = 100kΩ	> 1.0	mA
Secondary Specifications					
Symbol	**Parameter**		**Condition**	**Value**	**Unit**
SR	Slew Rate		A_V = 1V/V, 1V Step	> 0.15	V/μs
CMRR	Common Mode Rejection Ratio		@ DC	> 60	dB
PSRR	Power Supply Rejection Ratio		@ DC	> 60	dB
t_s	0.1% Settling Time		A_V = 1V/V, 1V Step	< 10	μs

Table 1-2: Design Specifications of Micropower Op Amp

With these specifications, the new design is expected to be a more versatile low-power general-purpose op amp than the *Micropower Op Amp* in *LTC1541*. The unity-gain frequency is specified to be greater than 300kHz so that the op amp can accommodate a broader range of applications. At this frequency, the op amp has to be properly compensated and well stable with 100pF load.

For supply current, the new op amp must take less than 21μA in order to be power-friendly to portable equipment and battery-powered systems. This power restriction implies that the ratio of gain-bandwidth product to supply current has to be greater than 14.3 MHz/mA at 100pF load, which is higher than that of the *Micropower Op Amp* in *LTC1541* or 8 MHz/mA at 0pF load.

Another main specification of the new design is a large DC open-loop gain of more than 100dB. The large DC open-loop gain is important for low-frequency detecting applications such as gas sensors because it minimizes the gain error. Moreover, in these applications, the input voltage is small and a large gain is needed to get a measurable output [6].

The input common-mode range of the new micropower op amp is specified to be wider than half of the supply voltage and must include the negative supply voltage. This specification is imposed because a number of single-supply applications, such as the photodiode amplifier in Figure 1-1, have to take the input at the ground level. In

addition, many dual-supply applications such as the inverting amplifier in Figure 1-2 are often biased at its mid supply voltage or ground [6].

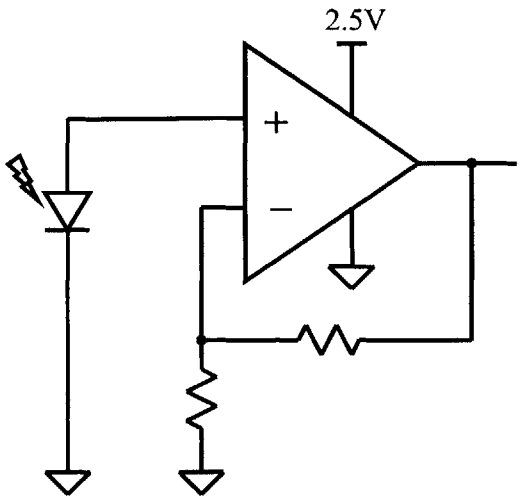


Figure 1-1: Photodiode Amplifier with Single-supply

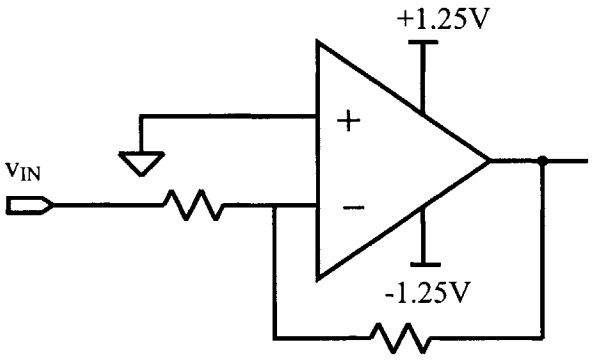


Figure 1-2: Inverting Amplifier with Dual Supplies

1.4 Thesis Organization

Chapter 1 gives an overview of low-power operational amplifiers and their applications, defines the problem of interest, and sets the goal that this thesis seeks to achieve.

The rest of the thesis is organized as follows. Chapter 2 discusses how the target specifications constrain the design of input stage of the micropower op amp, and demonstrates the input stage details resulted from the restrictions. Chapter 3 extensively

describes the output stage. The design of bias cell is presented in Chapter 4. Chapter 5 looks into the limitation on the gain bandwidth product in the context of frequency compensation of two-stage op amps. It then presents the complete micropower op amps, and selected simulation results. Lastly, Chapter 6 discusses the results and concludes the thesis work. In addition, the appendices provide a complete collection of simulation results of the proposed micropower op amp with different frequency compensation schemes.

Chapter 2 Input Stage

This chapter examines a number of common input stages and explains how the input stage design is shaped by the constraints from specification. It first reasons why the PMOS input pair is chosen over the NMOS one. The related constraints, namely input common-mode range, DC open-loop gain, and input offset voltage, are then discussed in the design context. The input common-mode range requirement sketches the preliminary topology of the input stage. The final architecture is the result of the open-loop gain restriction. Lastly, the input offset voltage constraint instructs how the transistors have to be sized.

Consideration of Transistor Type in Input Stage

One of the primary reasons that PMOS transistors are chosen for the input stage is the fact that its input common-mode range includes ground for single-supply operation [6]. There are a number of other benefits for having PMOS transistors as the input stage rather than NMOS transistors [7]. First, PMOS transistors have less 1/f noise. Second, a PMOS input stage results in a higher slew rate than an NMOS one.

The following sections explain the design details of input stage based on the consideration of the related constraints: input common-mode range, DC open-loop gain, and input offset voltage.

2.1 Constraint 1: Input Common-Mode Range

One of the primary specifications of the op amp in design is to have the input common-mode range that includes ground for single-supply operation as well as mid-supply voltage for dual-supply operation. This section discusses different input stage architectures and reasons why the single-ended folded-cascode configuration is used as the input stage in the proposed micropower op amp.

Most op amps employ one of the following common topologies or their variants as the input stage: single-ended or fully differential basic input stage, or single-ended or

fully differential folded-cascode input stage. The four common topologies are shown in Figure 2-1, Figure 2-2, Figure 2-3, and Figure 2-4 respectively [8]-[10].

The basic input stage in Figure 2-1 has the maximum common-mode input of V_{DD} - $(V_{SGP} + V_{DS,SAT})$, which is high enough to accommodate mid-supply inputs for dual-supply applications. However, its common-mode range cannot go down to ground for single-supply operation, and therefore does not meet the requirement. The lowest of the input range is only V_{GSN} - V_{SGP} + $V_{DS,SAT}$, which amounts to be approximately $1V_{DS,SAT}$ to $2V_{DS,SAT}$ above the ground (In general, $V_{GSN} > V_{SGP}$ because the input pair is usually weakly inverted due to its large width, but the current mirror transistors are strongly inverted).

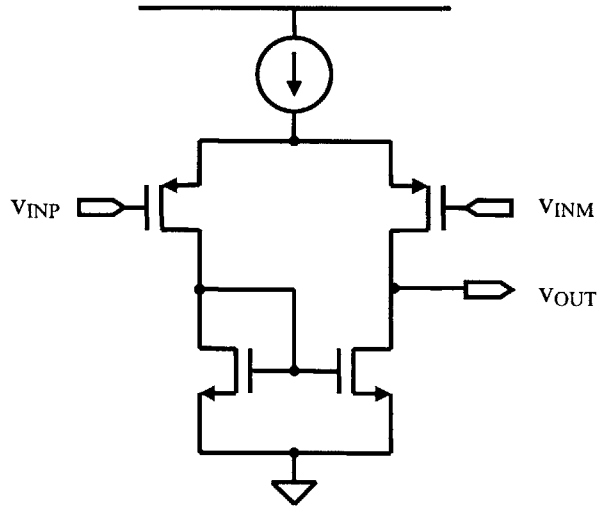


Figure 2-1: Basic Input Stage

The basic input stage may also be implemented as a fully differential architecture shown in Figure 2-2, simplified from [8]. Its common-mode input level can go up to V_{DD} - V_{SGP} - $V_{DS,SAT}$ (same as that of Figure 2-1) and can go down beyond the ground to as low as $2V_{DS,SAT}$ - V_{SGP}. Although it satisfies the input common-mode range specification, it requires a common-mode control circuit, which in turn increases power dissipation in the op amp. The second stage must also have differential inputs, which increases the power dissipation even more. These extra implementation costs are its disadvantages, especially for the op amp in design in which the total supply current has to be minimized.

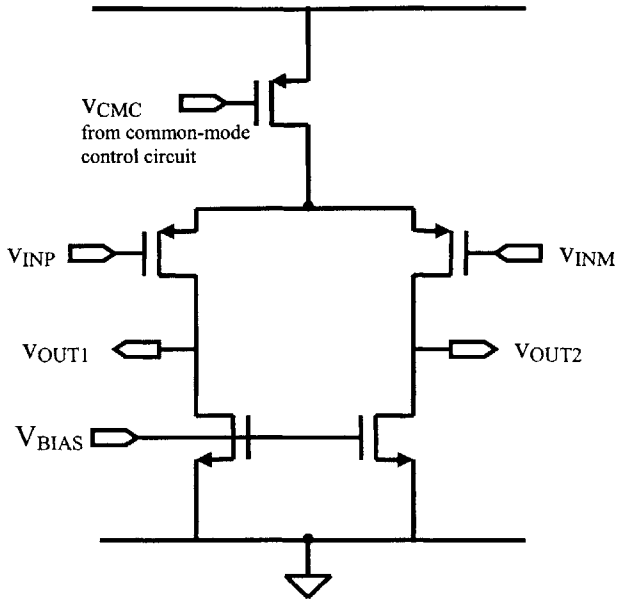


Figure 2-2: Fully Differential Basic Input Stage [8]

The folded-cascode topology in Figure 2-3, adapted from [9] to have the PMOS input pair, has the same input common-mode range as the fully differential basic input stage in Figure 2-2. Therefore, it satisfies the requirement. In addition, its input common-mode range remains the same if a cascode current mirror or a wide-swing current mirror is used instead of the simple current mirror shown in the schematic. The only drawback is it consumes more current than the basic input stage for the same tail current to implement the folded section. However, a wider input common-mode range that includes ground for single-supply operation is more important. The input stage of the proposed micropower op amp is based on this topology.

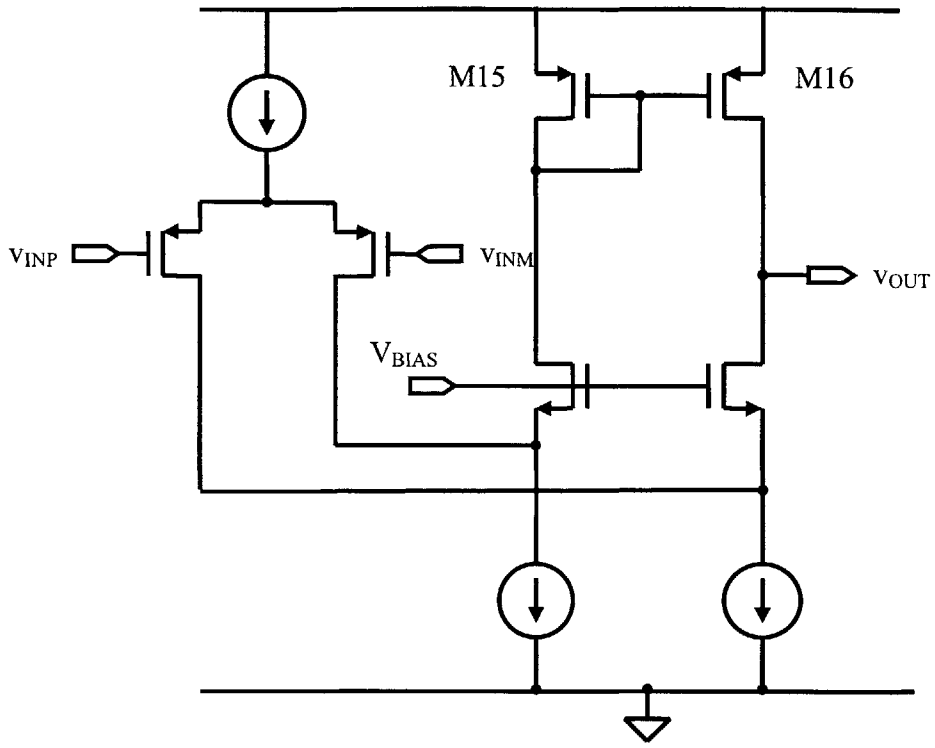


Figure 2-3: Folded-Cascode Input Stage (adapted from [9] to have the PMOS input pair)

The differential form of the folded-cascode input stage is shown in Figure 2-4 [9]. This topology has the same additional implementation need as the differential basic input stage, and therefore is not appropriate for the author's design. Other input stage topologies explored include the complementary input stage in [21]. It allows rail-to-rail inputs. However, it needs a transductance control circuit to ensure that the input stage has a constant transconductance across all the input range. This additional requirement increases design complexity and results in more power consumption. Therefore, the complementary input stage is not selected for the proposed micropower op amp.

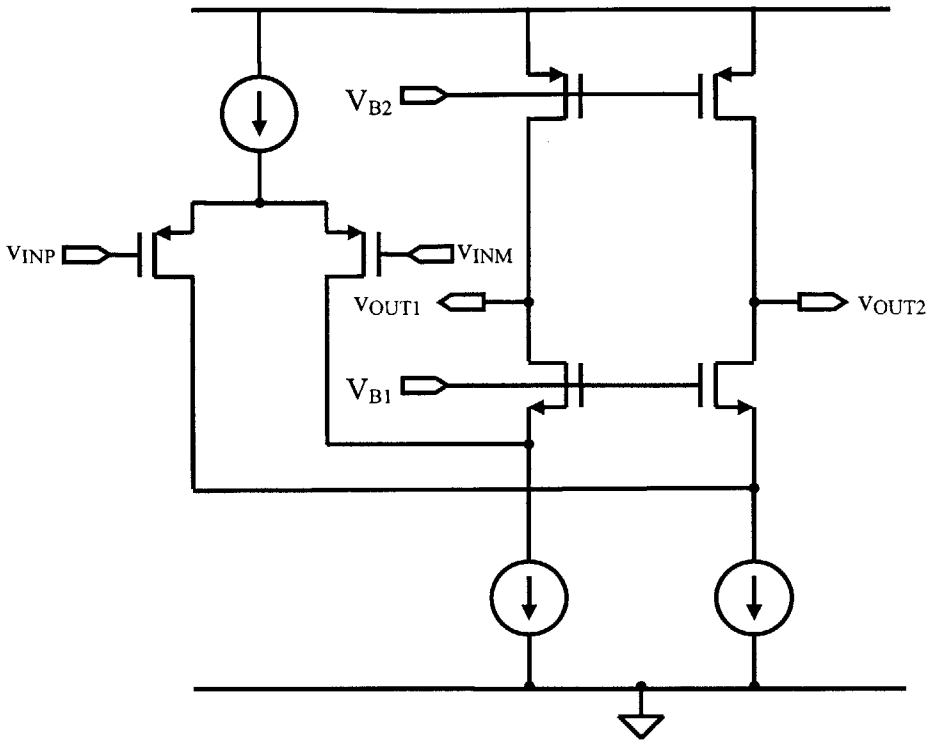


Figure 2-4: Fully Differential Folded-Cascode Input Stage [9]

2.2 Constraint 2: Large DC Open-Loop Gain

The specified DC open-loop gain is at least 100dB. This high DC open-loop gain is one of the design goals because the op amp has to support many applications that require very large gains at low frequencies. These applications include gas sensors and other transducers such as thermocouples, bridges, hall-effect sensors and photodiodes [10]. This high gain characteristic is not easy to achieve in a two-stage op amp.

The simple current mirror in the chosen folded-cascode input stage in Figure 2-3 has low output resistance, compared to Wilson current mirrors and cascode current mirrors, and thus making it more difficult to meet the required DC open-loop gain. In addition, V_{DS} of M16 in the simple current mirror changes with the operating supply voltage and the bias of the output stage, and thus undesirably causing the bias current in M16 to slightly vary upon those condition changes.

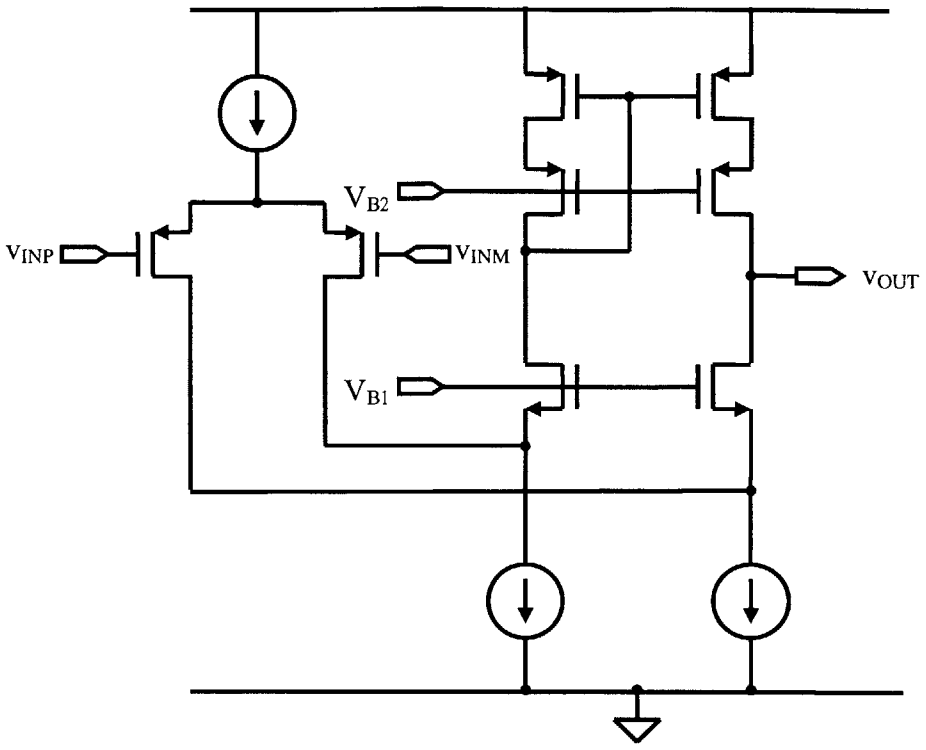


Figure 2-5: Input Stage of the Proposed Micropower Op Amp

The wide-swing current mirror [9] is chosen for the input stage of the proposed op amp as shown in Figure 2-5. It has high output resistance and has the highest bandwidth per drain current ratio after the basic Wilson mirror and the improved Wilson mirror [11]. In addition, the wide-swing current mirror can operate with voltage down to $2V_{SD,SAT}$ across its output side, unlike both forms of Wilson current mirrors and the cascode current mirror that require at least $V_{SG} + V_{SD,SAT}$ across the output side to operate properly, i.e. the transistors stay in the saturation region. With the increased output impedance of the current mirror, the op amp not only has a higher DC gain, but also higher CMRR and PSRR [10].

2.3 Constraint 3: Input Offset Voltage

The input offset voltage comes from two sources. They are systematic offset voltage and random offset voltage [12], [13]. The systematic offset voltage is caused by asymmetry in the op amp architecture. The random offset voltage is the consequence of mismatches in transistor pairs such as the differential input pair. The contribution of the

random offset voltage on the total offset voltage is more significant than that of the systematic offset voltage when the first stage gain is large. This condition is particularly true in the author's design in which most of the op amp gain is from the input stage. (Simulation results show the input stage gain is on the order of 10^4 in the proposed op amp). As a result, only the random offset voltage will be considered in this section.

Transistor pair mismatch comes from the difference in their threshold voltage V_T and current factor β [14]. In general, the variation in the threshold voltage and current factor becomes less as the transistor area increases. The following calculation of input offset voltage for transistor sizing is based on the model in [14] and [15]. The standard deviation of the threshold voltage difference ΔV_T is described by

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{WL}}$$

where A_{VT} is a constant depending on the process technology (usually less for smaller processes)

(2-1)

The standard deviation of the relative current factor difference $\frac{\Delta\beta}{\beta}$ is described by

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}}$$

where A_β is a constant depending on the process technology

(2-2)

According to [14], the variance of the gate-source voltage difference in a transistor pair with the same drain current can be described as

$$\sigma^2(V_{OS}) = \frac{1}{WL}\left[A_{VT}{}^2 + \frac{(V_{GS} - V_T)}{4} A_\beta{}^2\right]$$

where V_{OS} is the offset voltage (or gate - source voltage difference of a transistor pair)

(2-3)

Equation (2-3) implies the effect of the current factor mismatch reduces as the overdrive voltage decreases. In almost all circumstances, the threshold mismatch dominates the offset voltage. For a 0.7μm CMOS technology, the effect of the threshold mismatch is more significant than the current factor mismatch for overdrive less than 1.4V [14]. In

the author's design where the total supply current is under 20μA, most transistor pairs are weakly or moderately inverted. Therefore, the offset voltage can be estimated by only considering the component due to threshold mismatch as

$$\sigma^2(V_{OS}) \approx \frac{A_{VT}^{\ 2}}{WL} \tag{2-4}$$

This following section explains transistor sizing and input offset voltage consideration.

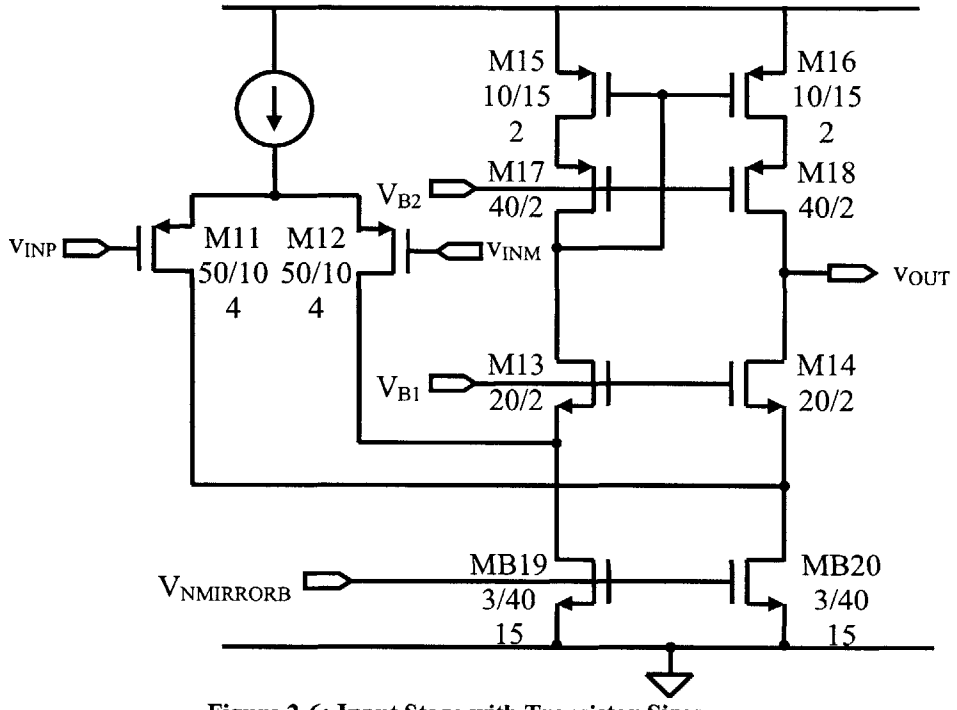


Figure 2-6: Input Stage with Transistor Sizes

The input stage with transistor sizes is depicted in Figure 2-6. The input referred offset voltage is the result of the mismatch in the following 3 transistor pairs: M11-M12, M15-M16, and MB19-MB20. Transistor pairs M17-M18 and M13-M14 do not affect the input offset voltage. It is also not necessary to consider the offset voltage due to any mismatch in the output stage because that offset voltage is divided by the gain of the input stage when referred to the input [10], [14].

The micropower op amp is specified to have an untrimmed input offset voltage of less than 5mV. In order to achieve good yields in IC production, the transistors are sized

such that three standard deviations of input offset voltage is less than 5mV. This condition corresponds to yielding 99.7% of fabricated ICs having untrimmed input offset voltage within +/- 5mV [16]. The transistor sizes in the final input stage design in Figure 2-6 evolve from preliminary hand calculation and simulation. The differential input pair is sized to be very wide for two main reasons. The first goal is to make the input pair having the highest transconductance g_m, compared to other transistor pairs in the input stage, so that the offset voltage due to the other pairs is attenuated as implied by (2-6). The other intention is to keep its gate-source voltage small so that the input common-mode range is increased. For the wide-swing current mirror, transistor pair M15-M16 is sized to be long to get high output impedance. The cascode transistor pair M17-M18 of the mirror is sized to be wide to have high transconductance [10]. The following calculation shows the course of preliminary hand calculation of input offset voltage using the final transistor sizes.

Require $3\sigma(V_{OS}) < 5\text{mV}$

$$\sigma(V_{OS}) < \frac{5}{3}\text{mV} \tag{2-5}$$

From the input stage in Figure 2 - 6,

$$\sigma(V_{OS}) = \sqrt{{\sigma_{11}}^2 + \left(\frac{g_{m15}}{g_{m11}}\right){\sigma_{15}}^2 + \left(\frac{g_{mB19}}{g_{m11}}\right){\sigma_{B19}}^2} \tag{2-6}$$

From (2-6), the transconductance ratio $\left(\frac{g_{m15}}{g_{m11}}\right)$ and $\left(\frac{g_{mB19}}{g_{m11}}\right)$ will be made to be one to simplify the calculation. Hence, the calculated offset voltage will be an overestimate.

$$\sigma(V_{OS}) = \sqrt{{\sigma_{11}}^2 + {\sigma_{15}}^2 + {\sigma_{B19}}^2} \tag{2-7}$$

For 0.7μm CMOS technology [14][4],

$A_{VTP} = 22\text{mV} \cdot \mu\text{m}$

$A_{VTN} = 13\text{mV} \cdot \mu\text{m}$

$$\sigma_{11}^{2}(\Delta V_{GS}) = \frac{A_{VTP}^{2}}{(WL)_{11}} = \frac{(22\text{mV} \cdot \mu\text{m})^2}{[4 \cdot (50\mu\text{m}) \cdot (10\mu\text{m})]} = 0.242\text{mV}^2$$

$$\sigma_{15}^{2}(\Delta V_{GS}) = \frac{A_{VTP}^{2}}{(WL)_{15}} = \frac{(22\text{mV} \cdot \mu\text{m})^2}{[2 \cdot (10\mu\text{m}) \cdot (15\mu\text{m})]} = 1.61\text{mV}^2$$

$$\sigma_{B19}^{2}(\Delta V_{GS}) = \frac{A_{VTN}^{2}}{(WL)_{B19}} = \frac{(13\text{mV} \cdot \mu\text{m})^2}{[15 \cdot (3\mu\text{m}) \cdot (40\mu\text{m})]} = 0.094\text{mV}^2$$

$$\sigma(V_{OS}) = \sqrt{0.242 + 1.61 + 0.094}\text{mV}$$

$$\sigma(V_{OS}) = 1.39\text{mV} < \frac{5}{3}\text{mV}$$

If the input offset voltage were not a concern, the author could size input stage transistors to be extremely small. This sizing would make the parasitic capacitances minimal, so the unity-gain frequency would be higher without any other changes. However, in practice, it is desirable for the op amp to have low input offset voltage, and the input offset voltage specification must be met. Therefore, some transistors in the input stage need to be sized to have large areas as shown in the calculation and Figure 2-6.

[4] The constant A_{VT} for 0.6μm CMOS technology was not found in literature, so the one for 0.7μm CMOS technology is used instead. This choice will result in a conservative estimate of offset voltage because this constant decreases as the process becomes smaller.

Chapter 3 Output Stage

In this chapter, the background on output stages and desired characteristics of the proposed op amp are first explored. Then, the design of the output stage employed in the proposed op amp is explained.

3.1 Output Stage Background

The output stage is needed for op amps that have to drive resistive loads or heavy capacitive loads [17]. This section presents a brief introduction on the configuration of output transistors and the classification of output stage biasing.

Configuration of Output Transistors

The arrangement of the output transistors in an output stage can be classified into two basic configurations. They are complementary source-follower and complementary common-source as shown in Figure 3-1 and Figure 3-2, respectively [18]. Since the proposed micropower op amp needs to have a rail-to-rail output stage, the complementary common-source configuration is used in the design.

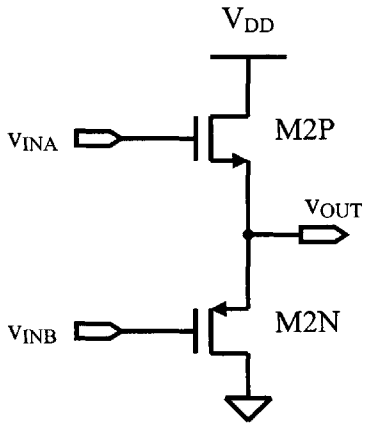


Figure 3-1: Complementary Source Follower Configuration [18]

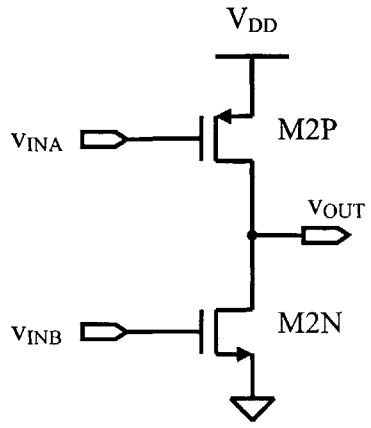


Figure 3-2: Complementary Common-Source Configuration [18]

Output Stage Biasing

The three common biasing schemes for the output stage are Class A, Class B, and Class AB. Class A output stage is easy to implement, but it dissipates power all the time and cannot source or sink current from the load more than its quiescent current value. Class B output stage saves power because it is inactive when there is no signal, but it has crossover distortion when transitioning between the active input ranges of the two devices. Class AB output stage keeps both of the output transistors on with a small amount of biasing current so it does not have the distortion problem [19]. Moreover, it can source or sink current when required by the load.

Desired Characteristics of Output Stage

The output stage of the proposed micropower op amp has to be able to swing rail-to-rail. For the biasing, the output stage should maintain relatively constant quiescent current across the operating supply voltage of 2.5V to 6.0V. Moreover, because of the output source/sink current specification, it needs to have a large ratio of the maximum sourcing/sinking current to the quiescent current. As a result, the output stage of the proposed micropower op amp is in the complementary common-source configuration and is biased by a Class AB scheme described in the next sections.

3.2 Translinear-Loop-Biased Output Stage

The biasing scheme of the proposed op amp output stage evolves from the translinear-loop-biased configuration shown in Figure 3-3. This translinear-loop-biased topology was presented in [20] and extensively investigated in [21]-[22]. It is also called the Yin-Yang output stage due to the symmetry of biasing [23]. This output stage exhibits Class AB characteristics. It can operate down to a supply voltage of $2V_{GS}$ + $2V_{DS}$ if cascode current sources are used, and down to $2V_{GS}$ + V_{DS} if simple current sources are used. In addition, this output stage topology does not add noise and offset to the op amp, provided that the two current sources biasing the bridging transistors, M23 and M26, are implemented by the existing bias currents in the input stage [21]. The signals from the input stage, v_{inA} and v_{inB}, feed directly to the gate of their respective output transistor and also feed to the other transistor through the bridging transistors, M23 and M26. While M23 and M26 actively bias the output transistors, nodes v_{INA} and v_{INB} are always of high impedance regardless of supply voltage.

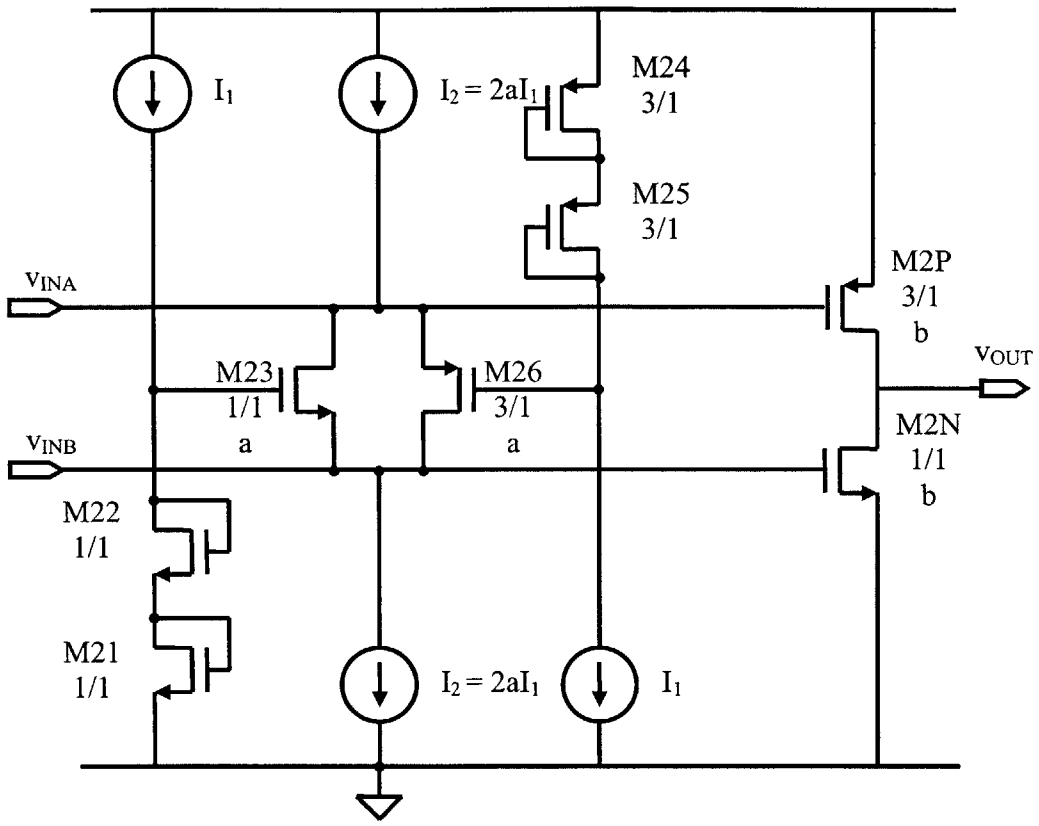


Figure 3-3: Translinear-Loop-Biased Class AB Output Stage

In the NMOS translinear loop, M23 is sized to be *a* times as wide as M21 and M22 to accommodate I_2 which is *2a* times as large as I_1. The output device M2N is sized to be *b* times as wide as M21 and M22 so that the output pair can sink and source large currents and have high g_m's. The same geometry guideline applies to the PMOS translinear loop. In addition, PMOS transistors are sized to be 3 times as wide as their NMOS counterparts because the hole mobility is approximately one third of the electron mobility. This decision is made so that PMOS transistors have the same transconductance and the same gate-source voltage as NMOS transistors under the same condition, i.e. equal bias currents [18].

Quiescent Current

When the output stage is at rest, the quiescent current can be calculated from either of the translinear loop. Consider the NMOS translinear loop M21-M22-M23-M2N, the quiescent current is determined as follows, similar to an example in [18].

From the translinear loop,

$$V_{GS21} + V_{GS22} = V_{GS23} + V_{GS2N} \tag{3-1}$$

Since $V_{GS} = V_{TN} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}}$ for NMOS transistors in saturation assuming the effect of channel length modulation is negligible.

(3-2)

$$V_{TN21} + \sqrt{\frac{2I_{D21}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{21}}} + V_{TN22} + \sqrt{\frac{2I_{D22}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{22}}} = V_{TN23} + \sqrt{\frac{2I_{D23}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{23}}} + V_{TN2N} + \sqrt{\frac{2I_{D2N}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{2N}}} \tag{3-3}$$

Since $V_{TN21} = V_{TN2N}$ and $V_{TN22} \approx V_{TN23}$

(3-4)

(Note that $V_{TN22} > V_{TN21}$. The body effect causes $V_{TN22} > V_{TN0}$ because $V_{SB22} > 0\text{V}$).

$$\sqrt{\frac{I_{D21}}{\left(\frac{W}{L}\right)_{21}}} + \sqrt{\frac{I_{D22}}{\left(\frac{W}{L}\right)_{22}}} = \sqrt{\frac{I_{D23}}{\left(\frac{W}{L}\right)_{23}}} + \sqrt{\frac{I_{D2N}}{\left(\frac{W}{L}\right)_{2N}}} \tag{3-5}$$

$$\sqrt{I_{D2N}} = \sqrt{\left(\frac{W}{L}\right)_{2N}}\left[\sqrt{\frac{I_{D21}}{\left(\frac{W}{L}\right)_{21}}} + \sqrt{\frac{I_{D22}}{\left(\frac{W}{L}\right)_{22}}} - \sqrt{\frac{I_{D23}}{\left(\frac{W}{L}\right)_{23}}}\right] \tag{3-6}$$

$$I_{D2N} = \left(\frac{W}{L}\right)_{2N}\left[\sqrt{\frac{I_{D21}}{\left(\frac{W}{L}\right)_{21}}} + \sqrt{\frac{I_{D22}}{\left(\frac{W}{L}\right)_{22}}} - \sqrt{\frac{I_{D23}}{\left(\frac{W}{L}\right)_{23}}}\right]^2 \tag{3-7}$$

$$I_{D2N} = \frac{\left(\frac{W}{L}\right)_{2N}}{\left(\frac{W}{L}\right)_{21}}\left[\sqrt{I_{D21}} + \sqrt{I_{D22}} - \sqrt{\frac{I_{D23}}{a}}\right]^2$$

(3-8)

In the quiescent state, half of I_2 flows through M23 and the other half goes through M26.

$$I_Q = I_{D2N} = b\left[2\sqrt{I_1} - \sqrt{\frac{\frac{I_2}{2}}{a}}\right]^2$$

(3-9)

Since $I_2 = 2aI_1$

(3-10)

$$\boxed{I_Q = I_{D2N} = bI_1}$$

(3-11)

The conclusion is the same for the PMOS translinear loop because of the symmetry. The actual quiescent current may slightly differ from (3-11) from two causes. The first one is all the transistors do not have the same V_{DS}'s, but the effect of channel length modulation is ignored in the derivation. The other error source contributes to the deviation from calculation if the transistors are not well in strong inversion. This deviation is particularly true in the author's design because the currents of the translinear transistors (except the output pair) are only in the range of 0.2 – 2.0μA. Although the transistors have $V_{GS} > V_{TN}$, their overdrive voltages are less than 50mV, and thus operate in moderate inversion. From the simulation of one of the proposed op amps in Figure 3-6, the quiescent current is found to be within 11% of the calculated value, i.e. the simulated quiescent current is 8.33μA at $V_{DD} = 2.5$V while the calculated value is 9.85μA.

As far as the current allocation is concerned, the total supply current should be invested in the output pair transistors as much as possible so that the output stage transconductance, g_{m2}, is high. This design choice is made in order to put the op amp's second pole location as high as possible. However, the remaining current has to be enough for the first stage for two reasons. One is the tail current of the differential pair

input cannot be too small, otherwise the slew rate is too low. The other need is the summing current mirror in the input stage has to be high enough so that the mirror pole does not affect the op amp frequency response near the crossover point. In the proposed op amps, the author distributes approximately half of the total current in the output pair transistors, and verifies by simulation that the current left for the first stage after the bias cell and the biasing of the output stage is sufficient.

Minimum Current in Output Transistors

When the load requires the op amp to source or sink current, one of the output pair transistors is driven hard while the other is retained active with a small bias current. For example, if the load draws current from the output stage, V_{SG2P} increases to allow more drain current in M2P. As a result, V_{SG26} reduces, following the translinear relation $V_{SG24} + V_{SG25} = V_{SG26} + V_{SG2P}$, because V_{SG24} and V_{SG25} are fixed by bias current I_1. Therefore, more of bias current I_2 flows through M23. When all of I_2 goes through M23, M2N is biased with the minimum current rather than turns off as in the Class B output stage.

The following calculation for the minimum current is done for M2N, but the same result also applies to M2P in the opposite scenario [18].

Consider NMOS translinear loop M21-M22-M23-M2N.

From (3-8), $I_{D2N} = \dfrac{\left(\dfrac{W}{L}\right)_{2N}}{\left(\dfrac{W}{L}\right)_{21}}\left[\sqrt{I_{D21}} + \sqrt{I_{D22}} - \sqrt{\dfrac{I_{D23}}{a}}\right]$

The minimum current in M2N occurs when all I_2 goes through M23.

$$I_{MIN} = I_{D2N} = b\left(2\sqrt{I_1} - \sqrt{2I_1}\right)^2 \tag{3-12}$$

$$I_{MIN} = I_{D2N} = (2-\sqrt{2})^2 bI_1 \tag{3-13}$$

Since $I_Q = bI_1$

$$\boxed{I_{MIN} = I_{D2N} = \left(2-\sqrt{2}\right)^2 I_Q}$$

(3-14)

$$I_{MIN} = I_{D2N} = 0.343I_Q$$

In this proposed micropower op amp, the minimum current in the output transistors is close to $0.46I_Q$ according to the simulation result in Figure 3-7. This difference from the calculation is caused by the fact that the transistors in the translinear loops are in moderate inversion because of very low bias currents.

Maximum Current in Output Transistors

The maximum current is defined to be the maximum current that one of the output transistors is capable of sourcing/sinking current while the other output transistor is biased with the minimum current (rather than being turned off). To continue the analysis from the minimum current section, the following absolute maximum current calculation is performed for M2P [18], [23]. Again, the same result applies to M2N as well.

When M2N is biased at the minimum current, all of I_2 flows through M23. V_{G2P} is pulled down to V_{G2N} by M23, and it can be pulled down to be as low as V_{G2N} + $V_{DS,SAT23}$ at most (to allow M23 to remain in saturation). The lowest gate voltage of M2P is described by the following equation.

$$V_{GS21} + V_{GS22} - V_{GS23} + V_{DS,SAT23} = V_{G2P}$$

(3-15)

Under this condition, V_{SG2P} is the largest and M2P conducts the maximum current. The source-gate voltage of M2P can be expressed as.

$$V_{SG2P} = V_{DD} - \left(V_{GS21} + V_{GS22} - V_{GS23} + V_{DS,SAT23}\right)$$

(3-16)

Rewrite V_{SG} and V_{GS} in terms of V_{TP}, V_{TN}, and I_D.

$$-V_{TP2P} + \sqrt{\frac{2(-I_{D2P})}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{2P}}} =$$

$$V_{DD}-\left(V_{TN21}+\sqrt{\frac{2I_{D21}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{21}}}+V_{TN22}+\sqrt{\frac{2I_{D22}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{22}}}-V_{TN23}-\sqrt{\frac{2I_{D23}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{23}}}+V_{DS,SAT23}\right) \tag{3-17}$$

Since $V_{TN22}=V_{TN23}$

$$-V_{TP2P}+\sqrt{\frac{2(-I_{D2P})}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{2P}}}=$$

$$V_{DD}-\left(V_{TN21}+\sqrt{\frac{2I_{D21}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{21}}}+\sqrt{\frac{2I_{D22}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{22}}}-\sqrt{\frac{2I_{D23}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{23}}}+V_{DS,SAT23}\right) \tag{3-18}$$

$$\sqrt{\frac{2(-I_{D2P})}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{2P}}}=$$

$$V_{DD}+V_{TP2P}-V_{TN21}-V_{DS,SAT23}-\left(\sqrt{\frac{2I_{D21}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{21}}}+\sqrt{\frac{2I_{D22}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{22}}}-\sqrt{\frac{2I_{D23}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{23}}}\right) \tag{3-19}$$

Use the approximation,

$$\mu_p C_{ox}=\frac{1}{3}\mu_n C_{ox}$$

$$\sqrt{2(-I_{D2P})}=\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_{2P}}\left(V_{DD}+V_{TP2P}-V_{TN21}-V_{DS,SAT23}\right)-\left(\sqrt{2bI_{D21}}+\sqrt{2bI_{D22}}-\sqrt{\frac{2bI_{D23}}{a}}\right) \tag{3-20}$$

$$\sqrt{2(-I_{D2P})}=\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_{2P}}\left(V_{DD}+V_{TP2P}-V_{TN21}-V_{DS,SAT23}\right)-\left(2\sqrt{2bI_1}-\sqrt{\frac{2b(2aI_1)}{a}}\right) \tag{3-21}$$

$$I_{MAX} = -I_{D2P} = \frac{1}{2}\left[\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_{2P}}\left(V_{DD} + V_{TP2P} - V_{TN21} - V_{DS,SAT23}\right) - \left(2\sqrt{2bI_1} - 2\sqrt{bI_1}\right)\right]^2 \quad (3\text{-}22)$$

$$I_{MAX} = -I_{D2P} = \frac{1}{2}\left[\sqrt{\mu_p C_{ox}\left(\frac{W}{L}\right)_{2P}}\left(V_{DD} + V_{TP2P} - V_{TN21} - V_{DS,SAT23}\right) - 2\sqrt{bI_1}\left(\sqrt{2} - 1\right)\right]^2 \quad (3\text{-}23)$$

For the following parameter values,

$V_{DD} = 2.5$V

$V_{TP2P} = -0.9$V (typical value from [24])

$V_{TN21} = 0.8$V (typical value from [24])

$I_1 = 0.2\mu$A

$a = 5$, and $b = 50$

and $V_{DS,SAT23}$ is approximated to be 0.1V (because it is moderately inverted). The maximum current, I_{MAX}, calculated from (3-23) is found to be 0.98mA while the simulated I_{MAX} is approximately 1.1mA as shown in Figure 3-7. At this point, the minimum bias current in M2N is down to approximately 3μA. This result indicates that the ratio of the maximum current to the quiescent current is 133.

As (3-23) implies, the maximum current increases as the supply voltage goes up. The derivation also applies to the case when M2N conducts I_{MAX} and M2P is biased with I_{MIN}.

Variation of Quiescent Current over Supply Voltage Range

The translinear-loop-biased topology in Figure 3-3 is a robust Class AB output stage, but it has a minor problem. The output pair quiescent current increases as the supply voltage increases. This variation is due to the effect of the channel-length modulation. Consider the NMOS translinear loop, M21-M22-M23-M2N, M21 and M22 have the same V_{DS} regardless of the supply voltages because their gate and drain are connected together. However, V_{DS23} and V_{DS2N} become larger as the supply voltage increases. For M23, as V_{DS23} goes up with supply voltage but the bias current is the same, V_{GS23} becomes slightly smaller. As a result, V_{GS2N} is slightly larger at a higher supply

voltage because the available voltage for M23 and M2N, which is set up by M21 and M22 is the same. Together with the increase in V_{DS}, M2N conducts more quiescent current at higher supply voltages. The same observation is also true for the PMOS translinear loop. The simulation in Figure 3-4 shows as much as 47% increase in I_Q when V_{DD} goes up from 2.5V to 6.0V.

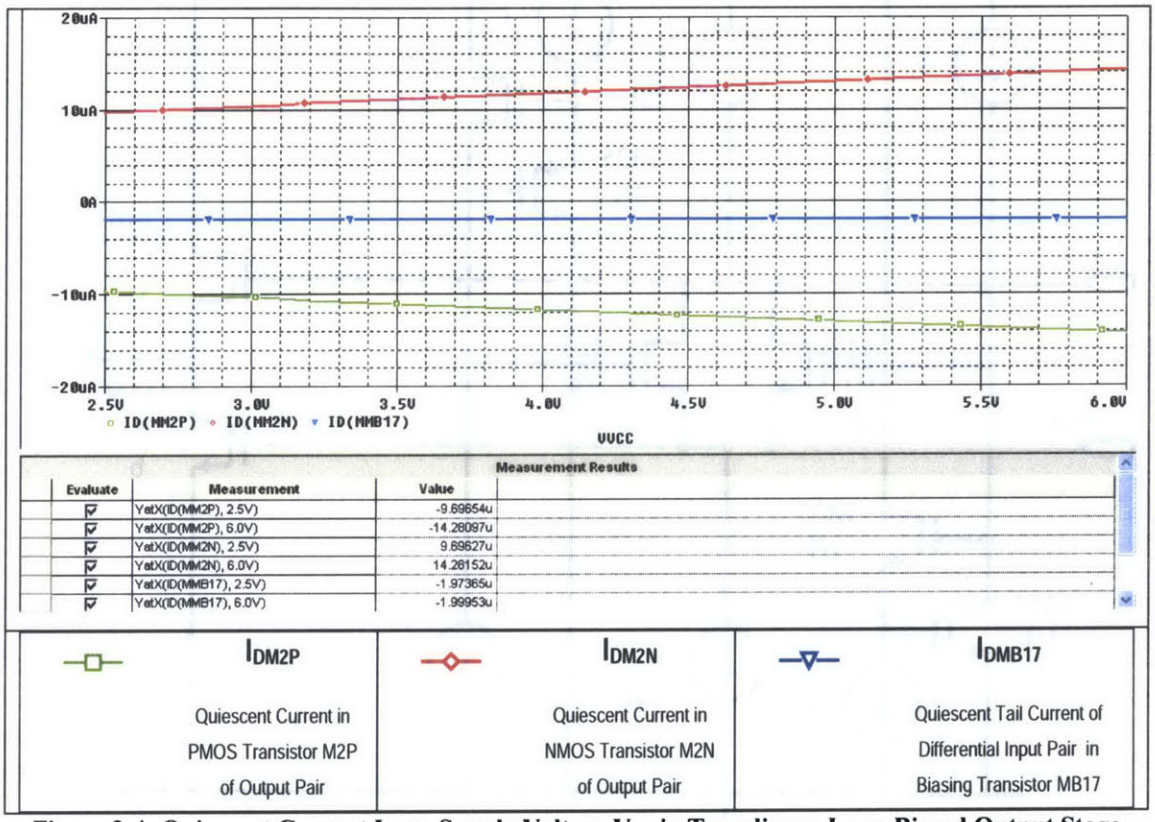


Figure 3-4: Quiescent Current I_Q vs. Supply Voltage V_{DD} in Translinear-Loop-Biased Output Stage

3.3 Modified Translinear-Loop-Biased Output Stage

The modified configuration shown in Figure 3-5 mitigates the variation in the quiescent current over the supply voltage change. It is the topology used in the proposed micropower op amp. This modified biasing scheme alleviates the change in I_Q at a small cost of extra bias currents.

The variation in I_Q is reduced by allowing V_{DS22} and V_{SD25} to increase with the supply voltage [23]. V_{GS22} and V_{SG25} then become slightly lower as the supply voltage increases, thereby leaving less voltage available for M23 and M2N, and M25 and M2P,

respectively. This effect counters the increase in V_{DS23} and V_{SD26}, and thus keeps V_{GS2N} and V_{SG2P} more constant over the supply voltage change. The simulation result in Figure 3-6 shows the variation in I_Q is down to only 20% with the supply voltage change from 2.5V to 6.0V.

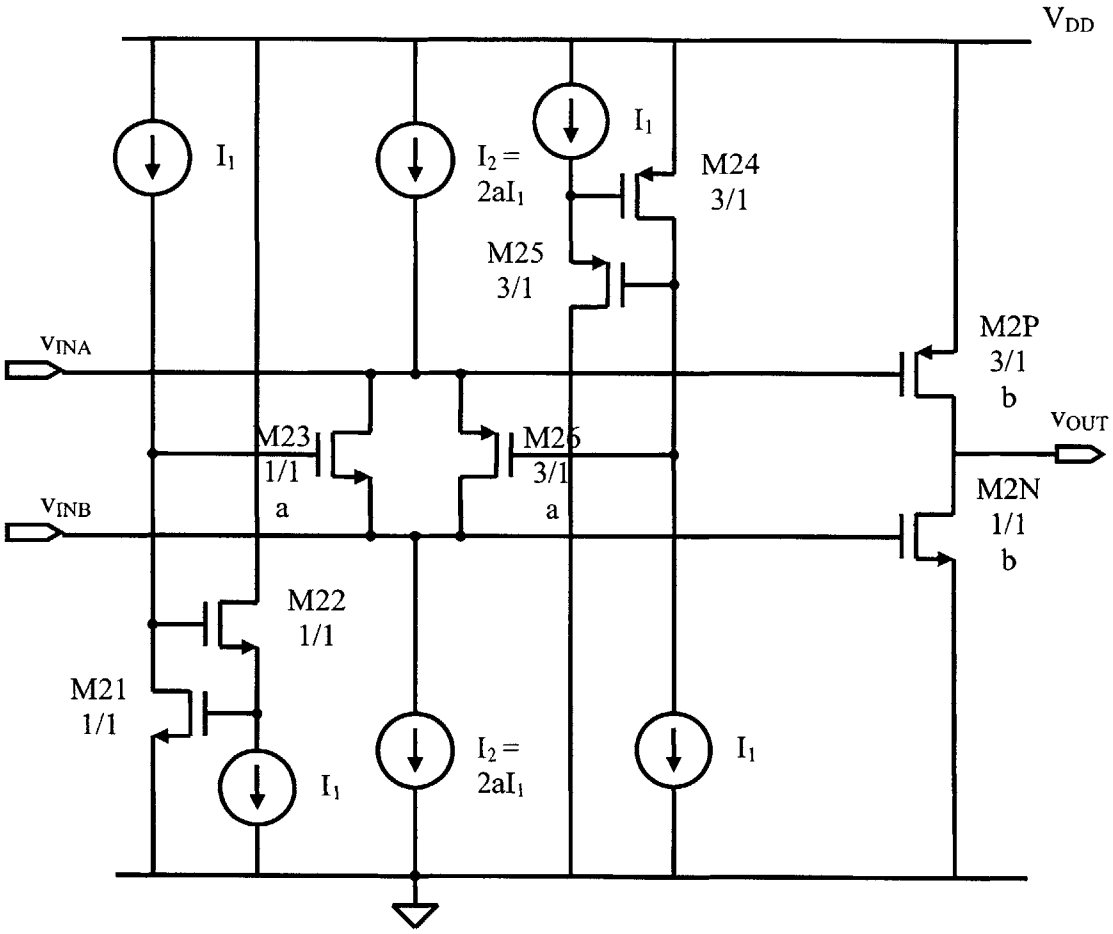


Figure 3-5: Modified Translinear-Loop-Biased Class AB Output Stage

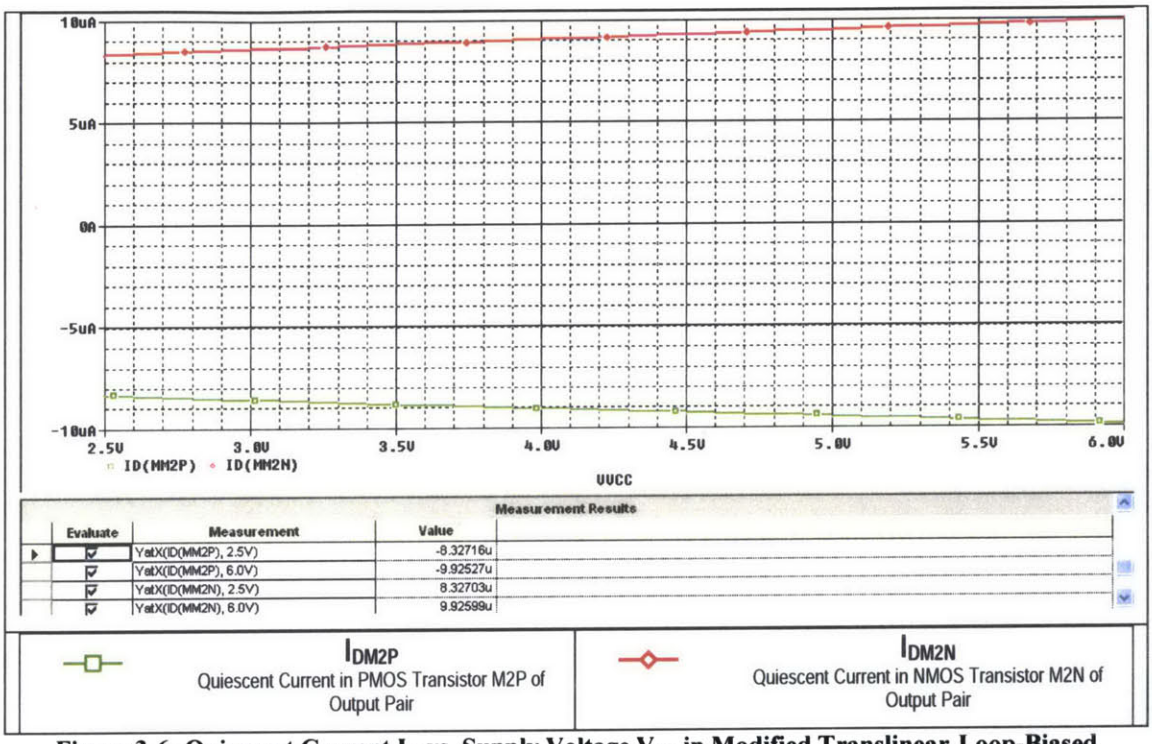


Figure 3-6: Quiescent Current I_Q vs. Supply Voltage V_{DD} in Modified Translinear-Loop-Biased Output Stage

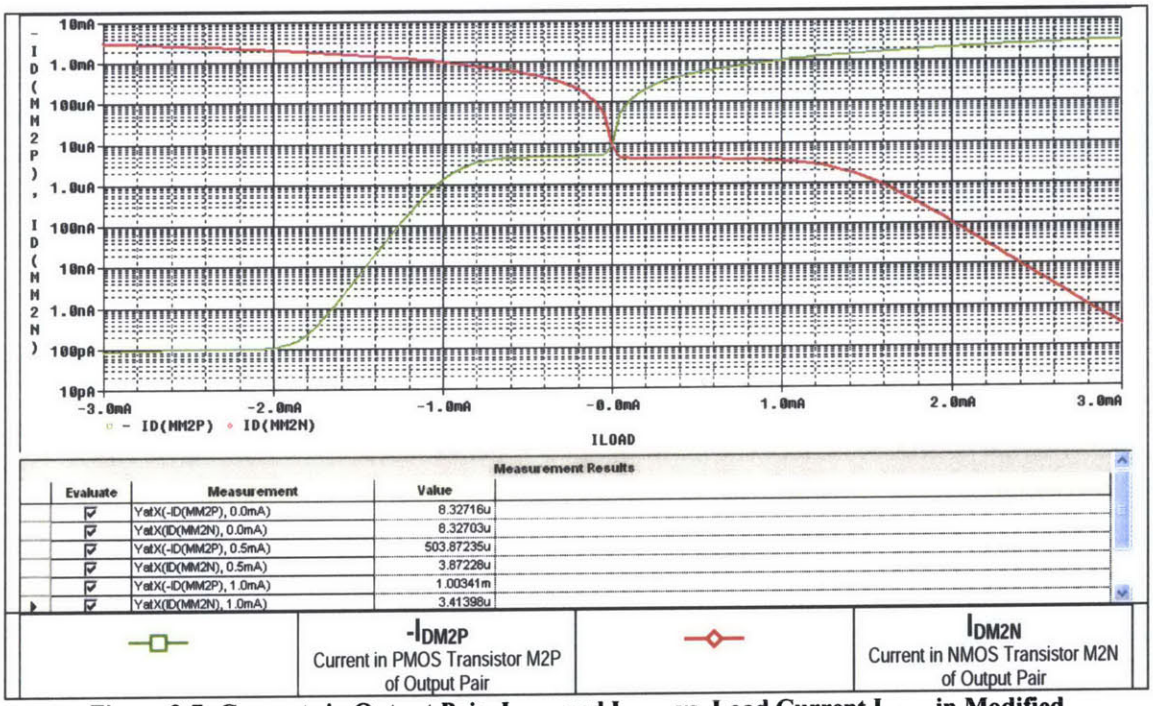


Figure 3-7: Currents in Output Pair, I_{DM2P} and I_{DM2N} vs. Load Current I_{LOAD} in Modified Translinear-Loop-Biased Output Stage

Chapter 4 Bias Cell

This chapter demonstrates the design of the bias cell used in the proposed op amp. It explains how the reference current and reference voltages are generated and passed on to the op amp. The need and the implementation of the start-up circuit in the bias cell are also explained.

4.1 Reference Current in Bias Core

The bias cell core is implemented by the bipolar Widlar current source in Figure 4-1 [25], [26]. Transistor QB2's emitter area is N times as large as that of transistor QB1. In this design, N is chosen to be 5, which is the minimum of emitter area ratio normally used. The reference current is generated by the base emitter voltage difference between QB1 and QB2 across resistor R_B. Note that transistors QB1 is in the forward active region because QB1 is diode-connected. At the minimum supply voltage of 2.5V, QB2 is also in the forward active region because $V_{CEB2} = V_{DD} - V_{SGMB2} - I_{REF}R_B$, which is greater than $V_{CE,SAT}$ if the V_{SGMB2} and the drop across R_B are not too high.

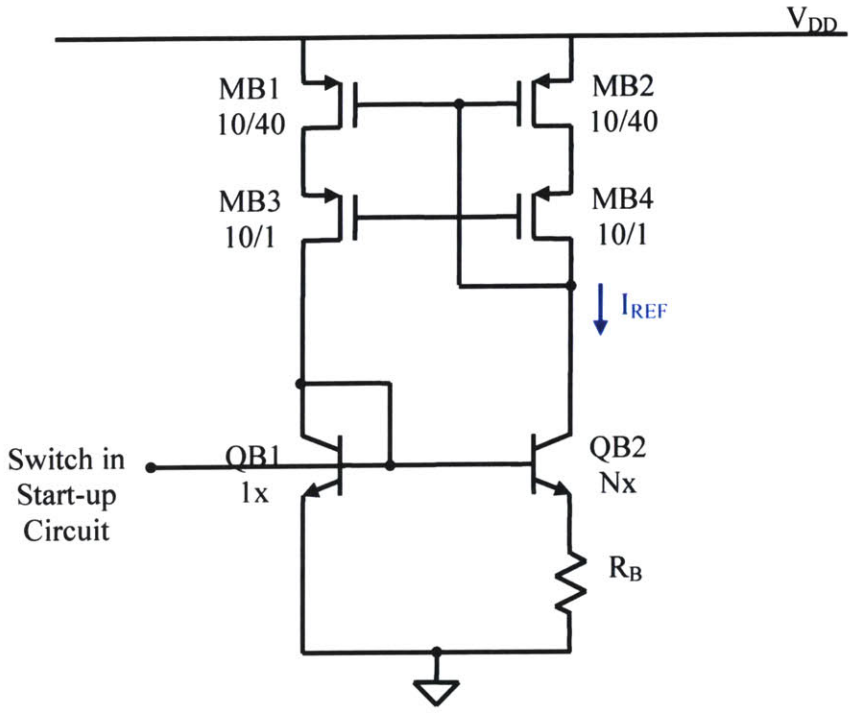


Figure 4-1: Bias Core Generating Reference Current [25], [26]

The reference current, I_{REF}, can be determined by starting from the KVL equation of the QB1-QB2-R_B loop, as presented in [26].

$$V_{BE1} - V_{BE2} - \frac{\beta_F + 1}{\beta_F} I_{REF} R_B = 0 \tag{4-1}$$

Find V_{BE} in terms of I_C.

Since $I_C = I_S\left(1 + \frac{V_{CE}}{V_A}\right)e^{\frac{V_{BE}}{V_T}}$, and assume $V_A >> V_{CE}$ [27]

(4-2)

$$I_C = I_S e^{\left(\frac{V_{BE}}{V_T}\right)}, \text{where } V_T = 26\text{mV at 300K} \tag{4-3}$$

$$\text{Therefore, } V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right) \tag{4-4}$$

$$V_T \ln\frac{I_{C1}}{I_{S1}} - V_T \ln\frac{I_{REF}}{I_{S2}} - \frac{\beta_F + 1}{\beta_F} I_{REF} R_B = 0$$

(4-5)

Since $\beta_F >> 1$, $\frac{\beta_F + 1}{\beta_F} \approx 1$

(4-6)

$$V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{REF}}{I_{S2}} - I_{REF} R_B = 0$$

(4-7)

$$V_T \ln \frac{N I_{C1}}{I_{REF}} - I_{REF} R_B = 0$$

(4-8)

$$\boxed{I_{REF} = \frac{V_T}{R_B} \ln N}$$

(4-9)

This result implies the bias cell's ability to provide a constant reference current under process variation. From (4-9), the mismatch in the emitter area ratio ΔN from process shifts is reduced to $ln(\Delta N)$. Hence, the remaining source for error is the resistor R_B value (± 25% maximum) which can be reduced by adding a trimming resistor [25]. The current mirror transistors are sized to have the width of 10μm and the length of 40μm so that they have a reasonable area and the mismatch is minimal.

4.2 Start-Up Circuit

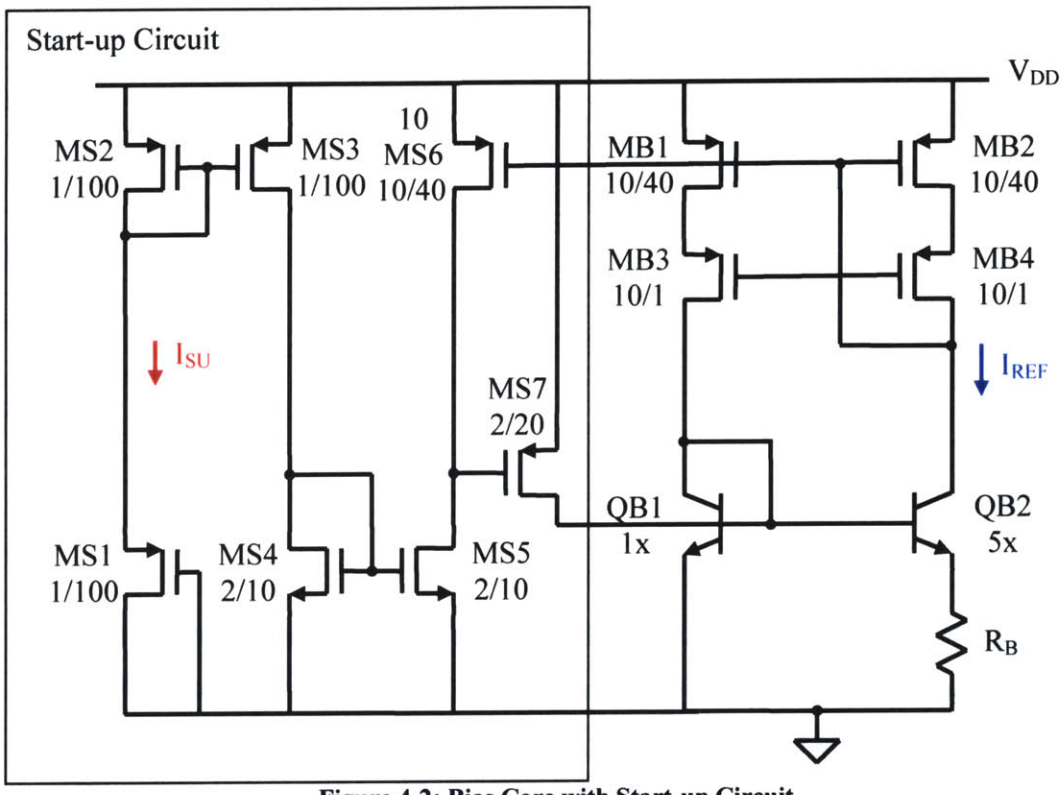


Figure 4-2: Bias Core with Start-up Circuit

The bias core has two stable points: one with $I_{C1} = I_{C2} = 0$, the other with $I_{C1} = I_{C2} = I_{REF}$. Without the start-up circuit, V_B of transistors QB1 and QB2 could be at GND, and thus not generating the reference current. For the bias core to generate a reference current, the base voltage of QB1 and QB2 must be initially pulled up from the ground by a start-up circuit. A compact start-up circuit used in this op amp is shown in Figure 4-2 [25]. MS1 and MS2 are sized to be narrow and long to minimize the start-up current, I_{SU}.

The first two devices in the start-up circuit becoming active upon the power up are MS1 and MS2. The supply voltage across their gate-source voltages forces them to turn on, and thereby, MS1 and MS2 start to conduct start-up current I_{SU}. The start-up current is then mirrored to MS3-MS4, and MS5 respectively. At this moment, MS5 tries to sink current from MS6, but MS6 cannot source any current because the bias core has not been turned on. Therefore, the gate of MS7 is pulled to ground, causing MS7 to pull the bases of QB1 and QB2 up from ground and the bias core is in operation. Now, MS6

can source enough current to MS5 and turn MS7 off by pulling its gate up. Note that MS6 is sized to be 10 times as wide as MB1 and MB2 so that MS7 can be easily turned off as soon as the bias core starts to supply I_{REF}. The final current in MS6 is limited by MS5.

The start-up current, I_{SU}, can be estimated by the following. Upon the power up, MS1 and MS2 see the supply voltage across their gate-source voltages according to the relation.

$$V_{SGMS1} + V_{SGMS2} = V_{DD} \tag{4-10}$$

To simplify the calculation, the body effect on V_{TP} increase of MS1 is ignored, and the following approximation is made.

$$V_{SGMS1} \approx V_{SGMS2} \tag{4-11}$$

And thus,

$$V_{SGMS2} \approx \frac{V_{DD}}{2} \tag{4-12}$$

MS2 is in saturation because it is diode-connected. The start-up current can be approximated by

$$I_{SU} = -I_D \approx \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{SGMS2} + V_{TPMS2}\right)^2 \tag{4-13}$$

$$I_{SU} = -I_D \approx \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)\left(V_{SGMS2} + V_{TP0}\right)^2 \tag{4-14}$$

$$\boxed{I_{SU} = -I_D \approx \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)\left(\frac{V_{DD}}{2} + V_{TP0}\right)^2} \tag{4-15}$$

This approximation is an overestimate of I_{SU} because in reality $V_{SGMS1} > V_{SGMS2}$ due to the body effect.

4.3 Reference Voltages Bias Circuit

Besides the reference current generated by the bias cell, the op amp needs two reference voltages: one is the reference voltage for PMOS cascode transistors, the other is that for NMOS cascode transistors.

The circuit in Figure 4-3 shows how to set up the two reference voltages.

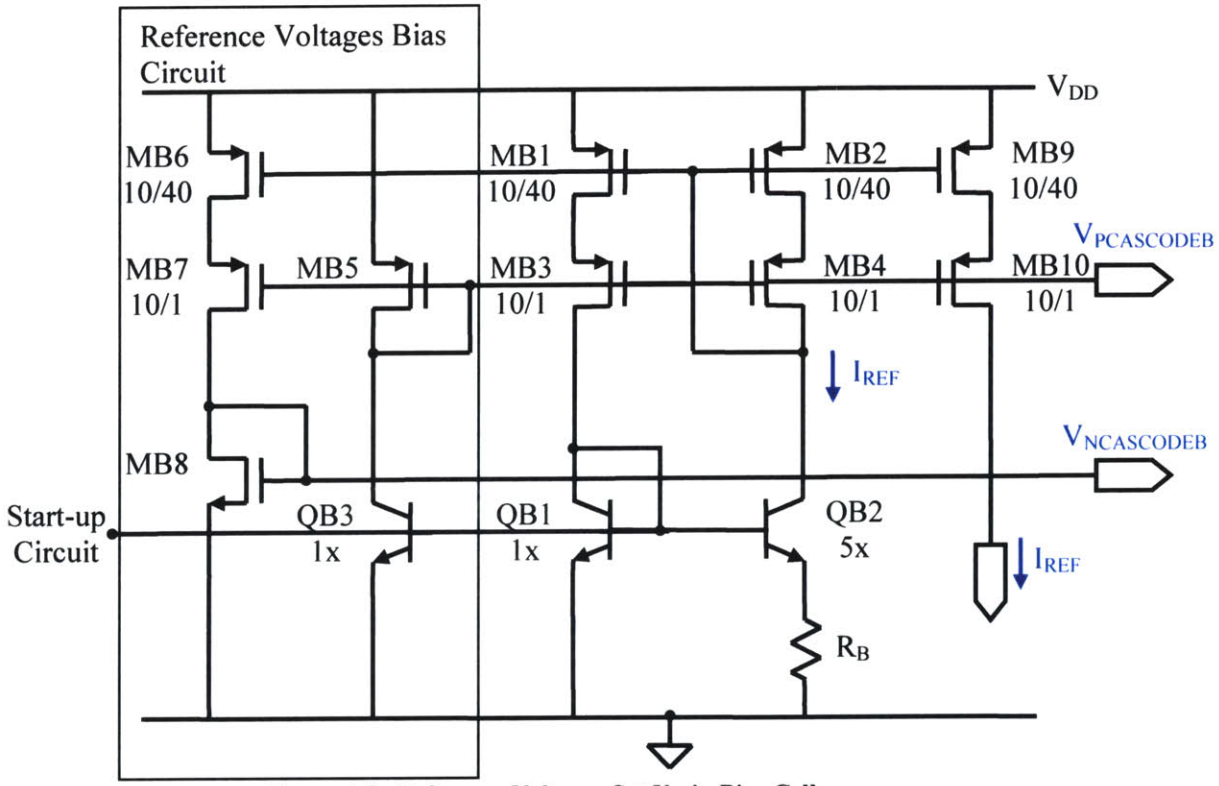


Figure 4-3: Reference Voltages Set Up in Bias Cell

MB5 sets up the reference voltage for PMOS cascode transistors, and MB8 sets up the reference voltage for NMOS cascade transistors. The voltage at the gate of MB8, $V_{NCASCODEB}$, can be determined as follows.

Transistor MB6 mirrors the reference current, I_{REF}, to MB8. Since MB8 is diode-connected, it operates in the saturation region and

$$V_{NCASCODEB} = V_{GSMB8} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)}} + V_{TN0} \tag{4-16}$$

Similarly,

$$V_{PCASCODEB} = V_{DD} - V_{SGMB5} = V_{DD} - \left(\sqrt{\frac{2I_D}{\mu_p C_{ox}\left(\frac{W}{L}\right)}} - V_{TP0} \right) \tag{4-17}$$

In the design, $V_{NCASCODEB}$ and $V_{PCASCODEB}$ are set up such that all the inner transistors of current mirrors (e.g. transistors MB1 and MB2 of current mirror MB1-MB2-MB3-MB4, for example) operate in the saturation region by having $V_{DS} > 0.4V$. Together with I_{REF}, $V_{PCASCODEB}$, and $V_{NCASCODEB}$, are passed on to the op amp.

In an IC, especially large ones, the supply voltage line and common ground line vary slightly from one corner to another. Therefore, reference current I_{REF} is fed to the op amp as a current instead of the gate voltage of MB2 to ensure the accuracy of bias currents in the op amp. In contrast, the cascode transistors' voltages, $V_{PCASCODEB}$ and $V_{NCASCODEB}$, are supplied to the op amp as voltages because their deviation from the intended value has little effect on the biasing in the op amp.

The complete bias cell is shown in Figure 4-4. The value of reference current varies as little as 3.1nA when changing from the supply voltage of 2.5V to 6.0V. Figure 4-5 show the values of I_{REF}, I_{SU}, $V_{NCASCODEB}$, and $V_{PCASCODEP}$ as a function of supply voltage V_{DD}.

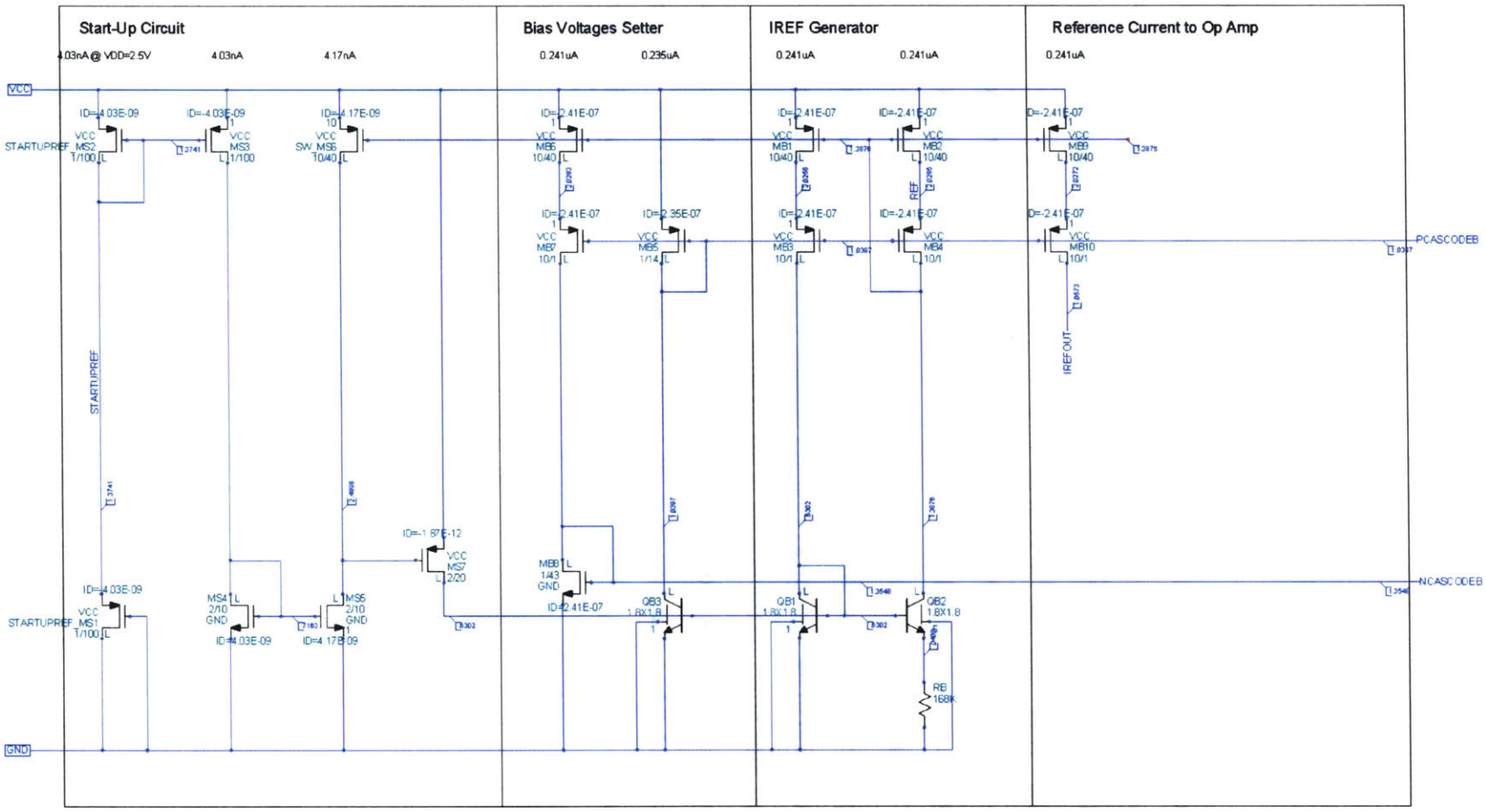
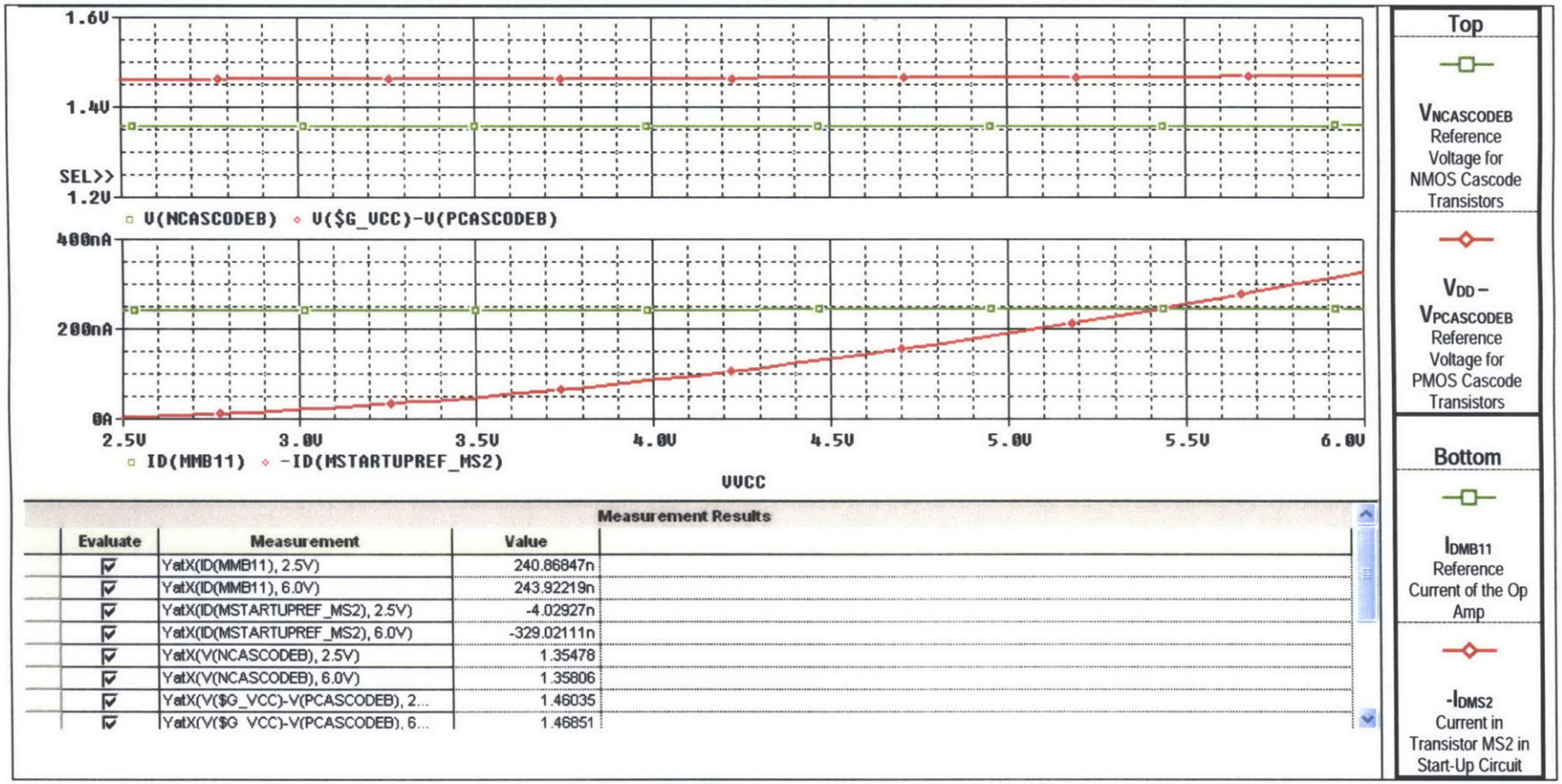


Figure 4-4: Schematic of Bias Cell



Measurement Results

Evaluate	Measurement	Value
☑	YatX(ID(MMB11), 2.5V)	240.86847n
☑	YatX(ID(MMB11), 6.0V)	243.92219n
☑	YatX(ID(MSTARTUPREF_MS2), 2.5V)	-4.02927n
☑	YatX(ID(MSTARTUPREF_MS2), 6.0V)	-329.02111n
☑	YatX(V(NCASCODEB), 2.5V)	1.35478
☑	YatX(V(NCASCODEB), 6.0V)	1.35806
☑	YatX(V($G_VCC)-V(PCASCODEB), 2...	1.46035
☑	YatX(V($G_VCC)-V(PCASCODEB), 6...	1.46851

Figure 4-5: I_{REF}, I_{SU}, $V_{NCASCODEB}$, and $V_{PCASCODEB}$ vs. V_{DD}

Chapter 5 Frequency Compensation

The previous chapters have explained the design process of the op amp and the bias cell. The remaining part to complete the micropower op amp design is the frequency compensation. This chapter briefly discusses two frequency compensation schemes. The most popular compensation scheme, simple Miller compensation, is considered first. Next, cascode compensation is explored as a potential scheme in extending the gain bandwidth product but with a defect of causing peaking in the frequency response. The combination of the previous two compensation schemes is then presented as the solution which offers moderate improvement in gain bandwidth and eliminates the peaking problem in the frequency response of the op amp.

5.1 Proposed Micropower Op Amp with Simple Miller Compensation (SMC)

The most common scheme to compensate two-stage op amps is Simple Miller Compensation (SMC) [28], [29]. The implementation is achieved by feeding the output signal back to the input of the output pair transistors through capacitors C_{C1} and C_{C2} as shown in Figure 5-1. A disadvantage of SMC is that the right half plane zero severely compromises the phase margin. This problem can be alleviated by inserting nulling resistors R_{C1} and R_{C2} in series with the existing compensation capacitors to reduce the feedforward signal. However, there is limitation on the values of the nulling resistors. As their values increase, the left half plane zero moves toward lower frequencies. Although this movement of the left half plane zero helps increase the phase margin of the op amp, it also reduces the gain margin at the same time. In the proposed op amp with simple Miller compensation, the gain margin is designed to be at least 10dB and this requirement is the limit on the nulling resistors size. The complete micropower op amp with Simple Miller Compensation (SMC) is illustrated in

Figure 5-2. Figure 5-3 and Figure 5-4 show its frequency response and transient response respectively. With supply current of 20μA, the proposed op amp with SMC has a unity gain frequency of 360kHz with 61.5° phase margin at 100pF load.

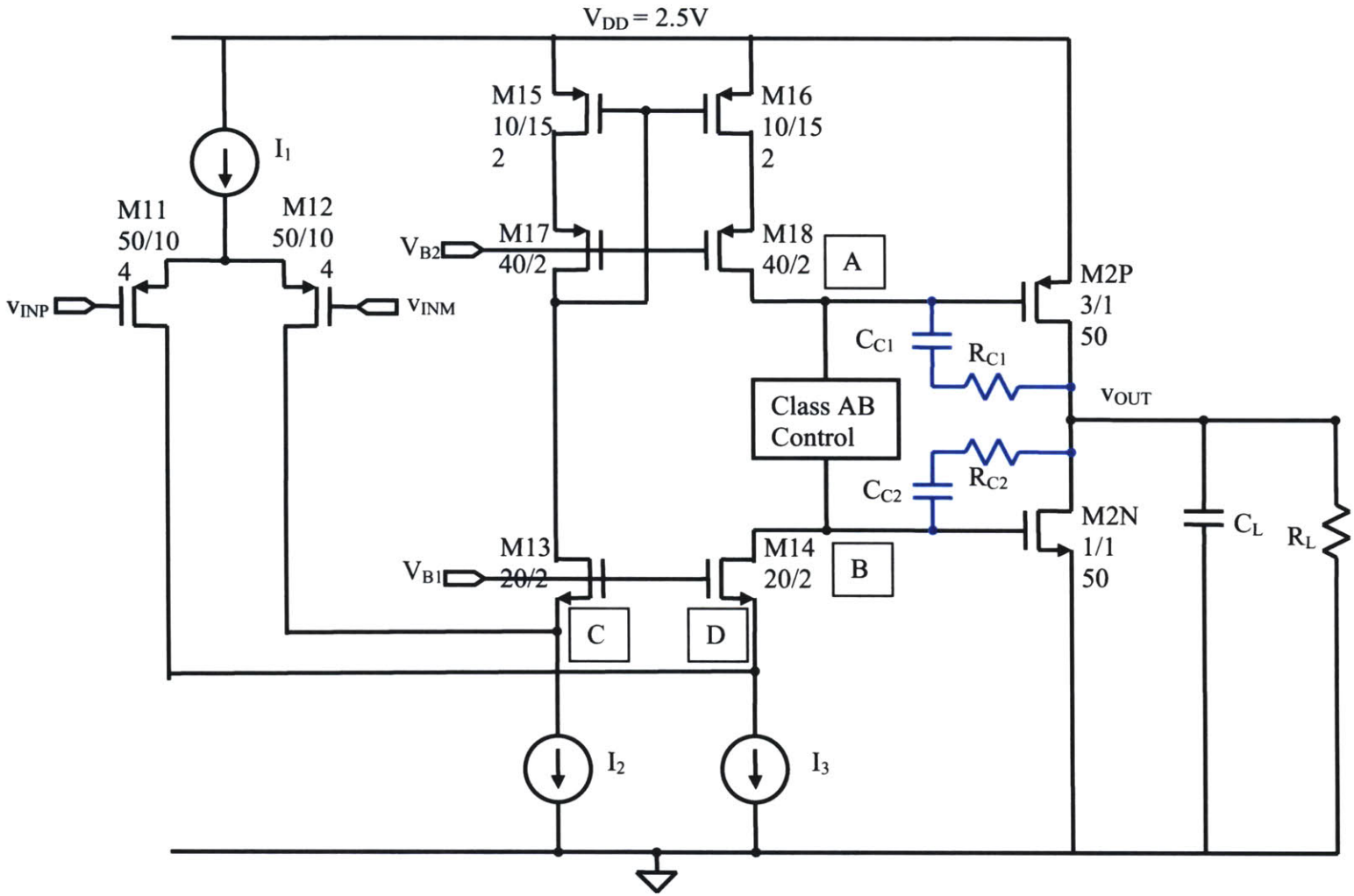


Figure 5-1: Simplified Schematic of Proposed Micropower Op Amp with Simple Miller Compensation (SMC)

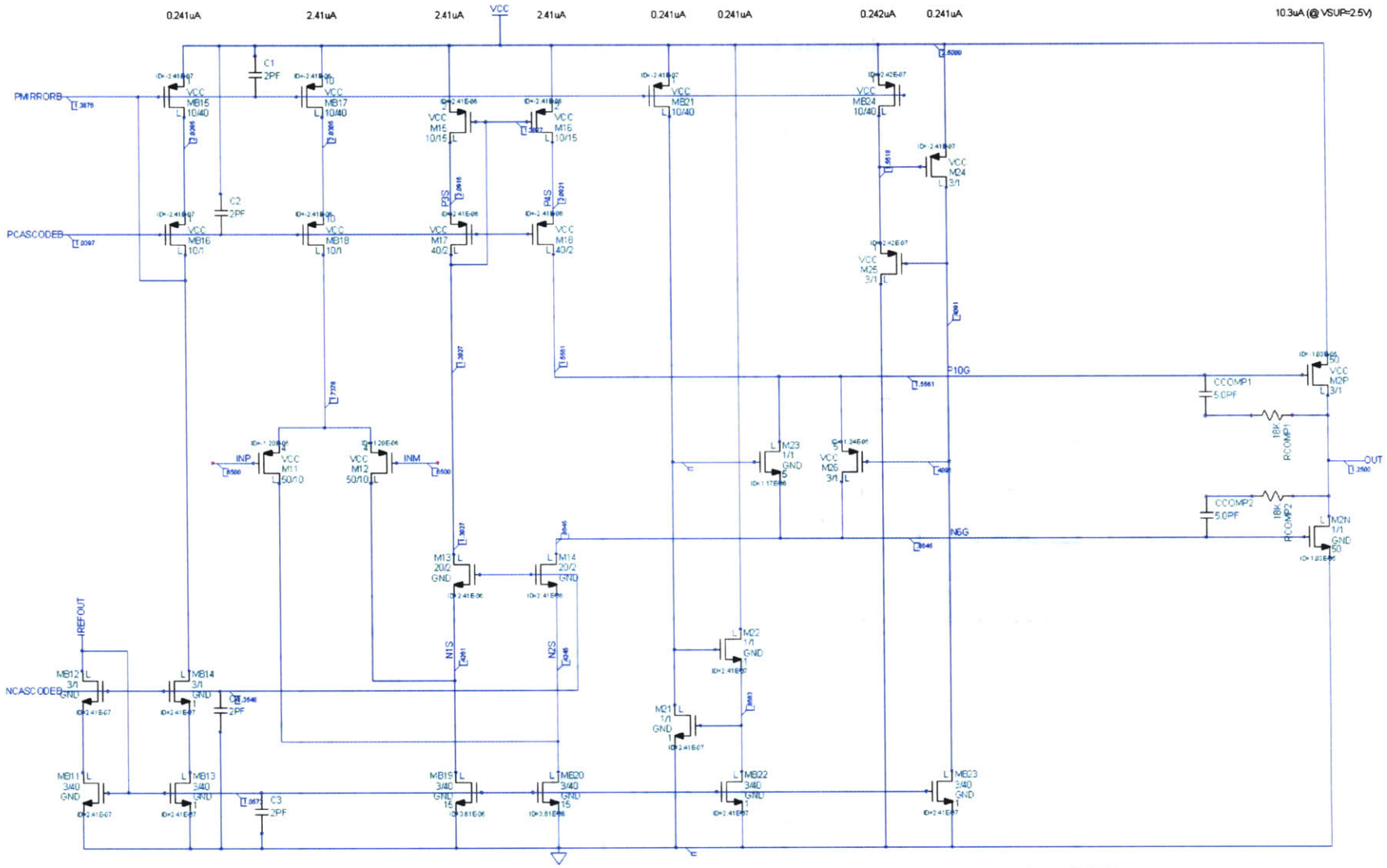


Figure 5-2: Schematic of Proposed Micropower Op Amp with Simple Miller Compensation (SMC)

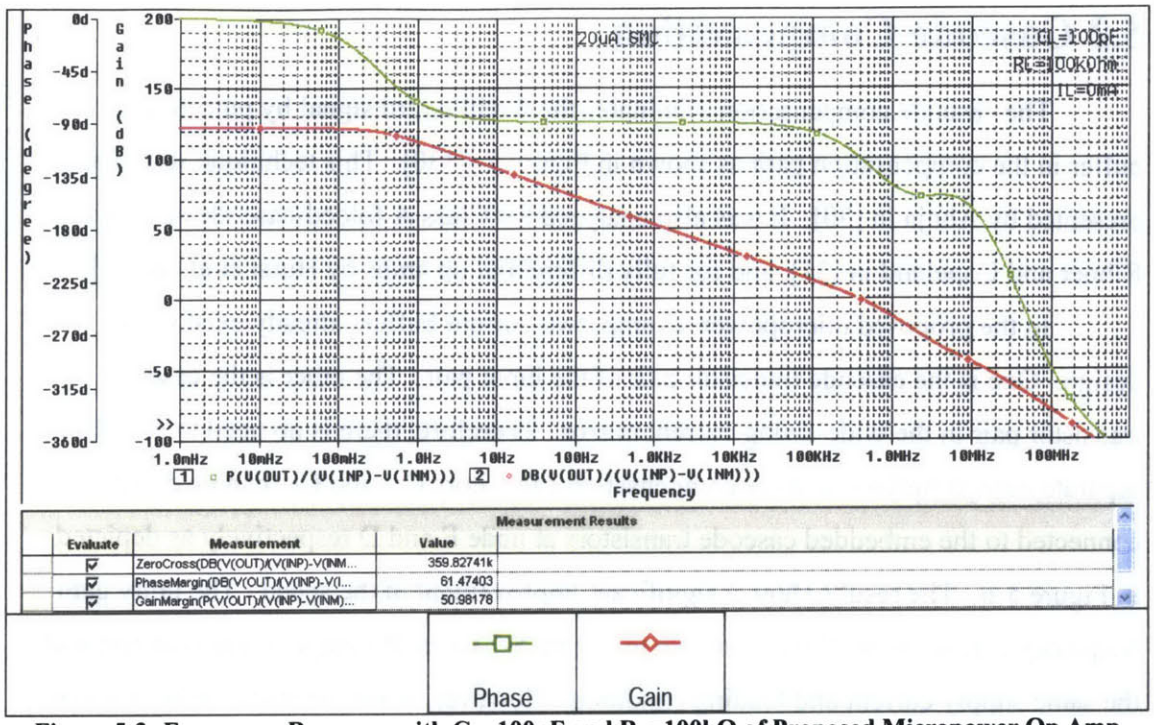


Figure 5-3: Frequency Response with C_L=100pF and R_L=100kΩ of Proposed Micropower Op Amp with Simple Miller Compensation (SMC)

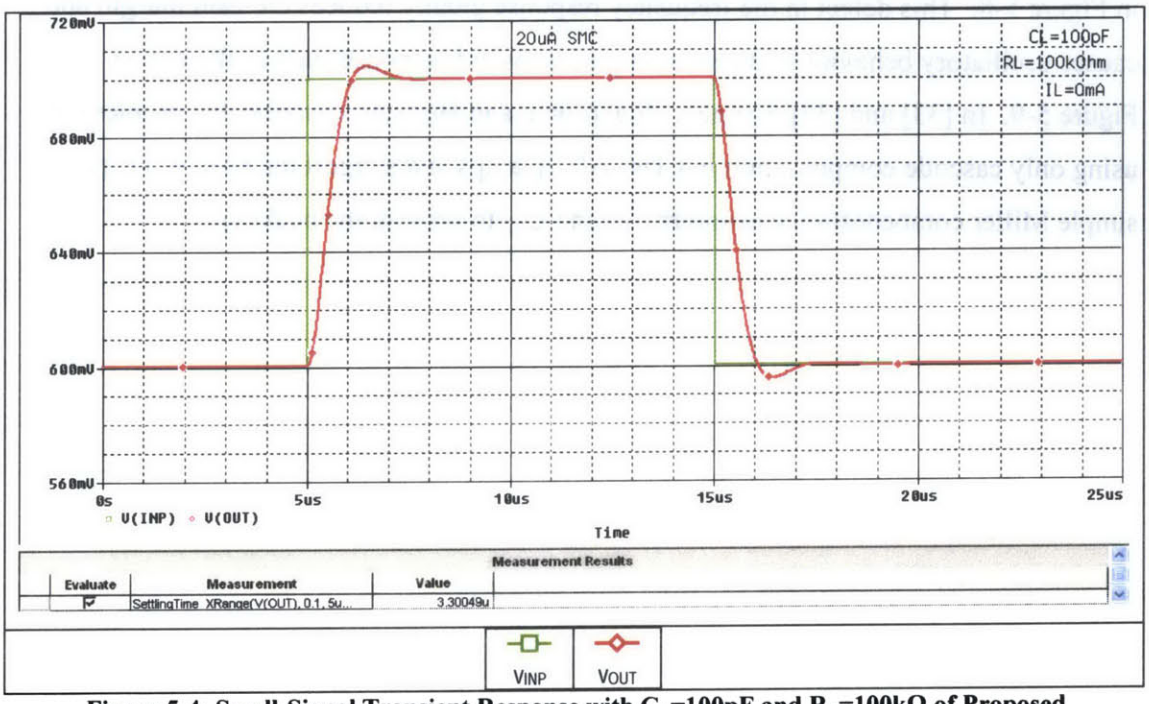


Figure 5-4: Small-Signal Transient Response with C_L=100pF and R_L=100kΩ of Proposed Micropower Op Amp with Simple Miller Compensation (SMC)

5.2 Cascode Compensation

The cascode compensation eliminates the feedforward signal by putting a current buffer in the compensation path as shown in Figure 5-5 [30]. This technique was first presented by Ahuja in [30]. It was also analyzed for Class A folded-cascode op amps by Ribner and Copeland in [31], and for fully differential op amps by Hurst et al. in [32].

In the proposed micropower op amp, two current buffers already exist in the design. One is the cascode transistor pair of the input pair. The other is the cascode transistor pair in the wide-swing current mirror. Therefore, there is no need to establish separate current buffers, and the compensation capacitors C_{C3} and C_{C4} can be directly connected to the embedded cascode transistors at node E and D respectively as depicted in Figure 5-6. The results show a significant improvement in the speed. The unity gain frequency extends to 991kHz as shown in Figure 5-7 when the output stage is at rest with the same supply current and loading condition. However, when the transconductance of the output stage transistors changes, there is peaking in the frequency response as shown in Figure 5-8. This defect in the frequency response greatly reduces the gain margin and causes oscillatory behavior in the small-signal transient response such as the one in Figure 5-9. In [33] and [34], Langen, Hogervorst, and Huijsing describe this problem of using only cascode compensation in Class AB op amps and suggest the need of keeping simple Miller compensation capacitors C_{C1} and C_{C2} to prevent the peaking.

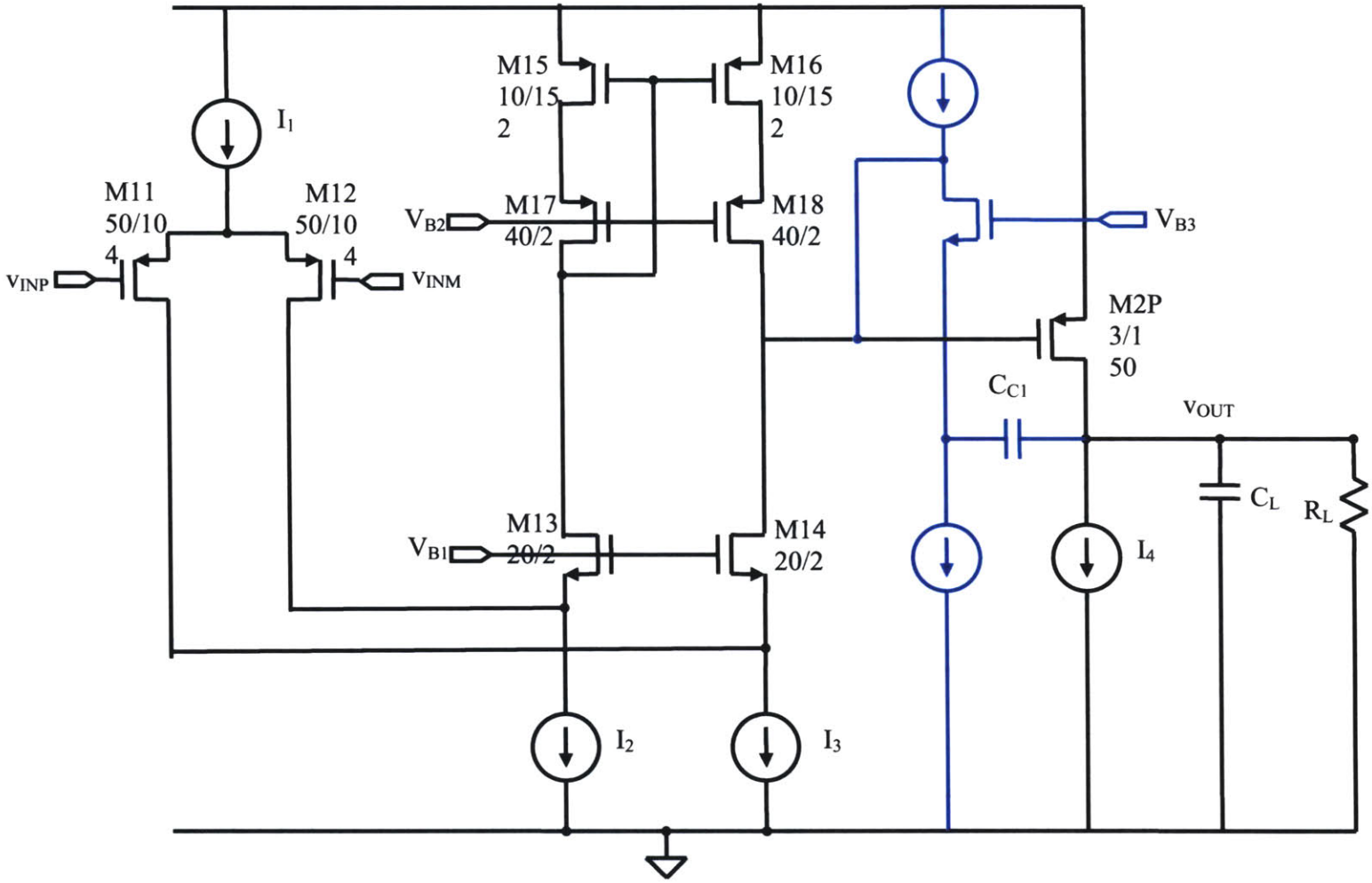


Figure 5-5: Class A Op Amp with Cascode Compensation (Adapted from [30])

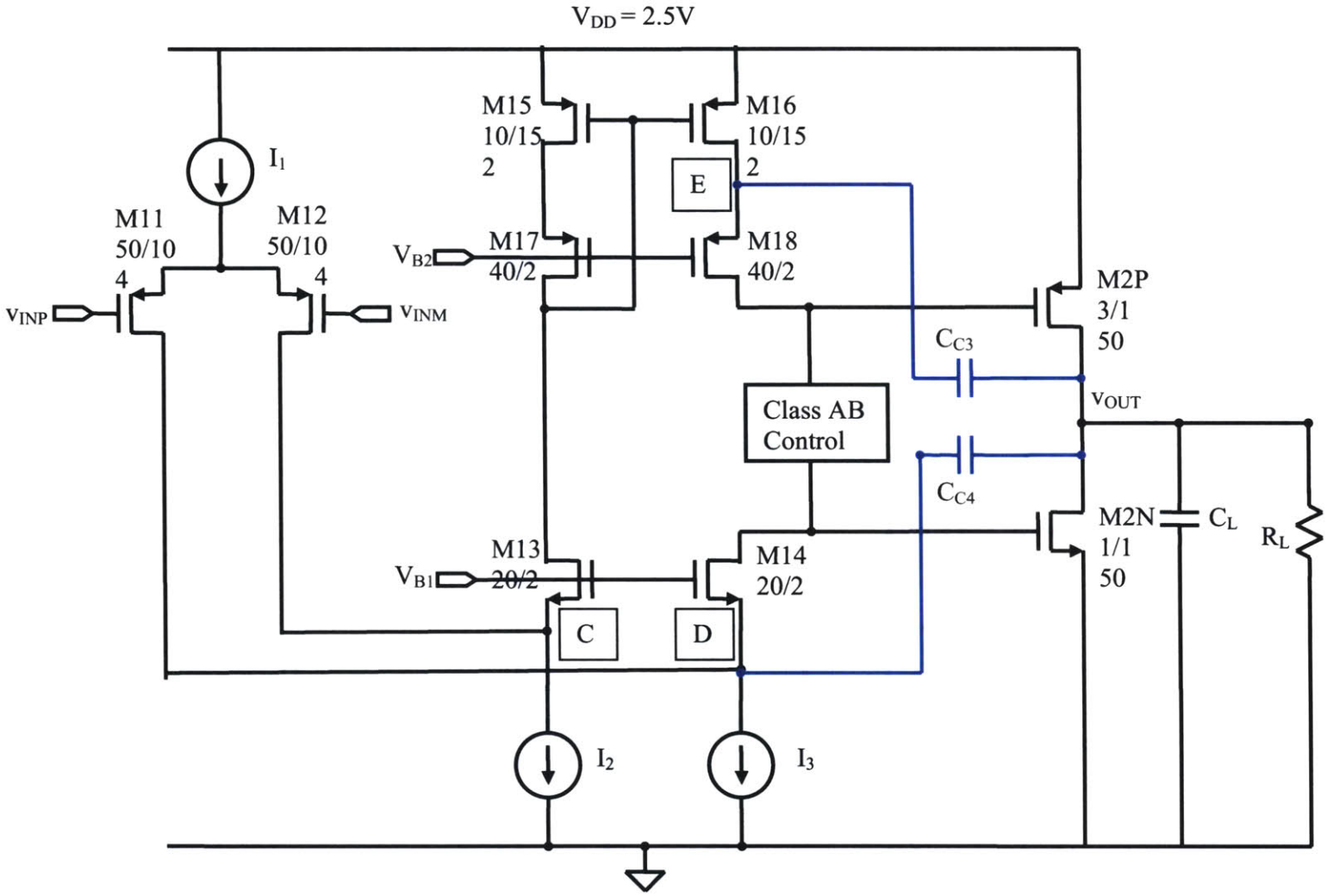


Figure 5-6: Simplified Schematic of Proposed Micropower Op Amp with Embedded Cascode Compensation (ECC) Only

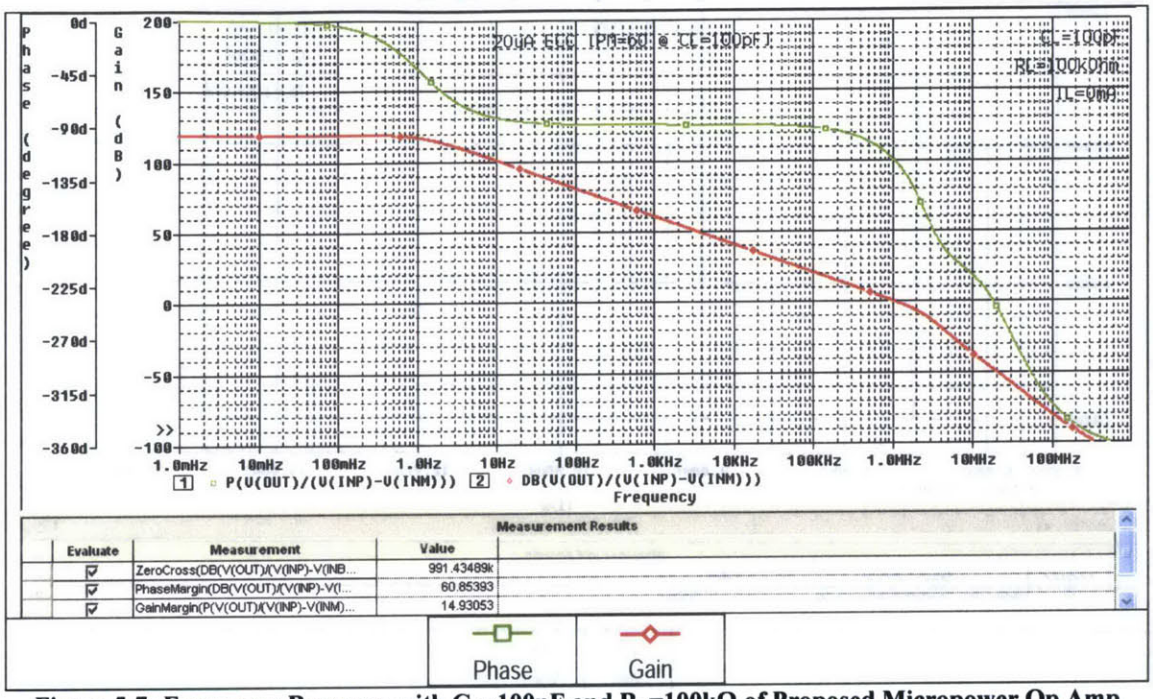


Figure 5-7: Frequency Response with C_L=100pF and R_L=100kΩ of Proposed Micropower Op Amp with Embedded Cascode Compensation (ECC) Only

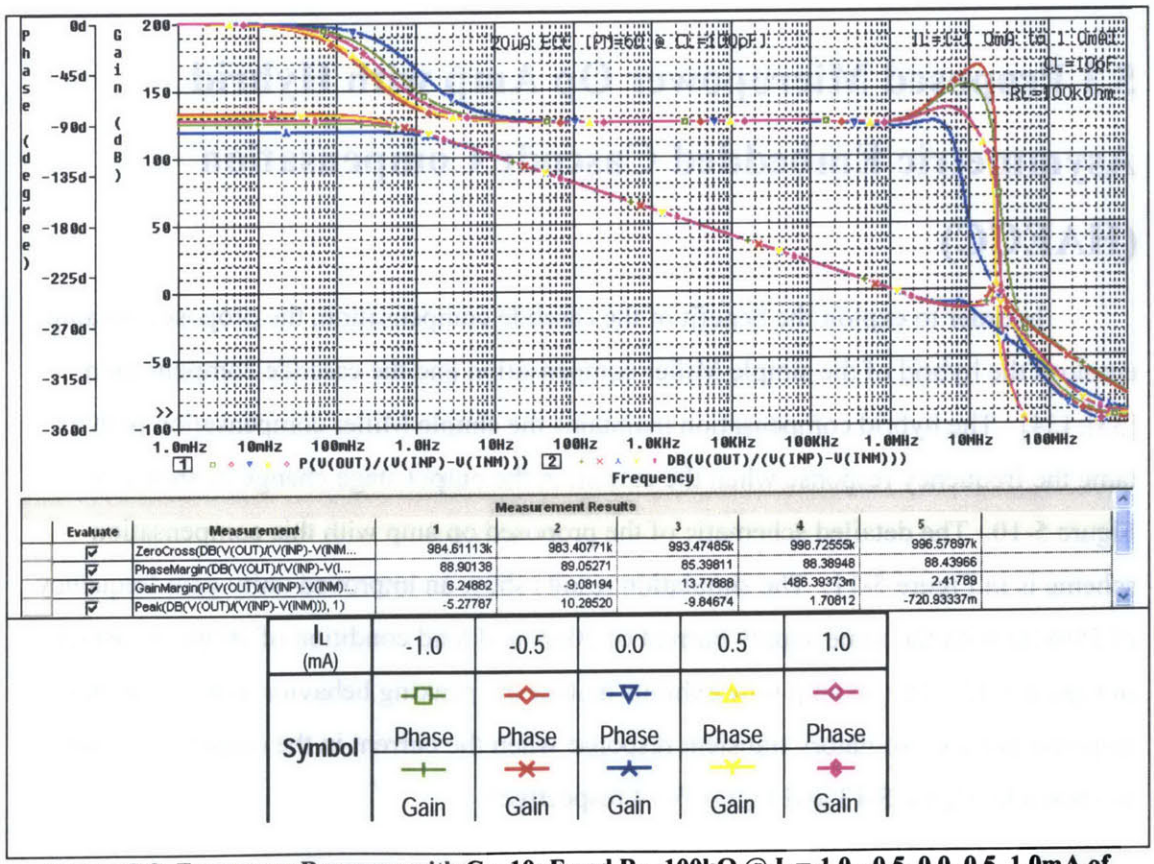


Figure 5-8: Frequency Response with C_L=10pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA of Proposed Micropower Op Amp with Embedded Cascode Compensation (ECC) Only

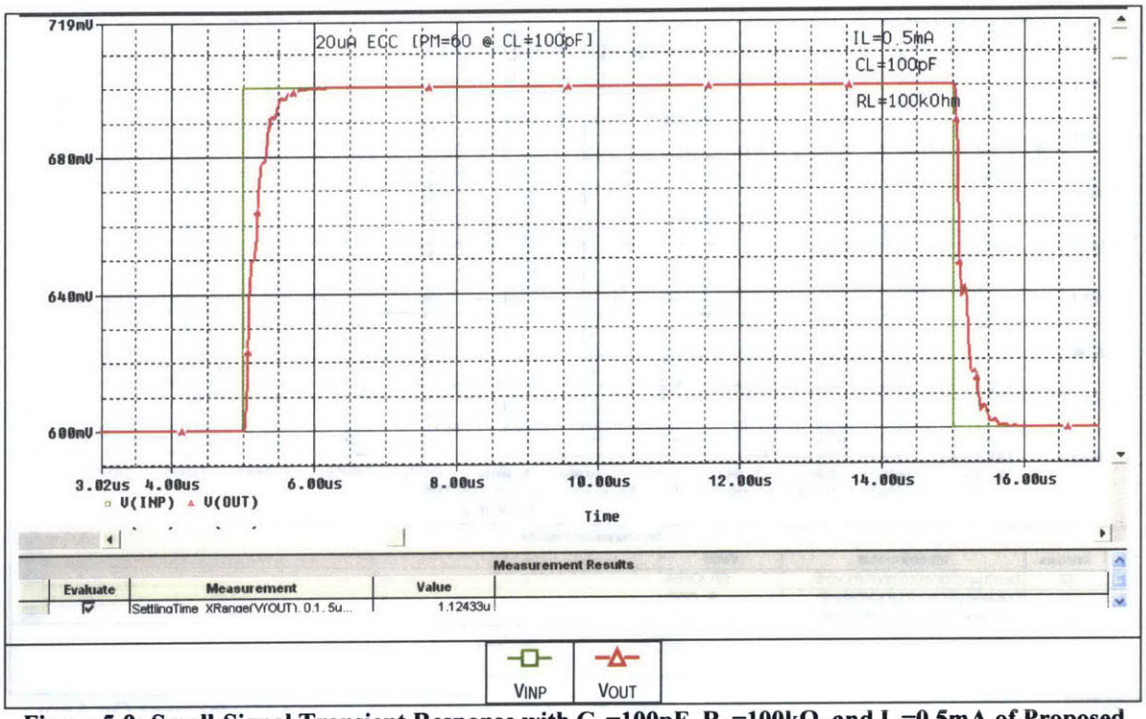


Figure 5-9: Small-Signal Transient Response with C_L=100pF, R_L=100kΩ, and I_L=0.5mA of Proposed Micropower Op Amp with Embedded Cascode Compensation (ECC) Only

5.3 Proposed Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)

In order to exploit the benefit of the cascode compensation, the proposed op amp employs the hybrid of the simple Miller compensation and the cascode compensation [33], [34]. The hybrid compensation maintains the simple Miller compensation path to tame the frequency response when the current in the output stage change as shown in Figure 5-10. The detailed schematic of the proposed op amp with this compensation scheme is in Figure 5-11. The simulation results show an improved unity gain frequency of 589kHz with the same supply current of 20μA and load condition of 100pF as depicted in Figure 5-12. The op amp now exhibits neither the peaking behavior in its frequency response nor the oscillatory transient response when the current in the output pair change as shown in Figure 5-13 and Figure 5-14 respectively

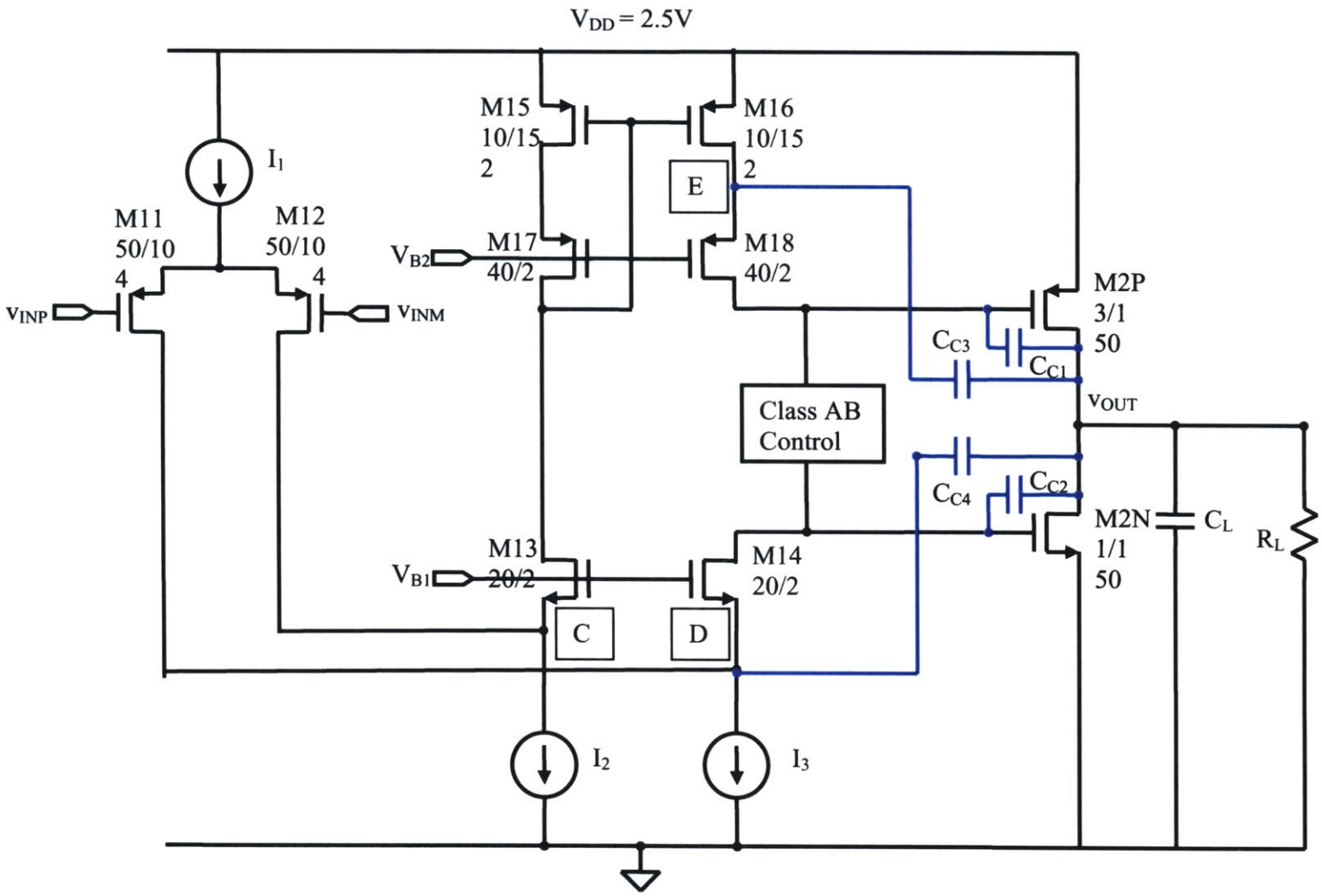


Figure 5-10: Simplified Schematic of Proposed Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)

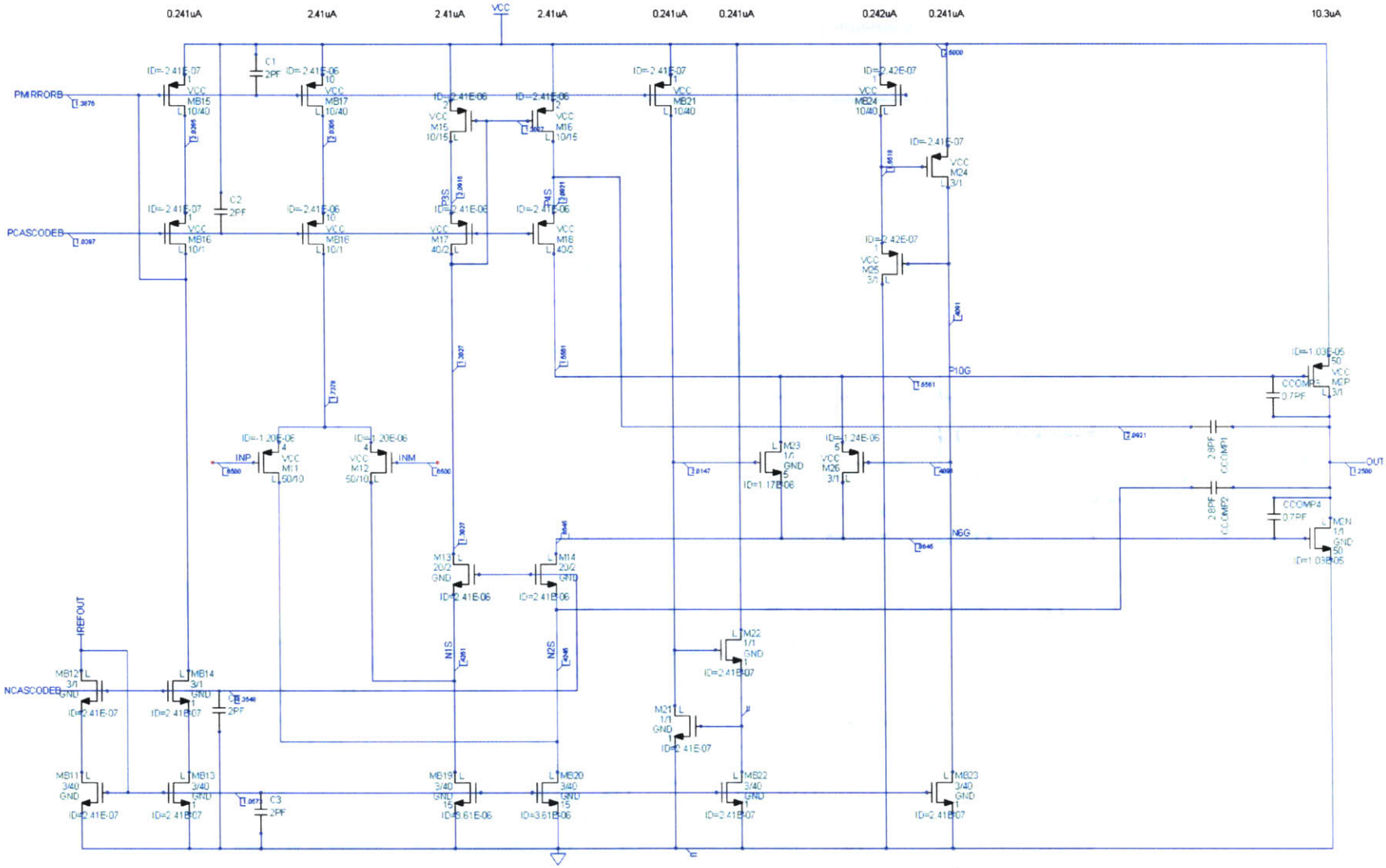


Figure 5-11: Schematic of Proposed Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)

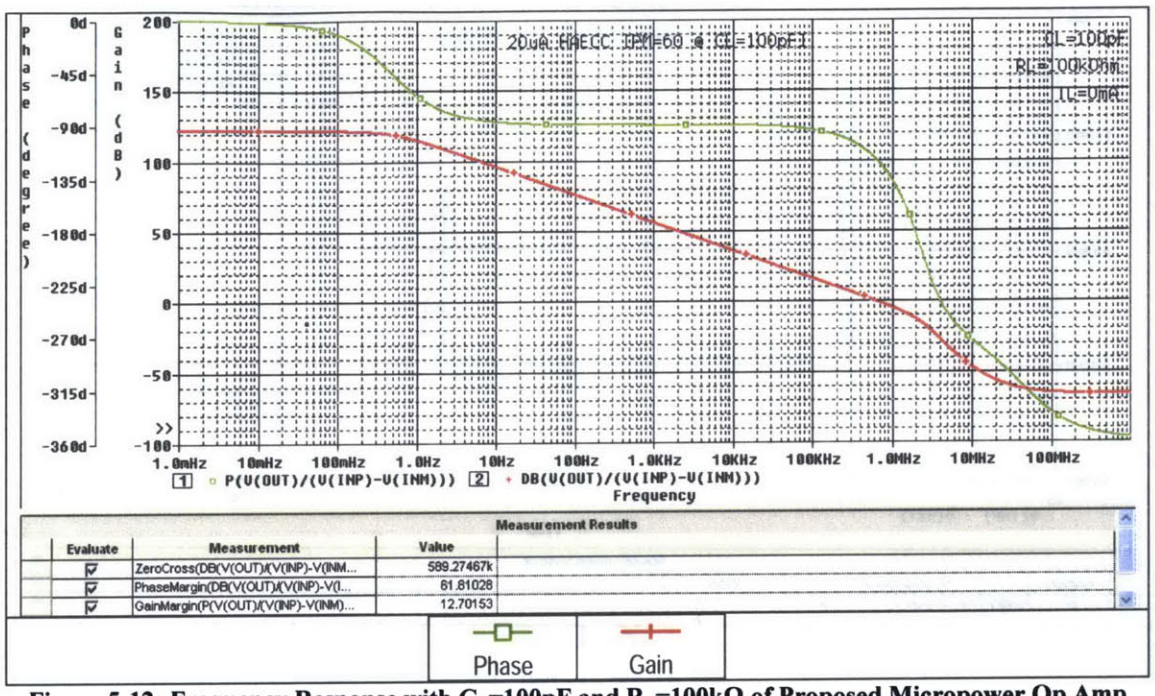


Figure 5-12: Frequency Response with C_L=100pF and R_L=100kΩ of Proposed Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)

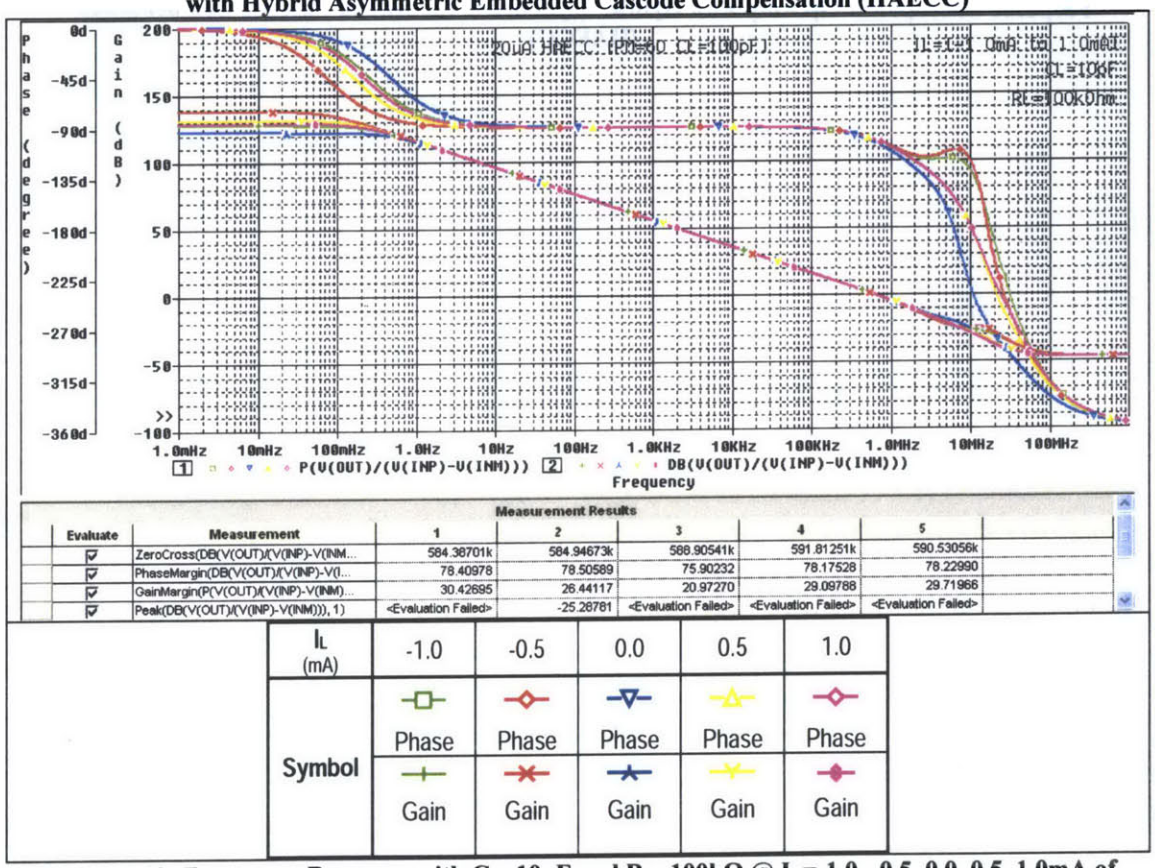


Figure 5-13: Frequency Response with C_L=10pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA of Proposed Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)

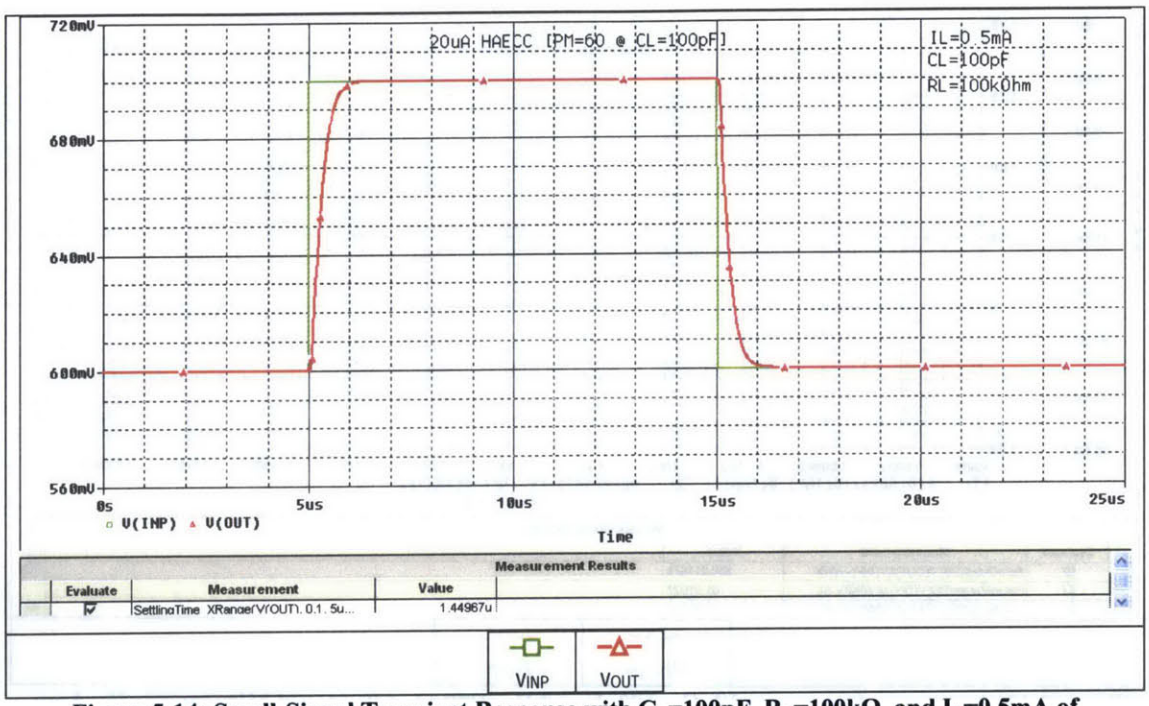


Figure 5-14: Small-Signal Transient Response with C_L=100pF, R_L=100kΩ, and I_L=0.5mA of Proposed Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)

Chapter 6 Final Results and Conclusion

Final Results

Two micropower op amp designs have proved to satisfy the project specifications set forth in Chapter 1. They essentially have the same architecture, but employ different frequency compensation schemes. The first one (Figure A-1 in Appendix A) uses Simple Miller Compensation (SMC). The other one (Figure D-1 in Appendix D) is compensated by a combination of simple Miller compensation and cascode compensation, or called Hybrid Asymmetric Embedded Cascode Compensation (HAECC) in this thesis. The detailed simulation results of all op amp designs are in the appendices. Table 6-1 summarizes the characteristics of the proposed micropower op amp with simple Miller Compensation (SMC). It has a unity gain frequency of 360kHz with 61.5° phase margin when loaded with 100pF. The proposed micropower op amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC) has a higher unity gain frequency of 589kHz at the same loading and power dissipation condition. Table 6-2 includes the detailed simulated characteristics of the design with HAECC.

Table 6-1: Characteristics of 20μA Micropower Op Amp with Simple Miller Compensation (SMC)

Simulation results are at 25°C. V_{DD} = 2.5V and V_{SS} = 0V.					
Primary Characteristics					
Symbol	**Parameter**	**Condition**	**Value**		**Unit**
			Specified	**Simulated**	
GBW[5]	**Gain Bandwidth Product**	C_L = 100pF R_L = 100kΩ	**> 0.3**	**0.360** (Φ_M = 61.5°)	**MHz**
A_{VOL}	**Large-Signal Voltage Gain (DC Open-Loop Gain)**	C_L = 100pF R_L = 100kΩ	**> 100**	**122**	**dB**
I_S	**Supply Current**	No Load	**< 21**	**19.95**	**μA**
V_{INCM}[6]	Input Common-Mode Range	-	> V_{DD} - 1.25V	**1.3**	V

[5] Gain bandwidth product per supply current GBW/ I_S = 18MHz/mA @ C_L = 100pF.
[6] Verified by CMRR simulation in Figure A-4.

				and must include negative supply voltage	and includes negative supply voltage	
V_{OS}[7]	(Untrimmed) Input Offset Voltage		V_{INCM} = 0.65V	< 5	**4.18**	mV
V_{OUT}	V_{OUTH}	High Output Voltage	I_{SOURCE} = 1.0mA	> V_{DD} - 0.3V	**2.34**	V
	V_{OUTL}	Low Output Voltage	I_{SINK} = 1.0mA	< V_{SS} + 0.3V	**0.19**	V
I_{SOURCE}[8]	Output Source Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.55**	mA
I_{SINK}	Output Sink Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.04**	mA
Secondary Characteristics						
Symbol	**Parameter**		**Condition**	**Value**		**Unit**
				Specified	**Simulated**	
SR	Positive Going Slew Rate		A_V = 1V/V, 1V Step	> 0.15	**0.223**	V/μs
SR-	Negative Going Slew Rate		A_V = 1V/V, 1V Step	< -0.15	**-0.236**	V/μs
CMRR	Common Mode Rejection Ratio		@ DC	> 60	**144**	dB
PSRR+	Positive Power Supply Rejection Ratio		@ DC	> 60	**84.5**	dB
PSRR-	Negative Power Supply Rejection Ratio		@ DC	> 60	**99.4**	dB
t_s	0.1% Settling Time		A_V = 1V/V, 1V Step	< 10	**5.29**	μs

Table 6-2: Characteristics of 20μA Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)

Simulation results are at 25°C. V_{DD} = 2.5V and V_{SS} = 0V.					
Primary Characteristics					
Symbol	**Parameter**	**Condition**	**Value**		**Unit**
			Specified	**Simulated**	
GBW[9]	**Gain Bandwidth Product**	C_L = 100pF R_L = 100kΩ	**> 0.3**	**0.589** (Φ_M = 61.8°)	**MHz**

[7] Conservative estimate from calculation.
[8] Maximum output source current is measured when the other transistor in the output pair starts to turn off, i.e. its current goes down to as low as 1μA.
[9] Gain bandwidth product per supply current GBW/ I_S = 29.5MHz/mA @ C_L = 100pF.

A_{VOL}	**Large-Signal Voltage Gain (DC Open-Loop Gain)**		C_L = 100pF R_L = 100kΩ	**> 100**	**122**	**dB**
I_S	**Supply Current**		No Load	**< 21**	**19.95**	**µA**
V_{INCM}[10]	Input Common-Mode Range		-	> V_{DD} - 1.25V and must include negative supply voltage	**1.3** and includes negative supply voltage	V
V_{OS}[11]	(Untrimmed) Input Offset Voltage		V_{INCM} = 0.65V	< 5	**4.17**	mV
V_{OUT}	V_{OUTH}	High Output Voltage	I_{SOURCE} = 1.0mA	> V_{DD} - 0.3V	**2.34**	V
	V_{OUTL}	Low Output Voltage	I_{SINK} = 1.0mA	< V_{SS} + 0.3V	**0.19**	V
I_{SOURCE}[12]	Output Source Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.55**	mA
I_{SINK}	Output Sink Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.03**	mA

Secondary Characteristics

Symbol	**Parameter**	**Condition**	**Value**		**Unit**
			Specified	**Simulated**	
SR+	Positive Going Slew Rate	A_V = 1V/V, 1V Step	> 0.15	**0.315**	V/µs
SR-	Negative Going Slew Rate	A_V = 1V/V, 1V Step	< -0.15	**-0.342**	V/µs
CMRR	Common Mode Rejection Ratio	@ DC	> 60	**144**	dB
PSRR+	Positive Power Supply Rejection Ratio	@ DC	> 60	**84.6**	dB
PSRR-	Negative Power Supply Rejection Ratio	@ DC	> 60	**99.5**	dB
t_s	0.1% Settling Time	A_V = 1V/V, 1V Step	< 10	**3.70**	Ms

[10] Verified by CMRR simulation in Figure D-4.
[11] Conservative estimate from calculation.
[12] Maximum output source current is measured when the other transistor in the output pair starts to turn off, i.e. its current goes down to as low as 1µA.

Discussion

The two proposed micropower op amp designs have a higher unity gain frequency than the two commercial low-power op amp ICs previously mentioned, MAX9914 and MIC861, when compared at approximately the same supply current and loading condition. The design with HAECC offers a gain bandwidth product of 1.87MHz when compensated to have phase margin of 45° at 15pF load as shown in Figure 6-1. Table 6-3 summarizes the frequency domain performances of the proposed design and MAX9914.

In addition, when the proposed design is biased at 5μA, the one with HAECC compensation gives a gain bandwidth product of 375kHz with the phase margin of 45° at 50pF as depicted in Figure 6-2, which is higher than that of MIC861. Table 6-4 presents the overview of the comparison between the proposed designs and MIC861.

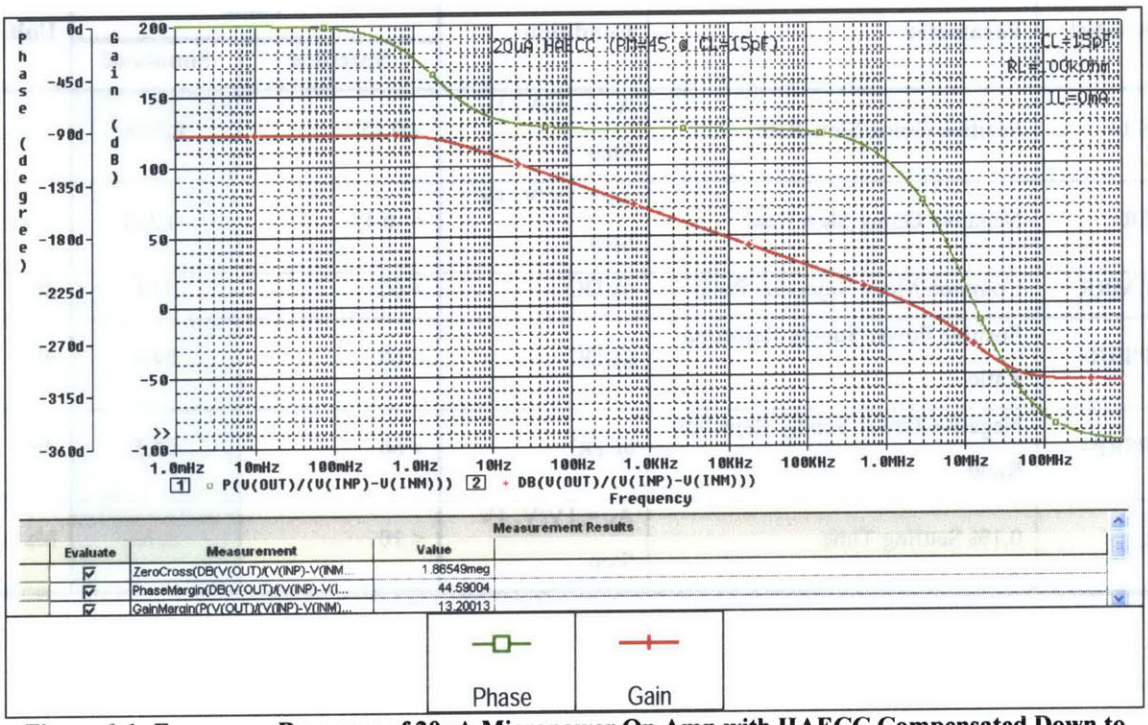


Figure 6-1: Frequency Response of 20μA Micropower Op Amp with HAECC Compensated Down to Have $\Phi_M = 45°$ at 15pF Load to Compare with MAX9914

20µA Op Amp [Φ_M=45 @ CL=15pF, vs MAX9914]		Frequency Response			
		C_L = 0pF, R_L = 100kΩ		C_L = 15pF, R_L = 100kΩ	
		GBW (MHz)	Φ_M (°)	GBW (MHz)	Φ_M (°)
Simple Miller Compensation	***SMC***	**1.79**	**72**	**1.65**	**47**
Hybrid Explicit Cascode Compensation	*HECC*	1.63	68	1.56	46
Hybrid Asymmetric Embedded Cascode Compensation	***HAECC***	**1.91**	**63**	**1.87**	**45**
MAX9914[3]		**-**	**-**	***1.0***	***45***

Table 6-3: Comparison of Unity Gain Frequency between the Proposed 20µA Micropower Op Amps and MAX9914

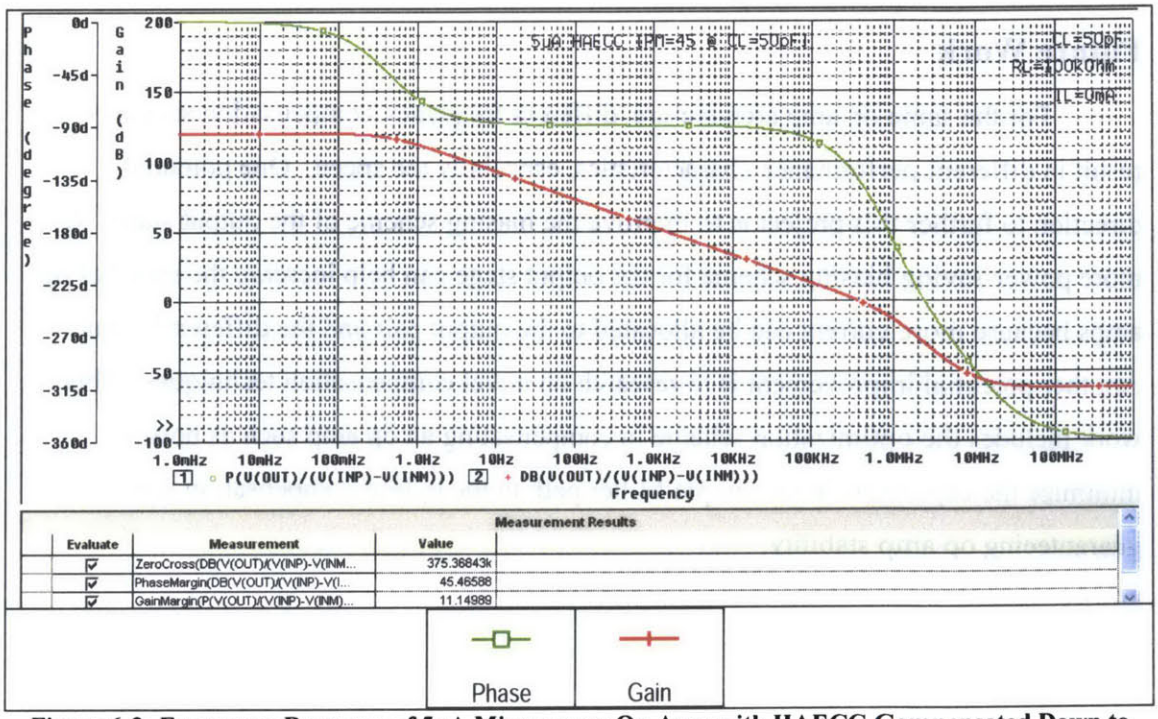


Figure 6-2: Frequency Response of 5µA Micropower Op Amp with HAECC Compensated Down to Have Φ_M = 45° at 50pF Load to Compare with MIC861

5μA Op Amp [PM=45 @ CL=50pF, vs MIC861]		Frequency Response			
		C_L = 0pF, R_L = 100kΩ		**C_L = 50pF**, R_L = 100kΩ	
		GBW (kHz)	Φ_M (°)	GBW (kHz)	Φ_M (°)
Simple Miller Compensation	***SMC***	**329**	**81**	**267**	**45**
Hybrid Explicit Cascode Compensation	*HECC*	369	79	327	46
Hybrid Asymmetric Embedded Cascode Compensation	***HAECC***	**403**	**72**	**375**	**45**
MIC861[4]		***350***	***N/A***	***225***	***≈ 45***[13]

Table 6-4: Comparison of Unity Gain Frequency between the Proposed 5μA Micropower Op Amps and MIC861

Future Work

For the same op amp architecture, different frequency compensation schemes result in different performance characteristics, especially the speed. One potential direction to further this project is to improve the biasing scheme of the output stage. A more power-saving biasing scheme for the output stage can help increase the speed of op amps because more current can be allocated to the output pair and the differential pair. Another potential improvement is to research on novel compensation techniques. This work includes the optimization scheme in compensating an op amp such as how to minimize the capacitors in the simple Miller path in the hybrid compensation while guaranteeing op amp stability.

[13] The phase margin is not given in [4]. It is estimated from the datasheet that the IC has 2-3 periods of decayed oscillation in the small-signal pulse response at 50pF load.

Appendices

Appendix A Schematics and Characteristics of 20μA Micropower Op Amp with Simple Miller Compensation (SMC)

Appendix B Schematics and Characteristics of 20μA Micropower Op Amp with Hybrid Explicit Cascode Compensation (HECC)

Appendix C Schematics and Characteristics of 20μA Micropower Op Amp with Hybrid Symmetric Embedded Cascode Compensation (HSECC)

Appendix D Schematics and Characteristics of 20μA Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)

Appendix A Schematics and Characteristics of 20μA Micropower Op Amp with Simple Miller Compensation (SMC)

LIST OF FIGURES IN APPENDIX A

Table A: Characteristics of 20µA Micropower Op Amp with Simple Miller Compensation (SMC) from Simulation

Simulation results are at 25°C. V_{DD} = 2.5V and V_{SS} = 0V.						
Primary Characteristics						
Symbol	**Parameter**		**Condition**	**Value**		**Unit**
				Specified	**Simulated**	
GBW[14]	**Gain Bandwidth Product**		C_L = 100pF R_L = 100kΩ	**> 0.3**	**0.360** (Φ_M = 61.5°)	**MHz**
A_{VOL}	**Large-Signal Voltage Gain (DC Open-Loop Gain)**		C_L = 100pF R_L = 100kΩ	**> 100**	**122**	**dB**
I_S	**Supply Current**		No Load	**< 21**	**19.95**	**µA**
V_{INCM}[15]	Input Common-Mode Range		-	> V_{DD} - 1.25V and must include negative supply voltage	**1.3** and includes negative supply voltage	V
V_{OS}[16]	(Untrimmed) Input Offset Voltage		V_{INCM} = 0.65V	< 5	**4.18**	mV
V_{OUT}	V_{OUTH}	High Output Voltage	I_{SOURCE} = 1.0mA	> V_{DD} - 0.3V	**2.34**	V
	V_{OUTL}	Low Output Voltage	I_{SINK} = 1.0mA	< V_{SS} + 0.3V	**0.19**	V
I_{SOURCE}[17]	Output Source Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.55**	mA
I_{SINK}	Output Sink Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.04**	mA
Secondary Characteristics						
Symbol	**Parameter**		**Condition**	**Value**		**Unit**
				Specified	**Simulated**	
SR+	Positive Going Slew Rate		A_V = 1V/V, 1V Step	> 0.15	**0.223**	V/µs
SR-	Negative Going Slew Rate		A_V = 1V/V, 1V Step	< -0.15	**-0.236**	V/µs

[14] Gain bandwidth product per supply current GBW/ I_S = 18MHz/mA @ C_L = 100pF.
[15] Verified by CMRR simulation in Figure A-4.
[16] Conservative estimate from calculation.
[17] Maximum output source current is measured when the other transistor in the output pair starts to turn off, i.e. its current goes down to as low as 1µA.

CMRR	Common Mode Rejection Ratio	@ DC	> 60	**144**	dB
PSRR+	Positive Power Supply Rejection Ratio	@ DC	> 60	**84.5**	dB
PSRR-	Negative Power Supply Rejection Ratio	@ DC	> 60	**99.4**	dB
t_s	0.1% Settling Time	A_V = 1V/V, 1V Step	< 10	**5.29**	µs

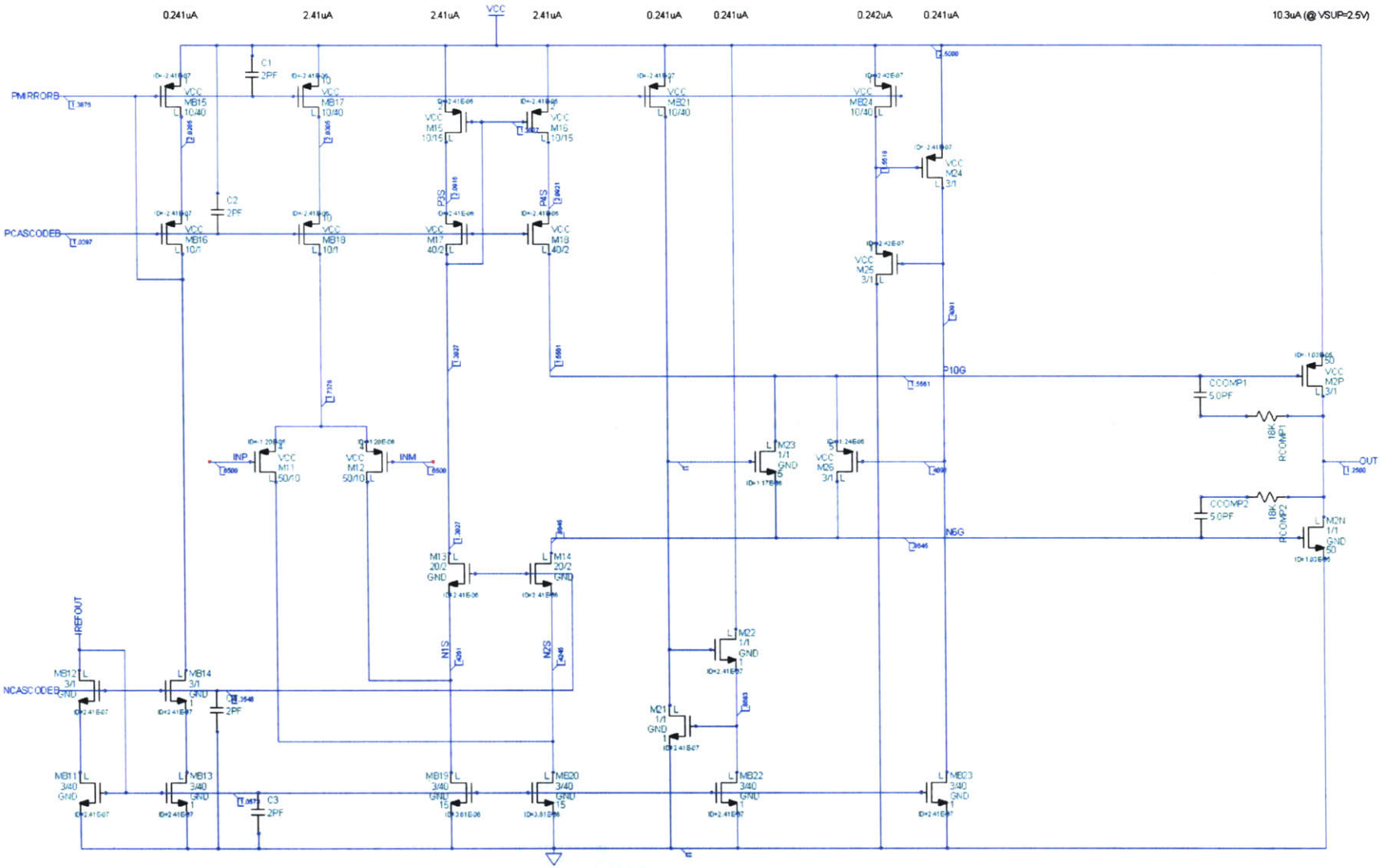
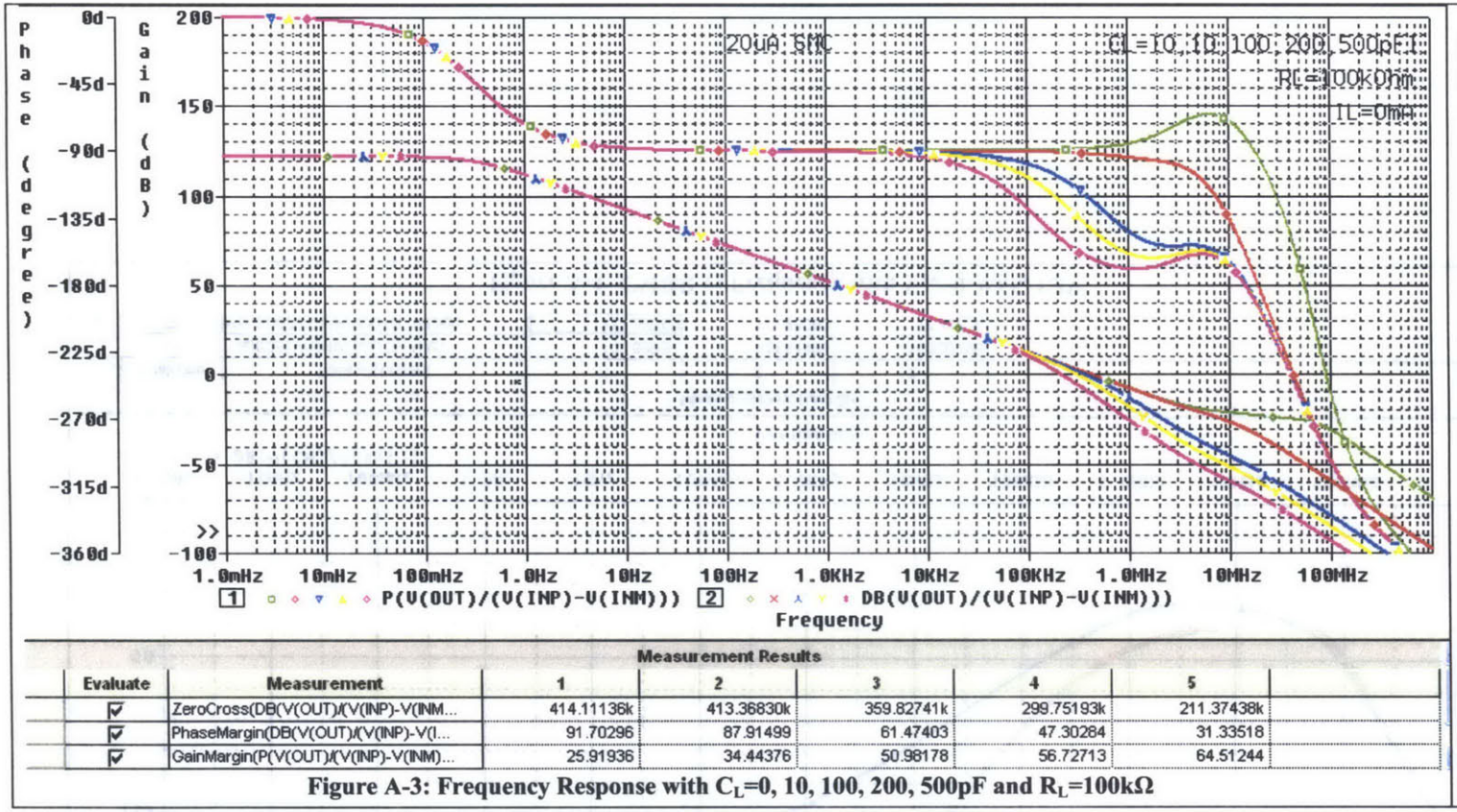


Figure A-1: Schematic of 20µA Micropower Op Amp with Simple Miller Compensation (SMC)

Measurement Results

Evaluate	Measurement	Value
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	359.82741k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	61.47403
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	50.98178

Figure A-2: Frequency Response with C_L=100pF and R_L=100kΩ

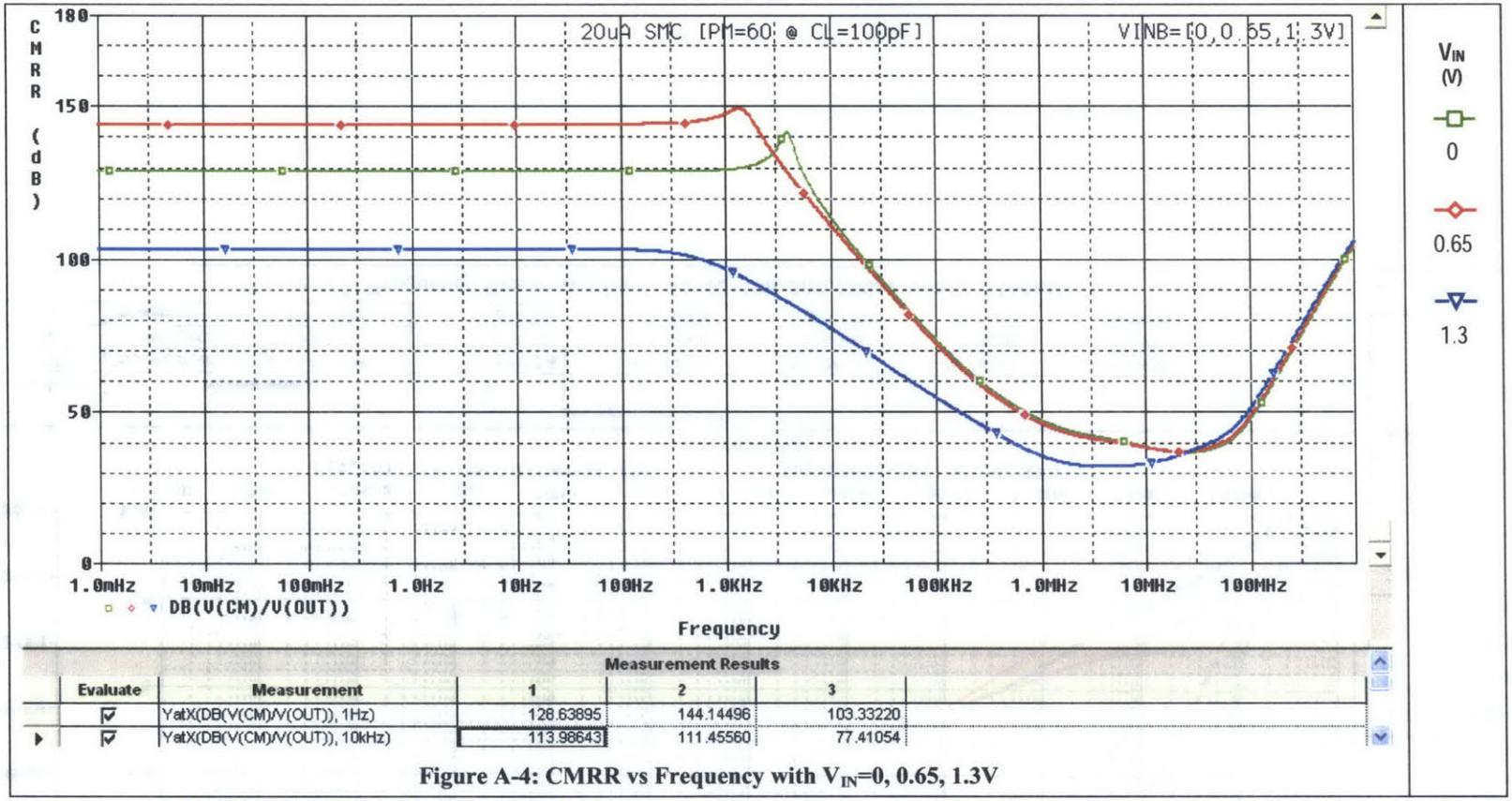


C_L (pF)	Symbol
0	Phase, Gain
10	Phase, Gain
100	Phase, Gain
200	Phase, Gain
500	Phase, Gain

Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	414.11136k	413.36830k	359.82741k	299.75193k	211.37438k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	91.70296	87.91499	61.47403	47.30284	31.33518
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	25.91936	34.44376	50.98178	56.72713	64.51244

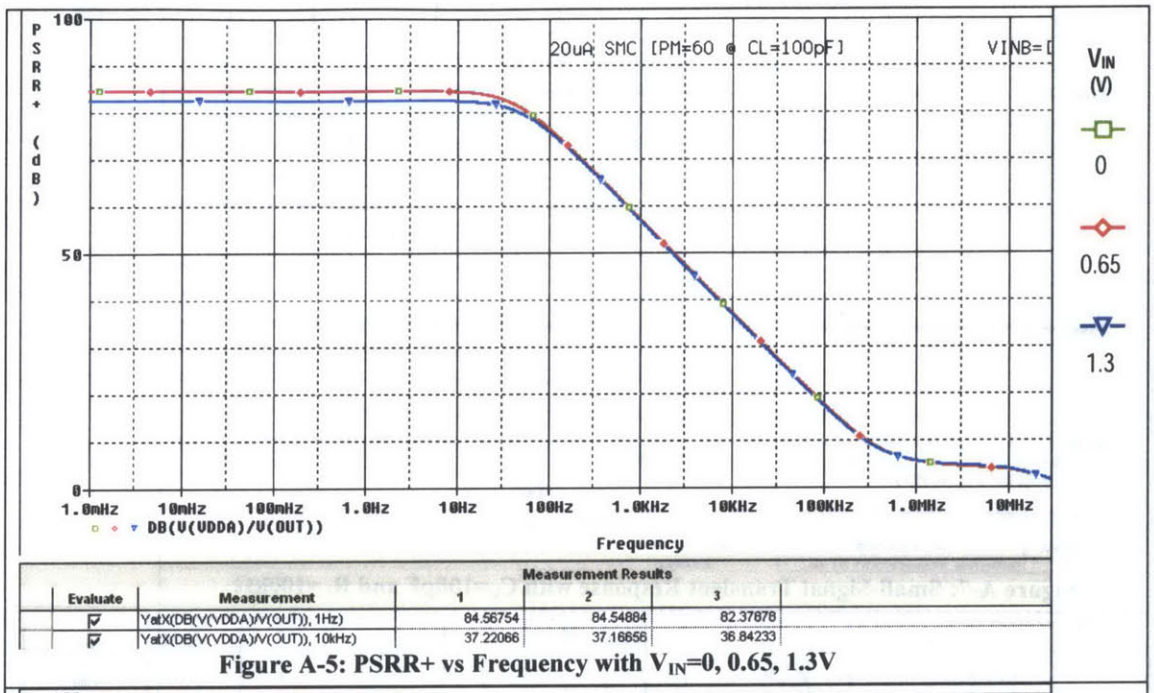
Figure A-3: Frequency Response with C_L=0, 10, 100, 200, 500pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	1	2	3
☑	YatX(DB(V(CM)/V(OUT)), 1Hz)	128.63895	144.14496	103.33220
☑	YatX(DB(V(CM)/V(OUT)), 10kHz)	113.98643	111.45560	77.41054

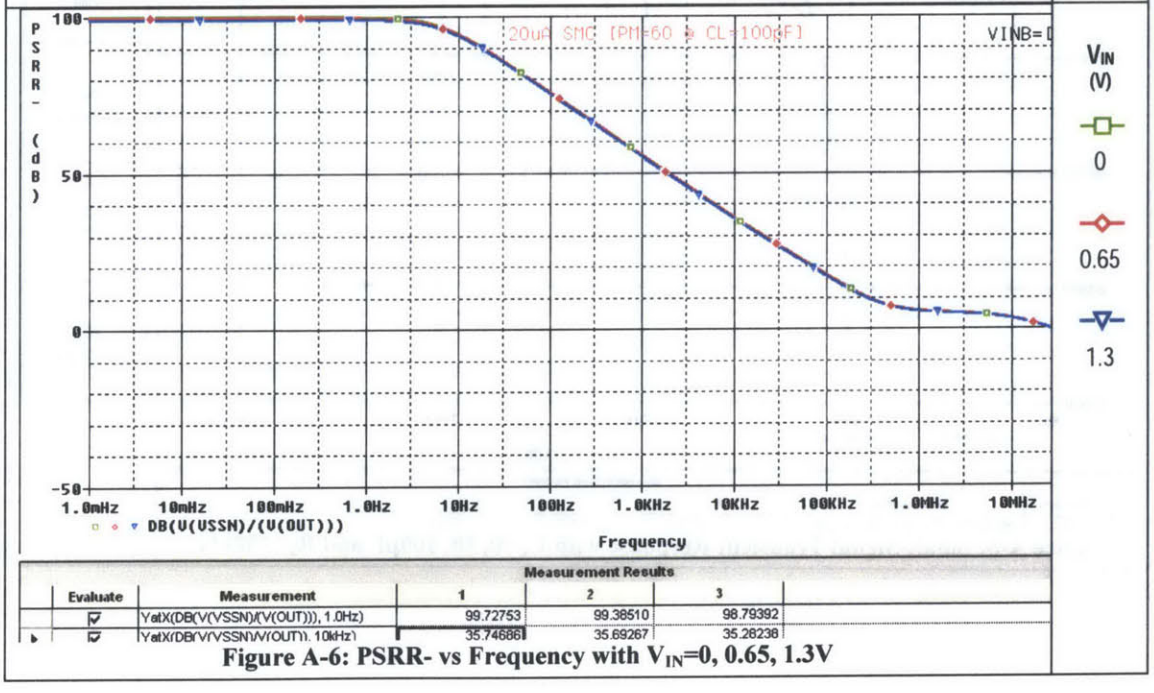
Figure A-4: CMRR vs Frequency with V_{IN}=0, 0.65, 1.3V



Measurement Results

Evaluate	Measurement	1	2	3
☑	YatX(DB(V(VDDA)/V(OUT)), 1Hz)	84.56754	84.54884	82.37878
☑	YatX(DB(V(VDDA)/V(OUT)), 10kHz)	37.22066	37.16656	36.84233

Figure A-5: PSRR+ vs Frequency with V_{IN}=0, 0.65, 1.3V



Measurement Results

Evaluate	Measurement	1	2	3
☑	YatX(DB(V(VSSN)/(V(OUT))), 1.0Hz)	99.72753	99.38510	98.79392
☑	YatX(DB(V(VSSN)/V(OUT)), 10kHz)	35.74686	35.69267	35.28238

Figure A-6: PSRR- vs Frequency with V_{IN}=0, 0.65, 1.3V

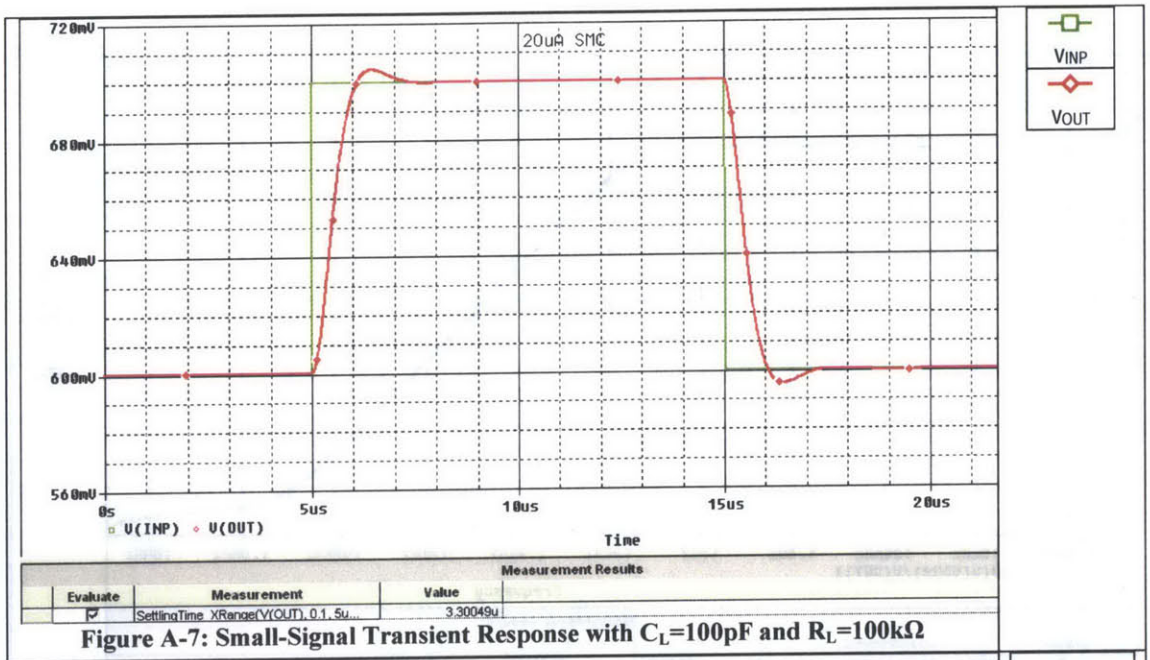


Figure A-7: Small-Signal Transient Response with C_L=100pF and R_L=100kΩ

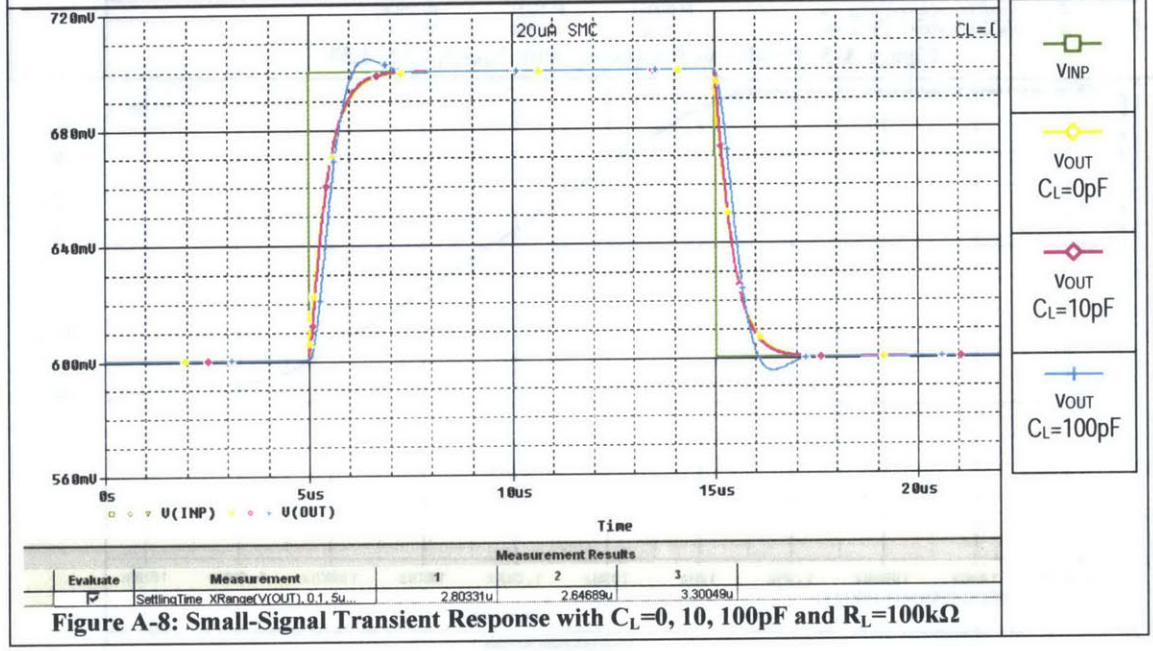
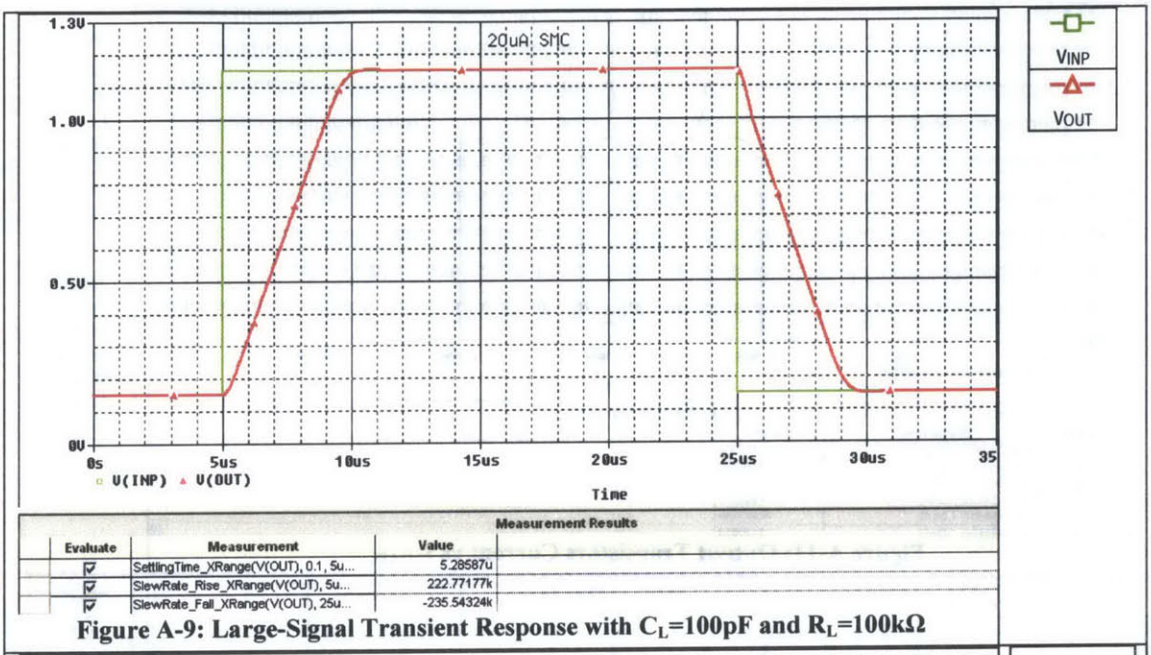


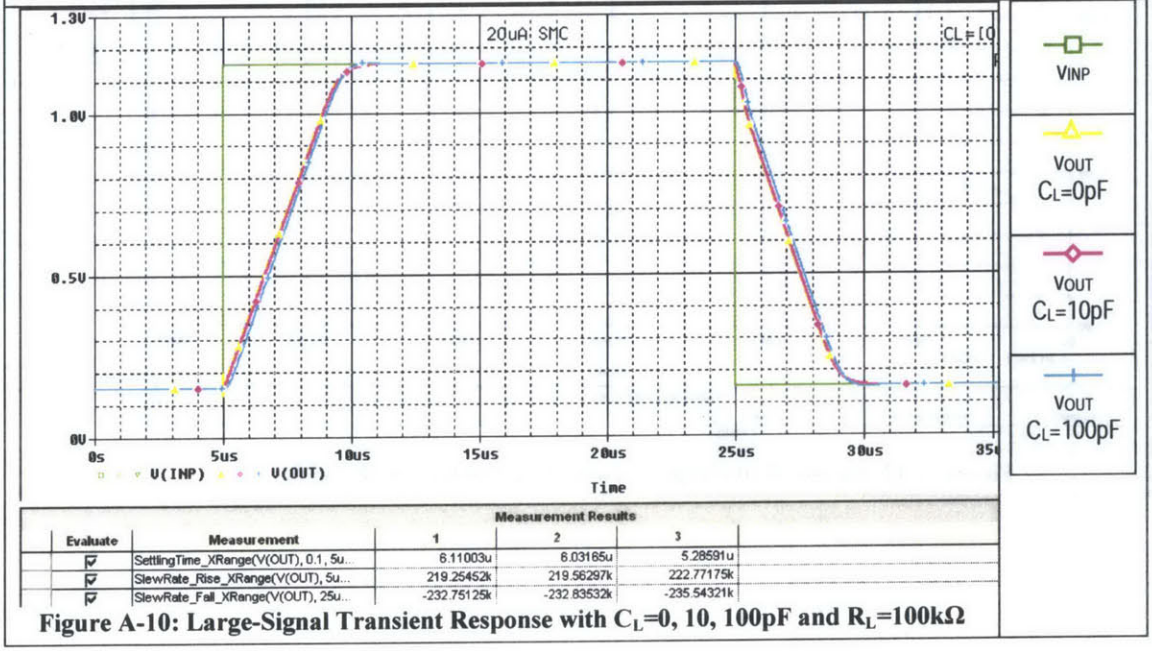
Figure A-8: Small-Signal Transient Response with C_L=0, 10, 100pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	Value
☑	SettlingTime_XRange(V(OUT), 0.1, 5u...	5.28587u
☑	SlewRate_Rise_XRange(V(OUT), 5u...	222.77177k
☑	SlewRate_Fall_XRange(V(OUT), 25u...	-235.54324k

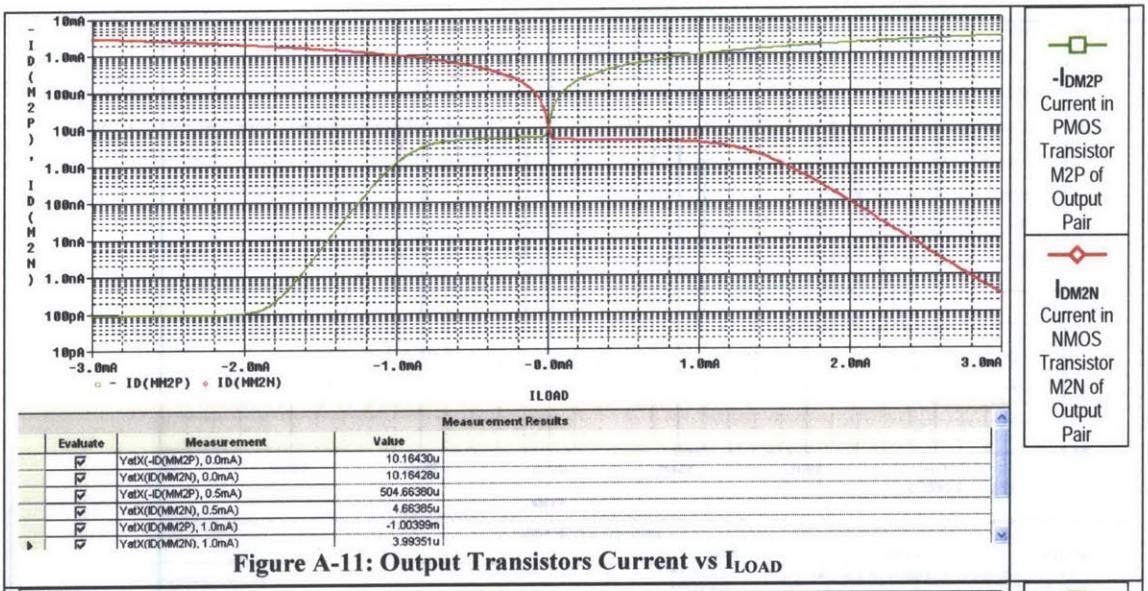
Figure A-9: Large-Signal Transient Response with C_L=100pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	1	2	3
☑	SettlingTime_XRange(V(OUT), 0.1, 5u...	6.11003u	6.03185u	5.28591u
☑	SlewRate_Rise_XRange(V(OUT), 5u...	219.25452k	219.56297k	222.77175k
☑	SlewRate_Fall_XRange(V(OUT), 25u...	-232.75125k	-232.83532k	-235.54321k

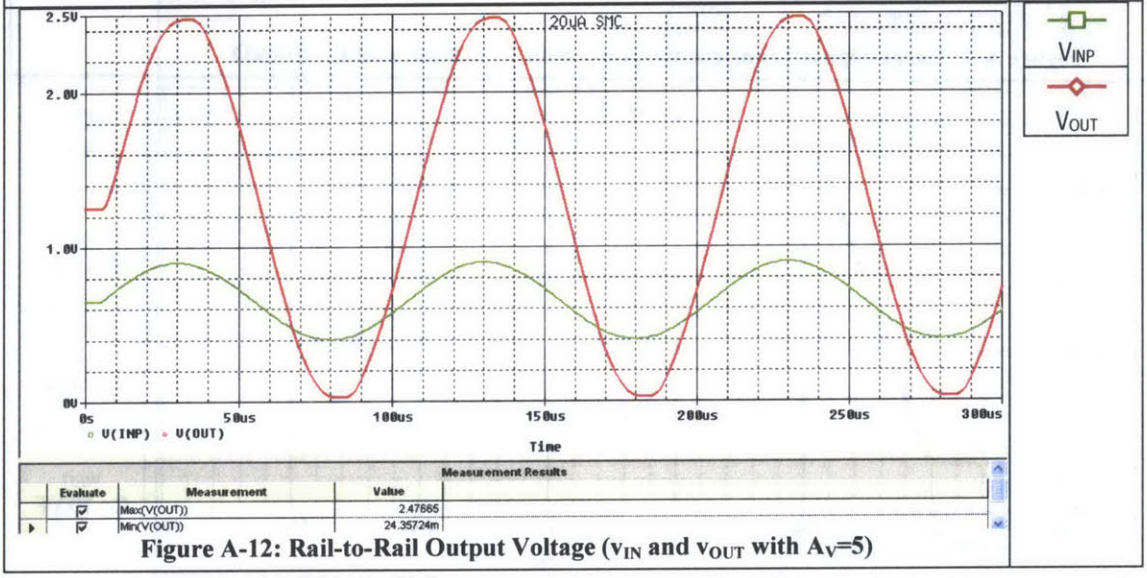
Figure A-10: Large-Signal Transient Response with C_L=0, 10, 100pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	Value
☑	YatX(-ID(MM2P), 0.0mA)	10.16430u
☑	YatX(ID(MM2N), 0.0mA)	10.16428u
☑	YatX(-ID(MM2P), 0.5mA)	504.66380u
☑	YatX(ID(MM2N), 0.5mA)	4.66385u
☑	YatX(ID(MM2P), 1.0mA)	-1.00399m
☑	YatX(ID(MM2N), 1.0mA)	3.99351u

Figure A-11: Output Transistors Current vs I_{LOAD}



Measurement Results

Evaluate	Measurement	Value
☑	Max(V(OUT))	2.47665
☑	Min(V(OUT))	24.35724m

Figure A-12: Rail-to-Rail Output Voltage (v_{IN} and v_{OUT} with A_V=5)

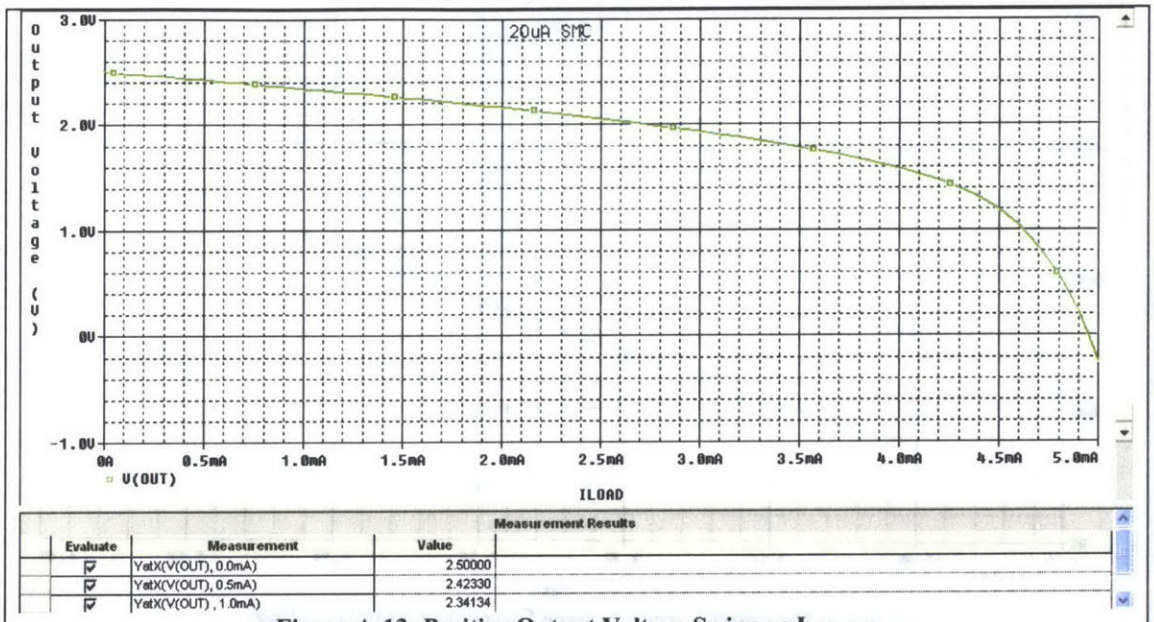


Figure A-13: Positive Output Voltage Swing vs I_{SOURCE}

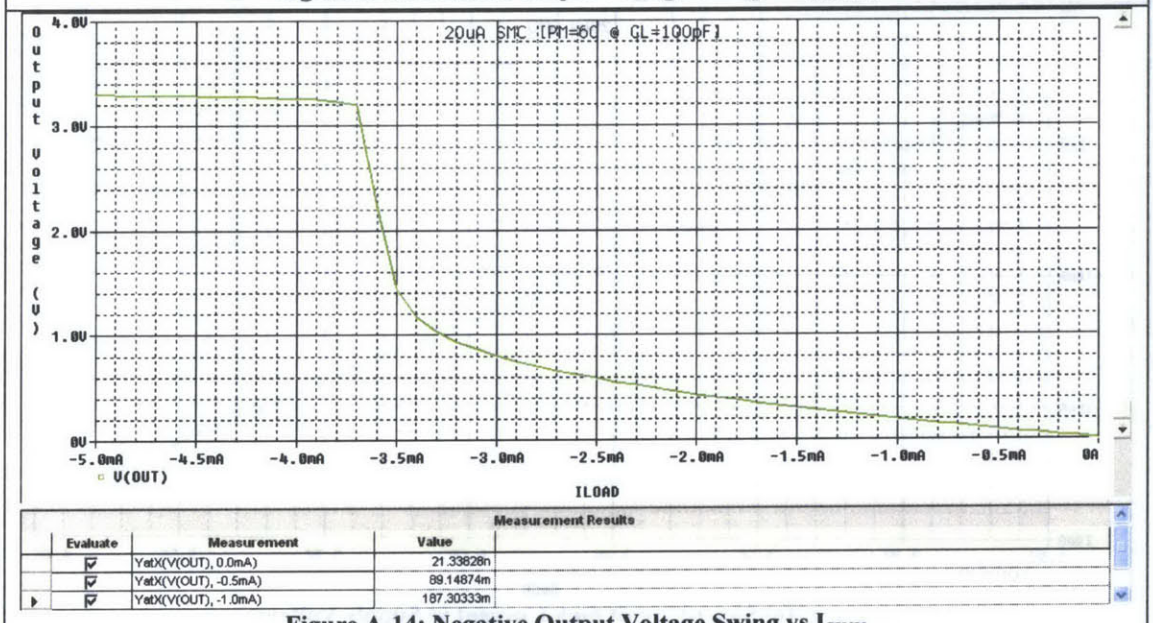


Figure A-14: Negative Output Voltage Swing vs I_{SINK}

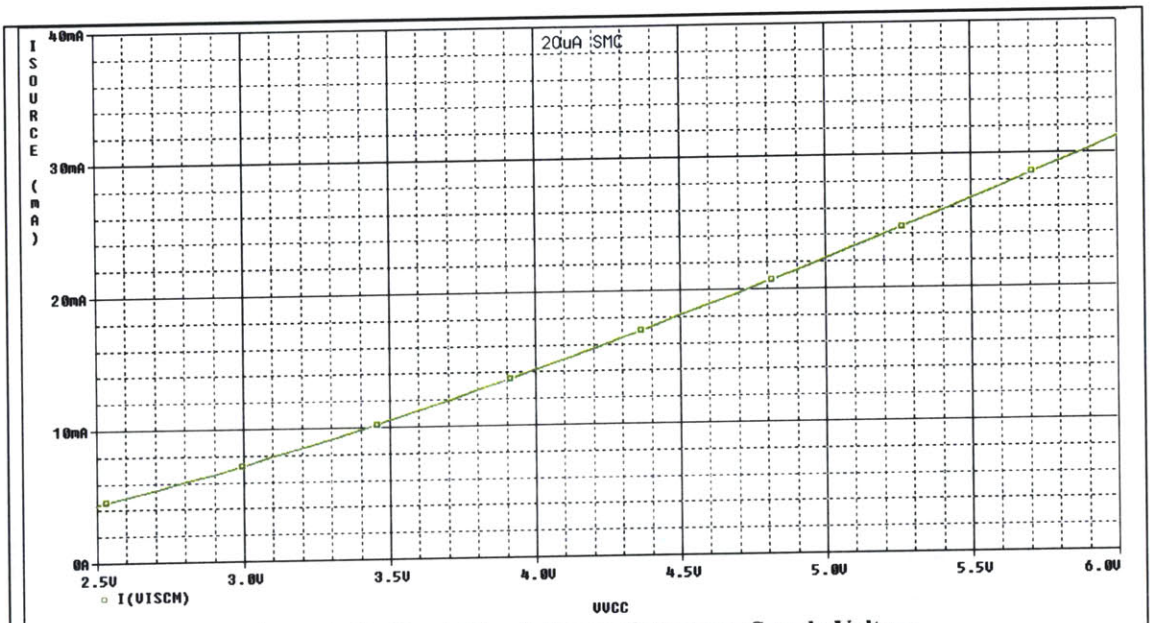


Figure A-15: Short-Circuit Source Current vs Supply Voltage

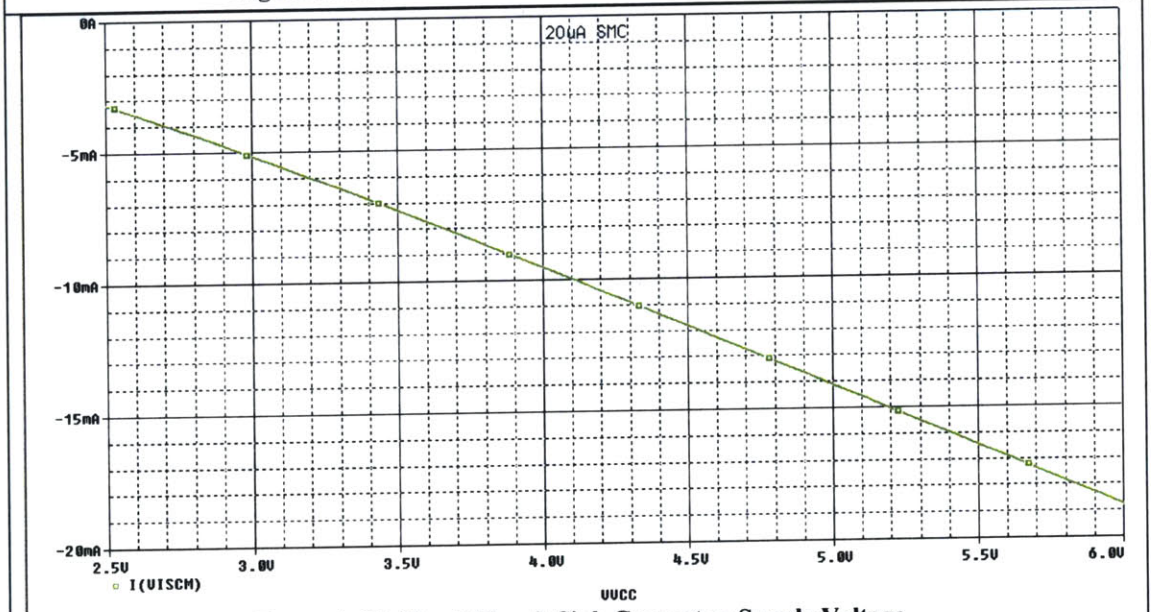
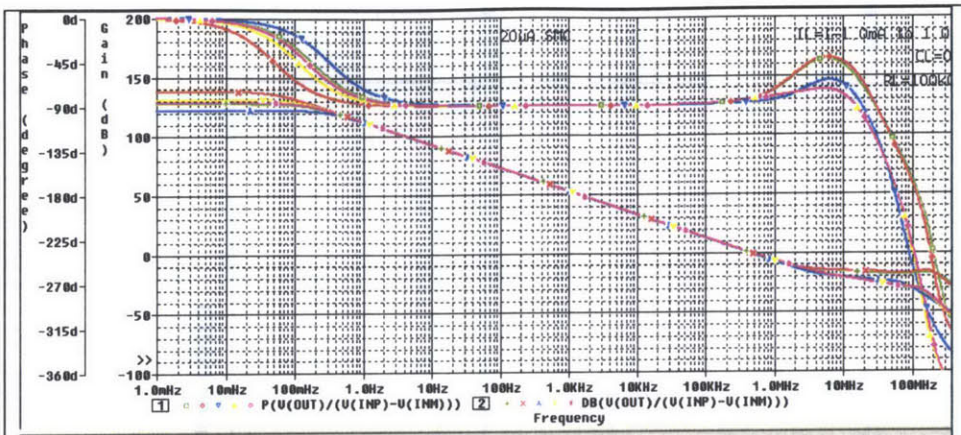


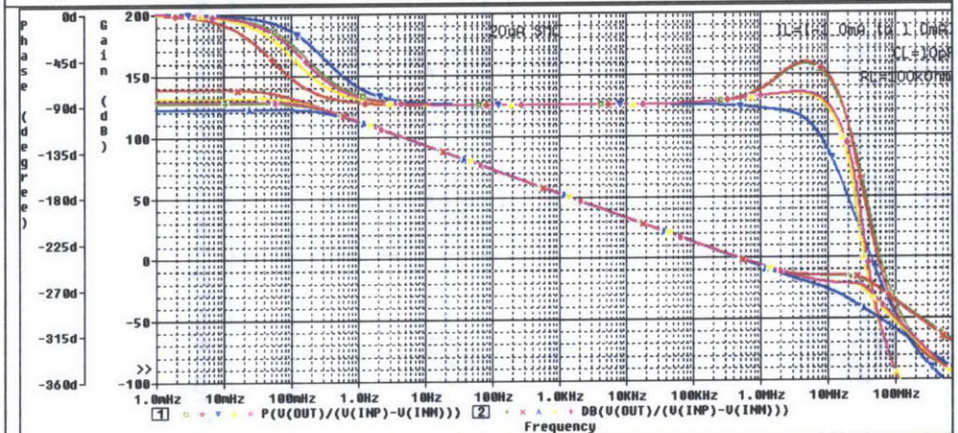
Figure A-16: Short-Circuit Sink Current vs Supply Voltage



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	418.07663k	421.28463k	414.11136k	433.43692k	430.16475k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	95.50545	95.68010	91.70296	94.90656	94.91432
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	18.59197	17.48470	25.91936	28.64230	28.89374
☑	Peak(DB(V(OUT)/(V(INP)-V(INM))), 1)	-17.89259	-16.64812	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

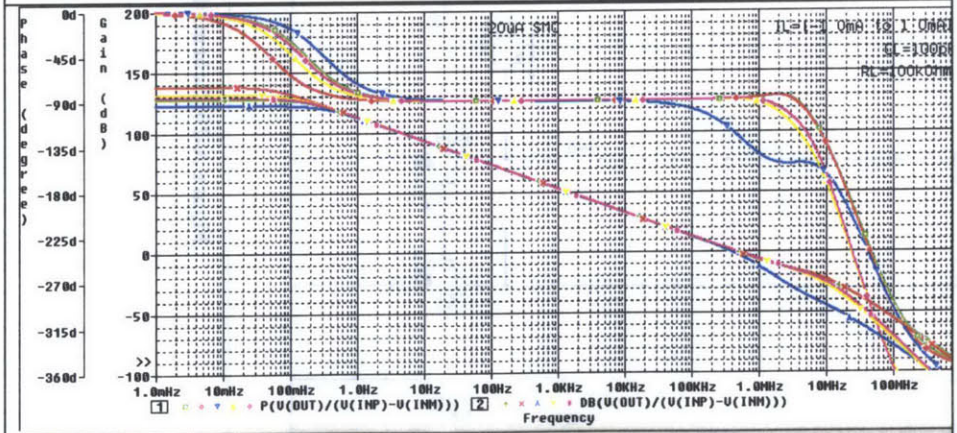
Figure A-17: Frequency Response with C_L=0pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	418.21424k	421.67050k	413.36830k	433.86426k	430.45688k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	94.99161	95.22150	87.91499	94.49051	94.57436
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	20.10780	18.59552	34.44376	22.72739	22.81272

Figure A-18: Frequency Response with C_L=10pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	417.92143k	423.92718k	359.82741k	436.65943k	432.37773k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	90.34538	91.01890	61.47403	90.67716	91.47514
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	32.68559	31.95491	50.98179	29.85602	29.04385

Figure A-19: Frequency Response with C_L=100pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA

I_L (mA)	Symbol
-1.0	Phase Gain
-0.5	Phase Gain
0.0	Phase Gain
0.5	Phase Gain
1.0	Phase Gain

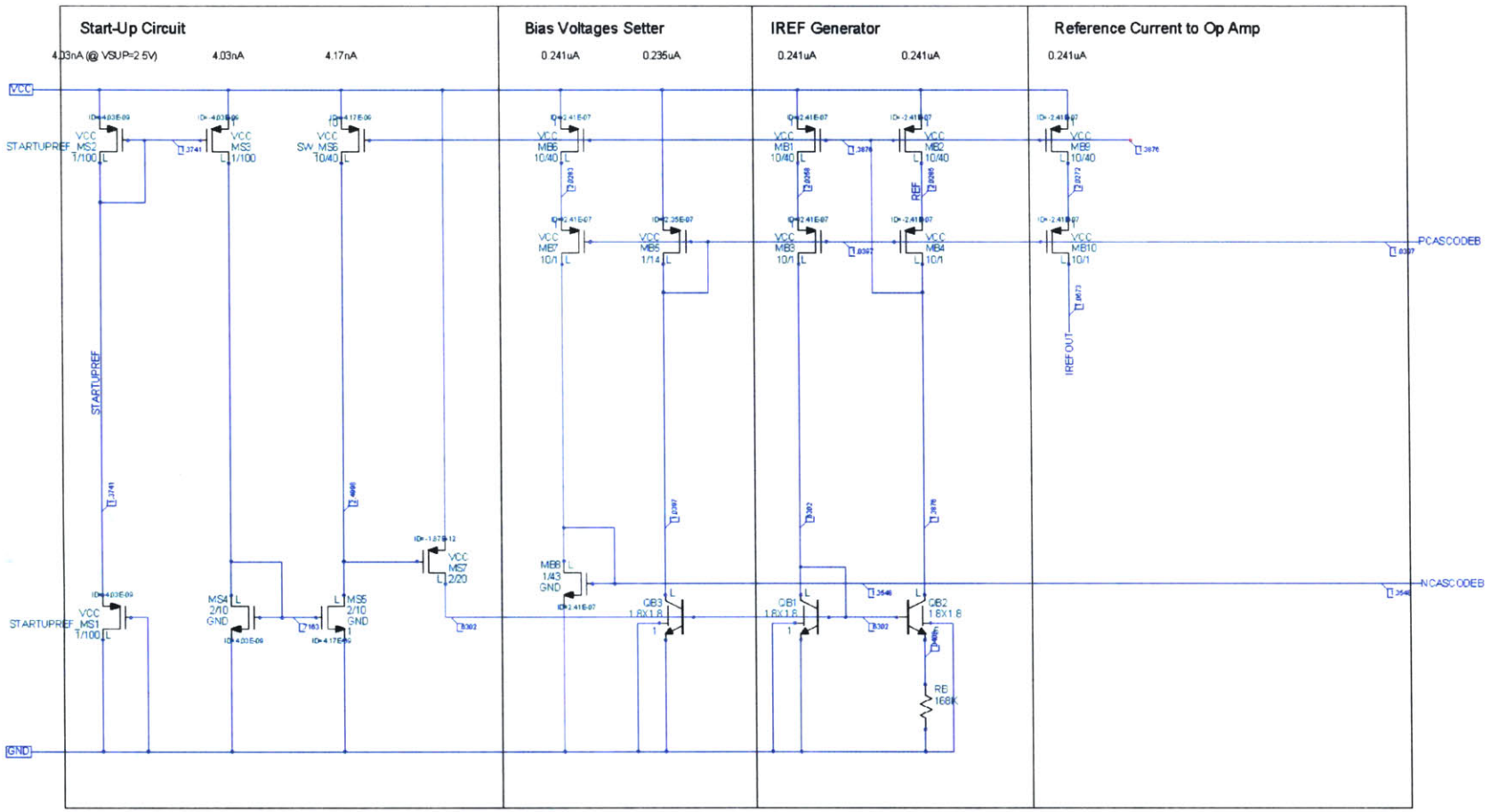
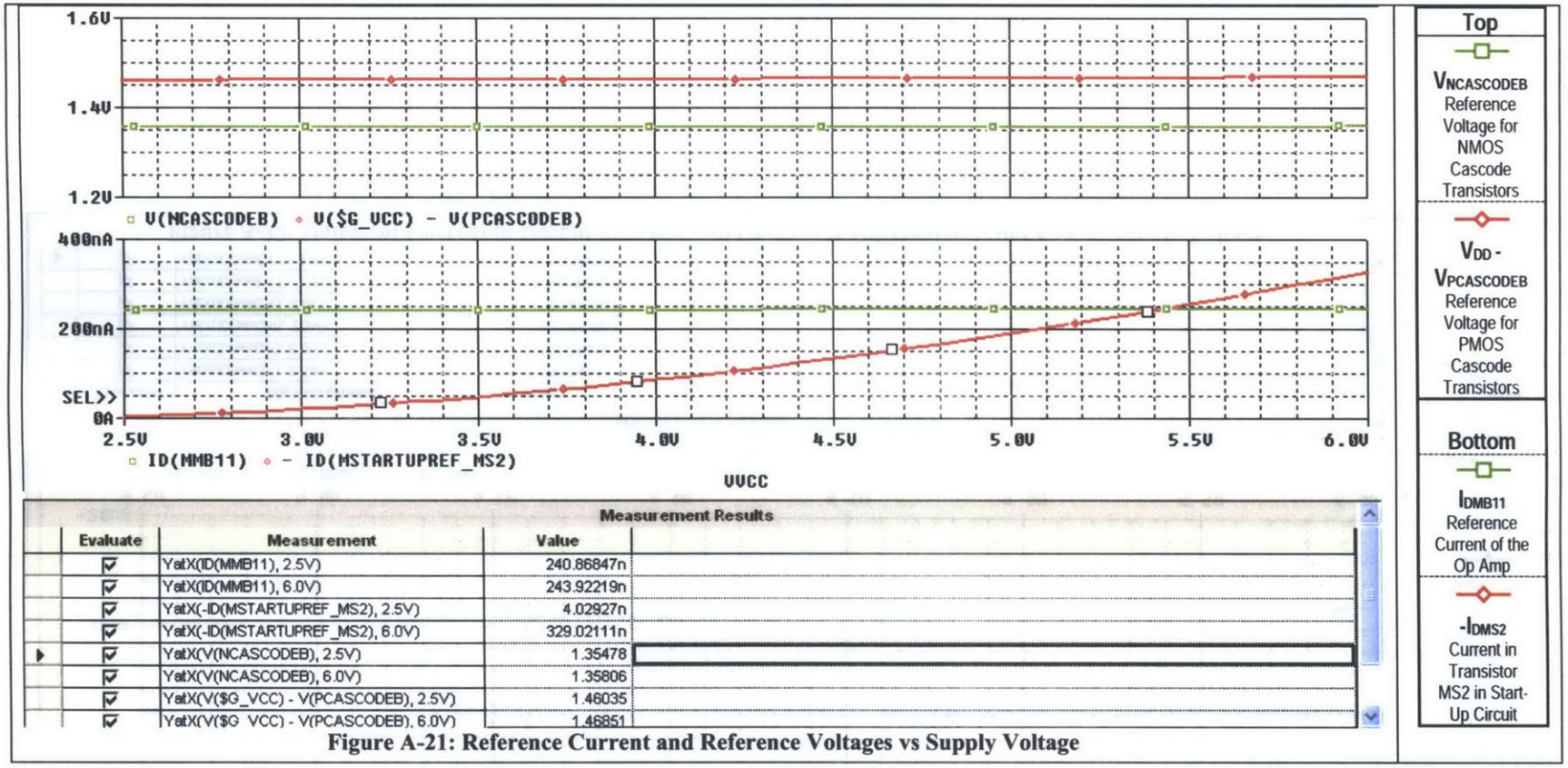


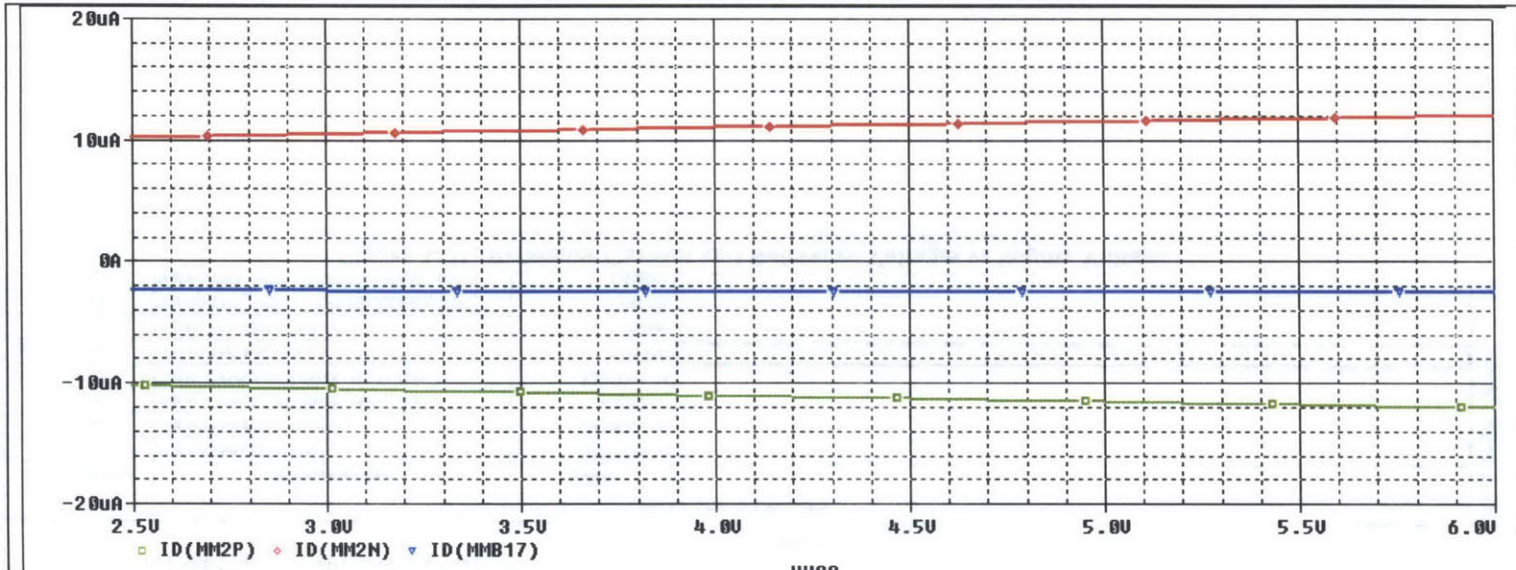
Figure A-20: Schematic of Bias Cell for 20µA Op Amp with Simple Miller Compensation (SMC)



Measurement Results

Evaluate	Measurement	Value
☑	YatX(ID(MMB11), 2.5V)	240.86847n
☑	YatX(ID(MMB11), 6.0V)	243.92219n
☑	YatX(-ID(MSTARTUPREF_MS2), 2.5V)	4.02927n
☑	YatX(-ID(MSTARTUPREF_MS2), 6.0V)	329.02111n
☑	YatX(V(NCASCODEB), 2.5V)	1.35478
☑	YatX(V(NCASCODEB), 6.0V)	1.35806
☑	YatX(V($G_VCC) - V(PCASCODEB), 2.5V)	1.46035
☑	YatX(V($G_VCC) - V(PCASCODEB), 6.0V)	1.46851

Figure A-21: Reference Current and Reference Voltages vs Supply Voltage



Measurement Results

Evaluate	Measurement	Value
☑	YatX(ID(MM2P), 2.5V)	-10.16430u
☑	YatX(ID(MM2P), 6.0V)	-12.06189u
☑	YatX(ID(MM2N), 2.5V)	10.16428u
☑	YatX(ID(MM2N), 6.0V)	12.06226u
☑	YatX(ID(MMB17), 2.5V)	-2.40866u
☑	YatX(ID(MMB17), 6.0V)	-2.43992u

Figure A-22: Quiescent Current in Output Pair and Tail Current in Differential Input Pair vs Supply Voltage

Appendix B Schematics and Characteristics of 20μA Micropower Op Amp with Hybrid Explicit Cascode Compensation (HECC)

LIST OF FIGURES IN APPENDIX B

Table B: Characteristics of 20μA Micropower Op Amp with Hybrid Explicit Cascode Compensation (HECC) from Simulation

Simulation results are at 25°C. V_{DD} = 2.5V and V_{SS} = 0V.						
Primary Characteristics						
Symbol	**Parameter**		**Condition**	**Value**		**Unit**
				Specified	**Simulated**	
GBW[18]	**Gain Bandwidth Product**		C_L = 100pF R_L = 100kΩ	**> 0.3**	**0.507** (Φ_M = 61.2°)	**MHz**
A_{VOL}	**Large-Signal Voltage Gain** **(DC Open-Loop Gain)**		C_L = 100pF R_L = 100kΩ	**> 100**	**120**	**dB**
I_S	**Supply Current**		No Load	**< 21**	**19.88**	**μA**
V_{INCM}[19]	Input Common-Mode Range		-	> V_{DD} - 1.25V and must include negative supply voltage	**1.3** and includes negative supply voltage	V
V_{OS}[20]	(Untrimmed) Input Offset Voltage		V_{INCM} = 0.65V	< 5	**4.83**	mV
V_{OUT}	V_{OUTH}	High Output Voltage	I_{SOURCE} = 1.0mA	> V_{DD} - 0.3V	**2.34**	V
	V_{OUTL}	Low Output Voltage	I_{SINK} = 1.0mA	< V_{SS} + 0.3V	**0.19**	V
I_{SOURCE}[21]	Output Source Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.55**	mA
I_{SINK}	Output Sink Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.04**	mA
Secondary Characteristics						
Symbol	**Parameter**		**Condition**	**Value**		**Unit**
				Specified	**Simulated**	
SR+	Positive Going Slew Rate		A_V = 1V/V, 1V Step	> 0.15	**0.271**	V/μs
SR-	Negative Going Slew Rate		A_V = 1V/V, 1V Step	< -0.15	**-0.298**	V/μs

[18] Gain bandwidth product per supply current GBW/ I_S = 25.5MHz/mA @ C_L = 100pF.
[19] Verified by CMRR simulation in Figure B-4.
[20] Conservative estimate from calculation.
[21] Maximum output source current is measured when the other transistor in the output pair starts to turn off, i.e. its current goes down to as low as 1μA.

CMRR	Common Mode Rejection Ratio	@ DC	> 60	**126**	dB
PSRR+	Positive Power Supply Rejection Ratio	@ DC	> 60	**72.4**	dB
PSRR-	Negative Power Supply Rejection Ratio	@ DC	> 60	**62.7**	dB
t_s	0.1% Settling Time	A_V = 1V/V, 1V Step	< 10	**4.40**	µs

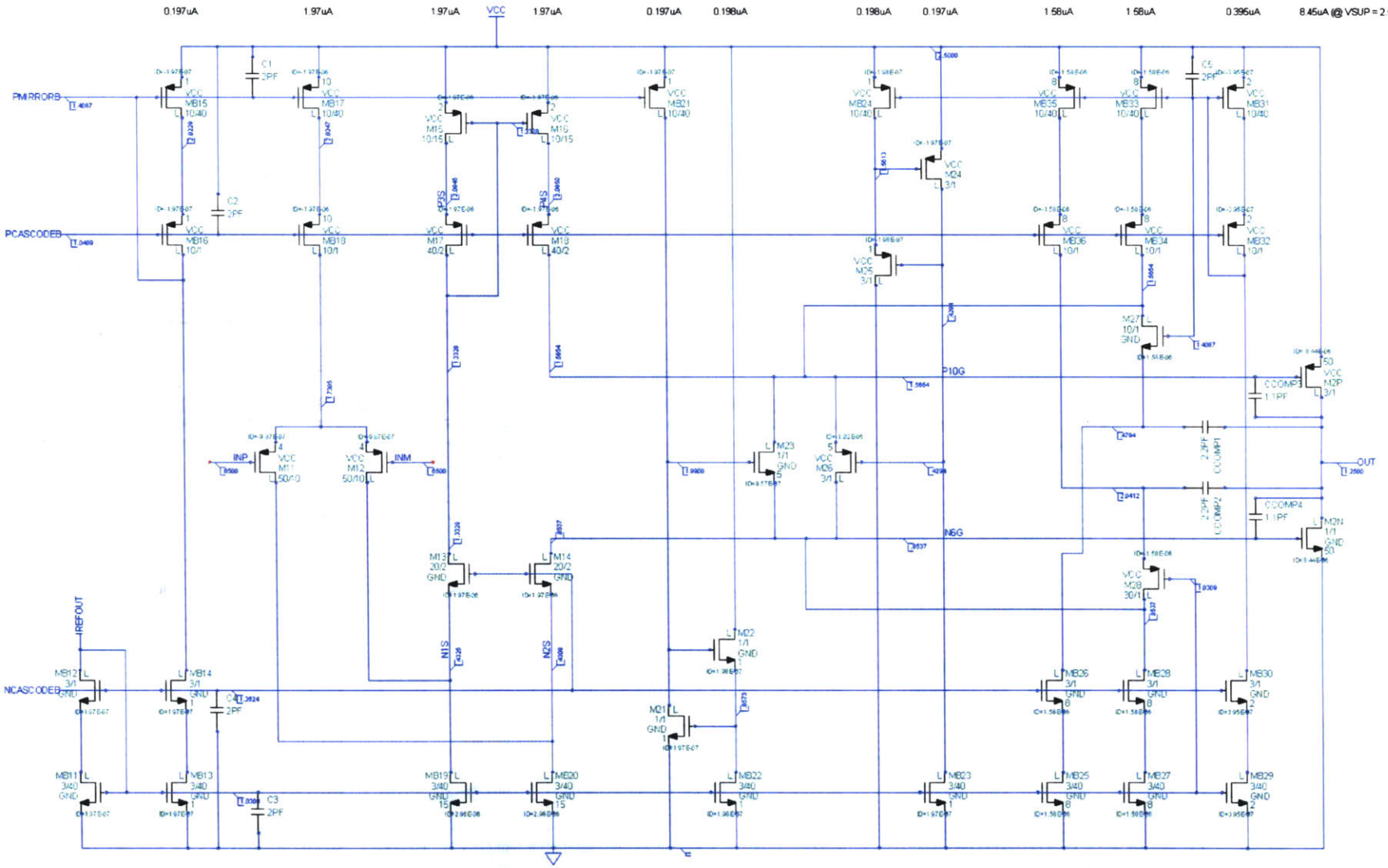
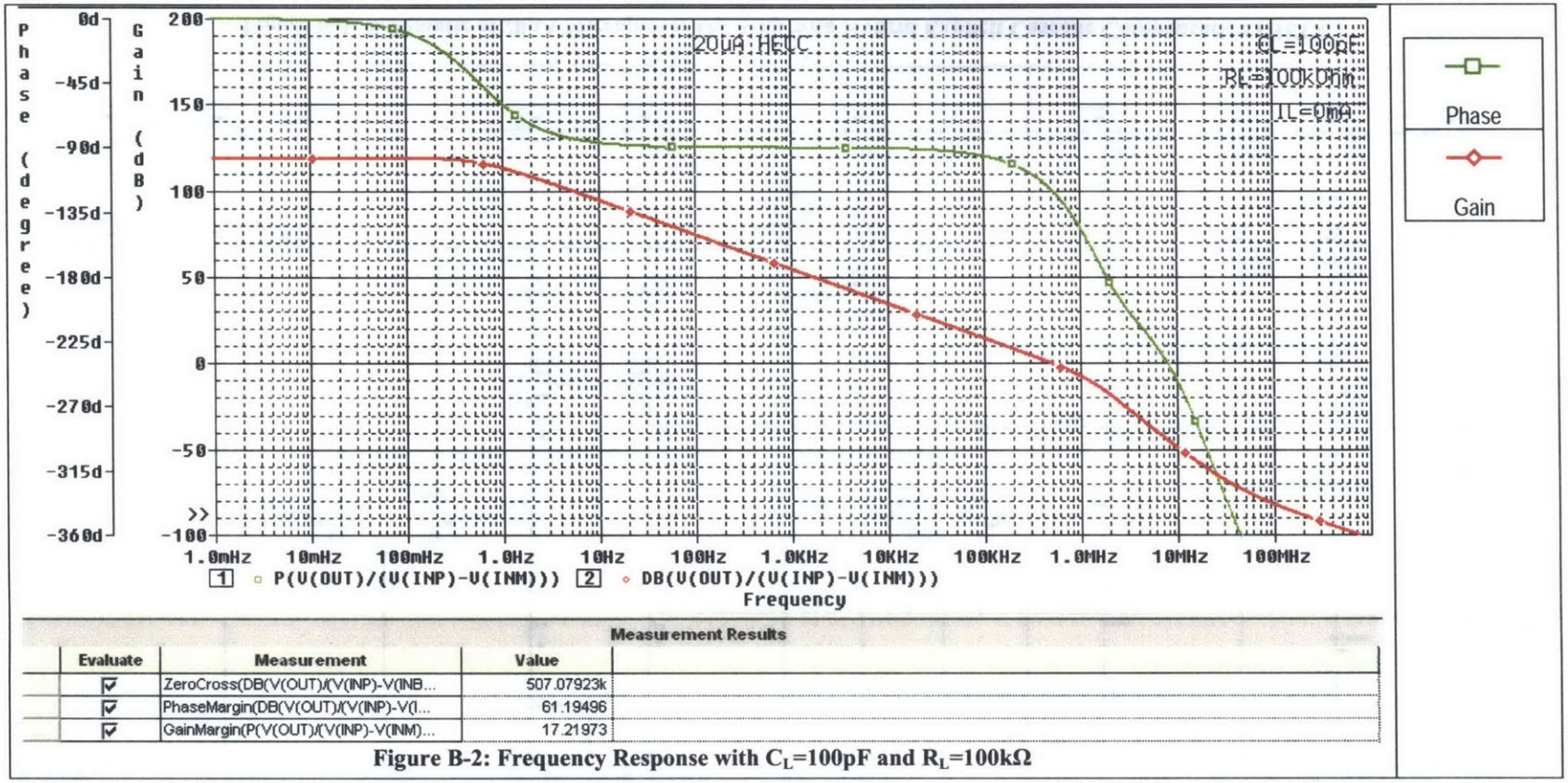


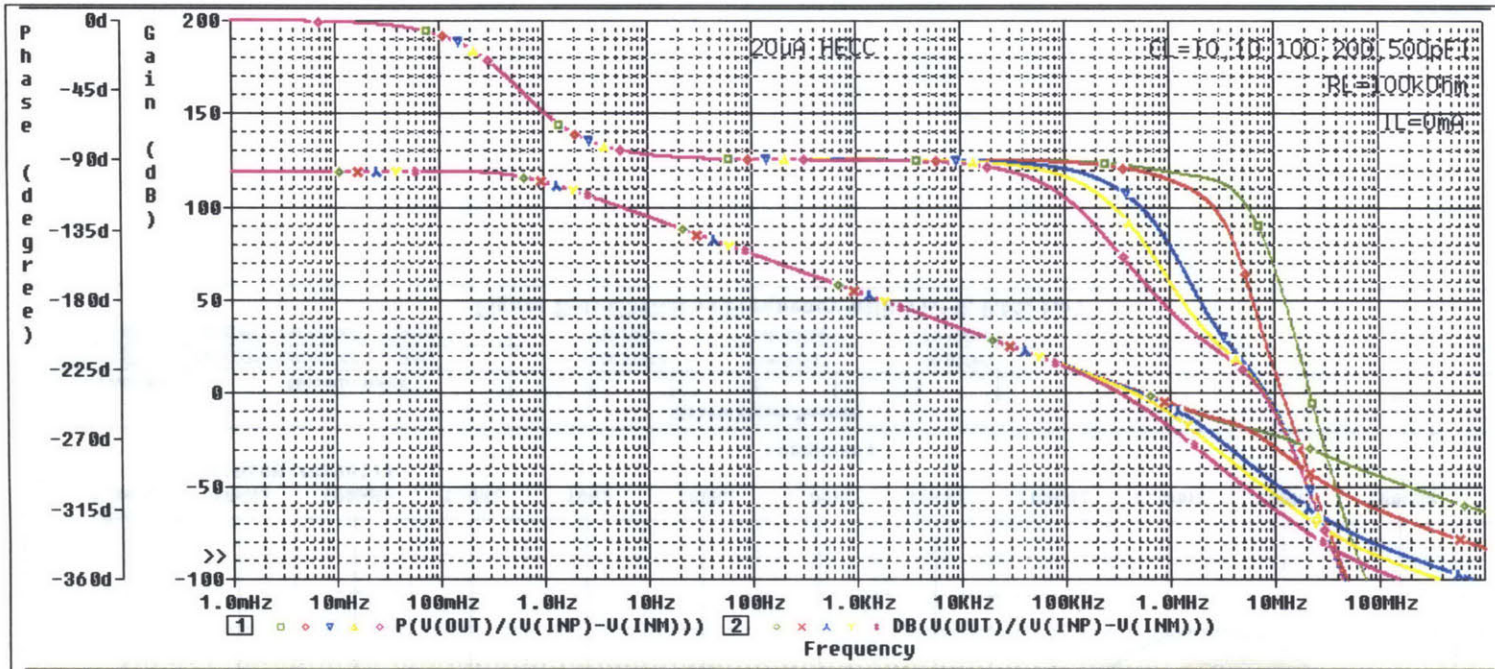
Figure B-1: Schematic of 20µA Micropower Op Amp with Hybrid Explicit Cascode Compensation (HECC)



Measurement Results

Evaluate	Measurement	Value
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INB...	507.07923k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	61.19496
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	17.21973

Figure B-2: Frequency Response with C_L=100pF and R_L=100kΩ

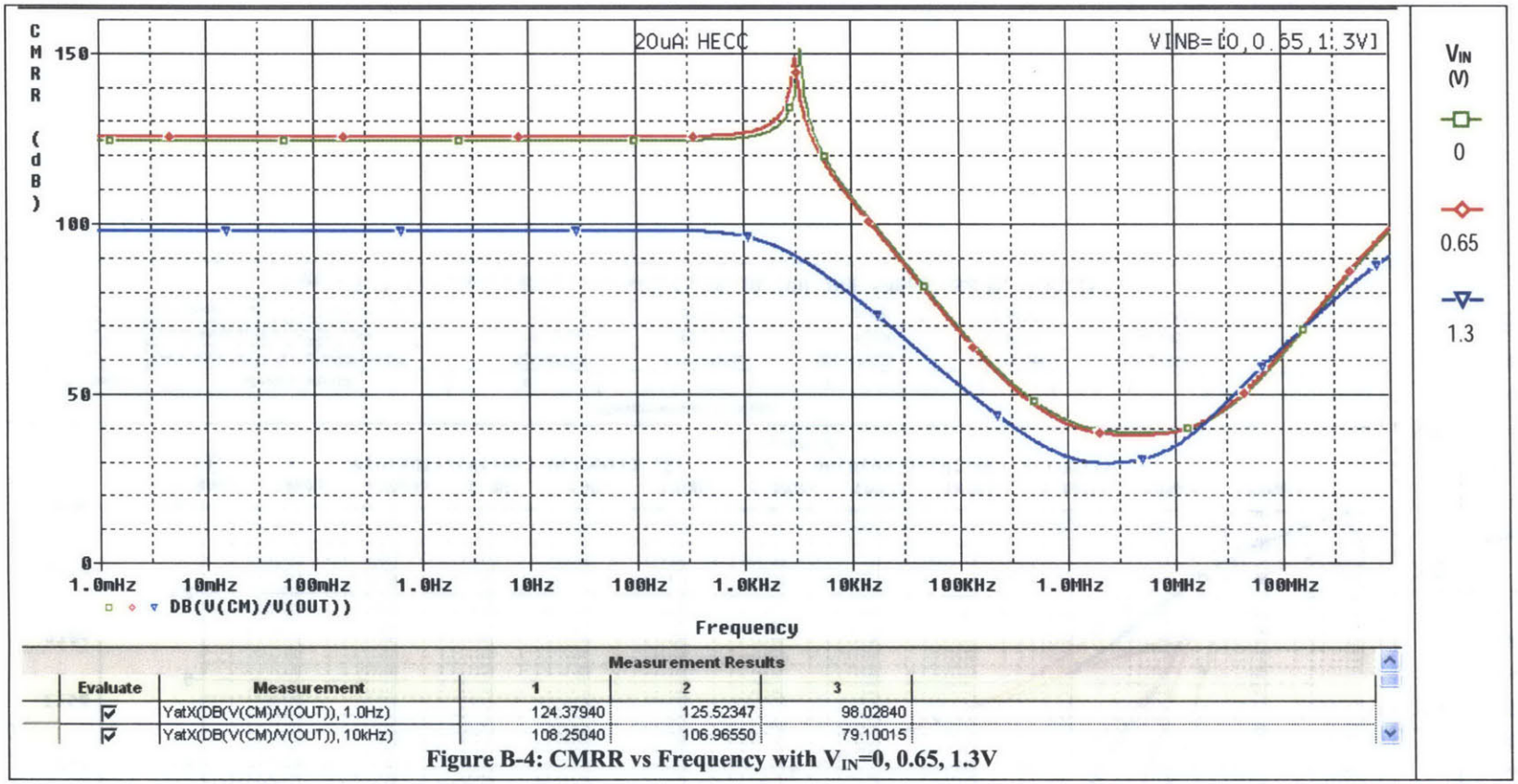


C_L (pF)	Symbol
0	Phase, Gain
10	Phase, Gain
100	Phase, Gain
200	Phase, Gain
500	Phase, Gain

Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INB...	529.42157k	531.57973k	507.07923k	445.03026k	325.27533k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	85.29589	82.68383	61.19496	46.91552	30.42577
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	24.51848	21.11787	17.21973	15.84261	14.65101

Figure B-3: Frequency Response with C_L=0, 10, 100, 200, 500pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	1	2	3
☑	YatX(DB(V(CM)/V(OUT)), 1.0Hz)	124.37940	125.52347	98.02840
☑	YatX(DB(V(CM)/V(OUT)), 10kHz)	108.25040	106.96550	79.10015

Figure B-4: CMRR vs Frequency with V_{IN}=0, 0.65, 1.3V

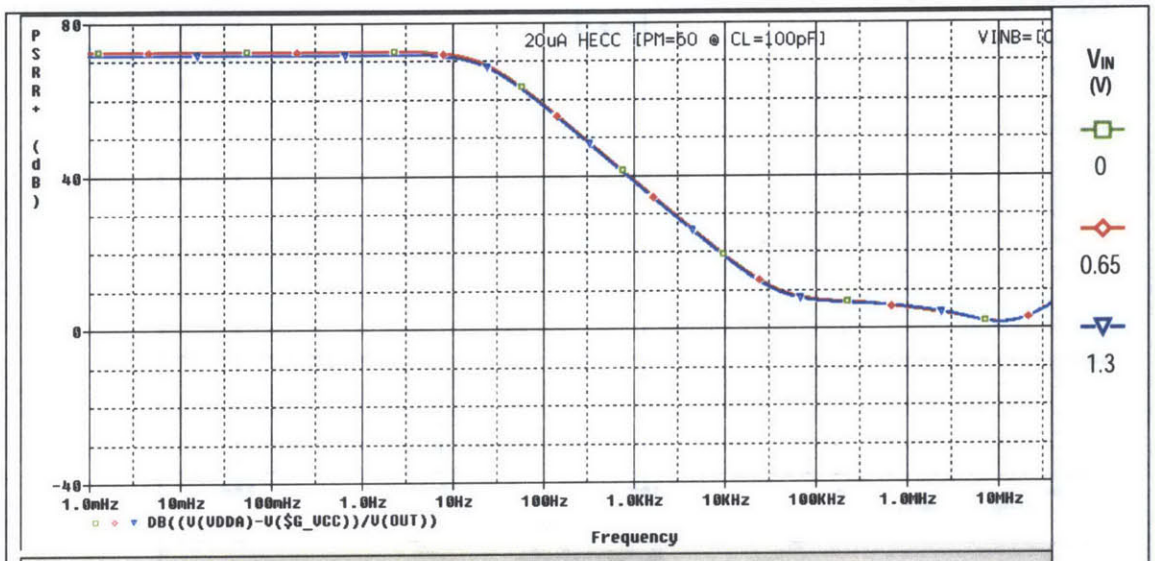


Figure B-5: PSRR+ vs Frequency with V_{IN}=0, 0.65, 1.3V

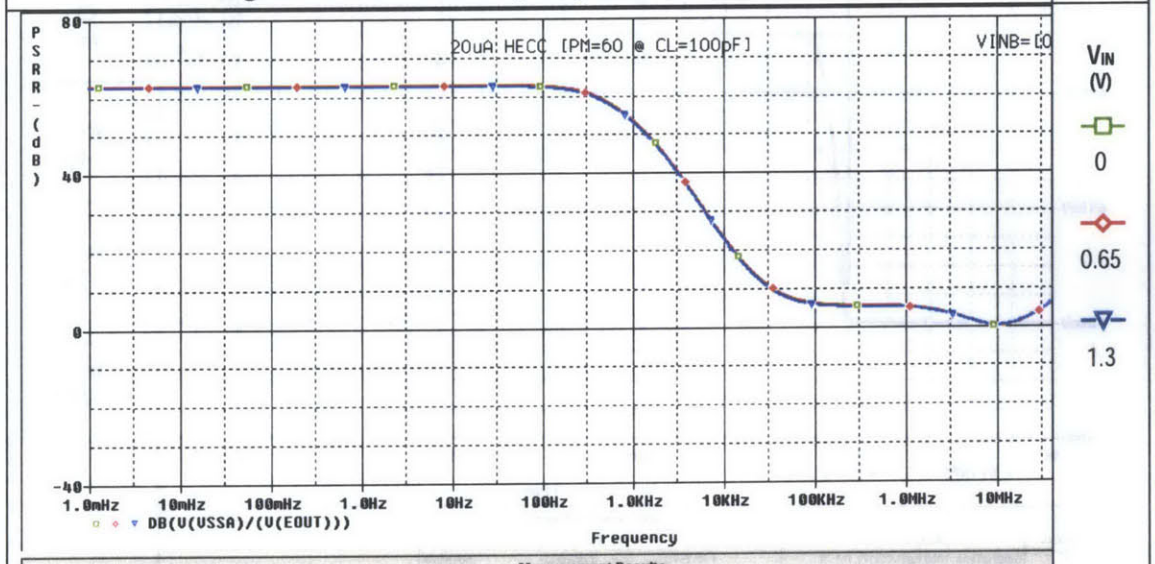


Figure B-6: PSRR- vs Frequency with V_{IN}=0, 0.65, 1.3V

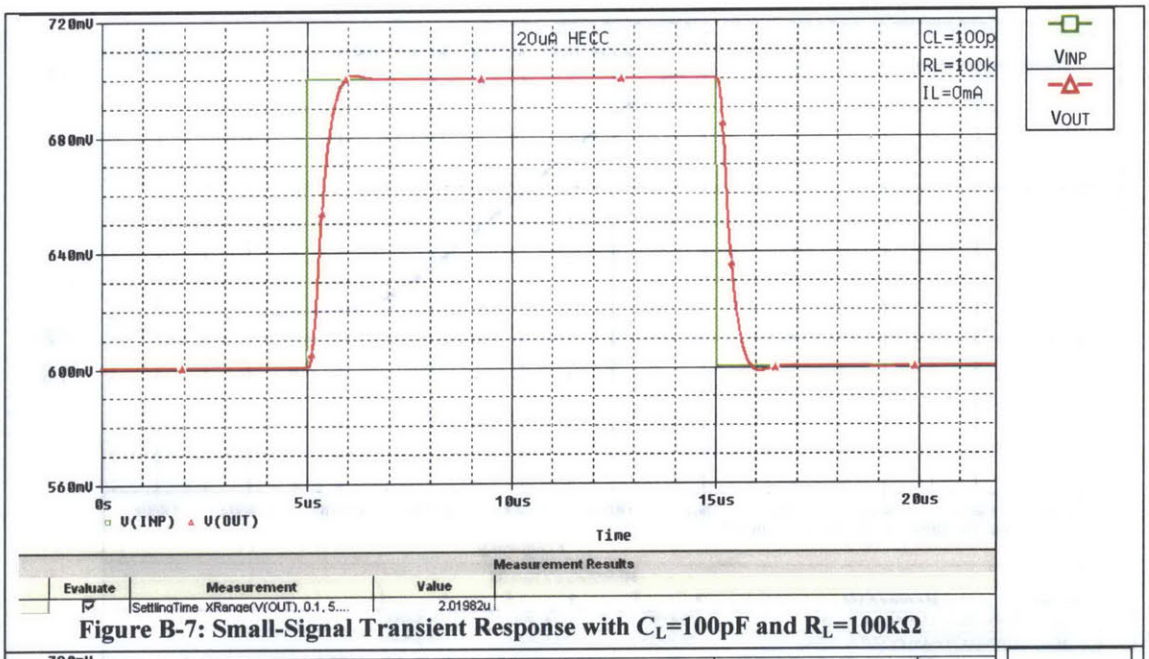


Figure B-7: Small-Signal Transient Response with C_L=100pF and R_L=100kΩ

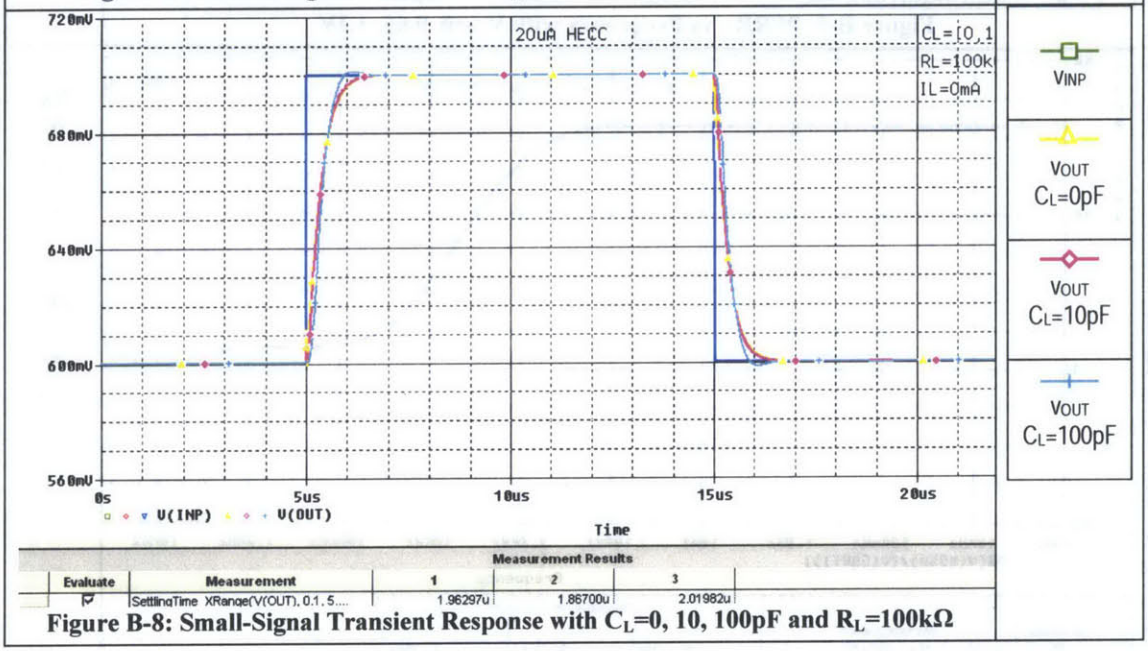
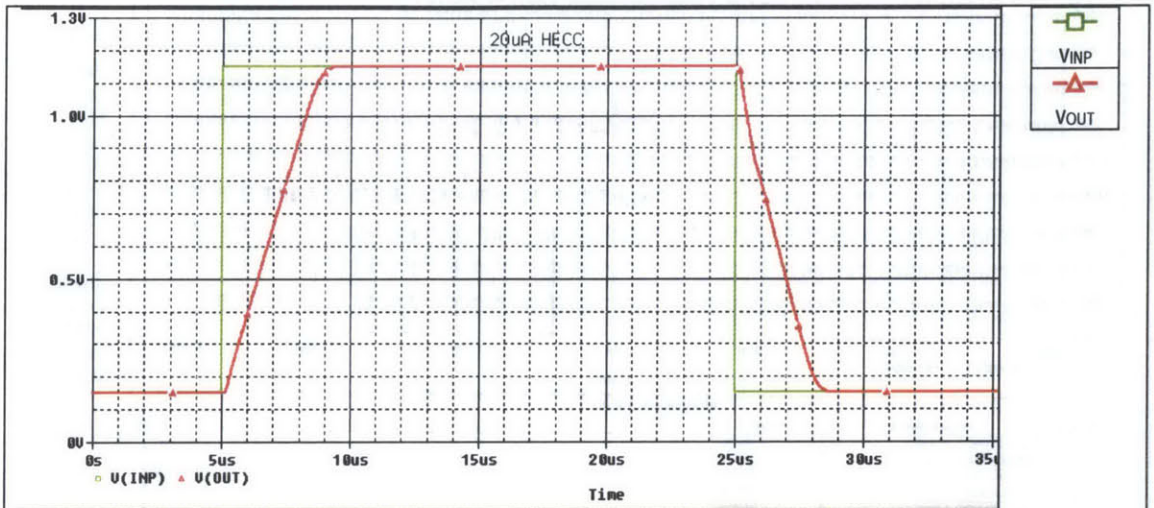


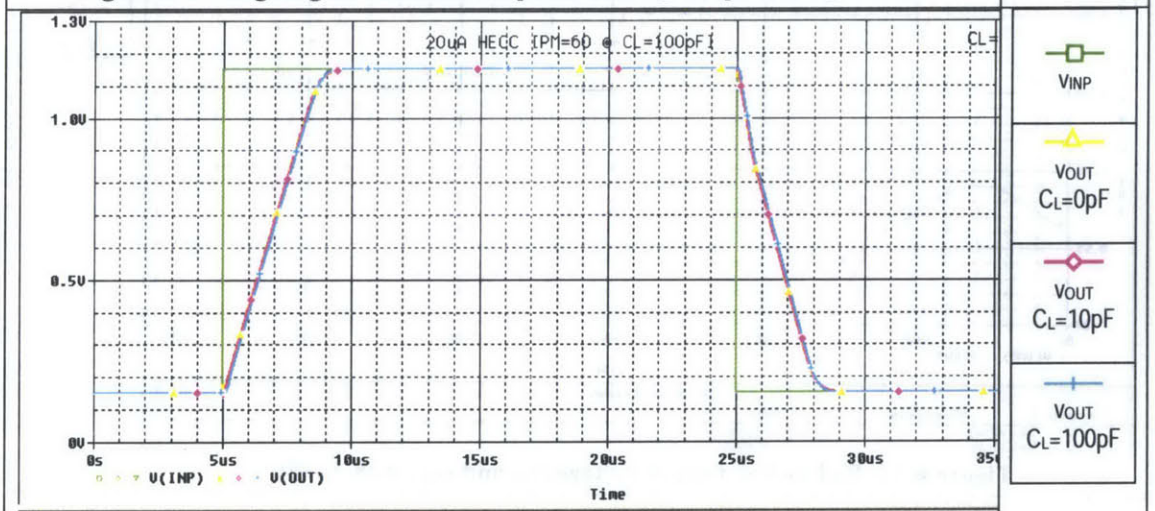
Figure B-8: Small-Signal Transient Response with C_L=0, 10, 100pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	Value
☑	SettlingTime_XRange(V(OUT), 0.1, 5u...	4.40273u
☑	SlewRate_Rise_XRange(V(OUT), 5u...	270.95672k
☑	SlewRate_Fall_XRange(V(OUT), 25u...	-298.15344k

Figure B-9: Large-Signal Transient Response with C_L=100pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	1	2	3
☑	SettlingTime_XRange(V(OUT), 0.1, 5u...	4.84287u	4.81335u	4.40273u
☑	SlewRate_Rise_XRange(V(OUT), 5u...	268.58725k	268.86134k	270.95671k
☑	SlewRate_Fall_XRange(V(OUT), 25u...	-299.53399k	-299.25452k	-298.15351k

Figure B-10: Large-Signal Transient Response with C_L=0, 10, 100pF and R_L=100kΩ

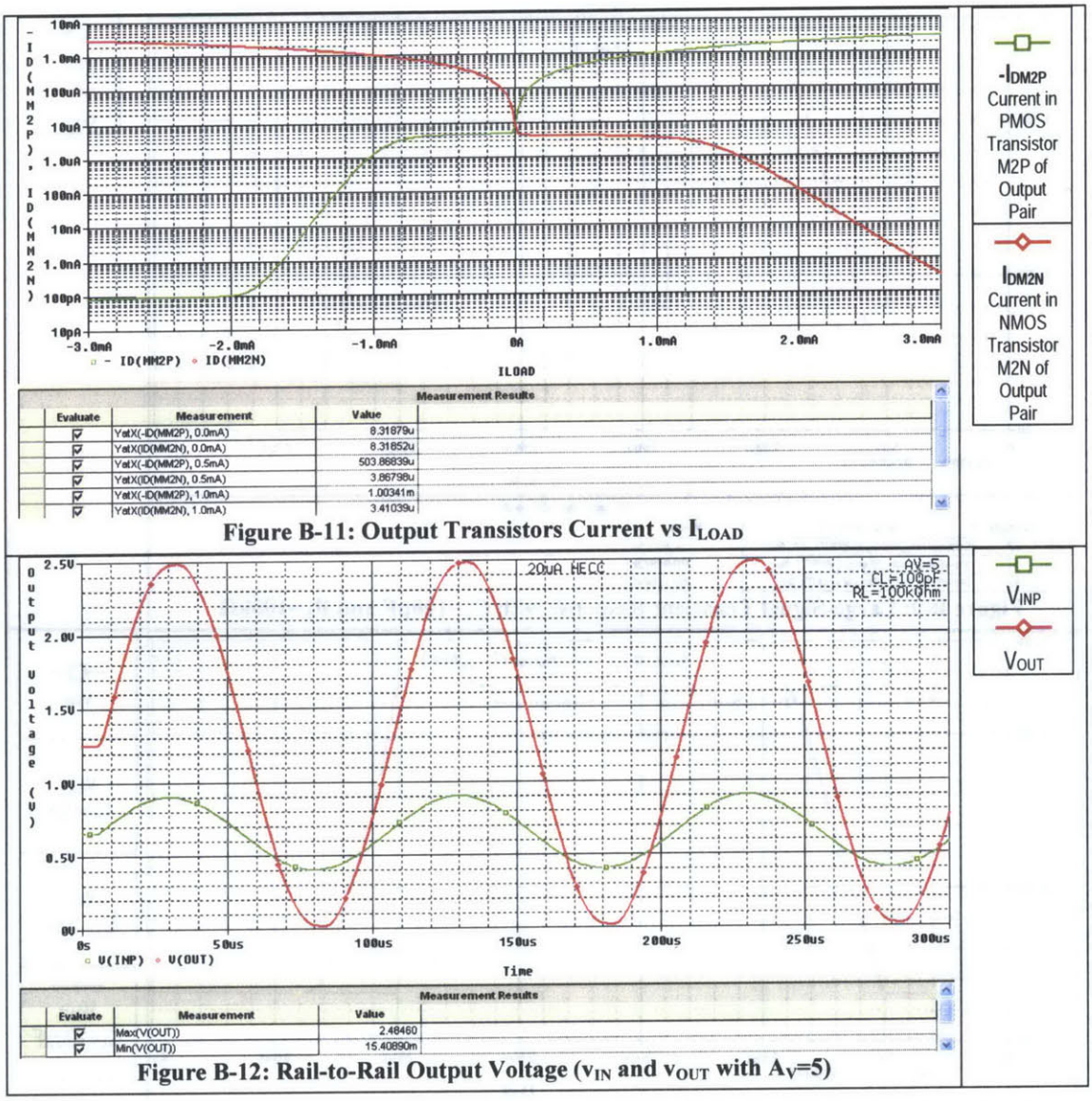
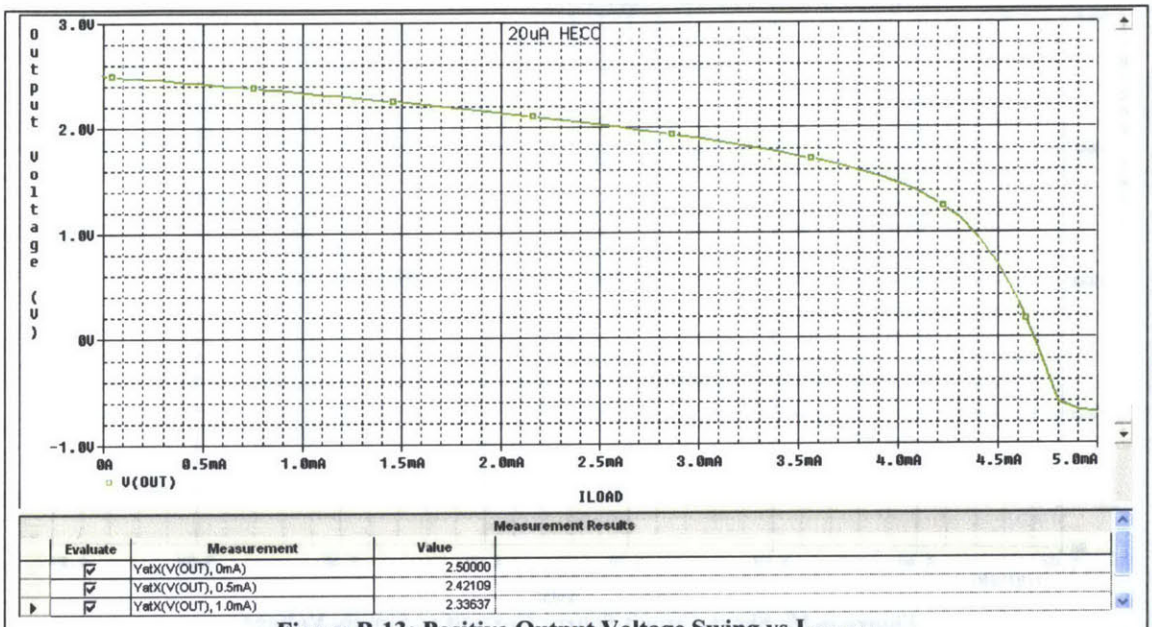


Figure B-11: Output Transistors Current vs I_{LOAD}

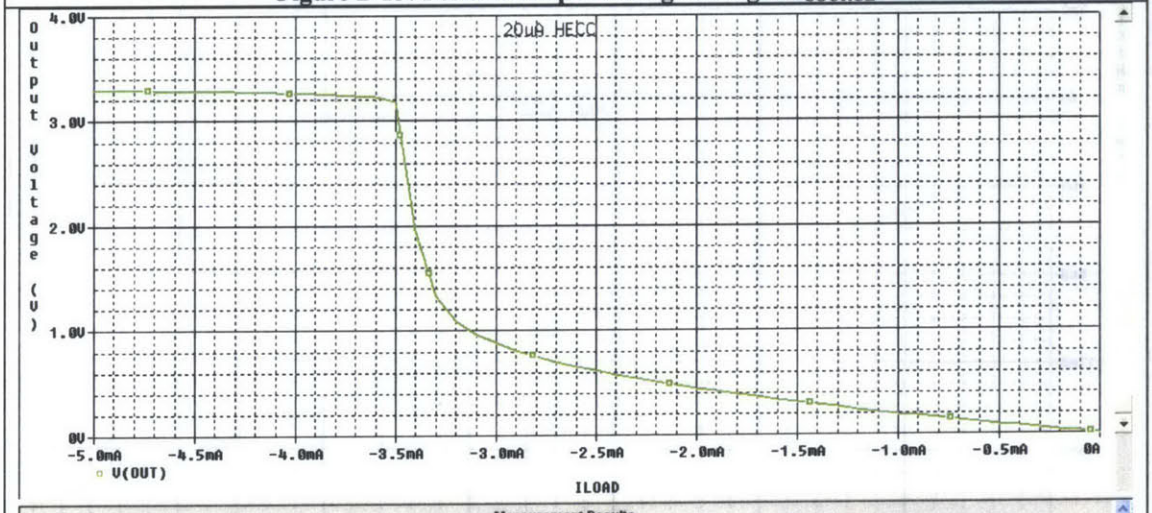
Figure B-12: Rail-to-Rail Output Voltage (v_{IN} and v_{OUT} with A_V=5)



Measurement Results

Evaluate	Measurement	Value
☑	YatX(V(OUT), 0mA)	2.50000
☑	YatX(V(OUT), 0.5mA)	2.42109
☑	YatX(V(OUT), 1.0mA)	2.33637

Figure B-13: Positive Output Voltage Swing vs I_{SOURCE}



Measurement Results

Evaluate	Measurement	Value
☑	YatX(V(OUT) , 0mA)	21.90152n
☑	YatX(V(OUT), -0.5mA)	91.73155m
☑	YatX(V(OUT), -1.0mA)	193.36736m

Figure B-14: Negative Output Voltage Swing vs I_{SINK}

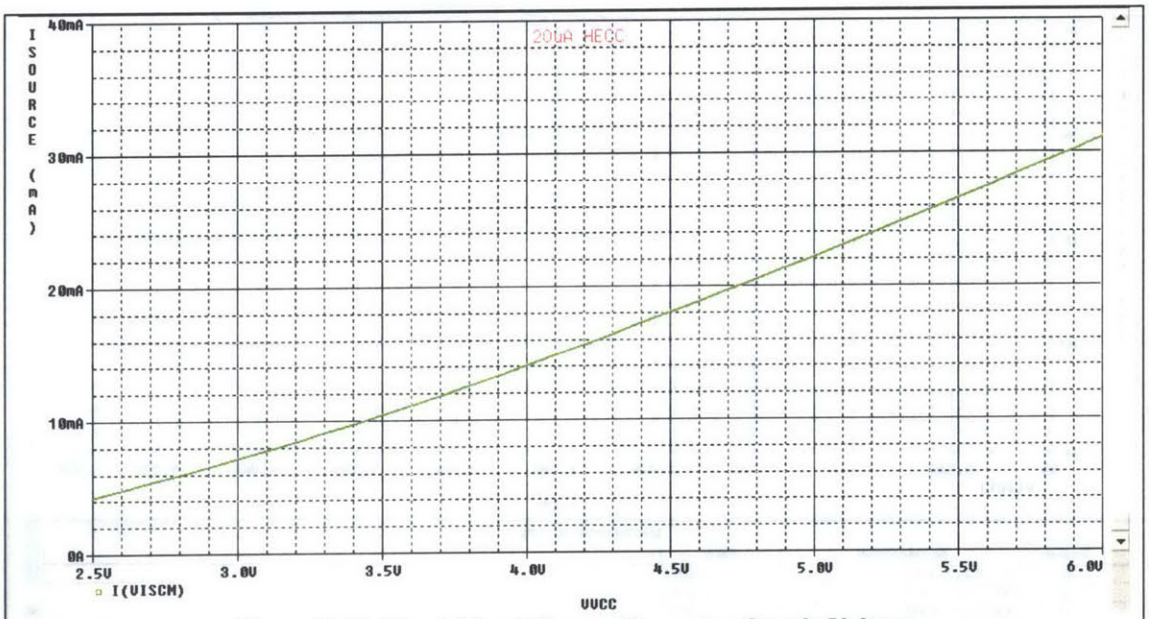


Figure B-15: Short-Circuit Source Current vs Supply Voltage

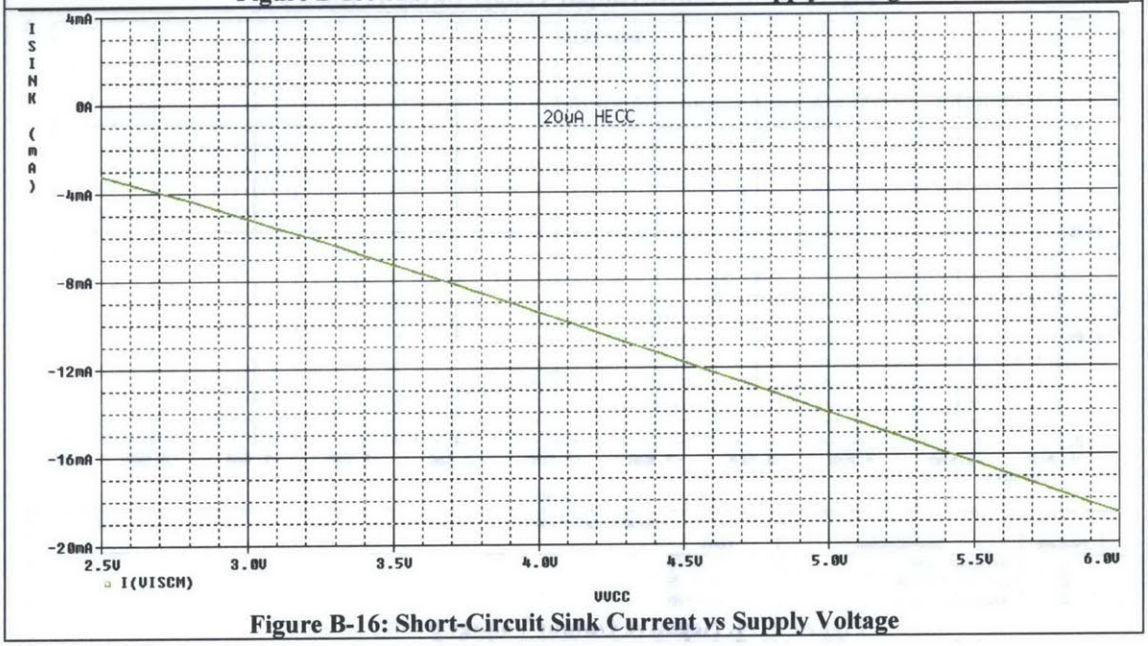
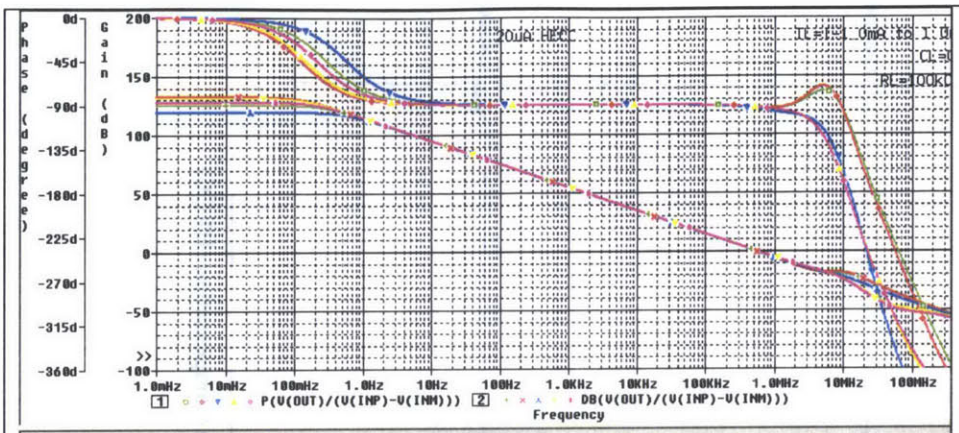


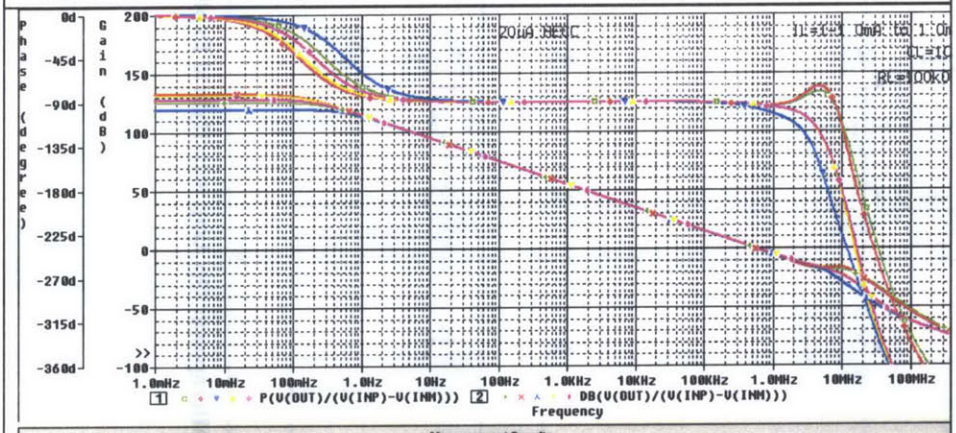
Figure B-16: Short-Circuit Sink Current vs Supply Voltage



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	528.89464k	529.87237k	529.42157k	539.81927k	538.11436k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	87.12035	87.18727	85.29589	86.76815	86.77688
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	28.81183	27.49626	24.51847	26.17053	26.28977
☑	Peak(DB(V(OUT)/(V(INP)-V(INM))), 1)	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

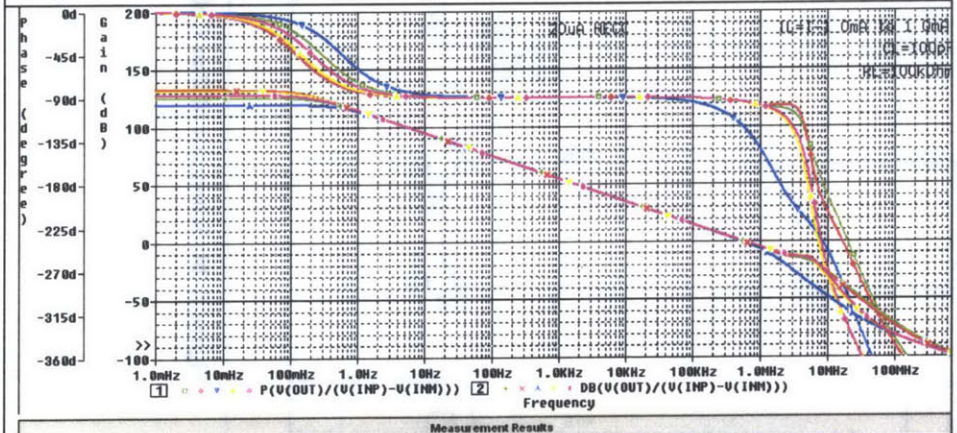
Figure B-17: Frequency Response with C_L=0pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	529.23750k	530.24913k	531.57973k	540.22721k	538.42925k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	86.84758	86.95542	82.68383	86.52456	86.58145
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	24.93064	22.37302	21.11787	22.67337	23.49443
☑	Peak(DB(V(OUT)/(V(INP)-V(INM))), 1)	<Evaluation Failed>	-16.83024	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

Figure B-18: Frequency Response with C_L=10pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	531.84333k	533.31947k	507.07923k	543.52150k	541.02001k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	84.36594	84.84181	61.19496	84.30372	84.80643
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	24.38642	19.28923	17.21973	14.99323	15.94021
☑	Peak(DB(V(OUT)/(V(INP)-V(INM))), 1)	<Evaluation Failed>	-14.01218	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

Figure B-19: Frequency Response with C_L=100pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA

I_L (mA)	Symbol
-1.0	Phase Gain
-0.5	Phase Gain
0.0	Phase Gain
0.5	Phase Gain
1.0	Phase Gain

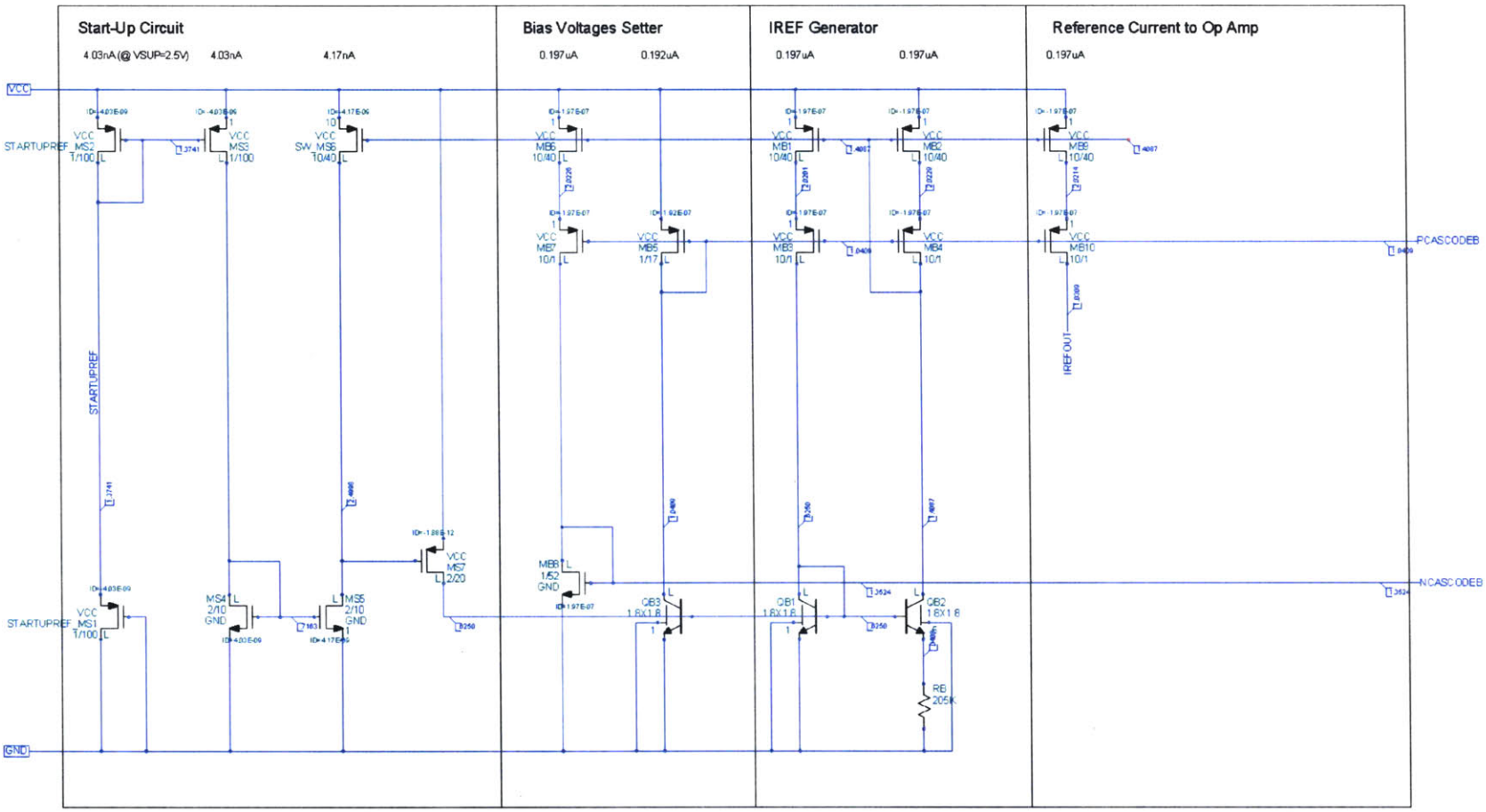
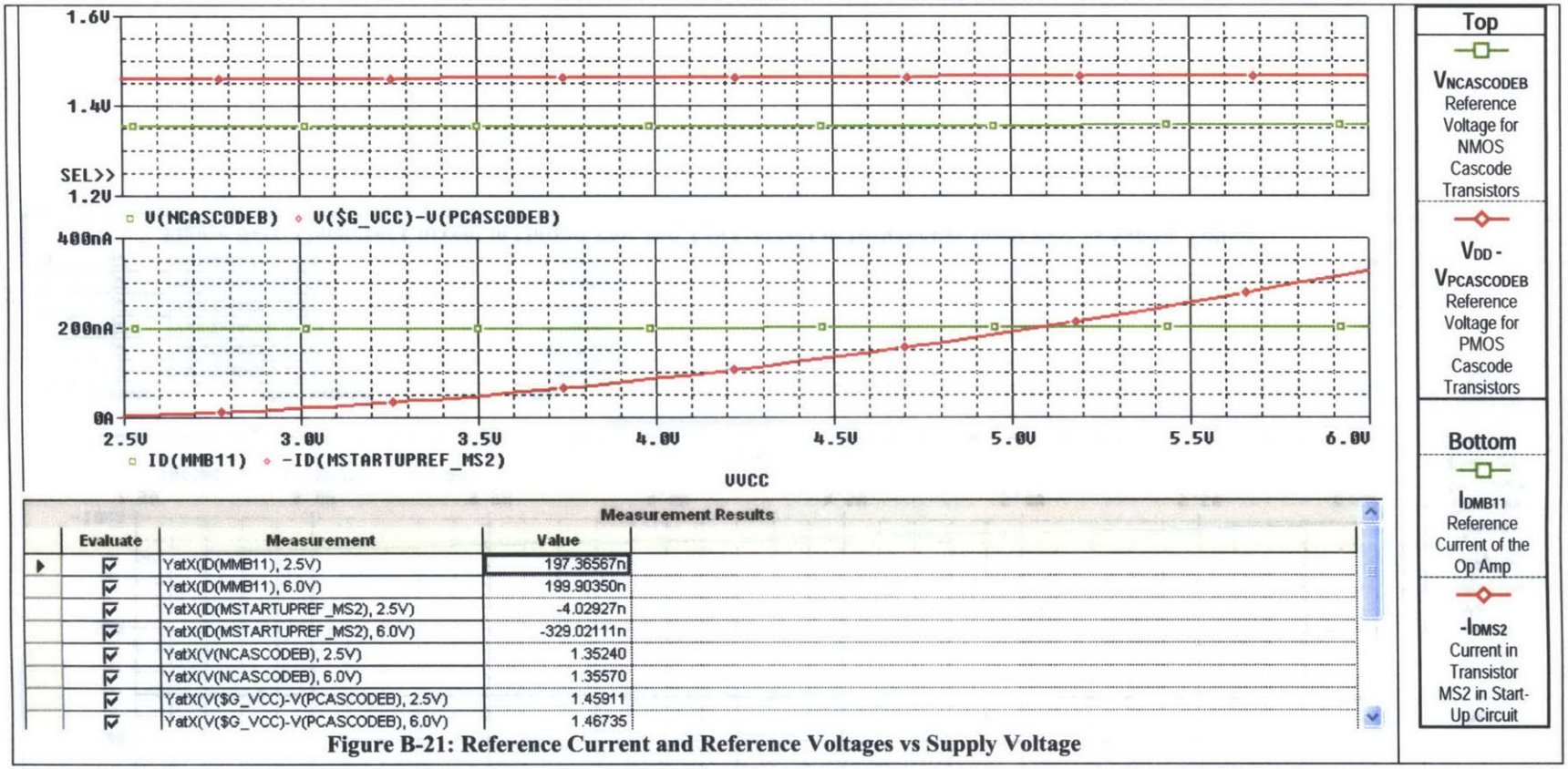


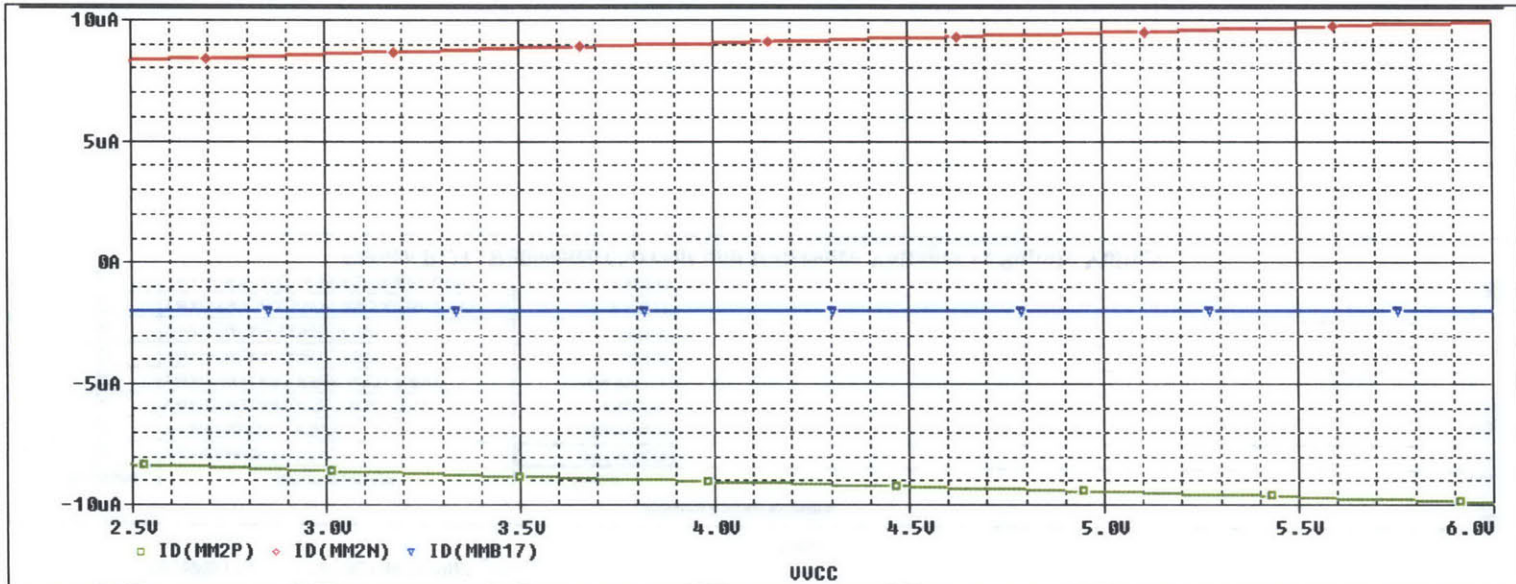
Figure B-20: Schematic of Bias Cell for 20µA Micropower Op Amp with Hybrid Explicit Cascode Compensation (HECC)



Measurement Results

Evaluate	Measurement	Value
☑	YatX(ID(MMB11), 2.5V)	197.36567n
☑	YatX(ID(MMB11), 6.0V)	199.90350n
☑	YatX(ID(MSTARTUPREF_MS2), 2.5V)	-4.02927n
☑	YatX(ID(MSTARTUPREF_MS2), 6.0V)	-329.02111n
☑	YatX(V(NCASCODEB), 2.5V)	1.35240
☑	YatX(V(NCASCODEB), 6.0V)	1.35570
☑	YatX(V($G_VCC)-V(PCASCODEB), 2.5V)	1.45911
☑	YatX(V($G_VCC)-V(PCASCODEB), 6.0V)	1.46735

Figure B-21: Reference Current and Reference Voltages vs Supply Voltage



Measurement Results

Evaluate	Measurement	Value
☑	YatX(ID(MM2P), 2.5V)	-8.31879u
☑	YatX(ID(MM2P), 6.0V)	-9.91346u
☑	YatX(ID(MM2N), 2.5V)	8.31852u
☑	YatX(ID(MM2N), 6.0V)	9.91404u
☑	YatX(ID(MMB17), 2.5V)	-1.97365u
☑	YatX(ID(MMB17), 6.0V)	-1.99953u

Figure B-22: Quiescent Current in Output Pair and Tail Current in Differential Input Pair vs Supply Voltage

Appendix C Schematics and Characteristics of 20μA Micropower Op Amp with Hybrid Symmetric Embedded Cascode Compensation (HSECC)

LIST OF FIGURES IN APPENDIX C

Table C: Characteristics of 20μA Micropower Op Amp with Hybrid Symmetric Embedded Compensation (HSECC) from Simulation

Simulation results are at 25°C. V_{DD} = 2.5V and V_{SS} = 0V.						
Primary Characteristics						
Symbol	**Parameter**		**Condition**	**Value**		**Unit**
				Specified	**Simulated**	
GBW[22]	**Gain Bandwidth Product**		C_L = 100pF R_L = 100kΩ	**> 0.3**	**0.617** (Φ_M = 60.6°)	**MHz**
A_{VOL}	**Large-Signal Voltage Gain (DC Open-Loop Gain)**		C_L = 100pF R_L = 100kΩ	**> 100**	**123**	**dB**
I_S	**Supply Current**		No Load	**< 21**	**19.43**	**μA**
V_{INCM}[23]	Input Common-Mode Range		-	> V_{DD} - 1.25V and must include negative supply voltage	**1.3** and includes negative supply voltage	V
V_{OS}[24]	(Untrimmed) Input Offset Voltage		V_{INCM} = 0.65V	< 5	**4.17**	mV
V_{OUT}	V_{OUTH}	High Output Voltage	I_{SOURCE} = 1.0mA	> V_{DD} - 0.3V	**2.34**	V
	V_{OUTL}	Low Output Voltage	I_{SINK} = 1.0mA	< V_{SS} + 0.3V	**0.19**	V
I_{SOURCE}[25]	Output Source Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.55**	mA
I_{SINK}	Output Sink Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.04**	mA
Secondary Characteristics						
Symbol	**Parameter**		**Condition**	**Value**		**Unit**
				Specified	**Simulated**	
SR+	Positive Going Slew Rate		A_V = 1V/V, 1V Step	> 0.15	**0.254**	V/μs
SR-	Negative Going Slew Rate		A_V = 1V/V, 1V Step	< -0.15	**-0.269**	V/μs

[22] Gain bandwidth product per supply current GBW/ I_S = 31.8MHz/mA @ C_L = 100pF.
[23] Verified by CMRR simulation in Figure C-4.
[24] Conservative estimate from calculation.
[25] Maximum output source current is measured when the other transistor in the output pair starts to turn off, i.e. its current goes down to as low as 1μA.

CMRR	Common Mode Rejection Ratio	@ DC	> 60	**147**	dB
PSRR+	Positive Power Supply Rejection Ratio	@ DC	> 60	**88.4**	dB
PSRR-	Negative Power Supply Rejection Ratio	@ DC	> 60	**103**	dB
t_s	0.1% Settling Time	A_V = 1V/V, 1V Step	< 10	**$12 < t_s < 20$**	µs

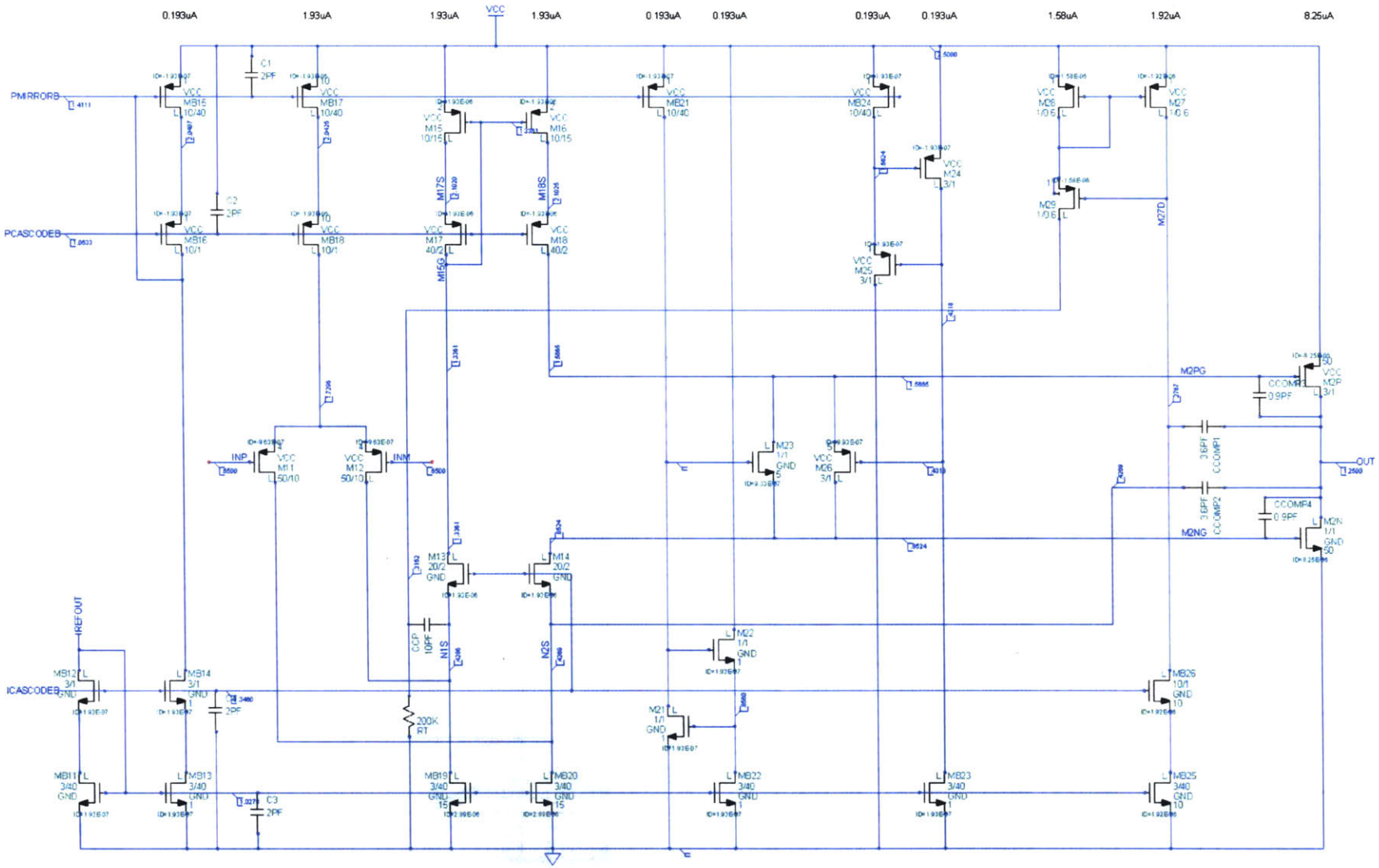
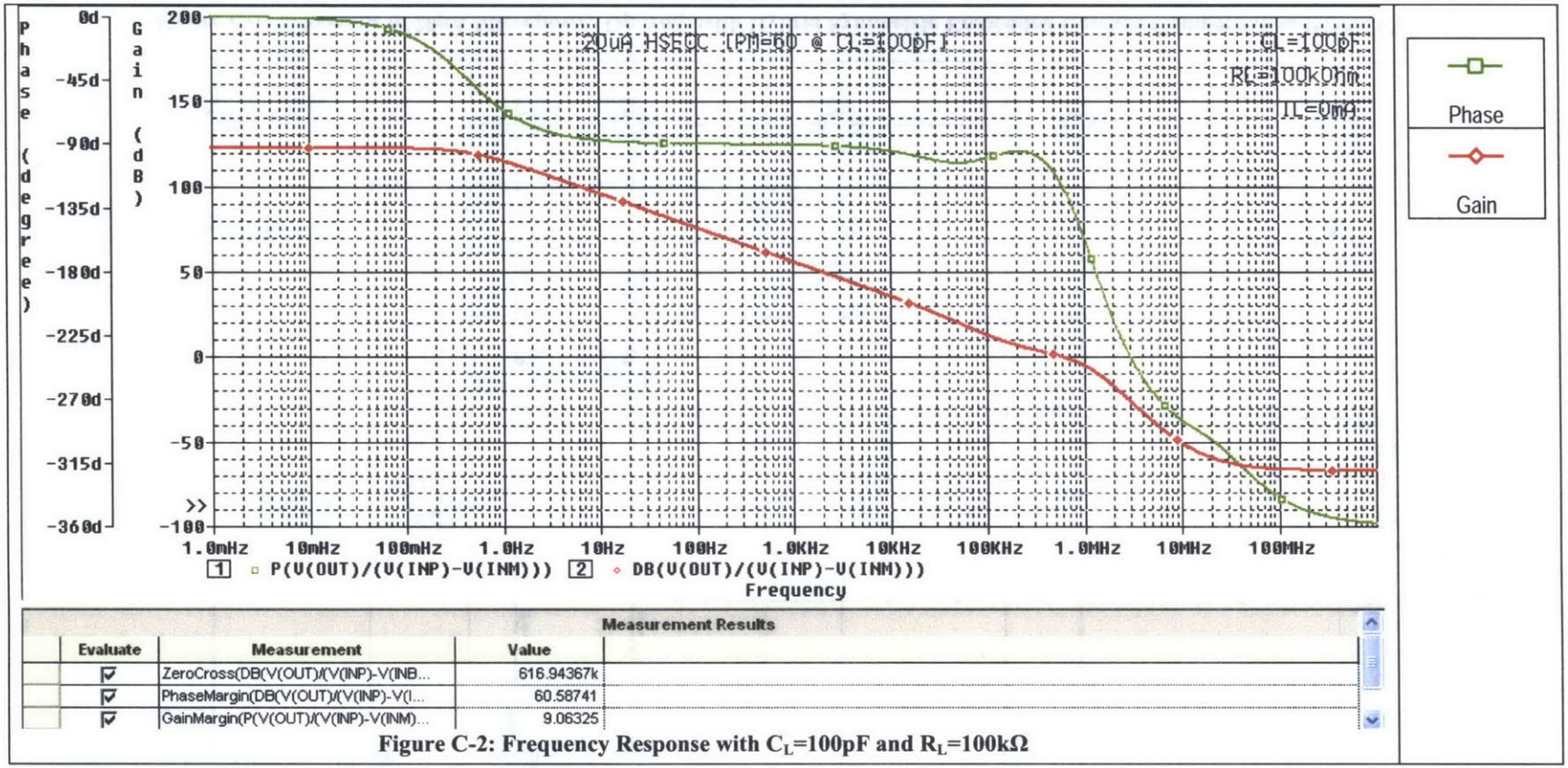


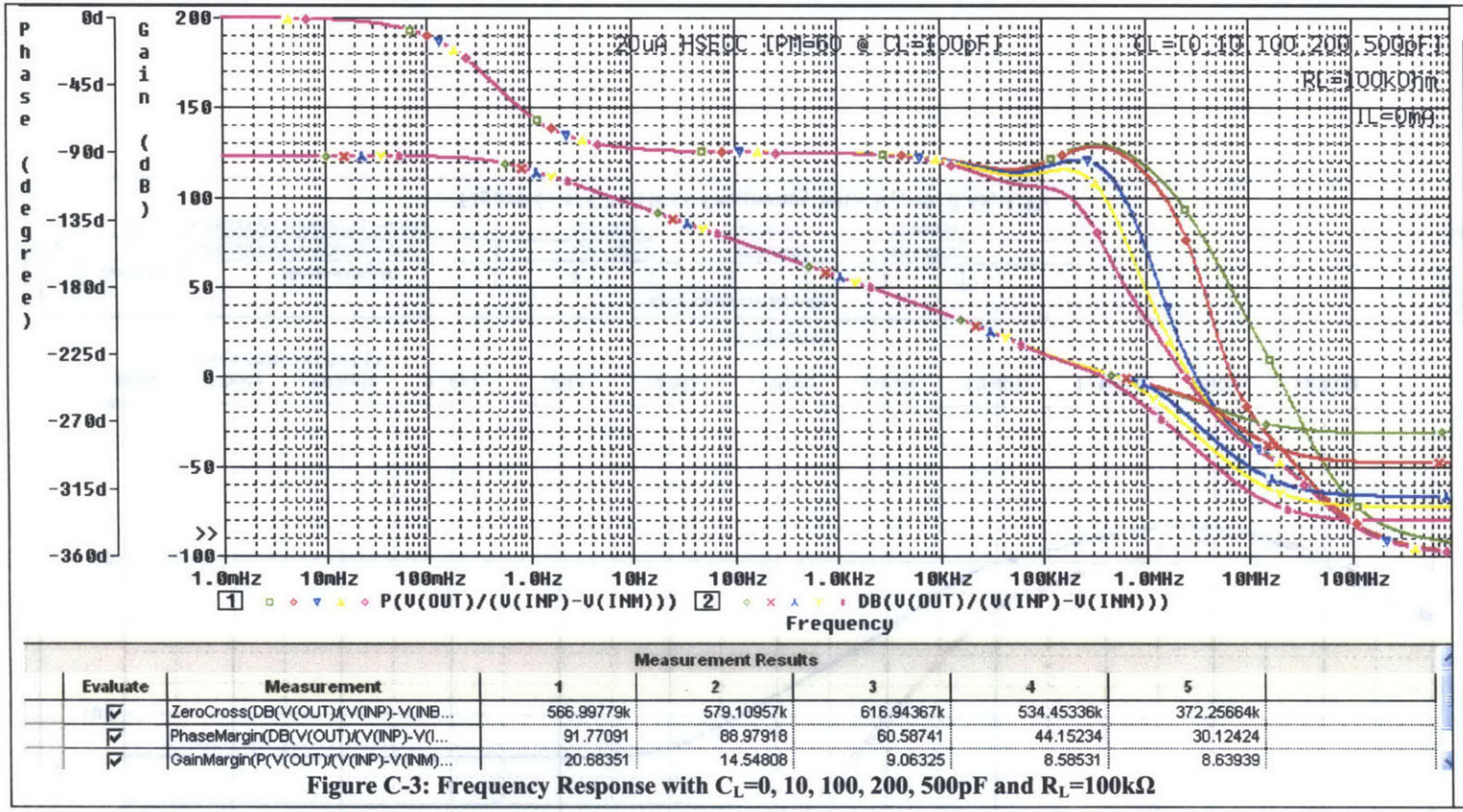
Figure C-1: Schematic of 20µA Micropower Op Amp with Hybrid Symmetric Embedded Cascode Compensation (HSECC)



Measurement Results

Evaluate	Measurement	Value
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INB...	616.94367k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	60.58741
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	9.06325

Figure C-2: Frequency Response with C_L=100pF and R_L=100kΩ



C_L (pF)	Symbol
0	Phase, Gain
10	Phase, Gain
100	Phase, Gain
200	Phase, Gain
500	Phase, Gain

Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INB...	566.99779k	579.10957k	616.94367k	534.45336k	372.25664k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	91.77091	88.97918	60.58741	44.15234	30.12424
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	20.68351	14.54808	9.06325	8.58531	8.63939

Figure C-3: Frequency Response with C_L=0, 10, 100, 200, 500pF and R_L=100kΩ

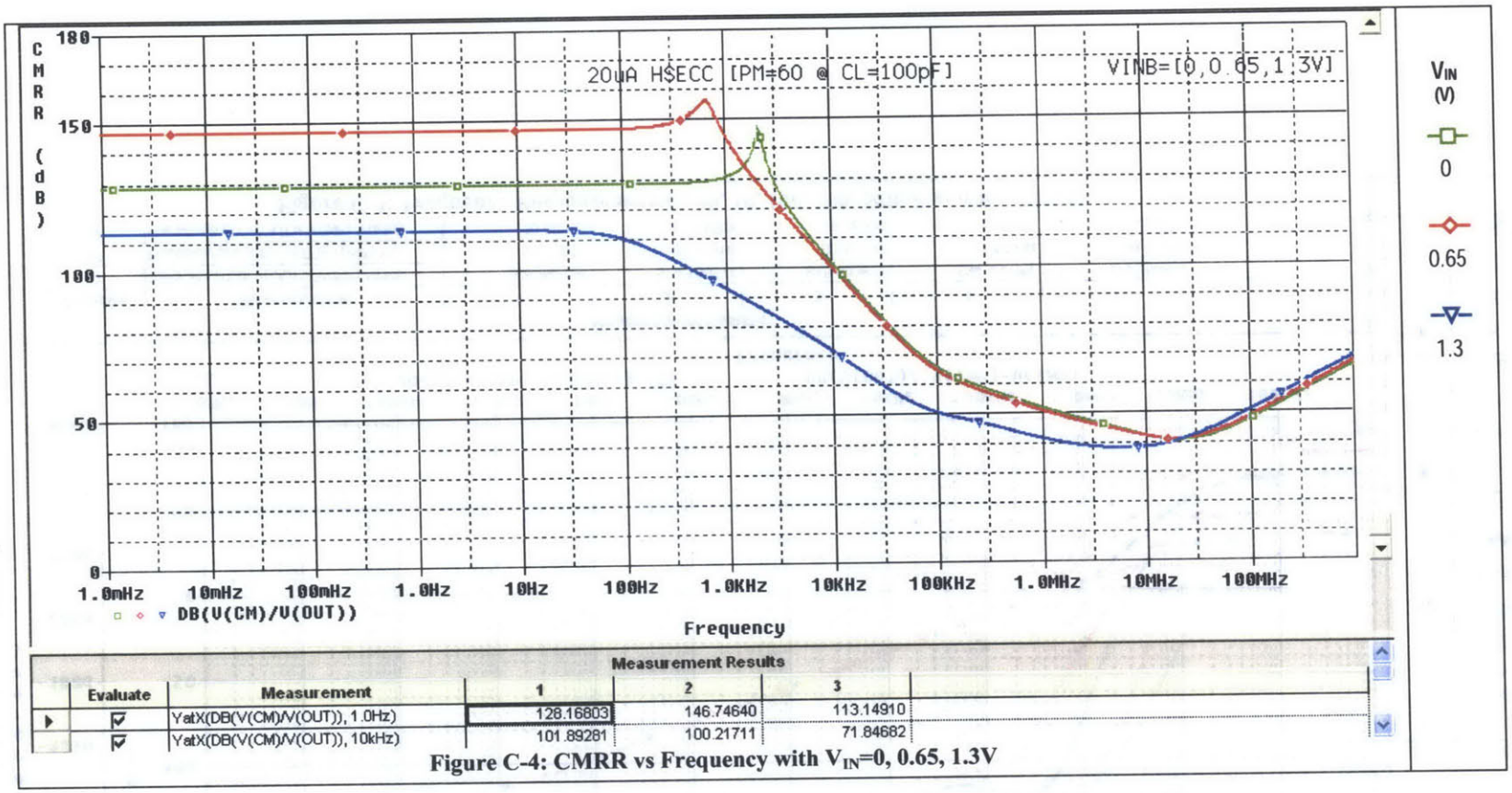
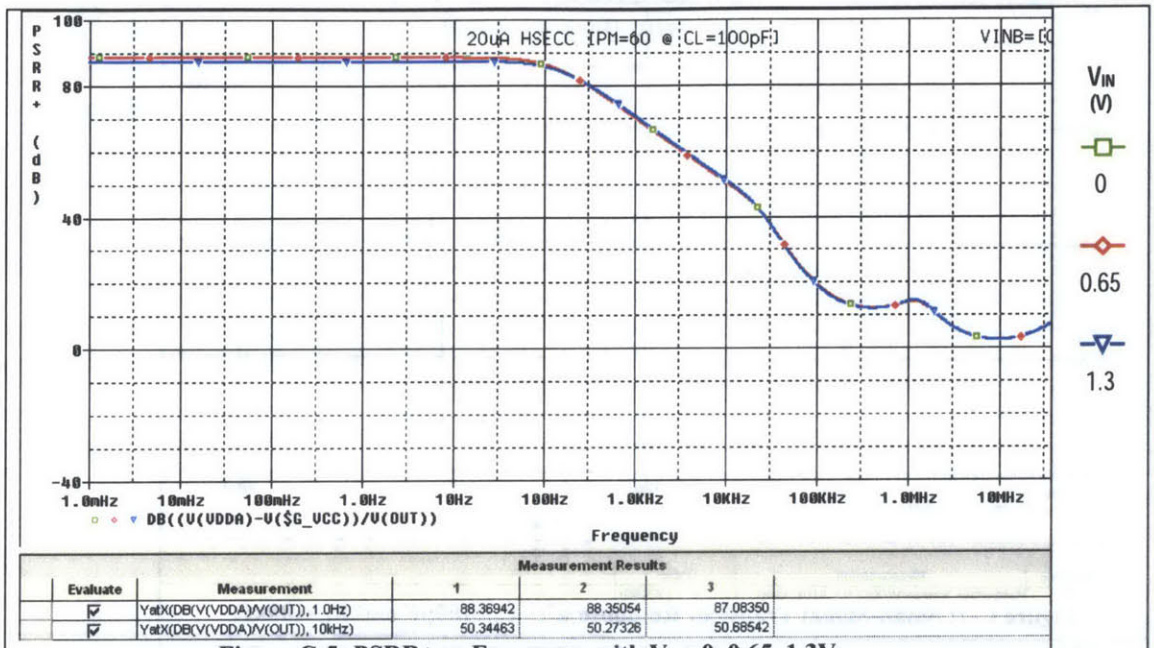


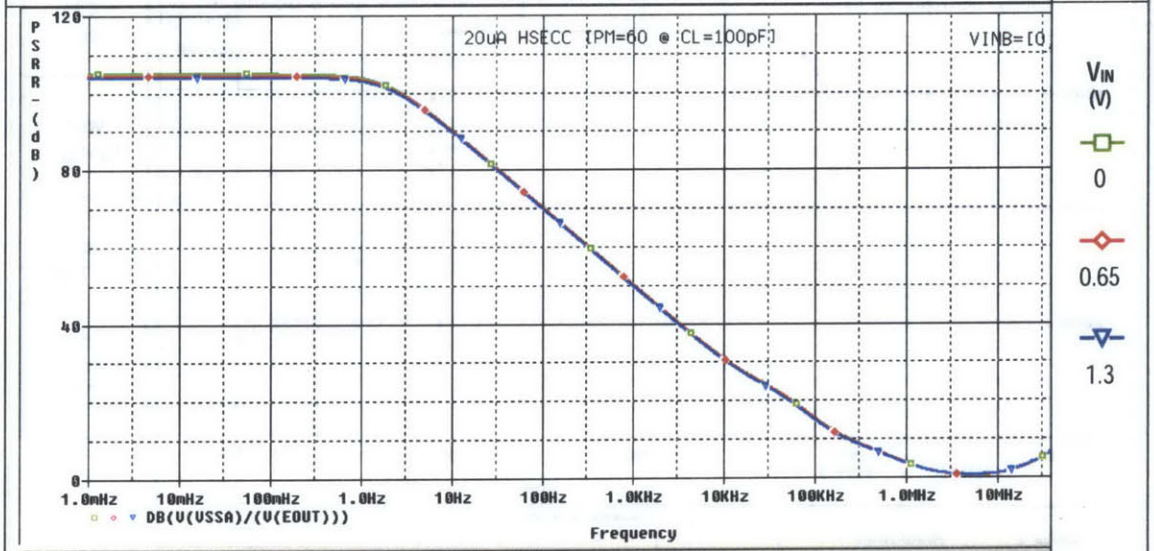
Figure C-4: CMRR vs Frequency with V_{IN}=0, 0.65, 1.3V



Measurement Results

Evaluate	Measurement	1	2	3
☑	YatX(DB(V(VDDA)/V(OUT)), 1.0Hz)	88.36942	88.35054	87.08350
☑	YatX(DB(V(VDDA)/V(OUT)), 10kHz)	50.34463	50.27326	50.68542

Figure C-5: PSRR+ vs Frequency with V_{IN}=0, 0.65, 1.3V



Measurement Results

Evaluate	Measurement	1	2	3
☑	YatX(DB(V(VSSA)/V(EOUT)), 1Hz)	103.66850	103.20685	102.74368
☑	YatX((V(VSSA)/V(EOUT)), 10kHz)	34.80874	34.52018	33.21969

Figure C-6: PSRR- vs Frequency with V_{IN}=0, 0.65, 1.3V

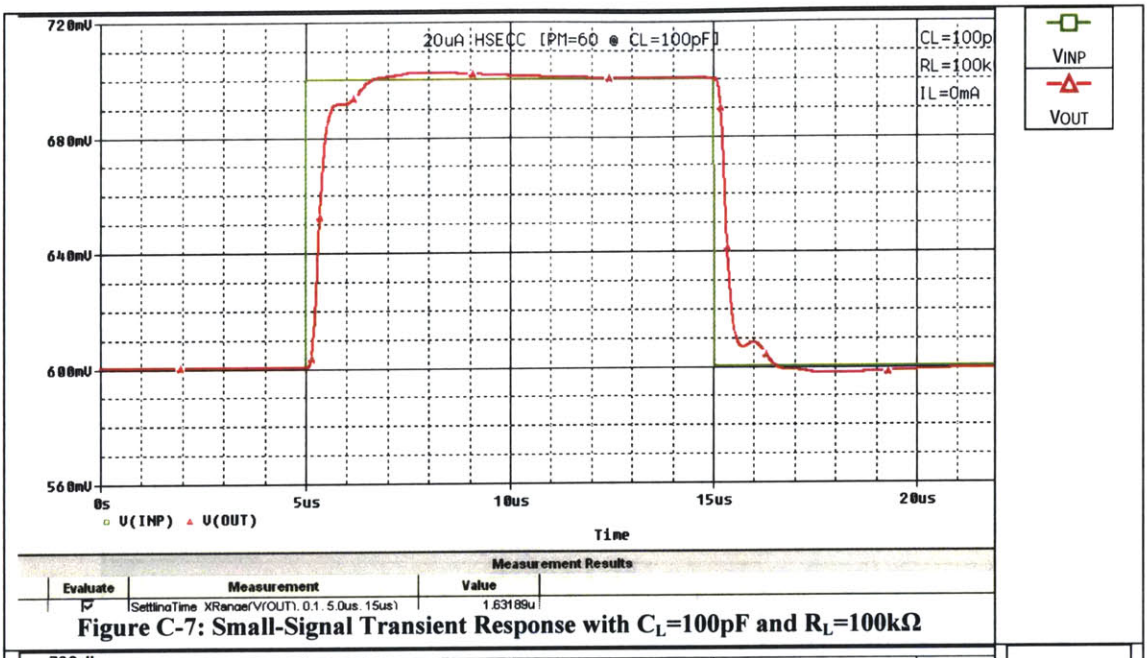


Figure C-7: Small-Signal Transient Response with C_L=100pF and R_L=100kΩ

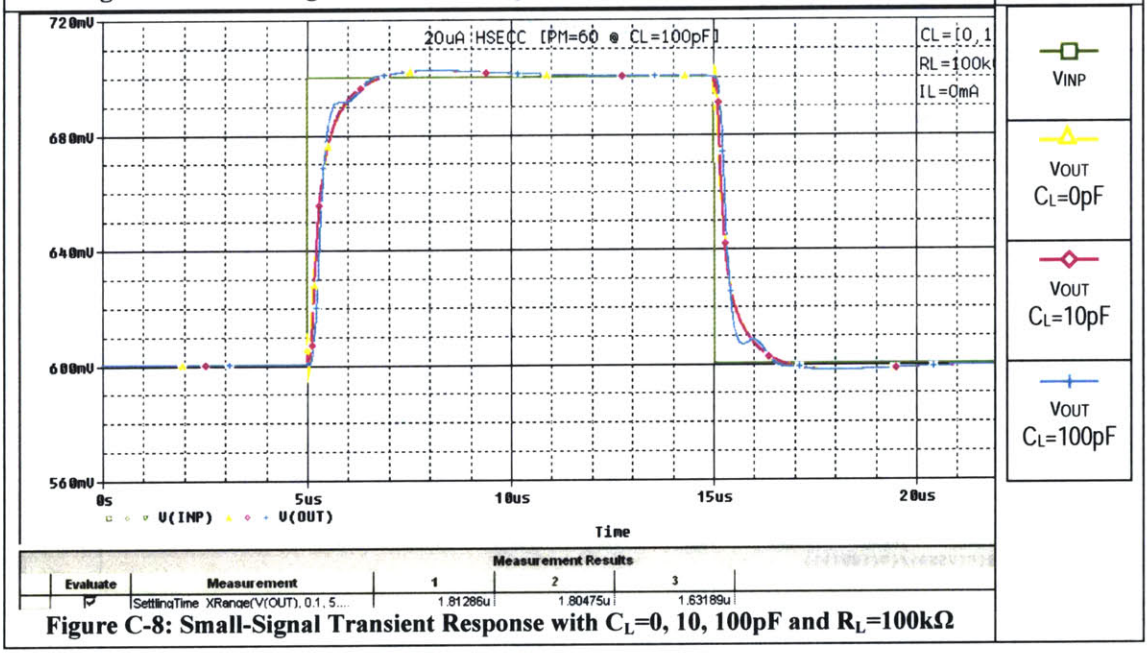
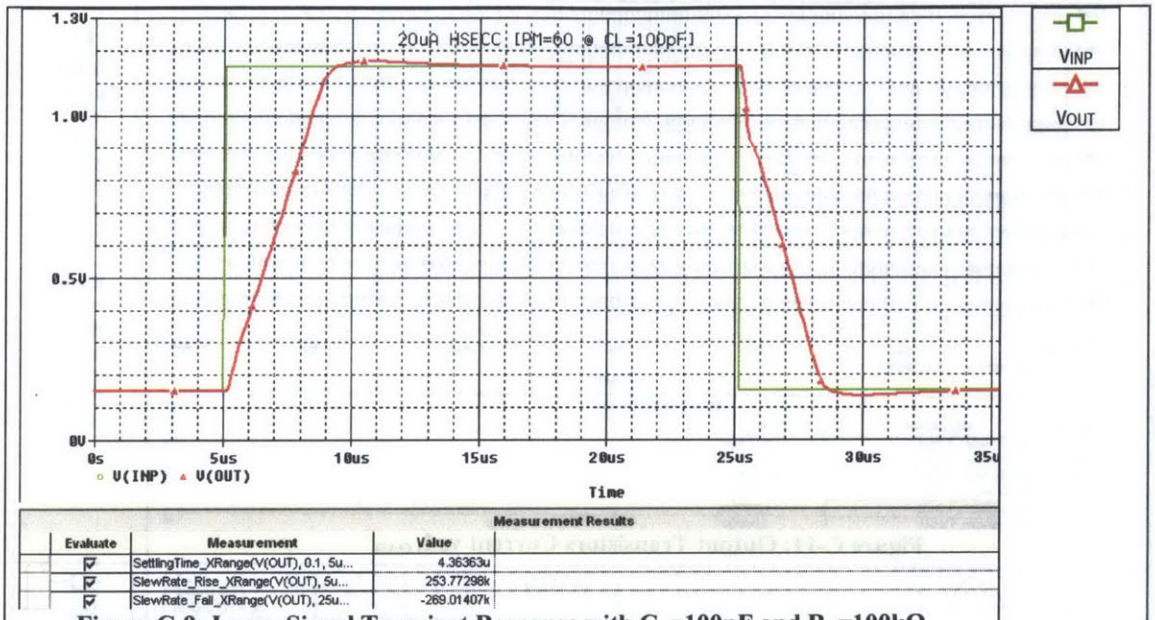


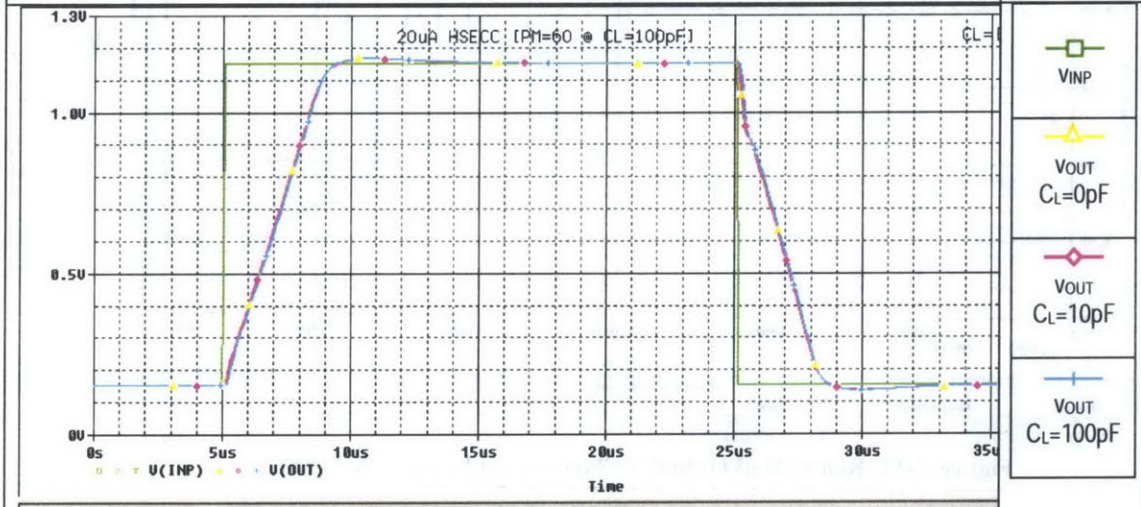
Figure C-8: Small-Signal Transient Response with C_L=0, 10, 100pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	Value
☑	SettlingTime_XRange(V(OUT), 0.1, 5u...	4.36363u
☑	SlewRate_Rise_XRange(V(OUT), 5u...	253.77298k
☑	SlewRate_Fall_XRange(V(OUT), 25u...	-269.01407k

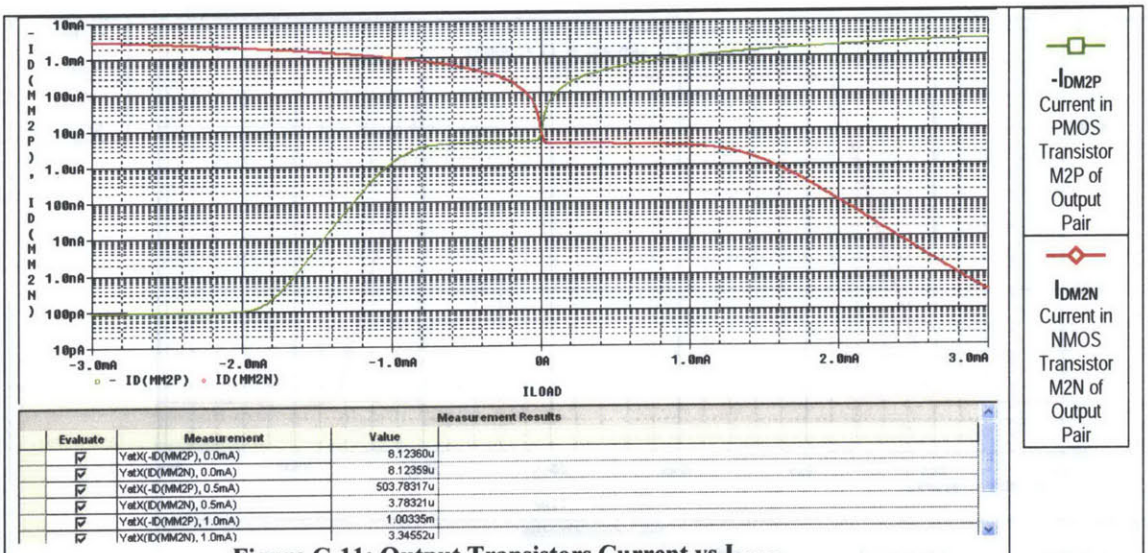
Figure C-9: Large-Signal Transient Response with C_L=100pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	1	2	3
☑	SettlingTime_XRange(V(OUT), 0.1, 5u...	4.41545u	4.41423u	4.36386u
☑	SlewRate_Rise_XRange(V(OUT), 5u...	252.19235k	252.32318k	253.77462k
☑	SlewRate_Fall_XRange(V(OUT), 25u...	-271.36560k	-270.56605k	-268.84326k

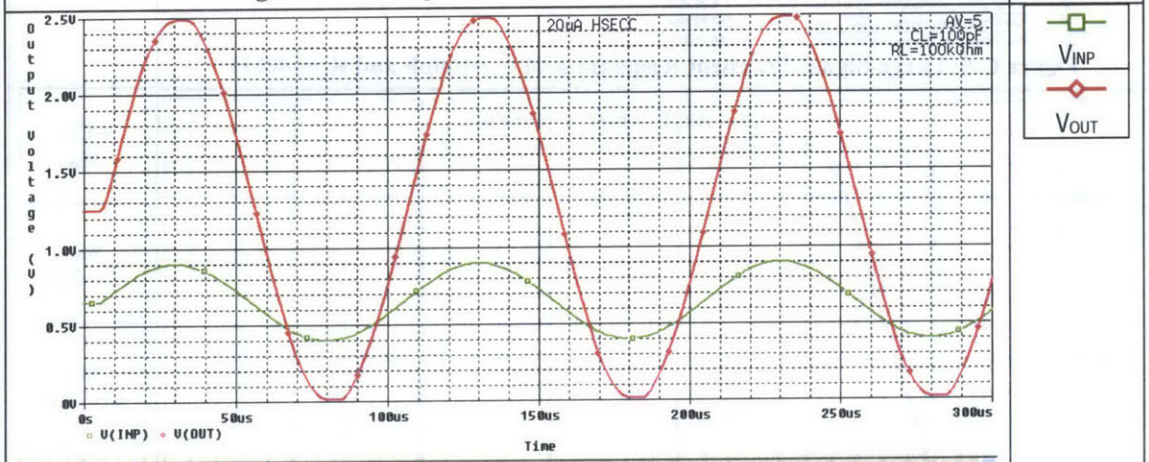
Figure C-10: Large-Signal Transient Response with C_L=0, 10, 100pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	Value
☑	YatX(-ID(MM2P), 0.0mA)	8.12360u
☑	YatX(ID(MM2N), 0.0mA)	8.12359u
☑	YatX(-ID(MM2P), 0.5mA)	503.78317u
☑	YatX(ID(MM2N), 0.5mA)	3.78321u
☑	YatX(-ID(MM2P), 1.0mA)	1.00335m
☑	YatX(ID(MM2N), 1.0mA)	3.34552u

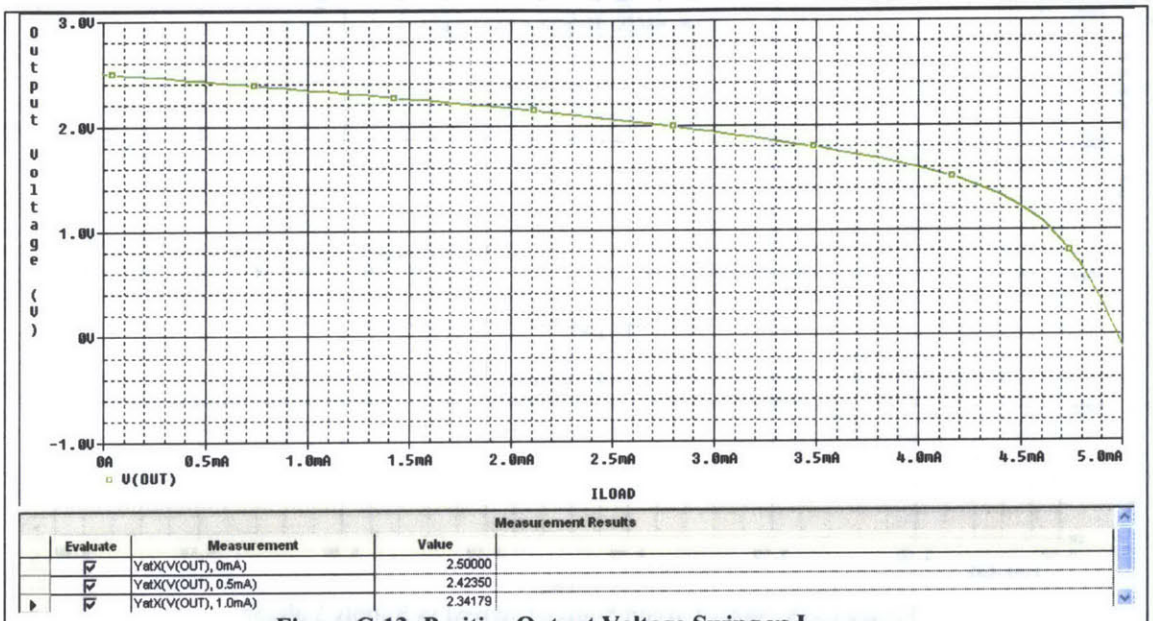
Figure C-11: Output Transistors Current vs I_{LOAD}



Measurement Results

Evaluate	Measurement	Value
☑	Max(V(OUT))	2.48933
☑	Min(V(OUT))	10.43630m

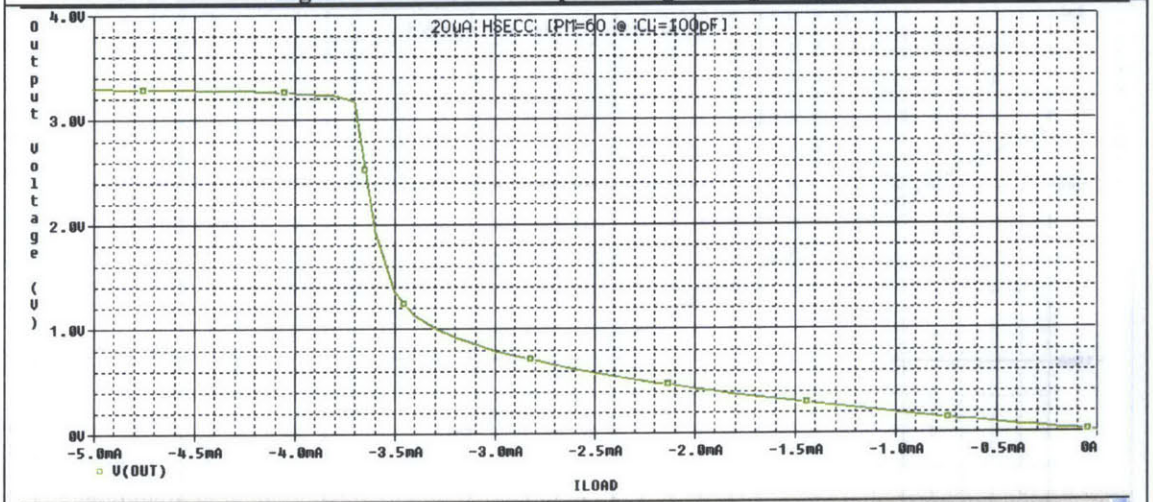
Figure C-12: Rail-to-Rail Output Voltage (v_{IN} and v_{OUT} with A_V=5)



Measurement Results

Evaluate	Measurement	Value
☑	YatX(V(OUT), 0mA)	2.50000
☑	YatX(V(OUT), 0.5mA)	2.42350
☑	YatX(V(OUT), 1.0mA)	2.34179

Figure C-13: Positive Output Voltage Swing vs I_{SOURCE}



Measurement Results

Evaluate	Measurement	Value
☑	YatX(V(OUT) , 0mA)	21.25867n
☑	YatX(V(OUT), -0.5mA)	88.78508m
☑	YatX(V(OUT), -1.0mA)	186.45455m

Figure C-14: Negative Output Voltage Swing vs I_{SINK}

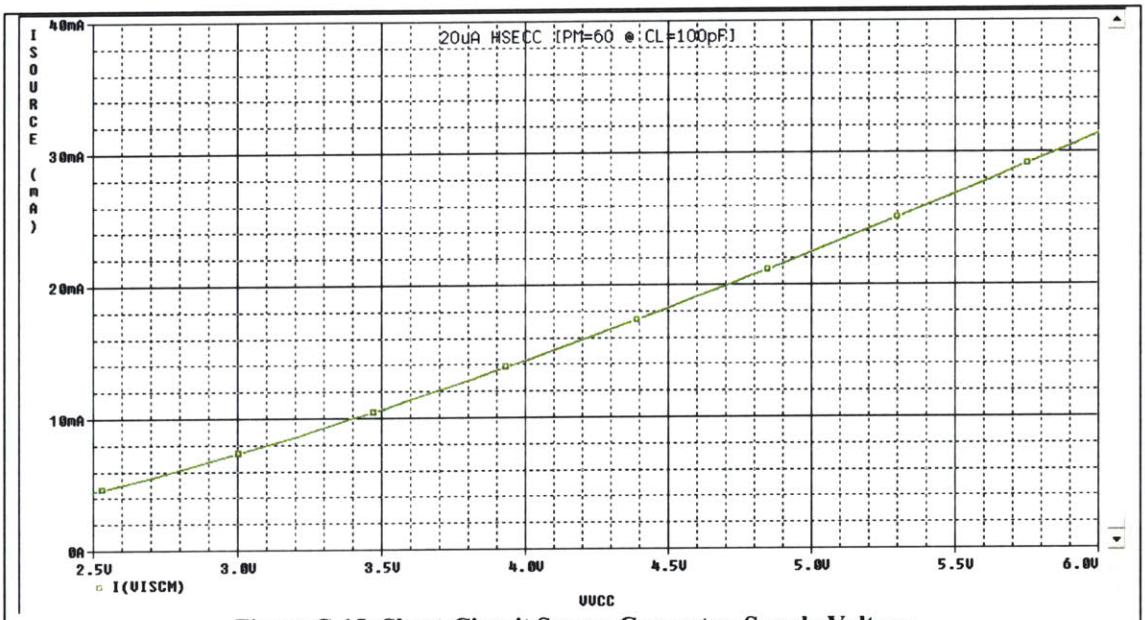


Figure C-15: Short-Circuit Source Current vs Supply Voltage

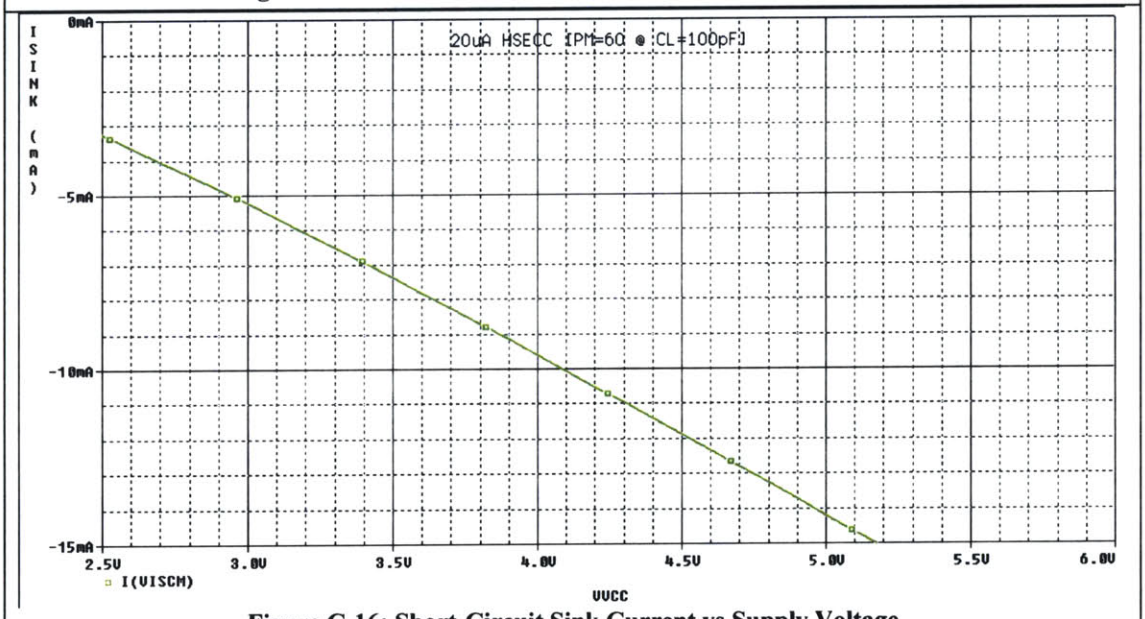
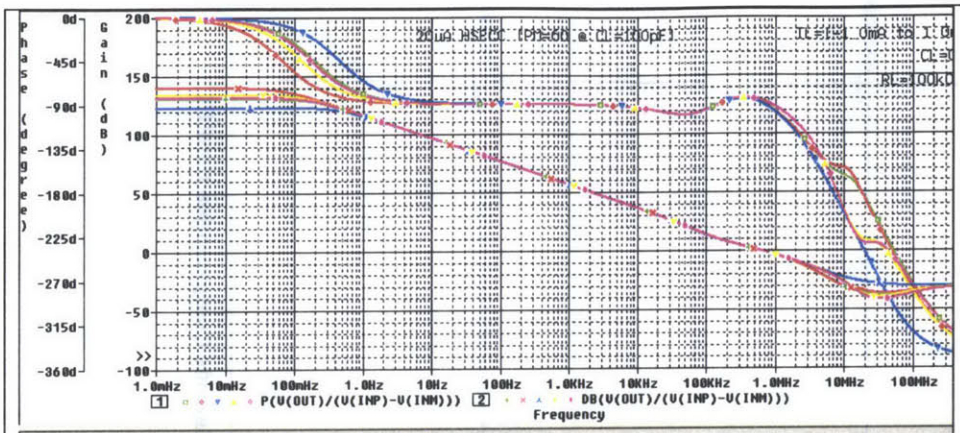


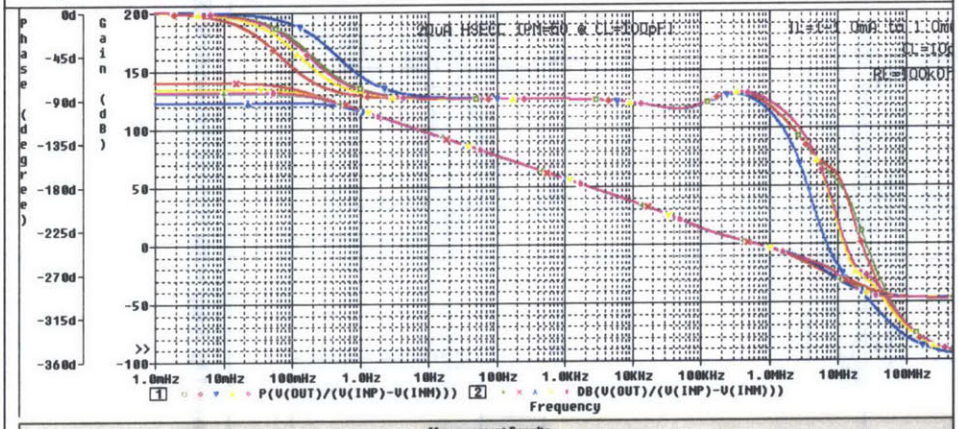
Figure C-16: Short-Circuit Sink Current vs Supply Voltage



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	571.37602k	574.66444k	566.99779k	565.08727k	562.96307k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	92.57320	92.36617	91.77091	94.64436	94.64645
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	36.18881	34.44103	20.68351	23.56914	23.74197
☑	Peak(DB(V(OUT)/(V(INP)-V(INM)))), 1)	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

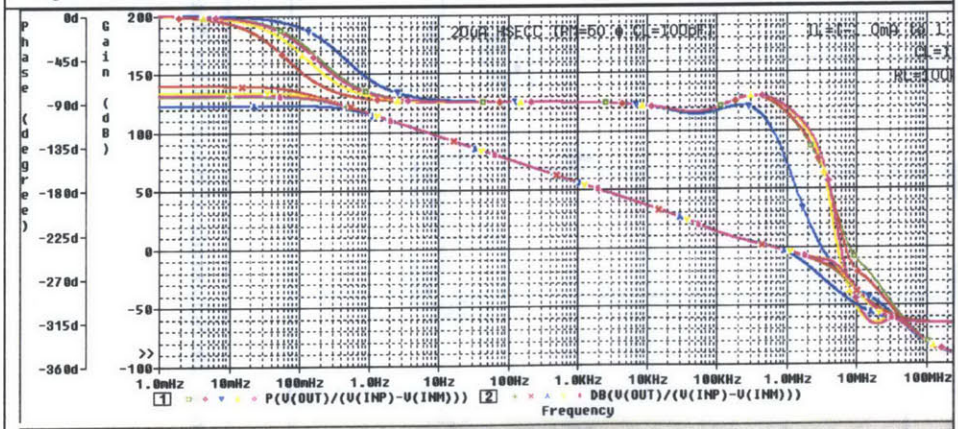
Figure C-17: Frequency Response with C_L=0pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	572.68644k	575.90129k	579.10957k	566.39577k	563.99347k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	92.29344	92.12199	88.97918	94.41416	94.46241
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	31.81152	30.74409	14.54808	20.83354	21.39307
☑	Peak(DB(V(OUT)/(V(INP)-V(INM)))), 1)	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

Figure C-18: Frequency Response with C_L=10pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	584.47849k	587.12479k	616.94367k	578.33466k	573.32750k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	89.66368	89.83185	60.58741	92.24928	92.74914
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	17.61417	17.12073	9.06325	11.74109	13.00868
☑	Peak(DB(V(OUT)/(V(INP)-V(INM)))), 1)	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

Figure C-19: Frequency Response with C_L=100pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA

I_L (mA)	Symbol
-1.0	Phase Gain
-0.5	Phase Gain
0.0	Phase Gain
0.5	Phase Gain
1.0	Phase Gain

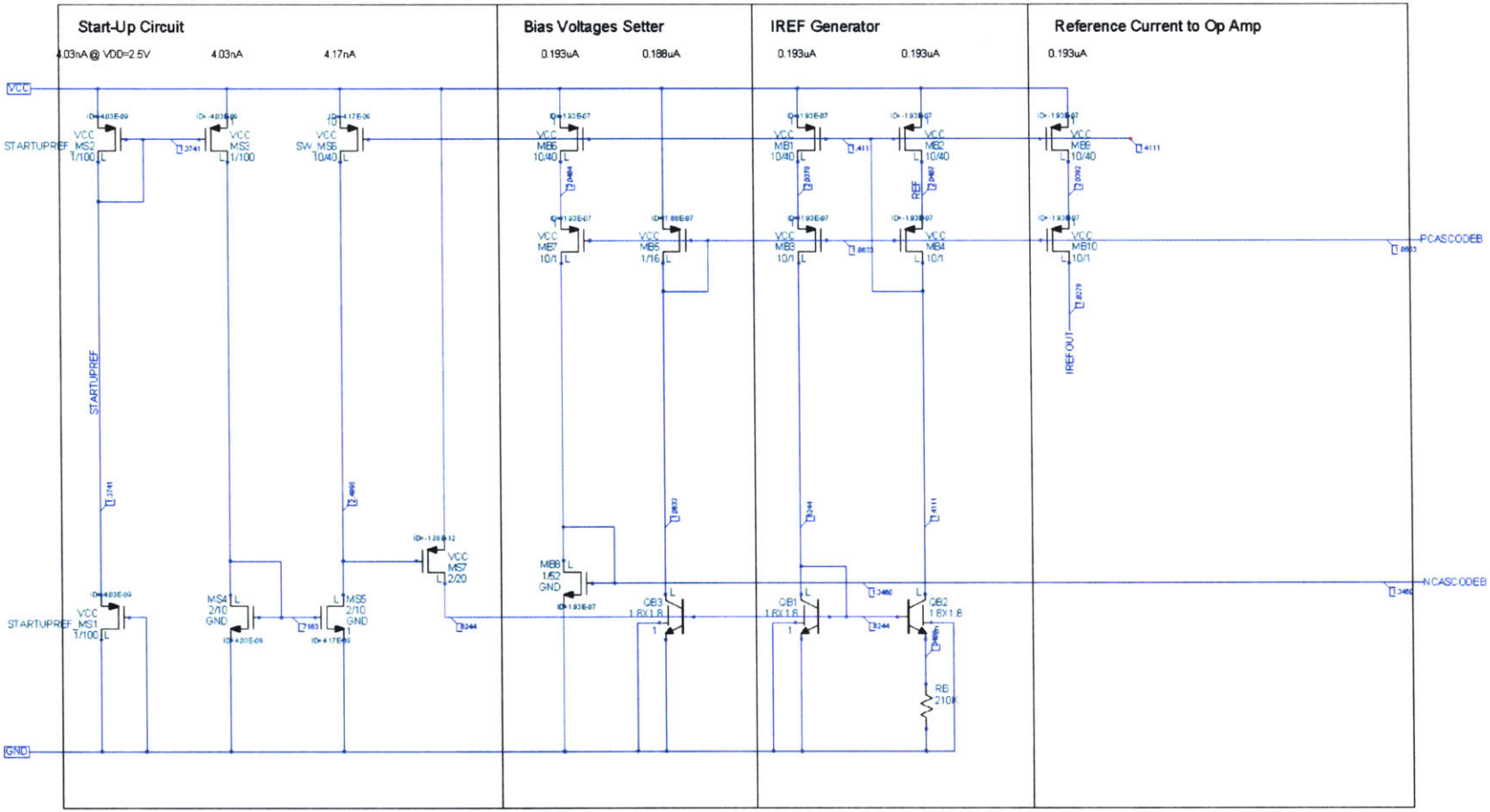
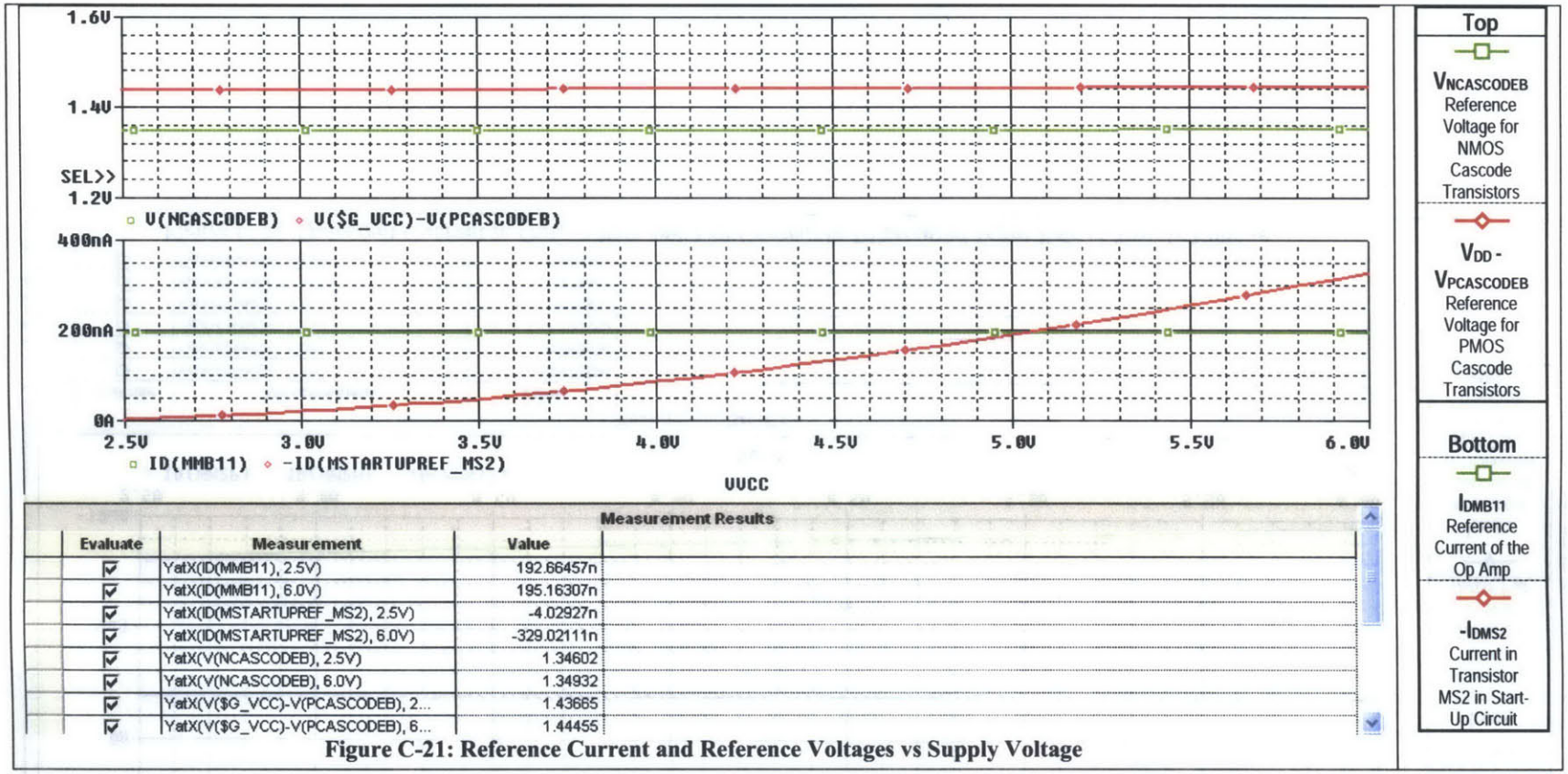


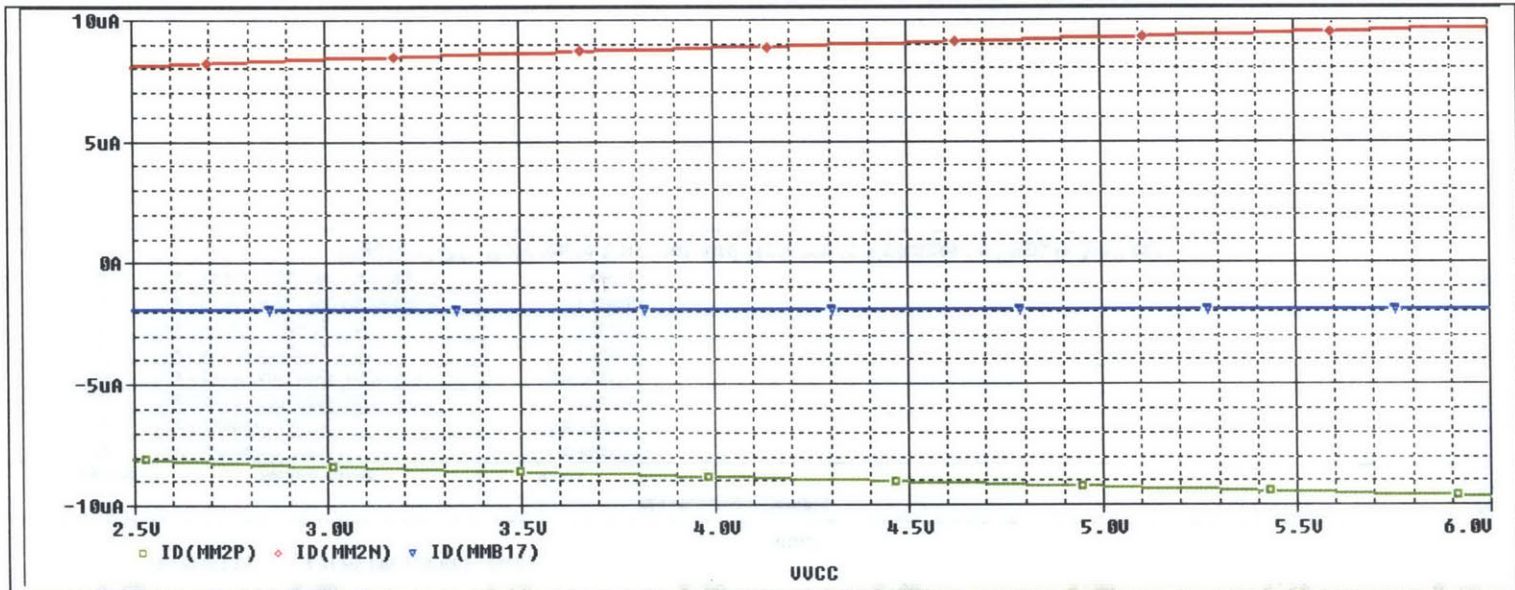
Figure C-20: Schematic of Bias Cell for 20µA Micropower Op Amp with Hybrid Symmetric Embedded Cascode Compensation (HSECC)



Measurement Results

Evaluate	Measurement	Value
☑	YatX(ID(MMB11), 2.5V)	192.66457n
☑	YatX(ID(MMB11), 6.0V)	195.16307n
☑	YatX(ID(MSTARTUPREF_MS2), 2.5V)	-4.02927n
☑	YatX(ID(MSTARTUPREF_MS2), 6.0V)	-329.02111n
☑	YatX(V(NCASCODEB), 2.5V)	1.34602
☑	YatX(V(NCASCODEB), 6.0V)	1.34932
☑	YatX(V($G_VCC)-V(PCASCODEB), 2...	1.43665
☑	YatX(V($G_VCC)-V(PCASCODEB), 6...	1.44455

Figure C-21: Reference Current and Reference Voltages vs Supply Voltage



Measurement Results

Evaluate	Measurement	Value
☑	YatX(ID(MM2P), 2.5V)	-8.12359u
☑	YatX(ID(MM2P), 6.0V)	-9.68356u
☑	YatX(ID(MM2N), 2.5V)	8.12359u
☑	YatX(ID(MM2N), 6.0V)	9.68392u
☑	YatX(ID(MMB17), 2.5V)	-1.92664u
☑	YatX(ID(MMB17), 6.0V)	-1.95214u

Figure C-22: Quiescent Current in Output Pair and Tail Current in Differential Input Pair vs Supply Voltage

Appendix D Schematics and Characteristics of 20μA Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)

LIST OF FIGURES IN APPENDIX D

Table D: Characteristics of 20μA Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC) from Simulation

Simulation results are at 25°C. V_{DD} = 2.5V and V_{SS} = 0V.						
Primary Characteristics						
Symbol	**Parameter**		**Condition**	**Value**		**Unit**
				Specified	**Simulated**	
GBW[26]	**Gain Bandwidth Product**		C_L = 100pF R_L = 100kΩ	**> 0.3**	**0.589** (Φ_M = 61.8°)	**MHz**
A_{VOL}	**Large-Signal Voltage Gain (DC Open-Loop Gain)**		C_L = 100pF R_L = 100kΩ	**> 100**	**122**	**dB**
I_S	**Supply Current**		No Load	**< 21**	**19.95**	**μA**
V_{INCM}[27]	Input Common-Mode Range		-	> V_{DD} - 1.25V and must include negative supply voltage	**1.3** and includes negative supply voltage	V
V_{OS}[28]	(Untrimmed) Input Offset Voltage		V_{INCM} = 0.65V	< 5	**4.17**	mV
V_{OUT}	V_{OUTH}	High Output Voltage	I_{SOURCE} = 1.0mA	> V_{DD} - 0.3V	**2.34**	V
	V_{OUTL}	Low Output Voltage	I_{SINK} = 1.0mA	< V_{SS} + 0.3V	**0.19**	V
I_{SOURCE}[29]	Output Source Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.55**	mA
I_{SINK}	Output Sink Current		C_L = 100pF R_L = 100kΩ	> 1.0	**1.03**	mA
Secondary Characteristics						
Symbol	**Parameter**		**Condition**	**Value**		**Unit**
				Specified	**Simulated**	
SR+	Positive Going Slew Rate		A_V = 1V/V, 1V Step	> 0.15	**0.315**	V/μs
SR-	Negative Going Slew Rate		A_V = 1V/V, 1V	< -0.15	**-0.342**	V/μs

[26] Gain bandwidth product per supply current GBW/ I_S = 29.5MHz/mA @ C_L = 100pF.
[27] Verified by CMRR simulation in Figure D-4.
[28] Conservative estimate from calculation.
[29] Maximum output source current is measured when the other transistor in the output pair starts to turn off, i.e. its current goes down to as low as 1μA.

		Step			
CMRR	Common Mode Rejection Ratio	@ DC	> 60	**144**	dB
PSRR+	Positive Power Supply Rejection Ratio	@ DC	> 60	**84.6**	dB
PSRR-	Negative Power Supply Rejection Ratio	@ DC	> 60	**99.5**	dB
t_s	0.1% Settling Time	A_V = 1V/V, 1V Step	< 10	**3.70**	µs

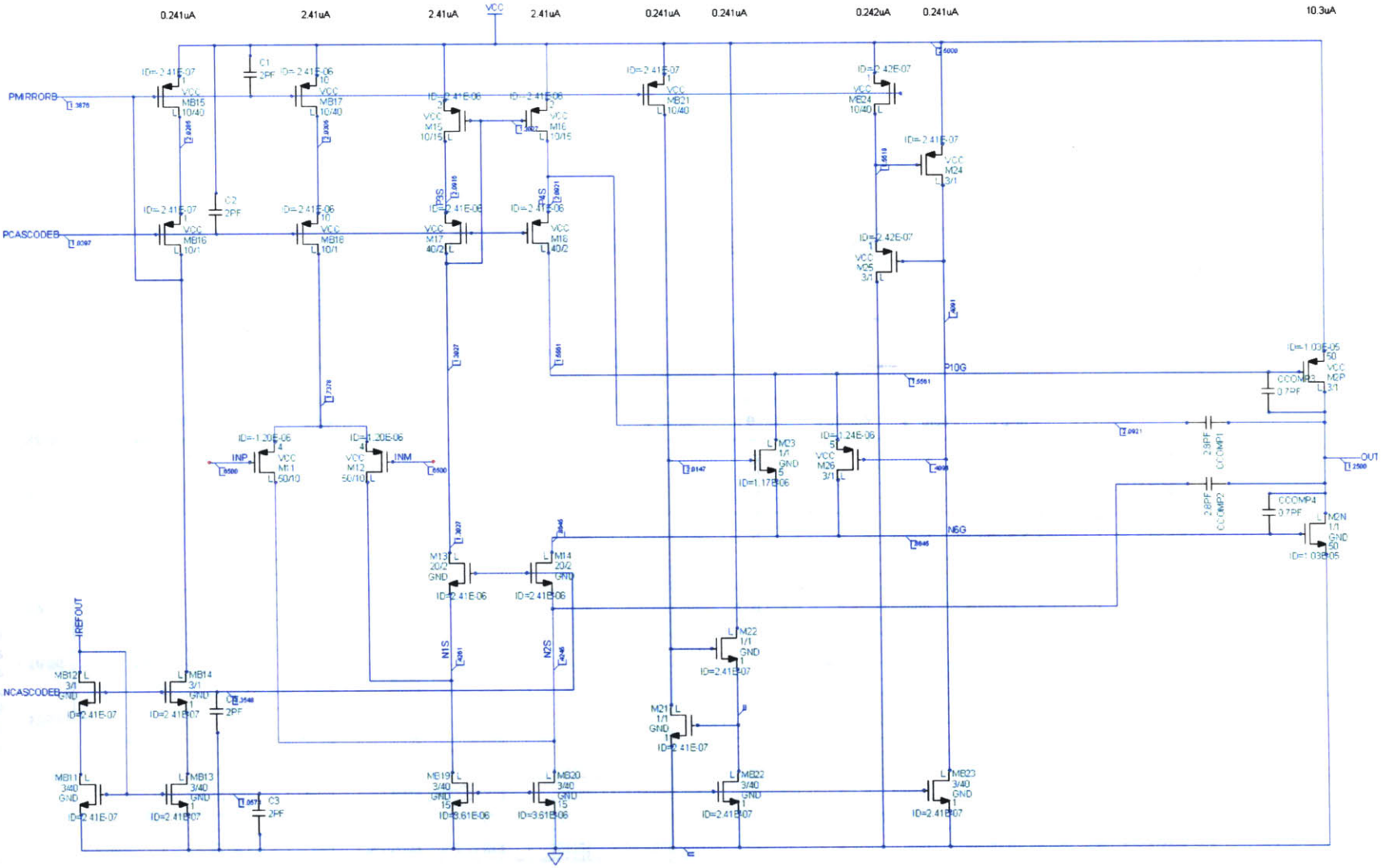
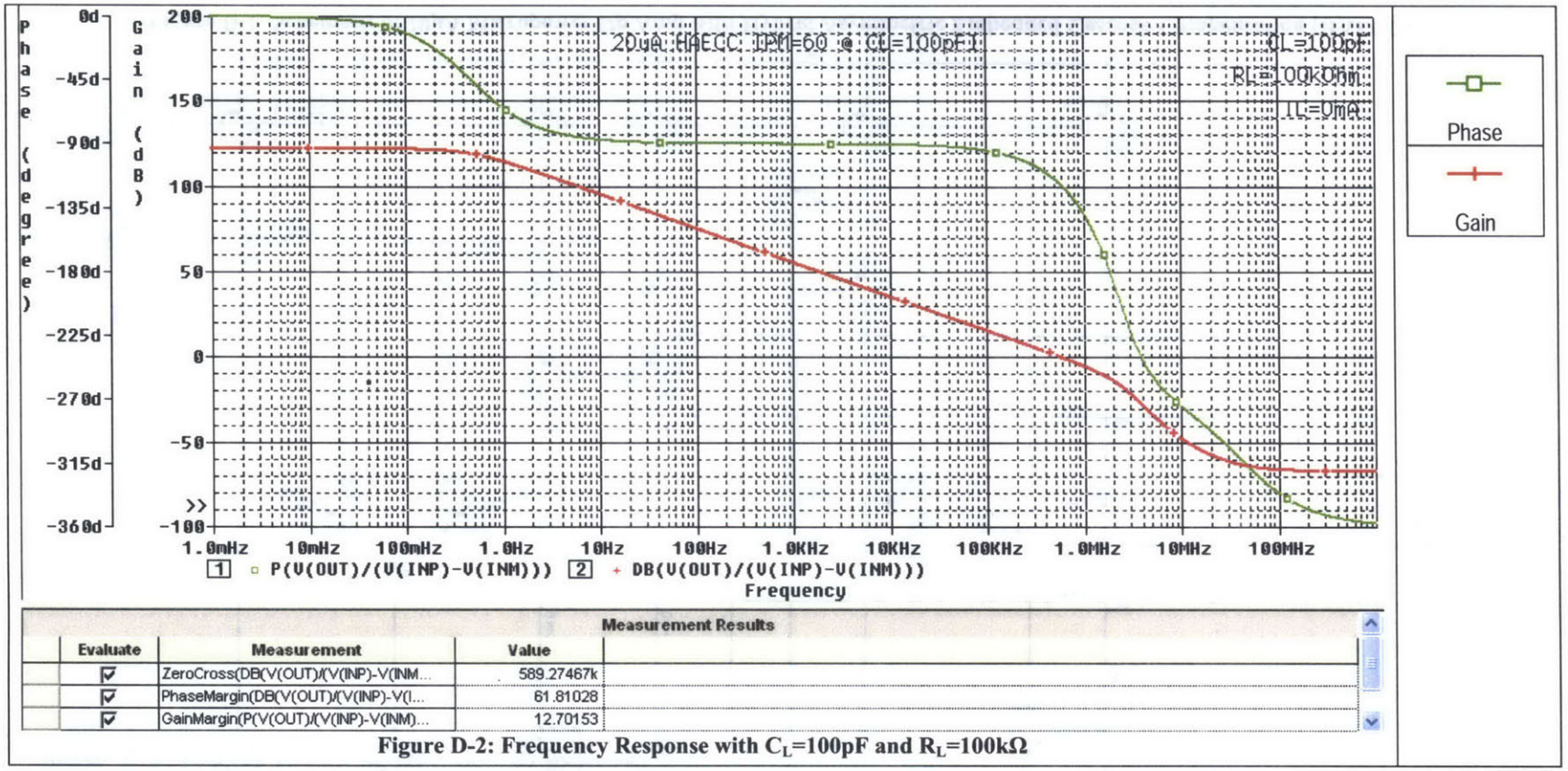


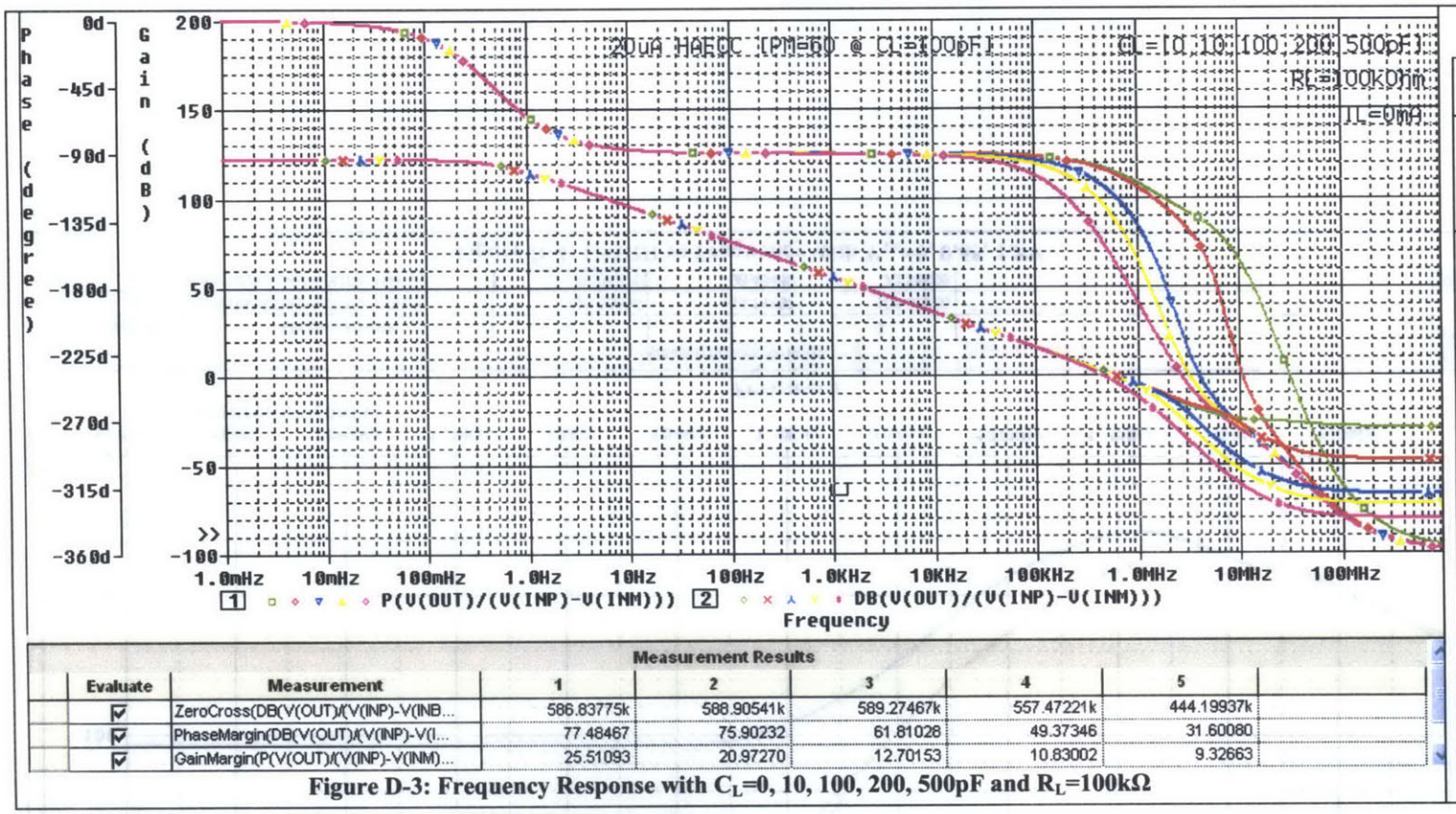
Figure D-1: Schematic of 20µA Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)



Measurement Results

Evaluate	Measurement	Value
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	589.27467k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	61.81028
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	12.70153

Figure D-2: Frequency Response with C_L=100pF and R_L=100kΩ

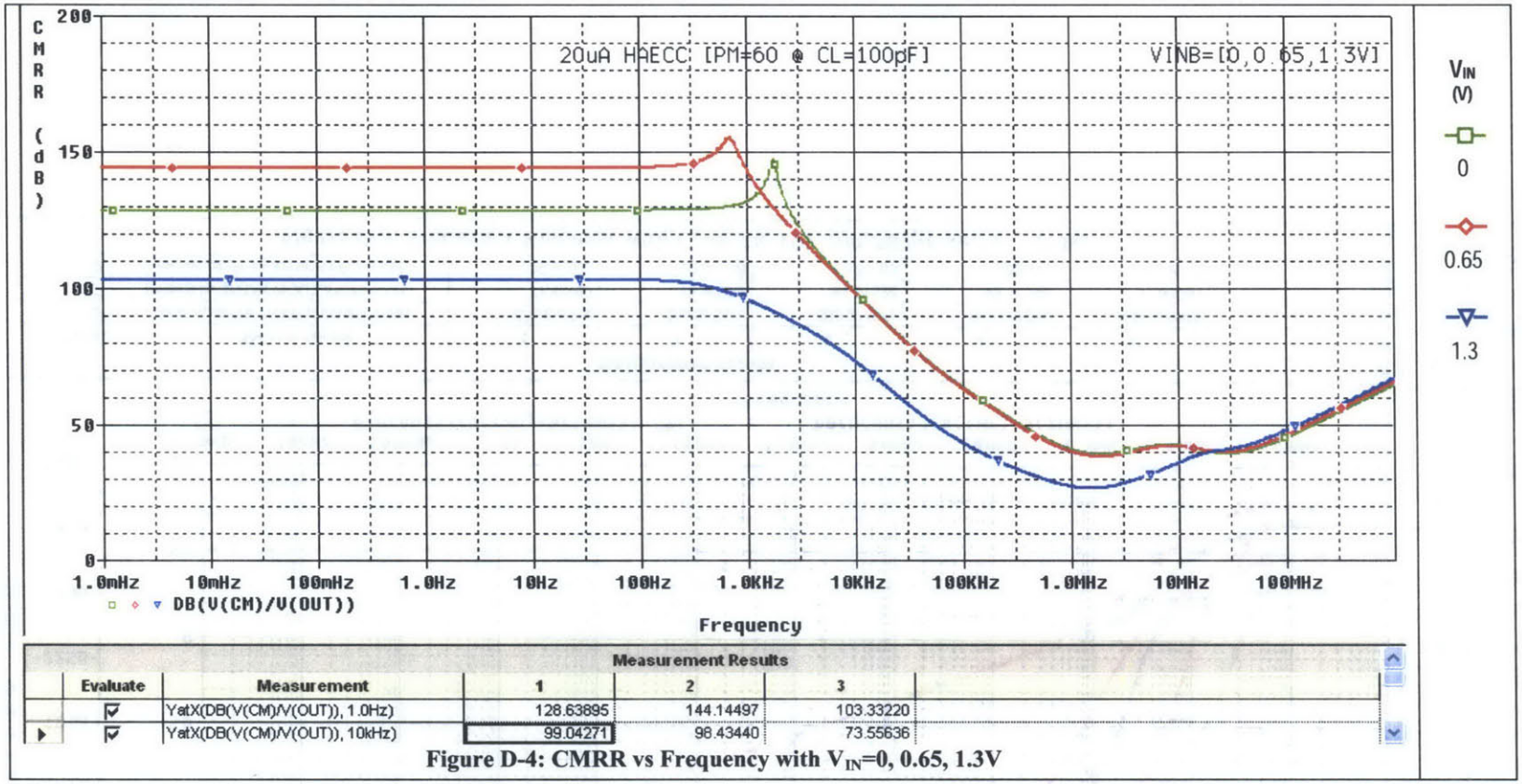


C_L (pF)	Symbol
0	Phase
	Gain
10	Phase
	Gain
100	Phase
	Gain
200	Phase
	Gain
500	Phase
	Gain

Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INB...	586.83775k	588.90541k	589.27467k	557.47221k	444.19937k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	77.48467	75.90232	61.81028	49.37346	31.60080
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	25.51093	20.97270	12.70153	10.83002	9.32663

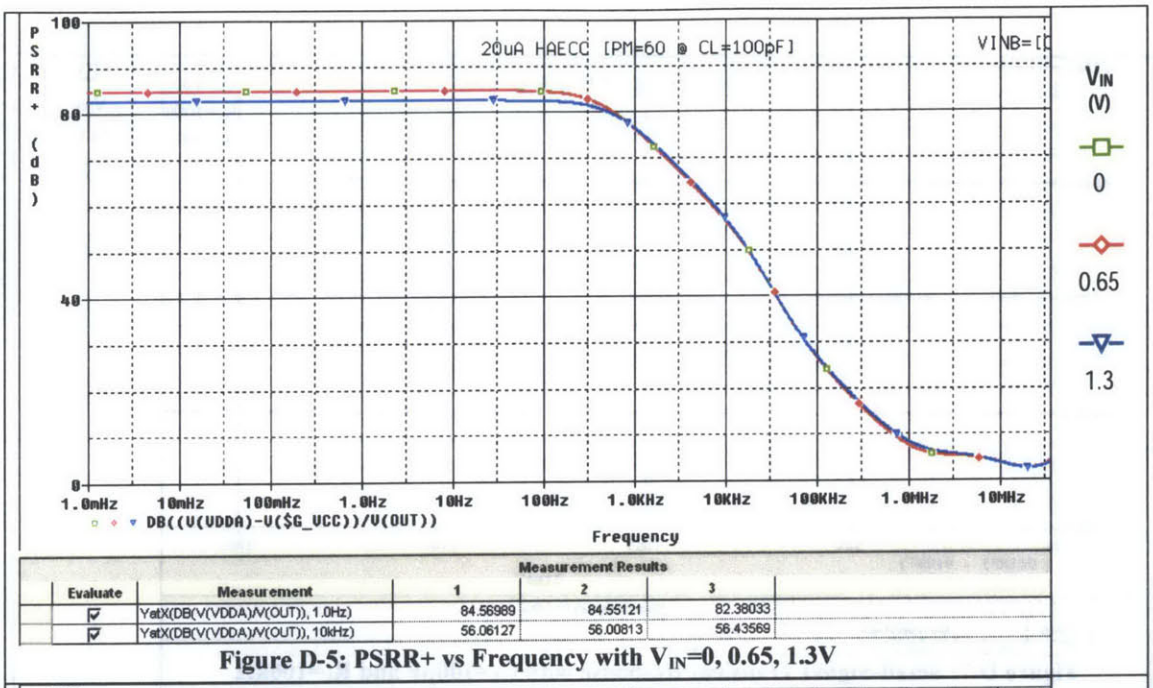
Figure D-3: Frequency Response with C_L=0, 10, 100, 200, 500pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	1	2	3
☑	YatX(DB(V(CM)/V(OUT)), 1.0Hz)	128.63895	144.14497	103.33220
☑	YatX(DB(V(CM)/V(OUT)), 10kHz)	99.04271	98.43440	73.55636

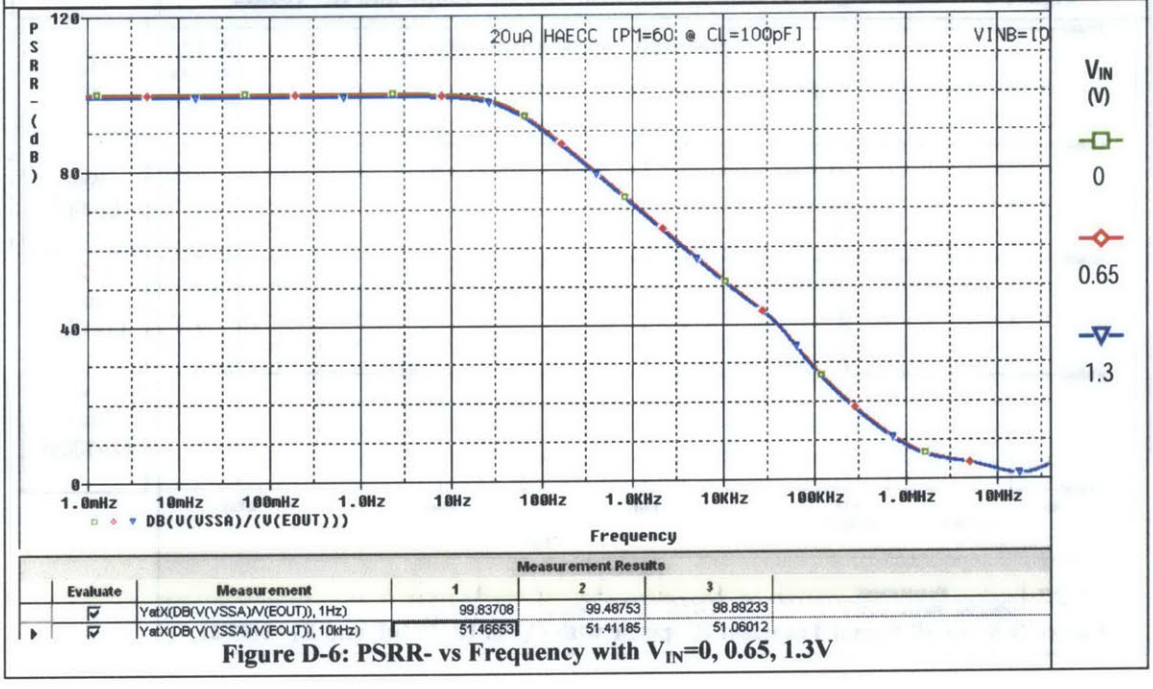
Figure D-4: CMRR vs Frequency with V_{IN}=0, 0.65, 1.3V



Measurement Results

Evaluate	Measurement	1	2	3
☑	YatX(DB(V(VDDA)/V(OUT)), 1.0Hz)	84.56989	84.55121	82.38033
☑	YatX(DB(V(VDDA)/V(OUT)), 10kHz)	56.06127	56.00813	56.43569

Figure D-5: PSRR+ vs Frequency with V_{IN}=0, 0.65, 1.3V



Measurement Results

Evaluate	Measurement	1	2	3
☑	YatX(DB(V(VSSA)/V(EOUT)), 1Hz)	99.83708	99.48753	98.89233
☑	YatX(DB(V(VSSA)/V(EOUT)), 10kHz)	51.46653	51.41185	51.06012

Figure D-6: PSRR- vs Frequency with V_{IN}=0, 0.65, 1.3V

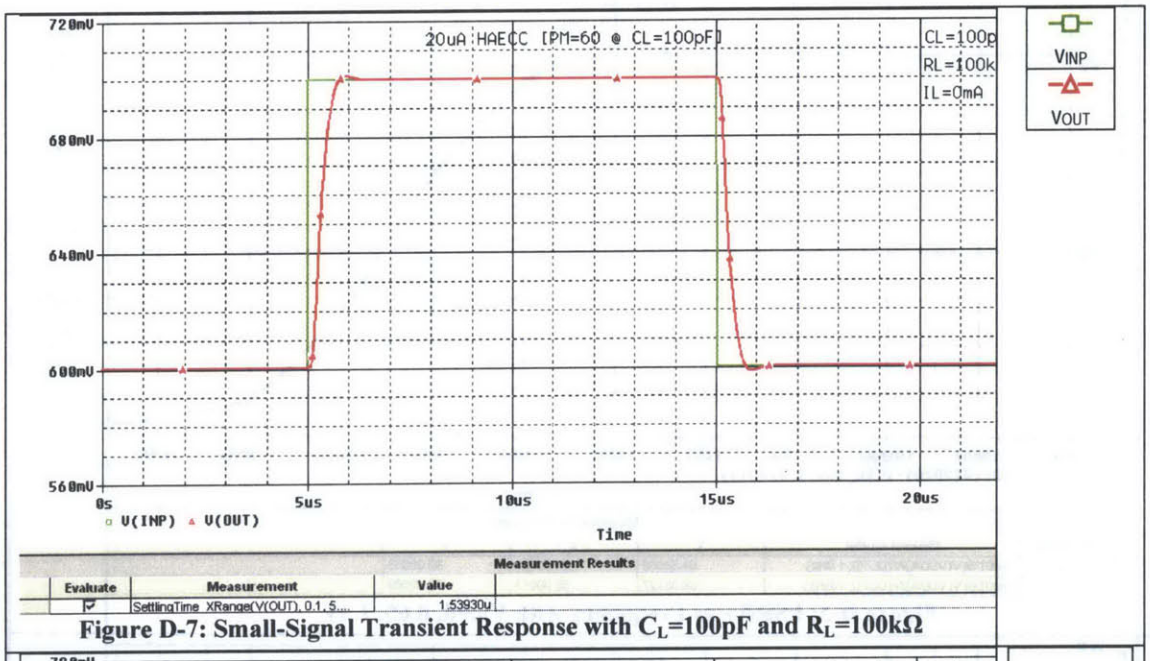


Figure D-7: Small-Signal Transient Response with C_L=100pF and R_L=100kΩ

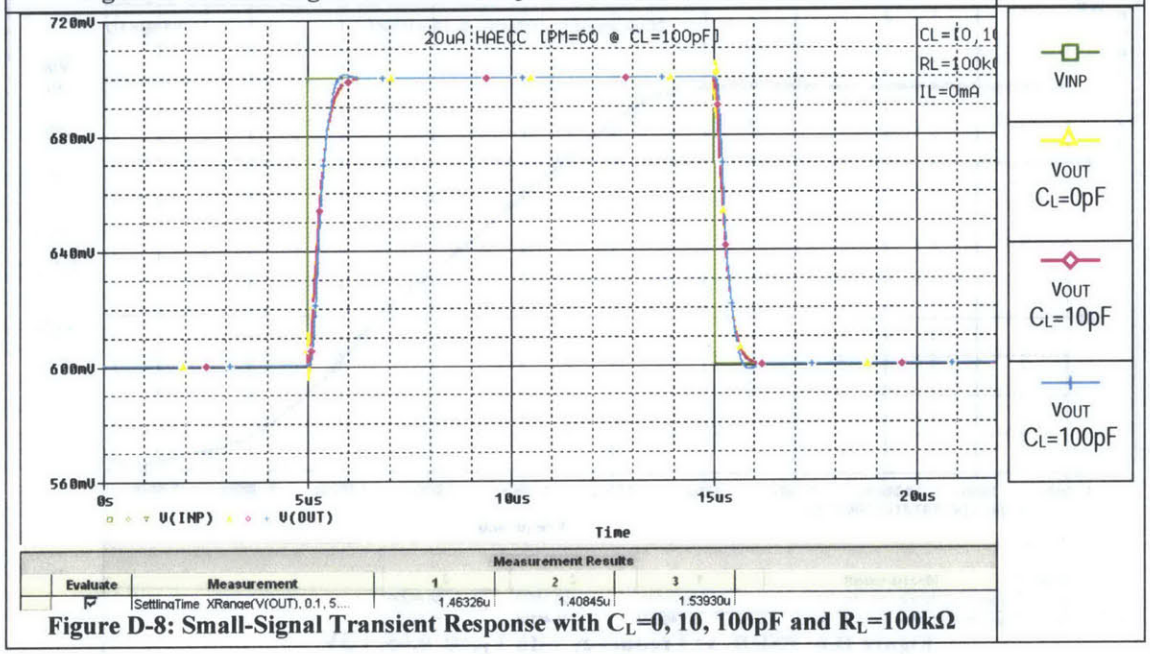
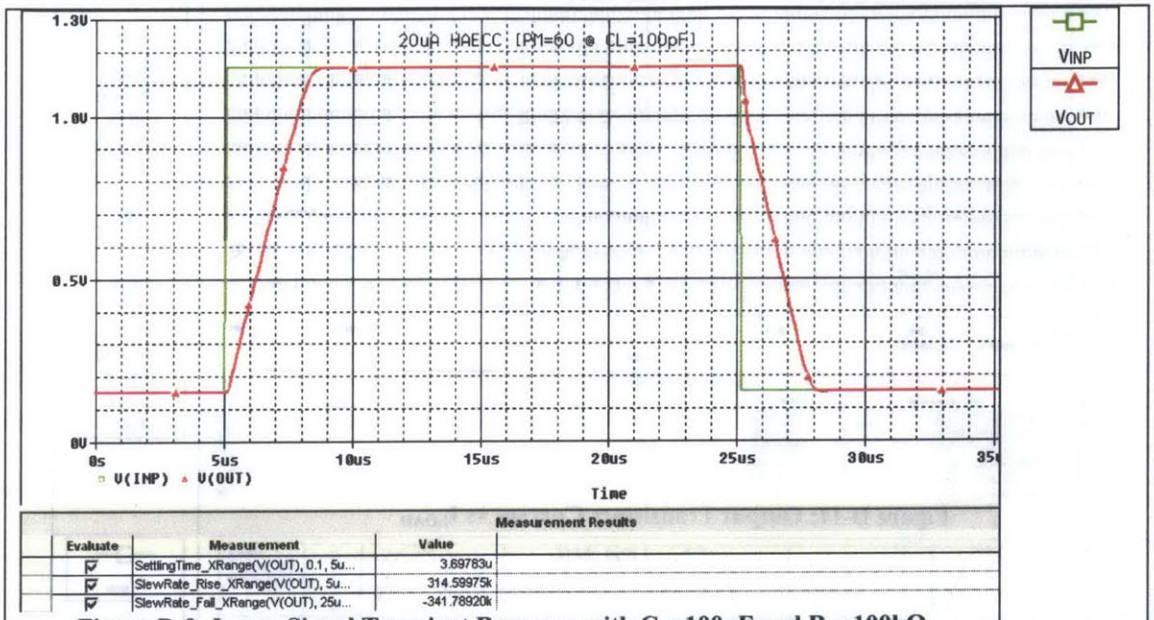
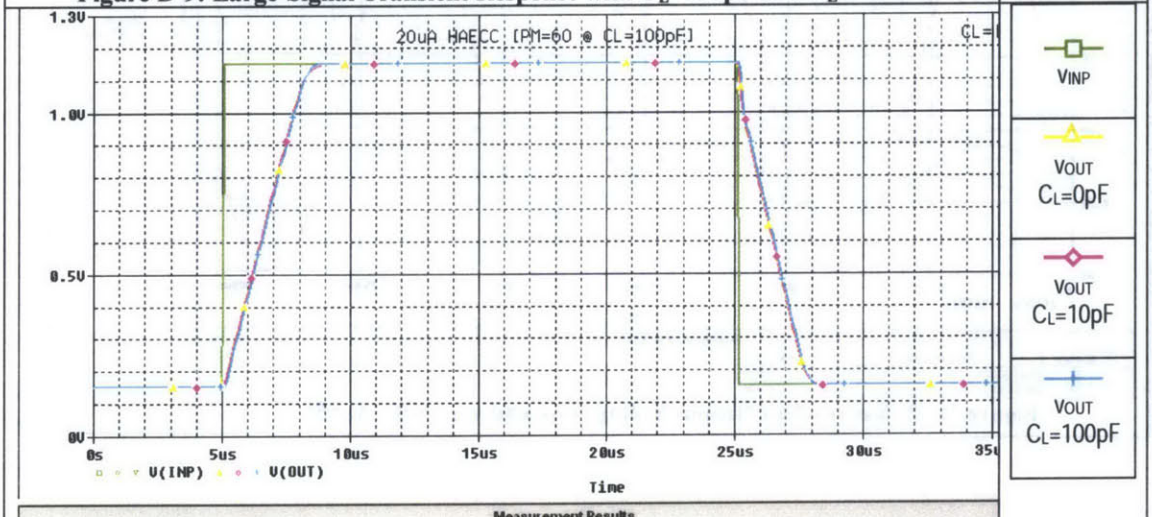


Figure D-8: Small-Signal Transient Response with C_L=0, 10, 100pF and R_L=100kΩ



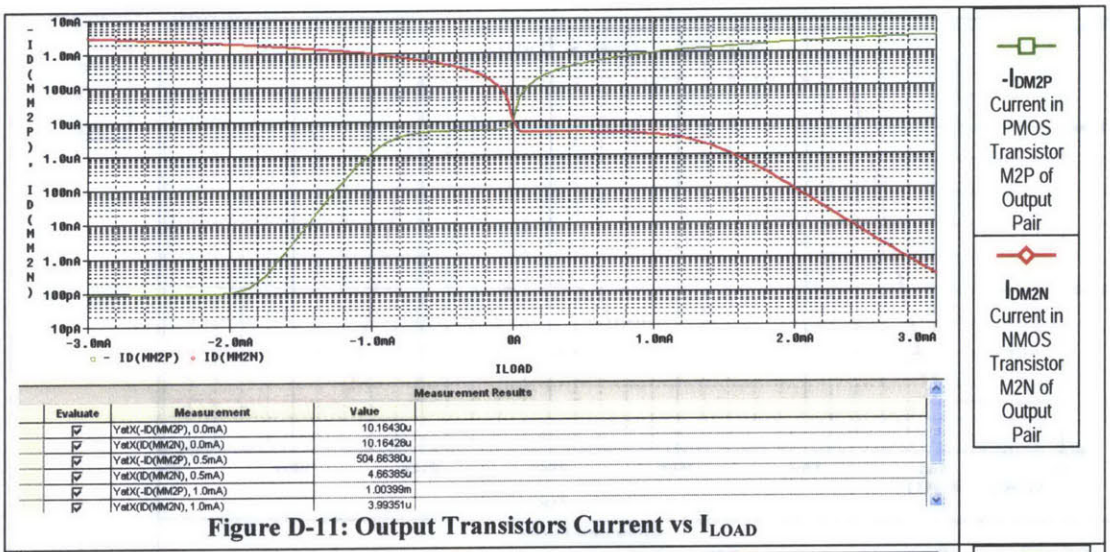
Measurement Results		
Evaluate	Measurement	Value
☑	SettlingTime_XRange(V(OUT), 0.1, 5u...	3.89783u
☑	SlewRate_Rise_XRange(V(OUT), 5u...	314.59975k
☑	SlewRate_Fall_XRange(V(OUT), 25u...	-341.78920k

Figure D-9: Large-Signal Transient Response with C_L=100pF and R_L=100kΩ



Measurement Results				
Evaluate	Measurement	1	2	3
☑	SettlingTime_XRange(V(OUT), 0.1, 5u...	4.03636u	4.00577u	3.70704u
☑	SlewRate_Rise_XRange(V(OUT), 5u...	313.07980k	313.22573k	314.60272k
☑	SlewRate_Fall_XRange(V(OUT), 25u...	-339.29720k	-339.58408k	-341.88000k

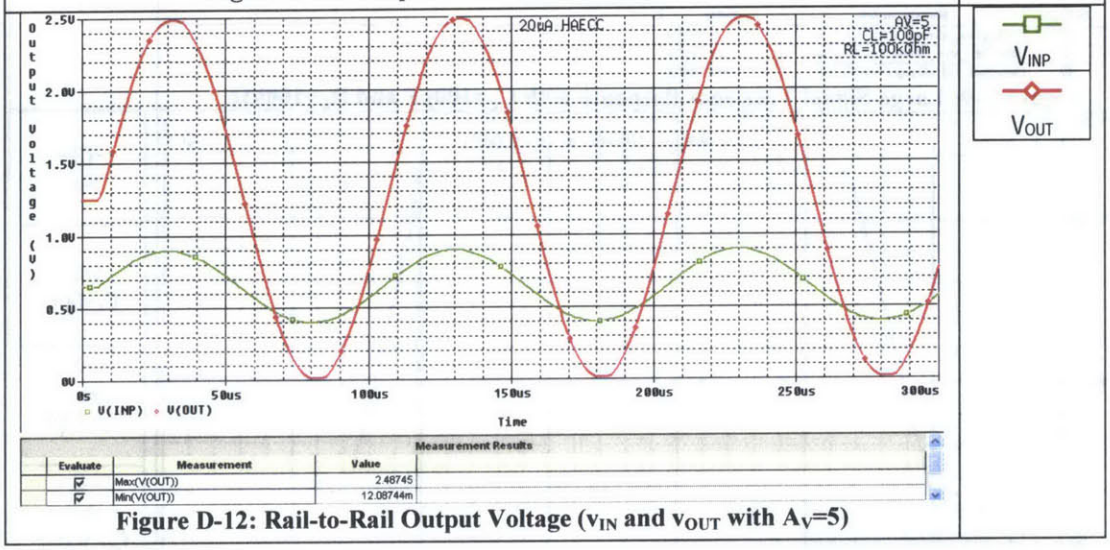
Figure D-10: Large-Signal Transient Response with C_L=0, 10, 100pF and R_L=100kΩ



Measurement Results

Evaluate	Measurement	Value
☑	YatX(-ID(MM2P), 0.0mA)	10.16430u
☑	YatX(ID(MM2N), 0.0mA)	10.16428u
☑	YatX(-ID(MM2P), 0.5mA)	504.66380u
☑	YatX(ID(MM2N), 0.5mA)	4.66385u
☑	YatX(-ID(MM2P), 1.0mA)	1.00399m
☑	YatX(ID(MM2N), 1.0mA)	3.99351u

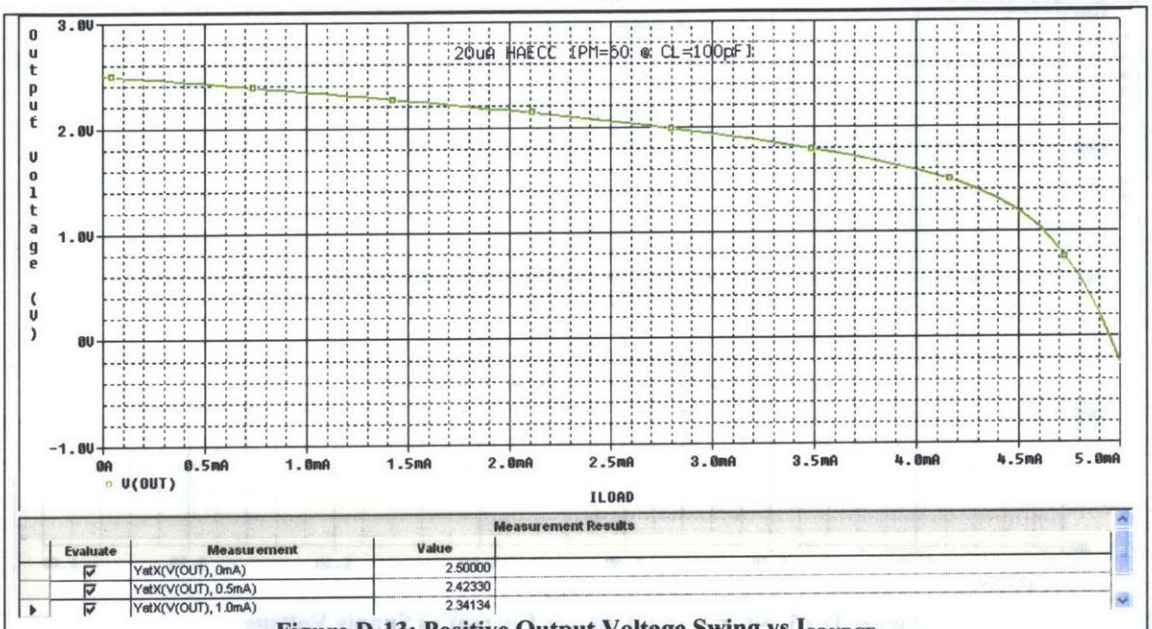
Figure D-11: Output Transistors Current vs I_{LOAD}



Measurement Results

Evaluate	Measurement	Value
☑	Max(V(OUT))	2.48745
☑	Min(V(OUT))	12.08744m

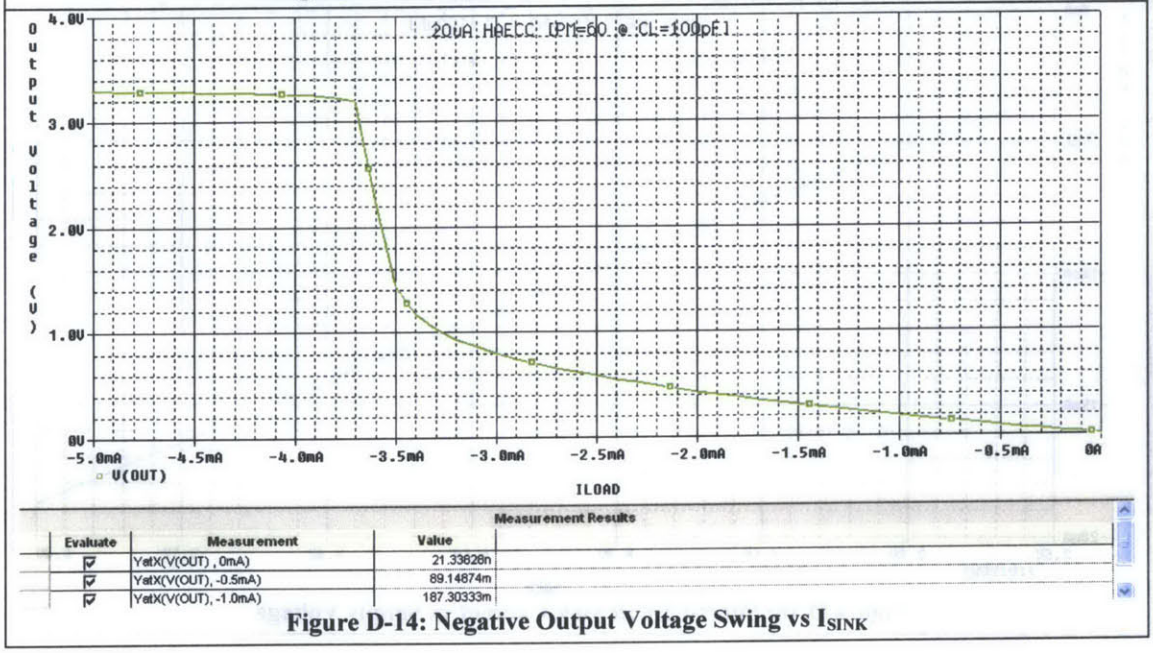
Figure D-12: Rail-to-Rail Output Voltage (v_{IN} and v_{OUT} with A_V=5)



Measurement Results

Evaluate	Measurement	Value
☑	YatX(V(OUT), 0mA)	2.50000
☑	YatX(V(OUT), 0.5mA)	2.42330
☑	YatX(V(OUT), 1.0mA)	2.34134

Figure D-13: Positive Output Voltage Swing vs I_{SOURCE}



Measurement Results

Evaluate	Measurement	Value
☑	YatX(V(OUT), 0mA)	21.33628n
☑	YatX(V(OUT), -0.5mA)	89.14874m
☑	YatX(V(OUT), -1.0mA)	187.30333m

Figure D-14: Negative Output Voltage Swing vs I_{SINK}

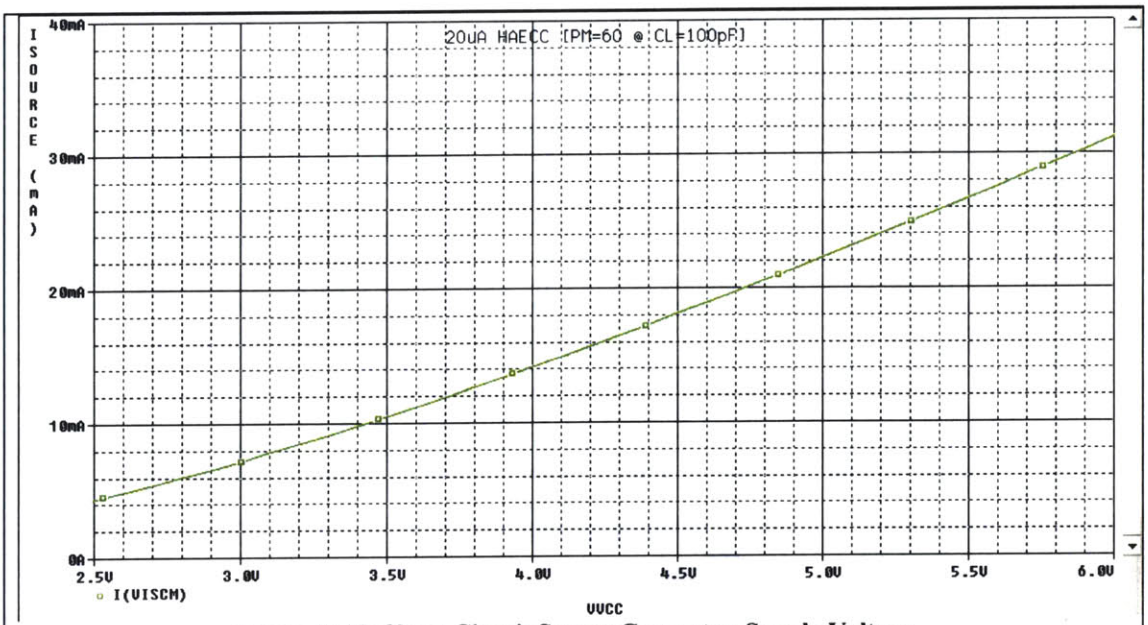


Figure D-15: Short-Circuit Source Current vs Supply Voltage

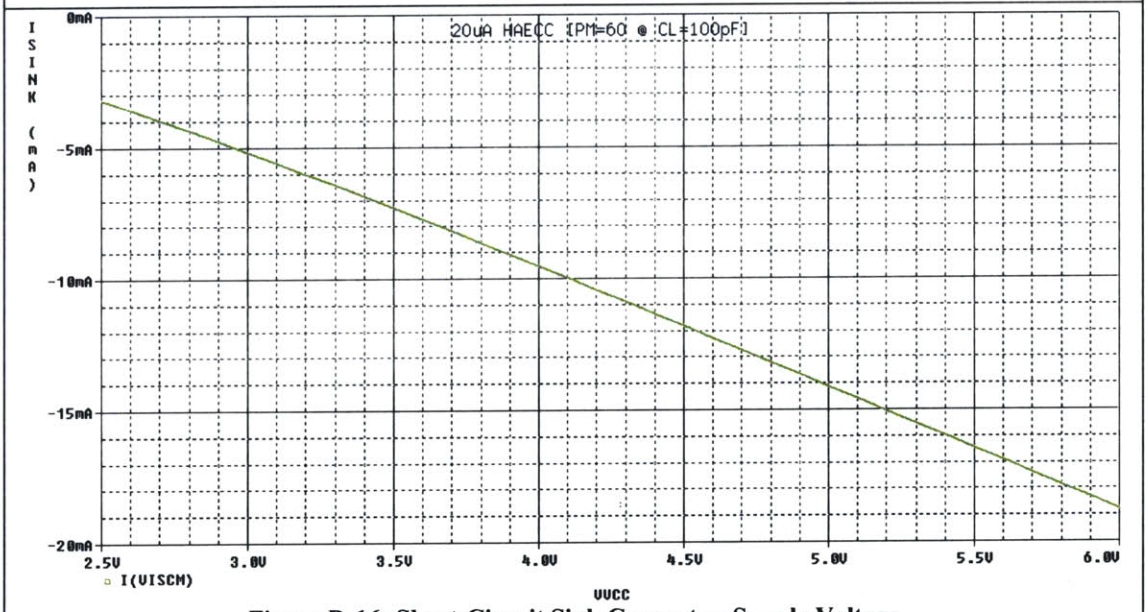
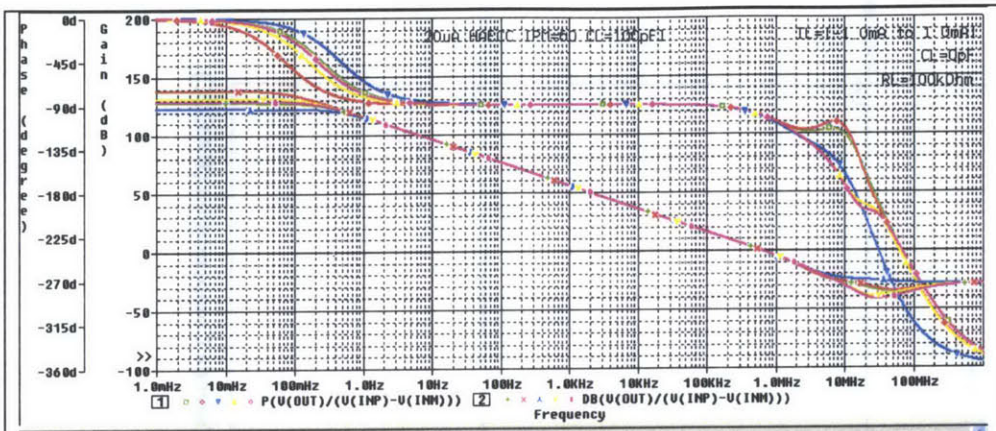


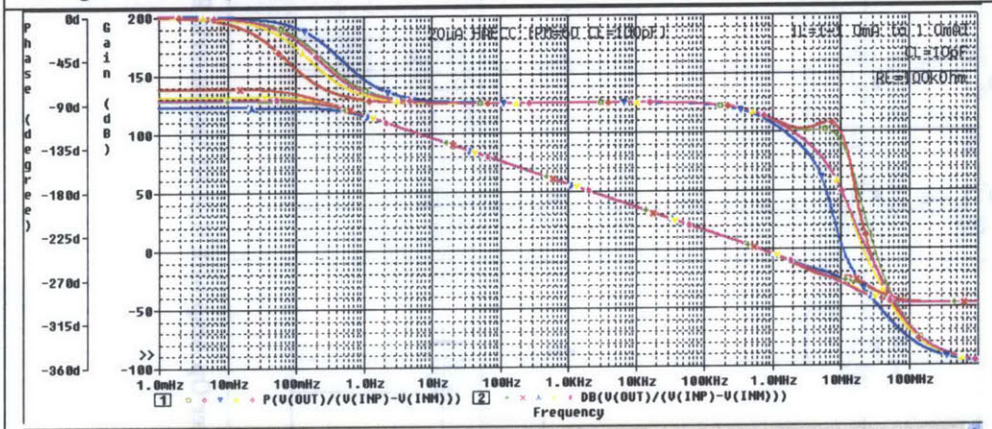
Figure D-16: Short-Circuit Sink Current vs Supply Voltage



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	584.07659k	584.65041k	586.83775k	591.48469k	590.26984k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	78.60797	78.66815	77.48467	78.35283	78.37453
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	34.25113	32.20876	25.51093	32.75536	32.45539
☑	Peak(DB(V(OUT)/(V(INP)-V(INM))), 1)	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

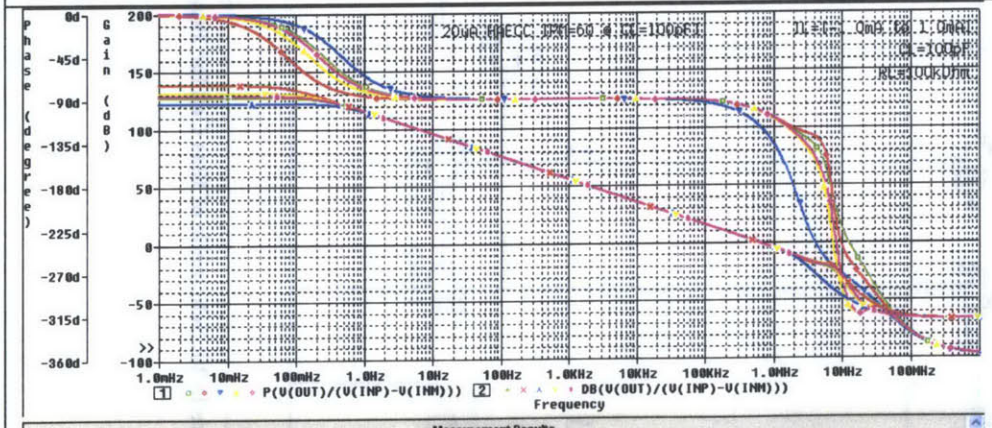
Figure D-17: Frequency Response with C_L=0pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	584.38701k	584.94673k	588.90541k	591.81251k	590.53056k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	78.40978	78.50589	75.90232	78.17528	78.22990
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	30.42695	26.44117	20.97270	29.09788	29.71966
☑	Peak(DB(V(OUT)/(V(INP)-V(INM))), 1)	<Evaluation Failed>	-25.28781	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

Figure D-18: Frequency Response with C_L=10pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA



Measurement Results

Evaluate	Measurement	1	2	3	4	5
☑	ZeroCross(DB(V(OUT)/(V(INP)-V(INM...	586.93508k	587.46075k	589.27467k	594.57008k	592.74819k
☑	PhaseMargin(DB(V(OUT)/(V(INP)-V(I...	76.61241	77.03397	61.81028	76.56415	76.91957
☑	GainMargin(P(V(OUT)/(V(INP)-V(INM)...	23.31790	19.51872	12.70153	19.05997	20.37360
☑	Peak(DB(V(OUT)/(V(INP)-V(INM))), 1)	<Evaluation Failed>	-19.24604	<Evaluation Failed>	<Evaluation Failed>	<Evaluation Failed>

Figure D-19: Frequency Response with C_L=100pF and R_L=100kΩ @ I_L=-1.0, -0.5, 0.0, 0.5, 1.0mA

I_L (mA)	Symbol
-1.0	Phase Gain
-0.5	Phase Gain
0.0	Phase Gain
0.5	Phase Gain
1.0	Phase Gain

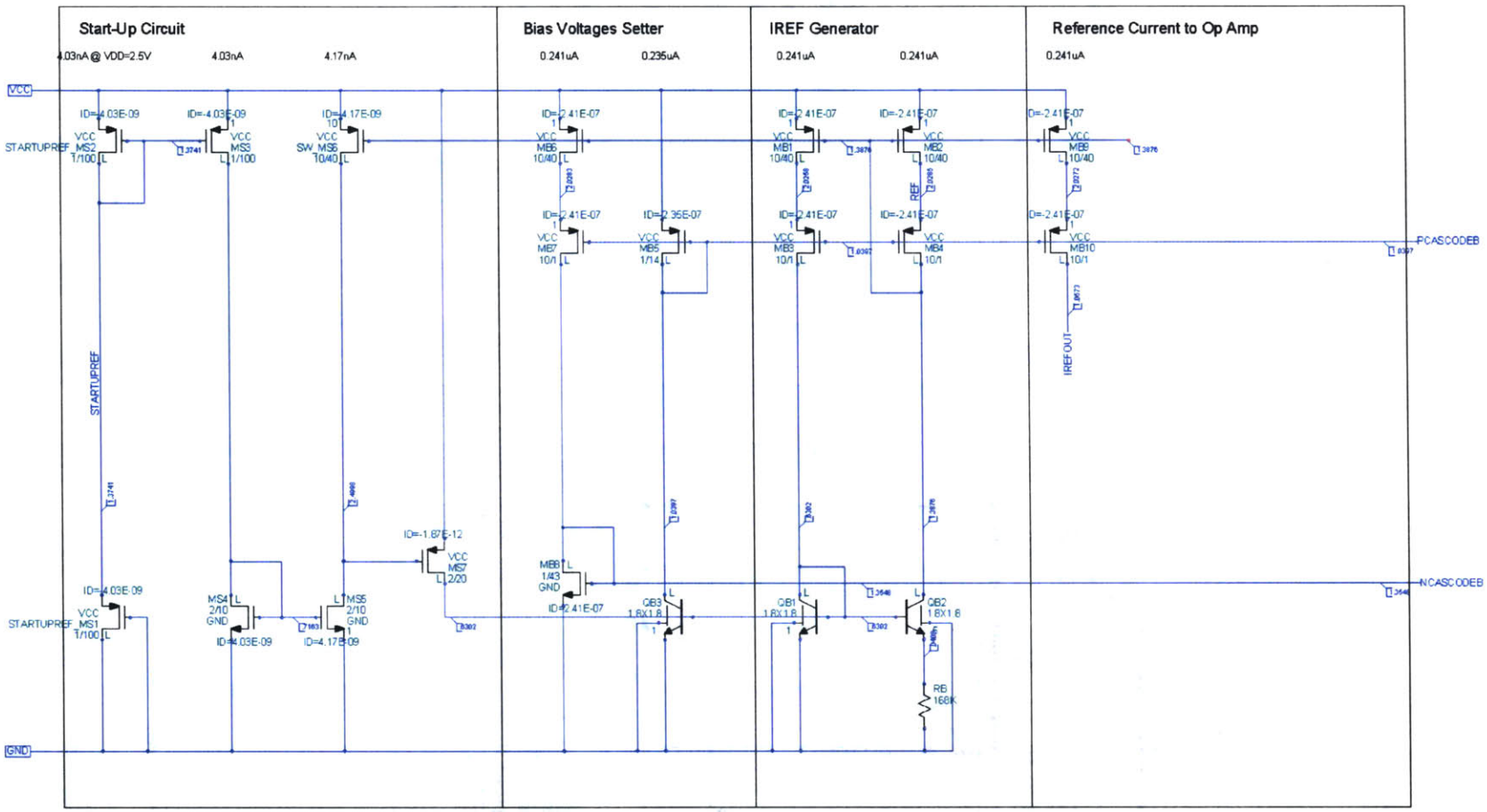
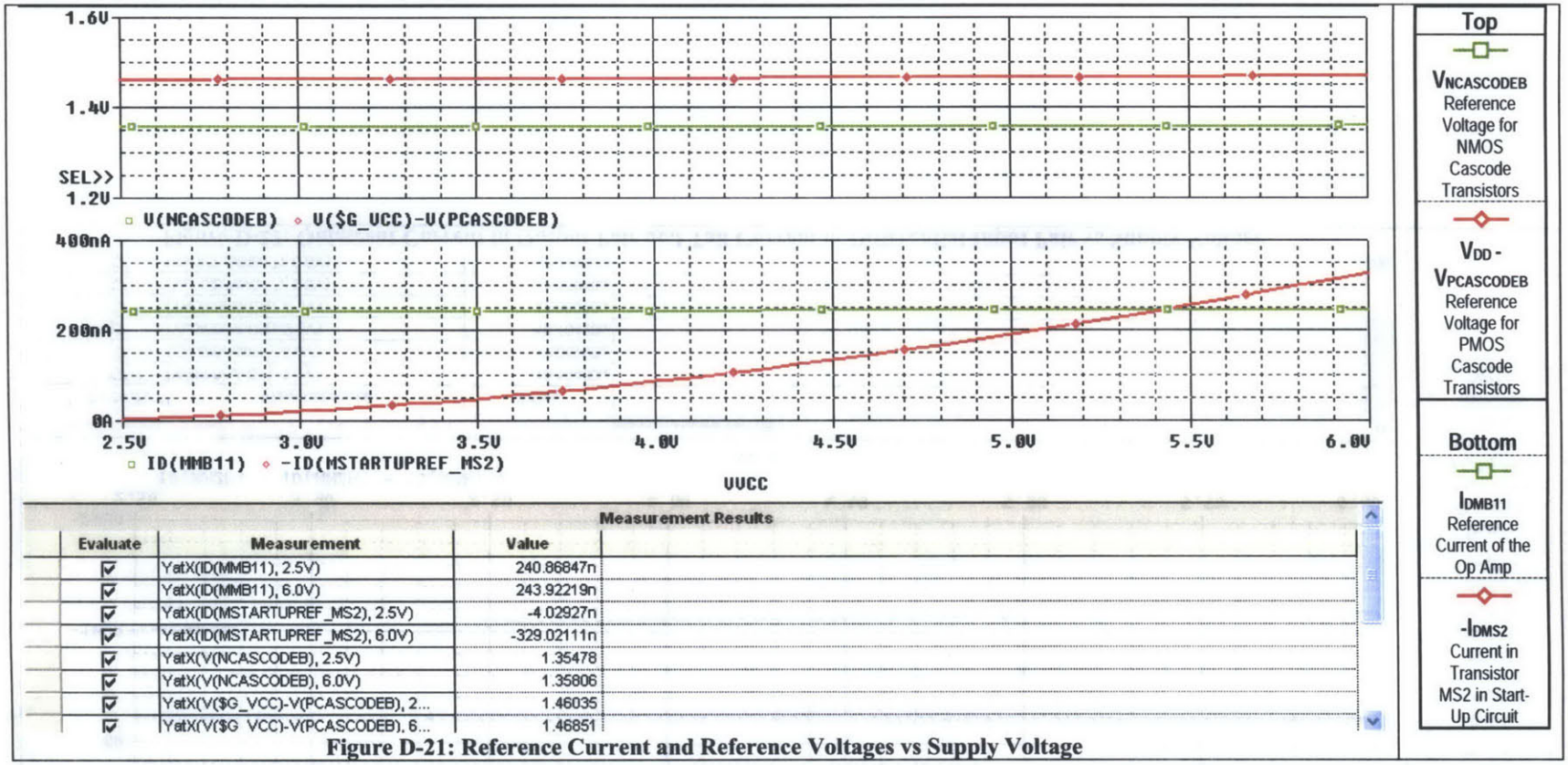


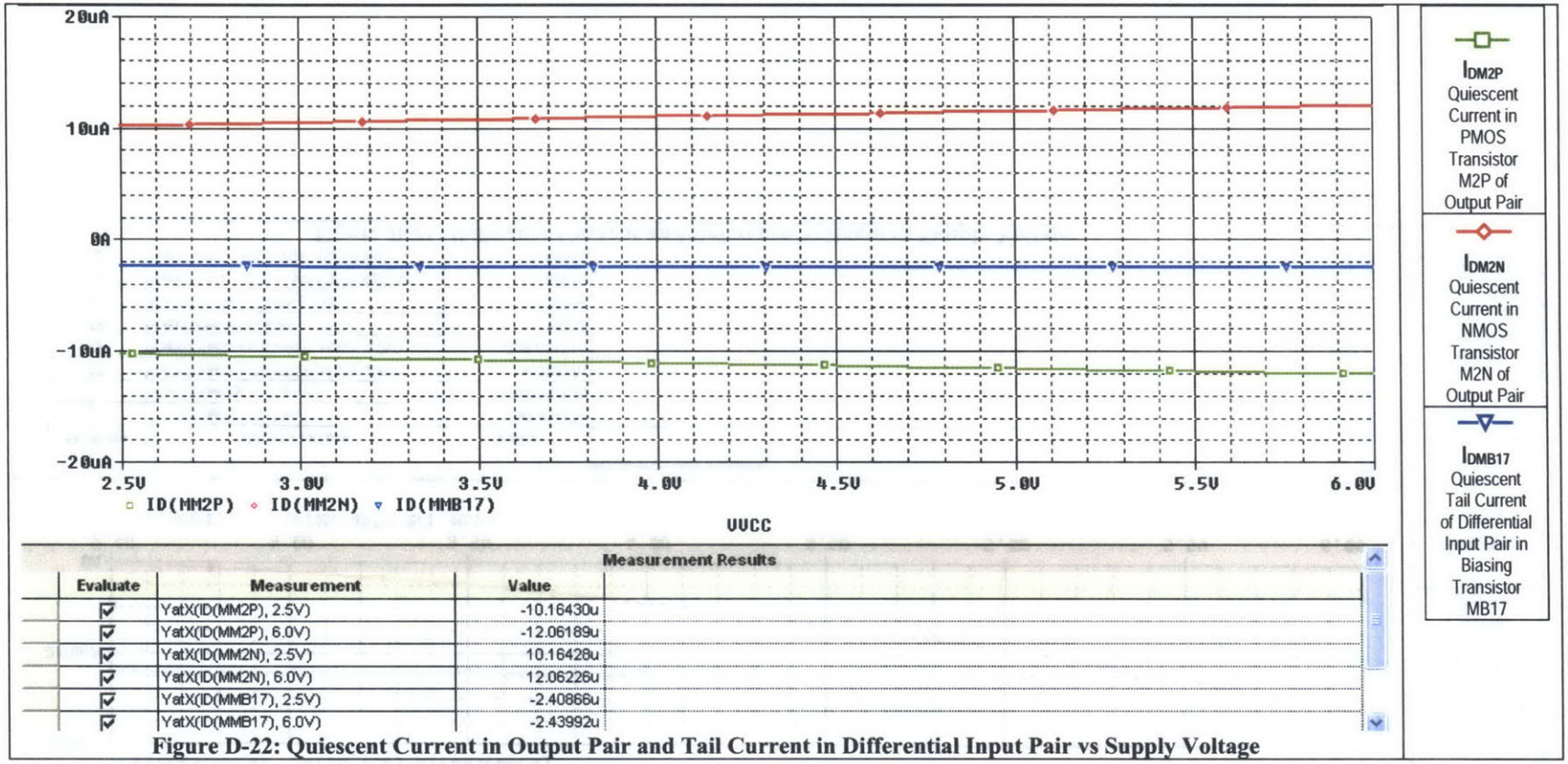
Figure D-20: Schematic of Bias Cell for 20µA Micropower Op Amp with Hybrid Asymmetric Embedded Cascode Compensation (HAECC)



Measurement Results

Evaluate	Measurement	Value
☑	YatX(ID(MMB11), 2.5V)	240.86847n
☑	YatX(ID(MMB11), 6.0V)	243.92219n
☑	YatX(ID(MSTARTUPREF_MS2), 2.5V)	-4.02927n
☑	YatX(ID(MSTARTUPREF_MS2), 6.0V)	-329.02111n
☑	YatX(V(NCASCODEB), 2.5V)	1.35478
☑	YatX(V(NCASCODEB), 6.0V)	1.35806
☑	YatX(V($G_VCC)-V(PCASCODEB), 2...	1.46035
☑	YatX(V($G_VCC)-V(PCASCODEB), 6...	1.46851

Figure D-21: Reference Current and Reference Voltages vs Supply Voltage



Measurement Results

Evaluate	Measurement	Value
☑	YatX(ID(MM2P), 2.5V)	-10.16430u
☑	YatX(ID(MM2P), 6.0V)	-12.06189u
☑	YatX(ID(MM2N), 2.5V)	10.16428u
☑	YatX(ID(MM2N), 6.0V)	12.06226u
☑	YatX(ID(MMB17), 2.5V)	-2.40866u
☑	YatX(ID(MMB17), 6.0V)	-2.43992u

Figure D-22: Quiescent Current in Output Pair and Tail Current in Differential Input Pair vs Supply Voltage

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