

Observation of Joule Heating-Assisted Electromigration Failure Mechanisms for Dual Damascene Cu/SiO₂ Interconnects

C.W. Chang, C.L. Gan, C.V. Thompson, K.L. Pey, W.K. Choi

Abstract— Failure mechanisms observed in electromigration (EM) stressed dual damascene Cu/SiO₂ interconnects trees were studied and simulated. Failure sites with ‘melt patch’ or ‘crater’ are common for test structures in the top metal layer, though the occurrence of such failure modes probably depends on the passivation layer thickness. Interconnects that were EM stressed for a short time and then stressed with increasing current to induce Joule heating in the line had similar failure sites to lines that were stressed to failure under standard EM conditions. This shows that some failure mechanisms during EM could be assisted by Joule heating effect.

Index Terms—Electromigration, Joule heating, failure mechanism.

I. INTRODUCTION

As features of integrated circuits are scaled to submicron dimensions for faster switching speed, the cross sections of interconnects are scaled concurrently while the lengths of interconnects are increased to accommodate larger chips with increasing functionality. These make the interconnects more sensitive to subtle defects that had not previously encountered in chip reliability [1]. These defects could be intrinsic defects caused by non-conformal processes due to an increasing difficulty in fabricating narrower lines and higher aspect ratio vias, which in turn aggravated by electromigration (EM) due to higher operational current density in the interconnects.

Obviously a highly reliable wiring that allows high current density is essential. Copper with its lower resistivity (1.67μΩ-cm), higher melting point (1085°C), good mechanical strength and better EM performance [2-5] emerges as a new material

for advanced interconnect metallization, replacing conventional materials such as aluminum (ρ=2.69μΩ-cm, T_m=660°C) or AlCu alloy.

However, the advantage of copper over aluminum is not as great as earlier anticipated due to copper electromigrates through interfacial diffusion path with activation energy lower than that of grain boundary diffusion. For narrow thin film line, interfacial and grain boundary diffusion could be the dominant fast diffusion paths, and the effective diffusivity can be given by [3]

$$D_{eff} = \frac{\delta_{gb}}{d} D_{gb} + \sum_i \left(\frac{n\delta}{t} D \right)_i \quad (1)$$

where the subscripts *gb* and *i* refer to the grain boundary and interface diffusion respectively, δ denotes the width of the diffusion path, *d* is the grain size, *t* is the line cross-sectional dimension (height or width) and *n* is the number of similar *t* that has the same interface. For a typical dual-damascene Cu/SiO₂ metallization scheme with Si₃N₄ as the capping layer and Ta as a diffusion barrier layer, if interfacial diffusion is the dominant diffusion path, equation (1) is reduced to

$$D_{eff} = \left(\frac{2}{h} + \frac{1}{w} \right) \delta_{Ta} D_{Cu/Ta} + \frac{\delta_{SiN}}{w} D_{Cu/SiN} \quad (2)$$

where *h* and *w* represent the height and width of the Cu metal respectively. In fact, recent studies [6,7] showed that the Cu/Si₃N₄ interface could be the dominant diffusion path, and the first term on the right side of equation (2) can then be neglected.

The EM failure distribution for fine Cu interconnects usually is bi-modal or sometimes even multi-modal. This is particularly true for fine Cu interconnect lines, i.e. 0.28μm line width [6,8]. Systematic study [8] showed that other than very early failure (infant mortality), three different modes of behavior can be observed in the drift resistance versus time plot. Some of the EM stressed samples exhibited an instantaneous, rapid increase of the resistance, leading to sudden failure. Some samples showed gradual, almost linear increase of the resistance after an incubation period, leading to eventual failure, while small portion of samples were immortal with little resistance shift. The reason for this multi-modal failure distribution is unclear, but it is obvious that different modes of failure correspond to different failure

C.W. Chang & C.L. Gan are with Singapore-MIT Alliance, 4, Engineering Drive 3, Singapore 117576 (e-mail: smap1040@nus.edu.sg; smap9005@nus.edu.sg).

C.V. Thompson is with Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139 (e-mail: cthomp@mtl.mit.edu).

K.L. Pey is with School of Electrical & Electronic Engineering, Nanyang Technology University, Nanyang Avenue, Singapore 639798 (e-mail: eklpey@ntu.edu.sg).

W.K. Choi is with Department of Electrical & Computer Engineering, National University of Singapore, 4, Engineering Drive 3, Singapore 117576 (e-mail: elechoi@eng1.nus.edu.sg).

mechanisms, and this controls when and how the samples fail over the stressing period.

This paper intends to explain some of the observed failure mechanisms due to electromigration, with experiments carried out to simulate the same failure mechanisms.

II. OBSERVATION OF EM-STRESSED SAMPLES

Samples that were electromigration-stressed were inspected using confocal microscope and scanning electron microscope (SEM). The samples were dual damascene Cu/SiO₂ width transition structures in the top metal layer of a 2-metal-layer wafer, with narrow to wide line width ratio ranged from 0.6:1.2 μ m to 0.6:4.8 μ m, and narrow to wide line length ratio ranged from 10:290 μ m to 280:20 μ m. The capping layer was Si₃N₄ and the diffusion barrier layer was Ta. A total of 90 samples were stressed in 6 runs of EM experiments with stressing current density of 2.5MA/cm² at the narrow lines and temperature at 350°C.

Three types of failure characteristics observed under the confocal microscope. Figure 1 shows some of the observed failure sites. A 32% (29 out of 90) of the total samples showed large black dots right at the cathode, 24% (22 out of 90) showed black patches of ‘melt’ at the cathode, and no damage observed for the rest. No correlation was found between the observed failure characteristics with the test structure’s width ratio and length ratio. The times-to-failure of the observed samples were also random.

When inspected under SEM, no irregularity was found for the samples with black patches of ‘melt’. Figure 2 shows an SEM image of a sample with large black dot at cathode end. A crater was found with a hole where the via is directly located beneath. The Si₃N₄ passivation layer was opened up entirely with splashes of materials around the hole. Traces of Cu were detected by EDX near the hole. Craters were also found for all samples having the same failure characteristics.

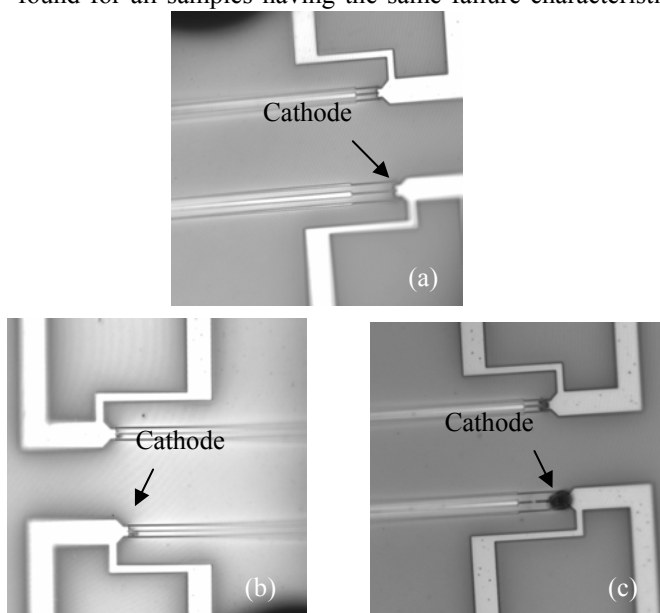


Fig. 1. (a) Cathode without damage observed. (b) ‘Melt’ at cathode. (c) Large black dots at cathode. Magnification: 400x.

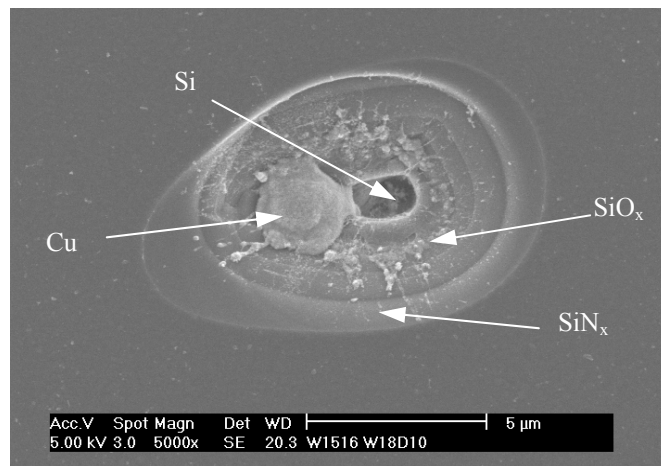


Fig. 2. SEM image of crater at cathode end. The element was confirmed by EDX.

Similar ‘volcano craters’ were also observed at some EM-stressed samples with other structures such as dotted-I’s (straight liner with 3 vias), T’s and cross interconnect trees.

The existence of the crater suggests that an eruption might have taken place at the cathode end during the EM stressing probably just before the line failed, leading to an open failure. Joule heating could be a possible factor for the eruption. When void is nucleated and material is drained away from the cathode during EM stressing, the cross-sectional area is reduced, and current density increased. It may come to a stage where the material left behind is so thin that the high current density induced Joule heating that raises the temperature locally high enough and melts the remaining metal. The weak passivation layer may then erupt and a crater is created. If the passivation layer did not break away, the melted metal would spread under the nitride layer at the failure site. The following experiments were designed to proof if the above postulation is valid.

III. EXPERIMENTS

A. Joule Heating

Joule heating effect was purposely introduced by feeding increasing current into the Cu line until it failed by exhibiting sudden increase of high resistance. Current sweep was done on L-shaped and asymmetric dotted-I interconnects trees using a HP-4155A parameter analyzer at room temperature. The L-shape interconnect consists of a long limb of 500 μ m and a short limb of 50 μ m, while the asymmetric dotted-I consist of a long limb of 200 μ m and a short limb of 100 μ m with a via in between. The line width of both structures was 0.28 μ m. A current sweep was set from 0 to 40mA to observe the resistance change. The current ramping step was set at 100 μ A with no delay between steps.

B. EM + Joule Heating

L-shape interconnect trees were EM pre-stressed to purposely create voids at the cathodes before carrying out the Joule heating test. The samples were EM stressed either at one limb or both limbs for various periods with a current density

of $2.5\text{MA}/\text{cm}^2$ at 350°C . The Joule heating test setting was same as above, except a delay of 60s was set between the current ramping steps for a set of samples.

IV. RESULTS AND DISCUSSION

A. Joule Heating

The resistance of the interconnect trees as a function of current is shown in Figure 3. For D37 and D38, only the $500\mu\text{m}$ long limbs of the L-shape interconnect trees were stressed. For D35, the $50\mu\text{m}$ short limb was also stressed in addition to the long limb. For D20, which is the asymmetric dotted-I line, both the $200\mu\text{m}$ long-limb and the $100\mu\text{m}$ short-limb were stressed. For D37 and D38 (single limb stressed), the lines failed at about 44mA while D35 and D20 (both limbs stressed) failed at about 41mA . All the lines showed almost instantaneous increase in the resistance, indicating a sudden open failure in the lines. The reduction of the resistance after the maximum point was due to the compliance of the parameter analyzer.

According to Figure 3, the maximum resistance when the failure occurred could be as high as 725Ω . If the resistance of the interconnects follow linear temperature dependence model $R=R_0(1+\alpha\Delta T)$ with the thermal coefficient of the resistance (α) for Cu of 0.0034K^{-1} , using $R = 174\Omega$ and $R_0 = 54\Omega$ for D20, the temperature in the line before failure was only 679°C , far below the Cu melting point of 1085°C . This temperature is not high enough to cause the eruption. But when open failure

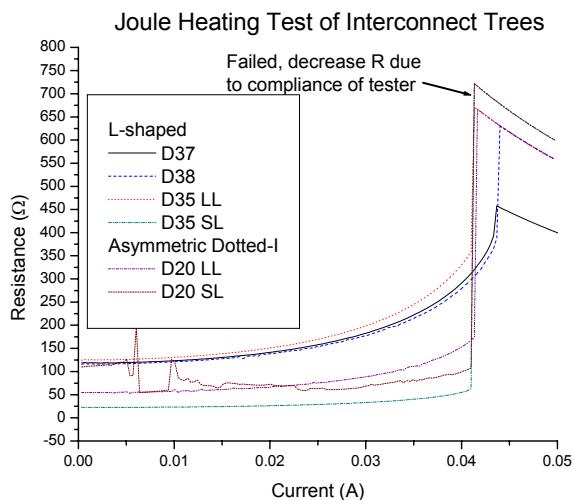


Fig. 3. Plot of interconnect resistance vs. current for Joule heating.

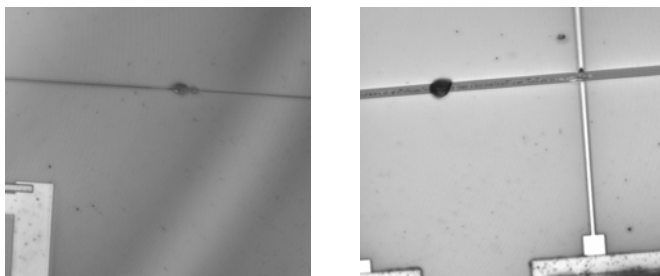


Fig. 4. Con-focal image of (a) L-shape interconnect of D37 (b) Dotted-I interconnect of D20. Magnification: 400x.

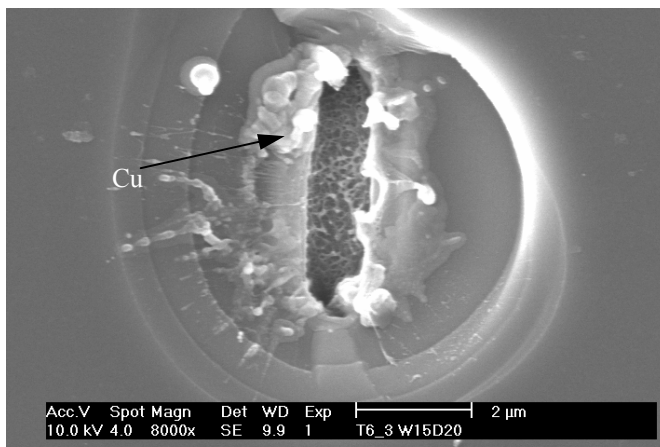


Fig. 5. SEM image of dotted-I interconnect failure site of D20.

occurred and the Cu metal was depleted in the interconnect, all the current would shunt through the thin Ta barrier layer. The high current density in the Ta layer would cause very high temperature in the void and melted Cu in the vicinity due to the high resistivity of Ta ($13\mu\Omega\text{-cm}$ for bulk material, compare to $1.7\mu\Omega\text{-cm}$ for Cu). The melted Cu would create very high pressure in the line and burst the weak Si_3N_4 passivation layer, hence created the crater. However, when observed under a confocal microscope, melt and black dot were found not directly at the cathode via but at about half of the liner length, at which SEM inspection showed similar eruption mechanism. Figures 4 and 5 show the confocal and SEM image of the damages respectively.

B. EM + Joule Heating

A plot of the interconnect resistance versus current is given in Figure 6. For D28, D29 and D33, only the $500\mu\text{m}$ long limb was EM pre-stressed before conducting joule heating test, and only the long limbs were stressed for Joule heating. For D4 and D5, both limbs were EM pre-stressed, while only the long limbs were stressed for Joule heating. No delay between current ramping steps was set for D29 and D4,

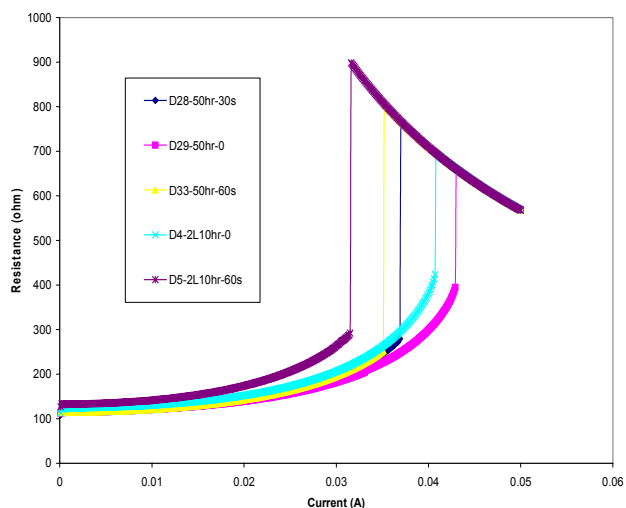


Fig. 6. Plot of interconnect resistance against current for EM + Joule heating.

whereas 30 seconds was set for D28, and 60 seconds was set for D33 and D5.

Without delay, the samples failed at about 40mA, similar to Joule heating without EM pre-stress. With delay of 30s, the current before open failure significantly reduced to 35mA. With delay of 60s, minimum failure current of 31.5mA was recorded. When observed under the confocal microscope, all samples Joule-heated without delay had failure sites similar to the melt patches at about half of the liner length. With delay of 30s and 60s, the failure sites shifted to about 1/4 of the liner length from the cathode end, though no failure site was observed right at cathode end. No crater was found for all samples. Figure 7 shows the confocal image of a failure site in D4 in the line middle. Figure 8 shows the SEM image of a failure site in D28 located close to the cathode. Note there are cracks at the nitride layer.

The absence of crater in this experiment was probably due to the fact that different structures may have different thickness of passivation layer though the samples were from the same lot, as thin or weak passivation layer may form crater easier. Another reason may be due to the probabilistic nature of the crater formation as only 32% of the total EM stressed samples

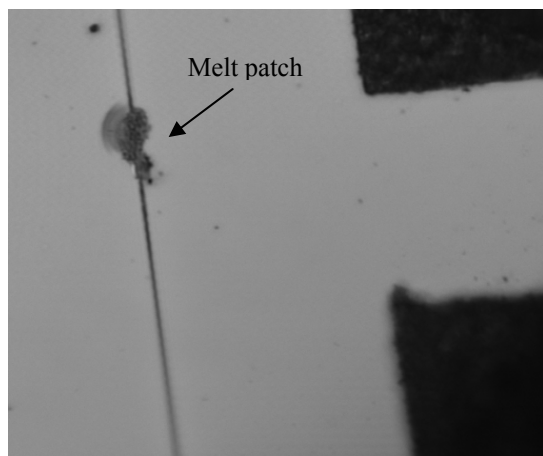


Fig. 7. Confocal image of L-shape interconnect with EM + Joule heating. Magnification: 400x.

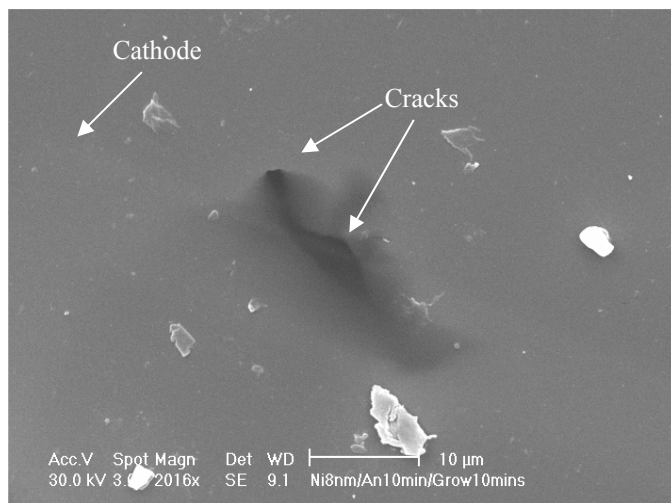


Fig. 8. SEM image of L-shape interconnect with EM + Joule heating. 60s delay between current ramping steps.

were observed to have the craters. This may also be attributed to the distribution of nitride layer thickness across the wafer or lot.

The shift of failure sites from middle of line to location closer to the cathode end when delay was set could be due to an equilibrium temperature has been reached that caused failure to occur at voided location in the line. Without the delay, though void existed in the line, the ramp of current was so fast that high heat was generated along the whole line in a short time. The middle of line could be the hottest part as it is furthest away from the vias where heat could be conducted away easily, and as a result, failure occurred at the location. If delay was set, as current ramped up slowly, the voided location of the line with the highest current density could be the hottest part where failure could occur. This may represent the actual failure mechanism for EM stressed samples.

V. CONCLUSION

Failure mechanisms observed in EM stressed samples were studied and simulated. Failure sites with melt patch or crater are common for Cu/SiO₂ test structures at the top metal layer. The occurrence of such failure modes probably depends on the passivation layer thickness. Interconnects with voids due to EM pre-stressing that were Joule-heated slowly had failure sites similar to lines that only had EM stressing. This suggests that the failure due to conventional EM stressing is assisted by Joule heating. Further work needs to be done to confirm the void existence under the melt patches. Joule heating directly in EM furnace after EM pre-stressing will also be conducted in the future to see if the existence of crater is affected when EM stressing and Joule heating are conducted separately.

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