Progress in Developing and Extending RM^3 Heterogeneous Integration Technologies

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***Abstract*—This paper describes recent progress in a continuing program to develop and apply RM^3 (recess mounting with monolithic metallization) technologies for heterogeneous integration. Particular emphasis is placed on the APB (aligned pillar bonding) and MASA (magnetically assisted statistical assembly) technologies. Next, ongoing research on applications of RM3 integration to produce optoelectronic integrated circuits (OEICs) for optical clock distribution, diffuse optical tomography, and smart pixel arrays are described. Finally, potential new applications of these technologies in intra- and interchip optical signal interconnects, in fluorescent dye detection and imaging for biomedical applications, and in III-V mini-IC integration on Si-CMOS for enhancing off-chip drive capabilities are outlined.**

***Index Terms*—** optoelectronic integration, heterogeneous integration, self assembly, III-V heterostructures, photodiodes, VCSELs, LEDs**.**

I. Introduction

THE desirability of integrating compound semiconductor functionality, including very high speed operation and efficient light emission and detection, with silicon CMOS circuitry has been recognized for many years, and so too have the challenges of doing such integration monolithically. These challenges include (1) significant differences between the lattice periods of silicon, gallium arsenide, and indium phosphide, (2) large differences in the thermal expansion coefficients of these same materials, and (3) the unavailability of large diameter III-V substrate wafers matching the commonly used silicon wafer diameters (200 and 300 mm). Over the years, a variety of approaches have been proposed to overcome these challenges, but in fact the only practical methods available at present to combine III-V functionality with Si-CMOS are in reality only modest refinements of hybrid assembly and bump-bonding techniques first developed almost 40 years ago[1]. A monolithic solution does still not exist.

A promising set of three technologies is being studied and developed at MIT to meet this monolithic integration need and thereby to extend the wafer level, batch processing method of manufacture that has had such a major economic impact on integrated electronics, to optoelectronic integration and ultimately to all mixed-media, mixed-material integration. The three technologies are Epitaxy on Electronics (EoE), Aligned Pillar Bonding (APB), and Magnetically Assisted Statistical Assembly (MASA).

These three technologies share a number of very important traits. First, they are all modular in nature in that they all add to, and build upon, an existing and established silicon integrated circuit foundation, and involve additional processing only after the silicon processing has been essentially completed on a commercial process line.[1] Second, in all of these technologies, the device or devices to be integrated with the silicon IC are placed in recesses formed in the dielectric layers covering the semiconductor wafer as shown in Figure 1a.

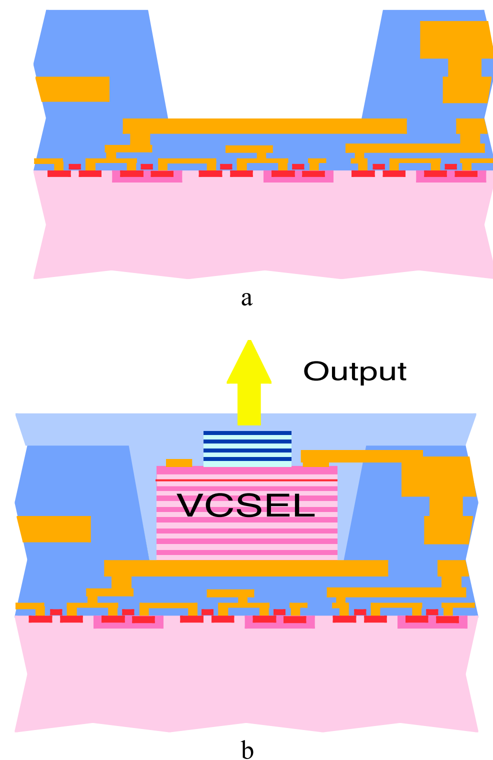

Figure 1 - The RM^3 concept: a. A cross-section of one of the recesses formed in the dielectric layers covering a commercially-processed integrated circuit wafer. b. After compound semiconductor heterostructure devices (VCSELs in this illustration) have been put into position in the recesses, their processing has been completed, and they have been connected monolithically with the underlying electronics.

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[1] "Essentially" because the additoinal processing occurs before the bond pads have been openned for bonding and before the wafer has been sawn into individual die.

The depth of the recess and thickness of the device structure being integrated are coordinated so that the upper surfaces of the devices are coplanar with the top surface of the integrated circuit wafer. This facilitates subsequent processing because it results in a planar surface on which one can deposit continuous metal films and on which precision photolithographic patterning can be performed.

The processing of the wafer is then continued to complete any remaining processing of the devices and to connect them monolithically to the underlying silicon circuitry using photolithographically defined thin-film metal lines.[2] The resulting integrated unit is pictured in Figure 1b.

This type of integration is described as recess-mounting with monolithic metallization, RM^3. The three technologies, EoE, APB, and MASA, differ in the method used to do the placement or mounting in the recesses, as will be explained in Section II. This leads to important differences in the applicability and utility of each process. The comparative advantages and disadvantages of the three RM^3 technologies will be discussed, and their current state of development will be reviewed.

In Section III ongoing research directed at applying RM^3 technology to three representative problems will be presented. And in Section IV several new applications and new integrated device structures will be proposed, and a potentially very significant extension of RM^3 technologies into a totally new application space, IC mini-chips, will be described. Finally, the paper will be concluded in Section V with an overview of the present status of RM^3, and comments on future directions the technologies can be expected to take.

II. The Current Technologies

A. Epitaxy on Electronics

The original RM^3 technology was proposed almost ten years ago when VLSI-level GaAs integrated circuits processed with Si-like backend processing (gold-free refractory ohmic contacts and gate metals, and Al-based interconnect metallization) became available from companies such as Vitesse Semiconductor [2]. When it became established that these circuits could withstand the temperatures encountered in molecular beam epitaxy of III-V heterostructures [3], it then became feasible to grow optoelectronic device heterostructures in recesses opened to the substrate on processed GaAs ICs. This technology is called Epitaxy on Electronics, EoE [4].

EoE has been used to produce a variety of optoelectronic integrated circuit chips and in 1996 was made available to the optoelectronics community in the form of a limited foundry run, the OPTOCHIP Project, which combined standard MOSIS processing and custom processing at MIT. A 6 mm by 6 mm chip containing 2 mm by 2 mm chip designs from researchers at 9 universities in the US and Canada and containing almost 200 EoE-integrated InGaP/GaInAs LEDs was produced, and several copies of their completed 2 mm square mini-chips were supplied to each of the participating groups. At the present time the most active work on the EoE process is being done by Dr. Aitor Postigo at the Instituto Microelectronica de Madrid in Madrid Spain and by SMA Fellow Professor Yoon Soon Fatt at Nanyang Technological University. These efforts concern integrating in-plane laser diodes and 1.55 µm GaInNAs photodiodes on GaAs ICs, respectively.

The EoE process has been used to produce some of what are arguably the most complex monolithic optoelectronic integrated circuits ever made, yet it clearly has important limitations. The epitaxial growth temperature must be kept below 375 °C, which can compromise the material quality and the device performance. Furthermore, the substrate provided by the integrated circuit wafer is also often not optimum for epitaxy because it is optimized for the IC manufacturer's primary focus, his integrated electronics. Finally, EoE is not compatible with silicon integrated circuits, and this is perhaps its most significant limitation. The solution of trying to do the necessary epitaxy on silicon IC chips is obvious, but in spite of many years of investigation by many researchers around the globe, it has not yet been possible to grow III-V heterostructures with sufficient quality on silicon substrates to make EoE on silicon feasible, and alternative approaches to RM^3 integration have had to be developed.

B. Aligned Pillar Bonding

With the dramatic increase in applications of various types of wafer bonding techniques and the availability of precision aligned bonding equipment it has become practical to use these tools to implement the RM^3 concept. This realization has led to the development of the Aligned Pillar Bonding technique. In APB the heterostructures to be integrated are grown separately on their optimal substrate and under the optimum conditions. The epitaxial wafer is then etched to form an array of shallow mesas, or pillars, whose pattern mirrors that of the recesses on the integrated circuit wafer. The two wafers can then be placed face-to-face, aligned to match the pillars with their recesses, brought into contact, and bonded together. The substrate under the epitaxial heterostructures is then removed leaving them in place in the recesses and ready for further processing, just as was done in EoE. This aligned bonding step in this process is illustrated in Figure 2.

As mentioned above, an important advantage of APB is that the III-V heterostructures can be grown under much more favorable conditions than in EoE. In fact, they can be grown by anyone anywhere in the world and delivered to the group doing the APB assembly, just as the integrated circuits can be obtained form a chip foundry anywhere in the world. In both cases the optimum source can be used for each unit. In the present MIT work, for example, InGaAs/InP p-i-n photodiode heterostructures grown by SMA Fellow Professor Yoon Soon Fatt at Nanyang Technological University are being integrated on Si-CMOS chips designed at MIT and processed at TSMC in Taiwan (see Section III-A below).

Another important new feature introduced to RM^3 processing by the APB process is the option of increasing the

[2] The importance of patterned thin film metal interconnects was first recognized by Robert Noyce in 1957 when he invented the monolithic silicon integrated circuit at Fairchild Semiconductor, and with Jack Kilby of TI started the silicon microelectronics revolution. The RM^3 technologies recognize that this simple but profound concept is no less important to doing successful heterogeneous integration.

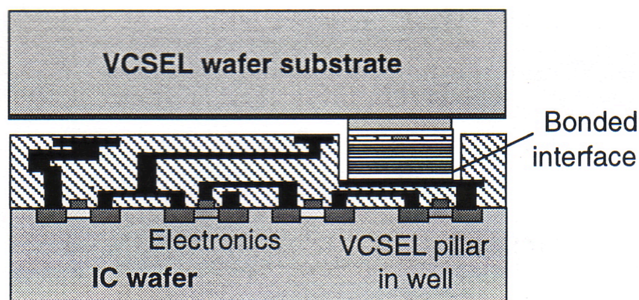

Figure 2 - A cross-section cartoon of the point in the APB process after which the pillars on the heterostructure wafer have been aligned with the recess on the integrated circuit wafer and the two have been bonded together. Immediately after this the region between the two wafers is filled with epoxy and then the substrate of the heterostructure wafer is removed leaving the recesses filled with device heterostructures.

chip density through the use of three-dimensional integration. That is to say, the recesses on the IC chip prepared for APB integration in general terminate on a metal pad, rather than on the substrate surface as they do for EoE. Thus if this pad can be formed in one of the upper metal layers it is possible to place devices underneath the recess and to use this otherwise lost wafer real estate.

The APB process was originally demonstrated by MIT graduate student Hao Wang [5]; it is currently being refined and extended by two current students, Wojciech Giziewicz and Eralp Atmaca.

One of the important issues in the APB process is the type of bonding used. In developing APB the MIT group has chosen to use metal-to-semiconductor bonding, and specifically to form a bond between palladium and the III-V compound (in general an arsenide, either GaAs or InGaAs). The advantages of this type of bond are that it (1) forms at temperatures as low as 230˚C, (2) uses metal films with a total thickness less than a micron, (3) does not involve the use of a flux, (4) is thermally robust, and (5) is compatible with forming low resistance ohmic contacts on both n-type and p-type layers. In the present APB process, the Pd-based bonding layers are deposited and patterned in the recesses on the integrated circuit wafer, and bare pillars are bonded to them. The alignment and bonding process is currently being done on a Research Devices Model M8A Flip-Chip aligner/ bonder.

Another important issue in APB is the removal of the epitaxial wafer substrate after bonding. The most elegant way of accomplishing this ultimately will be to use an etch-release layer near the base of the pillars that can be selectively etched away to undercut and release the pillars from their substrate. In the short term, however, an easier approach which involves fewer materials compatibility issues is to fill the space between the two bonded wafers with an epoxy designed for this purpose and for use with bump-bonded chips on multi-chip modules, and to then etch the substrate completely away down to an etch-stop layer near the base of the pillars. Often this etch-stop layer is the same one that would be used as an etch-release layer in the more elegant approach; in the case of GaAs-based structures it can be AlAs, and in the case of InP-based structures it can be InGaAs. The etchant used to etch away the substrate also depend on the substrate. For GaAs it is best to use a rapid etchant to remove the bulk of the substrate, and to then switch to a slower etchant which provides better selectivity, to finish the etching. For InP it is possible to use a rapid etchant, HCl, for the entire process because the selectivity of this etchant is sufficiently high.

APB offers significant advantages over EoE, but it still has limitations. In particular, one must still be careful to match the thermal expansion coefficients of the two wafers being bonded. This means that silicon-on-sapphire (SOS) ICs can now be used, as well as the GaAs ICs used in EoE, but it is still an important limitation if APB is to be extended to full-wafer processing. For chip-by-chip processing, which is what is being done in the applications research program (see following sections) APB works well with silicon CMOS chips, and APB is the current work-horse technology for this work.

There is a second wafer mismatch issue in APB which it will be important to deal with simultaneously with the thermal expansion coefficient mismatch issue. That is the mismatch between the available diameters of III-V materials and silicon. The standard diameters for silicon IC processing today are 200 mm and 300 mm, whereas the diameter of the largest GaAs available is 150 mm and for InP it is 100 mm. Since in APB two wafers are being bonded together, it is far more efficient if both are the same diameter.

A possible solution of for both of these wafer mismatches, i.e. of the thermal expansion coefficients and of the diameters, is to revisit the problem of III-V epitaxy on silicon wafers. With APB it is no longer necessary to do the epitaxy on silicon integrated circuits, so that constraint can be removed. This is true because once the III-V heterostructures have been grown on the silicon substrates they can be etched into pillars and transferred by standard APB processing to the silicon ICs. This in turn means that the misoriented Si substrates that are necessary to suppress anti-phase domains in III-V layers grown on Si can be used, and it also means that many of the newer developments in the growth of III-Vs on Si, such as the use of Si-Ge buffers proposed at MIT by SMA Fellow Prof. Eugene Fitzgerald, can be incorporated. Whether such buffers will be sufficient to produce sufficiently high quality III-V heterostructures remains to be seen, of course, but if they are successful they can immediately be used with the APB process.

An alternative approach to growing III-V heterostructures on silicon is being pursued at MIT by Professor Fonstad's group. In 1992 Burns and Fonstad demonstrated that strain-free laser diodes could be fabricated on silicon if the thermal expansion mismatch strain was relieved using an etch-free layer between the device heterostructure and the underlying silicon [6]. Building on this work and on processes developed for MEMS, Ph.D. student Henry Choy at MIT is investigating the MBE growth of InP-based heterostructures on silicon membranes, again with the idea of relieving the thermal expansion mismatch stain. If this work is successful

it can be used to provide III-V heterostructures on large diameter silicon substrates for use in APB integration.

Other work on III-V epitaxy on silicon that is of interest in this program is work of SMA Fellow Professor Chua Soo Jin at the National University of Singapore on the growth of GaN and GaAlInN heterostructures on silicon. These materials are of importance for green, blue, and ultraviolet light emitting diodes, and experience indicates that they are easier to grow on silicon than are GaAs and InP based heterostructures. Consequently, this work can also supply material on silicon for APB integration (see also Section IV-A).

C. Magnetically Assisted Statistical Assembly

APB is a powerful technology, and it is currently being used to implement several optoelectronic integrated circuits for a variety of applications (see Section III), but there are still reasons to look for other ways of doing RM^3 integration. For example, it is not at all certain that all of the heterostructures of interest can ultimately be grown on silicon. In fact, in is almost certain that many cannot. And even for those device structures that can be grown on silicon, the APB process makes relative inefficient use of the epitaxial material because the density of pillars in quite low. In fact, for most applications only a fraction of a percent of the epitaxial material area will remain after the pillars are formed; the rest will have been etched away.

To overcome these final shortcomings Professor Fonstad has proposed a radical new RM^3 technology, Magnetically Assisted Statistical Assembly (MASA). In MASA the heterostructure pillars are etched in a dense close-packed array and then are etched free from their original substrate to yield thousands of nanopills. A typical nanopill might be 40 to 50 microns diameter and 5 to 7 microns thick; a photograph of a representative nanopill is shown in Figure 3. In forming these nanopills very efficient use is made of the epitaxial material, unlike the situation in APB and EoE.

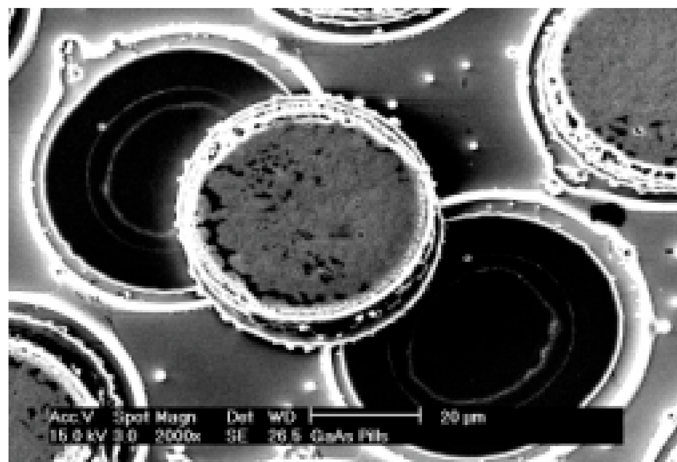

Figure 3 - A photomicrograph of a GaAlAs heterostructure nanopill prepared for MASA integration. The diameter of this pill is 45 microns and it is 5 microns thick. The patterns in the background are on the underlying substrate from which the nanopill has been released.

The "assembly" part of the MASA process refers to the step of next filling the recesses on the integrated circuit wafer with these heterostructure nanopills. This will be done cascading the pills over the wafer surface and having them fall into the recesses as illustrated in Figure 4, using a process often referred to as fluidic self assembly [7]. The "fluidic" part of this name is appropriate because the nanopills are contained in a low viscosity non-polar fluid such as ethyl alcohol. The "self assembly" part is, however, somewhat misleading because it implies that the nanopills assemble themselves in the recesses automatically. In fact there is nothing automatic about the process and care has to be taken to make it highly probably that all of the recesses on a wafer will be filled with properly oriented and aligned nanopills. A term which better reflects this fact is "statistical assembly" and

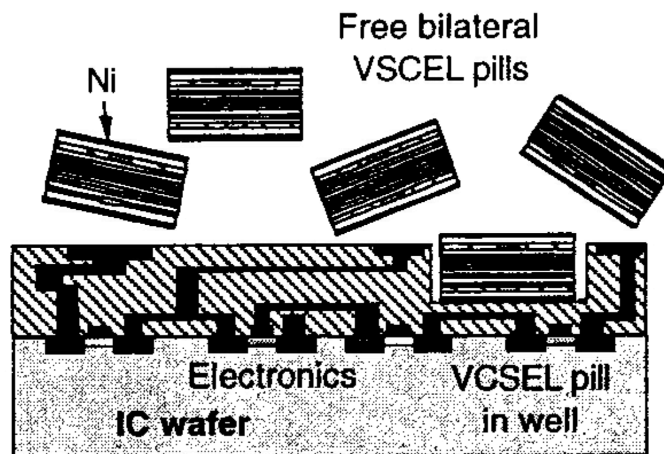

Figure 4 - The signature step in the MASA processing sequence showing pictorially how statistical assembly is used to fill the recess on an IC wafer with heterostructure nanopills.

in order to insure that all of the recesses will be properly filled the MASA process incorporates the following elements:

(1) There will be many more pills than recesses to insure that a each unfilled recess will have many pills that can fill it. After all the recesses on a given wafer are filled the excess pills can be collected and reused with subsequent wafers so there is no waste associated with this process.

(2) The pills will be highly symmetrical so it easy for the pills to enter the recesses and there is a high probability that a pill near a recess will fall into it. To increase this probability the pills will be cylindrically symmetrical and it is possible to also make them bilateral so they can enter a recess with either side up, but this may not be necessary (see next item).

(3) A magnetized pattern in the bottom of the recesses and a soft magnetic film on one side of the nanopills will make certain that once a pill enters a recess it is held in place there. Analysis shows that if the magnetized pattern is properly designed the attractive force experienced by a nanopill decreases exponentially with separation between the soft magnetic film and the magnetized pattern. Furthermore it is possible to tailor this attractive force so that the nanopill will not feel sufficient force to hold it in a recess

if it goes in upside down, and will only experience a significant attraction after it begins to enter the recess properly. If it is entering correctly the attraction increases rapidly as the separation decreases and the nanopill is effectively sucked into the recess. Magnetic attraction, if it can be realized in practice as theory indicates is possible, will make the use of bilateral nanopills unnecessary and will produce a very robust process. This is the primary feature of MASA which distinguishes it from other similar assembly techniques.

(4) The most basic MASA process will involve assembly of device heterostructures that are subsequently converted into devices through post-assembly processing, just as is done in EoE and APB. Because the active device area is defined photolithographically only after the nanopills are in position in their recesses, all alignment of the devices to each other and to the underlying circuitry is done by the mask patterns and can be done very precisely. It does not rely on the precision of the assembly process. In applications where this alignment is not a critical issue, it may be possible to assemble partially, or even fully, processed devices by the MASA technique, in which case the post-assembly processing might only involve opening contact vias, depositing and patterning the thin film interconnect metallization, and encapsulating and/or passivating the top surface of the completed circuit.

Development of the MASA process is the subject of an active research effort at MIT and forms the focus of two graduate students, Joseph Rumpler and James Perkins. To date proceedures have been developed to form and collect III-V nanopills with soft magnetic nickel films on one surface. The formation and patterning of hard magnetic films has been done in several ways, but this part of the process is still evolving.

The original concept for the hard magnetic structure was to use a pattern of stripes magnetized normal to the wafer surface. The easy magnetization direction for most patterned thin film materials, however, is in the long sample direction and this would be in the plane of the film along the stripe, which is not what is needed. To get significant remnant magnetization normal to the surface requires special materials processing. For example, a multi-layer stack of cobalt and platinum layer, each only a few nanometers thick, will have this property. An example of such a patterned layer structrure prepared for this research by Dr. Chong Tow Chong and his colleagues at the Data Storage Institute in Singapore is shown in Figure 6. While this is exactly the structure needed for the original concept, it is clearly impractically complex and requires unique capabilities making it unattractive for general RM^3 processing. These Co-Pt multi-layer films are also difficult to pattern, ion milling being the preferred technique.

An alternative hard magnetic structure that is more compatible with the realities of magnetic materials is a hard magnetic thin film of cobalt or iron patterned into squares and magnetized parallel to the wafer surface. Such a structure has recently been analyzed with the assistance of Professor Markus Zahn at MIT. It has been found that it too can provide the desired exponential decay of the attractive force and an attraction of sufficient strength at close proximity to hold the nanopills in place in the recesses. Such films, being much simpler than the multi-layers films that can be magnetized normal to the surface, can be e-beam deposited and patterned using lift-off techniques, both of which are more compatible with conventional integrated circuit processing and, equally importantly from a practical standpoint, with putting these structures at the bottom of recesses on an IC wafer surface. Work on these structures is continuing.

The next series of experiments that are in preparation are quantitative studies of the recess filling process with a series of nanopills and resesses of varying relative diameters. Studies of the magnetic attractive force itself are also planned.

Prior to leaving the discussion of the three RM^3 technologies it is important to make note of the fact that APB and MASA should not be viewed exclusively as alternative processes because in some circumstances they may in fact be used together. Specifically, MASA may be used to organize heterostructure or device nanopills on a carrier substrate which in turn would be used in an APB procedure to place and bond those nanopills in the recesses on an integrated circuit wafer. In this manner the patterned hard magnetic film, which as we have discussed can be quite complex and elaborate to produce, can be reused repeatably, rather than being used once and then being buried under the nanopills on the IC wafer.

It is perhaps only a modest overstatement to say that with the advent of MASA processing it will be possible to monolithically integrate anything on anything. With MASA all of the constraints in EoE and APB on the heterostructures and devices that can be integrated, and on the substrates on which they are placed, will be eliminated. There are clear challenges yet to be met (and undoubtably also unforeseen challenges that will arise) before MASA is fully developed and available for use in applications, but these challenges can be met and the advantages MASA offers gives urgency to doing so.

III. ONGOING APPLICATIONS RESEARCH

A. Optical Clock Distribution

One of the most significant factors limiting future microprocessor performance and one of the great consumers of microprocessor power is the clock distribution network. As clock rates continue to rise, the design of the clock distribution network will assume an increased importance. From the power point of view, the H-tree or other networks that distribute the global clock to functional subunits are continually growing and must be charged and discharged during each cycle. From the performance point of view, as die sizes and clock rates increase, clock skew becomes very significant.

Clock skew may be divided into two classes. The first may be called deterministic clock skew and refers to the difference in time required for the global clock to reach different units of the chip. It is relatively benign since it may be extracted from a chip layout and compensated for in the integrated circuit. The other form of clock skew may be called random and refers to the difference in arrival time of a clock

edge due to process variation (e.g. thickness of intermetal dielectric or width of metal line). Since this skew is process-dependent (and therefore also time- and location-dependent assuming an unchanging process), it is not possible to compensate for it at the design stage. Circuits must instead be designed conservatively to tolerate a certain degree of random skew, and this sort of design limits performance.

Optical clock distribution could address all of the above problems. Depending on the scheme in use, deterministic skew may be significantly reduced. A global optical clock would also decrease power consumption as large metal lines (designed for high current-carrying capacity) would no longer require charging at each clock cycle. Optical distribution would also avoid a good deal of random skew for the same reason. Random skew in this design would be contributed by process variations affecting the performance of the optical receivers of the global clock. Circuit techniques to perform compensation of this sort of variation are being investigated and developed by Professor Duane Boning and his group at MIT.

In this work, InP-InGaAs PiN diodes are used to provide a photocurrent. The heterostructures are being grown by Professor Yoon Soon Fatt at NTU. The performance of these diodes depends strongly on the thickness of the i-layer and the area of the devices. The former factor is very strictly controlled as the devices are grown by MBE. The latter factor is not a significant issue since device dimensions are significantly larger than the expected variation of the photolithography and etching processes. As shown in Figure 5, the diodes will be bonded to 0.18 μm Si-CMOS test chips

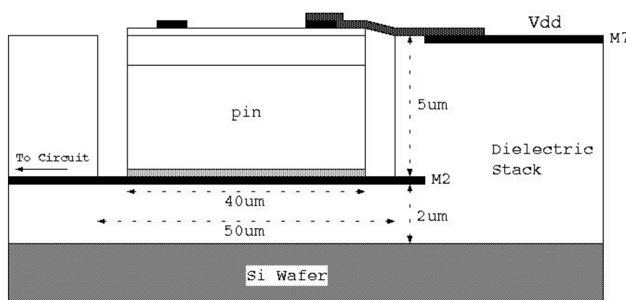

Figure 5 - Cross-sectional drawing illustrating a InP-InGaAs PiN photodiode ABP integrated on a CMOS integrated circuit chip for use in optical clock distribution studies. The heterostructures are much more complicated that shown in this figure, and involve 8 different epitaxial layers. They are grown in Professor Yoon's laboratory at NTU.

manufactured at Taiwan Semiconductor Manufacturing Company (designed by Prof. Boning and his group). Bonding will be done using the APB process onto the chip's Metal-2 layer. The bonding metallization is CMOS-compatible and will absorb the plastic stress of the thermal mismatch between the silicon target wafer and the III-V diodes. Following bonding, the diodes will be processed in place on the chip by the deposition of ohmic contacts, a mesa etch to control dark current, passivation dielectric material, and a metal line to join the diode ohmic contacts with Metal-7 V_{DD} lines.

Alternative clock distribution circuits have been proposed by Professor Mark Horowitz at Stanford University which require integrated detector/amplifier combinations with extremely low input node capacitances (under 10 fF). We find APB integration of two diode heterostructures, on n-side up and the other p-side up can uniquely meet this constraint. Consequently, we have begun a collaboration with Horowitz and Professors James Harris and David Miller, also at Stanford, to pursue this integration further.

B. *Diffuse Optical Tomography*

In August 2001 we began a three year collaborative research program with Professors Dana Brooks and Sheila Prasad of Northeastern University in Boston applying and using our technologies for monolithic optoelectronic integration to address problems and needs of biomedical research and diagnosis. Specifically we are working to monolithically integrate light sources and detectors with complex high density, high performance electronic circuitry to realize of a wide variety of sensors and measurement arrays for medical research and diagnostics.

We have identified as an initial vehicle for applying this technology a integrated source/detector array for diffuse optical tomography (DOT). The proposed unit will permit DOT observations with a resolution exceeding that of present techniques and will lead to the use of DOT in procedures and situations in which it is currently unfeasible.

Stated in the most general terms, this U.S. National Science Foundation supported effort is directed at developing, applying, and making available a technology to monolithically integrate III-V optical emitters and detectors with commercially fabricated, custom-designed integrated circuits to produce high resolution two-dimensional arrays of individually addressable smart excitor/sensor pixels tailored for biomedical research applications and studies. A representative pixel might measure 250 to 500 microns on a side, and contain, for example, a diode light emitter (LED or laser), one or more light sensors, and a significant amount of electronic signal processing circuitry. This basic unit is a building block from which a wide variety of biomedical optical measurement systems can be realized in a very rugged, compact chip-size format. It promises to lead, in the future, to totally new sensor geometries and measurement procedures.

The challenges that the program will face include continuing development of the OEIC technology and adapting this technology for biomedical research; developing suitable signal processing algorithms and designing compact, high performance signal processing circuit arrays in the relevant electronics technologies to interface with the optoelectronic devices; and suitably packaging the OEIC chips for their biomedical utilization.

The biomedical research and diagnosis area is one with many potential applications of RM^3 integration technologies, and this DOT probe is viewed as an initial entry vehicle to these applications, as well as an important end in itself. An example of further directions this work might take is given in Section IV-A below.

C. *Free-space Optics and Smart Pixel Arrays*

In September 2002 funding was received from the U.S. National Science Foundation for a collaborative program with Professor Cardinal Warde at MIT to apply APB to realize smart pixel arrays for free-space optical signal processing. The overall objective of the research program is to develop algorithms and architectures, and fabricate and demonstrate a rugged, compact, modular, versatile, optoelectronic integrated-

circuit (OEIC) neural network and fuzzy logic co-processor system that would work in conjunction with the standard PC microprocessor. This OEIC co-processor will perform sophisticated parallel and/or fuzzy processing operations more efficiently than the standard PC microprocessor. The key feature and advantage of this class of OEIC co-processors are that they combine the parallel processing and longitudinal (inter-plane) free-space communication strengths inherent in optics with the transverse (intra-plane) communication and computation strengths of electronics to realize extremely powerful and versatile machines.

To demonstrate the feasibility of the co-processor, the hardware development tasks include: (1) design, fabrication and characterization of novel 2-D arrays of GaAs-SOS (silicon-on sapphire) OEIC cascadable smart pixels with a detector, integrated-circuit logic and a light source in each pixel [resonant cavity light-emitting diodes (RCLEDs) in the first two years of the program, and vertical-cavity surface-emitting lasers (VCSELs) replacing the RCLEDs in the third year], (2) design, fabrication and characterization of novel reconfigurable optical interconnection elements based on arrays of Bragg-holographic phase gratings, (3) aligning (with the help of a mask aligner) and gluing all the components of the co-processor (OEICs, interconnection elements, and output photodetector array) together into a rugged, compact, modular multi-layer sandwich configuration so as to permanently solve any micro-optics alignment problems, and (4) characterizing the resulting high-speed, multilayer optoelectronic co-processor.

The final product at the end of the three-year program will be a rugged, compact, modular and versatile co-processor prototype that is a permanently-aligned, hermetically-sealed unit. Its reconfigurable interconnection architecture will permit the processing of electronic as well as optical signals. Such a co-processor will significantly enhance the state-of-the-art of machine vision systems, robotics, diagnoses from medical images, and contribute to the general understanding of the limitations of OEIC-based neural network processing.

IV. NEW CONCEPTS AND APPLICATIONS

A. Biomedical Fluorescent Imaging and Microscopy

The recent dramatic advances in GaN-based blue-green, blue, and near-UV light emitting diodes and diode lasers have had a tremendous impact in the area of displays and have led to the proliferation of large-scale video screens along major thoroughfares in cities around the world. Combined with RM^3 integration they promise to have an even more significant, though much less visible, impact on biomedical imaging and microscopy. The photons emitted by these new light emitting devices have sufficient energy to excite commonly used medical fluorescent dyes. This opens the way to extend the concepts being used with probes like the one for diffuse optical tomography described in Section III-B above, to integrate higher energy light emitters with complex Si electronics promises for numerous applications in biomedical imaging and microscopy. We expect to continue working with Professor Chua to explore such extensions of our RM^3 processes.

B. In-plane Laser Diodes and Planar Waveguides

The primary focus of laser diode research in the past ten years has been on vertical cavity surface emitting lasers (VCSELs), but as interest in chip-to-chip, and even on-chip, optical interconnect has grown dramatically in the past year, it has become clear to some researchers that in-plane lasers offer many advantages in this context. Their geometry and in-plane emission are better suited to this particular application, they can be modulated at much higher data rates than can VCSELs, and they can readily fabricated with multiple contacts along the active layer [8] to reduce drive requirements and further increase the modulation frequency. Furthermore one can easily envision adding another layer (or layers) of interconnect to a back-end process sequence, this time for planar optical waveguides. RM^3 integration will make it possible to easily align the active laser stripe vertically and laterally with these waveguides, as shown in Figure 6, forming a tightly and efficiently integrated unit. A program of research has been proposed to explore applying RM^3 technology to integrating multi-contact in-plane laser diodes for inter- and intra-chip optical communications.

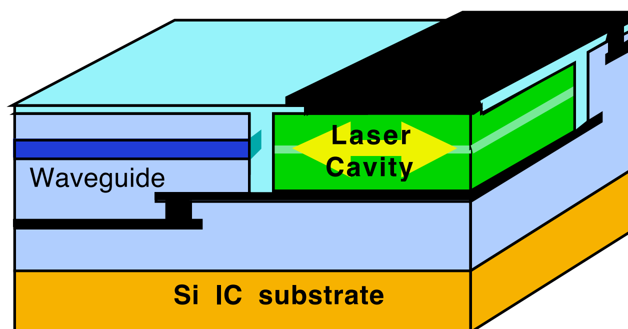

Figure 6 - Cross-sectional drawing illustrating an in-plane laser diode RM^3 integrated on a CMOS integrated circuit chip with its output aligned with a planar waveguide for use in on-chip optical interconnect. The laser stripe and facet are formed after bonding to insure precise lateral alignment with the waveguides; vertical alignment is insured by accurate control when the heterostructure is grown.

C. Mini-IC Integration

Speaking with semiconductor manufacturers one finds that an important area of concern, particularly with higher performance circuitry, is the increasing difficulty of driving signals off-chip with the voltage and power levels demanded by many of the devices to which they interface. It is often the case that signals can be processed on-chip very efficiently and extremely high data rates, but that the power consumed and the data rate penalty paid going off-chip severely limit the overall system performance. One way of dealing with this problem would be to integrate GaAs or InP input and output buffer or interface stages with the silicon and silicon-germanium integrated circuits. Consequently we have begun in collaboration with Vitesse Semiconductor Corporation to investigate the feasibility of extending RM^3 integration to bonding fully processed InP integrated circuit mini-chips

containing, for instance, an output buffer, on Si ICs. The same integration principles will be used, but applied now to large pills (no longer nanopills, but rather mini-chips) containing not individual devices, but full integrated sub-circuits.

V. Conclusion

In this paper we have seen that recess mounting with monolithic metallization, RM^3, techniques for mixed-material integration on silicon have been demonstrated in several variations, Epitaxy on Electronics (EoE) and Aligned Pillar Bonding (APB), and are already being used in research on a wide range of applications for complex optoelectronic integrated circuits in sensing, signal processing, and integrated circuit interconnects. Simultaneously, we have seen that development of Magnetically Assisted Statistical Assembly (MASA), the "ultimate" RM^3 technique, continues at a rapid pace. Just as the electronic industry is facing the increasingly difficult challenge of making devices smaller and smaller, and the cost of doing so becomes greater and greater, it is clear that the ability to add III-V semiconductor functionality to silicon integrated circuits will play a larger and larger role in generating new applications and markets for integrated circuits, and will be increasingly important to the electronics industry. RM^3 technologies promise to play a major role in providing this ability.

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