Control and Current Sensing Systems for the Parallel Resonant Pole Inverter Architecture

by

Henrik Martin

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Master of Science in Computer Science and Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

May 1994

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Abstract

This thesis explores two important issues in the development of the Parallel Resonant Pole Inverter (PRPI) architecture, namely the current sensing and control systems. A reliable, robust and yet inexpensive control system is designed and developed, and five different current sensing systems are designed, developed and compared. The thesis also presents the design of a Resonant Pole Inverter (RPI), and highlights many of the issues involved in designing such a system.

Thesis Supervisor: John G. Kassakian
Title: Professor

Acknowledgements

Five years at MIT is now coming to an end. They say your college years are supposed to be the best years in your life, and that has certainly been true for me.

The work related to my Master's Thesis has been incredibly rewarding. I would like to thank my thesis advisor, Professor John G. Kassakian, for providing the guidelines, facilities, and support for my work. I also greatly appreciate the funding provided by the Leader's for Manufacturing (LFM) Program. The best part of my experience as a graduate student, however, was to have the opportunity to work with Dave Perreault. Dave supervised my work, supported me during those long nights of debugging, taught me EE design, and became a great friend and companion. Dave: You are a truly exceptional person. Without your help, this thesis would never have been written, and for this I will forever be indebted to you.

Everybody else in LEES also deserves to be mentioned for making this a memorable experience. I am especially grateful to Vivian for helping out with all the administrative stuff: You're the best! Special thanks go to Tracy, Ahmed, Kamakshi, Joaquin, Niels, Mo, John, and Andres.

Without friends life would be unbearable. I would like to thank Mats, Lisa, and Matilda for being there. Petter and Mattias for being Swedish, guaranteed to be pals for life. MIT UNIHOC Club for all the work-outs. Nu Delta for being Nu Delta, the place where I learned to respect people for who they are. And of course, Mark, Marc, John, Andres, Brian, Paul, Soykan, Al, Andy, and all the other people I was fortunate enough to meet.

Finally, I must mention my family. Despite being away for five years, I feel closer than ever to them. Pappa, Mamma, Peter+Ulrika+Julius, Robert: TACK! I am *really* looking forward to seeing more of you in the future.

To my Christine, I dedicate this thesis. You are the best thing that ever happened to me, and I look forward to spending the rest of my life with you.

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Chapter 1

Introduction

The paralleling of low power inverter cells to form a high power converter system has substantial potential advantages over single cell designs. Some of these advantages, as outlined in [1], are:

1. Multiple inverters offer a possibility for redundancy, useful in applications where reliability is of importance.

2. For a given input voltage level and efficiency, smaller inverters, processing only a fraction of the full power, can usually be switched at a higher frequency than a large inverter processing full power. This results in a better waveform quality for the smaller units, leading to smaller filters required to filter the output signal.

3. The techniques of mass production and economies of high volume might reduce the cost per kW, possibly making the paralleling of inverter cells very attractive from an economic point of view.

4. In the case of an inverter cell failure, the cell can easily be replaced without interrupting the power supply, improving the mean time to repair the system and therefore its availability.

5. The heat dissipated in the system will not be localized in one place, but rather shared by several physically separate units. This may reduce the level of complexity and cost required for the cooling system.

The idea of parallel inverter cells has been successfully implemented in the realm where very high power is required, such as in large AC motor drives [2] [3]. Another realm where paralleled converter systems have excelled is where a high degree of reliability is needed, as is the case in uninterruptible power supply systems [4][5] [6]. However, in the realm where mass production manufacturing techniques and high frequency switching are available, the potential benefits of a paralleled converter system are yet to be realized. In order to capture the potential benefits of the parallel architecture, the design issues of converter topology and control techniques must first be appropriately addressed. It is the purpose of this thesis to examine current sensing and control in a parallel inverter architecture.

Most components in a paralleled system are equivalent to a redistribution of larger components in a single inverter system. In other words, an inductor in a single inverter system can, in a parallel converter system with N cells, be redistributed as N inductors where each one is N times the inductance of the single inverter inductor. There are, however, two important exceptions to this argument: the control system and the current sensing system do not scale with increasing modularity. For every additional cell that is attached to the parallel system, an additional control system as well as current sensing system are required. It is therefore important to design these subsystems in the most inexpensive and yet reliable fashion.

There are two purposes for this work. The first purpose is to design and test an accurate, robust and yet inexpensive control system. The second purpose is to develop and compare five different schemes for sensing current, resulting in a recommendation as to which system is most appropriate for this particular parallel architecture. In order to perform all the necessary experiments, single and parallel inverter systems are constructed.

Chapter 2

The Parallel Resonant Pole Inverter Architecture

2.1 Introduction

In recent years, much research in the area of switching power converters has focused on topological issues. One class of topologies which has gained increased attention is the soft switching inverter. Soft switched inverters are designed to reduce device switching losses by switching the devices only at zero voltage or zero current. This leads to a reduction in switching losses, allowing the devices to be operated at a much higher switching frequency. Resulting advantages over hard switched inverters include smaller component size, higher power density, higher efficiency, lower acoustic noise and low EMI.

2.2 The Resonant Pole Concept

The resonant pole inverter (RPI) is one member of the soft switching inverter family. Despite the advantages over hard switched converters, the RPI has not met with general approval due to drawbacks such as high rms current stresses on the filter capacitors and the difficulty of constructing resonant elements using off-the-shelf components at high power levels. The *parallel* resonant pole inverter (PRPI) architec-

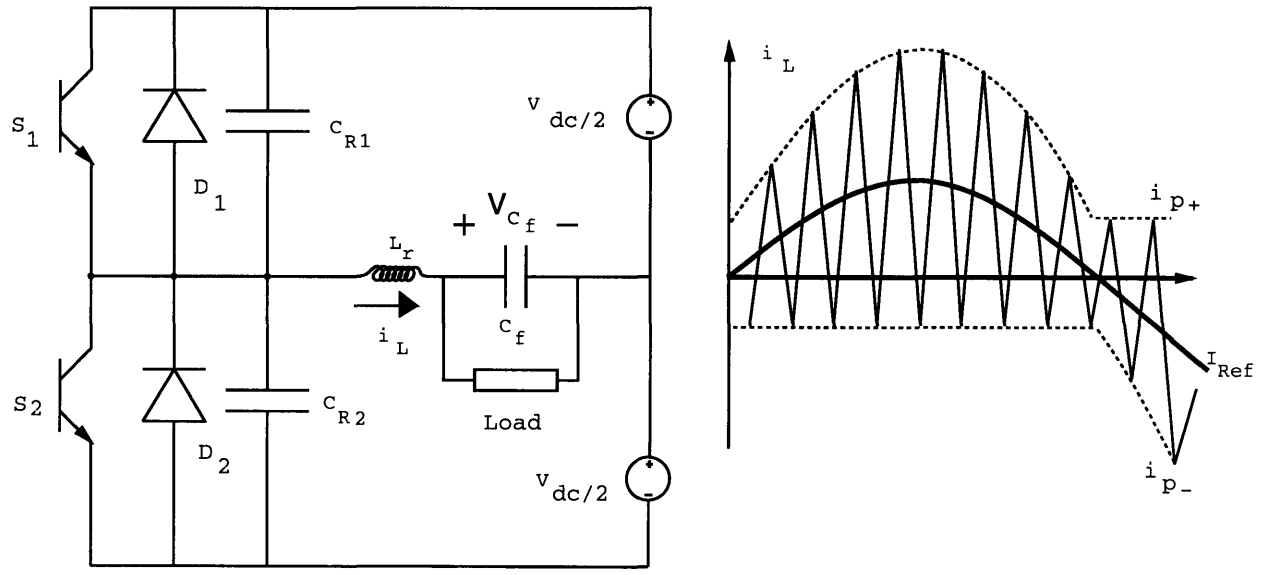


Figure 2-1: The resonant pole inverter and its switching waveform

ture, however, possesses all the positive characteristics of an RPI, while eliminating the two abovementioned limitations of the resonant pole topology.

The RPI is very well suited to the parallel architecture because of its simplicity, small component size, and ability to operate at elevated switching frequencies [7]. In addition to the power devices, it consists of a pair of resonant capacitors, C_{R1} and C_{R2}, and a resonant inductor, L_R as shown in Fig. 2-1. The switching waveform displayed in Fig. 2-1 shows that the control system is fundamentally hysteretic, with large hysteresis bands around the reference current. A complete description of the switching waveform and the control system is given in chapter 3.

An operational cycle of a single resonant pole inverter is shown in Fig. 2-2. A basic assumption underlying the following analysis is that the output filter capacitor is large enough to clamp the output voltage for the duration of the entire cycle. In the first picture, designated as mode 1 in Fig. 2-2(a), only the top switch (S1) is conducting. The resonant inductor current builds up linearly because the voltage across L_r is constant at $V_{dc}/2$. The current will continue to ramp up until it reaches a predetermined value i_{p+} set by the controller. At this point, S1 is turned off at zero voltage since the device voltage is clamped by the resonant capacitor C_{R1}, and

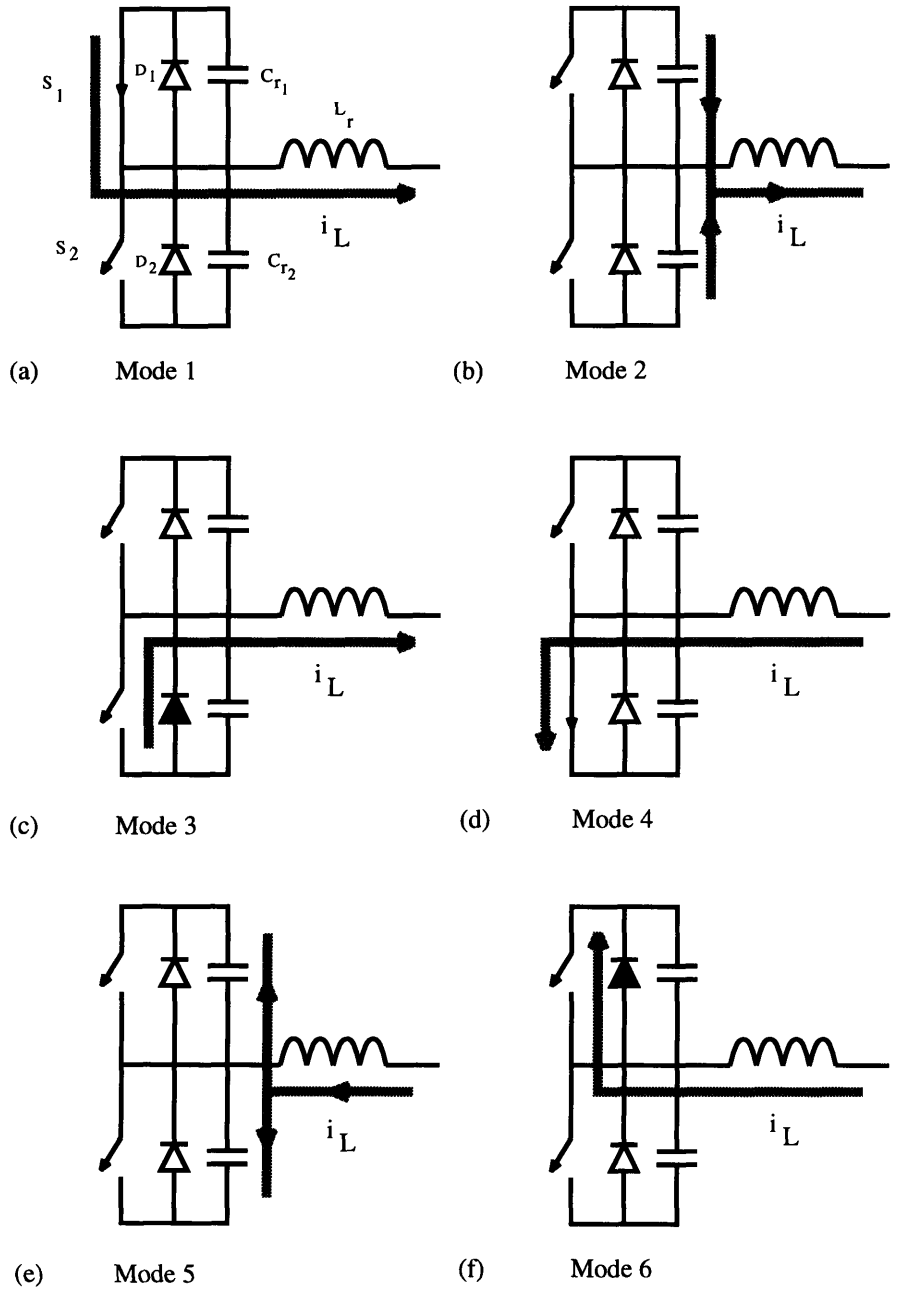


Figure 2-2: An operational cycle of the Resonant Pole Inverter

the circuit enters mode 2 in which the resonant inductor, L_r, rings with the two resonant capacitors, as shown in Fig. 2-2(b). This ringing will continue until D2, the bottom diode, starts conducting and operation enters mode 3, as shown in Fig. 2-2(c). During mode 3, the lower main device, S2, may be turned on at zero voltage, since the diode D2 is conducting. The current through the resonant inductor L_r decreases linearly and eventually reverses, causing S2 to carry the current. At this time the circuit enters mode 4, shown in Fig. 2-2(d). When i_L reaches a minimum value i_{p-} determined by the controller the bottom switch is turned off at zero voltage (the device voltage is clamped by the resonant capacitor C_{R2}), and the bus now rings up in mode 5, as shown in Fig. 2-2(e). The ringing continues until the upper diode, D1, starts conducting, at which time the operation enters mode 6. In this final mode, the top switch may be turned on, again at zero voltage, and circuit operation is back in mode 1. The cycle is then repeated.

The switching frequency of an RPI varies dynamically, as it does for a standard hysteresis-controlled PWM system. On the basis of the assumption that the resonant transitions are short and do not significantly affect the inductor current, the instantaneous switching period can be expressed as:

$$T = \frac{V_{dc} L_r (i_{p+} + i_{p-})}{0.25 V_{dc}^2 - V_{cf}^2} \tag{2.1}$$

The constraints on the values of i_{p+} and i_{p-} stem from the necessity of having enough energy stored in the inductor to ring the resonant capacitor voltages to zero in order to ensure zero-voltage switching. With ideal components, the minimum inductor current required at the end of mode 1 for a positive voltage V_{cf} can be expressed as:

$$i_{min} = 2\sqrt{\frac{C_r V_{dc} |V_{cf}|}{L_r}} \tag{2.2}$$

No current is required for the case when V_{cf} is smaller than or equal to zero. Similarly, at the end of mode 4, the magnitude of i_{p-} must exceed i_{min} for a negative V_{cf} if the bus is to ring appropriately, but may be zero in the case where V_{cf} is larger than or equal to zero.

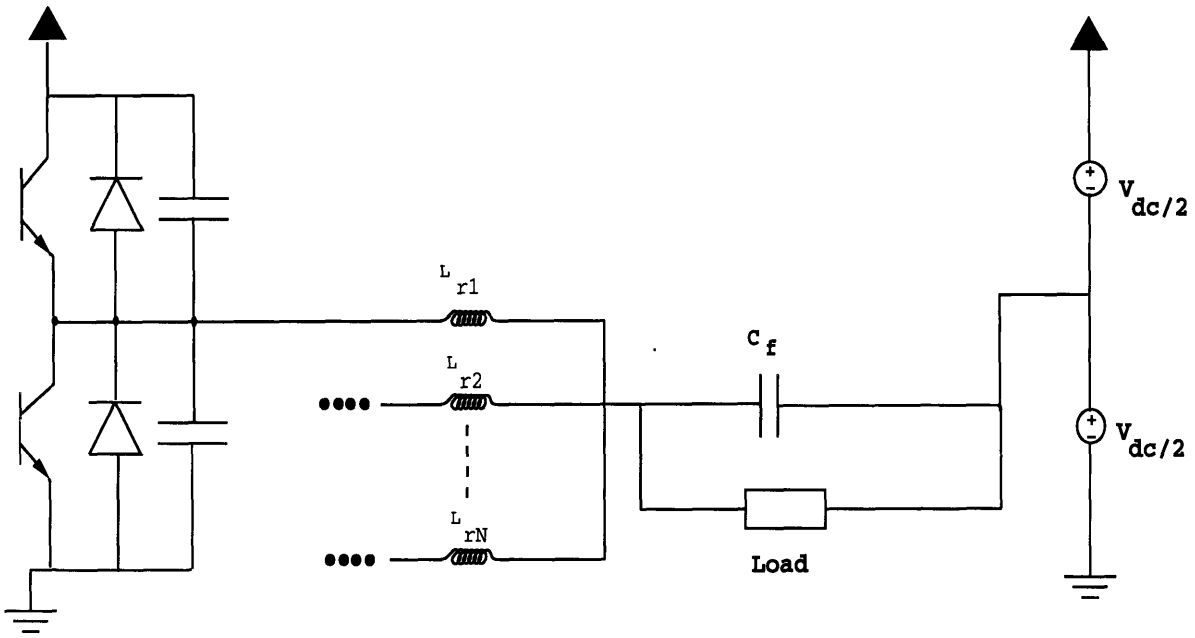


Figure 2-3: The parallel resonant pole inverter architecture.

2.3 The Paralleling of RPI's

The paralleling of multiple inverter cells raises several concerns. One is that a current sharing mechanism must be implemented in order to prevent individual converters from exceeding their power rating. An illustration of the parallel resonant pole inverter architecture is shown in Fig. 2-3. Current sharing is achieved through the use of a suitable control system combined with inductors at the cell outputs which absorb the instantaneous voltage difference between inverter cells. The inductors are added to the output of each individual inverter cell, as shown in Fig. 2-3. The output inductors make each inverter cell behave as a current source for times on the order of the switching period. The design of the output inductors is very important, since the inductors can make a significant contribution to a converter's overall cost and size.

The paralleling of RPI's has many advantages. As [8] shows, the PRPI results in minimum output magnetics, which, from the argument above, is very important. The PRPI requires only a simple control system, and can operate at higher frequencies than can a single large inverter due to the availability of high-performance devices,

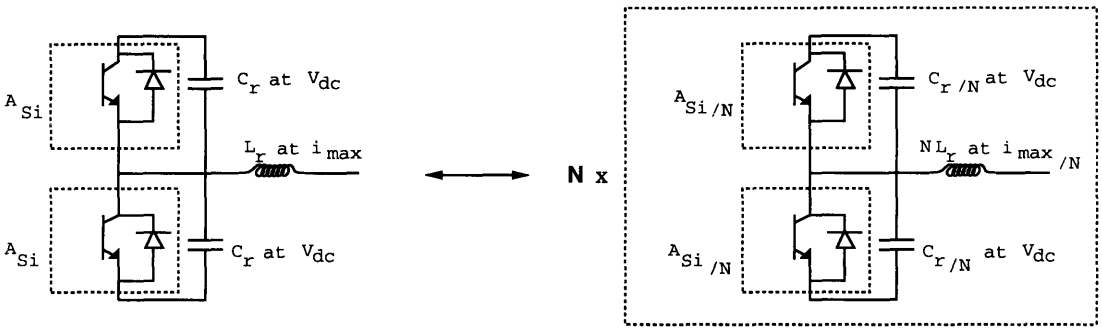


Figure 2-4: A resonant pole inverter leg and its equivalent parallel resonant pole components

distribution of heat generation, and the reduction of parasitics [7]. It also eliminates two major drawbacks of the single RPI. The practical size of an RPI is often limited by the difficulty of constructing output inductors with sufficiently large ratings using off-the-shelf components [9]. With a PRPI, however, this is no longer necessarily a limitation. To see this, consider Fig. 2-4. An N cell PRPI can be constructed which is functionally equivalent to a single RPI with N times the power rating. An equivalent PRPI has, to first order, the same device area, resonant component energy storage and losses as a single RPI, while each inverter cell operates at the same frequency as the original. By distributing the inductance, the inverter becomes much more manufacturable, and is not limited in size by the output inductors.

Another major drawback of the resonant pole inverter is the high current stresses on the output filter capacitors, as discussed in [10]. This drawback is again alleviated by the PRPI architecture. Basically, significant ripple cancellation occurs among the individual inverter cells, reducing the rms current stress significantly on the filter capacitors, compared to a single large inverter. This occurs even with independent open loop control of individual cells, as is shown in [8]. Current stresses on the output filter capacitors can be reduced even further using active ripple cancellation or an interdependent control system.

2.4 Conclusion

The PRPI architecture is a very promising addition to the area of inverter topologies. It retains all the advantages of the single RPI while eliminating many of the drawbacks. However, in order to make the PRPI economically feasible, careful analysis of its current sensing and control system is necessary.

Chapter 3

The Control System

3.1 The Control Strategy

The purpose of the control system is to regulate a converter system output current waveform, while ensuring that the individual cells share the load equally. This is done by means of a modified hysteresis control scheme applied to each cell individually and independently. Basic hysteresis control is conceptually very simple. It ensures that the controlled variable never exceeds a given upper or lower bound around a specified reference. This is illustrated in Fig. 3-1 for the case where the variable is the output current and the reference is some dc-value, I_{ref}. Assume that the operation starts with the top switch turned on. Whenever the output current reaches the top hysteresis band, the top switch is turned off and the bottom switch turned on. The current through the inductor will start to fall linearly since there is a constant voltage across it. Conversely, when the signal reaches the bottom hysteresis band, the top switch is turned on and the bottom switch is turned off. The current will then start rising again. The bands are generated by simple op-amp circuits, and the check to see if a signal is outside the hysteresis band is readily implemented by two comparators.

It was shown in [11] that the RPI can be controlled by a modulation strategy which is fundamentally hysteretic. The reference waveform (I_r) is in this case the desired sinusoidal output. Whenever the reference waveform I_r is positive, the top hysteresis band is set equal to $2I_r+I_{min}$, where I_{min} is the minimum current required to ring

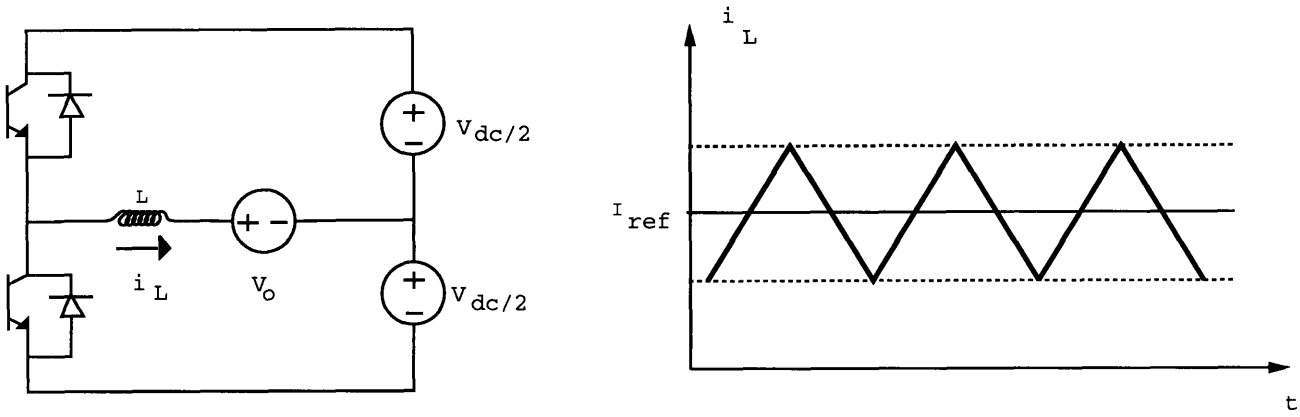


Figure 3-1: Illustration of basic hysteresis control.

I_r	High	Low
> 0	$2I_r+I_{min}$	$-I_{min}$
< 0	I_{min}	$2I_r-I_{min}$

Table 3.1: Summary of the High and Low hysteresis bands signals.

up to the rail as discussed in chapter 2. The bottom hysteresis band is simply $-I_{min}$ under these conditions. Whenever the reference is negative, the top hysteresis band is I_{min} while the bottom hysteresis band is $2I_r-I_{min}$. A summary of these conditions is shown in Table 3.1. An illustration of the hysteresis waveforms generated in this control scheme is shown in Fig. 3-2.

It is then the object of the control system to produce the correct hysteresis bands and, based on the information from the fedback current, send the appropriate signals to the gate drives of the inverters to implement this strategy. A block diagram of the control system is shown in Fig. 3-3

The design of the control system provides several challenges. Since the RPI is fully soft switched, it allows for elevated switching frequencies. The control system must therefore be very fast in order to be able to correctly control the individual inverter cells. The challenge is then to design a very fast and reliable control system while remaining within cost constraints.

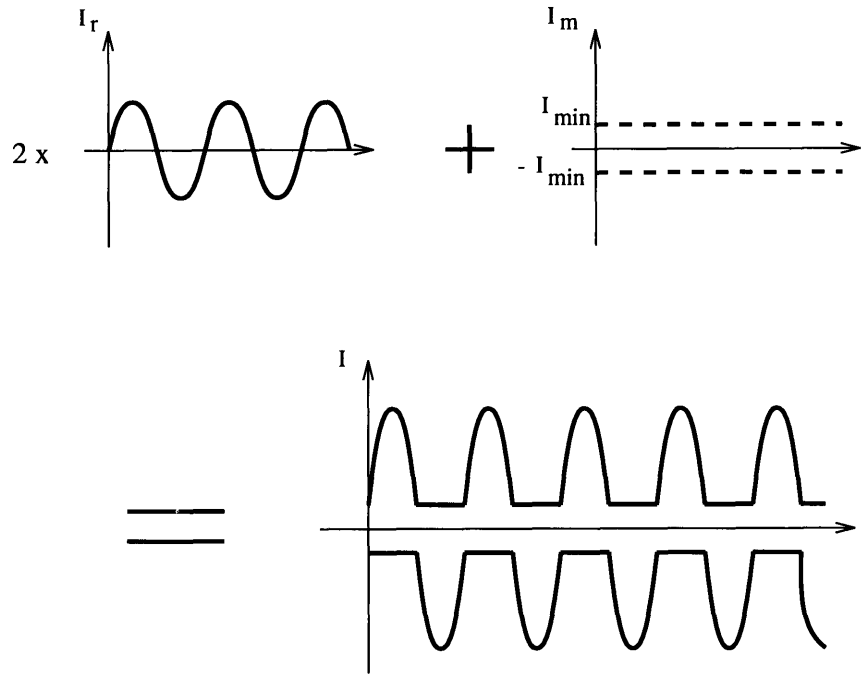


Figure 3-2: The RPI Modulation Strategy

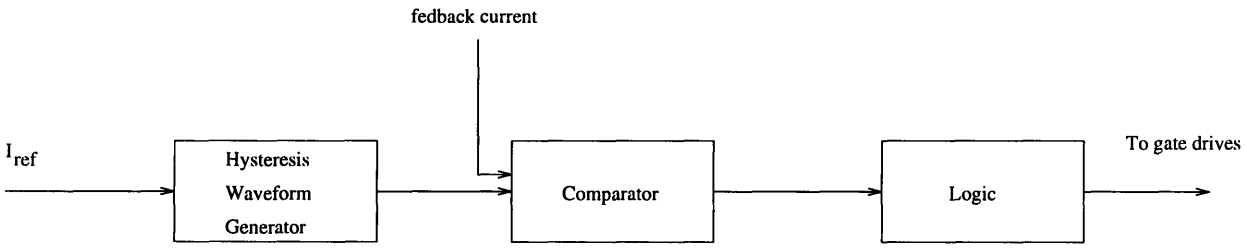


Figure 3-3: Block diagram of the control system

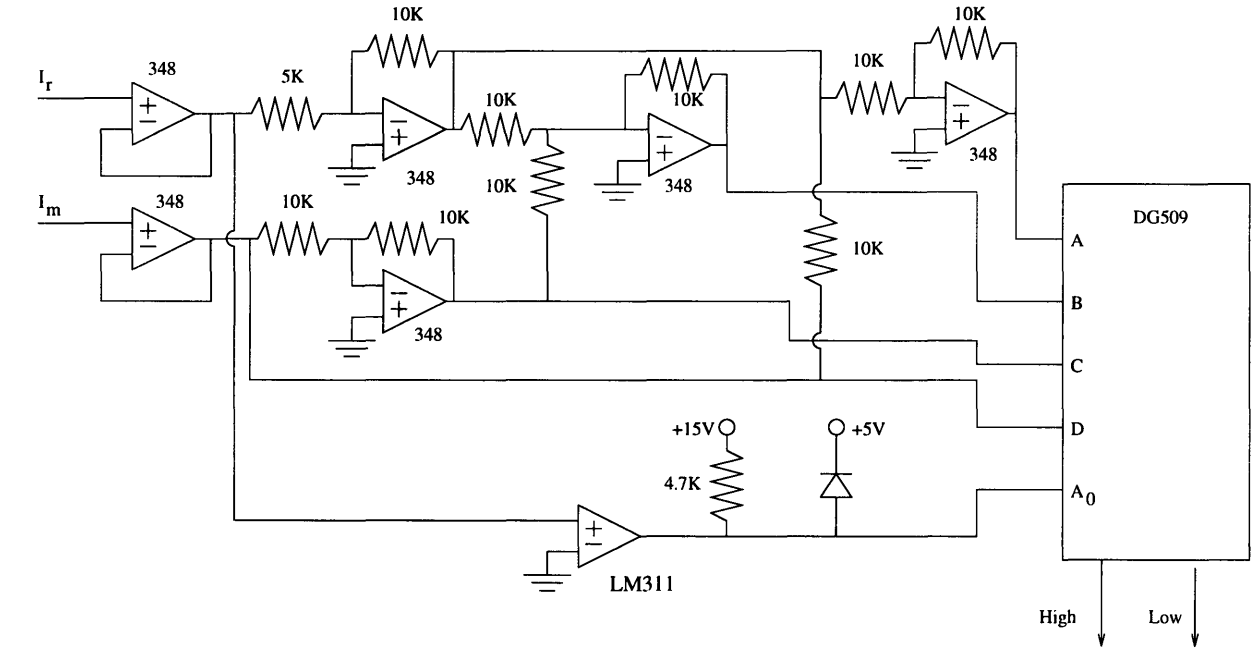
3.2 The Control System Design

The control system was developed over an extended period of time, and many different versions were experimented with. The final design is shown in Fig. 3-4. This design implements an inexpensive and yet fully functional control system that may be used at the elevated switching frequencies of the RPI.

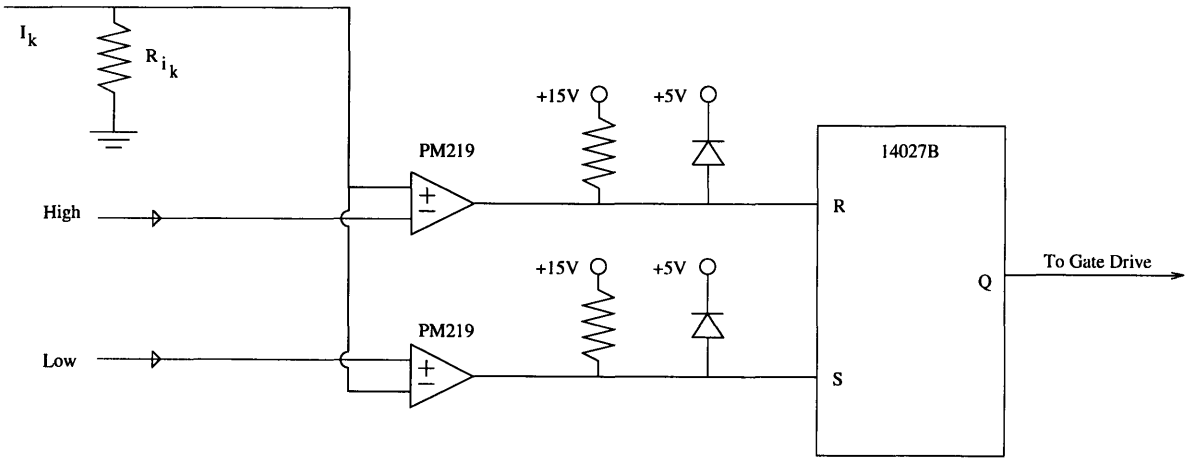
The top circuit of Fig. 3-4(a) generates the appropriate hysteresis bands. The inputs can be seen at the left hand side as I_r and I_m, and the outputs are shown at the bottom of the DG509 as High and Low. The main component used in this part of the control system is the LM348, a common op-amp. The 348's farthest to the left are simply input buffers while the other ones are performing the additions and subtractions required to obtain the desired hysteresis signals. Input A to the DG509 is then $2I_r$-I_m, input B is $2I_r$+I_m, input C is -I_m, and input D is +I_m.

The DG509 is a dual 4-channel analog multiplexer. It has 2 address inputs, A_0 and A_1, to control its dual 4 channels. Since the control system only needs to distinguish between two states, namely when I_r is positive or negative, only one address input is required, in this case A_0. In order to select the appropriate state for A_0, a comparator was introduced, the LM311. Whenever I_r is larger than zero, the output of the LM311 is high, and whenever I_r goes below zero, the LM311 output goes low. The conditions for the High and the Low hysteresis bands are summarized in the Table 3.1.

The components selected for the circuit in Fig. 3-4(a) are all inexpensive but also comparatively slow. This is, however, of little importance since this part of the control system only generates the required hysteresis bands, which are based on the relatively slow reference signal. The circuit in Fig. 3-4(b) deals with the fast switching waveforms (possibly over 100kHz), so it is of vital importance that the components in that part of the system are very fast. Fig. 3-4(b) shows that there are only two different IC's in this part of the control system: a comparator (PM219) and a flip-flop with set and reset (14027B). The PM219 is a very fast comparator with a response time of only 80ns and an input offset voltage of only 0.7mV. The flip-flop is not a particularly fast part: it has a set-to-Q response time of 150ns and a reset-to-Q



(a)



(b)

Figure 3-4: Schematic for the control system

response time of 350ns. The flip-flop was therefore replaced by its TTL functional equivalent, the LS279, in an updated version of the control system. The LS279 has a set-to-Q and a reset-to-Q response time on the order of 25ns. The experiments described in this chapter, however, are based on the system containing the 14027B.

There are three different inputs to the comparators: the current fedback from the inverter, I_k, and the High and Low signals. The fedback current is compared to the hysteresis bands, and if I_k is larger than High or smaller than Low the flip-flop changes its output state. It is worth noting the function of the resistor R_{Ik}: it scales the fedback current to an appropriate voltage level. It is evident that by changing the value of R_{Ik}, the magnitude of the inverter output current can be altered.

One drawback in using the fast PM219 comparator is that its maximum input voltage differential may not exceed 5V. Several attempted clamping schemes turned out to be unsuccessful, and it is therefore up to the designer to ensure that the input voltage differential limit is not exceeded for a specified value of R_{Ik}.

3.3 The Set-up for Testing the Control System

In order to be able to experiment with the control system, and to improve its characteristics, a complete converter system had to be assembled. The inverter cells used for this purpose had been designed by David Perreault and David Otten in LEES at MIT. A complete description of the inverter cells is included in appendix A.

Once the inverter cells had been constructed, some additional components also had to be designed and assembled. When connecting two or more inverter cells to each other, it is important to connect them through inductors, interphase transformers, or some other magnetic structure to provide buffering among the cell outputs. This buffering also enables control of current sharing among the cells. In this case, individual inductors were constructed using the method outlined in [12, pp. 575-77]. It was also decided to keep the power processed to a minimum for experimental reasons, and the bus voltage was set to a mere 25 V. The complete test set-up and its parameters are shown in Fig. 3-5.

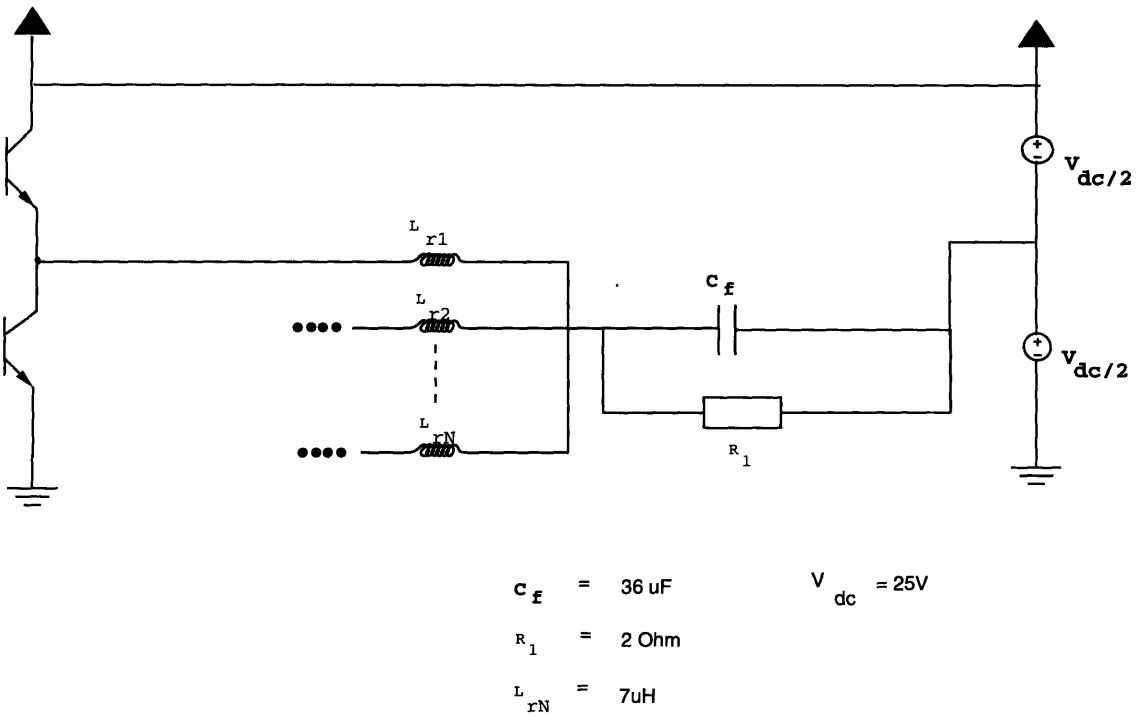


Figure 3-5: Test Set-up for developing the control system

3.4 Testing the Control System

Several tests were performed in order to demonstrate the functionality of the system. First, only the control system was turned on, without applying any power to the inverter bus. This was done in order to check that the control system generates the appropriate hysteresis bands. All the oscilloscope pictures shown below were captured by a black and white polaroid oscilloscope camera, and then scanned into a file by means of a HP Scan-Jet IIc. The file was imported into the graphics package XV, where it was inverted as well as digitally enhanced. Fig. 3-6 shows the two outputs High and Low of the DG509. Here, I_r is a 60Hz sinusoidal input, with a peak-to-peak voltage of 1.6V, and I_{min} is 0.8V. The input resistor in Fig. 3-4 has been set so that the demanded current will be of the same magnitude as four times the magnitude of I_r.

The voltage across the bus was then applied, and the system was allowed to run. In order to verify that the control system was switching the inverters at the appropriate

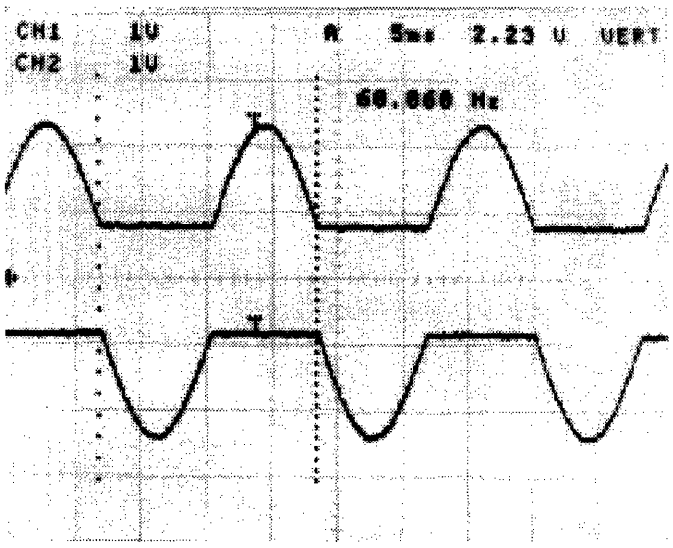


Figure 3-6: Picture of the High and Low signals output by the DG509

instances, and not letting the current signals exceed the desired hysteresis bands, another oscilloscope measurement was taken. A probe was attached to the High signal coming out of the DG509, and another probe was attached to measure the voltage across i_k, due to the fedback current. Fig. 3-7 displays the result. The solid waveform shows the High signal coming out of the DG509, while the switching waveform is the fedback current. Fig. 3-7 seems to suggest that the control system is not functioning properly. In particular, the fedback current does not seem to always reach the upper hysteresis band before it starts falling again. As it turns out, this is not an error in the control system, but rather due to the sampling limitation of the oscilloscope. One way to demonstrate this fact is to look at the switching waveform at a smaller time scale. This is shown in Fig. 3-8. Not only does Fig. 3-8 show that the control system is working properly. It also shows that there is very little overshoot over the desired hysteresis band.

Another way to verify the functionality of the control system is by looking at the output currents. Instead of looking at the current fed back by the Hall-effect sensor, a current probe was attached just before the load resistor (R_1 in Fig. 3-5). The current probe was set to measure 2A per division as seen on the oscilloscope.

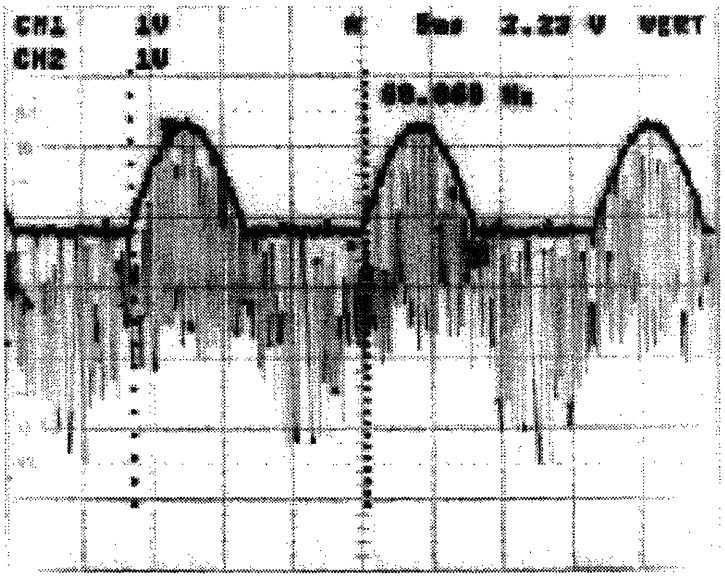


Figure 3-7: The solid waveform shows the High signal (the upper hysteresis limit) coming out of the DG509, while the switching waveform is the fedback current

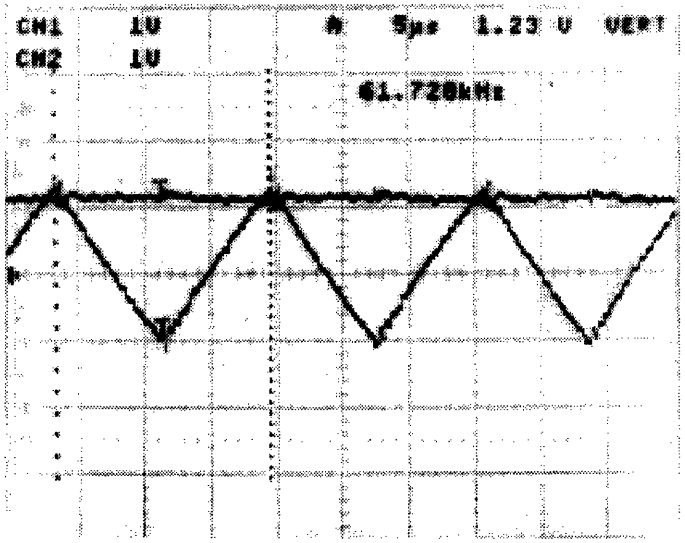


Figure 3-8: Demonstration that the current switches at the upper hysteresis boundary. The solid waveform shows the High signal coming out of the DG509, while the switching waveform is the fedback current.

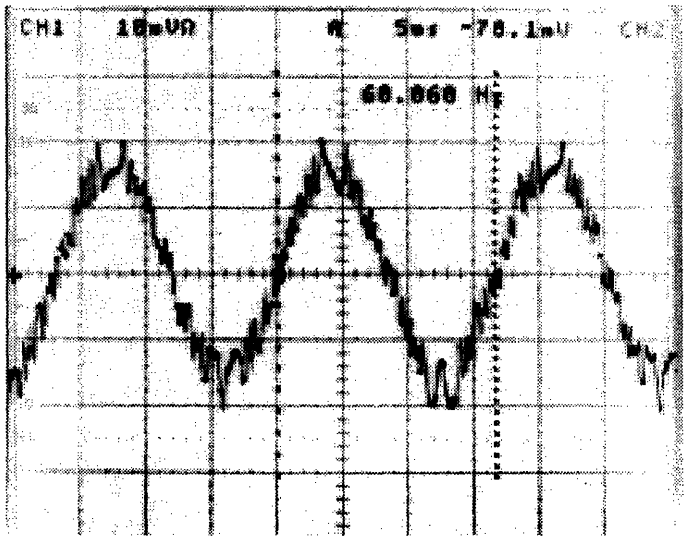


Figure 3-9: Output waveform as measured by a current probe attached just before the load resistor R_1 in Fig. 3-5. The scale is 2A/div.

Since only one inverter was run for this part of the experiment, the output waveform measured by the current probe was not expected to be very clean since no harmonic cancellation is present. A picture of the output current as seen on the oscilloscope is shown in Fig. 3-9. The picture suggests that the control system is producing the desired output waveform, even though there are plenty of harmonics. This is not surprising, however, since only one inverter is operating. The peak-to-peak current is about 6.4A, and the frequency is almost exactly 60Hz, which is precisely what was expected.

Three inverter cells were then connected in parallel. Each cell was controlled by its own independent control system. The three cells did, however, all have the same input reference waveform, I_r. Again, I_r was set to be a 60Hz sinusoid with a peak-to-peak voltage of 1.6V. The total expected peak-to-peak output current would then be 19.2A. The current probe was attached right after the joining node of the output inductors (see Fig. 3-5), and was set to measure 5A per division on the oscilloscope. The result of the current probe measurement is shown in Fig. 3-10. It is clear that the total output current is marginally smaller than the expected peak-to-peak value of 19.2A. Here, the effects of harmonic cancellation are apparent: The output inductor

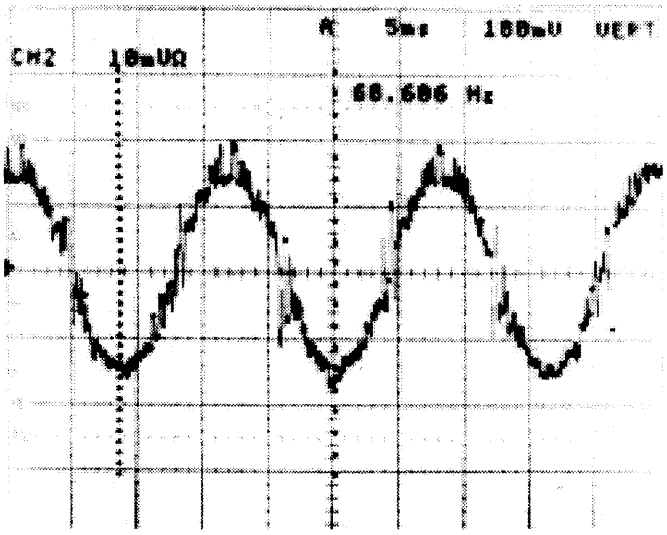


Figure 3-10: Three inverter cell output waveform as measured by a current probe attached right after the joining node of the output inductors in Fig. 3-5. The scale is 5A/div.

current from three inverters operating in parallel has very small ripple in comparison to the one inverter output, significantly reducing rms current ripple strain on the filter capacitor.

Finally, two more measurements were made to fully verify the system set-up. First, the current probe was attached to measure the current going into the filter capacitor, C_f. The result is shown in Fig. 3-11. From Fig. 3-11 it is clear that the maximum ripple is about 3A, and the average ripple is less than 1A.

The last measurement in these series of experiments was made by attaching the current probe to the input of the load resistor. Since most of the ripple components have been filtered out by the filter capacitor, it is expected that the current going into the load should very much resemble the desired output current waveform I_r. The result displayed in Fig. 3-12 shows that this indeed is the case. It is also interesting to note that the distortion on the waveform is significantly less than in the one inverter cell case (compare to Fig. 3-9). This is expected due to the harmonic cancellation that occurs in a parallel inverter cell structure.

The experiments performed, supported by the oscilloscope pictures, all support the

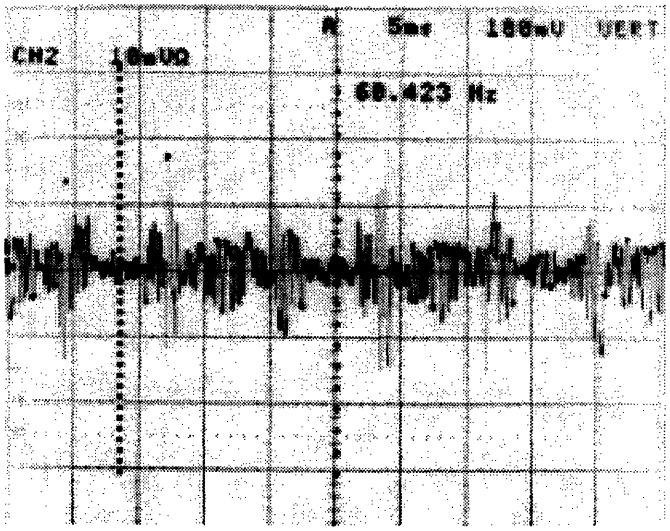


Figure 3-11: The current going into the filter capacitor for three inverter cells operating in parallel. The scale is set to 2A/div.

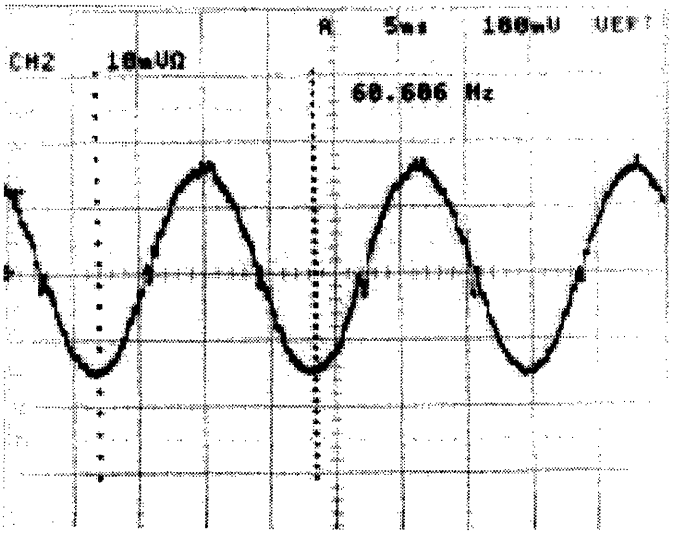


Figure 3-12: Output waveform as measured by a current probe attached just before the load resistor R_1. The scale is set to 5A/div.

fact that a functioning control system for a parallel resonant pole inverter architecture has been successfully constructed. The attention can now be turned to setting up a complete PRPI system, which is the topic of the next chapter.

Chapter 4

The RPI System

4.1 Introduction

This chapter describes the resonant pole inverter system. The system in its entirety includes the RPI itself, the control system, the output inductor, the load, and the power supply. The specifications for the RPI are summarized in Table 4.1.

4.2 The Power Supply

The 300V dc power supply was implemented by rectifying a three-phase 208V input. This was achieved by attaching a variac and a three-phase diode bridge to the input from the mains. Beyond the fundamental three-phase bridge, some additional safety features were incorporated into the design. A schematic of the power supply is shown in Fig. 4-1.

As can be seen in Fig. 4-1 the path between the mains and the variac is interrupted by a heavy duty vacuum breaker in order to allow the user to shut down the system at

Bus Voltage V_{bus}	300V
Peak Current I_{peak}	44A
Switching Frequency f_{sw}	20-80kHz

Table 4.1: Specifications for the RPI

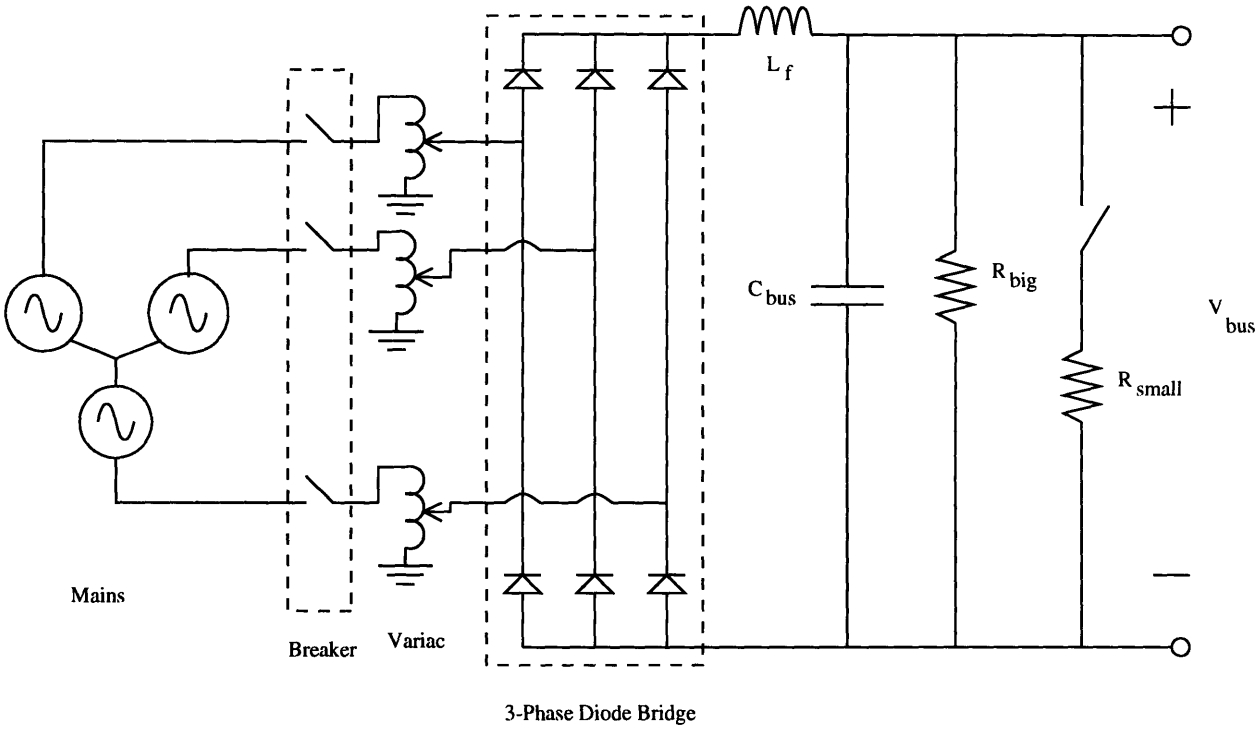


Figure 4-1: Schematic of power supply

any instant. The output of the breaker is connected to the input of the three-phase variac which scales the ac input voltage appropriately. The output of the variac is subsequently connected to the diode bridge. The three-phase diode bridge was purchased as a package (Powerex ME501206) and is mounted on an appropriately sized heatsink.

4.2.1 Sizing the Capacitor

The role of the bus capacitor, C_{bus} in Fig. 4-1, is to hold the output voltage steady at 300V. It needs to be large enough such that the bus voltage does not fluctuate significantly when the inverter is processing full current.

The capacitor is charged through the six-pulse rectifier. An illustration of how the capacitor voltage varies over time is shown in Fig. 4-2. In order to simplify the analysis, it is assumed that the capacitor is recharged to its full voltage by six impulses during each cycle. It is possible to solve for the capacitor value needed to

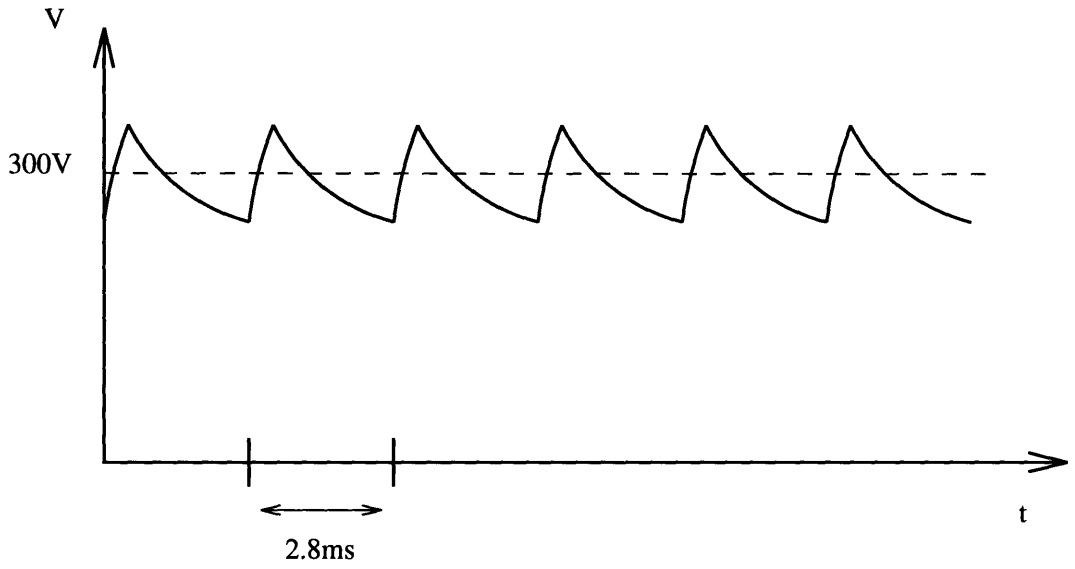


Figure 4-2: Illustration of the variations in bus capacitor voltage over time

limit the ripple to a desired value by applying the following equation:

$$C = \frac{I\Delta t}{\Delta V} \tag{4.1}$$

Here, C is the bus capacitor value, Δt is the time between two pulses from the rectifier, ΔV is the maximum voltage deviation allowed from the desired 300V in the bus voltage, and I is the average current drawn by the inverter. Since I_{rms} of the inverter is specified to be 15A, the maximum current the inverter would ever draw would be approximately 20A. If the bus voltage is allowed to fluctuate by 10% around the 300V specified, the calculated bus capacitor value comes out to be approximately 1000μF. The value of the bus capacitor in the actual system was chosen to be 1600μF, simply because that particular value capacitor happened to be available.

It is worth noting that by increasing the capacitance of the bus capacitor, the voltage bus will deviate less from the desired 300V. The disadvantages in making the bus capacitor too large, however, are that it increases the stresses on the three-phase diode bridge, and it makes it more difficult to discharge the capacitor when the system is shut down.

4.2.2 Sizing the Resistors

The resistors are added for safety reasons only. They are included in the design so that the energy stored in the capacitor can be dissipated safely. The resistor R_{small} is the fastest means for dissipating the energy stored in the capacitor. By throwing the switch to connect the small resistor in parallel with the capacitor, the capacitor will discharge very quickly through R_{small}. The discharge time was set to be less than one second. This means that five times the RC time constant, τ, must be less than one second. In order to satisfy this condition, a resistor value of less than 125Ω is required. A suitable power resistor with a resistance of 91Ω was available. It is important to realize that this resistor must have a instantaneous current carrying capacity of V_{max} / R_{small}=300/91=3.3A.

The resistor R_{big} is needed to ensure that if the user turns off the variac but forgets to discharge the energy stored in the capacitor manually through R_{small}, the capacitor energy will eventually discharge through R_{big}, but over a longer time span. The upper constraint on the resistance of R_{big} is determined by the maximum allowable time to fully discharge the bus capacitor. The lower limit is set by on-state power dissipation limits, since R_{big} dissipates power while the system is running. It was decided that no more than 1W should be dissipated in R_{big}. Then, from the equation,

$$P_{diss} = \frac{V^2}{R} \tag{4.2}$$

where V=V_{bus} and R=R_{big}, it is clear that R_{big} must be larger than 90kΩ. Picking R_{big} to be 100kΩ results in a discharge time of $5R_{big}C_{bus}$ = 13 minutes.

4.2.3 Sizing the Heatsink

As was mentioned above, the three-phase diode bridge was bolted to a heatsink. The reason for this is that the losses in the bridge appear as heat, which then must be removed from the system. The design of the heatsink is based on conservative estimates as well as on information provided by the manufacturer.

Based on the thermal modeling procedures suggested in [12], a model for the

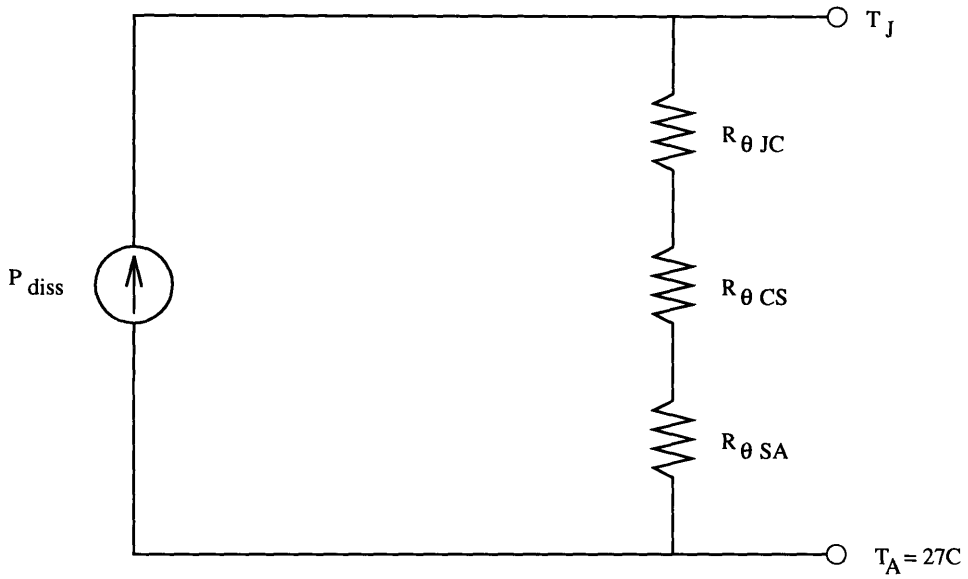


Figure 4-3: The thermal system used for modeling the rectifier device, the device casing, and the heat sink.

I_{dcmax}=60A	$R_{\theta JC}$=0.3°C/W	$R_{\theta CS}$=0.06°C/W	V_{ON}=1.3V

Table 4.2: Information about the rectifier available from the manufacturer

device, the device casing, and the heatsink as shown in Fig. 4-3 was used. Here, T_A represents the ambient temperature and T_J represents the junction temperature. The three resistors model the thermal resistance between the junction and the case ($R_{\theta JC}$), between the case and the heatsink ($R_{\theta CS}$), and the heatsink and the ambient temperature ($R_{\theta SA}$). The information available from the manufacturer concerning the three-phase diode bridge is summarized in table 4.2.3.

The information about the heatsink specifies that the thermal resistance between the heatsink and the ambient is 0.35°C/W. The only thing missing from the model is then the value for P_{diss}, which is found by using the fact that two bridge diodes will be conducting at any given time. From this:

$$P_{diss} = 2 * 60A * 1.3V = 156W \tag{4.3}$$

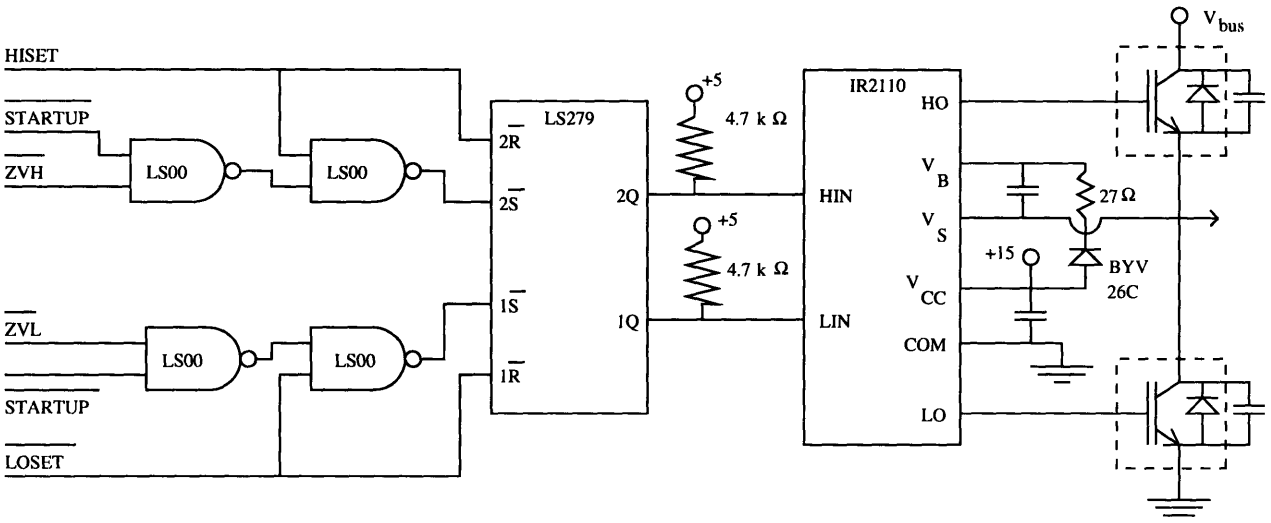


Figure 4-4: Schematic of the RPI inverter

Assuming that the heatsink is sized to 6" results in a maximum junction temperature of:

$$\begin{aligned} T_J &= T_A + P_{diss} * (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \\ T_J &= 27 + 156 * (0.3 + 0.06 + 0.35) \\ T_J &= 138°C \end{aligned} \tag{4.4}$$

The three-phase rectifier device is rated to operate at 150°C, so this is clearly a sufficient heatsink. While the inverter system will never process 60A, the heat sink has been overrated to match the limits of the rectifier devices for future applications.

4.3 The Inverter

The inverter was designed in conjunction with David Perreault at LEES, MIT. A schematic of the RPI is shown in Fig. 4-4. The power devices used in the RPI are IXYS IXGH24N60AU1 IGBT's with internal diodes. In parallel with each IGBT is the CD30FD103J03 silvered mica resonant capacitor from Cornell Dubilier. The gate signals for the IGBT's are provided by an IR2110 high voltage mos gate drive. The low side channel (LO) is referenced to ground and the high side (HO) is referenced

to a floating rail V_S. The charging of the top capacitor is achieved by means of a bootstrap technique, implemented by a resistor and a fast recovery diode BYV26C. The conditions determining which switch is turned on are set by the control system, the zero voltage detection system, and a startup signal. The startup signal is a simple RC-network shorted by a switch. The startup signal starts at +5V, and the IR2110 will not receive HIN/LIN unless the startup signal goes low (achieved by throwing the switch). The HISET signal is provided by the output of the control system. LOSET is simply HISET inverted. Finally, the zero voltage detection signals for the low and high side are provided by the zero voltage detection scheme outlined below.

During normal operation the startup signal will remain off. Assuming that the bottom device is conducting, the output current will be decreasing. When the output current reaches the level set by the control system, the control system will tell the RPI to turn off the bottom switch and turn on the top switch by setting LOSET low and HISET high. The RPI will turn off the bottom switch, but the top switch will remain off. The bridge output node will then ring from zero to V_{bus}. When the top device voltage reaches zero, the zero voltage signal for the high side will go low, and the top switch will turn on. The same logic is used for top to bottom transitions.

4.3.1 Zero Voltage Detection

The zero voltage detection system detects whenever there is zero voltage across a device. This information is required by the RPI in order to ensure zero voltage turn-on/off. It is also used to detect zero current in some of the current sensing schemes described in chapter 5.

The zero voltage detection schematic for the high side device is shown in Fig. 4-5. It is implemented using a MAX913 comparator and a HCPL2611 opto-coupler. The MAX913 and the input side of the opto-coupler are referenced with respect to the V_s pin on the IR2110, while the output side of the opto-coupler is referenced to ground.

The positive input to the MAX913 is kept constant at 2.5V. Whenever the power diode is conducting, the negative input to the MAX913 goes low, and the output (Q) of the MAX913 goes high. The negative input could potentially go below zero, which

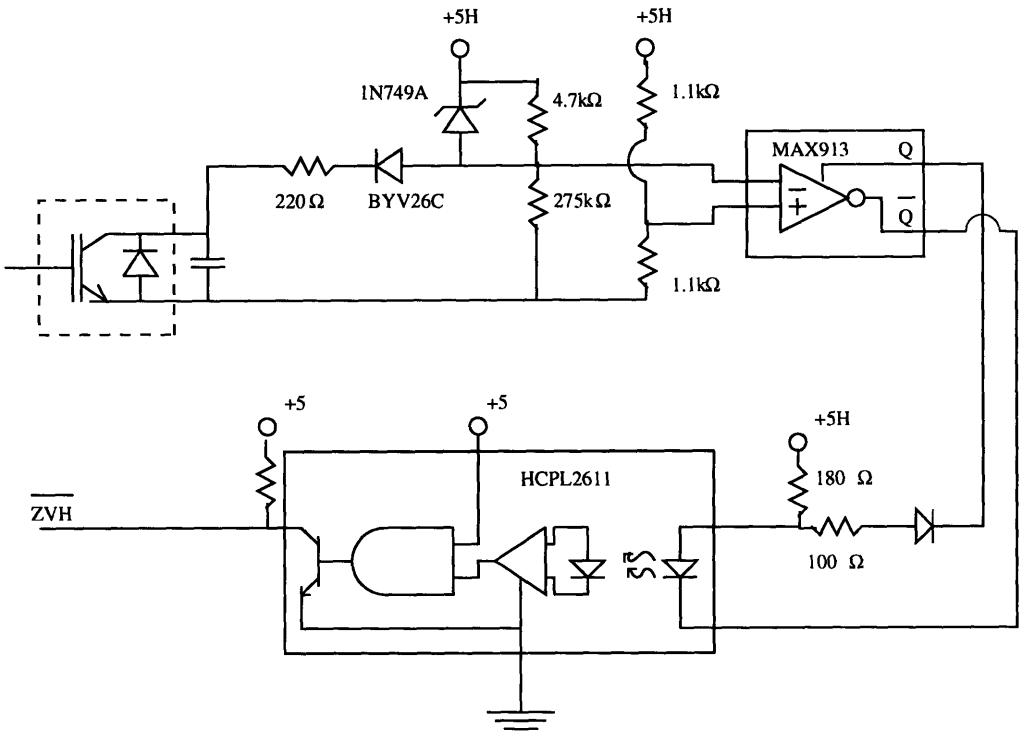


Figure 4-5: Schematic of the zero voltage detection system.

is outside the operating region of the MAX913. The zener diode 1N749A prevents this from happening by clamping the negative input at 0.7V. When the IGBT is conducting, the negative input will go to at least 3.4V (2.6V from the IGBT, and 0.8V from the BYV26C). This will make the MAX913 output (Q) go high. The HCPL2611 provides the required isolation, and also inverts the signal. Subsequently, the zero voltage sensing system's output will be low whenever the power diode is conducting, and will otherwise remain high.

The low side zero voltage detection scheme does not require the opto-coupler, but in order to simplify debugging, it was constructed in the same manner as the high side system.

4.4 The Load

The RPI was assembled in its entirety as shown in Fig. 2-1. A 30μH output inductor was constructed by winding 21 turns on the Arnold Engineering core A-123068-2. The load was a 2Ω power resistor, in parallel with a 36μF filter capacitor.

4.5 Testing the RPI

The RPI was successfully tested at low power levels. However, since neither the control system nor the current sensing systems require an RPI during the design and evaluation process, the RPI was not used to test either the control system or the current sensing schemes.

Chapter 5

Current Sensing

5.1 Introduction

There are many different methods available to sense currents. Based on the current levels to be sensed in the system, and the cost and performance constraints, five different current sensing schemes have been selected as promising for this particular application. Sensing current by resistive methods, by current transformer, by Rogowski coil, by Hall-effect, and via a secondary winding on the output inductor are considered. These schemes are evaluated with respect to three fundamental characteristics: Their accuracy, their bandwidth and their total cost.

5.2 The Hall Effect Sensor

5.2.1 Introduction

Out of the five different schemes that are being evaluated here, the Hall effect sensor is the most commercially available. It is also very accurate: The LEM50-A from LEM USA measures currents of up to 70A with an accuracy of 0.5% of full scale and can follow waveforms up to 100A/μs. Furthermore, it is also simple, non-intrusive, small, requires no additional circuitry and has a high bandwidth (0-150kHz). Unfortunately, it is also very expensive. Therefore, the Hall-effect sensor will be used primarily as a

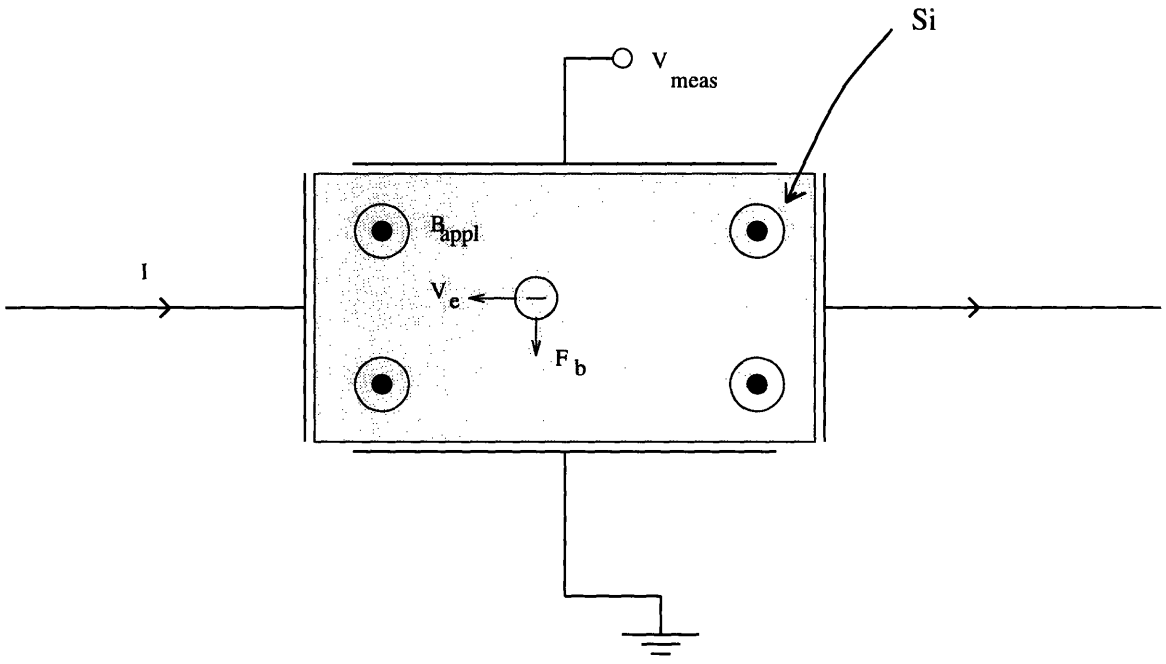


Figure 5-1: The Hall effect sensor.

reference, and its performance will serve as a benchmark for the other current sensing schemes.

The Hall-effect sensor is built around a phenomena discovered by Edwin H. Hall in 1879. He showed that it is possible to deflect conduction electrons traveling in a conductor by means of a magnetic field. Consider a strip of silicon with a known level of doping. If a current is sent through the silicon while applying a magnetic field B_{appl} transverse to the direction V_e the electrons are traveling, the electrons will experience a deflecting force inside the conductor, as illustrated in Fig. 5-1. The magnetic deflection force, denoted as F_b in Fig. 5-1, pushes the electrons to the bottom of the strip, leaving uncompensated positive charges on the top edge. Therefore, a constant electric field will build up at all points inside the silicon strip, which acts on the electrons in the opposite direction from the magnetic force. An equilibrium will eventually develop where the magnetic force is exactly offset by the electric force, and the charge carriers will no longer be deflected. At this equilibrium, there will be a constant potential between the top and bottom of the silicon strip,

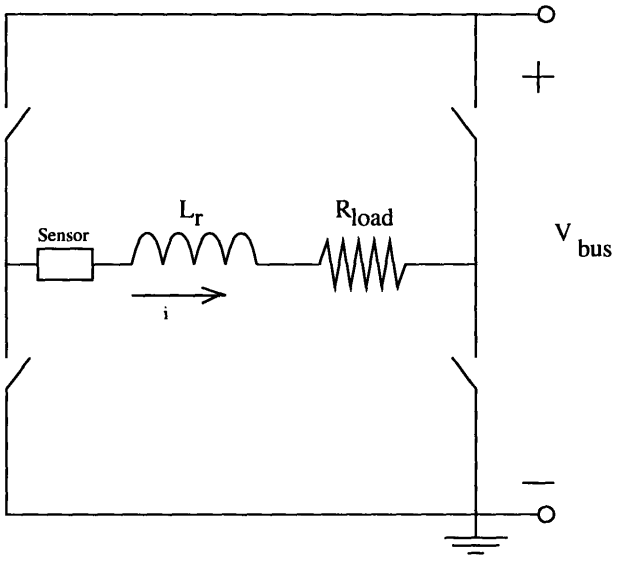


Figure 5-2: The setup for testing the current sensing systems.

called the Hall potential difference. This potential can be used to deduce the current going through the silicon strip as the current and the Hall potential difference are related through the following equation:

$$I = \frac{V_{Hall} te}{B_{appl}} \tag{5.1}$$

Here, V_{Hall} denotes the Hall potential difference, t is the thickness of the strip, and e is the charge of an electron [13]. The equilibrium is established very rapidly, which makes this method very suitable for current measurements at elevated frequencies.

5.2.2 Testing the Hall-Effect Sensor

The five different current sensing methods were all tested under similar conditions. The test setup consisted of two inverter legs connected in an H-bridge as shown in Fig. 5-2. The specifications for the inverter cells are outlined in Appendix A. The control system was set up to generate dc-level hysteresis bands at $3I_m$ and -I_m by simply connecting I_r to the I_m pin. This results in an output current waveform whose frequency and magnitude can be altered by changing I_m (implemented by means of

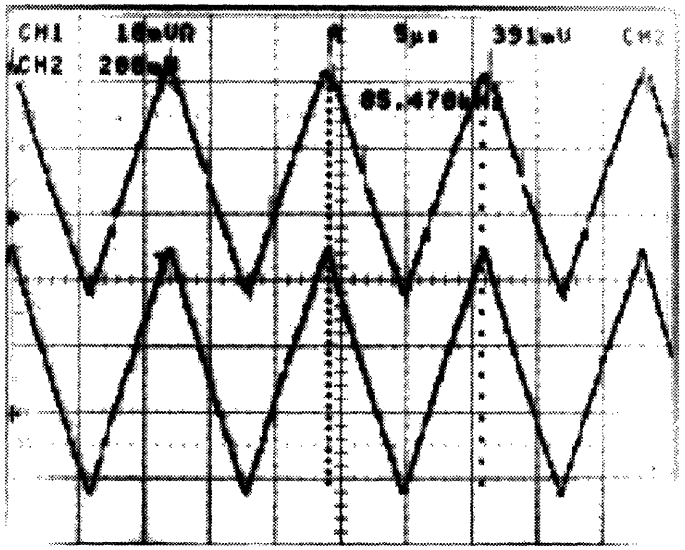


Figure 5-3: Output waveform for Hall-effect sensor (top waveform) as compared to a current probe measurement (bottom waveform). The setting is 2A/div, and the switching frequency 85.5kHz.

a 1KΩ pot between +5V and ground). It also has the advantage that the magnitude and frequency stays fixed, unlike the RPI output waveform.

The Hall-effect sensor was tested at high and low current levels, as well as at high and low frequencies. First, the general output waveform of the Hall-effect sensor was examined. The switching frequency was set to about 85kHz in order to test high frequency behavior. The resulting oscilloscope picture is shown in Fig. 5-3. It is clear that the Hall-effect sensor measures current accurately even at the elevated frequency of 85kHz. In order to measure just how accurate the Hall-effect sensor is, two more measurements were made: One at low current levels, and one at high current levels. Figure 5-4 shows a measurement made at 1A/div and 60kHz. There are actually two traces superimposed which is evident if one examines the tip of the switching waveform: The waveform put out by the Hall-effect sensor contains some switching noise at the peak, while the current probe measurement is clean. Figure 5-4 shows that the Hall-effect sensor provides a very accurate current measurement at this current level and switching frequency. In fact, it is so accurate that any errors are difficult to discern. However, an error of approximately 0.5% can be seen in the

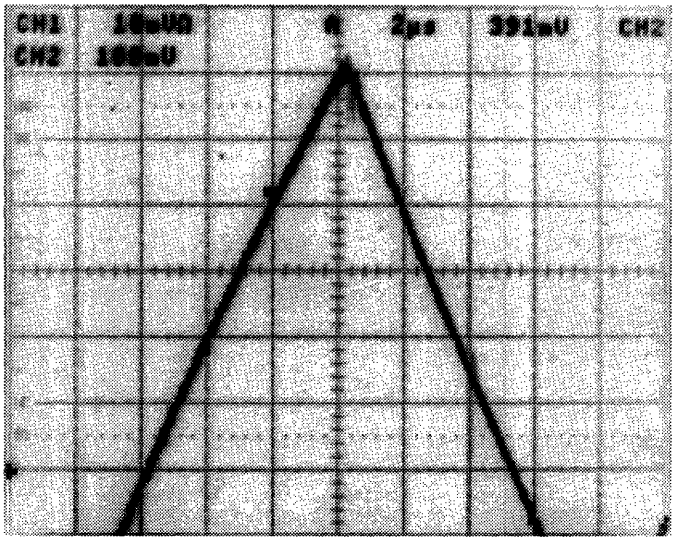


Figure 5-4: Output waveform for Hall-effect sensor (contains some switching noise) as compared to a current probe measurement (clean) at a high switching frequency. The setting is 1A/div and the switching frequency is 60kHz.

last measurement. The same turned out to be true for high current levels (and low switching frequency). Figure 5-5 shows the same measurement as in Fig. 5-4 except that now the switching frequency is only 13.3 kHz, and the oscilloscope is set to display 5A/div. The peak current can be seen to be about 30A.

5.2.3 Conclusion

On the basis of the measurements presented above, it is clear that the Hall-effect sensor possesses the required bandwidth and accuracy required for the control of an RPI. It is also small, and requires no additional components. The only disadvantage is the cost. The Hall-effect sensors used in these experiments cost about $34 each ($25 if bought in bulk), which is too expensive if the PRPI system is to become economically feasible. A summary of the findings for the Hall-effect sensor is shown in Table 5.1. The worst case error is the specified error from the manufacturer added to the 1% error from the resistor value. The measured error is the maximum approximate error found during the experiments documented above. The cost and the bandwidth were specified by the manufacturer.

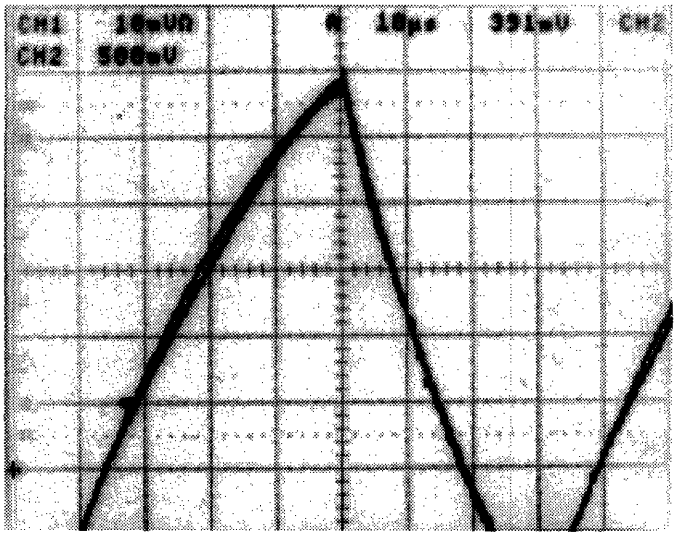


Figure 5-5: Output waveform for Hall-effect sensor (lower trace) as compared to a current probe measurement (upper trace) at a low switching frequency. The setting is 5A/div and the switching frequency is 13.3kHz.

Worst Case Error:	1.5%
Measured Error:	0.5%
Bandwidth:	0-150kHz
Cost:	High

Table 5.1: Summary of the findings for the Hall-effect sensor.

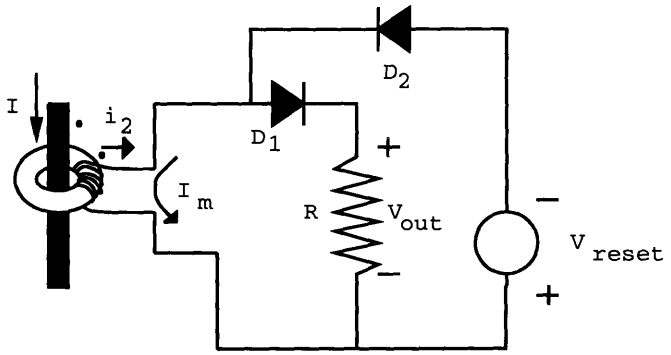


Figure 5-6: The current transformer and its reset mechanism.

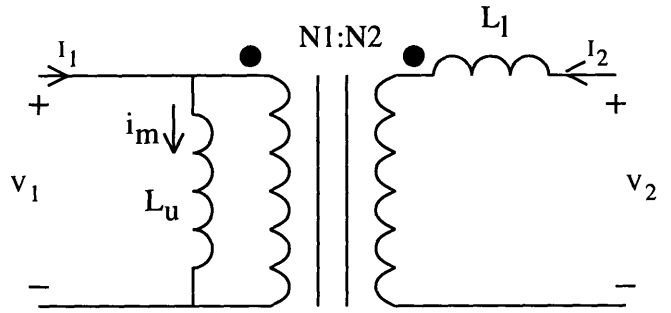


Figure 5-7: A model for the transformer

5.3 The Current Transformer

5.3.1 Introduction

Another nonintrusive and reliable way to measure currents is to use a current transformer, called a CT for short. The CT works by transforming the primary inverter current into an appropriate secondary current that can be measured by monitoring the voltage across a burden resistor. The proposed current transformer topology is shown in Fig. 5-6. The inverter output current, I in Fig. 5-6, will flow through the primary, thereby inducing a flux in the toroidal core. The flux will then be coupled through the secondary windings, which induces a current in the secondary. This secondary current, i_2 in Fig. 5-6, can be measured by monitoring the voltage across the burden resistor, R. A model of a transformer is shown in Fig. 5-7, where L_μ is the

magnetizing inductance, and L_l is the leakage inductance. If magnetizing and leakage effects are negligible, the ideal transformer results. The ideal transformer relations then relate the primary and secondary voltage and currents:

$$\frac{V_1}{V_2} = \frac{N_1}{N_2} \tag{5.2}$$

$$\frac{I_1}{I_2} = -\frac{N_2}{N_1} \tag{5.3}$$

In the case of the current transformer, the voltage across the burden resistor is then related to the primary inverter current by the following equation:

$$V_{out} = \frac{N_1}{N_2} IR \tag{5.4}$$

There are many sources that contribute to the over-all error of this method. Non-idealities in the current transformer can have significant effects: The finite permeability of a real core requires that a nonzero difference between the two currents exists in order to create the flux in the core. This difference is called the magnetizing current, and has been indicated as I_m in Fig. 5-6 and Fig. 5-7. It is important to realize that the magnetizing current will subtract from i_2 and will decrease the voltage measured across the burden resistor. It is therefore necessary to keep I_m as small as possible, which can be achieved by having a high permeability toroidal core, a large cross-sectional area, and by having many turns on the secondary winding, issues that must be addressed in designing the current transformer.

Errors might also arise if the permeability of the core changes over frequency or current levels. For a particular region of operation, selecting an appropriate core therefore becomes important. Another error source can of course be found in the burden resistor, for which reason a 1% resistor is recommended.

The leakage inductance does not have an effect in this case, since the transformer is transforming current.

One problem with this method is that it can only measure ac currents above a

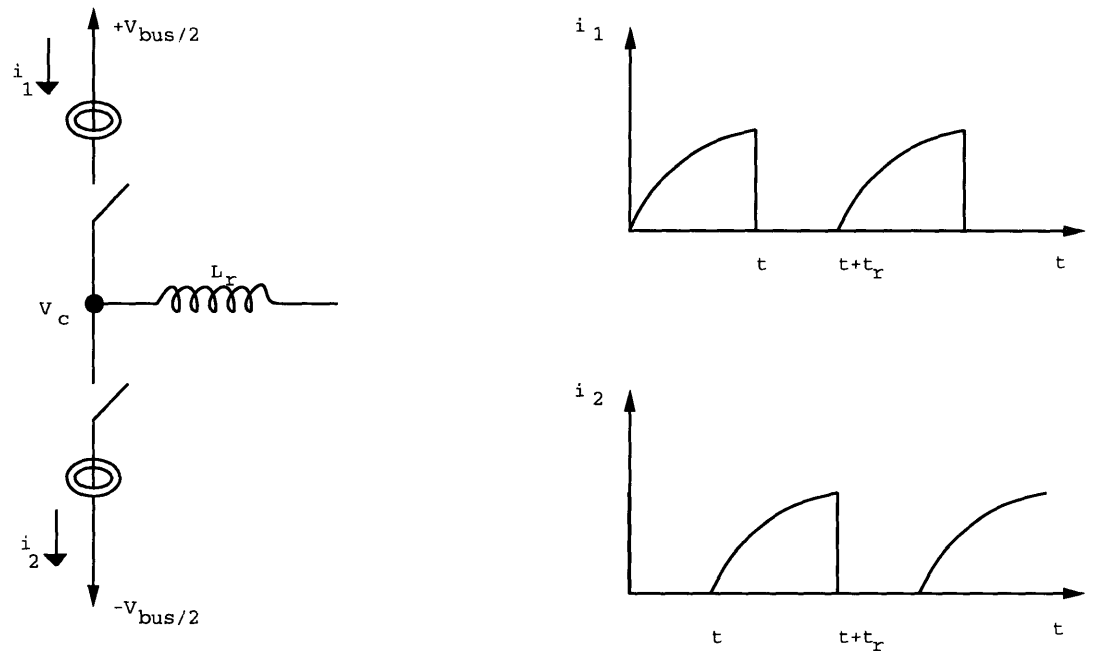


Figure 5-8: The placement of the current transformers

certain frequency. This is due to the magnetizing current which, at a sufficiently low frequency, will saturate the core. Therefore, two current transformers must be used in conjunction with a resetting mechanism. The two CT's should be placed on the top and bottom switch, since the current is known to be exactly zero in each switch for part of the cycle (see Fig. 5-8). This will allow the CT closest to the open switch to reset its magnetizing current by means of its resetting mechanism while the other CT is measuring the current through the closed switch. This also implies that the size of the core will be related to the frequency that needs to be sensed: The larger the maximum magnetizing current (or equivalently, the lower the switching frequency), the larger must the core cross-sectional area be, holding all other parameters constant. The issue is then to ensure that the magnetizing current of the secondary winding remains small, and that V_{reset} is sufficiently large to reset the flux in the core during t_r (see Fig. 5-8) where t_r depends on the duty ratio.

5.3.2 Designing the Current Transformer

From the specifications of the inverter, it is known that V_{bus} is 300V, I_{peak} is $2I_r+I_{min}$ which amounts to a maximum current of 44A, and that the switching frequency ranges from 20kHz to 80kHz. The goal is to design a system where the output voltage is 0.1V for every 1A going through the primary. Then, allowing for a power dissipation of 1W, the voltage on the primary can be calculated:

$$\begin{aligned} V &= \frac{P}{I} \\ V &= \frac{1W}{50A} \\ V &= 0.02V \end{aligned} \tag{5.5}$$

Assuming that the desired peak voltage on the secondary is 5V, the size of the resistor, R, can be calculated using:

$$P = \frac{V^2}{R} \tag{5.6}$$

From the equation above, R is selected to be a 25Ω, 1% resistor. Then, it is necessary to invoke the ideal transformer relations. An illustration showing how the transformer variables are defined can be seen in Fig. 5-7. By means of Eqn. 5.2 it is possible to calculate the number of turns on the secondary:

$$\begin{aligned} N_2 &= \frac{N_1 V_2}{V_1} \\ N_2 &= \frac{5}{.02} \\ N_2 &= 250 \end{aligned} \tag{5.7}$$

Having chosen these parameters, it is now possible to pick a suitable core. In Phillips "Ferrite Materials and Components Catalogue", it is stated that B_{sat} for a toroidal ferrite core is approximately 0.38T. Since the analysis that follows ignores core losses as well as imperfections in flux linkage, a conservative value of B_{sat}=0.30T will be used in the following equations. In order to stay out of saturation, the total

permissible flux is:

$$\lambda = N_2 A_c B_{sat} \tag{5.8}$$

Since the minimum switching frequency is 20kHz, with a worst case duty ratio of 0.75, the maximum number of Volt-seconds across the transformer will be:

$$\begin{aligned} \lambda_{max} &= \frac{5V}{20{,}000Hz} * \frac{3}{4} \\ \lambda_{max} &= 1.88x10^{-4}\,Vs \end{aligned} \tag{5.9}$$

Then,

$$\begin{aligned} A_c &= \frac{1.88x10^{-4}}{250x0.3} \\ A_c &= 2.50x10^{-2}\,cm^2 \end{aligned} \tag{5.10}$$

Based on these values, an appropriate core was selected. Its parameters are A_c=0.128cm^2, l_c=2.95cm, and μ=2700μ_0. This core has a constant permeability up to 100kHz, and saturates at about 0.38T.

Since all the design parameters are known, it is now possible to calculate the magnetizing inductance, L_μ. This value will aid in determining the actual performance of the CT, as is shown below.

$$\begin{aligned} L_\mu &= \frac{N^2 \mu A_c}{l_c} \\ L_\mu &= 92mH \end{aligned} \tag{5.11}$$

It is necessary to check what the magnetizing current I_m will be at different frequencies, since the error of the current measurement is directly proportional to the magnetizing current. Thus, using:

$$\Delta I = \frac{\Delta t\, V}{L_\mu} \tag{5.12}$$

it is clear that at 20kHz:

$$\Delta I = 2.7mA \tag{5.13}$$

at 50kHz:

$$\Delta I = 1.1mA \tag{5.14}$$

at 80kHz:

$$\Delta I = .70mA \tag{5.15}$$

These values of magnetizing current must then be compared to the current through the secondary. At maximum primary current input, the secondary current can be seen to be:

$$\begin{aligned} i_2 &= \frac{44A}{250turns} \\ i_2 &= 176mA \end{aligned} \tag{5.16}$$

Evidently, the magnetizing current will be very small (at all frequencies of interest) in comparison to the full scale current induced in the secondary, resulting in a very small full scale error. The worst case full scale error will be:

$$\begin{aligned} error_{magnetizing} &= \frac{2.7mA}{176mA} * 100\% \\ error_{magnetizing} &= 1.5\% \end{aligned} \tag{5.17}$$

A full scale error of 1.5% is more than acceptable.

As was shown above, the magnitude of the magnetizing current grows with decreasing switching frequency. At some low switching frequency the magnetizing current will be so significant that the measurement no longer is useful. Allowing for 10% error in the measurement means a ΔI of 17.6mA, and the lower limit on the bandwidth is then:

$$\begin{aligned} f_{min} &= \frac{V}{L_\mu \Delta I} \\ f_{min} &= 2kHz \end{aligned} \tag{5.18}$$

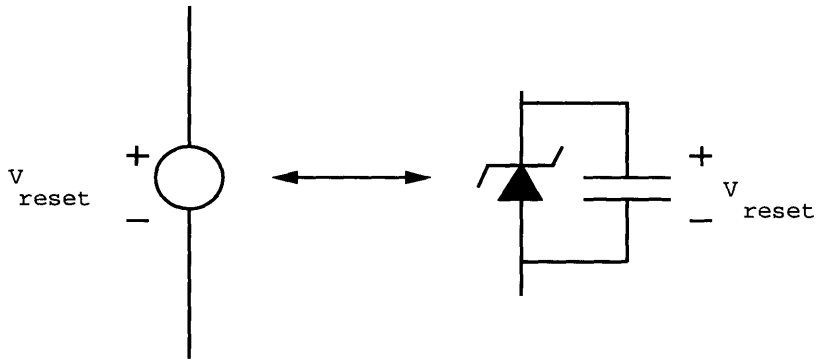


Figure 5-9: Implementation of the resetting voltage

There is in fact a simple way to lower the minimum switching frequency even further if necessary. The magnetizing current could be reduced by reducing the voltage on the secondary. To compensate for this, an op-amp with some gain can be added to the output of the secondary. This would decrease the minimum switching frequency (holding all other parameters constant), or alternatively, allow the user to select a smaller core (with f_{min} at 2kHz) since the number of Volt-seconds have decreased. The disadvantage of this scheme is the added cost of the extra chip.

5.3.3 Designing the Resetting Mechanism

The purpose of the resetting mechanism is to ensure that the magnetizing current is reset to zero while the CT is not measuring any current. The resetting voltage source is implemented by means of a zener diode in parallel with a capacitor as shown in Fig. 5-9. In order to choose the appropriate resetting voltage, the worst case duty ratio must be known. The worst case duty ratio occurs when the output voltage is at its maximum. Under the assumption that there is 80% bus utilization, the maximum output voltage, V_{cf}, will be 240V. From the illustration in Fig. 5-10, it is clear that for $t_0 < t < t_1$, the top switch is on, and the voltage across the inductor, L, is 300V less 240V. For $t_1 < t < t_2$, the bottom switch is on, and the voltage across the inductor

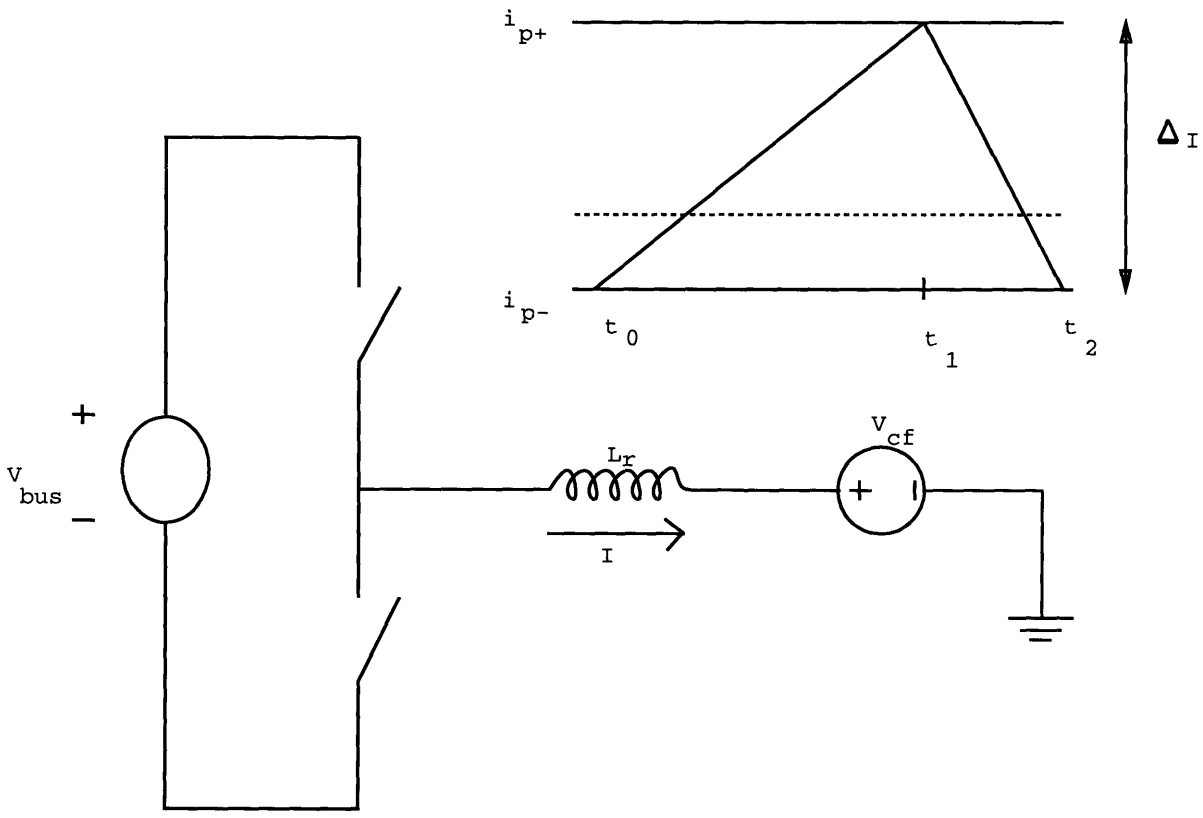


Figure 5-10: Illustration of worst case duty ratio

is minus 240V. Then, using the relationship that

$$\Delta I = \frac{\Delta t V}{L} \tag{5.19}$$

the minimum time required to reset a core during operation can be calculated, which in turn dictates the size of the resetting voltage. From Fig. 5-10 it is then clear that:

$$\begin{aligned} \Delta I_1 &= \frac{\Delta t_1 V_1}{L} \\ \Delta I_2 &= \frac{\Delta t_2 V_2}{L} \end{aligned} \tag{5.20}$$

In this case, $\Delta I_1 = \Delta I_2$, so it follows that:

$$V_1 \Delta t_1 = V_2 \Delta t_2 \tag{5.21}$$

Therefore, the ratio between Δt_1 and Δt_2 is equal to the absolute ratio between the two voltages applied across the inductor, in this case 0.25. This means, that in the worst case scenario, a CT will only have one quarter of the time to reset I_m compared to the time the secondary voltage was applied across L_μ. The zener diode, subsequently, must be at least four times the maximum secondary voltage of 5V. In this design, a zener diode of 24V was selected in order to provide some margin of safety.

The reset mechanism also sets the upper limit of the bandwidth in this case. A reset voltage of 24V means that the maximum switching frequency is:

$$\begin{aligned} f_{max} &= \frac{24}{20} * 80kHz \\ f_{max} &= 96kHz \end{aligned} \tag{5.22}$$

5.3.4 Testing the Current Transformer

The test conditions for the current transformer were the same as for the Hall-effect sensor. The behavior of the CT was examined at low and high current levels as well

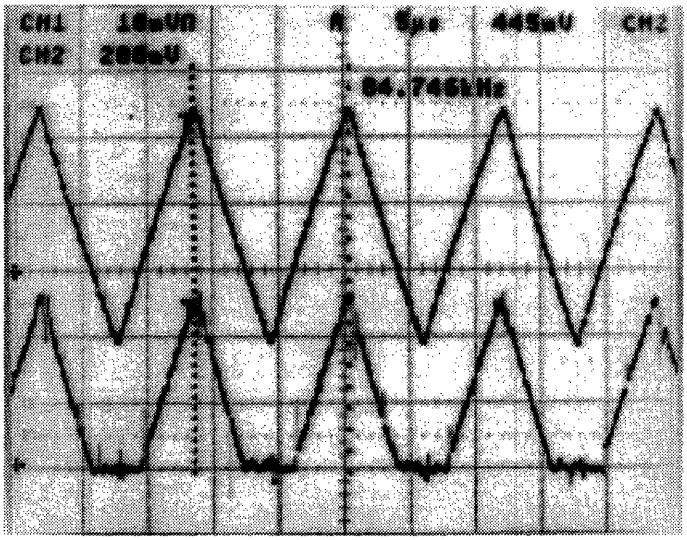


Figure 5-11: Output waveform for current transformer (bottom waveform) as compared to a current probe measurement (top waveform) at a high switching frequency. The setting is 2A/div and the switching frequency is 84.7kHz.

as low and high switching frequencies. Even though two current transformers would be required in order to measure both negative and positive current, it is sufficient to test only one CT to determine bandwidth and accuracy. Therefore, all measurements taken display positive currents only. Figure 5-11 shows a measurement made at 84.7kHz. The oscilloscope is set to display 2A/div. Even though there is some noise on the CT output waveform (bottom), it still follows the current probe measurement (top) quite accurately.

The waveform was examined in closer detail in order to determine the accuracy at low current levels. The result is displayed in Fig. 5-12. Here, the switching frequency is 60kHz, and the oscilloscope is set to 1A/div. The CT output waveform (noisy) slightly exceeds the current probe measurement (clean). The error, however, is negligible. At high current levels the error turned out not to be negligible. This measurement is shown in Fig. 5-13. The switching frequency is 13.3kHz, and the oscilloscope is set to display 5A/div. Here, the CT waveform exceeds the current probe measurement, resulting in a 5% error. This error, however, is still acceptable.

Finally, a measurement was made in order to capture how the resetting mechanism

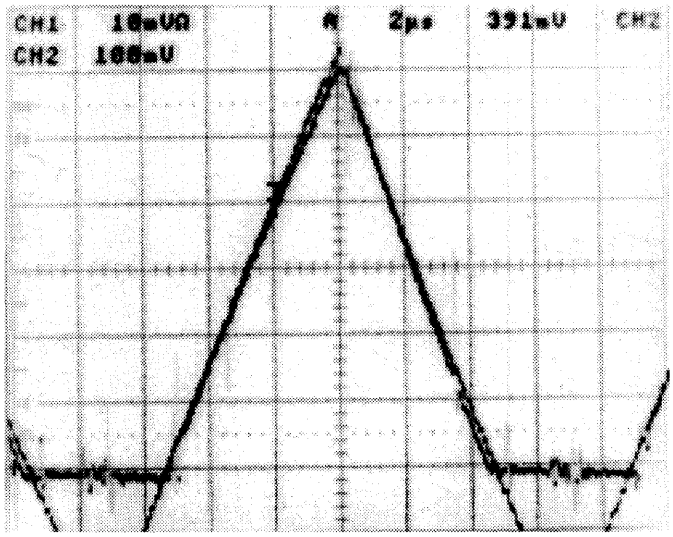


Figure 5-12: Output waveform for current transformer (noisy, cutoff waveform) as compared to a current probe measurement (clean, full waveform) at low current levels. The setting is 1A/div and the switching frequency is 60kHz.

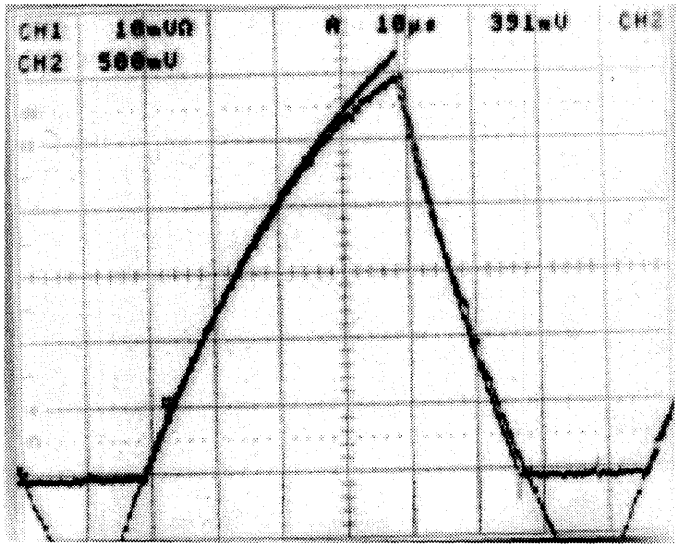


Figure 5-13: Output waveform for current transformer (cutoff waveform) as compared to a current probe measurement (complete waveform) at a low switching frequency. The setting is 5A/div and the switching frequency is 13.3kHz.

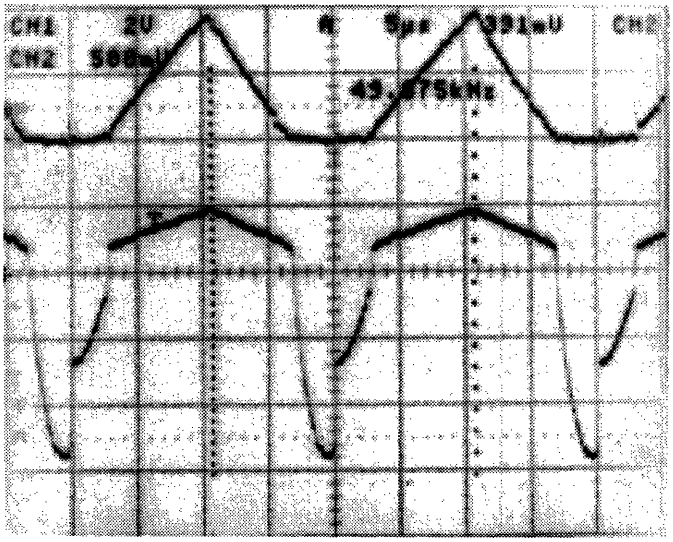


Figure 5-14: Oscilloscope picture showing the resetting mechanism. The top waveform shows the current measured by the CT, displayed at 5A/div. The bottom waveform shows the voltage measured at the CT terminals at 2V/div.

works, shown in Fig. 5-14. The top waveform shows the current as measured by the CT, displayed at 5A/div. The bottom waveform shows the voltage measured at the terminals of the current transformer. When the CT actually measures current, the voltages at the burden resistor and the terminal are equal (except for the diode drop). When the core is resetting, the burden resistor voltage goes to zero, and a negative voltage occurs at the terminals which resets the core.

5.3.5 Conclusion

The advantages of the CT are that it is nonintrusive, simple, it has a rather small power dissipation, gives an isolated measurement, and there is no need to sense any other voltages and currents since the reset mechanism is automatic. The downside is that two extra toroidal cores must be added to each RPI. The errors measured in the prototype were discernible, but not excessive. A summary of the CT results is shown in Table 5.2. The worst case error is approximated as the sum of all the individual errors. The measured error signifies the largest error measured under the experimental circumstances above. The bandwidth is based on a theoretical estimate:

Worst Case Error:	3%
Measured Error:	5%
Bandwidth:	2kHz-96kHz
Cost:	Very low

Table 5.2: Summary of the findings for the current transformer.

The lower limit is determined by the magnitude of magnetizing current, and the upper limit is determined by the resetting mechanism. The cost is an estimation of the cost of one complete CT system for an RPI relative to that of a Hall-effect sensor.

5.4 Resistive Current Sensing

5.4.1 Introduction

Resistive current sensing is a seemingly inexpensive means of measuring current. The idea is to put a small sense resistor of a known value in series with the output that is to be sensed. The voltage across that resistor is then directly proportional to the current, where the constant of proportionality is the resistance of the sense resistor. The voltage can be measured by using a simple op-amp configuration as is suggested in [14]. An example of such an implementation can be seen in Fig. 5-15.

However, several characteristics of the parallel inverter system complicates the implementation of this method. First, neither side of the sense resistor is connected to ground, which means that the inputs to the op-amp must somehow be isolated from the sense resistor, for example by means of an opto-coupler. Also, the currents are high, so a very small resistor is required if power dissipation is not to be excessive. This, in turn, results in very small voltage drops across the resistor, making it difficult to measure the voltage accurately, and possibly making the inductance of the resistor significant as an error source.

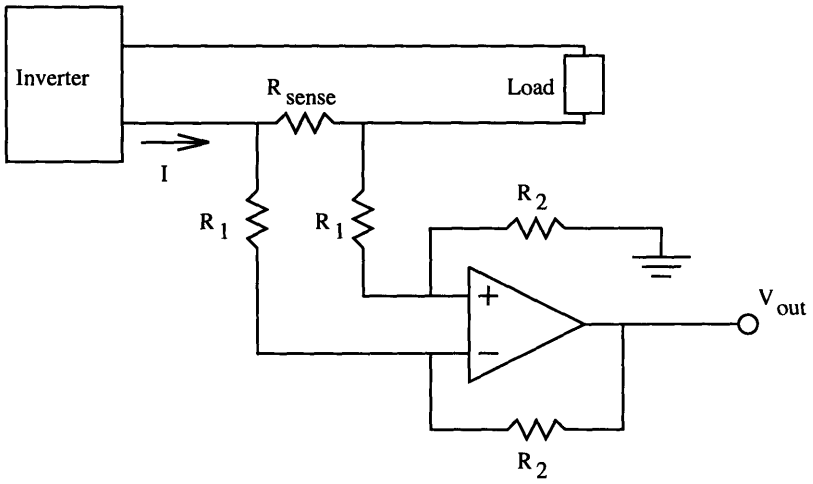


Figure 5-15: The resistive current sensing system.

5.4.2 Designing the Sense Resistor

The upper constraint on the value of the sense resistor is set by power dissipation considerations. By deciding that power dissipation may not exceed 2W, and by knowing that the rms value of the inverter output current is 20A, the value of the sense resistor is dictated by:

$$R_{sense} = \frac{P_{diss}}{I^2} \tag{5.23}$$

By inserting the values above it is clear that the sense resistor must not exceed 5mΩ. The maximum voltage across the sense resistor, 220mV, would occur when the inverter output current is at its maximum of 44A.

A maximum voltage across the sense resistor of 220mV clearly is not very much. Since the inverter output current is switching at 20kHz or more, the inductance of the resistor might therefore become significant. This argument is evident from:

$$V_{sense} = IR_{sense} + L_{sense}\frac{dI}{dt} \tag{5.24}$$

Clearly, if the second term on the right hand side of Eqn. 5.24 is comparable to the first term, the current measurement in terms of V_{sense} will be incorrect. The issue then becomes to keep the inductance of the sense resistor low. In order to find out

how low it needs to be, a worst case scenario was considered. The maximum $\frac{dI}{dt}$ will occur when the waveform is switching between I_{min} and I_{max} at 80kHz. Under those conditions, $\frac{dI}{dt} = 3.84 * 10^6 \text{A/s}$. Assuming that the first term in Eqn. 5.24 should be at least one order of magnitude larger than the second term, the maximum allowable inductance can be calculated. Since $L\frac{dI}{dt}$ must then be less than 22mV the constraint on the inductance of the sense resistor can be seen to be:

$$\begin{aligned} L_{sense} &< \frac{22mV}{\frac{dI}{dt}} \\ L_{sense} &< 5.7nH \end{aligned} \tag{5.25}$$

This is clearly a very tight constraint. In order to evaluate the feasibility of the sense resistor concept as a current sensing scheme for this system, a 5mΩ prototype sense resistor was constructed. However, the inductance of the prototype was 300nH, far exceededing the inductance constraint imposed in Eqn. 5.25. Based on the experience with the prototype, it was decided that the resistive current sensing scheme is very difficult to implement for this system, if not impossible. The scheme was therefore deemed impractical, and no further attempts to implement the resistive current sensing system were made.

5.5 The Rogowski Coil

5.5.1 Introduction

Another non-intrusive way to measure the output current of the inverter is by means of a Rogowski coil, also called a Maxwell worm. A Rogowski coil is a uniformly wound coil of constant cross-sectional area on a non-magnetic former shaped into a closed loop to surround a current carrying conductor [15]. The voltage at the open terminals of the Rogowski coil is directly proportional to the time derivative of the current passing through it. The advantages of the Rogowski coil include the facts that it has an excellent bandwidth, it does not load the circuit, it does not saturate, it gives an isolated current measurement, and it adds a significantly lower cost to the

circuit than does a comparable Hall-effect sensor.

The Rogowski principle has been known since 1912 [16]. It can be shown by using Faraday's law that the induced voltage at the open circuited terminals of the winding is directly proportional to the permeability of the former (usually air), the area of each turn (A_t), the number of turns (N), and the time derivative of the current passing through the coil. This is expressed as:

$$V = \frac{\mu N A_t \, dI}{dt} \tag{5.26}$$

Note that the Rogowski coil need not be circular, as long as every turn has the same crossectional area.

The complete Rogowski coil current sensing system consists of three parts: The coil itself, an integrator to integrate the output voltage, and a reset mechanism to reset the integrator whenever zero current is passing through the Rogowski coil.

5.5.2 Designing the Rogowski Coil System

One of the reasons for which this method has not been widely used in power converters has been the difficulty in designing the integrators. In an op-amp implementation the output of the integrator will be the integrated voltage from the Rogowski coil plus the integral of the constant offset voltage of the op-amp. The integral of the constant offset voltage will be a ramp, leading to an error that always grows with time which eventually will make the op-amp go into saturation, unless the necessary precautions are taken.

The op-amp instability can be circumvented by adding the resetting mechanism. One way of using the resetting mechanism is to reset the op-amp integrator to zero at every instance the current through the coil is zero. A simple voltage sensor is already available in the RPI that detects zero voltage crossings for each switch, which is information that can be used to deduce when the current through the coil is zero and the integrator can be reset. The Rogowski coil system, as suggested by [17] is illustrated in Fig. 5-16.

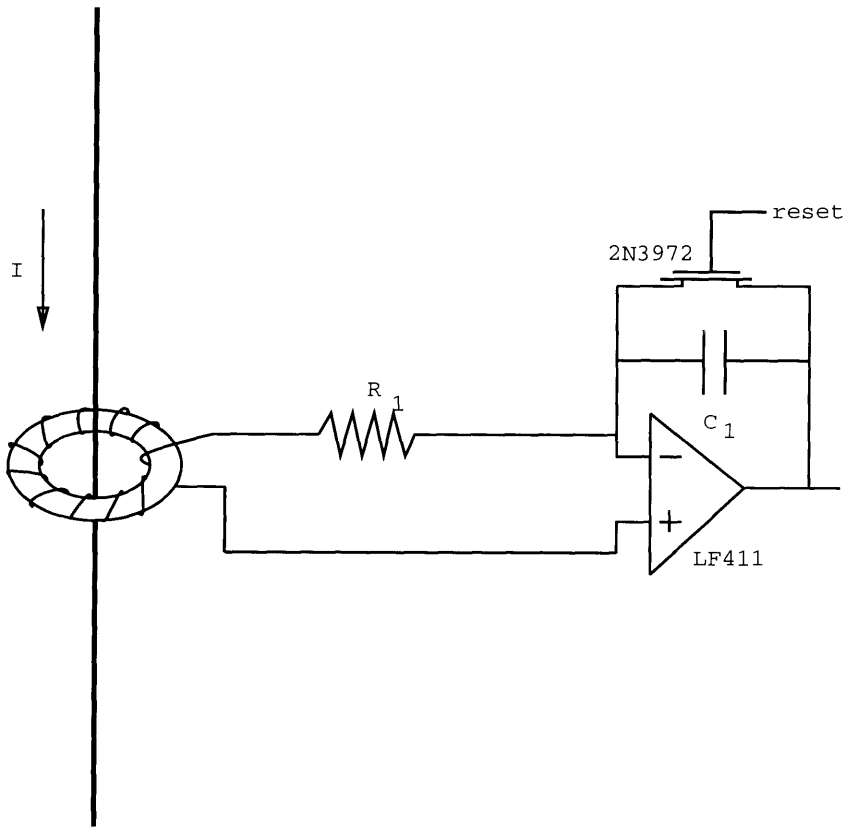


Figure 5-16: Rogowski Coil System

The design of the Rogowski coil system requires many trade-offs to be examined. The choice of op-amp is one such example. All op-amps will have a both a voltage offset and a current offset which will become part of the measurement error. For example, the additional voltage V_{err} put out due to the voltage offset can be seen to be:

$$V_{err} = \frac{V_{offset} t_{max} l}{N A_t \mu I} \tag{5.27}$$

The choice of op-amp also limits the selection of integrating components. The lower limit of the integrating resistor is set by the current sinking capability of the op-amp: Whenever the output voltage of the Rogowski coil is non-zero, a current will flow through the integrating resistor since the negative input to the integrator is at virtual ground. This current must be sunk by the op-amp, which means that R_i must be large enough so that the maximum current through R_i does not exceed the current sinking limitation. However, if R_i becomes too large, the currents through the resistor will be small, and the current offset error might become significant.

The value of the integrating capacitance C_i is limited by what switch is selected to implement the resetting mechanism. The lower limit is determined by the parasitic capacitance of the switch. When the switch is turned off, all the charge in the parasitic capacitance is transferred to the integrating capacitance. This will be part of the measurement error:

$$error_{parasitic} = \frac{C_{parasitic}}{C_i} * 100\% \tag{5.28}$$

Therefore, C_i should preferably be some order of magnitude greater than the parasitic capacitance of the switch.

The upper limit of C_i is determined by the on-state resistance of the switch. When the switch changes from its non-conducting to its conducting state, the on-state resistance will be in parallel with the integrating capacitor, resulting in an R-C time constant delay before the switch is actually closed. It is of interest to keep this time constant sufficiently small so that the integrator can be reset in the time period

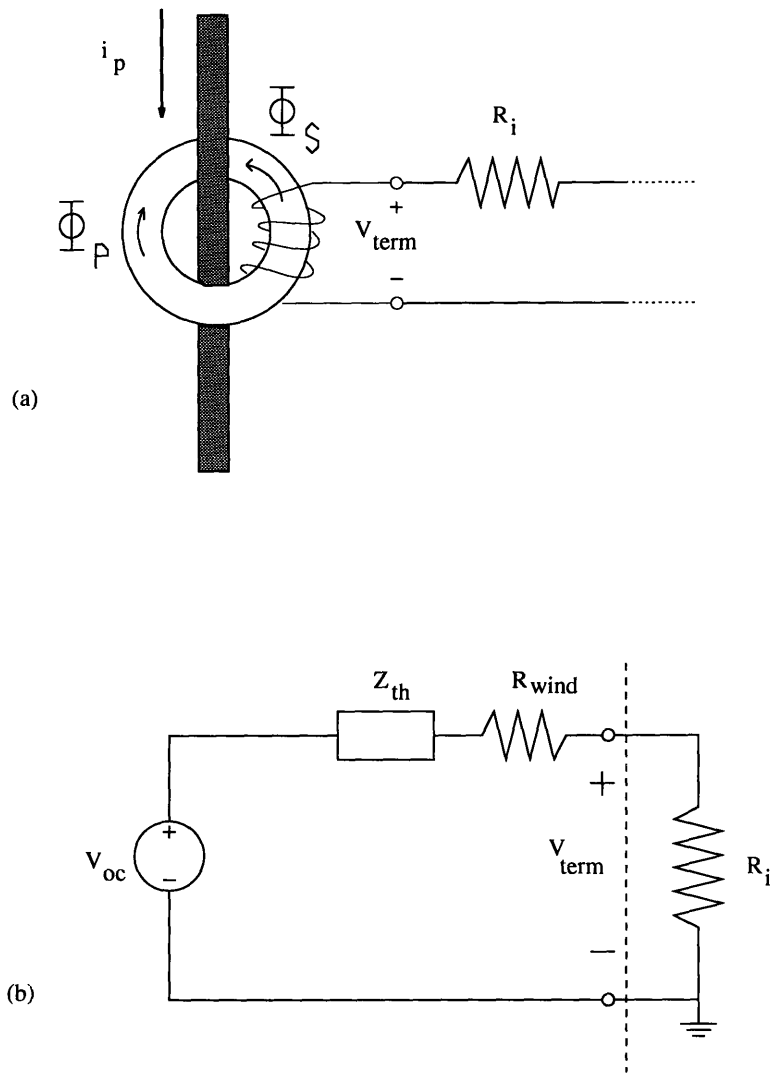


Figure 5-17: The Rogowski coil and its Thevenin equivalent.

provided by the zero voltage detection system.

In contrast to the current transformer, the Rogowski coil will not saturate since it is an air-core structure. One problem that might arise, however, is the phenomenon of loading. To see this, consider Fig. 5-17a. The primary current I_p gives rise to flux Φ_p in the core. It is this flux that is coupled by the secondary windings, giving rise to the voltage at the terminals of the secondary. However, the current going through the integrating resistor gives rise to a flux in the opposite direction in the core, denoted as Φ_s in Fig. 5-17a. This will in effect reduce the total flux linked by the secondary,

which in turn will contribute to the error of the desired current measurement. In order to mathematically check that this error is not significant, the coil is modeled as its Thevenin equivalent, as illustrated in Fig. 5-17b. Here, R_{wind} is the winding resistance of the Rogowski coil, V_{oc} is voltage at the terminals of the coil when no loading occurs, and Z_{th} is the Thevenin impedance that is to be determined. Then, ignoring the winding resistance, it follows that:

$$V_{term} = \frac{d}{dt}N(\Phi_p - \Phi_s) = \frac{d}{dt}(\frac{N\mu_0 A_t i_p}{l} - L_{coil}i_s) \tag{5.29}$$

Since $i_s = \frac{V_{term}}{R_i}$,

$$V_{term} = \frac{N\mu_o A_t}{l}\frac{di_p}{dt} - \frac{L_{coil}}{R_i}\frac{dV_{term}}{dt} \tag{5.30}$$

This can be rewritten as:

$$V_{term} = \frac{N\mu_o A_t i_p}{l}\frac{s}{1+\frac{L_{coil}}{R_i}s} \tag{5.31}$$

From Eqn. 5.31, it is clear that the Thevenin impedance is in the form of an inductor, with an inductance of L_{coil}. This inductor will combine with the integrating resistor to look like an L-R low-pass filter, which in effect limits the bandwidth of the Rogowski coil. Clearly, the input resistor should be as large as possible in order to push the pole further out on the negative real axis. However, if loading does become a significant problem, it can easily be alleviated by adding a follower before the integrating resistor. This will work as a buffer, and no loading will occur. The disadvantage of this addition is that it will add another chip to the circuit, which in turn will add cost as well as more offset errors to the system.

Another issue that speaks for a large input resistor is the winding resistance effect. The winding resistance will attenuate the voltage measured across the integrating

resistor by a factor of $\frac{R_i}{R_i+R_{wind}}$, which will be referred to as the winding resistance error. Clearly, the larger the integrating resistor, the smaller the attenuation effect.

In conclusion, there are many possible sources of error in the system. The offset errors, either voltage, current, or both, can become significant under certain circumstances. The parasitic capacitance of the resetting switch will add to the voltage across C_i, resulting in a measurement error. The loading of the circuit can become a significant error depending on the selection of components, as can the winding resistance. Also, the integrating components will only be specified to a certain degree: The resistor within 1% and the capacitor within 10%. All of these issues must be taken into account during the design of the Rogowski coil system.

5.5.3 Designing the Rogowski Coil

The design of the Rogowski coil calls for a former which has the same permeability as air. In this case, a wooden former was selected, since this gives appropriate structural strength while allowing flexibility in selecting the size of the former.

The design started with a wooden toroid with an inner radius r_{in} of 1.0cm and an outer radius r_{out} of 1.5cm. Its cross-sectional area A_t was measured to be $0.475*10^{-4}m^2$, and the average circumference was 0.0785m. The desired scaling was set such that the output voltage of the integrator is 0.1V for every 1A passing through the primary. The R_i-C_i time constant divided by N, the number of turns, can then be calculated from Eqn. 5.26.

$$\frac{N}{R_iCi} = \frac{V_{out}l}{A_t\mu I} = \frac{5*.0785}{.475*10^{-4}*1.26*10^{-6}*50} = 1.31 * 10^8 \tag{5.32}$$

In order to pick the appropriate R-C time constant for the integrator, several design trade-offs had to be explored. The limits for the integrating capacitance are determined by the characteristics of the device shorting the capacitor. In this case, the 2N3972 was used to short the integrating capacitor at the desired instances. The 2N3972 is an N-channel JFET with a on-state resistance of about 25Ω, and a parasitic

capacitance on the order of 25pF.

The lower limit of the integrating capacitance is determined by the parasitic capacitance of the 2N3972. All the charge in the parasitic capacitor will be dumped into the integrating capacitor as the 2N3972 is turned off. This is a measurement error inversely proportional to the size of the integrating capacitor. If the maximum error allowed is 1%, clearly, the integrating capacitance must be larger than 2.5nF. The upper limit of the integrating capacitor is determined by considering the on-state resistance of the 2N3972. This resistance will be in parallel with the integrating capacitor during turn-on, resulting in an R-C time delay before the switch is shorted. For a value of C_i=4nF, the R-C time constant is on the order of 100ns, which for this application is sufficiently fast.

The integrating resistor R_i value was determined by trial and error using Eqn. 5.32, while complying with all the constraints mentioned above. It was found that an appropriate value is 470Ω. This leads to that the number of turns N must be equal to:

$$N = 1.31 * 10^8 R_i C_i = 247 turns \tag{5.33}$$

The op-amp selected for this application was the LF411. This JFET input op-amp has very low offset voltage (0.5mV max), low input bias current (50pA), wide gain bandwidth (3MHz), and high slew rate (10V/μs). From these specifications it was concluded that the current offset is negligible and that the designer should be concerned primarily with the offset voltage. The effect of the offset voltage was shown in Eqn. 5.27. The value for t_{max} must clearly be the inverse of the slowest switching frequency, 1/20kHz. The maximum contribution from the offset voltage then comes to $V_{err} = .05V$. This worst case error contribution is only 0.5% of the maximum output voltage which is acceptable.

After having constructed the Rogowski coil, its characteristics were measured in order to examine the significance of the loading effect, as well as the winding resistance

Parameter	Value
N	247
A_t	$0.475x10^{-4}m^2$
l	0.0785m
R_i	470Ω
C_i	4nF

Table 5.3: Summary of the design parameters for the Rogowski coil.

effect. The winding resistance and the inductance of the Rogowski coil were measured to be 33Ω and 52μH respectively. Since the integrating resistor R_i is 470Ω, the $\frac{L_{coil}}{R_i}$ time constant is on the order of 1.7μs. This means that the L-R lowpass filter breakpoint is at 588kHz, which is sufficiently above the maximum switching frequency of 80kHz, suggesting that loading is not limiting the bandwidth of the Rogowski coil in this implementation. The winding resistance will contribute 33/(470+33)=6% to the overall error. The design parameters chosen for this particular implementation are summarized in Table 5.3.

The lower limit of the bandwidth of this design is dictated by the offset voltage of the op-amp. If the maximum offset error allowed is set to be 10% of full scale, using Eqn. 5.27 shows that the minimum switching frequency is 1kHz. The upper limit of the bandwidth is dictated by the low-pass filter stemming from the loading effect. The upper limit of the bandwidth is then 600kHz.

The worst case error contribution is approximated as the sum of all the individual errors. There would then be 0.5% contribution from the offset voltage, 0.5% from the parasitic capacitance of the 2N3972, 6% from the winding resistance, 1% from the integrating resistor, and 10% from the integrating capacitor. This results in a worst case error of 18%.

5.5.4 Designing the Resetting Mechanism

The resetting mechanism for the Rogowski coil consists of a switch that shorts the capacitor (C_i) in every instance in which the inverter output current is zero. The

'On'	'Off'
GND	-15V

Table 5.4: Summary of the logic signals required to operate the JFET.

logic signal stating when the integrator can be reset was meant to be provided by the zero voltage crossing detection system described in chapter 4. However, since the RPI was yet to be completed at the time of the current sensing experiments, the zero voltage detection scheme was emulated using two op-amps. The emulation method is documented in appendix B. For the discussion it suffices to know that the zero voltage crossing signal is at +5V whenever the current through the Rogowski coil is not zero, and drops to ground whenever the primary current is within some delta of zero.

As was mentioned above, the switch to reset the integrator was implemented using a 2N3972 N-channel JFET. To turn the JFET off requires that the gate voltage is held at least 3V lower than either the drain or source voltage. In order to turn the JFET on, the gate has to be held at the drain or source voltage, but should not surpass it, or a diode will conduct in the device. Since one of the inputs is at virtual ground, it is sufficient to hold the gate at ground in order to turn the JFET on. The logic signals required to operate the JFET as the resetting switch are summarized in Table 5.4.

In order to level shift the zero voltage signal to the signal levels required by the 2N3972, the circuit shown in Fig. 5-18 was constructed. The level shifting circuit also current limits the stage by setting the resistor R_2 to the correct value. R_3 determines the turn-off time for the 2N3972 since it combines with the gate capacitance of the JFET to form an R-C time constant. For this application R_2 was selected to be 2.2kΩ and R_3 to be 470Ω. This current limits the stage to (5-0.6)/470=9mA, and results in a turn-off time on the order of 50nF. R_1 is a pullup resistor at the input selected to be 470Ω.

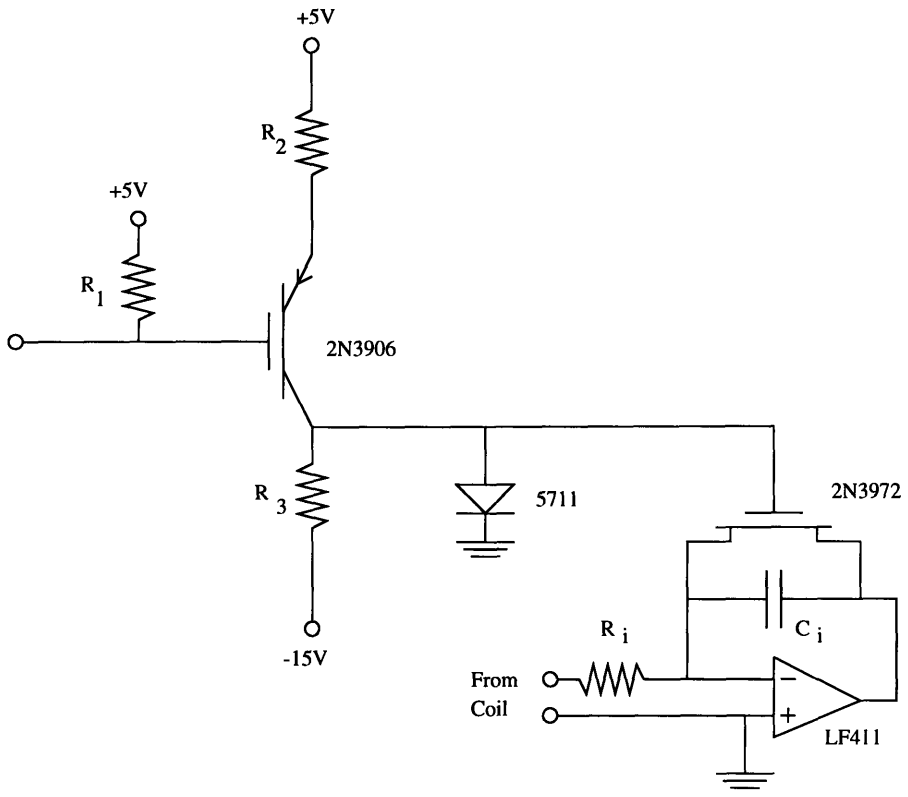


Figure 5-18: The circuit that shifts the zero voltage detection signals to the level required to operate the 2N3972 appropriately.

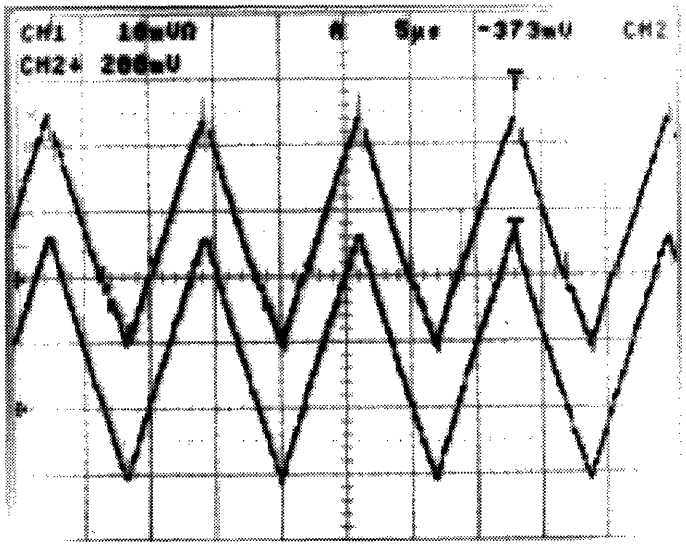


Figure 5-19: Output waveform for Rogowski coil (top waveform) as compared to a current probe measurement (bottom waveform) at a high switching frequency. The setting is 2A/div and the switching frequency is 85.5kHz.

5.5.5 Testing the Rogowski Coil System

The Rogowski coil system was tested under the same conditions as the Hall-effect sensor. Measurements for low and high current levels and switching frequencies were made. First the general current sensing capability at high switching frequencies of the Rogowski coil was examined, as shown in Fig. 5-19. The oscilloscope picture suggests that the Rogowski coil measures current accurately at the given switching frequency (85.5kHz) and current levels (2A/div). In order to examine in detail just how accurate the Rogowski coil is, two additional measurements were made. The first, shown in Fig. 5-20, displays the Rogowski coil measuring low currents at a high switching frequency. The oscilloscope setting is 1A/div, and the switching frequency is 65kHz. The upper waveform is the current measured by a current probe, while the lower waveform shows the Rogowski coil measurement. The difference amounts to a 3% error, which is acceptable. The second measurement was taken at high current levels and low switching frequency as shown in Fig. 5-21. Here, the Rogowski coil output is again the lower waveform, and the error actually seems to be less than 3%. This suggests that the offset voltage of the LF411 is coming into play: The

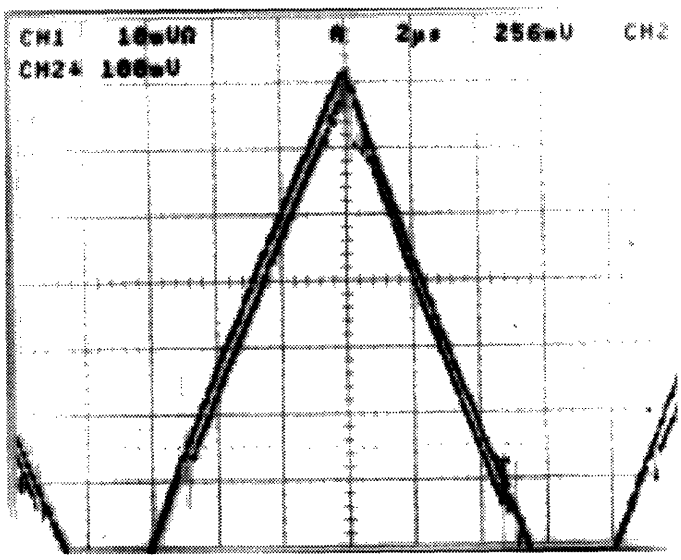


Figure 5-20: Output waveform for Rogowski coil (lower waveform) as compared to a current probe measurement (upper waveform) at a low current level. The setting is 1A/div and the switching frequency is 65kHz.

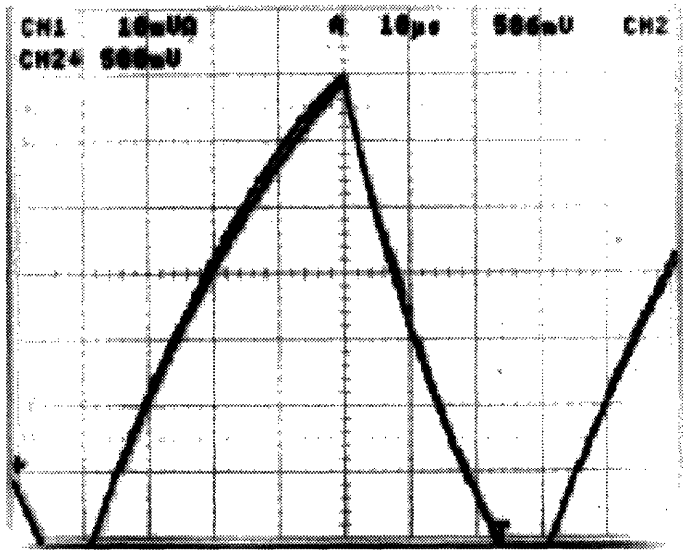


Figure 5-21: Output waveform for Rogowski coil (lower waveform) as compared to a current probe measurement (upper waveform) at a high current level. The setting is 5A/div and the switching frequency is 14kHz.

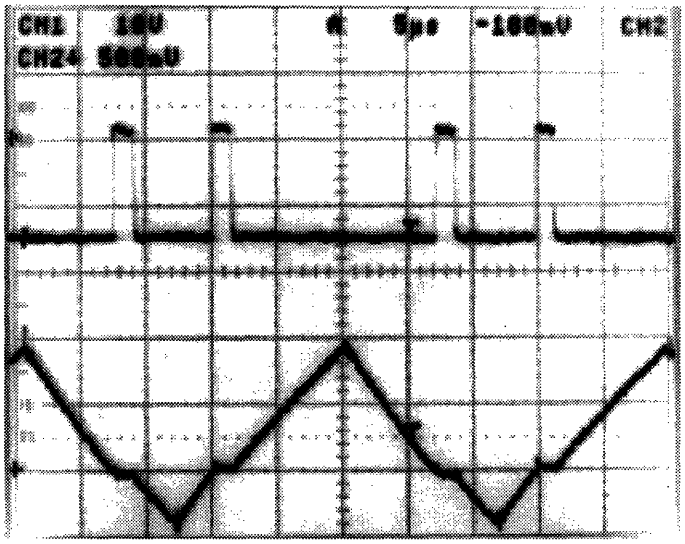


Figure 5-22: Oscilloscope picture showing the Rogoswski coil resetting mechanism. The top waveform shows the gate drive to the 2N3972, and the bottom waveform shows the Rogowski coil output waveform.

integrator is reset less often at lower switching frequencies which increases the effect of the voltage offset, which in turn increases the current measurement. This increase leads to a decrease in the net error.

Finally, one more measurement was taken in order to illustrate the resetting mechanism. Figure 5-22 shows two waveforms: The top waveform is the gate drive to the 2N3972, and the bottom waveform shows the output of the Rogowski coil. The resetting pulses have for illustration purposes been made longer by increasing the delta region in Fig. B-2. The integrator works as usual while the 2N3972 is open, that is, the gate drive is kept at -15V. Whenever the gate voltage goes up to GND, the 2N3972 shorts the integrating capacitor. This effect can be seen as the horizontal line in the Rogowski coil current measurement.

5.5.6 Conclusion

The Rogowski coil also seems to be an appropriate alternative to the Hall-effect sensor in measuring the currents in a PRPI system. It is small, inexpensive, non-intrusive, accurate, and has excellent bandwidth. The drawback of the Rogowski coil is that it

Worst Case Error:	18%
Measured Error:	3%
Bandwidth:	1-600kHz
Cost:	Low

Table 5.5: Summary of the findings for the Rogowski coil.

requires a resetting signal for its integrator, which in turn requires some sort of zero voltage detection scheme. In this particular application, the zero voltage detection scheme is already available since it is required to ensure the zero voltage switching condition of the RPI, but in a general case this might not true. Adding such a system is both costly and might affect the reliability of the inverter system.

A summary of the findings for the Rogowski coil is shown in Table 5.5. The worst case error is the sum of all individual errors that were considered. The measured error is the maximum error displayed during the experiments performed above. The lower limit of the bandwidth is in this case dictated by the offset voltage. The upper limit of the bandwidth is limited by the loading phenomena described above. The cost is the estimated cost of an entire Rogowski coil current sensing system as compared to a Hall-effect sensor.

5.6 The Second Winding

5.6.1 Introduction

The fifth and final current sensing system to be evaluated is the second winding approach. Sensing the output current by winding a second winding on the output inductor is conceptually a very pleasing idea. No new sensing components are added to the circuit since the output inductor is already present for current sharing. In this scheme, the output inductor is actually serving three purposes: It fulfills the current sharing requirements, it serves as the resonant inductor in the resonant topology, and it is used to measure the output current. One disadvantage of this scheme is that the constant of proportionality linking the primary and the secondary depends

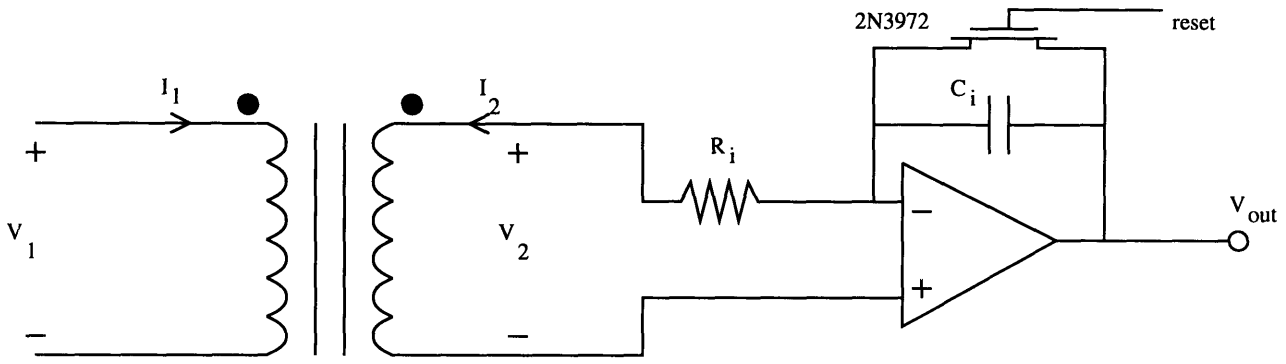


Figure 5-23: The second winding current sensing system

upon the material properties, and it is doubtful whether an accurate current sensing scheme that is sufficiently insensitive to variations in the inductor core properties and temperature can be devised. Another disadvantage of the second winding is that it also requires a resetting mechanism for the integrator, similar to the case of the Rogowski coil.

Winding a second winding on the output inductor effectively makes it look like a transformer. Again, assuming that the leakage inductance in the inductor is negligible means that the ideal transformer relations described in Eqns. 5.2 and 5.3 can be used. The importance of this assumption must not be underestimated, since the leakage inductance can potentially be the primary source of error. A model of the ideal transformer is shown in Fig. 5-7.

The ideal transformer relations can then be used to derive how the voltage across the secondary is related to the primary current through the inductor. Using Eqn. 5.2 yields the fact that:

$$V_2 = \frac{N_2}{N_1} V_1 = \frac{N_2}{N_1} L_r \frac{dI_1}{dt} \tag{5.34}$$

Here, L_r is simply the inductance of the resonant inductor. Again, as was the case for the Rogowski coil, the output voltage of the secondary must be integrated since it is proportional to the time derivative of the current passing through the primary. The complete system for sensing currents using the second winding approach is shown in Fig. 5-23. Note that the integrator is configured exactly as the integrator for the

Rogowski coil, but now new values for the resistor and the capacitor must be found. All the constraints on the Rogowski coil integrator also apply to the second winding integrator. The overall error contributions will also be similar. The specifications of the integrating components, the leakage inductance, loading effects, and offset errors might also occur in the second winding current sensing system. Finally, depending on the design of the output inductor, the permeability variations of the core over temperature and current levels might contribute significantly to the overall error.

5.6.2 Designing the Second Winding System

First, it is necessary to determine how many windings there should be on the secondary, N_2. For this purpose, one must recall the design specifications of the output inductor, as well as some additional specifications for the system. The output inductor was designed with 21 turns and had an inductance of 30μH. The maximum voltage across the inductor is 270V with 80% bus utilization. The maximum voltage on the second winding must therefore be:

$$V_{2max} = \frac{N_2}{N_1} V_{1max} = \frac{N_2}{21} 270 \tag{5.35}$$

For the input to the integrator to be less than 15V evidently requires the second winding to consist of only one winding, N_2=1. This would result in a maximum voltage on the secondary of V_{2max}=12.9V.

Making N_2=1 ensures that the input to the op-amp performing the integration does not saturate the op-amp. It is also necessary to ensure that the output of the op-amp does not exceed the point of saturation for the op-amp. Specifically, at 50A through the primary, an output voltage of 5V should appear at the output of the integrator in order to be consistent with the other current sensing systems. This is achieved by setting the R_i-C_i time constant to an appropriate value. Another reason to keep the output voltage below 5V is that the differential input voltage of the control system may not exceed 5V due to the inherent limitations of the PM219 (see Chapter 3).

In the current configuration of the current sensing system, the output voltage of the op-amp will be:

$$V_{out} = -\frac{1}{R_i C_i}\int_0^{\Delta t} V_{1max}dt = 12.9\Delta t\frac{1}{R_i Ci} \tag{5.36}$$

In order to solve this integral, it is of course necessary to find Δt.

$$\Delta t = \frac{L\Delta i}{V_{1max}} = \frac{30 * 10^{-6} * 50}{270} = 5.56 * 10^{-6} \tag{5.37}$$

Then, it follows that the R_i-C_i product must be:

$$R_i C_i = \frac{V_{1max}\Delta t}{V_{2max}} = \frac{12.9 * 5.56 * 10^{-6}}{5} = 1.43 * 10^{-5} \tag{5.38}$$

Now the issue becomes to select the appropriate R_i and C_i. This can be done by considering a number of ancillary issues. First, consider the integrator: Whenever V_2 is not zero, a current must flow through the resistor R_i since V_- is at virtual ground. This current must subsequently flow through the capacitor and eventually be sunk by the op-amp. Therefore, the current sinking capability of the op-amp determines the lower limit of the resistor R_i. From the specification sheets of the LF411, it is clear that the current sinking capability at room temperature is 25mA. It is then evident that the lower limit on the resistor must be about 500Ω. Of course, if R_i is made too large, the current through it will be very small, and the input current offset error can become significant. This sets the upper limit of R_i. Since the input current offset error for an LF411 is only 50pA, the upper limit is set to more than 2.5GΩ. A third issue needs to be considered when picking the component values for the integrator: The 2N3972 across the integrating capacitor will inevitably have some on-state resistance. When the switch is shorted, this results in an RC time constant delay before the switch is actually shorted. Consequently, if C_i is very large, the closing of the switch will not seem instantaneous. However, C_i cannot be made arbitrarily small: The 2N3972 has a parasitic capacitance of 25pF, which means that when the JFET is turned off over 15V all the charge in the parasitic capacitance

Parameter	Value
N_2	1
R_i	3.3kΩ
C_i	4nF

Table 5.6: Summary of the design parameters for the second winding approach.

will end up on the integrating capacitor. This will lead to a spike in the current measurement. Then, as was argued in the Rogowski coil case, C_i must be larger than 2.5nF. After having paid due attention to these constraints, the values selected were $R_i = 3.3k\Omega$ and $C_i = 4nF$. The design parameters for the second winding approach are summarized in Table 5.6.

In order to examine the effects of loading, the influence of the winding resistance, and the leakage inductance in this case, a number of measurements were made. The winding resistance R_{wind} was found to be 0.5Ω. This does not contribute significantly to the overall error. The leakage inductance was also measured not to contribute significantly to the overall error. Also, loading was not significant, due to the high value of the integrating resistor.

The lower limit of the bandwidth for this scheme is dictated by the offset voltage. As was the case for the Rogowski coil, the lower limit is about 1kHz. The upper limit is now dictated by the performance of the inductor core. This core will behave properly up to about 100kHz, which sets the upper limit.

The worst case error contribution is the sum of all the individual errors. There would be 0.5% contribution from the offset voltage, 0.5% from the parasitic capacitance of the 2N3972, 1% from the integrating resistor, and 10% from the integrating capacitor. The core was specified within 4%. This results in a worst case error of 16%.

5.6.3 Testing the Second Winding Approach

The second winding approach was tested under the same conditions as the Hall-effect sensor. Measurements for low and high current levels as well as switching

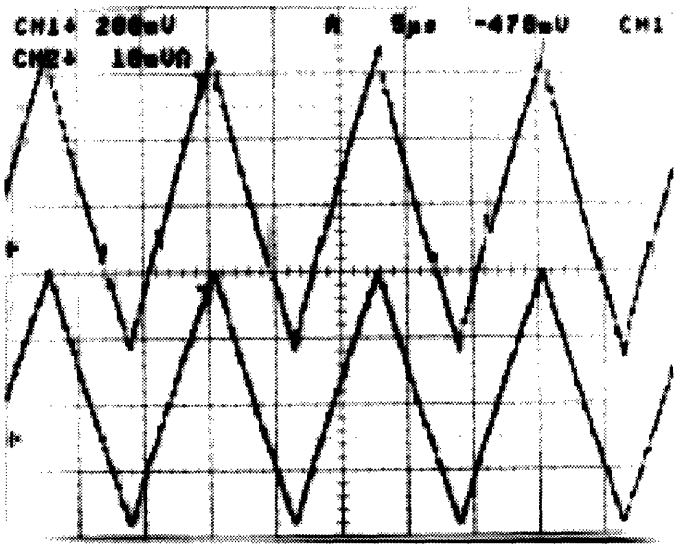


Figure 5-24: Output waveform for second winding sensor (top waveform) as compared to a current probe measurement (bottom waveform). The setting is 2A/div, and the switching frequency 80kHz.

frequencies were made to verify that the design works in the specified operation region. The picture displayed in Fig. 5-24 shows the second winding method measuring currents switching at 80kHz (at 2A/div). The top waveform is the output of the integrator, while the bottom waveform was measured by means of a current probe. From Fig. 5-24 it is evident that the method works qualitatively, but the second winding measurement is larger than the current probe measurement. In order to find out how big the error is, two more measurements were made. The first, shown in Fig. 5-26, measures low currents at high switching frequencies. The scale is set to 2A/div, and it is clear that the second winding output indeed is above the current probe measurement. The error amounts to about 12%. The second measurement was made at a low switching frequency and a high current level, as displayed in Fig. 5-25. The oscilloscope is set to display 5A/div and the switching frequency is 14kHz. Again, the top waveform is the output of the second winding integrator, and the bottom waveform is the current as measured by a current probe. The error was measured to be about 12%. This implies that the offset error never comes into play: If the offset error of the integrator was significant, the error would be larger for measurements

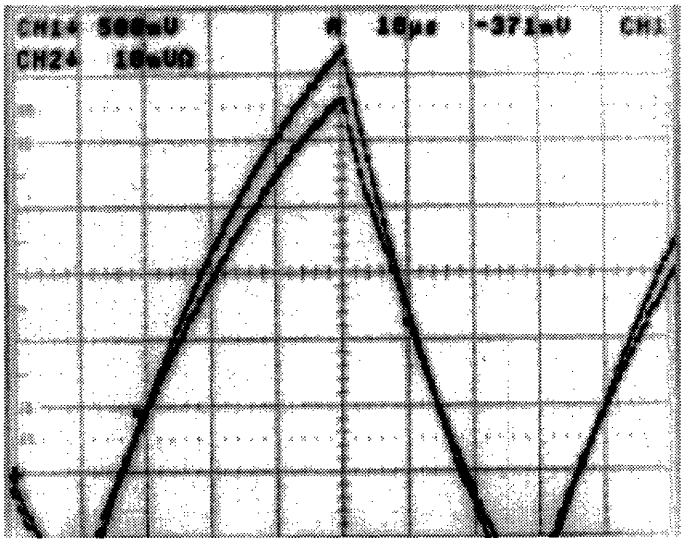


Figure 5-25: Output waveform for second winding sensor (upper waveform) as compared to a current probe measurement (lower waveform) at a low current level. The setting is 1A/div and the switching frequency is 60kHz.

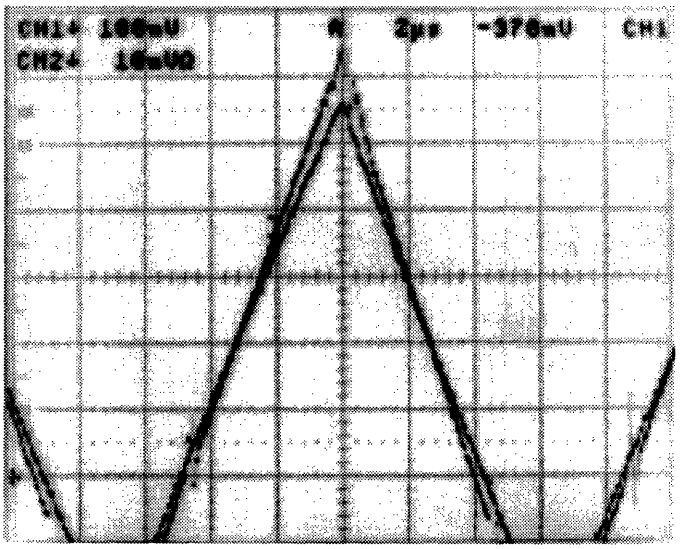


Figure 5-26: Output waveform for second winding sensor (upper waveform) as compared to a current probe measurement (lower waveform) at a high current level. The setting is 5A/div and the switching frequency is 14kHz.

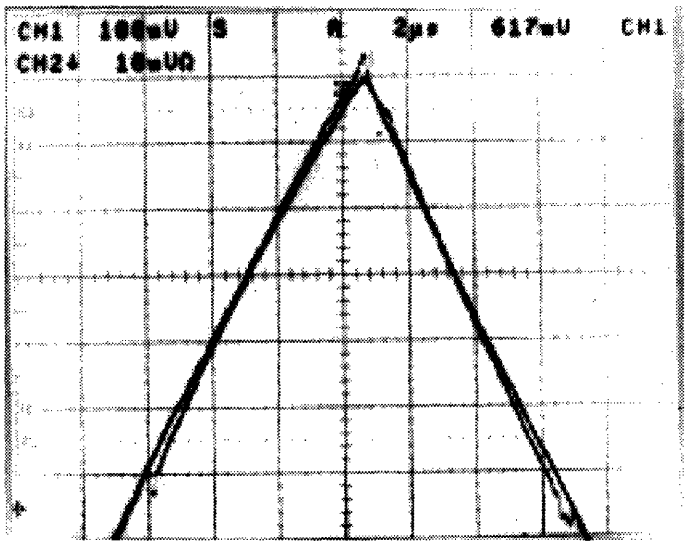


Figure 5-27: Output waveform for second winding sensor (upper waveform) as compared to a current probe measurement (lower waveform) at a low current level after the inductance of the output inductor has been adjusted. The setting is 1A/div and the switching frequency is 50kHz.

at lower switching frequencies. However, since the error remains constant over the operating range of current levels as well as switching frequencies, the error must be a scaling error. Upon examining the system in closer detail, it was noticed that the output inductor was actually 33μH instead of the 30μH that had been supposed. This in itself makes up for 10% of the error, an error that could be alleviated by changing the number of turns on the inductor, or by changing the RC-time constant slightly.

In an attempt to reduce the error in the measurement, a winding was removed from the inductor, effectively reducing its inductance from 33μH to 29.8μH. The current measurements made at the extremes of the operating region were then repeated, and are displayed in Fig. 5-27 and Fig. 5-28. Figure 5-27 shows the case where the current level is low, and the switching frequency high, and Fig. 5-28 shows the case where the current level is high, and the switching frequency is low. The error is both cases is now undiscernible.

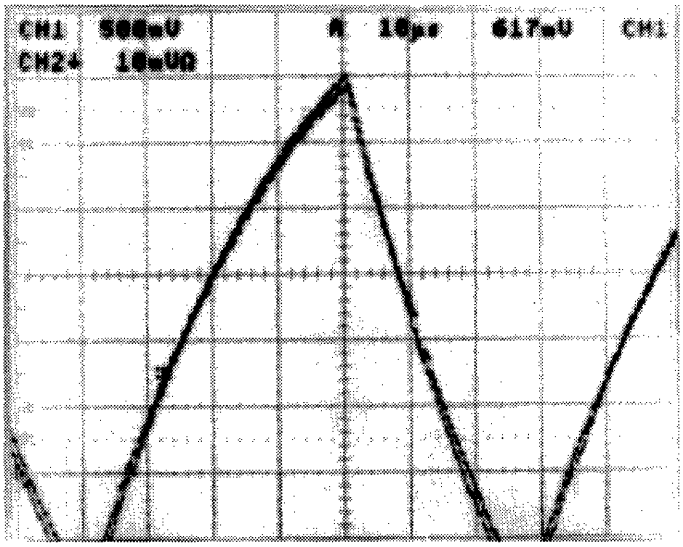


Figure 5-28: Output waveform for second winding sensor (upper waveform) as compared to a current probe measurement (lower waveform) at a high current level after the inductance of the output inductor has been adjusted. The setting is 5A/div and the switching frequency is 14.9kHz.

5.6.4 Conclusion

Perhaps the biggest drawback of the second winding approach became evident as a result of the experiments above. The magnitude of the sensed current is directly proportional to the inductance of the output inductor. This inductance is not very well specified, and varies from core to core, as well as with frequency and temperature. The experiments above shows that the second winding can be made to work properly, but the method is clearly not conducive to mass production. Another drawback of the second winding is that it requires a resetting signal for its integrator, which in turn requires a zero voltage detection scheme. In this particular application, the zero voltage detection scheme is already available since it is required to ensure the zero voltage switching condition of the RPI, but this might not be true in the general case. The second winding approach is therefore not recommended as a suitable replacement for the Hall-effect sensor.

A summary of the findings for the second winding is shown in Table 5.7. The worst case error is the sum of all individual errors that were considered. The measured error

Worst Case Error:	16%
Measured Error:	12%
Bandwidth:	1-100kHz
Cost:	Very Low

Table 5.7: Summary of the findings for the second winding.

is the maximum error displayed during the experiments performed above. The lower limit of the bandwidth is in this case dictated by the offset voltage. The upper limit of the bandwidth is limited by the frequency performance of the core. The cost is the estimated cost of an entire second winding current sensing system as compared to a Hall-effect sensor.

5.7 Conclusion

Out of the five current sensing systems evaluated here, the Hall-effect sensor, the current transformer, the Rogowski coil, and the second winding approach measured current successfully. The fifth system, resistive current sensing, was deemed inappropriate for this particular area of application due to the high current levels and the high $\frac{di}{dt}$ of the RPI output current.

The Hall-effect sensor is the most accurate system tested, and for this reason it was also made the benchmark of the current sensing tests. It's prohibitively high cost, however, makes it a poor candidate for the current sensing system in a PRPI. The second winding approach, albeit conceptually very pleasing, is too sensitive to variations in the inductor core parameters, which was verified in the experiments on that system. The choice then falls on either the Rogowski coil or the current transformer. Both these systems measure current accurately, but based on the worst case error estimate, the current transformer emerges as a clear victor. In addition, the Rogowski coil has the added disadvantage of the resetting signal. There are also more components, as well as more connections required to make this system work, which will reduce reliability. The current transformer is accurate, small, simple, inexpensive,

reliable, and manufacturable. It is therefore the recommendation of this thesis that the current transformer, in one form or another, should be implemented as the current sensing system in a parallel resonant pole inverter architecture.

Chapter 6

Conclusion and Recommendations for Future Work

The parallel resonant pole inverter architecture possesses all the positive attributes of a soft switched inverter topology, while alleviating some of the drawbacks of, for example, the resonant pole inverter. The disadvantage of the PRPI is that current sensing and control system implementations might become prohibitively expensive. This work, however, has shown that it is possible to construct inexpensive, yet reliable current sensing as well as control systems. Out of the five different current sensing schemes evaluated, the current transformer came out as the best candidate for the current sensing in a PRPI system, based on cost, bandwidth, and accuracy.

The next step in the design process is to improve the control sensing system so that it can incorporate closed loop control. It will be necessary to sense the output voltage and feed it back. The current sensing techniques can be further refined, and the designer should attempt to optimize the manufacturability of the current transformer, in order to make the PRPI system economically feasible.

Appendix A

Inverter Module Description for the Testing of the Control System

The inverter module used in this part of the project was designed by David Perreault and Dave Otten in LEES at MIT. A block diagram representing one bridge leg of this module is shown in fig. A-1. The implementations of the different blocks can be seen in fig. A-2. The basic idea is simple: when the top MOSFET is off and the bottom MOSFET is on, the output will be low. Similarly, when the top MOSFET is on and the bottom one off, the output will be high. The purpose of the rest of the circuit is to ensure that switching occurs at the desired times, and to incorporate some safety features.

The Gate Drive block is implemented by two MOSFETs in a push-pull configuration. It is this stage that provides most of the current gain necessary to drive the power MOSFETs in the output stage. It is worth noting that the top Gate Drive is referenced to v_o and not to ground.

The Gate Drive Logic blocks are implemented using inverting Schmitt triggers. The Schmitt triggers are used for noise immunity, and are paralleled in order to provide some additional current gain.

The High Side Power Supply is implemented by a clamping capacitor and a high-speed diode. The diode allows the power supply capacitor to recharge when v_o is low, and lets the power supply float with the output when v_o is larger than zero.

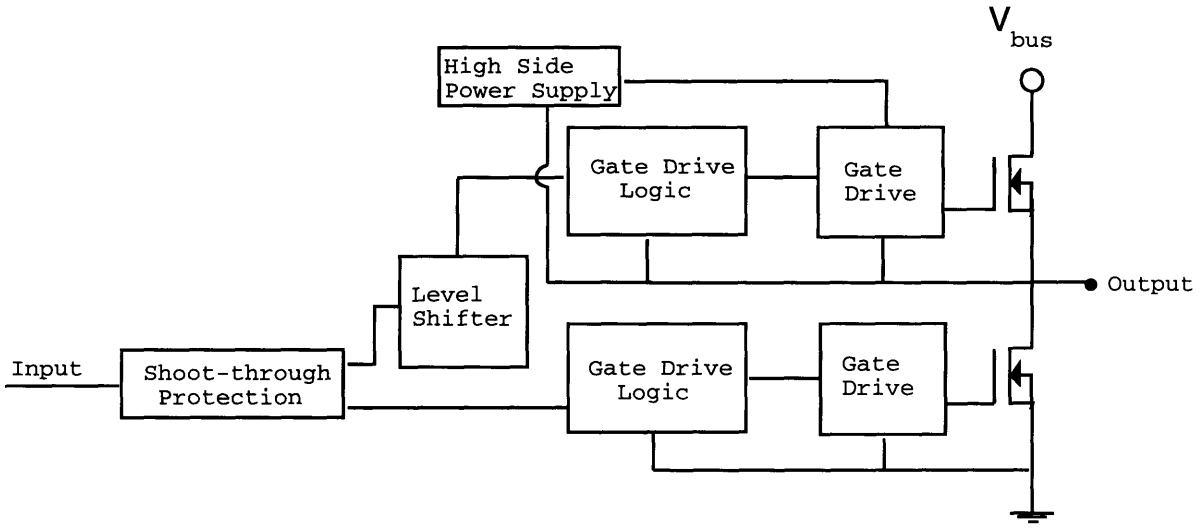


Figure A-1: Block diagram of inverter leg

The Level Shifter translates signals referenced to ground to a v_o reference for the high side gate drive. It is implemented by means of a MOSFET, Q_{LS}, and a diode, D_{LS}, as shown in fig. A-2. When the MOSFET is turned on, the diode is forward biased, thus effectively pulling the input to the high side gate drive logic low. When Q_{LS} is turned off, the input to the gate drive logic is pulled high through R_1 and R_2.

Shoot-through protection is included to insure that the two power MOSFETs are never turned on at the same time, since this would short out the voltage bus. The protection is implemented by means of a diode and an RC-filter. This configuration creates a delay between the time one power MOSFET turns off, and the time the other turns on. The time delay can be regulated by changing the RC time constant.

Some components that were included in the construction of the inverter are not shown in fig. A-2. A large capacitor was put across the bus in order to clamp the bus voltage. The output is fed to a Hall-effect current sensor so that the output current, i_o, can be monitored. Also, a level-shifter was connected to the input from the control system to convert 5V logic level signals to the 15 V levels required by the Schmitt triggers.

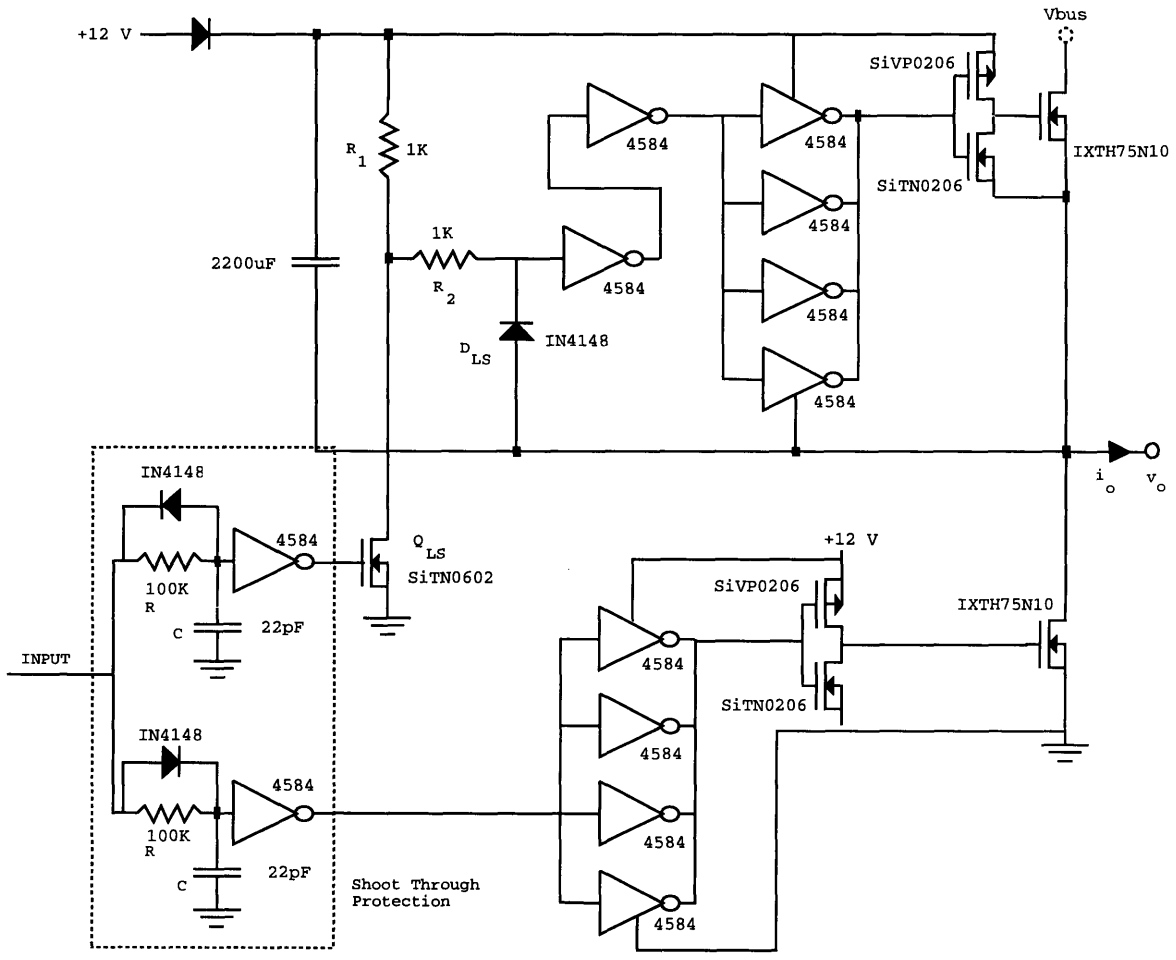


Figure A-2: Bridge leg of inverter

Appendix B

The Emulated Zero Voltage Crossing Detection

The zero voltage crossing detection scheme used for the RPI was described in chapter 4. However, while developing the current sensing systems described in chapter 5, the RPI was still under construction. Therefore, the zero voltage signals were not available for the current sensing experiments, and had to be emulated. The emulation is shown in Fig. B-1.

The input i_k is the fedback current from the Hall-effect sensor. Whenever i_k is within a delta limit of zero, the integrator can be reset. The reset signal is active low and is displayed in Fig. B-2.

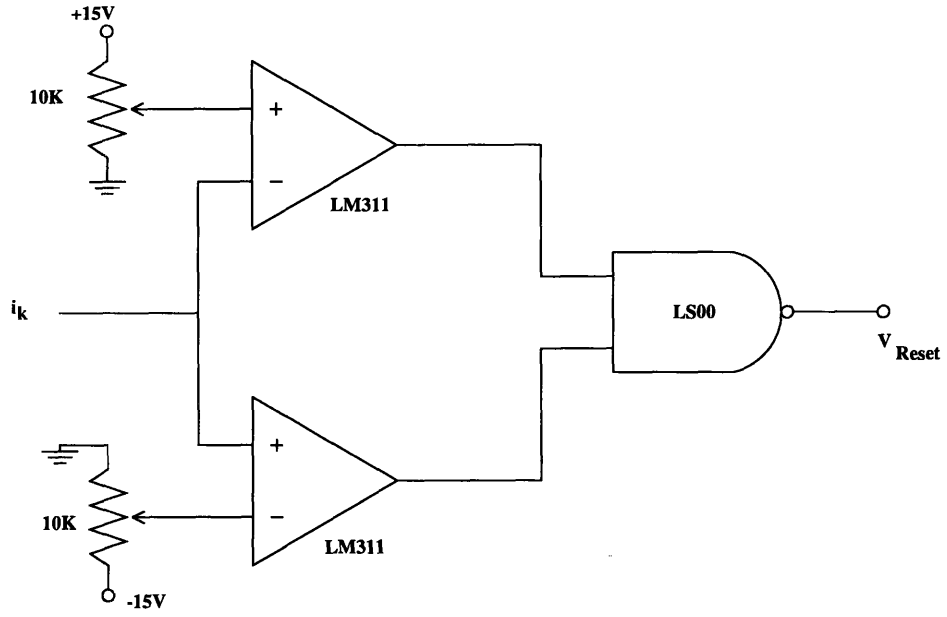


Figure B-1: The emulation of zero crossing detection signals

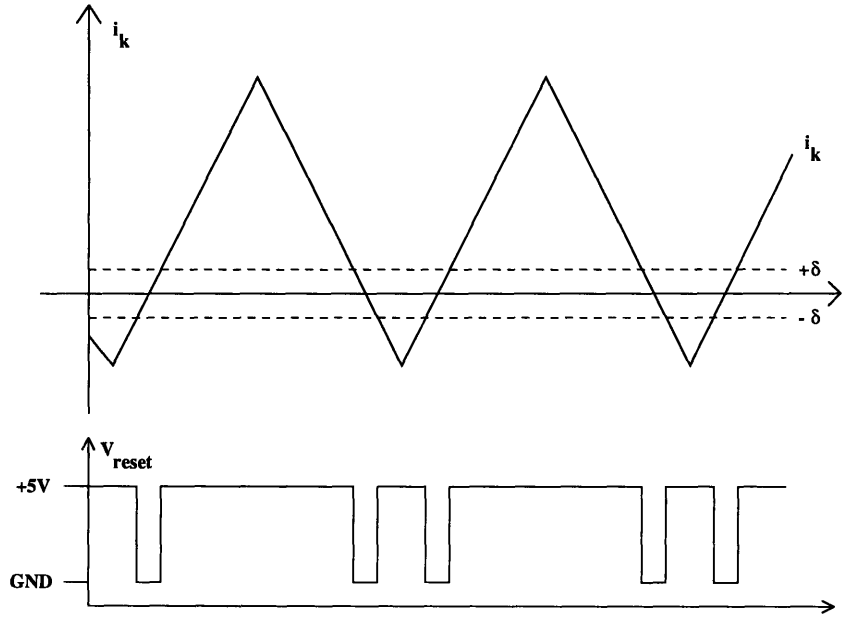


Figure B-2: Input and output waveforms for zero voltage detection emulation

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