Technology and Market Analysis of Standard Electronic Photonic Package

by

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ABSTRACT

Electronic industry will suffer a major turn around in the near future. The current infrastructure will no longer be able to support the increasing data rates. All the disadvantages of copper as current legacy are amplified with the level of bandwidth we are going to experience soon. On the other hand, photonic industry is in the need of finding a new demand source to be able to bring back the state of industry to the "boom" era. With both conditions in mind, it is likely for photonic and electronic industry to emerge. However, the platform for the collaboration has not been mature enough. One of the biggest problems in the photonic industry is the high cost of the package. This, so far, has been one of the major issues holding the industry from gaining back to its golden era. In order to overcome this barrier, standardization has been suggested to be implemented in the industry.

This thesis examines the current state of optoelectronic industry, as a convergence of photonic and electronic industry. More specifically, the condition of lack of standardization is analyzed and proven to be the case. Interviewing relevant industry players and working closely with the MIT Communications Technology Roadmap-Integration, Packaging and Interconnects Technical Working Group also determine the reason of the condition. Finally, suggestions on the need of standard package and the requirement of standard package are made to hopefully direct the research towards more focused area.

For the standard to be the ultimate standard, industry wide implementation has to be the resulting condition. This thesis also examines and suggests steps needed to be taken in order to promote the full implementation of the standard package.

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Title: Thomas Lord Professor of Materials Science and Engineering

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Chapter One: An Introduction

1 *Fiber will displace copper*

Communication technologies are becoming more and more important each day. Not only that they are becoming the backbone of United States industry, the domestic appliances that drive the daily life of people are driven by these technologies. People are getting more longing than ever for a link to the world's information sources. This expansion of communication channels usage demands higher bandwidth and higher reliability. Higher bandwidth implies higher data capacity. They have driven the usage of optical interconnect in the "long-reach" level. Nowadays, these optical connections are already made commercially available in computer-to-computer level. However, since the demand for higher bandwidth keeps on increasing, we must give attention to inside the computer and try to make a significant improvement on the bandwidth there.

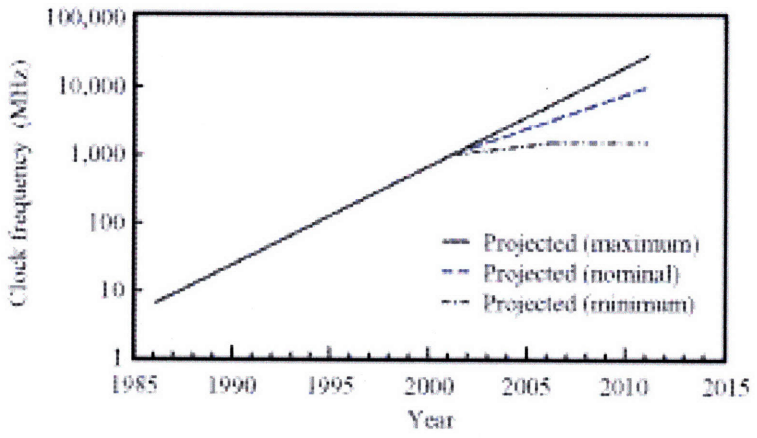


Figure 1 Moore's Law on clock frequency. It was predicted and proven to be the case that the clock frequency is doubling every 18 months.

The above figure shows the Moore's Law plots on the clock frequency. Moore's Law predicted that the clock frequency will be doubled every 18 months, and it has been

the industry's challenge to introduce the technologies that are able to allow this law to occur. So far that is what has happened until the last introduction of copper as the interconnect material on the chip. Seeing to the future, the question is now whether using copper is enough for maintaining the growth predicted by Moore's Law.

Unfortunately, there are several arguments that copper interconnection would not be able to scale to higher bandwidth. Electronic connections, copper in this case, are getting more and more reach-limited as data rates get higher. The 10 Gb/s line threshold is soon going to be passed. Physical limitations; such as distortion from dispersion, signal attenuation and crosstalk; are becoming more prevalent at this high speed.[1] Thus, optical interconnects are starting to show their cutting edges at this higher data rates.

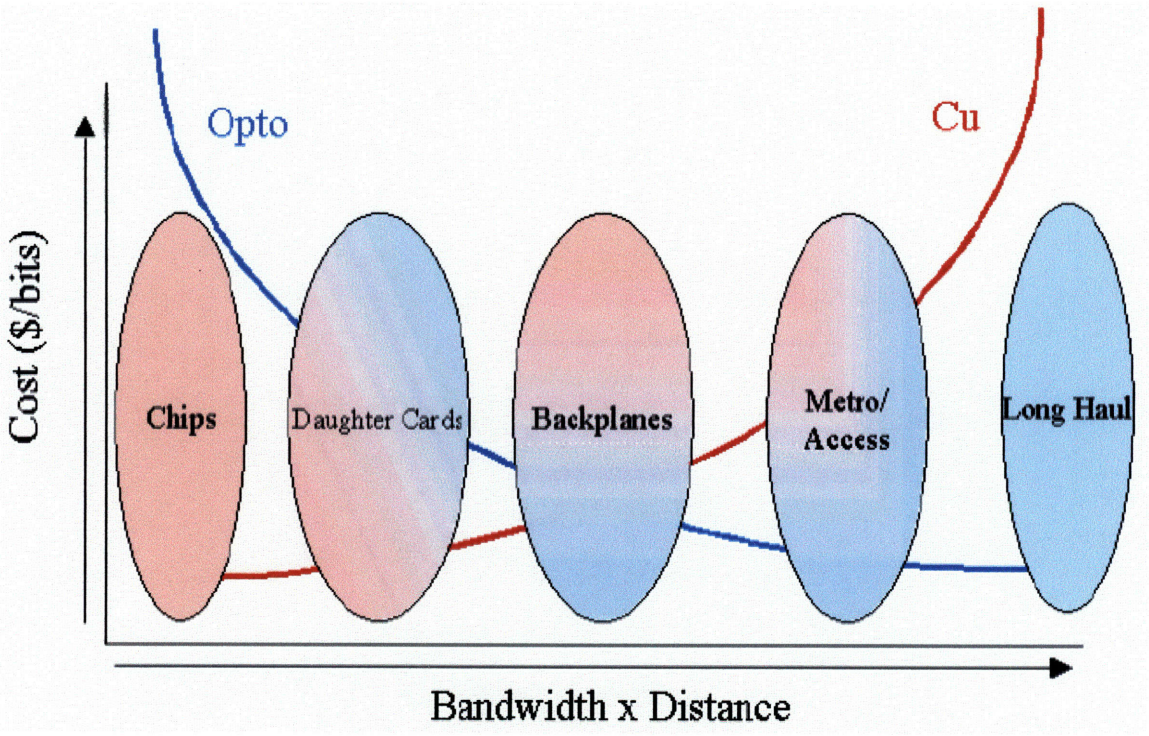


Figure 2 Copper vs. Opto (Optical) in terms of Bandwidth x distance and cost/bits.[2] The cost of optical interconnects are decreasing with increasing bandwidth vs. distance, while the cost of copper interconnects are increasing with increasing bandwidth vs. distance.

So far, it is always the figure above that prevents optical, in this case fiber, from going into the chip level and replace copper. It is simply not cost effective to use it.

However, due to those limitations stated above, we could not afford to use copper in supporting the bandwidth demand. Higher bandwidth in the chip level shift the bandwidth x distance to the right and it means that it is more and more advantageous to use fiber than copper.

The resistance of changing copper also lies on the assumption that copper is a "legacy infrastructure". People think that copper is already so established that changing copper is not an option. However, this phrase is somehow misleading. Only a small fraction of the existing 1G (equivalent to the speed of 1 Gb/s) copper cable infrastructure will support any 10G standard. Thus, nearly all 1G copper media will need to be ripped out and replaced for 10G. Standard copper cabling, Cat 5e, is definitely not suitable for 10G. Only Cat A6 unshielded twisted pair (UTP) and Cat 7 shielded twisted pair (STP) are the copper media capable of 10G, yet they have no outlook above 10G.[3] Therefore, the question now is not whether optical interconnects will replace copper for shorter links, but when the transition will occur. However, beyond interconnection, in areas such as Fast Fourier transform, combined electronic-photonic signal processing is beginning to show value. Thus, the future will not so much on the replacement of electronics by photonics, but it will be on the partitioning of function that will continue to develop as designers become more skilled in the art.[4]

Fiber offers several indisputable advantages over copper. The following bullet points give some of its advantages.[3]

- Optical signals traveling through single mode optical fiber suffer very little attenuation since the fiber absorbs light only weakly. The absorption loss is noted at around 0.25dB/km and it is independent of data rate. On the other hand, electrical connection dissipates energy by radiating the signal away into space. These losses increase drastically as the data rate increases.
- Dispersion is negligible in fiber over distances of a couple of kilometers. In copper, each pulse typically overlaps neighboring bits after only a few meters in 10G transmission systems.

- Fiber optic signals are not affected by electromagnetic interference nor do they generate electromagnetic interference. Electrical signals, on the other hand, are highly susceptible to electro magnetic interference, especially the noise from adjacent wire pairs within one cable (crosstalk) or from neighboring cables (alien crosstalk). The need to mitigate alien crosstalk will in some cases limit bundling of copper cables in cable trays and conduits.
- Longer reach and higher bandwidth are obvious for fiber optics compared to copper. Future scalability beyond 1T through the process of dense wavelength division multiplexing (DWDM) gives more cutting edges for fiber, since copper media will need to be upgraded just to support 20G or 40G, and no practical copper media are likely ever to support 100G.
- Lower media cost, smaller size and lower weight, easier cable management and robustness are another advantages that move fiber ahead of copper in terms of interconnection.

In addition to the advantages listed above, which are true for any set of design choices, fiber acquires several additional advantages over copper at data rates of 10G and higher. In electrical connections, compensating for higher signal attenuation, dispersion and crosstalk at 10G results in much more sophisticated analog and digital signal processing than is necessary at 1G. This additional circuitry creates several further advantages for fiber optic solutions. Optical transceivers add just a few nanoseconds of latency, which is a negligible contribution to the total link latency. However, 10G electrical links incur a very long latency (1-3μs). This is because of the delay involved in data encoding, signal processing, and the extensive forward error correction required in achieving acceptable bit error rate. The speed of light in the fiber is larger than the speed of electron in the copper. That fact, combined with the earlier advantages of fiber over copper, which are low attenuation and lower dispersion, help fiber in obtaining a comparatively very low latency over copper. Fiber will also require lower power consumption. Optical transceivers consuming less than 2W can transmit signals across links as long as 10 km. 10G transceivers for copper links will likely require at least 10W per port, possibly 15W or higher, to

achieve only 100 m reach. Finally, the very high thermal dissipation of 10G transceivers for copper links will limit their density on the edge of a port card. This added thermal load will also increase the space required between equipment in switch closets and data centers.[3]

These advantages of fiber over copper in cabling have clearly put fiber as the winner in terms of performances. And now one has to see whether those same advantages as we scale to short level of interconnection.

The figure below illustrates the hierarchy of the interconnection. In today's world, optical connections between individual computers are commercially available. It is expected in 2 to 5 years for the optical interconnections to shift to board-to-board, 5 to 10 years to chip to chip and 15 years to subsystems within a chip eventhough it is still open for discussions.

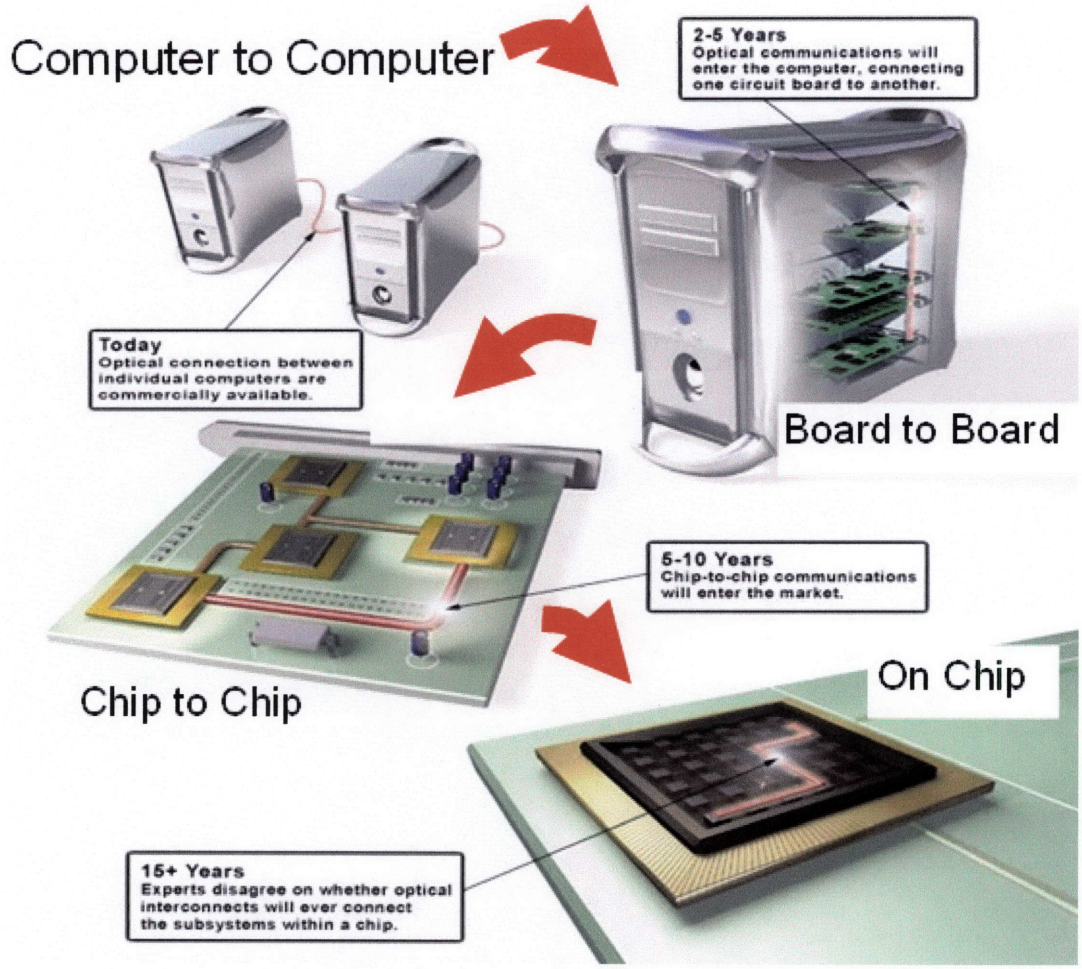


Figure 3 Electronic photonic interconnection hierarchies. With the existence of optical interconnection between computers today, it is predicted that within the next 2 to 5 years it will enter computer, within the next 5 to 10 years it will penetrate board or chip-to-chip level, and within more than 15 years of time it will go onto the chip level.

One factor that is historically very significant and also the driving factor for industry is the cost. Luxtera Inc. [3] has made an analysis which resulted in the conclusion that the total cost of ownership of fiber network is lower than copper, independent of the specific network assumptions for data rate 10 Gb/s or higher. This condition applies for the same distance vs. bandwidth condition for fiber and copper. This cost includes transceivers, media, installation, electronics, building infrastructure, maintenance, and service life cost. One factor that has not been covered thus if we want to progress toward the hierarchy shown in figure above is packaging factor.

Packaging is a very significant factor especially in the optoelectronic industry. A study by Sergiusz Patela [5] has shown the comparison of cost structure in the electronic and optoelectronic devices. It is shown in the figure below that for electronic devices, 90 percent of the cost is the wafer processing cost while only 10 percent of it comes from packaging. In the optoelectronic devices, however, the reverse is true. Optoelectronic device cost is only responsible for the 20 percent of the total cost while the majority of the cost, 80 percent, lies on the packaging cost. This implies that improvement on the packaging of optoelectronic device that reduces the cost significantly is desirable.

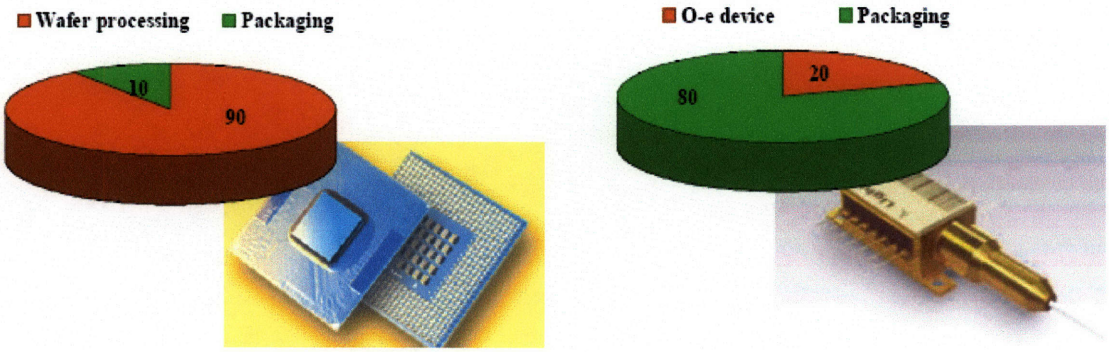


Figure 4 Electronic vs. Optoelectronic cost structure comparison. In electronics, 90 percents of the cost come from the wafer processing and 10 percents of the cost come from the packaging. In optoelectronic, however, only 20 percents of the cost come from optoelectronic device and 80 percents come from the packaging.

Another good illustration on the high cost of optoelectronic package is shown in the following figure. It is shown that for 2 dollars IC, around 22 dollars are spent on the packaging and interconnection. This is somehow too expensive and it will be excellent to have this high package cost reduced.

Silicon Technical Working Group in Communications Technology Roadmap I have identified the reason of this high packaging cost.[6] They mentioned that in today's state-of-the-art commercial optical links, it does not have sufficient volume for it to have a low cost structure. High-level drivers will increase pressure for monolithic integration, which will further lowering the cost and increase the volume. This infrastructure does not appear to exist today. Jeff Swift from Analog Devices also

acknowledged this missing infrastructure in his talk on the Communication Technology Roadmap meeting on May 2005.[7]

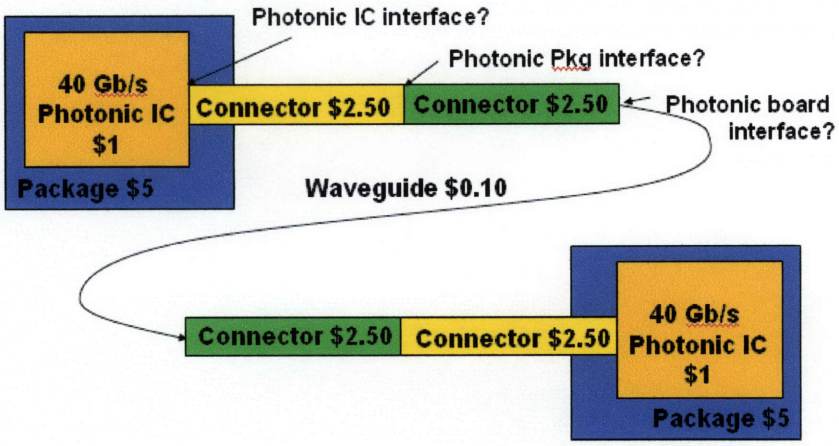


Figure 5 Illustration on optoelectronic cost on each component. For a 2 dollars IC, we need to spend around 22 dollars for packaging and interconnection.[7]

2 *Overview of Optoelectronic industry*

During the middle to late 1990s, the telecommunication industry was booming. Plenty of investments to build new networks and infrastructure were available. Suppliers had numerous businesses and very little competition was experienced. Each firm developed and marketed its own brand with the corresponding optical equipment. This is what they called as telecom bubble. Investment boom in the industry due to promise of massive growth in broadband demand. The end result was an industry fragmented and disorganized. Each customers would be equipped with optical components from different vendors.[1]

However, between the years of 2000 and 2002 following the burst of the bubble, the optoelectronics industry suffered a major decline in revenues. The Total Addressable Market (TAM) was approximately $2 billion USD in 2003 and $2.5 billion USD in 2004. Whereas the addressable market is significant, it pales in comparison to its former size of $10.7 billion USD in 2000.[6] The investment obtained during the bubble years have made the manufacturing capacity built much greater than what was

actually needed and over capacity is now threatening. The result was that optoelectronics manufacturing industry was left with too much to sell and nobody to buy.[1] The economies of scale were lost and the industry players felt major decline in revenues. However, during 2004 the market rebounded strongly and although some sectors experienced a slowdown in the final months of the year, the industry went through beyond the forecast to show strong and sustained growth. That being said, it sill faces many challenges. Major changes in both technology and marketplace occur as frequently as ever. Overall, the marketplace is experiencing the effects of global positioning by major corporations. At the same time it has seen the attrition of older names and formation of new start-ups. Companies are stepping up their operations through mergers, acquisitions and investment. Another interesting development is the emergence of China as an important market for the manufacture and use of opto and other components.[8]

With all that stated above, the main challenge is now on how to drive the volume up again and introduce back the economies of scale to the industry players, which then will advance the health of the optoelectronic industry.

3 *Statement of Objective and Scope*

This report will analyze the reason on the high cost of the optoelectronic package, the current state of the optoelectronic packaging industry as well as introducing standard package requirement and suggestions to be used in the optoelectronic industry based on the analysis. Respective business model will also be recommended to be taken into action. According to figure 2, the main focus in this report will be on the interchip or chip-to-chip level.

Chapter Two: Analysis

1 *Finding root causes*

In the search of the reason for the high package cost as described in the earlier section, systematic fishbone diagram introduced by Ishikawa[9] has been used. The following figure shows schematically the fishbone diagram of the specified problem.

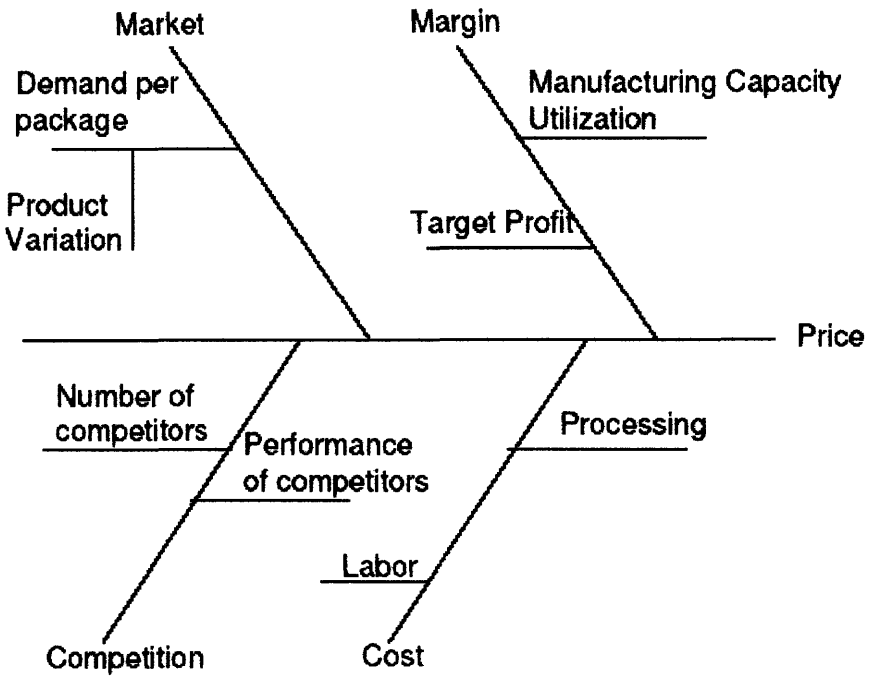


Figure 6 Ishikawa fishbone diagram. Price of package is affected by margin, cost, market and competition.

The figure above illustrates the factors contributing to price. They are margin, cost, market, and competition. High price can come from high cost, which consists of labor cost and processing cost. The processing of the optoelectronic package, which will be discussed later, is much more complex compared to electronic package, especially in the alignment and thermal management. Alignment is a very critical step in the

optoelectronic processing and some of the process is extremely expensive. In terms of labor cost, high labor cost might be resulted from the less-automated type of process. Therefore, the type of labors needed requires higher salary and the number of labors needed is higher as well. High price could come from high margin as well, which is driven by the manufacturing capacity utilization and target profit. Another factor is market. High product variation will give low demand per package and therefore the price could go up for the company to bear with the cost. Competition is another factor illustrated here as the factor attributing to the price. High number of competitors and performance of competitors' product could affect the pricing of the OE device by the industry.

From above breakdown, the most essential causes for the price have been determined to be complexity of optoelectronic processing steps and high product variation. The first cause could be concluded from the cost factor of the price, while the later could be concluded from the market, margin, and competition factors. Questionnaire has been set up to be sent out to the industry and get their response. Copy of the questionnaire is attached on appendix I. In the process of building this questionnaire, five significant variables are taken for the industry. They are industry revenue, average cost per bit, number of types of products, manufacturing capacity as well as manufacturing capacity utilization.

High product variation case can be shown by some characteristics such as high number of types of products, low demand, low manufacturing capacity utilization and high margin. Likewise, for complexity of optoelectronic processing steps, it is shown by advanced dedicated process, utilized manufacturing capacity, low margin because the actual cost is already high and adequate demand.

The response from the industry will be shown in the later chapters according to the topics discussed by each chapter.

2 Why standardization is an answer

System Dynamics is used to perform the analysis to come out with the solution for both excessive type of package and difficult processing steps case. It is a method proven to be useful in analyzing various market environments that was developed by faculty at the MIT Sloan School of Management. It has been a part of numerous decision making processes in companies such as GM, the Department of Energy, the Department of Defense, foreign governments, and many others. The diagram used in the following analysis is obtained by taking an analogy to the transceiver analysis on Michael Speerschneider's thesis.[1]

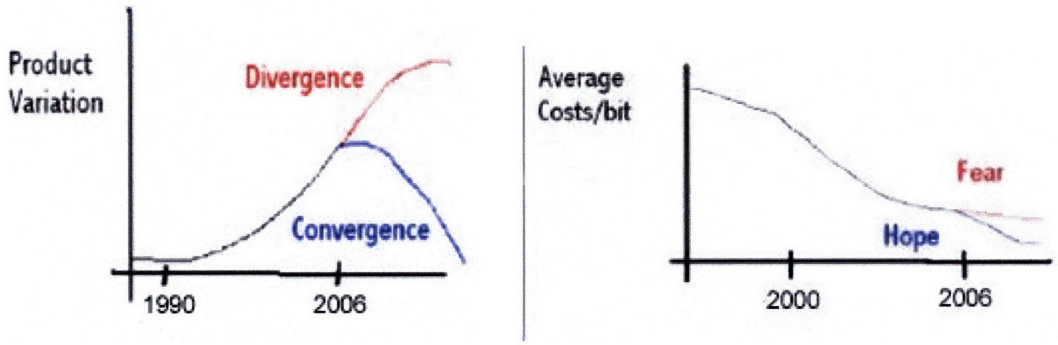


Figure 7 Condition and concerns of industry on product variation and average costs per bit. This is said to be the reference mode of further analysis to determine the needs of standardization for the package. Product variation grew during the "boom" years and continues to grow despite the market crash. Cost per bit has decreased more quickly since the crash.

It might be useful to take a look into the condition and concerns of the industry, as can be shown on the above figure. In terms of product variation, the industry has witnessed high rates of proliferation, and fears that it will continue for some time without taking some measures to control the divergence. It can be noticed that the product variation is increasing both during the bubble years and the crash (after 2000). This implies that there are multiple and independent forces driving proliferation. In terms of average cost per bit, the crash has made manufacturers redoubling their efforts to further reduce costs once they realized that demand was falling sharply. With the prospect of rapidly falling demand, the only way to make up the revenue in short term would be increasing margins by lower costs. However, the

fear is that the prices will not drop low enough to allow more serious competition and thus create greater volumes. Following this, causal loop diagram has been made to analyze each condition, high product variation and complexity of optoelectronic processing steps, and we shall see that standardization could be the solution for both cases.

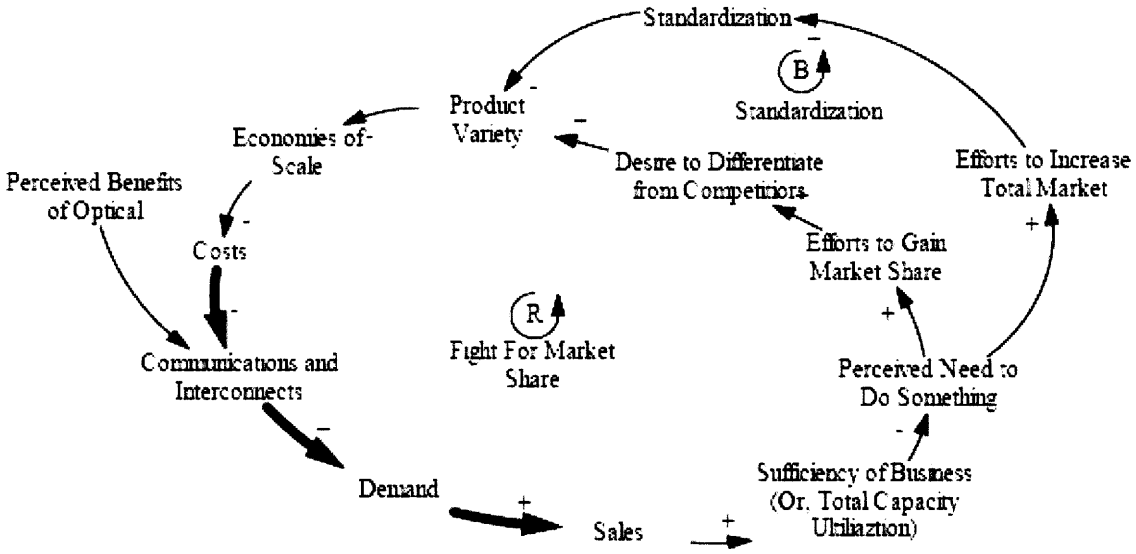


Figure 8 Causal loop diagram on product variation hypothesis. The higher the capacity utilization, there is less perceived need to do something, which will lead to increase in product variety. The standardization loop, however, will try to reduce the product variety.

When the reason is high product variation, the above loop diagram is used for analysis. The root of any drive to improve the industry comes from capacity utilization. Other factors can provide motivation for action, but generally speaking, if capacity utilization is high, there is less force on the manufacturers.

This loop contends that when capacity utilization is high, there is a little perceived need to do something. In this case, corresponding to the bubble years, there is a low drive to differentiate to secure market share, thereby weakening the "Fight For Market Share" loop. However, there is no driving force to increase the total market through standardization. The "Standardization" loop is short-circuited during periods of high capacity utilization. The differentiation loop wins by default. Essentially, it costs more to organize the industry and plan a path to standardization than it does to

simply continue to trying to produce a superior product, particularly when there is little cause to out-compete when there is plenty of business to go around. The crash resulted in a drop in capacity utilization, and the "Standardization" loop is now more active, as evidenced by the MSAs (Multi Source Agreements) and the formation of efforts such as the MIT CTR.[1] However, thus far the "Fight For Market Share Loop" has dominated and differentiation continues. It is, however, obvious that standardization will bring the product variety down which will increase the economies of scale and reduce the costs.

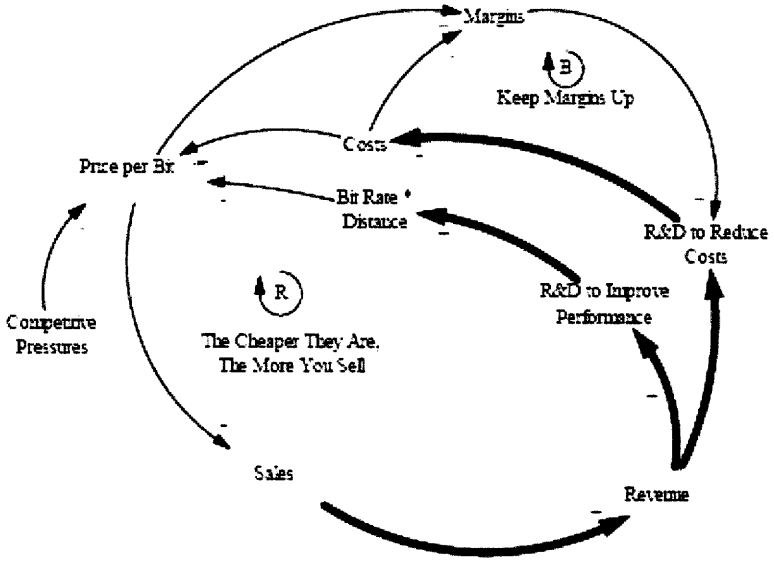


Figure 9 Causal loop diagram on cost hypothesis. Standardization will increase the R&D fund available to improve performance since it is now more focused. This will eventually reduce the costs and the price.

If the reason is processing complexity, above figure is used in the analysis. Before the crash and during the bubble years, the reinforcing loop entitled "The Cheaper They Are, The More You Sell" drove R&D investment and resulted in lower costs. After the crash, the "The Cheaper They Are, The More You Sell" loop worked in reverse and may have caused an increase in costs if not for the "Keep Margins Up" balancing loop proved stronger than the reinforcing loop, resulting in an acceleration of the costs reductions. Competitive price pressure then eroded the margins, forcing costs down more and more. The fear is that real costs savings cannot be achieved without a

fundamental shift in manufacturing processing including automation and active alignment. The investment needed for such an overhaul is unlikely to come with such poor prospects for significant volumes that would provide returns on the investment. The existing production techniques can only be improved so much. The hope is that volumes will materialize; prompting investment and costs will fall further. Standardization is also an answer in a way that it will increase the R&D fund to reduce cost for each package since the number of product variation is decreased. This will drive the cost down as well as the price.

From above analysis, it can be seen that standardization will do good in either way. Therefore, standard package is required to drive down the high optoelectronic package cost.

Another interesting concept came from Jerry Hausman, a McDonald Professor of Economics at MIT Department of Economics. In his talk at MIT Consortium Meeting at May 2005, he acknowledged that the optoelectronics industry serves broad number of applications which has led to industry fragmentation with a large number of firms and small shares.[10] The largest share seems only about 15% (Agilent and JDS Uniphase). The number of suppliers is much too large for a sustainable industry structure. The classic approaches of decreasing costs by economies of scale (the higher the production, the lower the cost) and learning by doing (greater experience in production leads to lower costs because of lower failure rate in production) are no longer enough.

The reason of the condition is that the large number of technical specifications makes reaching economies of scale difficult. The basic problem is that the component price is such a low overall share of total device (package and chip) cost that even a major cost and price reduction does not significantly increase demand. In other words, the elasticity of the demand is low such that even a 90% drop in price will have little effect. He then concluded that the telecom demand as a main target market for optoelectronics is not enough to support the optoelectronics industry as a whole.

Standardization will definitely help, but it is not enough. The demand curve must be shifted outwards; new demand sources for the industry are required. Information processing seems like a possible source of new demand, due to the opportunities stated in the previous sections. Therefore, it is important that the standard package could be applied to wider base of uses.

3 Package Introduction

In the later stages of this report, certain type of packages will be discussed and therefore basic knowledge of the design is needed for reader to understand the analysis fully. Therefore, in this section we will discuss the different types of package, namely Dual In-line Package (DIP), Ball Grid Array (BGA) and butterfly package.

Dual In-line Package (DIP)

Dual in-line package (DIP), or sometimes also called DIL package, is an electronic device package widely used in microelectronics with a rectangular housing and two parallel rows of electrical connecting pins, usually protruding from the longer sides of the package and bent downward. It may be used for integrated circuits or for arrays of discrete components such as resistors or toggle switches. It can be mounted on a printed circuit board either directly using through-hole technology, or using inexpensive sockets to allow for easy replacement of the device and to reduce the risk of overheat damage during soldering.

The most common DIPs have an inter-lead spacing, called lead pitch, of 0.1 inches and a row spacing of either 0.3 inches or 0.6 inches. Typical pin counts are 8 or any even number from 14 to 24 for 0.3 inches packages, and 24, 28, 32, or 40 for 0.6 inches packages. Some other standards, such as JEDEC, also specify less common packages with a row spacing of 0.4 inches or 0.9 inches with a pin-count of up to 64.

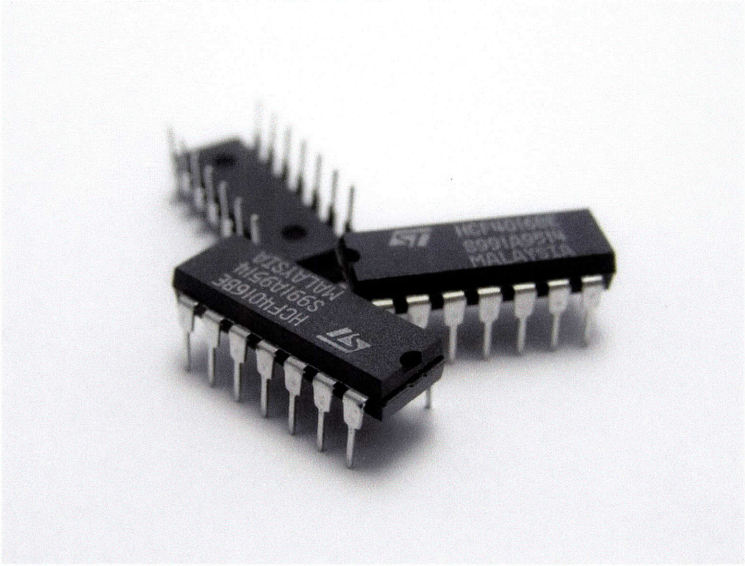


Figure 10 An example of Dual In-line Package (DIP). This particular one has seven leads on each side and therefore called DIP14.[11]

Several DIP variants exist, mostly distinguished by packaging material. They are named basically based on the main material used in the package. Ceramic Dual In-line Package (CERDIP), Plastic Dual In-line Package (PDIP) and Shrink Plastic Dual In-line Package (SPDIP), which is a shrink version of the PDIP with a 0.07 inches lead pitch, are examples of some variants.

DIPs were the mainstream of the microelectronics industry in the 1970s and 1980s. Their use has subsided in recent years, however, due to the emerging new surface-mount technology (SMT) packages.[12]

Ball Grid Array (BGA)

A ball grid array is a type of surface-mount packaging used for integrated circuits. It is descended from the pin grid array (PGA), which is a package with one face covered with pins in a grid pattern. These pins are used to conduct electrical signals from the integrated circuit to the PCB it is placed on. However, in the BGA, balls of solder stuck to the bottom of the package replace the pins. The device is then placed on a PCB that carries copper pads in a pattern that matches the solder balls. This assembly is then heated, causing the solder balls to melt. Surface tension causes the molten solder to hold the package in alignment with the circuit board, at the correct

separation distance, while the solder cools and solidifies. The composition of the solder alloy and the soldering temperature must be carefully chosen so that the solder does not completely melt, but stays semi-liquid, allowing each ball to stay separate from its neighbors.

BGA is often found as the solution to the problem of producing a miniature package for an integrated circuit with many hundreds of pins. PGA and DIL surface mount packages were being produced with more and more pins, and with decreasing spacing between the pins, but this was causing difficulties for the soldering process. As package pins got closer together, the danger of accidentally bridging adjacent pins with solder grew. BGAs do not have this problem, simply because the solder is factory-applied to the package in exactly the right amount.

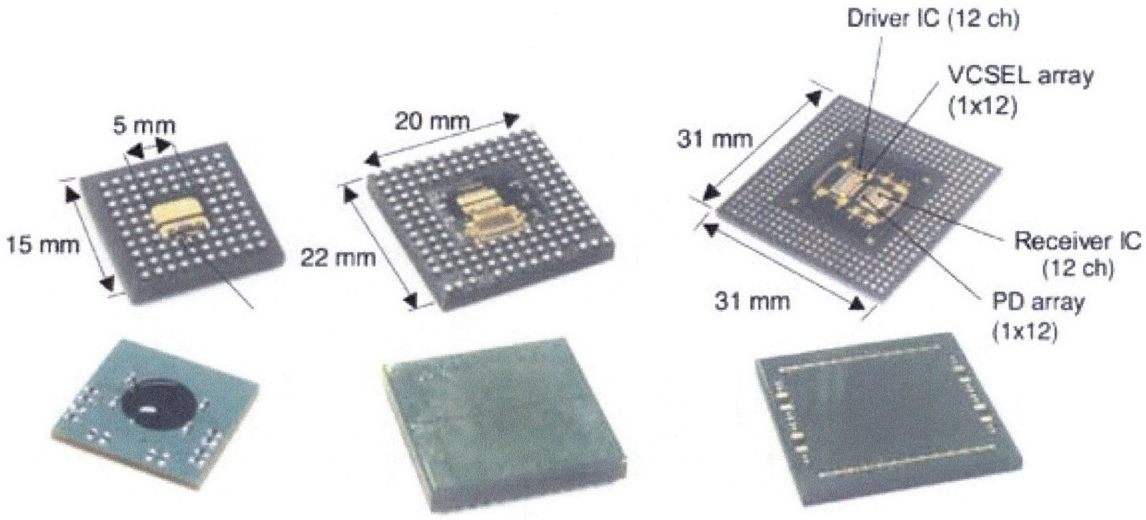


Figure 11 Schematic of Ball Grid Array (BGA) package. The package would then be mounted on the printed circuit board with the solder balls connection the chip and interconnects on board.

A further advantage of BGA packages over leaded packages is the lower thermal resistance between the package and the PCB. This allows heat generated by the integrated circuit inside the package to flow more easily to the PCB, preventing the chip from overheating. BGAs also have a very short distance of interconnection between the package and the PCB, allowing them to have low inductances and therefore have far superior performance to leaded devices.

A disadvantage of BGAs, however, is that the solder balls cannot flex in a way that longer leads can, so that bending and thermal expansion of the PCB is transmitted directly to the package. This can cause the solder joints to fracture under high thermal or mechanical stress. BGAs are therefore unpopular in certain fields, such as aerospace and military electronics, where reliability is the most important issue. This problem can be overcome by matching the mechanical and thermal characteristics of the PCB to those of the BGA, eventhough it is not widely used due to the extra cost needed.

In terms of application, BGAs find some use in security-sensitive applications, especially where it is impossible to prevent physical access to the chip. For instance, a ROM chip with a BGA configuration is considerably more difficult to access because tracing circuit paths to the BGA chip is limited by the contact points being obscured by the chip itself.[13]

Butterfly package

Butterfly package is a type of optical package that is widely used in the industry. It is named due to the physical structure of the package that looks like a butterfly with two series of leads on each side. Butterfly packages are basically can-and-cover type arrangements that contain an optical subassembly may be built up separately, outside of the can, and then later installed in the can. The circuits within the optical subassembly are wire-bonded to the leads of the butterfly can, which is then sealed with a lid to create a hermetic enclosure.[14]

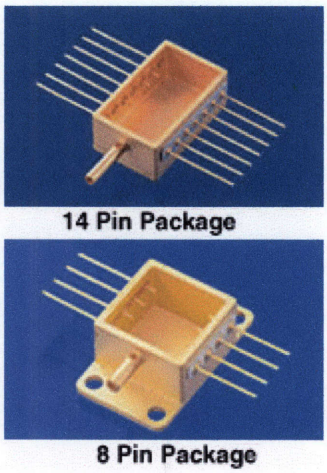


Figure 12 Butterfly package.[15] The existence of pins as the way of connecting package and the outer world remind us of dual in-line package in microelectronics, except light is what we are more concerned about here.

Butterfly package, in a way, is an equivalent to the DIP in microelectronics. The schematic and the design is pretty much similar, with of course difference in what they transported; electron for DIP and light for butterfly. It has even number of pins as well on each side, with 14 and 8 being the most used. Additional information on the package, mainly performances, will be discussed in the upcoming section.

4 Market analysis

Lack of standardization

Lack of standardization is said to be the situation happening in the optoelectronic package. However, less prove has been shown to support the statement so far in this report. The pie chart shown below can provide an idea on the lack of standardization.

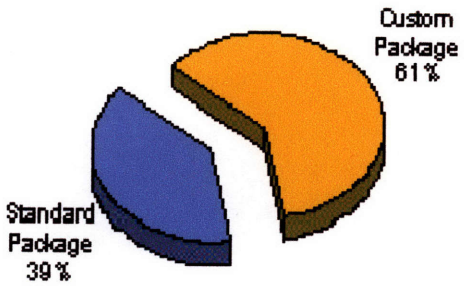


Figure 13 Optoelectronics package type proportion.[16] Lack of standardization state is shown by the major usage of custom package, rather than standard package, in the industry.

From that pie chart, it is shown that the majority of the package used in the industry is custom package, while standard package such as TO Butterfly and mini-DIL, only contribute to 39% of the total package used. Another prove is shown in the table below. Eventhough the data is only obtained from 6 companies; Finisar, JDSU, Infineon, Agilent, Excelight and Intel, we can already get such a big number of variation of package.

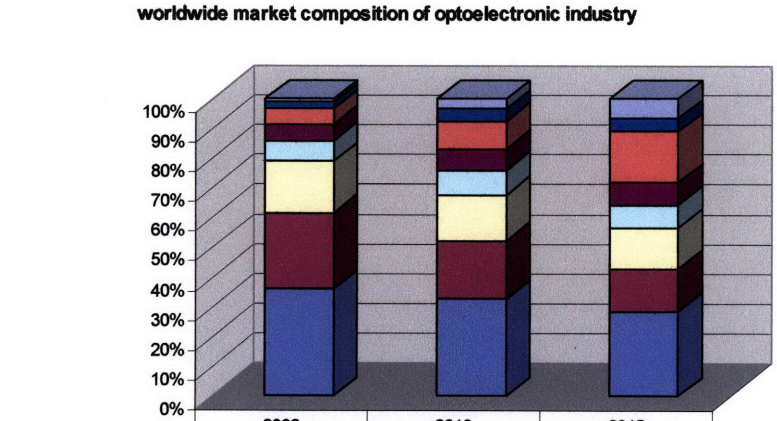
Table 1 Number of different types of transceiver package available in the market

Form Factor	Types
SFF	143
SFP	96
GBIC	20
XFP	5
MSA	50
Other	17

Market size

The following bar chart is taken from Optoelectronic Industry and Technology Development Association in their report titled "Future Vision of Optoelectronics

Industry" back in the year of 2004.[17] The chart shows the worldwide market composition of optoelectronic industry. The association predicted that the market would grow such that by 2010 the market size will be around $500 billion USD and around $900 billion USD by 2015. Important feature that might be pointed out is that the majority of the market will be display/lighting market with also the growing of the info-communications market. The input output market itself, the more significant market towards the application of standard package, size at around $100 billion USD by 2010 and $130 billion USD by 2015. This gives quite a huge market opportunity for the package.



	2002	2010	2015
Optical (Solar) Energy	2.56	17.05	61.40
Medical care/Welfare	5.97	20.47	38.37
Info-Communications	12.79	47.75	156.90
Processing	13.64	36.67	68.22
Environment/Sensing	17.05	41.78	69.07
Optical Memory	42.64	79.30	126.20
Input & Output	63.95	99.77	130.47
Display/Lighting	88.68	165.43	258.38

Figure 14 Worldwide optoelectronic industry market compositions.[17] Input Output market is the more significant market towards the application of standard package and sized at around $100 billions USD by 2010.

As for the segmentation of market for each region, North America is still the place where majority of the market for optoelectronic industry is, holding 37% of the market, and it is not expected to shift drastically in the coming 10 years.

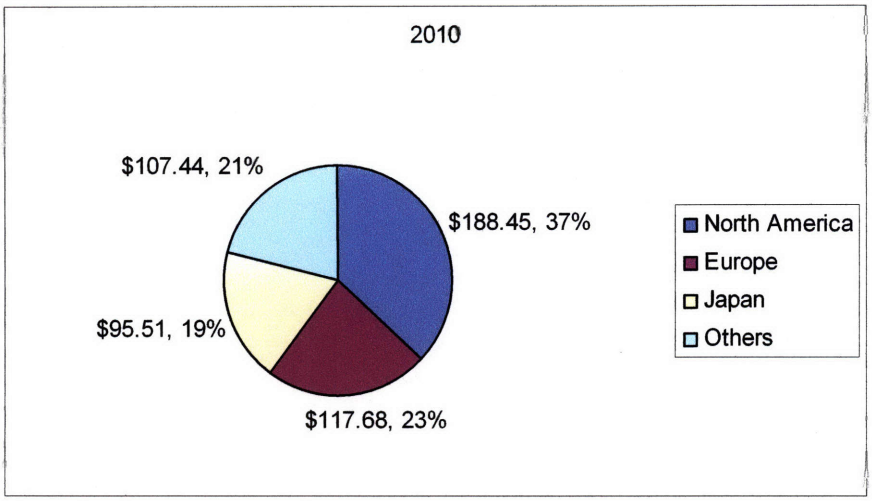


Figure 15 Optoelectronics market segmentation by area. North America is still the place where major market is located.[17]

Optoelectronic package trend

In the optoelectronic industry, device functionality dictates the package format. High performance devices are generally assembled in rugged butterfly packages. Lower performance, cost sensitive devices are assembled in less expensive transistor outline package formats such as TO-46 and TO-56.[18] The butterfly package is still the most popular optoelectronic packaging choice. It complies with a standard maximum "envelope" of outside dimensions and connecting lead (pin) specifications, but may have modifications of mounting detail, dimensional tolerances, interior sub-mounts or other features, as well as sealing details. The butterfly fabrication may incorporate glass mounted or ceramic co-fired lead feedthroughs. The global consumption of standard and modified standard butterfly packages represented 58 percent of global standard device package consumption in 2000.[19] These packages are proven to be acceptable at frequencies as high as 2.5 Gb/s and, with some accurate chosen design options, they can go up to 10 Gb/s. Considering the wide usage of butterfly type of package, it should be considered to be the solution for standard package based on optoelectronic package market.

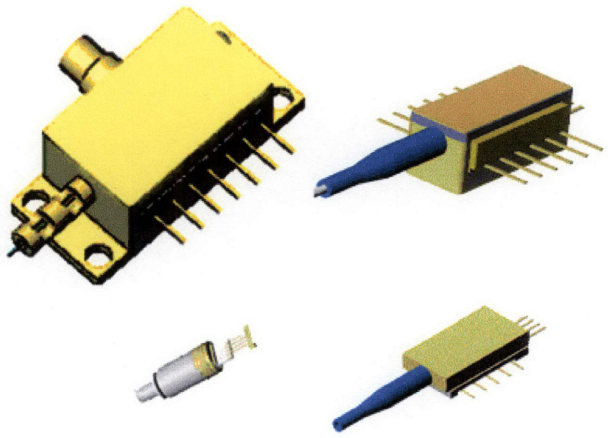


Figure 16 Optical module packaging options. Upper left shows a standard cooled "butterfly" can with coaxial RF interface. Upper and lower right show cooled and uncooled modules, respectively, with coplanar RF interface. Lower left shows uncooled TO can with coplanar RF interface.[20]

Electronic package trend

Since we are looking for a platform that facilitates electrical and optical abilities, it is valuable to analyze electronic package to get the same ability to flow from different hierarchies in the package. In other words, it will somehow replace some of the electronic package and we would like to see whether we could fit optics to electronics. Barrier towards the implementation of standard package also lies in the acceptance of the respective players to apply the standard package. Therefore it is wise to choose the type of standard package that is used widely in the market to lower the barrier. So it's worth to take a look at the electronic package segmentation and try to find the packaging solution from the market analysis. It is shown on the chart below, the electronic package segmentation for different types of electronic package; DIP, BGA, QFN, WLP, SIP, SO, etc. There are some trends that needed some extra attention. It is clear that the DIP (Dual In Line Package) holds the majority of the package type used, but it seems like the market size of it will be decreased over the future. On the other hand, BGA represents small percentage of the package, but the use of it will be growing in quite significant rate. While the others are either smaller in percentage or just expected to grow in a slower rate, package type similar to DIP or BGA has been chosen as the market answer for the standard package based on electronic package segmentation.

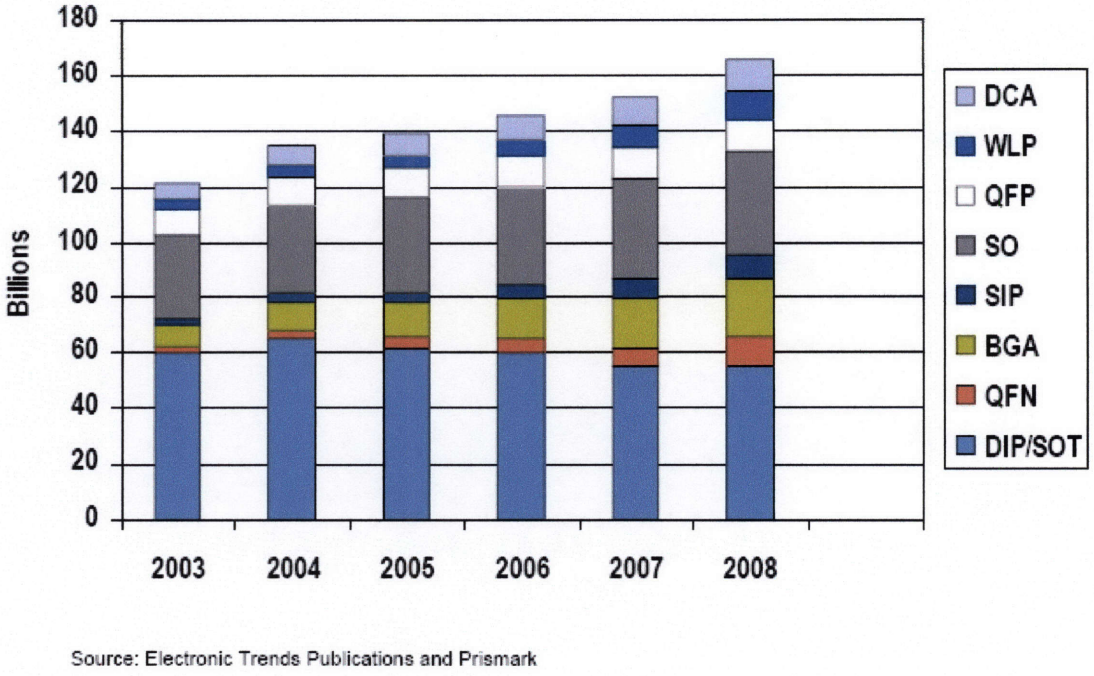


Figure 17 Electronic package segmentation for different type of package.[21] DIP has been the major type of packages used in the industry with BGA increasingly used.

5 Technology analysis

Optoelectronic package requirement and technology

The requirements for optoelectronic package depend on the application. For undersea or long haul application, reliability is most important, while for data communication low cost is significant. However, in general, all applications of optoelectronic package require good alignment for good and efficient optical link performance. Optical alignment requirements are generally much tighter, by about an order of magnitude, than those required by electronic packages. This is due to the condition that misalignment will cause significant optical losses.[22]

To achieve accurate optical alignment, three approaches are available, namely active alignment, passive alignment and self-alignment. In the active alignment, alignment

is done while the device is turned on because the location of active region is not known. This method can achieve sub micron alignment, but it takes minutes to be completed. Passive alignment is done when the location of active region is already known, thus the device does not need to be turned on. It takes significantly faster time, seconds; however it can go only until micron alignment accuracy. Self-alignment can be achieved by using the restoring force of solder reflow. Patterned templates are usually used to promote the alignment accuracy. Compared to electronic package alignment, those are relatively more difficult and less automated in today's world of optoelectronic industry. Some other technologies included in optoelectronic packaging are pretty similar to electronic packaging. They include using wire bonding, laser welding, soldering, die attachment, epoxy and hermetic or nonhermetic sealing.[22]

Additionally, thermal management requirement for optoelectronic package has to be more stringent. CTE mismatch may introduce stress, which will lead to misalignment and lost of performance. Another important phenomenon is thermal optics effect, which is the varying of index of refractive with temperature. Index of refractive mismatch will cause more dispersion and degrade the performance of the chip. This is important considering the active regions in optoelectronic devices are extremely small in size, although not much heat generated. Thus, the volumetric heat sources are large enough to introduce problem to the package. A system wide view of thermal management has to be developed. Heat sink and other cooling methods might need to be applied.

Standard transceiver inside the package

In order to come out with standard package, the chip inside the package has to be chosen. The requirement for that transceiver is the one that can accommodate the bit rate x distance performance parameter for each segment to take advantage of large product volume. Local area network has a bandwidth of 10 Gb/s (15 km-reach), while broadband access has 1 Gb/s (1 km-reach); storage area networks has 40 Gb/s (25 m-reach) and sever buses has 1 Tb/s bandwidth (1 m-reach). The standard transceiver

must have a robust design to achieve all technical specifications, process steps that can achieve mass production with high yield and minimal number of fiber and waveguide connection.[1]

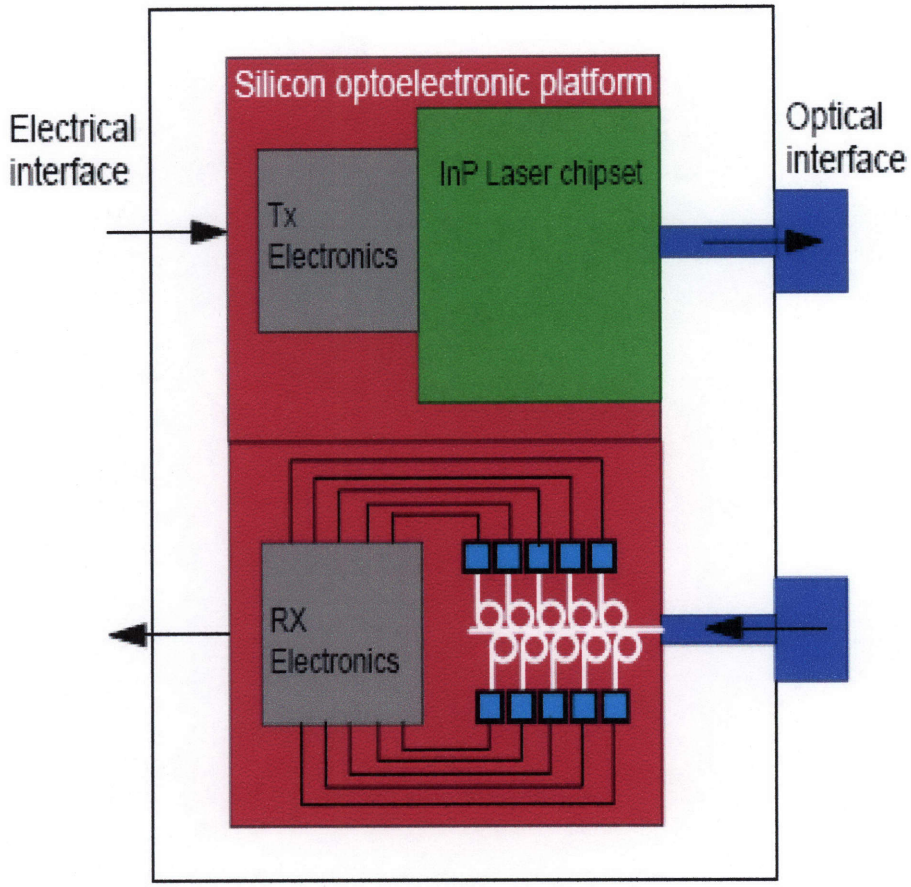


Figure 18 MIT Tb/s silicon platform transceiver. The optical components are built on InP substrate and then hybrid-bonded with the silicon platform where the electronic components are located.

Michael Speerschneider, Kelvin Chan, George Whitfield, and Emily Zhang on a MIT group project as part of course 3.46 Optical and Optoelectronics Materials create the architecture design shown above.[1] It is an MIT Tb/s silicon platform transceiver. It has been chosen to be the standard transceiver used for the consideration of the standard package that is going to be designed. It was chosen for its ability to meet the requirements of the four market segments with minimal mechanical contacts. The modulator/laser structure used for this design, InP laser, is capable of speeds up to 25 Gb/s, even though 40 Gb/s InP modulated lasers have been demonstrated. Ge/Si

detector technology is relatively new and might also accommodate 40 Gb/s. Allowing for unforeseen technology advancement in laser design and electrical interconnect capabilities, the design could allow transmitters and receivers up to the material dispersion limit for bit rate, approaching 100 Gb/s.

Additional advantage of the architecture is the use of monolithic integration of device and waveguides. While the laser cannot be easily grown on Si, the detector and waveguides have been selected so that they could be grown in a single processing step. The advantage to monolithic integration is a reduction in the processing costs and enhanced coupling efficiencies. All the optical components are to be grown on an InP substrate and then flip-chip bond the InP substrate to Si Substrate. In essence, the Si substrate supplies only electrical power and control signals to the InP substrate on which all the optical components are present. [1]

There is resistance to having III-V materials into the clean rooms of Si processing. This is because Ga and In in our case can contaminate Si and become dopants within Si. As dopants, Ga and In act as non-radiative recombination centers. FET and BJTs are engineered on an IC chip to exact performance specifications. If the minority carrier recombination lifetime is not precisely controlled, IC chips produces will have varying switching speeds and thus varying processor speed. In or Ga-mediated recombination depends on their concentration, and thus this is something uncontrolled for IC fabrication. Hence the great ban on III-Vs in Si microelectronic cleanrooms.

However, the integration of III-Vs material (InP laser) onto the Si platform in the standard transceiver design is hybrid rather than monolithic. Thus, the issue described in the previous paragraph is not provoked in the standard transceiver's case and the standard transceiver design has been proven and able to be produced in today's research.

Standard package requirement

After few discussions with the Communications Technology Roadmap's Technology Working Group, constraints have been set on what the optoelectronic package should have to be able to be the standard package.

First, the data rate of 10 Gb/s has to be allowed. However, considering the ability of standard transceiver to achieve Tb/s performance, the standard package has to support this data rate, while 10 Gb/s is more like the short run solution. In terms of number of channels, 100 optical channels are expected with power dissipation below 10W.

The questionnaire set has helped us also in determining the performance requirement of the standard package. Alan Benner from IBM and Ashok Krisnamoorthy from Sun are ones of the industry experts interviewed. Alan agreed on the data rate requirement of the CTR, which is 10 Gb/s, and starting to get into 40 Gb/s and starting to think about 100-200 Gb/s rates. However, parallelism seems to be one of the main issues that need to be overcome by the standard package. There are other bottlenecks higher in the system that limits the speed that is actually usable. Thus, more often more parallel 10 Gb/s channel is more useful than 1 Tb/s channel. Pluggability seems to be another requirement which will make the standard package a very useful and adoptable module to the industry.[23]

In terms of power dissipation, Ashok pointed out that it is another driver for the standard package. In past, the thermal and cooling aspects of system design were looked upon as the last step in the design cycle, with thermal engineers forced to find acceptable cooling solutions in a highly constrained environment with little ability to alter the logical design of the system or to influence the design of the microchips. This is now changing. With the advent of 100W+ super-processors, it is becoming critical to include thermal considerations and I/O considerations early in the design of the chips.[24] Thus, for the standard package, he mentioned that it should be able to handle 50 to 100 W of power dissipation.

In power per bit rate unit, Alan mentioned that he believed and would like to see the power dissipation of 5 to 10 mW per Gbps. That would be a decrease by a factor of 10 from the current situation which is around 100 mW per Gbps.[23]

Traditionally, due to the difficult problem of achieving stable high optical coupling in a reliable manner, butterfly style packages have been used. Smaller, lower cost cooled packages with coplanar RF interfaces have been developed to enable smaller form factor transceivers without sacrificing performance. Finally, coaxial TO-can-style optics with either coplanar ceramic or glass feedthrough RF interfaces are emerging to provide a very low-cost package that still provides adequate signal integrity for 10 Gb/s operation. It is critical that new optical packaging technologies increase yields and the quality of performance and reliability while decreasing the cost of the components, simplifying their manufacture, and reducing testing.[20]

The main focus on this standard package would be on the interchip or chip-to-chip level. At that level, fiber or waveguide is the interconnection on the board. It is thus expected for the electronic circuit interconnection to be happened only inside the package. For this reason, the package has to provide ability for the electronic IC to interact with one another. By that rationale, Systems-in Package (SIP) has to be another requirement for standard packaging answer.

Package analysis

If one uses market penetration for determining the standard optoelectronic package, the type of package would rather be DIP-like or BGA-like and butterfly-like. Earlier analysis has also added another requirement for the package, which is SIP. What needed to be analyzed now is whether the types of package dictated by the market are able to provide the technical requirement (data rates, channels, power, etc.). Table shown below summarizes the situation to ease the illustration of analysis.

Table 2 Standard package type and requirement metrics

Package Type	Technical requirement
DIP-like	Data rate of 10 Gb/s
BGA-like	100 optical channels
Butterfly-like	Power dissipation below 10W
Systems-in-Package	

First, data rate issue is going to be analyzed. In the case of Systems-in-Package, the limiting factor will be the electrical connections inside the package. However, for such a small distance (within a chip), electrical connections have shown reasonable performances. Therefore SIP requirement would not be a problem for the standard optoelectronic package. In the case of butterfly-like, the following matrix shows different types of optoelectronic package with respect to their reach and data rates. It was taken from Claudio Truzzi's article in Chip Scale Review Magazine, back in the year 2003.[25] It can be seen from the matrix that to get 10 Gb/s data rate and short reach, surface mount type of package is the solution. However, noting that this matrix is made in 2003, butterfly types of package (Butterfly Mini-DIP) nowadays have shown the ability to perform up to 10 Gb/s data rate. Thus, butterfly-like requirement could be implemented to the standard package design, as far as data rate is concerned.

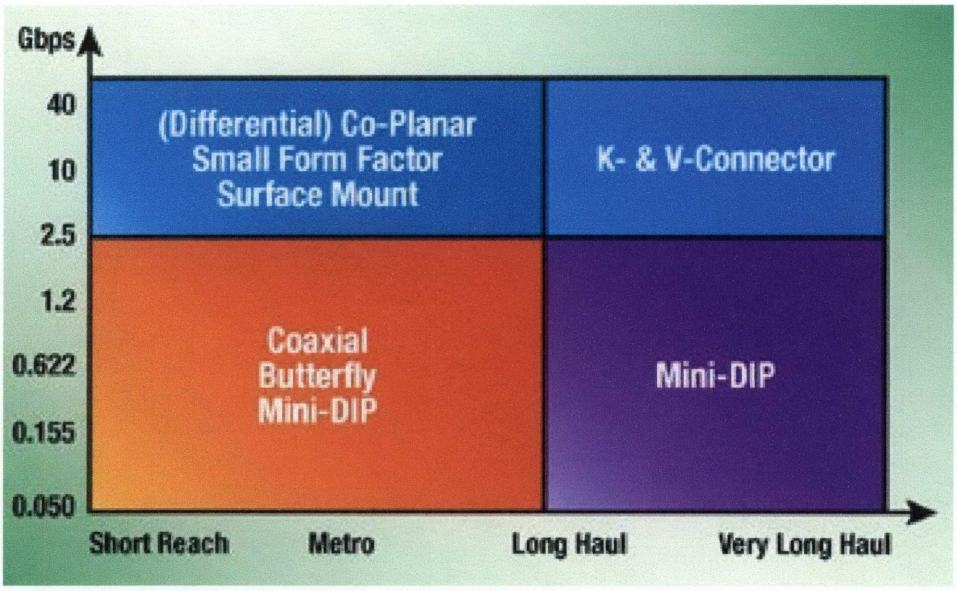


Figure 19 Data rate vs. reach of optoelectronic packages.[25] For short distance, surface mount type of packages can serve higher bandwidth compared to butterfly and mini-DIP types of packages.

It is important to note that it is always optimum for the optoelectronic device to perform in the dispersion limited regime rather than attenuation limited. Thus, high data rates can be obtained for interchip level with the compromise of reasonable dispersion. The following plot illustrates the regimes described.

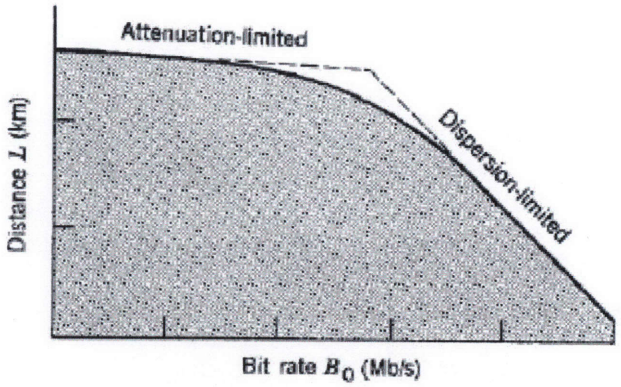


Figure 20 Attenuation limited and dispersion-limited regimes. It is important to have the system running in the dispersion limited regimes since it is the most efficient usage of the device.

In the case of BGA-like or DIP-like, it is rather similar to either butterfly mini-DIP or surface mount (BGA is a surface mount device). Thus, data rate issue has been discussed as we discussed the butterfly-like case earlier. However, there are some

advantages of surface mount device (BGA-like) over the DIP. First, as have been stated before, eventhough butterfly mini-DIP is able to perform up to the required data rate; surface mount device is able to perform even at higher data rate. This will allow further expansion of data rate, and suits the standard transceiver better (up to Tb/s performance). Then, the size is smaller making it possible to have a higher density of package. The following picture compares the size of butterfly mini-DIP to surface mount package. Being surface mounted, it allows double side utilization of the board, hence again higher density is possible. Finally, the solder used in the surface mount package could perform self-alignment and making it easier to be processed.

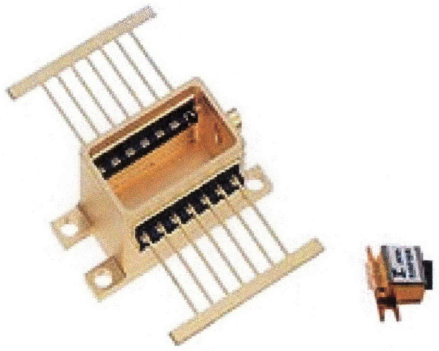


Figure 21 Size comparison of butterfly mini-DIP and surface mount package.[25] Surface mount package is much smaller than butterfly mini-DIP, which leads to higher density of package, can be applied onto the board.

In terms of number of optical channels, 100 is not a really big number since 200 and even higher number of optical channels has been shown. This number can be increased by using the concept of dense wavelength division multiplexing (DWDM) in which one line of input output can contains numerous wavelength, hence increasing the number of channels, as well as the data rate. Typical power dissipation of the optoelectronic package and interconnection is around 2W if we recall back from chapter 1. Thus, the requirement of power dissipation is not so much of an issue as well in the standard package determination.

So, now it is up to the decision on whether DIP-like or BGA-like device is going to be implemented. Historically, the electronics industry moved to surface mount

technology to achieve higher performance and lower cost with miniaturized geometry. Optoelectronics should not be an exception. It has been reported that optimized via-hole structured surface mount package solutions for 40 GHz applications is now offered. Therefore, surface mount package with systems-in-package would be the standard package solution for the standard transceiver.

6 *Possible Current Applications*

The initial focus of the MIT CTR IPI Technical Working Group is to provide the package for the emerging current applications. There are some applications in the need of high bandwidth (10 Gb/s) and therefore the standard package could be applied. From these applications, it is hoped that the package will be improved simultaneously and the package will be ready for the massive applications in the future optoelectronic interconnection.

Pluggable High-End Processors

An example of this application is pluggable processor chip directly interfaced to OE/EO chip with 2 to 8 I/O optical interconnects to or from other CPU, GPU, or storage chip. There are some attributes needed for the application. In terms of physical appearance, the package should be a typical chip or Multi-Chip Module (MCM) package with approximately 3x3 cm^2 in size. The maximum fractional plan area for I/O is approximately 60 percents of the area. Maximum toggle rate from source IC is needed to be 10 Gb/s with a latency of less than 6 ns. The target power dissipation, measured as the total power above the power required for chip function, should be less than 80 W in total. This application is also targeted to cost around $50 from end to end, including transport, relative to cost of electrical implementation. Following is a cartoon showing a general schematic of the pluggable high-end processor.

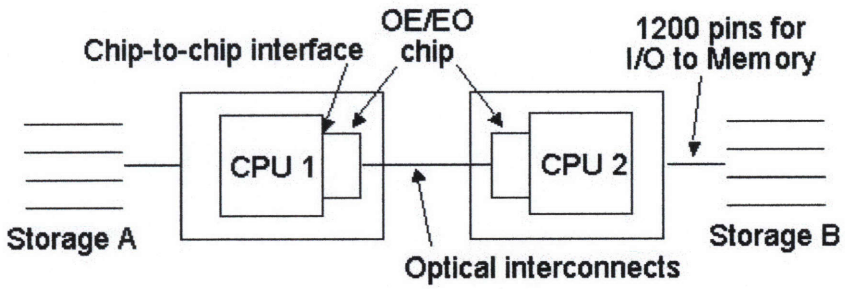


Figure 22 Emerging application for the package: pluggable high-end processor schematic diagram.

Pluggable Large-Matrix Optical Cross-connects

Pluggable 1024x1024 optical cross-connects electronic photonic integrated circuit is an example of this application. It has 16 optical I/O ports for degree-8 node, which carry 1280 Gb/s per aggregate line. That is equivalent to 128 Wavelength Division Multiplexer (WDM) channels with 10 Gb/s per channel. This also gives a total aggregate bandwidth of 20.48 Tb/s, with 2048 lines carrying 10 Gb/s each. Eight 128-channel Mux/Demux pairs are expected and 128 8x8 switches and electronic control circuitry are integrated in the module. Following is the schematic diagram of this application, pluggable large-matrix optical cross-connects.

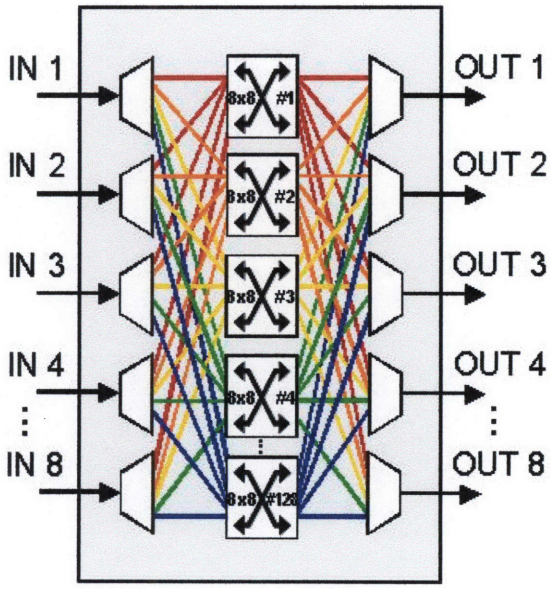


Figure 23 Emerging application for the package: pluggable large-matrix optical cross-connects schematic diagram.

Volume Interconnects for High-Slot-Count Backplanes

It is expected in the future to have 10-20 spatial channels per module, 100-200 spatial channels per board and 1000-2000 spatial channels per backplane. The example of current emerging applications is a backplane having 10 slots on it with 100 spatial channels to or from each board and 1000 spatial channels on backplane. This is the derivation of Tyco's development in 2002, which is 144-channel optical backplane interconnects having optical connectors. These connectors are 144-channel Super MT connector for strip-to-strip connection and 24-channel modified MT connector for waveguide strip to fiber array connection. The actual schematic of the backplane interconnects is shown in the following figure.

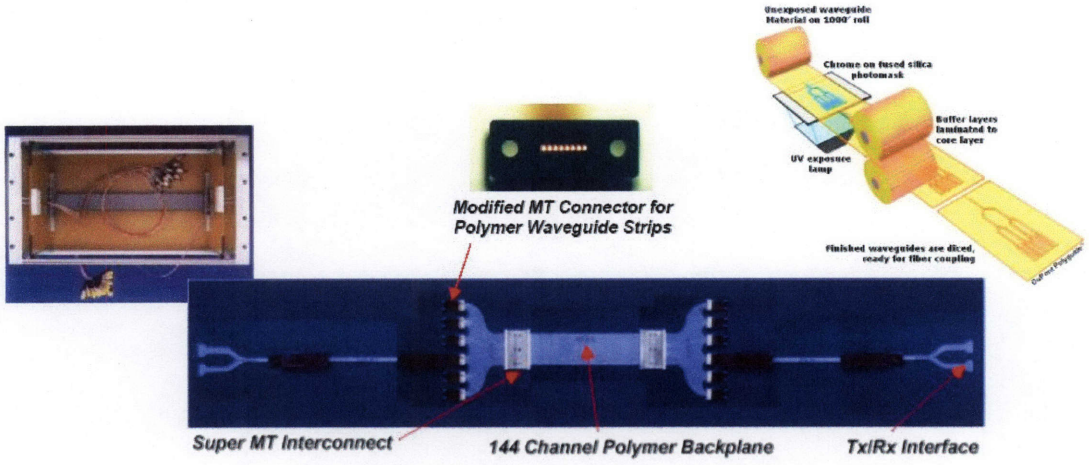


Figure 24 Emerging application for the package: high-density backplane interconnects with 144 parallel optical lines.

Chapter Three: Intellectual Property

Upon obtaining the standard package, intellectual property associated with it should be analyzed. According to United States Patent and Trade Offices (USPTO), a patent is the grant of property right to its inventor and generally valid for 20 years. Within this timeframe, no other individual is permitted to make, use, offer for sale or sell the invention in the United States or import the invention into the United States. Therefore, potential impinging patents should be analyzed to define the business model of the standard package. Following are the patents relevant to the optoelectronic package.

US Patent 6,935,792

General Electric's US Patent #6,935,792 entitled "Optoelectronic Package and Fabrication Method" is published on 30th August 2005.[26] This patent claims on the fabrication method as well as the optoelectronic package made through the fabrication. One of the probable impinging claims is claim 20, which claimed the following.

An optoelectronic package comprising:

(a) a substrate;

(b) an optical device positioned within a window of the substrate active-side up and below a top substrate surface;

(c) an optical polymer material surrounding the optical device within the window and having a planar surface with respect to the top substrate surface; and

(d) waveguide material patterned over the optical polymer material and the substrate and forming an optical interconnection path and a mirror configured for reflecting light from the optical device to the interconnection path, the waveguide having a via to expose a bond pad of the optical device.

This claim is quite broad and it needs to be considered, along with the next claims containing claim 20, when determining the physical design of the standard optoelectronic package.

US Patent 6,910,812

This patent entitled "Small-Scale Optoelectronic Package" is published by Peregrine Semiconductor Corporation on 28th of June 2005.[27] Main claims are on an integrated circuit/optoelectronic packaging system which comprises OE and IC components packaged to provide electrical I/O, thermal management, an optical window, and precise passive or mechanical alignment to external optical receivers or transmitters. The functionality of the package is the main emphasis of this patent and it does contain statement with regards to optoelectronic devices that are mounted on the transparent insulating substrate. Having decided on the surface mount package, further careful has to be performed in designing the standard package in order not to impinge this patent.

US Patent 6,860,652

Intel Corporation's published US Patent entitled "Package for Housing an Optoelectronic Assembly" which dated on 1st of March 2005.[28] They claim the specific type of package for housing an optoelectronic device and integrated circuit. The type is surface mounted; however they are pretty specific on the description. Thus, it would not be so much of a problem for the standard optoelectronic package design.

US Patent 6,841,799

This patent is published by Agilent Technologies, Inc. entitled "Optoelectronic Package" on the 11th of January 2005.[29] They claim an optical device having housing for one or more optoelectronic components. This is quite coherent with the idea of our standard optoelectronic package, particularly systems-in-package requirement.

Intellectual property has been a very important factor in the process of developing new technology. Increasing awareness of IP infringement has been notified for the past decades. We obviously do not want to spend our effort in designing the standard package, which will later turn out to infringe someone's intellectual property. Therefore, more rigorous intellectual property analysis by authorized and professional body should be done in the process of designing the standard optoelectronic package.

The problem that may arise is that some of the patent's owner described above is the member of the Communications Technology Roadmap TWG. Each of them may want to introduce a standard package, which lies around their intellectual properties so that it will be an advantage for them. TWG leaders should be aware of this situation and make sure that the standard package should not be determined based on some parties' benefit but mainly based on the performance required and the health impact on the industry.

Chapter Four: Business Model

Business model describes how technology is transferred into business and finally money. For standard optoelectronic package, there are at least two main models to be considered as business model. It is either by intellectual property (IP) or manufacturing model.

IP model is done basically through the ownership of the technology. The technology consisting of the package design, performance ability, etc. should be patented to respective patent office. Following that, the technology is licensed to parties with interests towards it by charging license fees. The parties are usually industry players who will then manufacture the product out of the license and throw the product to the market. On the other hand, manufacturing model is done through being part in the supply line of the product. In this analysis, we will assume that by taking a manufacturing model, we will only take part in the manufacturing of the package.

The following analysis in this chapter is designed for start up and ongoing company in the industry. The result might be different for each case and will be discussed more thoroughly in the following sections.

1 Basic Issues

The key to the success of the standard package is the wide usage of it or in other words driving up the volume. The question is now lies on how the process of driving up the volume to use the standard package will be done. The answer lies on the high performance and low cost of the package. One of the constraints given by the technical working group to be worked on is the cost. The package cost, including the transceiver, is targeted at $0.50/Gbps. Comparing to the current price of transceiver and package which is averaged at around $10/Gbps, the cost of standard package is very competitive. Recalling the high level performance of it, combined with the low

cost, it is quite convincing that the standard package volume will materialize. The barrier to implementation now left in the materialization of the package. As far as the transceiver is concerned, the performance has been proven on research-based. CTR TWG consists of reputable people from the industry, such as Intel, Analog Devices, Agilent, DuPont, etc. These people are very important in the industrialization of the transceiver. As for the package, design based on the requirement stated earlier has to be more properly done to overcome the barrier.

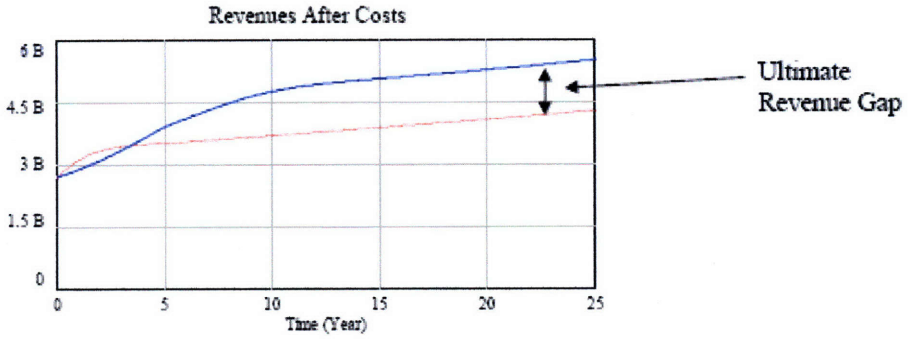


Figure 25 Barrier to implementation shown in the revenue vs. time chart.[1] The period of lost revenue could stand as a barrier towards the implementation of the standard eventhough the ultimate revenue gap will be reaped at the later stages of the application period.

Besides technology challenge, there would be another barrier for this standard package to be implemented, although it's already well designed. Analogy from transceiver analysis in Speerschneider's thesis is taken, so the above graph is for illustration purposes only. The number is not of an importance. This revenue graphic shows that initially the revenues are greater if the industry continues to diverge. That period of lost revenues is a powerful barrier to implementation of the standard, as there is no guarantee for the firms that the period will pass and standardization will reap the significant revenue increase (ultimate revenue gap) suggested by the model.[1]

2 *Quantitative analysis*

Following quantitative analysis was done using Vensim PLE and Microsoft Excel software. A model is built using a principle of system dynamics, as have been explained earlier. Conceptualization stage was done by defining the purpose of the model and the variables of importance. The purpose of the model is to compare quantitatively IP model to manufacturing model. This comparison is done in terms of revenue in this model. Following are the variables of importance, both for IP model and manufacturing model.

Table 3 List of variables for the revenue modeling

Variables	
IP Model	**Manufacturing Model**
Licensing rate	Price per unit per Gbps
Licensing payment	Price reduction
Licensing revenue	Cost per unit per Gbps
Market share	Cost reduction
Increase in market share	Cost reduction rate
Market size	Profit per unit per Gbps
Market growth	Market share
Market growth rate	Increase in market share
	Sales volume
	Bit rate
	Sales
	Manufacturing Revenue

From the above list of variables, model was made to represent the concept of revenue either by doing IP or manufacturing model of business. This model was built using Vensim PLE and it is shown in the figure below.

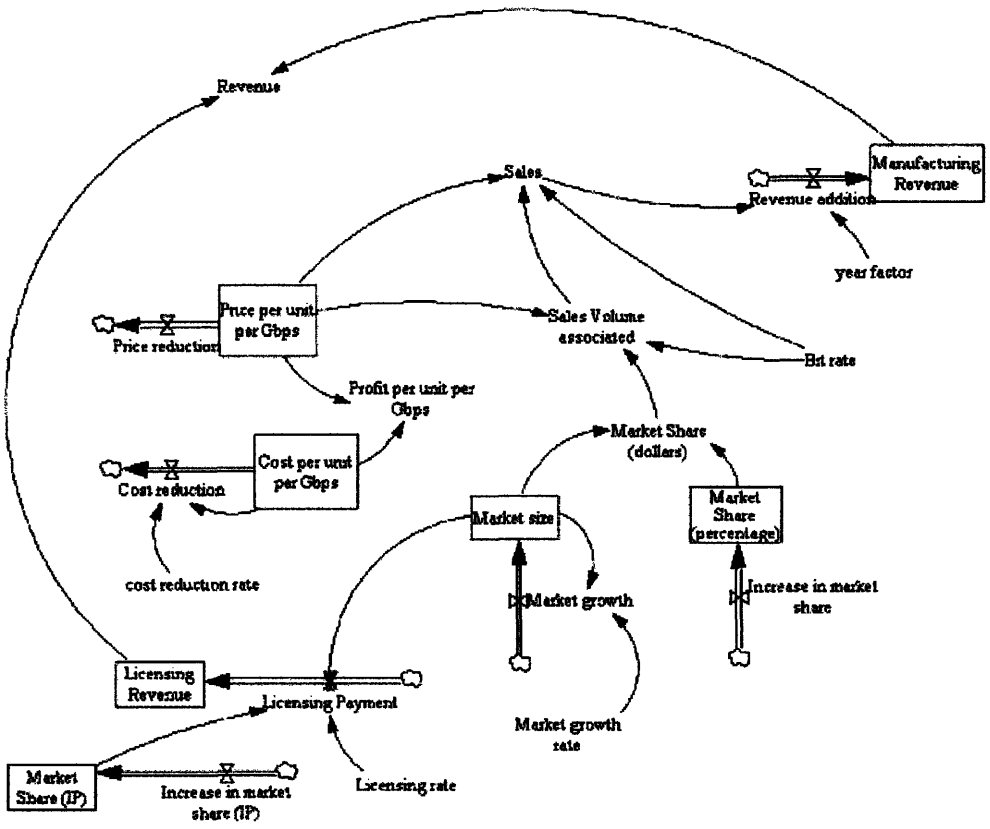


Figure 26 Revenue model. Manufacturing and IP model is included here and certain assumptions and formulae were assigned and can be seen in the appendix.

From the model we can see that for the manufacturing model; as reflected by the manufacturing revenue model; the contribution comes from the sales. The higher the market share and market size, the sales figure is also higher. In this model, the rates of increase in market growth and market share are assumed to be constant. It is also assumed that the cost as well as price of the package will be reduced in a constant rate for the next five years. As for the IP model; as reflected by the licensing revenue model; the licensing rate is taken to be 5% from the market share. Thus, the higher the usage of license is, the licensing revenue is going to be higher too.

Formulae were then assigned to each of the variables in the model. Numbers of assumptions have been made in order to finalize the model. For the reason of simplicity, some variables were assumed to be constant, such as market growth rate, cost reduction rate, price reduction rate, and increase in market share. However, these assumptions were obtained based on the market research data and the industry survey

results. Therefore, it is hoped that the model really demonstrates the close, if not real, picture of the market. Detailed assumptions, formulation and coding can be referred to appendix 2.

Using market data in Figure 11, the market size for input output industry is around US$ 100 billions in 2005. Assuming that currently 10 Gb/s devices only contributed by 10% of the market, we can get the total market available for either business model. Another statement for the model is that the market share for IP model is far greater than manufacturing model. This is based on the opinion that it is very hard to gain large market share for start-up company, especially in the manufacturing industry. Therefore, market share for IP model is assumed to be 10% and the market share for manufacturing model is 1% of the total available market. Increase in market share is assumed to be constant at a rate of 5% for IP model and 0.6% for manufacturing model. Following those assumptions, the revenue for respective model can thus be calculated and is plotted in the graph below.

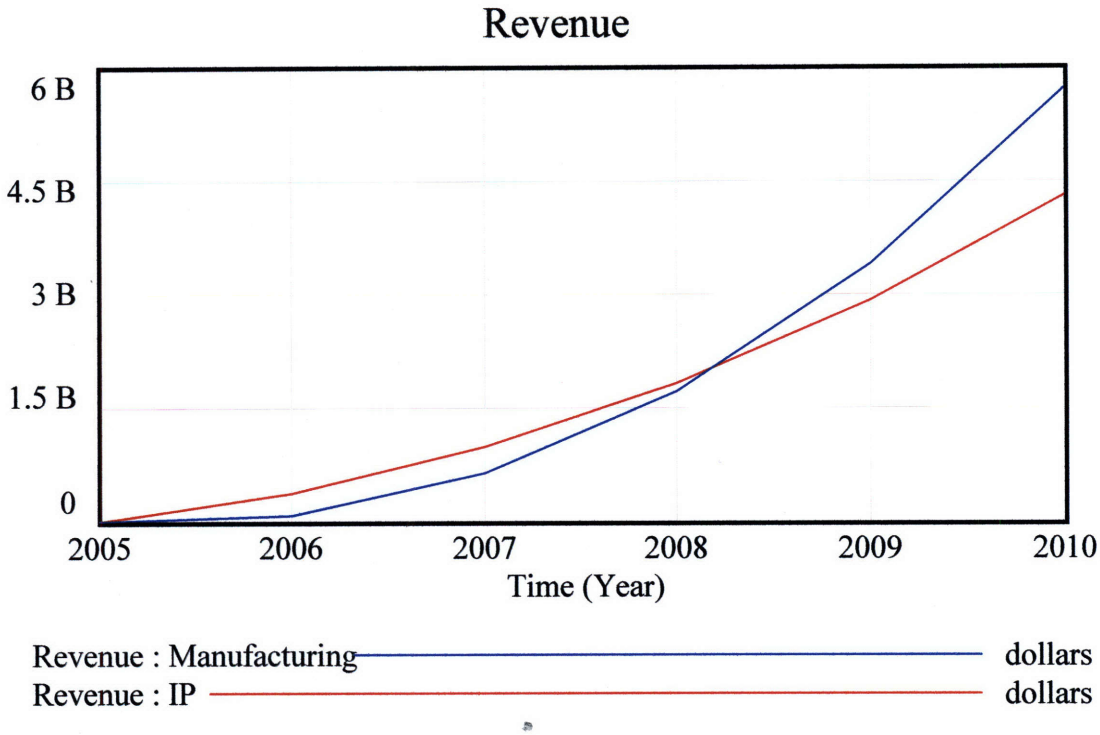


Figure 27 Revenue accumulated comparison IP model vs. manufacturing model. Units are in billions of dollars. This graph was made using the dynamic model in earlier figure and assumptions listed in the appendix.

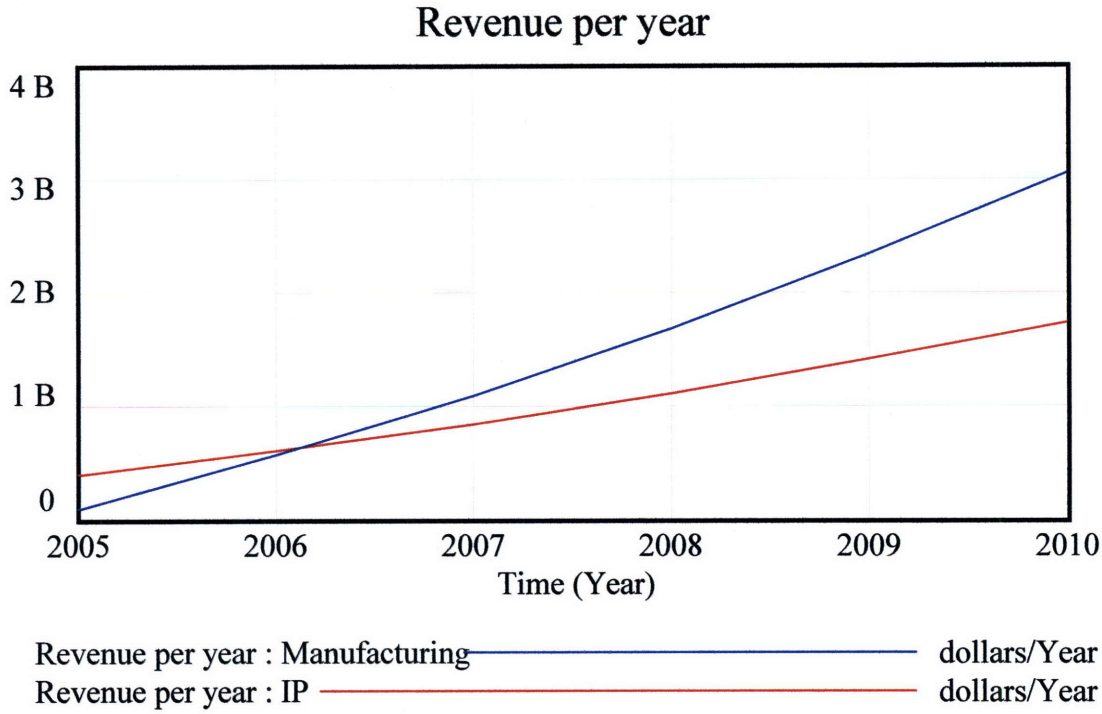


Figure 28 Revenue per year comparison IP model vs. manufacturing model. Units are in billions of dollars. This graph was made using the dynamic model in earlier figure and assumptions listed in the appendix

From the above figures, we can see that IP model initially looks more profitable than manufacturing model. However, after certain period of time, the manufacturing model takes the lead and seems more lucrative. In order to perform the decision fairly, we also have to account for the discount rate per year, in other words, net present value. Net present value is a way of comparing the value of money now with the value of money in the future. A dollar today is worth more than a dollar in the future, because inflation erodes the buying power of the future money, while money available today can be invested and grow.[30] The discount rate is assumed to be 10% per year, and with all the assumptions above still hold, we came out with NPV of around US$ 4.4 billions for IP model and US$ 5 billions for manufacturing model, a difference of around US$ 600 millions. The sensitivity analysis has been done in Excel towards the changing of initial market share and it is shown in the following graph.

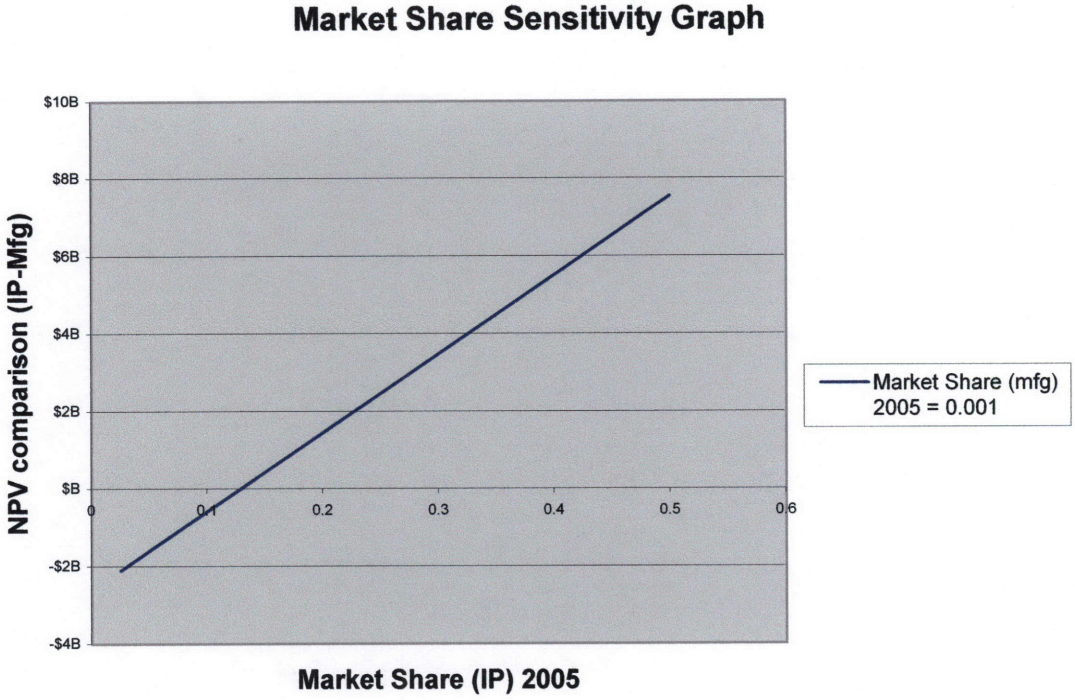


Figure 29 NPV comparison between IP and manufacturing model with changing market share for IP model. Units are in billions of dollars. This graph was made using the dynamic model in earlier figure and assumptions listed in the appendix

The term that we used in the sensitivity analysis is NPV comparison, which is the difference between NPV of the IP model and NPV of manufacturing model. From Figure 26 we can see that for the IP model to be as profitable as manufacturing model, its initial market share has to be 12.5%, the point where the blue line intersects the x-axis. This is a pretty high number, although not impossible in the future, considering that our first assumption is the 10Gb/s devices contributed to 10% of the total market size. It is also shown in Figure 27 that even for high market share for IP model, 50%, the manufacturing model can be as profitable with only gaining 2.7% market share, the point where the line intersects the x-axis. Therefore, from the net present value and sensitivity analysis, manufacturing model seems to be more profitable than IP model.

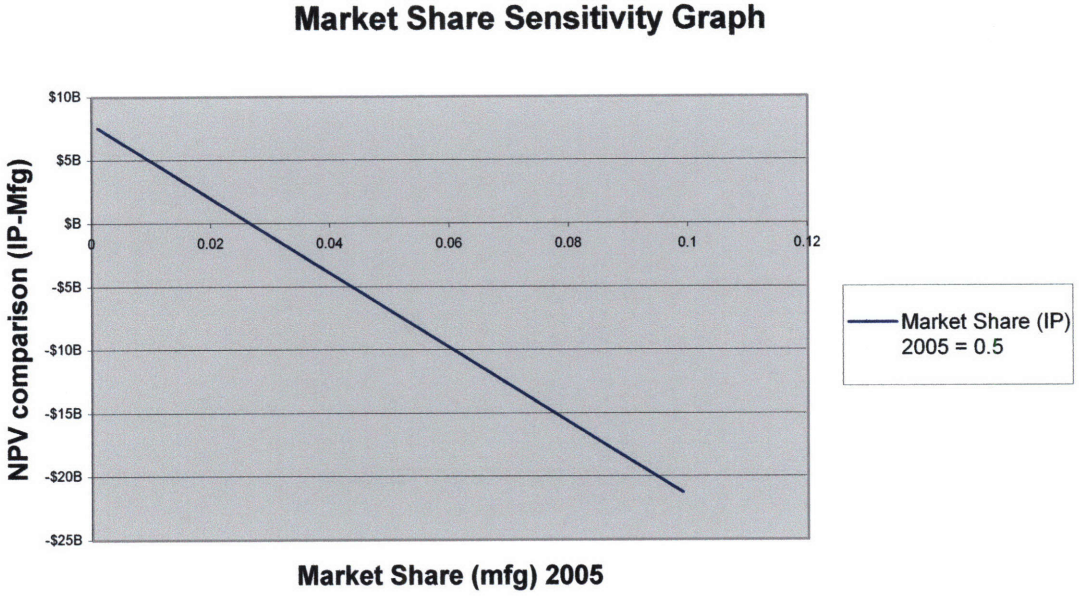


Figure 30 NPV comparison between IP and manufacturing model with changing market share for manufacturing model. Units are in billions of dollars. This graph was made using the dynamic model in earlier figure and assumptions listed in the appendix

3 *Qualitative Analysis - Sustainability*

Having analyzed quantitatively, we still need to do a qualitative analysis on what our decision will be. Our qualitative analysis will be done based on the sustainability issue of a technology. We might consider identifying whether the standard optoelectronic package will be a sustaining or disruptive force in the market. According to Christensen in his book "The Innovator's Dilemma", sustaining technology is a new incremental technology, which targets an established high-end market. A disruptive technology, on the other hand, targets emerging or low-end markets. Major characteristic of disruptive technology is that it emphasizes formerly overlooked attributes, which are attractive to the consumers. If a technology falls into the sustaining category, then it targets a well-defined high-end market with a lot of big competitors. Therefore, starting a new company based on a sustaining technology would not be a good option. On the other hand, a disruptive technology could enable the foundation of a start-up company. There are less and smaller competitors, thus no

significant competition that will endangered the survival of the start-up company.[31] This is summarized in the following figure.

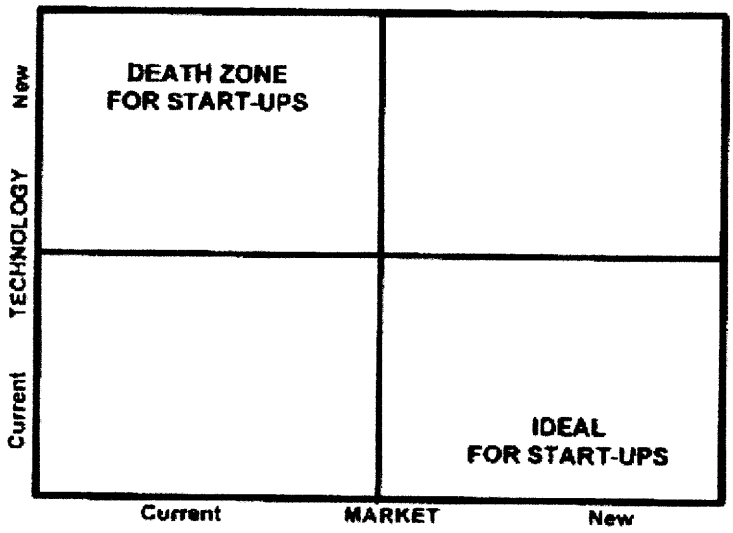


Figure 31 Technology-Market matrix for business. Sustainable force (new technology in current market) is more applicable to be done by ongoing company in the industry while disruptive force (current technology in new market) is the ideal condition for start-up company.

Optoelectronics market is not a new market; in fact it is quite well established. The standard package introduced is a cooperation of new technology and existing technology. According to the figure above, our business then lies in the death zone for start-ups. Therefore, the idea of starting up a company and manufacturing the product does not sound really solid. For a startup company, it is thus better to start by doing IP business model rather than manufacturing model. However, IP model is unlikely to make the package as standard since IP creates barrier to entry and will prevent industry wide usage of the package. For an ongoing company in the industry, it is recommended to do the manufacturing model of business. Being manufactured by a big company, high volume of standard package will be created and the application of standard can be enforced industry wide. Additionally, according to the matrix above, the standard package classify as a sustainable force to the market. This makes the ongoing company to have an advantage of implementing the standard rather than a start up company. Intel, Agilent, Analog Devices, Fairchild and other big players in the market might be the right options for the standard to be implemented. Intel

reported their sales to be $39 billion USD last year, while Agilent, Analog Devices and Fairchild reported $5 billion, $2.4 billion, and $1.5 billion USD respectively.

4 Road to Standardization

For the standard package to be implemented industry wide, a number of parties have to come together and collaborate. As a first step, it is vitally important that the industry team up to formulate the standard. The MIT Communications Technology Roadmap is a good start to the level of cooperation that is needed, however, to achieve universal buy-in path laid by the roadmap, the work and conclusions of the CTR should be subject to industry wide review whenever possible. Publication in widely circulated industry journals is one way to achieve this review. The other component of cooperation concerns changing the cultural norms of the OEM industry and providers. It will take a paradigm shift in corporate expectations to accept a device that may not be optimal for the desired network in exchange for a more viable components industry.

During this transition period, the industry must be able to survive. Consolidation is going to happen in the industry for it to happen. Currently, there are too many firms chasing too little demand. Industry must consolidate and downsize so that remaining firms have economic critical mass. However, consolidation alone is unlikely to complete solving current industry problems.

Interaction of industry and government is likely needed. Regulation, in this case, government plays a vital role as well in this process. Regulators must provide fair competition in the market. The corresponding infrastructure needs to be controlled as well by the regulators to allow the standard package to be applied. Nevertheless, in the long term, industry must be able to support itself without government involvement and without government investment subsidies. This outcome can only occur if demand grows sufficiently and industry consolidates so individual firms are profitable enough to attract money for research and development.

A thought on another way of implementing the standard package, instead of convincing big industry players to manufacture it and pay some performance penalty, is by introducing it to the government. The government in this case may not be necessarily United States or the big ones. Assuming that it is easier to convince one or two people in the government rather than the whole industry, this method sounds a little bit easier to be done. However, the drawback is that a very costly infrastructure needs to be developed in that country, hence big investment. That being said, if the result of standardization in the country would later found to be very good, the industry seeing this might be more interested in implementing the standard. From there, the standard could then be implemented industry wide, eventhough it is somehow a little bit risky to build the whole infrastructure only to show the industry the impact of standardization. Nevertheless, this method is worthwhile to be considered.

The new market, as has been analyzed in the previous section, is likely to be information system, data computing, and servers. By penetrating into these markets, the demand curve can be shifted outwards and thus the demand is increased.

What needs to be taken into caution in developing the standard package is the possibility of this standard package in becoming just another custom package. Currently, there are too many standards, or at least what they call standard, available in the market until we no longer know for sure which one is the real standard. This condition is surely not what we are expecting from the standard package we are designing. Therefore, as have been emphasized over and over, different parties consisting of industry, academics and government need to work together to analyze the design, performance and capabilities of this standard package.

Another difficulty is going to be the price performance on apple-to-apple basis against existing technologies. The competing technologies, which are more heterogeneous aggregation of different technologies, sort of tightly packaged, are

pretty mature and pretty cost effective. For system designers, the important thing is not really the technology, but how to communicate data from place to place as cheaply and reliably as possible. With the above suggestions being done and price competition overcome, industry wide application of the package can only then be fulfilled.

Chapter Five: Conclusion and Future Recommendations

1 Conclusion

Electrical connections are having a problem with the increasing data rates. The shift to optoelectronic connections and devices is inevitable. However, optoelectronics industry is experiencing a high package cost. Either high product variation or complexity of processing steps may cause this. However, standardization has been shown in analysis to be able to overcome the situation. Therefore, standard package for optoelectronic devices is needed to drive the volume up and introduce economies of scale and finally reduce the cost of package.

Market analysis has been done and it is shown that there are huge market opportunities for the standard package. Based on the market data, DIP-like or BGA-like and butterfly-like package is obtained to be the market answer for standard package design. MIT Tb/s silicon platform has been chosen to be the transceiver used in the standard package. Based on technology analysis, technical requirements on data rate, optical channels and power dissipation have been set. As a result of the analysis, systems-in-package adds in to the requirement. Finally, after analyzing the technical requirements with the market answer, we have come out with the standard package requirements, which are surface mounted with systems in package.

In terms of business model, manufacturing model done by big ongoing company in the industry has been chosen as the best way to implement the standard as wide as possible. Calculation shows that the manufacturing model is more profitable than IP model and the sustainability nature of the manufacturing model is more advantageous than IP model's. Finally, industry wide cooperation as well as government regulation is very significant in the success of the standard package to serve its purposes, plus the ability of the industry to level the competition.

Factors affecting the standard package as well as our proposed path to standardization are schematically summarized in the following fishbone diagram. It is our hope that the diagrams give a brief but complete picture on what are needed in order to guide the standard package materialization.

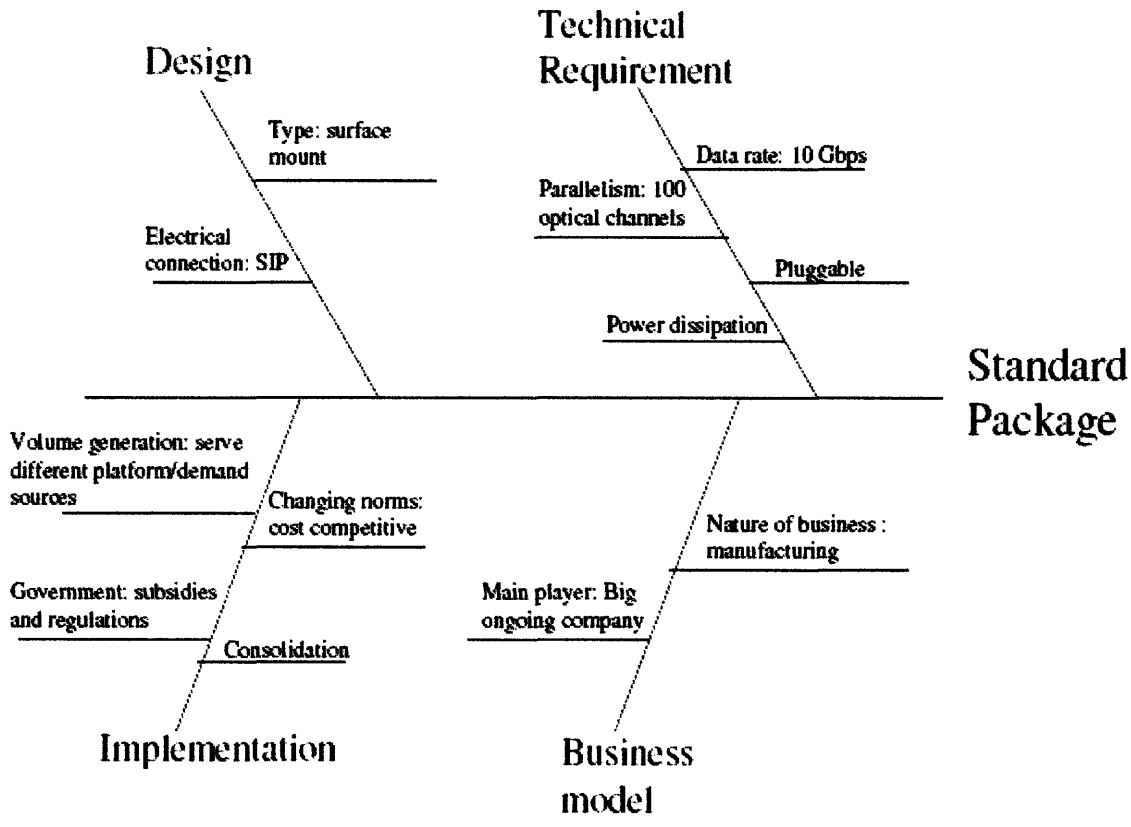


Figure 32 Fishbone diagram showing factors attributing to the success of the standard package materialization.

2 *Future Recommendations*

Having done all the analysis, there are still a lot of things need to be settled on before the standard package can be introduced into the market. Continual work in the research and consortium, MIT CTR in this case or probably the introduction of another consortium, need to be done in the preparation of the standard package.

First of all, of course, the standard transceiver needs to be fully materialized as it has been proven to be working in the research state. The idea of hybrid electronic photonic integrated circuit really relies on the condition that the transceiver is able to perform the way the research proposed and the industry required. Once that is possible to be done, or might as well simultaneously, the standard package needs to be materialized. Hopefully, the analysis done in this thesis report could be a significant guidance in designing the standard electronic photonic package. That includes the physical design as well as the performance specifications. Rigorous research in the industry as well as university would be a very good start in the introduction of the standard package.

As have been stated before, more focused study on the intellectual property is also really critical. It is surely not desired to design a package that will impinge claims on someone's intellectual property. Even if that claims turn to be one of the important factors for the standard package, it is better to approach the owner in the first place and probably better research towards the package could be done.

In terms of what CTR can do in the future, it is not necessarily needed to identify the appropriate level of modularization of the industry. It doesn't necessarily need to be the organization to define things, but instead it can bring the right parties in the room. More industry participation could be encouraged by CTR, inviting more people from industry by showing the advantages of the roadmap. Having said that, academics and researchers are still needed to be brought by CTR to do a collaborative work, which can be optimized. The professors could give insight on what theoretically feasible, the researchers give contribution on what can or cannot be happening in the research state, and the industry people give insight on what is practically happening and what is needed and feasible in the future direction. With this discussion, the progress towards the goal could be made at a higher rate.

With all the future works being done, it is highly possible that in the near future we could really see the standard package play into action in the optoelectronic market.

We surely hope from this, the advancement of technology can progress significantly and the health of optoelectronic industry could be brought to the level where they used to be.

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Appendix I: The Questionnaire

The goal of the questionnaire is to be able to answer following questions:

- What is the current state of packaging technology in the market and the level of standardization in packaging?
- If standardization is found to be lacking, what are the reasons behind this condition or the barriers towards standardization?
- What are the industry's expectations on standard package, in terms of performance and cost, for them to use it?

The questions:

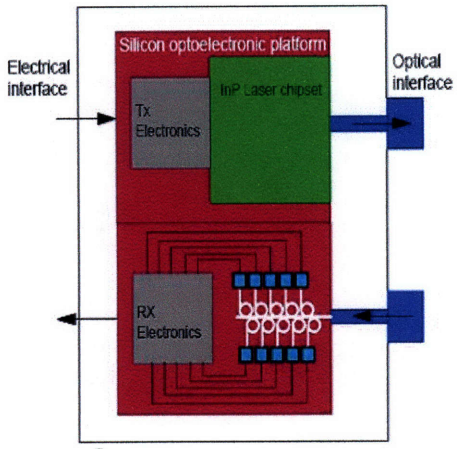
- Currently and within the next two years, what types of OE products does your organization produce?
    - If high # of products, which one would you classify as your main product?
- Do you produce the OE packages you use or do you buy them?
- How many types of OE packages do you use? What percentage are standard packages? Are any pluggable?
    - If small % of standard packages: Why do you use custom packages rather than standard packages? What are the features that you do not find in standard packages?
- Do you manufacture most products (chip, sub-assembly, package) internally or at a Contract Manufacturer? What is the ratio?
- For internally manufactured products (chip, sub-assembly, package), what is your manufacturing capacity utilization (as percentage of full usage, 3 shifts)?
- What percent of your cost is from the chip, from packaging, and from testing (of chip and packaged component)?

- In an optimistic scenario, what would you expect to see happen to the average price of a package in 3, 5, 10 years? Which barriers would have to be overcome for this to happen?
- What kind of performance would you want to see in the package, say, in terms of power dissipation?
- What are your thoughts on hybrid electronic-photonic ICs (EPICs)? Do you see hybrid EPICs to have a significant role or any benefit in the next year or two? What are the barriers in hybridizing electronics and photonics (material issues [III-V vs. Si], integration, bonding technology, other material problems, cost, etc.)?
- Have you used any OE/EO chip to achieve EPIC-based module?
    - IF YES: In what application do you use it? What type of module do you produce (# optical I/O ports, wavelength, waveguide vs. fiber, SM vs. MM, parallel vs. WDM, signal bandwidth, distance, multicast ability, pluggability & number of insertions, environment [temperature, vibration], required lifetime, electrical & optical power budgets, cost)? What was the main challenge in getting to this point, what are the barriers for further integration, and what cost & performance advantages do you expect to see realistically if barriers are overcome?
    - IF NO: Do you anticipate using at some point an OE/EO chip (cartoon on next slide as example) to achieve an EPIC-based module?
        - IF YES: In what application would you use it (compute, server interconnect, telecom, etc)? What type of EPIC-based module do you anticipate needing in 3,5,10 years (# optical I/O ports, wavelength, waveguide vs. fiber, SM vs. MM, parallel vs. WDM, signal bandwidth, distance, multicast ability, pluggability & number of insertions, environment [temperature, vibration], required lifetime, electrical & optical power budgets, cost expectation)?
        - IF NO: Why not?

OE/EO chip cartoon shown:

OE/EO chip

- MIT Tb/s silicon platform
- InP Laser: up to 40 Gbps
- Ge/Si detector: approaching 100 Gbps
- Monolithic integration



Appendix II: Quantitative Analysis

1 *Vensim PLE*

Referring to Figure 23 on revenue model, following are the formulations and assumptions of the model.

(01) Bit rate=10

Units: gbps

(02) Cost per unit per Gbps=INTEG (-Cost reduction, 5)

Units: dollars/(unit*gbps)

(03) Cost reduction=cost reduction rate*Cost per unit per Gbps

Units: dollars/(Year*unit*gbps)

(04) cost reduction rate=0.3

Units: 1/Year

(05) FINAL TIME = 2010

Units: Year

The final time for the simulation

(06) Increase in market share=0.006

Units: 1/Year

(07) "Increase in market share (IP)"=0.05

Units: 1/Year

(08) INITIAL TIME = 2005

Units: Year

The initial time for the simulation

(09) Licensing Payment=Licensing rate*"Market Share (IP)"*Market size

Units: dollars/Year

(10) Licensing rate=0.05

Units: 1/Year

(11) Licensing Revenue=INTEG (Licensing Payment, 0)

Units: dollars

(12) Manufacturing Revenue=INTEG (Revenue addition, 0)

Units: dollars

(13) Market growth=Market size*Market growth rate

Units: dollars/Year

(14) Market growth rate=0.055

Units: 1/Year

(15) "Market Share (dollars)"="Market Share (percentage)"*Market size

Units: dollars

(16) "Market Share (IP)"=INTEG ("Increase in market share (IP)", 0.1)

Units: 1

(17) "Market Share (percentage)"= INTEG (Increase in market share, 0.001)

Units: 1

(18) Market size= INTEG (Market growth, 7.5e+010)

Units: dollars

(19) Price per unit per Gbps= INTEG (-Price reduction, 10)

Units: dollars/unit/gbps

(20) Price reduction=0.5

Units: dollars/(unit*gbps*Year)

(21) Profit per unit per Gbps=Price per unit per Gbps-Cost per unit per Gbps

Units: dollars/(unit*gbps)

(22) Revenue accumulated =A FUNCTION OF (Licensing Revenue, Manufacturing Revenue)

Units: dollars

(23) Revenue addition=Sales*year factor

Units: dollars/Year

(24) Revenue per year = A FUNCTION OF (Licensing Payment, Revenue addition)

Units: dollars/Year

(25) Sales=Price per unit per Gbps*Sales Volume associated*Bit rate

Units: dollars

(26) Sales Volume associated="Market Share (dollars)"/(Price per unit per Gbps*Bit rate)

Units: unit

(27) SAVEPER = TIME STEP

Units: Year [0,?]

The frequency with which output is stored

(28) TIME STEP = 1

Units: Year [0,?]

The time step for the simulation

(29) year factor=1

Units: 1/Year

2 *Microsoft Excel*

Following are the data used for the Microsoft Excel calculation in net present value analysis and sensitivity analysis. The data is inserted to be as equal it is in giving the result as Vensim PLE.

Free IP model

Year	2005	2006	2007	2008	2009	2010
Market growth	0.055	0.055	0.055	0.055	0.055	0.055
Market size	$75,000,000,000.00	$79,125,000,000.00	$83,476,875,000.00	$88,068,103,125.00	$92,911,848,796.88	$98,022,000,480.70
Increase in market share	0.05	0.05	0.05	0.05	0.05	0.05
Market share	0.1	0.15	0.2	0.25	0.3	0.35
Licensing Rate	0.05	0.05	0.05	0.05	0.05	0.05
Licensing Revenue (per year)	$375,000,000.00	$593,437,500.00	$834,768,750.00	$1,100,851,289.06	$1,393,677,731.95	$1,715,385,008.41
Licensing Revenue (accumulated)	$375,000,000.00	$968,437,500.00	$1,803,206,250.00	$2,904,057,539.06	$4,297,735,271.02	$6,013,120,279.43

Manufacturing model

Cost per unit	$5.00	$3.50	$2.45	$1.72	$1.20	$0.84
Price per unit	$10.00	$9.50	$9.00	$8.50	$8.00	$7.50
Profit per unit	$5.00	$6.00	$6.55	$6.79	$6.80	$6.66
Increase in market share	0.006	0.006	0.006	0.006	0.006	0.006
Market share (percentage)	0.001	0.007	0.013	0.019	0.025	0.031
Market share (dollars)	$75,000,000.00	$553,875,000.00	$1,085,199,375.00	$1,673,293,959.38	$2,322,796,219.92	$3,038,682,014.90
Sales Volume associated	7500000	58302631.58	120577708.3	196858112.9	290349527.5	405157602
Manufacturing Revenue (per year)	$37,500,000.00	$349,815,789.47	$789,783,989.58	$1,335,682,295.81	$1,974,231,612.17	$2,698,207,824.07
Manufacturing Revenue (accumulated)	$37,500,000.00	$387,315,789.47	$1,177,099,779.06	$2,512,782,074.86	$4,487,013,687.03	$7,185,221,511.11

Net Present Value (IP)	$4,448,485,804.70	Discount rate	10.00%
Net Present Value (Manufacturing)	$5,035,547,800.32		
Difference in NPV (IP-Manufacturing)	-$587,061,995.62		