Transport in Thin-Body MOSFETs Fabricated in Strained Si and Strained Si/SiGe Heterostructures on Insulator

by

Ingvar Åberg

M.S., Engineering Physics
Lund University, January 2001

Submitted to the
Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements
for the degree of

Doctor of Philosophy in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2006

© 2006 Massachusetts Institute of Technology
All rights reserved

Signature of Author____
Department of Electrical Engineering and Computer Science
March 17, 2006

Certified by____
Judy L. Hoyt
Professor of Electrical Engineering
Thesis Supervisor

Accepted by____
Arthur C. Smith
Professor of Electrical Engineering
Chairman, Department Committee on Graduate Students

Transport in Thin-Body MOSFETs Fabricated in Strained Si and Strained Si/SiGe Heterostructures on Insulator

by

Ingvar Åberg

Submitted to the Department of Electrical Engineering and Computer Science
on March 17, 2006 in partial fulfillment of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering and Computer Science

Abstract

The combination of channel mobility enhancement techniques such as strain engineering, with non-classical MOS device architectures, such as ultra-thin body or multiple-gate structures, offers the promise of maximizing current drive while maintaining the electrostatic control required for aggressive device scaling in future CMOS technology nodes. Two structures that combine strain engineering and new materials with the ultra-thin body silicon-on-insulator (SOI) technology are examined primarily from the point of view of hole mobility: (1) strained Si directly on insulator (SSDOI), and (2) strained Si/SiGe (with 46-55% Ge)/strained Si heterostructure-on-insulator (HOI).

In SSDOI, high strain levels are required to obtain hole mobility enhancements at both low and high inversion charge densities. As the strained Si channel thickness is reduced below 8 nm, hole mobility in SSDOI decreases, as in unstrained SOI. The hole mobility of 3.9 nm-thick 30% SSDOI is still enhanced compared to hole mobility in 15 nm-thick unstrained SOI. Below 4 nm thickness, hole mobility in SSDOI decreases rapidly, which is found to be due to scattering from film thickness fluctuations. Comparisons between SSDOI of two strain levels indicate benefits of strain engineering down to 3 nm thickness.

The hole mobility in HOI is improved compared to that in SSDOI, due to the high hole mobility in the $Si_{1-z}Ge_z$ channel. The mobility enhancement is similar at low and high hole densities even at moderate strain levels. The hole mobility in HOI with SiGe channel thickness below 10 nm is observed to follow a similar dependence on channel thickness as hole mobility in SSDOI. Simulations of electrostatics in HOI and SSDOI with ultra-thin channel thicknesses indicate similarities in the confinement of the inversion charge in ultra-thin body HOI and SSDOI. This suggests that the similar reduction of hole mobility in HOI and SSDOI with 4-10 nm-thick channels is associated with an increase in phonon scattering from the reduced effective channel thickness.

Thesis Supervisor: Judy L. Hoyt
Title: Professor of Electrical Engineering

Acknowledgments

A great number of people have contributed to the preparation of this thesis. First, I would like to thank Professor Judy L. Hoyt who served as my advisor throughout my time at MIT. Many of the ideas that are now incorporated in this thesis or perhaps in future theses were the product of frequent and inspiring meetings that always seemed brief, though the clock told differently. Judy's enthusiasm and leadership created a work environment in which I was able to achieve things I am very proud of, enabled me to participate as presenter or visitor to international conferences, and allowed me to balance work with life outside of MIT.

The thesis readers, Professor Jesus A. del Alamo and Professor Dimitri A. Antoniadis contributed and enhanced the final product by their insightful suggestions and comments, through the joint research programs and indirectly by keeping a wealth of talent in their groups, from which I learned a lot.

I was fortunate to interact with Professor Tayo Akinwande trough my teaching assignment in 6.012, he gave an example for excellence in both teaching and research. At conferences, I met with Professor Shin-ichi Takagi of University of Tokyo, whom I thank for interesting discussions about scattering during the preparation of this thesis. For the same reason, I would like to thank Professor Mark Lundstrom at Purdue, who kindly provided further insight into some equations of his book on carrier transport.

The staff at MTL served me well during my many and intense process lots. Without proper tool, clean-room, and facilities maintenance, high-level research would not be possible. Often I had the chance to interact with Dr. Vicky Diadiuk, in particular during the PTC meetings, where I learned a lot about the fab. Some of her excellent staff members deserve special mentioning for the above-and-beyond type of support and instruction they gave, or while working on some particular issue relating to my processes: Bernard Alamariu, Brian McKenna, Paul Tierney, Bob Bicchieri, Eric Lim, Donal Jamieson, Joe Walsh, Dan Adams, Tim Turner, and Dave Terry. I thank Sam Crooks for getting the money in so Debb Hodges-Pabon and her social teams could create wonderful events such as the MTL reviews and summer barbecues.

The Hoyt group in its past and present form has, of course, contributed tremendously. Gary Riggott grew the wafers for this project, using recipes developed in large part by Oluwamuyiwa Olubuyide. Celia Mokalled, Lindsay Petrillose, and Rose Previte each helped with the administrative tasks so I wouldn't have to. Cait Ni Chleirigh contributed some of the simulations of this thesis. Tonya Drake developed the original 4" SSDOI substrate process at MIT, and trained me on many of the process steps, which made it easier to transfer the process to 6". Guangrui (Maggie) Xia, Leo Gomez, Meekyung (MK) Kim, Nicole DiLello, and Pouya Hashemi helped review too long presentations during group meetings, as did our visiting research affiliates through the years: Dr. Satoshi Eguchi, Dr. Scott Yu, Dr. Kosuke Kusakari, and Dr. Ryan Lei.

From Dimitri's group, Osama Nayfeh helped with some simulation work, and I appreciate discussions with Ali Khakifirooz regarding tight binding simulations on UTB-

SSDOI. I learned many processing tricks from Dr. Isaac Lauer and inherited his mask set. From Prof. Fitzgerald's group, I owe thanks especially to Dr. Larry Lee, Dr. Arthur Pitera, and Saurabh Gupta for discussions about SiGe. I would like to acknowledge Dr. Charles Cheng and his Amberwave Systems friends for interesting discussions.

The clean-rooms in MTL, and the "6th floor" is a great place to be because of the great friendships that develop while waiting for processes to finish, or while having lunch. In addition to those mentioned above, Dennis Ward, Niamh Waldron, Dr. Nisha Checka, Dr. Chuan-Seng Tan, Joyce Wu, Anita Villanueva, Dr. Dae-Hyun Kim, John Hennessy, Jae-Kyu Lee, Andy Fan, Andrew Ritenour, Dr. Luis Velasquez-Garcia, Ole Nielsen and honorary Hoyt group affiliate Oliver Donnelly are just some of those who I had the privilege to spend time with at or after work. From my time in the Tang and GSC student governments, I want to recognize all the friendships and experiences I had by interacting with various MIT and student administrative and community building functions.

I thank the MARCO MSD Focus Center, and the SRC for providing financial support to this research. I thank Applied Materials for the graduate fellowship that supported me for part of my time at MIT.

Finally, I would like to thank my family for the support they have given me and my siblings. My parents always supported us to academic achievement and to work hard to achieve our goals. I was honored that my parents traveled far to be present at the defense of this thesis. Most of all, I thank my wife and love, Ana Paula for her continuous support and love. As I end the Ph.D. student chapter of my life, it is a great comfort to know that you will be with me as we enter a new phase of our life together.

Contents

Chapter 1 21
Introduction 21
1.1 The MOSFET 22
The Long Channel MOSFET 24
1.2 Chapter Summary 25

Chapter 2 27
Introduction to Strained Si and SiGe Heterostructure MOSFETs 27
2.1 Biaxially Strained Si and SiGe 28
Biaxial Strain 28
Valence Band Structure of Biaxially Strained Si and SiGe 32
Mobility in Bulk Strained Si/SiGe MOSFETs 36
2.2 Uniaxial Strain 40
2.3 Phonon Scattering and Transport in UTB SOI MOSFETs 42
Theoretical Background 43
Observed Mobility in UTB SOI MOSFETs 47
2.4 Effective Mobility Extraction 48
2.5 Chapter Summary 52

Chapter 3 53
Substrate Fabrication and Characterization 53
3.1 The Epitaxial Growth Process 54
3.2 Bond and etch-back 58
3.3 Chapter Summary 62

Chapter 4 63
Strained Silicon Directly on Insulator MOSFETs 63
4.1 The MOSFET device fabrication process 64
4.2 Basic Device Results 69
4.3 Mobility of moderately thin SSDOI MOSFETs 72
SSDOI Electron Mobility 74
SSDOI Hole Mobility 75
4.4 The Ultra-thin Body SSDOI p-MOSFET 77
Device Fabrication 77
Strained Si Thickness Extraction 80
Mobility of the UTB SSDOI p-MOSFET 83
4.5 Chapter Summary 90

Chapter 5 93
Strained Si/SiGe Heterostructure on Insulator MOSFETs 93
5.1 The HOI Structure 94
5.2 The HOI MOSFET fabrication process 96
5.3 Basic Device Results 98
Extraction of the strained Si cap thickness 100
5.4 Mobility of the HOI MOSFET 102
The HOI n-MOSFET 103
The HOI p-MOSFET 104
5.5 Thermal Processing and Mobility of HOI 110
5.6 Chapter Summary 112

Chapter 6 113
Hole Transport in Ultra-thin Body HOI MOSFETs 113
6.1 Device Fabrication 115
6.2 Basic Mobility and Device Results 118
6.3 Off-state Leakage Current 122
6.4 Mobility of the Ultra-thin Channel HOI p-MOSFET 128
6.5 Chapter Summary 134

Chapter 7 137
Summary and Suggestions for Future Work 137
7.1 Thesis Summary 137
Strained Si Channel Devices 138
Strained SiGe Channel Devices 139
Technological Implications 141
7.2 Contributions 142
New heterostructure materials development: 143
Research on SSDOI MOSFETs: 143
Research on HOI MOSFETs: 144
7.3 Suggestions for Future Work 145
Structures, Substrates and Patterning 145
Electron Transport 146
Hole Transport 147

Appendix A 149
Average Vertical Field in HOI and 149
Influence of Series Resistance on Field Effect Mobility in UTB-MOSFETs 149
A.1 Average Vertical Field in HOI 150
A.2 Charge Allocation in HOI 154
A.3 Field Effect Mobility at High Parasitic Series Resistance 158

Appendix B **163**
SSDOI and HOI Substrate Fabrication Flow **163**
B.1 Low-T Bond 163
B.2 Etch-Back 165

Appendix C **167**
Device Fabrication Flow **167**
C.1 The HOI MOSFET Device Flow 167

Bibliography **173**

List of Figures

Figure 1.1 Sketch of an SOI MOSFET. 22

Figure 2.1 SiGe/Si strained layer epitaxy.................... 29
Figure 2.2 Definition of indices for stress and strain components.................... 31
Figure 2.3 Valence bands in bulk Si from k.p calculations.................... 34
Figure 2.4 Valence bands in strained Si from k.p calculations. 35
Figure 2.5 Valence bands in strained $Si_{0.45}Ge_{0.55}$ (on relaxed $Si_{0.75}Ge_{0.25}$) from k.p calculations. 35
Figure 2.6 The strained Si/relaxed SiGe n-MOSFET. 37
Figure 2.7 Strained Si and strained SiGe p-MOSFET mobilities. 38
Figure 2.8 The Si bulk HH band with **(a)** no applied stress and **(b)** 1GPa uniaxial compressive stress in the <110> direction from k.p calculations. 42
Figure 2.9 The infinite well approximation and the piecewise constant DOS in **(a)**, and **(b)** the sub-band separations for thick and thin SOI. 45
Figure 2.10 Qualitative sketch of how the phonon scattering mechanisms would affect electrons and holes. 48
Figure 2.11 Example of parasitic resistances extracted on p-MOSFETs with ultra-thin Si thickness (without recessed gates or raised source/drains). 50
Figure 2.12 The mobility extraction MOSFET used in this work. 50

Figure 3.1 The **(a)** SSDOI and **(b)** HOI structures.................... 55
Figure 3.2 The HOI fabrication process.................... 55
Figure 3.3 Nomarski micrograph (the view is 170 μm x 205 μm) of an as grown $Si_{0.6}Ge_{0.4}$ buffer layer after defect etching. 57
Figure 3.4 The etch rate of $Si_{1-y}Ge_y$ in SC-1 at 80ºC as a function of Ge content y of the layer.................... 60

Figure 3.5 Atomic force micrograph of a 40% SSDOI substrate.............................. 61

Figure 4.1 The general process flow for fabrication of MOSFETs on SSDOI or HOI substrates.. 65
Figure 4.2 XTEM of 30% SSDOI long channel device with 15 nm-thick body. 68
Figure 4.3 Long channel drain current (I_D) vs. drain bias (V_D) for **(a)** a 25% SSDOI n-MOSFET (approximately 17 nm thick strained Si layer) and for **(b)** a 30% SSDOI p-MOSFET (approximately 25 nm thick strained Si layer)......... 69
Figure 4.4 **(a)** Drain current (I_D) vs. gate bias (V_G) for a W=50 µm, L=1 µm 25% SSDOI n-MOSFET. **(b)** I_D vs. V_G for a W=50 µm, L=1 µm long 30% SSDOI p-MOSFET.. 71
Figure 4.5 Gate-to-channel inversion capacitance of a 25 nm thick 30% SSDOI p-MOSFET.. 72
Figure 4.6 Hole mobility of 13 nm thick 30 % SSDOI p-MOSFET......................... 73
Figure 4.7 **(a)** Electron effective mobility of 25% and 30% SSDOI (~15 nm thick) as a function of effective electric field. **(b)** Hole effective mobility of 30% SSDOI (8 nm thick) and 40% SSDOI (14 nm thick) vs. E_{eff}. 74
Figure 4.8 Peak hole mobility (low field mobility) as a function of strained Si layer thickness for 30% SSDOI. 77
Figure 4.9 Selective thinning of gate regions for ultra-thin body MOSFETs............ 78
Figure 4.10 The etch step time for the (over-) etch of strained Si in SC-1. 79
Figure 4.11 Simulated (lines) and measured (symbols) *C-V* of 3.2 nm thick 30% SSDOI at two back-bias conditions. 82
Figure 4.12 XTEMs of **(a)** 3.1 nm-thick 40% SSDOI, and **(b)** 1.4 nm-thick 30% SSDOI. 82
Figure 4.13 Sub-threshold characteristics of 40% SSDOI p-MOSFET with 3.1 nm-thick strained Si layer.. 83
Figure 4.14 **(a)** Hole mobility vs. effective field for unstrained SOI control devices of this work (symbols), and from Ref. [60] (lines, labeled with *). **(b)** Hole

mobility vs. effective field for 30% SSDOI with ultra-thin strained Si thickness (the thickness is indicated) of this work.................................. 84

Figure 4.15 Hole mobility vs. film thickness at a vertical effective field of 0.5 MV/cm for the 30% SSDOI of this work and the unstrained SOI from Uchida, et al. [60].. 84

Figure 4.16 Thickness fluctuation induced scattering... 86

Figure 4.17 The hole mobility vs. inversion charge density for a range of .temperatures for **(a)** 7.2 nm-thick 30% SSDOI and **(b)** 3.5 nm-thick 30% SSDOI. **(c)** For the 7.2 nm-thick SSDOI the mobility vs. temperature increases monotonically as the temperature is lowered, while for the 3.5 nm-thick SSDOI mobility is relatively constant. 87

Figure 4.18 Hole mobility vs. vertical effective field for 30% SSDOI and 40% .SSDOI with two, pair-wise matched thicknesses... 90

Figure 5.1 The HOI structure. 95

Figure 5.2 The experimental splits.. 96

Figure 5.3 SIMS of HOI.. 97

Figure 5.4 XTEM of HOI MOSFETs. 99

Figure 5.5 **(a)** Drain current vs. gate bias for a long channel HOI p-MOSFET with thick strained Si cap. **(b)** The sub-threshold swing vs. Si cap thickness. . 99

Figure 5.6 Gate-to-channel inversion capacitance for HOI. 101

Figure 5.7 Experimental n-MOSFET effective mobility as a function of electron density for 46/25 HOI, 25% and 30% SSDOI and SOI......................... 103

Figure 5.8 Experimental p-MOSFET effective mobility as a function of hole density for 46/25 HOI with 2 nm cap thickness, 30% and 40% SSDOI (from Chapter 4) and SOI. 105

Figure 5.9 Effective hole mobility as a function of hole density of 46/25 HOI (triangles) with 4 and 2 nm cap thickness, and 35/25 HOI (circles) with 4 nm cap thickness... 105

Figure 5.10 Simulation of the hole distribution between the strained Si cap (to the left of the divider line) and the $Si_{0.54}Ge_{0.46}$ layer (to the right) for three different cap thicknesses and at N_{inv}=1x10^{13} cm^{-2}. 107

Figure 5.11 Hole mobility as a function of Si cap thickness at N_{inv}=1x10^{13} cm^{-2}. The cap thicknesses were extracted from analysis of *C-V* characteristics, as .. in Figure 5.6. 107

Figure 5.12 Hole mobility vs. Si cap thickness. 108

Figure 5.13 The mobility enhancement factor of 46/25 HOI relative to an ideal un-strained FD-SOI mobility, derived from the universal mobility............ 109

Figure 5.14 Hole mobility in HOI after aggressive thermal annealing. 111

Figure 6.1 Simulated p-MOSFET sub-threshold slope vs. effective channel length, using Dessis. 114

Figure 6.2 **(a)** Low energy (300 eV) SIMS of ultra-thin channel HOI. **(b)** Raman spectroscopy intensity (laser λ=442 nm) of HOI vs. wave number after MOSFET fabrication. 117

Figure 6.3 XTEM of HOI with SiGe layer thickness of 4 nm and top cap thickness of 5 nm. 117

Figure 6.4 **(a)** Electron effective mobility of moderately thin HOI vs. inversion layer density. **(b)** Hole effective mobility of moderately thin HOI vs. inversion layer density. 119

Figure 6.5 **(a)-(c)** Simulated and measured *C-V* for 55/25 HOI with 10, 6, and 4 nm buried SiGe thickness and 5 nm cap thickness. **(d)** Measured *C-V* of 55/25 HOI with 10 and 4 nm SiGe thickness with applied back bias.............. 121

Figure 6.6 I_D vs. V_G characteristics for **(a)** electrons and **(b)** holes in long-channel 25% SSDOI and 55/25 HOI MOSFETs with n+ poly-Si gates. 123

Figure 6.7 Off-state leakage (I_{LEAK}) vs. drain bias (V_D) for n- and p-MOSFETs. 123

Figure 6.8 Temperature dependence of off-state current (I_{LEAK}) of a 55/25 HOI p-MOSFET with 4 nm-thick $Si_{1-z}Ge_z$ layer... 124

Figure 6.9 XTEM of 55/25 HOI p-MOSFET gate edge region. 125

Figure 6.10 (**a**) Off-state leakage current vs. strained Si cap thickness. (**b**) Off-state leakage current vs. thickness of the $Si_{1-z}Ge_z$ layer for 55/25 HOI with a strained Si cap thickness of 5 nm. 127

Figure 6.11 (**a**) Measured hole mobilities in 55/25 HOI with ultra-thin $Si_{1-z}Ge_z$ channels. (b) The mobility enhancement factor at a hole density of $4x10^{12}$ cm^{-2} (low vertical field) vs. thickness of the buried buried $Si_{1-z}Ge_z$ layer thickness.. 129

Figure 6.12 Hole mobility vs. inversion charge density for a range of temperatures for 55/25 HOI with (**a**) 10 nm-thick $Si_{1-z}Ge_z$ and (**b**) 6 nm-thick $Si_{1-z}Ge_z$... 129

Figure 6.13 Hole density profile vs. depth in 55/25 HOI (top part of the figure, (**a**)) and 25% SSDOI (bottom part, (**b**)).. 132

Figure 6.14 The peak hole mobility in 55/25 HOI (from this chapter) and 30% SSDOI (from Chapter 4) vs. the thickness of the channel. 133

Figure A.1 Average vertical field in a 55/25 HOI p-MOSFET with 5 nm-thick strained Si cap and 10 nm-thick buried $Si_{0.45}Ge_{0.55}$ layer. 153

Figure A.2 Experimental, normalized *C-V* for a 55/25 HOI p-MOSFET with 5 nm-thick strained Si cap and 10 nm-thick buried $Si_{0.45}Ge_{0.55}$ layer (right axis), and the simulated (*nextnano³*) fraction of newly generated inversion charge that appears in the strained Si cap (left axis).............................. 155

Figure A.3 Experimental, normalized *C-V* for a 55/25 HOI p-MOSFET with 5 nm-thick strained Si cap and 10 nm-thick buried $Si_{0.45}Ge_{0.55}$ layer (right axis), and the fraction of the total inversion charge that populate the buried $Si_{0.45}Ge_{0.55}$ layer (left axis).. 156

Figure A.4 Average total vertical field and the average field in the Si cap and buried $Si_{0.45}Ge_{0.55}$ layer of a 55/25 HOI p-MOSFET with 5 nm-thick strained Si cap and 10 nm-thick buried $Si_{0.45}Ge_{0.55}$ layer. 156

Figure A.5 Mobility vs. hole density for a 30% SSDOI p-MOSFET. 158

Figure A.6 Mobility vs. hole density for 30% SSDOI p-MOSFETs with 3.9 nm-thick body (open symbols, high series resistance) and ~15 nm-thick body (filled symbols, lower series resistance).. 159

Figure A.7 Calculated series resistance correction factor, γ (unit-less, see Equation A.12), of field effect mobility at the point of maximum effective mobility as a fraction of effective mobility (equation shown as inset), vs. series resistance.. 161

List of Tables

Table 2.1 32
Table 2.2 36

Table 3.1 58

Table 4.1 66
Table 4.2 68
Table 4.3 80

Chapter 1

Introduction

For decades, geometric scaling of metal-oxide-semiconductor (MOS) field-effect transistors (FETs) resulted in a dramatic improvement in device switching speed averaging around 17% per year [1]. The driving force was the reduction of the effective gate length, L_{eff}, while scaling other dimensions and doping profiles to maintain electrostatic control of the channel, despite the sub-100 nm gate lengths. Starting in the 90 nm node (with L_{eff} roughly half of that), the historical rate of improvement in switching speed could only be achieved by substituting the conventional Si channel material with strained Si (see e.g. [2]). The introduction of strain in the Si lattice changes the band-structure to improve the transport properties of both electrons and holes which results in higher transistor drain currents, as will be described in the next chapter. To further improve the performance of complimentary MOS (CMOS) beyond the 90 nm and 65 nm nodes, additional "technology boosters" will be required and further improvements in the original booster, strain, will be needed [1,3]. Some boosters under consideration are metal gates, high-k dielectrics, novel high-mobility materials (perhaps combined with strain), and novel transistor structures such as single gate ultra-thin body silicon-on-insulator (SOI) MOSFETs [4], double gate (e.g. planar [5] or FinFET [6]), or other multiple gate MOSFETs. Any candidate for future technology nodes needs to

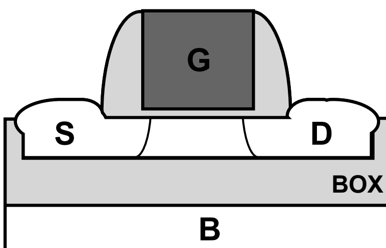

Figure 1.1 Sketch of an SOI MOSFET. The channel between the source (S) and drain (D) terminals is controlled by the gate (G), which is isolated by a gate oxide. When turned on, a current flows through the source and drain terminals. One difference between an SOI MOSFET and a "bulk" MOSFET is the buried oxide (BOX), which electrically separates the back gate (B) terminal from the device.

demonstrate simultaneous enhancement of transport above the present state of the art and ability to control short channel effects [7]. In this thesis, the simultaneous combination of strain, novel materials and ultra-thin body SOI MOSFET technology is studied. In particular, the hole mobility in ultra-thin-body strained Si directly on insulator (SSDOI) and strained Si/SiGe/Si heterostructure-on-insulator (HOI) MOSFETs with channel thicknesses below 10 nm are studied. Before these structures are introduced, the fundamentals of MOSFETs will be reviewed.

1.1 The MOSFET

The MOSFET is the work horse of CMOS technology, and is the most common switch in modern micro-electronic devices. A schematic of a silicon-on-insulator MOSFET is shown in Figure 1.1. In short or long channel devices the drain currents, I_{Dlin} in the linear [8] and I_{Dsat} in the saturation [9] regions are given by scattering theory as

$$I_{Dlin} = WC_{ox} \frac{v_T}{2k_b T/q}(1 - R_{lin})(V_{GS} - V_T)V_{DS}, \quad \text{(Equation 1.1a)}$$

$$\text{with } R_{lin} = \frac{L}{L + \lambda_0} \quad \text{(Equation 1.1b)}$$

$$I_{Dsat} = WC_{ox} v_T \frac{1 - R_{sat}}{1 + R_{sat}}(V_{GS} - V_T), \quad \text{(Equation 1.2a)}$$

$$\text{with } R_{sat} = \frac{l}{l + \lambda_0}, \quad \text{(Equation 1.2b)}$$

where $v_T = \sqrt{2k_b T / \pi m^*}$ is the thermal velocity, R is the channel back-scattering coefficient, L is the channel length, l is the critical length for back-scattering under high bias (a short region near the source), and λ_0 is the mean free path, with the other symbols having their usual meaning, see e.g. [10]. By assuming that mobility is proportional to the mean free path, Lundstrom Ref. [11], showed that the fractional change in drain current in response to a fractional change in mobility is

$$\frac{\delta I_D}{I_D} = \frac{\delta \mu}{\mu}(1 - B), \text{ with} \quad \text{(Equation 1.3a)}$$

$$B_{lin} = \frac{\lambda_0 / L}{1 + \lambda_0 / L} \quad \text{(Equation 1.3b)}$$

$$B_{sat} = \frac{\lambda_0 / 2l}{1 + \lambda_0 / 2l} \quad \text{(Equation 1.3c)}$$

Since $l<L$, even in short channel devices, the drain current in the linear regime has a more direct dependence on mobility than the current in saturation; however, the typical B_{sat} is still ~0.5 in recent experimental devices [11,12], so that even the saturation current

increases if the mobility is improved (in the ballistic limit, it is expected that $B \rightarrow 1$). Though mobility can be extracted from short channel devices [13,14], mobility extraction methods are more reliable and well defined in long channel devices. In this thesis, long channel mobility is studied extensively, but due to Equation 1.3(a) and technological factors, the structures suggested in this thesis ultimately need to be implemented in short channel devices before the actual improvement in drive current or switching speed can be evaluated.

The Long Channel MOSFET

The MOSFETs used for mobility extraction in this work typically have a gate length of 100 μm. At such long channel lengths, the drive current of the MOSFET in the linear and saturation regime is described by

$$I_{Dlin} = \frac{W}{L}\mu_{eff}C_{ox}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \qquad \text{(Equation 1.4)}$$

$$I_{Dsat} = \frac{W}{L}\mu_{eff}C_{ox}\left(V_{GS} - V_T\right)^2 \qquad \text{(Equation 1.5)}$$

The effective mobility, μ_{eff}, (further described in section 2.4) has a universal dependence on the vertical effective field in the channel of a Si transistor [15]. The vertical effective field is given by

$$E_{eff} = \frac{1}{\varepsilon}\left(Q_b + \eta Q_{inv}\right), \qquad \text{(Equation 1.6)}$$

where ε is the dielectric constant of Si (if it is a Si channel transistor), Q_b is the bulk charge (primarily the depletion charge), Q_{inv} is the channel inversion charge, and η is 1/2

for electrons and 1/3 for holes. Intuitively, the effective field can be thought of as the average field in the inversion layer, which is true for Si n-MOSFETs with η=1/2, but not for p-MOSFETs or multiple channel MOSFETs, as detailed in Appendix A. Generally speaking, η could be interpreted as a fitting parameter to achieve a universal mobility condition. In bulk devices both Q_b and Q_{inv} in Equation 1.6 are derived from split capacitance-voltage measurements [16,17], but in fully-depleted SOI devices with thick buried oxides (BOX), Q_b is given by [18]

$$Q_b = T_{Si} q N_A - \frac{\varepsilon_{ox}}{T_{BOX}} V_{BS} \,. \qquad \text{(Equation 1.7)}$$

In Equation 1.7, T_{Si} is the thickness of the SOI layer, q = 1.6x10^{19} As, N_A is the doping concentration of the SOI layer, V_{BS}=V_B-V_S is the back-gate (substrate) to source voltage difference, and T_{BOX} is the BOX thickness. Thus, with a shorted substrate, low doping concentration and thin SOI thickness (as in this work), Q_b is usually small in comparison to Q_{inv} for most of the effective field range, so that the effective field is approximately

$$E_{eff} \approx \frac{\eta Q_{inv}}{\varepsilon} \,. \qquad \text{(Equation 1.8)}$$

1.2 Chapter Summary

In this introduction, the MOSFET transistor was introduced. Despite the small gate lengths in present MOSFET technology, effective mobility continues to be an important parameter for transport.

Thesis Goals and Organization

In this thesis, mobility is studied in MOSFETs that combine strain, novel materials (SiGe), and ultra-thin body silicon-on-insulator technologies. This is motivated by the need in future CMOS technology nodes to further improve transport while introducing structures that scale better than the present-day planar technology. The ultra-thin body SOI MOSFET is the simplest of these structures with better electrostatic control in short channels, and is ideal for transport studies due to the relative ease of fabrication. The strained Si/strained SiGe system is combined with the ultra-thin body technology since research on corresponding bulk heterostructures indicates that high mobility enhancements may be achieved. The goal is to investigate the hole mobility in MOSFETs that combine ultra-thin channels with mobility enhancement techniques. A related goal is to explore the reasons for transport degradation or enhancement in such structures. In particular, the hole mobility in MOSFETs with strained Si or strained SiGe channel thicknesses less than 10 nm will be studied.

In chapter 2, key concepts are introduced from theory, and prior experimental work of relevance to the thesis is reviewed. The mobility extraction methods are introduced. In chapter 3, the fabrication of the strained Si and heterostructure-on-insulator substrates is described. In chapter 4, the transport in thin and ultra-thin body strained Si directly on insulator is discussed. In chapter 5, the heterostructure-on-insulator (HOI) MOSFET is introduced, which is extended to include ultra-thin channel HOI in chapter 6. Contributions to knowledge and suggestions for future work are listed in chapter 7, as part of the thesis summary.

Chapter 2

Introduction to Strained Si and SiGe Heterostructure MOSFETs

In this chapter, strained Si and SiGe heterostructure MOSFETs are introduced. Select background information in the field is presented to put the contributions of this work in context, and to provide the foundation for understanding the material of later chapters. First, the concept of biaxial strain is reviewed and the valence band structure is presented for structures relevant to the later chapters. The mobility in strained Si and strained SiGe heterostructure-on-bulk transistors is discussed. Next, the concept of uniaxial strain is discussed, primarily due to its significance in current CMOS production, but also to inspire the reader to think about paths to further the work of this thesis by combining materials, strain configurations, and novel structures in yet to be conceived ways. One section describes transport in ultra-thin body silicon-on-insulator (SOI) MOSFETs. The increased electrostatic control in SOI MOSFETs with ultra-thin channels motivates the combination of new materials and strain in the ultra-thin body structure. Finally, mobility extraction methods used in this work are presented.

2.1 Biaxially Strained Si and SiGe

In this section, a general introduction to biaxial strain is first given. Next, the band structure of strained Si and strained SiGe is introduced, followed by a discussion of implications for mobility.

Biaxial Strain

Silicon and Germanium are both column IV semiconductors, and have similar crystal structure, the familiar diamond structure [19]. An alloy of Si and Ge can be formed ($Si_{1-x}Ge_x$) in which the Si and Ge atoms are randomly distributed in the lattice to some average Ge fraction x. While the lattice structure is the same for both Si and Ge, there is 4.2% mismatch between the lattice parameters of Si and Ge, as illustrated in Figure 2.1(a). The relaxed SiGe alloy lattice parameter can be estimated reasonably well [20] by linear interpolation of the lattice parameters of Si and Ge (Vegard's law), so that the lattice parameter of a $Si_{1-x}Ge_x$ alloy with a Ge fraction x is

$$a(x) = x * a_{Ge} + (1 - x) * a_{Si} . \qquad \text{(Equation 2.1)}$$

If a thin layer of Si is grown pseudomorphically on an unstrained bulk-$Si_{1-x}Ge_x$ substrate, the lattice of the epitaxially grown Si is stretched in-plane (since the strain is symmetric with respect to the in-plane x and y-axes in Figure 2.2, it is said to biaxial) to match the lattice parameter of the underlying $Si_{1-x}Ge_x$ layer, as shown schematically in Figure 2.1(b). By convention, such a structure is said to be tensily strained, referring to the in-plane strain state. Note that while stretching in the plane parallel to the surface, the

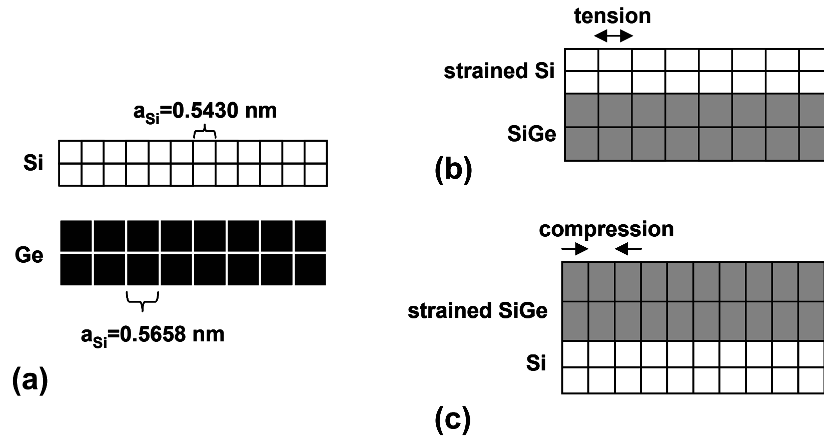

Figure 2.1 SiGe/Si strained layer epitaxy. In **(a)**, the equilibrium lattice constant of Si and Ge is mismatched by 4.2%. When growing strained Si on a relaxed SiGe substrate, the Si lattice is stretched in the plane to match the lattice parameter of SiGe **(b)**, and in **(c)** SiGe is grown strained on a Si substrate.

lattice is compressed in the growth direction. Thus, the in-plane strain, $\varepsilon_{//}$, and the out-of plane strain, $\varepsilon_{\perp}$, are related to the lattice mismatch and Poisson's ratio, υ, by [21]

$$\varepsilon_{\parallel} = \frac{a_s}{a_l} - 1 \qquad \text{(Equation 2.2)}$$

$$\varepsilon_{\perp} = -\frac{\varepsilon_{\parallel}}{\upsilon}, \qquad \text{(Equation 2.3)}$$

where a_s and a_l denote the equilibrium lattice parameters of the substrate and epitaxially grown strained layer respectively (i.e. the lattice parameters of corresponding relaxed layers given by Equation 2.1). Note that in the above equations, the substrate and strained layer can have arbitrary Ge concentrations. To grow a tensily strained layer (recall that by convention, tension refers to the in-plane strain state $\varepsilon_{//}>0$), the Ge concentration of the epitaxial layer is lower than the Ge concentration of the substrate, as in Figure 2.1(b). By analogy, to grow a compressively strained layer ($\varepsilon_{//}<0$) one would

grow a layer with high Ge concentration on a substrate with lower Ge concentration, as in Figure 2.1(c). In the literature, biaxially strained layers are sometimes quoted in terms of their in-plane biaxial strain or lattice mismatch, but a frequent way of quoting a certain biaxial strain technology is in terms of the Ge concentrations of the various layers. For example, rather than quoting a strained Si layer as having $\varepsilon_{//}$=1.26%, one could say "strained Si on relaxed (i.e. unstrained) $Si_{0.7}Ge_{0.3}$". If this is supplemented with experimental strain measurements (e.g. by making sure by Raman spectroscopy that all layers are fully strained, as in chapter 6), quoting Ge concentrations can be more informational. Mobility is not only a function of strain, but also the chemical composition of the layer. In this thesis, Ge composition and strain state is usually quoted by specifying the chemical Ge concentrations of the strained layer and the relaxed SiGe substrate, but this will be clarified in detail in later chapters.

The strain in a semiconductor can be associated with the stress components that cause the lattice deformation through the elasticity tensor. Due to the high level of symmetry in a cubic semiconductor, the tensor relationship can be reduced to the general matrix equation [22]

$$\begin{bmatrix} s_{xx} \\ s_{yy} \\ s_{zz} \\ s_{yz} \\ s_{zx} \\ s_{xy} \end{bmatrix} = \begin{vmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44} \end{vmatrix} \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{yz} \\ \varepsilon_{zx} \\ \varepsilon_{xy} \end{bmatrix} \quad \text{(Equation 2.4).}$$

In the strain components ε_{ij} and stress components s_{ij}, the first index is the direction of the strain or stress, and the second index is the normal direction of the surface this strain or

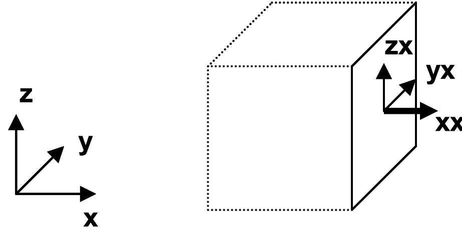

Figure 2.2 Definition of indices for stress and strain components. For example, a stress component s_{yx} is directed in the y-direction on the surface with normal direction in x. Thus, s_{yx} is a shear component.

stress component is applied to, as exemplified in Figure 2.2 (assuming x, y, and z are aligned with the three main crystal coordinates). From this, it is clear that for biaxial strain (with x and y being the in-plane coordinates), $\varepsilon_{xx} = \varepsilon_{yy} = \varepsilon_{//}$ and $\varepsilon_{zz} = \varepsilon_{\perp}$, with all the shear components zero. Since the growth direction (z) is free from stress, the stress and strain in biaxially strained materials are correlated through

$$s_{xx} = (c_{11} + 2c_{12})\varepsilon_{xx} + c_{12}\varepsilon_{zz} \quad \text{(Equation 2.5)}$$

$$\varepsilon_{zz} = -\frac{2c_{12}}{c_{11}}\varepsilon_{xx} \quad \text{(Equation 2.6)}$$

The material constants, c_{ij}, in the elasticity matrix can be found in tables of material properties, see e.g. [23]. In Equation 2.6, c_{11} is referred to as Young's modulus and Poisson's ratio is given in terms of c_{11} in c_{12} by the straightforward combination of Equations 2.3 and 2.6. In this work, stress values will not be used to characterize structures, but are often used in device literature regarding local or uniaxial stress techniques, discussed below. In Table 2.1, calculated stress and strain values are quoted for some of the biaxial films in this work. Very high stress levels can be achieved when introducing biaxial strain by epitaxial growth.

TABLE 2.1
STRAIN AND STRESS IN EPITAXIAL LAYERS IN THIS THESIS

Ge concentration of relaxed buffer	Ge concentration of layer	Strain in layer[a,b] (%)	Stress in layer[a] (GPa)
25%	0%	1.05	1.9
30%	0%	1.26	2.3
40%	0%	1.68	3.0
25%	46%	-0.86	-1.4
25%	55%	-1.23	-1.9

[a]Tensile if positive, compressive if negative
[b]In-plane
Elastic constants were interpolated linearly between Si and Ge.

Due to the high stress levels in typical devices, the thickness of the grown stressed layers has to be kept below the critical thickness, or in the metastable regime to avoid strain relaxation by the introduction of threading dislocations [24,25]. Sometimes, defects are introduced intentionally, in order to relax epitaxial layers. In the graded buffer layer technique (used to create relaxed SiGe layers, see e.g. [26,27,28]), the concentration of Ge in the $Si_{1-x}Ge_x$ alloy is graded linearly while allowing the lattice to relax. This reduces the density of dislocations that thread up into the top (device) portion of the epitaxial layer structure. The fabrication sequence for the wafers of this work is further described in Chapter 3. Besides the graded buffer technique, relaxed SiGe layers can also be created by the related internal-oxidation and Ge condensation [29,30,31] methods.

Valence Band Structure of Biaxially Strained Si and SiGe

The band structure of Si as well as SiGe changes with the application of biaxial strain. A great deal of effort has been made to describe the conduction and valence bands in the Si/SiGe material system both experimentally and theoretically [32,33,34,35,36,37]. In

this section, the valence band structure will be examined in some detail, since this thesis is primarily focused on hole transport. Basic knowledge of the conduction band will be described in the next sub-section, when the implications on mobility are presented for bulk strained-Si MOSFETs.

As we will find, hole mobility is different in strained Si or strained SiGe compared to hole mobility in unstrained Si because of changes in both the shape (which affects effective masses and density of states) and relative separation between the bands. In this thesis, the band structures of bulk strained and unstrained Si as well as SiGe were examined by 6-band k.p theory (see e.g. [38]). The calculations were made using the *nextnano*^{3} simulator, using the standard material coefficients (references to the simulation tool, as well as sub-references to the standard material parameters are available via Ref. [39]). Epitaxial layers were assumed grown in the <001> direction on a standard (001) substrate. As described in more detail in e.g. [22,40], k.p calculations use material and strain information to calculate the separation between the bands, and then the shape of the bands from the center of the Brioullin zone is expanded from knowledge of the K, L, and M band parameters (see Singh [22]), similar to a Taylor series expansion. In Figure 2.3, the valence bands of bulk Si are shown. At the valence band edge (k=0), the heavy hole (HH) and light hole (LH) bands are degenerate. Due to spin, each of these bands actually consists of two degenerate bands. Since the effective mass is related to the curvature of the band through

$$\frac{1}{m^*} \equiv \frac{1}{\hbar^2}\frac{\partial^2 E(k)}{\partial k^2} \qquad \text{(Equation 2.7)}$$

the HH band has a larger effective mass than the LH band, at least in unstrained Si. To "track" the bands as they move under the application of strain, note that the HH band has a non-parabolic shape, while the LH band is nearly parabolic (as seen from the symmetry in the <100> and <110> directions). With the application of biaxial strain (corresponding to a Si layer grown on a relaxed $Si_{0.7}Ge_{0.3}$ layer), in Figure 2.4, the band degeneracy at k=0 is lifted, so that the LH band is at a lower hole energy than the HH band. The splitting of the two top-most valence bands is roughly 40 meV/10% of Ge in the relaxed SiGe layer on which the Si is grown. Since the biaxial strain is symmetric in the plane of growth, the band structure is also symmetric in the plane (for example, the band structure is identical along <100> and <010>, but is not the same as for the growth direction <001>). In Figure 2.5, the band structure is shown for strained $Si_{0.45}Ge_{0.55}$ (compressively strained as if grown on a $Si_{0.75}Ge_{0.25}$ relaxed layer). Again, the HH and

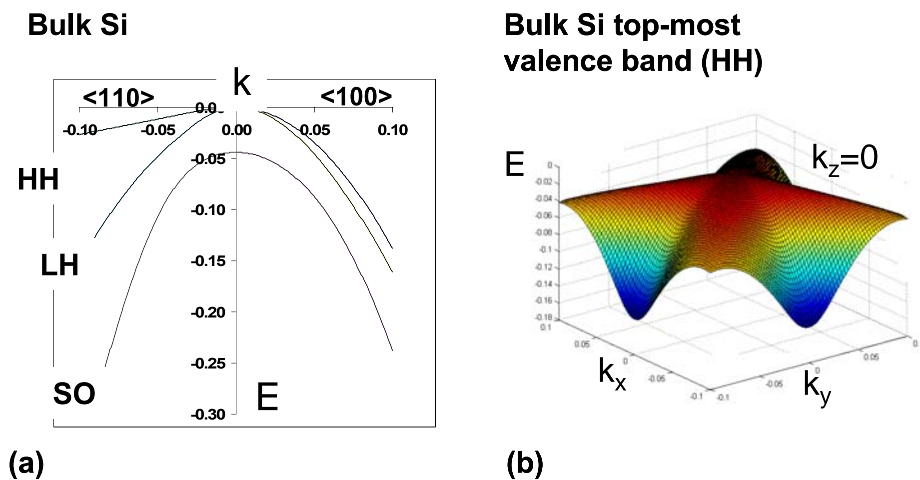

Figure 2.3 Valence bands in bulk Si from k.p calculations performed using the *nextnano*^{3} simulator. In (a), the HH and LH bands are degenerate at the band edge (k=0); the HH band is the lowest hole energy band and has a different curvature (b) in the <100> and <110> directions.

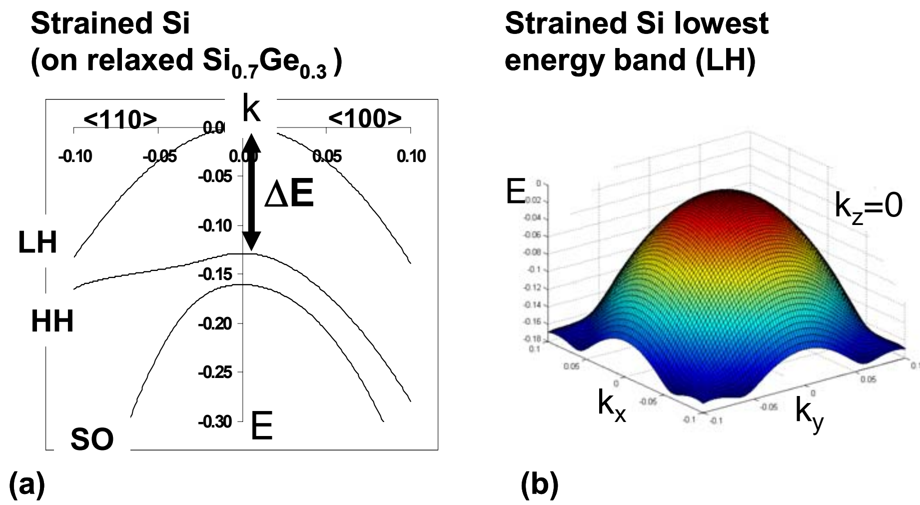

Figure 2.4 Valence bands in tensily strained Si (on relaxed $Si_{0.7}Ge_{0.3}$) from k.p calculations performed using the *nextnano³* simulator. The LH band is the lowest energy band, separated from the HH band by 128 meV (a). In (b), the LH band is nearly parabolic.

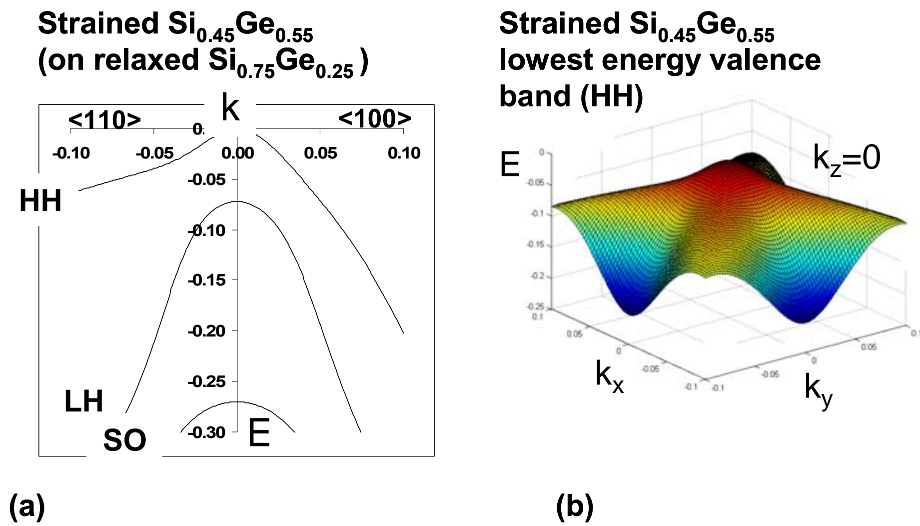

Figure 2.5 Valence bands in compressively strained $Si_{0.45}Ge_{0.55}$ (on relaxed $Si_{0.75}Ge_{0.25}$) from k.p calculations performed using the *nextnano³* simulator. The compressive strain separates the HH band from the LH band (a) so that the HH band has the lowest energy. The HH band is parabolic near the band edge, but is warped at higher hole energies (b).

TABLE 2.2

EFFECTIVE MASSES IN (STRAINED) SI AND SIGE FROM K.P

Ge concentration of relaxed buffer	Ge concentration of layer	HH[a] (<100>,<001>)	LH[a] (<100>,<001>)
0%	0%	0.28,0.28	0.24,0.24
25%	0%	0.27,0.28	0.28,0.20
30%	0%	0.27,0.28	0.28,0.20
25%	55%	0.25,0.23	0.06,0.17

[a]In units of the free electron mass, m_0.
Note 1: In unstrained or compressively strained layers, the lowest energy band for the holes is the HH band, while in tensily strained layers it is the LH band.
Note 2: Masses were extracted 25 meV below the band maxima.

LH bands are no longer degenerate, but after application of compressive strain, the HH band is the lowest energy valence band. Approximate effective masses for select layers are shown in Table 2.2, extracted by fitting the curvature of the calculated energy bands to Equation 2.7 in the <100> and <001> directions. Notice that at the lowest energies (within ~25 meV from the band edge) the strained $Si_{0.45}Ge_{0.55}$ HH band is reasonably parabolic so that the effective mass at that point is significantly improved for all carriers traveling in the <110> direction over unstrained Si, but becomes less parabolic at higher energies.

Mobility in Bulk Strained Si/SiGe MOSFETs

The lowest energy of the unstrained Si conduction band is in the 6 Δ-valleys, as illustrated in Figure 2.6(a). In unstrained bulk Si, these valleys are equivalent, due to symmetry. Biaxial tensile in-plane strain splits the degeneracy of these valleys into 4 equivalent in-plane valleys (Δ_4), and two out-of plane valleys (Δ_2). Note that in inversion layers, there is also splitting of this degeneracy, associated with the breaking of the symmetry by the vertical electric field. This field-induced splitting is superimposed on

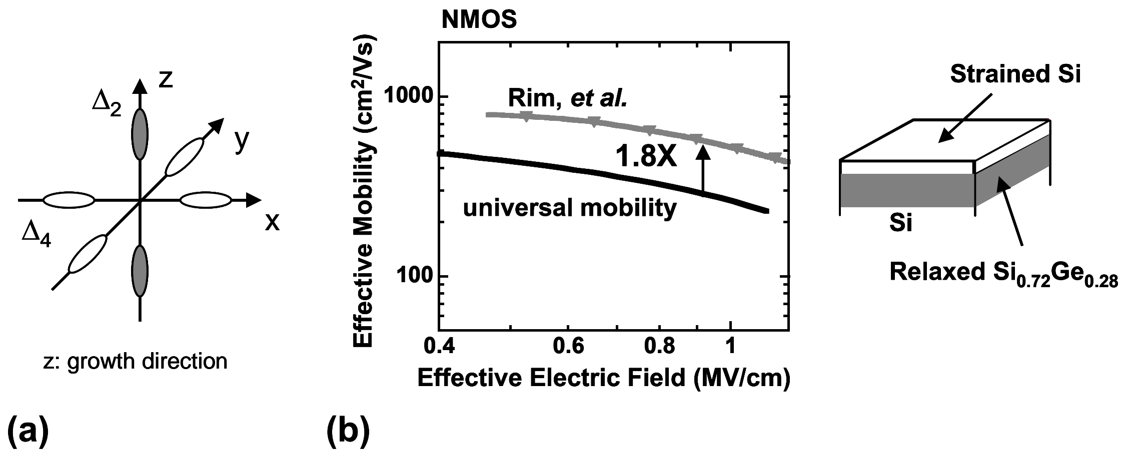

Figure 2.6 The strained Si/relaxed SiGe n-MOSFET. In unstrained bulk Si (a) the six conduction valleys are identical, but biaxial tensile strain breaks the symmetry, lowering the Δ_2-valleys in energy, which enhances mobility (b) by 1.8X over unstrained Si for all vertical effective fields. The example structure from Rim, *et al.* [41] is shown to the right. The universal mobility is from [15].

the strain-induced splitting, for inversion layers in strained Si as discussed in [42]. For each 10% of Ge in the relaxed SiGe buffer layer, the strain-induced splitting is ~67 meV [36,38], shifting the Δ_2-valleys to a lower energy. Due to the valley splitting, a majority of electrons populate the Δ_2-valleys where their effective mass is low in the direction of transport (usually in the <110> direction). From $\mu = q\tau/m^*$, it is expected that electron mobility in tensily strained Si should increase relative to that in unstrained Si as a result of both the lower average effective mass m^* of the inverted carriers, as well as from reduction of the inter-valley scattering rate, τ, which is dominant at room temperature [42]. Experimentally, the electron mobility enhancement is ~1.8X regardless of vertical effective field for strained Si on relaxed $Si_{1-y}Ge_y$ with y>20% [41], as shown in Figure 2.6(b).

As discussed above, tensile strain lifts the degeneracy of the valence bands in strained Si with and energy splitting of ~40 meV per 10% of Ge in the relaxed SiGe buffer layer, which suppresses inter-subband phonon-scattering [40]. In addition to lifting the degeneracy, the shapes of the valence bands are also deformed, causing slight changes in the effective mass in addition to making the LH lower in energy than the HH band. At low vertical fields, the mobility enhancement in tensily strained Si on bulk $Si_{1-y}Ge_y$ is significantly enhanced due to the valence band splitting. As an example, see Figure 2.7, where data from Ref. [41] is shown (y=0.28). The structure is the same as the one in Figure 2.6(b), with a surface strained Si hole channel. However, at high vertical effective fields, where the holes are confined by a steep approximately triangular potential well,

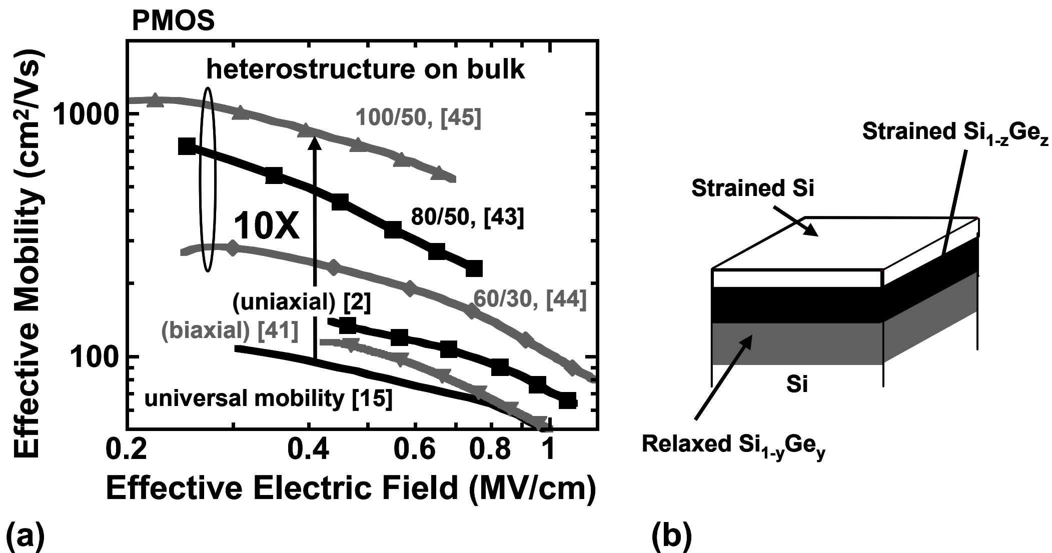

Figure 2.7 Strained Si and strained SiGe p-MOSFET mobilities (a). The universal Si [15], biaxially tensily strained Si [41], and uniaxially compressively strained Si (see section 2.2 below and Ref. [2]) mobilities are much lower than the mobility in biaxially compressively strained $Si_{1-z}Ge_z$ heterostructure-on-bulk [43,44] (the structure shown in (b)) p-MOSFETs. Mobility increases with increasing Ge concentration. The mobility enhancement is 10X in pure Ge on relaxed $Si_{0.5}Ge_{0.5}$ [45]. The shorthand notation 100/50, etc. in (a) refers to z/y, defined in (b).

the mobility enhancement vanishes. In a triangular well, the energy levels depend on effective mass as $E \propto 1/\sqrt{m_z}$, where m_z is the quantization mass. For tensily strained Si, the quantization mass of the LH band (which is the lowest energy band) is lower than for the HH band (see Table 2.2), so that the separation between the ground state energy level (from the LH band) and first excited level (from the HH band) decreases for increased confinement from an electric field, as discussed and illustrated in [46,47]. This effect counter-acts the strain-induced band-separation and associated reduction of phonon scattering. Thus, it appears from experiments, in particular from the vertical field dependence of the hole mobility, that the main contributor to mobility enhancement in biaxially tensily strained Si is the strain-induced splitting of the LH and HH bands.

In biaxially compressively strained SiGe (e.g. the $Si_{0.45}Ge_{0.55}$ on relaxed $Si_{0.75}Ge_{0.25}$ structure in Figure 2.5 and Table 2.2) the valence band degeneracy is also lifted, but with the HH band having the lowest energy. Opposite to the situation in tensily strained Si, the hole mobility in compressively strained SiGe would therefore be expected to have a more favorable mobility at high vertical fields than tensily strained Si, since the band splitting increases at higher fields [46]. Further, the effective mass in SiGe is lower than in Si (especially the LH mass, but also low energy HH mass), which means higher absolute mobilities can be achieved. In Figure 2.7, the hole mobility in heterostructure-on-bulk devices is shown from Refs. [43,44]. The Ge-concentration, z of the hole channel and, y of the relaxed SiGe layer, expressed as a percentage, have been indicated by shorthand notation (z/y) in the figure, as explained in the schematic layer structure for heterostructure-on-bulk in Figure 2.7(b).

For compressively strained Ge on relaxed $Si_{0.5}Ge_{0.5}$, a 10X hole mobility enhancement was achieved by Lee, *et al.* [45] over the universal Si hole mobility, showing the great potential of exploring SiGe or Ge as channel material rather than Si. The possibility of achieving such high mobility enhancements in thin-body devices is the motivation for studying a similar structure, on insulator (heterostructure-on-insulator) in later chapters of this thesis.

2.2 Uniaxial Strain

Though biaxial strain methods were dominant in early strained Si work, much of the recent work has been focused on uniaxial stress techniques (i.e stress along only one symmetry axis rather than two axes). While biaxial strain is typically introduced globally on the entire substrate, uniaxial strain is obtained in the channel region of a regular unstrained Si MOSFET by the application of stressed nitride layers [48,49] alone or in combination with epitaxial growth in the source and drain regions [2]. These process-induced, local stress techniques are made possible by the small size of Si MOSFETs in today's technologies. For electrons, tensile stress is implemented, and for holes compressive stress is used.

The low cost and relatively straightforward integration of local stress techniques made uniaxial strain the first production strain method in the 90 nm node, and is the strain method of choice in production for 65 nm CMOS [50]. The local stress techniques have been particularly beneficial for the hole mobility. In fact, as illustrated in Figure 2.7, Ref. [2], the 90 nm node uniaxial compressive stress shows better performance than biaxial

tensile stress of higher stress level (Ghani, *et al.* [2] estimated the stress level to up to 0.5 GPa in the channel in the uniaxial process, while from Table 2.1, the stress in Rim, *et al.* [41] is ~2 GPa). In the 65 nm node, hole mobility enhancements of nearly 2X have been demonstrated using uniaxial strain [50] with stress levels possibly approaching 1 GPa in the channel [51].

The reason for the high hole mobility in uniaxially strained Si is twofold. First, the band degeneracy in unstrained Si is lifted (for compressive strain the HH band will have the lower energy, which is favorable at high fields). Second, the asymmetry of the strain (applied in the <110> direction) lowers the energy in those parts of the HH band that have lower conduction effective mass, which is illustrated in the simplified iso-energy diagram of the HH in bulk Si and bulk uniaxially compressively strained Si (1 GPa) in Figure 2.8. Further analysis of the hole mobility in uniaxially strained Si inversion layers is available in Ref. [52].

To get an idea of the strain levels in uniaxially strained devices (rather than stress), it should be noted that for a true <110> applied stress (of magnitude S), the stress components in the crystal directions (see Figure 2.2) can be written as [53]

$$s_{xx} = s_{yy} = s_{xy} = S/2 \quad \text{(Equation 2.8)}$$

$$s_{zz} = s_{yz} = s_{zx} = 0 \quad \text{(Equation 2.9).}$$

Combined with Equation 2.4, Equations 2.8 and 2.9 yield the strain. For example, for 1 GPa compressive stress in <110>, ε_{xx} ~ -0.3%, and ε_{xy} ~ -0.6%. Due to the nature of the process induced stress methods, the true stress state is likely not purely uniaxial. Interesting for future work to further increase mobility is to study the combination of new

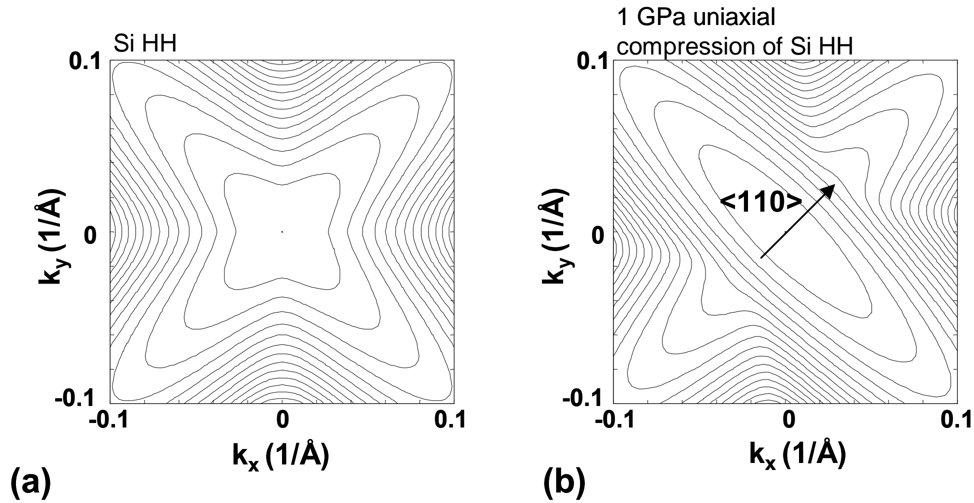

Figure 2.8 The Si bulk HH band with **(a)** no applied stress and **(b)** 1 GPa uniaxial compressive stress in the <110> direction obtained from k.p calculations performed using the *nextnano*^{3} simulator. The iso-energy lines are separated by 10 meV. For a standard MOSFET with <110> channel direction on a (001) substrate, the average conduction mass in the HH band decreases after application of uniaxial stress since holes are energetically favored to invert in the lobe with lower mass in the <110> direction (b). In unstrained Si (a), both lobes are equally favored.

materials, biaxial and process-induced stress. Recently, the application of low levels of mechanical strain superimposed on a biaxially strained Si directly on insulator substrate was studied by Lauer, *et al.* [54].

2.3 Phonon Scattering and Transport in UTB SOI MOSFETs

The mobility in ultra-thin body (UTB) SOI MOSFETs is different from mobility in bulk or thick-SOI. The overall trend is that mobility is degraded as the thickness of the SOI layer is reduced, with several mechanisms involved. Though the physical mechanisms are the same for electrons and holes, the experimental results suggest that differences in the conduction and valence bands make a quantitative difference.

Theoretical Background

Following the description in Lundstrom [55], the scattering rate for a carrier with momentum $\boldsymbol{p_0}$ entering a semiconductor is the sum of the transition rates between the initial and final available states (***p'***).

$$\frac{1}{\tau(\mathbf{p_0})} = \sum_{\mathbf{p'}} S(\mathbf{p}_0, \mathbf{p'}) \qquad \text{(Equation 2.10)}$$

In Equation 2.10, it is assumed that the likelihood that the final state is free is high (if not, one has to involve the probability that the final state is free). Once the scattering rate is determined for the carrier, the mobility limited by this scattering mechanism depends on the scattering rate, effective mass, m^*, and charge, q, as

$$\mu = \frac{q\tau}{m^*} \qquad \text{(Equation 2.11)}$$

so that the longer the time between scattering events, the higher the mobility. It is worth mentioning that the effective mass enters explicitly in Equation 2.11, but the shape of the bands and the density-of-states (DOS) are also implicitly involved in the scattering rate, which is already obvious from the summation in Equation 2.10. The transition rate in Equation 2.10 is given by Fermi's golden rule, and is composed of an overlap-matrix element H and the condition of energy conservation, so that

$$S(\mathbf{p}, \mathbf{p'}) = \frac{2\pi}{\hbar} \left| H_{\mathbf{p},\mathbf{p'}} \right|^2 \delta(E(\mathbf{p'}) - E(\mathbf{p}) - \Delta E) \qquad \text{(Equation 2.12a)}$$

$$H_{\mathbf{p},\mathbf{p'}} = \int_{-\infty}^{+\infty} \psi^*_{\mathbf{p'}} U_s \psi_{\mathbf{p}} d^3 r, \qquad \text{(Equation 2.12b)}$$

where ΔE is the energy difference between the initial and final states and U_s is the scattering potential, which for acoustic *phonon* scattering is $U_s = K_\beta u_\beta$, with $\left|K_\beta\right| = \beta^2 D_A^2$, and u_β is the Fourier component of the lattice vibration, with wave number β, and acoustic deformation potential D_A.

The matrix element (Equation 2.12b) expresses momentum conservation, so that both energy and momentum are conserved in the scattering event. In three dimensions, the acoustic phonon scattering rate is given by

$$\frac{1}{\tau(p)} = \frac{\pi D_A^2 k_B T_L}{\hbar c_l} g_{3D}(E), \qquad \text{(Equation 2.13)}$$

where c_l is the elastic constant for the material, and enters through the dispersion relation for the phonons, and g_{3D} is the density of states. The dependence on effective mass enters in the DOS, which for parabolic bands is $g_{3D} \propto E^{1/2}$, and $g_{3D} \propto \left(m^*\right)^{3/2}$. However, in two dimensions, for example in an UTB-SOI layer or even in a bulk MOSFET inversion layer, the DOS is piecewise constant in the confined layer $g_{2D} = m^* / \pi\hbar^2$ (see Figure 2.9), and the scattering rate for intra- or inter-subband scattering between an initial sub-band i and final subband f is

$$\frac{1}{\tau_{fi}} = \frac{\pi D_A^2 k_B T_L}{\hbar c_l} \frac{1}{W_{fi}} g_{2Df}(E), \qquad \text{(Equation 2.14)}$$

which is different from the three dimensional form primarily through the DOS but also due to the emergence of the effective width of the well (or inversion layer thickness), W_{fi} [56], which is discussed below in reference to Equation 2.17. Equation 2.14 states

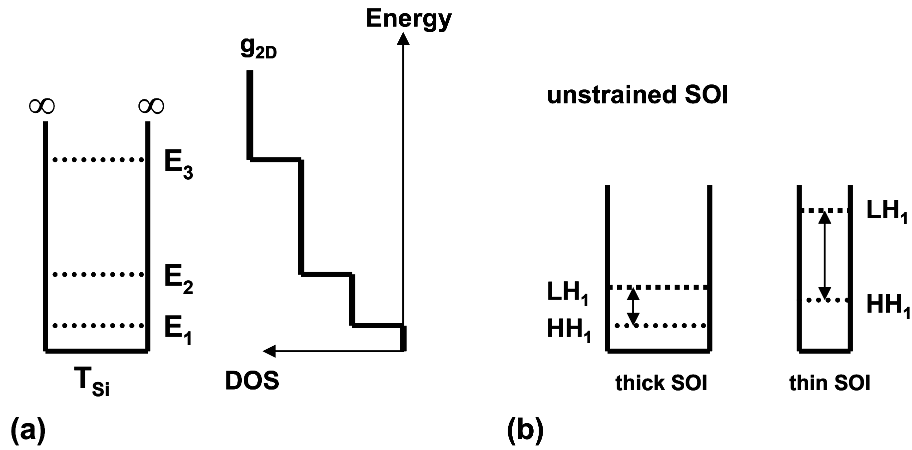

Figure 2.9 The infinite well approximation and the piecewise constant DOS in (a), and (b) the sub-band separations for thick and thin SOI. Since the quantization mass is larger for the HH band than in the LH band, the separation between the first and second sub-bands in the valence band of unstrained Si increases as the SOI thickness is reduced [46].

that the scattering rate goes up as the confinement increases. This means that as the effective inversion layer thickness decreases (all other things equal), the mobility is degraded. The effective width originates from the matrix element, which in three dimensions expresses momentum conservation. In the confined structure, momentum is no longer well-defined in the quantization direction, as expressed by Heisenberg's uncertainty principle

$$\Delta p \Delta x \geq \frac{\hbar}{2}, \qquad \text{(Equation 2.15)}$$

so that if a particle such as an electron or hole is confined in position (x), it will become fuzzy in momentum (p). Physically, as the electron or hole is confined in real space, and spreads in momentum-space, it allows interaction with more phonons, which leads to more frequent scattering events. This is the reason a layer thickness enters in Equation

2.14. Mathematically, the fuzziness enters in the matrix element, from which the integral in the quantization direction, z is lifted out from the in-plane integral

$$H_{\mathbf{p},\mathbf{p}'} = \int_{-\infty}^{+\infty} \psi^*_{//p'} U_{s//} \psi_{//p} d^2 r \int_{-\infty}^{+\infty} \psi^*_{f'}(z) \psi_i(z) e^{\pm i\beta_z z} dz \qquad \text{(Equation 2.16)}$$

$$\frac{1}{W_{fi}} = \left| \int_{-\infty}^{+\infty} \psi^*_{f'}(z) \psi_i(z) e^{\pm i\beta_z z} dz \right|^2 = \left| \int_{-\infty}^{+\infty} \psi^*_{f'}(z) \psi_i(z) dz \right|^2 \qquad \text{(Equation 2.17)}$$

so that W_{fi} is a measure of the fuzziness in the quantization direction (z). From the reduction of the inversion layer thickness, phonon scattering increases.

Just as with confinement from a high field (see section 2.1), the confinement in the oxide/Si/oxide quantum well affects the energy levels of the sub-bands, causing sub-bands to separate in energy which can cause a reduction in inter-subband or inter-valley phonon scattering. Using the infinite well approximation, the nth sub-band energy level (see Figure 2.9) in a band with quantization mass m_z is

$$E_n = \frac{\hbar^2 \pi^2}{2 m_z T_{Si}^2} n^2 , \qquad \text{(Equation 2.18)}$$

where T_{Si} is the thickness of the SOI layer. For electrons, the carriers in the Δ_2-valleys have a larger quantization mass (the z-direction in Figure 2.6(a)) than the carriers in the Δ_4-valleys, $m_l > m_t$. Therefore, in-plane and out-of plane energy ladders separate as the thickness of the SOI layer is reduced. Since larger energy is required to scatter carriers from one valley to the other, this reduces the phonon inter-valley scattering for the electrons [42,56] in a similar fashion as the application of biaxial tensile strain, discussed above. For holes in unstrained Si, a similar separation of the HH and LH bands occurs

when reducing the SOI thickness, which in the case of holes would reduce the inter-subband scattering (i.e. scattering between the lowest HH state and the next, LH state, [46]).

Observed Mobility in UTB SOI MOSFETs

So far, two different effects of layer thickness on phonon scattering have been presented, and they are essentially the same for electrons and holes. The first mechanism lowers mobility due to spreading of the wave function in momentum space (and coupling with more phonons) as the layer thickness is reduced. This mechanism is expected to lead to a monotonic reduction in mobility as the layer thickness is reduced. The second mechanism is a reduction in inter-subband or inter-valley scattering as the thickness is reduced. However, as in biaxially strained Si [57] the impact on mobility from this second mechanism saturates once the band separation is large enough. Phonon limited mobility changes are important for transport in layers of 3-10 nm thickness. Depending on the details of the band structure, phonon limited mobility may have a local maximum [46,56,58], as illustrated qualitatively in Figure 2.10. Experimentally, the mobility follows this trend for electrons as demonstrated by Uchida, *et al.* [59,60], while for holes, the mobility decreases monotonically [60,61]. Experimental results for unstrained UTB-SOI hole mobility are shown along with the results for strained SOI in Chapter 4. The experimental hole mobility does not have a local maximum because its phonon limited mobility peak occurs at such thin layers that another scattering mechanism, thickness fluctuation limited mobility [62], dominates [46].

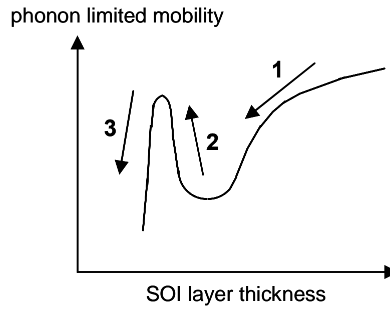

Figure 2.10 Qualitative sketch of how the phonon scattering mechanisms would affect electrons and holes. For detailed simulations, see e.g. Takagi, *et al.* [56] for electrons, and Fischetti, *et al.* [46] for holes. Real space confinement causes wave function spread in momentum, allowing interaction with more phonons, which leads to a decrease in phonon limited mobility (1). As the sub-bands or valleys separate in energy, this leads to a reduction in phonon scattering between these bands or valleys, causing an increase in phonon limited mobility in a certain thickness range (2). However, for even thinner layers, the confinement induced degradation dominates again (3).

A simplified theoretical background on the thickness fluctuation limited mobility will be given in Chapter 4, since it is best illustrated by experimental results. For now, it is enough to know that this mechanism has a very strong thickness dependence, $\mu_r \propto T_{Si}^6$, and becomes dominant for SOI thicknesses below 3-4 nm for both electrons and holes.

2.4 Effective Mobility Extraction

In this section, the experimental mobility extraction technique used in this work is presented. Due to the ultra-thin thickness (<10 nm) of strained Si layers, special efforts were made to reduce or eliminate the impact of parasitic series resistance on the extracted mobility. Field effect mobility and effective mobility are two common measures of transport in MOSFETs, and are given by

$$\mu_{FE} = \frac{L}{WC_{ox}V_D} \cdot \frac{dI_D}{dV_G} \quad \text{(Equation 2.19)}$$

$$\mu_{eff} = \frac{L}{W} \cdot \frac{1}{Q_{inv}} \frac{dI_D}{dV_D} \approx \frac{L}{W} \cdot \frac{1}{Q_{inv}} \frac{I_D}{V_D}, \quad \text{(Equation 2.20)}$$

where I_D, V_D (small), and V_G are the measured drain current, intrinsic drain-to-source voltage, and gate-to-source voltage. Q_{inv} is the inversion charge density determined from split capacitance-voltage (C-V) measurements. For simplicity, sign conventions are following those for n-MOSFETs, and all currents and voltages are relative to the source. The impact of series resistance on field effect mobility (Equation 2.19) is described in Appendix A. The effective mobility (Equation 2.20) better captures the mobility dependence on gate bias (see Appendix A) than the field effect mobility, which has made it the more popular choice for transport studies. One source of error in the effective mobility comes from the value of V_D. In absence of parasitic series resistance, V_D is simply the applied drain bias, but is reduced to $V_D = V_{Dtot} - R_{sr} I_D$ for a device with a constant series resistance. V_D is the intrinsic drain bias and V_{Dtot} is the total, applied bias. R_{sr} is the sum of resistance in the contacts and the source and drain regions and increases rapidly as the thickness of the Si layer (T_{Si}) is reduced, particularly below 6 nm (Figure 2.11). To extract the intrinsic V_D, a special mobility extraction MOSFET was used (Fig. 2.12) [63]. The intrinsic V_D is given by $V_D = (V_1 - V_2) \cdot L / \Delta$ (long channel device). The accuracy of this extraction is limited by the accuracy with which V_1 and V_2 can be determined. For each device, multiple measurements were made and the reproducibility of the extraction was confirmed. When comparing devices with different R_{sr}, an

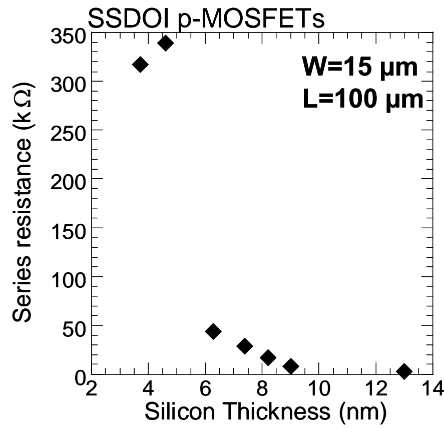

Figure 2.11 Example of parasitic resistances extracted on p-MOSFETs with ultra-thin Si thickness (without recessed gates or raised source/drains).

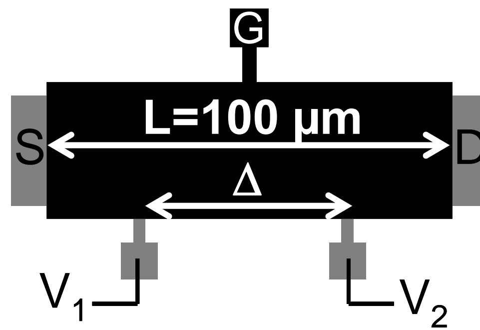

Figure 2.12 The mobility extraction MOSFET used in this work [63]. Current is flowing through the source and drain contacts, but the channel potential drop between source and drain is extracted from the additional "channel taps", allowing for extraction of intrinsic drain bias.

appropriate drain bias should be applied to yield similar $V_D(V_G)$ relationship for the devices (at least at the point of interest for the comparison). Notice that the approximation in Equation 2.20 is necessary to avoid numerical differentiation of I_D with respect to a noisy variable. The gate bias V_G is independent of series resistance, and

assuming a correct V_D has been extracted, I_D will represent the current at the applied gate bias. Typical intrinsic V_D values for mobility extraction were in the 20-40 mV range.

In order to accurately extract mobility, a correct measurement of the gate to channel capacitance-voltage *C-V* curve must be obtained. In the equations for mobility, the *C-V* data enters as the maximum point of the *C-V* curve as C_{ox}, and in the inversion layer charge, calculated from [17]

$$Q_{inv}(V_g) = \int_{-\infty}^{V_G} C_{gc} dV_G \ . \qquad \text{(Equation 2.21)}$$

Due to the frequency dependence of the complex impedance $Z = R + 1/j\omega C$, the *C-V* measurement must be carried out at sufficiently low frequency. Measurements were typically done at 10 kHz. This frequency was chosen so that no reduction of the maximum point of the *C-V* curve occurred when changing the frequency from 5 kHz to 20 kHz. However, if the frequency is too low, interface density traps D_{it} may respond to the small signal, causing the integrated charge to change slightly at low gate bias, when comparing measurements at 5 kHz and 20 kHz. For the main region of interest (V_G considerably above V_T) the error in mobility due to inaccuracy in the integrated charge is small. For the mobility results on ultra-thin strained Si directly on-insulator (SSDOI) in Chapter 4, the effect of a change of ± 5% in C_{ox} and a ± 50 mV shift of the *C-V* curve, respectively were below ± 5% of the measured mobility. The error from a ± 10 mV shift in the intrinsic V_D was found to be less than 2%. In Chapter 4, the robustness of the mobility extraction technique is exemplified on SSDOI MOSFETs.

2.5 Chapter Summary

The chapter started with a review of biaxial strain technology. First, a general introduction to strain and biaxial strain was given, providing tools to interpret strain levels, SiGe and buffer layer epitaxial methods, and previous experimental knowledge in the field. Biaxially strained materials are the foundation of all the structures studied in this thesis. Next, a brief introduction to uniaxial strain was given, following a similar approach. While the thesis is mainly concerned with biaxial strain, uniaxial strain is the mainstream production method of choice for 90 nm and 65 nm CMOS technologies, and may continue to provide mobility improvements, perhaps combined with heterostructure channel technologies in future nodes. Next to strain and novel materials, the additional booster studied in this work is the use of ultra-thin body SOI technology, which may serve to improve electrostatic control either in single or multiple-gate implementations. The phonon scattering mechanisms relevant to such thin-body SOI technology were reviewed. The additional scattering mechanism, called thickness fluctuation limited mobility was introduced, but will be further explained in Chapter 4. Finally, methods to extract mobility in the experiments of this work were presented.

Chapter 3

Substrate Fabrication and Characterization

In this work, MOSFETs were fabricated on two types of 150 mm substrates not yet commercially available: strained Silicon Directly on Insulator (SSDOI), and strained Si/strained SiGe/strained Si Heterostructure on Insulator (HOI). In this chapter, the fabrication procedures of SSDOI and HOI substrates are described, and the starting material and substrate characterization is discussed. A detailed process flow for a typical substrate fabrication lot has been attached as Appendix B.

The SSDOI and HOI substrates are illustrated in Figure 3.1. The SSDOI is similar to an unstrained silicon-on-insulator (SOI) wafer, but the active device layer is biaxially tensily strained Si. HOI is a more complex substrate with three device layers on top of the buried oxide (BOX). The top layer (also referred to as the Si cap), is biaxially tensily strained Si, the next layer is biaxially compressively strained $Si_{1-z}Ge_z$ layer (the "buried channel"), and the third layer is again biaxially tensily strained Si. Thus, the body thickness in SSDOI is just the thickness of the strained Si layer, whereas the body thickness in HOI is the sum of three layer thicknesses. The indices y and z are used to indicate the Ge concentration and/or strain state of the SSDOI and HOI structures, as will be discussed below.

The fabrication of SSDOI and HOI is accomplished by epitaxial growth of relaxed $Si_{1-x}Ge_x$ buffer layers and etch stop layers, oxide deposition and wafer bonding, followed by mechanical grind-back and etch-back by wet chemical etching [64,65].

3.1 The Epitaxial Growth Process

An abbreviated process flow for the fabrication of SSDOI and HOI substrates is illustrated schematically in Figure 3.2. Linearly graded $Si_{1-x}Ge_x$ buffer layers with 10% Ge per micrometer of growth were grown, and relaxed $Si_{1-y}Ge_y$ layers (here, y is the final Ge content of the graded buffer) were grown at 900ºC in an Applied Materials Epi Centura reactor on 150 mm Si substrates. In order to improve the quality of the epitaxial growth, the wafers were dipped in a dilute hydrofluoric acid (HF) bath after the pre-epi RCA clean. An initial Si epi layer was grown at 1080ºC prior to growth of the relaxed $Si_{1-x}Ge_x$ buffer layers. For the SSDOI substrates used in this work, the Ge content of the relaxed layers in the donor wafers was y=0.25, 0.3, and 0.4. To indicate the strain level, the corresponding final SSDOI substrates are referred to as 25%, 30% or 40% SSDOI, though they are Ge-free (thus, the index y in Figure 3.1). The HOI relaxed SiGe layers had y=0.25 and 0.3. The thermal budget during epitaxial growth is indicated in Figure 3.2(a).

After the growth of relaxed $Si_{1-y}Ge_y$ layers and strained Si etch stop layers, a compressively strained $Si_{1-z}Ge_z$ device layer (as grown z=0.55) and a final strained Si layer completed the as grown HOI structure, shown in Figure 3.2(a). The SSDOI as grown structure is identical, except the omission of the last two layers from the growth

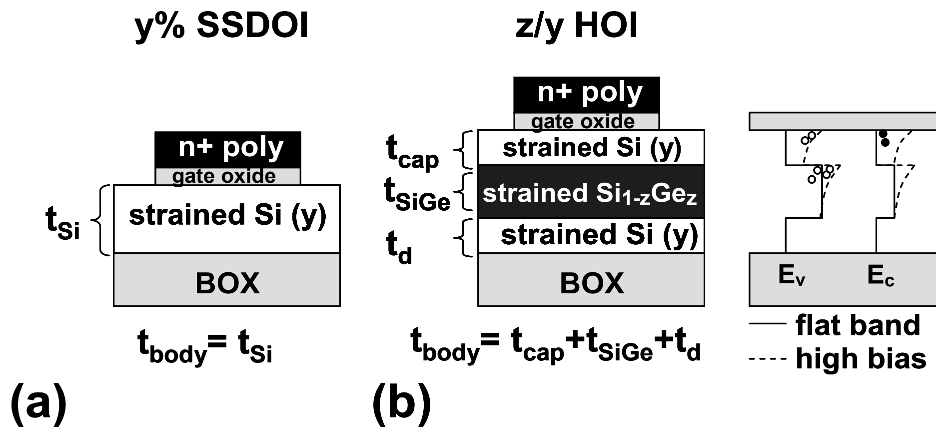

Figure 3.1 The **(a)** SSDOI and **(b)** HOI structures. The SSDOI is simply a biaxially tensily strained Si layer (strained to an equivalent in-plane lattice parameter as in relaxed $Si_{1-y}Ge_y$) on a buried oxide. The HOI is composed of three layers. Two strained Si layers surround a high Ge content biaxially compressively strained $Si_{1-z}Ge_z$ layer, so that z>y. The band structure in (b) indicates the inversion preferences in the different layers for the conduction and valence bands of HOI, and will be covered in detail in Chapter 5.

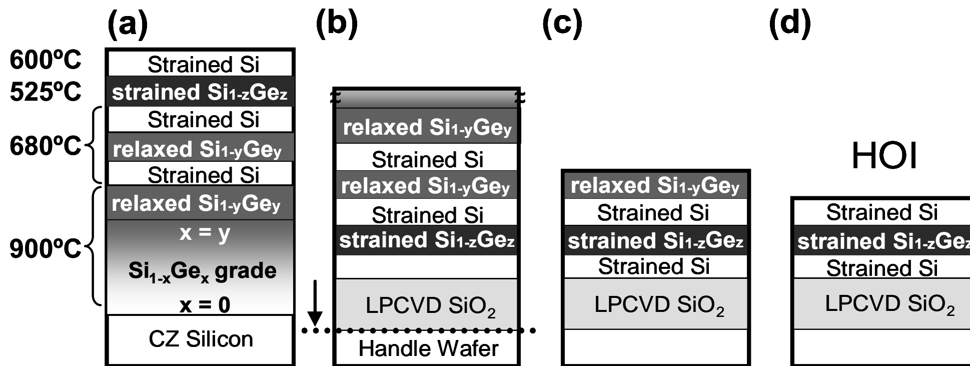

Figure 3.2 The HOI fabrication process: (a) as grown structure, (b) deposition of oxide, flip, bond (arrow marks bond interface), grind back and TMAH etch, (c) removal of remaining etch stop layers by selective wet etching, and (d) final HOI structure. SSDOI fabrication is by the same process, except the exclusion of the topmost two layers in the as grown structure in (a).

sequence. While the Si etch stop layers were typically grown 10-15 nm thick, the thickness of the device layers was varied depending on the target thickness of each device lot, which will be described in later chapters.

In addition to these design-driven device layer thickness considerations, other factors contributed to the choice of thickness of the as grown device layer. The lower limit for device layer thickness was set by limitations in the growth process (particularly for the $Si_{1-z}Ge_z$ device layer in HOI), as well as by diffusion of Ge during later thermal steps (true for both HOI and SSDOI). The upper limit was set by critical thickness considerations. Strained layers were grown either in the stable or meta-stable regime [25]. Ge concentrations were calibrated by secondary ion mass spectroscopy (SIMS) and Rutherford back-scattering techniques (RBS). Epitaxial layer thicknesses were estimated by SIMS.

The purpose of the relaxed SiGe buffer layers is to induce a lattice mismatch between the virtual substrate and the device layers grown pseudomorphically on top of the virtual substrate while controlling the levels of threading defects that reach the surface, as discussed in the review by Mooney [66]. In this work, threading defects were monitored by defect etching of the relaxed $Si_{1-y}Ge_y$ layer in a solution of 4 g of CrO_3 in 200 ml HF and 250 ml de-ionized water (modified Schimmel etch [67]). Figure 3.3 shows a Nomarski micrograph of the surface of a relaxed $Si_{0.6}Ge_{0.4}$ layer grown at the typical conditions yielding etch pitch density of approximately $5x10^5$ cm^{-2}. Typical levels of threading defects in the relaxed SiGe used in this work were in the range of $10^5 – 10^6$ cm^{-2}. The defect and roughness analysis indicated that a high relaxed buffer growth

temperature can suppress the defect level; however the cross-hatched pattern on the epitaxial structure is more significant for higher growth temperatures. The growth temperature of the relaxed buffer layers (900ºC), and the linear ramp rate (10% Ge/µm of buffer) were chosen to keep defect levels below 10^6 cm^{-2} while limiting the cross-hatch peak-to-valley to 20 nm or less, for buffer layers with up to 40% Ge. It should be noted that while the roughness of the cross-hatch is relatively long range, and thus does not affect transport [35], it makes wafer bonding more difficult, since wafer bonding requires planar surfaces.

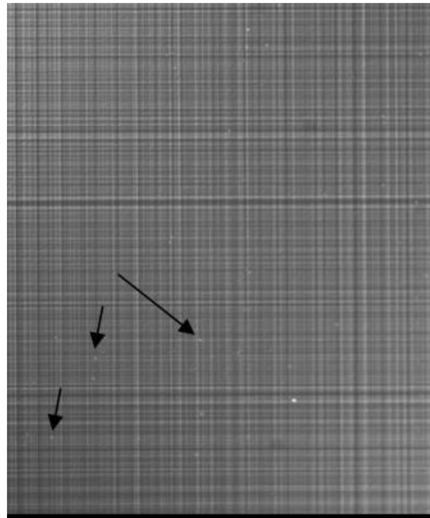

Figure 3.3 Nomarski micrograph (the view is 170 µm x 205 µm) of an as grown $Si_{0.6}Ge_{0.4}$ buffer layer after defect etching. Etch pits mark the end of threading arms from misfit dislocations (see e.g. Mooney [66] for more detail). In the micrograph, the etch pits are seen as faint bright dots (arrows mark a few of many). Etch pits were counted by sweeping over large areas of the wafer surface, counting pits manually. Here, the count is 5 x 10^5 cm^{-2}, a typical value.

TABLE 3.1
THERMAL PROCESSES[a]

STEP	SSDOI and SOI	46/25 HOI	55/25 HOI
BOX Densify	750-800ºC (1.5 h)	750ºC (1.5 h)	600ºC (2.5 h)
Bond Anneal	750-800ºC (1 h)	750ºC (1 h)	<550ºC (0.5 h)
Gate Oxide[b]	800ºC (1.5 h)	650ºC (3 h)	600ºC (5 h)
Dopant Activation	1000ºC (10 s)	850ºC (10 s)	800ºC (10 s)

[a]Only main thermal budget events have been included.
[b]Time includes anneal time in addition to oxidation time.

3.2 Bond and etch-back

After epitaxial growth, a low pressure chemical vapor deposition (LPCVD) oxide was deposited at 400ºC and densified. The post-epitaxial thermal treatments during the substrate fabrication process (as well as during device processing, for comparison) have been summarized in Table 3.1. After chemical mechanical polishing (CMP) to remove the cross hatched surface pattern which is transferred to the oxide by the conformal deposition, the substrates were bonded to Si handle wafers. To achieve high bond strengths in the lowest thermal budget process (labeled "55/25 HOI" in Table 3.1), the wafers in that lot were bonded to wafers with 100 nm-thick thermal oxide, following plasma-activation and pre-cleaning treatment, as described in [68]. In the higher thermal budget processes (SSDOI and 46/25 HOI), the LPCVD oxide wafer was bonded to a bare Si handle wafer, without plasma activation. Note that in either case, the wafer bond interface (marked by an arrow in Figure 3.2) is away from the device layers, underneath some oxide or even the entire buried oxide (BOX). The BOX thickness was 300-500 nm for the bonded wafers.

After the post-bond anneal in a nitrogen ambient, the original epitaxial wafer was mechanically ground back [69], and then planarized by CMP. To avoid damage to the epitaxial layers during grind-back, roughly 100 μm of the original epi-wafer was spared, including a thick Si layer and all the graded buffer layers. These layers were removed selectively in a sequence of wet etches, as in Ref. [70]. The remaining Si substrate and most of the graded buffer was etched back in tetra-methyl ammonium hydroxide (TMAH), heated to 80ºC. TMAH is selective to $Si_{1-x}Ge_x$, especially with $x>0.2$ [70]. The substrate after these steps is shown in Figure 3.2(b). The substrate was subjected to CMP again and the remaining SiGe relaxed layer was etched by a 3:2:1 solution of acetic acid: hydrogen peroxide: hydrofluoric acid, which has good selectivity to Si once it has stabilized for a couple of hours [71]. The remaining Si etch stop layer was dipped off in TMAH, leaving the structure shown in Figure 3.2(c).

The final etch was a 5:1:1 solution of ammonium hydroxide, hydrogen peroxide, and de-ionized water, heated to 80ºC (commonly referred to as SC-1). The etch rate of SiGe in SC-1 is slower than in the acetic acid based etch used for the previous SiGe layers, but is still strongly dependent on the Ge concentration of the layer (Figure 3.4), yielding a selectivity of 32:1 for removal of $Si_{0.6}Ge_{0.4}$ over the strained Si device layer, while the selectivity for removing $Si_{0.75}Ge_{0.25}$ over strained Si is only 7:1. In order to remove residual Ge atoms, an over-etch of 5-10 nm was carried out in the SC-1, leaving a Ge free SSDOI substrate, or in the case of HOI, two strained Si layers with a high Ge content layer in between (Figure 3.1).

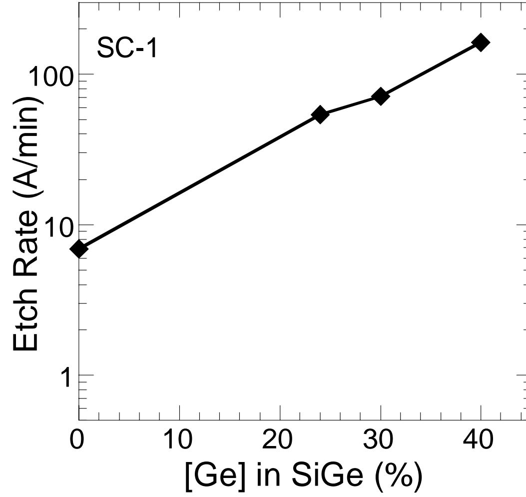

Figure 3.4 The etch rate of $Si_{1-y}Ge_y$ in SC-1 at 80ºC as a function of Ge content y of the layer. Fabrication of SSDOI or HOI with low concentration of Ge in the relaxed buffer is complicated by low selectivity of both the SC-1 etch and the TMAH etch (not shown).

The thermal treatments during substrate preparation and device processing are summarized in Table 3.1. The lowest thermal budget HOI process was implemented in order to successfully fabricate 4, 6, and 10 nm ultra-thin $Si_{1-z}Ge_z$ layers with retained layer thickness and Ge concentration (z=0.55) even after device processing (see Chapter 6). Early studies on thermal treatments and strain relaxation in SSDOI showed that the SSDOI substrate can withstand extended processing at or above 900-1000ºC, which was confirmed on material fabricated by the above process [72,73,74]. Since the SSDOI substrate is Ge-free, SSDOI does not suffer from the strong temperature dependence of Ge diffusion [75]. In HOI, the existence of a compressively strained $Si_{1-z}Ge_z$ layer with high Ge content makes the structure less suitable for high-temperature processes, as will be discussed further in Chapter 5. In fact, recent work has shown that Ge diffusion in

compressively strained SiGe layers is more enhanced than Ge diffusion in un-strained or relaxed SiGe layers [76].

In addition to strain, another important aspect of the device substrates is the level of short-range roughness, which could contribute to mobility degradation. Due to the absence of planarization of the $Si_{1-y}Ge_y$ buffer layers in the above fabrication sequence, the final SSDOI or HOI substrates will have cross-hatched device layers, as seen in the atomic force micrograph of a 40% SSDOI substrate in Figure 3.5. The cross-hatched surface has not been found to affect transport due to its long range character [35]. Analysis of short-range roughness of 40% SSDOI by AFM (on scan areas of 50 nm x 50 nm) reveals roughness of < 0.2 nm, similar to Si CZ wafers. Thus, the short-range surface roughness is expected to be similar in the SSDOI, HOI, and commercial SOI wafers.

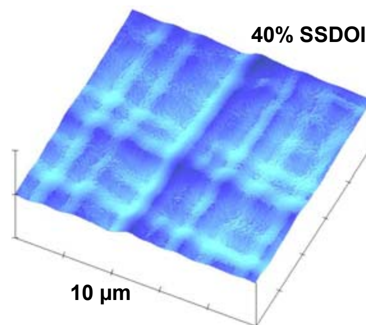

Figure 3.5 Atomic force micrograph of a 40% SSDOI substrate. The long range cross-hatch (typically with a peak-to-valley depth of < 20 nm and a period measured in µm) is a characteristic of graded SiGe layers, but does not affect mobility. Small-area scans (50 x 50 nm) indicate roughness on the order of < 0.2 nm, similar to the as-grown epitaxial structure or Si bulk wafers, illustrating that the SC-1 etch in Figure 3.4 does not cause measurable surface roughness.

3.3 Chapter Summary

The fabrication of SSDOI and HOI substrates by epitaxial growth followed by bond and etch-back has been described. This process is not intended as a high-volume approach, but is suited for small, fast-turnaround research lots. An advantage compared to other more sophisticated processes is the relative in-sensitivity to the exact structure (e.g. layer thicknesses), which enables a large number of substrate level splits to be achieved using the same process conditions, even in the same lot. The strain was incorporated in the substrates by growth of relaxed SiGe buffer layers and growth of strained Si or strained SiGe layers lattice matched to the buffer layers. An oxide was deposited on the epitaxial wafer, to serve as the BOX layer. Thus, the bonding interface of the fabricated SSDOI and HOI substrates is away from the device layers, i.e. below the BOX. Through mechanical grinding and selective wet etching, all but the device layers were removed, leaving a Ge-free SSDOI substrate or a substrate with one strained SiGe layer surrounded by two strained Si layers (HOI). The strain in the fabricated substrates is held in place by the BOX, and strain measurements on SSDOI substrates indicate little or no tendencies to strain relaxation, even after generous thermal treatments in excess of 1000ºC. Short-range roughness on the fabricated substrates was similar to Si CZ control wafers.

Chapter 4

Strained Silicon Directly on Insulator MOSFETs

To further the scaling of CMOS devices to extremely short channel lengths where improved electrostatic control of the channel is required, a number of structures have been proposed. Among these, multiple gate MOSFETs such as double gate (planar or FinFET) and triple gate (tri-gate) structures have been proposed, as well as fully-depleted silicon-on-insulator (FD-SOI) with ultra-thin bodies (UTB) [4,5,6]. Any proposed structure will need to be compatible with transport enhancing techniques, such as strain and novel materials to compete with current drives in traditional planar bulk-devices, where strain enhancement techniques were introduced already in the 90-nm node [2,3]. One of the first and most promising structures that enables the incorporation of strain in extreme UTB-SOI technology is the recently proposed strained Si directly on insulator (SSDOI) [72,73,74].

In this chapter, the fabrication of n- and p-MOSFETs on the SSDOI substrates is described. A detailed process flow listing the fabrication of SSDOI MOSFETs is attached as Appendix C. Following the discussion on device fabrication below, device characteristics are presented, followed by a discussion of electron and hole mobility in SSDOI MOSFETs of different strain levels. In the initial sections of this chapter, the FD-

SSDOI MOSFETs have Si thickness of 8-25 nm [77], thick enough that only very small thickness dependent effects on transport properties are expected. In a later section, the UTB-SSDOI p-MOSFET is described, with mobility results presented for structures with strained Si layer thickness down to 1.4 nm [78].

4.1 The MOSFET device fabrication process

In this section, the fabrication of moderately (8-25 nm) thin-channel SSDOI MOSFETs is described. N- and p-MOSFETs were fabricated on separate wafers. For n-MOSFETs, 25% and 30% SSDOI substrates were used, for p-MOSFETs, 30% and 40% SSDOI substrates were used. The as grown thicknesses of the strained Si layers on 30% SSDOI wafers were in the range 20-40 nm, while 40% substrates had as grown strained Si layer thickness in the range 15-26 nm. Unstrained 150 mm SOI wafers from SOITEC [79] were used as device controls, following the same process flow as the SSDOI wafers. The general process flow is also relevant for the fabrication of UTB-SSDOI MOSFETs and heterostructure-on-insulator (HOI) MOSFETs of later chapters; however the details of certain process modules will be described separately in respective chapter. The details below relate to the device lots for moderately thin-channel SSDOI MOSFETs.

The general process flow is illustrated by modules in Figure 4.1. First, the wafers went through a substrate preparation module. For the SSDOI substrates, fabrication of substrates was described in Chapter 3, and no further substrate preparation was required before device fabrication. On the other hand, the unstrained SOI control wafers were

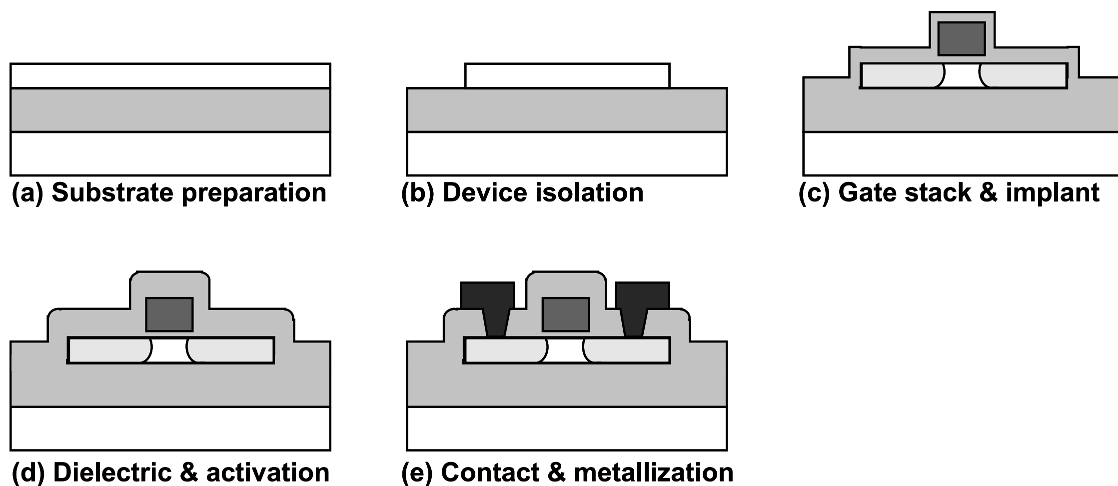

Figure 4.1 The general process flow for fabrication of MOSFETs on SSDOI or HOI substrates. **(a)** The substrates are fabricated and prepared to the desired thickness and structural specifications. **(b)** Device isolation by dry etched mesas. **(c)** Gate oxidation, poly-Si deposition and source/drain implants of P (n-MOSFETs) or BF_2 (p-MOSFETs). **(d)** Deposition of interlayer dielectric and rapid thermal annealing. **(e)** Contact patterning and metallization, and forming gas sintering conclude the process.

obtained from the manufacturer with a 100 nm Si film on top of the 200 nm buried oxide (BOX). To yield a similar thickness of the final device layer as of the SSDOI wafers, these substrates were thinned by a series of thermal oxidations, until typically 15-30 nm of Si remained, as in [80]. It should be noted that the method of thinning was different between the unstrained SOI wafers (thermal oxidation) and strained wafers (over-etch in SC-1). Careful analysis of the roughness of the strained substrates (see Chapter 3) indicated that the roughness of the wet etched wafers was similar to the roughness of un-treated Si CZ wafers. The evolution of the strained Si thickness in the process sequence is described in Table 4.1. In Table 4.1, the as grown thickness is the target thickness from the calibrated growth time, the SSDOI strained Si thickness was measured by ellipsometry, and the final thickness of the strained Si in the fabricated

TABLE 4.1
THICKNESS EVOLUTION OF SSDOI STRAINED SI LAYER

Ge fraction	Epi As Grown[a] (nm)	Etched Back[b] (nm)	After Device Process[c] (nm)
25%	27	22	-
30%	20	13	8
30%	25	17	13
30%	30	18	-
30%	40	30	25
40%	26	18	14

[a]As grown thickness was estimated from growth time and growth rate tables (calibrated with SIMS).
[b]The etched back SSDOI layer thickness was measured by ellipsometry.
[c]Post device process thicknesses by SIMS or ellipsometry.

device was estimated by cross-section transmission electron micrographs (XTEMs). The p-MOSFETs (on both SOI and SSDOI) received a light phosphorus implant to a simulated target level of $5x10^{16}$ cm^{-3} prior to the main device process.

The main process flow starts by the isolation module (Figure 4.1(b)). All devices were isolated by dry etching of a mesa. The lateral dimension of the mesa was always above 10 µm, so that geometry effects on strain are expected to be negligible [81,82]. Parasitic side-wall transistors are sometimes observed in mesa-isolated devices, but due to the limited mesa height in this experiment, little or no effect of parasitic edge devices was observed [83]. Since the wafer bond interface is below the buried oxide (BOX), not between the BOX and device layer, the adhesion of the mesa to the BOX was good even after patterning.

After device isolation, 4 nm of gate oxide was grown by dry oxidation at 800ºC, and a phosphorus in-situ doped poly-Si gate (for n-MOSFETs) or un-doped poly-Si gate (for the p-MOSFETs) was deposited. The gate etch was in an anisotropic Cl_2/Br or Cl_2 plasma. In order to avoid etching through the gate oxide (which would create device open circuits), an over-etch step with high selectivity to silicon dioxide was used for

removal of the final estimated 10-20% of the gate thickness and to avoid polysilicon stringers along the mesa edges. A 15-20 nm-thick low pressure chemical vapor deposition (LPCVD) oxide was then deposited to act as an implant screen and protection of the source and drain regions.

The ion implants for gate and source/drain regions (phosphorus or BF_2) were performed at Innovion [84], and conditions are indicated in the Appendix C. Relatively high energy implants and high doses were used to allow the same implant to be used for a variety of device layer thicknesses, thus wasting some of the implant dose for the purpose of process flexibility.

After deposition of an LPCVD inter-layer dielectric (100-150 nm), gate and source/drain dopants were activated in a rapid-thermal anneal system at 650ºC for 2 minutes followed by 1000ºC for 10s, the highest temperature step in the process. Despite the high thermal budget during both substrate and device processing, strain analysis has indicated that strain levels are maintained at the as-grown levels in similarly prepared substrates [74]. One advantage of the SSDOI structure compared to strained-Si on relaxed SiGe-on-insulator [70] is that Ge-diffusion issues are eliminated in the Ge-free SSDOI. The thermal processing steps (including estimated ramp times) are indicated in Table 4.2.

The final process module is the patterning of 2 x 2 μm^2 contact openings in a diluted buffered hydrofluoric acid, followed by metallization by sputtering. While initial device wafers had only 50 nm-thick titanium and 0.5 µm aluminum, it was later realized that the

TABLE 4.2
THERMAL PROCESSING OF SSDOI AFTER EPITAXIAL GROWTH

Step	25% or 30% substrates	40% substrates	Time (incl. ramp)
Oxide Densify	800ºC	750ºC	105 min
Post Bond Anneal	800ºC	770ºC	60 min
Gate Oxidation	800ºC	800ºC	100 min
S/D Activation	1000ºC	1000ºC	10 sec

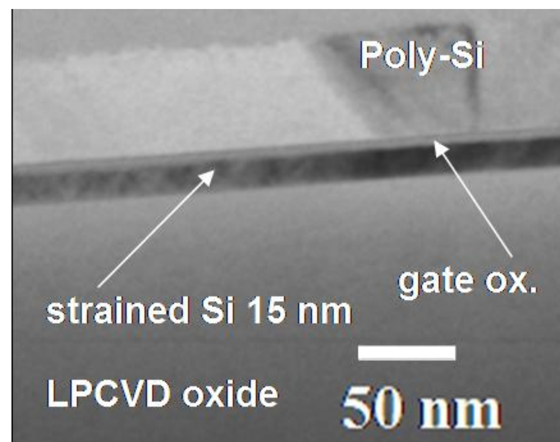

Figure 4.2 XTEM of 30% SSDOI device with 15 nm thick channel. The strained Si channel is directly on the typically 300-500 nm thick BOX, eliminating all Ge from the final structure. XTEM courtesy of J. Li.

Ti barrier was too thin to allow for sufficient forming gas anneals without spiking of the Al into the Si layer. Furthermore, the relatively thin Al layer proved difficult to probe and wire bond. Therefore, the metal thicknesses were increased to 150 nm Ti and 1 µm Al in later device iterations. A forming gas anneal at 450-470ºC for 30 minutes concluded the device process. An XTEM of a 30% SSDOI long-channel MOSFET (W= 15 µm, L=100 µm) is shown in Figure 4.2. Note the absence of any Ge layers in the 15 nm thick strained-SOI structure.

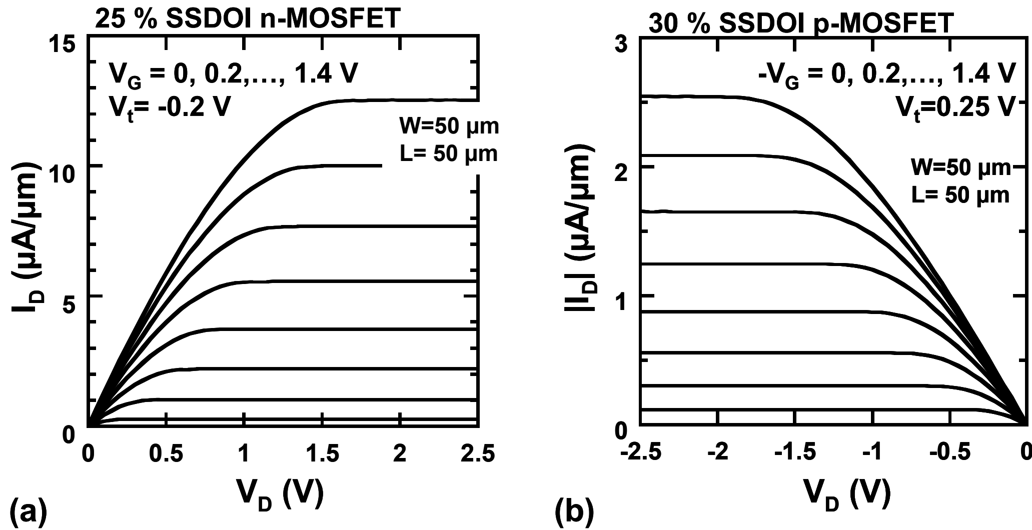

Figure 4.3 Long channel drain current (I_D) vs. drain bias (V_D) for **(a)** a 25% SSDOI n-MOSFET (approximately 17 nm thick strained Si layer) and for **(b)** a 30% SSDOI p-MOSFET (approximately 25 nm thick strained Si layer). Despite the higher nominal strain level (and similar series resistance) of this p-MOSFET than the n-MOSFET in (a), current drive is roughly a factor of 5X lower for the p-MOSFET. This is an indication of the mobility enhancement mismatch between SSDOI n- and p-MOSFETs.

4.2 Basic Device Results

Drain current vs. drain voltage output characteristics of square, long channel, moderately thin SSDOI MOSFETs are shown in Figure 4.3(a) (n-MOSFET), and Figure 4.3(b) (p-MOSFET) for a number of different gate bias conditions. The substrate contact (i.e. the wafer chuck) was at 0 V during the measurements, as was the source. The n-MOSFET in Figure 4.3(a) was fabricated on a 25% SSDOI substrate with t_{Si}~17 nm (after device processing). The p-MOSFET in Figure 4.3(b) was fabricated on a 30% SSDOI substrate with t_{Si}~25 nm. With the low or un-doped bodies, both n- and p-MOSFETs have non-ideal threshold voltages (V_t), but between the two devices the threshold voltages are roughly symmetric, as indicated in the graph.

From Equation 1.5 (long channel I_D in saturation), and ignoring the slight asymmetry in threshold voltage, we obtain an approximate ratio of the effective mobilities in saturation for the long channel 25% SSDOI n-MOSFET to the 30% SSDOI p-MOSFET:

$$\frac{\mu_{eff_NMOS}^{sat}}{\mu_{eff_PMOS}^{sat}} = \frac{I_{D_NMOS}^{sat}}{I_{D_PMOS}^{sat}} \approx 5 \qquad \text{(Equation 4.1)}$$

This number is higher than the typical asymmetry between n- and p-MOSFETs in unstrained Si (in terms of mobility, the extracted linear mobility data for the same devices is a factor 5.5 higher for the n-MOSFET at similar V_{GS}). Thus, even with this simple analysis (which among other things ignores differences in series resistance), we find that the mobility enhancement in strained SSDOI n-MOSFETs seems favorable compared to the p-MOSFET.

In Figure 4.4(a), the drain current vs. gate bias transfer characteristic is shown for a 25% SSDOI n-MOSFET, from the same wafer as the one in Figure 4.3(a). The width of the device is still large, however the device length is reduced to 1 μm (to highlight possible source to drain leakage paths along misfits dislocations, as observed in [85]). As expected for a FD-SOI device, the subthreshold slope is near ideal at 64 mV/decade, similar to unstrained SOI control devices, indicating good gate oxide interface quality. The off-state current level is low. Similarly, for the p-MOSFET in Figure 4.4(b), leakage levels are low and the subthreshold slope is 69 mV/decade for the device shown. Overall, we found that subthreshold slopes were at or below 70 mV/decade for all SSDOI devices. The off-state current level is low (e.g. 0.75 V below threshold), despite the

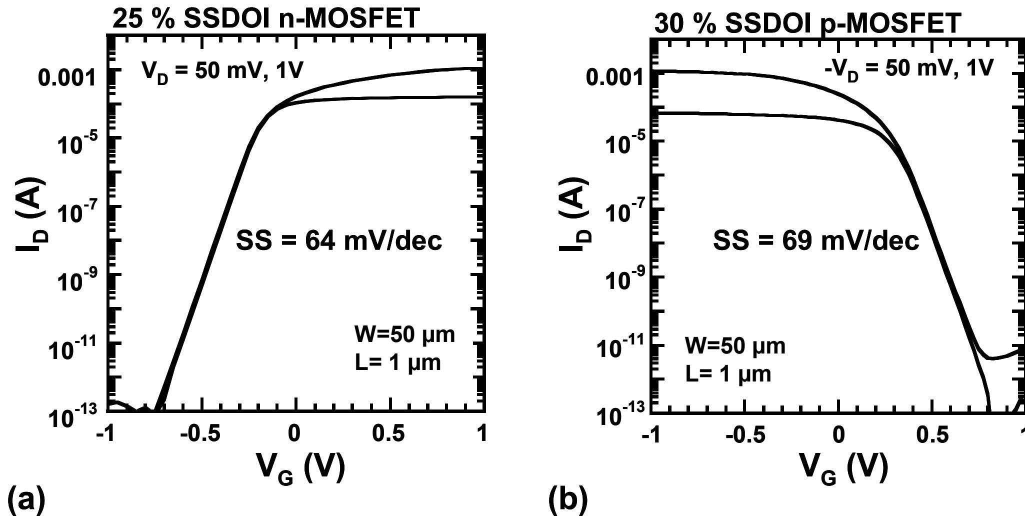

Figure 4.4 (**a**) Drain current (I_D) vs. gate bias (V_G) for a W=50 µm, L=1 µm 25% SSDOI n-MOSFET (same wafer as in Figure 4.3(a)). The off-state current level is low, despite the super-critical thickness as grown strained Si layer thickness (26 nm as grown), confirming the results of Lauer, *et al.* [85]. (**b**) I_D vs. V_G for a W=50 µm, L=1 µm long 30% SSDOI p-MOSFET (same wafer as in Figure 4.3(b), 40 nm as grown thickness of strained Si layer). Sub-threshold swing was typically below 70 mV/dec for both n- and p-MOSFETs.

as-grown layer thickness of 40 nm, which is above the critical thickness [25]. This confirms earlier studies, which have shown that super-critical thickness SSDOI MOSFETs are less prone to off-state leakage than strained Si on bulk relaxed SiGe [85,86].

Due to the lack of a body and body-contact in the FD-SOI devices, split *C-V* techniques can only be used with the device in inversion, when there is a path for carriers in the channel to enter and exit via the source and drain contacts. In accumulation, the reverse-bias pn-junctions prevent collection of carriers from these contacts (in devices with a body contact, such as a bulk Si MOSFETs, the body contact can be used to collect carriers in accumulation). In Figure 4.5, the capacitance-voltage characteristic for a 30%

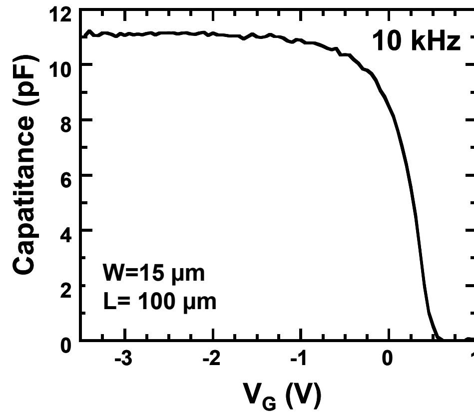

Figure 4.5 Gate-to-channel inversion capacitance of a 25 nm thick 30% SSDOI p-MOSFET. The capacitance was measured at a frequency of 10 kHz to minimize series resistance effects. p-MOSFET SSDOI gates were implanted and typically had poorer electrical activation than the in-situ doped n+ poly-Si gates for the n-MOSFETs.

SSDOI p-MOSFET long channel device used for mobility extraction is shown. The p+ implanted poly-Si gate was activated well after 10 s at 1000ºC. The integrated capacitance is used for extraction of the effective mobility, discussed in the next section.

4.3 Mobility of moderately thin SSDOI MOSFETs

As was described in Chapter 1, the effective mobility (μ_{eff}) is a relevant measure of transport if the inversion charge, Q_{inv}, (integrated capacitance), linear current I_D, and intrinsic drain-to-source voltage V_{DS} can be determined accurately. In the presence of high parasitic resistance (series resistance), the capacitance-voltage curve (*C*-*V*) can shift, e.g. the peak capacitance can decrease in the presence of high series resistance. To minimize errors in the inversion charge, obtained by integration of the *C*-*V* curve as discussed in Chapter 2, capacitance was measured at relatively low frequencies (typically

10 kHz), and it was verified that the capacitance was similar when measuring at half or twice the frequency.

Due to the integration of the *C-V* curve to obtain the channel charge, errors due to lateral shifts in the *C-V* (e.g. from frequency dependent response of traps) are expected to be small when the total inversion charge is large. Multiple measurements of current-voltage (*I-V*) characteristics of each device were taken. The intrinsic V_{DS} was extracted by using the special mobility extraction MOSFET, as described in Chapter 2.

In Figure 4.6, the hole mobility of a 30% SSDOI MOSFET is shown, with two different values of series resistance for the same device. The external resistance was applied in series with the source and drain. The mobility extraction MOSFET (see Figure 2.12) is able to compensate for the large difference in external resistance. The applied (extrinsic) V_{DS} was typically 50 mV for the SSDOI devices described in this section.

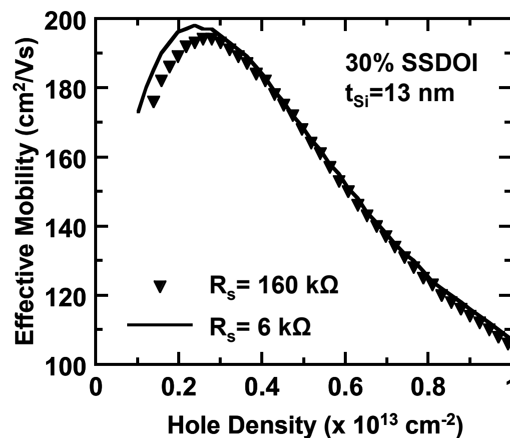

Figure 4.6 Hole mobility of 13 nm thick 30 % SSDOI p-MOSFET. The special mobility extraction MOSFET (Figure 2.12) was used to extract the mobilities in this and later chapters. To illustrate the effectiveness of the technique, the same device was measured using two different external values of series resistance applied in series with the source and drain contacts. The extracted effective mobility is nearly identical in the two cases.

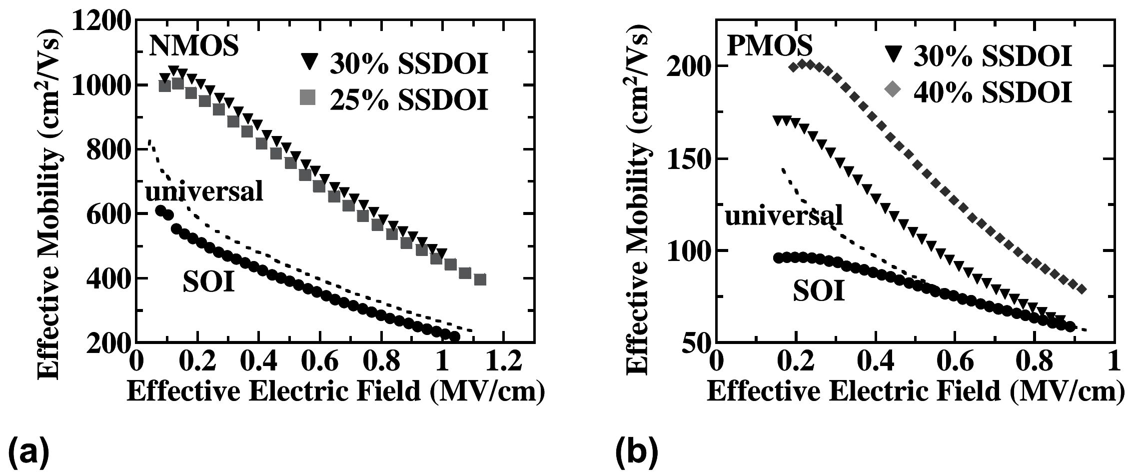

Figure 4.7 (**a**) Electron effective mobility of 25% and 30% SSDOI (~15 nm thick) as a function of effective electric field (E_{eff}, see Equation 1.6). As in bulk strained Si on relaxed SiGe, the electron mobility enhancement is 1.8X at all fields compared to universal mobility. (**b**) Hole effective mobility of 30% SSDOI (8 nm thick) and 40% SSDOI (14 nm thick) vs. E_{eff}. The hole mobility in SSDOI is enhanced primarily at low fields. High strain levels, corresponding to 40% SSDOI (~1.7% lattice in-plain strain) are required to achieve mobility enhancement at high fields. The universal mobilities in (a) and (b) are from Takagi *et al.* [15].

SSDOI Electron Mobility

The electron mobilities of moderately thin 25% and 30% SSDOI as a function of the vertical effective electric field (E_{eff}, see Chapter 2) are shown in Figure 4.7(a) [77]. For comparison, the mobilities of the unstrained SOI control as well as the universal mobility have been included [15]. As in biaxially tensily strained Si on relaxed $Si_{1-y}Ge_y$, the electron mobility in SSDOI is enhanced by 1.8X compared to the universal mobility at all fields, and the enhancement compared to the unstrained SOI control is approximately 2X, i.e. twice the mobility is achieved in SSDOI.

As previously discussed, since the electron mobility enhancement in biaxially tensily strained Si is primarily due to a re-population of the electrons from the Δ_4 to the Δ_2

valleys where they have a lower in-plane conductivity mass, the mobility enhancement saturates once most electrons are in the lower valley. Thus, between 25% and 30% SSDOI, little further enhancement in electron mobility is gained.

The mobility of the unstrained SOI control appears slightly degraded compared to the universal mobility (from Ref. [15]) at all fields. Differences in the processing environment such as gate oxide growth conditions and quality could explain this difference, but errors from the mobility extraction procedure and lot to lot variations could also contribute. For this reason, the mobility comparisons in this thesis are kept within lots (and with similar processing) whenever possible so that mobility control wafers and strained device wafers have received similar processing conditions.

SSDOI Hole Mobility

The hole mobility of moderately thin 30% and 40% SSDOI is shown in Figure 4.7(b) [77,87]. At low fields, the hole mobility doubles for 40% SSDOI compared to the unstrained SOI control. At high fields, the SSDOI hole mobility enhancement factor decreases and is nearly eliminated at the highest fields for 30% SSDOI. The 14 nm thick 40% SSDOI has a mobility enhancement factor of 1.4X at the highest fields.

In the introductory chapter (section 2.1), it was argued that in tensily strained Si, the quantization mass of the ground-state band (the light hole band) is lower than the quantization mass of the first excited state band (the heavy hole band). Thus, as the field-induced confinement is increased due to an increased vertical field, the separation between the bands is decreased causing an increase in phonon scattering at higher fields.

This has been proposed as one of the mechanisms behind the decreasing mobility enhancement factor in biaxially tensily strained Si [46]. In this respect, SSDOI again behaves similar to strained Si on bulk relaxed $Si_{1-y}Ge_y$.

One advantage of SSDOI compared to the bulk strained Si is the absence of Ge altogether in the substrate entering device fabrication. Thanks to the Ge-free structure, even super-critical thick strained SOI layers (see Table 4.1) can be fabricated with high thermal processing in the device process (Table 4.2) without issues related to Ge up-diffusion. Furthermore, in the thick super-critical thickness layers, off-state leakage can be kept low in SSDOI, which has been attributed to the removal of the lateral misfits at the Si/SiGe interface during substrate preparation [80]. For example, the 25 nm thick 30% SSDOI device in Figure 4.4(b) was fabricated from a 40 nm thick as-grown strained Si layer, in the meta-stable regime [25,35]. Yet, the mobility enhancement in such thick SSDOI was still retained, and the leakage was low. In Figure 4.8, the peak mobilities of 30% SSDOI across a wide range of moderately thin channel thicknesses are shown. The upper limit to the thickness is given by critical thickness considerations and the growth and processing conditions. For the 25 nm thick SSDOI (as grown 40 nm), strain relaxation corresponding to approximately 5 atomic percent compared to the target strain level was recorded by UV-Raman analysis [82], though with little effect on leakage and mobility. Note that substantially thicker layers can be achieved by decreasing the substrate strain level such as the record thick SSDOI in Ref. [88]. In Section 4.4, the SSDOI mobility vs. thickness relationship will be examined for ultra-thin (<5 nm) body thicknesses.

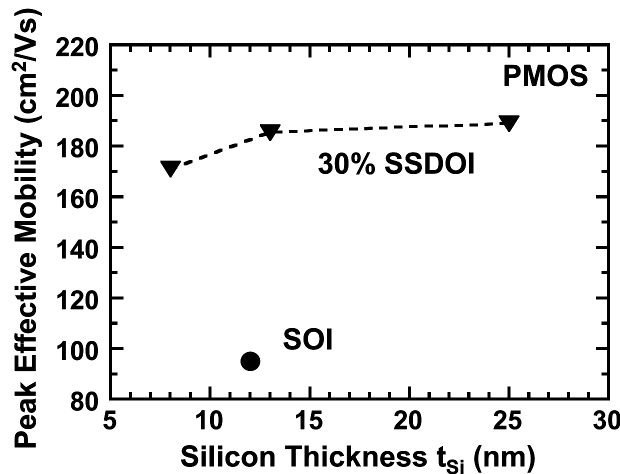

Figure 4.8 Peak hole mobility (low field mobility) as a function of strained Si layer thickness for 30% SSDOI. In the range 8-25 nm (as grown thicknesses 20-40 nm) peak mobility is nearly constant. For results on even thicker SSDOI, see [88].

4.4 The Ultra-thin Body SSDOI p-MOSFET

In this section, the transport in ultra-thin body SSDOI p-MOSFETs is described [78]. First, relevant changes in the device fabrication scheme from section 4.1 are described; next the method of strained Si thickness extraction is covered. The section is concluded with a discussion of measured mobility in the ultra-thin body SSDOI p-MOSFET.

Device Fabrication

The device fabrication scheme was described for moderately thin SSDOI MOSFETs in section 4.1. This flow was slightly altered to achieve working UTB SSDOI MOSFETs. In order to reduce series resistance, the strained Si film was locally thinned under the gate areas on select substrates as part of the substrate preparation module (see Figure 4.1(a)). The substrate preparation for UTB SSDOI is illustrated in Figure 4.9. The starting

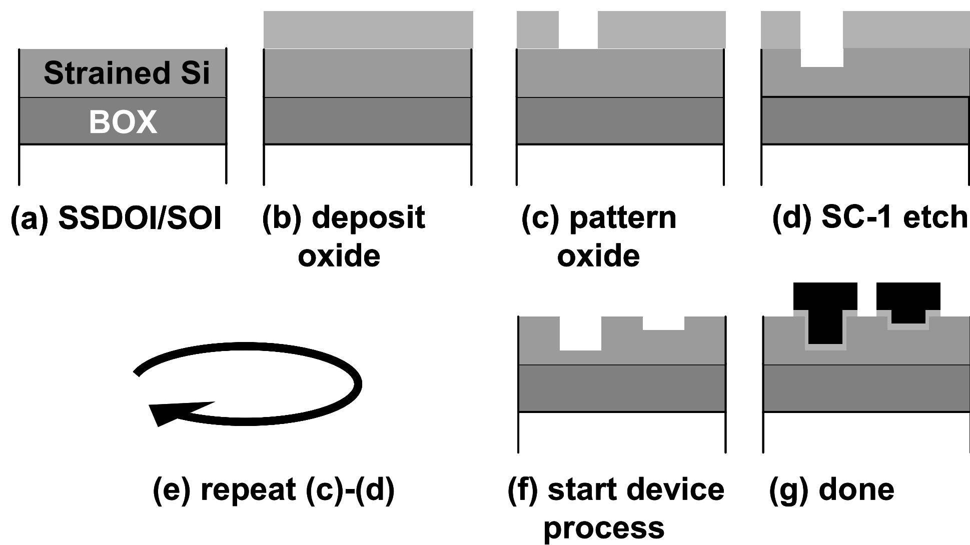

Figure 4.9 Selective thinning of gate regions for ultra-thin body MOSFETs: (a) starting SSDOI or SOI substrate (b) an LPCVD oxide is deposited (100-200 nm) to serve as hard-mask (c) oxide patterning by diluted buffered HF (d) slow and well controlled etch of substrate in SC-1, layer thickness measured by ellipsometry (e) To create multiple thickness splits on each wafer the sequence is repeated. (f) The device process continues as usual (see Figure 4.1). (e) The final devices have a recessed gate. Note that the drawing is not to scale. Mobility extraction devices are 100 μm long. The recessed gate enables thick source and drain regions even with channel thicknesses in the 1-5 nm range.

substrate in 4.9(a) was approximately 20-30 nm thick 30% or 40% SSDOI. In Figure 4.9(b) and (c), a low pressure chemical vapor deposition oxide hard mask was deposited and etched by buffered HF in gate regions to create openings in the oxide layer. The heated SC-1 etch (see Chapter 3) was subsequently used to etch the strained Si in the openings (Figure 4.9(d)). The oxide patterning and strained Si etch were repeated three to four times to create a number of different thickness splits on a single wafer. The final device after completing the device process of section 4.1 is shown in Figure 4.9(g). This process creates recessed gate MOSFETs with ultra-thin strained Si layers but thicker source and drain regions, which allows for extraction of mobility on extremely thin

substrates. The critical step is etching of the strained Si layer in SC-1. In Figure 4.10, the etch rate of strained Si in SC-1 is shown as a function of the etch time. Prior to the etch step and prior to measuring the film thickness by ellipsometry, the native oxide was stripped in diluted HF. As evident in Figure 4.10, the initial etch rate is higher than for longer etch steps. Careful characterization of the SC-1 etch enabled precise layer thickness control.

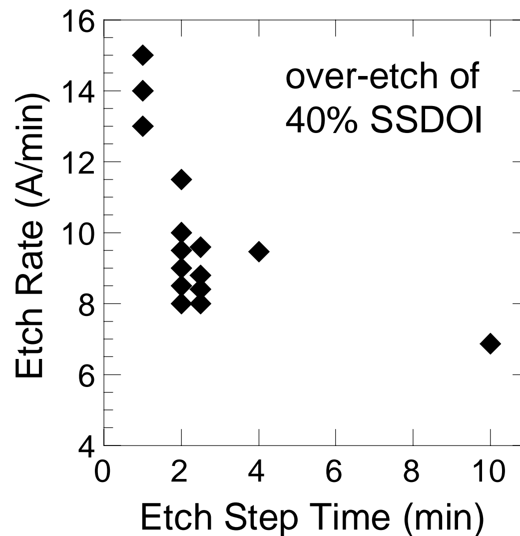

Figure 4.10 The etch step time for the (over-) etch of strained Si in SC-1 is carefully selected in the selective thinning process (Figure 4.9(c)) to closely meet the target final layer thickness. The usual sequence consisted of multiple 2 minute etches, with diluted HF dips in between. The loss of Si thickness in the device process (cleaning and gate oxidation) was ~4 nm. To create the thinnest MOSFETs in this work, the strained Si thickness after this thinning procedure was 5-7 nm.

Strained Si Thickness Extraction

The mobility is a strong function of layer thickness in the sub-5 nm regime. Even errors on the order of 1 nm in layer thickness extraction could lead to misinterpretation of results, and erroneous comparisons with previously published data. For this reason, the extraction of strained Si layer thicknesses on the UTB-SSDOI p-MOSFETs was primarily done by lattice-imaging cross section transmission electron micrographs (XTEM), performed on actual devices after mobility extraction was completed. The XTEM preparation and microscopy was done by Accurel Systems [89]. However, to extend the number of data points, film thicknesses on devices within the same die as a XTEM-device were extracted by matching capacitance-voltage (*C-V*) characteristics to

TABLE 4.3
SUMMARY OF UTB-SSDOI DEVICES

y% SSDOI[a]	Si Thickness (nm)	Si Thickness Extraction Method[b]	Local Substrate Thinning[c]
40%	2.8	XTEM	Yes
40%	3.1	XTEM	Yes
40%	5.5	XTEM	Yes
30%	1.4	XTEM	Yes
30%	3.2	XTEM	Yes
30%	3.3	*C-V*	Yes
30%	3.5	*C-V*	Yes
30%	3.7	*C-V*	Yes
30%	3.9	XTEM	No
30%	4.8	*C-V*	Yes
30%	5.5	*C-V*	Yes
30%	6.0	*C-V*	Yes
30%	7.2	XTEM	No

[a]An SSDOI substrate with as grown relaxed $Si_{1-y}Ge_y$ buffers is referred to as “y% SSDOI”.
[b]Devices with Si thickness extracted by XTEM were used to calibrate the *C-V* extraction.
[c]Locally thinned regions were masked by LPCVD oxide and thinned by chemical etching in SC-1.

measurements in one dimensional coupled effective mass Poisson-Schrödinger quantum simulations in *Schred* and *nextnano*^{3} [90,39]. The extraction of effective masses from bulk *k.p* simulations in *nextnano*^{3} (see section 2.1, table 2.2) indicated an in-plane effective mass of approximately 0.28 (in units of the free electron mass) and out of plane mass of 0.2 for the light hole band (which is the lowest energy band in the tensily strained Si). Extractions were made keeping the effective masses constant, but allowing variations in buried oxide thickness (across the wafer buried oxide variations were experimentally sometimes 100 nm or more), and minor DC-shifts due to fixed charge. After these varying parameters had been calibrated on a given XTEM device (with a known strained Si thickness), all parameters except the strained Si thickness were kept constant for devices within the same die, i.e. within ~5 mm from the XTEM site. In Table 4.3, the UTB SSDOI p-MOSFET devices are summarized, with their respective thickness extraction technique indicated. In Figure 4.11, the simulated (*Schred*) and measured *C-V* for an 3.2 nm thick 30% SSDOI p-MOSFET is shown for two back-bias configurations. XTEMs of 3.1 nm 40% SSDOI and 1.4 nm thick 30% SSDOI p-MOSFETs are shown in Figure 4.12. The continuity of the thin films was monitored by studying the capacitance, making sure the area remained constant between different devices.

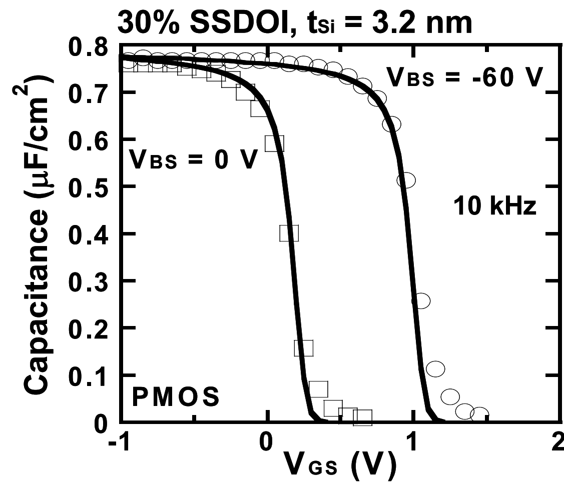

Figure 4.11 Simulated (lines) and measured (symbols) *C-V* of 3.2 nm thick 30% SSDOI at two back-bias conditions. The simulation was done in Schred, a self-consistent Schrödinger-Poisson electrostatics simulation tool [90].

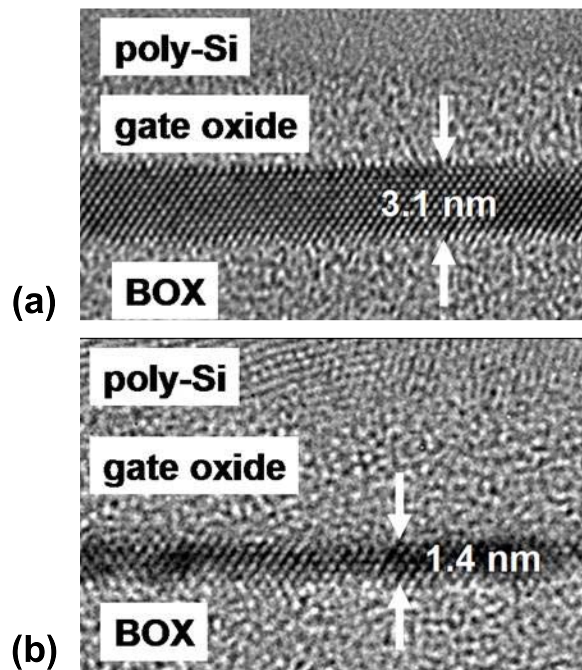

Figure 4.12 XTEMs of (a) 3.1 nm-thick 40% SSDOI, and (b) 1.4 nm-thick 30% SSDOI. XTEM by Accurel Systems.

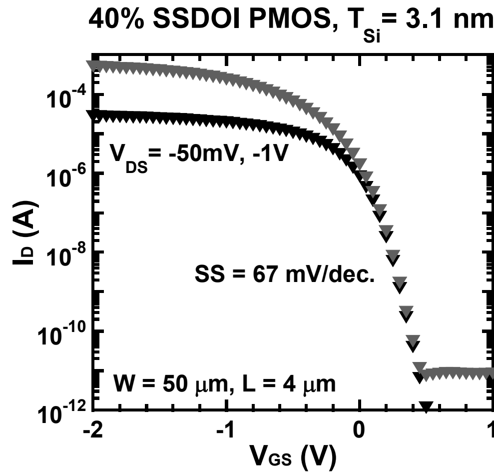

Figure 4.13 Sub-threshold characteristics of 40% SSDOI p-MOSFET with 3.1 nm-thick strained Si layer. Sub-threshold slopes remained at or below 70 mV/dec. even for the thinnest devices, indicating good interface quality.

Mobility of the UTB SSDOI p-MOSFET

The sub-threshold characteristics remained good (< 70 mV/dec.) for the UTB SSDOI p-MOSFETs presented in this section, despite the ultra-thin channel thicknesses, as in Figure 4.13. Unstrained SOI mobility is expected to decrease rapidly as the film thickness is scaled below 4 nm, as discussed in Chapter 2. In Figure 4.14(a), the hole mobility of unstrained SOI control p-MOSFETs is shown. The hole mobility of our measured SOI devices (symbols) agrees well with previously published data by Uchida, *et al.* (lines) [60], indicating the ability of the processing conditions to re-produce the hole mobility trend for unstrained SOI. The 30% SSDOI device results in Figure 4.14(b) indicate that hole mobility is also decreasing for ultra-thin films of strained Si. However, the hole mobility in 3.9 nm thick 30% SSDOI is still enhanced compared to the 15 nm thick unstrained SOI control device. For film thicknesses above ~ 4 nm, the mobility is degraded primarily at low vertical effective fields. Below 4 nm, the mobility

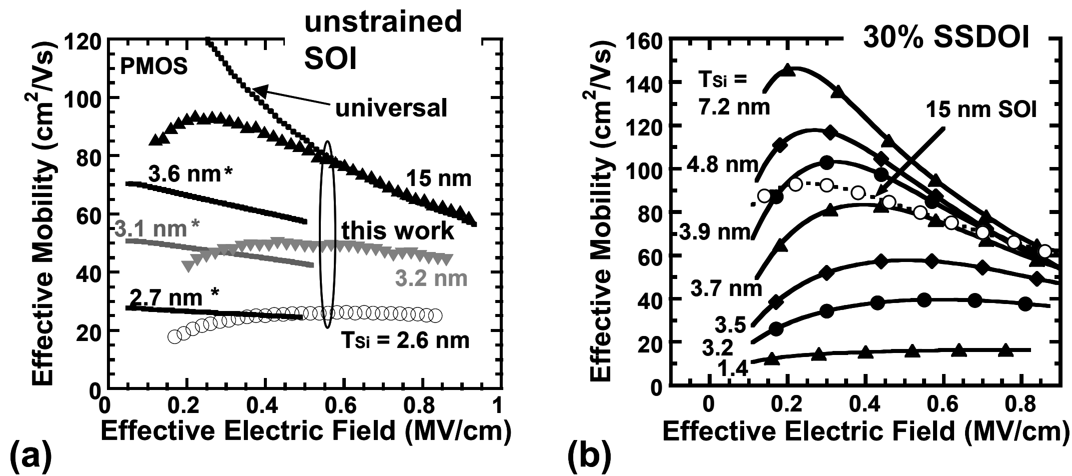

Figure 4.14 (**a**) Hole mobility vs. effective field for unstrained SOI control devices of this work (symbols), and from Ref. [60] (lines, labeled with *). The universal mobility is indicated [15]. The unstrained SOI mobility corresponds well with earlier published results. The mobility decreases rapidly in ultra-thin unstrained SOI. (**b**) Hole mobility vs. effective field for 30% SSDOI with ultra-thin strained Si thickness (the thickness is indicated) of this work. Though SSDOI hole mobility decreases for thin film thicknesses, the mobility of 3.9 nm-thick 30% SSDOI is still enhanced compared to the 15 nm-thick unstrained SOI control.

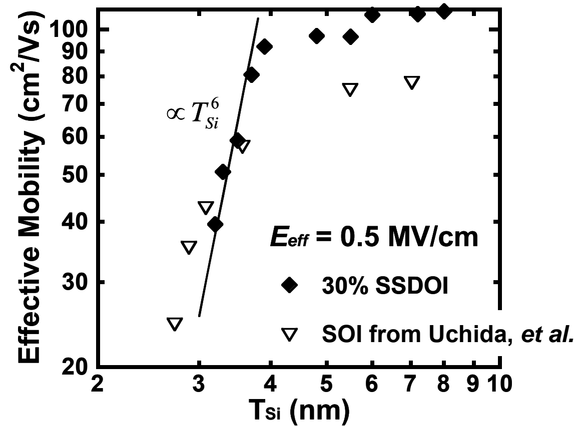

Figure 4.15 Hole mobility vs. film thickness at a vertical effective field of 0.5 MV/cm for the 30% SSDOI of this work and the unstrained SOI from Uchida, *et al.* [60]. At this field, the low dose channel implant has limited influence on mobility [91]. Mobility for SSDOI decreases rapidly below 3.9 nm thickness, similar to the trend in unstrained SOI. The mobility dependence for thickness fluctuation induced scattering ($\propto T^6$) agrees well with the hole mobility in 30% SSDOI thinner than 4 nm.

degradation is different in character and affects both low- and high-field mobility, and decreases very quickly with thickness. In Figure 4.15, the low field hole mobility from the 30% SSDOI of this work is compared to the unstrained SOI hole mobility from Uchida, *et al.* [60]. Both strained and un-strained mobilities show similar trends with slowly decreasing mobilities down to 4 nm thickness, and rapidly decreasing mobilities below that thickness.

In unstrained SOI, the rapid change in mobility below 4 nm has been attributed to the layer thickness fluctuation limited mobility, which can be verified by its characteristic low-temperature behavior (which distinguishes it from e.g. phonon scattering) [62]. A simplified description of the layer thickness fluctuation limited mobility is shown in Figure 4.16. When the total layer thickness is only a few nm, even thickness fluctuations on the order of atomic layers lead to variations in the ground state energy level. If a simple infinite well approximation is assumed, then this leads to fluctuation of the potential ΔV according to

$$E = \frac{\hbar^2 \pi^2}{2 m_z T_{Si}^2}, \qquad \Delta V = \frac{\partial E}{\partial T_{Si}} \Delta, \qquad \text{(Equation 4.2,4.3)}$$

where Δ is the height of the fluctuation. The potential variation scatters carriers so that

$$\mu_r \propto \left(\frac{1}{\Delta V} \right)^2 \propto T_{Si}^6. \qquad \text{(Equation 4.4)}$$

The strong thickness dependence of the mobility makes this scattering mechanism dominant for ultra-thin channel thicknesses. In Figure 4.16, it should be clear that in this

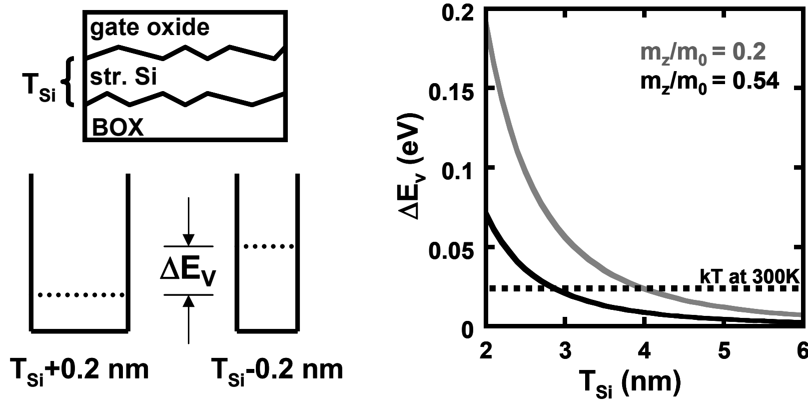

Figure 4.16 For ultra-thin SOI or SSDOI films, uneven oxide interfaces (even with mono-layer steps) cause variations in thickness that are large on a relative scale. The fluctuation of the film thickness causes variations in the energy levels of the quantized valence bands, inducing potential variations that scatter the holes. The corresponding mobility is a strong function of film thickness ($\propto T_{Si}^6$) but also depends on the effective mass (in the diagram, m_z=0.2 is the strained Si value from Table 2.2 and m_z=0.54 is the Si HH default value in *nextnano³* [39]) and temperature. Though this model [62] is simplified, it provides a reasonable qualitative picture of the origin of the thickness fluctuation induced scattering.

very rough model, the ground-state variations are worse for lower quantization-mass materials, for thinner films, but also for lower temperatures. The reason is that at lower temperatures, the carriers have a lower thermal energy, making ground state variations proportionally larger.

Since the hole mobility of 30% SSDOI (with T_{Si} < 4 nm) in Figure 4.15 agrees well with the thickness dependence for thickness fluctuation induced scattering, $\mu \propto T_{Si}^6$, measurements were performed on wire bonded devices at low temperatures to confirm the cause of the mobility reduction. The result for devices with 7.2 nm and 3.5 nm strained Si thickness is shown in Figure 4.17. The mobility vs. hole density is qualitatively different for the two thicknesses shown in Figure 4.17 (a) and (b). The 7.2

nm-thick device has increasing mobility at all hole densities as the temperature is lowered, which is the usual behavior for thick SOI or bulk Si (or strained Si). This is consistent with a decrease in the phonon limited scattering as the temperature is reduced.

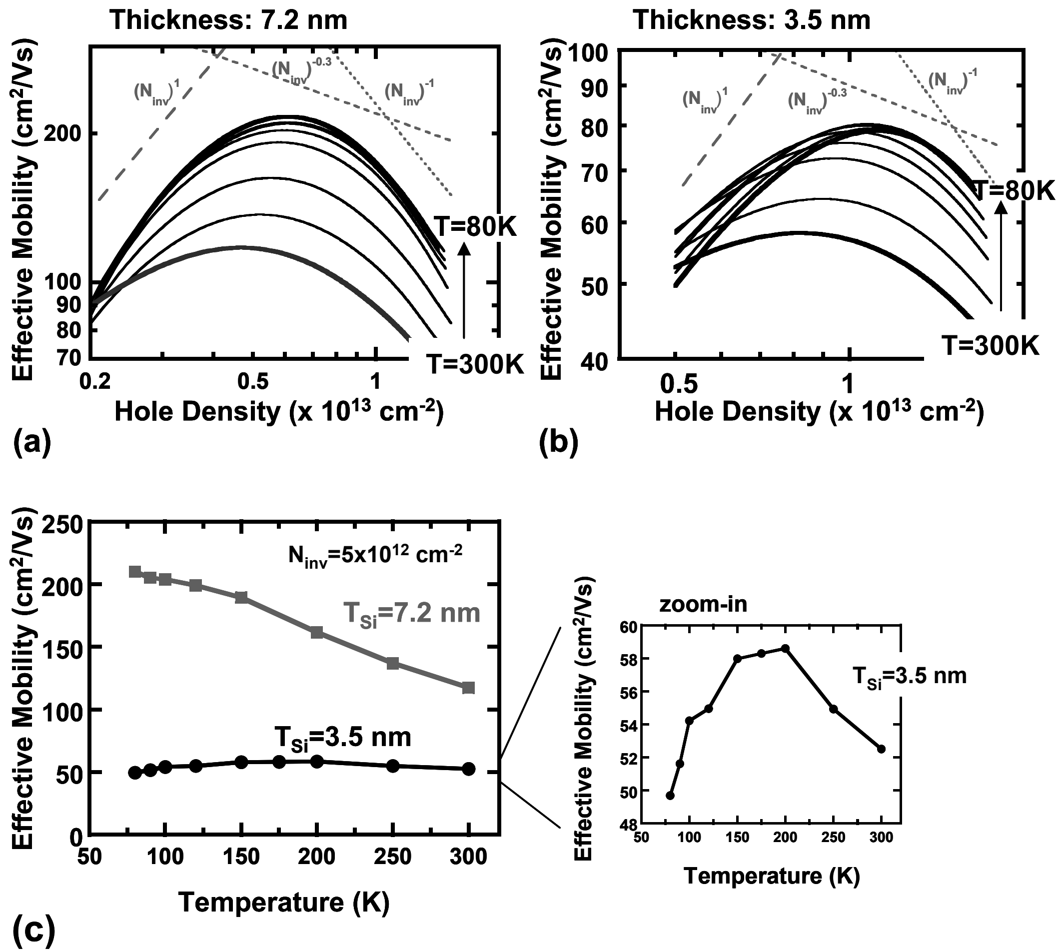

Figure 4.17 The hole mobility vs. inversion charge density for a range of temperatures for **(a)** 7.2 nm-thick 30% SSDOI and **(b)** 3.5 nm-thick 30% SSDOI. The typical bulk Si trend-lines for Coulomb-, phonon-, and surface roughness-limited mobility have been indicated [15], in UTB-SOI, the phonon limited mobility has a flat field dependence [56]. **(c)** For the 7.2 nm-thick SSDOI the mobility vs. temperature increases monotonically as the temperature is lowered, while for the 3.5 nm-thick SSDOI mobility is relatively constant. The zoom-in shows that the mobility in the thin sample first increases, then decreases as temperature is lowered. This is a signature of the influence of both phonons and layer thickness fluctuation scattering [62,92].

For the 3.5 nm thick device, the mobility follows the same trend as for the thicker device at high hole densities, where phonons and surface roughness (SR) scattering usually dominate. At high hole densities, the high field causes carriers to be more influenced by the triangular potential from the field than at low hole densities, even in ultra-thin layers. At low hole densities, the 3.5 nm thick device has a non-traditional behavior with first increasing, then decreasing mobility as the temperature is lowered. This behavior cannot be explained solely by the reduction of phonon scattering.

In Figure 4.17(c), the mobility vs. temperature at a low hole density is shown, making the qualitative difference between the two samples clear. On the large scale, the mobility of the thin sample looks almost independent of temperature, an indication that the influence of phonons is limited. The zoom-in again shows the characteristic increase and then reduction in mobility as the temperature is lowered. This behavior is consistent with a reduction of phonon scattering at lower temperatures coupled with an increased effect of the thickness fluctuation limited mobility as the temperature is lowered, and has previously been observed similarly for electrons in GaAs/AlAs quantum wells intentionally grown with rough interfaces [92], and in unstrained SOI [62]. Intuitively, at low temperatures, the fluctuation induced energy changes are more significant on a relative scale, as discussed with respect to Figure 4.16.

The formalism in more advanced models of thickness fluctuation limited mobility follows that of surface roughness (SR) limited mobility, see e.g. [46,92], but since the scattering is due to confinement between two surfaces, it is the thickness of the layer (not the field as in SR mobility) that creates the strongest dependence. In fact, the

experimental evidence suggests that thickness fluctuation limited mobility is most severe at low bias, where the confinement is mostly induced by the well thickness and not the field. Therefore, while the formalism of thickness fluctuation induced scattering is similar to SR scattering, its dependency on vertical field is weak or even opposite that of SR scattering. For this reason, bulk-like SR scattering is not responsible for the mobility degradation in ultra-thin SSDOI. Coulomb scattering is a mechanism mostly appearing in Si MOSFETs at low fields (it is screened by the inversion charge at higher fields). Though it cannot be excluded that an increase in Coulomb scattering contributes to the mobility in Figure 4.17(b), it appears unlikely that it is a major factor. It was confirmed that sub-threshold swing is comparable at low and high temperatures even in the 3.5 nm-thick device.

To summarize, the experimental evidence from the mobility vs. thickness (Figure 4.15) and mobility temperature response (Figure 4.17) supports the finding that thickness fluctuation induced scattering is indeed the cause of the observed rapid degradation of hole mobility in 30% SSDOI of less than 4 nm thickness. The thickness fluctuation limited mobility is best distinguished from the mobility degradation from phonon scattering (see Chapter 2) by its temperature response, and much stronger dependence on thickness, $\mu \propto T_{Si}^{6}$.

Biaxial tensile strain seems to be effective in enhancing hole mobility primarily down to ~ 4-5 nm thick films. Below this point, the thickness fluctuation limited mobility degrades mobility sharply. In the discussion above, the comparison was made between UTB-30% SSDOI and SOI. Since one of the main scattering mechanisms in this

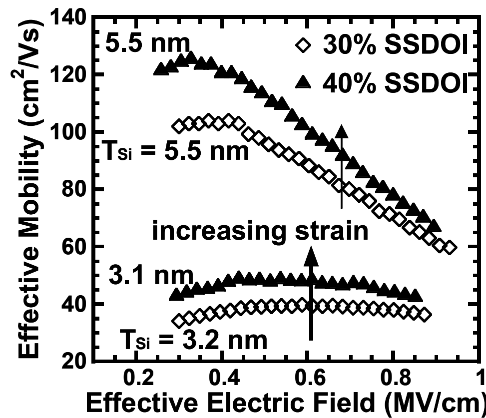

Figure 4.18 Hole mobility vs. vertical effective field for 30% SSDOI and 40% SSDOI with two, pair-wise matched thicknesses. For both the thicker (5.5 nm) and thinner (~3 nm) sample pairs, the mobility increases when the strain level is increased. Strain engineering is thus effective even in extremely thin-body MOSFETs. Locally thinned MOSFETs were used for this comparison.

thickness range is related to fluctuations in the film thickness, it is important to compare films with similar expected roughness on both the top and bottom oxide interfaces. For the unstrained SOI of this work, the buried oxide was grown thermally (by the manufacturer, SOITEC, [79]), different from the deposited oxide of the SSDOI. A limited number of 40% SSDOI UTB-MOSFETs were also prepared by the bond and etch-back process. In Figure 4.18, four mobility curves are shown. Two of them are for 40% SSDOI and two of them are for 30% SSDOI. These mobility curves are paired so that each 40% SSDOI device has a 30% SSDOI device with matched strained Si thickness. Though this is a limited sample set, the results indicate that even for SSDOI as thin as 3 nm, there could be a benefit from strain engineering. A recent theoretical study by Khakifirooz, *et al.* [93] has studied the effective masses and scattering in ultra-thin SOI and SSDOI more rigorously in a tight binding model. The results indicate that band

separation, as well as changing effective masses, may help explain the result that high levels of biaxial tensile strain may be beneficial even in such thin films where thickness fluctuation induced mobility scattering is dominant.

4.5 Chapter Summary

In this chapter, the fabrication of n- and p-MOSFETs in SSDOI of moderately thick channel thickness (~8-25 nm) was first described. In this thickness range, transport in SSDOI inversion layers is similar to transport in bulk strained Si on relaxed SiGe inversion layers. For electrons, the mobility at all fields is enhanced by 1.8X-2X compared to universal and unstrained SOI control mobilities. The enhancement of electron mobility is similar for 25% and 30% SSDOI (i.e. equivalent to the strain level in strained Si on relaxed $Si_{0.75}Ge_{0.25}$ and $Si_{0.7}Ge_{0.3}$ respectively), which follows earlier observations in bulk biaxially tensily strained Si. For holes, the mobility of 30% SSDOI is enhanced primarily at low fields and the mobility enhancement decreases at high fields. At high fields, the hole mobility of 30% SSDOI is identical to the mobility of unstrained SOI control devices. For this reason, biaxial tensile strain technology favors electron mobility enhancement. The decreasing hole mobility enhancement at high fields can be qualitatively understood from the decreasing separation between the first and second sub-band in the (approximately) triangular well as the field increases. This is similar to observations in bulk strained Si on relaxed SiGe. In order to obtain mobility enhancement at the highest fields, high strain levels corresponding to 40% SSDOI need

to be introduced. In this chapter, we found that in 14 nm thick 40% SSDOI, the hole mobility enhancement at high fields is approximately 1.4X.

In SSDOI p-MOSFETs with Si thickness of 1.4-7 nm, the mobility is decreasing as the thickness is reduced. First, the decrease in mobility is slow and primarily at low fields, a result of increased phonon scattering. 30% SSDOI with 3.9 nm thickness has enhanced mobility compared to 15 nm thick unstrained SOI control devices. For film thicknesses below 4 nm, the strained Si hole mobility decreases rapidly. The observed mobility dependence on thickness, $\mu \propto T_{Si}^{6}$, and measurements at low temperature suggest that thickness fluctuation induced scattering dominates for films of less than 4 nm thickness, similar to observations in unstrained SOI. However, measurements on 30% and 40% SSDOI with thickness down to 3 nm indicate that strain engineering can still be used to improve mobilities for such thin films.

Chapter 5

Strained Si/SiGe Heterostructure on Insulator MOSFETs

In the previous chapter, we found that while strained Si directly on insulator (SSDOI) has attractive electron transport properties, hole mobility enhancements at high fields require very high strain levels. Furthermore, the hole mobility in (001) Si is already low. To address this, hybrid-orientation substrates with (001) Si for electrons and (011) Si for holes have been proposed [94]. As was discussed in the introductory material, the first strain enhanced p-MOSFETs in production made use of a compressively strained Si channel on (001) Si, which has been an effective way to enhance hole transport and performance [2]. Another approach, investigated in this chapter, is to implement compressive biaxial strain rather than biaxial tensile strain for the p-MOSFET, and to combine the strain with a new channel material (SiGe) with higher hole mobility than Si. In Chapter 2, results from experiments on strained Si/strained SiGe heterostructure-on-bulk MOSFETs were reviewed, indicating hole mobility enhancements of up to 10X in biaxially compressively strained Ge on bulk $Si_{0.5}Ge_{0.5}$ [45]. Such high mobility enhancement factors motivate further study of strained Si/SiGe heterostructures,

especially for ultra-thin fully-depleted applications which might allow for better electrostatic control, coupled with higher hole mobilities.

In this chapter, strained Si/strained SiGe heterostructure-on-insulator (HOI) MOSFETs with a 12 nm thick $Si_{0.54}Ge_{0.46}$ buried hole channel are presented. Both n-MOSFETs and p-MOSFETs were fabricated on the HOI substrates (see Chapter 3 for a description of the substrate fabrication process), but emphasis will be on the p-MOSFET. First, the HOI structure is introduced and the experimental splits on strain and Ge concentration are presented. Next, the MOSFET device fabrication process is described. Basic device characteristics are presented, with particular attention paid to the extraction of the strained Si cap thickness from capacitance-voltage (*C-V*) characteristics. The mobilities of HOI n- and p-MOSFETs are presented. Comparisons will be made with SSDOI MOSFETs, and the importance of the strained Si cap will be examined. The chapter is concluded with a presentation of transport in HOI p-MOSFETs after thermal annealing.

5.1 The HOI Structure

In this section, the HOI structure is introduced [65]. Figure 5.1 shows a diagram of an HOI structure and associated band diagram. From Chapter 3, recall that the HOI substrate is derived from the three top-most layers of the as-grown epitaxial wafer, as depicted in Figure 5.1(a). The in-plane biaxial lattice parameter is matched to the relaxed $Si_{1-y}Ge_y$ layers, which are subsequently removed during the layer transfer process, leaving only a compressively strained $Si_{1-z}Ge_z$ layer, surrounded by tensily strained Si.

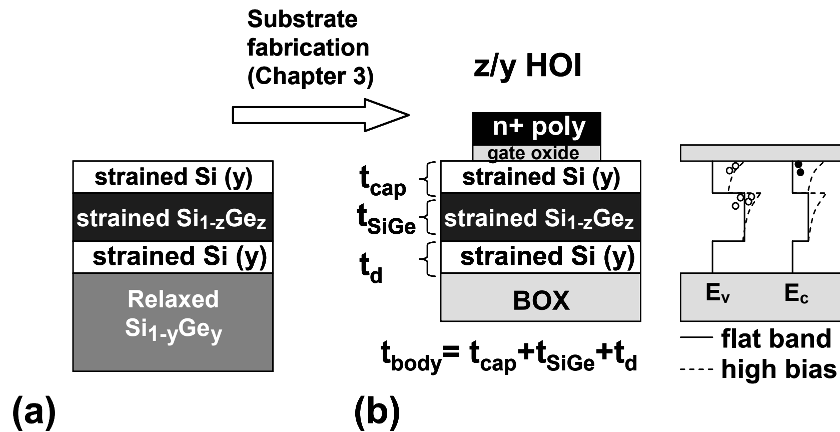

Figure 5.1 The HOI structure. **(a)** The as grown epi layer stack, indicating that the starting wafer, as well as the HOI is lattice matched to a relaxed $Si_{1-y}Ge_y$ layer. **(b)** After substrate fabrication (see Chapter 3), the top three layers (two tensily strained Si layers surrounding a compressively strained $Si_{1-z}Ge_z$ layer) of the as grown epi stack have been transferred to an oxidized handle wafer. The band diagram indicates that the n-MOSFET is a surface channel device, the p-MOSFET is a buried, or mixed buried/surface channel device.

Consider the conduction band in Figure 5.1. The top strained Si layer (later referred to as the Si *cap*) hosts the inversion layer for the electrons. The HOI n-MOSFET is a surface channel device and the channel material is strained Si, as in SSDOI or strained Si on bulk relaxed SiGe. For the p-MOSFET, the valence band off-set (~0.45 eV, [37]) between the Si cap and the strained $Si_{1-z}Ge_z$ layer favors hole inversion in the buried $Si_{1-z}Ge_z$ layer. However, with an increasing field, holes may eventually start to populate the Si cap layer as well, which negatively impacts the overall hole mobility. The most straightforward solution would be to consider a p-MOSFET structure without either the top or bottom strained Si layer (a strained SiGe-directly-on-insulator device), as in [95]. Due to the lack of a suitable gate dielectric on SiGe, such structures have other issues. One way of thinking about the Si layers in the HOI p-MOSFET is as interfacial layers

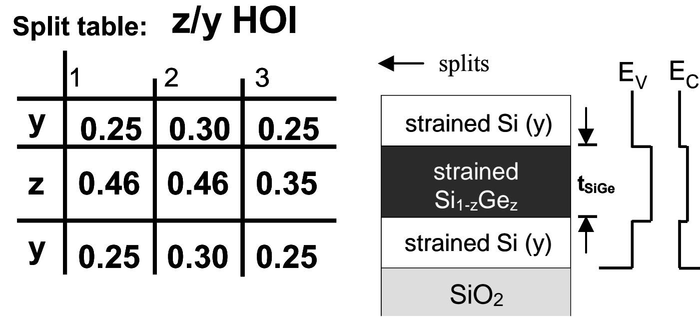

Figure 5.2 The experimental splits. Three splits were prepared, varying the z and y parameters in the z/y HOI structure. Here, z is the concentration of Ge in the buried $Si_{1-z}Ge_z$ layer and y is indicating the in-plane lattice parameter of the three layers (in equivalent Ge content of a relaxed $Si_{1-y}Ge_y$ relaxed layer).

near the oxide interfaces, necessary (for now) to create interfaces with high electrical quality at the top and bottom electrodes. In Figure 5.2, the experimental splits are defined. The tensile strain level (determined by the substrate Ge fraction y) and buried channel Ge fraction z (where z>y and z-y is a measure of the compressive strain of the buried $Si_{1-z}Ge_z$ layer) were varied, as well as the Si cap thickness. The thickness of the buried SiGe channel was kept constant at 12 nm, and the bottom strained Si layer was 3-4 nm. In the following presentation, the emphasis will be on p-MOSFETs, though n-MOSFETs were fabricated as well to serve as mobility references.

5.2 The HOI MOSFET fabrication process

In this section, the fabrication of moderately thin SiGe-channel HOI MOSFETs is described. The fabrication sequence of HOI and SSDOI is similar, except minor details relating to thermal budget and gate stack deposition. For this reason, refer to Chapter 4.1 and Figure 4.1 for a description of the general process sequence (and to Appendix C for a

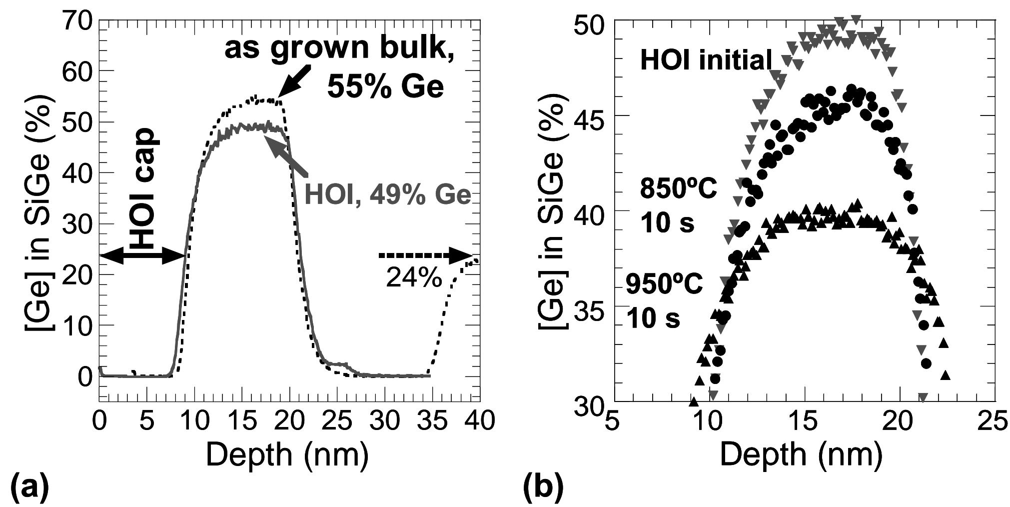

Figure 5.3 SIMS of HOI. **(a)** The as grown bulk wafer and as fabricated HOI substrate. Due to the thermal processing in the bond process, the Ge concentration is lowered by ~5 atomic percent in the HOI substrate. **(b)** After rapid thermal anneal at 850ºC, the final Ge concentration is ~ 46%, thus the 46/25 notation. Higher thermal anneal leads to even larger drops in peak Ge concentration.

detailed process flow presentation). As in the SSDOI experiment, HOI n- and p-MOSFETs were fabricated on separate wafers, using SSDOI and SOI wafers as process and device monitors. Because of the high Ge-content buried $Si_{1-z}Ge_z$ layer, thermal budget is more constrained in HOI than in SSDOI. Phosphorus in-situ doped n+ poly-Si gates were used for both n- and p-MOSFETs on HOI, to allow for lower activation temperatures. The thermal budget associated with the fabrication of the HOI substrates and HOI MOSFETs of this chapter were presented in Table 2.1 (2nd column, labeled "46/25 HOI"). The starting wafers had up to z=0.55 (with y=0.25 or 0.3), which was reduced to ~0.5 after the extended thermal processing of the HOI substrates, as seen in the secondary ion mass spectroscopy (SIMS) profile of Figure 5.3(a). After device processing, including gate oxidation at 650ºC (wet oxidation) and dopant activation at

850ºC (10 s), SIMS analysis indicated that the Ge concentration was even lower, down to z~0.46, despite the lower thermal budget than for SSDOI, thus the 46/25 HOI label of the final devices. In the SIMS result in Figure 5.3(b), it is also demonstrated that annealing at higher temperatures (950ºC for 10s) leads to even further drop in the peak Ge concentration. The mobility of HOI after annealing at temperatures up to 1000ºC will be examined in a later section of this chapter. In addition to the main 46/25 and 46/30 HOI splits, a limited 35/25 HOI split was also prepared (from an as grown Ge concentration of ~40%) to study the effect of varying the buried channel Ge fraction and lowering the compressive strain level simultaneously. In Figure 5.4, cross-section transmission electron micrographs (XTEMs) of two different 46/25 HOI gate stacks are shown. In Figure 5.4(a), the high Ge-content layer is seen as a dark band in between the thick top strained Si and the bottom thinner strained Si layer. In Figure 5.4(b), the HOI structure has an aggressively scaled < 2 nm thin strained Si cap. Below, the extraction of strained Si cap thickness is described. It is essential to know the strained Si cap thickness in order to understand the mobility of the HOI p-MOSFET.

5.3 Basic Device Results

In Figure 5.5(a), the drain current vs. gate bias transfer characteristic is shown for a 46/25 HOI p-MOSFET with a 7 nm thick strained Si cap. As with the SSDOI of the previous chapter, subthreshold slopes were typically below 70 mV/dec. Furthermore, the subthreshold slope in long channel HOI was independent of the strained Si cap thickness, as shown in Figure 5.5(b). This is a benefit of the fully-depleted SOI structure, and is an

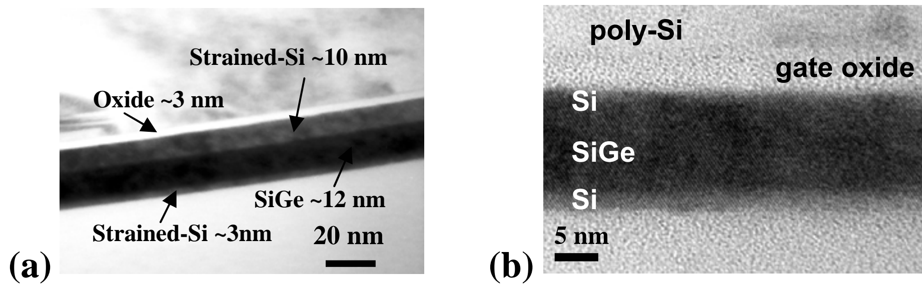

Figure 5.4 XTEM of HOI MOSFETs. (**a**) Low resolution image of 46/25 HOI with a 10 nm thick strained Si cap and a 12 nm thick $Si_{0.54}Ge_{0.46}$ layer on another 3 nm thick strained Si. XTEM courtesy of J. Li. (**b**) High resolution micrograph of a 46/25 HOI with < 2 nm strained Si cap. Such thin caps are required to achieve high mobility enhancements at high inversion charge densities. XTEM courtesy of X. Duan.

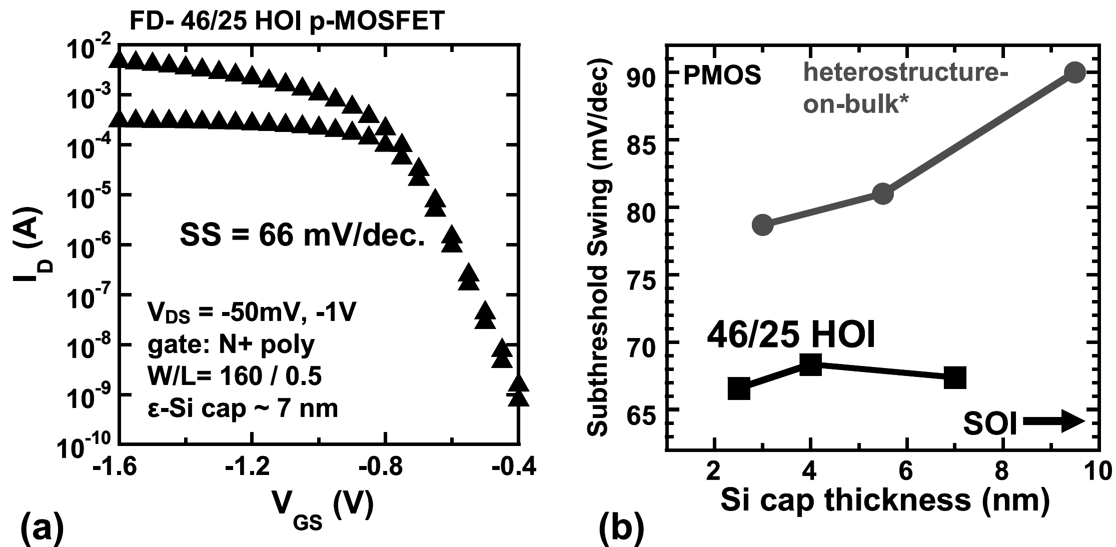

Figure 5.5 (**a**) Drain current vs. gate bias for a long channel HOI p-MOSFET with thick strained Si cap. Excellent sub-threshold slope values were obtained, indicating good interfacial quality. (**b**) The sub-threshold swing vs. Si cap thickness. In the FD-HOI, long channel swing is independent of cap thickness, an improvement from heterostructure-on-bulk MOSFETs. The bulk values, marked * were reproduced from Jung, *et al.* [96].

improvement from heterostructure-on-bulk (dual-channel) p-MOSFETs, which display a degradation in subthreshold slope as the cap thickness is increased [96]. The low subthreshold slope of the HOI MOSFETs also indicates good oxide interface quality.

Extraction of the strained Si cap thickness

The strained Si cap thickness is an important parameter to monitor, as it affects hole transport in a dramatic way. One possible way of extracting the cap thickness is from XTEMs, as in Figure 5.4. However, this method is not only tedious and expensive, but also requires excellent XTEMs to obtain high resolution and good contrast. In this work, XTEMs were only used occasionally on HOI to confirm the extraction of cap thickness from electrical measurements and simulations. Consider the capacitance-voltage (C-V) characteristics of three different 46/25 HOI p-MOSFETs illustrated in Figure 5.6, with strained Si cap thicknesses of 7 nm, 4 nm, and 2 nm. The symbols are measured device results and the lines are fits to the measurements by simulation. The two dimensional simulation was performed in Dessis [97], taking quantum effects into account by the density gradient model with the Dessis default parameters [98]. Except for the difference in cap thickness, the structures are identical. For the HOI with 4 and 7 nm-thick strained Si caps, there is a plateau in the C-V, and the capacitance again increases for larger magnitudes of gate bias. Since the valence band of the buried $Si_{1-z}Ge_z$ layer is lower in energy than the surrounding strained Si layers by ~0.45 eV [37], holes will invert in the buried layer once the device reaches the threshold voltage, as illustrated in the hypothetical "flat band" condition of Figure 5.6(b). The measured capacitance is then

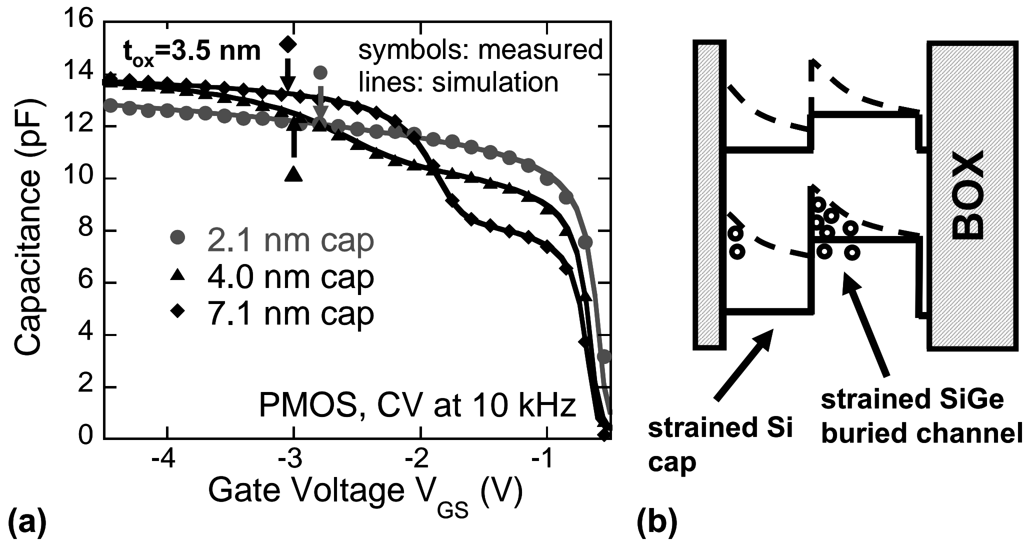

Figure 5.6 Gate-to-channel inversion capacitance for HOI. **(a)** The strained Si cap thickness was extracted by fitting experimental capacitance to simulations [97]. The plateau is due to inversion of the buried channel. For each *C-V*, the arrow indicates the gate bias at which the integrated charge is 1×10^{13} cm^{-2}. Due to the band offset **(b)**, inversion first occurs in the buried layer. As the band bends a second threshold is reached and the surface channel inverts, if the cap is thick enough. Dessis simulation courtesy of Cáit Ní Chléirigh.

effectively the series combination of the capacitance across the gate oxide and the Si cap layer, so that

$$\frac{1}{C} \approx \frac{1}{C_{ox}} + \frac{1}{C_{cap}} = \frac{1}{C_{ox}} + \frac{t_{cap}}{\varepsilon_{Si}}, \qquad \text{(Equation 5.1)}$$

where t_{cap} is the thickness of the strained Si cap layer. This explains why the device with the thickest cap (7 nm) has the smallest capacitance in the plateau region. With increasing gate overdrive, more carriers invert in the buried layer leading to an increased band bending and field, even in the strained Si cap (the field and charge allocation in an HOI p-MOSFET is further examined in Appendix A). Eventually, the situation of the dashed lines in Figure 5.6(b) occurs, and holes populate the strained Si surface channel.

At this second threshold voltage, the capacitance increases again, and approaches the conventional, surface channel value given by the capacitance across the gate oxide, C_{ox}. Due to the strong dependence of capacitance on Si cap thickness, the cap thickness can be accurately extracted from fitting simulated *C-V* to measurements, using the cap thickness as fitting parameter. More information about the extraction technique and band energy values is available in [37]. Note that in Figure 5.6(a), the thinnest cap *C-V* curve does not show this plateau behavior, and stays below the other *C-V* curves even at the highest gate bias (despite the thin Si cap, this is still a buried device). This is an indication that as the cap is thinned to ~ 2 nm, only the buried channel will invert, which will be further examined below as we turn our attention to the transport properties of the HOI MOSFET. From a scalability point of view, the capacitance penalty in Equation 5.1 is undesirable. From this point of view, the strained Si cap should be as thin as possible, or eliminated if gate dielectric issues can be overcome. The scalability of the HOI p-MOSFET will be further examined in Chapter 6.

5.4 Mobility of the HOI MOSFET

In this section, the mobility of HOI n- and p-MOSFET transistors will be examined [87]. Special attention will be paid to the p-MOSFET, and the influence of the strained Si cap, but the influence of the strain level and Ge concentration of the buried channel are also briefly discussed.

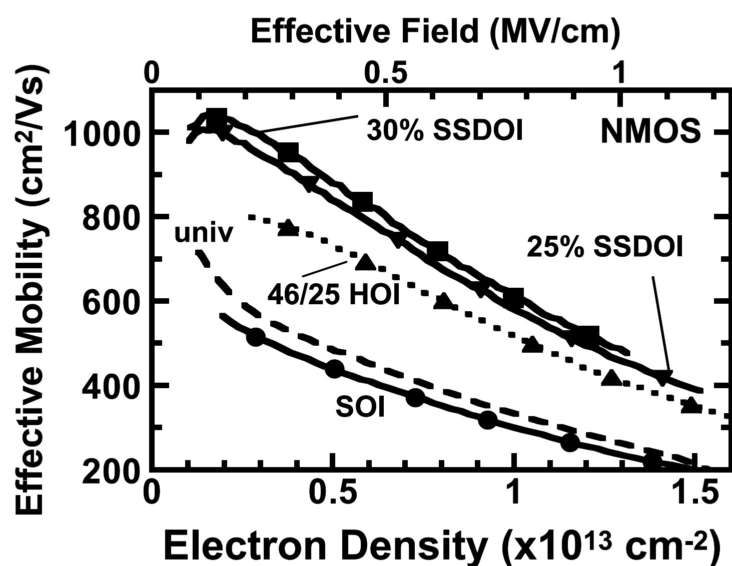

Figure 5.7 Experimental n-MOSFET effective mobility as a function of electron density for 46/25 HOI, 25% and 30% SSDOI and SOI. The externally applied drain bias was 50 mV. The electron mobility of 46/25 HOI is similar to 25% SSDOI, but slightly degraded, possibly due to the limited channel thickness and influence from the underlying SiGe layer. The universal mobility is indicated [15].

The HOI n-MOSFET

In Figure 5.7, effective electron mobility for 46/25 HOI n-MOSFETs is shown as a function of inversion charge density, alongside mobilities for SSDOI and SOI, as well as the universal mobility [15]. The universal mobility is defined as a function of the vertical effective electric field, given by Equation 1.6. From the energy bands shown in figure 5.1, we expect the channel material to be strained Si in both the SSDOI and HOI cases, i.e. the device is a surface channel device. In the HOI case, the electron mobility is slightly degraded at all inversion charge densities compared to SSDOI. This has been observed for all n-MOSFET HOI device lots in this work. One plausible explanation relates to influence from the underlying SiGe layer in the HOI case. The strained Si cap

thickness is estimated to ~ 5 nm in the HOI case, thin enough that some of the transport may be affected by scattering in the SiGe alloy, or at the interface between Si and SiGe. In addition to the thermal budget limitations of HOI, integration difficulties, and more complex structure, it seems that even the transport would favor SSDOI over HOI as the choice of substrate for the n-MOSFET.

The HOI p-MOSFET

Measured HOI p-MOSFET mobilities are shown in Figure 5.8. Note that while the vertical effective field can be defined for SOI and SSDOI according to Equation 1.7, the effective field as a universal parameter has not been established for heterostructure devices (see further discussion in Appendix A). The hole mobility for 46/25 HOI is enhanced by 2X compared to the 46/25 HOI mobility (the strained Si cap thickness is 2 nm for the HOI). Also evident in Figure 5.8 is the difference in the mobility dependence on inversion charge density, for HOI and the 30% and 40% SSDOI. As discussed in the previous chapter, the hole mobility in SSDOI is primarily enhanced at low inversion charge densities, where the band separation causes suppression of the phonon scattering. In the introductory chapters, it was argued that by reversing the sign of the stress from tensile to compressive stress, this shortcoming could be addressed. Indeed, it appears that the hole mobility in HOI is enhanced by a factor that is independent of hole density.

In Figure 5.9, the same HOI hole mobility curve is repeated (46/25 HOI with 2 nm cap thickness), together with a 46/25 HOI with 4 nm cap thickness. While these two curves

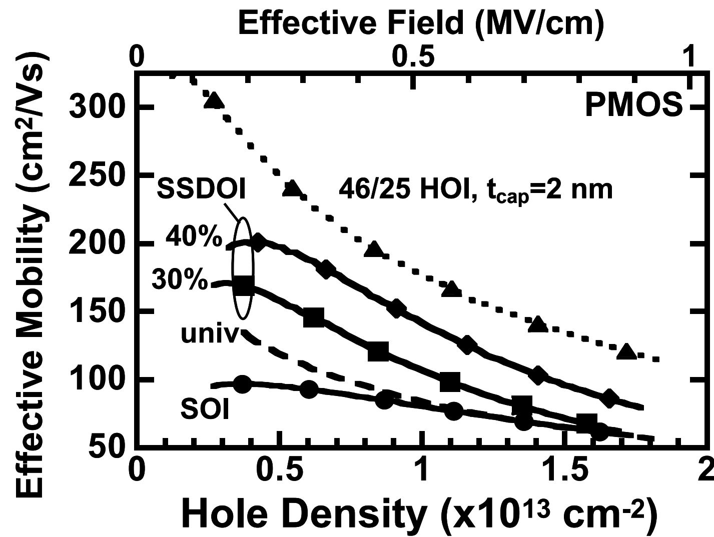

Figure 5.8 Experimental p-MOSFET effective mobility as a function of hole density for 46/25 HOI with 2 nm cap thickness, 30% and 40% SSDOI (from Chapter 4) and SOI. The externally applied drain bias was 50 mV. Due to the buried, compressively strained $Si_{0.54}Ge_{0.46}$ channel, the HOI mobility is superior at all inversion charge densities. The universal mobility is indicated [15].

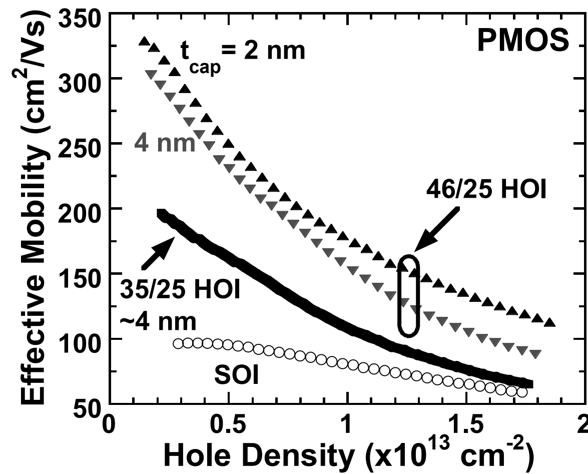

Figure 5.9 Effective hole mobility as a function of hole density of 46/25 HOI (triangles) with 4 and 2 nm cap thickness, and 35/25 HOI (circles) with 4 nm cap thickness. For the same Ge concentration and strain level, the thinner cap device has higher mobility, in particularly at high inversion charge densities. This is due to inversion in the surface channel in the thicker cap device. Keeping the cap thickness fixed at 4 nm, a higher Ge concentration and strain dramatically improves the mobility.

approach each other at low inversion charge densities, the mobility at high inversion charge is higher for the structure with the thin Si cap. A third HOI device, with 4 nm cap but with lower Ge fraction in the buried channel (z=0.35) is also shown. The mobility is much lower than in the higher Ge fraction device of similar cap thickness, which confirms the observations in heterostructure-on-bulk p-MOSFETs [99] that the Ge concentration plays a significant role in the mobility enhancement.

The mobility dependence on cap thickness deserves more attention. In Figure 5.10, the simulated hole distribution at an integrated charge density of N_{inv}=1x10^{13} cm^{-2} is shown as a function of depth. The interface between the strained Si cap and the $Si_{0.54}Ge_{0.46}$ layer has been marked. Note that the three simulated conditions approximately correspond to the device measurements in the *C-V* of Figure 5.6 (where arrows indicate the gate bias for N_{inv}=1x10^{13} cm^{-2}). At N_{inv}=1x10^{13} cm^{-2}, there is already dominant surface inversion in the 7 nm-thick cap device, which would cause significant mobility degradation since the mobility in the strained Si layer is expected to be lower than in the buried $Si_{1-z}Ge_z$ layer. For the device with a less than a 2 nm-thick cap, there is only one inversion charge peak, in the buried channel, confirming our reasoning from inspecting the *C-V* curves. In Figure 5.11, the measured mobility of 46/25 and 46/30 HOI has been displayed as a function of the Si cap layer thickness, at a fixed inversion charge density of 1x10^{13} cm^{-2}. As the cap thickness is reduced, the mobility increases, qualitatively consistent with the understanding of the location of the charge carriers. The 46/30 split has the same buried channel material, but a lower compressive strain level. Thus, a higher compressive strain level yields a higher hole mobility.

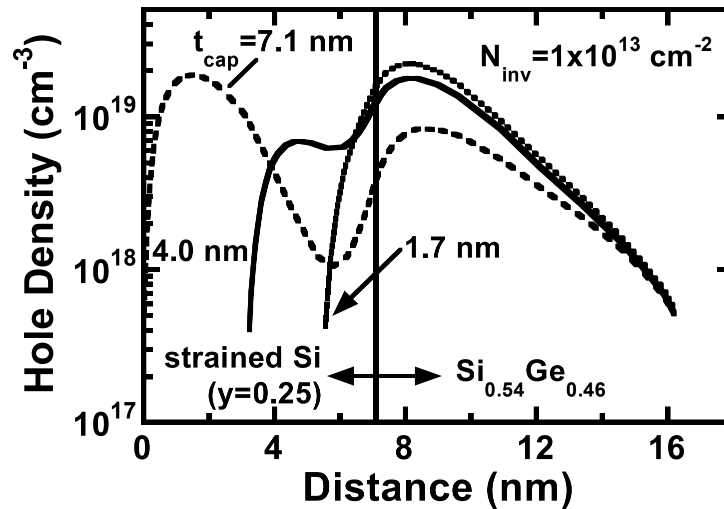

Figure 5.10 Simulation of the hole distribution between the strained Si cap (to the left of the divider line) and the $Si_{0.54}Ge_{0.46}$ layer (to the right) for three different cap thicknesses and at N_{inv}=1x10^{13} cm^{-2}. For the 7.1 nm thick cap, the holes populate mainly the strained Si cap layer. For the thinnest caps, holes primarily populate the buried $Si_{0.54}Ge_{0.46}$ layer. The Dessis simulation used quantum correction by the density gradient model with the Dessis default parameters [97,98]. Simulation courtesy of Cáit Ní Chléirigh.

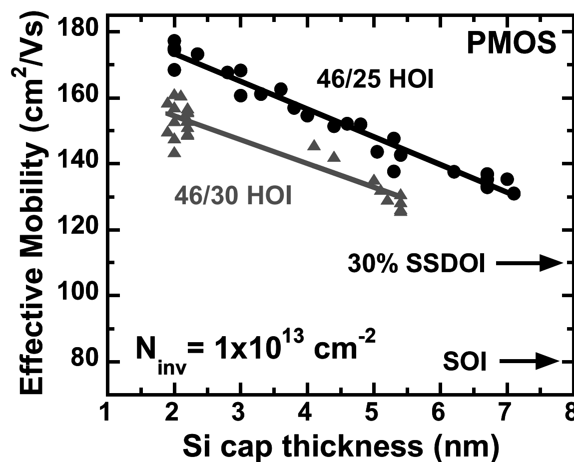

Figure 5.11 Hole mobility as a function of Si cap thickness at N_{inv}=1x10^{13} cm^{-2}. The cap thicknesses were extracted from analysis of *C-V* characteristics, as in Figure 5.6. Mobility increases as the Si cap thickness is reduced. The compressive strain in the buried channel is given by the difference z-y, so that the strain level is higher in the 46/25 HOI than in the 46/30 HOI (but with a constant Ge fraction). The results indicate that a higher compressive strain level improves hole mobility.

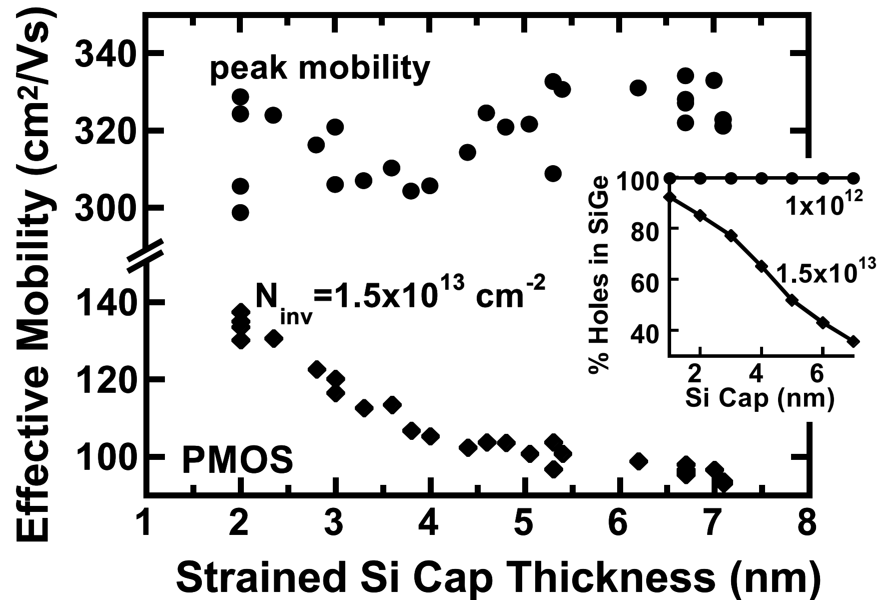

Figure 5.12 Hole mobility vs. Si cap thickness. At low inversion charge density (where the peak mobility is found, approximately at $1x10^{12}$ cm^{-2}) the mobility is independent of Si cap thickness. As verified by the simulation in Dessis (see inset, calculated for two inversion charge densities indicated in units of cm^{-2}), this is because carriers populate only the buried, high mobility $Si_{1-z}Ge_z$ channel. At high inversion charge densities, a larger fraction of the holes populate the surface channel in the thicker cap devices, leading to the observed mobility dependence on cap thickness. For correct interpretation, please note the cut y-axis in the main graph. Dessis simulation courtesy of Cáit Ní Chléirigh (inset).

In Figure 5.12, it is shown that the mobility dependence on Si cap thickness is primarily taking place at high inversion charge densities. The inset serves as a reminder as to the cause: at low inversion charge densities, nearly all of the charge is in the buried channel (regardless of the Si cap thickness) since the bands are relatively flat. At high inversion charge densities, the band bending will cause the strained Si channel to invert, provided that the cap is thick enough. The effect on mobility enhancement factor can be quite significant. In Figure 5.13, the mobility enhancement factor relative to universal mobility is shown for three cap thicknesses. The enhancement factor is >2X for the 46/25 HOI

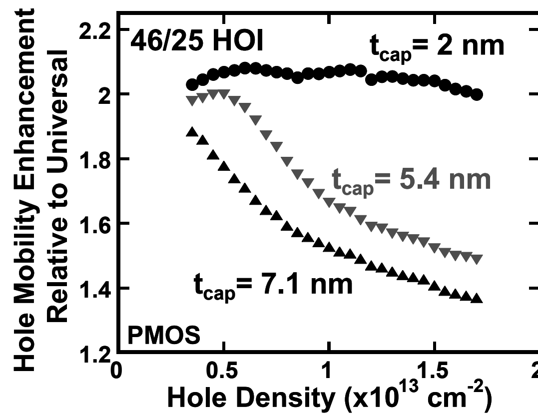

Figure 5.13 The mobility enhancement factor of 46/25 HOI relative to an ideal un-strained FD-SOI mobility, derived from the universal mobility [15]. The 2 nm thick cap HOI has a mobility enhancement factor of > 2X independent of the inversion charge density. This is due to nearly exclusive transport in the buried $Si_{1-z}Ge_z$ compressively strained hole channel.

with 2 nm cap, *regardless of the inversion charge density* – an improvement compared to hole mobility in SSDOI. However, if a thick cap is implemented, the enhancement factor quickly decreases at the higher hole densities since some fraction of the transport is in the lower-mobility surface channel. In summary, the mobility enhancement of the buried SiGe channel is attributed both to the higher hole mobility in SiGe (compared to Si), but also to suppression of phonon scattering from the strain induced band separation. Unlike SSDOI, the enhancement factor can remain high in HOI at high hole densities due to the compressive strain state. Since the quantization mass of the hole ground state (heavy hole band) is larger than for the quantization mass of the first excited state (the light hole band), the band separation is maintained at high inversion charge densities.

5.5 Thermal Processing and Mobility of HOI

In the above presentation of HOI mobility, the thermal budget during rapid thermal annealing to activate dopants was restricted to 850ºC for 10 s. This is because SIMS analysis indicated that for more aggressive thermal anneals, the peak concentration of Ge in the $Si_{1-z}Ge_z$ channel was lowered too much due to the diffusion of Ge atoms, as in Figure 5.3(b). In this section, this thermal budget constraint will be re-examined. In addition to the previous 850ºC (10 s) anneal, wafers were also annealed at 900ºC for 10 s and at 1000ºC for 1 s (spike anneal). The high thermal budget diffuses Ge towards the gate oxide interfaces, leading to a higher density of interface traps. Also, the peak Ge concentration is expected to fall, and the barrier between the Si cap and $Si_{1-z}Ge_z$ channel will become less sharp.

The mobility results are shown in Figure 5.14 [100]. The peak effective mobility (at low inversion charge density) with a thick Si cap is nearly independent of the choice of thermal anneal condition, indicating that the lowering of Ge concentration and barrier sharpness has not yet significantly affected the peak mobility. However, the thinnest cap devices subject to the 1000ºC spike anneal show a much degraded peak mobility performance. Measurements of subthreshold slope show degraded swing (>100 mV/dec.) for these devices, indicating the presence of traps (likely due to up-diffused Ge) at the gate oxide interface. As a reference, the swing for the base-line 850ºC anneal is < 70 mV/dec.

At high inversion charge densities, as in Figure 5.14(b), the mobility as a function of cap thickness is more complicated, due to the inversion of the surface channel for the

thick cap devices. However, measurements indicate that at high inversion charge densities, the mobility is also degraded by the excessive thermal processing. The implication of these results is that the main challenge for HOI with respect to thermal processing may not necessarily be the lowering of Ge concentration in the channel, but the up-diffusion of Ge into the strained Si cap. For transport as well as electrostatic considerations, a very thin cap (1 nm or thinner) is desirable. For such thin caps, control of Ge up-diffusion is expected to be critical for device performance.

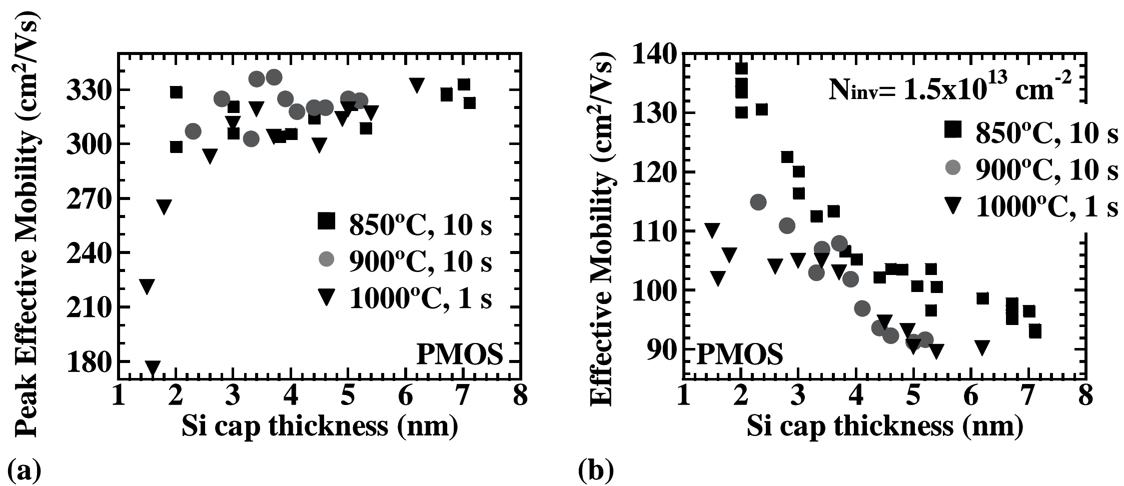

Figure 5.14 Hole mobility in HOI after aggressive thermal annealing. **(a)** The peak mobility remains high for thick cap devices even after processing at 1000ºC. For the thinnest cap devices, the peak mobility is severely degraded (as well as sub-threshold characteristics), likely an effect of up-diffusion of Ge to the gate oxide interface. **(b)** At high inversion charge densities, mobility is degraded for all cap thicknesses after high temperature anneals.

5.6 Chapter Summary

In this chapter, the HOI structure was introduced, and basic device and mobility results were presented for HOI with moderate (12 nm) SiGe channel thickness. The focus was on hole mobility and the significance of the strained Si cap for hole mobility and hole mobility enhancement factor.

A 46/25 HOI p-MOSFET with a 12 nm thick strained $Si_{1-z}Ge_z$ layer (with z=0.46 lattice matched to a relaxed $Si_{1-y}Ge_y$ buffer with y=0.25) and with a strained Si cap thickness of 2 nm was presented. The hole mobility enhancement factor was >2X independent of the inversion charge density, which is different and improved compared to hole mobility in SSDOI. The mobility enhancement is due to a combination of the higher hole mobility observed in strained SiGe compared to Si channels, as well as to the biaxial compressive strain state. In compressively strained SiGe, the quantization mass of the ground state is larger than for the next excited state. Thus, as the structure is confined by the vertical field, the strain induced separation between the first and second bands will not decrease, which is an improvement and different from the tensily strained SSDOI p-MOSFET.

Mobility results from HOI p-MOSFETs subject to high thermal processing indicated that thermal budget and Ge diffusion is not only a challenge to maintain a high Ge concentration in the hole channel, but also to minimize up-diffusion and degradation of interface properties at the strained Si/oxide interface. For highly scaled HOI with extremely thin Si caps, it is predicted that thermal budget must be kept very low – perhaps by the implementation of novel anneal methods such as laser and flash annealing.

Chapter 6

Hole Transport in Ultra-thin Body HOI MOSFETs

In Chapter 4, the hole mobility in strained Si directly on insulator (SSDOI) with ultra-thin strained Si thickness was observed to decrease significantly compared to hole mobility in its thicker SSDOI counterparts. In the previous chapter, the heterostructure-on-insulator (HOI) transistor was introduced and a significant hole mobility enhancement that is independent of inversion charge density was demonstrated. The observation was made in relation to Equation 5.1 that for HOI, the strained Si cap acts as an added capacitor in series with the gate dielectric. For this reason alone, elimination or reduction of the strained Si cap thickness was proposed as one requirement for the realization of scalable HOI substrates (i.e. scalable to short gate lengths). In reality, reducing just the strained Si cap thickness is not enough. Even in unstrained SOI and SSDOI, the thickness of the body is an important parameter to control and optimize in order to suppress short channel effects. In Figure 6.1(a), the simulated subthreshold slope of SOI (open symbols and dashed lines) and HOI (filled symbols and solid lines) is shown for three different body thicknesses as a function of the effective gate length. In this analysis, the total body thickness of the SOI is just the thickness of the Si layer, whereas for HOI it is the sum of the strained Si cap, the SiGe layer, and the strained Si buried oxide interface layer.

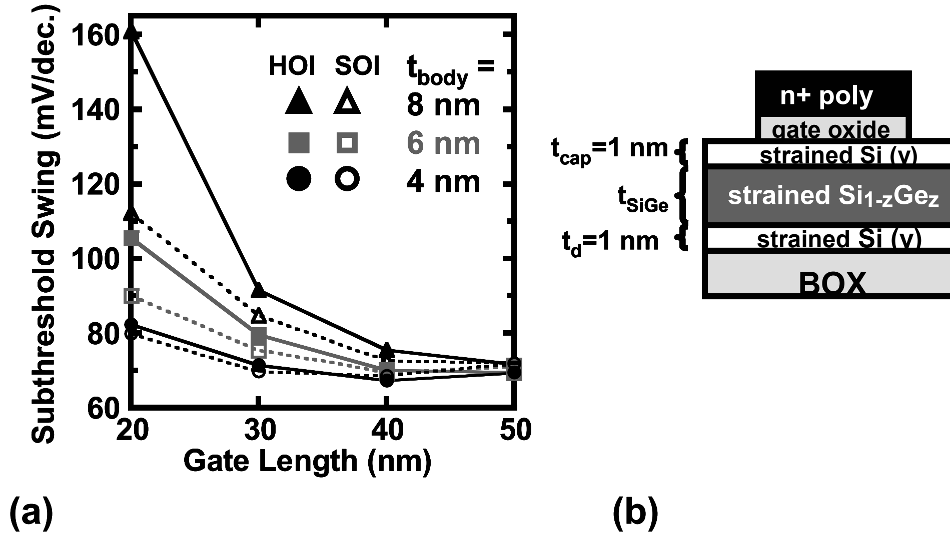

Figure 6.1 Simulated p-MOSFET sub-threshold slope vs. effective channel length, using Dessis [97]. The following parameters were used in the simulation: t_{ox}=1 nm, t_{BOX}=100 nm, body doping (uniform) N_D=10^{17} cm^{-3}, no halos. The source/drain doping profile was graded by 2 nm/decade of doping. For HOI the strained Si layers were 1 nm each, as indicated in the illustration. In order for HOI to scale similar to SOI, the total body thickness must be very thin, motivating the study of hole mobility with thin SiGe-layers. Dessis simulation courtesy of O. M. Nayfeh.

For HOI, the simulated top and bottom strained Si layers were assumed to be 1 nm each, varying only the thickness of the SiGe layer, as illustrated in Figure 6.1(b). Thus, for a given body thickness, the simulated thickness of the SiGe layer is 2 nm thinner than the indicated body thickness. For longer channels, HOI and SOI have similar sub-threshold swing, and the swing is not too sensitive to body thickness variations. At shorter channels, the trend is that both SOI and HOI sub-threshold swings are increasing, and that for thinner bodies the swing is improved. For a channel length of 20 nm, the simulation indicates that a body thickness of 6 nm is required for the HOI to achieve ~100 mV/dec., which means the strained SiGe channel thickness would have to be

limited to just 4 nm. Since the hole mobility in 4 nm-thick 30% SSDOI was much degraded compared to the mobility in thicker layers, the study of HOI with ultra-thin layers is of interest. In particular, it is important to investigate whether the mobility enhancement will remain as the thickness of the buried $Si_{1-z}Ge_z$ hole channel is decreased. Another important question is whether the mechanism for mobility degradation in ultra-thin channel HOI is similar to the mechanisms in SSDOI. Since in HOI, the wavefunction is confined by the barrier at the Si/SiGe interface, as opposed to the Si/oxide interface in the case of SSDOI, it is expected that there may be some differences in the mobility dependence on channel thickness in these two cases.

In this chapter, the hole mobility in HOI with strained $Si_{1-z}Ge_z$ channel thickness of down to 4 nm is presented, and electrostatic quantum simulations are used to answer some of the questions relating to these extreme structures. In this chapter, the off-state leakage of HOI (again, primarily in p-MOSFETs) is also presented. While the mobility enhancements in heterostructure MOSFETs can be quite high, so is often the leakage, since some of the increased leakage is likely coupled to the narrower band gap in high mobility SiGe materials.

6.1 Device Fabrication

Both n- and p-MOSFET 55/25 HOI devices were fabricated. Though the purpose of the mobility experiment was to study the hole mobility dependence on the thickness of the buried strained $Si_{0.45}Ge_{0.55}$ channel, n-MOSFETs were fabricated as mobility controls on

the same wafers as the p-MOSFETs. Both 25% SSDOI and unstrained SOI devices were fabricated for control and mobility comparisons in the same lot.

For this experiment, all relaxed buffers were grown to a final Ge content of y=0.25, so that the in-plane biaxial strain in the 25% SSDOI was the same as the strain of the strained Si cap layer in the 55/25 HOI. The as-grown thicknesses of the buried $Si_{0.45}Ge_{0.55}$ layer were 4, 6, and 10 nm. To avoid peak Ge concentration lowering and layer widening, as in the HOI experiment in Chapter 5, the thermal budget was lowered in the experiment on ultra-thin SiGe channels. Table 3.1 (column "55/25 HOI") summarizes the thermal budget of the 55/25 HOI substrate and device fabrication process. Most significantly, for the low thermal budget process, the densification and post-bond anneals were lowered to 600ºC or below, thermal oxides were grown in a wet ambient at 600ºC (for HOI, SSDOI, and SOI) and the dopant activation process was 800ºC for 10s. All other process steps were identical to the process description for HOI MOSFETs in section 5.2.

With the above thermal budget reductions, the secondary ion mass spectroscopy (SIMS) results in Figure 6.2(a) indicate that the peak Ge concentration is approximately maintained at 55% for the 10 and 6 nm thickness splits, whereas the 4 nm split has a peak Ge concentration corresponding to ~48%. Raman spectroscopy (λ=442 nm) results are shown in Figure 6.2(b). Assuming the SiGe layer is fully strained, the Ge concentrations extracted from Raman agree with SIMS. This is a reasonable assumption since Raman indicates that the strained Si cap layer is fully strained.

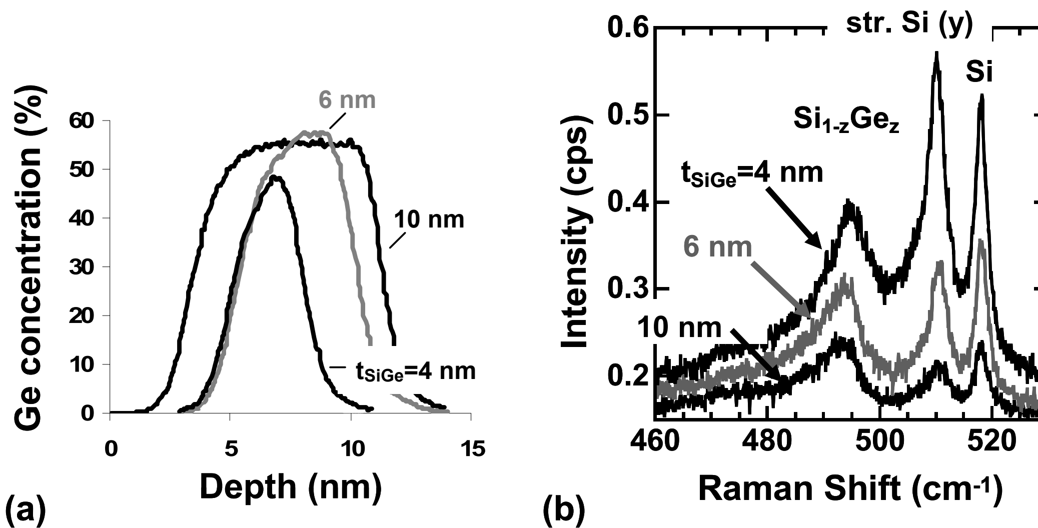

Figure 6.2 (**a**) Low energy (300 eV) SIMS of ultra-thin channel HOI. The 10 and 6 nm thick SiGe channel splits have a peak Ge concentration of ~ 55%, reduced to ~48% in the 4 nm split. (**b**) Raman spectroscopy intensity (laser λ=442 nm) of HOI vs. wave number after MOSFET fabrication. The peaks from left to right represent the buried SiGe channel, the strained Si caps, and the unstrained Si substrate peak from beneath the BOX. SIMS and Raman courtesy of M. Canonico and Freescale Semiconductor, Inc.

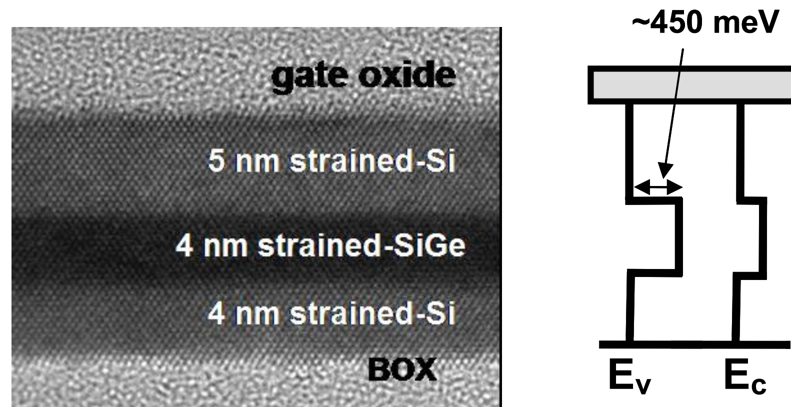

Figure 6.3 XTEM of HOI with SiGe layer thickness of 4 nm and top cap thickness of 5 nm. The body is 13 nm thick. The band structure is sketched at the right. The valence band off-set is roughly 0.45 eV. XTEM courtesy of Accurel Systems.

A cross section transmission electron micrograph of a p-MOSFET device with a 4 nm-thick $Si_{0.45}Ge_{0.55}$ layer, shown in Figure 6.3, confirmed the layer thickness in addition to the SIMS results. For the 10 and 6 nm splits, a range of Si cap thicknesses were obtained. However, for the 4 nm-thick SiGe split, devices with thin (< 5 nm thickness) Si caps were non-functional, due to contact problems. The contact difficulties are likely due to the simplicity of the contact process and non-optimized process flow. Future work is therefore expected to circumvent these difficulties. Due to the contact problems, the mobility comparisons between the three splits are made for devices with a 5 nm-thick Si cap. For this Si cap thickness, low hole densities give the best indication of the mobility of the buried $Si_{0.45}Ge_{0.55}$ layer. At high hole densities, devices with 5 nm-thick strained Si caps will have mixed-channel conduction with both the buried and surface channel inverting.

6.2 Basic Mobility and Device Results

The electron and hole mobilities as a function of inversion charge density are shown in Figure 6.4. The n-MOSFET results are similar to those presented in Chapter 5. The p-MOSFET 55/25 HOI mobility results are for a 10 nm-thick $Si_{0.45}Ge_{0.55}$ buried channel with ~3 nm-thick Si cap. The mobility enhancement factor is slightly higher than in Chapter 5, likely an effect of the increased Ge concentration used in this experiment (55% vs. 46% Ge). The hole mobility of the 25% SSDOI is much lower than for the 55/25 HOI, making it intuitively clear why the HOI device should be designed to avoid hole transport in the Si cap layers. A more in-depth discussion about transport in

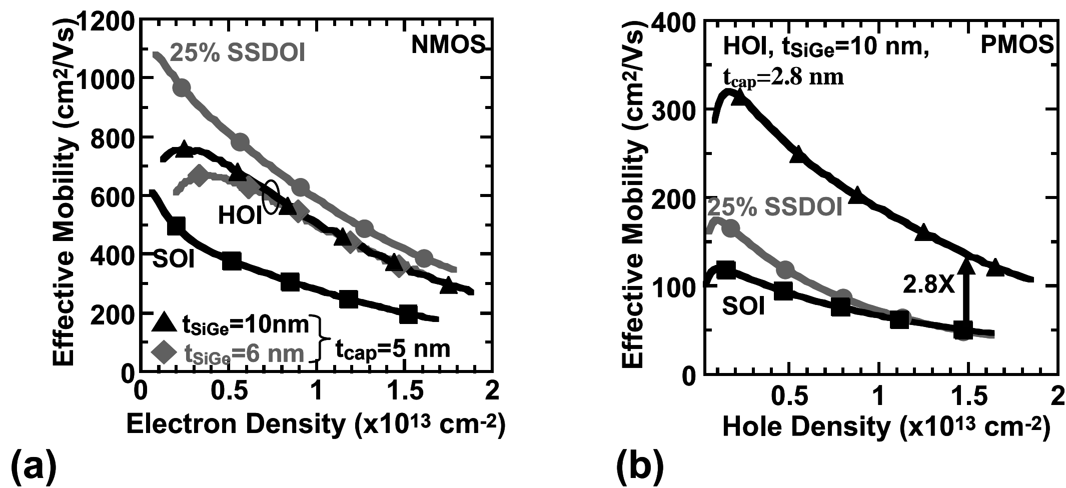

Figure 6.4 (**a**) Electron effective mobility of moderately thin HOI vs. inversion layer density. Results obtained in this experiment are close to those presented in Chapter 5 for the earlier HOI device lot. (**b**) Hole effective mobility of moderately thin HOI vs. inversion layer density. While 25% SSDOI offers no mobility enhancement beyond N_{inv}=1x10^{13} cm^{-2}, HOI with thick $Si_{0.45}Ge_{0.55}$ channel and thin strained Si cap offers enhancement factors in excess of 2.8X for all N_{inv}. The 25% SSDOI control is 26 nm thick.

relatively thick SiGe-channel HOI, the influence of the strained Si cap layer, the strain and Ge concentration is given in Chapter 5.

As before, the strained Si cap thicknesses were extracted from matching simulated gate-to-channel capacitance (*C-V*) to measurements. These simulations were done in Dessis, using the density gradient model as before (see Chapter 5 and [97]). However, to better model the hole density profiles in the thin layers where quantum effects are assumed to be important, simulations were also performed in *nextnano^3*, an effective-mass model coupled Poisson-Schrödinger solver [39]. For the 10 and 6 nm splits the required band off-set to fit experimental *C-Vs* was 0.44 eV, in close agreement with previously published band off-sets for strained Si/SiGe heterostructure capacitors of

similar composition [37]. In the 4 nm split, the off-set was reduced by 65 meV, due to the lower Ge concentration. Effective mass parameters for the different layers were extracted from k.p bulk simulations in *nextnano[3]*, as discussed in section 2.1 and table 2.2. The measured and simulated *C-V* for the 10, 6, and 4 nm thick-channel 55/25 HOI are shown in Figure 6.5. All three devices have a strained Si cap thickness of 5 nm. Note that for simplicity, we use the notation 55/25 HOI for all three splits, despite the slight Ge concentration lowering in the 4 nm split. The agreement between measurements and simulations is good with these band and effective mass parameters.

In Figure 6.5(d), the measured *C-V* from the 10 nm (circles) and 4 nm (squares) splits are shown with 0 V and -60 V applied to the back-gate. The threshold voltage is shifted in the negative direction for the 4 nm-thick device, mainly due to the lower Ge concentration of the channel (and reduced valence band off-set as previously mentioned). There is also an effect of quantum confinement in the SiGe layer, which effectively reduces the valence band off-set at the Si/SiGe interface. The confinement of the carriers is also seen in the qualitative difference between the change in the *C-V* curves for the 10 and 4 nm-thick devices with an applied back-bias. Since the applied bias is negative, the p-MOSFET channel is pulled further away from the top gate in the 10 nm thick buried SiGe channel, lowering the measured top-gate capacitance (similar to Equation 5.1). This shows that in the 10 nm-thick SiGe channel, the carriers are not yet significantly “squeezed” or confined. The situation is different in the device with a 4 nm thick SiGe channel. The applied back-bias does not affect the shape of the *C-V* curve, indicating that

carriers remain at the same distance from the top gate (i.e. they are well confined). The confinement will be explored by simulations of hole density profiles later in this chapter.

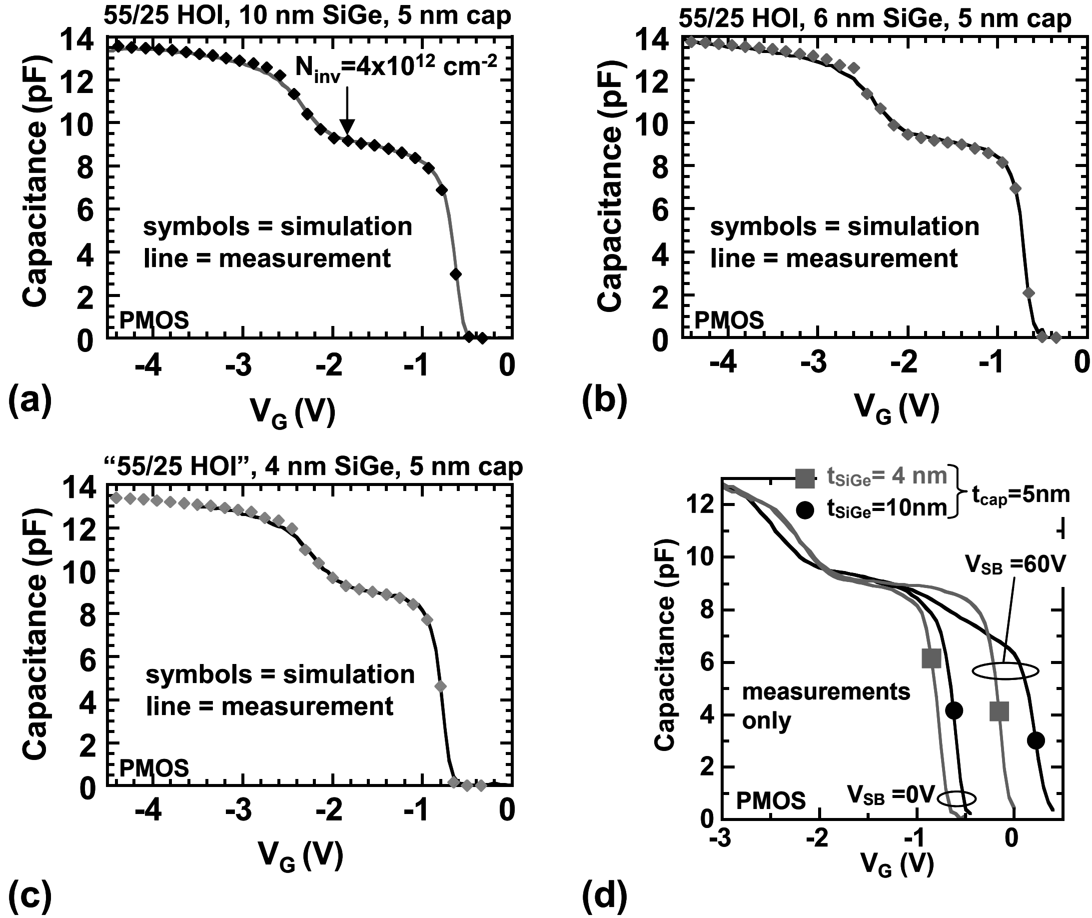

Figure 6.5 **(a)-(c)** Simulated and measured *C-V* for 55/25 HOI with 10, 6, and 4 nm buried SiGe thickness and 5 nm cap thickness. The valence band off-set was reduced by 65 meV in the 4 nm split (c) compared to (a) and (b), due to the reduction of Ge concentration by ~7 atomic percent. The electrostatic simulation was done in *nextnano*[3] [39], using an effective mass model and parameters from section 2.1, and table 2.2. **(d)** Measured *C-V* of 55/25 HOI with 10 and 4 nm SiGe thickness with applied back bias. Confinement of the wave functions in the 4 nm case prevents modulation of the charge centroid location, preventing capacitance reduction.

6.3 Off-state Leakage Current

While the main purpose of this chapter is to describe transport in HOI with ultra-thin SiGe channel layers, other factors also impact the choice of technology. The ability of a structure to suppress short channel effects is one such consideration. In Figure 6.1, the short channel indicator sub-threshold swing was simulated for this purpose. A related topic is the off-state current. Poor off-state current can be the result of large sub-threshold swing, but can also arise from other types of leakage (junction leakage, GIDL, etc). In this section, the off-state current in HOI is presented and compared to the off-state current of SSDOI and SOI. It is found that off-state leakage is one challenge in the higher mobility, SiGe-containing device [101].

Long channel drain current as a function of gate bias is shown in Figure 6.6 for 25% SSDOI and 55/25 HOI. The sub-threshold slopes are again good for both n- and p-MOSFETs on both SSDOI and HOI substrates. The finite Si cap thickness (3-5 nm) and band structure difference between strained Si and $Si_{1-z}Ge_z$ result in threshold voltage shifts between SSDOI and HOI, as further described in [102,103]. One major difference between the SSDOI and HOI is the off-state current level. It appears that in HOI, there is an increase in leakage compared to in SSDOI. In Figure 6.7, the off-state leakage current is shown as a function of drain bias (keeping the gate voltage fixed). Leakage is increased by 2-3 orders of magnitude in HOI relative to SOI. A smaller increase in leakage relative to the SOI devices is observed for 25% SSDOI. At high drain bias, the HOI p-MOSFET leakage current scales with device width and is relatively independent of temperature, as illustrated in Figure 6.8. This is qualitatively consistent with

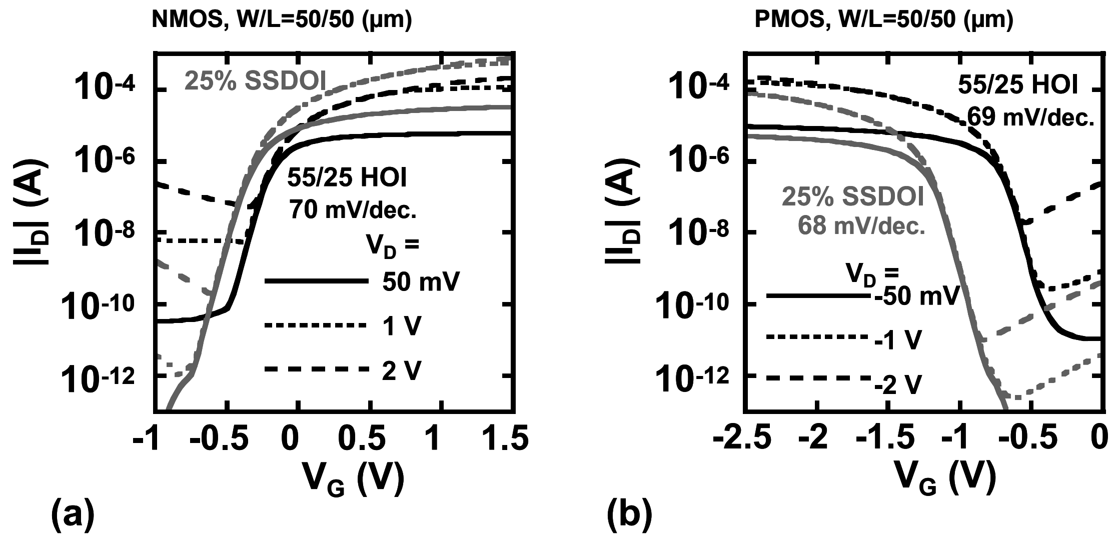

Figure 6.6 I_D vs. V_G characteristics for **(a)** electrons and **(b)** holes in long-channel 25% SSDOI and 55/25 HOI MOSFETs with n+ poly-Si gates. The HOI and SSDOI body thickness is similar, ~20 nm, the HOI $Si_{1-z}Ge_z$ thickness is 10 nm. Sub-threshold slopes are ≤ 70 mV/dec. for both n- and p-MOSFETs. Off-state leakage is higher in HOI than in SSDOI. The finite cap thickness (3-5 nm) and band structure difference between strained Si and $Si_{1-z}Ge_z$ result in threshold voltage shifts between SSDOI and HOI for electrons and holes [102,103].

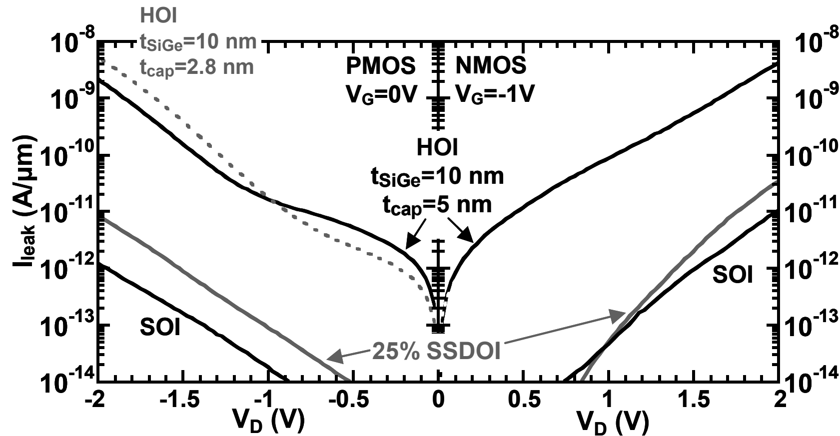

Figure 6.7 Off-state leakage (I_{LEAK}) vs. drain bias (V_D) for n- and p-MOSFETs. Due to the threshold voltage asymmetry between n- and p-MOSFETs, a gate bias of -1V (for n-MOSFETs) and 0V (for p-MOSFETs) was applied to create similar off-state conditions. Leakage is increased by 3 orders of magnitude in HOI relative to SOI.

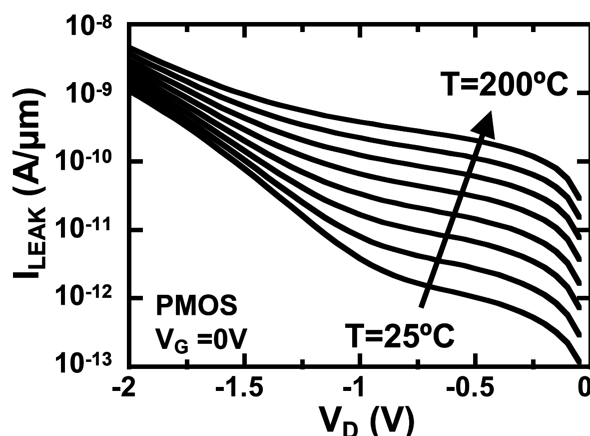

Figure 6.8 Temperature dependence of off-state current (I_{LEAK}) of a 55/25 HOI p-MOSFET with 4 nm-thick $Si_{1-z}Ge_z$ layer and 5 nm-thick strained Si cap. At low $|V_D|$ (e.g. at 0.5V), the relatively weak V_D dependence and strong temperature dependence of I_{LEAK}, and device geometry dependencies are consistent with traps/mesa edge effects. At high $|V_D|$ (e.g. at 2V), the stronger V_D dependence and weaker temperature dependence is consistent with a combination of band-to-band and trap-assisted tunneling in the gate-to-drain overlap region. In this bias range, I_{LEAK} scales with device width.

band-to-band tunneling (BBT), which occurs in the drain near the gate edge. At low drain bias, geometry dependences indicate an edge effect for the HOI devices. From the process flow description and device geometry, this might be due to states at the SiGe/oxide interface where the gate wraps over the mesa edge, which was not protected by a Si liner.

BBT depends on the field in the gate-to-drain overlap region, as well as on the band gap. In the 55/25 HOI (for example with 10 nm channel thickness), simulations to fit experimental *C-V* curves indicate a band gap in the strained Si of 1.0 eV, and 0.7 eV in the buried $Si_{0.45}Ge_{0.55}$ (primarily due to the valence band off-set). Therefore, an increase

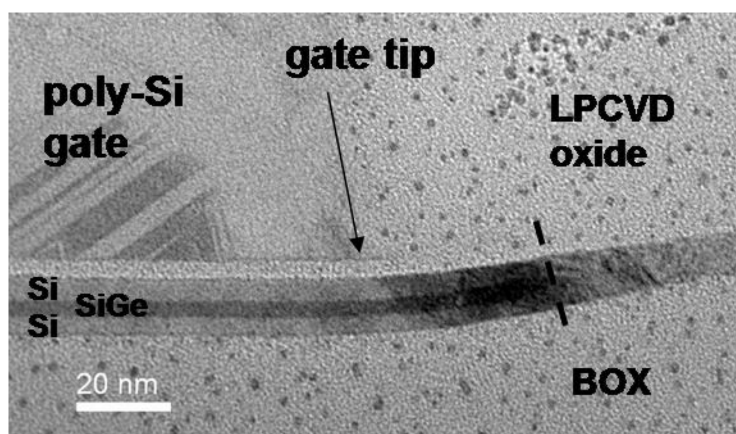

Figure 6.9 XTEM of 55/25 HOI p-MOSFET centered on the gate edge region. The device layers are single crystalline to the left of the dashed line, poly-crystalline to the right, a result of the BF_2 implant in the drain region. The implant ($4x10^{15}$ cm^{-2}, 25 keV) may have caused electronic traps near the gate edge region. Future work to optimize implant screen oxides, spacers, implant and anneal conditions is needed to clarify any technological contributions to off-state leakage. The layer image is bent due to the thin XTEM specimen thickness, and the "dots" in the interlayer and BOX dielectrics are due to sample preparation residues that were not removed prior to imaging. XTEM courtesy of Accurel Systems.

in BBT in SSDOI is expected compared to SOI, and an increase in BBT is expected in HOI compared to both SOI and SSDOI. Future work will be needed to create quantitative models of the expected leakage currents, and compare to measurements. It is possible that technological issues relating to the processing conditions may play an important role. For example, the XTEM of the gate edge region of the drain of a 55/25 HOI transistor (with 4 nm SiGe thickness) in Figure 6.9 indicates that the heavy drain implant caused damage in the drain region. Since the XTEM was prepared after all processing was completed, the as implanted damage and amorphization is not shown. After re-crystallization and poly-Si creation (30-35 nm to the right of the gate tip), it appears that the region immediately below and to the left of the gate tip is single

crystalline. The 30-35 nm space between the gate tip and the poly-Si area could be explained by ion beam reflections and shadowing, but also because the 15-20 nm thick screen oxide acts like a spacer on the gate side-wall. In addition, lateral re-crystallization of some part of the amorphized layer, as in [104], is expected. Further work is needed in order to verify to what extent damage [105] and thermal processing flows may influence the leakage in heterostructure-on-bulk or HOI MOSFETs by creation of traps.

The leakage mechanism in HOI n-MOSFETs appears to depend upon drain bias. At high drain bias ($V_D > 1$ V with $V_G = -1$V), the mechanism is likely similar to that in HOI p-MOSFETs (e.g. BBT related). For lower drain bias, the leakage is independent of gate voltage (see Figure 6.6(a)), and appears to be related to the bandstructure itself though other mechanisms may still contribute. In early heterostructure-on-bulk work, it was observed that the n-MOSFET bands were "pinned" due to accumulating holes in the valence band, preventing effective turn-off of the device, which was supported by simulations [106]. In this respect, the HOI band-structure is similar to its on-bulk cousin.

In Figure 6.10(a), the HOI p-MOSFET off-state leakage current at high and low drain bias is shown as a function of strained Si cap thickness. The leakage at high bias is slightly increased at small cap thicknesses, as might be expected from increasing the field in the smaller band-gap material. For a fixed strained Si cap thickness, in Figure 6.10(b), the thinnest cap device shows somewhat reduced leakage levels. Due to quantum confinement, which increases the effective band gap, it is expected that ultra-thin channel HOI MOSFETs would have reduced BBT. However, electrostatic one-dimensional

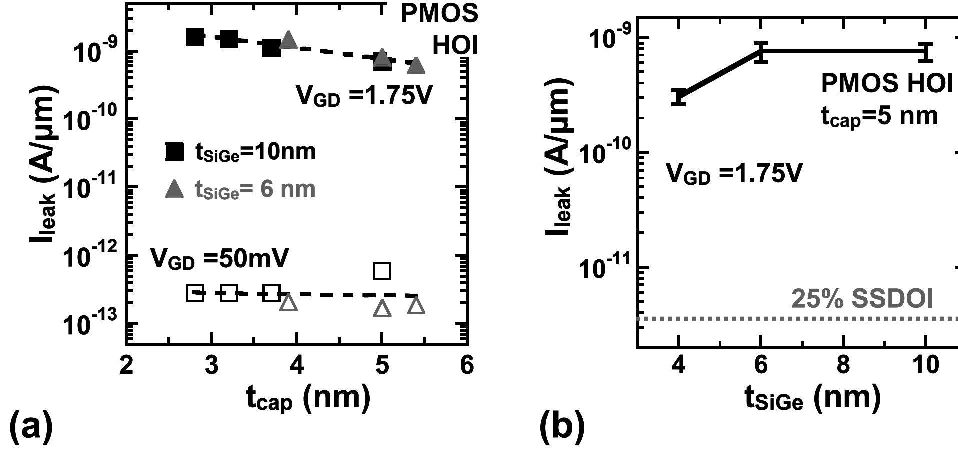

Figure 6.10 (**a**) Off-state leakage current vs. strained Si cap thickness. Leakage is slightly higher for the thinner cap devices. (**b**) Off-state leakage current vs. thickness of the $Si_{1-z}Ge_z$ layer for 55/25 HOI with a strained Si cap thickness of 5 nm. The error bar length is 3σ based on 50 devices for each thickness point. The slight reduction in leakage for the 4 nm-thick $Si_{1-z}Ge_z$ HOI devices is qualitatively consistent with the wider band-gap from a slight decrease in Ge concentration (by 7 atomic percent), with only a minor contribution from quantization.

simulations as the ones used to fit the *C-V* characteristics above, suggest that the overwhelming effect of band-gap increase is due to the lowering of the valence band off-set by 65 meV as a result of the 7 atomic percent reduction of Ge concentration in the HOI sample with 4 nm SiGe channel thickness compared to the thicker samples. Further, the reduction of leakage in the 4 nm-thick SiGe channel HOI is still modest compared to the total increase in leakage over the 25% SSDOI, indicating the need for further study and improvement in this area. Work by Krishnamohan *et al.* [107] suggests that it may be possible to trade-off some of the mobility enhancement for lower leakage in bulk Ge-channel MOSFETs by reducing the channel thickness below 4 nm, thus widening the band gap by quantum confinement.

6.4 Mobility of the Ultra-thin Channel HOI p-MOSFET

The simulated short channel sub-threshold slope characteristics in Figure 6.1 indicate the need to study HOI with body thickness of 6 nm to maintain satisfactory electrostatic control over the channel for effective channel lengths approaching 20 nm. Due to the strained Si cap and oxide barrier layers, the required thickness of the $Si_{1-z}Ge_z$ hole channel is therefore less than 6 nm.

The hole mobilities of 55/25 HOI with SiGe channel thickness of 10, 6, and 4 nm are shown in Figure 6.11(a) [101]. At low hole densities the conduction is concentrated to the buried SiGe channel, despite the 5 nm thick strained Si cap. The low hole density mobility enhancement factor is reduced from 2.8X to approximately 1.5X when the SiGe channel thickness is reduced from 10 to 4 nm, as suggested by Figure 6.12(b). One possible contributor is the lowering of the Ge concentration by 7 atomic percent in the 4 nm thick channel compared to the 6 and 10 nm thick channels. From the results of Chapter 5, and also more complete studies of mobility vs. Ge concentration in bulk devices [99], this contribution to mobility reduction is believed to be a small fraction of the observed mobility reduction. This is also highlighted by the fact that the mobility is already degraded in the 6 nm thick channel compared to the 10 nm thick channel.

Measurements of mobility at low temperatures in the 10 and 6 nm thick SiGe-channel HOI (Figure 6.12) give further clues to the cause of the mobility reduction. Up to carrier densities of $7x10^{12}$ cm^{-2}, low-temperature mobility measurements highlight that transport is primarily in the buried $Si_{0.45}Ge_{0.55}$ layer. Below $7x10^{12}$ cm^{-2}, the scattering at room

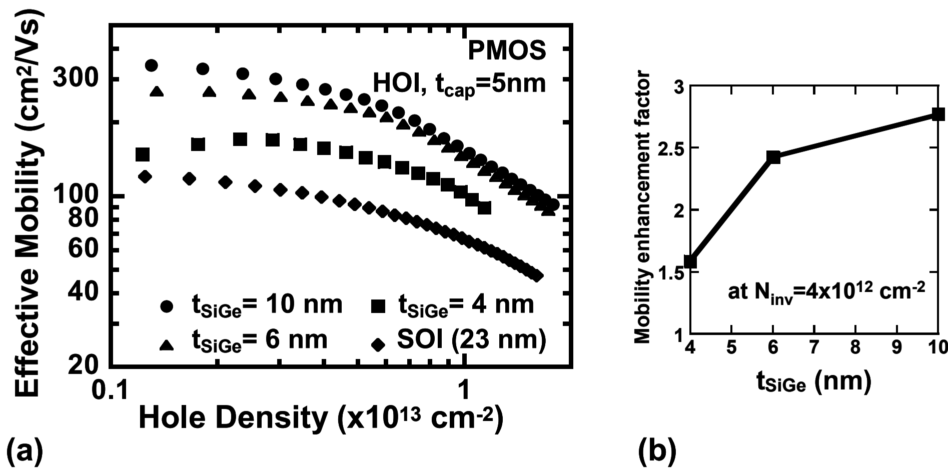

Figure 6.11 (**a**) Measured hole mobilities in 55/25 HOI with ultra-thin $Si_{1-z}Ge_z$ channels. The top strained Si layer thickness is 5 nm and the bottom strained Si layer is 4 nm (kept constant). When the thickness of the buried $Si_{1-z}Ge_z$ layer is reduced, mobility degrades at both low and high hole densities. (**b**) The mobility enhancement factor at a hole density of $4x10^{12}$ cm^{-2} (low vertical field) vs. thickness of the buried buried $Si_{1-z}Ge_z$ layer thickness. The enhancement factor is reduced from 2.8X to 1.5X as the SiGe channel thickness is reduced from 10 to 4 nm.

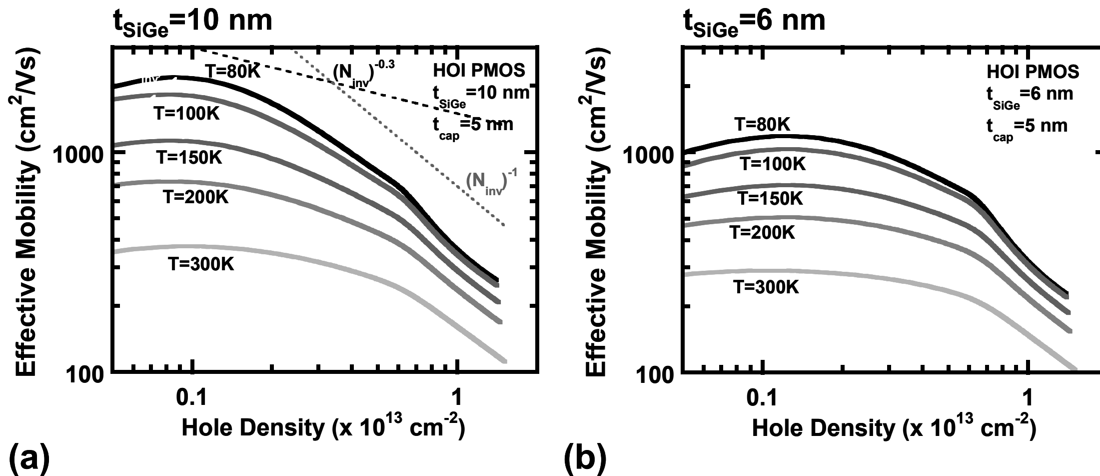

Figure 6.12 Hole mobility vs. inversion charge density for a range of temperatures for 55/25 HOI with (**a**) 10 nm-thick $Si_{1-z}Ge_z$ and (**b**) 6 nm-thick $Si_{1-z}Ge_z$. The temperature dependence is consistent with a large contribution of phonon limited mobility in most of the low hole density range. Scattering from thickness fluctuations is not a dominating scattering mechanism at these channel thicknesses. The typical trend-lines for mobility limited by phonon scattering and surface roughness scattering have been indicated [15].

temperature is heavily influenced by phonons, which are gradually reduced (not eliminated) as the temperature is lowered to 80K. At the lower hole densities, Coulomb scattering appears to contribute, and closer to 7x10^{12} cm^{-2} the scattering mechanisms are mixed between phonons and surface roughness induced scattering. Most important, the temperature dependence indicates that the layer thickness fluctuation induced scattering mechanism is not yet dominant for 6 nm channel thickness. Due to high parasitic resistance, low temperature measurements for the 4 nm thick SiGe channel splits were not possible (due to unreliable capacitance measurements).

Interestingly, it appears that beyond 7x10^{12} cm^{-2} (where the Si cap transport dominates), the mobility is surface roughness limited, an expected effect of the high vertical field in the surface channel as a result of the buried layer charge. The field and hole density allocation between the various channels are detailed in Appendix A.

Phonon scattering in ultra-thin layers is a strong function of the effective channel width as introduced in Equation 2.17, repeated here for convenience [55].

$$W_{fi} = \frac{1}{\left| \int_{-\infty}^{+\infty} \psi_{f'}^{*}(z)\psi_{i}(z)dz \right|^{2}} \qquad \text{(Equation 6.1)}$$

Please refer to section 2.3 for a detailed discussion of the above equation and acoustic phonon scattering. As discussed in section 2.3, the acoustic phonon scattering rate is proportional to the inverse of the effective channel width [55],

$$\frac{1}{\tau_{fi}} = \frac{\pi D_A^2 k_B T_L}{\hbar c_l} \frac{1}{W_{fi}} g_{2Df}(E), \qquad \text{(Equation 6.2)}$$

which is valid in a confined layer, such as an inversion layer or quantum well. For approximately triangular wells in bulk semiconductors, the effective width is largely determined by the quantization mass [42], but is increasingly affected by the confinement from the physical channel thickness and the heterostructure band off-sets for ultra-thin channels.

In Figure 6.13, the simulated inversion charge density as a function of depth in 55/25 HOI (top graph) and 25% SSDOI (bottom graph) is shown for an integrated hole density of $4x10^{12}$ cm^{-2}. The figure was obtained from self-consistent Schrödinger-Poisson simulation of the electrostatics, and was coupled to the measurements by matching experimental *C-V* results shown in Figure 6.5. Despite the much smaller valence band off-set between strained Si and strained $Si_{1-z}Ge_z$ (~0.44eV) for the HOI than between the strained Si and the oxide (~ 5eV), carriers in the 4 nm ultra-thin channel HOI are well confined in the $Si_{1-z}Ge_z$ by the top and bottom strained Si layers with limited "spill-over" into the neighboring cap layers. For this reason the low field mobility reduction in ultra-thin SiGe channel HOI cannot be explained by considering mobility reduction by conduction in the Si capping layers. Instead, it appears most likely that the mobility reduction is due to increased phonon scattering from a decrease in the effective channel width by confinement (Equations 6.1-6.2) as in ultra-thin SSDOI down to 4 nm thickness (though in the SSDOI, confinement is even stronger due to the larger valence band off-set).

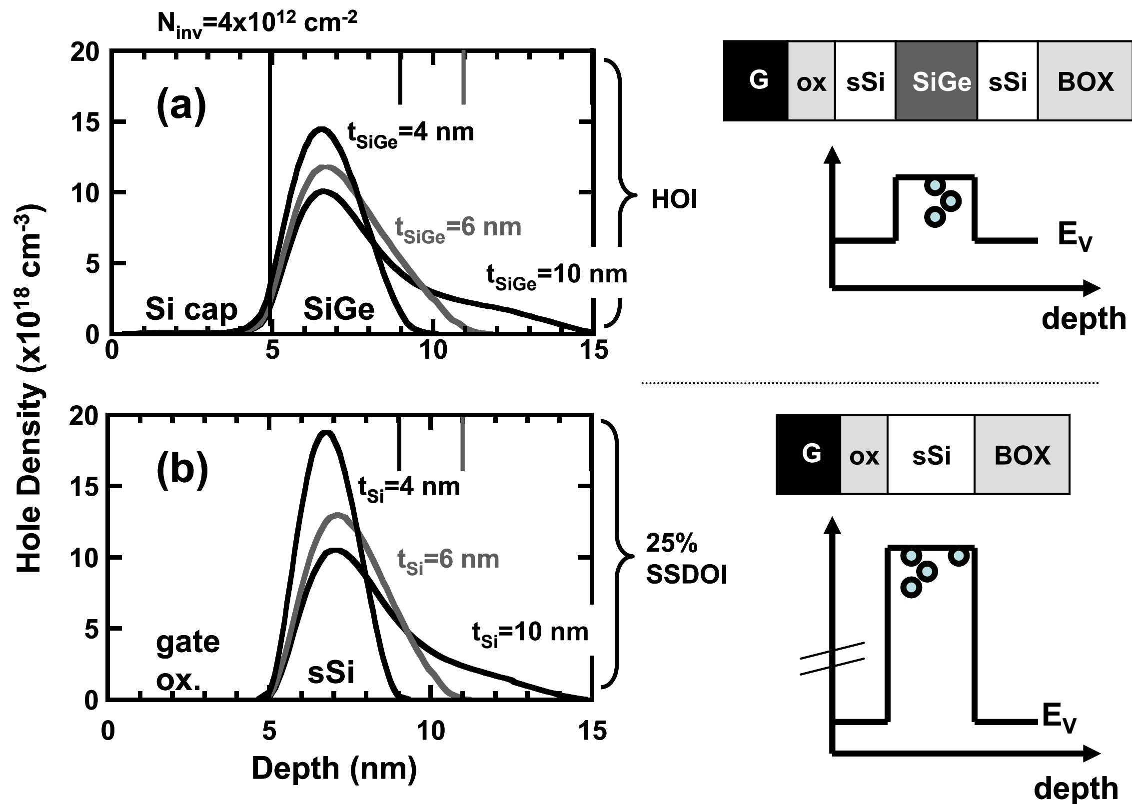

Figure 6.13 Hole density profile vs. depth in 55/25 HOI (top part of the figure, (**a**)) and 25% SSDOI (bottom part, (**b**)). The coupled Schrödinger-Poisson simulation was in *nextnano*^{3} using the mass parameters in Table 2.2, and HOI valence band off-set of 0.44eV for the 10 and 6 nm splits, reduced by 65 meV for the 4 nm split. Due to the large band gap of SiO_2, the valence band "off-set" for the 25% SSDOI is ~5 eV. Despite the much smaller band off-sets in the HOI, carriers are still well confined to the $Si_{1-z}Ge_z$ layer, and get squeezed by both top and bottom interfaces in the 4 nm-thick channel, which could cause an increase in phonon scattering.

The mobility as a function of physical channel thickness (thickness of the $Si_{1-z}Ge_z$ layer for HOI, thickness of the body for SSDOI) is shown in Figure 6.14 for 55/25 HOI and the previously discussed 30% SSDOI. The similar trend in mobility degradation for channel thicknesses above 4 nm further suggests a similar mechanism may be responsible for the mobility degradation. Thus, when comparing the mobility enhancement between HOI and SSDOI of similar channel thickness, the enhancement factor is approximately constant in this thickness range. Note that unless a gate dielectric technology on SiGe is developed, short channel requirements may require the HOI SiGe channel to be at least 1-2 nm thinner than similarly scalable SSDOI technology, somewhat decreasing the mobility advantage of HOI.

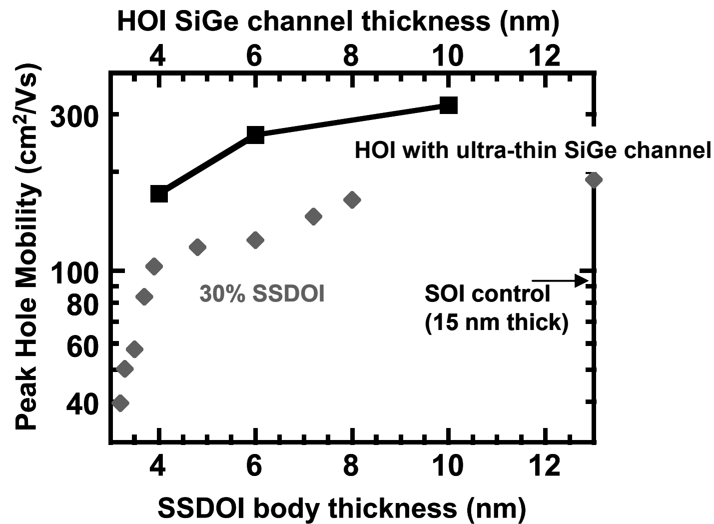

Figure 6.14 The peak hole mobility in 55/25 HOI (from this chapter) and 30% SSDOI (from Chapter 4) vs. the thickness of the channel. For HOI, the channel thickness is the thickness of the $Si_{1-z}Ge_z$ layer. For SSDOI the channel thickness was defined as the body thickness. For similar channel thickness, peak mobility (i.e. low field mobility) trends are similar in HOI and SSDOI down to at least 4 nm thickness.

6.5 Chapter Summary

Transport and leakage for ultra-thin channel heterostructure-on-insulator p-MOSFETs were presented in this chapter. Off-state leakage is increased by 2-3 orders of magnitude in HOI compared to co-processed SOI and SSDOI. While detailed quantitative models need to be developed to understand the separate contributions from fundamental physics and from technological and processing issues, the results are in qualitative agreement with the smaller band gap in strained $Si_{1-z}Ge_z$ than in strained Si. The demonstrated reduction of leakage in HOI with a SiGe channel thickness of 4 nm compared to leakage in thicker-SiGe HOI is modest and may be associated with the lowering of Ge concentration by 7 atomic percent in this sample, which would increase the band gap of the $Si_{1-z}Ge_z$ layer, but could also be coupled in part to band gap widening from quantization.

The hole mobility in 55/25 HOI follows the same trend as in the UTB 30% SSDOI of section 4.4, and for a similar physical channel thickness (not body thickness), the HOI hole mobility maintains its enhancement factor over SSDOI, showing the benefit of the higher mobility compressively strained $Si_{1-z}Ge_z$ channel. At 6 nm thick SiGe layer thickness, the hole mobility is still strongly affected by phonon scattering (not thickness fluctuation induced scattering). Simulations of electrostatics in ultra-thin channel HOI and SSDOI revealed that confinement induced reduction of the channel width may be contributing to the reduction of hole mobility in both ultra-thin HOI and SSDOI by increasing the acoustic phonon scattering rate. In conclusion, due to the similar scattering and mobility reduction processes, strain and materials engineering appears to

be an effective way to enhance mobility even in structures with ultra-thin channel thicknesses, but the enhancement of mobility may come at the cost of increased off-state leakage.

Chapter 7

Summary and Suggestions for Future Work

In this final chapter, the thesis is concluded. The major conclusions relate to the underlying physics of ultra-thin body (UTB) heterostructure-on-insulator (HOI) and UTB strained Si directly on insulator (SSDOI) MOSFETs but they also involve technological implications of the work. Contributions to knowledge are listed in a separate section, and finally, suggestions for future work are listed. The reader is reminded that each chapter was also summarized separately.

7.1 Thesis Summary

The thesis was motivated by the need to improve transport in future CMOS technologies in structures that are able to maintain electrostatic control of the channel better than in conventional bulk Si technology. Mobility was studied in strained Si directly on insulator and strained Si/SiGe/Si heterostructure-on-insulator UTB MOSFETs, primarily with focus on hole transport. In order to maintain good electrostatic control as devices are scaled, simulations (see Chapter 6) indicated that for UTB technology, channel thicknesses of 4-6 nm would be required.

Strained Si Channel Devices

The electron and hole mobility in biaxially tensily strained SSDOI of moderate thickness (> 8-10 nm) follows the same trends as in strained Si on bulk SiGe. In this thickness range, the effect of confinement from the oxide/strained Si/oxide quantum well is very weak, so that carriers are essentially confined by an approximately triangular well (due to the vertical field), as in bulk MOSFETs. For n-MOSFETs, the strain-induced splitting of the degeneracy between the Δ_2 and Δ_4-valleys causes a re-distribution of charge so that a majority of carriers populate the lower energy out-of-plane Δ_2-valleys, where they benefit from a lower in-plane conductivity mass (m_t) than in the Δ_4-valleys. This combined with a reduction of inter-valley phonon scattering causes an electron mobility enhancement of 1.8X-2X compared to unstrained SOI independent of the vertical field. The HOI n-MOSFET is a surface channel device with the electrons inverting in the strained Si cap layer; thus, the electron mobility is expected to be similar to the SSDOI n-MOSFET. However, due to the limited thickness of the cap layer (causing alloy scattering and other Ge-related effects in part of the inversion layer), HOI n-MOSFETs consistently had slightly lower mobilities than their SSDOI counterparts. This is primarily a technological issue.

The hole mobility in moderately thick SSDOI (> 8 nm) is primarily enhanced at low vertical fields, where the LH band is sufficiently separated from the HH band to cause a significant decrease phonon scattering between the sub-bands. As in bulk strained-Si on relaxed SiGe MOSFETs, the mobility enhancement is reduced at high fields due to the

reduced separation between the bands. For sufficiently high strain levels, corresponding to 40% SSDOI, a mobility enhancement of 1.4X was observed even at the highest fields.

In ultra-thin 30% SSDOI, the hole mobility first decreases slowly, and primarily at low fields, as the thickness of the strained Si layer is reduced from 8 nm to 4 nm. This is consistent with an increase in inter-band phonon scattering, similar to that observed at high fields for moderately thin SSDOI. Another possible contribution is from the reduction of the effective width of the channel, which increases the acoustic phonon scattering. Simulations of hole density distributions in SSDOI with 4, 6, and 10 nm channel thickness indicate that the confinement of the wave function in the well becomes significant below 6 nm thickness.

In ultra-thin (< 4 nm-thick) 30% SSDOI, the mobility degrades with a dependence on thickness as $\mu \propto T_{Si}^{6}$, much faster than for thicknesses above 4 nm. Additional evidence from low-temperature measurements suggests that this is due to scattering induced by fluctuations of the strained SOI layer thickness. However, the enhancement of mobility in 3 nm-thick 40% SSDOI relative to 30% SSDOI of equal thickness shows that strain engineering is still possible and effective in such, ultra-thin SSDOI layers.

Strained SiGe Channel Devices

In HOI p-MOSFETs with moderate thickness of the buried biaxially compressively strained $Si_{1-z}Ge_z$ channel (10-12 nm thick, z=0.46-0.55), high hole mobility enhancement of 2-3X independent of inversion charge density can be achieved, provided the strained Si cap thickness is less than 2-3 nm. Band structure considerations suggest that this

mobility enhancment is due to a strained-induced separation of the lowest energy HH band from the LH band, which decreases inter-subband phonon scattering. Opposite from SSDOI, the band separation remains large at high hole densities, which explains the maintained mobility enhancement factor. Additional benefit may come from a reduced effective mass for carriers near the band edge in the HH band, and a very large reduction of effective mass for the portion of carriers in the LH band. As in heterostructure-on-bulk [45,108] higher hole mobility enhancements may be achievable by increasing the Ge concentration and strain level of the buried channel of the HOI device structure.

In the HOI p-MOSFET, the strained Si cap acts as a parasitic surface hole channel if the thickness of the cap is too large. This causes the mobility enhancement for HOI devices with thick caps to degrade significantly at high hole densities, when band bending causes inversion in the surface channel. An additional consequence is that the cap acts as a parasitic capacitor, in series with the gate oxide, making HOI of equal body thickness as SOI more prone to short channel effects. In HOI p-MOSFETs, the increased off-state leakage is consistent with band-to-band tunneling (possibly with trap-assisted contributions), which could in part be due to the lower band gap in the strained SiGe material.

In HOI p-MOSFETs with 10 nm, 6 nm, and 4 nm $Si_{1-z}Ge_z$ channel thickness (5 nm thick cap, z=0.55), the low field mobility enhancement degradation with decreasing thickness is attributed primarily to confinement-induced reduction of the effective channel width. Low temperature measurements for 6 nm and 10 nm-thick channels indicated that phonon scattering is important in this thickness range. The similarity

between the mobility degradation of SSDOI and HOI p-MOSFETs with comparable channel thickness further suggests that similar mobility degradation mechanisms contribute in these two types of structures.

Technological Implications

From the summary above, some technological consequences are already clear. For example, it appears that while SSDOI offers promise for enhancement of electron mobility (slightly better than HOI), it is less suited for hole mobility engineering. Therefore, mixed substrates with SSDOI for n-MOSFETs and HOI for p-MOSFETs seem promising. The integration aspects and fabrication sequence of such a substrate was recently described by Ref. [109]. A "pure" HOI substrate is less appealing not only because of the slight lowering of mobility in the n-MOSFET (which could probably be overcome by increasing the cap thickness), but more important because of the scalability disadvantage of the thicker-body HOI n-MOSFET compared to the SSDOI n-MOSFET.

One advantage of the SSDOI p-MOSFET over strained Si on relaxed SiGe technologies is that once the strained layer has been transferred to insulator, the un-patterned layer is relatively immune to strain relaxation so that thicker strained Si layers can be achieved with less off-state leakage than if those layers were produced on bulk [88]. The absence of Ge from the wafer also greatly simplifies process integration issues.

The HOI experiments suggest that diffusion of Ge during thermal processing steps can be harmful to carrier transport, which is highlighted in HOI with extremely thin caps and thin SiGe channels. Therefore, dielectric deposition and dopant activation processes need

to be implemented with very low thermal budgets. An additional challenge is the leakage in HOI. Though an increase in leakage is expected from the smaller band gap, process induced leakage from traps or implant damage may have contributed. The technological conclusion is that while HOI offers a path to much improved transport, the integration challenges ahead require further research.

For both HOI and SSDOI, there is a fundamental trade-off between the thickness of the channel and mobility, as summarized above. From a design point of view, this becomes very critical especially after the on-set of thickness fluctuation induced scattering, which degrades mobility rapidly (in this thesis, this mechanism was confirmed only in the ultra-thin SSDOI p-MOSFET with thickness < 4 nm). Due to the technological challenges with producing ultra-thin substrates with atomic layer thickness precision, it is undesirable to rely on a device technology (the low-doped UTB-SOI MOSFET) which will ultimately require thicknesses below 5 nm. The results of this work indicate that related multiple gate-structures, such as planar double gate, or FinFETs, or other surround-gate technologies, in which the thickness requirement is somewhat relaxed, should be an interesting field for further study.

7.2 Contributions

The contributions of this work have been divided into three main sections: (1) New heterostructure materials development, (2) Research on SSDOI MOSFETs, and (3) Research on HOI MOSFETs.

New heterostructure materials development:

1. Developed techniques for fabricating SSDOI and HOI 150 mm substrates at MIT by a bond- and etch back technique.
2. Developed clean reduced-thermal-budget oxide-to-oxide bonding process for HOI substrate with high Ge content.
3. Characterized etching of SiGe and strained Si in SC-1 to allow for fabrication of SSDOI of customized thickness and HOI with a pre-determined Si cap thickness.
4. Developed a technique for local thin-back of gate regions on SSDOI MOSFETs by wet etching to allow fabrication of multiple SSDOI thicknesses per wafer with constant source and drain thickness (to minimize series resistance).

Research on SSDOI MOSFETs:

1. Demonstrated some of the first SSDOI MOSFETs, including the first SSDOI MOSFETs in sub-10 nm strained Si layer (down to 1.4 nm thickness).
2. Discovered that despite the strong influence of thickness-fluctuation-induced scattering for sub-4 nm thick films, biaxial strain engineering can benefit hole mobility for high strain levels.
3. Showed that 40% hole mobility enhancements in 14 nm thick 40% SSDOI can be achieved (as grown thickness 26 nm) with maintained low leakage despite the super-critical thickness film.

4. Discovered experimentally that hole mobility in sub-4 nm 30% SSDOI p-MOSFETs is greatly reduced by thickness fluctuation induced scattering (as in unstrained SOI of similar thickness).

Research on HOI MOSFETs:

1. Demonstrated the first heterostructure-on-insulator MOSFETs suitable for ultra-thin body MOSFETs, utilizing strained Si and strained SiGe layers.
2. Demonstrated that simultaneous and high electron and hole mobility enhancements can be achieved in HOI substrates and that both electron and hole mobility enhancement is independent of inversion charge density with proper design of the Si cap thickness.
3. Extended previous understanding of average field in heterostructure-on-bulk to heterostructure-on-insulator, and presented an analytic formula and procedure to accurately describe the field in the respective layers from inspection of inversion capacitance data.
4. Showed that a parallel channel description of the HOI can give a qualitative understanding of mobility in HOI with >10 nm thick SiGe layers.
5. Demonstrated first heterostructure-on-insulator with SiGe channel thickness down to 4 nm.
6. Showed that peak mobility is reduced in HOI with channel thickness reduced below 10 nm.

7. Discovered experimentally that phonon-scattering is similar in 55/25 HOI with 6 nm and 10 nm $Si_{0.45}Ge_{0.55}$ channel thickness.
8. Demonstrated that off-state leakage in HOI is higher than in comparable SOI and SSDOI.

7.3 Suggestions for Future Work

As already hinted at in the thesis summary (section 7.1), this work has addressed many questions regarding fundamental physics of ultra-thin body strained Si and Si/SiGe/Si heterostructure-on-insulator MOSFETs, and some technological implications are also clear. However, as questions have been answered, new questions have been raised. In this section, suggestions for future work are given based on the results of this thesis.

Structures, Substrates and Patterning

1. Explore multi-gate strained Si or Si/SiGe heterostructure MOSFETs from a transport and scalability point of view. For example, is the implication of strained Si cap similar in tri-gate structures where the inversion charge is naturally more centered in the structure?
2. Another "technology booster" is the high-*k* dielectric. It is common to introduce an interface layer between the high-*k* and channel to avoid mobility degradation. This is similar to the cap layer in HOI. Perhaps interfacial layers for high-k are not necessary for HOI, reducing somewhat the scalability penalty for HOI that was indicated in this thesis. An initial experiment could be the study of gate

oxide tunneling leakage in capacitors on HOI (or bulk heterostructure-on-insulator) with thin caps. Can the thickness of the oxide be reduced compared to SOI with respect to tunneling? How much?

3. Creating free surfaces in strained layers can result in strain relaxation, as in Ref. [82]. More work is suggested in the area of strain relaxation or strain engineering due to small geometry patterning, particularly for HOI structures.
4. Technological and integration schemes for cost effective implementation of both SSDOI and HOI on a common substrate is an area for future work.
5. Investigate further the mechanism behind the leakage in HOI (and heterostructure-on-bulk) MOSFETs. Is increased leakage a fundamental or technological issue, or both?
6. Further modeling of band structure and transport in ultra-thin body and ultra-thin channel HOI and SSDOI n- and p-MOSFETs in various strain configurations to achieve quantitative understanding of the optimal stress, directional and material configurations.

Electron Transport

1. Study the electron mobility as a function of strained Si thickness in SSDOI (with a range of strain e.g. 20%, 30%, 40% SSDOI) in the range 2 nm to 10 nm, and compare to unstrained SOI.
2. What is beyond SSDOI for the n-MOSFET? As with holes, new materials might be necessary to bring the n-MOSFET much beyond the transport offered by

SSDOI. Substrates combining III-V materials and Ge will offer new possibilities for both electron and hole mobility improvements, perhaps in particular combined with process-induced strain.

Hole Transport

1. Study short channel HOI (varying the biaxial stress component, possibly even with relaxed SiGe, e.g. 50/50 HOI) p-MOSFETs with state-of-the-art raised S/D and contact techniques and with and without the addition of process induced stress technology (e.g. stress liner) to study the effect of high levels of uniaxial stress superimposed upon the biaxial component.
2. Investigation of the impact of mechanical stress, induced by bending, on hole mobility in SiGe channel devices is of interest, and may give some initial insights into the potential of combining process-induced stress technology with SiGe channel materials.
3. Study HOI and/or heterostructure-on-bulk with thin SiGe and cap layers and very sharp and smooth strained Si/SiGe interfaces to eliminate technological contributions to mobility reduction observed in this work.
4. Study the effects of S/D doping and pocket implants on mobility in short channel heterostructure devices, develop and compare with alternative source/drain formation techniques.

Appendix A

Average Vertical Field in HOI and Influence of Series Resistance on Field Effect Mobility in UTB-MOSFETs

In the following sections, a few side-topics will be covered in more detail than the individual chapters allowed. In the interest of space, familiarity with the earlier chapters and the terminology of this thesis is assumed. As previously mentioned the universality of mobility relative to an effective field has not yet been established for HOI. However, understanding of the average field and charge allocation may help us to obtain a better qualitative, if not quantitative, understanding of transport in dual- or multi-channel MOSFETs. First, Gauss' law is used to develop a general formula for the average field in an HOI device with j layers; the formula is compared to simulations. Second, more intuition regarding the allocation of charge to the buried and surface channels is developed, using a simple approximate model from analysis of the *C-V*.

In the final section of this appendix, the effect of series resistance on mobility will be analyzed in more detail than in earlier chapters. In particular, the effect of series resistance on the field effect mobility is treated.

A.1 Average Vertical Field in HOI

For a bulk-Si device, by Gauss' law, the field at some distance x from the gate oxide/Si surface is

$$E(x) = \frac{Q_b}{\varepsilon} + \frac{1}{\varepsilon}\int_x^{x_i} qD(x')dx' , \qquad \text{(Equation A.1)}$$

where Q_b is the bulk charge, and D is the inversion charge density. The effective field was first defined as the average field in the channel [110]:

$$E_{eff} = \int_A^B D(x')E(x')dx \bigg/ \int_A^B D(x')dx , \qquad \text{(Equation A.2)}$$

(where the points A and B are determined so that the D is essentially 0 there) which can also be deduced from Gauss' law as the average between the field at the top and bottom of the inversion layer, so that

$$E_{eff} = \frac{1}{\varepsilon}(Q_b + \eta Q_{inv}) = \frac{1}{\varepsilon}\left(Q_b + \frac{1}{2}Q_{inv}\right). \qquad \text{(Equation A.3)}$$

Experiments have shown that for electrons, this definition leads to universality of mobility vs. the vertical effective field [15], but for holes, η=1/3 is needed to satisfy the universality condition. For this reason, the effective field is typically interpreted as the field from Equation A.3 with η chosen to satisfy universality rather than being the average field.

For heterostructure-on-insulator (HOI), the universality of hole mobility with respect to some field has not yet been established. While attempts to use the average mobility to describe transport in heterostructure-on-bulk have had limited success [111], a basic

understanding of the vertical average electric field in various layers of HOI is useful. First, mobility models based on transport in bulk-Si devices may not adequately describe mobility in for example HOI capping layers, where screening from carriers in the buried SiGe layer will be a strong function of cap thickness, as well as the field at the onset of inversion. Second, a better understanding of the average field may help explain qualitative transport behavior, such as the behavior of mobility as a function of inversion charge density shown in Figure 6.12, and may help with more intuitive understanding of how to link *C-V* profiles with the distribution of charge between the buried SiGe and Si cap layers, as discussed in Section A.2 below. As in Ref. [111], Equation A.2 will be used to calculate the average field in various layers from simulations in *nextnano³* (see Chapter 6). Just as in the bulk-Si device, Gauss' law can also be used directly to find the average field in the top Si cap layer, buried $Si_{1-z}Ge_z$ layer, and the bottom strained Si layer:

$$E_{ave_cap} = \int_{cap} D(x')E(x')dx \Big/ \int_{cap} D(x')dx = \frac{1}{\varepsilon_{Si}}\left(Q_{SiGe} + Q_d + \frac{1}{2}Q_{inv_cap}\right) \quad \text{(a)}$$

$$E_{ave_SiGe} = \int_{SiGe} D(x')E(x')dx \Big/ \int_{SiGe} D(x')dx = \frac{1}{\varepsilon_{SiGe}}\left(Q_d + \frac{1}{2}Q_{inv_SiGe}\right) \quad \text{(b)} \quad \text{(Equation A.4)}$$

$$E_{ave_d} = \int_{d} D(x')E(x')dx \Big/ \int_{d} D(x')dx = \frac{1}{\varepsilon_{Si}}\left(\frac{1}{2}Q_{inv_d}\right) \quad \text{(c)}$$

where the sub-script *d* is used for the bottom Si layer. It was assumed that the doping level is low enough that the depletion charge in the thin layers can be excluded, as in Equation 1.8, and that the field is negligible at the BOX interface, which is typically true for V_{BS}=0 and thick buried oxides. Note that the inversion charge of layers "below" the

one under consideration (e.g. Q_{SiGe} and Q_d in Equation A.4(a)) is treated just as the depletion charge in a bulk-Si transistor, though it is not constant with bias. For this reason, though all the charges in Equation A.4 are integrated inversion charges, only the inversion layer charge of the layer under consideration was explicitly marked with the sub-script *inv*. The combined average field is a weighted average of the field of individual layers, as in Equation A.2

$$E_{ave} = \int_{HOI} D(x')E(x')dx \Big/ \int_{HOI} D(x')dx = \frac{\left(E_{ave_cap} \cdot Q_{inv_cap} + E_{ave_SiGe} \cdot Q_{inv_SiGe} + E_{ave_cap} \cdot Q_{inv_d}\right)}{\sum Q_{inv}}$$

(Equation A.5)

A more general heterostructure device with *j* layers can be treated similarly to yield the overall average field and average field for the nth layer as

$$E_{ave} = \int_{HOI} D(x')E(x')dx \Big/ \int_{HOI} D(x')dx = \frac{\sum_{n=1\ldots j} E_{ave_n} \cdot Q_{inv_n}}{\sum_{n=1\ldots j} Q_{inv_n}} = \frac{\sum_{n=1\ldots j} \frac{1}{\varepsilon_n}\left(\frac{Q_{inv_n}}{2} + \sum_{m=1\ldots n-1} Q_{inv_m}\right) \cdot Q_{inv_n}}{\sum_{n=1\ldots j} Q_{inv_n}}$$

(Equation A.6)

$$E_{ave_n} = \frac{1}{\varepsilon_n}\left(\frac{Q_{inv_n}}{2} + \sum_{m=1\ldots n-1} Q_{inv_m}\right), \qquad \text{(Equation A.7)}$$

where the layers were numbered in such a way so that the layer closest to the BOX is layer number 1 and the layer closest to the gate oxide is layer number *j*.

The problem of calculating the average field in a particular layer of an HOI structure, or the overall average field is now reduced to finding the inversion layer charges for the respective layer. Since Q_{inv} is obtained from Equation 2.20, it is natural to break down

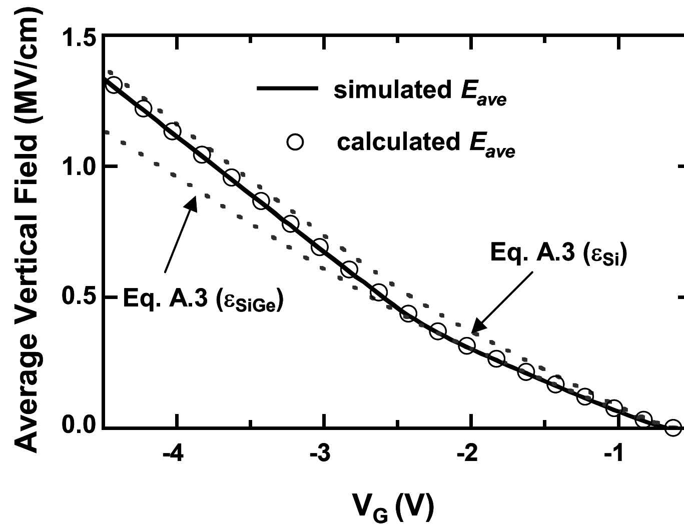

Figure A.1 Average vertical field in a 55/25 HOI p-MOSFET with 5 nm-thick strained Si cap and 10 nm-thick buried $Si_{0.45}Ge_{0.55}$ layer, showing agreement between simulated (*nextnano³*) and calculated field values.

the inversion layer charge into different layers by closer analysis of the *C-V* data. In the next section, this will be done by an approximate method, which allows for quick evaluation of the fields in an HOI MOSFET. First, to test the validity of Equation A.5, the inversion charge densities were extracted by fitting simulated *C-V* to experimental measurements (see Figure 6.5(a)), then integrating the charge density profiles in the respective layer. In Figure A.1, the average field integrated over the full HOI structure is shown as a function of the gate bias. The simulated curve (solid line) was obtained by integrating the local field calculated by the simulator, multiplied with the local charge density as in the left side of Equation A.5. The agreement is good between simulated average field and the field calculated from combining the right side of Equation A.5 with Equation A.4 (symbols), which shows that the simplifying assumptions of small field at the BOX and ignoring the depletion charge were good approximations. For comparison,

the average field from Equation A.3 is shown (using the total Q_{inv}, and η=1/2) with ε for Si or $Si_{0.45}Ge_{0.55}$. As expected, the correct average field from Equation A.5 is determined by charge inversion in the buried SiGe layer for low gate bias while the Si cap field dominates for higher gate bias conditions.

A.2 Charge Allocation in HOI

In order to justify the use of Equation A.5, an approximate way of extracting the allocation of charge between the channels in HOI directly from the *C-V* is desired. If simulations are needed to determine the charge in each layer, it would be just as easy to calculate the average field directly from the integral in Equation A.5. In addition, further understanding of the charge allocation in an HOI transistor will make for more intuitive interpretation of experimental results. Consider the experimental gate-to-channel *C-V* for a 55/25 HOI p-MOSFET with 5 nm strained Si cap, and 10 nm buried layer in Figure A.2 (the capacitance is normalized so that the maximum point is 100% on the y-axis). The simulated fit to this experimental *C-V* was shown in Figure 6.5(a). Also shown in Figure A.2 is the simulated fraction of newly inverted holes in the HOI structure that are generated in the strained Si cap layer, $\Delta Q_{cap}/\Delta Q_{inv}$. At V_G=-2.43V, 50% of newly generated holes are allocated to the cap layer, and for higher gate bias the fraction rapidly increases. From now on, this particular bias condition (i.e. when 50% of new holes are allocated into the cap channel) will be referred to as V_{mid}. On the *C-V*, V_{mid} corresponds

to roughly the point where the slope of the "hump" is largest. The steep slope of the simulated curve in Figure A.2 suggests that it is reasonable to approximate that below V_{mid}, nearly all generated carriers invert in the buried channel, and beyond V_{mid}, nearly all generated carriers invert in the cap. Figure A.3 shows the simulated fraction of holes in the buried layer as a function of the inversion charge density (superimposed on the experimental *C-V*), with the approximation above indicated. There is reasonable agreement away from the switching point V_{mid}. The effect of picking the mid-point

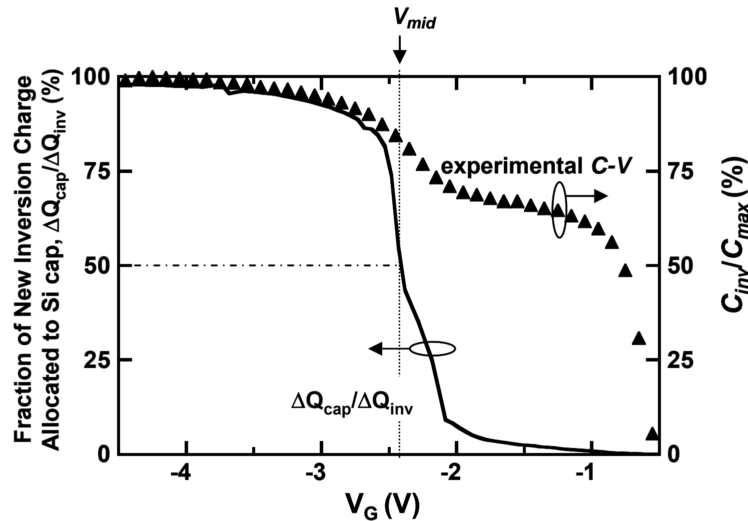

Figure A.2 Experimental, normalized *C-V* for a 55/25 HOI p-MOSFET with 5 nm-thick strained Si cap and 10 nm-thick buried $Si_{0.45}Ge_{0.55}$ layer (right axis), and the simulated (*nextnano*^{3}) fraction of newly generated inversion charge that appears in the strained Si cap (left axis). For the indicated voltage (V_{mid}), half of the newly generated carriers invert in the cap. This bias condition approximately corresponds to the point at which the slope is highest in the "hump" of the *C-V*.

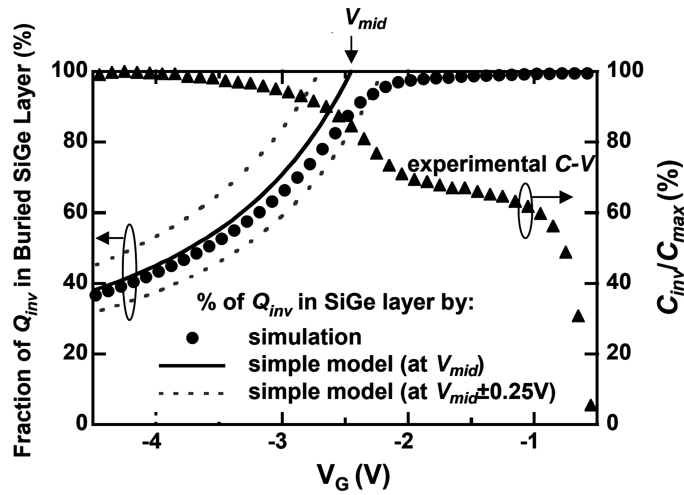

Figure A.3 Experimental, normalized *C-V* for a 55/25 HOI p-MOSFET with 5 nm-thick strained Si cap and 10 nm-thick buried $Si_{0.45}Ge_{0.55}$ layer (right axis), and the fraction of the total inversion charge that populate the buried $Si_{0.45}Ge_{0.55}$ layer (left axis). The simple model (line) approximates the simulated (*nextnano*^{3}) hole allocation (filled circles) well, especially away from V_{mid}. The effect of a ±0.25V extraction variation in V_{mid} is indicated (dashed lines).

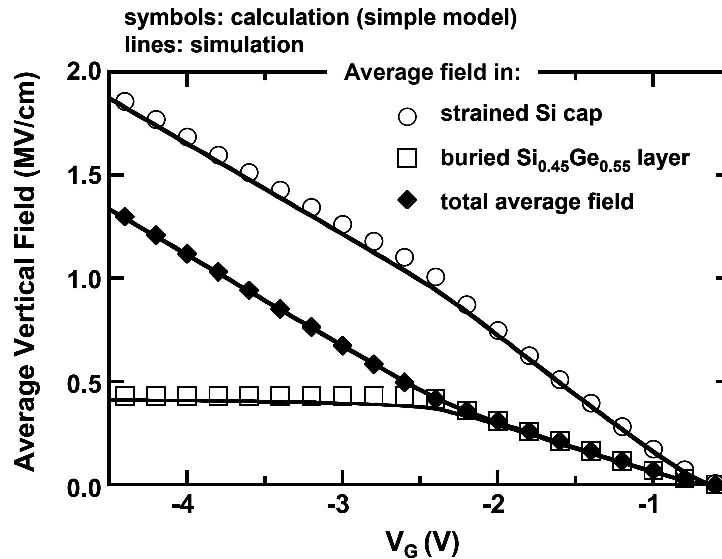

Figure A.4 Average total vertical field and the average field in the Si cap and buried $Si_{0.45}Ge_{0.55}$ layer of a 55/25 HOI p-MOSFET with 5 nm-thick strained Si cap and 10 nm-thick buried $Si_{0.45}Ge_{0.55}$ layer. Symbols are calculated from the simple charge allocation model (see Figure A.3), and lines are from simulations in *nextnano*^{3}.

±0.25V away from the simulated value has been indicated. While this model doesn't provide more than a first order, rough approximation, it gives a reasonable qualitative view of the allocation of charge in the HOI p-MOSFET.

Finally, connecting this approximate approach for carrier allocation to the discussion in section A.1, the average field in the various layers of a heterostructure device can be approximately determined. In Figure A.4, the average vertical field obtained from Equations A.4 and A.5 by the approximate approach is compared to the field obtained by using the simulated charge distribution in the device. With respect to the average field, the approximate method is forgiving, and yields a surprisingly accurate estimate of the average field in each layer as well as in the overall structure.

The above approach seemingly works best on structures with a relatively clear "hump" in the *C-V*, since it relies on finding an approximation for V_{mid} by inspection in the *C-V*. However, as the "hump" gradually disappears from the *C-V* when the cap thickness is reduced (see Figure 5.6), this physically means that conduction in the cap layer has less significance, and any error from poor estimates of V_{mid} will move to the very highest fields and inversion charge densities. For this reason, a poor estimate of V_{mid} has less significance for most of the field range. As an example, for a 55/25 HOI p-MOSFET with 2.8 nm strained Si cap, and 10 nm buried layer, the total inversion charge density at $V_G=V_{mid}$ is already > 1.2×10^{13} cm^{-2}, and simulations show that even a very large ±0.5 V error in estimating V_{mid} only leads to a maximum error of the overall average vertical field by roughly ±5% (for a total average field of ~ 1 MV/cm). For HOI

with cap thicknesses larger than 3 nm, the "hump" is clear so that V_{mid} can easily be extracted with reasonable accuracy, and for cap thicknesses below 3 nm, the inversion population in the cap layer becomes negligible as shown in Figure 5.6 and 5.10.

A.3 Field Effect Mobility at High Parasitic Series Resistance

In Chapter 2, the extraction of effective mobility was described. When using the mobility extraction device in Figure 2.12, the correct effective mobility could be extracted despite the high series resistance. Another measure of mobility is the field effect mobility, Equation 2.19. In this section, it will become clear that the field effect mobility is affected by series resistance in a more complicated way than the effective mobility.

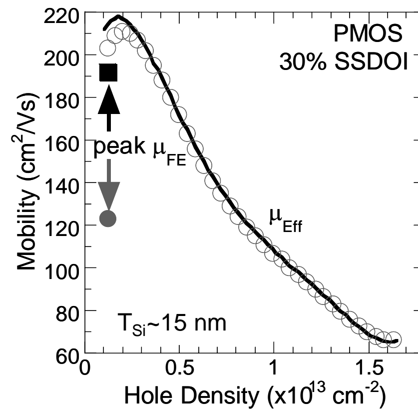

Figure A.5 Mobility vs. hole density for a 30% SSDOI p-MOSFET. The line is the effective mobility for an external R_{sr} of 6kΩ and the filled square is the peak field effect mobility for the same R_{sr}. The same device was subsequently measured with R_{sr}=160 kΩ (open circles for effective mobility and filled circle for peak field effect mobility). With the use of the mobility extraction MOSFET (Figure 2.12), the extracted effective mobility is not sensitive to series resistance, while this is not true for the field effect mobility.

It is clear from Figure A.5 that whereas effective mobility is independent of series resistance, the corresponding field effect mobility, extracted from Equation 2.19 is not. This is due to the non-linearity of the channel conductance as the device is turned on. Combining Equations 2.19, 2.20, 2.21 and

$$I_d = \frac{W}{L}\mu_{Eff}(V_g)\cdot Q_{inv}(V_g)\cdot V_d(V_g), \qquad \text{(Equation A.8)}$$

yields the field effect mobility

$$\mu_{FE} = \frac{C_{gc}}{C_{ox}}\mu_{Eff} + \frac{Q_{inv}}{C_{ox}}\cdot\frac{\partial \mu_{Eff}}{\partial V_g} + \mu_{Eff}\frac{Q_{inv}}{C_{ox}V_d}\cdot\frac{\partial V_d}{\partial V_g} \qquad \text{(Equation A.9)}$$

The impact of the second term, which represents the dependence of the mobility on gate bias, has already been discussed by Sun and Plummer [112], in which they stress the

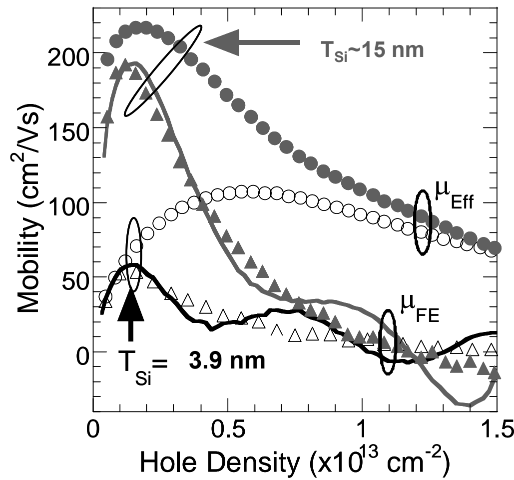

Figure A.6 Mobility vs. hole density for 30% SSDOI p-MOSFETs with 3.9 nm-thick body (open symbols, high series resistance) and ~15 nm-thick body (filled symbols, lower series resistance). The series resistance differs by approximately two orders of magnitude between the two devices. Measured effective mobility (circles) and field effect mobility (triangles) are shown. The calculated field effect mobilities from Equation A.9 (lines) are noisy away from the peak value due to differentiation, but correctly predict the measured field effect mobilities, which are affected by series resistance.

importance of using μ_{Eff} to characterize transport. However, the third term depends upon the series resistance. Since $V_d = V_{dtot} - R_{sr} I_d$, we can not disregard the third term if the series resistance R_{sr} is large. By comparing μ_{FE} obtained from Equation 2.19 to that of differentiating μ_{Eff} and V_d according to Equation A.9, we find that series resistance is indeed the cause of the observed shifts in μ_{FE} (Figure A.6). Therefore, it is even more important for devices with high series resistance to use effective mobility for device modeling of transport properties.

From Equation A.8 and $V_d = V_{dtot} - R_{sr} I_d$, we can rewrite the current in terms of the applied drain bias, V_{dtot}, as

$$I_d = \frac{\frac{W}{L}\mu_{Eff}(V_g)\cdot Q_{inv}(V_g)\cdot V_{dtot}}{1+\frac{W}{L}\mu_{Eff}(V_g)\cdot Q_{inv}(V_g)\cdot R_{sr}} \qquad \text{(Equation A.10)}$$

Thus, after solving for V_d and differentiating with respect to V_g

$$\frac{dV_d}{dV_g} = -R_{sr}\left[\frac{\frac{W}{L}\left(\frac{\partial \mu_{Eff}}{\partial V_g}Q_{inv} + \mu_{Eff}\frac{\partial Q_{inv}}{\partial V_g}\right)V_{dtot}}{1+\frac{W}{L}\mu_{Eff}Q_{inv}R_{sr}}\left(1-\frac{1}{1+\left(\frac{W}{L}\mu_{Eff}Q_{inv}R_{sr}\right)^{-1}}\right)\right],$$

(Equation A.11)

we can more easily model the series resistance correction term (third term of Equation A9). In order to estimate how this correction varies with R_{sr}, we assumed *W/L = 15/100* (as in the mobility extraction device of this work) with $Q_{inv}(V_g) = C_{ox}(V_g - V_t)$. With this approximation, and for the point at which $d\mu_{Eff}/dV_g = 0$ (the peak mobility), we find

$$\mu_{FE} = \mu_{Eff}\left(1+\gamma\right), \text{ where } \gamma = \frac{Q_{inv}}{C_{ox}V_d} \cdot \frac{\partial V_d}{\partial V_g} < 0 \,. \qquad \text{(Equation A.12)}$$

As is seen (Figure A.7), γ is significant in the range of R_{sr} observed in this study (Figure 2.11). For the calculation, we assumed $\mu_{Eff} = 100\,\text{cm}^2/\text{Vs}$, similar to the mobility of the 3.9-nm thin device in Figure A.6.

In conclusion, it appears that the effective mobility is the preferred mobility measure, not only from a physics point of view [112], but also since extraction of field effect mobility relies on more complicated series resistance compensation methods, which are noisy – in particular away from the peak mobility point.

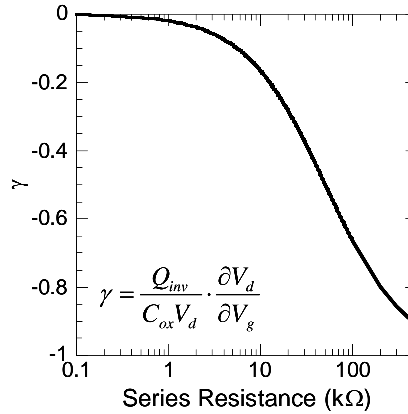

Figure A.7 Calculated series resistance correction factor, γ (unit-less, see Equation A.12), of field effect mobility at the point of maximum effective mobility as a fraction of effective mobility (equation shown as inset), vs. series resistance. For the observed resistance values of this work (10–100 kΩ) the series resistance strongly affects the field effect mobility, showing why it is better from an extraction point of view to analyze effective mobilities. A constant mobility of 100 cm^2/Vs was assumed for the calculation.

Appendix B

SSDOI and HOI Substrate Fabrication Flow

Below, a typical low temperature HOI substrate fabrication flow is listed. SSDOI substrates and HOI substrates with higher thermal budget were fabricated similarly, except for the differences listed in Chapter 3. For an abbreviated, but more descriptive general process introduction to all the substrate processes, please refer to Chapter 3.

B.1 Low-T Bond

Process started on 3/15/2005. The process starts after the substrates have been grown epitaxially.

1. rca clean modified recipe — rcaICL
   10 min pirahna ~101C
   15 s HF
   10 min SC-2

2. LTO dep — 6C-LTO
   133 min "400C 45A/min" (2 h 13 min)

5. Densify LTO, 5B-Anneal — 5B-Anneal
   2A600 (600C), 2 hours (effectively 2.5 hours 600C)
   run time 3h 24 min

6. measure thickness (ellipsometry) — UV1280

7. CMP oxide

rate by doing cmp room meas on dummies
TS35,QS15,DF6,BP5,slurry150
cmp 90 s

8. clean premetal(ICL)
10+5 pclean

9. oxide measurement UV1280
average removal rate in CMP was ~28A/s

10. pre-activation rca (bond round 2)rcaTRL

5 SC-1
10 SC-2
3-5 s HF (remove 20A LTO)
5 SC-1

11. activation AME5000
recipe IABERG-O2, 20s
(condition by ChA clean+5 recipe dummies)

12. bond clean rcaTRL
8 min piranha 100C (black)

13. wafer bonding EV620
particles ok, but not perfect ~1-2 per wafer

14. anneal A1-GateOx

2 hr ~310C (setp 271) in 11 AM
2 hr 400C (including up ramp), setp 353
1.5 hr 450C (including up ramp), setp.
20 min up ramp to 550C, take wafers out after a few minutes of hold

process ended on 3/18/2005

B.2 Etch-Back

Process started on 3/24/2005. The process starts after the substrates have been ground back mechanically at GDSI.

Step	Location
1. sponge clean DI water+sponge N2 gun dry	CMP room
2. post outsource clean 10 min blue piranha 10 min green piranha 10-15 min HF (STRIP BACKSIDE OXIDE!)	premetal-Piranha
3. CMP 10 min TS35,Q13,6,5,150 std shim=1brown 2 green	CMP
4. post cmp clean 10 min blue piranha 10 min green piranha 15 s HF	premetal-Piranha
5. Si etch back TMAH etch for total of 3 h 30 min no backside protection	TMAH/KOH-hood
6. post tmah cmp rinse in DI first and swab off flakes…modified A param, 6 df, 5 bp 1blue 1 clear 90s per wafer	CMP
7. post cmp clean dbl piranha 10+10 min + HF	premetal-Piranha
8. SiGe etch 1 (acetic based, Ch3) 20-25 min, 25% relaxed layer	acid-hood2
9. TMAH strip	KOH/TMAH-hood

1:1 TMAH:2-propanole
80C, ~<=30s, move in wet proc. box

10. Post TMAH clean — premetal-Piranha
10 blue
10 green
15s HF

11. SiGe2 (SC-1) — acid-hood2
25+5+2+2+2

process ended on 3/29/2005

Appendix C

Device Fabrication Flow

Below, a typical low temperature HOI device fabrication flow is listed. SSDOI substrates and HOI substrates with higher thermal budget were fabricated similarly, except for the differences listed in Chapter 4, and 5. For an abbreviated, but more descriptive general process introduction to all the device processes, refer to Chapters 4-6. In the below, some key differences between processing of SSDOI and low-T HOI have been indicated in the flow.

C.1 The HOI MOSFET Device Flow

Process started on 4/1/2005. The process starts after the substrates have been prepared by the process in Appendix B.

1. coat wafers 1.03 mu resist coater6
IA-L2small program (modified for step pitch 11.3mm)

2. expose STI level (mesa) i-stepper
used 125 ms, -0.2 focus
dev6, develop

4. Etch mesa AME5000
use recipes iaberg lto (1)
and Keith CP (2)
according to sequence (1), 10desc,10smain, (2) 35smain (1), 7smain

5. double piranha premetal-Piranha
(strip resist&clean)
10 min blue, SRD
5 min green, SRD

6. modified RCA clean rcaICL
10 min pirahna (~100C)
15 s HF
10 min SC-2

13. gate oxidation 5D-ThickOx
3h 15 min at 600C, wet est. 39A
run time 5h 43min, 5h in furnace
uv1280: 38 A
(SSDOI: 4 nm gate oxide at 800C, dry oxidation in 5A)

14. poly dep 6A-nPoly
doped poly 560 PH3 flat
last time 12.7A/min, target 1000A
now, dep: 1 hour 20 min (80 min)
(SSDOI: used undoped poly-Si for p-MOSFET)

15. backside & frontside native oxide strip premetal-Piranha

16. frontside coat coater6
coat w hardbake 130 60s

17. backside poly strip LAM490B
mount wafers backways
run poly timed recipe, Cl2, 15s+15s oe
cleared after 13-14s

18. ash asher
ash frontside resist
2 min 30s/wafer

19. oxide strip premetal-Piranha

20. frontside coat coater6
1.01 micron thick resist, spin 1 mu thick at 4000rpm

21. FG pattern i-stepper
120ms, -0.2focus

22. gate etch LAM490B
poly timed Cl2. Main 14s, oe 14s
(sometimes used AME5000 for gate etches)

23. resist strip, all wfrs premetal-Piranha
(strip resist&clean)
2x10 min piranha 3:1

26. rca clean mod rcaICL

5 min pirahna ~95C
5 s HF (avoid gate undercut and mesa problems)
10 min SC-2 80C

27. LTO deposition 6C-LTO
LTO-GATE1 recipe
15 min dep time, 132 A oxide by UV1280 (step 28)
run time 4h00min

29. photo PIN 1. i-stepper, coater6
0 11000 0 11000 -5491 -5500
also, blanket PMOS dies
For this lot, made PIN diodes and also NMOS and PMOS on
The same wafer. For this reason, used a PR implant mask
To mask off dice or areas. For PIN, used active mask layer
shifted side-ways by the measurement of the source+1 micron
to get implant on one side of gate only.

30. uv cure LL

31. implant at Innovion, parameters:
pmos:
1: BF2 4e15 7t, 25keV

32. Post implantation clean premetal-Piranha
10 min blue piranha

33. ash 3 min (pmos/nmos only)

34. photo PIN 2. 125,-0.2 1 micron resist i-stepper, coater6
0 11000 0 11000 -5509 -5500
also, blanket NMOS dies

35. uv cure LL

36. implant nmos/pmos PIN wfrs only
Phosphorus 4e15 7t, 17keV

37. Post implantation clean (pmos/nmos) premetal-Piranha
10 min blue piranha

38. (a) ash 3 min (pmos/nmos only)
(b) 5 min green piranha

39. spin 1 micron resist coater6
40. shoot blank dies 125,-0.2 i-stepper
41. develop dev6 coater6

42. oxide strip (screen)
in material dice oxide-BOE

43. etch poly in blank dies LAM490B
poly-timed 14s+14s
uv1280 S14 238A (50A ox on top)
loss estimate: 25A

(step 42 and 43 opens up blanket "material" dies so they can be easily accessed later on by a simple HF dip. Note: done after implant, and done so metal will never be in contact with surface)

44. modified RCA clean RCAICL
10 piranha 92C
5s HF
10 SC-2 85C

45. LTO dep (via isolation) 6C-LTO
30 min dep, 400C, dep rate ~60 A/min

46. rca clean rcaICL
mod. pclean

47. S/D/G activation RTP1 wafers RTP
lta800 (10s at 800C after 2 min 625C)
(For SSDOI, used 1000C process)

48. coat wafers (1 mu resist) coater6
0.8 resist spun 2600, ~1-1.1 micron thick

49. Shoot contact level — i-stepper
125ms (5 ms longer than FG), -0.2 ok

50. contact etch — acid-hood2
5:1 diluted (7:1) BOE
wfrs: 2.15 min+45s oe (30%)

51. resist strip — premetal-Piranha
10 min blue
5 min green
1 min HF

52. metallization — endura
1500A Ti + 1 micron Al front
no backside metal

53. coat wfrs 1mu resist — coater6

54. metal litho — i-stepper
95ms, -0.2, align to gate

55. metal wet etch — acidhood2
PAN Etch RT (16 ph:2 H_2O:1nitr:1acet)
heated 45C
final etch: 2desheet, total time 2.45 min
dilute BOE (just a little in a bucket of DI) for TI, time varies depending on dilution

56. ash resist — asherICL
3 minutes

57. sinter
450C, 30 min (setp. 470)

process ended 5/11/2005.

Bibliography

1 *International Technology Roadmap for Semiconductors*, 2003 Edition, available at http://public.itrs.net

2 T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90 nm high volume manufacturing logic technology featuring novel 45 nm gate length strained silicon CMOS transistors," in *IEDM Tech. Dig*., 2003, pp. 978-980.

3 *International Technology Roadmap for Semiconductors*, 2005 Edition, available at http://public.itrs.net

4 Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Ultrathin-Body SOI MOSFET for Deep-Sub-Tenth Micron Era," *IEEE Electron Device Lett.*, vol. 21, pp. 254-255, 2000.

5 T. Ernst, S. Cristolovean, G. Ghibaudo, T. Ouisse, S. Horiguchi, Y. Ono, Y. Takahashi, and K. Murase, "Ultimately Thin Double-Gate SOI MOSFETs," *IEEE Trans. Electron Dev.*, vol. 50, pp. 830-838, 2003.

6 X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," in *IEDM Tech. Dig.,* 1999, pp. 67-70.

7 T. Irisawa, T. Numata, T. Tezuka, K. Usuda, S. Nakaharai, N. Hirashita, N. Sugiyama, Eiji Toyoda, and S. Takagi, "High Performance Multi-Gate p-MOSFETs using Uniaxially-Strained SGOI Channels," in *IEDM Tech. Dig*., 2005, s30p1.

8 Z. Ren, and M. Lundstrom, "Simulation of nanoscale MOSFETs: a scattering theory interpretation," Superlattices and Microstructures, vol. 27, pp. 177-189, 2000.

9 M. Lundstrom, "Elementary Scattering Theory of the Si MOSFET," *IEEE Electron Device Lett.*, vol. 18, pp. 361-363, 1997.

10 S. Wolf, *Silicon Processing for the VLSI Era, Volume 3 – The Submicron MOSFET*, 1995, Lattice Press.

11 M.S. Lundstrom, "On the Mobility Versus Drain Current Relation for a Nanoscale MOSFET," *IEEE Electron Device Lett.*, vol. 22, pp. 293-295, 2001.

12 A. Lochtefeld, and D.A. Antoniadis, "Investigating the Relationship Between Electron Mobility and Velocity in Deeply Scaled NMOS via Mechanical Stress," *IEEE Electron Device Lett.*, vol. 22, pp.591-593, 2001.

13 G. Niu, J.D. Cressler, S.J. Mathew, and S. Subbanna, "A Total Resistance Slope-Based Effective Channel Mobility Extraction Method for Deep Submicron CMOS Technology," *IEEE Trans. Electron Dev.*, vol. 46, pp. 1912-1914, 1999.

14 K. Rim, S. Narasimha, M. Longstreet, A. Mocuta, and J. Cai, "Low Field Mobility Characteristics of Sub-100 nm Unstrained and Strained Si MOSFETs," in *IEDM Tech. Dig.,* 2002, pp. 43-46.

15 S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: part I-effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol 41, pp. 2357-2362, 1994.

16 J. Koomen, "Investigation of the MOST channel conductance in weak inversion," *Solid-State Electron.*, vol. 16, pp. 801-810, 1973.

17 C.G. Sodini, T.W. Ekstedt, and J.L. Moll, "Charge accumulation and mobility in thin dielectric MOS transistors," *Solid-State Electron.*, vol. 25, pp. 833-841, 1982.

18 J. Koga, S. Takagi, and A. Toriumi, "Influences of Buried-Oxide Interface on Inversion-Layer Mobility in Ultra-Thin SOI MOSFETs," *IEEE Trans. Electron Devices*, vol 49, pp. 1042-1048, 2002.

19 C. Kittel, *Introduction to Solid State Physics*, 7th edition, 1996, John Wiley & Sons, Inc.

20 R.W. Olesinski, and G.J. Abbaschian, "The Ge-Si (germanium-silicon) system," *Bull. Alloy Phase Diagrams*, vol. 5, p. 180, 1984.

21 C.G. Van de Walle, and R.M. Martin, "Theoretical calculations of heterojunction discontinuities in the Si/Ge system," *Phys. Rev. B*, vol. 34, pp. 5621-5634, 1986.

22 J. Singh, *Physics of semiconductors and their heterostructures*, 1993, New York: McGraw-Hill.

23 Landolt-Börnstein, *Numerical Data and Functional Relationships in Science and Technology*, 1987, Berlin, New York: Springer-Verlag.

24 R. People, and J.C. Bean, "Calculation of critical layer thickness versus lattice mismatch in Ge_xSi_{1-x}/Si strained layer heterostructures," *Appl. Phys. Lett.*, vol. 47, pp. 322-324, 1985.

25 D.C. Houghton, "Strain relaxation kinetics in $Si_{1-x}Ge_x/Si$ heterostructures", *J. Appl. Phys.*, vol. 70, pp. 2136-2151, 1991.

26 Y.H. Xie, E.A. Fitzgerald, D. Monroe, P.J. Silverman, and G.P. Watson, "Fabrication of high mobility two-dimensional electron and hole gases in GeSi/Si", *J. Appl. Phys.*, vol. 73, pp. 8364-8370, 1993.

27 J. Welser, J.L. Hoyt, and J.F. Gibbons, "Growth and Processing of Relaxed-SiGe/Strained-Si Structures for Metal-Oxide Semiconductor Applications," *Jpn. J. Appl. Phys.*, vol. 33, pp. 2419-2422, 1994.

28 E.A. Fitzgerald, "GeSi/Si Nanostructures," *Annu. Rev. Mater. Sci.*, vol. 25, pp. 417-454, 1995.

29 T. Tezuka, N. Sugiyama, and S. Takagi, "Fabrication of strained Si on an ultrathin SiGe-on-insulator virtual substrate with a high-Ge fraction," *Appl. Phys. Lett.,* vol. 79, pp. 1798-1800, 2001.

30 T. Mizuno, N. Sugiyama, T. Tezuka, and S. Takagi, "Relaxed SiGe-on-insulator substrates without thick SiGe buffer layers," *Appl. Phys. Lett.*, vol. 80, pp. 601-603, 2002.

31 S. Takagi, T. Mizuno, T. Tezuka, N. Sugiyama, T. Numata, K. Usuda, Y. Moriyama, S. Nakaharai, J. Koga, A. Tanabe, N. Hirashita, and T. Maeda, "Channel Structure Design, Fabrication and Transport Properties of Strained-Si/SiGe-On-Insulator (Strained-SOI) MOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 57-60.

32 J.M. Hinckley, and J. Singh, "Hole transport theory in pseudomorphic $Si_{1-x}Ge_x$ alloys grown on Si(001) substrates," *Phys. Rev. B*, vol. 41, pp. 2912-2926, 1990.

33 T. Manku, and A. Nathan, "Energy-band structure for strained p-type $Si_{1-x}Ge_x$," *Phys. Rev. B*, vol. 43, pp. 12634-12637, 1991.

34 M.M. Rieger, and P. Vogl, "Electronic-band parameters in strained $Si_{1-x}Ge_x$ alloys on $Si_{1-y}Ge_y$ substrates," *Phys. Rev. B*, vol. 48, pp. 14276-14287, 1993.

35 J.J. Welser, Ph. D. Thesis, Stanford University, 1994.

36 M.V. Fischetti, and S.E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge and SiGe alloys," *J. Appl. Phys.*, vol. 80, pp. 2234-2252, 1996.

37 C. Ni Chleirigh, C. Jungemann, J. Jung, O. O. Olubuyide, and J. L. Hoyt, "Extraction of band offsets in strained Si/strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ dual-channel enhanced mobility structures," in *ECS 2004 Proceedings: SiGe: Materials, Processing and Device,* vol. PV2004-7, pp. 99-109.

38 J.M. Hinckley, and J. Singh, "Influence of substrate composition and crystallographic orientation on the band structure of pseudomorphic Si-Ge alloy films," *Phys. Rev. B*, vol. 42, pp. 3546-3566, 1990.

39 *nextnano*[3] available at http://www.nextnano.de

40 R. Oberhuber, G. Zandler, and P. Vogl, "Subband structure and mobility of two-dimensional holes in strained Si/SiGe MOSFETs," *Phys. Rev. B*, vol. 58, pp. 9941-9948, 1998.

41 K. Rim, J. Chu, H. Chen, K. A. Jenkins, T. Kanarsky, K. Lee, A. Mocuta, H. Zhu, R. Roy, J. Newbury, J. Ott, K. Petrarca, P. Mooney, D. Lacey, S. Koester, K. Chan, D. Boyd, M. Ieong, and H.-S. Wong, "Characteristics and device design of sub-100 nm strained Si N- and PMOSFETs," in *Symp. VLSI Tech. Dig.*, 2002, pp. 98-99.

42 S. Takagi, J.L. Hoyt, J.J. Welser, and Gibbons, "Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 80, pp. 1567-1577, 1996.

43 C. W. Leitz, M. T. Currie, M. L. Lee, Z. -Y. Cheng, D. A. Antoniadis, and E. A. Fitzgerald, "Hole mobility enhancements in strained $Si/Si_{1-y}Ge_y$ p-type metal-oxide-semiconductor field effect transistors grown on relaxed $Si_{1-x}Ge_x$ ($x<y$) virtual substrates," *Appl. Phys. Lett.*, vol. 79, pp. 4246-4248, 2001.

44 J. Jung, M. L. Lee, S. Yu, E. A. Fitzgerald, and D. A. Antoniadis, "Implementation of both high-hole and electron mobility in strained Si/strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ ($x<y$) virtual substrate," *IEEE Electron Device Lett.*, vol. 24, pp. 460-462, 2003.

45 M. L. Lee and E. A. Fitzgerald, "Optimized strained Si/strained Ge dual-channel heterostructures for high mobility P- and N-MOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 429-432.

46 M.V. Fischetti, Z. Ren, P.M. Solomon, M. Yang, and K. Rim, "Six-band k.p calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain, and silicon thickness," *J. Appl. Phys.,* vol. 94, pp. 1079-1095, 2003.

47 S.E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, “Key Differences For Process-induced Uniaxial vs. Substrate-induced Biaxial Stressed Si and Ge Channel MOSFETs,” in *IEDM Tech. Dig.*, 2004, pp. 221-224.

48 S. Ito, H. Namba, K. Yamaguchi, T. Hirata, K. Ando, S. Koyama, S. Kuroki, N. Ikezawa, T. Suzuki, T. Saitoh, and T. Horiuchi, “Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design,” in *IEDM Tech. Dig.*, 2000, pp. 247-250.

49 A. Shimizu, K. Hachimine, N. Ohki, H. Ohta, M. Koguchi, Y. Nonaka, H. Sato, and F. Ootsuka, “Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement,” in *IEDM Tech. Dig.*, 2001, pp. 433-436.

50 S. Tyagi, C. Auth, P. Bai, G. Curello, H. Deshpande, S. Gannavaram, O. Golonzka, R. Heussner, R. James, C. Kenyon, S.-H. Lee, N. Lindert, M. Liu, R. Nagisetty, S. Natarajan, C. Parker, J. Sebastian, B. Sell, S. Sivakumar, A. St Amour, and K. Tone, “An advanced low power, high performance, strained channel 65nm technology,” in *IEDM Tech. Dig.*, 2005, s10p8.

51 R. Arghavani, L. Xia, H. M’Saad, M. Balseanu, G. Karunasiri, A. Mascarenhas, and S.E. Thompson, “A Relibable and Manufacturable Method to Induce a Stress of > 1 GPa on a P-Channel MOSFET in High Volume Manufacturing,” *IEEE Electron Device Lett.*, vol. 27, pp. 114-116, 2006.

52 E. Wang, P. Matagne, L. Shifren, B. Obradovic, R. Kotlyar, S. Cea, J. He, Z. Ma, R. Nagisetty, S. Tyagi, M. Stettler, and M.D. Giles, “Quantum mechanical calculation of hole mobility in silicon inversion layers under arbitrary stress,” in *IEDM Tech. Dig.*, 2004, pp. 147-150.

53 J.-S. Lim, S.E. Thompson, and J.G. Fossu, “Comparison of Threshold Voltage Shifts for Uniaxial and Biaxial Tensile-Stressed n-MOSFETs,” *IEEE Electron Device Lett.*, vol. 25, pp. 731-733, 2004.

54 I. Lauer, I. Aberg, Z.-Y. C. Cheng,T.A. Langdo, A. Lochtefeldt, J.L. Hoyt, and D.A. Antoniadis, “Effects of Uniaxial Strain on Mobility in Thick and Ultra-thin SOI and SSDOI NMOS and PMOS FETs,” submitted for publication.

55 Mark Lundstraom, *Fundamentals of carrier transport*, 2nd edition, 2000, Cambridge University Press.

56 S. Takagi, J. Koga, and A. Toriumi, “Mobility Enhancement of SOI MOSFETs due to Subband Modulation in Ultrathin SOI Films,” *Jpn. J. Appl. Phys.*, vol. 37, pp. 1289-1294, 1998.

57 J.L. Hoyt, H.M. Nayfeh, S. Eguchi, I. Aberg, G. Xia, T. Drake, E.A. Fitzgerald, and D.A. Antoniadis, "Strained Silicon MOSFET Technology," in *IEDM Tech. Dig.*, 2002, pp. 23-26.

58 M. Shoji, and S. Horiguchi, "Phonon-limited inversion layer electron mobility in extremely thin Si layer of silicon-on-insulator metal-oxide-semiconductor field-effect transistor," *J. Appl. Phys.*, vol. 82, pp. 6096-6101, 1997.

59 K. Uchida, J. Koga, R. Ohba, T. Numata, and S. Takagi, "Experimental Evidences of Quantum-Mechanical Effects on Low-field Mobility, Gate-channel Capacitance, and Threshold Voltage of Ultrathin Body SOI MOSFETs," in *IEDM Tech. Dig.*, 2001, pp. 633-636.

60 K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata and S. Takagi, "Experimental Study on Carrier Transport Mechanism in Ultrathin-body SOI n- and p-MOSFETs with SOI Thickness less than 5 nm," in *IEDM Tech. Dig.*, 2002, pp. 47-50.

61 Z. Ren, P.M. Solomon, T. Kanarsky, B. Doris, O. Dokumaci, P. Oldiges, R.A. Roy, E.C. Jones, M. Ieong, R.J. Miller, W. Haensch, and H.-S. Philip Wong, "Examination of Hole Mobility in Ultra-thin Body SOI MOSFETs," in *IEDM Tech. Dig.*, 2002, pp. 51-54.

62 K. Uchida, and S. Takagi, "Carrier scattering induced by thickness fluctuation of silicon-on-insulator film in ultrathin-body metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 82, pp. 2916-2918, 2003.

63 D. Esseni, M. Mastrapasqua, G.K. Celler, C. Fiegna, L. Selmi, and E. Sangiorgi, "Low Field Electron and Hole Mobility of SOI Transistors Fabricated on Ultrathin Silicon Films for Deep Submicrometer Technology Application," *IEEE Trans. Electron Devices*, vol 48, pp. 2842-2850, 2001.

64 T.S. Drake, C. Ní Chléirigh, M.L. Lee, A.J. Pitera, E.A. Fitzgerald, D.A. Antoniadis, D.H. Anjum, J. Li, R. Hull, N. Klymko, and J.L. Hoyt, "Fabrication of ultra-thin strained silicon on insulator," *J. Elec. Mat.*, vol. 32, pp. 972-975, 2003.

65 I. Åberg, O.O. Olubuyide, J. Li, R. Hull, and J.L. Hoyt, "Fabrication of strained Si/strained SiGe/strained Si heterostructures on insulator by a bond and etch-back technique," in *IEEE International SOI Conf. Tech Dig.*, 2004, pp. 35-36.

66 P.M. Mooney, "Strain relaxation and dislocations in SiGe/Si structures," *Material Science and Engineering*, vol. R17, pp. 105-146, 1996.

67 D.G. Schimmel, “Defect Etch for <100> Silicon Evaluation,” *J. Electrochem. Soc.: Solid-State Science and Technology*, vol. 126, pp. 479-483, 1979.

68 C.S. Tan, and R. Reif, “Microelectronics Thin Film Handling and Transfer Using Low-Temperature Wafer Bonding,” *Electrochemical and Solid-State Letters*, vol. 8, pp. G362-G366, 2005.

69 GDSI, Grinding and Dicing Services Inc., http://www.wafergrind.com

70 Z.-Y. Cheng, M.T. Currie, C.W. Leitz, G. Taraschi, E.A. Fitzgerald, J.L. Hoyt, and D.A. Antoniadis, “Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates,” *IEEE Electron Device Lett.*, vol. 22, pp. 321-323, 2001.

71 T.K. Carns, M.O. Tanner, and K.L. Wang, “Chemical Etching of $Si_{1-x}Ge_x$ in $HF:H_2O_2:CH_3COOH$,” *J. Electrochem. Soc.*, vol. 142, pp. 1260-1266, 1995.

72 T.A. Langdo, M.T. Currie, A. Lochtefeld, R. Hammond, J.A. Carlin, M. Erdtmann, G. Braithwaite, V.K. Yang, C.J. Vineis, H. Badawi, and M.T. Bulsara, “SiGe-free strained Si on insulator by wafer bonding and layer transfer,” *Appl. Phys. Lett.*, vol. 82, pp. 4256-4258, 2003.

73 K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, F. Cardone, L. Tai, S. Koester, M. Cobb, D. Canaperi, B. To, E. Duch, I. Babich, R. Carruthers, P. Saunders, G. Walker, Y. Zhang, M. Steen, and M. Ieong, “Fabrication and mobility characteristics of ultra-thin strained Si directly on insulator (SSDOI) MOSFETs,” in *IEDM Tech. Dig.*, 2003, pp. 47-52.

74 T.S. Drake, C. Ni Chleirigh, M.L. Lee, A.J. Pitera, E.A. Fitzgerald, D.A. Antoniadis, D.H. Anjum, J. Li, R. Hull, N. Klymko, and J.L. Hoyt, “Effect of rapid thermal annealing on strain in ultrathin strained silicon on insulator layers,” *Appl. Phys. Lett.*, vol. 83, pp. 875-877, 2003.

75 N.R. Zangenberg, J. Lundsgaard Hansen, J. Fage-Pedersen, and A. Nylandsted Larsen, “Ge Self-Diffusion in Epitaxial $S_{i1-x}Ge_x$ Layers,” *Phys. Rev. Lett.*, vol. 87, pp. 125901:1-4, 2001.

76 G. Xia, O.O. Olubuyide, J.L. Hoyt, and M. Canonico, “Strain dependence of Si-Ge interdiffusion in epitaxial $Si/Si_{1-y}Ge_y/Si$ heterostructures on relaxed $Si_{1-x}Ge_x$ substrates,” *Appl. Phys. Lett.*, vol. 88, pp. 13507:1-3, 2006.

77 I. Åberg, O.O. Olubuyide, C. Ní Chléirigh, I. Lauer, D.A. Antoniadis, J. Li, R. Hull, and J.L Hoyt, “Electron and hole mobility enhancements in sub-10 nm-thick strained silicon directly on insulator fabricated by a bond and etch-back technique” in *Symp. VLSI Tech. Dig.*, 2004, pp. 52-53.

78 I. Aberg, and J. L. Hoyt, "Hole transport in ultra-thin body MOSFETs in strained silicon directly on insulator with strained silicon thickness less than 5 nm," *IEEE Electron Device Lett.*, vol. 26, pp. 661-663, 2005.

79 SOITEC SA, http://soitec.com

80 I. Lauer, Ph. D. Thesis, Massachusetts Institute of Technology, 2005.

81 T. Irisawa, T. Numata, T. Tezuka, K. Usuda, N. Hirashita, N. Sugiyama, E. Toyoda, and S. Takagi, "High Current Drive Uniaxially-Strained SGOI pMOSFETs Fabricated by Lateral Strain Relaxation Technique," in *Symp. VLSI Tech. Dig.*, 2005, pp. 178-179.

82 R.Z. Lei, W. Tsai, I. Aberg, T.B. O'Reilly, J.L. Hoyt, D.A. Antoniadis, H.I. Smith, A.J. Paul, M.L. Green, J. Li, and R. Hull, "Strain relaxation in patterned strained silicon directly on insulator structures," *Appl. Phys. Lett.*, vol. 87, pp. 251926:1-3, 2005.

83 J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, 2nd Edition, 1997, Kluwer Academic Publishers.

84 Innovion Inc., http://www.innovion.cc

85 I. Lauer, T.A. Langdo, Z.-Y. Cheng, J.G. Fiorenza, G. Braithwaite, M.T. Currie, C.W. Leitz, A. Lochtefeld, H. Badawi, M.T. Bulsara, M. Somerville, and D.A. Antoniadis, "Fully Depleted n-MOSFETs on Supercritical Thickness Strained SOI," *IEEE Electron Device Lett.*, vol. 25, pp. 83-85, 2004.

86 J.G. Fiorenza, G. Braithwaite, C.W. Leitz, M.T. Currie, J. Yap, F. Singaporewala, V.K. Yang, T.A. Langdo, J. Carlin, M. Somerville, A. Lochtefeld, H. Badawi, and M.T. Bulsara, "Film thickness constraints for manufacturable strained silicon CMOS," *Semicond. Sci. Technol.*, vol. 19, pp. L4-L8, 2004.

87 I. Åberg, C. Ní Chléirigh, O.O. Olubuyide, X. Duan, and J.L. Hoyt, "High electron and hole mobility enhancements in thin-body strained Si/strained SiGe/strained Si heterostructures on insulator," in *IEDM Tech. Dig.*, 2004, pp. 173-176.

88 I. Åberg, Z. Cheng, T.A. Langdo, I. Lauer, A. Lochtefeld, D.A. Antoniadis, and J.L. Hoyt, "Transport and Leakage in Super-Critical Thickness Strained Silicon Directly on Insulator MOSFETs with Strained Si Thickness up to 135 nm," in *IEEE International SOI Conf. Tech Dig.*, 2005, pp. 24-26.

89 Accurel Systems International Corp., http://www.accurel.com

90 Schred 2.0 User's Manual [Online]. Available at: http://www.nanohub.org

91 H.M. Nayfeh, C.W. Leitz, A.J. Pitera, E.A. Fitzgerald, J.L. Hoyt, and D.A. Antoniadis, "Influence of high channel doping on the inversion layer electron mobility in strained silicon n-MOSFETs," *IEEE Electron Device Lett.*, vol. 24, pp. 248-250, 2003.

92 H. Sakaki, T. Noda, K. Hirakawa, M. Tanaka, and T. Matsusue, "Interface roughness scattering in GaAs/AlAs quantum wells," *Appl. Phys. Lett.*, vol. 51, pp. 1934-1936, 1987.

93 A. Khakifirooz, and D.A. Antoniadis, "Scalability of Hole Mobility Enhancement in Biaxially Strained Ultrathin Body SOI," accepted for publication in *IEEE Electron Device Lett.*

94 M. Yang, V. Chan, S.H. Ku, M. Ieong, L. Shi, K.K. Chan, C.S. Murthy, R.T. Mo, H.S. Yang, E.A. Lehner, Y. Surpris, F.F. Jamin, P. Oldiges, Y. Zhang, B.N. To, J.R. Holt, S.E. Steen, M.P. Chudzik, D.M. Fried, K. Bernstein, H. Zhu, C.Y. Sung, J.A. Ott, D.C. Boyd, and N. Rovedo, "On the Integration of CMOS with Hybrid Crystal Orientations," in *Symp. VLSI Tech. Dig.*, 2004, pp. 160-161.

95 T. Tezuka, S. Nakaharai, Y. Moriyama, N. Sugiyama, and S. Takagi, "Selectively-formed high mobility SiGe-on-Insulator pMOSFETs with Ge-rich strained surface channels using local condensation technique," in *Symp. VLSI Tech. Dig.*, 2004, pp. 198-199.

96 J. Jung, C. Ni Chleirigh, S. Yu, O. O. Olubuyide, J. Hoty, and D. A. Antoniadis "Tradeoff between mobility and subthreshold characteristics in dual-channel heterostructure n- and p-MOSFETs," *IEEE Electron Device Lett.*, vol. 25, pp. 562-564, 2004.

97 Dessis: Comprehensive semiconductor device simulator, Integrated Systems Engineering AG, Switzerland. http://www.ise.com.

98 M.G. Ancona, and G.J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor," *Phys. Rev. B*, vol. 39, pp. 9536-9540, 1989.

99 C. Ni Chleirigh, O. O. Olubuyide, and J. L. Hoyt, "Mobility and sub-threshold characteristics in high-mobility dual-channel strained Si/strained SiGe p-MOSFETs," in *IEEE DRC Tech Dig.*, 2005, pp. 203-204.

100 I. Åberg, C. Ni Chleirigh, and J. L. Hoyt, "Thermal processing and mobility in strained heterostructures on insulator," in *ECS 2005 Proceedings: Advanced Gate Stack, Source/Drain and Channel Engineering for Si-Based CMOS: New Materials, Processes, and Equipment,* vol. PV2005-05, pp. 505-514.

101 I. Aberg, C. Ni Chleirigh, and J.L. Hoyt, "Ultra-thin Body Strained Si and SiGe Heterostructure on Insulator MOSFETs," to appear in *IEEE Trans. Electron Devices*, April 2006.

102 H. M. Nayfeh, J. L. Hoyt, and D. A. Antoniadis, "A physically based analytical model for the threshold voltage of strained-Si n-MOSFETs," *IEEE Trans. Electron Devices*, vol 51, pp. 2069-2072, Dec. 2004.

103 S. Yu, J. Jung, J. L. Hoyt, and D. A. Antoniadis, "Strained-Si-strained-SiGe dual-channel layer structure as CMOS substrate for single workfunction metal-gate technology," *IEEE Electron Device Lett.*, vol. 25, pp. 402-404, 2004.

104 B.J. Greene, J. Valentino, J.L. Hoyt, and J.F. Gibbons, "Thin Single Crystal Silicon on Oxide by Lateral Solid Phase Epitaxy of Amorphous Silicon and Silicon Germanium," in *Mat. Res. Society Symp. Proceedings*, Spring 2000 Meeting, vol. 609, pp. A9.3.1-6, 2001.

105 G. Xia, H. M. Nayfeh, M. L. Lee, E. A. Fitzgerald, D. A. Antoniadis, D. H. Anjum, J. Li, R. Hull, N. Klymko, and J. L. Hoyt, "Impact of ion implantation damage and thermal budget on mobility enhancement in strained-Si n-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, pp. 2136-2144, 2004.

106 H.M. Nayfeh, Ph. D. Thesis, Massachusetts Institute of Technology, 2003.

107 T. Krishnamohan, Z. Krivokapic, K. Uchida, Y. Nishi, and K. C. Saraswat, "Low defect ultra-thin fully strained-Ge MOSFET on relaxed Si with high mobility and low band-to-band-tunneling (BTBT)," in *Symp. VLSI Tech. Dig.*, 2005, pp. 82-83.

108 O. Weber, Y. Bogumilowicz, T. Ernst, J.-M. Hartmann, F. Ducroquet, F. Andrieu, C. Dupré, L. Clavelier, C. Le Royer, N. Cherkashin, M. Hytch, D. Rouchon, H. Dansas, A.-M. Papon, V. Carron, C. Tabone, and S. Deleonibus, "Strained Si and Ge MOSFETs with High-K/Metal Gate Stack for High Mobility Dual Channel CMOS," in *IEDM Tech. Dig.*, 2005, s6p3.

109 F. Andrieu, T. Ernst, O. Faynot, Y. Bogumilowicz, J.-M. Hartmann, J. Eymery, D. Lafond, Y.-M. Levaillant, C. Dupré, R. Powers, F. Fournel, C. Fenouillet-Beranger, A. Vandooren, B. Ghyselen, C. Mazure, N. Kernevez, G. Ghibaudo, and S. Deleonibus, "Co-integrated Dual Strained Channels on Fully Depleted sSDOI CMOSFETs with HfO_2/TiN Gate Stack down to 15nm Gate Length," in *IEEE International SOI Conf. Tech Dig.*, 2005, pp. 223-225.

110 A.G. Sabnis, and J.T. Clemens, "Characterization of the electron mobility in the inverted <100> Si surface," in *IEDM Tech. Dig.*, 1979, pp. 18-21.

111 J. Jung, S. Yu, M.L. Lee, J.L. Hoyt, E.A. Fitzgerald, and D.A. Antoniadis, "Mobility Enhancement in Dual-Channel P-MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, pp. 1424-1431, 2004.

112 S.C. Sun, and J.D. Plummer, "," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1497-1508, 1980.