Measuring and Modeling Low Frequency Dispersion in GaAs MESFET's

by

Hemraj Singh Sodhi

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Abstract

The transconductance and output resistance of GaAs MESFET's as a function of frequency have been observed to change dramatically at low frequencies. So far, a good equivalent circuit-model description of this phenomenon has not been presented. This thesis characterizes low frequency dispersion in GaAs MESFET's as a function of both bias and frequency, and presents two new small-signal equivalent circuit models that capture the measured frequency dependence. To make the characterization possible, a methodology for measuring low frequency S-parameters using a network analyzer is developed. The methodology presented entails the design and implementation of bias-tees that may be used at frequencies as low as 10 Hz. To overcome the limitations of the network analyzer's calibration routines and isolate the device S-parameters, a two-tier de-embedding process is implemented as part of the methodology. Data at a number of bias points are measured and analyzed. The measurements show that the transconductance drops by 6% at around 50 Hz and the output resistance gradually drops by 40% at around 100 Hz. The output capacitance increases by seven orders of magnitude as the frequency is lowered to 10 Hz. The two newly proposed small-signal equivalent circuit models accurately fit the data from 10 Hz to 1 MHz.

Thesis Supervisor: Jesus del Alamo
Title: Associate Professor

Acknowledgments

I would like to thank Joe Staudinger for his moral and technical support over the course of this project. His generosity helped a great deal in bringing the effort to its successful conclusion. I was particularly impressed with his patience and his willingness to help. I was fortunate to have had the chance to work with him. Professor del Alamo, my thesis advisor, kept me pointed in the right direction, and helped enormously in the writing stage of the project. He made some excellent suggestions on how to make my thesis more crisp and to the point. The technicians at Compound Semiconductor Technologies, Steve Shaw, Bill Knappenberger, Dale Ekhardt, and Laura Kaufman, helped keep the lab equipment running. I also appreciated the support of Professor El-Ghazaley of ASU and Peter Blakey, who served as advisors to the project.

My roommate, Jeff Newbern, was extremely generous in providing storage space for my files on his computer. There were many hurdles to overcome in bringing the thesis work from Motorola to MIT, and Jeff's computer expertise proved very helpful. Khalid Shakir, a fellow PBE fraternity brother, lent me the use of his MacIntosh computer for the editting of my figures.

Lastly I would like to thank my parents and my sister. My experience at MIT would certainly not have been possible without their unending love and support.

Contents

1.0 Introduction

This project was motivated by a need to improve the understanding of issues related to measuring and modeling of low frequency dispersion in Gallium-Arsenide Metal-Semiconductor-Field-Effect-Transistors (GaAs MESFET's). This will lead to improved small-signal models that accurately capture the frequency dependence of transconductance and output resistance. Eventually, these improvements will be tied to the large-signal models and will have a direct role in achieving first-pass power amplifier design success. The two advisors of the project were J. M. Golio of Compound Semiconductor Technologies, and Professor Jesus del Alamo of MIT's Microsystems Technologies Laboratories.

In 1990, Golio presented measurements on electrical characteristics of GaAs MESFET's showing that the output resistance and transconductance change dramatically over a frequency range between DC and 100 kHz [1]. He built on the previous work of other researchers who had proposed models that approximated the observed dispersive behavior. (see references in [1]) Based on his simple measurements, he pointed out areas in which existing models could be improved, and then proceeded to suggest his own. He developed a small-signal equivalent circuit model intended to reproduce the frequency dispersion more accurately. This new model had its basis on the physics of the device, as will be shown in chapter 6 [1].

Golio's measurement methodology was used to generate data on device transconductance and output resistance versus frequency at various bias points [1]. However, a more complete picture of low frequency dispersion can be obtained by two-port network parameter measurements. In particular, the output capacitance can be accurately measured using S-parameters. As low frequency dispersion is often attributed to charge-trapping phenomena, measurements on the output capacitance will be crucial in showing the validity of further small-signal modeling of low frequency dispersion.

This thesis first presents an overview of the current methodology, including a review of the large-signal model. It then contrasts radio-frequency (RF) versus direct-current (DC) measurements taken with the existing modeling tools. The development of a new measurement methodology for generating network parameters is discussed, along with the design and implementation of a biasing circuit to be used as a part of the measurement configuration. The data collected are then analyzed. Two improved small-signal models are suggested. Finally, an evaluation of the newly proposed models is presented, with Golio's model used as a basis for comparison.

This project was carried out with the Compound Semiconductor Technologies (CST) organization in Motorola's Semiconductor Products Sector. All measurements were taken with CST equipment and on devices fabricated in the CS-1 factory.

2.0 Current Methodology for Large-Signal Model Extraction

A good description of the existing characterization process will help show where improvements can be made in the modeling process. The large-signal model extraction process involves finding values for parameters that go into equations characterizing MESFET behavior. Details of the procedures for measurements are not explained here. Instead, a description of the measurements taken and their use in the extraction process is provided. The large-signal model contains both linear and non-linear circuit elements to capture the behavior of the MESFET as a function of both bias and frequency. The equations of the Advanced Curtice model give the current from drain to source in terms of bias. The small-signal model is a linear circuit model that captures the frequency dependence of the MESFET. Its element values, however, are tabulated at different bias points. The large-signal model can emulate small-signal behavior when it is linearized at a specified bias point. This emulated behavior may be compared with the actual small-signal behavior, as exhibited in measurements. The small-signal data are used in conjunction with the DC current-voltage data to generate the large-signal model through a parameter-fitting process.

As described above, the RF small-signal data and the DC current-voltage data do not agree well. As a result, a compromise between the two has been the only recourse. A first step toward making such a compromise not needed would be to characterize the dispersion and suggest small-signal models that follow the measured data closely. Most applications require keeping both the DC current voltage characteristics as well as the RF performance in mind. For power amplifier applications in particular, both are crucial.

2.1 The MESFET Large Signal Model

The large-signal circuit model is shown in figure 1. The elements of the model may be classified into linear elements that do not change with bias and non-linear elements that depend on the applied voltages. The bias-dependent elements are indicated by arrows in the figure and are labeled Dgs, Dgd and Id. A second distinction may be made between the parasitic elements and those associated with the intrinsic FET. The series resistance (R) and inductance (L) elements at the gate, source and drain are the parasitic elements, while the rest make up the intrinsic FET [2]. The modeling of the diodes Dgs and Dgd is described in the appendix A.

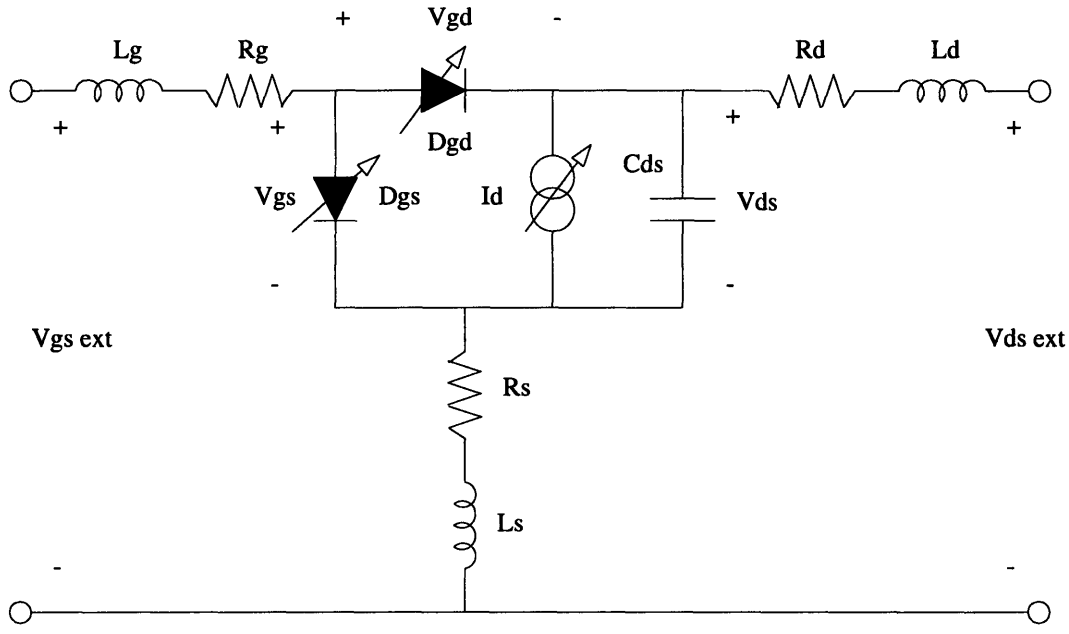

FIGURE 2.1. MESFET Large-signal equivalent circuit.

2.1.1 Parasitic elements

The parasitic elements of the large-signal model capture resistive and inductive effects at the gate, source and drain nodes. The drain to channel connection and the source to channel connection are made through ohmic contacts. The signal arrives at the FET through metal lines, and then passes through the metal contact. It must subsequently traverse a short distance through the n+ contact region to reach the channel. Rd and Rs are used to model the resistive losses that come about as the signal passes from the metal line to the intrinsic FET. The gate connection, a Schottky barrier junction, is formed when the gate-metal is placed on the n-type GaAs material. Rg captures the metallization resistance of the Schottky barrier. Each of these resistances is typically found to be on the order of 1-2 Ω for all devices [2].

The metal lines from the FET to the contact pads give rise to the small inductances shown in figure 2.1. These inductances are modeled by Lg, Ls, and Ld, and are customarily extracted to be on the order of 5 to 50 pH. The source inductance tends to be the smallest of the three, around 5 to 10 pH. The parasitic inductances that come from the packaging are not accounted for in the model [2]. The details on the extraction of these elements is included in appendix B.

2.1.2 The intrinsic FET

In figure 2.1, the four basic elements that make up the intrinsic FET can be seen. Two Schottky diodes are connected to the gate electrode: one from the gate to the source, and the other from the gate to the drain. The current-voltage characteristics of Dgs are a function of Vgs, and those of Dgd are dependent on Vgd. The current flowing through Id is calculated with both Vgs and Vds. One element that stands alone in the intrinsic FET is a voltage independent capacitor, Cds. Its value has been shown not to change appreciably when extracted over a wide range of bias points [7].

As may be seen in figure 2.1, there is a distinction drawn between Vgs ext, and Vgs. Vgs ext is known as the extrinsic gate-source voltage, and Vgs is called the intrinsic gate-source voltage. All voltages Vgs, Vgd, and Vds that are referred to below are intrinsic voltages. Once the parasitics are known, the intrinsic voltages may easily be calculated from the extrinsic voltages.

2.2 The Advanced Curtice Model

The model used to capture the non-linear behavior of the current source is the Advanced Curtice model. [7] A need for improvements in the ability of this model to capture small-signal behavior is the main motivation of this project. The parameters used to describe the DC behavior of the intrinsic FET are invariably the same parameters that influence the predicted small-signal behavior. Other models that are physically based have been suggested as a means of characterizing this current source. However, the Advanced Curtice model provides closer fits to measured data. Id is described by the following equation [2]:

(EQ 2.1)

$$Id = \beta_{eff} Vgst^{VGEXP} (1 + \lambda Vds) \tanh(\alpha Vds) \qquad \text{for } Vgs \geq Vt$$

$$Id = 0 \qquad \text{for } Vgs < Vt$$

where

$$\beta_{eff} = \frac{\beta}{1 + \mu_{crit} Vgst} \qquad \text{(EQ 2.2)}$$

$$Vgst = Vgs - Vt \qquad \text{(EQ 2.3)}$$

The threshold voltage Vt is given below.

$$Vt = Vto + \gamma Vds \qquad \text{(EQ 2.4)}$$

The current in Eq. 2.1 may be linearized mathematically at a fixed bias point. Gm, the transconductance, is found by taking the partial derivative of Id with respect to Vgs. Similarly, Gds, the output conductance, is derived by taking the partial derivative of Id with respect to Vds. The reciprocal of gds is rds, the output resistance. The expressions for gm and gds are given below [2].

$$gm = \frac{\partial Ids}{\partial Vgs} = Ids\left[\frac{VGEXP}{Vgst} - \frac{\mu_{crit}}{1+\mu_{crit}Vgst}\right] \quad \text{(EQ 2.5)}$$

$$gds = \frac{\partial Ids}{\partial Vds} = \beta_{eff}Vgst^{VGEXP}(1+\lambda Vds)\left[\frac{\alpha}{\cosh^2(\alpha Vds)}\right] \quad \text{(EQ 2.6)}$$

$$+\beta_{eff}Vgst^{VGEXP}\lambda\tanh(\alpha Vds) - gm\gamma$$

A conflict arises. From Eqs. 2.1, 2.5 and 2.6, it can be seen that Id, gm and gds depend on all seven parameters: α, β, γ, λ, μ_{crit}, VGEXP and Vto. Eq. 2.1 along with the seven parameters generate modeled IV curves that may be made to closely follow the DC data. If the same parameter values are put into Eqs. 2.5 and 2.6 for the comparison of modeled and measured RF gm and gds, a poor fit is obtained. On the other hand, when they are adjusted to match RF data only, the DC-IV curves are not well modeled [2].

The model also takes into account the time delay between the applied gate-source voltage and the response in drain current. This time delay is represented as τ, which is incorporated in the following equations [2].

$$Id(t_o+\tau) \approx Id(t_o) + \tau\frac{d}{dt}Id = Id(t_o) + \tau\left[\frac{\partial Id}{\partial Vgs}\right]\frac{dVgs}{dt} \quad \text{(EQ 2.7)}$$

$$Id(t_0-\tau) = Id(t_o) - \tau gm\frac{dVgs}{dt} \quad \text{(EQ 2.8)}$$

The above approximation is possible only because gds is significantly smaller than gm.

This time delay described by Eq. 2.8 translates, in the frequency domain, to a multiplication by $\exp(-j\omega\tau)$. When the measured transconductance is plotted against frequency, there is a roll-off at frequencies higher than 26 GHz, which is well corroborated by the model. This is the only way that the Advanced Curtice Model shows a frequency dependent effect. The dramatic change in transconductance and output resistance at low frequencies may not be captured by such a time constant.

2.3 The Small-Signal Model

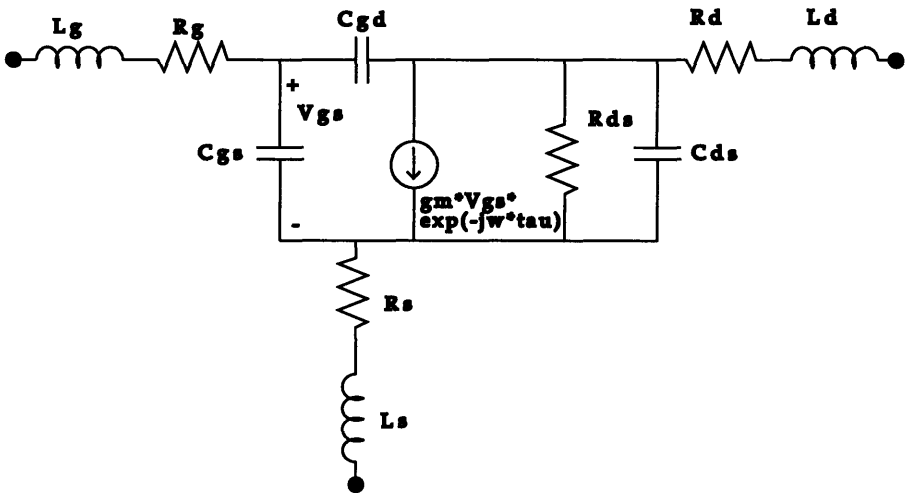

FIGURE 2.2. The Small-signal model circuit schematic for the FET in its constant-current region of operation.

The small-signal model is similar to the large-signal model, in that it is a linearization of the large-signal model at a fixed bias point. Figure 2.2 shows the circuit diagram for the small-signal model [2]. The parasitic elements of the large-signal model are found in the small-signal model as well. The diodes of the large-signal model have been replaced by the capacitors Cgs and Cgd. These capacitors are used to describe the capacitive effects of the space-charge region under the gate. The capacitor Cds, like the parasitic elements, is found in both models. Whereas the large-signal model has a current-source that depends on both Vgs and Vds, the small-signal model has a transconductance generator that captures the incremental change in Id resulting from an incremental change in Vgs. Lastly, the incremental dependence of Id on Vds could be modeled by another transconductance generator which is placed between the intrinsic drain and source nodes. This circuit configuration simplifies to the resistor shown in the figure, Rds. Rds is commonly known as "ro" or the output resistance for MOSFET's or bipolar transistors. The extraction of small-signal element values is outlined in appendix B.

2.4 Large Signal Model Parameter Extraction

Once both the DC and RF small-signal data have been collected, they must be combined to complete the large signal model of figure 2.1. It is at this stage of the modeling process that frequency dispersion creates uncertainty in the current methodology. Work done to better model frequency dispersion will have its most direct impact in tying the small-signal and DC-IV data to the large-signal model parameters. At each of the bias points selected, both a complete set of

RF small-signal element values and DC-IV data are tabulated. Parameter values are required for only the non-linear circuit elements. Those associated with the diodes are Is and η. The capacitors associated with those diodes have the parameters Cgs0, mcgs, Cgd0, and mcgd. The parameters needed for the current source in figure 1 are α, β, μ_{crit}, γ, Vto, VGEXP, and λ [7].

The parasitic elements are assumed to be bias and frequency independent, and so they are put directly into the large-signal model. Experience shows that Cds is bias independent for the most part, so it too is put directly in the large-signal model. τ is taken from the small-signal extraction as well.

Finally, the parameters of the Advanced Curtice Model must be found. Somehow, this current source must reproduce the DC-IV curves and the small-signal characteristics gm and gds by the parameters chosen. The parameters may be chosen so that Id of Eq. 2.1 closely follows DC data, or they may be chosen so that gm and gds of Eqs. 2.5-2.6 closely follow RF small-signal data. If only the DC data is used, the derivatives of Eqs. 2.5-2.6 do not agree with the extracted values of gm and gds. If only the RF data is considered, an overlay of modeled and measured DC data shows a poor fit. A trade-off must be made to approximate both the DC and RF data. This is done by assigning weighing factors to each of three error functions that arise from this trade-off. The error functions are called E_{id}, E_{gm}, and E_{gds}. The corresponding weighing factors are called W_{id}, W_{gm}, and W_{gds}. The net error function sums the errors of the three error functions over all the bias points measured. The expression to be minimized for the best fit is shown below [7]:

$$Error = \frac{\sum_{i=1}^{n} [E_{id}(i)\, W_{id} + E_{gm}(i)\, W_{gm} + E_{gds}(i)\, W_{gds}] \cdot 100}{3n} \qquad \text{(EQ 2.9)}$$

where n is the number of bias points. E_{id}, E_{gm}, and E_{gds} are calculated by:

$$E_{\alpha\alpha\alpha}(i) = \frac{[\alpha\alpha\alpha_{meas}(i) - \alpha\alpha\alpha_{mod}(i)]^2}{(\alpha\alpha\alpha_{meas}(i))^2} \qquad \text{(EQ 2.10)}$$

Work has been carried out by Joe Staudinger of Compound Semiconductor Technologies that investigates the effect of changing the weighing factors on power amplifier performance predictions [5].

3.0 DC versus RF Comparisons

The characterization process outlined in sections 2.0-2.4 is quite involved. State-of-the-art measurement apparatus along with a streamlined parameter extraction program gives rise to accurate models efficiently. However the weighing factors described in section 2.4 indicate that there is room for improvement. According to the model, if there was no frequency dispersion effects, the derivatives of the DC data and the RF gm and gds should line up exactly. This is not what is observed. There are two general sets of data that should be measured to develop a complete picture of how the low frequency dispersion behaves. One is comprised of measurements on the difference between DC and RF characteristics as a function of bias, and the other is measurements on how these characteristics change with frequency. Though the latter is the main thrust of the project, a characterization of the differences between DC and RF data will clearly show the magnitude of the problem.

3.1 RF versus DC Comparisons at various bias-points

The following approach to the problem relies heavily on the existing methodology. During the extraction process, a file is generated with small-signal intrinsic gm and Rds tabulated at various extrinsic voltages. Meanwhile, DC-IV data can be taken at a fine increment of bias points.

It is important to note that the bias points tabulated in the DC data file are extrinsic Vgs and Vds. To get at an intrinsic Vgs or Vds (to calculate an intrinsic DC Gm and Rds,) the voltage drop across the parasitics must be subtracted from the extrinsic voltage. As Id is given in milliamperes, the expressions for the simple conversion to intrinsic voltages are:

$$Vgs_{int} = Vgs_{ext} - Id \cdot Rs \qquad \text{(EQ 3.1)}$$

$$Vds_{int} = Vds_{ext} - Id \cdot (Rs + Rd) \qquad \text{(EQ 3.2)}$$

A DC intrinsic Gm and Gds can then be found by numerically calculating the center derivative at each bias point. The partial derivative of Id with respect to Vgs gives Gm, and the partial derivative of Id with respect to Vds gives Gds, as indicated in Eqs. 2.5 and 2.6. Thus to find Gm, the center derivative of Id must be taken while holding Vds constant. Similarly, Vgs is held constant while calculating the derivative of Id to find Gds. Note that the method for finding Gm does not incorporate the effects of Igs, or the gate to source leakage current. The derivatives are taken using the following expressions:

$$Gm_{intrin} = \left. \frac{Id(Vgs_{int,2}) - Id(Vgs_{int,1})}{Vgs_{int,2} - Vgs_{int,1}} \right|_{Vds = constant} \quad \text{(EQ 3.3)}$$

$$Gds_{intrin} = \left. \frac{Id(Vds_{int,2}) - Id(Vds_{int,1})}{Vds_{int,2} - Vds_{int,1}} \right|_{Vgs = constant} \quad \text{(EQ 3.4)}$$

Because of the format of the RF data file, plots comparing DC and RF intrinsic gm and gds versus extrinsic voltages can be made. It would be highly impractical to plot DC and RF gm and gds versus intrinsic voltages.

Many sets of data were taken and analyzed. Presented below are the data from the final experiment comparing dispersion characteristics of devices processed by three different flows. The names given to the three are the "Process A" flow, the "Process C" flow, and the "Process E" flow. This experiment was done to see whether the dispersion showed similar characteristics across the various flows. The test conditions are outlined by the instructions given below.

1. Set Vds=4.0 v.
2. Find what Vgs is required to bring the current Id to 25 mA, 50 mA, 75 mA, and 100 mA. Let us call these Vgs1, Vgs2, Vgs3, and Vgs4.
3. Run small-signal model extractions (with Cold FET parasitic extractions). The gate-source biases to be measured are Vgs1, Vgs2, Vgs3, and Vgs4. The drain-source voltages required are Vds=1 v to Vds=9 v in one volt increments.
4. Carry out DC-Id measurements for the DC comparison. Vgs=Vgs1-0.1, Vgs1, Vgs1+0.1, Vgs2-0.1, Vgs2, Vgs2+0.1, Vgs3-0.1, Vgs3, Vgs3+0.1, Vgs4-0.1, Vgs4, and Vgs4+0.1. Vds=0.0 to 9.1 in steps of 0.1 v.

The data were taken on a 1.2 mm power implant MESFET with a lightly doped drain. The device used from the Epi wafer had a 750 μm gate length, and not a 1.2 mm gate length. Results from the analysis helped identify which devices exhibited the most amount of Gm and Rds dispersion. Figures 3.1-3.6 show overlays of DC and RF Gm and Rds with Vgs set to that Id=50 mA when Vds=4.0 v. These graphs include data taken on devices processed under the Process A flow, the Proces C flow, and the Process E flow.

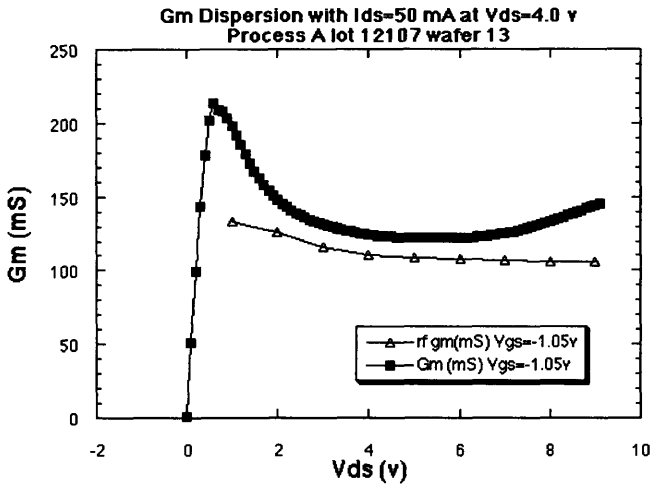

FIGURE 3.1. DC and RF Gm with Vgs set such that Id=50 mA when Vds=4.0 v. Device processed under the Process A flow.

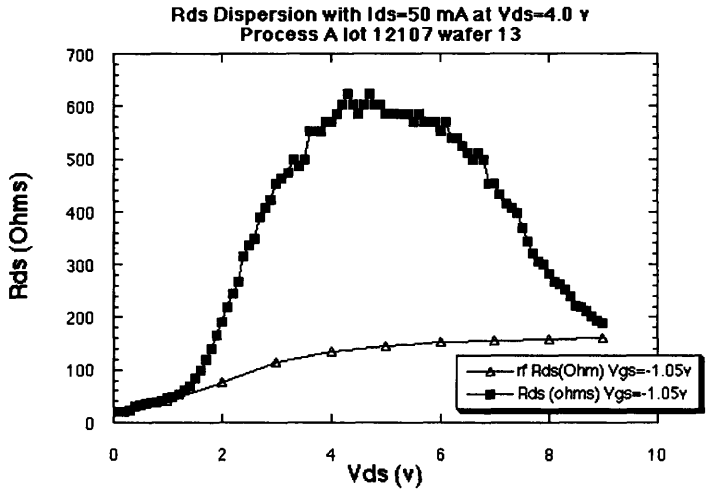

FIGURE 3.2. DC and RF Rds with Vgs set such that Id=50 mA when Vds=4.0 v. Device processed under the Process A flow.

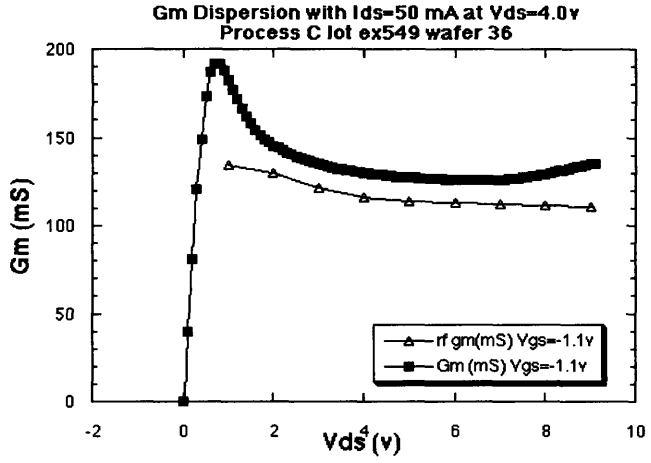

FIGURE 3.3. DC and RF Gm with Vgs set such that Id=50 mA when Vds=4.0 v. Device processed under the Process C flow.

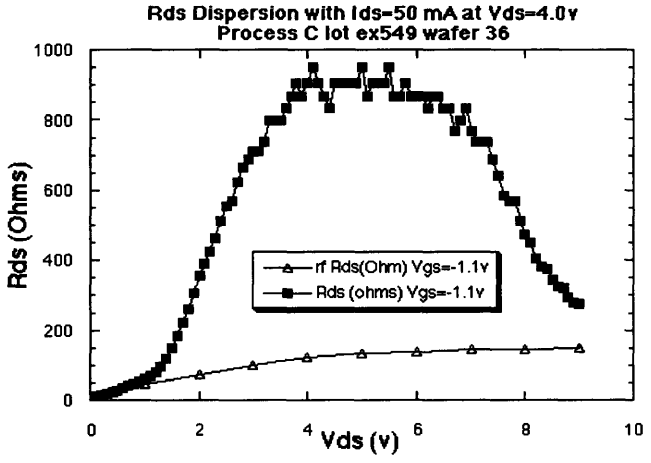

FIGURE 3.4. DC and RF Rds with Vgs set such that Id=50 mA when Vds=4.0 v. Device processed under the Process C flow.

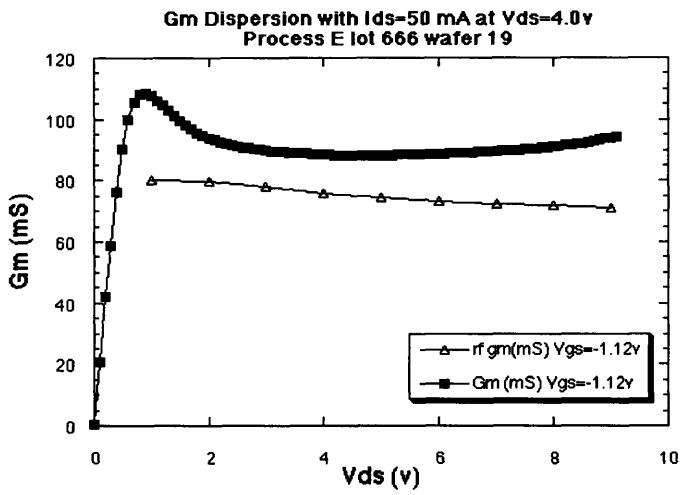

FIGURE 3.5. DC and RF Gm with Vgs set such that Id=50 mA when Vds=4.0 v. Device processed under the Process E flow.

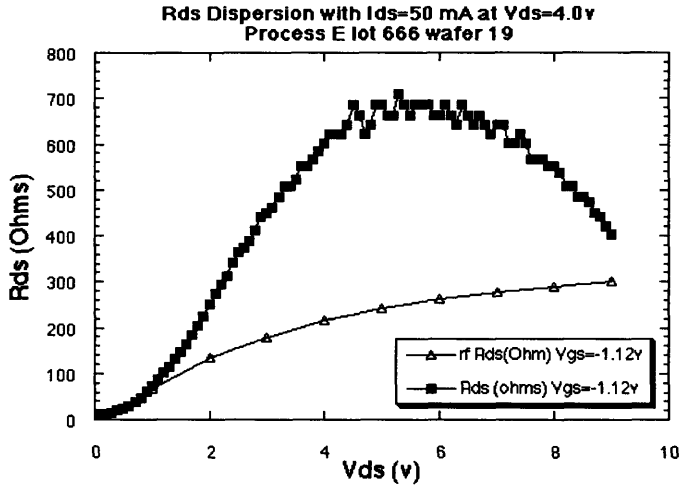

FIGURE 3.6. DC and RF Rds with Vgs set such that Id=50 mA when Vds=4.0 v. Device processed under the Process E flow.

4.0 Development of a Low Frequency S-Parameter Measurement System

The large-signal model is influenced by two forces: the DC-IV data and the RF small-signal data. Another approach to reconciling the difference between DC and RF gm and gds is to develop a small-signal model that captures the frequency dispersion effects. To generate such a model, very low frequency S-parameter data must be taken. The frequency of these measurements will range from 5 Hz to 1 MHz. Y-parameters at each frequency point may be used to give extracted circuit element values. Plotting each of these as functions of frequency will show the validity of the small-signal model, and at what frequency it begins to break down. New models may be suggested based on the measured data set.

4.1 The design of the bias-tees

However, taking S-parameter measurements at low frequencies is not trivial by any means. The HP 8751A is a vector network analyzer capable of taking measurements of reflection and transmission S-parameters at frequencies from 5 Hz to 500 MHz. One of the major hurdles of the project was to obtain clean accurate measurements from 5 Hz to 1 MHz. At 5 Hz, it is difficult to separate the DC component from the RF signal. The test ports of the 8751 allow only an RF signal with no DC bias, and so a capacitor placed between the test port and the device under test (DUT) allows RF power to pass, while protecting the analyzer from the DC voltage applied. An inductor from the DC rail to the DUT lets DC voltage to be applied, while preventing RF power from going to the DC source. This circuit is called a bias-tee, and is used in all S-parameter measurements. It is usually embedded in the internal circuitry of the analyzer. As this is not the case for the 8751, the bias-tee had to be designed fresh. The design used in this project is shown in figure 4.1.

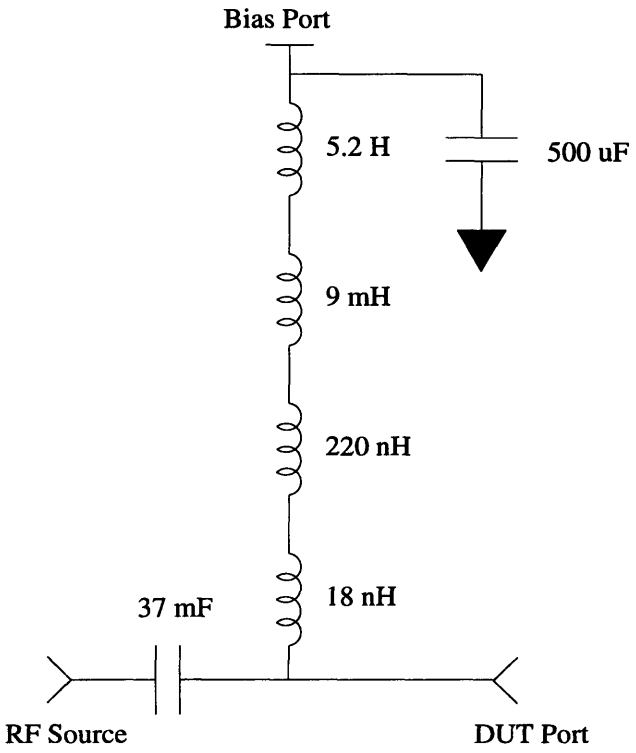

FIGURE 4.1. Diagram of the bias-tee circuit.

After many iterations on the design, the above circuit was soldered together on a micro-strip test board. The smaller inductors are placed with the intention of making the bias-tee work over a broader band of frequencies. Two bias-tees were built up, as one bias-tee is required for the gate-source port, and another is required for the drain-source port.

The main design consideration of the bias-tee focused on its functionality. At the DUT port, an AC signal superimposed on a DC bias is desired. An ideal bias-tee would not allow any AC signal to be lost to the inductors of the biasing circuitry. The capacitors should provide an AC short, and the inductors should provide a DC short. Since the inductors are made up of many windings around a ferrite core, these windings give rise to voltage drops across each inductor. These resistive losses in the inductors can be tolerated by boosting the voltage of the DC source. The performance question arises: How much AC signal is lost to the inductors? And to what extent is there an AC short from the RF source to the DUT?

The impedance offered by the bias-tee to the DUT should be 50 Ω. If the DUT is connected directly to the test set, this condition is automatically satisfied, because the test set is designed to offer a 50 Ω environment. However, at very low frequencies, the inductors do not offer signifi-

cantly more impedance compared to the test set, which could give rise to a parallel combination whose impedance is less than 50 Ω.

The HP 8751A itself serves as an ideal tool to make such an evaluation. A test set must accompany any analyzer to interface with the device under test. The 87512A/B test set is the only test set that operates at a frequency as low as 5 Hz. It has three inputs, R, A and B, and two outputs, A/R and B. R is the incident power put forth by the network analyzer, while A and B sense what power is either reflected or transmitted. The test set splits the incident power into two parts, sending half to the DUT and the other half back to the analyzer. Of the power sent to the DUT, the reflected power is sensed by A, and the transmitted power is sensed by B. The ratio of A to R is S11, and the ratio of B to R is S21. Thus only S11 and S21 can be measured simultaneously, and the device must be reversed to measure S22 and S12. Below is a table indicating the measurements that are possible in the forward or reverse direction.

TABLE 1. S-Parameter Definition and Description [8751 manual page 6-4]

S-Parameter	Measurement	Test Set Description	Direction
S11	A/R	Input reflection coefficient	Forward
S21	B/R	Forward gain	Reverse
S12	B/R	Reverse gain	Reverse
S22	A/R	Output reflection coefficient	Forward

S11 measurements were made by calibrating a short, open, and 50 Ω load to the RF port of the test set on the network analyzer. The bias-tees were then connected via BNC cables to the test set of the HP 8751A. S11 parameters were taken from 5 Hz to 1 MHz with short and open terminations at the DUT port as can be seen in figure 4.2. The DC rail was set to 0.0 v.

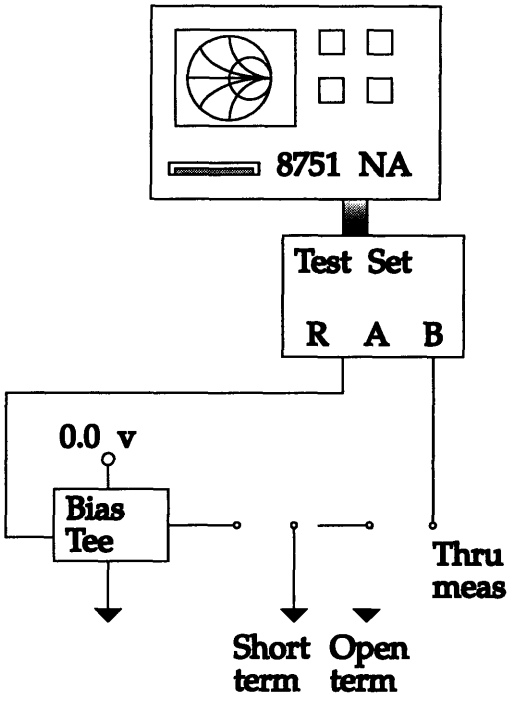

FIGURE 4.2. Measurement configuration alternatives for bias-tee evaluation.

With an open termination, the reflection coefficient, or Γ, should be 1. On a Smith chart, the measured Γ should have magnitude 1 and 0 phase. Figure 4.3 shows a plot of the measured magnitude of S11 versus frequency for the bias-tees of figure 4.1. Note that there are two curves in the graph, giving S11 data on both bias-tees. From the plots, one would expect a decent performance above 100 Hz. Below 100 Hz, the bias-tees' failure to provide an infinite impedance will give rise to loss in resolution of the measurement. In spite of this loss in resolution, accurate measurements may still be taken, as will be shown in section 4.6. The spikes resembling stalactites between 110 kHz and 130 kHz come from a resonance in the bias tees. Many inductors and capacitors were tried to optimize the performance. Placing a resistor in parallel with the large inductor serves to dampen out the resonance. The resonance spreads out over a wider bandwidth as this resistance is lowered, but the performance at low frequencies drops dramatically. The resonance frequency seems to be most directly a function of the inductance. Larger inductors cause resonances at lower frequencies.

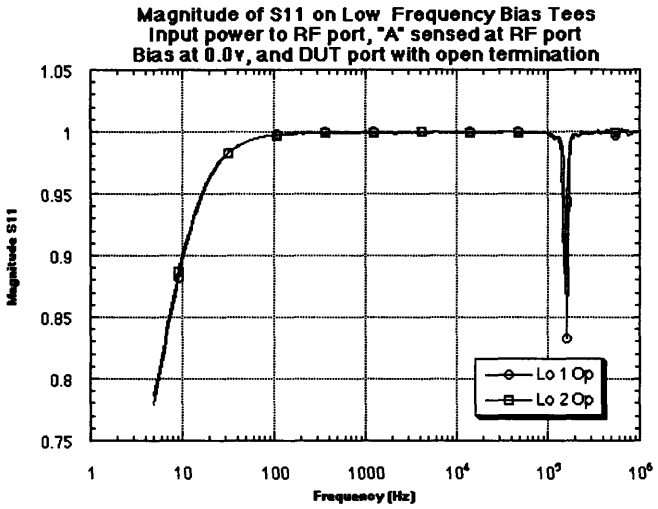

FIGURE 4.3. Magnitude of S11 measurements taken on low frequency bias-tees with an open termination.

To make measurements at higher frequencies, a second pair of bias-tees were built to operate at frequencies from 10 kHz to 1 MHz. The constraints of this second design effort were not as stringent as those of the first, especially since a medium-sized inductor will serve as a good RF choke at 10 kHz. The main difficulty was in picking an inductor that was sizeable, and yet did not cause a resonance below 1 MHz. The design is as shown in figure 4.4. The high frequency bias-tees do not offer as high an impedance as the low frequency bias-tees at frequencies below 1 kHz. Because they are not to be operated at frequencies below 10 kHz, this does not present a problem. The high frequency bias-tees do not exhibit the resonance seen in the low frequency bias-tees. There is a resonance not shown at approximately 1.5-2 MHz. However, it is just outside of the measurement band of interest, and may be ignored.

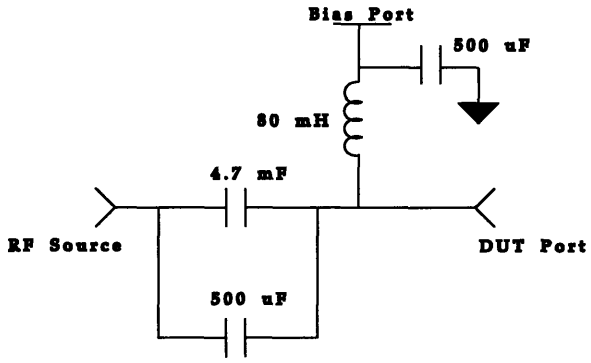

FIGURE 4.4. Circuit diagram for high frequency bias-tees.

The graph in figure 4.5 shows S11 data for both the low and high frequency bias-tees from 100 Hz to 1 MHz. The plot shows the familiar resonances in the low frequency bias-tees' data. The resonances may compensated for by a second measurement using the high frequency bias-tees.

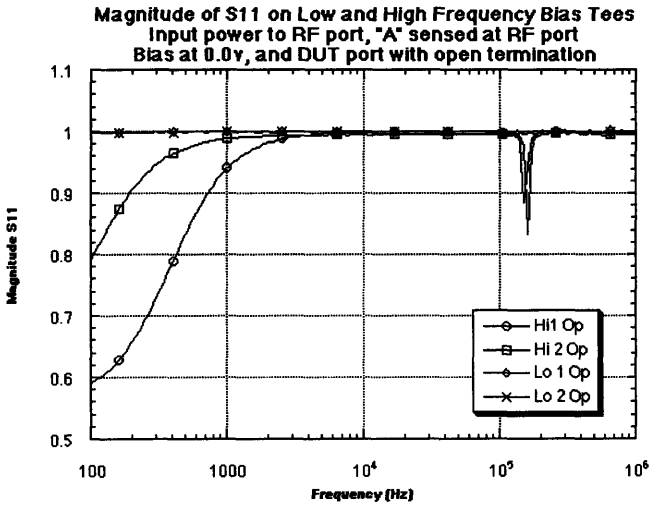

FIGURE 4.5. Magnitude of S11 measurements taken on low and high frequency bias-tees with an open termination. The low and high frequency data sets are overlaid to show the potential performance of the low and high frequency bias-tees used in tandem.

With a short termination, S11 should be -1 with no imaginary part. The RF power will be reflected as though the coupling capacitor is connected to ground. If this is not the case, one should check that good contact is established between the terminals of the capacitor and the test set. Large electrolytic capacitors are often found in aluminum cans that may be conveniently connected to a 12 gauge wire using a crimp termination. These terminations, however, are not

reliable, and can become loose easily. Even when properly connected, they give rise to 4 Ω series resistance. It is better to solder connections wherever possible, and minimize the number of connections that rely on one wire being pressed against another. Measurements taken with these considerations show that the magnitude of S11 is 0.99, but the phase changes as the reactance changes with frequency. Figure 4.6 presents a graph of the phase measured on all four bias-tees. The larger coupling capacitors give rise to measurements that have less phase difference from -180 degrees.

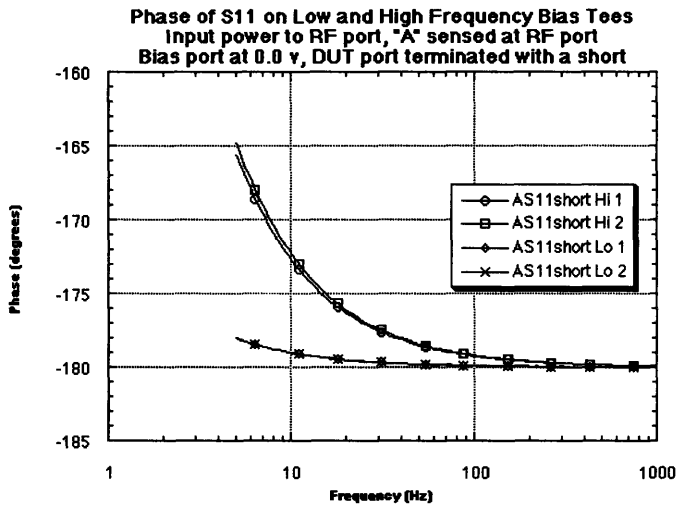

FIGURE 4.6. Phase of S11 measurements taken on low and high frequency bias-tees with a short termination.

As mentioned earlier, the DUT should be in a 50 Ω environment. When connecting any of the test ports to a device, the test set looks like 50 Ω from the perspective of the device. Connecting a bias-tee in between the test port and the device will change this environment. To measure this, the RF port of the bias-tee was terminated with a 50 Ω standard, the DC rail was once again 0.0 v, power was sent into the DUT port, and A/R was measured. This measurement may be called S22 and should be 0 in magnitude given the configuration, since a matched load will give no reflection coefficient. Figure 4.7 shows a fairly good load match for the low frequency bias-tees, and an adequate load match for the high frequency bias-tees above 10 kHz.

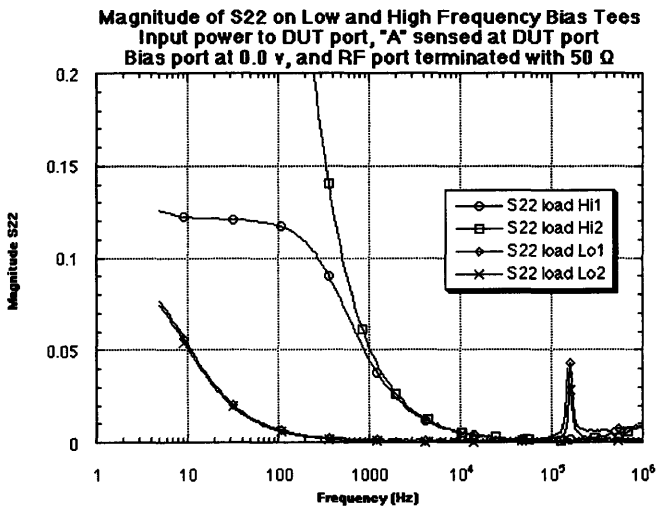

FIGURE 4.7. Magnitude of S22 measurements taken on low and high frequency bias-tees with a 50 Ω termination at the RF port.

Connecting a cable to the "B" port, and measuring S21 should give 1 with no imaginary part, indicating that all the RF power flows from the RF port to the DUT. Figure 4.8 shows the performance of the bias-tees under this test. Also, one may send the power to the DUT port of the bias-tee, sense "B" at the bias port, and terminate the RF port with a 50 Ω load. The bias-tee circuit is a three-port device, where port three is the bias port. The above measurement configuration is like measuring S32, to gauge what power is lost to the bias-tees. To be more precise, S32 would be defined as the root of the ratio of power transmitted to the bias port to the input power. Ideally, this measurement should be zero. The plots of S32 versus frequency in figure 4.9 show how close the bias-tees came to approximating this result. Both the low and high frequency bias-tees perform adequately for their respective measurement bands.

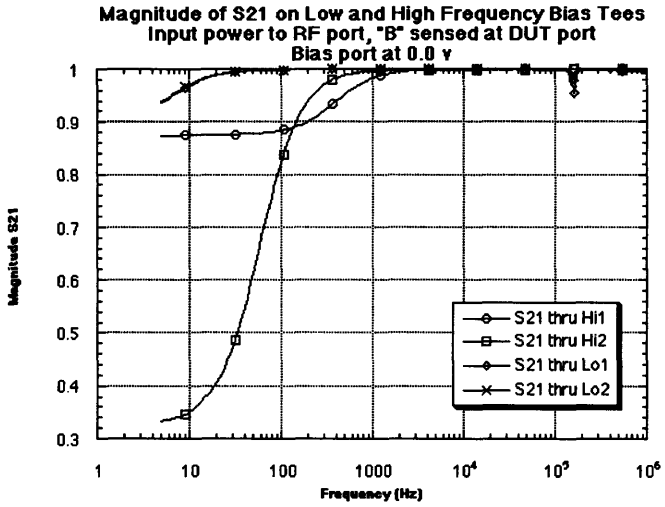

FIGURE 4.8. Magnitude of S21 measurements taken on low and high frequency bias-tees.

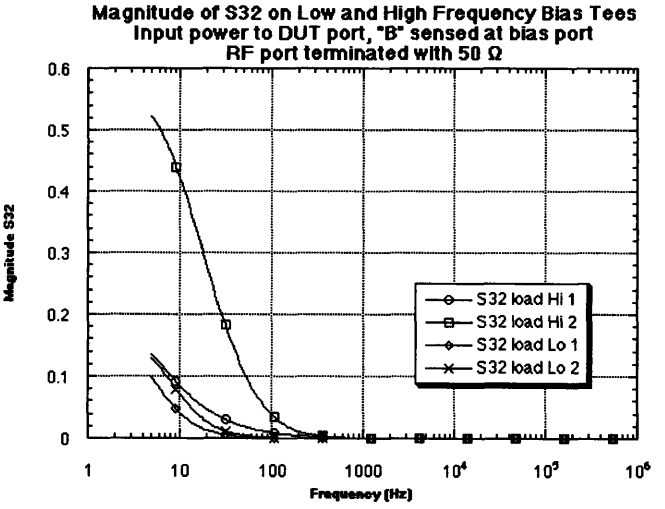

FIGURE 4.9. Magnitude of S32 measurements taken on low and high frequency bias-tees with a 50 Ω termination at the RF port.

The measurements shown above give rise to a complete characterization of the bias-tees. The non-idealities evident in the graphs may be dealt with by a two-tier de-embedding process described in section 4.4. As shown in section 4.4, the bias-tees and other measurement apparatus may be characterized in terms of an error model which can be used to isolate the device S-

parameters alone. Poor AC characteristics of the bias-tees measured alone are indicative of a poor measurement resolution once the de-embedding is complete. That was why careful attention was given to the choice of parts and the understanding of the bias-tee performance.

4.2 Incorporation of Bias-Tees to Measurement Setup

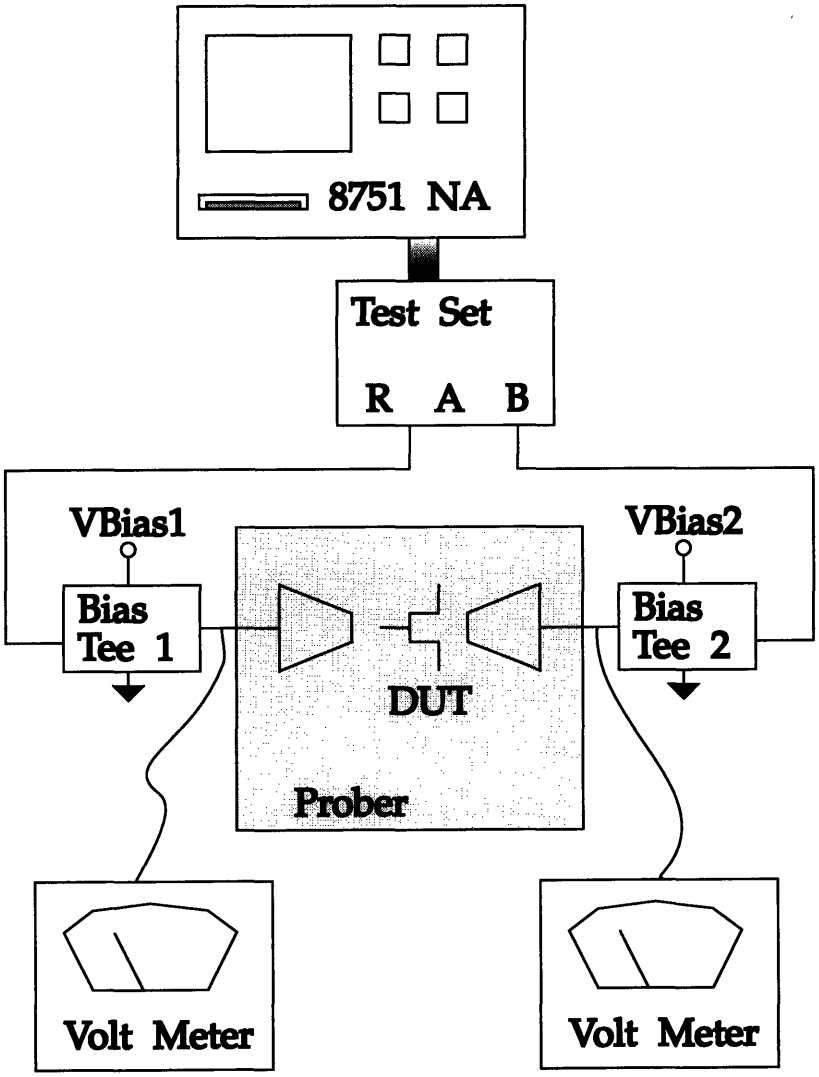

FIGURE 4.10. Measurement configuration.

The device must be biased to a desired operating point for small-signal analysis to be performed. Figure 4.10 shows a diagram of the measurement setup. The shaded region is the prober station, in which the trapezoidal shapes represent the coplanar probes. These probes have three contacts in a row, the outer two to be connected to ground. On a MESFET, these outer two would contact the source. By definition, the incident power must be sent to the gate of the

device when measuring S11 or S21, and for S22 or S12 measurements, the incident power must be sent to the drain of the device. Though it is not shown in the figure, the connections to the test set must be reversed when making the latter two measurements. Before an S-parameter measurement is taken, a 3457 multimeter is used to monitor the bias at the DUT port. The DC source is adjusted until the DUT bias settles to the desired value to within one one-hundredth of a volt. Once this is done, the multimeter is removed to reduce measurement noise. The HP 8751A is then triggered for a single sweep, and data is stored in a floppy disk.

4.3 Measurement Considerations in Using the 8751

In developing the measurement methodology for obtaining low frequency S-parameter data, there were a number of system issues, as well as network analyzer issues that had to be dealt with. These issues gave rise to corrections, and the corrections eventually led to a reliable measurement system.

4.3.1 Improving the noise floor and minimizing the effects of resonances

Having completed a calibration, one can expect a steady measurement. One can connect known standards to the DUT ports to obtain measurements referenced to the plane of the device. For measurements on one-port devices, the "S11 1-Port" calibration routine may be selected. The routine requires measurements on an open, a short and a load standard. Once the measurements on the standards have been obtained, the analyzer corrects the data so that the S11 measurement of a load has zero magnitude, which it should. In this way, the effects of all the reactances of the capacitors and inductors would be nullified. On the Smith chart, this should look like a dot at Γ=0. After eliminating some systematic errors, the return loss hovered around -60 dB. This residual magnitude of Γ is commonly termed the "noise floor" of the system.

If such a clean calibration does not come about from the standard one-port calibration routine, a few issues may be investigated before proceeding further. First, the test set must be properly grounded. The outer conductor of the test set must be connected to the ground of the analyzer. If this is not the case, measurements taken will seem random both in magnitude and phase.

Secondly, the power supply giving the rail voltage of the bias-tee should not have resonances in the measurement frequency range. There were two power sources considered: HP's digitally controlled 6628A, and the simpler knob-controlled E3610A. Setting the voltage to zero and measuring A/R into the sources revealed that the 6628A did much better at looking like an AC short. Whereas reflection measurements on the E3610A smoothly approached a Γ of -1, the 6628A had a resonance at 60 Hz and a much bigger resonance at 30 kHz. The 60 Hz resonance

comes from the AC signal that powers the 6628A, while the 30 kHz resonance is at the same frequency as the chopper converter used in setting the output voltage to the user-specified value. For these reasons, the E3610A was used. Some research groups have used car batteries for their DC sources.

The AC power outlets utilized by the components of the setup must have a good ground for an accurate measurement. The ground of the AC line that powers the network analyzer is the same ground as the measurement ground of the 8751. This ought to be the same ground as that used by DC sources or multimeters used in the setup. If all the units in the setup are not well grounded to the same potential, the potential difference between two units may seem to oscillate at a frequency of 60 Hz when connected via a BNC cable. This oscillation will appear as a resonance at 60 Hz, creating a large spike in the log magnitude plot of the measurement. Commonly known as "ground bounce," this problem may be remedied by connecting alligator clips to the chassis' of the various components, or by plugging all the units to steady power outlets. Plugging into different power outlets can also affect the level of the noise floor. Changing the outlet connection from the test bench to the wall changed the noise floor from -30 dB to -60 dB.

4.3.2 Network analyzer calibration considerations

The measurements require data calibrated to the reference plane of the coplanar probes. For a two-port measurement using this test set, the only calibration routine available is the "one path 2-port" calibration. A ceramic substrate may be obtained that has structures used in common calibration routines. The standards used in the calibration are a short, an open, a 50 Ω load, and a "thru," which simply connects one port to another. Upon completion of the routine, the analyzer requests that the device be connected for reverse measurement. Having reversed the device, the user needs to hit a button to continue. The analyzer carries out an initial sweep, and then directs the user to connect the device for forward measurement. Once the device is reversed once again, the user may obtain the specified S-parameter.

This approach is extremely impractical given the measurement configuration of figure 4.10. To reverse the device, the DC biases of both bias-tees must be brought back to 0.0 v before lifting the probes off the wafer. If this is not done, a huge build-up of charge on the probe tips can occur as the probes are lifted, causing potential damage to the analyzer. Once the probes are lifted, the wafer may be reoriented for reverse measurement, and the voltage polarity must be reversed on the bias-tees. The capacitor between the RF port and the DUT port is electrolytic, and will behave differently when reversed biased. This introduces an unsystematic error in the system. One might propose exchanging the bias-tees as the wafer is reversed to allow the gate of

the DUT to be biased by the same bias-tee. This, however, would ruin the reference plane of calibration. For an accurate measurement, the analyzer requires that the system being measured remains the same, and only the device is to be reversed.

Given the configuration of figure 4.10, there is yet another flaw in the measurement methodology set up by the one path 2-port calibration routine. The routine does not allow the user to measure the standards through both bias-tees. The measurements on the standards taken through one bias-tee are assumed to be the same as those taken through the second. The measurements shown in figures 4.5-4.9 clearly show that this is not the case.

4.4 The Two-Tier De-Embedding Process

Since the internal system of the analyzer proved inadequate for obtaining accurate data, a new approach was needed that would account for the measurement configuration of figure 4.10 and provide a good calibration to the reference plane of the probe tips. Staudinger [6] addressed this issue, and provided a number of de-embedding methodologies. In particular, Staudinger described the 12-term error model, which was used as the framework for the measurement correction.

The full two-port 12-term error model is an extension of the one-port error model. The one-port error model is concerned with the correction of one parameter, the reflection coefficient. When a measurement is made on a device through the bias-tee fixture, the data taken is a composite Γ of the fixture and the device. It is necessary to characterize the fixture across the measurement band to isolate the Γ of the device. Once the characterization of the fixture is complete, the device S11 can be calculated [6].

A signal flow graph is a convenient way to analyze systems in terms of their RF performance. It consists of branches and nodes. Each node is a variable that represents the power of an incident wave or the power of an emanating wave, and is termed an "a" node or a "b" node, respectively. Each branch is either an S-parameter or a reflection coefficient. Branches enter "a" nodes and emanate from "b" nodes. Algebraically, a node is equivalent to the sum of the branches entering it. In other words, the power of an emanating wave is calculated by considering the superposition of the incident waves scaled by the branch variables [4].

4.4.1 The one-port-error model

The one-port-error model consists of three error terms: the directivity, the source match, and the reflection tracking. Figure 4.11 shows this model in terms of a signal flow graph [8].

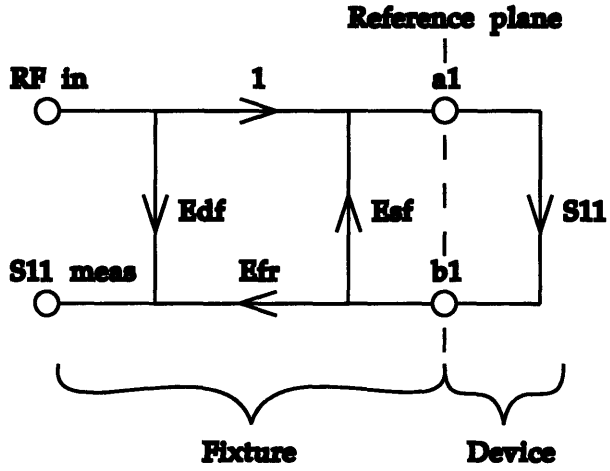

FIGURE 4.11. One-port-error model signal flow graph, including Edf, Esf, and Efr.

"RF in" is the incident power to the DUT, and S11meas is the reflected power back to the analyzer. The 8751 automatically gives S11 or A/R, by computing the root of the ratio of incident power to reflected power. For the model shown above, the equations relating a1 and b1 are as follows [6]:

$$a1 = 1 + Esf \cdot b1 \quad \text{(EQ 4.1)}$$

$$b1 = S11 \cdot a1 \quad \text{(EQ 4.2)}$$

$$S11meas = Edf + Efr \cdot b1 \quad \text{(EQ 4.3)}$$

By eliminating a1 and b1, S11meas can be found as a function of S11 and the error terms [6].

$$S11meas = Edf + \frac{Efr \cdot S11}{1 - Esf \cdot S11} \quad \text{(EQ 4.4)}$$

To obtain the error terms as functions of frequency, measurements on known standards must be taken. The above equation is then solved for Edf, Esf, and Efr. A 50 Ω load gives rise to a matched impedance condition, so S11 is 0. Measurements using this load give Edf. For a short-circuit termination, S11 is -1, and for an open-circuit termination, S11 is 1. Measurements with short and open circuit terminations provide two equations that may be solved for Efr and Esf. The results are summarized below [8].

$$Edf = S11load \quad \text{(EQ 4.5)}$$

$$Esf = \frac{S11open + S11short - 2Edf}{S11open - S11short} \quad \text{(EQ 4.6)}$$

$$Efr = \frac{-2\,(Edf - S11open)\,(Edf - S11short)}{S11open - S11short} \quad \text{(EQ 4.7)}$$

From Eq. 4.4, S11 may be solved for in terms of the error terms and S11meas [8].

$$S11 = \frac{S11meas - Edf}{Esf(S11meas - Edf) + Efr} \quad \text{(EQ 4.8)}$$

4.4.2 The two-port-error model

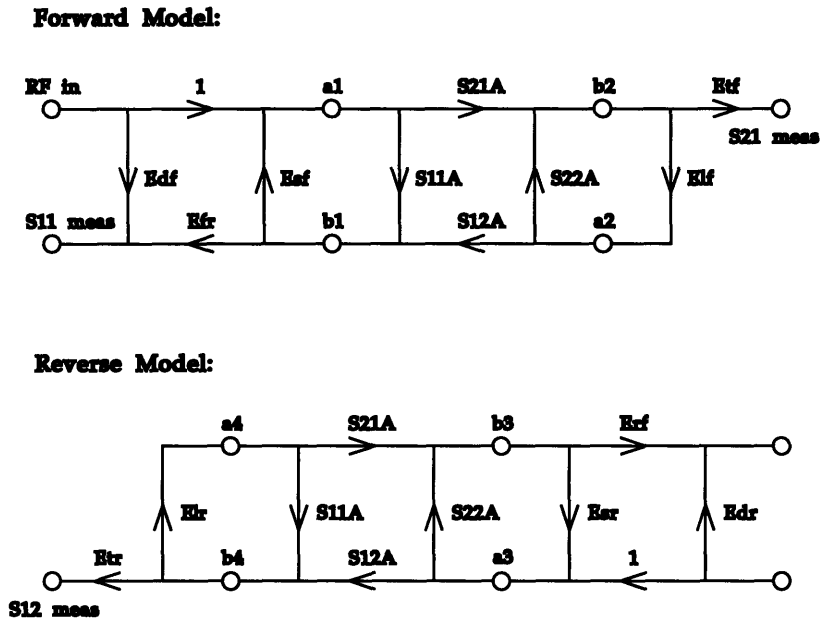

FIGURE 4.12. Signal flow graph of the two-port-error model.

The two-port-error model is made up of a forward measurement model and a reverse measurement model, as shown in figure 4.12. It has the same elements as the one-port-error model in that the directivity, source match, and load match error terms are reproduced for reverse measurement error correction. Additional terms are added to capture errors in the transmission of power and the load match of the system. Only derivations for the forward model are necessary because derivations for the reverse model are equivalent [8].

Three new terms are introduced by the two-port model. These are Etf, Elf, and Exf. Etf is known as the transmission frequency response. Elf is the load match, and Exf, which is not shown in the figure, is the isolation. The isolation is the signal picked up on B that does not go

through the device. Since it is very small at these frequencies, it has been omitted. Etf and Elf are found by measuring S11 and S21 on a "thru" standard. Eqs. 4.2 and 4.3 and the equations shown below are used [6].

$$S21meas = Etf \cdot b2 \quad \text{(EQ 4.9)}$$

$$a2 = Elf \cdot b2 \quad \text{(EQ 4.10)}$$

$$b1 = S11a1 + S12a2 \quad \text{(EQ 4.11)}$$

$$b2 = S21a1 + S22a2 \quad \text{(EQ 4.12)}$$

S11, S12, S21 and S22 for a "thru" standard are known to be 0, 1, 1, and 0, respectively. The variables a1, a2, b1, and b2 can be eliminated to give the error terms Etf and Elf [8].

$$Etf = \frac{Efr \cdot S21thru}{Efr + Esf(S11thru - Edf)} \quad \text{(EQ 4.13)}$$

$$Elf = \frac{Etf}{S21thru}\left(\frac{S11thru - Edf}{Efr}\right) \quad \text{(EQ 4.14)}$$

Once the measurements on the standards and the calculation of the error terms for each frequency data point are complete, the error terms along with the newly measured device data may be used to de-embed the device S-parameters alone [8].

$$S11A = \frac{\left(\frac{S11meas - Edf}{Efr}\right)\left[1 + \left(\frac{S22meas - Edr}{Erf}\right)Esr\right] - \left(\frac{S21meas \cdot S12meas}{Etf \cdot Etr}\right)Elf}{\left[1 + \left(\frac{S11meas - Edf}{Efr}\right)Esf\right]\left[1 + \left(\frac{S22meas - Edr}{Erf}\right)Esr\right] - \left(\frac{S21meas \cdot S12meas}{Etf \cdot Etr}\right)(Elf \cdot Elr)} \quad \text{(EQ 4.15)}$$

$$S21A = \frac{\left[1 + \left(\frac{S22meas - Edr}{Erf}\right) \cdot (Esr - Elf)\right]\frac{S21meas}{Etf}}{\left[1 + \left(\frac{S11meas - Edf}{Efr}\right)Esf\right]\left[1 + \left(\frac{S22meas - Edr}{Erf}\right)Esr\right] - \left(\frac{S21meas \cdot S12meas}{Etf \cdot Etr}\right)(Elf \cdot Elr)} \quad \text{(EQ 4.16)}$$

$$S12A = \frac{\left[1 + \left(\frac{S11meas - Edf}{Efr}\right) \cdot (Esf - Elr)\right]\frac{S12meas}{Etr}}{\left[1 + \left(\frac{S11meas - Edf}{Efr}\right)Esf\right]\left[1 + \left(\frac{S22meas - Edr}{Erf}\right)Esr\right] - \left(\frac{S21meas \cdot S12meas}{Etf \cdot Etr}\right)(Elf \cdot Elr)} \quad \text{(EQ 4.17)}$$

$$S22A = \frac{\left(\frac{S22meas - Edr}{Erf}\right)\left[1 + \left(\frac{S11meas - Edf}{Efr}\right)Esf\right] - \left(\frac{S21meas \cdot S12meas}{Etf \cdot Etr}\right)Elr}{\left[1 + \left(\frac{S11meas - Edf}{Efr}\right)Esf\right]\left[1 + \left(\frac{S22meas - Edr}{Erf}\right)Esr\right] - \left(\frac{S21meas \cdot S12meas}{Etf \cdot Etr}\right)(Elf \cdot Elr)} \quad \text{(EQ 4.18)}$$

4.5 The Measurement Methodology

The measurement methodology applies the error models, using measurements on the standards along with the device data. Measurement and analyzer issues have been taken into consideration

in developing the following methodology. Figure 4.10 illustrates the setup, and may be used in conjunction with the instructions below.

1. Set up the bias-tees and the measurement configuration using BNC cables.
2. Configure the analyzer in the following manner: the input source power is at -15 dB, the IF bandwidth is at "auto," there is a log sweep on the frequency, the sweep time is at "auto," and the start and stop frequencies are at the limits of the frequency range. If averaging is desired, set it to "on" at this time. This may be done for the higher frequency data collection, since the sweep time defaults to 0.7 seconds.
3. Run a preliminary calibration. On channel 1, do a one-port S11 calibration, and on channel 2, carry out the thru response calibration.
4. Measure and store S11 data (channel 1) on the load, short, and open standards on the calibration substrate through one bias-tee. Then repeat by measuring through the other bias-tee, being careful to reconnect the bias-tees to the test set. Even the cables are a part of the fixture to be characterized, and so the same cable must be used with a given bias-tee for both the measurement and the calibration procedures.
5. By putting the analyzer to a dual channel display mode, S11 and S21 may be measured simultaneously. Collect S11 and S21 on a thru standard, and then reconnect the cables to measure S22 and S12 on the same thru standard.
6. Identify the specific device to be measured on the wafer, and place the probes on it. Make sure that there is no residual charge in the coupling capacitors by shorting the two leads of the capacitors. The DC sources supplying DC voltages to the bias-tees must be at 0.0 v.
7. Put the analyzer trigger on "hold," so that it does not send any RF power to the bias-tees. Then proceed to adjust Vgs and Vds by adjusting the knobs of the DC sources. The voltages at the ports of the DUT should be monitored by the 3457 multimeter. Once the voltages have been set, disconnect the multimeters to reduce noise.
8. Measure S11 and S21. After reversing the cables, it may be necessary to check and readjust the DC bias before measuring S22 and S12. The large inductor cores will very likely have different resistances.
9. Using the twelve newly collected data sets, calculate the error terms, and use Eqs 4.15-4.18 to de-embed the device data.

The data analysis was carried out using Mathcad on a Macintosh PC. Mathcad has the flexibility to handle complex number arithmetic conveniently.

4.6 Test-Circuits to Test Validity of Measurement Methodology

Two test circuits were built to test the validity of the measurement methodology in terms of its accuracy. To minimize the analysis required in de-embedding from S-parameters to element values, simple networks made up entirely of resistors and capacitors were used. Measurements on these circuits helped identify problems in the measurement methodology. For example, if a

resistor value did not de-embed to the expected value, the S-parameters could be checked. If S22 did not agree well with the expected value, the bias-tee connected to port 2 could be inspected for a loose connection. Secondly, these measurements helped outline the limits of uncertainty in the data. When a measurement is done well, the test results show an accuracy to within 1% of the expected values for the frequencies above 12 Hz.

4.6.1 T-resistor network

The first circuit used was a simple T-resistor network. As shown in figure 4.13, three resistors form a T. From DC measurements on a 3457 multimeter, R1 was 149.9 Ω, R2 was 33.0 Ω, and R3 was 46.5 Ω. Two sets of S-parameter data were taken. The low frequency bias-tee was used in measurements from 5 Hz to 100 kHz, and the high frequency bias-tee was used in measurements from 10 kHz to 1 MHz.

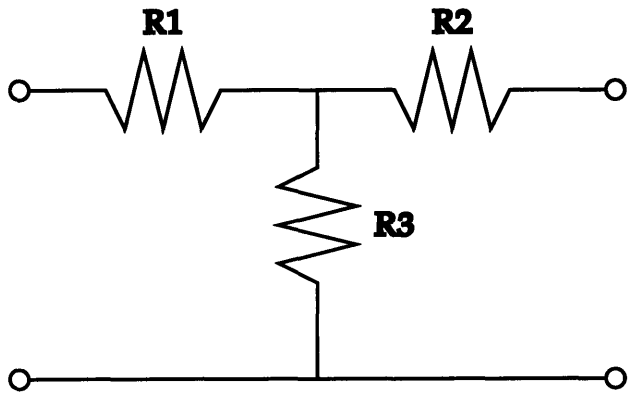

FIGURE 4.13. Tee resistor network used in testing the measurement system.

The extraction proved successful as can be seen from figures 4.14-4.16. The low and high frequency data are plotted together to show the continuity of the measurement. The spike in the measurement at 60 Hz comes from the AC line that powers the analyzer. The slight discontinuities around 1KHz come from the analyzer's adjusting its mixing bandwidth to measure at the higher frequency range.

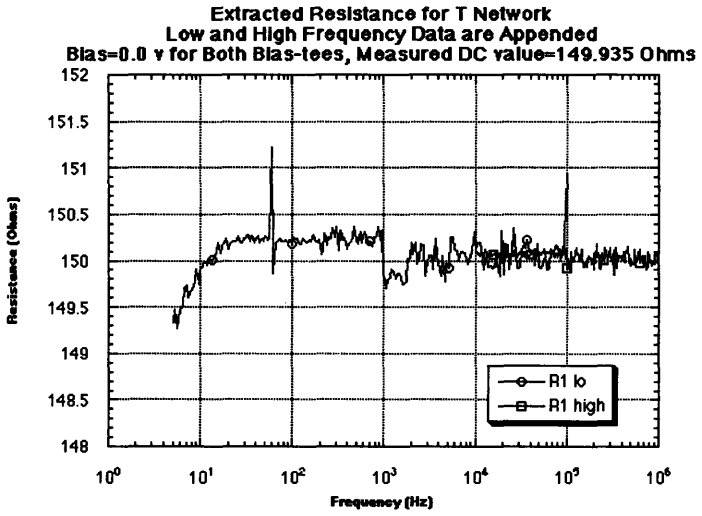

FIGURE 4.14. Extracted resistance from T-resistor network. DC measured R1=149.9 Ω

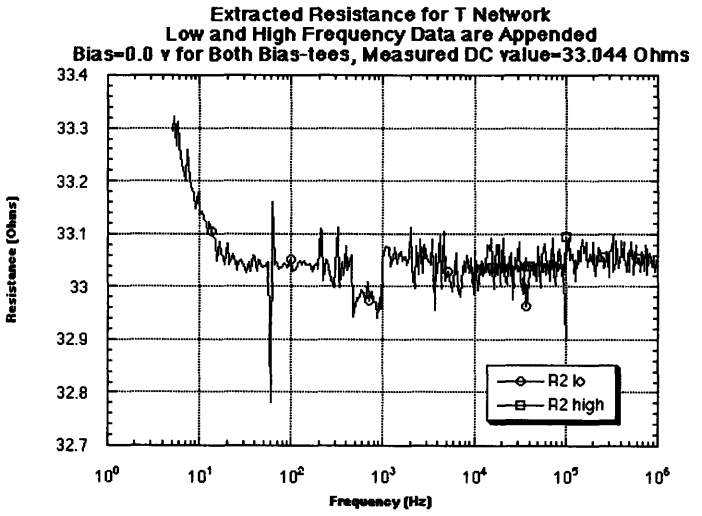

FIGURE 4.15. Extracted resistance from T-resistor network. DC measured R2=33.0 Ω

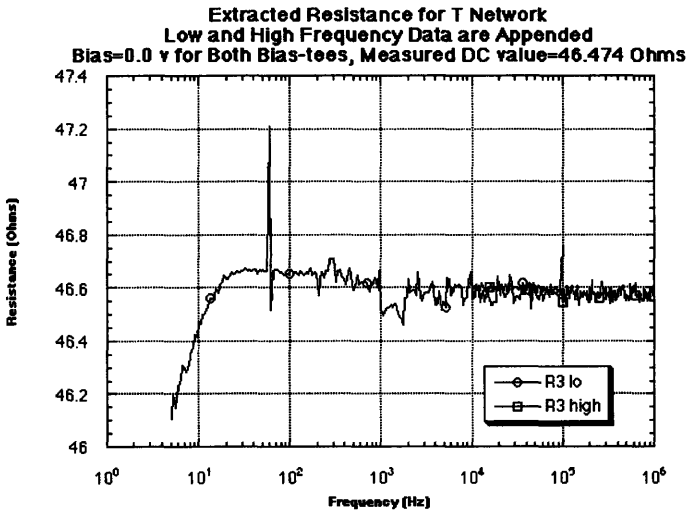

FIGURE 4.16. Extracted resistance from T-resistor network. DC measured R1=46.5 Ω

4.6.2 π-network using capacitors

With the resistor network, only resistances could be measured. To test the system's ability to measure capacitances, a second circuit was soldered together on a microstrip board. As shown in figure 4.17, there are two capacitors and one resistor put in a π formation.

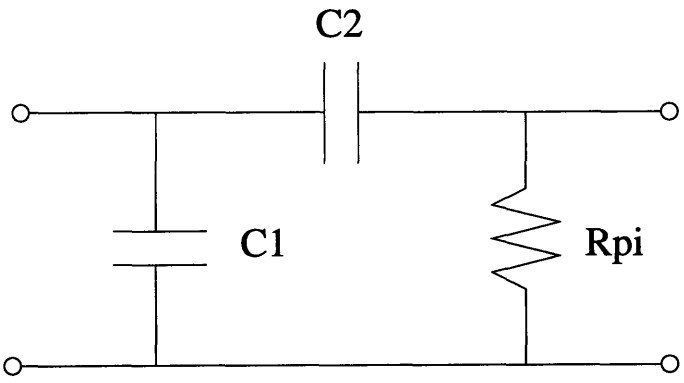

FIGURE 4.17. Pie network circuit diagram. This circuit was used to test the reactance extraction capability of the measurement system.

Accurate estimates of the element values were required to get the calculated S-parameters versus frequency. The DC value of Rpi was found to be 99.6 Ω. To find values for C1 and C2, measurements on a 4284 LCR meter were tried. However, the measured values were strongly a function of the frequency of oscillation. Higher capacitances were measured at lower frequen-

cies. Since only one value was required, an alternative approach that employed a fitting process and a basic model for the capacitor was used.

Each capacitor was modeled as a capacitor and a resistor in parallel, both in series with another resistor. The element values for the model were chosen to fit a separate set of data measured on the two capacitors C1 and C2. Each were mounted on a test board so that the negative terminal was connected to ground. Initial guesses were placed for the three elements of the model. Using the element values along with the frequencies selected for measurement, the modeled impedance was calculated at all frequencies. This modeled complex impedance was converted to the modeled complex reflection coefficient, Γ. The difference between the modeled and measured S11 were summed over all frequencies to give the net error, as shown below.

$$error = \sum_{frequency} [Re(S11meas) - Re(S11modeled)]^2 + [Im(S11meas) - Im(S11modeled)]^2 \qquad \text{(EQ 4.19)}$$

Using the solver in Excel, the net error as shown above could be minimized by changing only the element values of the model. C1 was found to be 91.0 nF and C2 was found to be 878.8 nF. The parallel and series parasitic resistances were either too small or too large to add any meaningful information to the model.

Using circuit analysis and the values extracted above, S-parameters were calculated from the circuit model. The modeled versus measured S-parameters show how well the system deembeds the reactances. As may be seen in figures 4.18-4.20, the calculated and measured S-parameters show good agreement.

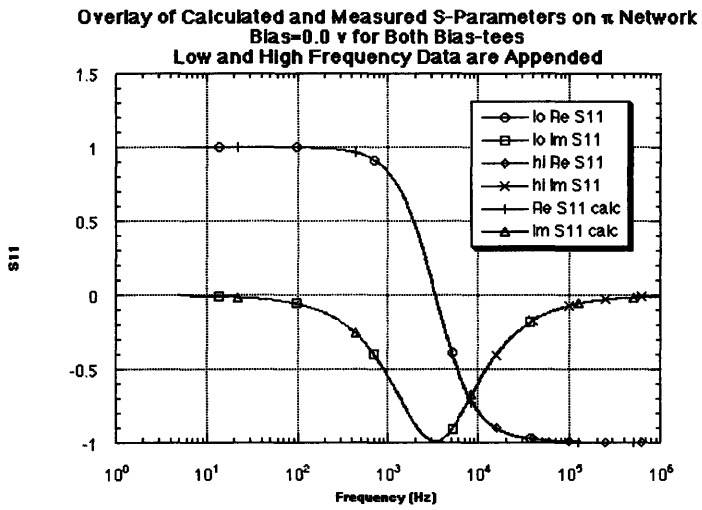

FIGURE 4.18. Measured and modeled S11 on π network.

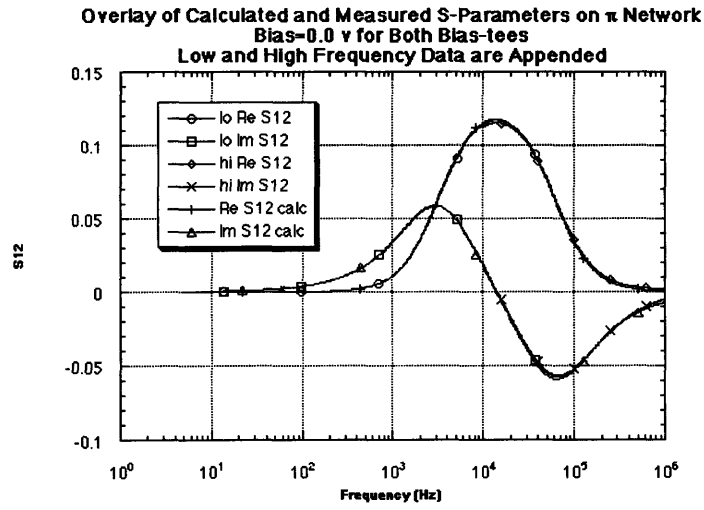

FIGURE 4.19. Measured and modeled S12 on π network.

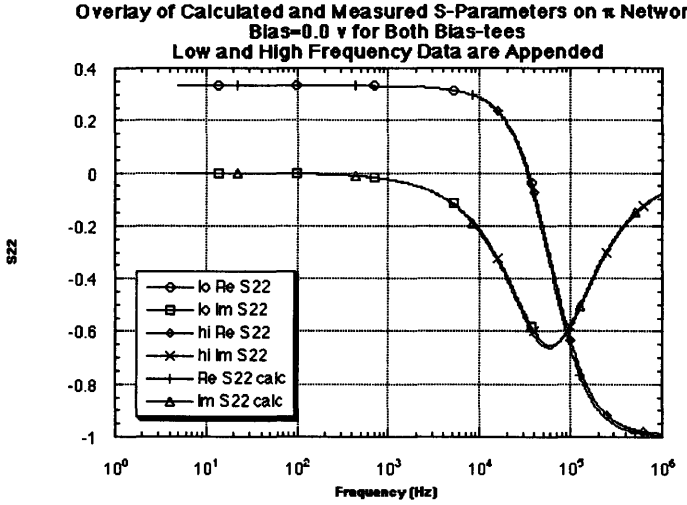

FIGURE 4.20. Measured and modeled S22 on π network.

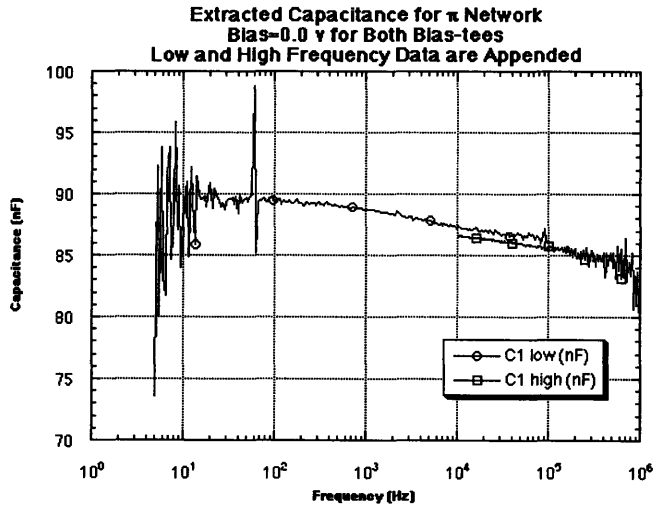

FIGURE 4.21. Extracted capacitance from π network. Measured C1=91.025 nF

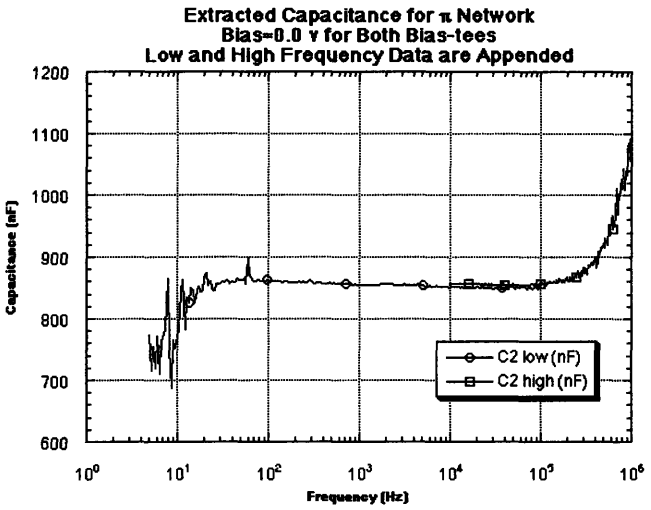

FIGURE 4.22. Extracted capacitance from π network. Measured C2=878.78 nF

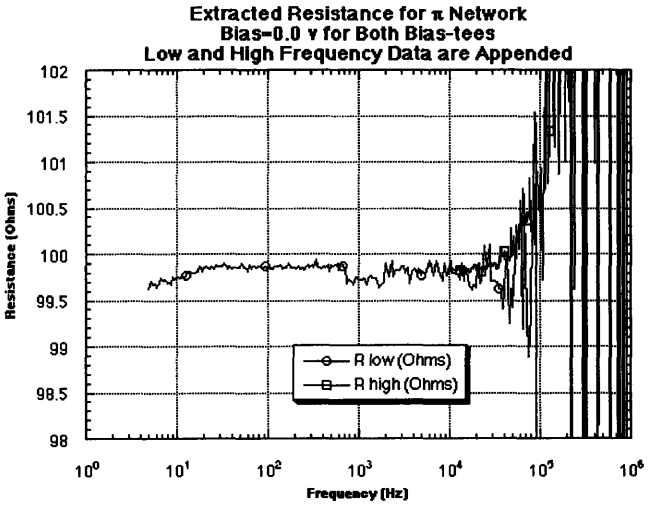

FIGURE 4.23. Extracted resistance from π network. Measured Rpie=99.645 Ω

Since the circuit is easily de-embedded from the Y-parameters, the S-parameters are converted to Y-parameters. The de-embedded element values are shown in figures 4.21-4.23. Good agreement with expected values is achieved between 12 Hz and 30 kHz. At 30 kHz, the capacitors do not offer much impedance as compared to Rpie. In spite of the analyzer's ability to measure S-parameters to within one one-thousandth of a unit, the resistor cannot be determined from the high frequency data. At 17.5 kHz, the magnitude of impedance offered by the smaller capacitor

equals that of the resistor, which is roughly the frequency at which the extraction of Rpi begins to fail. The extractions of C1 and C2 also begin to fail at these frequencies for the same reason.

While measuring GaAs MESFET's, it is important to remember that energy storage elements may only be extracted at frequencies at which their impedances are not too large or too small.

4.7 Measurement Accuracy

The measurement methodology of section 4.5 used in conjunction with the two-tier de-embedding process can generate accurate two-port S-parameter data from 12 Hz to 1 MHz. Random errors due to noise or slight differences in the connections between measurement sweeps give rise to an uncertainty of 2-3%. Below 12 Hz, the non-idealities in the bias-tee performance limit the resolution of the de-embedding, which eventually limits the accuracy of the extraction of small signal element values. To improve the overall accuracy of the measurement methodology, several narrow-band bias-tees may be used may be used in different frequency ranges. An operational amplifier may be employed to greatly amplify the effective inductance of the RF choke, which could lead to a high-performance low-frequency bias-tee. For the purposes of this project, the measurement accuracy of the system is adequate to perform meaningful modeling of low-frequency dispersion effects in GaAs MESFET's.

5.0 Measured Device Data

5.0.1 Network parameter data collection

Using the measurement methodology described above, two sets of data were collected using each pair of bias-tees. The low-frequency bias-tees were used for measurements taken at frequencies from 5 Hz to 100 kHz. The high-frequency bias-tees were used correspondingly from 10 kHz to 1 MHz. Processed under the Process C flow, the device to be measured was a 1.2 mm by 1.1 μm power FET, in which the gate was made up of eight 150 μm fingers. Each gate finger was sized to a width of 150 μm and a length of 1.1 μm. On the mask set available, there were three 1.2 mm devices to choose from, where each had a different amount of separation between the SiO_2 spacer and the N+ drain region. This separation is known as the "Lightly doped drain" region, or "LDD" region, and was formed for improved breakdown voltages. One device had 0.0 μm separation, another had 0.5 μm separation, and the last had 1.0 μm separation. This last device was chosen for measurement, because it was expected to show more low frequency dispersion than the other two. Subsequent process to its formation steps may cause damage to the LDD region, which can produce an abundance of surface states that may trap electrons travelling from the source to the drain. This is the phenomena that is conventionally attributed to give rise to low-frequency dispersion.

The bias points chosen for measurement are listed in the table below:

TABLE 2. Listing of bias points used for low frequency S parameter measurements.

	Vgs=-1.0v, Vds=2.0v	
Vgs=-0.8v, Vds=3.0v	Vgs=-1.0v, Vds=3.0v	Vgs=-1.2v, Vds=3.0v
	Vgs=-1.0v, Vds=4.0v	
Vgs=-0.8v, Vds=5.0v	Vgs=-1.0v, Vds=5.0v	Vgs=-1.2v, Vds=5.0v
	Vgs=-1.0v, Vds=6.0v	

5.0.2 DC extrinsic output resistance and transconductance data

To add one final data point at a very low frequency, DC data was taken for comparison with the de-embedded S-parameter data. For the calculation of DC small-signal characteristics, current-voltage data was measured on the same device as that described in section 5.0.1. Vgs and Vds were set to each of the bias points listed above. To obtain a center derivative, each Vgs0 bias was accompanied by Vgs0+0.1 v and Vgs0-0.1 v. The same was done in setting Vds. To ensure all transients had died away before data was collected, the measurement system had a 10 second delay before measuring Id.

For a proper comparison DC versus RF data, the parasitic elements of the small-signal model should be considered. At low frequencies, the small parasitic inductances may be ignored, and the method shown in section 3.1 would suffice. However, the parasitic resistances are also ignored in this analysis. As suggested by Eq. 3.2 of section 3.1, DC Rds extractions are inaccurate by an additive factor of approximately 3-5 Ω, or the sum of Rd and Rs. This is insignificant compared to the extracted values of 900-1000 Ω. Gm extractions are more strongly affected by ignoring the parasitic resistances. Because of the transconductance, there is a voltage gain across the parasitic resistances. This voltage gain gives rise to a more significant error in the intrinsic voltage calculation of Eq. 3.1. However, the parasitic elements were ignored in the analysis of the low-frequency de-embedded data as well. The DC data shown in the table below may only be used as a check to observe Rds and Gm at an extremely low frequency (DC). As will be explained in section 5.2, the disparities between the DC data points and the lowest frequency extractions do not give rise to a meaningful comparison.

TABLE 3. DC extrinsic output resistance and transconductance.

Vgs (v)	Vds (v)	Gm (mS)	Rds (Ohms)
-0.8	3.0	118.78	851.28
-0.8	5.0	119.7	856.90
-1.0	2.0	91.86	670.60
-1.0	3.0	93.53	966.99
-1.0	4.0	94.84	1265.82
-1.0	5.0	96.55	992
-1.0	6.0	98.43	937.74
-1.2	3.0	55.09	1519.88
-1.2	5.0	59.27	1626.84

5.1 Measured Y-Parameter Device Data

The low and high frequency data were appended so that a continuity may be observed between the two sets. Shown in figure 5.1 are the real and imaginary parts of Y11 and Y12. Because the magnitude of the admittance is very small, no meaningful circuit modeling of the input is possible. Hence, for the purposes of this project, the gate-source and gate-drain junctions will be modeled as open circuits. The standard Cgs and Cgd capacitances may be added later with the help of higher frequency data for a complete small-signal intrinsic FET model.

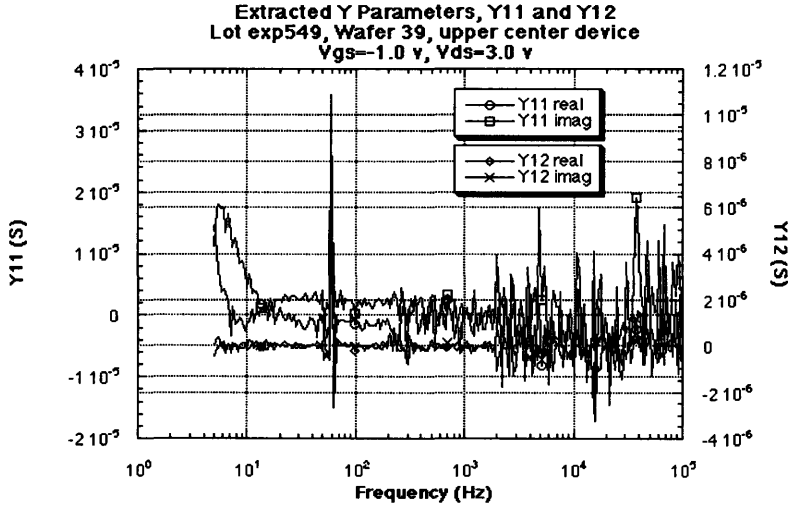

FIGURE 5.1. Measured Y11 and Y12 versus frequency at Vgs=-1.0 v, and Vds=3.0 v.

Figures 5.2-5.3 show the measured frequency dependence of Y21 and Y22. Y21 seems to settle to its final value at approximately 100 Hz. Y22, on the other hand, gradually approaches 7.5 mS at 100 kHz. Other bias points behaved similarly, but with different limiting values.

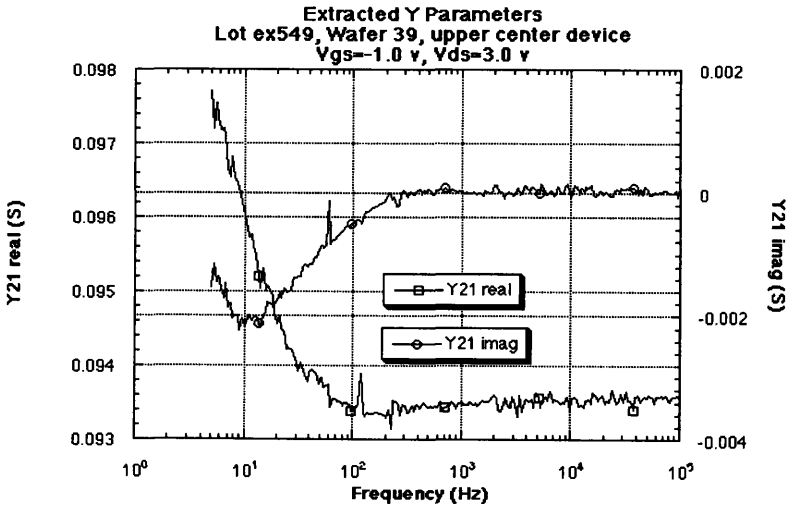

FIGURE 5.2. Measured Y21 versus frequency at Vgs=-1.0 v, and Vds=3.0 v.

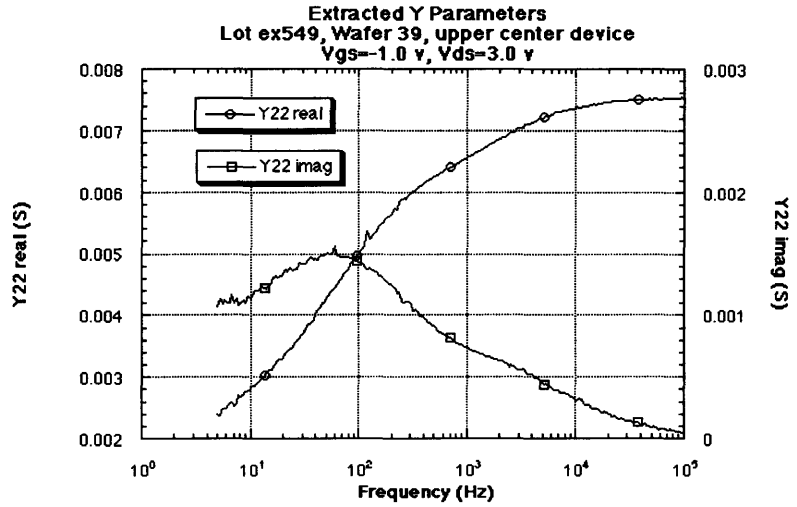

FIGURE 5.3. Measured Y22 versus frequency at Vgs=-1.0 v, and Vds=3.0 v.

5.2 Small-Signal Characteristics

A rudimentary model was used in analyzing the Y-parameters to obtain the small-signal element values. This model is shown in figure 5.4.

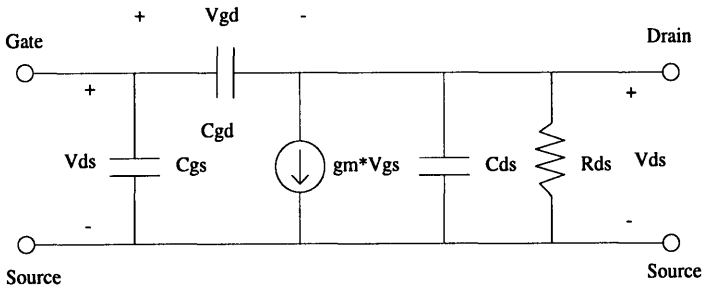

FIGURE 5.4. Small signal model used for analysis of measured data.

Once the Y-parameters have been obtained, the element values of the model above may be found using the following equations.

$$Cgd = \frac{-1}{\omega} Im(Y12) \qquad \text{(EQ 5.1)}$$

$$Cgs = \frac{1}{\omega} Im(Y11 + Y12) \qquad \text{(EQ 5.2)}$$

$$Rds = \frac{1}{Re\,(Y22 + Y12)} \quad \text{(EQ 5.3)}$$

$$Cds = \frac{1}{\omega} Im\,(Y22 + Y12) \quad \text{(EQ 5.4)}$$

$$gm = |Y21 - Y12| \quad \text{(EQ 5.5)}$$

Cgs and Cgd need not be plotted as mentioned above. Figures 5.5-5.6 show plots of extracted transconductance. Each graph has Vds held to a fixed value, either 3 volts or 5 volts. Vgs is varied between -0.8 v, -1.0 v, and -1.2 v. When the FET is more on, the transconductance shows greater dispersion. As may be seen in figures 5.7-5.8, the data also show an enormous output capacitance at the lower frequencies. This capacitance does not level off to a fixed value as the frequency is lowered. Rds does not change much at frequencies above 10 kHz. Below 10 kHz, Rds steadily climbs, and continues to climb at 10 Hz.

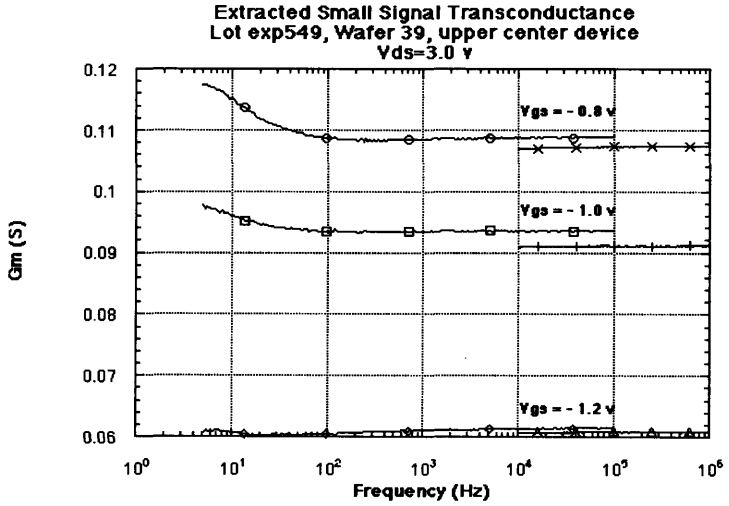

FIGURE 5.5. Measured transconductance versus frequency.

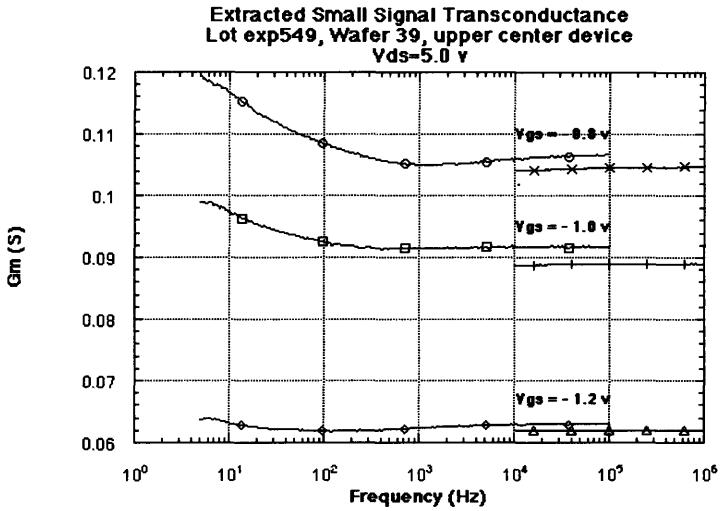

FIGURE 5.6. Measured transconductance versus frequency.

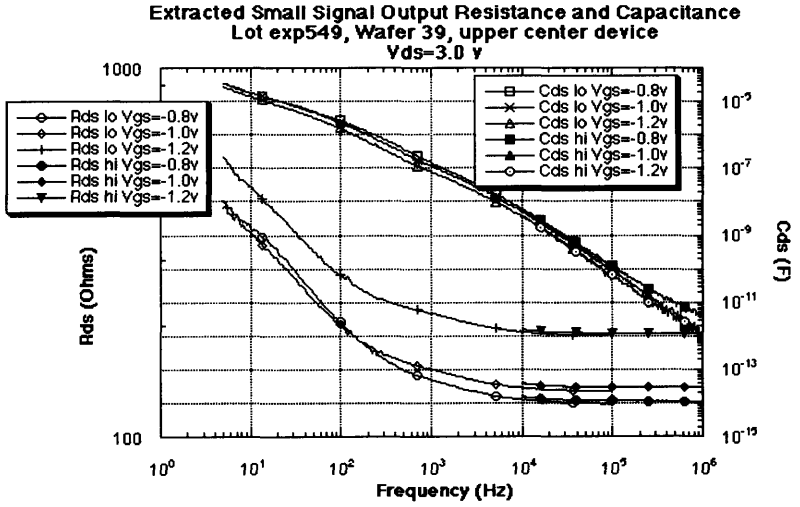

FIGURE 5.7. Measured output resistance and capacitance versus frequency.

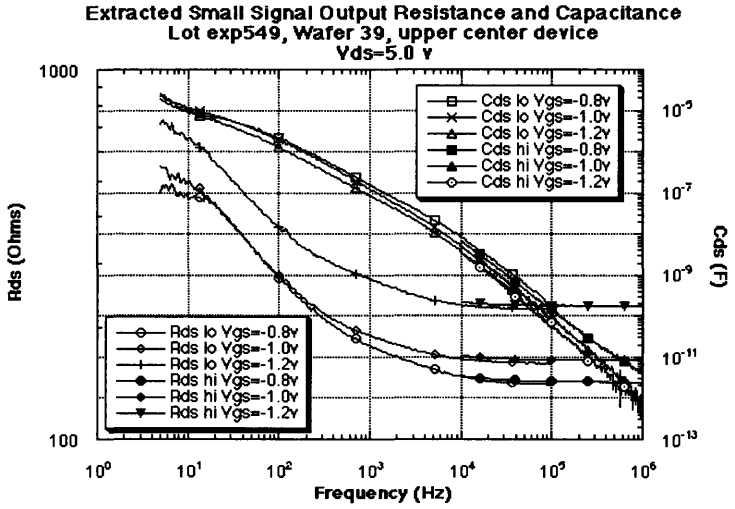

FIGURE 5.8. Measured output resistance and capacitance versus frequency.

Figures 5.9-5.11 show gm, Rds and Cds plotted with Vgs constant at -1.0 v, and Vds varied from 2 v to 6 v. The low and high frequency gm do not seem to lie on top of each other very well. This can be accounted for by the fact that the two sets of data were not taken at the same time. Though many precautions were taken in establishing the measurement methodology to ensure accuracy of data, the slight discontinuity in gm measurements seems to indicate that there is a 2-3% uncertainty in the data.

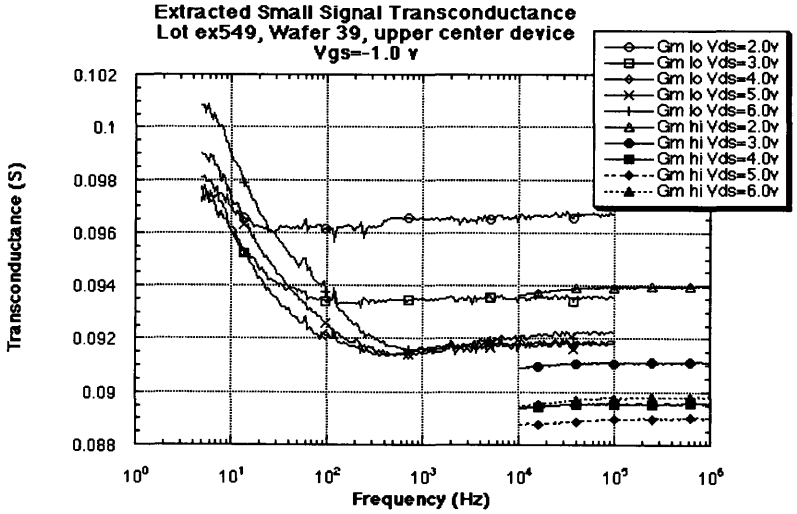

FIGURE 5.9. Measured transconductance versus frequency.

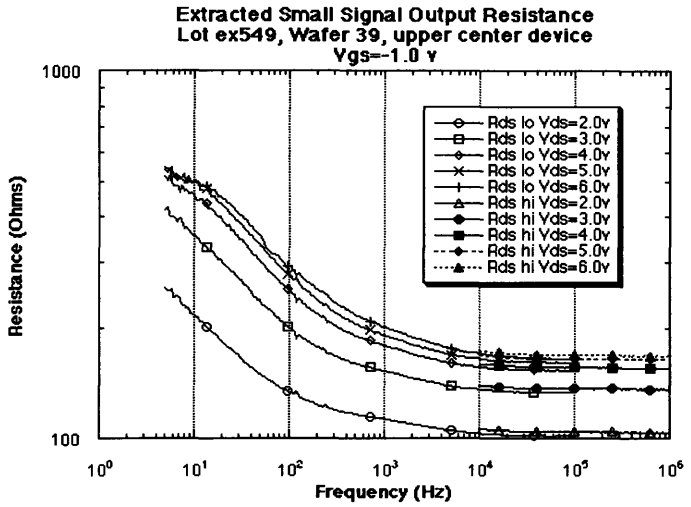

FIGURE 5.10. Measured output resistance versus frequency.

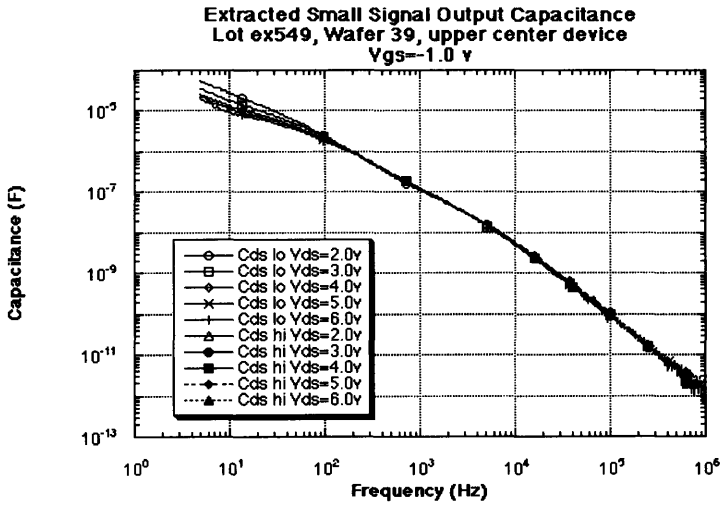

FIGURE 5.11. Measured output capacitance versus frequency.

For clean modeling with good agreement between predicted and measured performance, the data should be continuous, showing clear trends in output resistance and transconductance. The data taken with the high frequency bias-tee does not show appreciable dispersion of gm and Rds between the frequencies of 10 kHz and 1 MHz. The low frequency data should be sufficient, as it reaches a maximum frequency of 100 kHz.

The DC data presented in section 5.0.2 will not be combined with the low frequency extractions to add a DC point to be used in modeling. One may try to approximate the DC data by extrapolating Rds back in frequency. However, one can only guess the roll-off frequency. Secondly, the DC transconductance does not agree with the lowest frequency extracted transconductance. At some bias points, the DC gm is less than even the high frequency gm. It has been suggested that there may be a resonance phenomenon at work here, in which gm starts at the DC point, reaches some maximum, and then drops until it reaches its RF value at 1 kHz. For the modeling carried out in this project, only the data set taken with frequencies ranging from 5 Hz to 100 kHz will be used.

6.0 Modeling of Measured Data

Three models were evaluated in terms of their ability to capture the measured characteristics. Golio [1], proposed the first model, and the other two were developed during this study. These will be referred to as "Model #1" and "Model #2." Each of the three are based on a drop in output resistance and transconductance from DC to RF frequencies. The data used to extract model element values were the low frequency data taken at Vgs=-1.0 v, and Vds=5.0 v.

For a given measurement, there are three basic characteristics to observe: the lowest frequency data point, the highest frequency data point, and the shape of the plot as frequency is varied from the lowest frequency to the highest frequency. The extraction of circuit element values relies on each of these three. To establish a nomenclature, the lowest frequency data point will be called the DC data point, and the highest frequency data point will be called the RF data point. The DC data will be the extracted Gm and Rds at 5 Hz. The two may be called GmDC and RdsDC. Since neither the transconductance nor output resistance change appreciably above 100 kHz, the RF values of these quantities will be those extracted at 100 kHz. These will be called GmRF and RdsRF. Finally, to capture the frequency dependence, some intermediate data points at 15 and 97 Hz will be used.

6.1 Golio Model

The model used for analysis is a simpler version of the one presented by Golio [1]. Whereas Golio included parasitics and capacitances like Cds, the model shown in figure 6.1 has only elements that can be measured using the low frequency data set. Cgs is on the order of picofarads, and will not be accurately extracted at low frequencies. These elements may be added in for a complete modeling of the FET when high frequency data is taken.

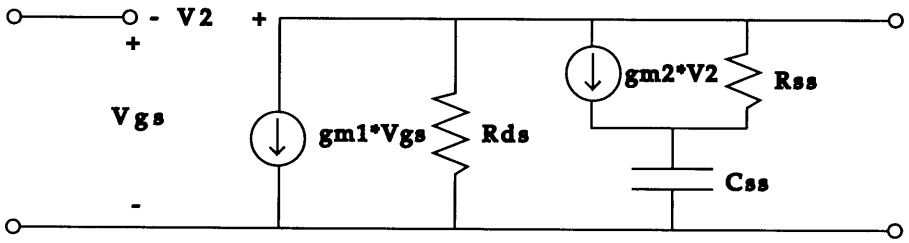

FIGURE 6.1. Small-signal model proposed in Golio's paper

As described in Golio's paper, the second current source (gm2*V2) is to reproduce a current injection mechanism into the trapping states along the channel, be they surface states, interface

states, or deep levels in the epitaxial layer. The voltage driven current source gm2 depends on v2 or equivalently -Vgd, instead of Vgs. To allow charge conservation by simulators under DC conditions, the current source is accompanied by a resistance Rss. Rss may be considered an attempt at modeling the injection impedance the charge experiences in going into the trapping states. Lastly, Css models the charge storage phenomenon of these trapped electrons. The Y-parameters may be derived by circuit analysis of the above model. Y11 and Y12 are both zero, because there is no coupling between the gate and the source, and between the gate and the drain. Y21 and Y22 are expressed as follows [1].

$$Y21 = gm1 - gm2\left(\frac{j\omega RssCss}{1 + j\omega RssCss}\right) \quad \text{(EQ 6.1)}$$

$$Y22 = \frac{1}{Rds} + \frac{j\omega Css\,(1 + gm2Rss)}{1 + j\omega RssCss} \quad \text{(EQ 6.2)}$$

The extractions of gm1, gm2 and Rds are simple, and are described below. Under DC conditions, the transconductance is gm1, and the output resistance is Rds. At 100 kHz, the transconductance is gm1-gm2.

$$gm1 = GmDC \quad \text{(EQ 6.3)}$$

$$gm2 = gm1 - GmRF \quad \text{(EQ 6.4)}$$

$$Rds = RdsDC \quad \text{(EQ 6.5)}$$

The product gm2*Rss is typically many orders of magnitude greater than 1 in Eq. 6.2. When this is the case, the Y22 will increase with the same frequency response as the drop in Y21. Rss and Css together account for an RC time constant that describes this frequency response. The product Rss*Css should be set so that the modeled frequency response of gm and Rds closely follows the measured data. One may change either Rss or Css, and so Golio suggests that Css should be set to Cgs+Cds so that all the capacitances of the model may be of similar orders of magnitude. Then Rss may be adjusted appropriately [1]. From previous analysis of the same variety of FET's of the same lot, Css was roughly approximated to be 1300 fF.

Many approaches may be taken in the extraction of Rss. Y21, Y22, and their real and imaginary parts may all be solved to give Rss. If only Y21 information is considered, a good fit of the transconductance data is obtained, but the output resistance is not well modeled. On the other hand, when Y22 data is used, the frequency response of modeled gm does not correctly reproduce the measured data. Because the DC and RF values of the transconductance are well predicted regardless what RC time constant is chosen, the real part of Y22 was used in extracting Rss with the following expression.

$$Rss = \frac{-1}{2}\left[\frac{\omega CssRds + \sqrt{K}}{\omega Css \cdot (1 - Rds \cdot Re(Y22) + Rds \cdot gm2)}\right] \quad \text{(EQ 6.6)}$$

where K is defined as

$$K = (\omega CssRds)^2 + 4Rds(gm2Rds(Re(Y22)) + 2Re(Y22) - gm2 - Rds(Re(Y22))^2) - 4 \quad \text{(EQ 6.7)}$$

6.2 Proposed Model #1

The first proposed model was designed to fit the measured data, both in terms of the transconductance and the output resistance. As may be seen from figure 6.2, two capacitors were used to capture two distinct frequency responses. Cr1, for transconductance dispersion, and Cout for output resistance dispersion. At DC, Cout looks like an open circuit, so that the output resistance will be the sum of Rr1 and Rrf. At higher frequencies, only Rrf will be the output resistance. The second current source, gmr2, depends on the voltage across the capacitor Cr1. This voltage will drop at higher frequencies, creating the desired Gm dispersion.

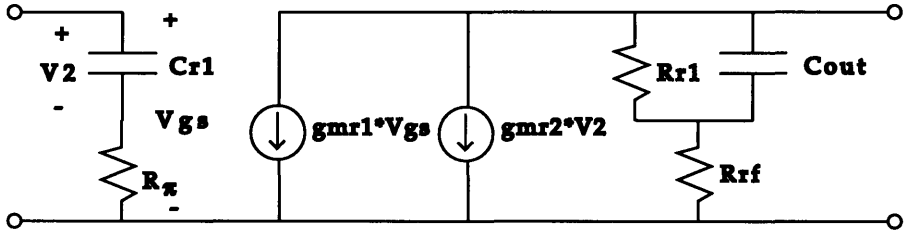

FIGURE 6.2. Circuit diagram of Small-Signal Model #1

With this model, Y11 is non-zero. The admittance of the series combination of Cr1 and Rπ must be considered when selecting this model. However, by making Rπ very large, this admittance will not be measured by any standard S-parameter measurement system. Moreover, it will not appreciably affect the accuracy of simulations of power amplifier circuit designs. For the modeling exercise of this project, Rπ was set to 1 MΩ. Circuit analysis gives rise to the following Y-parameters.

$$Y11 = \frac{j\omega Cr1}{1 + j\omega R\pi Cr1} \quad \text{(EQ 6.8)}$$

$$Y12 = 0 \quad \text{(EQ 6.9)}$$

$$Y21 = gmr1 + \frac{gmr2}{1 + j\omega R\pi Cr1} \quad \text{(EQ 6.10)}$$

$$Y22 = \frac{1 + j\omega Rr1\,Cout}{Rr1 + Rrf + j\omega Rr1\,RrfCout} \quad \text{(EQ 6.11)}$$

Cout may be solved algebraically in terms of an intermediate data point of Y22. The frequency of the data point selected was 97.56 Hz. The value of Cr1 can be solved in a similar fashion to fit the frequency response of Y21. The frequency selected was 10.51 Hz, as the data shows a dramatic roll-off in Gm at this frequency. The extraction was carried out using the following expressions.

$$Rrf = RdsRF \quad \text{(EQ 6.12)}$$

$$Rr1 = RdsDC - Rrf \quad \text{(EQ 6.13)}$$

$$gmr1 = GmRF \quad \text{(EQ 6.14)}$$

$$gmr2 = GmDC - gmr1 \quad \text{(EQ 6.15)}$$

$$Cr1 = Re\left[\frac{1}{j\omega R\pi}\left(\frac{gmr2}{Y21 - gmr1} - 1\right)\right] \quad \text{(EQ 6.16)}$$

$$Cout = Re\left[\frac{1}{j\omega Rr1}\left(\frac{Y22 \cdot Rr1}{1 - Rrf \cdot Y22} - 1\right)\right] \quad \text{(EQ 6.17)}$$

6.3 Proposed Model #2

The second model proposed is an extension of Golio's original model, in that the structure is very similar. However, there are two capacitors, Cgm and Crd, so that both the transconductance and output resistance dispersion may be fitted to measured data. The small-signal model is shown in figure 6.3.

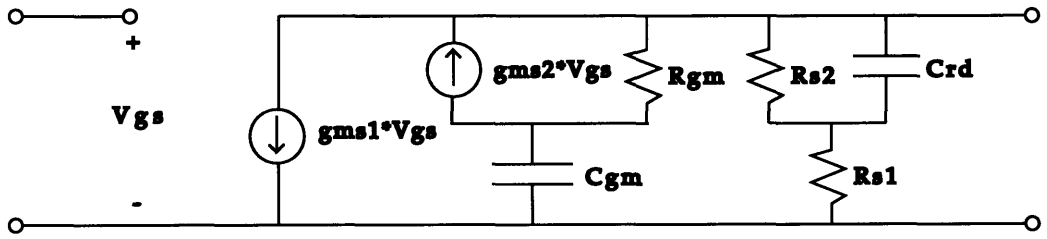

FIGURE 6.3. Small-Signal Model #2

Y11 and Y12 for the above circuit are both zero. Y21 and Y22 are given below:

$$Y21 = gms1 - gms2\left(\frac{j\omega RgmCgm}{1 + j\omega RgmCgm}\right) \quad \text{(EQ 6.18)}$$

$$Y22 = \frac{j\omega Cgm}{1 + j\omega RgmCgm} + \frac{1}{Rs1 + \dfrac{1}{\dfrac{1}{Rs2} + j\omega Crd}} \quad \text{(EQ 6.19)}$$

As may be seen from the expression for Y22, Cgm and Rgm play a role in the modeled output resistance. But once Rs1, Rs2, and Crd have been extracted, Rgm may be set to 100*(Rs1+Rs2), so that its effect on the output resistance is minimized. The following expressions provide the circuit element values of Model #2.

$$gms1 = GmDC \quad \text{(EQ 6.20)}$$

$$gms2 = gms1 - GmRF \quad \text{(EQ 6.21)}$$

$$Rs1 = RdsRF \quad \text{(EQ 6.22)}$$

$$Rs2 = RdsDC - Rs1 \quad \text{(EQ 6.23)}$$

$$Rgm = 100\,(Rs1 + Rs2) \quad \text{(EQ 6.24)}$$

$$Cgm = Re\left[\frac{j}{\omega Rgm\left(1 - \dfrac{gms2}{gms1 - Y21}\right)}\right] \quad \text{(EQ 6.25)}$$

$$Crd = Re\left[\frac{1}{j\omega}\left[(X^{-1} - Rs1)^{-1} - \frac{1}{Rs2}\right]\right] \quad \text{(EQ 6.26)}$$

where X is defined as follows

$$X = Y22 - \frac{j\omega Cgm}{1 + j\omega RgmCgm} \quad \text{(EQ 6.27)}$$

6.4 Summary of Extracted Small-Signal Circuit Element Values

Presented below is a table of the extracted element values for each of the three models. As a general rule, the capacitance values should not be of markedly different orders of magnitude, as some simulators may have difficulty achieving convergence. To reproduce low frequency dispersion effects in simulation, time-consuming simulations must be carried out to capture the long time constants of the RC networks.

TABLE 4. Extractions on 1.2 mm by 1.1 μm device biased at Vgs=-1.0 v, Vds=3.0 v.

Golio Model		Model #1		Model #2	
Element	**Value**	**Element**	**Value**	**Element**	**Value**
gmg1 (S)	0.09901	gmr1 (S)	0.09187	gms1 (S)	0.09901
gmg2 (S)	0.00714	gmr2 (S)	0.00714	gms2 (S)	0.00714
Rds (Ω)	545.286	Rπ (Ω)	$1*10^{6}$	Rs1 (Ω)	160.633
Rss (Ω)	$7.15436*10^{8}$	Rrf (Ω)	160.633	Rs2 (Ω)	384.653
Css (F)	$1.3*10^{-12}$	Rr1 (Ω)	384.653	Rgm (Ω)	$5.45286*10^{4}$
		Cr1 (F)	$9.19653*10^{-9}$	Crd (F)	$8.97856*10^{-6}$
		Cout (F)	$9.09421*10^{-6}$	Cgm (F)	$1.68655*10^{-7}$

6.5 Model Evaluations with Measured Data

As described in section 6.4, the circuit element values are extracted from the Y-parameters. Once the extractions are complete, modeled Y-parameters may be calculated to compare with the measured Y-parameters. Furthermore, these modeled Y-parameters may be analyzed in the same way as the measured data to give measured versus modeled transconductance, output resistance, and output capacitance. The measured data set used was that taken from 5 Hz to 100 kHz, with Vgs=-1.0 v, and Vds=5.0 v.

6.5.1 Evaluation of measured versus modeled Y-parameters

Figures 6.4 and 6.5 show plots of the measured and the modeled values of real and imaginary parts of Y21. The modeled Y21 from Models 1 and 2 lie right on top of each other and seem to capture the measured data reasonably well. This comes about because the frequency response was captured using the same intermediate data point, namely, the S-parameters at 15 Hz. Moreover, both models have a very similar approach in modeling the transconductance dispersion. The Golio model correctly approximates the endpoints of the measured transconductance, but seems to poorly reproduce the frequency response. The only degree of freedom for getting the frequency responses of Gm and Rds is the product Rss*Css. As discussed above, Rss was eventually set by the real part of Y22 for a reasonable fit on Rds. It is not surprising that the frequency response does not closely follow that of the measured Y21.

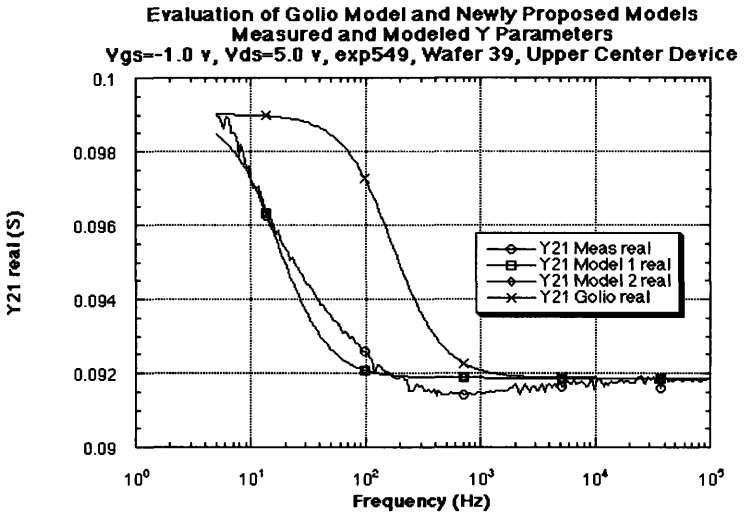

FIGURE 6.4. Measured and modeled real part of Y21. Vgs=-1.0 v and Vds=5.0 v.

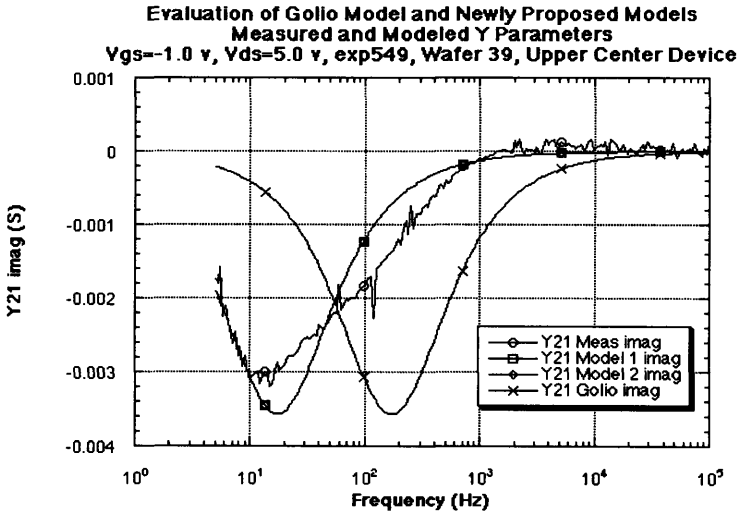

FIGURE 6.5. Measured and modeled imaginary part of Y21. Vgs=-1.0 v and Vds=5.0 v.

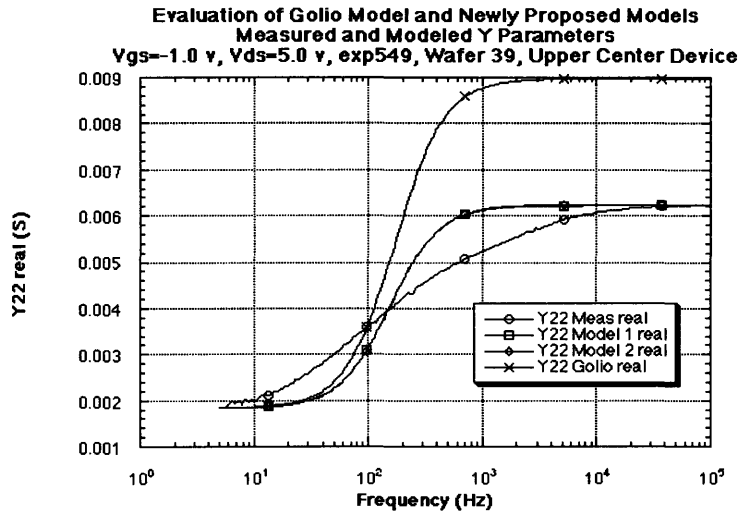

FIGURE 6.6. Measured and modeled real part of Y22. Vgs=-1.0 v and Vds=5.0 v.

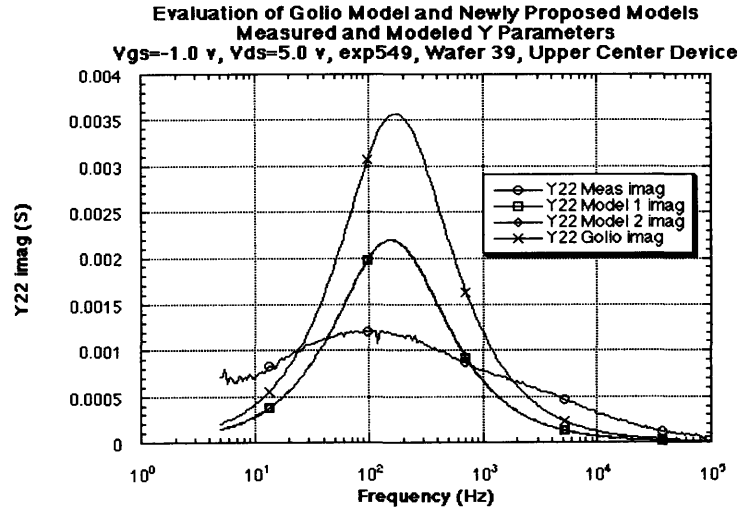

FIGURE 6.7. Measured and modeled imaginary part of Y22. Vgs=-1.0 v and Vds=5.0 v.

Shown in figures 6.6 and 6.7 are the measured and the modeled values of real and imaginary parts of Y22. The endpoints of the real part of Y22 are well modeled by models 1 and 2. Models 1 and 2 seem to predict the same results on Y22 because of their striking similarities at the output. The imaginary part of Y22 is not closely captured by any model. This requires more work.

6.5.2 Evaluation of measured versus modeled small-signal characteristics

The basic model of figure 5.4 was used in evaluating the modeled Y-parameters in terms of small-signal characteristics. Figure 6.8 shows plots of the measured and modeled transconductance. This graph is very similar to the plots of Y21 measured and modeled versus frequency in figure 6.4.

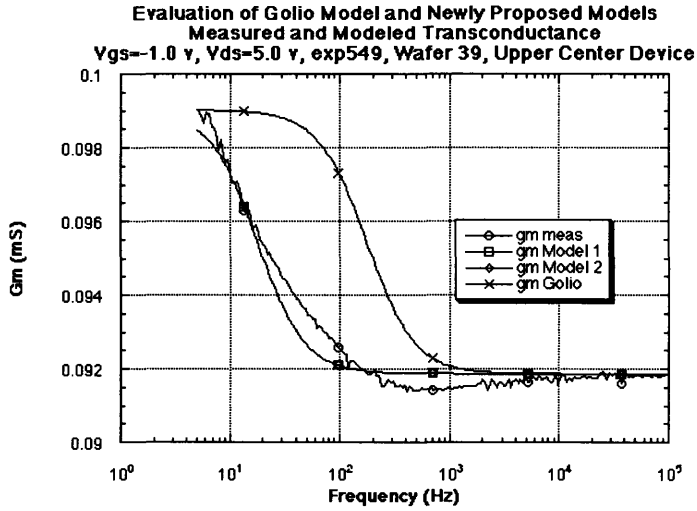

FIGURE 6.8. Measured and modeled transconductance. Vgs=-1.0 v and Vds=5.0 v.

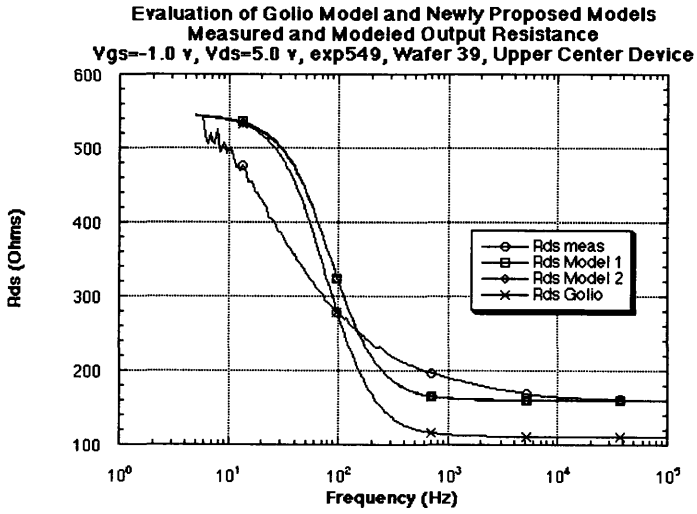

FIGURE 6.9. Measured and modeled output resistance. Vgs=-1.0 v and Vds=5.0 v.

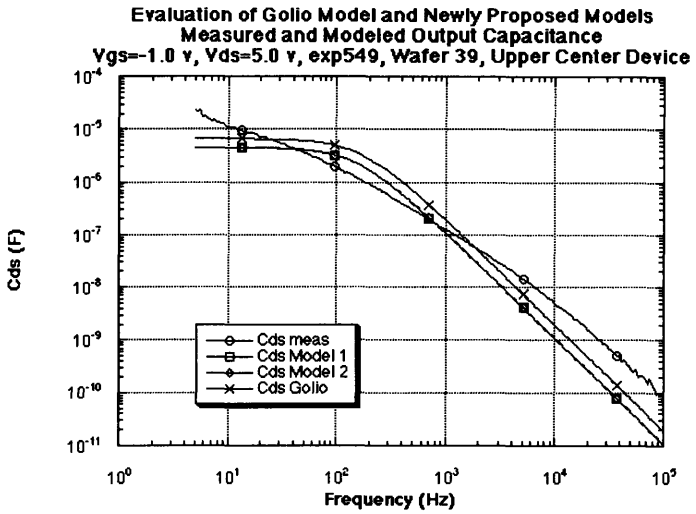

FIGURE 6.10. Measured and modeled output capacitance. Vgs=-1.0 v and Vds=5.0 v.

Figures 6.9and 6.10 show plots of the measured and modeled output resistance, Rds, and output capacitance, Cds. The fits on Rds are similar, not surprisingly, to those of the real parts of Y22 in figure 53. For the data set chosen, RdsDC was 545.3 Ω and RdsRF was 160.6 Ω. The Golio model fails to reproduce RdsRF because RdsRF is not considered in the model extraction process described in section 6.1. The models show distinct roll-off frequencies in Cds at 100 Hz. The measured Cds does not seem to have a clear roll-off frequency in the frequency range measured. As suggested by the modeled and measured imaginary parts of Y22, more work is needed in modeling Cds at low frequencies.

Models 1 and 2 have the flexibility to capture the frequency responses of both Gm and Rds, which allows for better fits to the measured data. The Golio model correctly predicts transconductance dispersion, however the output resistance is not well matched. The approach taken in the development of models 1 and 2 was to design a circuit that reproduces a drop in Gm and Rds with increased frequency. The results of these two models agree with the measured values reasonably well.

7.0 Concluding Remarks

In trying to capture the behavior of a non-linear device such as a GaAs MESFET, there are four main issues that must be faced. As illustrated in figure 7.1, they are characterization, parameter extraction, modeling and validation. First, extensive measurements must be carried out to learn how the device behaves. Then, salient characteristics may be documented by the process of parameter extraction. These parameters must be consistent across an extraction over a large number of similarly processed FET's. The parameter values may then be compiled into a model that attempts to reproduce the measured characteristics. Given that the differences between modeled and measured device characteristics have been minimized, the model should be validated by circuit simulation. Weaknesses or inaccuracies in any one of these steps will lead to problems in the production of a new component.

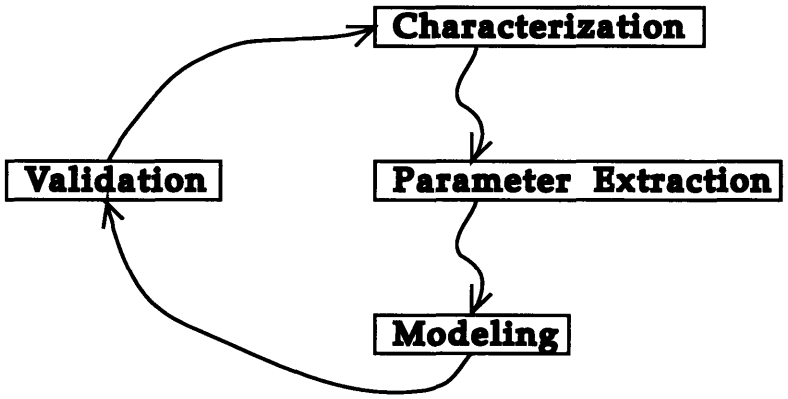

FIGURE 7.1. Diagram of characterization and modeling issues.

This project focused primarily on the characterization and measurement of low frequency dispersion. The extent of the low frequency dispersion found in GaAs MESFET's for power applications could be illustrated by comparing the DC and RF data at a number of bias points. How the electrical characteristics change from the DC to the RF endpoints is given by plotting the frequency response at a given bias point. However, collecting reliable accurate S-parameter data proved to be the most difficult part of the project. Supporting circuitry, along with a method for de-embedding the device S-parameters alone were implemented. Test circuits were used to determine the accuracy of the measurement methodology. Once all the problems with the data collection were eliminated, measurements on one device at many bias points were taken. These measurements suggested improvements in the existing models that addressed low frequency

dispersion. Two new models were proposed and compared with an existing model in terms of their accuracy.

The DC versus RF and frequency response data is only a good beginning toward a more complete measurement data set. Such a data set would include low frequency S-parameter data taken on many devices at many bias points across several temperatures. Even lower frequency network parameter data would complete the picture of the problem. Some issues that should be further investigated are the frequency at which Rds begins to roll off, the behavior of Gm between DC and 10 Hz, and whether the output capacitance continues to climb as the measurement frequency is lowered below 5 Hz. It may not be possible to use S-parameters for such low frequency measurements.

The measurement methodology presented in chapter 4 may be used for investigating correlations between power amplifier performance and device data. If one device shows an effect measured on a load-pull system that suggests trapping influences are at work, that same device may be checked to see whether a corresponding effect reveals itself in the network parameter data. Comparisons may be made on devices processed similarly to see whether the dispersion is exacerbated by a certain process step. This type of analysis, however, is extremely difficult given the number of process steps and the complexity of the device physics involved.

The models presented in chapter 6 seem to capture the small-signal measurements fairly well. However the frequency dependence of the output resistance and transconductance must be incorporated in a large-signal model, which may then be simulated in the time domain. A simulator with the flexibility to implement a new model easily may be used to this end.

This thesis effort should serve as a first step toward investigating and understanding low frequency dispersion in GaAs MESFET's. The work should be carried further to develop a data set that may be used for physically-based models, as well as models for circuit simulation.

Appendix A The Modeling of the Gate Diodes Dgs and Dgd

The current voltage characteristics of the diode Dgs of figure 2.1 are described by the following Shockley equation:

$$Id = Is\left(exp\left(\frac{Vgs}{\eta V_{th}}\right) - 1\right) \qquad \text{(EQ A.1)}$$

Id is the junction current; Vgs is the intrinsic gate-source voltage; Is is the reverse saturation current; η is the ideality factor; V_{th} is the thermal voltage (kT/q). The expression giving Id for Dgd is of the same form as Eq. A.1, except that Vgs is replaced by Vgd [7].

The diodes Dgs and Dgd are characterized by two parameters: Is and η. To determine these, two measurements of the forward conduction current are taken by setting Vgs and leaving the drain floating. The two diode parameters are then found from Eq. A.1. Correspondingly, to get the Dgd parameters, the gate-drain junction is forward biased with the source left floating [7].

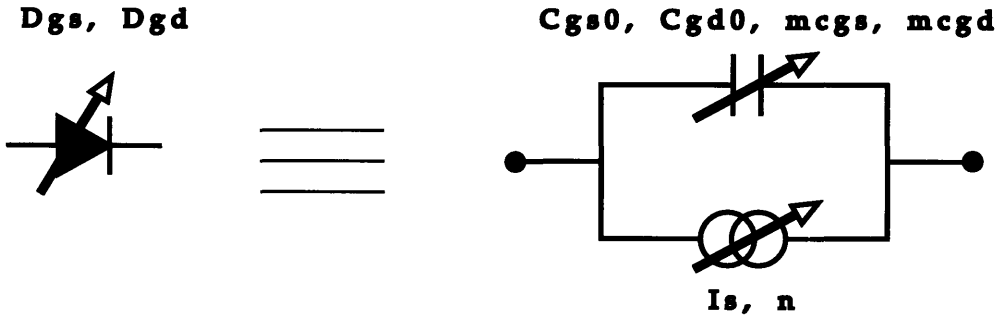

FIGURE A.1. Non-linear small-signal diode model.

The small-signal models for the reverse biased diodes Dgs and Dgd are shown in figure A.1. Capacitance is known to be a function of space-charge thickness. As a result, Cgs is strongly influenced by the gate-source voltage. It is not surprising that Cgs is modeled in this way, as shown below [7].

$$Cgs = \frac{Cgso}{\left(1 - \frac{Vgs}{Vbi}\right)^{mcgs}} \qquad \text{for Vgs < Vbi} \qquad \text{(EQ A.2)}$$

Vbi is the built-in potential difference between the metal gate and the substrate. Cgs0 and mcgs are fitting parameters to capture the bias-dependence of Cgs on Vgs [7].

The bias dependance of the capacitors Cgs and Cgd are captured in the large-signal model by the fitting parameters Cgs0, mcgs, Cgd0 and mcgd. To find Cgs0 and mcgs, Cgs from the small-signal extraction is plotted against intrinsic Vgs. The extraction of Cgs, however, is done at a matrix of both Vgs and Vds, and this results in a scatter plot of the extracted values at each Vgs. The capacitance model given in Eq. A.2 describes Cgs as a function of Vgs only, so a least square error fit of Cgs0 and mcgs is required. Similarly, Cgd is plotted against Vgd, and a least square error fit gives rise to Cgd0 and mcgd [7].

Appendix B Small Signal Model Element Value Extraction

There are two basic dependencies that any given circuit element can show: bias dependence and frequency dependence. In the Advanced Curtice model, Id is expressed in terms of Vgs and Vds does not exhibit frequency dependence. On the other hand the energy storage elements of the small-signal model introduce frequency dependence, and they are tabulated with the bias point at which they are extracted. The small signal element values are extracted using the general procedure described below and then used to complete the extraction of the large signal model.

B.1 Measurement setup

The measurement setup consists of an HP 8510C automatic network analyzer, an HP 4142B DC source monitor unit, an automatic wafer prober, and an IBM clone PC test controller. The HP 8510C can measure 2 port S-parameter data from 45 MHz to 20 GHz. The HP 4142B is an accurate DC source unit with a wide measurement range. To allow one to measure many devices, the automatic prober can make precise movements horizontally and vertically. All three of these components are run by a PC [7].

From the above setup, complete matrices of 2 port S-parameter data at various frequencies and bias points are obtained. Also, DC current-voltage characteristics are measured. Using the S-parameter data, small-signal models at each bias point are directly extracted as described below.

B.2 Extraction of parasitic elements

"Cold FET" measurements are taken in the extraction of the parasitic element values. They are typically taken with Vds=0v, and Vgs at three different biases, such as Vgs=0.8v, Vgs=0.9v, and Vgs=1.0v. Note that the gate-source and gate-drain junctions are forward-biased so that current can flow. The extracted values of parasitic elements are assumed to be unaffected by this biasing scheme, and so their extraction is made possible by the resulting simplified model. Because Vds=0v, the FET is not in its saturation mode of operation, and so the transconductance element can be ignored. Figure B.1 shows the model used for the FET under these bias conditions. To capture the resistive effects distributed along the gate, the channel could have been modeled by a complex resistive network. However, for simplicity, it is modeled by the elements 2Rgg and Rch. At frequencies below a few gigahertz, the inductors offer impedances that are insignificant compared to those of the resistors and may be ignored. Hence, only a resistive network remains [3].

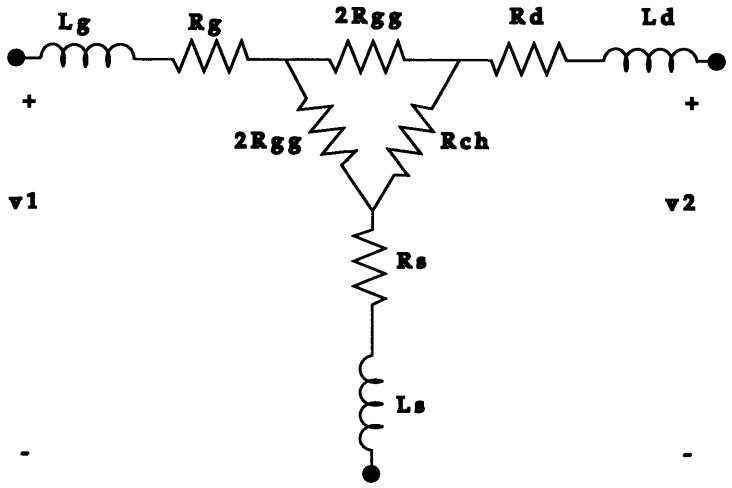

FIGURE B.1. Small signal model under "Cold FET" conditions

To extract the parasitics Rg, Rs, Rd, Lg, Ls, and Ld, an HP 8510C Network Analyzer is used to collect S-parameter data for the device under "Cold FET" conditions. The S-parameter data is then converted to measured Z-parameter data. Circuit analysis on the model shown in figure B.1 leads to the following equations for each Z-parameter [3]:

$$Z_{11} = \left.\frac{v_1}{i_1}\right|_{i2=0} = Rg + Rs + \frac{4Rgg(Vg)^2 + 2Rgg(Vg)Rch(Vg)}{4Rgg(Vg) + Rch(Vg)} + j\omega(Lg + Ls) \quad \text{(EQ B.1)}$$

$$Z_{21} = \left.\frac{v_2}{i_1}\right|_{i2=0} = Z_{12} = \left.\frac{v_1}{i_2}\right|_{i1=0} = Rs + \frac{2Rgg(Vg)Rch(Vg)}{4Rgg(Vg) + Rch(Vg)} + j\omega Ls \quad \text{(EQ B.2)}$$

$$Z_{22} = \left.\frac{v_2}{i_2}\right|_{i1=0} = Rd + Rs + \frac{4Rgg(Vg)Rch(Vg)}{4Rgg(Vg) + Rch(Vg)} + j\omega(Ld + Ls) \quad \text{(EQ B.3)}$$

As may be seen from Eqs. B.1-B.3, Rgg and Rch are functions of gate bias voltage. The parasitics on the other hand are assumed bias independent. To begin, one may assume that one measurement at Vgs=Vg1 has been taken. The extraction of the inductance values is straightforward, as the imaginary parts of the impedances lead to three expressions with three unknowns. To get at the resistance values on the other hand, the real parts must be analyzed. The first measurement at Vgs=Vs1 gives rise to three equations and five unknowns. The Z-parameters Z11, Z21, and Z22 are related by Rg, Rs, Rd, Rgg(Vg1), and Rch(Vg1). A second measurement at Vg2 considered in conjunction with the first produces six equations and seven unknowns. A third and final measurement gives three more equations and two more unknowns, bringing the number of equations and unknowns to nine. The system of equations may now be

solved to give rise to a unique solution for Rg, Rs, and Rd [3]. These equations are outlined below:

- Re{Z11(Vg1)} = f(Rg, Rs, Rgg(Vg1), Rch(Vg1))
- Re{Z21(Vg1)} = f(Rs, Rgg(Vg1), Rch(Vg1))
- Re{Z22(Vg1)} = f(Rd, Rs, Rgg(Vg1), Rch(Vg1))
- Re{Z11(Vg2)} = f(Rg, Rs, Rgg(Vg2), Rch(Vg2))
- Re{Z21(Vg2)} = f(Rs, Rgg(Vg2), Rch(Vg2))
- Re{Z22(Vg2)} = f(Rd, Rs, Rgg(Vg2), Rch(Vg2))
- Re{Z11(Vg3)} = f(Rg, Rs, Rgg(Vg3), Rch(Vg3))
- Re{Z21(Vg3)} = f(Rs, Rgg(Vg3), Rch(Vg3))
- Re{Z22(Vg3)} = f(Rd, Rs, Rgg(Vg3), Rch(Vg3))

In practice, however, measurements at a few additional bias points are taken to generate an average of parasitic resistances. Secondly, the inductances are not extracted at this stage, for historic reasons. Rather, they are assumed to be zero as a first pass, and then later recalculated. Thus the "Cold FET" measurements are only used for extracting Rg, Rs, and Rd [7].

B.3 Extraction of intrinsic small-signal element values at low frequencies

To extract the small-signal models for the FET in the constant current regime of operation, the 8510C is used to generate low frequency S-parameter data at a matrix of Vgs and Vds values. Some typical bias points may be taken on a depletion-mode device by sweeping Vgs from 0.0v to -1.6v, and Vds from 1v to 9v. The S-parameter data is converted to de-normalized Z-parameter data. The values for Rg, Rs, and Rd are used along with the extrinsic measured Z-parameter data to get measured intrinsic Z-parameters. These parameters can then directly give rise to the intrinsic element values of the small-signal model [7].

Just as there is a distinction between intrinsic and extrinsic voltages, a similar distinction may be made with impedances and admittances. The first equality shown in Eq. B.1 defines Z11. For the calculation of intrinsic Z11, v1 is the voltage across Cgs of figure 2.2, and i1 is the current flowing through the gate node. To calculate extrinsic Z11, the i1 used is the same but v1 is the extrinsic Vgs. One needs to distinguish whether intrinsic or extrinsic network parameters are being discussed. Given extrinsically measured Z-parameters, intrinsic Z-parameters are desired.

Some simple circuit analysis of the small-signal model of figure 2.2 gives the transformations required to convert between extrinsic and intrinsic Z-parameters:

$$Z11_{extrin} = Z11_{intrin} + (Rg + Rs) + j\omega (Lg + Ls) \quad \text{(EQ B.4)}$$

$$Z21_{extrin} = Z21_{intrin} + Rs + j\omega Ls \quad \text{(EQ B.5)}$$

$$Z12_{extrin} = Z12_{intrin} + Rs + j\omega Ls \quad \text{(EQ B.6)}$$

$$Z22_{extrin} = Z22_{intrin} + (Rd + Rs) + j\omega (Ld + Ls) \quad \text{(EQ B.7)}$$

At low frequencies, such as from 100 to 300 MHz, the parasitic inductances do not affect the calculated intrinsic Z-parameters appreciably, and are assumed to be zero at first as hitherto mentioned [7].

Using the intrinsic Z-parameters, the intrinsic model element values Cgs, Cgd, gm, gds, and τ are extracted by a series of equations. At this stage, these elements are assumed to be close to their final values. First, the intrinsic Z-parameters are converted to intrinsic Y-parameters. The extraction may be done using the following equations [7]:

$$Cgd = -\frac{Im\{Y12_{int}\}}{\omega} \quad \text{(EQ B.8)}$$

$$Cds = \frac{Im\{Y22_{int}\}}{\omega} - Cgd \quad \text{(EQ B.9)}$$

$$Cgs = \frac{Im\{Y11_{int}\}}{\omega} - Cgd \quad \text{(EQ B.10)}$$

$$gds = \frac{1}{Rds} = Re\{Y22_{int}\} \quad \text{(EQ B.11)}$$

$$gm = Re\{Y21_{int}\} \quad \text{(EQ B.12)}$$

$$\tau = -\frac{1}{\omega}\text{atan}\left(\frac{Im\{Y21_{int}\} + \omega Cgd}{Re\{Y21_{int}\}}\right) \quad \text{(EQ B.13)}$$

These extracted element values may be used to generate modeled Y-parameters, which may then be converted to a set of first-pass modeled Z-parameters at low frequencies [7].

B.4 Extraction of intrinsic small-signal element values at high frequencies

A second set of S-parameter data is taken at higher frequencies. At approximately 3 GHz for typical GaAs MESFET's, the parasitic inductances offer impedances comparable to those offered by the parasitic resistances. Their influence on these measurements can be isolated by comparing the high frequency data with the low frequency data. The inductances are assumed to offer zero impedance at the lower frequencies. From Eqs. B.4-B.7, it can be seen that the low frequency modeled Z-parameters may be subtracted from the high frequency measured Z-parameters, leaving only the impedances of the parasitics. In this way, accurate parasitic inductance values are found using the following equations [7]:

$$Im\{Z11_{extrin,\,meas,\,hifreq}\} - Im\{Z11_{intrin,\,mod,\,lofreq}\} = \omega(Lg + Ls) \qquad \text{(EQ B.14)}$$

$$Im\{Z21_{extrin,\,meas,\,hifreq}\} - Im\{Z21_{intrin,\,mod,\,lofreq}\} = \omega Ls \qquad \text{(EQ B.15)}$$

$$Im\{Z12_{extrin,\,meas,\,hifreq}\} - Im\{Z12_{intrin,\,mod,\,lofreq}\} = \omega Ls \qquad \text{(EQ B.16)}$$

$$Im\{Z22_{extrin,\,meas,\,hifreq}\} - Im\{Z22_{intrin,\,mod,\,lofreq}\} = \omega(Ld + Ls) \qquad \text{(EQ B.17)}$$

Once Lg, Ls, and Ld have been found, their values can be used with the low frequency data to get more accurate intrinsic element values. To do this, Eqs. B.4-B.7 are applied once again to generate a corrected matrix of intrinsic low frequency Z-parameters. After conversion to Y-parameters, the values of the intrinsic small-signal elements are recalculated by Eqs. B.8-B.13. Note that in the calculation of τ in Eq. B.13, high frequency Y-parameters are used [7].

B.5 Evaluation of error functions

Error functions at each bias point are calculated to gauge the success of the extraction. From the complete small-signal circuit with all its extracted element values, computed Y-parameters can be generated. These are converted to modeled S-parameters which are used to evaluate the model. The expression used for the error function is as follows [7]:

$$Eij = \frac{1}{n}\sum_{k=1}^{n} \frac{\left|\left(Sij^{k}_{Meas} - Sij^{k}_{Mod}\right)\right|}{\left|Sij^{k}_{Meas}\right|} \qquad \text{(EQ B.18)}$$

where n is the number of frequencies measured; i and j are indices indicating the S-parameter in question [7].

At each of the bias points, an average of the four error functions <Eij> is calculated and checked to see if it meets a specified tolerance. If the answer is yes, then the small-signal model is com-

plete. The final model element values are tabulated along with the error function values. If the tolerance is not met, another cycle of extractions begins with the extraction of parasitic inductance values. From there, the intrinsic element values are corrected once again [7].

At this point, a file is generated with the following element values extracted over various bias points: Cgs, Cgd, gm, tau, and Rds. The other element values that are not a function of bias are also tabulated: Rg, Rs, Rd, Lg, Ls, Ld and Cds. This direct extraction approach has proven to be both fast and accurate. The optimization approach of generating small-signal parameters has been avoided because of the variability of the final results. Optimizers generate different final answers based on different starting points.

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