Intrachip Clock Signal Distribution via Si-based **Optical Interconnect**

by

Donghwan Ahn

Submitted to the Department of Materials Science and Engineering in partial fulfillment of the requirements for the degree of

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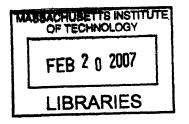
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Abstract

The Optical clocking has emerged as an innovative alternative approach to the electrical clocking, in order to overcome the difficulties associated with electrical interconnects in the synchronization of high-performance multi-GHz microprocessors. Because the on-chip optical interconnect must be embedded in current Si microprocessors, the optical clocking requires that the electronic-photonic integrated circuits (EPIC) consisting of Si-based photonic devices be developed on Si CMOS platform. We have identified the H-tree waveguide network and waveguide-integrated photodetectors as key photonic devices required for intrachip optical clocking for microprocessors.

We have demonstrated successful optical signal distribution through $\mathrm{SiO}_x \mathrm{N}_y$ waveguide H-tree network with 64 fanouts. A variable bending radius approach in H-tree design was used to optimize the performance of the optical clock signal distribution. The conventional y-splitter showed significant optical loss and unequal power-splitting ratio, which becomes increasingly problematic as the number of levels of a H-tree network increases and can result in increased skew. We devised a novel extended offset splitter, which reduced the splitting loss to < 3% and demonstrated 49:51 power split ratio.

We have fabricated Si vertical p-i-n photodetectors that are monolithically integrated with compact silicon-oxynitride channel waveguides. 830nm light guided by the waveguide was coupled to the photodetector through evanescent-wave coupling. We measured over 90% coupling efficiency. A two-step process that consists of 1) mode-coupling from a guided mode in the input waveguide to a leaky mode in the waveguide in contact with photodetector and 2) gradual evanescent wave coupling from waveguide towards photodetector, was a main coupling mechanism in the case of coupling with lower index-contrast waveguide, in contrast to high index-contrast waveguide case where coupling occurred nearly instantly at the front part of photodetector. It was shown that intentional introduction of an abrupt step in the waveguide at the transition interface to coupling region can improve mode-matching efficiency.

It is beneficial to design photodetectors made of a thin absorbing layer from SOI

or GOI(Germanium On Insulator) structures, in order to achieve the high speed and optical isolation. We studied the evanescent wave coupling behavior between silicon oxynitride (SiON) waveguides and thin Si photodetectors on SOI substrate at 850nm wavelength. We developed a simple and intuitive Leaky-Mode model using a ray-optics approach to determine the conditions for efficient coupling both in 2D and 3D structures. It is shown that the presence of leaky modes that are phasematched between the waveguide and the Si layer is the key condition for efficient coupling. The study showed that the Si layer thickness is the most critical factor that needs precise design and process control in this structure. With higher Δn (= $n_{core} - n_{cladding}$) waveguide design, the coupling rate to the Si layer is enhanced and becomes less sensitive to the Si layer thickness. Therefore, the change in coupling rate as a function of the Si layer thickness shows a sharp resonance-like dependence with low Δn waveguide design and a more muted oscillation-like dependence with high Δn waveguide.

Although Ge photodetectors have received great attention recently due to their absorption capability at longer wavelengths such as 1550nm and the compatibility with Si CMOS, the development of waveguide-integrated Ge photodetectors have remained an imperative but unaccomplished task. We developed Ge photodetectors monolithically integrated with silicon oxynitride and silicon nitride waveguides deposited on top of the photodetectors. High efficiency ($\sim 1.08A/W$) and high-speed (> 12 Gbit/s) performances were obtained. The Si CMOS-compatible detector devices retain their high performances even at low operation voltages, thus satisfying the low-voltage requirement of CMOS circuits, and have leakage currents that are low enough to meet the requirement of high-speed receiver designs. We also fabricated Ge photodetectors integrated with Si waveguides on SOI substrate. After the Si waveguide was formed on SOI substrate, Ge was selectively grown on a p⁺ doped area of Si waveguide and then a vertical p-i-n photodetector was formed by a n⁺ poly silicon. We have demonstrated the responsivity of 0.227 A/W and the 3dB frequency of 1.3 GHz.

Based on the understandings on waveguide-to-photodetector coupling obtained from experimental and theoretical studies, we present an evanescent coupling design map for Si photonics materials. Some novel designs of integrated photodetectors are presented. Potential prototype structures for intrachip optical clock signal distribution system are discussed.

Thesis Supervisor: Lionel C. Kimerling Title: Thomas Lord Professor of Materials Science and Engineering

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It took a bit more years than I wished. It took a bit more resources than I could imagine. It took a bit more delays, accidents, and failures than I expected. But, in the end, the feeling of overcoming those obstacles and accomplishing an MIT Ph.D with a modest measure of success is a truly rewarding one.

The education that I received from MIT was amazing. The education at this place enriched me by providing the chance to explore material to device to system perspectives of the engineering world and to study the theoretical, modeling, and experimental aspects of the research. Also, I was very fortunate to collaborate with many industrial partners from around the globe and gain insights into the dynamics of the global technology business. I feel comfortable in saying MIT is the best place in the world to learn science and engineering.

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> - Overlooking the Charles River from the Science Library, where I would spend the memorable time of my life Cambridge, MA, Oct. 2006

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Chapter 1

Introduction

Unceasingly growing demand for information-carrying capacity in the Information Age has resulted in the replacement of conventional communication via electrical cable with optical communications, especially in long-haul communication. Metal wire, in which electrons are transmitted to carry information, has a capacity limit inherently imposed by resistance and capacitance of the cable and also has the problem of significant power consumption [1]. We have seen, for these reasons, that optical communication plays an essential role especially in long-haul communication, which requires high bandwidth and long-distance information transfer.

As the demand for more communication capacity increases and information devices become faster, we can foresee the need for optical communication in much shorter-distance level applications. Not only do we begin to require optical approaches in short-distance local data networks like FTTH (Fiber-To-The-Home), we also are seeing the urge for optical interconnect between transistors on the chip level in microelectronics [2].

One of the most awaited applications of optical interconnect in microelectronics is clock signal distribution in VLSI systems and microprocessors. So far, the efforts to continue improving the performance of Si CMOS IC processors have been made by integrating more transistors and increasing the speeds of transistors and the operation frequency of clock signals. (The ability of the chip to perform logic operations can be approximated to be the number of gates times the clock rate.) While transistors

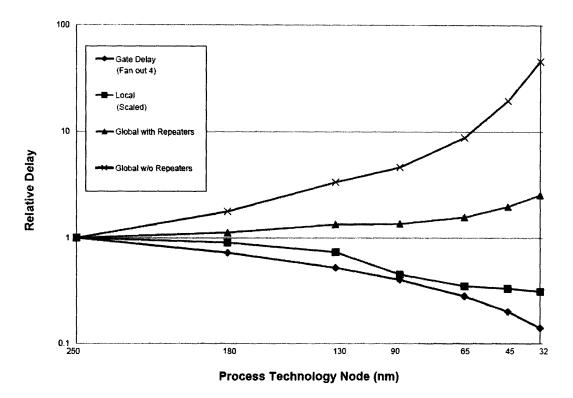


Figure 1-1: Delay for metal 1 and global wiring versus feature size [3].

still seem to have room for more integration and speed enhancement by simply scaling down the current planar technology, the continuous increase of clock signal speed, which governs the internal operation of microprocessor in the currently prevalent synchronous chip design, is facing a new physical limit. Interconnect cannot be scaled down as rapidly as electronic devices due to electro-migration and RC delays. Fig. 1-1 shows that the global electrical interconnect delay will even increase as smaller technology nodes are employed [3]. Interconnect delay will soon begin to dominate over gate switching delay and can be a limiting factor in the progress of microelectronics.

The problems with electrical interconnect become most prominent when used for clocking. Clock signals travel over the greatest distances, and operate at the highest speeds of any signals, within the entire chip [2]. Clock signal distribution via electrical interconnect will have problems of limited bandwidth, slow transfer of signal, and very high power consumption [4]. About 50% of power is dissipated as a result of clock distribution in modern high speed microprocessors. An additional problem is the large

number of pin-outs used for power distribution on a microprocessor. These problems become more critical as the clock speed increases. A potential solution to overcome this barrier is optical clock signal distribution. Optical clock signal distribution eliminates the problem of a limited bandwidth and may therefore enable us to increase the clock signal speed well above 10GHz, while keeping the power-consumption and heat generation constantly low [1]. Optical clocking is also a good first candidate that can demonstrate optical interconnects on a chip-sized level, because an on-chip light source is not needed when an off-chip clock-signal-generating laser source is used.

In this chapter, we will introduce the role of clocking in the microprocessor (Section 1.1), explain why electrical clocking is becoming increasingly difficult and how optical clocking can overcome such difficulties (Section 1.2 and 1.3). We will examine the possible optical clocking system architectures (Section 1.4), propose the fully integrated CMOS-compatible intrachip optical clocking, and identify key technical issues and challenges that need to be solved in such a structure (Section 1.5).

1.1 Clock Distribution in the Microprocessor

In a synchronous chip design which is used in virtually all electronic systems designed today, the clock signal is a time reference for the movement of data within the system. Fig. 1-2 shows the unit operation event that happens within one clocking period of time. Once the clock signal arrives at the register, the rising edge of the clock triggers the current data stored in input D to be copied to the Q output and leave the register. Time taken for this action is denoted by t_{C-Q} . There is propagation delay t_{int} from the register to the combinational logic. Combinational logic requires time $t_{logic(max)}$ to process the data. Another propagation delay time t_{int} is taken. t_{set-up} is a required time to latch within the final register of the data path and be settled before the next clock signal arrives. Therefore, the total path delay T_{PD} of one unit operation is as follows.

$$T_{PD} = t_{C-Q} + t_{int} + t_{logic(max)} + t_{int} + t_{set-up}$$
(1.1)

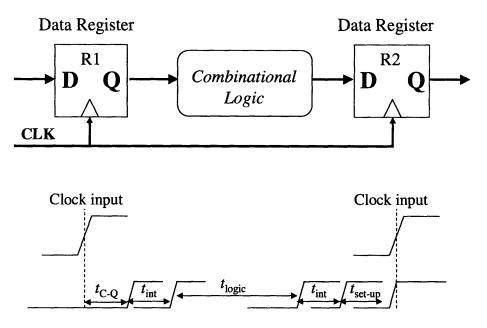


Figure 1-2: Block diagram of basic structure of a synchronous pipeline datapath and timing parameters [2].

The clocking period must be long enough for the data to propagate through the registers and logic and to be set up at the destination register before the next rising edge of the clock. This puts a time constraint on the clocking frequency as follows.

$$\frac{1}{f_{clocking}} = T_{clocking} > T_{PD} = t_{C-Q} + t_{int} + t_{logic(max)} + t_{int} + t_{set-up}$$
(1.2)

As the technology develops and the devices are scaled down, the delay times such as t_{logic} , t_{C-Q} , and t_{int} are reduced. Clock frequency can be increased and the overall chip performance improves accordingly. This has been the main way the semiconductor manufacturing industry has improved the computing speed of microprocessors until now.

As Fig. 1-1 indicates, the problem the industry is facing now is that it is very difficult to increase the clocking frequency any more at the pace that the logic speed keeps improving, due to growing global interconnect delay.

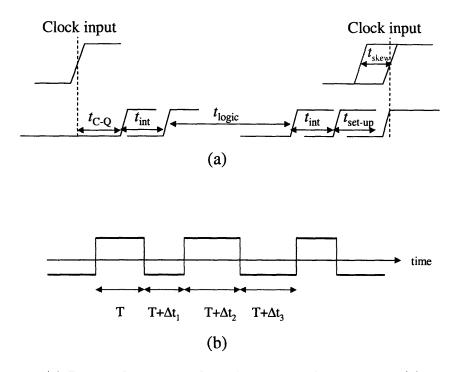


Figure 1-3: (a) Timing diagram to show the impact of clock skew. (b) Jitter as a temporal variation of the clock period.

1.2 Skew and Jitter

The difficulty with electrical clocking can be well understood by considering two critical system parameters in clocking; skew and jitter.

Skew is the spatial variation in arrival time of a clock signal among different registers on an integrated circuit. By definition, skew results in clock signal phase shift between different locations and is constant from cycle to cycle. Figure 1-3(a) shows the impact of negative clock skew. Because a clock signal arrives at the second register earlier than at the first register by t_{skew} for whatever reason, the new time constraint including skew considerations is now

$$\frac{1}{f_{clocking}} = T_{clocking} > T_{PD} = t_{C-Q} + t_{int} + t_{logic(max)} + t_{int} + t_{set-up} + t_{skew}$$
(1.3)

That is, the design of the clocking period $T_{clocking}$ has to be prolonged by no less than t_{skew} in order to allow for a safety margin to avoid race conditions. Thus, clock skew

is detrimental to the system performance.

It may seem that a positive skew (i.e., the clock signal arrives at the second register later than at the first register) can reduce the minimum clock period. However, a general logic circuit can have data flowing in both directions and therefore routing the clock so that only positive or negative skew occurs is not feasible. Increasing skew makes the circuit more susceptible to race conditions, which may harm the correct operation of sequential systems [5].

Jitter is the temporal variation of the clock period. That is, the clock period can be shorter or longer on a cycle-by-cycle basis, as depicted in Fig. 1-3(b). As skew does, jitter always has a negative impact on the clocking and system performance.

1.3 Electrical Clocking vs. Optical Clocking

The absolute delay of clock signal through distribution paths on a chip is not really important. What causes a problem is the relative discrepancy of signal arrival time, spatially and temporally; skew and jitter.

In an electrical clocking, there are may sources that can result in skew and jitter. First, on-chip clock-signal generator has some instability and can generate jitter. A voltage-controlled oscillator (VCO) is sensitive to intrinsic device noise, substrate noise, and power-supply variations. These noise sources generate cycle-to-cycle clockperiod variations. Second, skew results from the device and metal interconnect line variations on the chip and environmental variations. Since the signal propagates through metal line with RC delay time, the clock signal delay are unevenly affected among different propagation paths by capacitance variations due to non-uniform inter-level dielectric (ILD) thickness, electro-magnetic(EM) wave interference with local environment, the resistance/device function variation due to spatially-uneven temperature, etc [5].

As one try to increase clocking frequency and the clocking period decreases, the tolerance of skew and jitter must decrease accordingly. It becomes a very difficult task at more than 3.0GHz/10.0GHz global/local clocking frequency [6]. Moreover,

the higher clocking frequency dramatically increases the power consumption and heat generation in the chip, which is already a huge problem in a today's microprocessors.

The optical clocking can be an alternative solution. Signal propagation is very fast, with the speed of light divided by effective refractive index of the waveguide. Due to very high-speed propagation, variational factors such as path length difference or refractive index variation will have negligible impact on arrival time of optical clock signal. Optical signal does not get affected by crosstalk with nearby optical/electrical interconnect lines. For these reasons, skew by optical signal propagation will be very minimal. Jitter can be very minimal as well with a very stable optical clock source. Recently, mode-locked laser source with great than 10GHz repetition rate, less than 1 ps jitter was made possible [7]. Optical interconnects have no bandwidth limit imposed by optical signal itself (It is only limited by light source modulation and photo-receiver). They do not have heat-generation/power-consumption problems that increasingly become more difficult as the frequency increases.

With these many advantages, the optical interconnect can provide a microprocessor with above 10GHz clock signal distribution, which seems to be an excessively difficult task with electrical clocking. The challenge of implementing photonic circuitry to be co-integrated with microelectronics chip still remains. However, once this is possible, achieving a high frequency above 10GHz could be a relatively easy task.

1.4 Optical Clock Distribution Architecture Design

There have been extensive research approaches explored for optical clock distribution. They range from optical clock distribution within lower levels of the system packaging hierarchy [8–12] through the ones among separate boards of a complex system [13].

Fig. 1-4 [14] shows a few general approaches for optical clock distribution over IC. In Fig. 1-4(a), the optical waveguide has the H-tree geometry. External op-

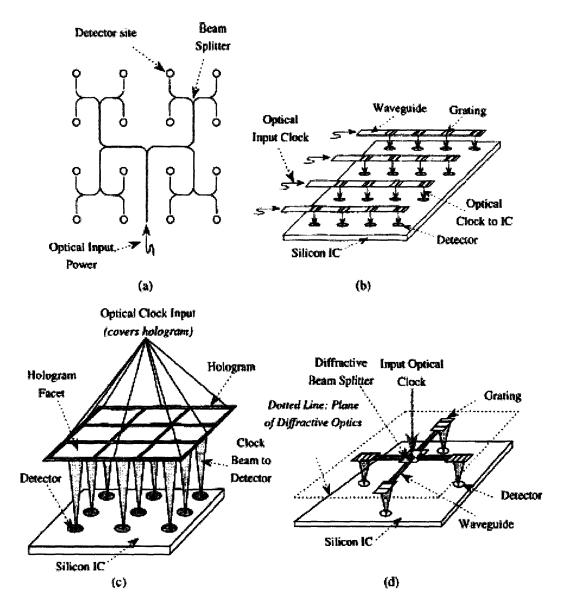
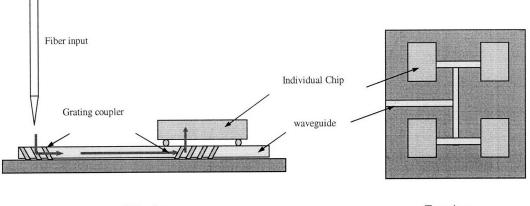


Figure 1-4: General approaches for optical clock distribution over the area of an IC [14]. (a) Waveguide emulating H-Tree. (b) Tapped waveguides. (c) Hologram distribution of clock. (d) Planar diffractive optics providing vertically optical clocks.



Side view

Top view

Figure 1-5: Schematic of optical clocking for multi-chip-module system [10, 15].

tical source is connected to H-tree waveguide network and the waveguide network distributes the optical signal to multiple leaf nodes, where optical signal is converted to electrical signal. Converted electrical clock signal continues to be delivered within the isochronous region by local electrical interconnects. Fig. 1-4.(b) shows signal distribution by tapped waveguide. From the traversing waveguide, a portion of optical energy is redirected towards underlying detectors at multiple tapping stages. Since the distances of paths are not equal, this structure will lead to some skews, which can be increasingly undesirable as the chip size increases or as clock speed becomes faster. In Fig.1-4(c), the optical clock signals are applied vertically through use of a hologram. This structure must have some separation distance from IC plane. In Fig.1(d), the structure has an plane with optical components, through which light is first distributed and then redirected vertically to IC.

Several research efforts have demonstrated optical clocking approaches for higher packaging levels such as in multi chip modules (MCM) and at the board(PCB) level [10,15–17]. A promising guided-wave approaches for optical clock signal distribution through multiple chip modules (MCM) have been demonstrated successfully [15] and may be references for designing viable optical clocking distribution on intra-chip scale. In Fig 1-5, optical signal from fiber is coupled into the waveguide through the tilted grating coupler. Optical clock signal is distributed by polymer-based waveg-

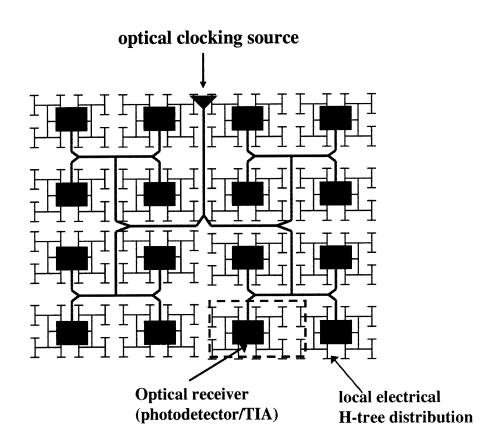


Figure 1-6: Proposed structure for monolithically integrated intra-chip optical clocking in the microprocessor.

uide H-tree system and is coupled into Si photodetector by an output surface-normal grating coupler. They demonstrated several-GHz optical signal distribution system that consists of CMOS process-compatible H-tree polymer waveguide, grating couplers and Si-based monolithic receivers. However, optical clockings that have been demonstrated mainly in high packaging level are not monolithically integrated and use free-space optics in a path to optical signal detection point. Those approaches are based on diffractive optics as shown in Fig.1-4 (b),(c),(d). It seems that they are not desirable approaches for applications of intra-chip optical clocking. It will cause the problems such as difficult system alignment and reliability concerns, and will increase the cost significantly. Also, the free-space optics will necessarily incorporate normal incidence of optical signal onto photodetectors and this scheme is generally unbeneficial for high-performance detector designs.

For intra-chip optical clocking application, monolithic integration of optical waveguide network and receiver circuitry with Si CMOS electrical IC must be pursued. For that reason, we will pursue the integrated optics approach as shown in Fig.1-4(a). Fig.1-6 shows the schematic of proposed optical clocking structure. An external light source is connected to the chip. On the chip, H-tree waveguide structure distributes optical signal to each leaf nodes, where the signal is converted to electrical signal. Converted electric signal continues to be distributed within local isochronous region via local electrical interconnect.

The ultimate goal for successful system performance is high-frequency clock signal distribution through all nodes with small skew, jitter, and reduced power consumption. More specifically, key issues for successful realization of the proposed structure are as follows: 1) development of H-tree waveguide structure with low loss and equal power distribution, 2) efficient coupling of light from waveguide to detector, and 3) development of detector with high responsivity and fast rise time. And these key issues constitute research tasks that have been conducted for this thesis.

The key components in optical clocking system and the key issues associated with each are discussed in more detail in the next section.

1.5 Key Technology Components for Intrachip Optical Clocking System

1.5.1 H-Tree Waveguide Network

H-tree waveguide structure distributes optical clock signals to each end leaf node all over the chip. The shape of H-tree is the standard design that have normally been used in electrical clockings, because it ensures that the distances the clock signal has to travel to reach each end node are all equal. Optical H-tree waveguide is simply the result of electrical H-tree metal lines being replaced with optics.

The ultimate goal of H-tree signal distributions is to successfully guide optical clock signal to the end nodes with the uniform signal arrival time. Therefore, key

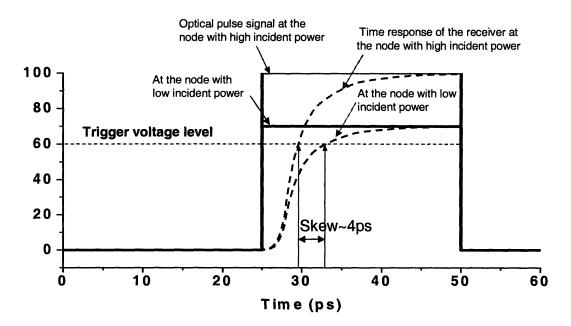


Figure 1-7: Time response of the photodector and transimpedance amplifier when there is the intensity difference of the optical signals arriving at the end nodes.

issues with H-tree waveguides are 1)low propagation loss through straight lines, bends and splitters, 2)minimal optical pulse signal dispersion, and 3)equal power-splitting with minimum loss at each splitting point.

The importance of equal power-splitting can be understood by the Fig.1-7. Optical clocking signal input at two different power levels are shown with photoreceiver responses. Because there is a latency in the response of photodetector and transimpedance amplifier to the incident optical signal, the rise times to a certain triggering voltage level are different depending on the optical signal intensity at the specific nodes locations. Therefore, it is very important to achieve even power-splitting, because the significant skew in clocking may arise from non-uniform optical signal distribution.

1.5.2 Waveguide-Integrated Photodetector

The photodetector is the most important device in the optical clocking system, because it is essentially the enabling technology of the optical clocking and the performance of the whole system relies on the detector performance. The fully-integrated intra-chip optical clocking approach that we chose to develop in this thesis research means that a waveguide-integrated detector is necessary. Its materials, device structure, and fabrications steps must be fully-compatible with Si CMOS materials and processes for the microprocessors.

The key issues in the performance of waveguide-integrated photodetector are 1) the high speed of the photodetector (i.e. the fast rise time responding to the optical clock signal), and 2) the high detector responsivity with efficient light coupling efficiency from waveguide to photodetector. The fast response of the photodetector is important because it enables high clocking frequency and reduces possible skew and jitter (Fig. 1-7 also demonstrates the importance of fast time response of photodetector). High detector efficiency improves signal-to-noise ratio and can reduce the required power budget of the optical clocking system.

Furthermore, the light-scattering at the coupling interface between the waveguide and photodetector must be minimal in order to prevent the noise and malfunction of the nearby devices. Back-reflection of the optical signal to the waveguide is also problematic for the system performance and it has to be minimized.

1.5.3 Trans-Impedance Amplifier Receiver Circuitry

The current signal, which a photodetector generated as a response to optical clocking signal, must be converted again to the voltage swing signal in order to be used as clocking signal in the digital electronic circuits. This conversion from the current signal to voltage signal is done by the trans-impedance amplifier (TIA).

Fig. 1-8 shows one schematic example of photo-receiver circuit designs. Once the incoming light signal is detected and photocurrent is generated, TIA pre-amplifier converts the photocurrent to voltage signals. Possible additional gain stages may amplify the signals further and the decision stages finally determines the trigger of clocking period.

The required characteristics of receiver circuits are fast response with minimal latency, low power consumption, low noise, robustness of process and environment variations, etc. Of course, the device and processing for these circuit components must

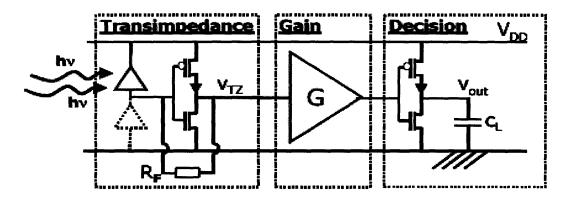


Figure 1-8: Schematic of one of the most typical front-end receiver configuration, which consists of a CMOS-inverter-based transimpedance front-end amplifier with additional gain stages.

be suitable for integration with CMOS-based microprocessor and photonic devices.

1.6 Outline of Thesis

The purpose of this thesis research is to address technical challenges identified in the Section 1.5 and to provide solutions towards the realizations of intra-chip optical clocking system. Especially a lot of research efforts were made for realizations of H-tree waveguides and waveguide-integrated photodetectors.

In Chapter 2, H-tree waveguides structure is demonstrated and the development of novel T-splitter will be discussed. In Chapter 3, design issues for the waveguideintegrated photodetectors such as speed, efficiency, and light coupling from waveguide to photodetector will be discussed. In Chapter 4, we demonstrate the integration of SiO_xN_y waveguides and photodetector employing evanescent coupling and discuss the dependence of the photon coupling rate on the design factors such as materials index contrast and waveguide designs. If the thickness of absorbing material becomes thin compared with its absorption length, the evanescent coupling from the waveguide to photodetector begins to show a different coupling behavior. This coupling behavior and a simple modeling method to predict coupling will be discussed in Chapter 5.

Then, from those theoretical and experimental knowledge we obtained on the photon coupling from waveguide to photodetector, we will present the evanescent coupling design map in the first part of Chapter 6. In the rest of the chapter, we will consider the design of silicon-waveguide-integrated Ge photodetector and discuss the related issues.

In Chapter 7, we present Ge integrated photodetectors coupled with the deposited waveguides on the top, such as silicon oxynitride and silicon nitride waveguides.

In Chapter 8, the bottom-waveguide-coupled Ge photodetector, where the Ge photodetectors are formed on top of Si waveguides on SOI substrate, will be presented.

Based on the research studies done in H-tree waveguides and the waveguideintegrated photodetectors, we will conclude by presenting a proposal for the on-chip optical clocking prototype in Chapter 9.

Chapter 2

Photon Distribution through H-tree Waveguide Network

In this chapter, $SiO_x N_y$ waveguide-based optical clocking signal distribution network with 64-nodes is demonstrated. The waveguide network consists of three levels of waveguide H-trees with decreasing bending radii and we developed a novel splitter structure, which demonstrated < 3% loss at the splitter and 49:51 power splitting uniformity.

We will begin the chapter with the materials choices and design considerations for the waveguide. In the next section, the fabricated H-tree waveguide prototype is presented. We will finish the chapter by discussing the design of the novel splitters that have good splitting uniformity and low split loss.

2.1 Waveguide Design and Materials Choice

The major waveguide materials candidates that can readily be used for silicon-based microphotonics are $SiO_x N_y$ [18, 19] and silicon materials.

As a dielectric material between SiO_2 and Si_3N_4 , both of which are well-developed and widely used in Si semiconductor processing, SiO_xN_y is fully compatible with Si CMOS fabrication processes. SiO_xN_y provides the flexibility such that we can adjust the refractive index within the range of 1.45-2.0 by changing composition ratio of nitrogen and oxygen [20]. Therefore, we have freedom to choose the core index of waveguide such that the waveguide can achieve the optimal performance in terms of bending radius and propagation loss, according to specific waveguiding-structure needs.

In contrast, silicon material has a fixed refractive index of 3.5. With usual cladding material SiO₂ that has refractive index of 1.45, an index contrast $\Delta n = 2.05$ of the silicon waveguide forces it to have a very compact dimension (for example, 200 nm $\times 500$ nm). This makes the silicon waveguide extremely susceptible to high propagation loss arising from non-ideal material issues such as sidewall roughness and non-crystallinity [21, 22]. However, some novel approaches [23, 24] to alleviate these problems and reduce the transmission loss have enabled silicon to emerge as a waveguide material of most interest.

The wavelength chosen to be used in the system places a restriction on the choice of waveguide material. Definitely, silicon cannot be used as a waveguide material at the wavelength shorter than 1.1μ m, which is the band gap wavelength of silicon. In contrast, SiO_xN_y can be used in a wider range of wavelengths from shorter wavelength such 850nm to the long wavelengths including 1550nm. In dielectric materials such as SiO_xN_y, bonding forces between some of constituent atoms in the material and the atoms associated during material deposition such as hydrogen may resonate with specific optical wavelength and absorb the energy, leading to the high absorption loss of the waveguide. Absorption peak due to N-H bonding that exists around 1510nm and leads to high propagation loss at 1550nm is one example [25]. This requires more sophisticated deposition process development [26] or additional processing steps such as high-temperature annealing to reduce atoms like hydrogen [25,27,28], which could have adverse effect on other CMOS devices.

Also, the choice of waveguide material is related to the vertical location of the waveguide in the layer levels of the chip. SiO_xN_y waveguide would be normally located a few microns (as high as a high metallization hierarchy level) above the active Si CMOS device level, since it is dielectric material and the under-cladding oxide material would be necessary. Si waveguide can be fabricated in the level above

substrate by deposition. However, being polycrystalline or amorphous, deposited-Si waveguide tends to have a high propagation loss. SOI wafers provide a single crystalline top Si layer separated by buried oxide from the substrate and the waveguide with this single-crystalline layer can have very low loss. Using SOI waveguide will place the waveguides at the level of Si active CMOS devices, therefore implementing photonics and electronics circuitry in the same level.

Being related to the issues such as materials for other devices, the wavelength in use and vertical placement in the material levels in a chip, the waveguide material has to be selected in the context of the whole optical systems design citekimerling:2006.

The rule of thumb about the waveguide design for photonic integrated chip is that we want to maintain a single mode in a waveguide. It is known that only singlemode propagation readily supports the various features for signal distribution such as bending, branching, and coupling with predictable performance and reasonable losses. Also, integrated wavelength filter, modulator, and other passive and active devices perform better when there is only one propagation mode in the waveguide. Therefore, a single mode waveguide is preferred for integrated photonics applications.

The first design consideration of waveguide comes from bending radius standard required by the system. While a bend with larger radius is always easier to implement with low loss, the restriction of real state on a chip sets the requirement of a certain bending radius [29]. To realize bends with acceptable loss and a radius less than a certain value, waveguide needs a certain or higher value of Δn , the index difference between core and cladding. An index engineering map from [30] shown in Fig.2-1 can help us find Δn appropriate for waveguide design. Given the desired index difference Δn of a waveguide, the condition of retaining only a single-mode within a waveguide places restriction on the maximum waveguide dimension. With waveguide dimensions greater than a certain value (a cut-off condition), the waveguide. Dimensions being slightly within the cut-off condition would be good numbers for the waveguide design, because reducing waveguide dimension further can increase the scattering loss of the waveguide.

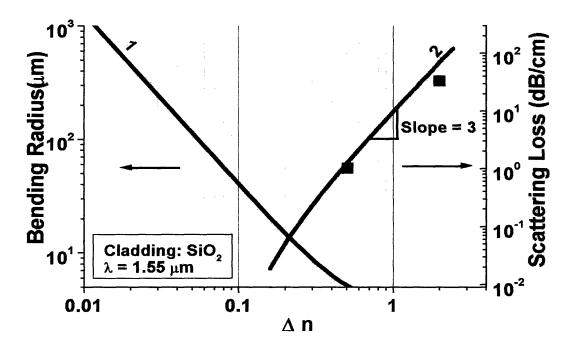


Figure 2-1: Index engineering plot [30]. The bending radius for $\alpha_L = 10^{-6} \mu m^{-1}$ criterion is plotted on the left against Δn . Scattering loss for square waveguide is plotted on the right against Δn . The RMS sidewall roughness $\sigma=10$ nm and the autocorrelation length $L_c=50$ nm are assumed.

Higher Δn requires smaller dimensions of waveguides. Smaller waveguides make difficult the coupling of waveguide with input light source (such as a fiber) and are more vulnerable to non-regularities such as core/cladding interface roughness that inevitably occur during fabrication processes. These problems may become very critical, although high Δn enables smaller bends preferred in large-scale integration. Therefore there is a trade-off for appropriate choice of n.

It should be noted that use of short wavelength like 850 nm demands more rigorous control of dimension in proportion to wavelength scale. The shorter wavelength generally requires the smaller waveguide and smaller index difference design. Therefore, the more rigorous control of physical dimensions and the refractive index is necessary.

2.2 H-Tree Waveguide Network Prototype Fabrication

As a first step to realize the optical clocking prototype in Si CMOS chip, we designed and fabricated H-tree waveguide structure.

Fig. 2-2 shows a photographic image of a fabricated optical waveguide H-tree distribution network circuitry made in a 5 mm × 5mm area of a silicon chip. The core of the waveguide is made of SiO_xN_y material and the cladding is SiO2. The H-tree is an H-shaped fan-outs that is essentially two 1 × 2 splitters with perfectly matched lengths from signal entering point to end nodes. 1×16 fanout distribution structure with two levels of H-trees are shown in the lower part of Fig. 2-2. And 1×64 fanout distribution structure with three levels of H-trees is shown in the upper part of Fig. 2-2, respectively. The waveguide design is based on single mode propagation of λ = 850 nm optical signals. For 1×16 H-tree structures, we designed the index contrast between core and cladding to be $\Delta n = 0.05$ and the waveguide core dimension was 1.5 μ m × 1.5 μ m. The bending radius was 250 μ m.

For 1×64 fanout H-trees, the index contrast was designed to be 0.07 such that it allows bending radius as small as 120 μ m at a theoretical radiation loss coefficient of

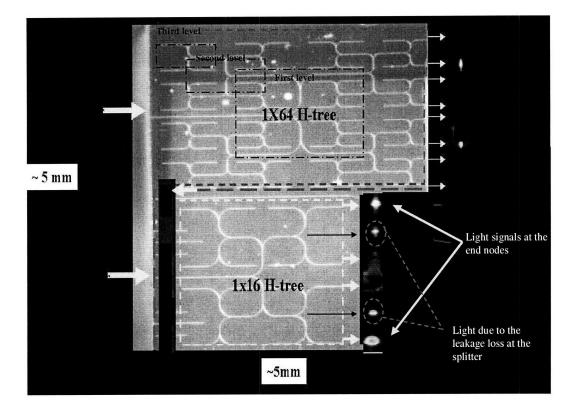


Figure 2-2: Photographic image of an H-tree optical clock signal distribution circuitries. Insert shows the side view image of the light at the waveguide output end.

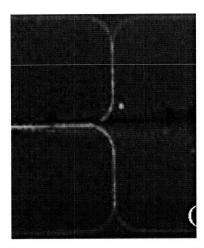


Figure 2-3: Top IR camera view of 1×4 H-tree, showing light propagation through waveguides and splitters with 800 μm bending radius. There is no noticeable light leakage at the splitter.

 $1 \times 10^{-8}/\mu m$. The waveguide core size was $1.5m\mu m \times 1.5\mu m$. We allowed the first level bending radius design to be 250 μm while the second and third level design was $120\mu m$. The use of variable bending radius design is to allow the largest bending at first level H-tree to improve the performance of waveguide H-tree. A larger bending radius allows smaller splitting angles that reduce splitting loss. Using a larger bending radius at earlier stage of H-tree is possible because a H-tree at earlier stage has a larger size therefore more open space is available for large bending radius.

Reducing a split loss at earlier stage is particularly beneficial, because the optical signal carries higher intensity in earlier stages and any optical power lost at a split is proportionally greater. The radiated light at a split may propagate on Si chip and cause transistors on Si chip to malfunction [31].

We observed the reduced optical power loss at the splitter with large bending radius. From the 1×4 H-tree structure that had as large as $800\mu m$ bending radius, there was no noticeable loss at the split, as shown in Fig. 2-3. In contrast, the side IR camera view in Fig. 2-2 inset revealed light leakage from the splitter with $250\mu m$ bending radius. The splitter design with greater bending radius, as long as space on the chip allows, helps reduce the loss of the H-tree waveguide. Therefore, use of variable bending radius (i.e., progressively reducing as it goes from high level to

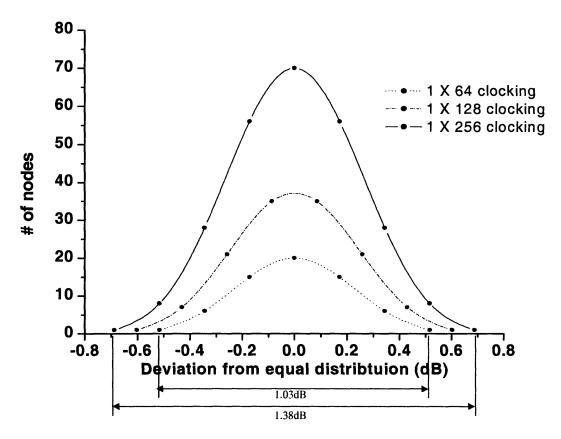


Figure 2-4: The distribution of optical power at the end nodes of 1×64 , 1×128 , and 1×256 H-tree network, when it was assumed that all the splitters have the 49:51 power split ratio.

low level), instead of having the bending radius of all splitters fixed to the minimum one required at lowest level stages, will save the optical energy loss in the H-tree waveguides.

2.3 Splitter Design

In Fig. 2-4, the distribution of optical power at the end nodes of H-tree network is shown. In the plot, it was assumed that all the splitters have a fixed 49:51 power split ratio. As one branch should have the higher power than the other at every split stage, the optical power at end nodes after multiple split stages will have a binomial distribution. As the number of levels of a H-tree network increases, the possible difference between the end node with the highest power and the node with the lowest power increases. The difference will be 1.03dB, 1.2dB, and 1.38dB for 1×64 , 1×128 , and 1×256 H-tree network, respectively.

This stresses the importance of equal power-splitting. Unequal power at individual end nodes leads to the time difference of when clock signal triggers the synchronization, i.e., the clocking skew, as explained in Section 1.5.1. Therefore, developing an equal power-splitter with minimum loss is a key issue in the H-tree waveguide network.

The conventional-type splitter, in which two bending output waveguides are overlapped and connected to the input waveguide (the inset in Fig. 2-5(a)), has some optical power loss due to the leakage at the split point. The split loss becomes more significant as the bending radius gets smaller, as Fig. 2-2 and Fig. 2-3 suggest. The power-splitting ratio of conventional splitters are poor as well (Fig. 2-5(e)).

To address this problem, we devised a novel splitter design. We offset the existing splitter waveguides from their entering optical axis by 50% of the waveguide width as indicated in Fig. 2-5 (b). In the 50% offset design, the splitting angle will be zero because the angle is formed by the inner walls of the two splitting waveguides. The inner walls are always tangential to each other. Such a zero angle splitter would be independent of the bending radius. A two-dimensional Finite Difference Time Domain (2D FDTD) simulation in Fig. 2-6 showed that such a design would result in a splitter that would reduce the splitting loss to zero in theory. In real experiments with an offset splitter, the split power loss was significantly reduced and the light propagation image captured by IR camera (Fig. 2-5(a) and (b)) showed apparent improvement over a conventional design. Measured split loss from offset splitters was less than 3%.

Power-splitting ratio was greatly improved as well. Conventional splitters showed a poor 56.2: 43.8 split ratio on the average (Fig. 2-5(e)). The offset splitters fabricated on the same sample as conventional one demonstrated a much better power-splitting uniformity of 51.2:48.8 on the average (Fig.2-5(f)).

Since all splitters are designed to have symmetrical shape, what causes the unequal

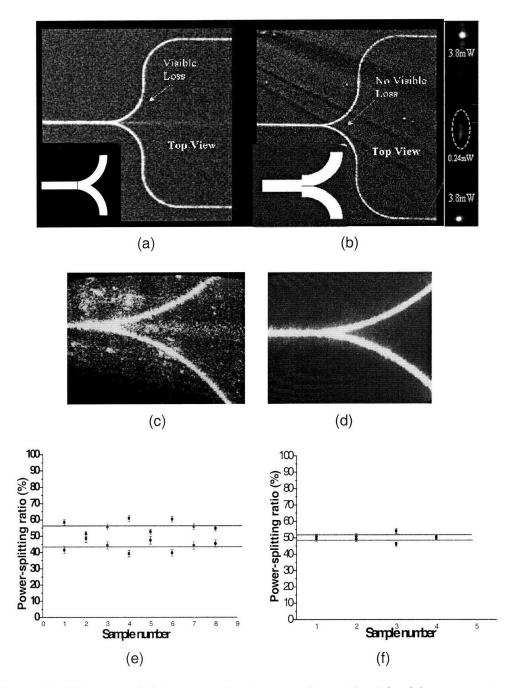


Figure 2-5: IR camera light propagation images taken at Intel for (a) a conventional Y-splitter and (b) a novel offset Y-splitter. Light propagation image taken at MIT for a close look at the split fork point for (c) a conventional Y-splitter and (d) an offset Y-splitter. (e) and (f) The power-splitting ratio of a conventional Y-splitter and an offset Y-splitter, respectively. The error bar in each sample indicates the measurement error. For waveguide design, 2.4 μ m(W) × 1 μ m(H) dimension with index contrast Δ =0.05 was used.

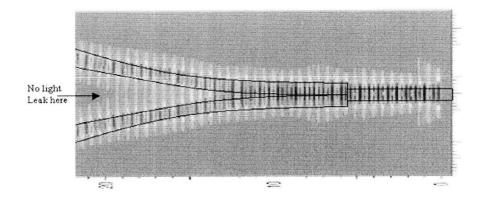


Figure 2-6: 2D FDTD simulation of a splitter design where splitter waveguides are offset from their optical entering axis by 50% of the waveguide width.



Figure 2-7: (a) the optical microscope and (b) SEM image of splitters, showing poor resolution at the point at split point.

power-splitting in real devices are likely to be non-idealities in processing. Fig. 2-7 shows the optical microscope and SEM images of a splitter at split point. They show poorly-resolved lithography at splitting points, which causes unpredictable deviation of splitter performance. The better lithography resolution is, the better power-split ratio will be. However, the lithography cannot be ideally perfect.

An offset splitter design allows the waveguide width at the merging point of the two splitting waveguides to be effectively twice as much as that of the simple Ysplitter waveguide, and thus the power splitter uniformity will be less sensitive to the waveguide fabrication error in terms of asymmetry by factor of 2. Therefore, under the same lithography resolution limit, an offset splitter design can demonstrate better power-splitting performance than a conventional splitter. We found that, from FDTD simulations, 49:51 split uniformity can be achieved if we maintain symmetry alignment control of the entering waveguide to that of the splitter to be less than 40nm in patterning definition.

2.4 Conclusion

Silicon CMOS compatible on-chip $SiO_x N_y$ waveguide H-tree optical clock signal distribution network with 64 fanouts was fabricated in a 3mmx5mm silicon area. A variable bending radius approach in H-tree design is used to optimize the performance of the optical clock signal distribution, and we observed successful transmission of light to all of the 64 fanouts. An extended offset splitter creates a zero splitter angle and reduces the splitting loss to < 3% and reduces the sensitivity of power-splitting ratio to asymmetric patterning error by a factor of 2. Both simulation and experiment demonstrated that power split uniformity of 49:51 or so is achievable.

Chapter 3

Design of Waveguide-Integrated Photodetector

Once photons are guided and distributed to the end nodes of H-tree waveguides for optical clocking, photons need to be absorbed in the photodetector to generate electric current such that electrical clock signal converted from optical clock signal can reach the register and trigger the data propagation.

There have been some prototype optical clocking systems [10, 15–17] that outcouple photons from the waveguide and transmit light via free-space to photodetectors located on another chip. However, only the photodetectors that are directly coupled to the waveguide and integrated monolithically on the same microprocessor chip serve the original goal of overall performance enhancement in an economical way.

Therefore, the monolithic integration of waveguides and photodetectors is one of the most important technologies required in an intrachip optical clocking system as well as in any photonic integrated chip (PIC).

Design of waveguide-integrated photodetectors is a process where one should consider multiple performance parameters one is targeting, such as frequency response, efficiency(responsivity), photon coupling with waveguide, materials choices, fabrication process etc. In many cases, these key parameters are correlated with one another and sometimes there may be a trade-off between some factors.

In this chapter, we will identify and discuss a few key parameters that need to be

considered in a design process of wave-integrated photodetector.

3.1 Photodetector Speed

The frequency response of a photodetector is one of the most important metrics used in evaluating photodetector performance. The data transfer rate of one communication channel will be limited by modulator speed on the transmitter side or the photodetectors on the receiver side.

In this section, we will attempt to calculate the frequency response time of p-i-n photodetector as a function of device design parameters such that it can serve as a guide in designing a photodetector. The discussion in this section is largely based on the derivation of photodetector response in [32].

3.1.1 Governing Equations for Carrier Transport in the Intrinsic Region

The electrical response of a photodetector is determined by the movement of electrons and holes generated by light absorption. This is prescribed by continuity equations of electrons and holes.

$$\frac{\partial p}{\partial t} = -\frac{p - p_0}{\tau_b} + g - \frac{\nabla \cdot \overrightarrow{J_p}}{q}$$
(3.1)

$$\frac{\partial n}{\partial t} = -\frac{n - n_0}{\tau_b} + g + \frac{\nabla \cdot \overrightarrow{J_n}}{q}$$
(3.2)

p and n are the densities of the holes and electrons. p_0 and n_0 are the equilibrium densities of holes and electrons. g is the volume electron-hole pair generation rate, either thermally or by optical excitation. q is the electronic charge and τ_b is the bulk lifetime of carrier. $\overrightarrow{J_p}$ and $\overrightarrow{J_n}$ are the hole and electron current densities and they consist of drift current and diffusion current terms as follows.

$$\vec{J_p} = p \,\mu_p \, q \, \vec{E} - q \, D_p \,\nabla p \tag{3.3}$$

$$\overrightarrow{J_n} = n\,\mu_n\,q\,\overrightarrow{E} + q\,D_n\,\nabla n\,. \tag{3.4}$$

 D_p and D_n are the diffusion constants for holes and electrons, μ_p and μ_n are the hole and electron mobilities, and E is the field present in the intrinsic region.

We now substitute equation (3.3) and (3.4) into (3.1) and (3.2). In doing so, we must note that the electric field is not constant inside the intrinsic region, because there is also a perturbation term in addition to the constant field by the externally applied bias. The light-generated electron and holes are separated in opposite directions by the applied reverse bias. The space charge variation inside the intrinsic region makes the electric field E be a function of the position x. Therefore, we must include the Poisson's equation

$$\nabla \cdot \vec{E} = \frac{q}{\varepsilon \,\varepsilon_0} (p-n) \,. \tag{3.5}$$

As a result, we obtain the following equations.

$$\frac{\partial p}{\partial t} = -\frac{p - p_0}{\tau_b} + g - \mu_p E \nabla \cdot p - \left(\frac{\mu_p q}{\varepsilon \varepsilon_0}\right) p(p - n) + D_p \nabla \cdot (\nabla p)$$
(3.6)

$$\frac{\partial n}{\partial t} = -\frac{n-n_0}{\tau_b} + g + \mu_n E \nabla \cdot n + \left(\frac{\mu_n q}{\varepsilon \varepsilon_0}\right) n(p-n) + D_n \nabla \cdot (\nabla n)$$
(3.7)

Equation (3.6) and (3.7) are governing equations for the movement of electrons and holes movement in the photodiodes. By applying these equations to the p-in photodetector structure shown in Fig.3-1, we are able to calculate the frequency response of the photodetector.

3.1.2 Simplification of Governing Continuity Equation with Adequate Assumptions

The governing continuity equation (3.6) and (3.7) are coupled with each other and look too complicated to be directly applied to the photodetector structure of Fig.3-1 and be solved. In fact, it is possible that we simplify them by making three major reasonable assumptions.

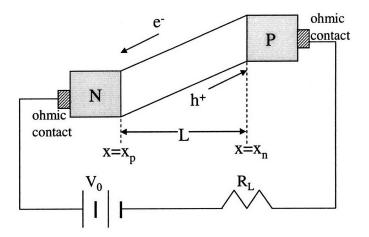


Figure 3-1: Schematic representation of reverse-biased p-i-n photodetector.

In the process of examining the validity of each assumption used to simplify the continuity equation, we, temporarily in this section, used the same mobility and diffusivity constant both for holes and electrons. We also assumed the uniform carrier generation independent of position in the intrinsic layer. These assumptions were done only for simplicity and would not change the validity of each assumption.

The first assumption is that the carrier lifetime in the intrinsic region is much longer than the average time τ which a light-generated carrier spends in the intrinsic region before reaching terminal electrodes. This is a reasonable statement that is easily satisfied in low-conductivity intrinsic semiconductor layer found in most photodetectors [33, 34].

The result is that the recombination rates of holes and electrons, $(p - p_0)/\tau_b$, $(n - n_0)/\tau_b$, are negligible compared to carrier-generation rates, because most lightgenerated carriers are swept out of the intrinsic region before any appreciable recombination can occur.

Therefore, we can remove the first terms from the right side of continuity equations (3.6) and (3.7)

$$\frac{\partial p}{\partial t} = -\frac{p - p_0}{\tau_b} + g - \mu_p E \nabla \cdot p - \left(\frac{\mu_p q}{\varepsilon \varepsilon_0}\right) p(p - n) + D_p \nabla \cdot (\nabla p)$$
(3.8)

$$\frac{\partial n}{\partial t} = -\frac{n - \mu_0}{\tau_b} + g + \mu_n E \nabla \cdot n + \left(\frac{\mu_n q}{\varepsilon \varepsilon_0}\right) n(p - n) + D_n \nabla \cdot (\nabla n)$$
(3.9)

The second assumption is that the space-charge-induced perturbation on the electric field in the intrinsic region is much smaller compared to the constant field E_0 arising from the applied bias. This means, in turn, that the amount of charge associated with carriers remaining in the junction is smaller than the amount of the charge on the plate of the capacitor, as explained in the following.

Under applied reverse bias, the p-i-n photodiode will have the characteristics of a parallel plate capacitor with plate separation equal to the intrinsic layer thickness L. The charge stored on the plate of the capacitor per unit area is given by

$$Q = \epsilon \epsilon_0 E_0 \tag{3.10}$$

The charge associated with carriers remaining in the junction is

$$qN = qLg\tau \tag{3.11}$$

N is the number of carriers in the intrinsic region per unit area and τ is the average time carriers take to be swept out of the intrinsic region and reach the electrodes. Thus,

$$\tau = \frac{\text{average distance traveled by a carrier}}{\text{the drift velocity within the intrinsic region}} = \frac{L/2}{\mu E_0} \ge \frac{L}{2v_{sat}}$$
(3.12)

In order that the perturbation on the field be small, it is required that $Q \gg qN$. That is,

$$Q = \epsilon \epsilon_0 E_0 \gg qN = qLg\tau = \frac{qL^2g}{2\mu E_0} \ge \frac{qL^2g}{2v_{sat}}$$
(3.13)

$$E_0^2 \gg \frac{L^2 qg}{2\mu\epsilon\epsilon_0} = \frac{LJ}{2\mu\epsilon\epsilon_0}$$
(3.14)

In most cases of photodetector operation, the condition (3.14) is satisfied. For an example of a silicon diode with an intrinsic thickness of 1μ m, the equation (3.14) becomes $E_0^2 \gg 5 \times 10^4 J$ where E_0 is in V/cm and J is in A/cm². It is advantageous and customary to operate photodetector at biases which saturate the carrier drift velocities. The electric field inside the intrinsic region under velocity saturation reaches

about 10^5 V/cm. The inequality is easily maintained for photocurrent densities as large as 10^5 A/cm².

When the perturbation of the field resulting from light generated carriers is small, the perturbation may be calculated to first order as follows. Referring to the coordinate system of Fig. 3-1, let $x_p = -L/2$, and $x_n = L/2$. Then the net positive space charge contained in the region from x = 0 to x = L/2 may be set equal to half the number of holes present in the I region as given by Equation (3.13), yielding

$$\int_{0}^{L/2} [p(x) - n(x)] dx = L^2 g / 4\mu E_0$$
(3.15)

$$p(x) - n(x) = (2g/\mu E_0)x \tag{3.16}$$

The third assumption is that the diffusion current is much smaller compared to the total current density and thus negligible. That is, from the following expression for the current density in the intrinsic region,

$$J = J_p + J_n = q\mu(p+n)E - qD\nabla(p-n) = Lqg$$
(3.17)

the assumption is

$$\frac{qD\nabla(p-n)}{Lqg} \ll 1 \tag{3.18}$$

Therefore,

$$J = Lqg = q\mu(p+n)E \tag{3.19}$$

$$p+n = \frac{J}{q\mu E} \tag{3.20}$$

From (3.16) and (3.20), we obtain

$$p(x) = (g/\mu E_0) \cdot (x + L/2) \tag{3.21}$$

$$n(x) = -(g/\mu E_0) \cdot (x - L/2) \tag{3.22}$$

For this linear variation of the carrier concentration, it is clear that the diffusion terms in the continuity equations, $D\nabla \cdot (\nabla p)$ and $D\nabla \cdot (\nabla n)$ vanish. It means we

can remove diffusion current term in equation (3.3) and (3.4). This will eliminate the fifth term in the continuity equation.

$$\frac{\partial p}{\partial t} = -\frac{p - p_0}{\tau_b} + g - \mu_p E \nabla \cdot p - \left(\frac{\mu_p q}{\varepsilon \varepsilon_0}\right) p(p - n) + \underline{D}_p \nabla \cdot (\nabla p)^*$$
(3.23)

$$\frac{\partial n}{\partial t} = -\frac{n - \mu_0}{\tau_b} + g + \mu_n E \nabla \cdot n + (\frac{\mu_n q}{\varepsilon \varepsilon_0})n(p - n) + \underline{D_n \nabla} (\nabla n)$$
(3.24)

Now, having estimated the distribution of light-generated carriers, we compare the nonlinear term (the fourth term) of (3.8) and (3.9) with the third term. That is,

$$\frac{\mu q p(p-n)}{\varepsilon \varepsilon_0 \mu E(dp/dx)} \cong \frac{L}{\mu \varepsilon \varepsilon_0} \frac{J_L}{E_0^2}$$
(3.25)

This ratio must be much less than one by the result (equation (3.14)) of the second assumption that the light generated carriers do not appreciably perturb the field produced by the external bias.

$$\frac{L}{\mu\varepsilon\varepsilon_0}\frac{J_L}{E_0^2} << 1 \tag{3.26}$$

These removes the fourth term in the right side of the continuity equations.

$$\frac{\partial p}{\partial t} = -\frac{p - p_0}{\tau_b} + g - \mu_p E \nabla \cdot p - (\underbrace{\mu_p q}_{\mathcal{E} \in 0}) p(p - n) + \underline{D}_p \nabla \cdot (\nabla p)$$
(3.27)

$$\frac{\partial n}{\partial t} = -\frac{n - \mu_0}{\tau_b} + g + \mu_n E \nabla \cdot n + (\frac{\mu_n q}{\varepsilon \varepsilon_0}) n(p - n) + D_n \nabla (\nabla n)$$
(3.28)

The above assumptions simplify the continuity equation as follows.

$$\frac{\partial p}{\partial t} = g - \mu_p E \frac{\partial p}{\partial x} \tag{3.29}$$

$$\frac{\partial n}{\partial t} = g + \mu_n E \frac{\partial n}{\partial x} \tag{3.30}$$

and the current density is given by

$$J = q(\mu_p p + \mu_n n)E + \varepsilon \varepsilon_0 (\partial E / \partial t)$$
(3.31)

3.1.3 Frequency Response of Photodetector

Now we can calculate the frequency response of photodetector model shown in Figure 3-1 by solving the equations (3.29) to (3.31) in a response to the sinusoidal variation of the incident light.

For simplicity, we consider the uniform carrier-generation case first here. Thus,

$$g = g_0 G(t) = g_0 (1 + A\cos\omega t) = g_0 Re(1 + Ae^{i\omega t})$$
(3.32)

For convenience, we use the complex periodic function rather than using only its real part. The solution for the real excitation function is simply the real part of the solution for the complex excitation function.

From (3.29) and (3.30), the differential equations to be solved are

$$(\partial p/\partial t) + v(\partial p/\partial x) = g_0(1 + Ae^{i\omega t})$$
(3.33)

$$(\partial n/\partial t) - bv(\partial n/\partial x) = g_0(1 + Ae^{i\omega t})$$
(3.34)

where $b = \mu_n / \mu_p$ is the ratio of the electron to the hole mobilities, and v is the velocity of the hole.

For the boundary conditions $p(x_p) = 0$ and $n(x_n) = 0$, the solutions to these equations are

$$p(x,t) = \frac{g_0}{v}(x-x_p) + \frac{g_0 A}{i\omega} \{1 - e^{-\frac{i\omega}{v}(x-x_p)}\}e^{i\omega t}$$
(3.35)

$$n(x,t) = \frac{-g_0}{bv}(x-x_n) + \frac{g_0 A}{i\omega} \{1 - e^{-\frac{i\omega}{bv}(x-x_n)}\}e^{i\omega t}$$
(3.36)

To obtain an expression for the current density, we need to evaluate an electric field E as a function of time to find out the displacement term in equation (3.31).

From Poisson's equation

$$E = \frac{q}{\epsilon\epsilon_0} \int^x [p(\xi, t) - n(\xi, t)] d\zeta + \frac{q}{\epsilon\epsilon_0} C(t) + E_0$$
(3.37)

,where C is the areal density of charges stored in the capacitor.

With use of (3.33) and (3.34),

$$\epsilon\epsilon_0 \frac{\partial E}{\partial t} = q \int^x \left[\frac{\partial p(\xi, t)}{\partial t} - \frac{\partial n(\xi, t)}{\partial t}\right] d\zeta + q \frac{\partial C(t)}{\partial t} = -qv[p(x, t) + bn(x, t)] + q\left[\frac{\partial C(t)}{\partial t}\right]$$
(3.38)

The current density, J, from equation (3.31) becomes

$$J = qv[p(x,t) + bn(x,t)] + \epsilon\epsilon_0 \frac{\partial E}{\partial t} = q \frac{\partial C(t)}{\partial t}$$
(3.39)

To evaluate the function C(t), we assume that the diode is in series with a battery of potential V_0 and a load impedance R as shown in Fig.3-1, and write a Kirchoff's equation for the loop

$$\int_{x_p}^{x_n} E \, dx = \frac{q}{\epsilon \epsilon_0} \int_{x_p}^{x_n} \int^x [p(\xi, t) - n(\xi, t)] d\zeta dx + \frac{q}{\epsilon \epsilon_0} C(t) L - V_0 = -V_0 - IR = -V_0 - qAR \frac{\partial C}{\partial t}$$
(3.40)

If C(t) varies with time as $e^{i\omega t}$,

$$C(t) = \frac{-\frac{1}{L} \int_{x_p}^{x_n} \int^x [p(\xi, t) - n(\xi, t)] d\zeta dx}{1 + i\omega R(\epsilon \epsilon_0 A/L)}$$
(3.41)

The current density in the diode is

$$J = q \frac{\partial C(t)}{\partial t} = \frac{-\frac{q}{L} \int_{x_p}^{x_n} \int^x [\frac{\partial p(\xi,t)}{\partial t} - \frac{\partial n(\xi,t)}{\partial t}] d\zeta dx}{1 + i\omega RC} = \frac{\frac{qv}{L} \int_{x_p}^{x_n} [p(x,t) + bn(x,t)] dx}{1 + i\omega RC}, \quad (3.42)$$

where C is $\epsilon \epsilon_0 A/L$, the capacitance of the diode.

By substituting p(x,t) and n(x,t) from equation (3.35) and (3.36), we get

$$J = \frac{Lqg_0}{1+i\omega RC} \left\{ 1 + Ae^{i\omega t} \left[\frac{(1+b)v}{i\omega L} + \frac{(1+b^2)v^2}{\omega^2 L^2} - \frac{v^2}{\omega^2 L^2} e^{-i\omega L/v} - \frac{v^2 b^2}{\omega^2 L^2} e^{-i\omega L/bv} \right] \right\} (3.43)$$

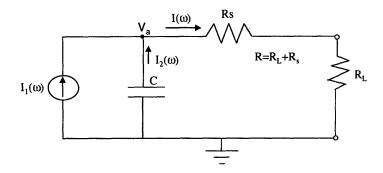


Figure 3-2: Photodetector equivalent circuit.

From the above equation, the frequency response function is obtained as the following.

$$I(\omega) = \frac{1}{1+i\omega RC} \left\{ \frac{(1+b)v}{i\omega L} + \frac{(1+b^2)v^2}{\omega^2 L^2} - \frac{v^2}{\omega^2 L^2} e^{-i\omega L/v} - \frac{v^2 b^2}{\omega^2 L^2} e^{-i\omega L/bv} \right\}$$
(3.44)

3dB frequency f_{3dB} is defined as the frequency at which the above frequency response function becomes equal to $1/\sqrt{2}$.

Thus far, beginning from the continuity equations for electrons and holes, we directly solved the movement of electrons and holes under given absorption function and the boundary conditions of intrinsic layer, obtained the photocurrent density as a time-varying function, and then extracted the frequency response function of the photodetector system.

In fact, the frequency response function of Equation (3.44) lets us view the p-i-n photodiode system as an equivalent circuit shown in Fig. 3-2. From the circuit of Fig.3-2,

$$I_1(\omega) + I_2(\omega) = I(\omega), \quad I_1(\omega) - \frac{V_a}{(\frac{1}{i\omega C})} = \frac{V_a}{R}, \quad I(\omega) = \frac{V_a}{R} = \frac{I_1(\omega)}{1 + i\omega RC} \quad (3.45)$$

That is, a photodetector can be seen as a current source with a response function by carriers transit of $I_1(\omega)$ that is connected in parallel with a capacitor with capacitance of $C = \epsilon \epsilon_0 (A/L)$ [35].

Therefore,

$$I_1(\omega) = \frac{(1+b)v}{i\omega L} + \frac{(1+b^2)v^2}{\omega^2 L^2} - \frac{v^2}{\omega^2 L^2} e^{-i\omega L/v} - \frac{v^2 b^2}{\omega^2 L^2} e^{-i\omega L/bv}$$
(3.46)

is defined as transit-time frequency response. And,

$$I_2(\omega) = \frac{1}{1 + i\omega RC} \tag{3.47}$$

is RC-time frequency response.

If the light is incident on the n side of the photodetector junction and if one considers that the coordinate x in Fig. 3-1 is increasing from x_p and x_n , the function of carrier generation by light absorption is

$$g(x) = \alpha g_0 e^{-\alpha (x-x_p)} (1 + A\cos\omega t) = \alpha g_0 e^{-\alpha (x-x_p)} Re(1 + Ae^{i\omega t})$$
(3.48)

For this generation function, the solutions of the continuity equations are

$$p(x,t) = g_0 / v [1 - e^{-\alpha(x-x_p)}] + \frac{\alpha g_0 A e^{i\omega t}}{(i\omega - \alpha v)} [e^{-\alpha(x-x_p)} - e^{-i(\omega/v)(x-x_p)}]$$
(3.49)

$$n(x,t) = -g_0/bv[e^{-\alpha L} - e^{-\alpha(x-x_p)}] + \frac{\alpha g_0 A e^{i\omega t}}{(i\omega + \alpha bv)} [e^{-\alpha(x-x_p)} - e^{-\alpha L} e^{i(\omega/bv)(x-x_n)}].$$
(3.50)

After substituting these into Equation (3.42), the current density is

$$J = \frac{qg_0(1 - e^{-\alpha L})}{1 + i\omega ZC} \{ 1 + \frac{Ae^{i\omega t}}{[(i\omega L/v) - \alpha L]} [1 - \frac{\alpha L}{(1 - e^{-\alpha L})} \frac{(1 - e^{-i\omega L/v})}{i\omega L/v}] + \frac{Ae^{i\omega t}}{(i\omega L/bv) + \alpha L} [1 - \frac{\alpha Le^{-\alpha L}}{(1 - e^{-\alpha L})} \frac{(1 - e^{-i\omega L/bv})}{i\omega L/bv}] \}.$$
(3.51)

The frequency response function is obtained as the following.

$$I(\omega) = \frac{1}{1 + i\omega ZC} \left\{ \frac{1}{((i\omega L/v) - \alpha L)} \left[1 - \frac{\alpha L}{(1 - e^{-\alpha L})} \frac{(1 - e^{-i\omega L/v})}{i\omega L/v} \right] + \frac{1}{((i\omega L/bv) + \alpha L)} \left[1 - \frac{\alpha L e^{-\alpha L}}{(1 - e^{-\alpha L})} \frac{(1 - e^{-i\omega L/bv})}{i\omega L/bv} \right] \right\}$$
(3.52)

Transit-time frequency response function and RC-time frequency response function are

$$I_{1}(\omega) = \frac{1}{((i\omega L/v) - \alpha L)} [1 - \frac{\alpha L}{(1 - e^{-\alpha L})} \frac{(1 - e^{-i\omega L/v})}{i\omega L/v}] + \frac{1}{((i\omega L/bv) + \alpha L)} [1 - \frac{\alpha L e^{-\alpha L}}{(1 - e^{-\alpha L})} \frac{(1 - e^{-i\omega L/bv})}{i\omega L/bv}]$$

$$I_{2}(\omega) = \frac{1}{1 + i\omega RC}$$
(3.54)

3.2 Efficiency

The efficiency of the photodetector is the measure of how efficiently photodetectors generate photocurrent given optical signal. The quantum efficiency η , from the quantum particles viewpoint, measures how many electron-hole pairs are generated and collected per unit number of photons. And, responsivity, R, measures the ampere of the generated photocurrent per optical power. Therefore,

$$R = \eta \frac{q}{h\nu} \tag{3.55}$$

While the quantum efficiency is the measure that indicates a simple conversion efficiency of photodiode irrespective of the wavelength used, the responsivity provides the easy conversion measures for electrical engineers to refer to in designing the system by using the ampere and watt units.

In most conventional p-i-n structure shown in Fig.3-3, the quantum efficiency would be

$$\eta = 1 - \exp(-\alpha d), \tag{3.56}$$

where α is the absorption coefficient of the photodetector material and d is the absorbing layer thickness. The quantum efficiency in equation (3.56) requires that all the carriers generated in the intrinsic layer be collected without recombination, which is a satisfiable condition in many cases as explained in section 3.1.2. Additionally, The quantum efficiency in equation (3.56) includes only drift current and neglected

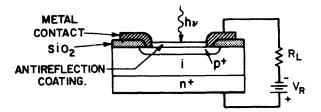


Figure 3-3: structure of typical p-i-n photodetector.

the diffusion current that can arise from diffusion of minority carriers generated in p+ and n+ region. Since the diffusion current is much slower than drift current, one design p-i-n photodetector such that the diffusion current is minimal. Therefore, equation (3.56) is reasonable in most cases.

An important properties parameter of a photodetector material is the absorption coefficient. Generally, efficient absorbing material with high absorption coefficient is beneficial, because the detector intrinsic layer can be made thinner, the detector size is smaller, and the speed is higher.

Fig. 3-4 shows the absorption coefficient of various semiconductor materials. The materials that can be introduced to Si microelectronics processes are group IV materials such as silicon and germanium. It should be noted that silicon and germanium are indirect band-gap materials and their absorption coefficients at optical communications wavelength (e.g., that of silicon at 850 nm or that of germanium at 1550 nm) are much lower than those of III-V compound semiconductor materials (e.g., that of GaAs at 850 nm or that of InGaAs at 1550 nm). If one increase the intrinsic layer thickness in order to increase efficiency, the speed will become slower. This is the disadvantage of group IV materials as photodetector materials, which we need to overcome in order to succeed in Si-based optoelectronics, and it is also one of the reasons why compound semiconductor material have been dominant so far in the photonic devices applications.

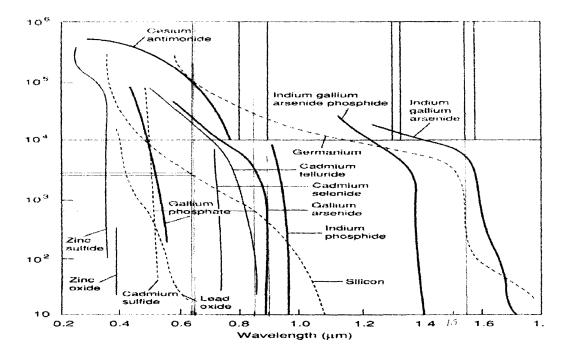


Figure 3-4: Absorption coefficients of various semiconductor materials as a function of wavelength.

3.3 Benefits of Photodetector Integration with Waveguide

The first benefit of photodetector integration with waveguide is the speed enhancement by down-scaling. To demonstrate this, we drew a design map that shows the dependence of a photodetector speed on the design parameters such as the size of photodetector and intrinsic layer thickness.

Fig. 3-5 is the plot of 3dB frequency of the photodetector, at which Equation (3.52) is equal to $1/\sqrt{2}$, as a function of depletion thickness L and detector size A. Ge photodetector material is taken as an example. Therefore, the dielectric constant $\epsilon_r = 16$ and the absorption coefficient $\alpha = 4000 cm^{-1}$ were used. The saturation velocities of $v_{s,hole} = 6 \times 10^6 cm/s$, $v_{s,electron} = 7 \times 10^6 cm/s$ were used in calculation. We assumed R_s , the parasitic series resistance of the photodiode, is negligible and used $R = 50 \Omega$, because the load resistance of $R_L = 50 \Omega$ is the standard impedance

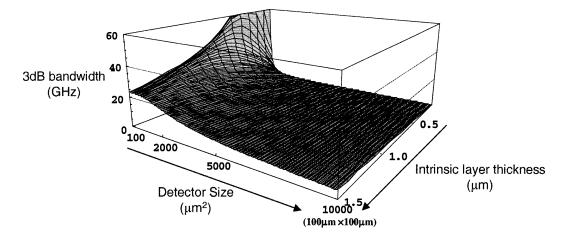


Figure 3-5: The 3dB frequency of Ge p-i-n photodetector as a function of depletion layer thickness and detector size.

normally used in RF circuitry.

The frequency response in Fig. 3-5 can be considered to be combined result of transit-time frequency response and RC-time frequency response shown in Fig. 3-6(a) and Fig. 3-6(b), respectively.

While transit time frequency is the function of intrinsic layer thickness only and the bandwidth can go very high with thin intrinsic layer, RC-time limit frequency response affects the photodetector speed especially when the detector size is great and intrinsic layer is thin.

For example, a photodetector with 100 μ m × 100 μ m area size will not be able to exceed 10 GHz speed, regardless of intrinsic layer thickness. As Fig.3-7 indicates, the only way to reach 20 GHz bandwidth for example, is to reduce the detector size enough not to be affected by RC-time effect significantly. This explains an important benefit of integration of photodetector with waveguide. If a discrete photodetector is used and its size is greater than, say, 2000 μ m² (which may be often the case, because the size of the normal-incident beam from free-space is normally big and additional margin area must be added for misalignment tolerance), the bandwidth of the photodetector will be RC-time limited and cannot achieve high speed. On the contrary, by doing integration with waveguide, we can down-scale photodetector size. The size of photon stream is greatly reduced from free-space light beam to the

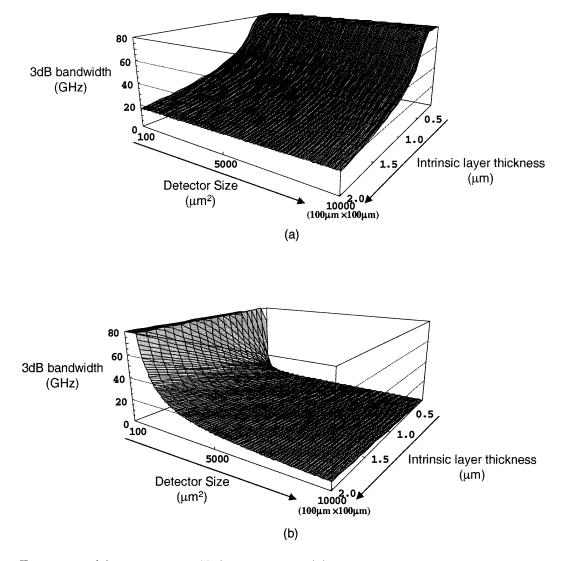


Figure 3-6: (a)transit-time 3dB frequency and (b)RC-time 3dB frequency of Ge p-i-n photodetector as a function of depletion layer thickness and detector size.

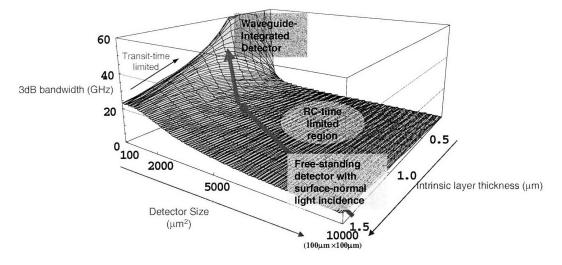


Figure 3-7: Down-scaling of photodetectors by integration enables high bandwidth by eliminating RC-time limitation.

mode in the waveguide, whose dimension typically ranges only from 0.2 μ m to a few microns. The width of photodetector can be only a few times of waveguide width and the length of the device will not exceed 200 μ m even with slow light coupling. This down-scaling by integration basically eliminates the issue related to the capacitance of photodetector and enables high speed well up to as high as 20 GHz bandwidth design.

Another benefit of photodetector integration with waveguide is that it can solve the trade-off problem between quantum efficiency and bandwidth of the photodetector.

Fig. 3-8 plotted the traces of the quantum efficiency and the 3dB frequency of conventional vertical p-i-n photodetectors(as in Fig. 3-3) made of various semiconductor materials, as the intrinsic layer thickness changes. It was assumed that the capacitance is negligible and RC-time limit does not affect the bandwidth performance. Therefore, Equation (3.53) for carrier transit-time frequency and Equation (3.56) for quantum efficiency were used.

In conventional discrete p-i-n photodetectors, light absorption path and carrierscollecting path are parallel. Therefore, as the intrinsic layer increases, the quantum efficiency increases but the bandwidth decreases due to prolonged transit length car-

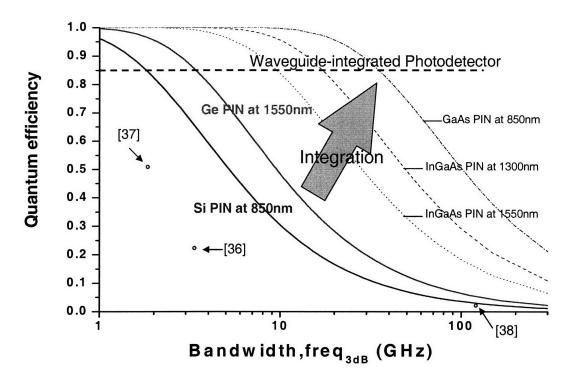


Figure 3-8: Calculated relations between 3dB bandwidth and quantum efficiency of surface-normal incidence discrete p-i-n photodetector structures as in Fig 3-3. The dots represent the reported performance of silicon lateral p-i-n detector demonstrated by other researchers [36–38]. For waveguide-integrated photodetectors (dashed line), the efficiency is independent of the bandwidth in principle. A 85% coupling efficiency is assumed in this graph.

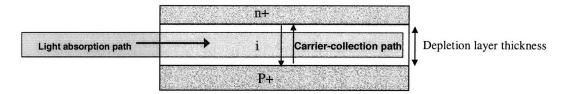


Figure 3-9: The waveguide-integrated photodetector structure.

riers have to travel, and vice versa. Fig. 3-8 shows that, due to its low absorption coefficient, especially group IV materials do not perform as well as compound semiconductor photodetector in terms of the bandwidth-quantum efficiency product, a Figure-of-merit for photodetector performance. For example, silicon p-i-n photodetector can never achieve high bandwidth and efficiency simultaneously using surfacenormal incidence designs. This is the case not only for vertical p-i-n photodetector design but also for lateral p-i-n photodetector structures, as demonstrated by other researchers [36, 38, 39].

A waveguide-integrated photodetector can have a photon-absorption path and a carriers-collection path perpendicular to each other as shown in Fig. 3-9. By decoupling the bandwidth and efficiency issues, it is possible to overcome the bandwidth-efficiency trade-off problem and maintain high efficiency while achieving high bandwidth. Because of the long absorption length of 850nm light in silicon, the benefits of a waveguide-coupled photodetector will be more significant for silicon than for III-V semiconductors in general. Generally, group IV materials, whose absorption coefficient are small at the wavelength of interest, will benefit greatly from the integration with the waveguide.

3.4 Coupling Structure of Waveguide and Photodetector (Butt-Coupling vs. Evanescent-Wave Coupling)

There are two major possible coupling structures for the integration of waveguide and photodetector. Fig. 3-10 shows the butt-coupling structure, where the waveg-

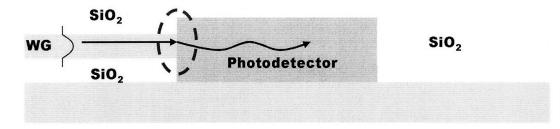


Figure 3-10: A schematic of butt-coupling structure. A dotted circle points to the interface area that is most important for coupling.

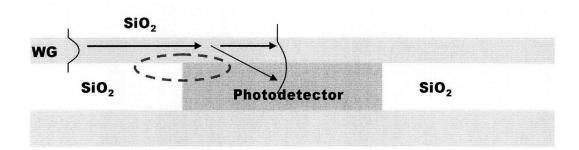


Figure 3-11: A schematic of evanescent-wave coupling structure. A dotted circle points to the transition from the input waveguide to coupling region.

uide terminates with the vertical wall of photodetector material such that a propagation mode in the waveguide directly enters photodetector. And, Fig. 3-11 shows the evanescent-wave coupling structure (also referred to as "leaky-wave coupling" or "vertical coupling"), where the cladding material of the waveguide on one side is replaced with photodetector material in the coupling region such that evanescent-wave of the mode in the waveguide radiates into the photodetector, whose refractive index is higher than that of the waveguide.

In a butt-coupling structure, the coupling behavior is rather simple. Once the waveguide mode enters the photodetector material, the absorption of light occurs at the same rate as specified by the absorption coefficient of bulk material. Therefore, the length of photodetector can be short, like 5 μ m length for a Ge photodetector at 1550 nm or 30 μ m length for a Si photodetector at 850 nm for example. Since the waveguide-photodetector interface is placed perpendicular to the direction of light

propagation, the reflection as much as

$$\Gamma = \left(\frac{n_{eff,WG} - n_{PD}}{n_{eff,WG} + n_{PD}}\right)^2 \tag{3.57}$$

, where $n_{eff,WG}$ is the effective index of the waveguide mode and n_{PD} is the refractive index of photodetector material, can occur and the reflected light propagates back in reverse direction through the waveguide. This back-reflection may cause the trouble in the optical system.

Another challenge for butt-coupling structure could be the fabrication process. The coupling scheme requires that waveguide and photodetector should be located in the same height level. But, fabricating two structures composed of different materials such that they directly face each other in the same level could be difficult. Especially clean-cut vertical interface between waveguide and photodetector, or inserting a desirable vertical anti-reflection(AR) layer in the interface to reduce back-reflection, is hard to achieve.

Evanescent-wave coupling structure is more accommodating in terms of fabrications. The waveguide and photodetector can be placed in different levels. In an evanescent-wave coupling structure, unlike butt-coupling, photons do not couple from the waveguide to the photodetector all at once, but rather gradually by radiation of the waveguide mode. Therefore, the required photodetector length for coupling tend to be greater than that for butt-coupling. How much coupling length is required, i.e. the coupling rate, can be controlled by the materials choices, the waveguide and photodetector design, the thickness of spacer material between waveguide and photodetector, etc.

Although the waveguide extends over the entire photodetector length until all photons are coupled to the photodetector, the most important part would be a transition area from the input waveguide to the waveguide-photodetector coupling region, as indicated in Fig.3-11. It is because the propagation mode of the waveguide can experience a sudden mode disruption as it enters the coupling region. This area is a place susceptible to the photon scattering and back-reflections. In summary, compared to the butt-coupling, the evanescent coupling structure is a preferable structure for the photonic integrated chip. However, it has more design variables and issues to study, such as the coupling rate, coupling efficiency, light scattering, back-reflection etc. To study how to design and control such issues will be the topics in the following chapters.

Chapter 4

Silicon Integrated Photodetector via Evanescent-wave Coupling

Understanding the photon coupling behavior between waveguide and photodetector material such as Si and Ge is an essential part of developing the integrated photodetectors. In this chapter, we chose the SiON waveguide and Si photodetector as an example case to help us understand the evanescent-wave coupling in Si-based waveguide and photodetector materials.

Although evanescent wave coupling structures are also found to be popular coupling schemes in several studies of III-V compound semiconductor waveguides and photodetectors [40–42], the evanescent coupling behavior in Si-compatible materials can be quite different from that in typical compound semiconductor cases, due to their larger index difference between waveguide and photodetector materials.

In this chapter, we will present the experimental results that monolithically integrates compact SiON channel waveguides and silicon vertical p-i-n photodetectors. We studied the coupling rate and efficiency in the evanescent wave coupling structures and investigated mode-matching issues in the coupling structure and the effect of waveguide index-contrast design on the coupling behavior.

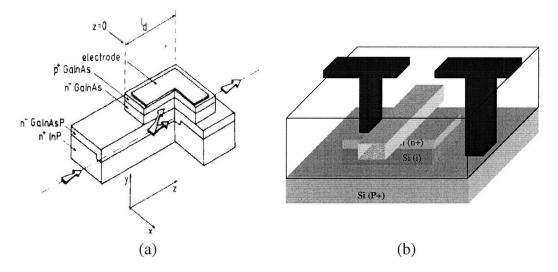


Figure 4-1: Schematic view of (a) an typical waveguide-integrated photodetector made of III-V compound semiconductor materials and (b) SiO_xN_y waveguide-coupled Si photodetector that we fabricated.

4.1 Device Fabrication and Measurement

In the III-V substrate process, the structure generally consists of waveguide and photodetector materials sequentially grown by a hetero-epitaxial process and the refractive index of waveguide and photodetectors are controlled by band-gap engineering, as shown in Fig. 4-1(a). Thus the photodetector sits on the waveguide and evanescent-wave coupling occurs from bottom waveguide to an upper photodetector.

On the contrary, choosing dielectric material such as silicon oxynitride for waveguides requires that the silicon photodetector should be fabricated first, followed by the waveguide on top of the photodetector (Fig. 4-1(b)), unless we elect to fabricate poly-crystalline silicon photodetector by depositing a poly-Si film on top of the dielectric waveguide, which will suffer from high dark current and great noise [43]. Due to these materials and structural differences in silicon-based systems, a different fabrication process needs to be developed.

The fabrication process we developed is schematically outlined in Fig.4-2. The starting substrate was p-type (0.01-0.02 $\Omega \cdot \text{cm}$) silicon with a 5-6 μ m thick lightly p-doped (16-24 $\Omega \cdot \text{cm}$) top Si epitaxial layer [Fig.4-2(a)]. After the epitaxial layer

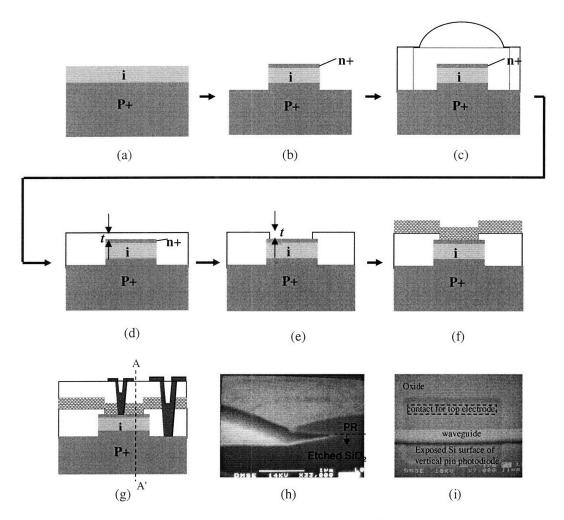


Figure 4-2: (a)-(g) Schematic of fabrication process flow for SiON waveguideintegrated Si photodetector structure (not scaled). (h) Cross section view of slopeetched oxide applied to some samples in order to replace the abrupt step at the process (e). (i) Top view SEM image of the device after step (f) and before step (g).

was etched down to 0.5μ m remaining thickness by plasma dry etch, phosphorus was implanted with 100KeV energy and a dose of 3×10^{15} /cm². Silicon vertical p-i-n diodes were patterned by a 2.2 μ m plasma dry etch using Cl₂ gas [Fig. 4-2(b)]. 2.2 μ m deep etching was for securing enough separation of waveguide from the Si substrate in order to prevent substrate-coupling loss of the waveguide. Then 3.5μ m SiO₂ was deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD) [Fig.4-2(c)], followed by planarizing the top surface by Chemical-Mechanical Polishing (CMP). The thickness of the remaining oxide layer on top of the silicon photodetector was evaluated by ellipsometry measurement on larger monitor features positioned close to photodetectors. The oxide layer was further reduced to the desired thickness by a timed CHF₃ plasma etch on the flat silicon oxide film [Fig.4-2(d)]. This was followed by patterning and opening an oxide window to expose the top silicon surface such that the waveguide can be in direct contact with silicon photodetector for higher evanescent-wave coupling rate [Fig.4-2(e)].

The opening of oxide window following the CMP process, in process (e) of Fig.4-2, results in an abrupt step t in the waveguide at the transition interface to the coupling region, which is apparent in the SEM image [Fig. 4-2(i)]. We fabricated samples with various step heights t from 0.1μ m to 0.3μ m and we also generated a vertical taper of oxide on additional samples, in order to achieve the smooth transition of the waveguide to the coupling region. In order to obtain the vertical taper, we conducted high-energy ion bombardment onto the silicon oxide layer by using a Si dry-etching recipe after process (d) of Fig.4-2 and opened the oxide window by BOE wet-etching (Fig. 4-2(e)). An increased lateral etch rate of the ion-damaged oxide resulted in the sloped surface of the oxide, as shown in Fig.4-2(h).

The above processes complete the platform on which we could put waveguide for coupling with photodetector. SiON waveguide core material was deposited by PECVD. Unlike conventional SiON deposition process [19,44], N₂ gas instead of NH₃ was used as nitrogen source in order to reduce hydrogen incorporation and N-H bond formation during the deposition. This enables us to achieve the low loss without high-temperature post-deposition annealing [26, 45]. After the lithography process,

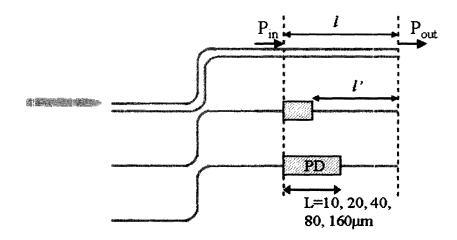


Figure 4-3: schematic design layout of waveguides and photodetectors on the chip.

waveguide etching was done using C_2F_6 and CH_3F gas. A 2.2 μ m-thick upper cladding SiO₂ layer was deposited, followed by opening contact holes. Aluminum with 2% silicon was next deposited by sputtering deposition. After the metal contact pads were patterned and etched, the wafers were annealed at 400°C for 30 min in N₂/H₂ forming gas.

In order to measure the coupling efficiency and the coupling rate between the waveguide and photodetector, both reference waveguides and waveguides integrated with the photodiodes in different lengths were fabricated in parallel on the chip (Fig.4-3). While injecting 830 nm CW light to the cleaved waveguide input facet, we simultaneously measured the photocurrent from the photodetector, I_{ph} , at -2V reverse bias and the remaining optical power from the output facet of the through waveguide, P_{out} . The input position of the waveguide was designed to be offset from the position of photodetector and the output waveguide by implementing two bends, in order to prevent any uncoupled or stray light from the fiber from entering the device and affecting the measurement. In order to obtain reliable data, it is very important to achieve high waveguide-to-waveguide uniformity of input coupling efficiency and waveguide loss. Alignment from the fiber to the sample was precisely controlled with a piezoelectric 3-axis translation stage. The standard variation of transmitted optical power through multiple waveguides was measured to be typically about 5 % of the average. Any measurement data from the sample that exceeded this 5% standard,

which we believe occurs mainly due to poorly-cleaved input facet, was discarded and not used in this paper.

Mode coupling efficiency η and the quantum efficiency are obtained in the following way. $P_{out(WG-PD)}$, the measured optical power at the output of the waveguide coupled with photodetector of length L will have the following relation.

$$P_{out(WG-PD)} = P_{in}\eta_{in}exp(-\alpha_{coupling}L)\eta_{out}10^{-\gamma l'/10}$$
(4.1)

where P_{in} is the optical power at the point of entering photodetectors. η_{in} and η_{out} are the mode coupling efficiency between the waveguide mode and the mode in the waveguide on the photodetector in the coupled region when photons enter the photodetector and exit from the photodetector, respectively. L is the detector coupling length and $\alpha_{coupling}$ is the coupling rate from the waveguide to Si photodetector. γ is the waveguide loss in terms of dB/cm and l' is the distance from the photodetector to the output facet of the through waveguide. $P_{out(WG)}$, the optical power from the reference waveguide without photodetector is

$$P_{out(WG)} = P_{in} 10^{-\gamma l/10}.$$
(4.2)

Normalizing (4.1) by (4.2), we obtain

$$P_{out(WG-PD)}/P_{out(WG)} = \eta^2 exp(-\alpha_{coupling}L)$$
(4.3)

, where η_{in} and η_{out} are assumed to be equal and l and l' are put equal as well because the difference (l - l') ($\leq 160 \mu m$) was negligible compared to l (typically, 1.5mm) in our sample.

Measurement data from the sample with a n=1.52, $1.2\mu m \times 1.2\mu m$ waveguide design and step height of $t = 0.1\mu m$ (sample no.1 in Table 1) are shown in terms of $P_{out(WG-PD)}/P_{out(WG)}$ as a function of detector length L in Fig. 4-4. Five data points were well fitted with the equation (4.3), showing that once incoming photons get coupled to the mode in the waveguide on the photodetector with 86.3% mode-

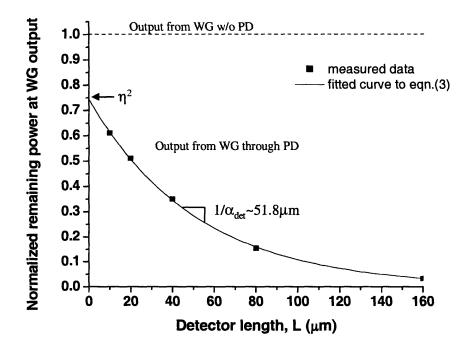


Figure 4-4: Measured optical power data through the waveguides coupled with photodetectors of different lengths, from the sample no.4 (Table 1).

matching efficiency, the remaining power in the waveguide decreases at $\alpha_{coupling} = 1/52\mu m^{-1}$ rate. Because the coupling rate to silicon is much larger than the scattering loss rate of the waveguide on the photodetector, the power decrease in the waveguide on the photodetector is mainly the coupling into Si. Enough long photodetector devices will absorb nearly all of photons that are coupled into the waveguide on the photodetector (For example, 200 μ m long detector absorbs 98%). Also, the rest 14% photons, which were not coupled from the input waveguide to the waveguide on the photodetector, are not all lost and some of them enter silicon, as will be discussed later. Therefore, the total coupling efficiency of photons from the incoming waveguide to silicon photodetector is well above 90%.

Another important parameter is the quantum efficiency of the integrated photodetector. Quantum efficiency is defined as follows.

$$Q.E = \frac{h\nu}{q} (I_{ph}/P_{in}) = \frac{h\nu}{q} (I_{ph} 10^{\gamma l/10}/P_{out(WG)})$$
(4.4)

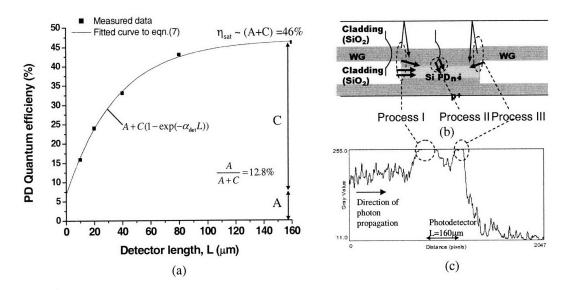


Figure 4-5: (a) Quantum efficiency of waveguide-coupled photodetector vs. detector length from sample.no.4 (Table 1) (b) Schematic of waveguide photodetector coupling device structure and photon absorption process (c) Intensity profile of scattered photons along the waveguide, taken from the top-view CCD camera image of the sample.

Measured quantum efficiency data as a function of detector length are shown in Fig.4-5. In determining a fitting function, we need to consider that there are multiple ways that photons can take until being fully absorbed in Si and contributing to photocurrent generation and that each path has a different dependence on the detector length L. We can reasonably categorize them into three main processes.

Process I : This process refers to all possible ways that photons enter silicon instead of first being coupled and settled to the mode in the waveguide on the photodetector. This process occurs at the very first part of the photodetector, around the transition interface from the input waveguide to coupled region. Some part of incoming photons can directly hit and enter silicon from the side, i.e. in a similar way to butt-coupling. Or, even after photons enter the waveguide momentarily, some photons radiates to silicon quickly without settling into the waveguide mode on top of silicon. Or some photons that were scattered to elsewhere (e.g. toward top surface) may be reflected back and end up entering silicon. Photocurrent component resulting from Process I, $I_{ph,I}$ can be expressed as follows.

$$I_{ph,I}(L) \cong P_{in}(1 - \eta_{in})C_1R_1f(L)$$
 (4.5)

where C_1 is the undetermined ratio of the photons entering silicon out of total uncoupled photons. R_1 is the internal responsivity of the detector resulting from this process. Since photons require some path length to be fully absorbed in silicon, f(L)is the function that increases from zero and saturates into 1 with detector length L. Since Process I consists of many different absorption path, C_1 , R_1 , and f(L) should be reflection of the combined effect of each different absorption process.

Process II : Evanescent wave coupling. Once the photons are coupled into the waveguide mode on top of the photodetector, the light in the waveguide will leak into silicon photodetector at a constant rate. Therefore,

$$I_{ph,II}(L) \cong P_{in}\eta_{in}(1 - exp(-\alpha_{det}L))R_2$$

$$\tag{4.6}$$

where R_2 is the responsivity that silicon photodetector has for this absorption process.

Process III : At the exiting interface, the light in the waveguide on the photodetector don't get fully coupled back into the mode in the output waveguide. Part of uncoupled light can be scattered back into Si.

These different absorption processes are schematically depicted in Fig.4-5(b).

Contribution to photocurrent from process III should be significantly smaller than those from process I and process II. Photocurrent from Process I saturates much more quickly with detector length than that from process II does, because the coupling to silicon in Process I occurs nearly instantly at the front of the photodetector and the absorption length inside silicon in lateral direction $1/\alpha_{x,I}$ cannot exceed at most $1/\alpha_{Si}$, which is about 14μ m at 830nm. Therefore, we can create a simplified form by assuming the photocurrent from process I to be nearly a constant term, especially because the data used are from the sample with $L \geq 10\mu m$. Therefore,

$$I_{ph}(L) = I_{ph,I}(L) + I_{ph,II}(L) + I_{ph,III}(L) = A + C(1 - exp(-\alpha_{det}L))$$
(4.7)

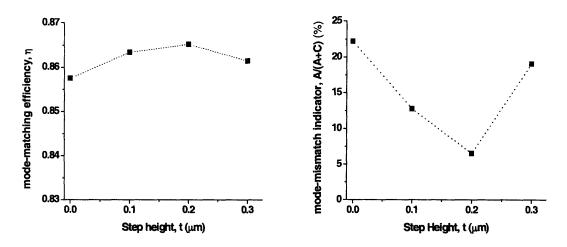


Figure 4-6: mode-matching efficiency η and mode-mismatch indicator A/(A+C), as defined in Fig.4-4 and Fig.4-5(a) respectively, from the samples with different step height t.

The term (A+C) represents the saturated photocurrent or the saturated quantum efficiency when normalized with incoming optical power. In addition, A/(A+C) can be used as a parameter that indicates how dominant Process I is in the whole photon absorption process, and in turn shows how large the mode-mismatch from the input waveguide to the waveguide on silicon is. These parameters, when (4.7) is fitted with measured data from sample no.1, are shown in Fig.4-5(a).

We had various samples sets that have three different waveguide designs and the step height t variation at the transition interface. The measured and fitted data from the samples are summarized in Table 1.

4.2 Effect of Step Height Variation; Mode-Matching Issue

As Fig.4-5(c) shows, process I and process III, which are the results of the modemismatch between input/output waveguide and coupling region, are related to photon scattering. In general, it is desirable that scattering of photons is minimized as much as possible in order to reduce optical energy loss and prevent the malfunction and noise in the nearby devices caused by scattered photons. In Fig.4-6, we re-

$1/\alpha_{coupling}$ fitting A	fitting C (ex-	fitting (fit-	(%)	Q.E (A+C)
	ponential	ted		(%)
term)	term)	• •		
		(un)		
5.96	40.68	35.2	12.8	46.64
3.02	43.16	23.4	6.5	46.18
9.27	39.33	38.5	19.1	48.60
10.16	35.57	38.5	22.2	45.73
1.43758	0.79249	28.58	64.44	
17.35 0.38338	0.234	18.36	62.1	
_	0.38338		0.134	0.234 26.36

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plotted the value of mode-matching efficiency parameter η and mismatch indicator A/(A+C) from Table 1, in terms of step height t variation of the samples with the same waveguide design (samples no.1-4). η maintains relatively stable values from $t = 0 \mu m$ to $t = 0.3 \mu m$, with a slightly higher value for the sample with $t = 0.2 \mu m$. Even the sample at $t = 0.3 \mu m$ still maintains the high η value, even though the abrupt step at the transition is as much as a quarter of total waveguide height. In addition, the plot of mode-mismatch indicator A/(A+C) in Fig.4-6(b) also shows that the mode-mismatch apparently reaches the minimum at $t = 0.2 \mu m$. Certainly, the smooth transition of waveguide with no abrupt step would not be best for mode-matching.

The experimental observation in Fig. 4-6 can be supported by optical simulations. 3D FDTD results in Fig.4-7 show that the propagation mode in the waveguide experiences an upward shift as it enters the coupling region, where the SiO₂ undercladding is replaced by silicon. The mode formed inside the waveguide in the coupling region is not a confined mode but a leaky-mode (or semi-confined mode) [46] with slow leakage (i.e. coupling) rate (e.g. $\alpha_{coupling} \sim 1/50 \ \mu m^{-1}$ in our sample). Due to the shape and position mismatch of the up-shifted leaky mode in the coupling region with the mode in the input waveguide, the coupling structure without step has some significant mode-mismatch.

The up-shift of the leaky mode in the coupling region can be understood by using analytical mode calculations. As an approximation, we converted the 3D coupling structures to 2D multilayer structures by applying the Effective Index Method (EIM) and then calculated the mode profile by applying the transfer matrix method in a multilayer structure with complex refractive indexes [47]. Fig. 4-8(a) shows that, unlike a symmetric mode in the input waveguide, the mode profile in the coupling region has its electric field fixed to have zero value at the interface between waveguide core material and the underlying silicon. TE light undergoes $-\pi$ phase shift when the light incident from lower-index material (the waveguide material in our device) is reflected at the interface with higher-index material (silicon in our device). In addition, a small reflection angle of the mode in the low-index contrast waveguide and

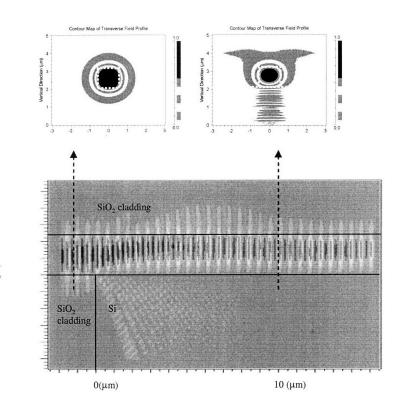


Figure 4-7: 3D FDTD side-section view (lower picture) of photon propagation in the coupling structure where waveguide has no step as it enters the coupling region. Cross-section view (upper pictures) of the mode profile in the waveguide before and after coupling. The mode in the waveguide on Si is asymmetrically shifted upward, compared to that of input waveguide.

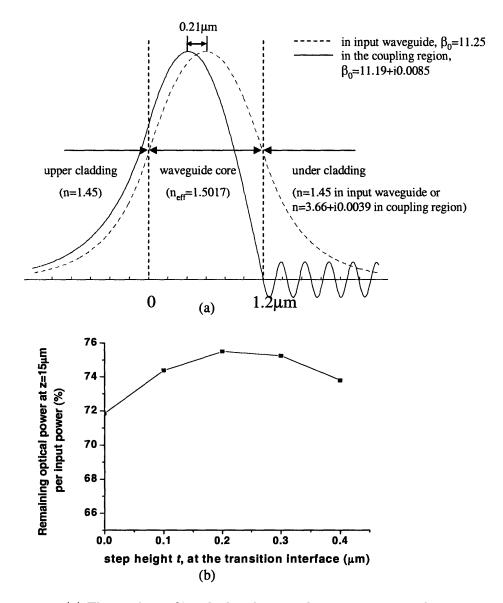


Figure 4-8: (a) The mode profile calculated in a multilayer structure where waveguide material is in contact with bottom oxide cladding layer or silicon absorbing layer (b) 3D FDTD simulation results, which shows the fraction of optical power remaining in the structure after 15 μ m coupling length vs. step height t

the large index contrast between the waveguide core and silicon make the absolute value of the reflection coefficient close to one. With reflection coefficient being close to -1, the incident and reflected wave at the interface nearly cancel each other, resulting in zero electric field at the interface. Due to this effect, the overall position of the mode in the waveguide in contact with silicon is shifted away from silicon. Fig.4-8(a) furthermore shows that the peak positions of the two modes, one in the input waveguide and the other in the coupling region, are 0.21μ m apart.

The step of the waveguide at the transition to the coupling region can compensate for the mode shift that results from the proximity to Si and therefore achieves a better mode-match. The experimental result in Fig.4-6 showed that a 0.2 μ m step is the optimal offset for best mode-matching. The modeling in Fig.4-8 supports that result as well. 3D FDTD simulation results in Fig.4-8(b) show that the coupling structure with 0.2 μ m offset experiences the least scattering at the transition interface to the coupling region thus has more power remaining in the structure after a certain length than other samples, which lost more light due to scattering as a results of modemismatch.

4.3 Coupling with High Index-Contrast Waveguide

The evanescent coupling behavior from the waveguide to the photodetector greatly depends on the waveguide design. We had sample 5 and 6, in which waveguide have higher refractive-index core materials and core sizes are smaller with flat rectangular shape, compared to lower-index waveguides. The coupling behavior of the higher index-contrast waveguides shown in Fig.4-9 is different from that of the lower index waveguide in that 1) the mode-matching efficiency η estimated from the measurement data are much lower with $\eta \sim 24.2\%$ and $\eta \sim 15\%$ for sample 5 and 6, respectively, 2) the mode mismatch indicator A/(A+C) is much higher, indicating that higher percentage of the incoming optical power is absorbed in the front part of the photodetector close to the transition interface, 3) the exponential characteristic length $1/\alpha_{coupling}$ is much shorter, indicating the evanescent wave coupling rate is higher, 4)

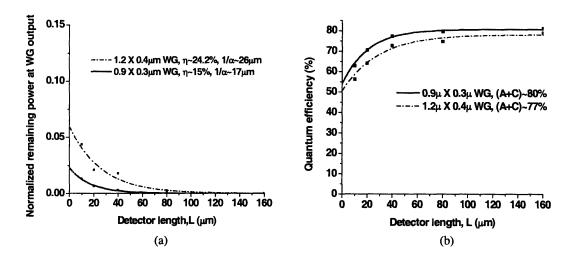


Figure 4-9: Measurement and fitted data of (a) normalized optical power output through the waveguides coupled with photodetectors (b) quantum efficiency of waveguide-coupled photodetector vs. detector length. Samples are no.5 and no.6 from Table 1.

saturated quantum efficiencies of long photodetectors are much higher compared to those in the coupling device with low-index contrast waveguide.

The ray-trace view of the propagation mode in waveguide can qualitatively explain the higher evanescent coupling rate in high index contrast waveguide. The higher refractive index of the core material, the greatly reduced dimensions especially in the vertical direction, and the greater portion of the mode perimeter being in contact with silicon can be translated to a ray's more frequent attempt of transmission into Si with smaller incident angle and less reflection at the waveguide/silicon interface, resulting in higher evanescent coupling rate to be higher.

As for higher index-contrast waveguide, the mode size in the waveguide is much smaller and the confinement factor is lower with more optical energy existing in the cladding material, compared to lower index-contrast waveguide. Therefore, the impact of silicon replacing SiO_2 at the transition from the input waveguide to the coupling region is greater and it is more difficult to achieve mode-matching between the guided mode in the input waveguide and the leaky mode in the waveguide in the coupling region. Simulation of this structure (Fig.4-10(a)) shows that, at the transition interface to coupling region, the significant portion of light from the in-

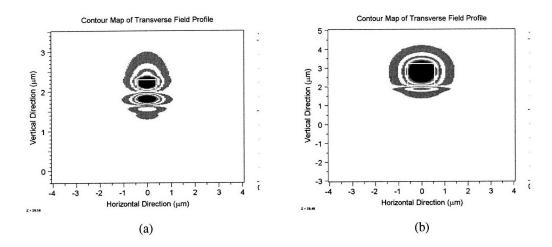


Figure 4-10: Cross-section view of the mode profile at $z=0.5 \ \mu m$ after coupling begins. (a) In the coupling structure with smaller high-index waveguide with flat rectangular shape (sample 6 in Table.1) (b) In the coupling structure with lower-index contrast waveguide with larger square dimensions.

put waveguide enters silicon directly instead of first being coupled to the mode in waveguide on the photodetector, whereas only a small portion of photons do so in low index-contrast waveguide case (Fig.4-10(b)). As photons that entered the waveguide also quickly leak into silicon, most photo-absorption occurs in the front part of photodetector. Therefore, the concept of the leaky-mode formation in the waveguide on silicon, which was effective in previous low index-contrast waveguide case, is less applicable here.

Process I being the dominant process of the absorption process can explain higher saturated quantum efficiency in higher index-contrast waveguide case, shown in Fig.8(b). Our Si photodetector has a quantum efficiency of 41% for 830 nm light under surfacenormal, free space illumination, which indicates the diffusion of carriers from up to about 7 μ m below the surface is responsible for photocurrent. Under that situation, process I, in which the light from the input waveguide enters silicon directly from the side largely in lateral direction without being coupled to the mode in waveguide on the photodetector, can have most light absorbed before reaching 7 μ m depth, leading to higher quantum efficiency. On the contrary, the evanescent coupling (process II) from the leaky mode in the waveguide towards silicon should have a light path that resembles the top surface-normal illumination and achieve the similar degree of quantum efficiency. In other words, R_2 as defined in equation (4.6) should be close to 41% efficiency of Si photodetector with surface-normal illumination, whereas R_1 as defined in equation (4.5) is much larger than that. For these reasons, the coupling structure with compact higher index-contrast waveguide, where Process I is the dominant process of photon absorption, had greater quantum efficiencies of up to 77% and 80% for sample 5 and sample 6, respectively, whereas the saturated quantum efficiencies of sample 1-4, where process II is a dominant process of photon absorption, were $46\sim48\%$, which is only slightly higher than the efficiency of Si photodetector with surface-normal illumination.

4.4 Conclusion

We have demonstrated waveguide-integrated silicon photodetectors that employ the top-to-bottom evanescent-wave coupling structures. We achieved over 90% photon coupling efficiency from SiON waveguide to Si photodetectors. From observations of experimental data, we could identify a few different ways that photons couple from waveguide to photodetector and investigate their changes influenced by coupling device design. A two-step process that consists of 1) mode-coupling from a guided mode in the input waveguide to a leaky mode in the waveguide in contact with photodetector and 2) gradual evanescent wave coupling from waveguide towards photodetector, was a main coupling mechanism in the case of coupling with lower index-contrast waveguide, in contrast to high index-contrast waveguide case where coupling occurred nearly instantly at the front part of photodetector. It was shown that intentional introduction of abrupt step in the waveguide at the transition interface to coupling region can improve mode-matching efficiency. The total quantum efficiency of integrated photodetector (46-48%, especially in coupling structure with low index-contrast waveguide) was repressed by the limited internal quantum efficiency of photodetector itself (41% with surface-normal illumination), in spite of very efficient coupling efficiency from waveguide to photodetector. However, the efficient evanescent coupling structures developed with silicon-based photonic materials in this work, if combined with improved photodetector design, will provide an important building block for silicon-based electronic-photonic integrated circuitry.

Processes and knowledge developed in this paper can be readily expanded to a broad range of coupling structures between dielectric waveguides such as silicon oxynitride and silicon nitride and silicon-based semiconductor photodetector such as Si, SiGe and Ge.

Chapter 5

Evanescent Wave Coupling with Thin Absorbing Layer

Waveguide-coupled Si photodetectors presented in Chapter 4 were fabricated mainly for the purpose of investigating coupling issues between waveguides and photodetectors and had a very slow response. The slow response of the photodetectors was due to the fact that the diffusion current, resulting from carrier absorption far below the intrinsic layer (it was estimated the diffusion length was about 7 μ m), was responsible for most of the photocurrent.

Therefore, it is necessary to use only a thin photodetector layer and minimize the p^+ and n^+ layer thicknesses in order to avoid the diffusion current. For a Si photodetector, a SOI substrate can provide a thin Si crystalline layer for a high-speed photodetector. Also, compared to discrete photodetectors used with normal-incident light, the integration with a waveguide can enhance the efficiency.

However, some initial optical coupling simulations with a SOI photodetector revealed that the expected efficient coupling to SOI layer did not occur, as shown in Fig.5-1. Although the waveguide was in direct contact with the absorbing material, photons remained in the waveguide without being coupled to the photodetector. A few attempts to vary the design parameters did not change the inefficient coupling significantly. We have realized that a different physical view is required to understand the photon coupling behavior when a photodetector absorbing layer is much

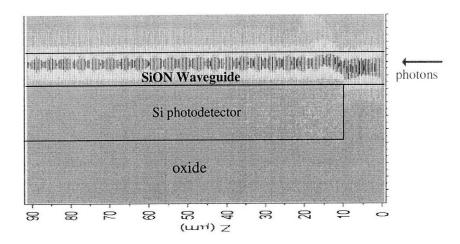


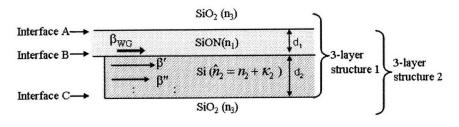
Figure 5-1: FDTD simulation of the coupling structure with 1.0 μ m SiON waveguide and 1.6 μ m Si layer on oxide.

thinner than the absorption length, $1/\alpha_{absorption}$, of the material. Because optical simulations with a few arbitrary dimension inputs do not seem to produce the acceptable coupling results easily, a design guide that we can rely on when designing a waveguide-integrated photodetector is necessary.

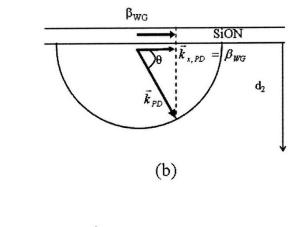
In this chapter, we developed a simple and intuitive model using a ray-optics approach to determine the conditions for efficient coupling both in 2D and 3D structures. It will be shown that the phase matching between the waveguide and the Si layer is the key condition for efficient coupling. We will also investigate the dependence of coupling efficiency on design parameters such as the Si layer thickness, the refractive index and thickness of a waveguide layer.

5.1 Introduction

The structure we modeled is shown in Fig.5-2 (a). We have chosen 850nm for modeling because it is the most widely-used wavelength in the absorption range of Si, due to the availability of an inexpensive light source. Silicon oxynitride (SiO_xN_y or SiON for short) was chosen as waveguide material because SiON is compatible with silicon microelectronics processing and provides flexibility in choosing the refractive index. Most theoretical and experimental studies of coupling behavior in waveguide-coupled



(a)



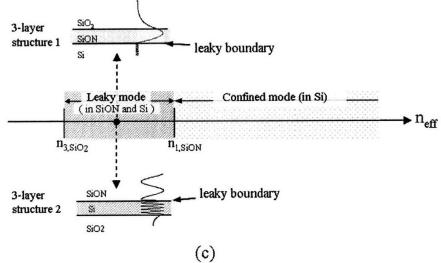


Figure 5-2: The graphical representation of evanescent wave coupling mechanism in (a) a waveguide-to-thin layer coupling structure ($d_2 <<$ absorption length of Si) vs. (b) waveguide-to-thick medium coupling structure ($d_2 >>$ absorption length of Si). (c) For efficient coupling, the effective index of the mode both in SiON and Si layer, must fall in the range where $n_{3,SiO2} < n_{eff} < n_{1,SiON}$ to be leaky modes. Exemplary leaky mode profiles are shown in insets. Coupling rate will be maximum when two modes have the same propagation constants.

photodetector so far concentrated on III-V semiconductor systems [40,42,48,49]. Our structure has different characteristics in that the refractive index difference between waveguide and detector is large and the Si layer thickness is much smaller than the absorption length ($1/\alpha$) of Si at 850nm. Batchman et al. [50] have analyzed the mode coupling in waveguides with poly-silicon cladding for polarizer applications. They have shown an oscillatory dependence of the dielectric waveguide mode attenuation constant on the semiconductor cladding thickness. In contrast, our structure shows resonance-like dependence, as will be shown in this chapter, due to the different design for photodetector application. A mode analysis approach based on the transfer matrix method [47,51] has previously been used to predict the coupling behavior and effective absorption rate in a multilayer structure [48–50]. While a mode analysis approach can treat complicated structures with arbitrary complex refractive indices as a whole, it requires solving the equations in a complex plane. Furthermore, obtaining a solution successfully depends on the selection of the initial value [52]. In order to simplify the approach, we regarded the structure as a combination of two adjoining individual waveguides. We used a simple ray optic model to determine the propagation constant for each waveguide. We will show that phase matching between these two waveguides is a determining factor for efficient coupling and subsequent absorption in the Si layer. The results were compared with 2D/3D BPM/FDTD optical simulations and modal analysis results calculated by a transfer matrix method [47].

5.2 Modeling and Analysis; Phase-Matching Issue

In waveguide-coupled photodetector designs using compound semiconductor materials whose absorption coefficient is high at the typical operation wavelength, the absorbing layer is often designed to be a multiple of the absorption length. In contrast, for our device structure, the absorbing layer must be designed to be much thinner than the absorption length to reach a high speed response (>GHz) [36]. In this case, the thin Si layer effectively behaves as a lossy waveguide, exhibiting certain propagation modes (Fig.5-2 (a)). The waveguide-detector coupling can be treated as a coupling between two waveguides. Phase matching should be a determining condition for efficient coupling and coupling may show discrete efficiency peaks depending on device design parameters. This is in contrast to the more usual waveguide-coupled photodetector designs that employ waveguide-to-thick medium coupling. In that case, the phase is easily matched because the propagation vector in the waveguide, β_{WG} always find its counterpart propagation vector $|\vec{k}_{PD}| = k_0 n_{Si}$ in Si, whose lateral component $\vec{k}_{x,PD}$ matches β_{WG} (Fig.5-2 (b)). Therefore, in this case the coupling efficiency is much less sensitive to design parameter variations, eliminating the efficiency peaks.

Photons from a SiON waveguide can couple into only one of many modes inside the Si layer (Fig. 5-2(b)). The effective index of a mode in the SiON waveguide is between $n_{3(SiO_2)}$ and $n_{1(SiON)}$ and this mode is leaky towards silicon because silicon has a higher index than the effective index of the mode. However, the decay of the optical energy in the SiON layer due to leakage into the Si is slow, since reflection at the SiON/Si interface is still near 100%. This mode is referred to as "leaky" or "quasi-confined" mode [46]. In order to couple this quasi-confined mode effectively into the Si layer, one of the existing modes in the Si layer has to phase-match the mode of the SiON waveguide. Therefore, the mode in the Si layer has to be also within the index range of $n_{3(SiO2)}$ and $n_{1(SiON)}$ and be a leaky mode towards SiON. A leaky mode does not always exist in the Si layer, but will appear only under specific conditions. Finding these specific conditions will be an essential part of designing the coupling structure.

To find the coupling conditions analytically, we separated the coupling structure of the SiON waveguide and the Si layer on SOI into two individual 3-layer structures and analyzed each with a ray-optics approach. Notations used in the formalisms are shown in Fig.5-2 (a).

As a first step, the TE propagation mode inside the SiON waveguide was obtained by the resonance condition that a wave should reproduce itself after each round trip of internal reflections.

$$\frac{2\pi}{\lambda_0} n_1 2d_1 \sin \theta_1 + \varphi_{1,A} + \varphi_{1,B} = 2\pi m (m = 0, 1, 2, ...)$$
(5.1)

$$\frac{2\pi}{\lambda_0} n_1 2d_1 \sin \theta_1 = -\varphi_{1,A} - \varphi_{1,B} + 2\pi m (m = 0, 1, 2, ...)$$
(5.2)

In equation (5.2), $\varphi_{1,A}$, the reflection phase shift at the upper boundary A, is introduced by total internal reflection, whereas $\varphi_{1,B}$, the reflection phase shift at the lower boundary B, is introduced by reflection from the absorbing medium [53]. Therefore,

$$\tan(-\varphi_{1,A}/2) = \frac{\sqrt{\cos^2 \theta_1 - (n_3/n_1)^2}}{\sin \theta_1}$$
(5.3)

$$\varphi_{1,A} = -2 \tan^{-1}\left(\frac{\sqrt{\cos^2 \theta_1 - (n_3/n_1)^2}}{\sin \theta_1}\right)$$
(5.4)

 $\varphi_{1,B}$ is obtained from

$$\hat{r}_{12s} = |\hat{r}_{12s}|e^{i\varphi_{1,B}} = \frac{\sin\theta_1 - (\hat{n}_2/n_1)\sqrt{1 - (1 - \sin^2\theta_1)(n_1^2/\hat{n}_2^2)}}{\sin\theta_1 + (\hat{n}_2/n_1)\sqrt{1 - (1 - \sin^2\theta_1)(n_1^2/\hat{n}_2^2)}}$$
(5.5)

The left-hand side (LHS) and the right-hand side (RHS) of equation (5.2) with $\varphi_{1,A}$ and $\varphi_{1,B}$ replaced by equation (5.4) and equation (5.5) are drawn in Fig.5-3(a) in terms of reflecting angle $\sin \theta_1$. We used λ =850nm, d_1 =1 μ m, n_1 =1.52, n_2 =3.66+i0.0039 and n_3 =1.45 in following equations and figures. Solving equation (5.2), i.e. finding the intersection in Fig. 5-3(a), determines the modes. Its propagation constant is obtained by

$$\beta_1 = (2\pi/\lambda_0) n_1 \cos \theta_1 \tag{5.6}$$

The propagation constant in the Si waveguide was obtained by neglecting the effect of the imaginary part of the refractive index and treating the Si waveguide as a lossless waveguide. For the purpose of obtaining the real part of propagation constant β_2 , this is an appropriate treatment in the case where higher-order terms of κ^2 can be neglected [54]. Therefore, similarly,

$$\frac{2\pi}{\lambda_0} n_2 2d_2 \sin \theta_2 = -\varphi_{2,B} - \varphi_{2,C} + 2\pi m (m = 0, 1, 2, ...)$$
(5.7)

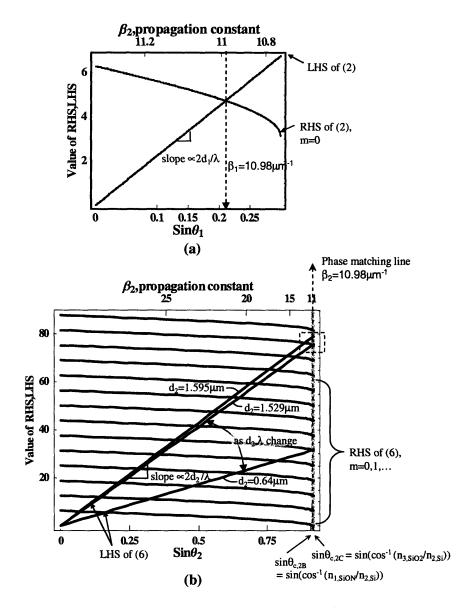


Figure 5-3: Design diagram for optimized coupling: (a) mode-determining equation (5.2) for SiON waveguide, (b) mode-determining equation (5.7) for Si absorbing waveguide. The value of the right-hand side (RHS) and the left-hand side (LHS) of equations are drawn in terms of reflection angle θ .

At the interface B, the reflection phase shift is

$$\varphi_{2,B} = -2 \tan^{-1}\left(\frac{\sqrt{\cos^2 \theta_2 - (n_1/n_2)^2}}{\sin \theta_2}\right)$$
(5.8)

where $heta_2 < heta_{C,2B} = \cos^{-1}(n_1/n_2)$ or $arphi_{2,B}$ is obtained from

$$\hat{r}_{21s} = |\hat{r}_{21s}|e^{i\varphi_{2,B}} = \frac{\sin\theta_2 - (n_1/n_2)\sqrt{1 - (1 - \sin^2\theta_2)(n_2^2/n_1^2)}}{\sin\theta_2 + (n_1/n_2)\sqrt{1 - (1 - \sin^2\theta_2)(n_2^2/n_1^2)}}$$
(5.9)

where $\theta_{C,2B} = \cos^{-1}(n_1/n_2) < \theta_2 < \cos^{-1}(n_3/n_2) = \theta_{C,2C}$.

At the interface C, the reflection phase shift is

$$\varphi_{2,C} = -2 \tan^{-1}\left(\frac{\sqrt{\cos^2 \theta_2 - (n_3/n_2)^2}}{\sin \theta_2}\right)$$
(5.10)

The resulting propagation constant in the Si layer is

$$\beta_2 = (2\pi/\lambda_0) n_2 \cos \theta_2 \tag{5.11}$$

The left-hand side (LHS) and the right-hand side (RHS) of equation (5.7) are drawn in terms of $\sin \theta_2$ in Fig. 5-3(b). At each intersection point representing a propagation mode, $\sin \theta_2$ can be solved and inserted into equation (5.11), thereby obtaining propagation constant. The region of interest in Fig. 5-3(b), is where the effective index of the mode is between $n_{3,SiO2}$ and $n_{1,SiON}$, i.e. $\cos^{-1}(n_{1,SiON}/n_{2,Si}) < \theta < \cos^{-1}(n_{3,SiO2}/n_{2,Si})$ such that a leaky mode towards the SiON waveguide material can exist as explained in Fig. 5-2. This region of interest is magnified and shown in Fig. 5-4(a). As an example, at a Si thickness of $d_2=1.529\mu$ m, a mode exists at the point where the resulting 12th mode in the Si layer has the propagation constant $\beta_2 = 10.98\mu m^{-1}$ thus phase-matches that of the SiON waveguide. At other conditions, for example, as the Si thickness changes to 1.595μ m, the left-hand side (LHS) of equation (5.7) does not intersect with the right-hand side (RHS) of equation (5.7) with m=12 and m=13 in the range of $\sin \theta_{C,B} < \sin \theta_2 < \sin \theta_{C,C}$, far away from phase-matching conditions (Fig.5-4(a)).

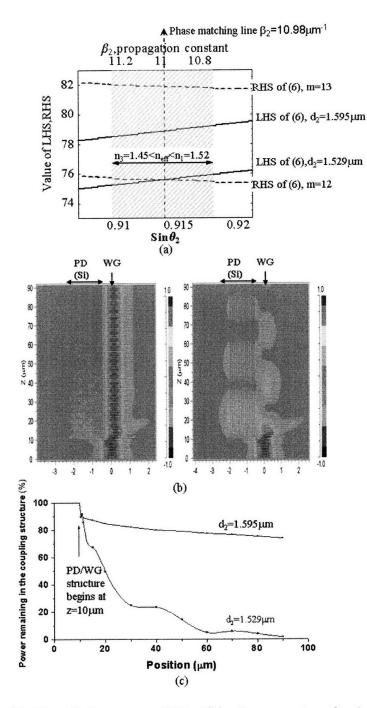


Figure 5-4: (a) Magnified portions of Fig.3(b) where quasi-confined (leaky) modes exist in SiON and Si. With a Si layer thickness of $d_2=1.529 \ \mu\text{m}$, the phase-matching condition is satisfied. (b) 2D FDTD simulation of waveguide and photodetector integration showing the inefficient coupling at $d_2=1.595 \ \mu\text{m}$ and the efficient coupling at $d_2=1.529 \ \mu\text{m}$. (c) FDTD-calculated power remaining in the waveguide-detector structure along the propagating direction, for phase-matched and unmatched conditions.

By viewing this coupling structure as a waveguide-to-waveguide coupling problem, we postulated that phase-matching is a determining factor for the coupling behavior and absorption rate [55]. We verified it by conducting 2D FDTD simulations. The FDTD results are shown in Fig. 5-4(b). As predicted, at a Si thickness of $d_2=1.595\mu m$, which is far from phase-matching, the evanescent coupling into the Si layer is so inefficient that almost no absorption occurs in the Si layer. However, at a Si thickness of $d_2=1.529\mu m$, which satisfies the phase-matching condition, evanescent coupling into Si as well as absorption are very efficient. When an efficient evanescent coupling into Si occurs, the location of the mode oscillates between the waveguide and the Si layer. Accordingly, the absorption rate varies, reaching maxima when the mode propagate in Si layer (Fig.5-4(c)).

In order to further examine the validity of the above analysis as a simple design tool for finding coupling conditions reliably, we compared with FDTD, BPM, and mode analysis. Computational methods such as FDTD or BPM can best simulate the behavior of the photons. Perturbation effects due to mode mismatch between input waveguide mode and waveguide/photodetector mode in the coupling region can be evaluated. However, FDTD and BPM simulation can not provide a good starting point for the device design. Fig. 5-5 shows that our phase matching method agrees very well with BPM and FDTD in predicting the Si thickness d_2 for the best absorption rate. A comparison between d_2 that minimizes the phase mismatch indicator $|n_{eff,SiON} - n_{eff,Si}|^2$ in our approach and d₂ that the maximizes the absorption rate in FDTD and BPM simulations shows less than 1nm discrepancy. While 3D FDTD is the most exact method to model the propagation of light, we could verify that BPM is also a good and much faster alternative to model the coupling structure although it does not take into account reflections and has limitations for high index waveguides. BPM simulations showed almost the same coupling behavior as FDTD in significantly less computing time. However, BPM simulations generated slightly different quantitative results most likely because they do not address back reflections and thus could be inaccurate at the interface between input wayeguide and the waveguide/photodetector coupling region.

Another conventional method, mode analysis, which solves the wave equation of a multilayer structure in a complex plane [40,47,48,50], is used as comparison in Fig. 5-5(b). In the calculation, we used both the algorithm in [47] and a secant method to find a solution of $f(\beta_m + i \alpha_m \lambda_0/4\pi) = 0$ in a complex plane. The attenuation constant α_m was defined as $2k_0 \times (\text{imaginary part of the solution})$. The mode analysis method results also showed good agreement with our approach and BPM/FDTD in finding the optimal Si thickness. A mode analysis is a convenient tool to predict the change of the absorption rate according to the variations of device parameters. However, a mode analysis is not a simple method for finding coupling conditions compared to our phase matching approach because a complex numerical algorithm is required to find a converging solution in the complex plane successfully and it can be challenging or even misleading unless the initial value for the solution algorithm is chosen very carefully. Fig. 5-5(b) shows that even slight variations of the initial value β_0 can produce invalid results. In fact, the first part of our analysis (5.1)-(5.6) is useful also for providing the good initial value that generates solutions simulating coupling behavior correctly. We can understand this from the fact that the value we obtain in (5.6) represents the mode in SiON layer, i.e the source from which a transfer of energy into Si layer occurs.

5.3 Design Consideration

Since it is important to achieve reliable efficiency of a waveguide coupled photodetector, it is necessary to predict the sensitivity of coupling and absorption to possible variations during processing. Three major parameters in design and processing are the Si layer thickness, refractive index, and the thickness of the SiON waveguide material. First, the variation of refractive index and thickness in the SiON waveguide will not change the propagation constant β_1 greatly. We can understand that, from Fig. 5-3(a), the shift of the intersecting point would not change the propagation constant β_1 much, mainly because the refractive index of SiON is small. Therefore, the change in $|\beta_1 - \beta_2|^2$ is relatively small and the coupling efficiency is

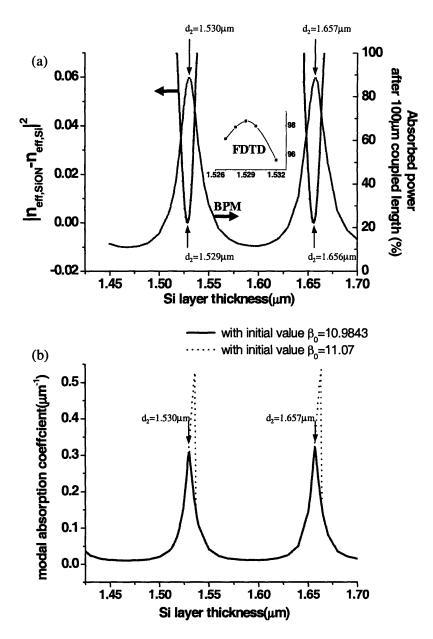


Figure 5-5: (a) Comparison of the Leaky-Mode model vs. BPM/FDTD 1) Our approach: phase mismatch indicator $|n_{eff,SiON}-n_{eff,Si}|^2$ calculated from (5.1)-(5.11) can be used to find the condition that generates best coupling efficiency. 2) BPM simulation: (1-remaining optical energy after 100 μ m coupling length/input power) 100(%), which is mostly absorption, as Si thickness varies. Inset shows FDTD results near peak. Simulated structure includes the input waveguide surrounded by SiO₂. (b) Mode analysis solution, the same method as used by [47, 49, 50]: initial value $\beta_0=10.9843$ was obtained from β_1 in (5.6). Use of a different initial value (for example, $\beta_0=11.07$, close to the propagation constant value in input waveguide) alters the results significantly.

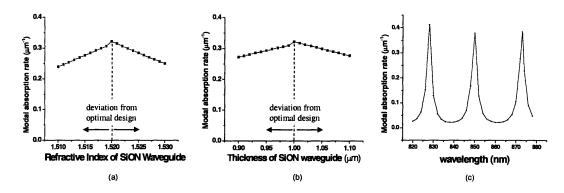


Figure 5-6: (a) and (b) : Dependence of modal absorption coefficient on the refractive index and the thickness of SiON waveguide, respectively. Standard optimal design refers to $n_1=1.52$, $d_1=1\mu m$, $d_2=1.53 \ \mu m$. (b)Wavelength-selective detection ($n_1=1.5$, $d_1=1.1 \ \mu m$, $d_2=4.823 \ \mu m$)

only slightly affected. Mode analysis calculations in Fig. 5-6(a) and 5-6(b) confirm that small deviations of refractive index and thickness of the SiON waveguide from the optimized design decrease coupling efficiencies only moderately. On the contrary, thickness variation in the Si layer will change β_2 greatly, thus affecting coupling behavior drastically. As seen from Fig. 5-3(b) and Fig. 5-4, efficient coupling can only occur when an intersecting point is within a narrow range where $\sin(\cos^{-1}(n_{1,SiON}/n_{2,Si})) < \sin \theta_2 < \sin(\cos^{-1}(n_{3,SiO_2}/n_{2,Si}))$. As d₂ changes (the straight line in the Fig. 5-3(b) rotates), this condition will be only met for a narrow range of d₂, generating the resonance-like coupling dependence, as shown in Fig. 5-5. Therefore, the Si layer thickness is the parameter that has to be controlled during processing very precisely.

A resonance-like coupling dependence can be expected as a function of wavelength as well. Since λ is only included in the left side of equation (5-7), a change in λ will lead to a change of the slope of the straight line in Fig. 5-3(b), thus generating resonance-like absorption behavior. By using this absorption behavior, wavelengthselective photodetectors can be made. Fig. 5-4(b) indicates that a greater Si thickness d₂ will lead to a smaller pitch and FWHM of the absorption peaks in the wavelength scale since the slope of the straight line is proportional to d₂/ λ . For example, a 70µm-long detector structure with a relatively thick silicon layer of 4.823µm absorbs most light at 850nm, but absorbs very little at 840nm (Fig. 5-6(c)).

The coupling behavior is also affected by the refractive index contrast between waveguide and cladding. Fig. 5-7 shows that the coupling rate is enhanced over all regions when a waveguide with higher index contrast is employed. A moderate coupling rate can be achieved even at out-of phase conditions. As a result, resonance-like coupling behavior in small Δn design changes into a more oscillation-like behavior in large Δn designs. To understand this change, we can apply the ray-optics approach. The ray-path angle, which is determined by (5.2), is greater for a higher index contrast waveguide than for a lower index contrast waveguide. For example, $\theta_1 = 25.8^{\circ}$ for $\Delta n=0.35$, while $\theta_1 = 12.1^{\circ}$ for $\Delta n=0.07$. The steeper incidence of light allows more transmission of optical energy into the Si layer. Alternatively, we can take the approach of coupled-mode theory, where we view waveguide-detector coupling as the coupling between two parallel similar waveguides. In the coupled-mode theory, the presence of one waveguide is seen by the other waveguide as a perturbation of the surrounding medium. The presence of a higher Δn waveguide results in a greater perturbation effect and enhances the coupling coefficient [55].

The dependence of coupling behavior on Δn suggests that we can control the coupling behavior well, since SiON provides a wide refractive index range. For an application such as wavelength-selective photodetection, a small Δn design, resulting in resonance-like coupling, will be preferred. For simple photodetection, a higher Δn design may be adopted such that absorption efficiency is not too sensitive to processing variation like Si layer thickness. However, higher Δn requires much better control of small dimensions during fabrication. Therefore, for evanescent coupling the optimal refractive index contrast must be found.

Several authors, who studied the coupling behavior of a waveguide clad with a top amorphous silicon layer for polarizer applications concluded that the most efficient coupling occurs at the cut-off condition of the Si layer [50, 56]. The cut-off condition was defined as the point where a mode in the Si layer changes from a fullyconfined mode to a leaky mode. Based on their conclusions, Marciniak et al. [56] reduced the coupling problem in a 4-layer structure to simply determining the Si

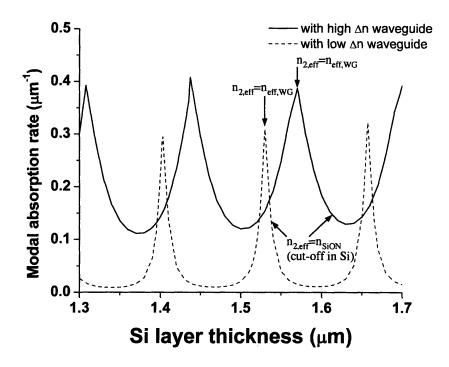


Figure 5-7: Dependence of the modal absorption rate on Si layer thickness in the coupling structure employing a waveguide design with low Δn ($\Delta n=0.07$, $n_1=1.52$, $d_1=1 \ \mu m$) vs. a waveguide with high Δn ($\Delta n=0.35$, $n_1=1.8$, $d_1=0.4 \ \mu m$)

layer cut-off condition thickness in 3-layer structure. However, Fig. 5-7 shows that such an approach will generate results deviating from the optimal coupling efficiency conditions. By following the method in [56] and equations (5.7)-(5.11), we found that the Si layer thickness for cut-off conditions are, for example, $d_2=1.537\mu$ m, 1.665 μ m, etc. for the structure with $\Delta n=0.07$ waveguide and $d_2=1.481\mu$ m, 1.614 μ m, etc. for the structure with $\Delta n=0.35$ waveguide as shown in Fig. 5-7, deviating from the correct coupling condition by about 8nm and 44nm, respectively. Si cut-off condition looks approximate to the highest coupling efficiency condition in low index-contrast waveguide design cases, but not accurate. Si cut-off condition deviates much from optimal coupling condition, especially when the effective index of waveguide mode is much different from the material index of the waveguide, as in high Δn waveguide design case. It will be necessary to follow our approach, which is to find the effective index of leaky modes in waveguide and Si layer and find the conditions where two modes match each other.

5.4 Modeling for 3D Structure

Some waveguide-coupled photodetector devices will require full 3-dimensional evaluation of the coupling behavior. All concepts that have been developed in the previous section for modeling of 2D structures can be applied to 3D structures as well. While the 2D approach successfully explains the qualitative behavior of a 3D structure, the design method must be adapted with special attention to 3D modeling for quantitative evaluation.

An example design of a SiON waveguide-coupled Si photodetector on SOI substrate is shown in Fig. 5-8. 3D BPM optical simulation of this structure shows that the evanescent wave coupling from SiON channel waveguide to the wider Si layer on buried oxide is efficient only under specific conditions. This is consistent with our observations on 2D slab structures, described in the previous section.

As the coupling to Si layer occurs, photons stay concentrated in the central region without diverging laterally to the wider Si layer (Fig.5-8(b)). This is a beneficial

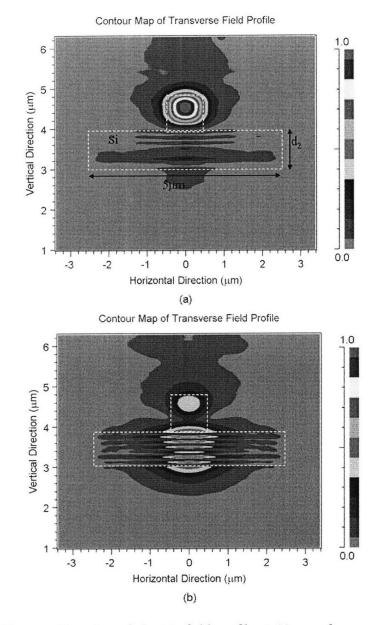


Figure 5-8: Cross-section view of electric field profile at 20 μ m after coupling begins. (a) When d₂=0.96 μ m, the mode remains in the waveguide (b) When d₂=0.895 μ m, the mode propagates in the detector. Waveguide has the refractive index of 1.57 with 0.9 μ m × 0.9 μ m dimension. The structure is all clad with SiO₂

phenomenon for the lateral p-i-n photodiode structure where the intrinsic region with highest electric filed is located beneath the waveguide. The ridge-like coupling structure generates a higher effective index in the central region, contributing to the lateral confinement. In fact, the coupling in this structure is the phenomenon where photons interacts mainly in the vertical direction (the mode keeps oscillating vertically between the top waveguide and the bottom Si layer as they propagate), and we have observed that varying the width of Si bottom layer has no significant effect on coupling behavior.

To find coupling conditions in 3-dimensional structure, we applied the same principles used in our analytical model in Section 5.2. We separate the whole coupling structure into two separate structures that are shown in Fig. 5-9 inset. One structure is a 3-dimensional SiON channel waveguide situated on a Si layer and the other structure is a 2-dimensional Si slab waveguide.

The effective index of the mode inside the SiON waveguide can be approximately calculated using the Effective Index Method (EIM). By considering light confinement in the lateral direction first, we obtain the effective index from solving the following equation.

$$\frac{2\phi}{\lambda_0}n_1 \cdot 2w_1 \sin\theta_1 = 4\tan^{-1}(\frac{\sqrt{\cos^2\theta_1 - (n_3/n_1)^2}}{\sin\theta_1(n_3/n_1)^2}), \ N_{1eff} = n_1\cos\theta_1$$
(5.12)

When we examine the TE mode in the 3D channel waveguide, the lateral confinement problem should be solved with TM mode equation, because the electric field is polarized perpendicular to the waveguide boundaries [57]. By reducing the 3D channel waveguide problem into a 2D slab waveguide problem, we can follow the same formalism (5.1)-(5.6) with only n_1 replaced by N_{1eff} obtained from (5.12) and find the propagation constant β_1 of the waveguide structure. For a Si photodetector structure, we can ignore the finiteness of lateral dimension and obtain β_2 by just following the same formalism (5.7)-(5.11).

By matching propagation constant β_1 and β_2 obtained by above procedures, we can determine the coupling conditions. In Fig. 5-9, this approach shows good agreement

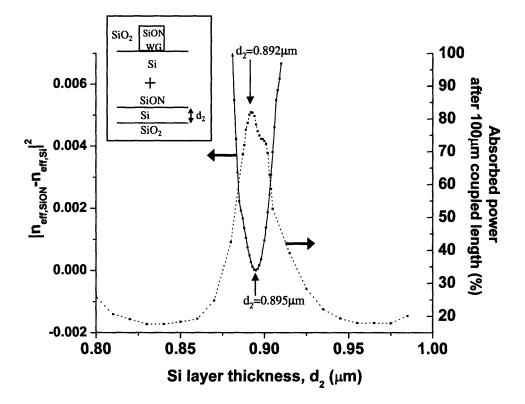


Figure 5-9: Comparison of phase mismatch indicator $|n_{eff,WG}-n_{eff,Si}|^2$ calculated from the Leaky-Mode model vs. 3D BPM simulation results, as Si thickness varies. Inset shows the modeled structure. The shoulder at $d_2=0.9 \ \mu m$ reflects the state of mixed mode propagation at the z=100 μm position.

with 3D BPM simulations in predicting Si layer thickness for the optimal coupling conditions. Still, there is a small discrepancy (2.5nm) in peak positions between our approach and BPM simulation. The main cause for the discrepancy is that EIM is not accurate in calculating the propagation constant β_1 of the waveguide structure. After applying the Finite-Difference-Method mode solver [58] to the waveguide structure in the Fig. 5-9 inset, we obtain a slightly lower effective index $n_{eff,SiON-WG}=1.487$. The modified β_1 will shift the $|n_{eff,SiON} - n_{eff,Si}|^2$ curve to the left and the peak positions will be only 1 nm apart, indicating a very good agreement between our phase-matching method and optical simulations.

5.5 Conclusion

Waveguide-coupled photodetector designs can remove the trade-off between speed and efficiency of conventional photodetectors. Especially, photodetectors with small absorption coefficients, such as Si at 850 nm, will benefit greatly from optimized waveguide-coupled photodetector designs. We presented a Leaky-Mode model that allows optimization of coupling by phase-matching of propagating modes in both the waveguide and photodetector.

Using SiON as waveguide material and thin Si photodetector on SOI substrate, we developed a simple and intuitive model that explains the evanescent coupling behavior between waveguide and detector. By treating the whole structure as a combination of two individual waveguides and analyzing each waveguide with a ray-optics approach, we showed that treating this coupling structure as waveguide-to-waveguide coupling is effective and phase matching between the waveguide and the Si layer is the key condition for efficient coupling. We demonstrated that our method provides a very simple but also a precise way to find optimal coupling conditions both for 2D and 3D coupling structures. The study showed that the Si layer thickness is the most critical factor that needs precise design and process control in this structure. We showed that the coupling behavior and further issues such as a coupling sensitivity and the design of waveguide index contrast can be easily understood by the formalism

and the plots from our approach. This method can be applied to broader range of evanescent wave coupling systems, when the absorbing material is much thinner than the absorption length $(\sim 1/\alpha)$ at the wavelength of interest and the refractive index difference between waveguide and photodetector material is large.

Chapter 6

Design and Simulation of High-Speed Germanium Integrated Photodetector

Germanium, as one of group IV semiconductor material that has a smaller band gap compared to silicon, has wider wavelength range of absorption. Ge has considerably high absorption coefficients at 1300nm ($\sim 6300 \text{ cm}^{-1}$) and 1500nm ($\sim 2000 \text{ cm}^{-1}$) [59]. The efficient absorption of Ge at near-IR communication wavelengths makes it a good photodetector material not only for optical clocking application but also for photonic integrated chips for telecommunication purposes.

In addition, Ge has higher electron and hole mobilities of $\mu_n \sim 3900 \, cm^2/(Vs)$ and $\mu_p \sim 1900 \, cm^2/(Vs)$, respectively. Therefore, due to electrons and holes moving faster than in silicon under the same circumstances (e.g., under the electric field not strong enough for carriers' velocity saturation), the transit time response of germanium photodetector can be faster than that of silicon photodetector.

When these good properties are combined with Si-compatibility, which means germanium can be introduced into current Si CMOS processing facilities without any complex issue, germanium becomes a nearly perfect photodetector material for Si microphotonics.

However, one technical challenge in using germanium in silicon processes is that

germanium growth on Si substrate is not an easy task, due to 4% lattice mismatch between Si and Ge. For pure Ge on Si, the critical thickness for relaxation through introduction of dislocations is only a few atomic layers thick [60].

Direct heteroepitaxy of Ge on Si have been attempted by several groups with several methods [61–70]. However, the problem with direct epitaxy of Ge or SiGe alloys is the high dislocation density. Due to the lattice mismatch, SiGe alloys with Ge concentrations greater than 30% generally have dislocation densities of 10^{11} - 10^{12} cm⁻² [71].

One possible approach to reducing the dislocation density is the use of buffer layers, as demonstrated by Fitzgerald et al [72–75]. However, Ge epitaxy without thick buffer layers is desirable for optical photodetector designs. Luan et al [76,77] has grown high quality epitaxial films by first growing a low temperature buffer layer and then raising the temperature to grow the remainder of the film. Post-growth cyclic annealing reduced the dislocation density to 10^7 cm⁻². This growth method has enabled the high quality germanium growth directly on Si and is the basis of Ge photodetector processing in this thesis.

From our group at MIT, demonstrations of Ge photodiodes using Luan's growth method followed [78–81]. Ge photodetectors made of a Ge layer directly grown on Si substrate showed the shrinkage of the band gap due to tensile strain caused by the difference of thermal expansion coefficient between Ge and Si, and therefore extends the responsivity towards longer wavelengths in L band telecommunications [82–85]. Liu et al. [86] have demonstrated 8.5GHz Ge p-i-n photodetector on Si platform with an detection spectrum of 650-1605 nm.

The growth of high-quality Ge film directly on Si substrate and the successful demonstration of Ge photodetectors in MIT have motivated several other groups to join in the field and demonstrate several different types of Ge photodetectors [87–93]. Dehlinger et al. from IBM demonstrated 29GHz bandwidth Ge lateral p-i-n photodetector on SOI substrate [94].

Ge photodetector researches demonstrated so far focused on the discrete photodetectors. To our knowledge, there are few reports in waveguide-integrated germanium and only some simulation results, not experimental results [95] are available as of the time of completion of this thesis. As a critical component of intrachip optical interconnect and electronic-photonic integrated circuits (EPIC), the development of waveguide-integrated Ge photodetectors has remained an imperative task.

The development of waveguide-integrated Ge photodetectors is the topic for the rest of the thesis. In this chapter, we discuss the possible structure designs for the waveguide-integrated Ge photodetector and will demonstrate optical simulation results. Since a top-waveguide-coupled structure was already discussed in chapter 4, we will mainly discuss other possible coupling structures. The experimental results from the fabricated waveguide-integrated Ge photodetectors will be presented in the following chapters.

6.1 Evanescent coupling design map

Before we investigate the designs for the waveguide-integrated Ge photodetector in the rest of the chapter, it will be beneficial to devise an evanescent coupling design map because it can help us understand how the photon coupling behavior can be influenced by the coupling structure design in a more organized way. The design map can provide us with a helpful guide in choosing materials for waveguide and photodetector and designing the device structures.

Such a design map would be more meaningful especially in silicon microphotonics, because the possible range of materials choice is very large in silicon microphotonics. For example, typical cladding material SiO₂ has the refractive index of 1.45 and Si and Ge has the refractive index of 3.5 and 4, respectively. There is huge flexibility in terms of waveguide core refractive index, because it is possible to use a low index SiO_xN_y material, which is close to 1.5, to the SiN material that has 2.0 refractive index, or all the way to Si waveguide hat has the refractive index of 3.5. Therefore, the coupling behavior from the waveguide to the photodetector in this material systems can be very much different, depending on which material is used.

It is in good contrast to the waveguide-integrated photodetector in III-V com-

pound semiconductor systems, in which all materials including waveguide core, cladding, and photodetector materials are typically grown in one epitaxial process by bandgap engineering. Therefore, the refractive index differences between waveguide core, cladding, and photodetector absorbing material are small in most cases.

In constructing a coupling design map, we used FDTD optical simulation method and extracted quantitative parameters that represents coupling phenomenon. Fig. 6-1 shows the simulation result of one example coupling structure, which consists of the $1.2\mu m \times 1.2\mu m$ SiON waveguide with 1.52 refractive index and the Si photodetector. We converted 3D coupling structure into 2D structure by applying the effective index method (EIM) [57] to the waveguide and conducted 2D FDTD simulations. In simulations, we placed the monitors that measures the optical power that remains in waveguide and upper cladding (as shown in Fig. 6-1(a)) every five micrometer after the coupling to the photodetector begins. Then we fitted the monitored optical power value to the exponential function $f = C * \exp(-\alpha_{coupling}x)$, as shown in Fig.6-1(b). C and α were extracted as the parameters that represent the coupling phenomenon. α indicates the evanescent coupling rate from the waveguide to the photodetector. C indicates the relative dominance of coupling process I or coupling process II (as defined in Section 4.1), through which photons couple from the input waveguide to the photodetector. The higher C is, the more dominant the coupling process II is relative to the coupling process I.

One of the control parameter that determines the coupling rate between the waveguide and photodetector is the refractive index difference between the waveguide and photodetector material. The higher $n_{PD} - n_{WG,core}$ is, the slower the evanescent coupling is, because the reflectivity at the interface between waveguide and photodetector increases. In the case of the discrete photodetectors used with the normally incident light, this index mismatch between the source material and destination material is the main factor.

In contrast, when the coupling from the waveguide to the photodetector is considered, it is very important that we realize the material index difference, $n_{PD} - n_{WG,core}$, is not a single main factor. Another important factor is the input waveguide de-

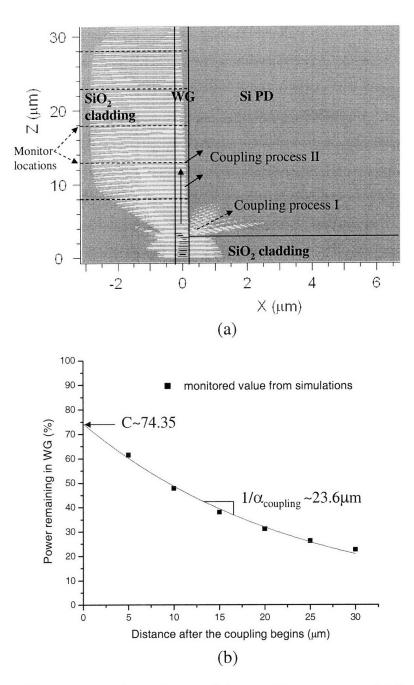


Figure 6-1: (a)FDTD optical simulation of the coupling structure of 1.2 μ m × 1.2 μ m SiON (n=1.52) waveguide and the Si photodetector. Dotted arrow and solid arrow represent the coupling process I and II, respectively. Optical power monitors are placed where marked with dotted lines (b)The remaining optical power in the waveguide structure vs. the coupling length.

sign. In addition to the fact that the different waveguide design affects the value of $n_{PD} - n_{WG,core}$, more importantly, the different waveguide geometry even with the same waveguide core material can change the coupling behavior greatly. Therefore, we need to define a waveguide geometrical factor.

One traditional way of understanding the propagation mode in the waveguide is to view the mode as the light rays undergoing multiple total internal reflections at the core/cladding interfaces with the angle θ against propagation axis. Following this viewpoint, we may think two other main factors that affect waveguide-tophotodetector coupling rate other than $n_{PD} - n_{WG,core}$, are the reflection angle θ and the frequency at which the light ray hits the interface with photodetector, 1/l (as shown in Fig.6-2(a)). As the 1/l and θ are higher, light rays will make more frequent attempt to enter the photodetector material with higher transmission efficiency.

Therefore, we define the waveguide geometrical factor as follows.

$$WG \ geometrical \ factor = (\sin \theta) \times (\frac{1}{l}) = (\frac{\sqrt{n_{core}^2 - n_{eff}^2}}{n_{core}})(\frac{\sqrt{n_{core}^2 - n_{eff}^2}}{2hn_{eff}}) = \frac{(n_{core} - n_{eff})}{2h}(\frac{1}{n_{core}} + \frac{1}{n_{eff}})$$
(6.1)

The effect of the geometrical design of a waveguide is reflected in the WG geometrical factor through n_{eff} and h. Generally, the The effect of the geometrical design of a waveguide is reflected in the WG geometrical factor through n_{eff} and h. Generally, the waveguide geometrical factor increases as the refractive index contrast between the waveguide core and cladding increases and as the waveguide dimension becomes more compact, especially as the thickness gets smaller.

Fig. 6-2(b) demonstrates optical simulation results for the evanescent coupling structures that consist of Si photodetector (n=3.66+i0.0039) and the waveguides with various refractive index and geometries at 850nm.

Single-mode waveguide design will have the correlation between $n_{PD} - n_{WG,core}$ and the waveguide geometrical factor. As the higher index-contrast waveguide is used, the index difference between the photodetector and waveguide core decreases.

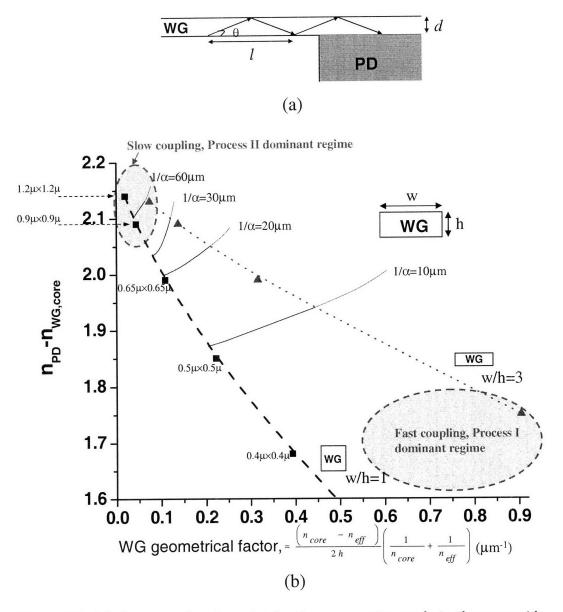


Figure 6-2: (a) the ray-optics viewpoint for the propagation mode in the waveguide (b)The change of evanescent coupling behavior ,according as the waveguide design varies. $\lambda = 850$ nm and the coupling to the Si photodetector (n_{PD}=3.66+i0.0039) is assumed. The contours for the same evanescent coupling rate are shown.

In addition, the WG geometrical factor increases as the difference among n_{core} , n_{eff} and $n_{cladding}$ gets bigger and the waveguide size becomes smaller.

For example, the single mode cut-off condition for square-type dielectric waveguides is approximated as

$$w_0 = h_0 = \frac{\sqrt{2\pi}}{n_{core}k_0 \sin(\cos^{-1}(n_{cladding}/n_{core}))}$$
(6.2)

The square-type single-mode waveguide designs based on Equation (6.2) follows the dashed line in Fig. 6-2(b). Likewise, the waveguide designs that are close to the single-mode cut-off condition and maintain a width-to-height ratio of 3:1 follows the dotted line in the design map of Fig. 6-2(b). The waveguide designs with the higher w/h ratios tend to have the smaller height h and the more optical power of the fundamental mode spread out to the outside cladding therefore have the higher waveguide geometrical factor, compared to the waveguides with w/h = 1 ratio.

With several exemplary waveguide designs of the square-type (w/h = 1) and the rectangular type (w/h = 3), as indicated by the dots on the guide lines of Fig. 6-2(b), we ran the FDTD simulations and extracted the value of $1/\alpha_{coupling}$ by the method explained in Fig. 6-1. By interpolating from those values at points, we constructed contour lines on which the evanescent coupling rate from the waveguide to the photodetector are equal.

The contour lines of $1/\alpha_{coupling} = 10, 20, 30, 60 \,\mu\text{m}$ shown in Fig. 6-2(b) indicate that the evanescent coupling from waveguide to photodetector occur more quickly as the index contrast between the waveguide and photodetector material, $n_{PD} - n_{WG}$ is smaller and the waveguide geometrical factor is larger.

With given materials, we can further enhance the coupling rate by increasing the waveguide geometrical factor, i.e., by shrinking the waveguide dimension or making the shape of flat rectangles. The enhancement will be more significant especially when the refractive index of waveguide core material is low, as seen from the slopes of contour lines in a low coupling rate regime.

We also have found that the parameter C, as defined in Fig. 6-1(b), is greater

when $1/\alpha_{coupling}$ is increased (the coupling is slower). That is, coupling process II is more dominant when the evanescent coupling is slower and coupling process I is more dominant when the evanescent coupling is faster. Therefore, we can define two different regimes in the coupling design map, i.e., 1) the regime where the coupling process II is dominant and the evanescent coupling from the waveguide to the waveguide is slow due to high $n_{PD} - n_{WG,core}$ and low waveguide geometrical factor and 2) the regime where the coupling process I is dominant and the evanescent coupling from waveguide to photodetector is fast due to the low $n_{PD} - n_{WG,core}$ and high waveguide geometrical factor. These regimes are indicated in the coupling design map.

The experimental observations of the evanescent coupling behavior that we obtained from various waveguide materials and designs in Chapter 4 agree well with the deign map we constructed here both qualitatively and quantitatively. Our design map enables us to predict the evanescent coupling behavior of the waveguide-integrated photodetectors without experimental demonstration or heavy numerical simulation for every design case. For example, we can easily expect that the photodetector evanescently-coupled with a rib waveguide should have slower coupling rate than the one coupled with a channel waveguide made of the same material, because, in a rib waveguide structure, the more portion of the waveguide mode is contained in the waveguide core and the effective index is closer to the core refractive index, therefore leading to the smaller waveguide geometrical factor and the slower evanescent coupling rate as a result.

The same principles of the coupling design map apply to the case for 1550 nm wavelength as well. Therefore, we can also expect the Ge photodetector evanescentlycoupled to Si waveguide at 1550 nm should have extremely fast evanescent coupling from the waveguide to the photodetector, because of very low $n_{PD} - n_{WG,core}$ of 0.5 and the very high waveguide geometrical factor arising from the high refractive index of silicon waveguide core and the small single-mode waveguide dimensions of 500 nm (W) × 200 nm (H). The fast coupling from Si waveguide to Ge photodetector will be demonstrated with simulation in many sections of this chapter and with experimental work in the following chapters.

6.2 Ge photodetector on Si substrate vs. SOI substrate

Whether using Si substrate or SOI substrate for coupling structures of Si waveguide and Ge photodetector makes a significant difference in photon coupling behavior. Thus we need to consider this issue before designing the coupling devices.

The rule of thumb in the light coupling in any multilayered structure is that the tangential component of the electric field must be continuous at the boundary. This principle dictates the behavior of light when it transfers from one material to the other, and Snell's law is simply derived from this principle.

When this basic principle is applied to an evanescent coupling structure as shown in Fig. 6-3, it means that the lateral component of light, i.e. the propagation constant of the mode will be maintained as photons from the top waveguide couple to Ge photodetector to the substrate on the bottom. When unabsorbed photons reach the substrate (most Ge photodetector designs would have Ge layer thickness not enough to absorb all photons), the different phenomena will occur depending on whether Si or SOI substrate is used.

In the case of SOI substrate (Fig. 6-3(a)), in which the bottom material is silicon oxide, the propagation constant of the coupled mode, $k_x = k_0 \times n_{eff}$ is even larger than the propagation vector in the oxide, $|\vec{k_{oxide}}| = k_0 \times$ (the refractive index of SiO₂). It is because the effective index of the propagation mode in the waveguide was originally between the refractive index of silicon oxide and silicon, i.e. $n_{SiO_2} < n_{eff} < n_{Si}$. This constraint means that when the light reaches the bottom oxide, it cannot continue the travel to the oxide and has to be totally reflected back to the top Ge.

In contrast, in the case of Ge photodetector grown on Si bulk substrate (6-3(b)), the light propagation mode originally from the top waveguide may propagate to the bottom Si bulk substrate, because $k_x = k_0 \times n_{eff} < |\vec{k_{Si}}| = k_0 \times n_{Si}$ in this case. It is even possible to estimate the radiating angle as $\theta = \cos^{-1}(n_{eff}/n_{Si})$. That is, higher refractive index of Ge compared to that of Si does not provide enough confinement to prevent photons from transmitting to Si substrate. The photons that radiate to

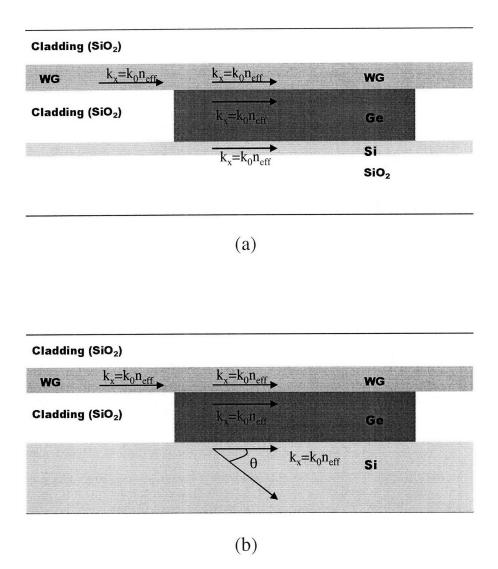


Figure 6-3: Schematics that show the propagation constants of light propagation in the coupling structures of Si waveguide and Ge photodetector (a) on Si substrate vs. (b) on SOI substrate.

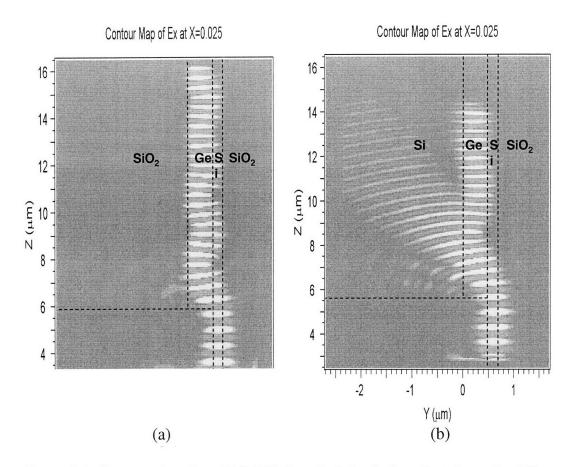


Figure 6-4: Cross-section view of 3D FDTD optical simulations that shows the different propagation of photons in the coupling structures of 0.2 μ m thick Si waveguide and 0.5 μ m Ge photodetector on (a) SOI substrate vs. (b) Si substrate. Absorbing function of Ge was repressed in this simulation by setting the imaginary refractive index of Ge to be zero, in order to show the light propagation more clearly.

bottom Si substrate will be lost without being absorbed and contributing to the photocurrent.

We conducted 3D FDTD optical simulations for the evanescent wave coupling structures with $0.5\mu m \times 0.2\mu m$ Si waveguide and $0.5\mu m$ Ge photodetector layer (as in Fig. 6-3) and its results are shown in Fig. 6-4. As expected, the coupling structure on Si bulk substrate, though Si/Ge interface partially reflects photons back to Ge and lets them be coupled to Ge layer, lose a significant portion of photons by letting them radiate to Si (Fig. 6-4(b)). Attempts to modify the device design such as varying the waveguide materials/dimensions or using the tapered waveguide would not prevent

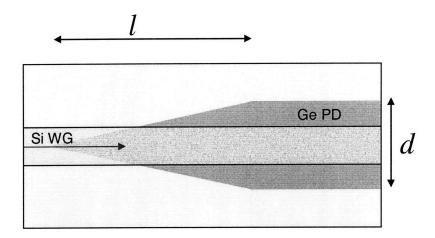


Figure 6-5: Top schematic view of the coupling structure that employ tapered Ge structure.

the radiation of photons to Si substrate completely, because the effective index of the waveguide mode, regardless of the waveguide design, should be less than the refractive index of silicon. In contrast, oxide bottom layer from SOI substrate can effectively confine all the photons to Ge layer.

The complete confinement of photons within Ge layer by SOI substrate enables the high-speed and high-efficiency photodetector. SOI substrate also provides the high-quality top crystalline Si layer that can be used as Si waveguide core, together with the buried oxide that can be used naturally as an undercladding layer of the waveguide. A Ge photodetector grown on Si waveguide, which is formed from SOI's top Si layer, can be a structure that best utilizes good traits of SOI substrate. This structure will be discussed in Section 6.4.

6.3 Enhanced Mode Coupling to a Tapered Ge Photodetector

Coupling to Ge photodetector fabricated on Si substrate will inevitably have the leakage of unabsorbed photons to the substrate, as shown in Fig.6-4(b). However, it is possible to decrease the relative amount of leakage into the substrate at Si/Ge interface and enhance the reflection into Ge layer by designing a novel structure. The

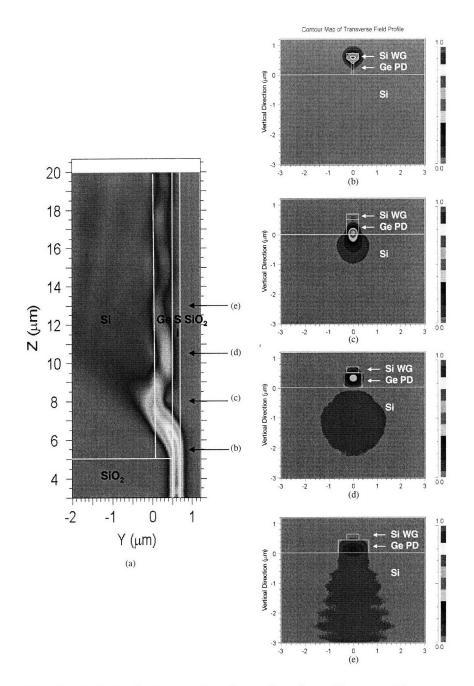


Figure 6-6: Optical simulation results of coupling from Si waveguide to tapered Ge photodetector on Si substrate. (a)Y-Z cross section view. X-Y cross section view of mode profile (b)at $z = 5.5 \ \mu m (0.5 \ \mu m$ after coupling) (c)at $z = 8 \ \mu m (3 \ \mu m$ after coupling) (d)at $z = 10.5 \ \mu m (5.5 \ \mu m$ after coupling) (e) at $z = 13 \ \mu m (8 \ \mu m$ after coupling). Ge's absorbing function is turned off in this function in order to show photon propagation more clearly. The coupling behavior, when Ge has absorption coefficient of 4000 cm^{-1} , should be the same as this except that optical intensity decreases whenever the mode goes through Ge.

coupling structure with a tapered Ge photodetector, whose top-view structure is as shown in Fig. 6-5 and cross-section view is as shown in Fig. 6-3(b), can have more optical power be coupled to Ge layer instead of being lost to the substrate. Fig. 6-6 is the optical simulation results of the coupling structure with a taper length $l = 10 \mu m$ and Ge detector width $d=1.5\mu m$. Y-Z cross section view (Fig. 6-6(a)) shows that the photons that reach Ge/Si interface partially leak towards the substrate and partially get coupled to Ge layer. X-Y cross section views (Fig. 6-6(b)-(e)) more clearly shows the photon coupling process progressively. As photon coupling to the tip of Ge photodetector starts at $z=5\mu m$, the mode in the Si waveguide begins to see the existence of Ge layer only in the small central part (Fig. 6-6(b)). The mode gets distorted, especially where it sees Ge in the central area, and moves slowly downward to Ge layer. About $3\mu m$ after coupling, the mode now reaches the interface between Ge and Si substrate (Fig.6-6(c)) and there will be partial reflection back to Ge and partial leakage to Si substrate. At $5.5\mu m$ after coupling, it is shown that the mode that remains and propagates in the Ge layer and the radiated optical power towards Si substrate are completely separated in Fig. 6-6(d). The optical power that transmitted to Si at the Ge/substrate interface continues moving downwards to the substrate. The optical power that was reflected and confined to Ge continues to propagate by bouncing vertically alternately within Si waveguide and Ge layer, which means the optical power in the layer is not completely stabilized into the mode yet. When these photons hit again the interface between Ge layer and Si substrate, partial leakage to the substrate occurs again, as shown in Fig. 6-6(e). The power that can be absorbed to Ge layer instead of being lost to the substrate seems to be about 60%.

The simulation results in Fig.6-6 are based on the design that has the ideal tapered structure of Ge photodetector. In reality, the tip can be dull due to lithography limit and etching process. Fig. 6-7 is the simulation result of the same structure as in Fig. 6-6, but with $0.4\mu m$ width at the taper tip. Therefore, the coupling starts at $z=7.66\mu m$ as the Si waveguide sees $0.4\mu m(W) \times 0.5\mu m(H)$ Ge photodetector structure. Fig.6-7(b) shows that, as soon as the coupling begins, the mode quickly expands as most optical power begin to move downwards. This coupling process to

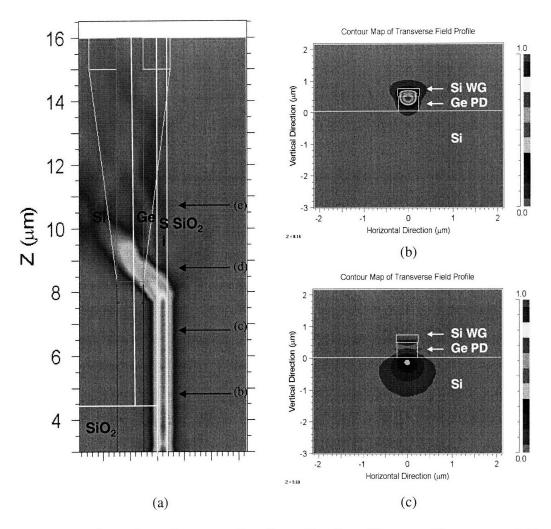


Figure 6-7: Optical simulation results of coupling from Si waveguide to tapered Ge photodetector with 0.4 μ m-wide tip on Si substrate. (a) Y-Z cross section view. X-Y cross section views of mode profile (b) at z = 8.16 μ m (0.5 μ m after coupling) and (c) at z = 9.60 μ m(2 μ m after coupling.

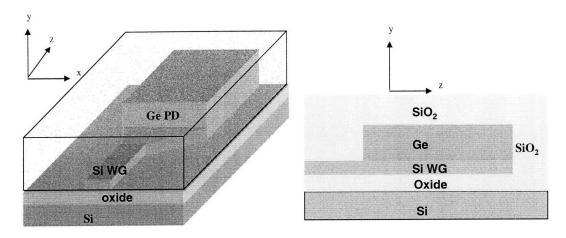


Figure 6-8: (a) 3D schematic of a Ge photodetector coupled to the bottom Si waveguide on SOI substrate (b) Y-Z cross section view of the structure.

Ge is sudden and quick. When photons reach the interface with Si substrate, most photons transmit through the interface and radiate into the substrate (Fig. 6-7(c),(a)).

This shows photon coupling to the untapered (or tapered with wide tip)Ge photodetector will have most power be lost to the substrate without confining and absorbing good amount of optical power. Coupling to the Ge photodetector taper with, e.g., $0.18\mu m$ will have the coupling efficiency to Ge layer between that of Fig.6-6 structure and that of Fig. 6-7.

In this section, we demonstrated that the use of tapered Ge photodetector structure with a sharp tip can slow down the coupling process from Si waveguide to Ge photodetector and enhance the photon coupling efficiency to Ge photodetector, which otherwise may be very low due to leakage to the Si substrate.

6.4 Bottom-Waveguide Coupled Ge Photodetector on SOI Substrate

One nice way of integrating Ge photodetector with Si waveguide is to grow Ge material directly on the top Si layer of SOI substrate and use the Si layer as a waveguide. The coupling structure from a Si waveguide at the bottom to a Ge photodetector on the top is formed (Fig. 6-8). The single-mode Si waveguide has the dimension

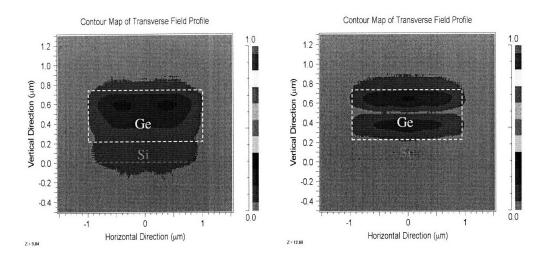


Figure 6-9: X-Y cross section view of mode profile at (a) $z=9.84\mu m$ (4.84 μm after coupling) (b) at $z=12\mu m$ (7 μm after coupling).

of $0.5\mu m(W) \times 0.2\mu m(H)$. In order to widen the Si waveguide to the greater width of Ge photodetector required for forming contacts, the adiabatic taper structure was inserted between the waveguide region and detector-coupling region. It is known that, as a mode expands laterally along the taper, most optical power remains in a fundamental mode inside the waveguide. Since photon coupling rate from Si to Ge is very high, the mode from the waveguide begins to rise and transfer to germanium as soon as the Si waveguide sees germanium in the coupling region. The mode oscillates vertically between Ge and Si as it propagates and the absorption process occurs whenever photons go through Ge structure (Fig. 6-9). The shape of a laterally stretched fundamental mode is maintained all the time throughout coupling and absorption process. When a Ge layer has $0.5\mu m$ thickness and $2\mu m$ width and is assumed to have $4000cm^{-1}$ absorption coefficient, about $12\mu m$ -long coupling structure can absorb about 95% optical power.

Since SOI wafer provides a high-quality Si crystalline layer with a very smooth surface and interface with buried oxide, this structure enables us to obtain a Si waveguide with a very low propagation loss. Coupling from waveguide to photodetector occurs through the direct epitaxial interface between Si and Ge. Therefore, the coupling process may be less susceptible to possible processing variation issues, compared to

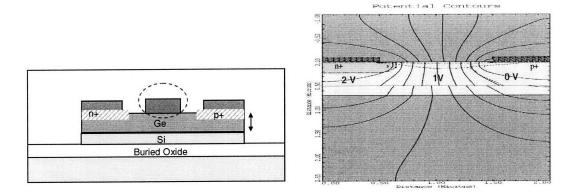


Figure 6-10: (a) The lateral p-i-n Ge photodetector structure grown on SOI substrate. The bump in a dotted circle indicates the mode-concentrating feature (b) Equi-potential contour lines (0.25V spacing) are shown in a lateral p-i-n structure, when 2V reverse bias voltage is applied. Electric field points in perpendicular to the lines.

top-waveguide coupled structure, in which the coupling region in the structure may require a very rigorous processing control to ensure the within-wafer uniformity of photodetector performance.

6.5 The Mode-Concentrating Feature for Photodetector Performance Enhancement

With Ge layer grown on the Si waveguide of SOI substrate, it is possible to form a vertical p-i-n photodetector or a lateral p-i-n photodetector.

For a vertical p-i-n photodetector, it is needed to form one electrode $(p^+ \text{ or } n^+)$ on the Si layer and the other electrode $(n^+ \text{ or } p^+)$ on the top part of Ge layer. Metal contacts to electrodes with unequal heights are required because the contact to the bottom electrode needs to be longer than the contact to the top electrode by the photodetector thickness. The vertical p-i-n photodiodes is similar to parallel capacitor and thus the electric field inside is uniform and unidirectional throughout the photodiode.

For a lateral p-i-n photodetector as shown in Fig. 6-10(a), the p⁺ and n⁺ electrodes are formed in parallel on the top surface of the Ge photodiode. The metal contacts

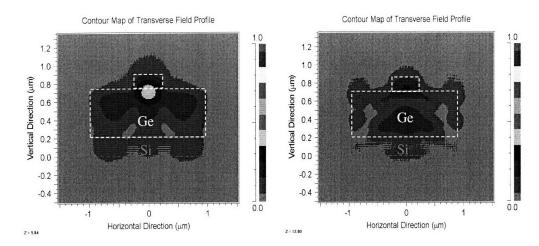


Figure 6-11: The cross-section view of mode profile in a Ge photodetector on SOI, when a bump is formed at the center. 0.5 μ m (W)× 0.2 μ m (H) Si bump is placed on top of 2 μ m (W)× 0.5 μ m(H) Ge photodetector on 0.2 μ m thick Si layer. (a) at z = 9.84 μ m (4.84 μ m after coupling) (b)at z=12 μ m(7 μ m after coupling)

can be formed in one process to both electrodes and the process integration may be an easier issue, because the geometry is more similar to MOSFET device.

However, a lateral p-i-n photodiode does not have the uniform electric field strength inside the absorbing layer, unlike a vertical p-i-n photodiode. As Fig.6-10(b) shows that the electric field lines are concentrated and strongest in the center area between p^+ and n^+ electrodes. At side area of the photodetector which is beneath the p^+ and n^+ electrodes, the electric fields are weak and do not point directly towards the electrodes. Problem is that photon coupling to the Ge photodetector grown on SOI substrate is uniform throughout the photodetector cross section, as shown in Fig. 6-9 and there should be many electrons and holes generated beneath the electrodes at sides. They will experience a much weaker electric field than those generated in the central region, and will take long time to be swept out of the photodiodes. This phenomenon will significantly slow down the response of the photodetector.

It is possible to mitigate this problem and enhance the photodetector speed by designing a ridge-like bump structure in the center of the photodetector. We can fabricate a structure as shown in the dotted circle of fig. 6-10(a), if we grow, e.g., Si layer immediately following Ge epitaxy and etch it away leaving the material only in the

middle. Fig. 6-11 shows the photon coupling behavior when $0.5\mu m(W) \times 0.2\mu m(H)$ Si bump is formed on top of Ge photodetectors. In ultimate comparison to coupling in Fig. 6-9, the optical power is shown to be much concentrated to the center region during the propagation throughout the coupling structure. High refractive-index material located only at the center forms a ridge-waveguide-like structure, generates a higher effective index in the middle compared to the sides, and lets the mode concentrate. Since more optical power propagates in the central region, most carries will be generated in the region where the electric field is strongest, enhancing the photodetector speed. This mode-concentrating feature had better be made of a non-absorbing because then it can only help the mode concentrate in the central part of germanium without absorbing photons in itself, which does not provide a good carrier drift path to the electrodes with strong electric field.

6.6 The Effect of Electrode Contact Materials on the Coupling

In the case of a top-waveguide-coupled photodetector design such as Fig.4-10 and Fig.5-8, the coupling process occurs in a way that the waveguide constantly emits photons to the part of the photodetector right beneath it. Therefore, most photons would not see the effect of electrode contacts that are placed at the sides of the waveguide, unless contacts are too close to the waveguide. That is, the coupling behavior in the structures like that of Fig. 4-10 and Fig. 5-8 would not be affected much by the existence of contacts.

In contrast, in the case of bottom-waveguide-coupled photodetectors considered in Section 6.4 and 6.5, the photodetector is located on the waveguide that is as wide as photodetector. The electrodes placed on the top surface of the photodetector will be seen by photons and thus will affect the optical coupling behavior. Therefore, in general, the optical simulation of the coupling for such structures must include the contact structures to the photodetectors, in order for the results to be realistic.

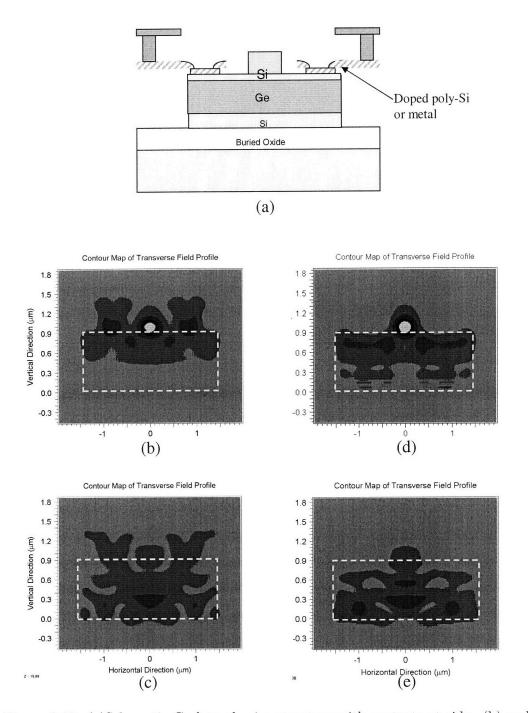


Figure 6-12: (a)Schematic Ge lateral p-i-n structure with contacts at side. (b) and (c): The cross-section view of mode profile (2.2 μ m and 4 μ m after coupling starts, respectively) in a photodetector structure of (a) with poly-Si used as a contact material. (d) and (e): The cross-section view of mode profile (2.2 μ m and 4 μ m after coupling starts, respectively) in a photodetector structure of (a) with metal used as a contact material.

We compared the effects of different electrode contact materials on the photon propagation in the coupling structure. In the structure of Fig. 6-12(a), it is possible to choose doped poly-Si or metal as a contact material to the Ge photodetector. Though it may be thought that a metal can function as a very quick absorber of photons and thus be detrimental to the coupling efficiency, the simulation results demonstrate it is not the case.

When poly-Si is used as a contact material instead of metal, these contacts attract photons to themselves the same way as the mode-concentrating bump does as explained in Section 6.5 (Fig. 6-12(b)&(c)). There will be free carrier absorption in this heavily-doped silicon material and also some photons can exit out of the coupling structure, following along the poly-Si material (Fig. 6-12(c)).

For the photodetector with aluminum metal contacts, we input 2.25+i12.5, the refractive index of aluminium at 1550nm, in a contact structure in the simulation. Despite very high imaginary part of refractive index, which may lead us to expect high absorption, it was shown aluminum contacts actually push photons away from themselves (Fig. 6-12(d)&(e)). Thus photons were contained nicely inside the photodetector structure and there were no photons being lost due to the contacts extracting photons.

It seems that, from simulation, the metal contacts are very reflective to photons in the coupling structure and therefore they neither absorb photons quickly or disturb the coupling behavior, despite its high imaginary refractive index. Experimental comparison will be necessary to investigate whether a real device work in the same way as the simulation (,where the metal/photodetector interfaces are perfectly smooth) and whether they are better than the poly-Si contacts, which will attract and scatters photons out of the coupling structures.

Chapter 7

Germanium Photodetectors Integrated with Top Deposited Waveguides

After design studies for possible coupling structures were conducted in the previous chapter, we progressed to experimentally demonstrate the waveguide-integrated Ge photodetector. Two major waveguide-photodetector integration schemes are the topwaveguide-coupled structure, where the waveguide with deposited material are placed on top of the photodetector, and the bottom-waveguide-coupled structure, where the photodetector is grown and fabricated on top of the waveguide at the bottom. In this chapter, we present Ge integrated photodetectors coupled with the deposited waveguides on the top, such as silicon oxynitride (SiO_xN_y or SiON for short), silicon nitride (Si_xN_y or SiN for short), and silicon waveguides. The bottom-waveguidecoupled Ge photodetector will be presented in Chapter 8.

7.1 Device Fabrication

In developing waveguide-integrated germanium photodetectors, we utilized knowledge earned from the evanescent coupling study between SiON waveguide and Si photodetector (Chapter 4). Therefore, the device structures and fabrication procedures employed in this chapter are similar to those in Chapter 4, mainly except that Ge epitaxial film is used for 1550nm detection instead of Si detector for 850nm operation.

The starting substrate was highly-doped (0.01-0.03 $\Omega \cdot cm$) p-type Si (100) wafer. Ge film was grown epitaxially on Si substrate in ultrahigh vacuum chemical vapor deposition (UHV-CVD) reactor ($\sim 5 \times 10^{-9}$ mbar). We preheated the Si substrate to 780°C with 6sccm H₂ flow (pressure= 10^{-3} mbar) for 20 minutes, in order to remove any residual native oxide and passivate the Si surface. After cooling down to 360°C while maintaining H₂ flow, Ge film was deposited on Si wafer in two growth steps, i.e., first growing 60nm Ge buffer layer at 360°C and then growing 1.1 μm Ge at higher temperature at 730 C. Cyclic thermal annealing treatment between 650°C and 850°C followed in order to reduce threading dislocation density. The dislocation density was estimated to be $\sim 2 \times 10^7$ /cm² by etch pit density (EPD) method.

A 200nm Si layer was deposited by LPCVD at 560°C. Then the wafers were implanted with 5×10^{15} /cm² dose of phosphorous at 85KeV energy, followed by an activation annealing in the rapid thermal processing (RTP) system at 750°C for 5 minutes. Germanium vertical p-i-n diodes were patterned through 1.9 μ m deep Si/Ge/Si layer plasma dry etching. Etching condition of 40 sccm Cl₂ flow and 40 sccm HBr flow at 400 W power and 100 mTorr pressure was used. 1.9 μ m deep etching was for securing enough separation of waveguide from the Si substrate in order to prevent optical loss due to the photon coupling to the substrate. Then 3.0 μm SiO₂ was deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD), followed by planarizing the top surface by Chemical-Mechanical Polishing (CMP). The thickness of the remaining oxide layer on top of the silicon photodetector was evaluated by ellipsometry measurement on larger monitor features positioned close to photodetectors. The oxide layer was further reduced to the desired thickness by a timed CHF_3 plasma etch on the flat silicon oxide film. This was followed by patterning and opening an oxide window to expose the top silicon surface of the photodetector such that the waveguide can be in direct contact with the photodetector for higher evanescent-wave coupling rate.

Then silicon oxynitride and silicon nitride layer as waveguide core materials were

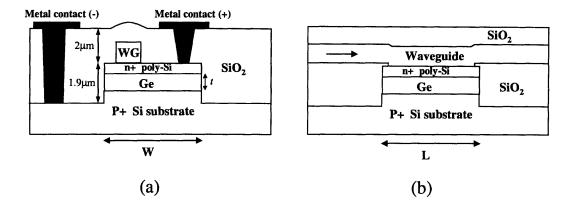


Figure 7-1: Schematic structure of a waveguide-integrated Ge photodetector (a) crosssection perpendicular to the waveguide direction (b) cross-section along the waveguide direction.

deposited by PECVD and etched using plasma etching with C_2F_6 and CH_3F gas. The SiON waveguide had the core refractive index of 1.8 and 0.9 $\mu m \times 0.9 \mu m$ dimensions and the silicon nitride waveguide had the core refractive index of 2.2 and 0.9 $\mu m(W)$ $\times 0.4 \mu m(H)$ dimensions. A 2 μ m-thick upper cladding SiO₂ layer was deposited, followed by opening contact holes. 50 nm titanium and 1.5 μ m aluminum with 2% silicon were next deposited by sputtering deposition. After the metal contact pads were patterned and etched, the wafers were annealed at 400°C for 30min in N₂/H₂ forming gas. The structure of the completed device is schematically shown in Fig. 7-1.

7.2 Photodetector Measurement Results

The I-V measurement results of the Ge diodes are shown in Fig. 7-2. The devices have very good rectifying characteristics, showing orders of magnitude difference of current between forward and reverse biases (Since voltage is applied to the n-side top electrode, positive voltage means the reverse bias to the photodetectors). The low leakage current is very important because the noise level and the power consumption in the photodetector operation are determined by the leakage current level. The leakage current of the photodetector is related to the quality of the photodetector materials and is considered as one of main challenges in the fabrication of photodiodes

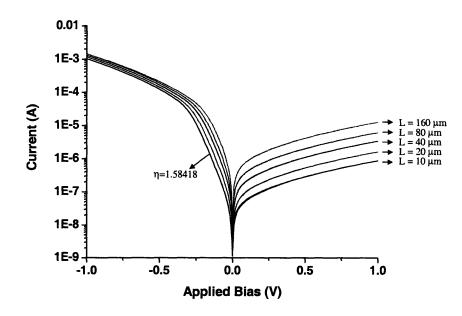


Figure 7-2: The dark I-V measurement results of Ge diodes. The width of the diodes is 7 μm and the length vary from 10 μm to 160 μm , as shown with different curves.

made of non-perfect materials, such as Ge directly grown on Si.

Our smallest diode ($7 \ \mu m(W) \times 10 \ \mu m(L)$) shows $0.8A/cm^2$ leakage current density at 1V reverse bias. This is still higher than what we previously reported with photodiodes made with Ge blanket film [85,86]. It is thought that the high density of imperfections along the perimeter of the diodes, which underwent the plasma dry etch, contributed to increased leakage current compared to the photodetector formed with Ge blanket film and the better passivation in germanium/oxide interface along the perimetric sidewall of photodetectors should reduce the leakage current.

Still, many of our diodes have leakage currents below 1 μ A. 1 μ A is generally considered by circuit designer as the maximum allowed leakage current level for highspeed receiver design including transimpedance amplifier (TIA) [96]. As will be discussed in more detail later in this chapter, the good coupling efficiency of our devices, which enables the use of small size photodetectors and the capability of low-voltage operation, at which leakage current is very low, indicate our photodetectors already well satisfy the requirement of high-speed photoreceiver designs.

From the forward bias current of photodetectors, we can determine the ideality

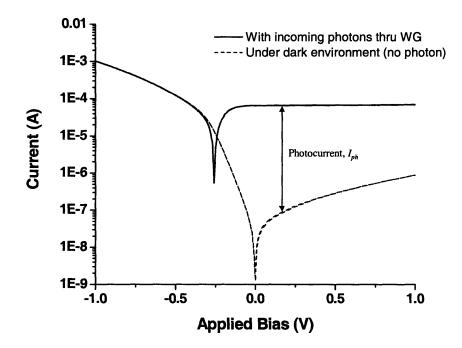


Figure 7-3: I-V characteristics of the photodetector when it is under dark environment without optical signal and when optical signal is detected.

factor η by

$$I_{forward} = e^{qV/\eta kT}.$$
(7.1)

As shown in Fig.7-2, our photodetector showed $\eta \sim 1.58$. The η being equal to 1 indicates the forward current is dominated by diffusion current, while $\eta \sim 2$ means the forward current is dominated by Shockley-Hall-Read (SHR) recombination due to defects in the mid-gap level. Our devices show the ideality factor commensurate with other Ge photodetectors reported [94,96], but have room to be improved.

The change of I-V characteristics of the photodetector, as an optical signal is coupled to the photodetector through the waveguide, is shown in Fig. 7-3. The increase of current in the revers bias region due to detected optical signal, which is the photocurrent, is apparent. The photocurrent, I_{ph} , is obtained by subtracting the dark current from the measured signal while illuminated. The photocurrent is flat over a wide range of reverse bias and nearly full DC responsivity can be achieved at zero voltage. The zero-bias responsivity shows that a strong electric field is already established within the Ge layer without applying a bias, indicating good Ge materials

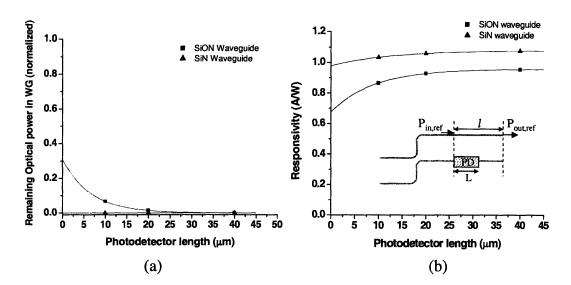


Figure 7-4: (a) Throughput optical power through the waveguides coupled with photodetectors with different lengths (b) The responsivity of waveguide-coupled Ge photodetector vs. detector length. An inset in (b) is the schematic layout of waveguides and photodetector devices on the chip.

quality. Our photodetector can be operated with a very high signal-to-noise ratio (SNR) at low voltage such as 0.1V, because of flat photocurrent response and low leakage current at low reverse bias.

The responsivity of waveguide-integrated germanium photodetectors was measured as follows. Light is coupled through an optical fiber to the waveguide and the photocurrent, I_{ph} , is measured. The optical power at photodetector, P_{in} , is determined from the measured transmitted optical power of reference waveguides, $P_{out,ref}$, and the measured transmission loss in the waveguide. Therefore, the responsivity R is given by

$$R = \frac{I_{ph}}{P_{in}} = \frac{I_{ph}}{P_{out,ref} \times 10^{\gamma l/10}}.$$
 (7.2)

where, γ is the waveguide transmission loss in the unit of dB/cm and *l* is the distance in cm from the photodetector edge to the waveguides output facets (as shown in the inset of Fig. 7-4(b)). The waveguide transmission loss γ is measured by using cut-back method with nearby paper clip structures on the same chip. The measured transmission loss of SiON waveguides was 6.91 ± 0.72 dB/cm and that of SiN waveguide (n =2.2, 0.9 μ m(W) × 0.4 μ m(H)) was 2.24 ± 0.42 dB/cm, both measured at 1550nm.

Fig. 7-4(b) shows the dependence of responsivity on the detector length for coupling light at 1550 nm from both the SiON and SiN waveguides. As we previously investigated in Chapter 4 with Si photodetector and low/high index contrast SiON waveguides, the use of the higher index waveguide leads to a higher coupling efficiency and faster coupling. Being consistent with the trend, the responsivity for the SiN coupled detector leveled off at 1.08A/W compared to 0.96 A/W for the SiON waveguide. The responsivity of the waveguide coupled detectors is significantly higher than for discrete vertical p-i-n Ge photodetectors where the responsivity for a 1.1 m thick Ge detector under normally-incident illumination at 1550nm is 0.45 A/W. Coupling from a waveguide to the Ge photodetector can reach efficiencies of 90 % or higher without being limited by the intrinsic layer thickness of the device. The results indicate that most photons from the waveguide couple to the Ge intrinsic layer mainly around the input port of the photodetector and travel mostly in the longitudinal direction until being fully absorbed. Photon coupling from a waveguide to the Ge photodetector in a lateral direction enhances the efficiency above the level possible with normal incidence. It is shown that efficient coupling can be achieved with short coupling lengths, allowing the use of small devices that are advantageous for higher speeds and low leakage currents.

The wavelength dependency of the responsivity, shown in Fig. 7-5, does not show the roll-off at 1540 nm that is typical for normal incident illumination [86]. The responsivity is flat through the full range of our tunable laser to 1570 nm for a 10 μ m long device. As a result of coupling from the waveguide, we expect that the efficiency of the Ge detectors can be high even at longer wavelength where photon absorption is much less efficient. For example, if we assume all photons couple to the mode in the Ge intrinsic layer and travel in longitudinal direction, a 50 μ m long Ge detector would achieve a responsivity of 0.76 A/W at 1650 nm, compared to 0.02 A/W responsivity expected from the same device with surface-normal illumination [82].

The speed of the photodetectors was measured using an impulse response measurement. In a measurement set-up shown in Fig. 7-6, Femto-second optical pulses

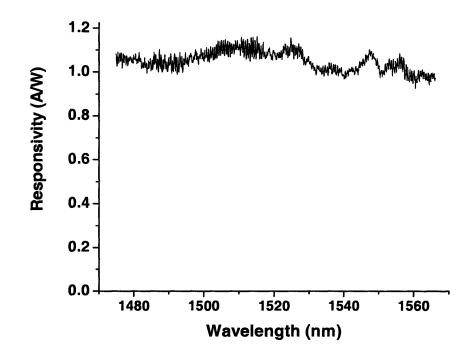


Figure 7-5: Dependence of responsivity on the wavelength. The Ge photodetector is 10m long and coupled with a SiN waveguide.

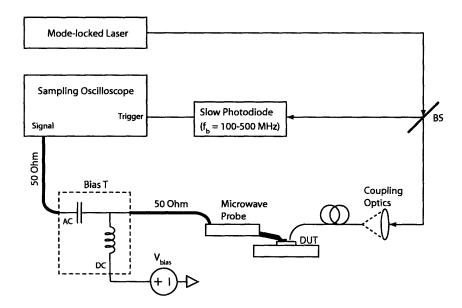


Figure 7-6: Schematic representation of an impulse response measurement system. The figure as drawn includes a free-space laser and coupling optics. In our measurement, a 1550 nm fiber-laser was used with a fiber splitter instead of free-space optics with a beam splitter. Courtesy of Dr. Wojciech Giziewicz.

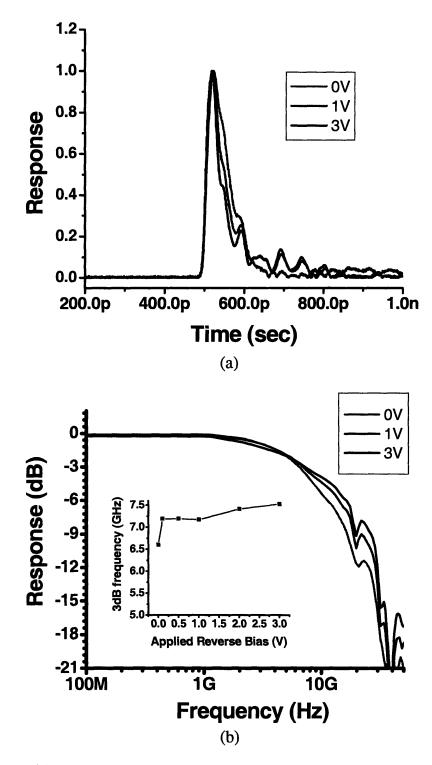


Figure 7-7: (a)Impulse response of a waveguide-integrated Ge photodetector at 1550 nm. (b)The transfer function $H(\nu)$, obtained by Fourier transform of the impulse response, shows \sim 7.5 GHz 3dB frequency.

with a center wavelength of 1550nm, produced by a mode-locked erbium fiber laser, were coupled into the waveguides. The laser pulse was guided through the waveguide and then absorbed by the Ge photodetector, generating an impulse response of the photocurrent.

From the measured detector impulse response function h(t) (Fig. 7-7(a)), the system's frequency response transfer function $H(\nu)$ is obtained by a Fourier transform, as in Fig. 7-7(b). The inset of Fig. 7-7(b) shows the frequency response for different reverse bias voltages. Without bias, the 3dB frequency is 6.6 GHz, equaling a bit rate of i11 Gbits/sec. With increasing reverse bias, the 3dB frequency reaches 7.5GHz at 3V.

The speed of the photodetector was RC-limited by 400 fF capacitance, which mainly resulted from the large probe pads used for easy probing. Therefore, if integrated with TIA, the bonding pads are no longer necessary and the Ge photodetector devices will achieve much higher bandwidth.

7.3 Conclusion

We developed Ge photodetectors monolithically integrated with silicon oxynitride and silicon nitride waveguides deposited on top of the photodetectors. High efficiency ($\sim 1.08A/W$) and high-speed (> 12 Gbit/s) performances were obtained. The Si CMOS-compatible detector devices retain their high performances even at low operation voltages, thus satisfying the low-voltage requirement of CMOS circuits, and have leakage currents that are low enough to meet the requirement of high-speed receiver designs.

Chapter 8

Germanium Photodetectors Integrated with Silicon Waveguides on SOI Substrate

In this chapter, we present the fabrication process and the measured performance of Ge photodetectors coupled with bottom Si waveguides on SOI substrate. This structure has the benefit of achieving a low-loss Si waveguide easily by using the crystalline Si layer of SOI substrate as a waveguide.

The goal was to integrate this photodetector device as a vital part of the electronicphotonic integrated circuit (EPIC) project. Therefore, special consideration was given to the compatibility issue of the photodetector with other photonic devices (such as modulator and filter) and Si CMOS driver circuit, in terms of device structure and process flow.

8.1 Process Flow and Device Fabrication

The process flow is shown in Fig. 8-1. The starting substrate was a SOI wafer with 200nm thick high-resistivity (13.5 - 22.5 ohm-cm) top Si layer. Because a Si waveguide is formed from the top Si layer, the layer must be doped as lightly as possible to minimize the waveguide loss due to free carrier absorption. The thickness

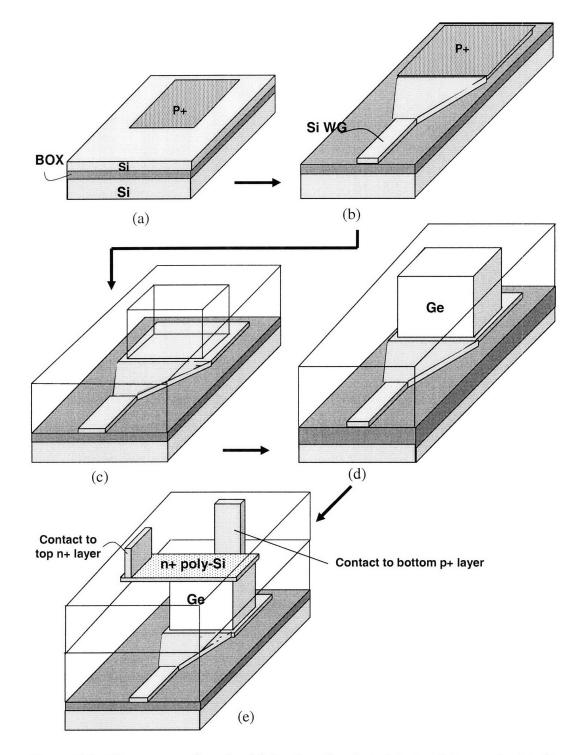


Figure 8-1: The process flow for fabricating Ge photodetector integrated with Si waveguide on SOI substrate.

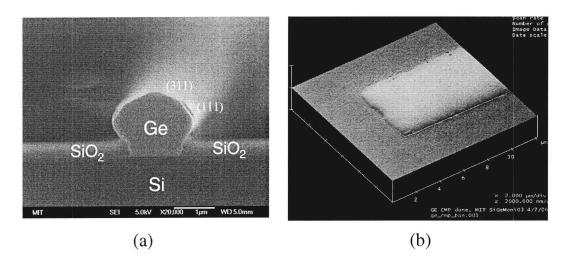


Figure 8-2: (a) cross-sectional SEM image of oxide trench overfilled with Ge (b) AFM image of a Ge-filled trench in the device area after CMP.

of the buried oxide layer was $2\mu m$, chosen to be sufficiently thick to prevent the mode in the waveguide from coupling to the substrate.

First, we patterned and implanted boron on the top Si layer only in the areas in which Ge photodetector were to be grown later (Fig.8-1(a)). This p^+ -doped area will serve as the bottom electrode of a vertical p-i-n photodetector. After activation annealing, a Si waveguide was patterned and etched (Fig. 8-1(b)). The etched Si waveguide had $500nm(W) \times 200nm(H)$ dimensions to maintain a single mode. We designed a taper structure such that the width of the Si bus waveguide gradually increases to that of the Ge photodetector (~ 2.5μ m), which generally requires greater width in order to accommodate contacts etc. As a mode expands laterally along the adiabatic taper, most optical power remains in a fundamental mode inside the waveguide. Therefore, the coupling behavior from Si waveguide to Ge photodetector can be approximated as a 2D slab structure. Next, we deposited an upper cladding oxide layer and carried out chemical-mechanical polishing (CMP) to flatten out the bump at the surface arising from the underlying waveguide. The thickness of the remaining silicon oxide on Si waveguide was $0.6\mu m$. In the area where a photodetector will be formed, oxide windows were patterned and etched to expose the Si active layer of the SOI substrate (Fig. 8-1(c)). Selective Ge epitaxial growth on Si followed to

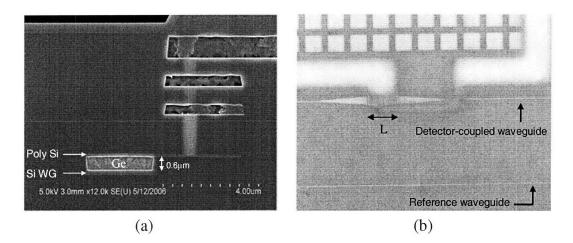


Figure 8-3: (a) Cross-sectional SEM image of a completed Si-waveguide-integrated Ge photodetector device, cut along A-A' line shown in Fig. 7-(a) (b) Top-view optical image of device. The one shown in this picture has a metal contact to the bottom p⁺-Si located at the side of Ge photodetector.

fill in the trench. Ge overgrew out of the trench and its facets, as determined by slow-growth planes, were (111) and (311) planes in the extruding parts (Fig. 8-2(a)). A CMP process followed to remove the overgrown Ge bulge (Fig. 8-1(d)). The post-CMP Ge top surface needs to be smooth in order to form a good p-i-n photodiode and prevent scattering loss of photons when they reach the Ge top surface. AFM measurement after CMP showed a RMS roughness of ~2nm (Fig. 8-2(b)). We grew 200nm poly-Si on top of germanium and implanted phosphorous to form the top n+ electrode. This n⁺ poly-Si electrode was extended to the side of the device, in order to keep the metal contact from affecting photon coupling behavior. Metallization was done by forming two different metal contacts to contact the bottom electrode which is on Si and to contact the top poly-Si pad (Fig. 8-1(e)). The completed device is shown in Fig. 8-3.

8.2 Device Performance Measurement

The measurement set-up for a waveguide-integrated photodetector is schematically shown in Fig. 8-4. The light signal from a 1470-1570nm wavelength-tunable laser is modulated by a low-frequency chopper and coupled to the waveguide on the sample

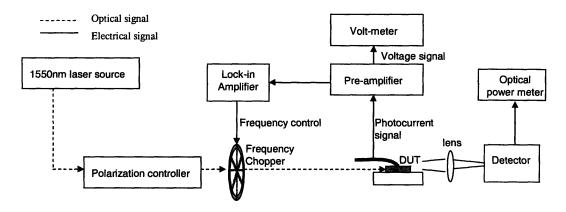


Figure 8-4: Schematic representation of a waveguide-integrated photodetector measurement system.

through a lens-tipped fiber. We simultaneously measure the optical power transmitted to the waveguide output with an objective lens and a discrete photodiode, as well as the photocurrent generated by the waveguide-integrated photodetector on the chip by probing the device. The lock-in amplifier extracts the photocurrent signal in sync with the chopper frequency such that only the photocurrent from the optical signal is included in the measurement.

The measured photocurrent by this method is compared with the incoming optical power, which we replaced by the power measured from the reference waveguide situated next to the device of interest. The photocurrent increases linearly with the incoming optical power (Fig. 8-5), suggesting the photocurrent measurement is reliable. From the slope of the plot in Fig. 8-5, the responsivity of 0.227A/W is obtained. It corresponds to 18.2% quantum efficiency.

The waveguide-to-photodetector photon coupling can be studied from the change in photocurrent and unabsorbed optical power as a function of detector coupling length, as shown in Fig. 8-6. From Fig. 8-6(a), the optical power unabsorbed in the photodetector and transmitted to the output waveguide quickly drops to less than 10% of the original power even after the shortest (5 μ m long) photodetector. Fig. 8-6(b), the responsivity in terms of detector coupling length, shows that responsivity quickly rises to a certain value at a short photodetector and saturates. Compared to the evanescent coupling cases previously studied in Chapter 4(Fig. 4-4, 4-5, and

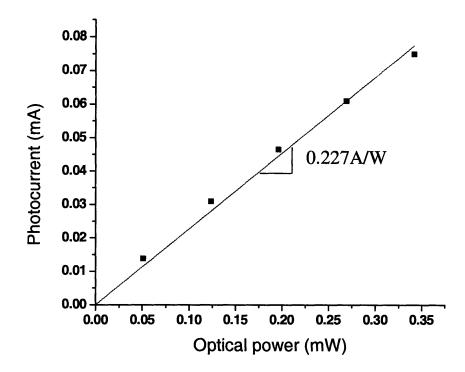


Figure 8-5: Photocurrent vs. the optical power that enters the waveguide-integrated photodetector, measured from the L= 20μ m long device.

4-9), it is clear that the coupling from Si waveguide to Ge photodetector occurs quickly within a short coupling length, as the simulation studies discussed in Chapter 6 suggest.

The change in photodetector responsivity as a function of wavelength provides an additional information. In a 5μ m-long photodetector device shown in Fig. 8-7(a), a decrease of photocurrent in the wavelength range of $\lambda > 1510$ nm was observed. The coupling behavior from waveguide to photodetector does not change significantly as a result of a 100nm wavelength variation. Instead, it is the absorption of Ge material itself that leads to the wavelength dependence in Fig. 8-7(a). Ge has a direct bandgap around 1510nm and it makes the absorption of photon at $\lambda > 1510$ nm less efficient than that at $\lambda < 1510$ nm.

However, in longer photodetector devices, the photons that remain unabsorbed after, e.g., the first 5μ m continue to travel along a coupling structure as confined within Ge and Si layer until they are fully absorbed. Therefore, a longer photodetector

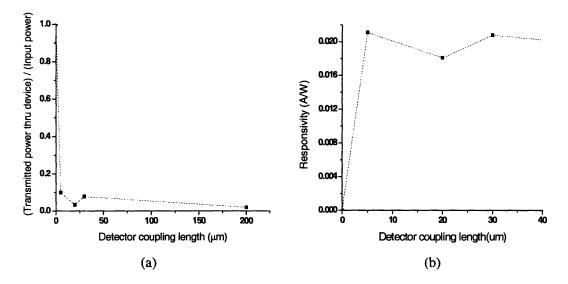


Figure 8-6: (a) the normalized transmitted optical power through the waveguide output and (b)the responsivity of the waveguide-integrated Ge photodetector, as a function of photodetector coupling length.

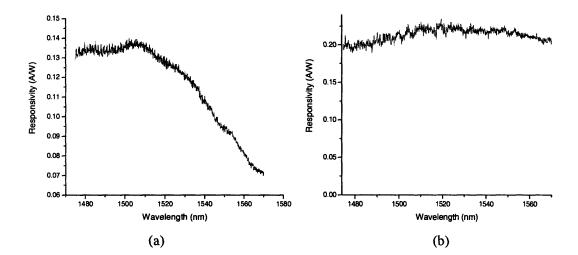


Figure 8-7: The change of the photodetector responsivity under a given constant incoming optical power as the wavelength of optical signal varies (a) for a $L = 5 \ \mu m$ long photodetector device (b) for a $L = 20 \ \mu m$ long photodetector device.

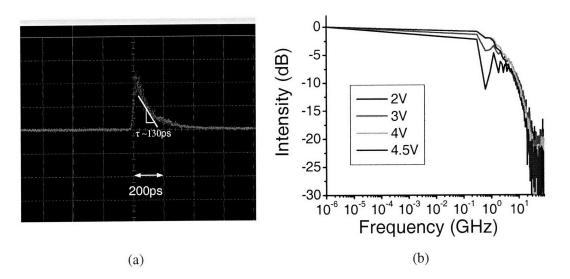


Figure 8-8: (a)Impulse response of a 5μ m long Ge integrated photodetector (b) the transfer function $H(\nu)$ shows ~1.3GHz 3dB frequency

device eventually should have as high an absorption efficiency for $\lambda > 1510$ nm as for $\lambda < 1510$ nm. This is demonstrated by 20μ m long Ge photodetector device in Fig. 8-7(b).

This experimental observation demonstrates the benefit of integration of the photodetector with waveguide. The waveguide-integrated photodetector can have a high efficiency even in the regime where the photodetector material absorbs inefficiently, by increasing the photodetector coupling length. Increased photodetector length does not decrease the speed of the photodetector, because RC-time response does not play a role due to its compact size in properly designed devices and its transit-time response is not affected due to the photon travel path decoupled from the carriers' collection path.

The speed of the photodetector was measured by an impulse response measurement setup, the same as shown in Fig. 7-5. Femto-second pulses produced by the mode-locked laser were launched into the waveguide coupled to a photodetector and the responding photocurrent signal were captured into the oscilloscope. The decay time of the photocurrent signal measured in 5μ m long photodetector was about 130ps (Fig. 8-8(a)).

From the measurement data of the detector impulse response function h(t), the

system's frequency response transfer function $H(\nu)$ is obtained by Fourier transform. That is,

$$H(\nu) = \int_{-\infty}^{\infty} f(t) exp(-i2\pi\nu t) dt$$
(8.1)

Applying the Fourier transform to the data in Fig. 8-8(a), we obtained the frequency response transfer function. The 3dB frequency is found to be ~ 1.3 GHz (Fig. 8-8(b)).

8.3 Discussion

The performance results of the Ge photodetectors demonstrated in this chapter are not as good as those of the top-waveguide coupled Ge photodetectors demonstrated in Chapter 7.

Most of all, the problem is that the overall leakage current of the selectively-grown Ge photodetector are orders of magnitude higher compared to the Ge photodetectors demonstrated in Chapter 7, which is made with blanket grown Ge film.

High-resolution TEM pictures in Fig. 8-9 can provide the clues to the Ge materials quality. The Fig.8-9(a) shows the Ge film grown selectively in the oxide trench of our devices and demonstrates the problem. It seems that RIE plasma etching of oxide trench has damaged the Si surface significantly. A thin Ge amorphous layer is formed at Ge/Si interface and the film above it has twins and other line defects. Another possibility could be that the polymer from the photoresist during the plasma etching got deposited into the trench and formed a fluoride polymer layer on Si surface, which could not be removed later. In contrast, the Fig.8-9(b) is from a Ge film growth in an oxide trench prepared with wet-etching of the oxide. It has an undamaged smooth Si/Ge interface as expected. Ge film quality is very good only with a few misfit dislocations at the interface, which are expected due to the lattice mismatch between Si and Ge. Since the same wafer cleaning and Ge growth conditions were used except the difference in the oxide etching process, the problem in the oxide etching process seems to result in the under-performance of our devices. We expect that, by plasmaetching the oxide trenches partially leaving the thin oxide and removing the thin oxide with wet-etching, the performance of re-fabricated devices will be improved greatly.

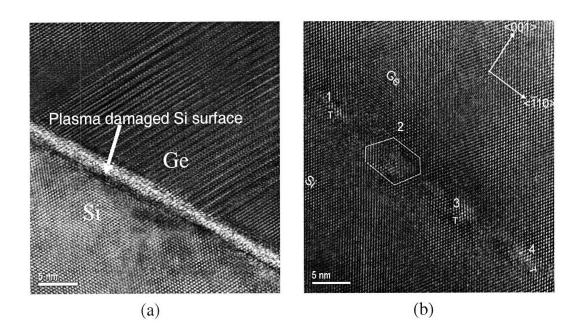


Figure 8-9: High-resolution transmission electron microscopy (HRTEM) images of (a)Ge grown in a dry etched oxide trench. A plasma-damaged Si surface of 2-3nm is revealed. (b) Ge grown in a wet etched oxide trench. 1 - 4 indicate misfit dislocations at the Si/Ge interface. Courtesy of Jinggang Lu and George Rozgonyi from North Carolina State University.

The another factor that is suspected to have affected the device performance is the series resistance of the photodetector devices. Achieving a low series resistance of the photodetector is very important because, otherwise, the speed of the photodetector will be limited by RC-limited bandwidth $f_{RC} = 1/(2\pi RC)$ with high R. Our devices seem to have large series resistance ranging over a few kilo-ohms. The challenging part, compared to the low-resistivity p⁺ Si substrates used in Chapter 7, is to form a good conducting layer on a 200nm thin Si layer on SOI substrate and achieve a low overall resistance. The implantation and activation-annealing/healing processes have to be optimized, in order to achieve the high concentration of active dopants but avoid the complete amorphization of Si layer and the resulting difficulty in the following healing processes.

Chapter 9

Conclusion

9.1 Summary and Overview

Optical clocking has emerged as an innovative alternative approach to electrical clocking, in order to overcome synchronization problems faced in high-performance multi-GHz systems. We have identified H-tree waveguide network and waveguide-integrated photodetectors as key photonic devices required for intrachip optical clocking for microprocessors.

In Chapter 2, we have demonstrated successful optical signal distribution through CMOS compatible on-chip $SiO_x N_y$ waveguide H-tree network with 64 fanouts. A variable bending radius approach in H-tree design was used to optimize the performance of the optical clock signal distribution. Conventional y-splitter showed significant optical loss and poor power split ratio. Especially, it was found that unequal power-splitting becomes increasingly problematic as the number of levels of a H-tree network increases and can result in increased skew. We devised a novel extended offset splitter, which reduced the splitting loss to < 3% and demonstrated 49:51 power split ratio.

Another essential technology component for optical clocking is a waveguide-integrated photodetector. Integration technology of waveguide and photodetector is important not only for optical clocking application but also for broader applications of photonic integrated chip. We discussed key performance parameters of waveguide-integrated photodetectors and investigated their relations to the device design in Chapter 3.

In Chapter 4, we have experimentally demonstrated SiO_xN_y -waveguide-integrated silicon photodetectors that employ the top-to-bottom evanescent-wave coupling structures. We achieved over 90% photon coupling efficiency from SiON waveguide to Si photodetectors. A two-step process that consists of 1) mode-coupling from a guided mode in the input waveguide to a leaky mode in the waveguide in contact with photodetector and 2) gradual evanescent wave coupling from waveguide towards photodetector, was a main coupling mechanism in the case of coupling with lower indexcontrast waveguide, in contrast to high index-contrast waveguide case where coupling occurred nearly instantly at the front part of photodetector. It was shown that intentional introduction of abrupt step in the waveguide at the transition interface to coupling region can improve mode-matching efficiency.

In order to enhance the photodetector speed, it is necessary to use only thin photodetector layer. SOI or GOI(Germanium On Insulator) substrate that provide thin photodetector layer with buried oxide can enable photodetectors to achieve high efficiency and high speed. We have found that evanescent coupling behavior is quite different from that of coupling to bulk absorbing material.

Therefore, using SiON as waveguide material and thin Si photodetector on SOI substrate, we developed a simple and intuitive model that explains the evanescent coupling behavior between waveguide and detector in Chapter 5. By treating the whole structure as a combination of two individual waveguides and analyzing each waveguide with a ray-optics approach, we showed that treating this coupling structure as waveguide-to-waveguide coupling is effective and phase matching between a leaky mode in the waveguide and that in the Si layer is the key condition for efficient coupling. We demonstrated that our Leaky-Mode model provides a very simple but also a precise way to find optimal coupling conditions both for 2D and 3D coupling structures. The study showed that the Si layer thickness is the most critical factor that needs precise design and process control in this structure. With higher Δn (= $n_{core} - n_{cladding}$) waveguide design, the coupling rate to the Si layer gets enhanced and becomes less sensitive to the Si layer thickness. Therefore, the change in coupling

rate as a function of the Si layer thickness shows resonance-like dependence with low Δn waveguide design and oscillation-like dependence with high Δn waveguide.

Based on the understandings on waveguide-to-photodetector coupling obtained from experimental and theoretical studies in previous chapters, we constructed an evanescent coupling design map for Si photonics materials in Chapter 6. We found that the evanescent coupling rate increases and the coupling process I (direct photon coupling from the input waveguide to photodetector, which occurs at the entering interface, without first being coupled to the waveguide on the photodetector) becomes more dominant, as 1) the waveguide core has higher refractive index such that n_{PD} n_{WG} decreases and 2) the waveguide geometrical factor as defined in Section 6.1 increases.

We also discussed the possible structure designs for the waveguide-integrated Ge photodetector in Chapter 6 and demonstrated optical simulation results. We have shown that photon coupling from Si waveguide on SOI substrate to Ge photodetector occurs immediately as Si waveguide faces Ge and photons propagate while oscillating between the Si and Ge layer. We demonstrated employing a tapered Ge structure helps avoid abrupt change of light propagation mode and, as a result, enhances the coupling efficiency to Ge layer in case that Si substrate is used. We suggested a lateral p-i-n photodetector with a high-index feature placed in the center of the coupling structure, as it can concentrate the mode into central region such that the speed of photodetector is enhanced.

We presented, in Chapter 7, Ge photodetectors monolithically integrated with silicon oxynitride and silicon nitride waveguides for top-coupled photodetectors. High efficiency (1.08A/W) and high-speed (i 12 Gbit/s) performances were obtained. The Si CMOS-compatible detector devices retain their high performance even at low operation voltages, thus satisfying the low-voltage requirement of CMOS circuits, and have leakage currents that are low enough to meet the requirement of high-speed receiver designs.

In Chapter 8, we have fabricated Ge photodetectors integrated with Si waveguides on SOI substrate. After Si waveguide was formed on SOI substrate, Ge was selectively grown on p^+ doped area of Si waveguide and then vertical p-i-n photodetector was formed by putting n^+ poly silicon. We have demonstrated the responsivity of 0.227A/W and the 3dB frequency of 1.3GHz.

9.2 Proposed Structure Optical Clock Signal Distribution

In this section, we discuss potential prototype structures for intrachip optical clock signal distribution system. Two important key technology issues are 1) photonic devices design that satisfy the performance requirement and 2) system structure and processing designs that allow the co-integration of photonic and electronic devices on the same chip without compromising the performance of microprocessor chip.

Fig. 9-1 shows the schematic optical clocking system structure and a few essential components. One possible structure is the one that uses the same silicon active layer of SOI substrate to form both CMOS electronics and Si H-tree waveguide network. The wavelength $\lambda > 1.1 \ \mu$ m is used. For this structure, a compact 1×2 Si MMI (multi-mode interferometer) can be a good choice for splitter (Fig. 9-1(b)) and the bottom-waveguide-coupled Ge photodetector discussed in chapter 7 can be used.(Fig. 9-1(d)). Lateral or vertical can be used. We should note that since Si waveguide requires 2-3 μ m oxide for cladding around itself, the H-tree waveguide interferes with the real estate of CMOS electronics on Si active layer and the CMOS devices on one side of the waveguide will have to communicate with the devices on the other side of the waveguide only through about 10 μ m long metal interconnect line. Therefore, the chip circuitry design has to be redone considering these restraints.

The other possible structure for optical clocking system is the one that uses deposited waveguides above the CMOS electronics level. For this structure, the silicon oxynitride (SiO_xN_y) , silicon nitride (Si_3N_4) , or deposited amorphous silicon can be used as waveguide material. With dielectric waveguide material, the shorter wave-

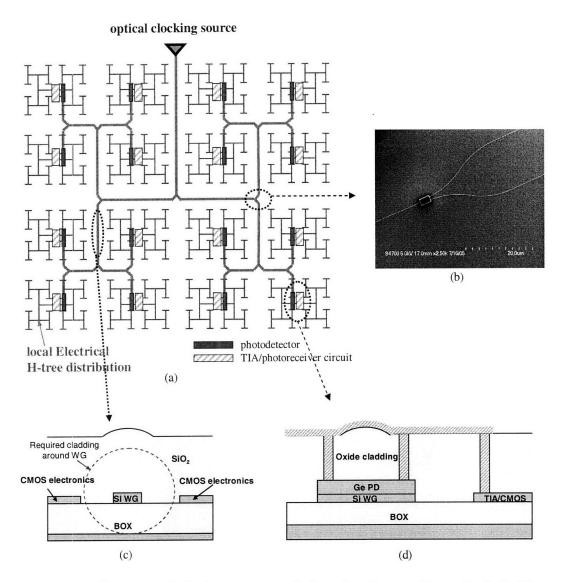


Figure 9-1: System and device structure designs for the on-chip optical clocking system that has both CMOS electronics and Si H-tree waveguide on the same silicon active layer of SOI substrate (a) schematic optical clocking structure (b) Si 1×2 MMI suggested for a splitter in H-tree waveguide network (c) the cross-sectional structure around the H-tree bus waveguide (d) A bottom-waveguide-coupled Ge photodetector and connection to the TIA circuit.

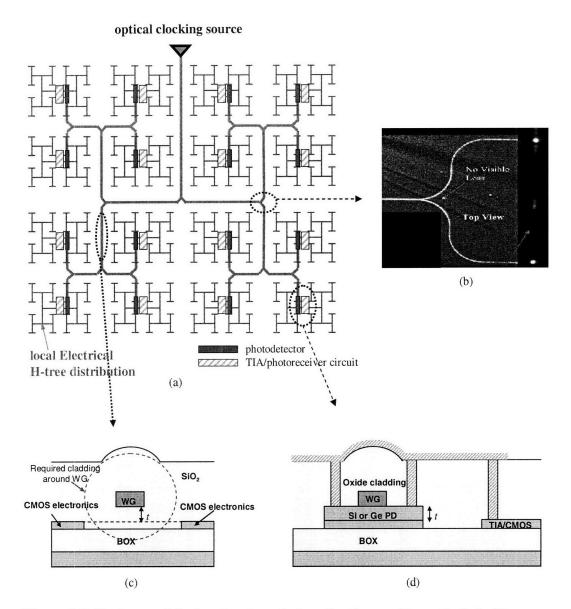


Figure 9-2: System and device structure designs for the on-chip optical clocking system that uses deposited waveguides above the CMOS electronics level (a) schematic optical clocking structure (b)A suggested SiON waveguide offset splitter, as shown in chapter 2 (c) the cross-sectional structure around the H-tree bus waveguide (d) A top-waveguide-coupled photodetector and connection to the TIA circuit.

length such as 850nm can be used. For splitters, the design presented in chapter 2 can be used (Fig. 9-2(b)). For photodetectors, the top-waveguide-coupled designs can be used with Si or Ge detector material (Fig. 9-2(d)). The regular silicon substrate may be used, but the SOI substrate still provides the benefits for the photodetectors, as we discussed throughout this thesis (chapter 5,6,8 etc.). Another essential issue that needs consideration is the height level of the waveguide above the Si CMOS surface level. The waveguide needs about 3 μ m (or even more with low-index waveguide material) oxide cladding around itself. If plain Si substrate is used and the waveguide is placed 3-4 μ m above the substrate surface, the coupling from the waveguide to the photodetector that is located on the device level can be a difficult problem. Generally, it is desirable that the waveguide level height from the Si surface (t in Fig. 9-2(c)) matches the intrinsic layer thickness of photodetectors. Since $t < 1 \mu m$ is preferable for high-speed photodetector, SOI substrate can help on the issue by providing a few micrometer thick buried oxide for undercladding (Fig. 9-2(d)). For these reasons, SOI still may be necessary for the structure with the upper deposited waveguides and the issue of dividing the CMOS electronics real estates may remain.

In terms of fabrication processes, the process flow and individual processes will have to be redesigned in order to allow the co-integration of photonic and electronic devices, especially when Ge material is introduced. For example, the Si CMOS process can be partially completed first and then Ge can be introduced by an epitaxial process on selective areas when there are no more high temperature steps required for Si CMOS side, which may damage Ge. Ge growth and annealing steps alters the thermal history of Si CMOS devices. Therefore, Si CMOS processes may need to be modified in consideration of the following Ge growth steps.

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