Degradation Mechanisms of GaN High Electron Mobility Transistors

by

Jungwoo Joh

B.S. Electrical Engineering, Seoul National University, 2002

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

Master of Science in Electrical Engineering

at the
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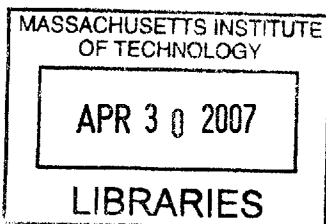
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ABSTRACT

In spite of their extraordinary performance, GaN high electron mobility transistors (HEMT) have still limited reliability. In RF power applications, GaN HEMTs operate at high voltage where good reliability is essential. However, physical understanding of the fundamental reliability mechanisms of GaN HEMTs is still lacking today. In this thesis, we carry out systematic reliability experiments on industrial GaN HEMTs provided by our collaborators, TriQuint Semiconductor and BAE systems. In our study, GaN HEMTs have been electrically stressed at various bias conditions while they are being characterized by a benign characterization suite. We have confirmed that electrical stress on devices results in an increase in drain resistance R_D and a decrease in maximum drain current I_{Dmax}. During the stress, traps are found to be generated. We have seen that this degradation is driven mostly by electric field, and current is less relevant to electrical degradation. From a set of our experiments, we have hypothesized that the main mechanism behind device degradation is defect formation through the inverse piezoelectric effect and subsequent electron trapping. Unlike current conventional wisdom, hot electrons are less likely to be the direct cause of electrical degradation in the devices that we have studied. Our studies suggest a number of possibilities to improve the electrical reliability of GaN HEMTs.

Thesis supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

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Contents

List of Figures 9

List of Tables 13

Chapter 1. Introduction 15

1.1. Introduction of GaN HEMT 15

1.2. Motivation 16

1.3. Previous Studies 17

1.4. Project Goals and Thesis Outline 19

Chapter 2. Experimental 21

2.1. Introduction 21

2.2. Devices 21

2.3. MIT Reliability Test Chip 22

2.4. Electrical Experiments 24

2.4.1. Experimental Setup 25

2.4.2. Characterization Suite 27

2.5. Stress Test Methodology 29

2.6. Summary 31

Chapter 3. Degradation Experiments 33

3.1. Overall Degradation Phenomena 33

3.2. OFF-state Step-stress 37

3.3. V_{DS}=0 Condition 38

3.4. Other Observations 40

3.4.1. Effect of Environment 41

3.4.2. Degradation of MISFET 42

3.4.3. Critical Voltage in other Stress Bias Conditions 44

3.4.4. The Origin of Gate Leakage Degradation 47
3.4.5. Effect of L_{GD} 48
3.5. Trapping Behavior 51
3.5.1. Off-state Stress-recovery 51
3.5.2. Enhanced Detrapping 53
3.6. Trap Generation 56
3.7. TLM Step-stress 58
3.8. Summary of Key Findings 60

Chapter 4. Degradation Mechanism 63
4.1. Introduction 63
4.2. Inconsistency with Hot-electron Related Mechanisms 63
4.3. Piezoelectric Effect of GaN 64
4.4. Hypothesis for Electrical Degradation of GaN HEMTs 65
4.5. Order-of-magnitude Calculation 67
4.6. Experimental Confirmation 69
4.6.1. L_G Dependency in V_{DS}=0 State 69
4.6.2. AlGaN Buffer 72
4.6.3. XTEM 73
4.7. Suggestions for Reliability Improvements 75
4.8. Conclusions 76

Chapter 5. Conclusions 77
5.1. Summary of Key Findings 77
5.2. Suggestions for Further Work 80

Bibliography 83

List of Figures

Figure 1-1. Change of I_D and P_{out} in a power soak stress test (data from TriQuint). Stress condition: 10 GHz, V_D=28 V, I_{DQ}=150 mA/mm, P_{in}=23 dBm, P_{out}=33.7 dBm.................. 16

Figure 1-2. Increased current collapse after a stress test (dashed: before stress; solid: after stress) [13]. 18

Figure 1-3. Degradation mechanism in AlGaN/GaN HEMT under high stress condition [17]. 19

Figure 2-1. Schematic cross section of GaN HEMT. 21

Figure 2-2. MIT reliability test chip. 23

Figure 2-3. A schematic of the whole experimental setup. 25

Figure 2-4. Graphical user interface of a stress experiment program. A window to select the type of stress experiment and to input stress bias conditions is shown. 26

Figure 2-5. Change in normalized drain and source resistance after 300 device characterizations. In phase I, basic figures of merit are extracted. In phase II, full output characteristics are also measured. In phase III, full transfer and sub-threshold characteristics are measured on top of the basic characterization and output characteristics measurement. 28

Figure 2-6. Conceptual stress schemes: (from left to right) stress-recovery, step-stress, and step-stress-recovery. 30

Figure 2-7. Stress bias points: High Power, ON state, OFF state, and V_{DS}=0 conditions.... 31

Figure 3-1. Change in normalized I_{Dmax}, R_D, and R_S in step-stress experiment in the high power state (V_{DS}=5~30 V in 5 V steps, I_D=800 mA/mm, 30 minutes per step). 34

Figure 3-2. Threshold voltage change in the same experiment as Figure 3-1 35

Figure 3-3. Output characteristics before (solid) and after (dashed) the same stress test as in Figure 3-1. V_{GS}=-4~2 V (2 V step). 35

Figure 3-4. Change in sub-threshold characteristics before (solid) and after (dashed) the same experiment as Figure 3-1. 36

Figure 3-5. Change in g_m before (solid) and after (dashed) the same experiment as Figure 3-1. 36

Figure 3-6. Change in normalized I_{Dmax}, R_D, and R_S in step-stress experiment in the OFF state (V_{DS}=5~40 V in 5 V steps, I_D=25 mA/mm, 30 minutes per step). 37

Figure 3-7. Change in normalized I_{Dmax}, R_D, R_S, and I_{Goff} as a function of stress voltage in a step-stress experiment in V_{DS}=0 state (V_{DG}=10~50 V in 1 V steps). 38

Figure 3-8. Stress current of the experiment in Figure 3-7. 39

Figure 3-9. Change in I_{Dmax}, drain current at stress bias point I_{D0}, and gate current at stress bias point I_{G0} in another V_{DS}=0 step stress experiment. 40

Figure 3-10. Change in normalized I_{Dmax} in V_{DS}=0 stress-recovery experiment with and without nitrogen gas. V_{GS}=-40 V is applied during the stress period of 120 minutes. 41

Figure 3-11. Typical I_{Dmax} (left) and I_{Goff} (right) degradation of MISFET and HEMT in V_{DS}=0 step-stress experiments. 42

Figure 3-12. The correlation between the critical voltage for I_D degradation and I_G degradation (triangle: HEMT, circle: MISFET) 43

Figure 3-13. The correlation between the current collapse increase and I_{Dmax} degradation (triangle: HEMT, circle: MISFET) 44

Figure 3-14. Change in I_{Dmax} in step-stress experiments and the critical voltage V_{DGcrit} for I_{Dmax} degradation. 46

Figure 3-15. Change in V_T in the same experiment in Figure 3-14. In V_{DS}=0 state, threshold voltage is not properly extracted after 25 minutes as the minimum drain current became larger than 1 mA/mm. 46

Figure 3-16. Change in gate leakage current I_{Goff} in the same experiment in Figure 3-14 and the critical voltage for I_{Goff} degradation. 47

Figure 3-17. Change in I_{Goff}, I_{Gss1}, and I_{Gss2} as a function of stress bias V_{DG} in an OFF state step stress experiment. I_{Gss1} is gate leakage current through gate to drain junction, and I_{Gss2} is gate leakage current through gate to source junction. 48

Figure 3-18. L_{GD} dependency of source and drain resistance of fresh devices. 49

Figure 3-19. Change in normalized R_D in OFF state stress experiments on different L_{GD} devices. Five different devices with different L_{GD}=1~5 um are stressed at V_{DS}=30 V and V_{GS}=-5 V for 50 minutes. 50
Figure 3-20. Absolute value of change in R_D and R_S as a function of L_{GD} in the same experiment as Figure 3-19. 50
Figure 3-21. Change in I_{Dmax}, R_D, and R_S in a stress-recovery experiment in the OFF state (V_{DS}=30 V, I_D=20 mA/mm) for 30 minutes of stress followed by 30 minutes at rest. This cycle is repeated for three times. 52
Figure 3-22. Time evolution of I_{Dmax} of the device in Figure 3-1. After the end of the stress experiment in Figure 3-1, the device was put at rest for 304 days before it were measured again. After the first measurement of I_{Dmax}, the same stress (V_{DS}=30 V, I_D=800 mA/mm) was applied for 2 more minutes 53
Figure 3-23. Change in I_{Dmax} in a stress-recovery experiment on a standard type device stressed at V_{DS}=0 and V_{GS}=-30 V for 15 minutes and at rest for 15 minutes. Additional stress is applied for another 10 minutes. From t=20 to 25 min, microscope light was illuminated. 54
Figure 3-24. Change in I_{Dmax} in a stress-recovery experiment on a standard type device stressed at V_{DS}=0 and V_{GS}=-30V for 30 minutes. Four stress cycles are repeated with different values of V_{GS} during the 30 minutes recovery phase (0, 1, 2, and 3 V). 55
Figure 3-25. Detrapping time constants in V_{DS}=0 stress-recovery experiments. 55
Figure 3-26. Change in I_{Dmax} and stress bias of a V_{DS}=0 step-stress-recovery experiment. V_{GS}=-15~-40 V is applied for stress, and -10 V diagnostic voltage pulses are applied during the recovery phase. The step size is -2.5 V, and the device is stress for 10 minutes in each step. To expedite detrapping, microscope light is turned on during the test. 57
Figure 3-27. Total damage and current collapse produced by diagnostic pulse as a function of the stress bias 58
Figure 3-28. A schematic picture of a HEMT and a TLM used for the comparison. L_{GD} of the HEMT is identical to the length of the TLM. 58

Figure 3-29. Change in I-V characteristics of the TLM before and after the experiment of Figure 3-30. The device was step-stressed at V=20~26 V for 140 minutes........................59
Figure 3-30. Change in I_{Dmax} of a TLM and a HEMT and low field resistance of the TLM. The HEMT is stressed at V_{DS}=20~26 V (1 V step, 20 min/step) and I_D=800 mA/mm. The TLM is stressed at the same voltage, but the current is around 1.7 A/mm. The length of the TLM (3 um) is the same as the gate-drain gap of the HEMT. 60
Figure 4-1. Schematic conduction band diagram of AlGaN/GaN heterostructure [23].......65
Figure 4-2. Vertical electric field under the gate edge and produced tensile strain due to inverse piezoelectric effect. 66
Figure 4-3. Comparison of measured critical thicknesses for strain relaxation in $Al_xGa_{1-x}N$/GaN [24]. 68
Figure 4-4. Gate length dependence of degradation in V_{DS}=0 step-stress experiments. Different gate length devices (L_G=0.25, 0.65, and 1.15 um) are stressed at V_{DS}=0 and V_{GS}=-15~-34 V (-1 V step, 5 min/step). The threshold of the degradation increases with L_G. 70
Figure 4-5. Overlap of strain field at the center of the gate region in the V_{DS}=0 state. 70
Figure 4-6. Change in R_D in stress experiments on different gate length devices (L_G=0.25, 0.35, 0.65, and 1.15 um) in V_{DS}=0 state (upper left), in OFF state (upper right), and in high power state (bottom). Stress conditions are V_{GS}=-30 V in the V_{DS}=0 state, V_{DS}=35 V and V_{GS}=-5 V in the OFF state, V_{DS}=25 V and I_D=800 mA/mm in the high power state. These devices are stressed for 50 minutes. 71
Figure 4-7. Total damage as a function of stress bias in V_{DS}=0 step stress experiment on type A1 (GaN buffer) and type A3 (AlGaN buffer) devices. 72
Figure 4-8. Output power degradation of 400 um type A1 devices (baseline structure, GaN buffer) and type A3 devices (AlGaN buffer). The devices are stressed at P_{out}=5 W/mm, V_{DS}=28 V, f=10 GHz...73
Figure 4-9. XTEM images of a degraded GaN HEMT. Left: source side; right: drain side [7]. 74

List of Tables

Table 2-1. Definition of device parameters measured by the characterization suite............ 27

Table 2-2. Changes in important figures of merit after 300 runs of the device characterization suite. 29

Table 3-1. Stress bias condition for three different step-stress experiments. 45

Chapter 1. Introduction

1.1. Introduction of GaN HEMT

Traditionally, GaN is used for optoelectronic devices. GaN-based light emitting diodes and laser diodes have become very important devices in lightning and blu-ray technology. GaN technology for optoelectronics has already achieved the state of mass production. Recently, GaN high electron mobility transistors (HEMT) have also become of great interest for high-voltage switching and RF power applications. As a result of the large band gap (~3.4 eV) and high breakdown electric field (>$3x10^6$ V/cm) of GaN, GaN-based devices can operate at a voltage as high as 120 V [1]. Also, due to strong piezoelectric effect and spontaneous polarization of both GaN and AlN, high sheet carrier density (~10^{13} cm^{-2}) can be achieved at the AlGaN/GaN heterointerface without any doping. In addition, high electron mobility (~1500 cm^2/V-s) and high saturation velocity (~$2x10^7$ cm/s) make GaN-based devices suitable for high power amplification at high frequencies [2]. A large conduction band offset between AlGaN and GaN is also desirable for carrier confinement in the channel. With all these characteristics, AlGaN/GaN HEMTs have already been demonstrated with an output power density of 10.7 W/mm at 10 GHz [3]. Recently, GaN-based HEMTs have also expanded their frequency range - a power density of 2.1 W/mm has been demonstrated at 80.5 GHz [4]. This outstanding performance makes these devices of great interest for high-power, high-frequency applications such as WiMAX or WLAN base stations and radars.

1.2. Motivation

The greatest impediment today preventing the wide deployment of GaN HEMT technology is its limited electrical reliability. As GaN is still a relatively new material system for electronic devices, many problems in material quality and process controls have not been solved yet. As shown in Figure 1-1 for some of the devices studied in this research, output power as well as the drain current decreases, and device characteristics degrade even just after a few hours under typical RF device operation. In particular, because GaN HEMTs are usually operated at high voltage and high current, high reliability is not only demanding but also challenging, and designs that maximize reliability are absolutely needed. In order to tackle this reliability problem, we need to understand physical failure mechanisms. However, at the present time, there is insufficient understanding of the fundamental mechanisms limiting the reliability of GaN HEMTs.

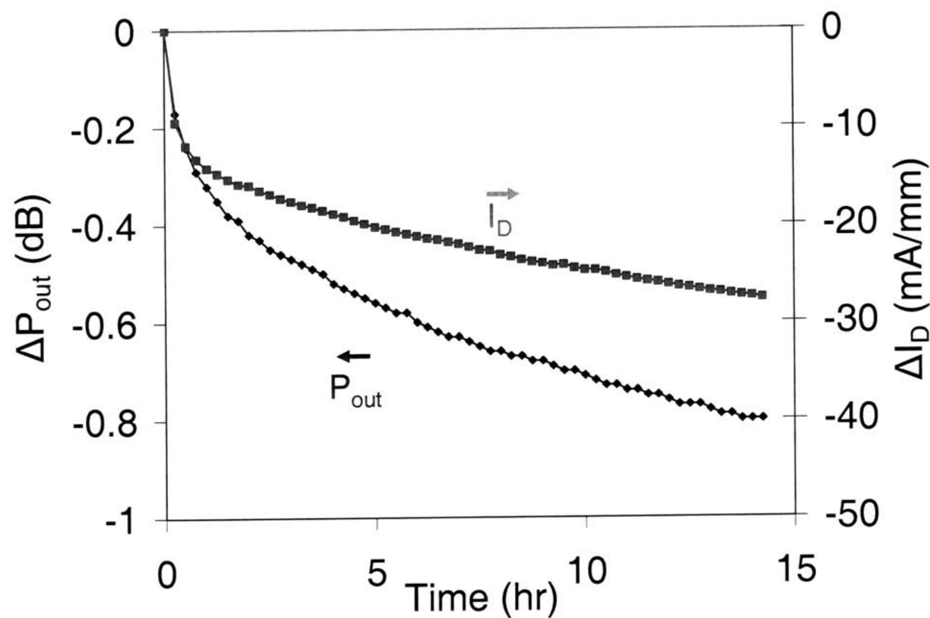

Figure 1-1. Change of I_D and P_{out} in a power soak stress test (data from TriQuint). Stress condition: 10 GHz, V_D=28 V, I_{DQ}=150 mA/mm, P_{in}=23 dBm, P_{out}=33.7 dBm.

1.3. Previous Studies

In previous studies, it has been shown that GaN HEMTs degrade significantly after bias stress test. In particular, reduction of drain current and output power was observed [5-9]. This degradation is reported to be accompanied by an increase in drain resistance although source resistance is relatively unaffected by electrical stress [5, 10]. Along with I_D degradation, transconductance degradation is observed [5, 11, 12], but there have been no agreement on the changes in threshold voltage. Also, after device operation, increased trapping behavior has been observed [11, 13]. On the other hand, no obvious ohmic contact degradation has been found after device degradation [6, 10]. Although there have been some studies on long term reliability [11], most of the reliability studies have focused on device degradation in a relatively short period of time, as GaN HEMTs normally degrade within a few hours of device operation.

Many of the previous studies on reliability have suggested that hot electrons are at the center of device degradation. The prevailing hypotheses are hot-electron induced trap formation [11] and electron trapping at the surface [5]. Sozza et al. have proposed that an increase of trap density at the surface region between gate and drain is the origin of device degradation [11]. They have also postulated that the same type of trap that causes current collapse is involved in the degradation mechanism. They have attributed this increase in trap density to hot electron effects. Also, as shown in Figure 1-2, it has been observed that current collapse increases after a bias stress test [13]. The current collapse is a temporary decrease of drain current after applying high voltage to the device.

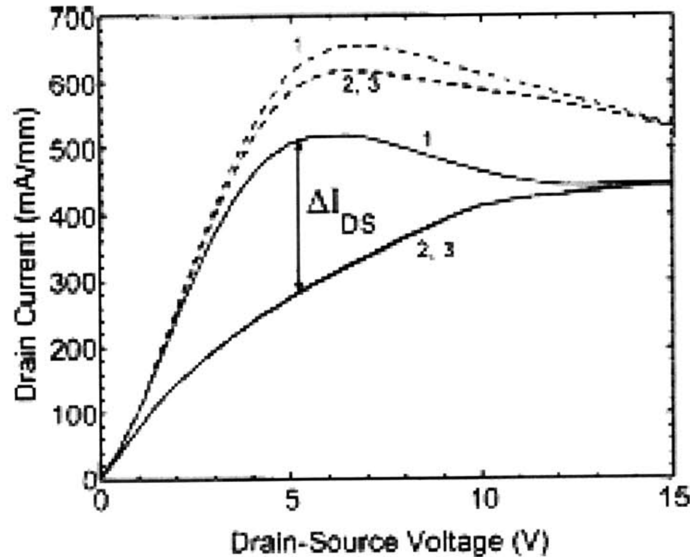

Figure 1-2. Increased current collapse after a stress test (dashed: before stress; solid: after stress) [13].

It has been reported that GaN HEMTs suffer from current collapse. It is widely believed that under high voltage, surface states between the gate and the drain trap hot electrons. These trapped electrons at the surface deplete the channel in the extrinsic drain resulting in a reduction of the drain current [14]. SiN passivation is known to reduce this current collapse problem. It has also been argued that electron trapping in the bulk causes the current collapse [15]. Another explanation for the current collapse is a reduction of tensile strain in the extrinsic device under negative gate bias [16].

Kim et al. have also argued that device degradation is attributed to hot electron trapping [5]. They have observed an increase in drain series resistance and suggested that this increase is caused by an increase of channel depletion due to electron trapping at the surface region between gate and drain [17]. As shown in Figure 1-3, hot electrons can gain enough energy to escape the channel and get trapped on the surface. These electrons form so called virtual gate [14] and deplete channel carriers in the drain extrinsic region.

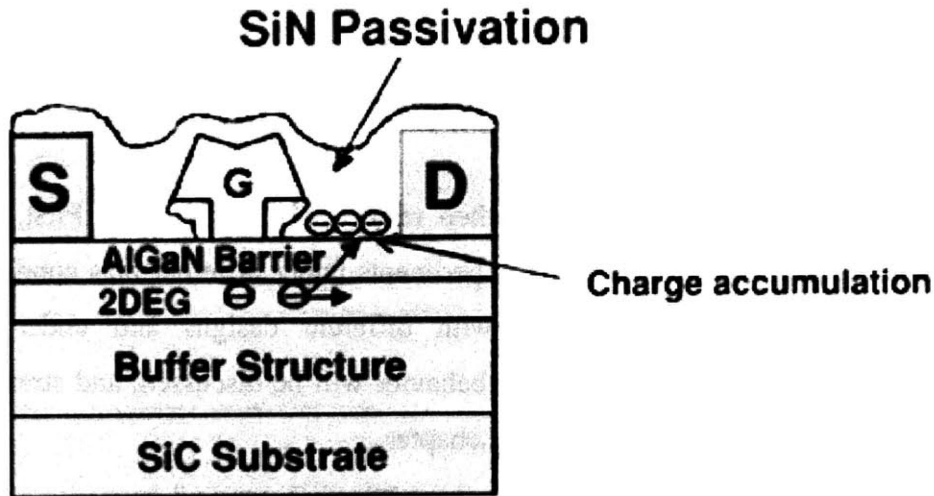

Figure 1-3. Degradation mechanism in AlGaN/GaN HEMT under high stress condition [17].

However, the detailed mechanisms behind the device failure are not still well known, and few solutions to this problem have been proposed to date. In most of the papers that suggests hot electrons as the main cause of the degradation, little experimental or theoretical proof has yet been provided. In fact, experiments that contradict to hot-electron related mechanisms will be presented in this thesis.

1.4. Project Goals and Thesis Outline

In this research, we have carried out systematic studies to understand the precise mechanisms of device degradation. Examining degradation phenomena in different stressing regimes on different kinds of devices, we especially focus on fundamental physics underlying device failure. Upon identifying the responsible physical mechanisms, we will then attempt to identify process and device design changes to improve the electrical reliability of GaN HEMTs.

This thesis will be organized as following: In chapter 2, GaN HEMT devices that are used in this study will be briefly described first. A reliability test chip that has been designed and

fabricated will be also introduced. Then, the experimental setup will be summarized, and a characterization suite that measures device parameters of the device under test will be presented. Finally, the stress test methodology will be explained.

In chapter 3, degradation experiments and their results will be discussed. First, it will be shown how devices degrade. Then stress experiments under different bias conditions will be presented. Experiments on devices with different designs and under different environment will be also studied. Trapping behavior will be discussed, and stress tests on other test structure will be also shown in this chapter.

Finally, a hypothesis to explain the degradation mechanisms will be proposed and supporting experiments will be discussed in chapter 4. The conclusions of this research will be presented in chapter 5.

Chapter 2. Experimental

2.1. Introduction

This chapter begins with the description of the GaN HEMTs that are used in this study. A reliability test chip that has been designed in the course of this research will be described. Finally, a device characterization suite and the different stress test schemes used in this work will be discussed.

2.2. Devices

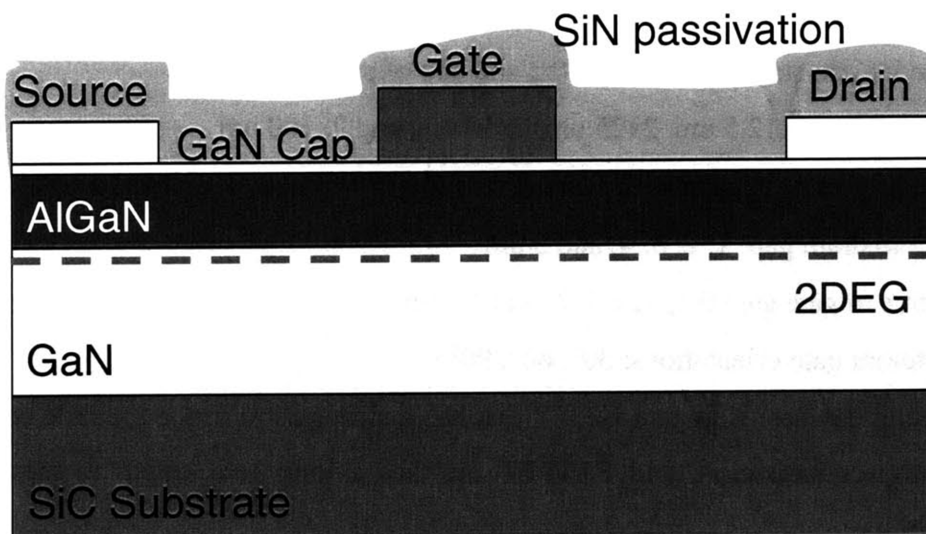

Figure 2-1. Schematic cross section of GaN HEMT.

Figure 2-1 shows a schematic cross section of the GaN HEMTs used in this study. These devices are fabricated by TriQuint Semiconductor and BAE Systems. The heterostructure is grown on a SiC substrate. GaN buffer and active channel layer is followed by AlGaN barrier layer below which 2-D electron gas is formed. Between the gate and the AlGaN layer, there is a thin GaN cap layer. Source and drain ohmic contacts are formed by annealing, and the surface is passivated by a SiN layer.

Standard devices that are mostly investigated in this study have 0.25 um (TriQuint) / 0.15 um (BAE) gate length and 2x25 um gate width. Source to drain spacing is 4 um. A typical virgin TriQuint device has a current-gain cut-off frequency f_T around 40 GHz, and I_{Dmax} is about 1.2 A/mm. The output power is about 8 W/mm, and PAE is 62 % at 10 GHz when the device is biased at 40 V [7].

2.3. MIT Reliability Test Chip

In order to carry out a systematic study of reliability, a reliability test chip was designed (Figure 2-2). Other than standard devices described in the previous section, HEMTs with different geometries are included in this chip:

- Gate length: standard, 2x, 5x, 10x, and 20x of standard device
- Gate width: 2x12.5 um, 2x25 um, 2x50 um, and 2x100 um
- The number of fingers with 100 um unit finger width: 2, 4, 6, and 10
- Gate to drain gap: 1, 2, 3, 4, and 5 um
- Source to gate gap: 0.5, 1, 1.5, 2, and 2.5 um
- Different gate orientations: 30°, 60°, 90°
- Special devices: side-gate HEMT that has a side-gate to probe the hole current due to impact ionization, and FATFET that has a long gate length to measure Hall mobility

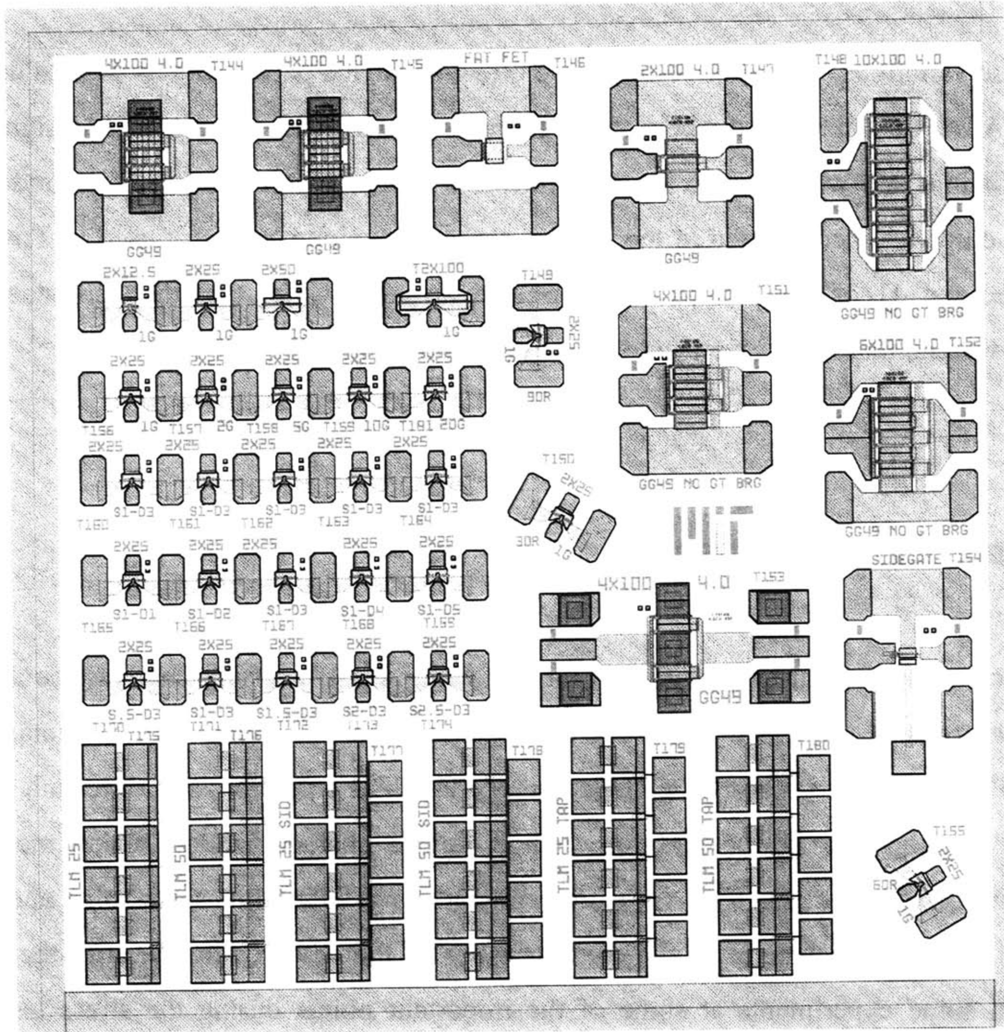

Figure 2-2. MIT reliability test chip.

As study of degradation of Transmission-Line Method (TLM) has revealed important degradation mechanisms of InGaAs and GaAs HEMTs [18, 19], we have also designed different types of TLMs:

- Standard TLMs: W=25 um, 50 um. L = 3, 5, 7, 9, 11 um
- Tapped TLMs: W=25 um, 50 um. A tap is used to monitor the voltage at the midpoint of TLM.
- Sidegate TLMs: W=25 um, 50 um. A side gate to probe the hole current due to impact ionization.

With these variations, we can investigate the effect of device parameters as well as device physics. Also, we can sort out where the degradation takes place, what is the key signature of degradation, and what are the key dependencies (current, voltage, etc) of degradation. This test chip was incorporated in the regular process development mask used in TriQuint and BAE, and 41 of these chips are fabricated in every wafer that they produce. For different wafers, these chips were cut out and sent to MIT for this study.

2.4. Electrical Experiments

The basic concept of our experiments is the following: First, we fully characterize a fresh device before stressing it. This first characterization is benign enough not to damage the device. Then, we start stressing the device in a certain bias condition, and once in a while, we stop stressing the device and run a short device characterization which measures important figures of merit. This measurement runs in a short time (< 1 min) and only produces very minor changes of the characteristics of the device. Finally, after the stress test or in some experiments at some of the important points during the stress test, full characterization is again run and compared to the characteristics before the stress.

For this, we have developed a benign device characterization suite. The characterization suite is an automated program that measures several figures of merit of the device under test in different manners. The key figures of merit include I_{Dmax}, R_S, R_D, and V_T. It also measures full I-V characteristics at selected times along the stress experiment (e.g. at the beginning and at the end of the experiment).

2.4.1. Experimental Setup

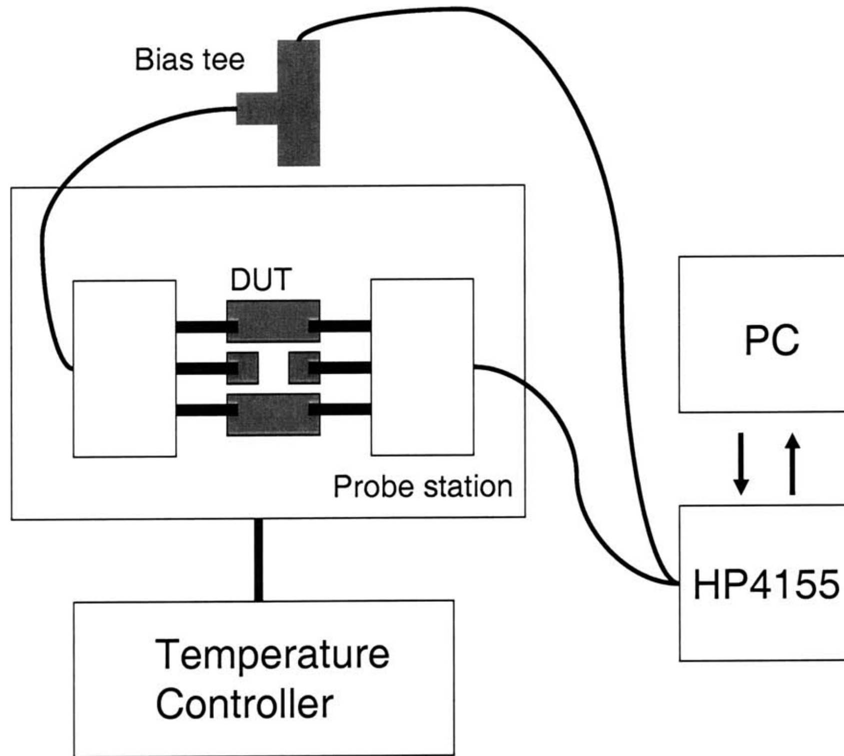

Figure 2-3. A schematic of the whole experimental setup.

A schematic diagram of our experimental setup is shown in Figure 2-3. It consists of a HP4155 semiconductor parameter analyzer with a HP41501A high power expander unit and a Cascade Microtech probe station. The chuck on the probe station is connected to temperature controller unit that regulates its temperature from -60°C to 200°C. An enclosed gas chamber enables performing measurements with the device under nitrogen and under controlled illumination conditions. As the devices under study are designed to operate at high power and high frequency, we use Picoprobe GSG 125 um microwave probes with a bias tee installed in the gate side in order to avoid any oscillations that may occur during the measurements. The HP4155 is controlled by a Windows OS PC through a GPIB connection. Some experiments were performed in air or under the microscope light illumination.

The characterization suite and the stress experiments were written in Agilent VEE 7.0, which runs the whole system. Stress experiments are programmed in a way that users can design new experiments easily without changing the structure of the whole program. For example, several drop-down options, such as step-stress, stress-recovery, constant I_D stress, and constant V_D stress, are provided for user-friendliness and efficient experiment design as shown in Figure 2-4.

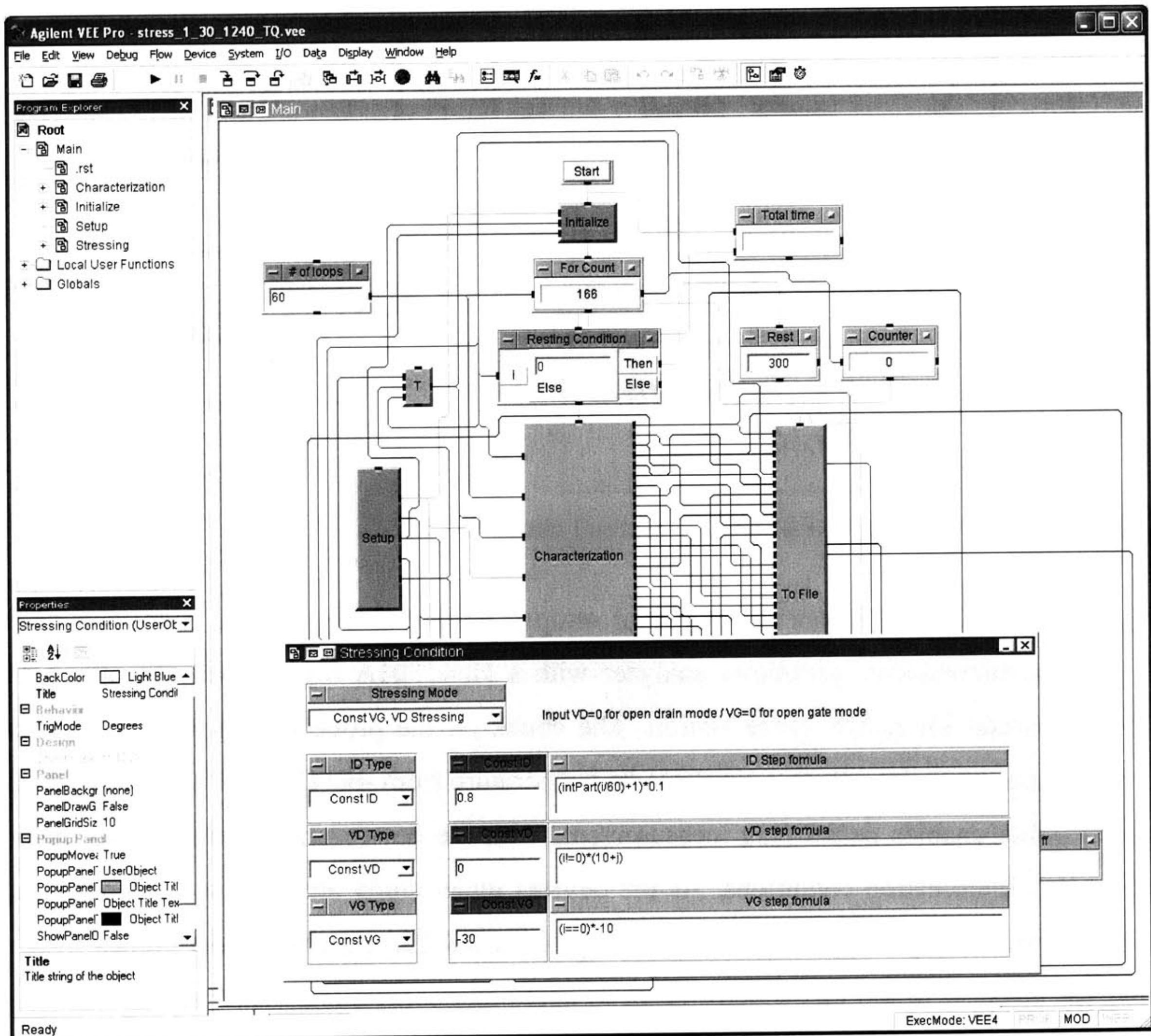

Figure 2-4. Graphical user interface of a stress experiment program. A window to select the type of stress experiment and to input stress bias conditions is shown.

2.4.2. Characterization Suite

The characterization suite commands the HP4155 to measure figures of merit and full I-V curves. Short device characterization is done every 1 or 2 minutes in the middle of a stress experiment to keep track of device parameters. It typically takes less than 1 minute to extract all the desired figures of merit. Most measurement techniques for extracting device parameters follow the previous work on reliability of GaAs PHEMT [19], and the definitions of all figures of merit are briefly summarized in Table 2-1.

Parameter	Definition
I_{Dmax}	Drain current at V_{DS}=5 V and V_{GS}=2 V (TriQuint) / 1 V (BAE)
R_S	Source resistance measured with I_G=20 mA/mm
R_D	Drain resistance measured with I_G=20 mA/mm
R_{TOT}	Total resistance between drain and source with gate floating.
R_{CH}	Channel resistance. $R_{TOT}-R_S-R_D$
V_T	$V_{GS}-0.5V_{DS}$ when I_D=1 mA/mm at V_{DS}=0.1 V
SS	Sub-threshold slope at V_{DS}=0.1 V and I_D=1 mA/mm
DIBL	$V_T\vert_{VDS=0.1\ V} - V_T\vert_{VDS=5\ V}$
g_{mpk}	Peak transconductance dI_D/dV_{GS} at V_{DS}=5 V
V_{Gpk}	Gate voltage where g_m is maximum at V_{DS}=5 V
g_{mpk2}	Peak transconductance dI_D/dV_{GS} at V_{DS}=0.1 V
I_{Dmin}	Minimum drain current in sub-threshold curve at V_{DS}=0.1 V
V_{Gmin}	Gate voltage where I_D is minimum at V_{DS}=0.1 V
I_{GVT}	Gate current at $V_{GS}=V_T$ and V_{DS}=0.1 V
V_{Gon}	Gate voltage where I_D=1 uA/mm
I_{Goff}	Gate current at V_{GS}=-5 V and V_{DS}=0.1 V
I_{Dss}	Drain current at V_{DS}=5 V and V_{GS}=0 V

Table 2-1. Definition of device parameters measured by the characterization suite.

The device characterization must be benign in that it must produce reliable and reproducible measurements without affecting the device under test. For this, the measurement conditions have to be selected carefully, and the effect of FOM extraction have been studied in detail. In our work, extensive repeated characterizations have been run on virgin devices to check if the characterization suite really does not produce any damage to the device.

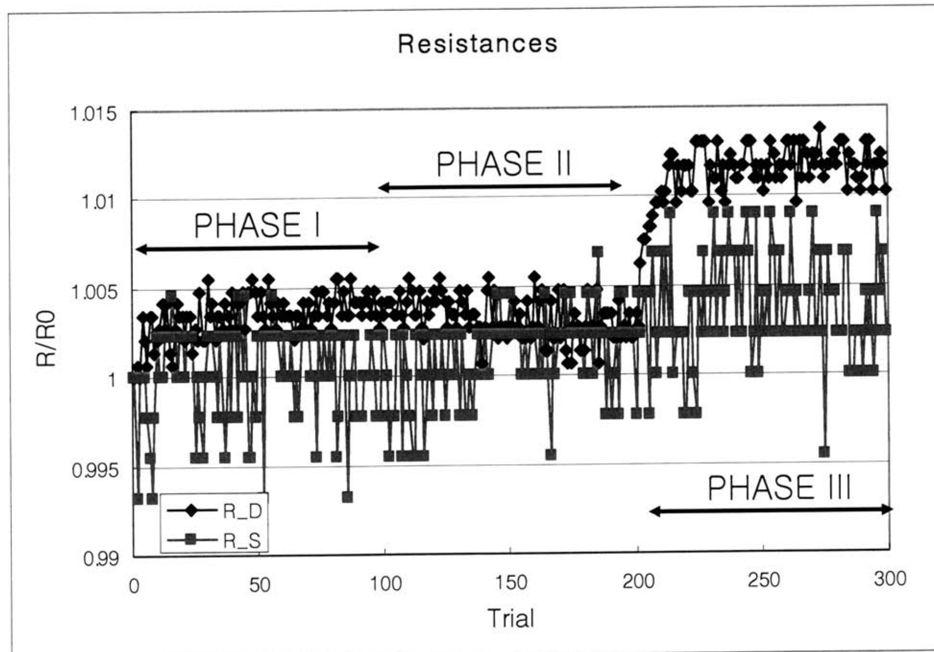

Figure 2-5. Change in normalized drain and source resistance after 300 device characterizations. In phase I, basic figures of merit are extracted. In phase II, full output characteristics are also measured. In phase III, full transfer and sub-threshold characteristics are measured on top of the basic characterization and output characteristics measurement.

Figure 2-5 describes such a typical experiment. In phase I, basic figures of merit including I_{Dmax}, R_S, R_D, V_T, and I_{Goff} are extracted 100 times in a row. In phase II, on top of this basic parameter extraction, output characteristics are measured. Finally, in phase III, transfer characteristics are also measured in addition to the measurements done in phase II. As shown in Figure 2-5, the characterization suite only produced less than 1 % changes in R_S and R_D in phase I, and less than 2 % even if the device is fully characterized 300 times in a row (this includes extraction of full I-V characteristics, Phase II & III). The changes in the most important device parameters are summarized in Table 2-2. Although not perfect, the characterization suite produces only minor changes in the device parameters, compared to typical changes during the stress test, which is usually in excess of 20 %. Also, from Figure 2-5, we can see that the measurements obtained from the characterization suite are reproducible and reliable.

	I_{Dmax}	V_T	R_S	R_D
Basic (100 times)	-0.3 %	+6 mV	+0.3 %	+0.4 %
Basic + Output (100 times)	-0.8 %	+4 mV	0	-0.1 %
Basic + Output + Transfer (100 times)	-0.9 %	+2 mV	+0.2 %	+0.9 %
Total (300 times)	-2 %	+12 mV	+0.5 %	+1.2 %

Table 2-2. Changes in important figures of merit after 300 runs of the device characterization suite.

In addition, this characterization suite can be easily adjustable to new device process designs, so that a new device with totally different characteristics can be easily measured by simply changing configuration parameters such as the bias point to extract I_{Dmax}.

2.5. Stress Test Methodology

In this thesis, we have focused on DC reliability studies. Rather than a simple stress test in which the stressing conditions are kept constant during the test, several electrical stress schemes have been investigated in the course of this research. These are graphically described in Figure 2-6.

Stress-recovery type of experiments in which stress is followed by a recovery period is performed to study how a device degrades as well as how it recovers from the degradation. In this type of experiment, a specific stress bias is applied in the stress phase, and this stress is removed in the recovery phase (Figure 2-6 left) while the device is characterized.

As discussed in previous works [18, 19], a step-stress scheme has been utilized to maximize productivity. In this type of experiment, the strength of the stress parameter such as voltage or current is stepped up from a smaller value to larger values in order to see the effect of that stress parameter over a wide range of values in a single device (Figure 2-6 middle). From this type of experiment, we obtain great insight into physical mechanisms. Finally, step-stress-recovery experiments have also been carried out (Figure 2-6 right).

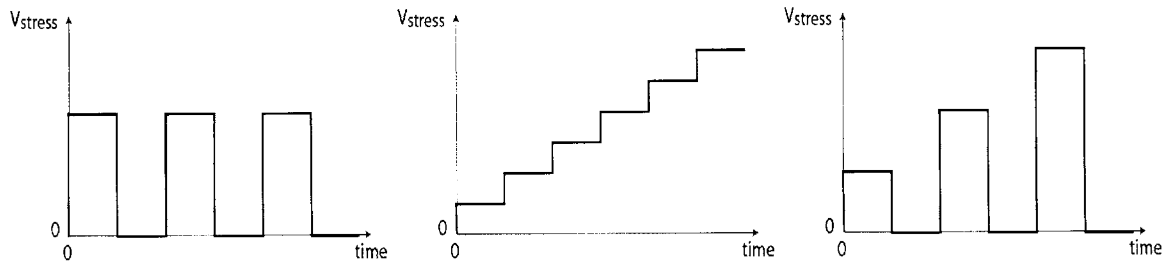

Figure 2-6. Conceptual stress schemes: (from left to right) stress-recovery, step-stress, and step-stress-recovery.

Regarding the period of stress, we have mostly focused on short-term degradation which happens within a few hours. We emphasize this short-term degradation because GaN-based HEMTs are known to degrade in relatively short period of time. In fact, we have seen significant degradation even within an hour of stress. However, medium-term stress experiments (on the order of one or two days) have also been performed in order to investigate phenomena which take place in a relatively longer period of time.

Different stress bias conditions were studied: *high power state* (high V_{DS}, high I_D), *ON-state* (low V_{DS}, high I_D), and *OFF-state* (high V_{DS}, low I_D). In high power condition, we tried to simulate the RF power amplifying operation in a more severe way. By investigating both ends of the load line, ON state and OFF state, we can study where the most stressful point is during a real RF operation. In addition, we have focused on the $V_{DS}=0$ *state* in which negative gate voltage is applied. In this condition, we can stress the both sides of the device simultaneously with a low current but a high voltage. These conditions are shown in Figure 2-7 relative to the position of the RF power load line that is typically followed in RF power applications.

Unless specified, all of our experiments are done at room temperature, with the device inside a dark chamber with nitrogen gas injected into it.

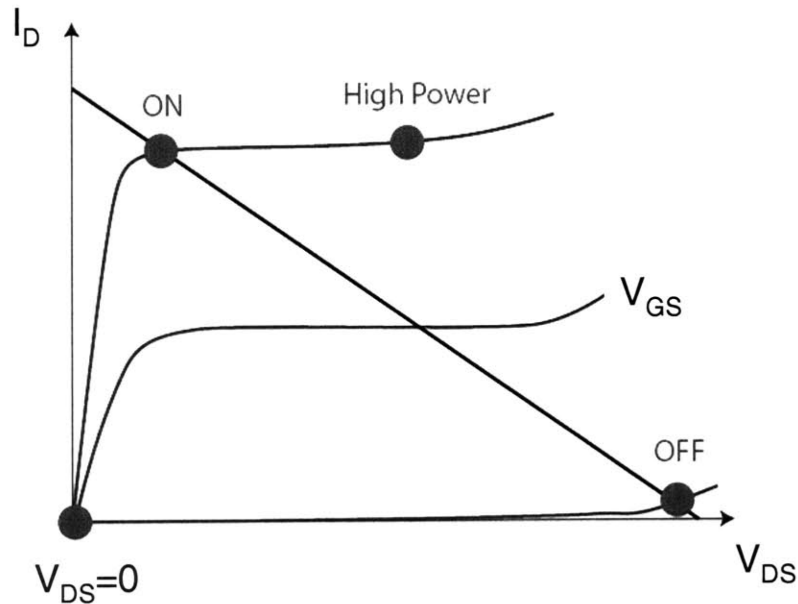

Figure 2-7. Stress bias points: High Power, ON state, OFF state, and V_{DS}=0 conditions.

2.6. Summary

In this chapter, we have introduced the GaN HEMT devices, the reliability test chip, and the electrical experimental setup used in this thesis. In order to study degradation phenomena of GaN HEMTs, we have developed a characterization suite. Although slight changes are produced by a number of repeated device characterizations, we have shown that the characterization suite performs reliable and benign measurements of GaN HEMTs. Finally, we have introduced stress test methodologies that were used in this study. In the next chapter, results of degradation experiments will be shown, and basic degradation phenomena will be discussed.

Chapter 3. Degradation Experiments

In the last chapter, we have introduced the experimental setup and the characterization and stress protocols for studying electrical reliability of GaN HEMTs. In this chapter, we describe several degradation experiments. Experiments performed in various stress bias conditions on HEMTs and TLMs are presented, and their results are discussed. Also, we discuss the effects of device geometries and environment. Based on the results, electron trapping behavior is investigated as a basic degradation mechanism.

3.1. Overall Degradation Phenomena

Figure 3-1 and Figure 3-2 show the overall result of a typical stress test. This is a high power step-stress experiment that is performed on a standard type device. In this experiment, the drain bias is stepped from 5 V up to 30 V. Stress current is set at 800 mA/mm throughout the experiment by adjusting the gate bias. As it can be seen in Figure 3-1, source resistance R_S increases little, whereas drain resistance R_D shows larger change as the device is stressed. The maximum drain current I_{Dmax} decreases. As shown in Figure 3-2, the threshold voltage first shifts positive at lower stress voltage, but it then shifts negative for V_{DS}>20 V.

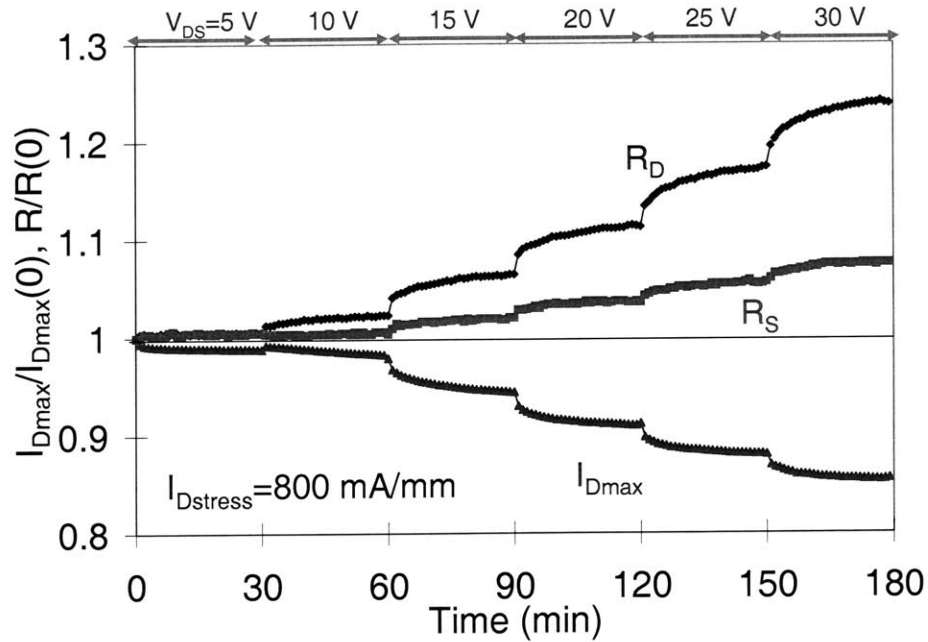

Figure 3-1. Change in normalized I_{Dmax}, R_D, and R_S in step-stress experiment in the high power state (V_{DS}=5~30 V in 5 V steps, I_D=800 mA/mm, 30 minutes per step).

Figure 3-3 shows the change in the output characteristics before and after the stress test. As it can be seen, drain current significantly decreases after the stress. As it can be seen in Figure 3-4 and Figure 3-5, the sub-threshold slope remains relatively constant, while the maximum transconductance decreases after the stress test. For the rest of this study, we will mostly focus on the changes in I_{Dmax}, R_S and R_D.

It is interesting to note in Figure 3-1 that degradation is negligible at low voltage (ON-state) in spite of the large current. It then seems that voltage is a more important factor for device degradation than current. This result motivated us to do similar experiments with much lower current, in the OFF state. This will be discussed in the following sections.

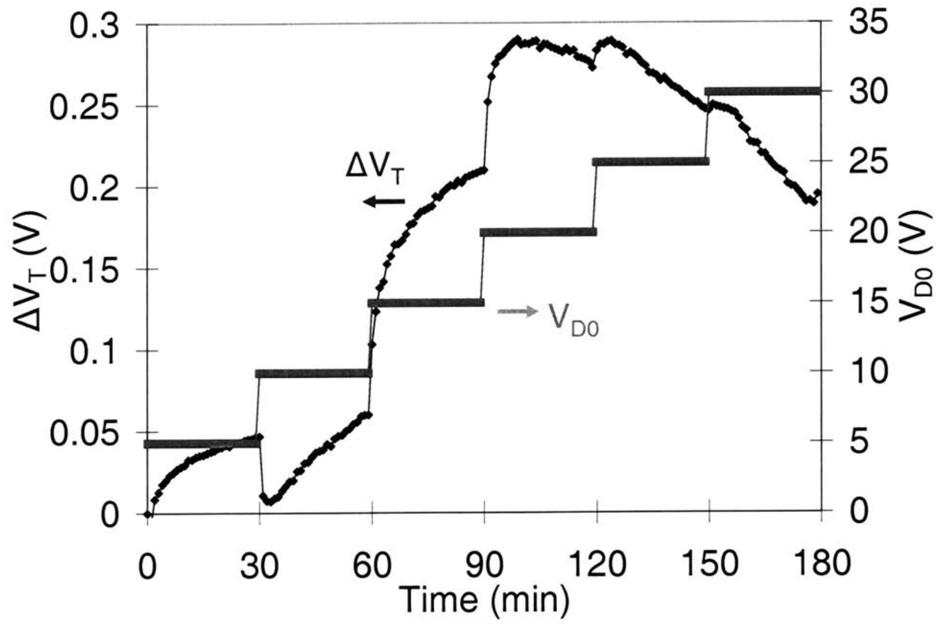

Figure 3-2. Threshold voltage change in the same experiment as Figure 3-1.

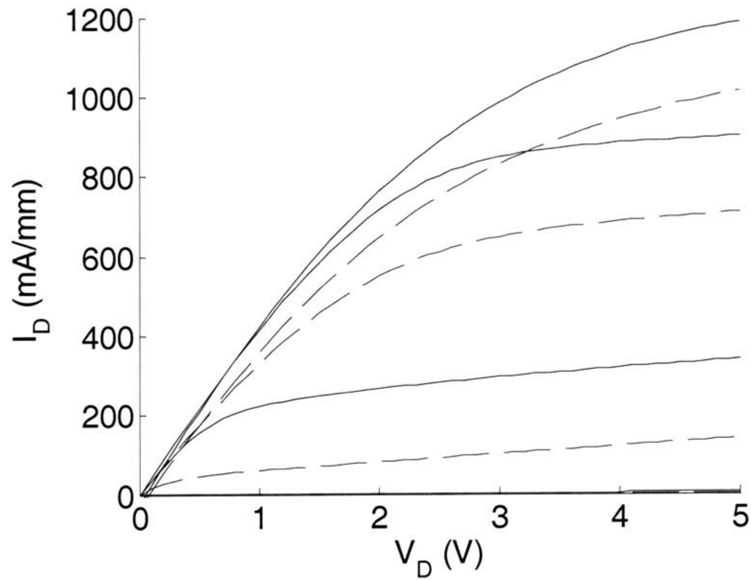

Figure 3-3. Output characteristics before (solid) and after (dashed) the same stress test as in Figure 3-1. V_{GS}=-4~2 V (2 V step).

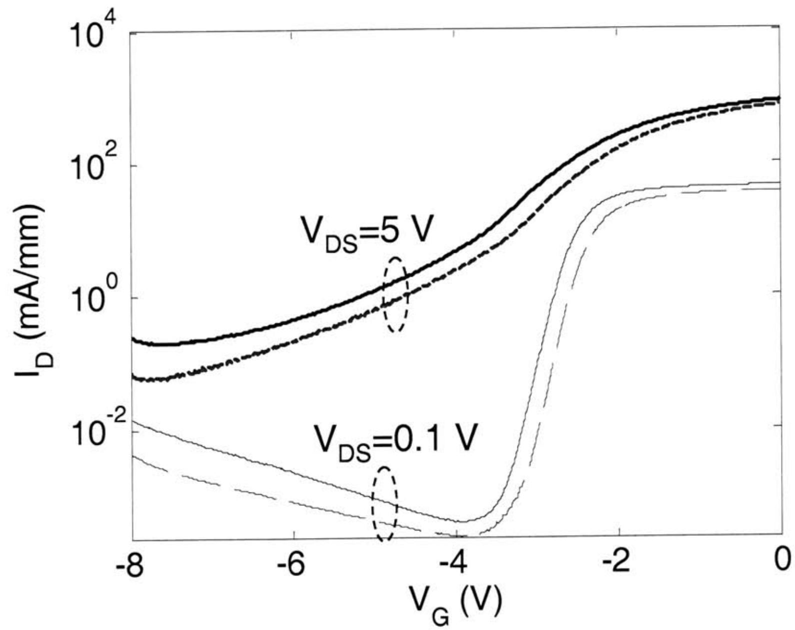

Figure 3-4. Change in sub-threshold characteristics before (solid) and after (dashed) the same experiment as Figure 3-1.

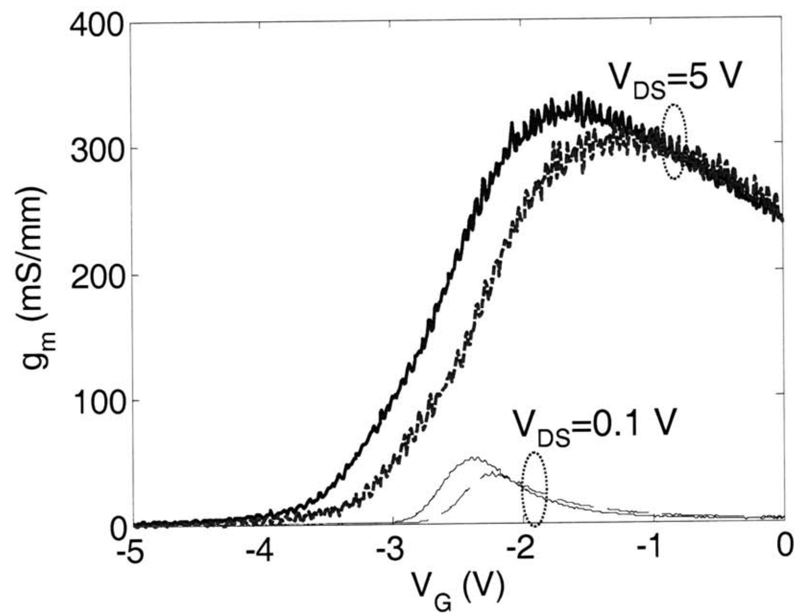

Figure 3-5. Change in g_m before (solid) and after (dashed) the same experiment as Figure 3-1.

3.2. OFF-state Step-stress

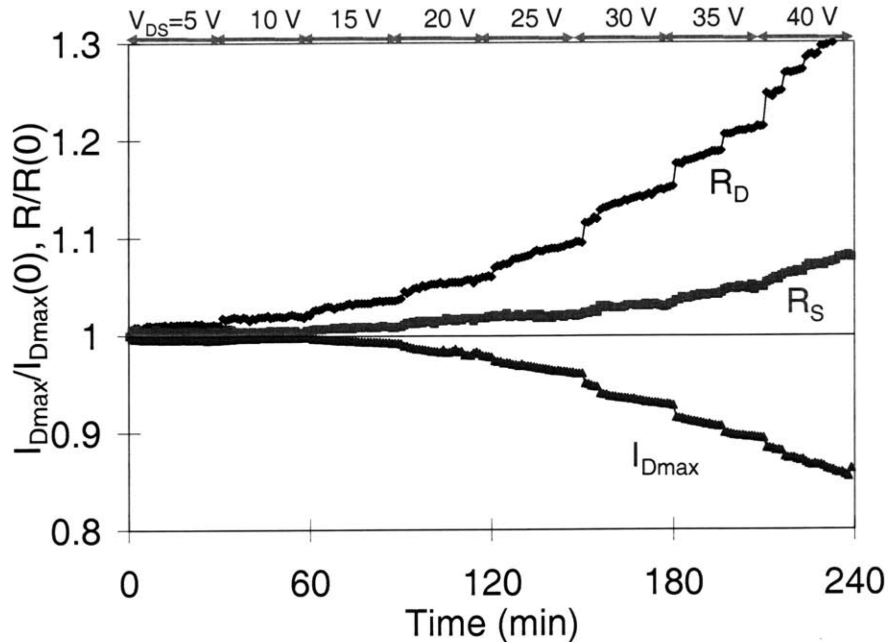

Figure 3-6. Change in normalized I_{Dmax}, R_D, and R_S in step-stress experiment in the OFF state (V_{DS}=5~40 V in 5 V steps, I_D=25 mA/mm, 30 minutes per step).

Figure 3-6 shows the result of an OFF state step-stress experiment. In this experiment, the stress current is 25 mA/mm, which is about 3 % of that in the high power stress experiment of Figure 3-1. We also find that in the OFF state, the source resistance shows little degradation. However, although the stress current is much smaller, the degradation in R_D and I_{Dmax} is comparable to that in the high power state (see Figure 3-1). This result confirms that voltage, or electric field, is the main driver for device degradation, and current is an accelerating factor [9]. However, it is not clear whether the effect of current is supplying hot electrons to the system or increasing the junction temperature. Our results are obviously inconsistent with hot-electron based mechanisms in that degradation in OFF state is comparable to that in high power state in spite of much fewer hot electrons in the channel.

3.3. V_{DS}=0 Condition

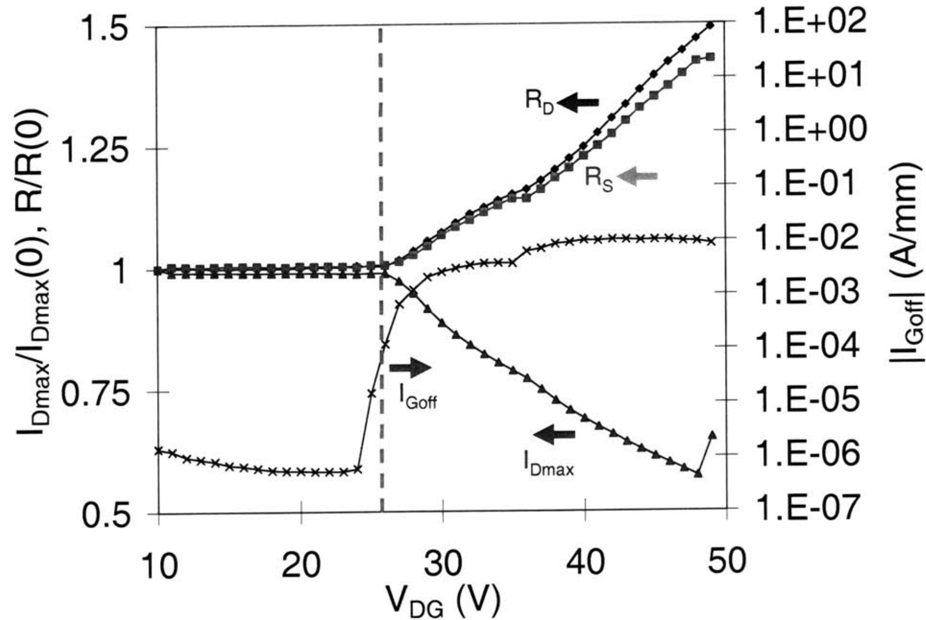

Figure 3-7. Change in normalized I_{Dmax}, R_D, R_S, and I_{Goff} as a function of stress voltage in a step-stress experiment in V_{DS}=0 state (V_{DG}=10~50 V in 1 V steps).

Stressing a device in V_{DS}=0 condition is interesting in that no current flows through the channel, and both sides of the device can be stressed at the same time. Figure 3-7 summarizes the results of a V_{DS}=0 step-stress experiment. In this experiment, V_{GS} is stepped from -10 V to -50 V. The voltage step size is -1 V, and the device is stressed for one minute at each step. As expected, both R_S and R_D degrade by about the same amount. Interestingly, we have seen no I_{Dmax} and series resistance degradation up to around 25 V, and degradation sharply starts beyond that voltage. Because of this, we define this sudden onset of degradation as taking place at a "critical voltage". Interestingly, I_{Goff}, which is defined as gate current at V_{DS}=0.1 V and V_{GS}=-5 V, also shows a sudden very large increase at around the critical voltage. This simultaneous degradation in I_D and I_G is generally seen in all our step-stress experiments.

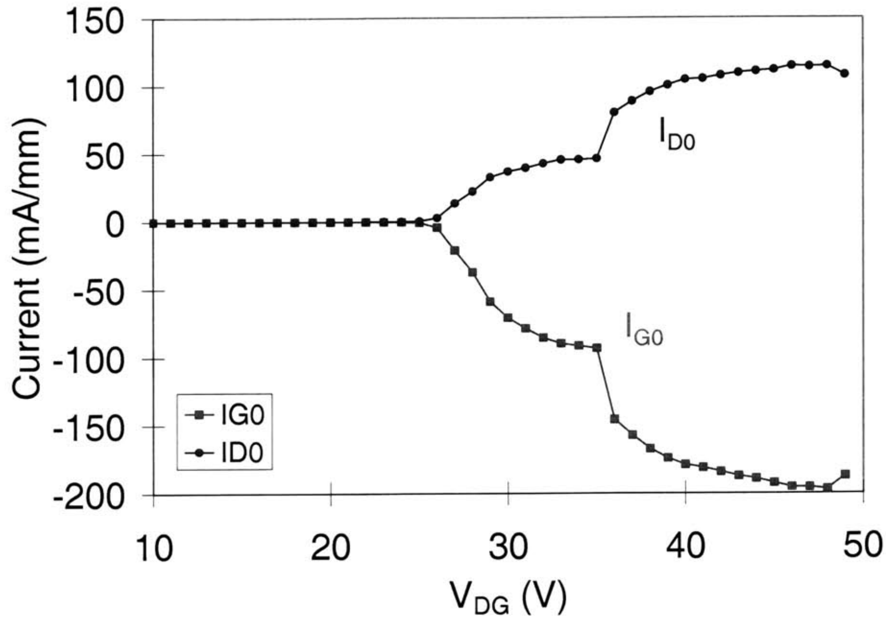

Figure 3-8. Stress current of the experiment in Figure 3-7.

As shown in Figure 3-8, the drain current at -27 V, where degradation becomes apparent, is about 13 mA/mm, and it is 104 mA/mm at -40 V in this particular experiment. This might suggest that degradation is driven by the relatively large current which can then produce hot electrons. However, two observations are contradictory to that argument: first, degradation does not suddenly increase around V_{DG}=35 V where stress currents again suddenly increase; second, degradation keeps increasing after 40 V without any signature of saturation, while the stress currents almost saturate.

Moreover, it has been found that degradation of I_{Dmax} and series resistances is not correlated to the stress current in similar V_{DS}=0 stress experiments carried out in other devices. In fact, in a V_{DS}=0 experiment shown in Figure 3-9, very large degradation (23 % of I_{Dmax} reduction at -27 V) is introduced in spite of negligible drain current of less than 0.1 mA/mm, which is three orders of magnitude less than the stress current in the experiment of Figure 3-7. Comparing this number to the experiment in Figure 3-7, we can see that the same amount of degradation can happen regardless of the stress current. This result again

3.4.1. Effect of Environment

In order to see the effect of atmosphere, we have performed a $V_{DS}=0$ stress-recovery experiment in air and compared the result with the experiment performed in nitrogen environment. As shown in Figure 3-10, we have found that degradation is the same in air as in nitrogen environment. This result is different from the GaAs PHEMT case, in which degradation is much more pronounced in air [19] than in N_2. This is consistent with a degradation mechanism for the GaN HEMT that is not of a surface type although it is also possible that these devices have a much more impermeable SiN passivation layer that protects the device from the environment in a much more effective way than the GaAs PHEMTs that we have studied [19].

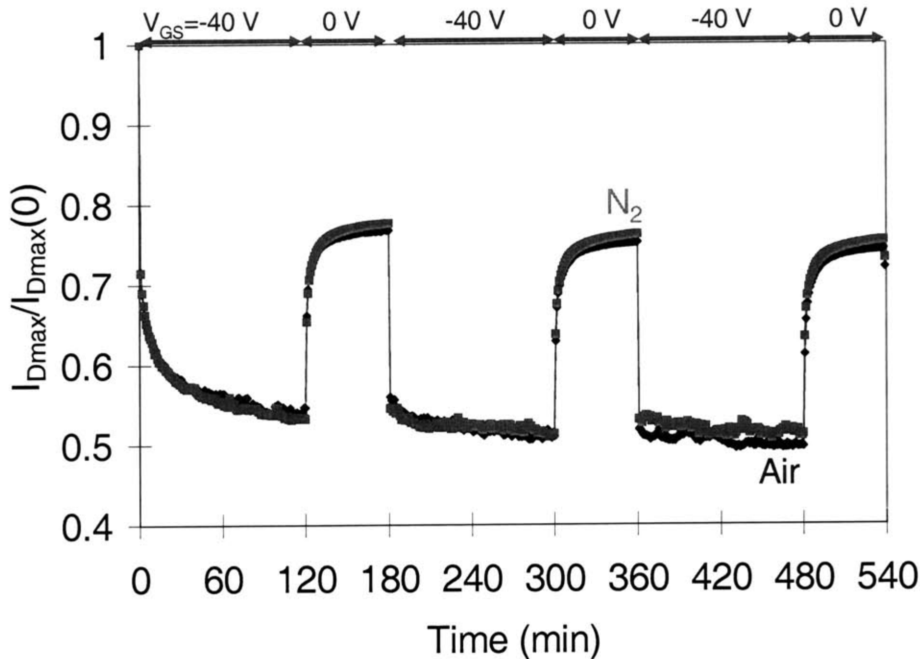

Figure 3-10. Change in normalized I_{Dmax} in $V_{DS}=0$ stress-recovery experiment with and without nitrogen gas. $V_{GS}=-40$ V is applied during the stress period of 120 minutes.

3.4.1. Effect of Environment

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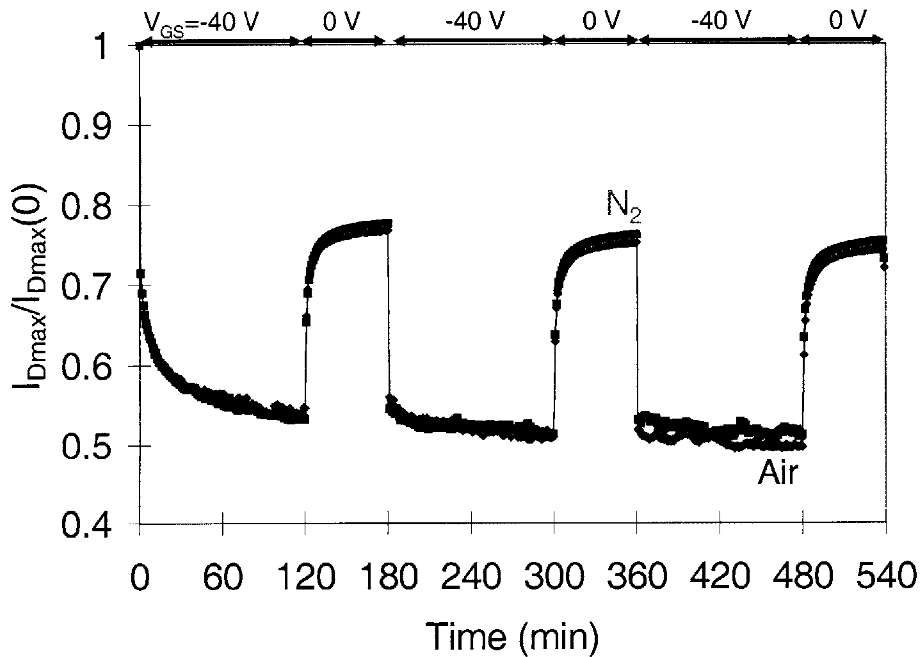

Figure 3-10. Change in normalized I_{Dmax} in $V_{DS}=0$ stress-recovery experiment with and without nitrogen gas. $V_{GS}=-40$ V is applied during the stress period of 120 minutes.

3.4.2. Degradation of MISFET

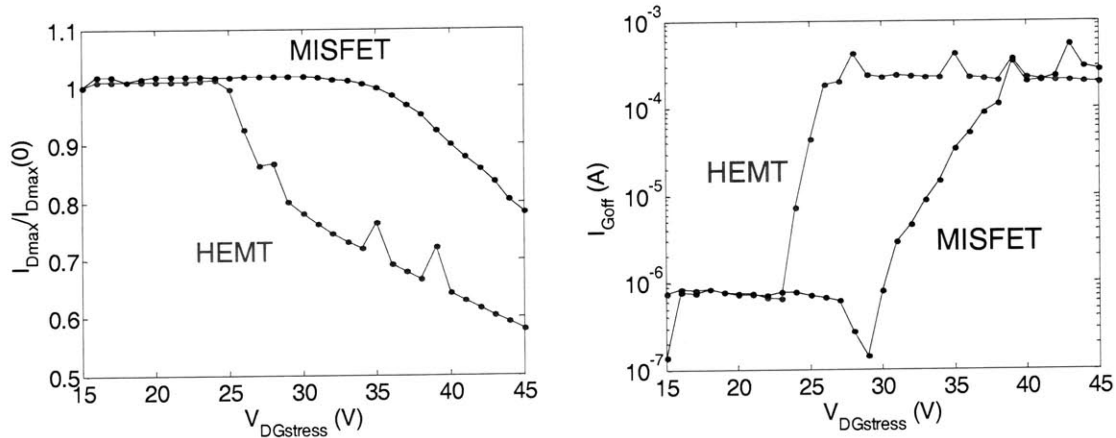

Figure 3-11. Typical I_{Dmax} (left) and I_{Goff} (right) degradation of MISFET and HEMT in $V_{DS}=0$ step-stress experiments.

We have investigated the degradation of MISFETs and compared it with the degradation of HEMTs. We have measured devices on a wafer that has both normal HEMTs (left half) and MISFETs (right half). The process is identical except that one half of the wafer has SiO_2 insulating layer between gate metal and semiconductor, while the other half does not.

Forty one devices across the wafer are step-stressed at the $V_{DS}=0$ condition. The gate voltage V_{GS} is stepped from -15 V to -45 V, and the drain voltage V_{DS} is fixed at 0 V. The step size is -1 V, and the device is stressed for 30 seconds in each step. After each step, two figures of merits are measured: I_{Dmax} (I_D @ V_{DS}=5 V, V_{GS}=2 V) and I_{Goff} (I_G @ V_{DS}=1 V, V_{GS}=-5 V). Figure 3-11 shows typical I_{Dmax} and I_{Goff} degradation of both types of devices.

As can be seen, the critical voltage for I_{Dmax} degradation of MISFETs is higher by about 10 V than that of HEMTs. Also, the gate leakage current of HEMTs starts to increase at a lower voltage than in the case of MISFETs. In fact, we find that the critical voltage for I_{Dmax} degradation exhibits a strong correlation with the critical voltage for I_{Goff} degradation as shown in Figure 3-12. The average and the standard deviation of the critical voltage for

I_{Dmax} degradation of HEMTs are 25.6 V and 4.1 V, respectively. For MISFETs, the average is 36.3 V and the standard deviation is 5.0 V.

We have also measured the current collapse by applying -10 V voltage pulse to the gate before and after the stress. As shown in Figure 3-13, a device with larger I_{Dmax} degradation shows greater increase of the current collapse, which gives us a clue that degradation is somehow correlated to increase in trap density. This is examined in more detail in section 3.6.

Although MISFETs show better DC reliability, they turn out to be worse in RF power soak measurements [20]. However, it is still not clear if the worse RF degradation results from higher V_{DG} due to more negative threshold voltage of MISFETs. Because these power soak experiments have been done with the same drain bias voltage and drain bias current, V_{GS} of MISFETs are more negative than that of normal HEMTs, resulting in higher V_{DG}. Although we have found that voltage is the main driver for DC degradation, further investigation is needed to sort out other mechanisms in RF stress, if any.

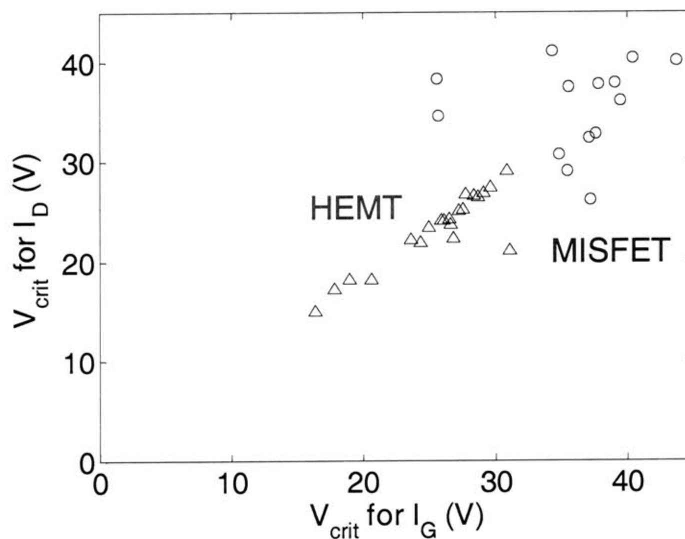

Figure 3-12. The correlation between the critical voltage for I_D degradation and I_G degradation (triangle: HEMT, circle: MISFET)

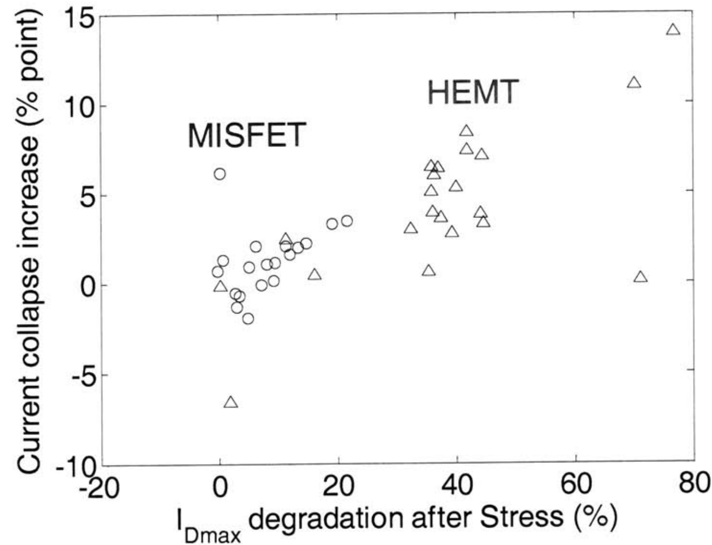

Figure 3-13. The correlation between the current collapse increase and I_{Dmax} degradation (triangle: HEMT, circle: MISFET).

3.4.3. Critical Voltage in other Stress Bias Conditions

In section 3.3, we have observed a critical voltage beyond which a device starts to degrade. In the V_{DS}=0 condition, this voltage is about 20~25 V. However, this critical voltage seems to be too low because devices operate normally at 30 V without degrading that much.
With standard devices (W=2x25 um, L_G=0.25 um, L_{SG}=L_{GD}=2 um), we have compared the critical voltage of degradation under different stress conditions: high power state, OFF state, and V_{DS}=0 state.

Figure 3-14 shows the I_{Dmax} degradation in three different step-stress experiments. The stress bias conditions for these experiments are summarized in Table 3-1. In these experiments, the devices have been stressed for 1 minute in each step, and the step size was 1 V.

	Stress condition
V_{DS}=0 state	V_{GS}=-10~-50 V
OFF state	V_{GS}=-7 V, V_{DS}=10~50 V
High power state	I_D=800 mA/mm, V_{DS}=10~50 V

Table 3-1. Stress bias condition for three different step-stress experiments.

As it can be seen in Figure 3-14, V_{DGcrit} is 25 V for V_{DS}=0 state, 38 V for OFF state, and 35 V for high power state. Here, this critical voltage is defined as the voltage at which a change in the slope of I_{Dmax} evolution curve occurs. In high-power condition, this definition is somehow ambiguous as the device degrades even at lower voltage. However, the part of decrease in I_{Dmax} before V_{DG} < 30 V is due to large positive shift of threshold voltage as shown in Figure 3-15, and this positive shift is only observed in the high-power state stress. As g_m is about 128 mS/mm around V_{DS}=5 V and V_{GS}=2 V where we measure I_{Dmax}, threshold voltage shift of +0.5 V results in 64 mA/mm reduction of I_{Dmax}. This change is responsible for about half of the change in I_{Dmax} in V_{DG}<30 V. At around V_{DG}=35 V, there is also a change in the slope of I_{Dmax} evolution although the threshold voltage is relatively constant beyond that point.

Figure 3-16 shows the time evolution of the gate leakage current. The critical voltages for sudden gate leakage current increase are 25, 38, and 36 V for V_{DS}=0 state, OFF state, and high power state, respectively, which are consistent with the critical voltage for I_{Dmax} degradation mentioned above. This critical voltage for I_{Goff} degradation is defined as the voltage at which there is a abrupt change in I_{Goff}. This large increase of gate leakage current turned out to be unrecoverable, and the correlation between the critical voltage for I_D and I_G degradation suggests a common origin. Although a different mechanisms for I_D degradation may seem to exist in high power state, this abrupt gate leakage degradation around V_{DG}=36 V justifies our previous definition of the critical voltage for I_D degradation in high power state. We can see that the critical voltage for degradation in the normal operating configuration, OFF state and high power state, is about 10~15 V larger than that in V_{DS}=0 condition.

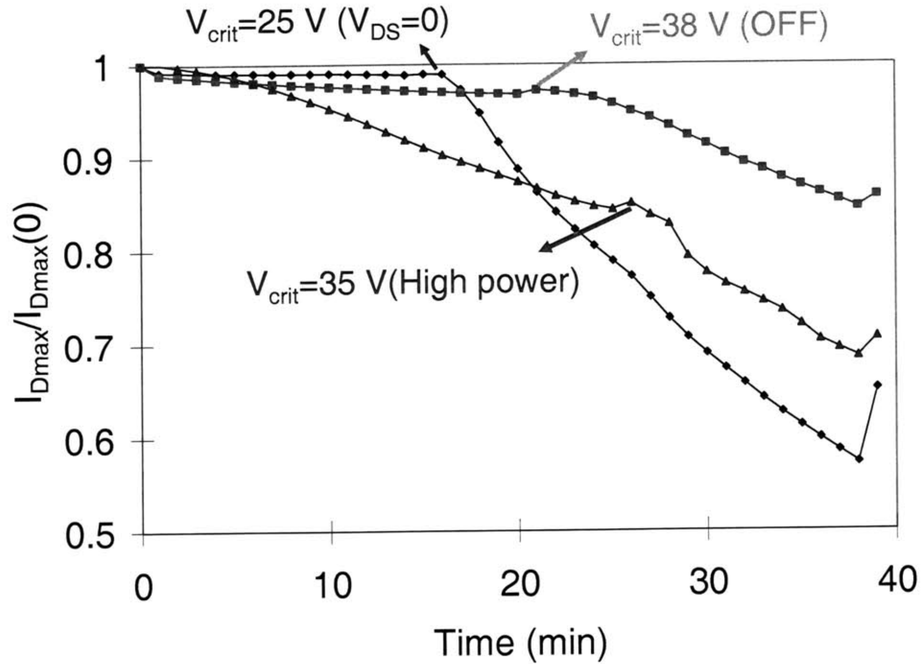

Figure 3-14. Change in I_{Dmax} in step-stress experiments and the critical voltage V_{DGcrit} for I_{Dmax} degradation.

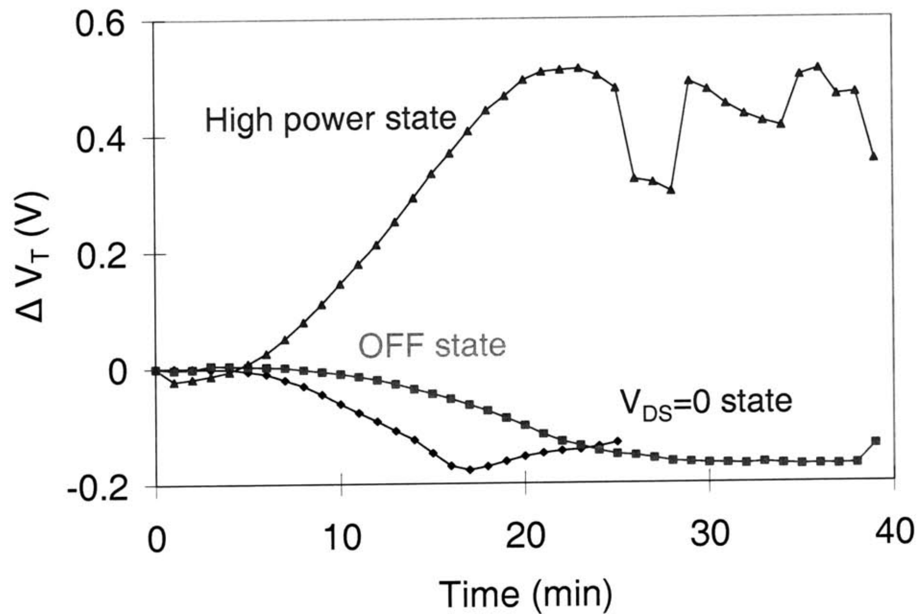

Figure 3-15. Change in V_T in the same experiment in Figure 3-14. In V_{DS}=0 state, threshold voltage is not properly extracted after 25 minutes as the minimum drain current became larger than 1 mA/mm.

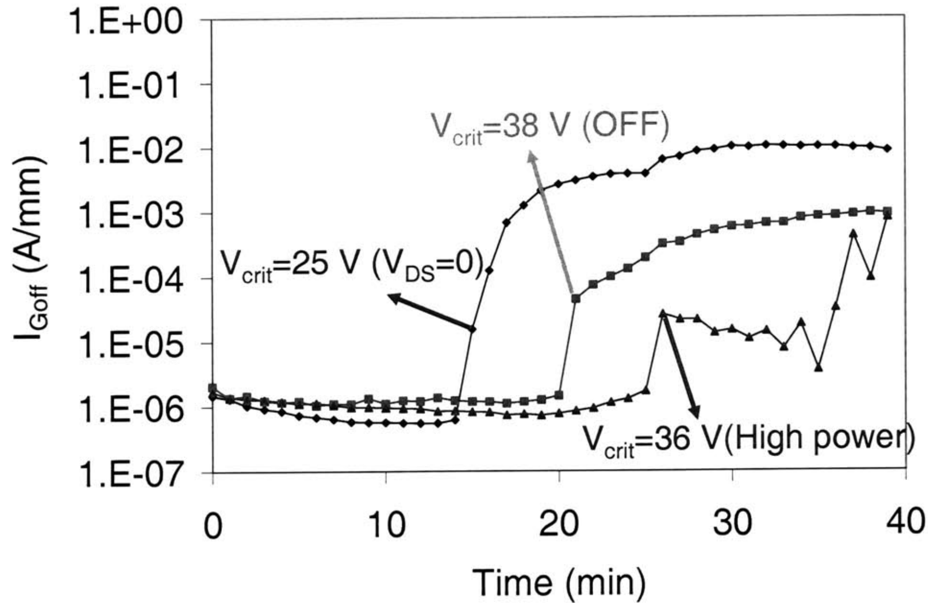

Figure 3-16. Change in gate leakage current I_{Goff} in the same experiment in Figure 3-14 and the critical voltage for I_{Goff} degradation.

3.4.4. The Origin of Gate Leakage Degradation

In section 3.4.3, we have shown that gate leakage current degrades permanently after applying a certain high voltage. In order to confirm which junction is responsible for this degradation, we have done an OFF state step-stress experiment in which we have measured two more figures of merit: I_{Gss1} is the gate current at V_{DS}=5 V and V_{GS}=0 V; I_{Gss2} is the gate current at V_{DS}=-5 V and V_{GS}=-5 V. As V_{GS} for I_{Gss1} and V_{GD} for I_{Gss2} are zero, all the gate current is from the other junction, gate-drain junction for I_{Gss1} and gate-source junction for I_{Gss2}. Therefore, by observing these currents, we can distinguish the origin of the leakage.

As shown in Figure 3-17, V_{DGcrit} for I_{Goff} degradation is 36 V in this experiment. At this voltage, I_{Gss1} starts to degrade simultaneously with I_{Goff}, whereas I_{Gss2} remains relatively unchanged. This result shows that gate leakage degradation in OFF state is originated from

gate to drain junction as expected. Similar result is also observed in high power condition. Not surprisingly, both junctions are found to degrade in $V_{DS}=0$ state.

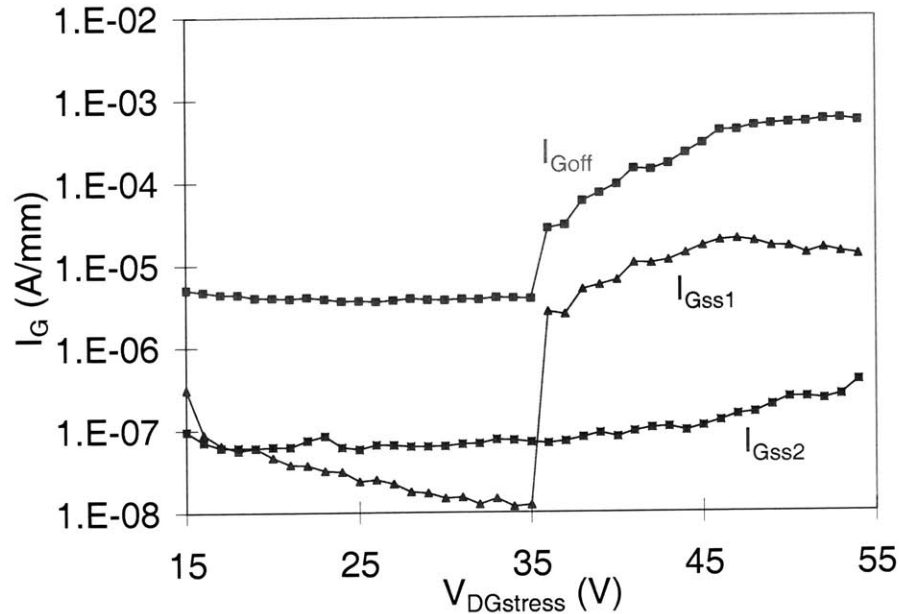

Figure 3-17. Change in I_{Goff}, I_{Gss1}, and I_{Gss2} as a function of stress bias V_{DG} in an OFF state step stress experiment. I_{Gss1} is gate leakage current through gate to drain junction, and I_{Gss2} is gate leakage current through gate to source junction.

3.4.5. Effect of L_{GD}

We have investigated the effect of gate-drain gap (L_{GD}) on device degradation. In order to understand the effect of L_{GD}, we have done OFF state stress experiments with five devices with different L_{GD}=1~5 um, L_{SG}=1 um, and W=2x25 um. These devices have been stressed at V_{DS}=30 V and V_{GS}=-5 V for 50 minutes. The measurement of drain resistance before the stress tests revealed a contact resistance of 0.517 Ω·mm (Figure 3-18). As expected, drain resistance increases with L_{GD}.

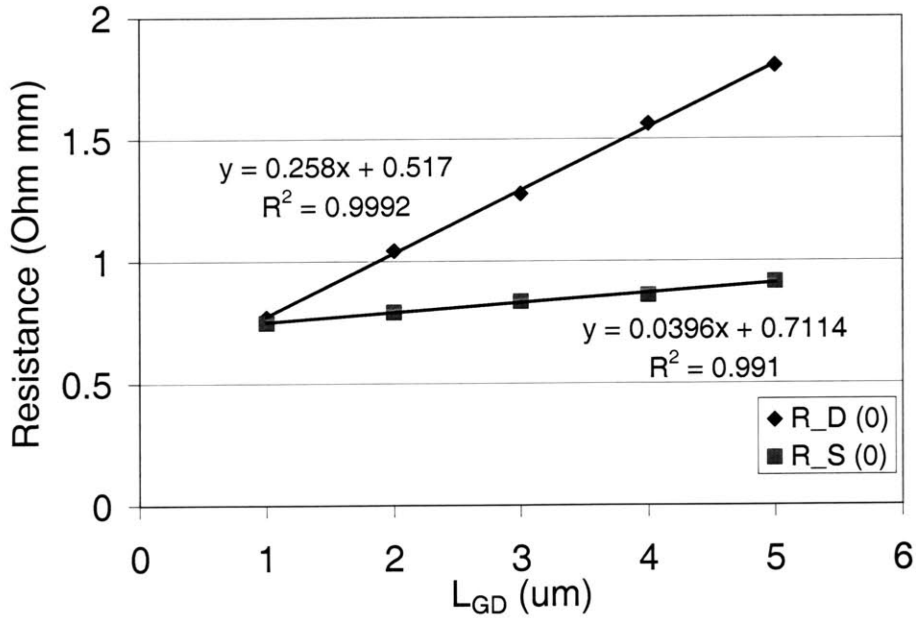

Figure 3-18. L_{GD} dependency of source and drain resistance of fresh devices.

As it can be seen in Figure 3-19, from the change in R_D, it appears that a device with longer L_{GD} tends to degrade less. However, it can be misleading to compare $R_D/R_D(0)$ because the drain resistances at t=0 are different as shown in Figure 3-18. Therefore, we also need to compare the absolute value of the change in R_D.

Figure 3-20 summarizes the absolute change in R_D and R_S as a function of L_{GD}. As it can be seen, ΔR_D seems to be quite independent of L_{GD}. This result confirms that drain resistance degradation is not a surface-type degradation because the same degree of $\Delta R_D/R_D(0)$ is expected if degradation occurs all over the surface between the gate and the drain as in the drain resistance degradation of GaAs PHEMTs [19]. In contrast, the L_{GD} independent increase of R_D suggests that drain resistance degradation takes place at a rather localized point, presumably right next to the gate edge.

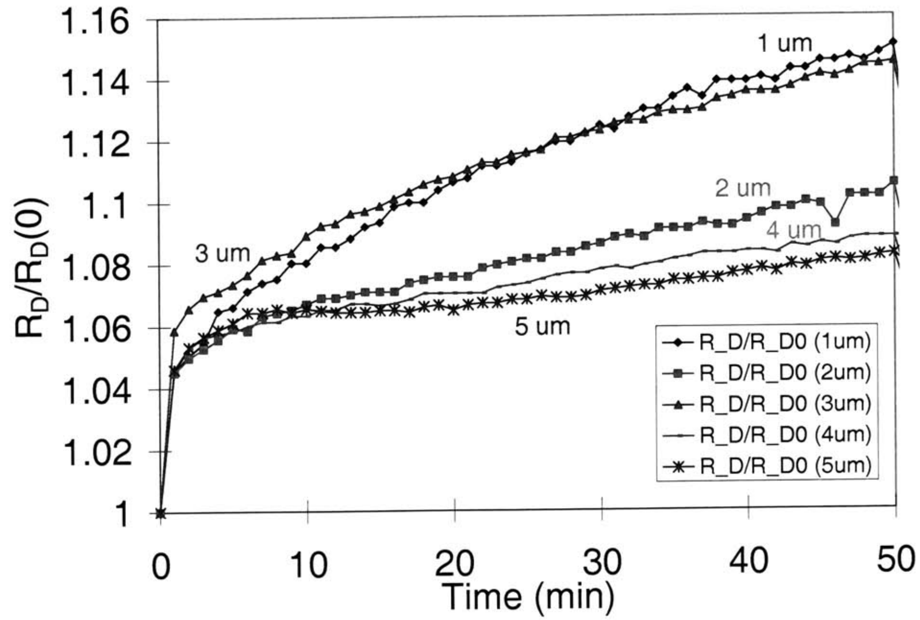

Figure 3-19. Change in normalized R_D in OFF state stress experiments on different L_{GD} devices. Five different devices with different L_{GD}=1~5 um are stressed at V_{DS}=30 V and V_{GS}=-5 V for 50 minutes.

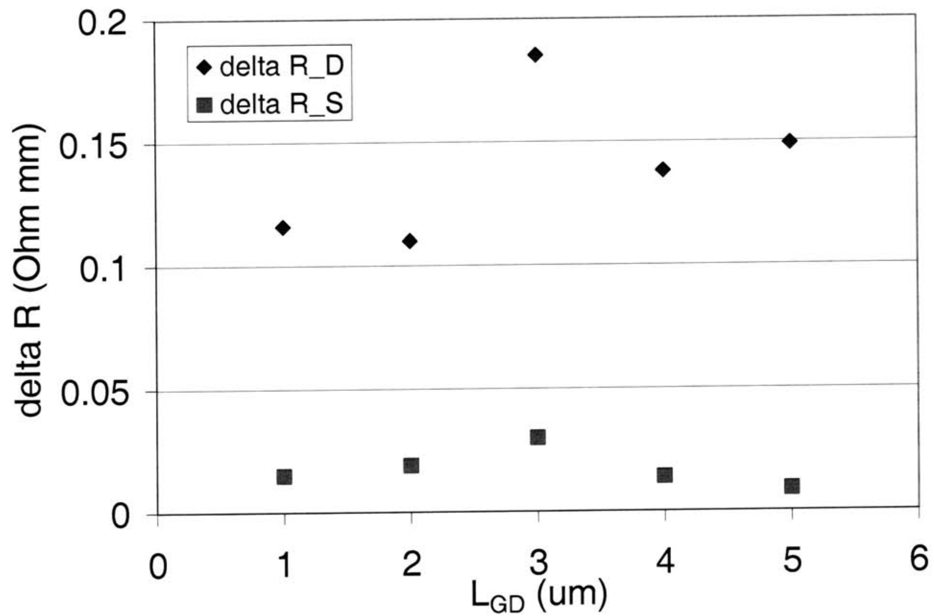

Figure 3-20. Absolute value of change in R_D and R_S as a function of L_{GD} in the same experiment as Figure 3-19.

3.5. Trapping Behavior

In the previous sections, we have shown our results for the degradation phenomena of GaN HEMTs. In this section, we try to figure out the basic mechanism behind device degradation. In particular, as many of the previous studies on reliability of GaN HEMTs have reported that electron trapping is one of the main reasons of device degradations [11, 13, 17], we also investigate the trapping behavior as a device degrades.

3.5.1. Off-state Stress-recovery

In our degradation experiments, we have seen that GaN HEMTs degrade in a relatively short time: I_{Dmax} decreases, R_D increases, and gate leakage current increases after a bias stress. In order to clarify why these parameters change, we have carried out OFF state stress-recovery experiments such as the one summarized in Figure 3-21. In this experiment, a 30 V drain bias is applied while the gate voltage is set to maintain a drain current of 20 mA/mm. This electrical stress is applied for 30 minutes. After the stress period, all stress biases are removed for another 30 minutes while the device continues to be characterized. This one hour cycle is repeated three times.

In the stress phase, as seen previously, the drain resistance increases, and I_{Dmax} decreases while the source resistance does not show significant degradation. In the recovery phase, both R_D and I_{Dmax} partially recover to some extent. However, as soon as the stress is reapplied, R_D and I_{Dmax} go immediately back to the value that they had when degradation stopped. From here on, degradation resumes. This is strong evidence of trapping behavior. This behavior repeats as the stress is turned on and off with the overall level of degradation increasing with every cycle.

This result can be understood in the following sense. First, in the stress period, traps seem to be generated, and electrons get trapped in these traps. If the stress is turned off, some of these traps get depopulated, and the device partially recovers. However, when the stress is reapplied, electrons immediately get trapped again, and trap formation continues. In that sense, recovery is not an appropriate term, and in fact, we have observed only minor recovery with the device at rest for more than 300 days. This is shown in Figure 3-22. The same device used in the experiment of Figure 3-1 has been stressed with the same stress condition at which it had been stressed. After 304 days at rest, I_{Dmax} of the device was partially recovered to some extent, but the device went back to the degraded state immediately upon reapplying the same stress bias. From experiments like this, we can conclude that degradation is irreversible.

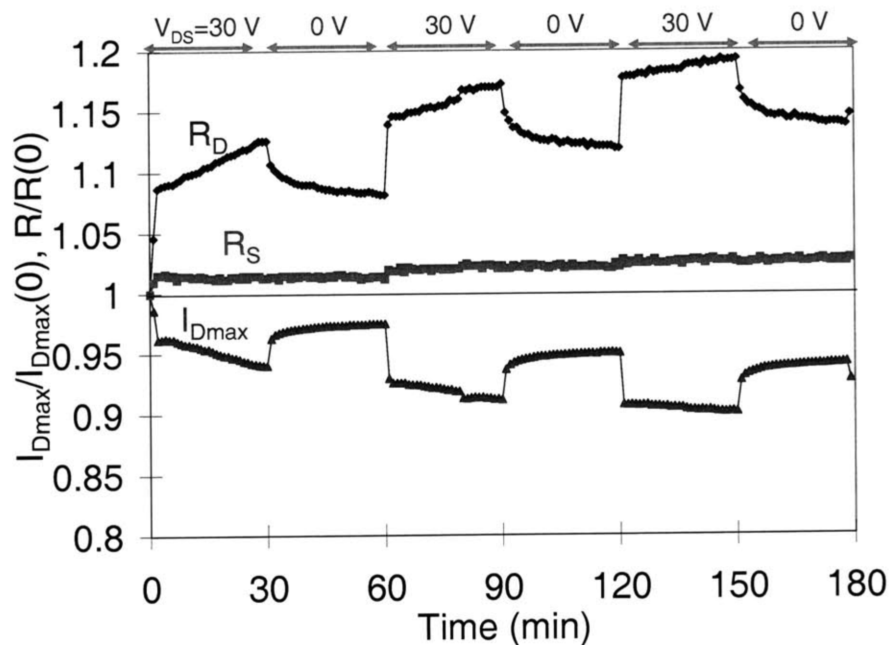

Figure 3-21. Change in I_{Dmax}, R_D, and R_S in a stress-recovery experiment in the OFF state (V_{DS}=30 V, I_D=20 mA/mm) for 30 minutes of stress followed by 30 minutes at rest. This cycle is repeated for three times.

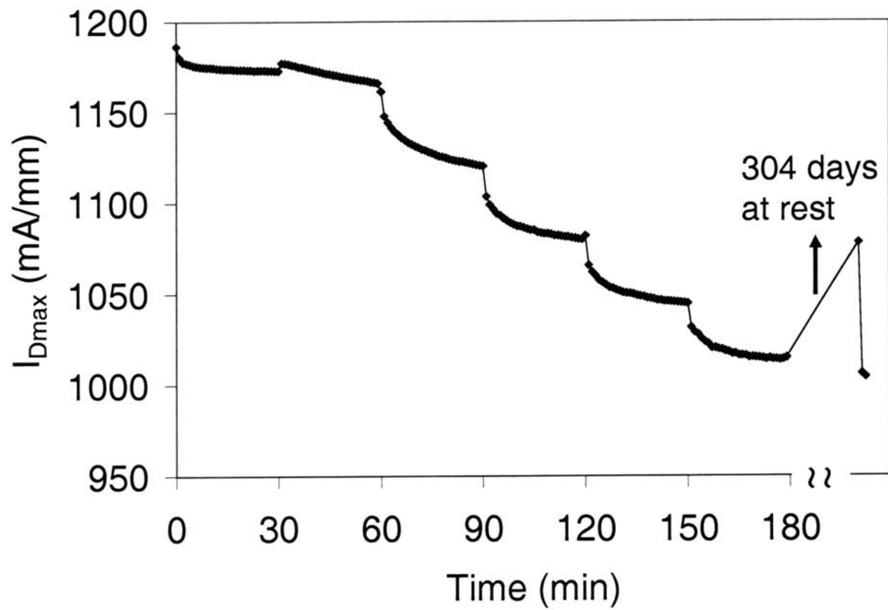

Figure 3-22. Time evolution of I_{Dmax} of the device in Figure 3-1. After the end of the stress experiment in Figure 3-1, the device was put at rest for 304 days before it were measured again. After the first measurement of I_{Dmax}, the same stress (V_{DS}=30 V, I_D=800 mA/mm) was applied for 2 more minutes.

3.5.2. Enhanced Detrapping

In order to confirm our trapping hypothesis, additional stress-recovery experiments have been performed. In these experiments, we could confirm trapping behavior by observing enhanced detrapping in the recovery phase in three different ways.

First, as shown in Figure 3-23, recovery can be enhanced by light illumination. In this experiment, microscope light is turned on for 5 minutes in the recovery period after stressing for 15 minutes. As it can be seen, light illumination greatly enhances recovery, which is a strong signature of electron detrapping.

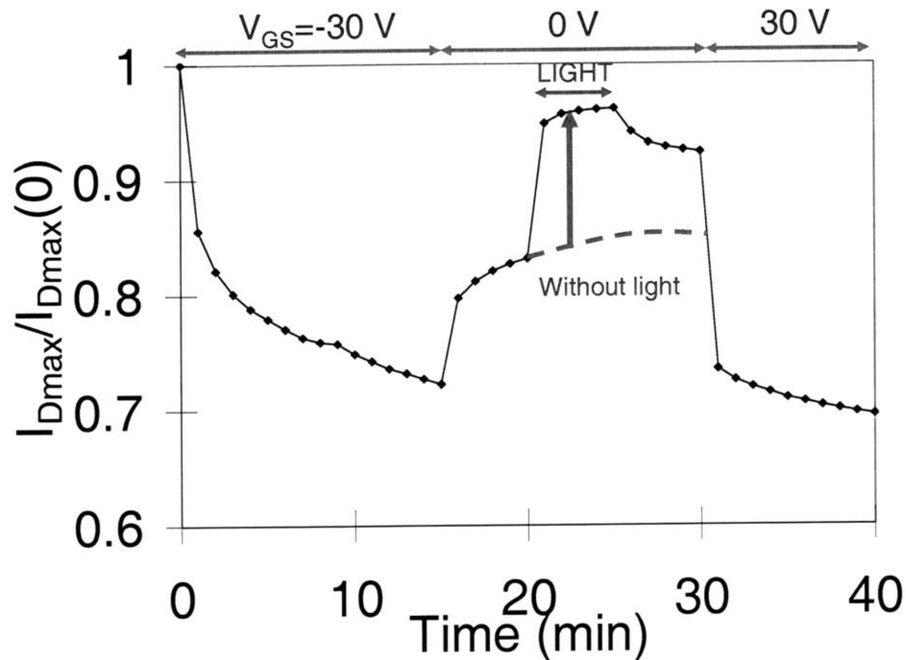

Figure 3-23. Change in I_{Dmax} in a stress-recovery experiment on a standard type device stressed at V_{DS}=0 and V_{GS}=-30 V for 15 minutes and at rest for 15 minutes. Additional stress is applied for another 10 minutes. From t=20 to 25 min, microscope light was illuminated.

We have also observed enhanced detrapping by applying positive gate bias. As shown in Figure 3-24, V_{GS}>0 is applied in the recovery phases in a V_{DS}=0 stress-recovery experiment. As it can be seen in Figure 3-24, this positive gate bias enhances electron detrapping as the voltage increases.

Finally, we have studied the impact of temperature on the recovery phase. We have performed V_{DS}=0 stress-recovery experiments at T=-10, 30, 70, and 110 °C. As shown in Figure 3-25, time constant of detrapping turned out to be smaller at higher temperature, and activation energy of 0.24 eV can be obtained from these experiments, which is consistent with [11].

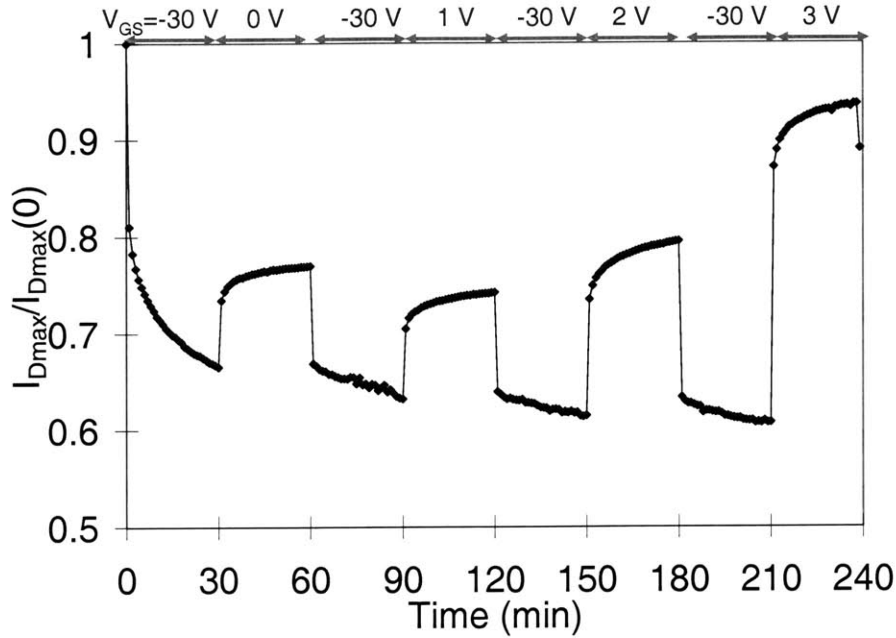

Figure 3-24. Change in I_{Dmax} in a stress-recovery experiment on a standard type device stressed at V_{DS}=0 and V_{GS}=-30V for 30 minutes. Four stress cycles are repeated with different values of V_{GS} during the 30 minutes recovery phase (0, 1, 2, and 3 V).

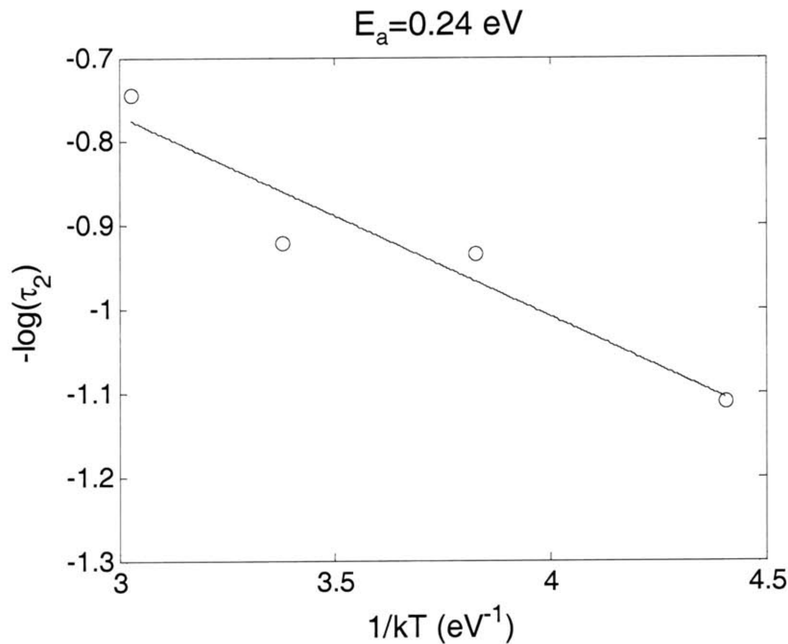

Figure 3-25. Detrapping time constants in V_{DS}=0 stress-recovery experiments.

All of these three experiments are consistent with an electron trapping/detrapping hypothesis, and we can confirm that device degradation is originated from increased electron trapping.

3.6. Trap Generation

In the previous section, we have seen that degradation of GaN HEMT is strongly related to electron trapping. However, it is not still clear whether those involved traps are produced during a device stressing or they are traps that existed before device operation. In order to investigate this problem, we have designed a step-stress-recovery experiment in which we have introduced diagnostic pulses to sample trap density.

The experiment is described in Figure 3-26. We stress the device at V_{GS}=-15 V to -40 V for 10 minutes, and then the device is allowed to recover for 5 minutes. To expedite detrapping time, microscope light is illuminated on the sample throughout the entire length of this experiment. During the recovery phase, a -10 V voltage pulse is applied to the gate, which produces a momentary reduction in I_{Dmax} which is known as current collapse. As the current collapse is known to relate to trapping, we can evaluate the trap density through the response to the -10 V diagnostic pulse. Therefore, in this experiment, we track two figures of merit: the total damage is the change in I_{Dmax} from its maximum value to that at the end of a stress period. In addition, the trap density is evaluated from the current collapse produced by the diagnostic voltage pulses.

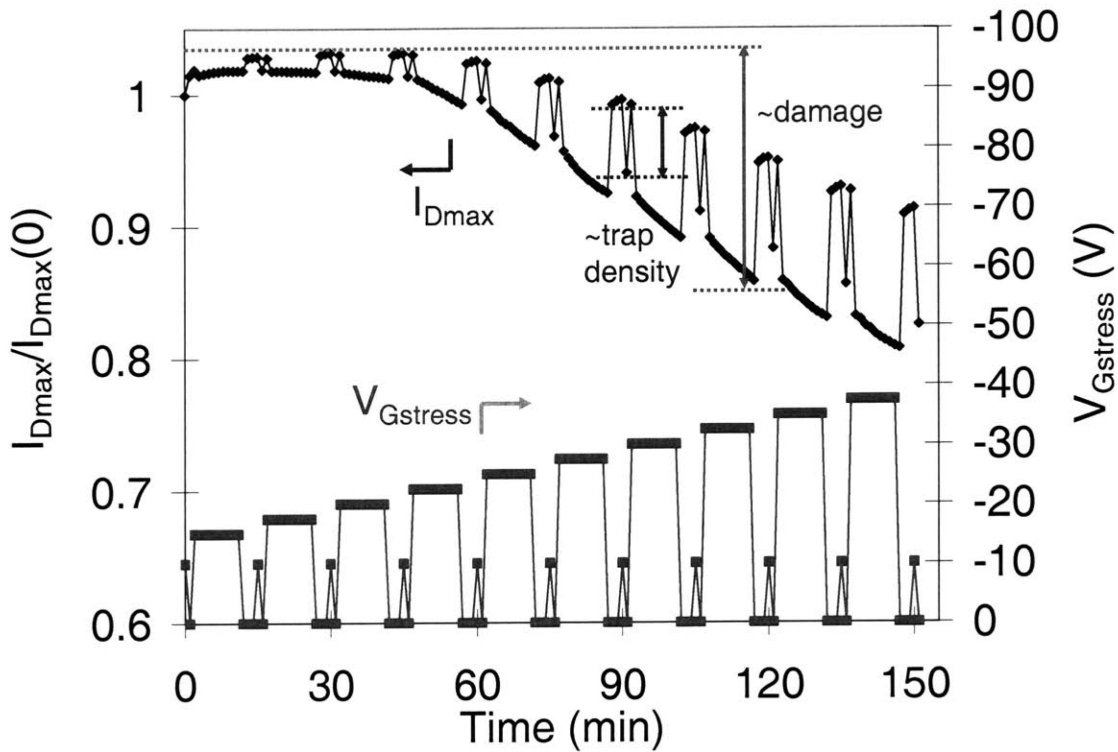

Figure 3-26. Change in I_{Dmax} and stress bias of a V_{DS}=0 step-stress-recovery experiment. V_{GS}=-15~-40 V is applied for stress, and -10 V diagnostic voltage pulses are applied during the recovery phase. The step size is -2.5 V, and the device is stress for 10 minutes in each step. To expedite detrapping, microscope light is turned on during the test.

As it can be seen in Figure 3-26, a sudden onset of degradation at a critical voltage can be again confirmed around 22.5 V. As the damage increase, so does the response to the diagnostic pulse and the trap density. This result is summarized in Figure 3-27 in which damage and current collapse are plotted as a function of the stress bias. It is clear that damage correlates with trap density, and we can confirm that traps are generated during the bias stress.

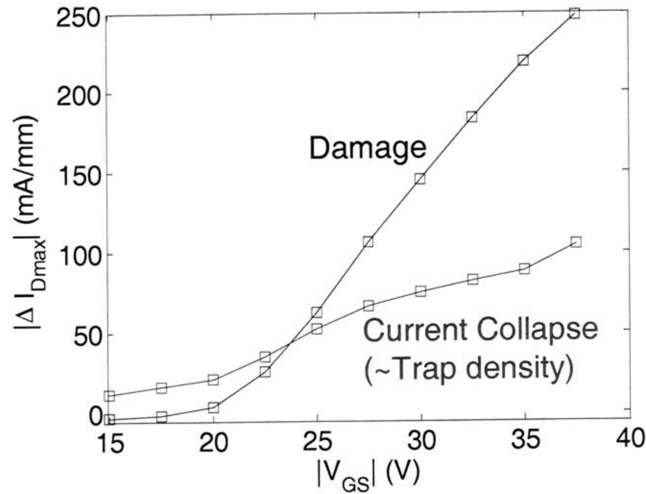

Figure 3-27. Total damage and current collapse produced by diagnostic pulse as a function of the stress bias.

3.7. TLM Step-stress

We have performed step-stress experiments with a Transmission Line Method (TLM) and compared the results with degradation in HEMTs. The TLM is a structure without a gate as shown in Figure 3-28. For a meaningful comparison, we have selected a TLM of which length is identical to L_{GD} of the HEMT.

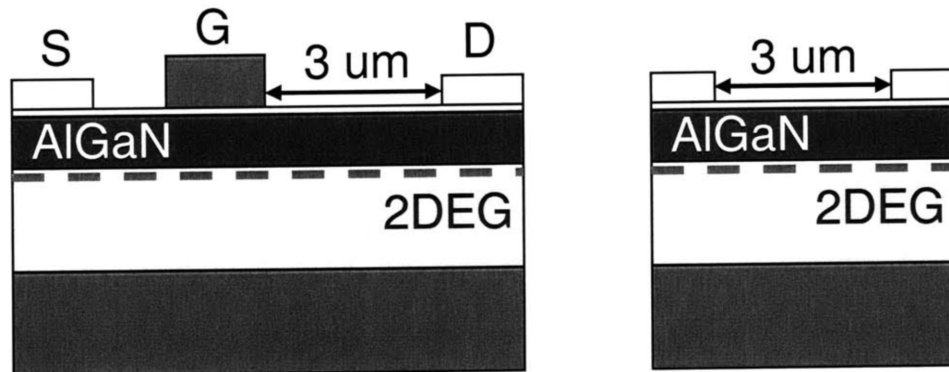

Figure 3-28. A schematic picture of a HEMT and a TLM used for the comparison. L_{GD} of the HEMT is identical to the length of the TLM.

The TLM is step-stressed from 20 V to 26 V, and the HEMT is step-stressed at the same voltage with the stress current at 800 mA/mm. The change in I-V characteristics of the TLM is shown in Figure 3-29. As shown in Figure 3-29 and Figure 3-30, this stress does not introduce any significant degradation of I_{max} of the TLM in spite of a huge current (~1.7 A/mm) [9]. On the other hand, I_{Dmax} of the HEMT degrades severely although the stress current is less than half of that of the TLM. This result strongly confirms that the main driver for degradation is not current. The fact that TLM does not degrade in spite of relatively large lateral electric field suggests that the main driver for HEMT degradation may be vertical electric field that exists only in HEMTs. Also, from the time evolution of low field resistance of the TLM, we cannot see any obvious ohmic contact degradation (Figure 3-30).

From this comparison, we can conclude that HEMT degradation does not correlate with TLM degradation. This is rather different from observations in GaAs and InP HEMTs in which case TLM degradation has revealed physics that has strong correlation with HEMT degradation [19, 21]. In those cases, hot electrons play important roles in device degradation.

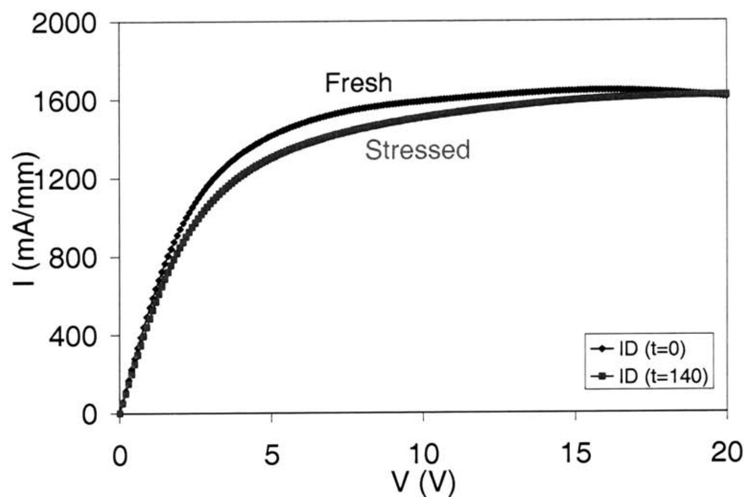

Figure 3-29. Change in I-V characteristics of the TLM before and after the experiment of Figure 3-30. The device was step-stressed at V=20~26 V for 140 minutes.

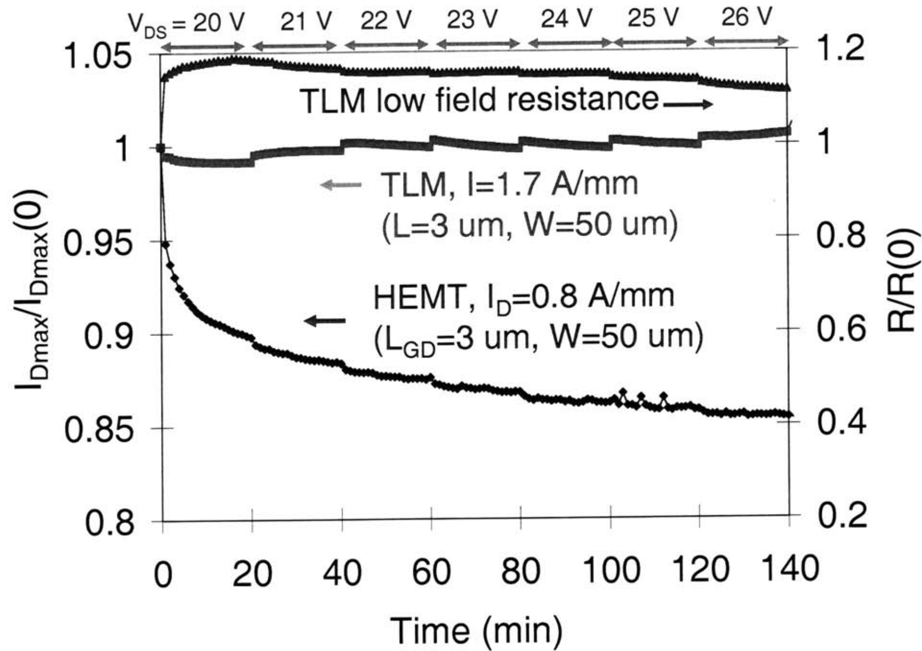

Figure 3-30. Change in I_{Dmax} of a TLM and a HEMT and low field resistance of the TLM. The HEMT is stressed at V_{DS}=20~26 V (1 V step, 20 min/step) and I_D=800 mA/mm. The TLM is stressed at the same voltage, but the current is around 1.7 A/mm. The length of the TLM (3 um) is the same as the gate-drain gap of the HEMT.

In conclusion, this result gives us additional evidence that hot electrons may not be the main cause of device degradation, especially trap formation as discussed in [11].

3.8. Summary of Key Findings

From a number of experiments, we have seen that degradation of GaN HEMT results from trap generation and subsequent electron trapping. This trap generation seems to occur in the drain-gate gap, and sheet carrier density in the extrinsic region to the drain side decreases. However, it appears that this is not surface type degradation. As a result, drain resistance increases and drain current decreases, and this R_D degradation is not dependent on L_{GD}. This degradation is irreversible in that the device goes back to the previously degraded state

when reapplying the stress after a period of recovery. We have observed no significant recovery even after more than 300 days of rest.

As for the origin of this degradation, we have found that electric field plays the most important role, and vertical electric field seems to be more relevant to device degradation. On the other hand, current appears to only be a mild accelerating factor, but it is not clear whether the role of current is supplying hot electrons to the system or increasing temperature in the device.

Also, we have found that there exists a critical voltage beyond which degradation starts to happen, and this voltage is around 25 V in $V_{DS}=0$ condition. When a voltage higher than the critical voltage is applied, both drain and gate current start to degrade. This critical voltage appears to be 10~15 V higher in normal bias conditions, OFF state and high power state.

It is important to note that this overall behavior is reproducible across different devices, wafers, and processes that we have studied. However, it should still be confirmed in the future with more devices that are fabricated in different processes with different wafers.

Chapter 4. Degradation Mechanism

4.1. Introduction

In the previous chapter, we have experimentally studied the electrical degradation of GaN HEMTs. In a preliminary analysis, we have shown that degradation is related to trap generation and electron trapping. In this chapter, our experimental evidence that contradicts the prevailing hypothesis, hot electron involved mechanisms, will be discussed in more detail, and our hypothesis for electrical degradation of GaN HEMTs will be introduced. This hypothesis is supported by a set of additional experiments. Finally, based on our hypothesis, solutions to improve reliability will be discussed.

4.2. Inconsistency with Hot-electron Related Mechanisms

In section 1.3, hot-electron related hypotheses for degradation of GaN HEMTs were introduced. To summarize those mechanisms, hot electrons can gain enough energy to escape the channel and get trapped at the surface area between gate and drain [5]. These trapped electrons deplete channel carriers and degrade the device. Also, it has been postulated that hot electrons produce traps during bias stress [11].

However, several of our experiments are found not to be consistent with a model in which hot electrons are the main cause of electrical degradation. First, we have found that

degradation in the OFF state is comparable to degradation in high power state in spite of the much less current that flows in the OFF state. Particularly remarkable is the V_{DS}=0 state in which the role of hot electrons is most suppressed due to the absence of channel current and in some cases negligible reverse bias leakage current. Despite little effect of hot electrons, degradation in the V_{DS}=0 state is sometimes more pronounced than in the high power state. Additionally, experiments on TLMs have revealed that they undergo negligible degradation in spite of a large current and relatively high lateral electric field. This result is remarkably different from GaAs and InP HEMT processes in which hot electrons produce significant damage to TLMs with a signature that is very similar to that of HEMTs [18, 19].

In our experimental results, hot electron mechanism alone cannot explain the degradation of GaN HEMT that we observe. Later in this chapter, we will see more examples of our experiments that cannot be understood by the hot-electron hypothesis. It then seems that another mechanism is involved to drive electrical degradation of GaN HEMT. This will be discussed in the following sections.

4.3. Piezoelectric Effect of GaN

III-N materials have large spontaneous polarization, and they are also strong piezoelectric materials. These properties are responsible for the high sheet carrier density n_S that can be achieved in AlGaN/GaN heterostructures even without any intentional doping [22]. On top of spontaneous polarization charges, sheet charge is formed through piezoelectric effect at the interface between AlGaN and GaN and at the surface as AlGaN barrier is strained due to lattice mismatch with GaN channel layer. As a result, an internal electric field appears in the vertical direction. This electric field bends the band structure in the AlGaN barrier, which forms a two dimensional electron gas (2DEG) at the AlGaN/GaN interface as shown in Figure 4-1. The source of the 2DEG is believed to be surface donors because of charge neutrality [23]. Since the sheet piezoelectric polarization charge density is a function of

strain, the Al composition of the AlGaN barrier layer strongly determines the sheet carrier density in 2DEG. Also, the thickness of AlGaN barrier mildly affects n_S through the interplay among the Fermi level, occupied levels at the surface, and the conduction band edge of GaN channel [23]. As it can be seen, strain and elastic energy in the AlGaN barrier is inevitable to obtain channel carriers in GaN HEMTs.

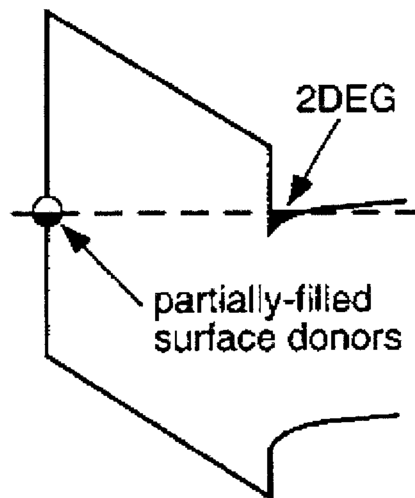

Figure 4-1. Schematic conduction band diagram of AlGaN/GaN heterostructure [23].

4.4. Hypothesis for Electrical Degradation of GaN HEMTs

The fact that electrical degradation is somehow not directly related to hot-electron effects and especially that vertical electric field seems to be mostly relevant to device degradation motivated us to consider the piezoelectric effect as being involved in reliability. Piezoelectricity is reversible in that a piezoelectric material gets mechanically strained under the applied electric field. This is called the inverse piezoelectric effect.

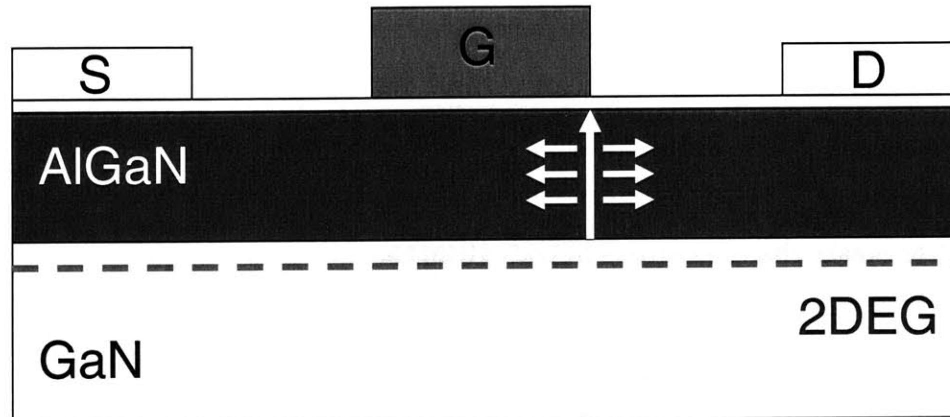

Figure 4-2. Vertical electric field under the gate edge and produced tensile strain due to inverse piezoelectric effect.

During typical device operation, a high voltage is applied to the drain. This produces a high electric field in the gate-drain gap. This field is highly non uniform. As sketched in Figure 4-2, the vertical electric field across the AlGaN barrier layer under the gate edge is very high. This high field produces tensile strain in the AlGaN layer through the inverse piezoelectric effect. If the elastic energy as a result of this additional strain exceeds the critical elastic energy that AlGaN can withstand, crystallographic defects such as dislocations and micro cracks can be formed. These defects can become trapping sites. As a result of carrier trapping, the sheet carrier density in the gate drain gap close to the gate edge decreases producing an increase in R_D and a decrease in I_{Dmax} and output power. Also, strain can relax locally if this damage is excessive resulting in a decrease in n_S. These are all irreversible changes in the device characteristics.

This hypothesis is consistent with all our observations. First, we found that there was a critical voltage at the onset of degradation. This is consistent with our hypothesis as degradation would not start to take place until the elastic energy reaches its critical value. Since elastic energy is proportional to strain squared, and strain is linearly proportional to the vertical electric field, and finally the electric field is a function of voltage, then this implies the existence of a critical voltage. In the previous chapter, we have seen that the critical voltage for degradation in the OFF state or high power state is higher than in the

V_{DS}=0 state. We think that this is due to the overlap of the strain field generated at both ends of the gate in the case of V_{DS}=0 state stress. As a result, crystallographic defects can be more easily produced than in a case in which no additional strain exists on one side of the channel. In the OFF state or high-power state, the strain at the source side is negligible because $|V_{GS}|$ is normally less than 5 V, and it does not affect the degradation in the drain side.

Also, it is important to note that piezoelectric tensor element d_{11}, which relates lateral electric field to normal strain, is zero in AlGaN. This means that the lateral electric field does not contribute to the normal strain as we have observed in TLM experiments. In contrast, the vertical electric field generates strain in both lateral and vertical directions, which increases the elastic energy in the AlGaN barrier. No long term recovery is expected as crystallographic damages are not likely to be recovered at room temperature. The observation that R_D degradation is not dependent on L_{GD} is also consistent with our hypothesis in that only a small area near the gate edge is affected since the vertical electric field decays away from the gate edge.

4.5. Order-of-magnitude Calculation

In order to see if our hypothesis is theoretically plausible, we have performed a back of the envelope calculation. Elastic energy per unit area of a thin film can be expressed as:

$$W = E_Y h \varepsilon^2 \qquad (1)$$

where E_Y is Young's modulus, and h and ε are thickness of the film and its strain, respectively. From the critical thickness curve of AlGaN on GaN (Figure 4-3), an initial elastic energy for the AlGaN barrier in our devices can be estimated to be about 70 % of the critical elastic energy.

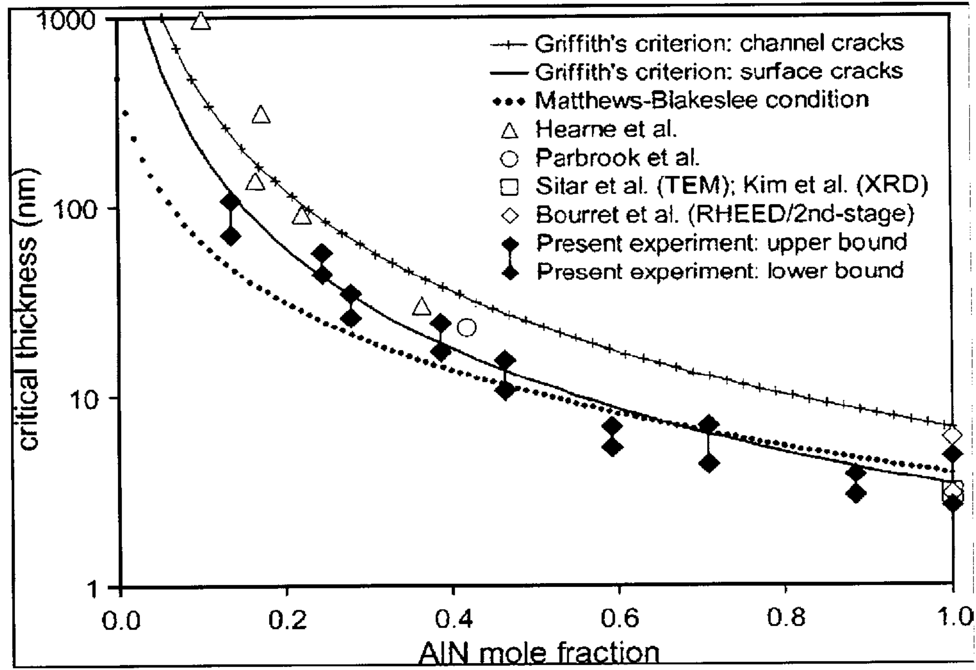

Figure 4-3. Comparison of measured critical thicknesses for strain relaxation in $Al_xGa_{1-x}N$/GaN [24].

Based on Somerville's analytical equation [25], the vertical electric field across the AlGaN barrier at the gate edge of a HEMT where it is maximum, is around 7 MV/cm when the device is biased at V_{DG}=30 V which is just below the critical voltage in the OFF state and high power state. This electric field produces a change in lateral strain in the AlGaN that is given by:

$$\Delta\varepsilon_1 = d_{13}E_3 \sim 0.0015$$

where d_{13} is a piezoelectric tensor element which connects vertical electric field to lateral strain [26] and E_3 is the vertical electric field. This change in mechanical strain is reasonably comparable to experimental measurement [27][1]. This additional tensile strain

[1] In this paper, a change in strain of 0.0004 has been measured at 40 V by micro Raman spectroscopy, which appears to be smaller than our calculation. However, this measurement is an average value of strain in GaN channel where the vertical electric field is much smaller than in AlGaN barrier.

due to the inverse piezoelectric effect is about 20 % of the initial strain due to lattice mismatch. As a result, by equation (1), the elastic energy at around the critical voltage condition becomes 98 % of the critical elastic energy, which is then reasonable to be the threshold for the production of crystallographic defects. From this simple calculation, we confirm that the tensile strain generated by the high vertical electric field can be strong enough to damage the devices.

4.6. Experimental Confirmation

In the previous section we have confirmed that back-of-the-envelope calculations are consistent with our proposed degradation hypothesis. In this section, we will provide additional experimental confirmation.

4.6.1. L_G Dependency in V_{DS}=0 State

As discussed in section 4.4, comparatively large degradation in V_{DS}=0 state appears to be originated from interaction of two strain field produced at both ends of gate edge. In order to confirm the effect of this interaction, we have compared the degradation of three different gate length devices in the V_{DS}=0 condition. The gate lengths are 0.25 um, 0.65 um, and 1.15 um, and other parameters are identical.

Figure 4-4 shows changes in R_D and I_{Dmax} in step-stress experiments. The change in R_S is similar to that in R_D as the stress is symmetric. In this experiment, V_{GS} is stepped up from -15 V to -34 V while V_{DS} is set to 0. As it can be seen, the longest device degrades less, and the critical voltage of the longest device is higher than that of the shortest device. This result is inconsistent with a hot electron hypothesis in that to the first order, the electrostatics in the extrinsic portion of the device must be the same for all three devices.

However, in our hypothesis, the two strain fields that appear at both ends of the gate edge overlap in the center region as shown in Figure 4-5. A longer device provides more room to accommodate mechanical stress towards the center of the device. As a result, the mechanical stress can be spread out more easily in a longer device, and the peak stress at the gate edge can be lower than in a shorter device.

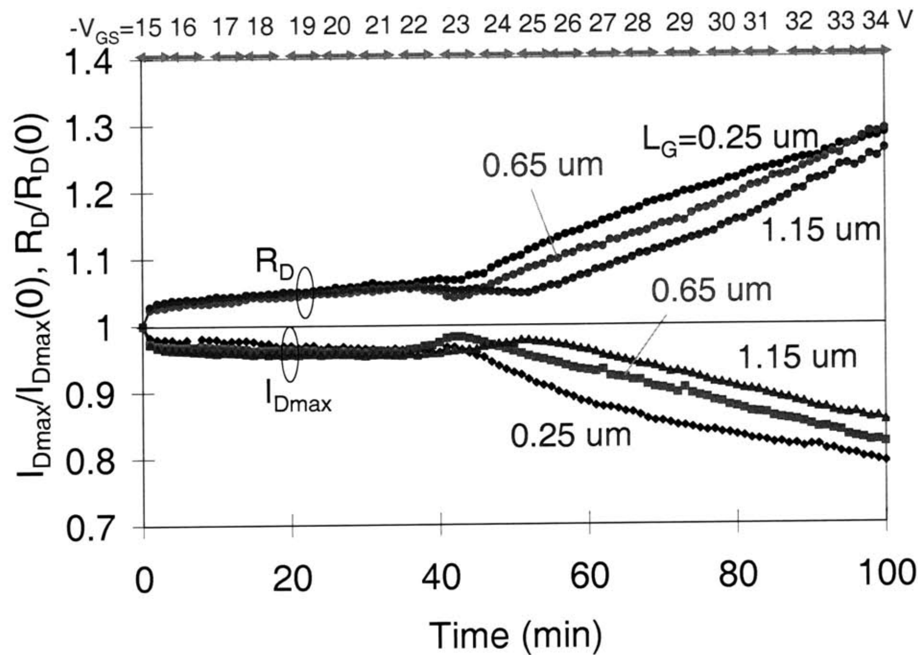

Figure 4-4. Gate length dependence of degradation in V_{DS}=0 step-stress experiments. Different gate length devices (L_G=0.25, 0.65, and 1.15 um) are stressed at V_{DS}=0 and V_{GS}=-15~-34 V (-1 V step, 5 min/step). The threshold of the degradation increases with L_G.

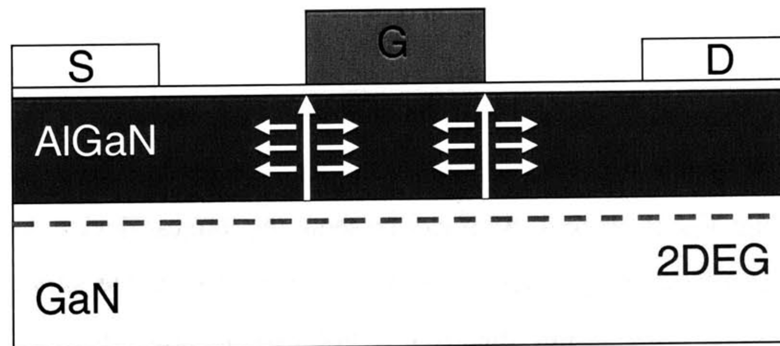

Figure 4-5. Overlap of strain field at the center of the gate region in the V_{DS}=0 state.

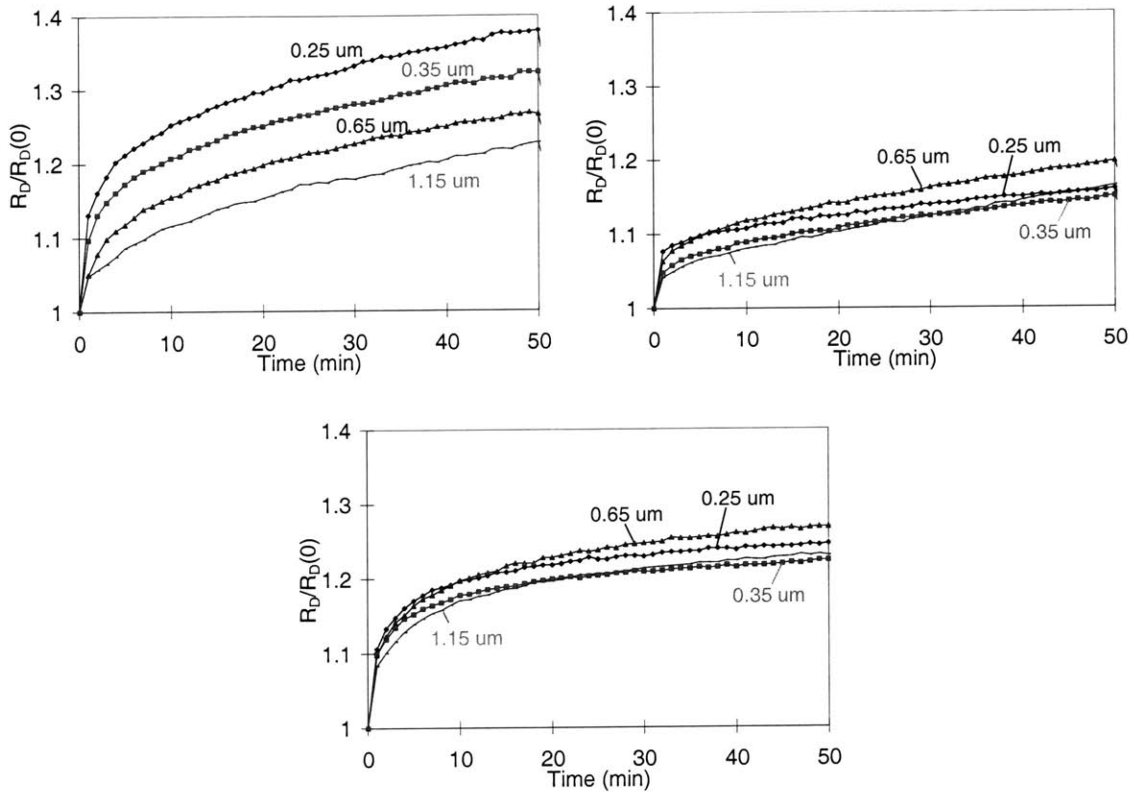

Figure 4-6. Change in R_D in stress experiments on different gate length devices (L_G=0.25, 0.35, 0.65, and 1.15 um) in V_{DS}=0 state (upper left), in OFF state (upper right), and in high power state (bottom). Stress conditions are V_{GS}=-30 V in the V_{DS}=0 state, V_{DS}=35 V and V_{GS}=-5 V in the OFF state, V_{DS}=25 V and I_D=800 mA/mm in the high power state. These devices are stressed for 50 minutes.

This hypothesis also suggests that no gate length dependent degradation is to be expected in the OFF state and in the high power state. This is because the strain produced under the source side of the gate is normally negligible due to relatively small $|V_{GS}|$. In fact, we have not seen a clear dependence on L_G of drain resistance degradation in the OFF state and in the high power state. Figure 4-6 compares the changes in R_D in V_{DS}=0 state (left), in OFF state (right), and in high power state (bottom). It is clear that degradation is more pronounced for shorter devices in the V_{DS}=0 state whereas no clear dependency on L_G is seen in the OFF state and in the high power state. In addition, degradation is much larger in the V_{DS}=0 state in spite of smaller stress voltage as discussed in section 4.4.

4.6.2. AlGaN Buffer

Another confirmation of our hypothesis has been obtained by comparing devices with different strain in the AlGaN barrier. Our hypothesis predicts that a device with less initial elastic energy or strain in the AlGaN barrier should degrade less. In order to see the effect of initial elastic energy, we have compared our baseline structure device to an otherwise identical device that features an AlGaN buffer. As the lattice constant of AlGaN buffer is closer to the lattice constant of the AlGaN barrier, introducing an AlGaN buffer should result in lower initial strain and elastic energy stored in the AlGaN barrier.

First, we have compared the effect of the AlGaN buffer in DC condition. Figure 4-7 shows the change of I_{Dmax} in a V_{DS}=0 step-stress experiment. As it can be seen, the device on AlGaN buffer degrades less than the device on the regular GaN buffer.

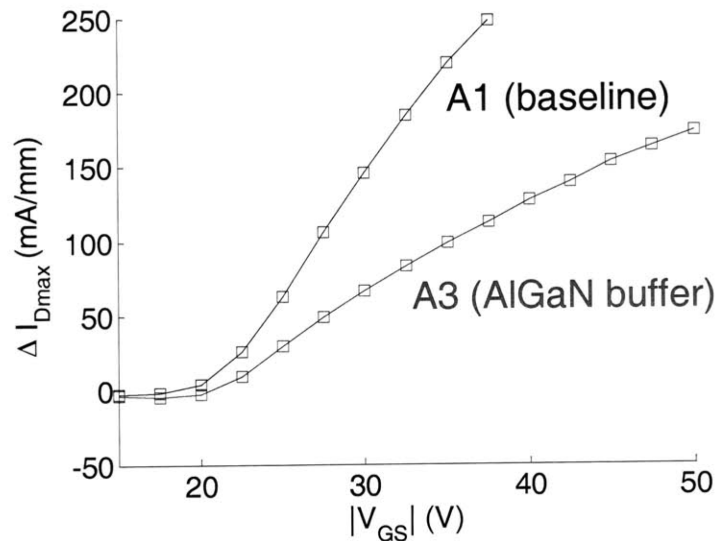

Figure 4-7. Total damage as a function of stress bias in V_{DS}=0 step stress experiment on type A1 (GaN buffer) and type A3 (AlGaN buffer) devices.

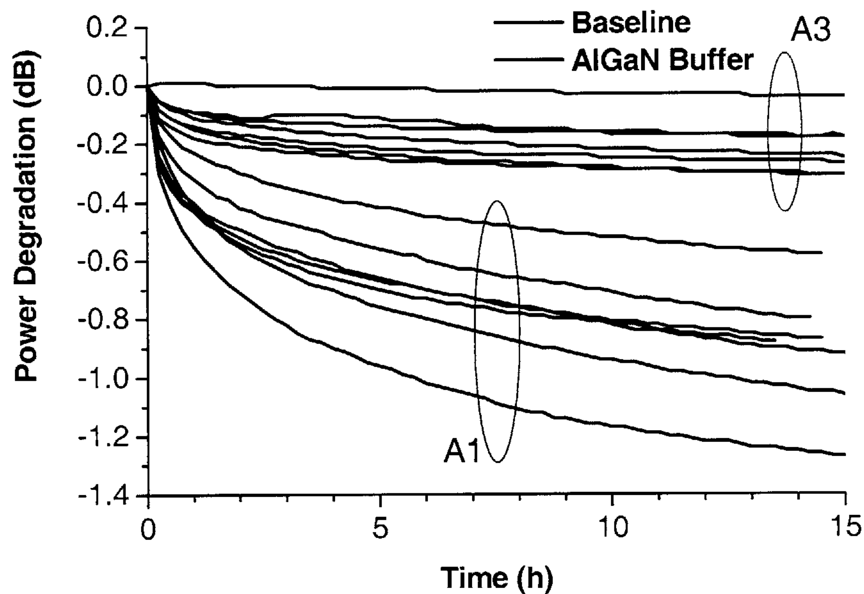

Figure 4-8. Output power degradation of 400 um type A1 devices (baseline structure, GaN buffer) and type A3 devices (AlGaN buffer). The devices are stressed at P_{out}=5 W/mm, V_{DS}=28 V, f=10 GHz.

RF Power soak stress experiments also show that output power degradation is smaller in AlGaN buffer devices as shown in Figure 4-8. Both RF and DC stress tests reveal that reducing strain and elastic energy provides better reliability. This result is also inconsistent with hot-electron hypothesis as the same amount of hot electrons should exist at the same electrical condition regardless of the elastic energy in the AlGaN barrier.

4.6.3. XTEM

Direct confirmation of defect formation is provided by TEM analysis. Our collaborators at TriQuint have produced TEM images of a device which went through a severe long term life test [7]. This device was stressed with V_D=28 V, I_{DQ}=150 mA/mm at 310 °C. The input power was 23 dBm. After the life test, the output power degraded by 3 dB.

In Figure 4-9, we can see a clear crystallographic defect in the AlGaN barrier under the gate edge of drain side. As the vertical electric field is the highest in the AlGaN area and initial strain in the GaN channel region is zero, defect formation seems to be confined to the AlGaN barrier. On the other hand, the source side does not show any obvious defect formation. In fresh devices, no defects can be found, and similar crystallographic damages can be seen in different degraded devices and in different sample cuts.

This result is the strongest evidence of our hypothesis. However, not every cut of degraded devices shows the damage as clear as Figure 4-9. This might suggest that defect does not form everywhere along the gate finger width. This needs to be investigated further in the future work.

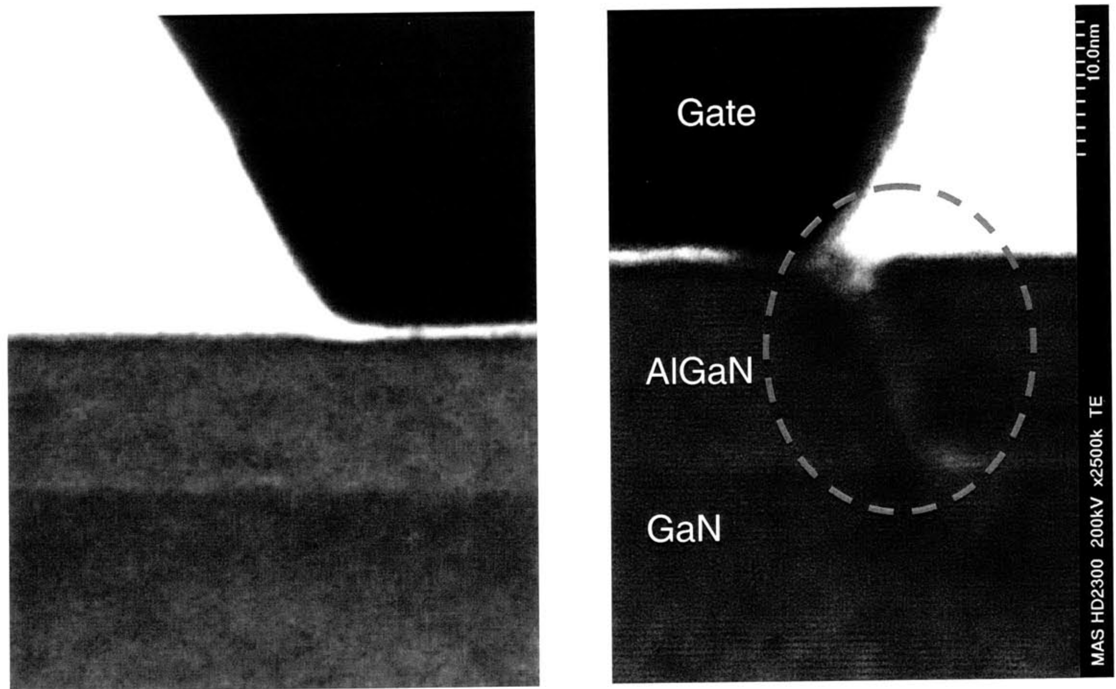

Figure 4-9. XTEM images of a degraded GaN HEMT. Left: source side; right: drain side [7].

4.7. Suggestions for Reliability Improvements

Our hypothesis for degradation suggests several approaches to improve reliability of GaN HEMTs. We discuss these in this section.

As degradation is not likely to happen if the total elastic energy in the AlGaN barrier does not exceed the critical elastic energy, minimizing initial elastic energy in the AlGaN barrier should be effective as it gives more room before reaching the critical value. Because elastic energy is a function of both the thickness of the film and the initial strain due to lattice mismatch, reducing the AlGaN barrier thickness [8] or its Al composition [28] should give rise to better reliability. In fact, it has been reported that GaN MESFETs, which do not have any AlGaN barrier, do not degrade at all even after 150 hours of bias stress at 350 °C [29]. However, both of these solutions have trade-offs with performance of the device because both approaches result in a lower sheet carrier concentration in the channel as discussed in section 4.3 [22]. As the sheet carrier density in 2DEG is a weaker function of the AlGaN thickness, it seems that reducing the AlGaN thickness instead of reducing the Al mole fraction is more effective, but further investigation is still needed.

Also, a mechanically strengthened AlGaN barrier should be considered. If the AlGaN barrier is supported by another layer on top of it, it should be able to withstand a higher mechanical stress. For this purpose, a GaN cap or a mechanically strong passivation layer could be effective. In fact, in [30], it has been speculated that by NH_3 treatment before passivation, the structure becomes more resistant to damages through the strengthening of bonds in the material. Also, it has been observed that a GaN capping layer helps preventing material degradation [31].

Finally, from electrostatics point of view, a design that minimizes electric field under the gate edge should improve reliability. A smaller electric field produces less mechanical stress that can produce crystallographic defects as well as generates fewer hot electrons,

which should be also better for reliability. It is well known that field plates help to improve reliability [7]. Operating devices at lower voltage should also mitigate electrical degradation of GaN HEMTs. Interestingly, all these solutions are experimentally proved in the literature.

4.8. Conclusions

In this chapter, we have reviewed our experimental observations that are inconsistent with the hot electron hypothesis for electrical damage in GaN HEMTs. Instead, we have investigated strong piezoelectric effect of GaN, which is one of the unique properties of the material, as an important mechanism for electrical degradation of GaN HEMTs. We have postulated a model in which mechanical strain generated by the vertical electric field across the AlGaN barrier through the inverse piezoelectric effect produces crystallographic defects. These defects produce trapping sites, and sheet carrier density decreases due to subsequent electron trapping. As a result, drain resistance increases, and drain current and output power decrease. Through a back-of-the-envelope calculation, we have shown that the critical elastic energy that AlGaN layer can withstand on GaN channel can be reached at around the critical voltage. In addition, as experimental confirmation, we have discussed L_G dependency of degradation in the V_{DS}=0 state and compared degradation of devices with different initial elastic energy in the AlGaN barrier. Finally, our hypothesis was strengthened by cross sectional TEM images that show defect formation under the gate edge on the drain side after severe device degradation.

Chapter 5. Conclusions

5.1. Summary of Key Findings

In this thesis, we have carried out a systematic study of the electrical reliability of GaN high electron mobility transistors. Following previous studies on reliability of GaAs pseudomorphic HEMTs [19] and InGaAs metamorphic HEMTs [18], we have developed an experimental framework for studying the reliability of GaN HEMTs. This framework includes a benign characterization suite that extracts important device parameters as the device is degraded. Also for this study, a special purpose reliability test chip has been developed. These have allowed us to test various devices with different geometries to reveal the origin of device failure. In our experiments on GaN HEMTs, different stress bias conditions have been investigated, and different stress methods are followed: step-stress, stress-recovery, and step-stress-recovery.

Under various stress conditions, we have confirmed that electrical stress results in an increase in R_D and a decrease in I_{Dmax}. Under regular bias condition, R_S changes negligibly. We have found that degradation in the OFF state is comparable to that in the high power state and that almost no degradation takes place in the ON state. This result suggests that it is not current but electric field that mostly drives electrical degradation. This is confirmed by experiments on Transmission-Line Method (TLM) structures in which I_{max} of the TLM did not degrade in spite of the large current, while I_{Dmax} in a similar HEMT showed significant degradation. The role of current appears to be a mild accelerating factor, but it is

not clear whether its role is through supplying hot electrons or increasing junction temperature. From the experiments on TLMs, we could also confirm that ohmic contacts are not significantly degraded during device operation. From the fact that TLMs do not degrade in spite of a relatively large lateral electric field, we have postulated that the vertical electric field is more relevant to the degradation of GaN HEMTs.

Step-stress experiments in the V_{DS}=0 state have revealed a clear onset for I_{Dmax} and series resistance degradation, which we have defined as the critical voltage for degradation. This critical voltage is found to be higher under ordinary bias conditions, high power state and OFF state. It turned out that gate leakage current also starts to degrade around the same critical voltage, and the origin of this I_G degradation is from the gate-drain junction. This implies the same origin of I_D and I_G degradation, but a precise mechanism of gate leakage degradation is still unclear. Also, stress experiments in V_{DS}=0 state have confirmed that a device can be severely degraded without the effect of hot electrons as we have seen significant degradation in the V_{DS}=0 state despite negligible current. This result supports our hypothesis that only the electric field matters in device degradation, and it is inconsistent with the widely believed hot-electron involved mechanisms.

In stress-recovery experiments, we have seen strong trapping behavior. By incorporating diagnostic voltage pulses, we could confirm that traps are created during device operation as mentioned in [11]. Some of the electrons that are trapped in these traps get detrapped when the device is put at rest, but they get immediately retrapped if the device is again stressed. Trapping behavior can be seen in other stress-recovery experiments in which detrapping is enhanced in the recovery period by light illumination, by applying positive gate voltage, and at higher temperatures.

In many of our experiments, a hot electron mechanism acting alone is inconsistent with our observations. This finding coupled with observations that the vertical electric field is more relevant to device degradation made us postulate a piezoelectric effect related mechanism.

Unlike other III-V materials, piezoelectricity of III-N is unique and strong. As GaN HEMTs usually operate at very high voltage, the vertical electric field is high especially across the AlGaN barrier under the gate edge. Through the inverse piezoelectric effect, this high vertical electric field gives rise to tensile strain in the AlGaN barrier that adds up on top of the original strain existing in the AlGaN layer due to the lattice mismatch with the GaN channel. If the elastic energy in the AlGaN barrier becomes comparable to the critical elastic energy that AlGaN can stand on GaN, crystallographic defects can be formed. If the stress is excessive, the local strain may actually partially relax. We hypothesize that defect formation through the inverse piezoelectric effect and subsequent electron trapping is the main cause of the decrease in sheet carrier concentration. This give rise to increase in R_D and decrease in I_{Dmax}, eventually resulting in a loss in output power.

Back of the envelope calculations support our hypothesis: we have shown that increased tensile strain due to high vertical electric field at around the critical voltage can produce elastic energy that is comparable to the critical elastic energy. Also, V_{DS}=0 step stress experiments on different gate length devices and comparison between devices with reduced strain in the AlGaN barrier and the baseline structure have supported our hypothesis experimentally. Finally, cross sectional TEM images of a severely degraded device have confirmed the formation of crystallographic defects under the gate edge on the drain side of the device. In contrast, the source side does not show any obvious degradation.

Based on our hypothesis, we have suggested several solutions to improve electrical reliability of GaN HEMTs. As it is important to keep the elastic energy well below the critical elastic energy, reliability can be improved either by reducing the initial elastic energy in the AlGaN barrier or by lowering the electric field under the gate edge. The former can be achieved by having thinner AlGaN or lower Al composition in the AlGaN. The latter can be achieved by an effective field plate design or device operation at lower voltages.

5.2. Suggestions for Further Work

Although we have proposed a new mechanism for the electrical degradation of GaN HEMTs, our research is still in the preliminary stages. This research should be continued to find more details about our proposed mechanisms as well as other mechanisms that might be degrading the devices in a concurrent way. There are many experiments that could be done. Here we suggest some of the most relevant ones for future research.

First of all, our hypothesis should be confirmed more carefully. Especially, the effect of vertical electric field is not perfectly clear at this point, and we should be able to find a way to separate the effects of vertical and lateral electric field. This might requires special test structures designed for this purpose. Also, more detailed studies may be needed to understand how mechanical stress produces crystallographic defects through the inverse piezoelectric effect. In addition, it would be interesting to investigate the reliability of AlGaN/GaN HEMTs fabricated on a wafer with a crystallographic orientation other than [0001] which is normally used for the fabrication of GaN devices. This is because the piezoelectric effect in GaN changes in crystals with different orientations. Finally, a precise understanding of traps involved in device degradation is still missing.

On top of the inverse piezoelectric effect induced mechanism, we believe that other mechanisms can play some roles in device degradation, and we need to understand them. In fact, we have focused mostly on changes in I_{Dmax}, R_D, and R_S in this thesis. However, for example, we still do not have a clear understanding of the change in threshold voltage, and it seems that this change is affected by some other mechanism as we observe sometimes positive and sometimes negative shifts in V_T. Also, the degradation mechanism of the gate current is still in question although we have found that degradation of gate current and drain current nearly always take place simultaneously. To investigate these issues further, we may need to design experiments under different bias conditions. Also, investigation of

the effect of junction temperature is of importance, and stress experiments at different temperatures will reveal more details of the physics of reliability.

In addition, light emission study as done in [19] will be also interesting. Although our main observations made us believe that hot electron effects and impact ionization are less important in GaN HEMT degradation, we expect to learn much from light emission experiments. Other than this, micro Raman spectroscopy can be helpful to measure local strain or temperature distribution in a device [27, 32]. Finally, a more systematic TEM analysis of degraded devices should be carried out in the future.

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