Low Pressure Epitaxial Growth, Fabrication and Characterization of Ge-on-Si Photodiodes

by

Oluwamuyiwa Oluwagbemiga Olubuyide

Masters of Engineering, Electrical Engineering and Computer Science
Massachusetts Institute of Technology, June 2001

Submitted to the
Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements
for the degree of

Doctor of Philosophy in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
[February 2007]
January 2007

Signature of Author _____
Department of Electrical Engineering and Computer Science
January 18, 2007

Certified by _____
Judy L. Hoyt
Professor of Electrical Engineering
Thesis Supervisor

Accepted by _____
Arthur C. Smith
Professor of Electrical Engineering
Chairman, Department Committee on Graduate Students

Low Pressure Epitaxial Growth, Fabrication and Characterization of Ge-on-Si Photodiodes

by

Oluwamuyiwa Oluwagbemiga Olubuyide

Submitted to the Department of Electrical Engineering and Computer Science on January 18, 2007 in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering and Computer Science

Abstract

In order to facilitate the integration of photonic systems onto an electronic chip, near infrared photodiodes utilizing novel materials such as germanium must be monolithically integrated onto the Si CMOS platform. Such near-infrared photodiodes can be utilized for a plethora of applications such as optoelectronic ADCs, optical interconnects, photonic integrated circuits, and near infrared cameras.

In this work, the major focus is on investigating processes utilizing a Low Pressure Chemical Vapor Deposition (LPCVD) Applied Materials Epi Centura™ system to deposit germanium onto silicon substrates (Ge-on-Si). A growth space is identified to deposit blanket and selective epitaxial 1 to 3 μm-thick Ge-on-Si films via a two-step process. These deposited Ge-on-Si films have a low root-mean-square surface roughness (below 2 nm) and a moderate threading dislocation density (~ 10^7 cm^{-2}) after an annealing process.

Utilizing these Ge-on-Si films, vertically illuminated Ge-on-Si *pin* photodiodes are fabricated in a CMOS compatible process. The best photodiodes fabricated in this work have low dark current values (below 10 mA/cm^2), high responsivity (~ 0.45 A/W at 1.55 μm wavelengths) and 3-dB frequency response in the gigahertz range. Due to the importance of the photodiode reverse bias leakage current for circuit applications, the reverse bias leakage current is investigated and characterized in detail for various Ge-on-Si *pin* photodiodes. Trap assisted tunneling was found to be the dominant reverse bias leakage mechanism.

These Ge-on-Si films show great promise for leveraging the integration of photonic devices onto the Very Large Scale Integration (VLSI) platform, and once there is improved reproducibility in the fabrication process, specifically the passivation of germanium surface states, the promise of these Ge-on-Si films can be fully realized.

Thesis Supervisor: Judy L. Hoyt
Title: Professor of Electrical Engineering

Acknowledgements

"Education is not the filling of a vessel but the lighting of a flame." This quote by Socrates exemplifies my ideas about the last few years at the Microsystems Technology Laboratories (MTL), and in this section, it is my deepest pleasure to acknowledge at least some of the people who have contributed their warmth, energy, and experience to not only make this thesis possible, but to teach me on a fundamental level how high quality research is conducted. I would like to thank my advisor, Professor Judy L. Hoyt, first and foremost for all the help over the past five plus years. She is always been willing to spend her time with her students and constantly encourages them whenever they run into the inevitable roadblocks that are part of the research process. Judy's creativity, seemingly boundless energy, meticulousness, and sheer determination when tackling scientific problems has been a constant source of inspiration to me, and I can only hope that I have inculcated some of the above qualities in our last half decade together. Thank you, Judy. I would also like to acknowledge the assistance of the remainder of my thesis committee, Professor Jesus del Alamo and Professor Akintunde (Tayo) Akinwande. I have known these two professors since my undergraduate days at MIT. For example, Professor del Alamo was my 6.012 recitation instructor in the spring semester of 1998, and it was during his stirring lectures that I seriously started considering learning more about this field of "semiconductors." Moreover, Professor del Alamo's ability to instantaneously grasp the key essentials of any problem, has been a constant pleasure to behold. Professor Akinwande knew my father, hence as soon as I came to MIT as an

undergraduate, he took me under his wing. Through the past decade, we have shared many invaluable discussions at his office, during our numerous "ice cream" socials, and at his home. Thank you, Professor Akinwande, you have truly enriched my MIT experience at all levels.

Analog Devices, Inc., has also been a integral part of my doctoral experience, not only through their funding, but also through the sharing of their expertise of the semiconductor device fabrication process. I would especially like to gratefully acknowledge the contribution of John Yasaitis, for his masks, process flows, and numerous ideas.

Of course, there was life outside the thesis, and for this I would like to acknowledge the support of various members of the Hoyt group. First, Gary Riggott, who has always been there to talk and share many jokes over the past few years, it has truly been to my benefit to have known you, even when we were confined to the using the "bucket." Meekyung Kim, whom I consider the perfect officemate, the only regret I have is that she just joined the group in 2005. Cait Ni Chleirigh has always been a valuable verbal sparring partner, I will miss many of our energetic discussions. Leonardo Gomez, I hope I'll be able to find another avid science fiction reader to have nice discussions with wherever I go. Moreover, many of the new Hoyt group members such as Nicole DiLello and Pouya Hashemi, I wish you all the best with your academic careers, you've certainly chosen wisely thus far. I will also like to acknowledge the support of many past group members such as Satoshi-san, who always had time to discuss soccer; Ingvar Aberg who has always been generous with his time and expertise;

Guangrui (Maggie) Xia and Ryan Lei, both of whom always gave me such good advice on all matters personal and professional; Tonya Drake, who always had such a effervescent personality. I would also like to acknowledge the useful discussions with Scott Yu and Kosuke Kusakari. Finally, the numerous administrators over the years, such as Michele Hudak, Celia Mokalled, Lindsay Petrillose, all of whom have made paychecks, meetings, conferences, and papers come together so seamlessly over the years, thanks, your help is greatly appreciated.

My project involved quite a number of collaborators outside the Hoyt group, I would like to acknowledge the assistance of the Electronic Photonic Integrated Circuits (EPIC) program, through which I got to work with many talented graduate students such as Jason Orcutt, Milos Popovic, Felix Grawert, Hyunil Byun, and Fuwan Gan. I would also like to acknowledge the insightful discussions with Professor Kaertner, Professor Rajeev Ram, and Professor Erich Ippen.

I also had the pleasure of working closely with Professor Kimerling and his group, who guided through my introduction to the world of photonics. I would especially like to thank David Danielson, Jifeng Liu, Xiaochen Sun, Wojciech Giziewicz, Jurgen Michel, for all the assistance with measurements, generosity with equipment and their invaluable expertise, thank you!

Most theses are not complete without the fabrication of a device, and practically all students gain familiarity with the fabrication sections of MTL and the staff. Although all of these staff members have contributed repeatedly of their

time and energy to make my project a success, I would like to note the special contributions of Bernard Alamariu, Eric Lim, Paul Tierney, Scott Poesse, Dennis Ward, Daniel Adams, Paudely Zamora, Kurt Broderick, Linhvu Ho, Bob Bicchieri, Brian McKenna, and David Terry.

A very special part of my thanks is devoted to Deborah Hodges-Pabon, who is a very special person at MTL, if the professors are the head and soul, the fabrication staff are the body, then Debb is the heart of MTL. There are so many ways in which Debb has contributed to my MIT experience, that listing them in complete detail would probably entail writing a treatise. To put is simply, Debb, please stay the person you are, and all the good in the world will continue to deservedly come your way.

I would also like to acknowledge the help of many of my friends at MTL, although work takes ninety percent of our time, some of my best ideas and thinking happened in the company of others. A short listing of the people who made the past five years fly by are Jörg Scholvin, Kwaku Abrokwah, Reginald Bryant, Bosun Adeoti, Andrew Fan, Ole Nielsen, Niamh Waldron, Andrew Ritenour, John Hennessy, Anita Villaneuva, Joyce Wu, Ali Khakifirooz, Blaise Gassend, and Valerie Leblanc (Gassend).

I would also like to acknowledge all the useful advice from Professor Martin Schmidt in his capacity as my academic counselor, Professor Charles Sodini, whose teachings during my Masters of Engineering program I have found to be of increasing relevance as the years roll by, and Professor Dawson, who has a knack of always putting situations in perspective. I also have to acknowledge

the generous assistance of Professor Mark Somerville and Tomas Palacios is allowing me access to their labs for some of my final measurements on the Ge-on-Si photodiodes.

I would also like to acknowledge the assistance of Clifford King and Malcolm Carroll who helped me learn all about the Applied Materials Epi Centura system in the summer of 2001.

My family has also been invaluable sources of feedback, advice, and encouragement during my entire doctoral process, thank you, I could not have gotten so far, so quickly without your assistance, and I will be forever grateful.

Finally, I will like to thank my wife, Natalie, who has always been my steadfast companion over the past ten years, you have been the light of my life, and it is with great happiness that I look forward to spending the remainder of our lives together.

This thesis is dedicated to the memory of

Professor Olusegun Ayokanmi Olubuyide

"The lighthouse that never fails"

Table of Contents

List of Figures

List of Tables

Chapter 1: Introduction

1.1 Motivation

Processing of information in digital systems requires data acquisition, devices and circuits for logic functions, and architectures for the storage and transfer of information. Moore's law, or the continuing exponential reduction of feature sizes in the silicon Complementary Metal Oxide Semiconductor (CMOS) industry has not only led to a greater number of digital devices available at dramatically lower costs per device, but has also led to continuous improvement in device speed. The corresponding ubiquitous, low cost, and high speed nature of digital devices has had an enormous impact on the field of digital signal processing (DSP), leading to a plethora of DSP devices and applications ranging from high speed communication networks to new imaging techniques. Although new applications for DSPs are continuously being developed, one of the key limitations to fully realizing the potential of the digital systems application space lies in the data acquisition step [1].

Real world information is almost universally encoded in an analog format, hence before the information can be processed in a digital system, it must first be sampled and digitized in an Analog-to-Digital Converter (ADC). For high speed communications in the gigasample per second range, the number of bits that can be encoded in a purely electronic ADC has only increased by ~2 bits in the last decade [2]. The current bottleneck of the high speed bit resolution of ADCs is the

timing jitter of the sampling pulses, which in purely electronic systems is fundamentally limited to the 250 femtosecond range. On the other hand, optical clock pulses from mode-locked lasers (MLL) currently exhibit sub-10 femtosecond timing jitter; making photonic sampling systems attractive for order-of-magnitude improvements in the bit resolution of novel photonic ADC systems. An additional advantage of photonic ADC architectures is that it also creates the possibility of channeling the optically sampled data at lower data rates for electronic quantization, further improving the bit resolution of ADCs.

The potential benefits of photonic analog-to-digital conversion techniques has led to intensive research in the last 10 years [1-6]. As shown in the time-interleaved optical sampling architecture of Figure 1.1, the requirement for high density device integration in photonic ADC architectures leads to a need for the optical sampling modulators, optical filters, and photodetectors to be integrated onto a single chip. All these devices should preferentially be monolithically integrated onto a CMOS compatible technology platform. Specifically, in this thesis, the feasibility of integrating near infrared wavelength germanium photodetectors onto the silicon CMOS platform will be addressed. Besides the potential applications in analog-to-digital conversion discussed above, integrated germanium on silicon (Ge-on-Si) photodetectors may find application in a wide range of areas, including but not limited to chip-to-chip optical interconnects, optical switches, ethernet transceivers, infrared imaging systems, and photonic integrated circuits [7].

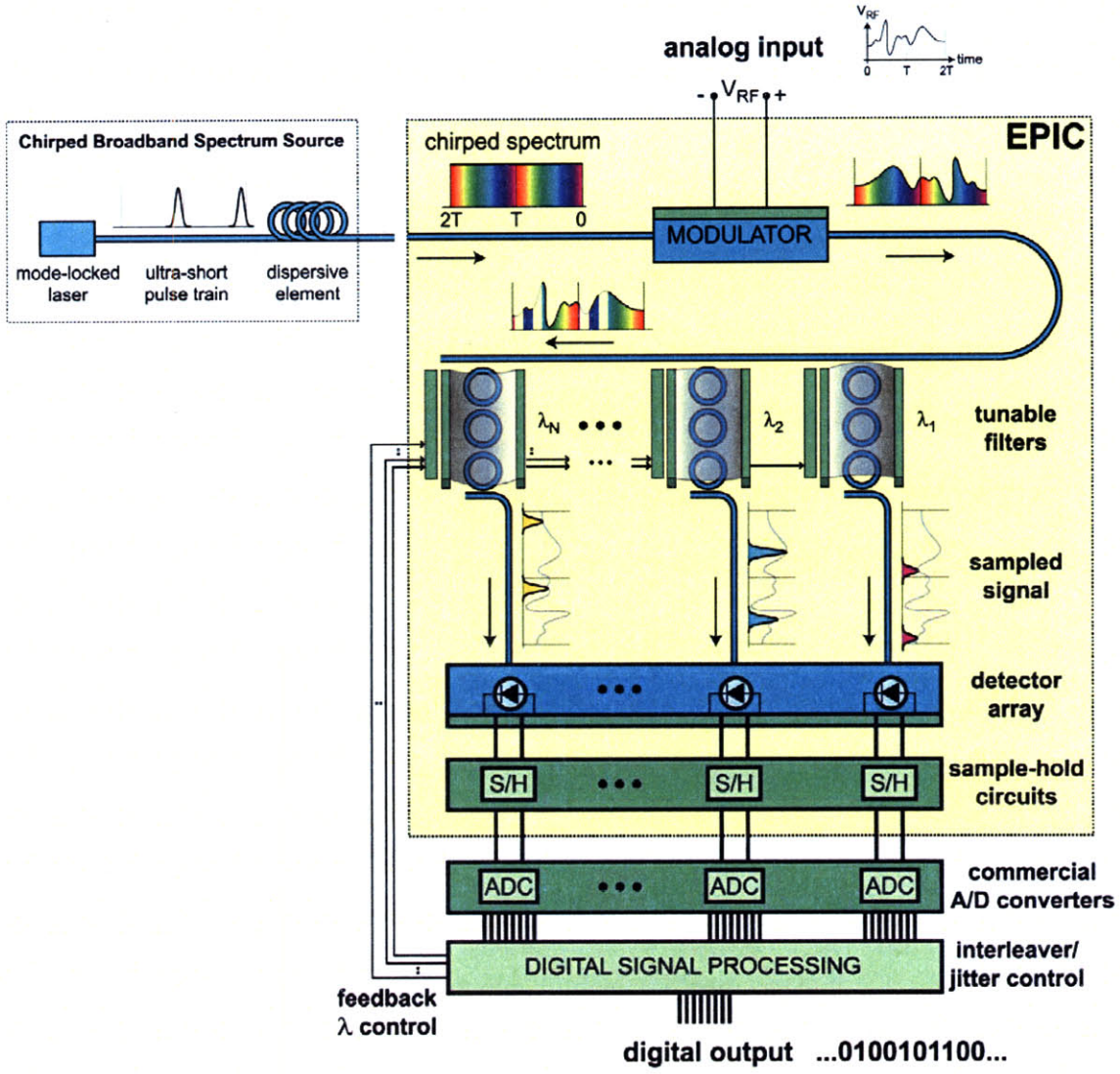
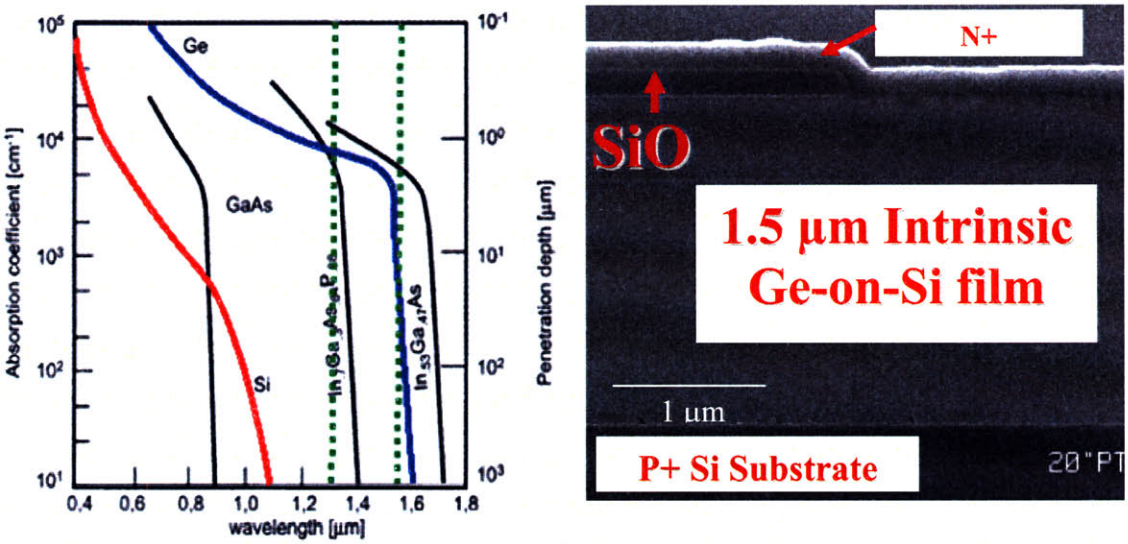


Figure 1.1 One possible architecture of a high-speed, high resolution optoelectronic ADC chip. A low-jitter femtosecond laser with repetition rates of a few GHz emits a stream of pulses that is dispersed. The RF-waveform to be sampled is imprinted on the chirped pulse stream via an electro-optic modulator. The signal is channeled with a filter bank, with each channel, which correspond to time interleaved sample sequences, separately digitized in low rate high resolution ADC's, that benefit from an on-chip Ge detector array and optically enhanced sample and hold-circuits. From Kaertner *et al,* [2].

The motivation for utilizing the near infrared wavelengths is motivated by practical concerns. The near infrared wavelengths, commonly referred to as the C and L bands, are commonly utilized for telecommunications data transmissions. Furthermore, there exists a plethora of high quality lasers available as optical sources, and there is an extremely low loss of optical signals in fibers in the wavelengths between 1.3 – 1.6 microns, Due to the transparency of silicon in the near infrared wavelength range, novel materials will have to be incorporated onto the silicon CMOS platform to serve as photodetectors. One excellent material candidate is germanium. As shown in Figure 1.2 (a), germanium has a high absorption coefficient in the wavelength ranges of interest and unlike many III-V materials, has been successfully epitaxially deposited onto the silicon substrate. In addition germanium material is already used in the semiconductor industry to create $Si_{1-x}Ge_x$ alloys that improve the mobility and/or velocity of mobile carriers. Prior approaches to depositing germanium onto the silicon substrate have used high vacuum depositions systems such as Molecular Beam Epitaxial (MBE) or Ultra High Vacuum Chemical Vapor Deposition (UHVCVD) tools [8-9]. Prior to this work there had not been a detailed study of depositing Ge-on-Si films in a low pressure deposition system had not been investigated.

In this thesis, the material, electrical, and optical characteristics of CMOS compatible germanium films deposited onto the silicon substrate in a tool that is broadly accessible to the silicon CMOS industry, such as an Applied Materials Epi Centura™ Low Pressure Chemical Vapor Deposition (LPCVD) system is

investigated. Photodiodes fabricated with these Ge-on-Si films are also investigated.



(a) (b)

Figure 1.2 (a) Plot of absorption coefficient versus wavelength for different semiconductors. The green dotted lines mark the telecom wavelengths of 1.3 and 1.55 µm. From Salib *et al*, [10]. (b) Cross section Scanning Electron Microscopy (SEM) image of an LPCVD CMOS compatible Ge-on-Si *pin* photodiode. The Ge-on-Si film was deposited in this work, in an Applied Materials Epi Centura™ LPCVD tool. SEM analysis was courtesy of Analog Devices, Inc.

1.2 Direction and Organization of Thesis

This thesis studies the feasibility of monolithically integrating near infrared wavelength photodetectors onto the silicon CMOS platform by epitaxially depositing germanium films onto the silicon substrate. In order to ensure the Ge-on-Si films deposition process is broadly accessible for industrial applications, the viability of depositing Ge-on-Si films in an LPCVD epitaxial growth system is investigated. The properties of the LPCVD Ge-on-Si films are further explored by fabricating and characterizing Ge-on-Si photodiodes. Finally,

the source of the fabricated Ge-on-Si photodiode reverse bias leakage current, a key factor for determining the power dissipation and dynamic range of photodetectors, is studied.

This thesis is organized as follows. Chapter two presents a short introduction of the theory of photodiode operation. This chapter also includes a background on the known methods of depositing germanium films onto the silicon substrate and the associated photodiode results. Chapter three is devoted to the development of Ge-on-Si deposition in an Applied Materials Epitaxial Centura™ LPCVD process. The Ge-on-Si deposition process is characterized in both blanket and selective epitaxial growth regimes with comparable results. In chapter four, the electrical and optical characteristics of Ge-on-Si photodiodes fabricated in a CMOS compatible process are presented. Chapter five focuses on analyzing the origin of the reverse bias leakage current via device measurements as well as two dimensional device simulations. In Chapter six, the major findings of this thesis are summarized and the next steps for integrating CMOS compatible Ge-on-Si photodiodes onto the Si CMOS platform are discussed.

1.3 Chapter Summary

In this chapter the motivation for developing CMOS compatible germanium on silicon (Ge-on-Si) photodiodes as an integral component of an optoelectronic Analog-to-Digital Converter (ADC) was introduced. These Ge-on-Si films can also be utilized for integrating optical interconnects, photonic integrated circuits, and near infrared cameras on the Si VLSI platform. The possible advantages of

depositing the Ge-on-Si films in an Applied Materials Epi Centura™ Low Pressure Chemical Vapor Deposition (LPCVD) tool was also briefly discussed. Finally, the goals and organization of this thesis was presented.

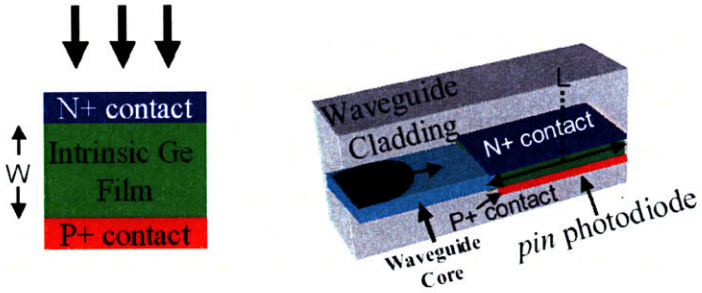
Chapter 2: Introduction to *pin* photodiode parameters and Ge-on-Si photodiodes

In this chapter some of the standard structures for *pin* photodiodes are introduced. The derivation and dependencies of major parameters of interest in *pin* photodiodes such as responsivity, reverse bias leakage current, and frequency response are also presented. Select background information on the various deposition techniques for Ge-on-Si films and measured results on vertically illuminated Ge-on-Si *pin* photodiodes over the past 15 years are summarized. This summary also provides a foundation for the following chapters and places the contributions of this thesis in context. The ADC photodetector requirements leading to the general design parameters of the LPCVD Ge-on-Si photodiode investigated in this work are also introduced.

2.1 General photodiode parameters

There are two standard architectures generally considered for *pin* photodiode integration; vertically illuminated *pin* photodiodes, and waveguide coupled *pin* photodiodes as shown in Figure 2.1. Although in the integration scheme presented in Chapter 1, waveguide coupled *pin* photodiodes will be required, in the remainder of this work, the focus will primarily be on vertically illuminated photodiodes due to ease of device fabrication and subsequent analysis. Moreover, many of the standard photodiode parameters is essentially the same for both architectures, and due to ease of analysis will be derived here

for vertically illuminated *pin* photodiode structures.



(a) (b)

Figure 2.1 (a) Schematic representation of a vertically illuminated *pin* photodiode. The optical signal and generated carriers effectively travel in parallel directions along W, the width of the intrinsic region. (b) Schematic representation of a waveguide coupled *pin* photodiode. The optical signal travels along L, the absorption length, while the generated carriers effectively travel transverse to L.

2.1.1 Responsivity

One of the most important parameters of a photodetector is the responsivity of the detector at the desired wavelength. Generally, it is desired that the photodetector responsivity is maximized in order to minimize the power requirements to reach a given bit-error-rate (BER), given by:

$$BER = \frac{N_{error}}{N_{bits}} \qquad \text{(Equation 2.1)}$$

where N_{error} is defined as the number of errors that occur in the transmission of information and N_{bits} is the number of bits that were transmitted.

In order to develop a model for the responsivity of a photodetector, the external quantum efficiency of the detector will first be calculated. The external quantum efficiency, η, can be represented as [11]:

$$\eta = (1-r)\delta\left[1-e^{-\alpha W}\right] \qquad \text{(Equation 2.2)}$$

where r represents the reflectance loss of the incoming light upon entering the photodetecting material, δ is the fraction of generated electron and hole pairs that are collected at the electrical contacts, α is the absorption coefficient of the photodetecting material, and W stands for the absorption width. In the derivation above, the contribution of back reflection from the interface of the Si and Ge layers and the Si and air boundary is assumed to be negligible. Generally, for well designed vertically illuminated *pin* diodes, W, is approximately equal to the width of the depletion region or essentially the intrinsic region. Thus, for vertically illuminated *pin* diodes, the external quantum efficiency increases as the width of the intrinsic region or the absorption coefficient increases. Furthermore, having an antireflection coating (ARC) will reduce the reflectance loss. Materials with a long recombination lifetime and high mobility also have greater collection efficiency. Reverse biasing the photodiode to create high electric fields increases the depletion distance and carrier velocity, also increasing the quantum efficiency.

The responsivity, R, is a simple rescaling of the external quantum efficiency by multiplying by units of electrical charge divided by optical power:

$$R = \eta \frac{q}{h\nu} \qquad \text{(Equation 2.3a)}$$

where R has the units of A/W and q is the electrical charge in coulombs, h is Planck's constant, and ν is optical frequency of the incoming light. The product, $h\nu$, is the optical power of one photon in watts. Since q and h are constants, and ν is inversely proportional to the wavelength, as shown in Equation 2.3b, the responsivity can also be related to the external quantum efficiency through the optical wavelength:

$$R \cong \eta \frac{\lambda}{1.24} \qquad \text{(Equation 2.3b)}$$

where λ is the optical wavelength in microns. Thus, as the wavelength of the incoming light decreases from being outside the photodiode detectable wavelength range into the detectable range, initially the responsivity increases as the quantum efficiency increases, but once the quantum efficiency saturates, the responsivity begins to decrease as a function of the wavelength of the incoming light.

2.1.2 Reverse Bias Leakage Current

The reverse bias leakage current, also known as the dark current, is the generated current from the photodiode under reverse bias with no illumination. In photodetectors, the dark current is a source of noise and contributes to the standby power consumption of the detector. Since photodetectors are typically operated under reverse bias in order to increase the responsivity and frequency response, it is generally desired to minimize the dark current. Fortunately, at high data rates above 1 Gigabits/s, the influence of the dark current on the photodetector BER becomes less significant than the photodiode capacitance [12]. Thus, when photodiodes are operated at high data rates, the leakage current primarily affects the standby power consumption of the photodetector.

There are four main sources of the reverse bias leakage current, the diffusion current component, the bulk generation component, the surface generation component, and the tunneling or emission component [13-14]. The diffusion current arises from minority carriers generated in the quasi-neutral

regions that are within a diffusion length of the photodiode junction. This diffusion current in the quasi neutral p-type region for minority electrons is given by:

$$J_{diff,n} = qD_n \frac{n_i^2}{N_A L_n}\left[\exp\left(\frac{qV}{kT}\right)-1\right] \qquad \text{(Equation 2.4)}$$

where D_n is the minority electron diffusion coefficient, N_A is the acceptor doping concentration, L_n is the minority electron diffusion length, V is the applied bias, and the remaining variables have the standard meaning. The minority hole diffusion current in the quasi neutral n type region can also be represented in a similar fashion . The diffusion current therefore increases as both the layer resistivity and minority carrier lifetime decreases. The temperature dependence of the diffusion current is primarily through the intrinsic carrier concentration n_i. The diffusion current is voltage independent and is only apparent for very high quality photodiodes under reverse biases conditions in the tens of millivolts range.

The bulk generation component in the space charge region arises due to the imperfections that exist in practically all crystal lattices. These impurity atoms and defects in the lattice result in trap levels in the semiconductor bandgap, which act as generation-recombination centers. When these trap centers are present in the depletion region, they give rise to a depletion region current that is swept out to the contacts by the high electric field in the depletion region. This generation current from the bulk depletion region can be represented by:

$$J_g = q\frac{n_i}{\tau_g}W\left[\exp\left(\frac{qV}{2kT}\right)-1\right] \qquad \text{(Equation 2.5)}$$

where τ_g is the minority carrier lifetime, and W is the width of the depletion region. The bulk generation current is greater for a shorter minority carrier lifetime and a larger substrate resistivity. The bulk generation current also scales linearly with the depletion region width, and thus increases as a function of $|V|^{1/2}$.

The surface generation current arises if the depletion region extends to the surface. In this regime, the abundant, electrically active impurities and defects that exist at the abrupt termination of the crystal lattice act as generation-recombination centers that contribute to the dark current. These defects and impurities are particularly important if the photodiode surface is not well passivated, as impurities can diffuse in over a period of time and lead to increased dark current. The surface generation current is modeled by:

$$J_{sg} = qS_0 n_i \frac{W_S L}{A}\left[\exp\left(\frac{qV}{2kT}\right) - 1\right] \qquad \text{(Equation 2.6)}$$

where S_o is the surface generation (recombination) velocity, W_S is the width of the depletion region near the surface, L is the perimeter of the photodiode active region, and A is the surface area of the photodiode. Thus, the surface generation current increases as the surface generation velocity increases, or as the density of surface states increases, and as the doping level near the surface of the diode decreases.

The tunneling or emission component of the reverse bias leakage current occurs generally when the electric field in the device is high enough that the carrier can either tunnel across or be emitted above the effective barrier between the carrier energy level and the desired energy band. Band-to-band tunneling occurs when the carrier tunnels between the valence and conduction bands of the

semiconductor. In most semiconductor materials, the onset of tunneling or emission occurs at electric field magnitudes greater than 10^4 Vcm^{-1} [15]. Such high fields typically occur first near the metallurgical junction or near an impurity or defect. The dark current is generally exponentially related to the applied bias when tunneling or emission is the dominant mechanisms. High densities of traps in the bandgap typically lowers the magnitude of electric field required for the onset of tunneling or emission to values less than 10^4 Vcm^{-1}, and also displays an exponential dependence on the bias voltage. The tunneling or emission component of the dark current generally has many parameters, but in this section will simply be modeled as being exponentially proportional to the electric field. This relationship is captured below:

$$J_{tunnel} \propto \exp(E^x) \qquad \text{(Equation 2.7)}$$

where E is the electric field magnitude and x varies between 0.5 and 1.5. The impact of tunneling on the dark current will be further discussed in Chapter 5.

2.1.3 Frequency response

The frequency response of photodetectors is determined by the total time delay of the system [11]. The total delay is the time it takes all photogenerated carriers from one light pulse to be collected by the photodetector prior to the onset of the following light pulse. If the period between light pulses is less than the total time delay, the detector will be unable to distinguish between individual bits. This time delay is composed of the transit time delay, or the time required photogenerated carriers to reach the contacts and the RC time delay.

The RC delay is related to the product of the load resistance on the circuit plus the internal resistance of the device and the capacitance of the device. The physical origin of the RC delay is that it represents the charge that must be supplied to the photodiode to maintain the required bias voltage. The bandwidth of a detector can be limited by either transit time delay and/or the RC delay, and is therefore dependent on the physical design of the photodiode.

The bandwidth due to the transit time delay can be represented as [11]:

$$F_t = \frac{0.45v}{W} \qquad \text{(Equation 2.8)}$$

where v is the electron or hole saturation velocity (and is assumed to be equal) and W is the depletion region width. Thus, the transit time is the carrier velocity divided by the transit distance, multiplied by the constant value of 0.45 to model the average depth distribution of photogenerated carriers in the depletion region. It has been demonstrated that illuminating the p-side of a *pin* photodiode results in a shorter transit time, because more holes, which have a lower mobility, are generated closer to the anode of the device and thus have a shorter distance to transverse before being collected [16]. The model above is valid under low power conditions where the photodiode has not become saturated [17]. In the saturation regime, the electric field due to the photogenerated carriers begins to screen the built-in electric field in the device, thus reducing the carrier velocity and frequency response.

In order to model the RC delay component, the photodiode is roughly approximated as a parallel plate capacitor,

$$C_{diode} = \frac{\varepsilon A}{W} \qquad \text{(Equation 2.9)}$$

where ε is the dielectric constant, A is the photodiode active region surface area, and W is the depletion region width. The bandwidth due to the RC delay is given by:

$$F_{RC} = \frac{1}{2\pi RC_{diode}} \qquad \text{(Equation 2.10)}$$

The complete frequency response of a *pin* photodiode is composed of the transit time and RC delay components and the 3-dB frequency is given by:

$$F_{3dB} = \sqrt{\left(\frac{1}{F_t^2} + \frac{1}{F_{RC}^2}\right)^{-1}} \qquad \text{(Equation 2.11)}$$

The overall frequency response is thus limited by the largest delay component, either the transit time and/or the RC delay. Generally, for well designed photodiodes, the largest delay component is the transit time delay.

2.1.4. Waveguide coupled photodiodes

A standard photodetector figure of merit, known as the bandwidth-efficiency product, illustrates an inherent performance advantage of waveguide coupled *pin* photodiodes relative to vertically illuminated *pin* photodiodes. Assuming that the bandwidth is transit-time limited, and combining Equation 2.8 and Equation 2.2 for vertically illuminated *pin* photodiodes, the bandwidth-efficiency product is obtained as:

$$Bandwidth * Efficiency \cong \frac{0.45v}{W} * (1-r)\delta\left[1 - e^{-\alpha W}\right] \qquad \text{(Equation 2.12)}$$

As shown in Equation 2.12, since the bandwidth of a well designed vertically illuminated *pin* photodiode is limited by the width of the depletion region, the photodiode bandwidth increases as the depletion width shrinks. However, efficiency, which can be represented by the photodiode responsivity, decreases as the depletion width shrinks. Thus, in well designed vertically illuminated *pin* photodiodes, to increase the bandwidth, the efficiency must decrease and to increase the efficiency, the bandwidth decreases. This is a fundamental trade-off.

One of the main advantages of waveguide coupled photodiodes is that the responsivity becomes a function of the horizontal dimension, while the bandwidth is largely a function of the vertical depletion width as shown in Figure 2.1 (b). Thus, this architecture decouples the bandwidth and efficiency, allowing simultaneous achievement of high bandwidth and high responsivity in the same device. The feasibility of waveguide coupled Ge-on-Si *pin* photodetectors will be examined in greater detail in Appendix H.

2.2 Background on monolithically-integrated near-infrared photodiodes fabricated on silicon

Numerous strategies to integrate vertically illuminated *pin* near infrared photodetectors onto the Si CMOS platform based upon $Si_{1-x}Ge_x$ alloys and $Si_{1-x}Ge_x$ heterostructures have been attempted. They can be split into two categories: the first is the use of strained, high quality $Si_{1-x}Ge_x$ alloys with Ge contents below 60% [18]. The second approach is the use of relaxed Ge-rich (> 60%) layers that take advantage of the high absorption coefficient of Ge-rich alloys and pure Ge.

In the first case, the formation of threading dislocation density is avoided by keeping the film thicknesses below the critical thickness value, but at the cost of a lowered absorption coefficient. In the second case, large absorption coefficients are obtained through Ge-rich layers and thick film thicknesses, but at the cost of higher threading dislocation densities. It has been demonstrated by Luan *et al*, that the impact of threading dislocation density primarily affects the static power dissipation from the leakage current [33]. Furthermore, at high bit rates, the noise due to the leakage current does not have as great an impact as the capacitance of a photodetector [12,19]:

$$< I_{thermal} >^2 = 8\pi V_T C_T q B^2 \qquad \text{(Equation 2.13a)}$$

$$< I_{shot} >^2 = 2qIB \qquad \text{(Equation 2.13b)}$$

where V_T is the thermal voltage, C_T is the total capacitance from the photodiode and MOSFET that typically compose a photodetector, B is the bit rate of the incoming data, q is the electrical charge in Coulombs, and I is the photodetector leakage current due to the photodiode dark current and the transistor gate leakage. Since the root-mean sauqre of the thermal noise is proportional to B and the shot noise is proportional to $B^{1/2}$, the thermal noise dominates at high frequencies. Thus, from a circuit applications perspective, lowering the effective capacitance of the photodetector becomes more important at high data rates.

One method to achieve this goal is to increase the absorption coefficient of the photodiode and thus reduce the interaction length ("W" and "L" in Figure 2.1 (a) and (b) respectively) and overall size of the photodiode, which lowers the capacitance required to reach a given photodiode responsivity. Therefore, there

has been a gradual shift in the research community towards incorporating pure germanium films onto the silicon substrate, especially in photodiodes targeted for operation at 1.55 μm wavelength.

Depositing blanket Ge-on-Si films

Over the past 15 years, many innovative approaches have been developed to deposit Ge-on-Si films, ranging from thermally evaporating polycrystalline germanium films onto the silicon substrate [20] to $Si_{1-x}Ge_x$ graded buffer layers prior to depositing the epitaxial germanium film [21]. In the following sections, a brief review of the various Ge-on-Si deposition methods will be presented.

2.2.1 Depositing blanket Ge-on-Si films: Polycrystalline Ge-on-Si photodiodes

One of the simplest methods to deposit polycrystalline Ge-on-Si films is through thermal evaporation of a germanium source onto the silicon substrate. The germanium is evaporated in a vacuum of 10^{-6} Torr, onto a silicon substrate that is kept at 300°C [20]. This method leads to polycrystalline germanium films that exhibit a similar optical absorption spectrum to monocrystalline germanium. However, the large grains of the polycrystalline germanium films lead to a high acceptor-like defect density [22]. This results in a low lifetime and short diffusion length of generated carriers in the polycrystalline film [22].

The reported responsivity values of fabricated vertically illuminated *pin* photodiodes with an intrinsic region of 0.12 μm is 5×10^{-3} A/W at a wavelength

of 1.55 microns while biased at –1 V [20]. While this responsivity is approximately 2 orders of magnitude lower than observed in monocrystalline Ge-on-Si films, these photodiodes have relatively low dark currents values of 1 mA/cm^2 [20]. A 3-dB cutoff frequency of 2.5 GHz is reported for a 200 x 200 μm^2 photodiode biased at –30 V [20].

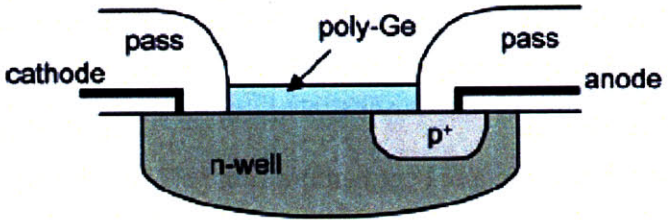


Figure 2.2 Schematic of polycrystalline Ge-on-Si photodiode. The polycrystalline germanium was deposited on top of a silicon p+/n diode by thermal evaporation at 300°C. From Masini, *et al*[20].

2.2.2 Depositing blanket Epitaxial Ge-on-Si films: Graded Buffer Ge-on-Si photodiodes

To achieve higher performance photodiodes, it is necessary to deposit single-crystal Ge films on Si. One approach to overcoming the 4% lattice mismatch between Ge and Si is to utilize the graded buffer method that is generally applied in depositing $Si_{1-x}Ge_x$ relaxed layers with low defect density [23]. In the graded buffer method demonstrated by Samavedam *et al*, high-quality Ge layers are grown on a graded $Si_{1-x}Ge_x$ buffer layer on silicon (001) substrates using an ultrahigh vacuum chemical vapor deposition (UHVCVD) tool [21]. In this approach, the $Si_{1-x}Ge_x$ graded buffer layer is grown with a germanium composition that increases at a rate of 10%Ge/micron, leading to an

approximately 10 micron thick buffer layer. Furthermore, an intermediate chemical mechanical polishing (CMP) step at the $Si_{0.5}Ge_{0.5}$ film composition was introduced. It is believed that this CMP step reduces dislocation pileups, and thus avoids the requirements of nucleating new dislocations to reduce the growing film stress. This leads to an optimized relaxation in the graded buffer, with existing threading dislocations utilized more effectively to relieve the film stress. The final dislocation density of the Ge film was measured to be approximately 2×10^6 cm^{-2}.

Photodiodes were fabricated in this Ge material with an in-situ doped mesa isolated *pin* Ge-on-Si structure shown in Figure 2.3. The intrinsic layer is approximately 0.24 μm thick in these films, partially due to persistent n-type doping from phosphine (PH_3) in the UHVCVD chamber. The reverse bias leakage current was determined to scale with the photodiode active region area and was in the range of 0.15 – 0.22 mA/cm^2. The estimated theoretical limit to the 3-dB frequency from capacitive and resistance measurements for 50 μm diameter diodes biased at –3 volts was approximately 2.4 GHz, and the external quantum efficiency was measured to be 12.6% at 1.3 μm wavelengths [21].

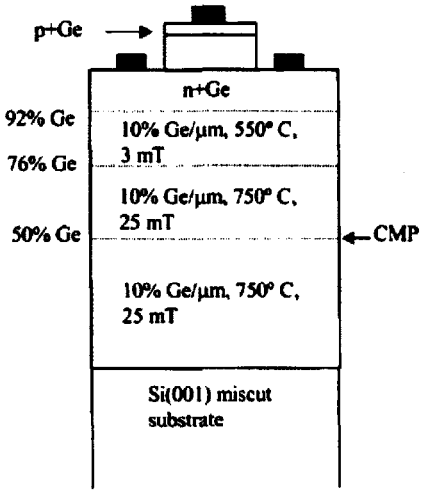


Figure 2.3 Schematic of photodiode structure fabricated on top of a graded buffer structure with a final dislocation density of ~2 x 10^6 cm^{-2}. From Samavedam, *et al* [21].

A related approach that has also been applied to Ge-on-Si film growth is to use antimony surfactant mediated graded buffer layer growth in a Molecular Beam Epitaxial system [24]. At low growth temperatures of approximately 500°C, antimony surfactant mediation helps the motion of misfit dislocations that are nucleated by the growing film stress. The enhanced movement of the misfit dislocation leads to greater annihilation of dislocations, of which there is a low number due to the low temperature growth. Using this method, the threading dislocation density is measured using a combination of plan view TEM images, cross-sectional TEM images (please see Figure 2.4), and defect etching to be approximately 5.4 x 10^5 cm^{-2}. Mesa isolated *pin* Ge-on-Si photodiodes were fabricated on a 4 μm thick $Si_{1-x}Ge_x$ graded buffer layer with a 25% Ge/μm grading rate and a 0.9 μm thick Ge top layer. The leakage current is measured to be 0.15 mA/cm^2. The internal quantum efficiency at 1.55 microns was measured

to be 70% and the 3-dB frequency from RC measurements is estimated to be 2.3 GHz for 100 x 200 μm^2 photodiodes [24]. These results are comparable to those obtained by Samavedam, *et al* using CVD-grown relaxed $Si_{1-x}Ge_x$ buffer layers.

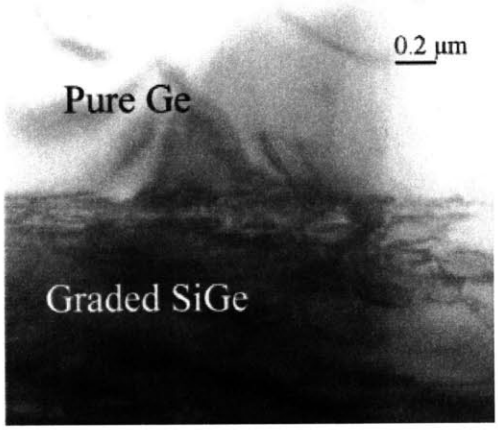


Figure 2.4 Bright field cross sectional TEM image of an antimony surfactant mediated 25% Ge/μm graded buffer layer grown by MBE. The final dislocation density of the 0.9 μm thick germanium film was ~5 x 10^5 cm^{-2}. From Liu, *et al* [24].

2.2.3 Depositing blanket Ge-on-Si films: Direct epitaxial growth of Ge-on-Si photodiodes

A final method that has been developed to deposit blanket Ge-on-Si films is a two step germanium deposition method in which a thin "seed" layer of germanium is deposited at a low temperature below 400°C, and then a thick "cap" layer of germanium is deposited at higher temperatures above 550°C. This approach has been demonstrated by several groups [8,25]. Utilizing this method of growth in UHVCVD chambers, groups have demonstrated the responsivity, dark current density, and frequency response values shown in Table 2.1. Liu *et*

al, has achieved high responsivity values of 0.56 A/W at 1.55 μm with reasonable frequency response and dark current values [26].

An innovative and related approach has been to create a complete *pin* Ge-on-Si structure at seed deposition temperatures without a dislocation anneal. Jutzi *et al*, has developed this approach in an MBE system with a growth temperature of 300 °C. As shown in Figure 2.5, at this low temperature, a 300 nm-thick p+ doped Ge layer is deposited on an intrinsic silicon layer, followed by a 300 nm-thick Ge intrinsic layer, and then capped by a 200 nm-thick n+ Ge layer. As shown in Table 2.1, the thin, unannealed intrinsic Ge-on-Si layer led to an extremely high frequency response of 39 GHz at a –2 volt bias for 10 μm diameter photodiodes, but with an associated penalty of low responsivity and high dark current [9].

The main drawback of utilizing UHVCVD or MBE systems is that these toolsets are not broadly accessible to industry, where silicon-germanium based films are commonly grown in Low Pressure Chemical Vapor Deposition (LPCVD) epitaxial growth systems. Thus, the aim of this work is to assess the feasibility of utilizing an LPCVD epitaxial growth system for depositing Ge-on-Si films by developing depositions techniques based upon the two step growth method originally developed for UHVCVD chambers.

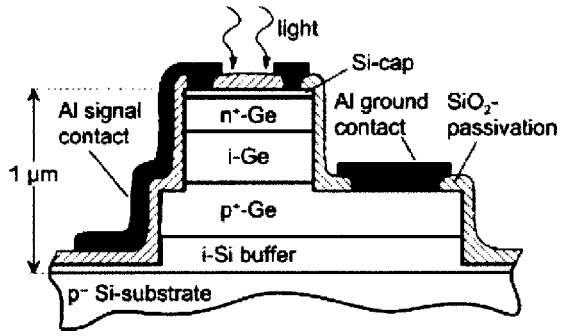


Figure 2.5 Schematic of a *pin* Ge-on-Si photodiode fabricated from direct MBE deposition of germanium onto silicon using the seed only growth method. From Jutzi, *et al* [9].

2.2.4 Depositing selective Ge-on-Si films: Direct epitaxial growth of Ge-on-Si photodiodes

In order to achieve selective epitaxial growth of germanium on silicon based on patterned silicon dioxide on silicon substrates, thermal evaporation to create polycrystalline films is not a viable option since it is not a selective process. In addition, the $Si_{1-x}Ge_x$ graded buffer layer method does not lend itself to selective deposition and to planar structures, since the thickness of the $Si_{1-x}Ge_x$ graded region tends to be on the order of several microns. On the other hand, the direct growth of Ge-on-Si is a viable option for selective germanium growth. It has been noted that germanium does not nominally deposit on SiO_2 surfaces and thus silicon dioxide is the material of choice for masking germanium growth [27].

Although there have been many publications on the growth of blanket Ge-on-Si films, there have been relatively few publications on selective Ge-on-Si films, with only one publication to date in this author's experience disclosing full

results for selective Ge-on-Si growth and device characterization [28]. Utilizing the two step growth method, selective diodes have been fabricated by Liu *et al* as shown in Figure 2.6. These devices have responsivities of 0.4 A/W at a 1.55 μm wavelength, with an intrinsic Ge layer thickness of 1.7 μm and a 3-dB frequency response of 2.5 GHz at –1 volt bias for a 20 x 100 μm^2 photodiode. The leakage of these photodiodes is also ~10 mA/cm^2. One of the aims of this work is to achieve comparable performance to or better than observed for selective UHVCVD growth in a selective LPCVD growth process.

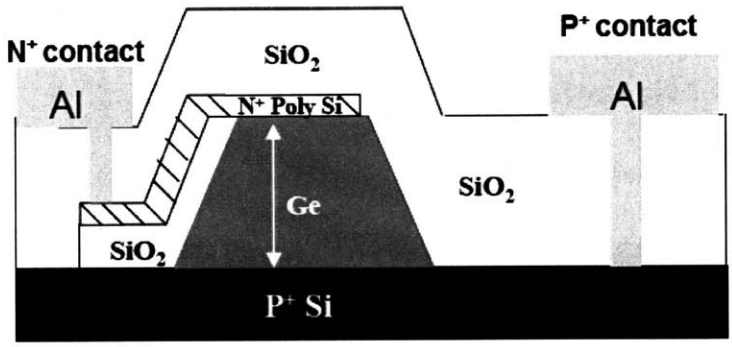


Figure 2.6 Selective photodiode structure fabricated with films deposited by the two-step epitaxial growth method. From J. Liu, *et al* [28].

Source	Deposition Method	Deposition type	Intrinsic Layer thickness (μm)	Leakage Current at -1V (mA/cm^2)	Responsivity at 1.55 μm (A/W)	3-dB Frequency (GHz)
Masini, *et al*	Thermal Evaporation	Blanket Poly	0.12	1	0.005	2.5
Samavedam, *et al*	Graded Buffer (10 μm)	Blanket Epi	0.24	0.2	<0.11	2.4
J.L. Liu, *et al*	Sb & Graded Buffer (4 μm)	Blanket Epi	0.9	**0.15**	<0.56	2.3
J.F. Liu, *et al*	2 step growth	Blanket Epi	2.35	12	**0.56**	8.5
Jutzi, *et al*	MBE growth at 300 °C	Blanket Epi	0.3	100	~0.03	**39**
J.F. Liu, *et al*	2 step growth	Selective Epi	1.7	12	0.4	2.5

Table 2.1 Summary of various Ge-on-Si deposition methods and associated results from fabricated vertically illuminated *pin* photodiodes. The best results for each parameter

2.3 Designing Optical Detectors: LPCVD Ge-on-Si *pin* photodiodes

BER	Laser Output Power (mW)	# of Photodetectors	Photodetector capacitance (pF)	3-dB Frequency (GHz)
$< 10^{-9}$	10	≥100	< 2.5	2

Table 2.2 Summary of photodetector specifications for an optoelectronic ADC targeting all-digital radar applications. From Kaertner, *et al* [29]. The combination of the Bit Error Rate and the laser output power determine the dark current requirement. Please see Table 2.3.

The initial target specifications for the vertically illuminated LPCVD Ge-on-Si *pin* photodiodes were based on vertically illuminated Ge-on-Si *pin* photodiodes results from the blanket UHVCVD 2-step growth process. The results from the UHVCVD photodiodes were evaluated relative to the performance requirements for a photodiode in an optoelectronic ADC chip as shown in Table 2.2.

In the optoelectronic ADC architecture, the major consideration for a photodiode is minimizing the BER at a given frequency while staying within the constraints of the laser output power. For Off-On-Key (OOK) transmission protocols, the BER can also be defined as the error probability, P_e, which is given by [30-31]:

$$P_e \cong \frac{\exp^{-x^2/2}}{x\sqrt{2\pi}} \qquad \text{(Equation 2.14)}$$

where x is also known as the signal to noise ratio (SNR) and is defined in Equation 2.15:

$$x = \frac{< I_1 > - < I_0 >}{\sqrt{< I_{1,shot} >^2 + < I_{thermal} >^2} + \sqrt{< I_{0,shot} >^2 + < I_{thermal} >^2}} \qquad \text{(Equation 2.15)}$$

$$< I_1 >=< I_{signal} > + < I_{dark} > \qquad \text{(Equation 2.16)}$$

$$< I_0 >=< I_{dark} > \qquad \text{(Equation 2.17)}$$

In Equations 2.15 to 2.17, $<I_{signal}>$ and $<I_{dark}>$ are the expected current for a given illumination level and photodiode responsivity, and the average dark current respectively. From Equation 2.14, the SNR must equal 6 in order for the receiver to have a BER equal to 10^{-9}. Although, generally the thermal noise is the most important consideration for optical photodetectors, the dark current from Ge-on-Si photodiodes is generally two to three orders of magnitude higher than in commercial photodetectors, hence the shot noise from the dark current must be included in the following analysis. Looking at Table 2.1, most photodiodes have intrinsic film thicknesses between 1 – 2.5 μm, thus the intrinsic photodiode capacitance calculated from Equation 2.9 will generally be less than 1.5 pF for photodiodes less than 100 x 100 μm^2 in size. Including parasitic capacitances and the transistor capacitance, the total capacitance is expected to be nominally less than 2.5 pF.

The average output power of the mode locked laser in the ADC is defined to be 10mW, which will be distributed over 100 photodetectors. Thus each photodiode will be illuminated by an average power of 100 μW when a digital one is being transmitted. A conservative value for the responsivity of 0.2 A/W is selected, leading to an $<I_{signal}>$ of 20 μA. For a frequency of 2 GHz, a thermal noise component calculated from a worst case capacitance of 2.5 pF, and using equations 2.15 – 2.17, the requirement for a SNR greater than 6 corresponds to having a dark current value equal to or less than 7.5 μA. Using Table 2.1, and

assuming an area dependent dark current, the blanket two step growth method is expected to yield photodiodes with dark currents between 0.25 – 2.5 μA for a 50 x 50 μm^2 active area, which is well within the design space for the noise level.

Assuming the 3-dB frequency response is dominated by the transit time delay, from Equation 2.8, the maximum thickness of the *pin* photodiode intrinsic region can be calculated. Thus, for a 3-dB frequency response of 2 GHz, the maximal intrinsic region thickness is expected to be 4.5 μm, where the carrier velocity is assumed to be 2 x 10^6 cm/s [32].

In order to calculate the required thickness for a responsivity of 0.2 A/W at 1.55 μm, the following parameters are assumed: an absorption coefficient of 3 x 10^3 cm^{-1} [26], a reflection coefficient of 0.4 from Fresnel's equations and Snell's law, and a collection efficiency of 100%. After entering these parameters into Equations 2.2 and 2.3 (b), the minimum Ge-on-Si film thickness to achieve a responsivity of 0.2 A/W at 1.55 μm wavelength was determined to be approximately 1.8 μm. Thus, for a vertically illuminated Ge-on-Si *pin* photodiode to sustain a BER rate of 10^{-9}, at an illumination intensity of 100 μW, and a 3-dB frequency of 2 GHz, the following parameters in Table 2.3 were targeted:

Deposition Method	Deposition Type	Photodiode Active Area (μm x μm)	Intrinsic Layer thickness (μm)	Leakage Current at -1V (μA)	Responsivity at 1.55 μm (A/W)	3-dB Frequency (GHz)
2 step growth	Blanket	50 x 50	1.8	< 7.5	> 0.2	> 2

Table 2.3 The calculated parameters for a vertically illuminated Ge-on-Si *pin* photodiode to sustain a BER of 10^{-9}, at an illumination intensity of 100 μW for a wavelength of 1.55 μm and a 3-dB frequency of 2 GHz.

2.4 Chapter Summary

In this chapter the vertically illuminated and waveguide coupled *pin* photodiodes were introduced. The derivation and dependencies of major parameters of interest in photodiodes such as responsivity, reverse bias leakage current, and frequency response are also presented. The capability for simultaneous achievement of high bandwidth and high responsivity due to the architecture of waveguide coupled photodiodes was briefly discussed. Select background information on thermally evaporated, graded buffer, and direct epitaxial growth of blanket Ge-on-Si films were outlined. The direct epitaxial growth of selective Ge-on-Si films was also presented. The advantages and disadvantages of each deposition method was evaluated via a comparison of measured results on vertically illuminated Ge-on-Si *pin* photodiodes. A detailed analysis of the ADC photodetector requirements leading to the general design parameters of the vertically illuminated LPCVD Ge-on-Si *pin* photodiodes are also introduced. The results achieved for LPCVD Ge-on-Si *pin* photodiodes will be discussed in Chapter 4.

Chapter 3: Development of LPCVD Epitaxial Blanket and Selective Ge-on-Si films

In this chapter, the Ge-on-Si deposition process is studied in an LPCVD epitaxial growth system (Applied Materials Epi Centura™). A detailed study of the impact of various growth conditions such as chamber temperature, pressure, and hydrogen flow on the germanium surface morphology of blanket and selectively deposited Ge is discussed. Basic materials properties of these films, including surface morphology and threading defect density are presented. The effect of boron doping in the seed and phosphorus doping in the blanket Ge cap layer are also presented. The impact of HCl flow during the selective Ge cap growth step is also discussed. The efficacy of various deposited and reacted germanium passivation films are briefly investigated, and the absorption coefficient of deposited Ge-on-Si films is studied.

3.1 Introduction

In this thesis, Ge photodetectors operating at 1.55 μm are of interest, and for vertically illuminated photodiodes, this requires the growth of 1 to 3 μm-thick epitaxial layers of Ge-on-Si. As discussed in Chapter 2, in Ultra High Vacuum Chemical Vapor Deposition (UHVCVD) systems, it has been demonstrated that depositing a thin, low temperature Ge layer (seed layer), followed by the deposition of a thick, high temperature layer (cap layer) with subsequent annealing can create a smooth, planar Ge film on a (100) silicon substrate with

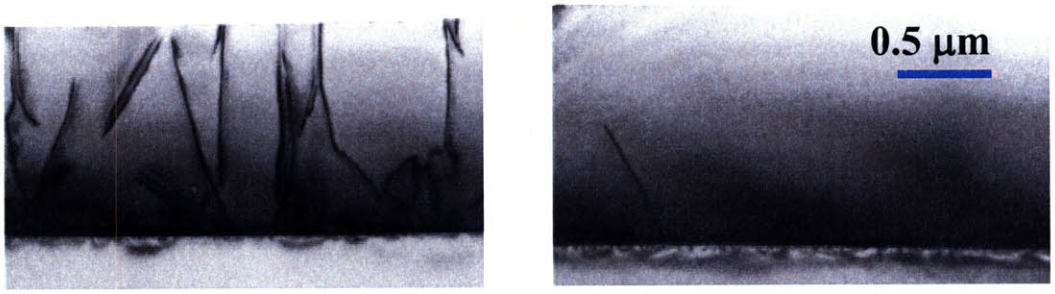
threading dislocation density on the order of 10^7 cm^{-2} [25]. Cross-section TEM micrographs of Ge films grown by this method are shown in Figure 3.1 [33]. The low temperature seed layer plastically relaxes the strain in the film while maintaining a smooth surface morphology. The deposition of the cap layer at high temperatures enhances the growth rate and also lowers the dislocation density.

3.2 Blanket Germanium on Silicon growth

The integration of Ge onto the Si substrate is difficult due to the difference in the Si lattice constant 0.543 nm and the Ge lattice constant of 0.566 nm. This corresponds to a lattice mismatch of ~4%. The larger lattice constant of Ge means that when it is deposited on a Si substrate, compressive strain is initially created in the growing Ge film. For Ge films thicker than about 2 to 3 nm, misfit and threading dislocations are formed due to the large lattice mismatch, and the strain in the film relaxes. Moreover, if the growth conditions are not optimal, three dimensional growth or islanding of the Ge film ensues when deposited on the silicon substrate [34]. A high dislocation density can degrade device performance and reliability while a high surface roughness increases the difficulty of process integration.

A two step growth process has been developed to address the tendency of Ge films to island when deposited on silicon and to lower the dislocation density. The first step is to grow a thin (~ 60 nm) Ge film at low temperatures (below 400°C) to suppress Ge surface diffusion and ensure that the Ge film does not

roughen. After depositing the thin "seed" layer, the second step is to deposit a thick "cap" layer at temperatures above 550°C. Finally, after deposition of the Ge-on-Si film is complete, a dislocation anneal is performed to lower the dislocation density from ~10^9 cm^{-2} to less than 10^8 cm^{-2}.



(a) (b)

Figure 3.1 (a) As deposited Ge-on-Si film using the two step growth process in a UHVCVD tool. Dislocation density is ~10^9 cm^{-2} (b) Ge-on-Si film after cyclic annealing between 780°C and 900°C. Dislocation density is ~2 x 10^7 cm^{-2}. From Luan, *et al* [33].

3.2.1 Experimental Procedure

Prior to the start of this work, a process for growing high quality, smooth Ge on Si in the Applied Materials Epi Centura™ system had not been developed. Thus, the first experiments were designed to find a temperature and pressure process window for seed and cap layer growths that suppresses the tendency for islanding, using a low pressure CVD process. The growth parameters examined were temperature, pressure, and seed thickness. Six inch P-type Czochralski Si (100) substrates with resistivities between 0.005 – 0.02 Ω-cm were used in this study.

The wafers were cleaned in a standard RCA clean process with an additional HF dip, DI water rinse, and spin-rinse dry step at the end. After

loading the wafers into the LPCVD chamber, the remaining surface oxide is removed with a short 30 second bake in H_2 at 1080°C. The chamber hydrogen flow rate was varied between 10 - 30 standard liters per minute (slpm) during the seed growth and fixed at 30 slpm during the cap growth. Germane (GeH_4) diluted in 30% H_2 is used as the Ge source.

3.2.2 Effect of chamber pressure, temperature variation, and hydrogen flow on seed layer morphology

In the seed layer experiment, the hydrogen flow was fixed at 30 slpm, the chamber pressure was varied from 15 to 60 Torr (2 to 8 kPa), while the growth temperature was varied from 320 to 375°C. The film thickness grown in this experiment was roughly in the range of 75 – 200 nm. Under these conditions, the seed growth rate is surface reaction rate limited, with an activation energy of 1.08 eV as shown in Figure 3.3.

Atomic force microscopy (AFM) micrographs of the Ge films are shown in Figure 3.2. At growth pressures of 15 Torr, crystallographic pits parallel to the <110> direction are observed on the seed surface. This phenomenon appears to be associated with a slow growth rate. At 60 Torr, large, irregular features in the AFM scans were observed. These features may be associated with gas phase nucleation due to the high partial pressure of GeH_4 in the chamber. A chamber

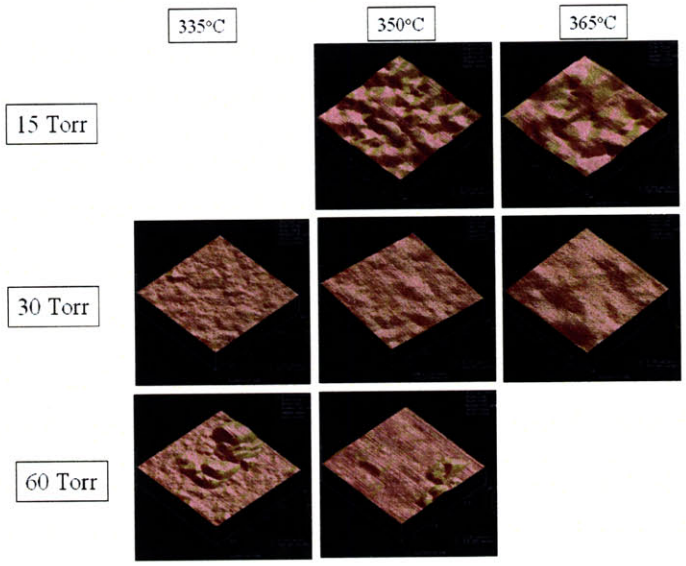


Figure 3.2 1 μm x 1 μm AFM scans of Ge seed layers (75 – 200 nm-thick) grown at various pressures and temperatures. As pressure increases, growth rate increases, but gas phase nucleation (bottom panels) becomes an issue. At high temperatures, surface roughness increases due to higher Ge mobility. Optimum seed growth conditions are 335°C at 30 T. AFM measurements are courtesy of David Danielson.

pressure of 30 Torr seems to avoid both the large irregular features observed at 60 Torr as well as the rough surfaces observed at 15 Torr.

When the Ge seed growth temperature was studied, it was found that for temperatures above 350°C, the surface begins to roughen, with the AFM RMS roughness values doubling between 350°C and 365°C. This roughening may be associated with rapid surface diffusion of Ge atoms at these elevated temperatures. The optimal condition for minimizing the seed surface roughness, as determined by atomic force microscopy, (RMS of ~1 nm for a 60 nm-thick seed) while sustaining a high growth rate (2 nm/min) was found to be 335°C at 30 Torr. A process window that maintains an RMS roughness ≤ 3 nm for 60 nm-

thick seed layers and has a growth rate of ≥ 1 nm/min was found to be 335°C ± 15°C and 30 Torr ± 10 Torr. The use of growth temperatures below 350°C suppresses Ge surface diffusion, creating films with less than half the RMS roughness of 4.1 nm achieved at 400°C in other work [35]. The use of higher growth pressure also compensates for the low growth rates associated with growth temperatures less than 350°C.

In the literature concerning germanium growth, it has been shown that lowering the surface diffusion of Ge atoms at 330 °C is probably the key parameter to explain the hindrance to the 2D–3D transition [36]. Reducing the growth temperature exponentially reduces the surface diffusion of Ge, but the hydrogen coverage coming from the germane decomposition is probably another major factor in avoiding three dimensional growth. It was indeed previously shown from MBE experiments that an atomic hydrogen flow can prevent the three dimensional growth mode of Ge-on-Si films [37-39]. These studies have demonstrated that a low temperature is not the only requirement to avoid the 2D–3D transition, but the combination of low temperature with the presence of hydrogen is needed [36].

Recently, experiments have been conducted under a slightly different range of films thickness and growth conditions [40]. Specifically, the effect of lower H_2 flows on the initial stages of Ge-on-Si growth is under investigation by Meekyung Kim. Recent results indicate that 60 nm-thick Ge seed films at 365 °C, 60 Torr have been grown that have an RMS surface roughness of 0.6 - 0.7 nm, almost a factor of 2x smoother than the 335°C, 30 Torr setpoint determined in the earlier

seed growth experiments discussed above. These results are still in the preliminary stage and experiments by Meekyung Kim are ongoing. Thus, unless otherwise stated, the Ge seed layers studied in this thesis were grown at 335°C, 30 Torr, with a hydrogen flow of 30 slpm.

3.2.3 Effect of chamber pressure, temperature variation on cap layer morphology

In the Ge cap layer experiment, the growth temperature was varied from 575 to 700°C at 30 Torr, and the chamber pressure was varied from 30 to 90 Torr at 650°C. The Ge film thicknesses grown in this experiment were in the range of 0.4 to 1.1 μm. At a growth temperature of 575°C, the Ge film developed pyramidal defects with an RMS roughness greater than 10 nm, but for temperatures from 600 to 700°C, the Ge film is smooth with an RMS roughness of less than 1 nm (see Figure 3.8 (b)).

In this temperature range, the growth rate is mass transport limited. Thus, there is a moderate dependence of the growth rate on the deposition temperature, but a strong dependence on the chamber pressure as shown in Figure 3.3. The measured RMS surface roughness appears to be independent of pressure and temperature within this range and was measured by AFM to be 0.4 ± 0.1 nm. There are also no irregular features (observed during seed layer growth at higher chamber pressures) under these growth conditions. Given these results, a growth condition of 700°C, 30 Torr was selected as the standard cap growth setting for depositing Ge-on-Si films.

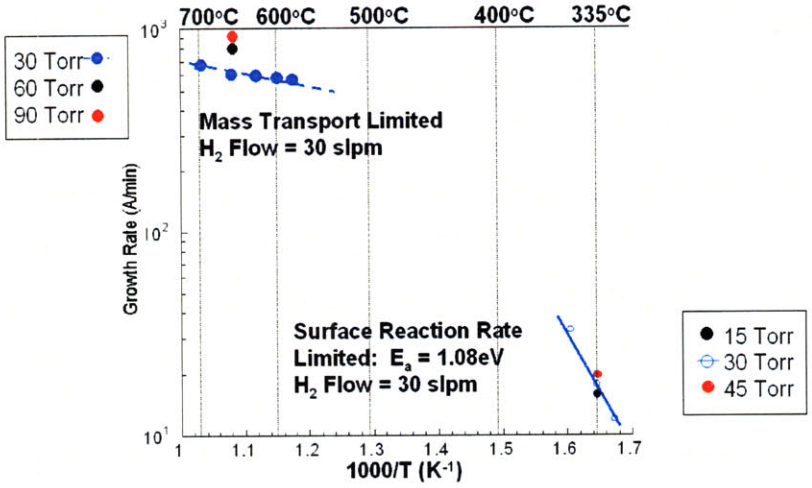


Figure 3.3 LPCVD Ge growth rates: Below 375°C, the Ge growth is surface reaction rate limited with an activation energy of 1.08 eV. Above 575°C, the Ge growth is mass transport limited, and increasing the growth pressure appreciably increases the Ge growth rate. Film thicknesses were measured by RBS, courtesy of Cait Ni Chleirigh.

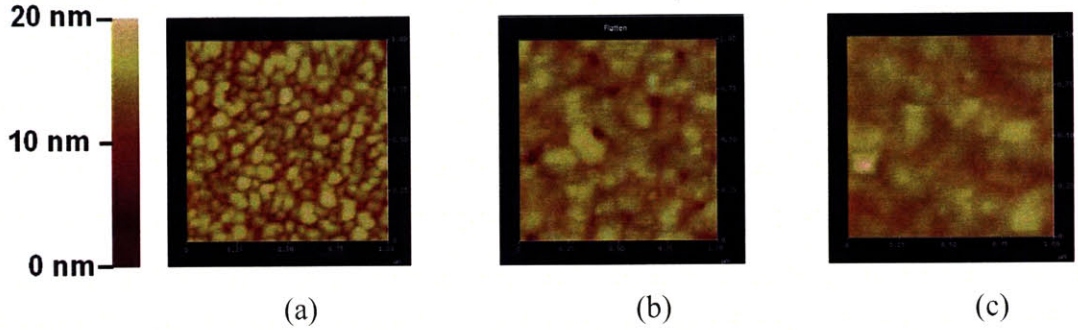


Figure 3.4 1 μm x 1 μm AFM scans showing the evolution of the Ge seed surface as a function of layer thickness at 335°C, 30 Torr, with 30 slpm of H_2 flow. (a) After 960 seconds of deposition (30 nm-thick seed), Ge islands are evident, with numerous pits between islands. (b) After 1920 seconds of deposition (60 nm-thick seed), the Ge islands are coalescing and the number of pits decreases due to preferential Ge adsorption to these sites. (c) After 3000 seconds of deposition (95 nm-thick seed), the Ge islands have fully coalesced and pits are no longer evident. AFM measurements are courtesy of David Danielson.

3.2.4 Qualitative growth model for seed layer

A qualitative growth model for the LPCVD Ge seed layer growth at 335°C, 30 Torr has been developed. As shown in Figure 3.4, it appears that in the first few monolayers of the Ge seed growth, the Ge film grows in a three dimensional mode [41]. The three dimensional growth is driven by the ~4% lattice mismatch between the Si and Ge lattices. After the first few layers of

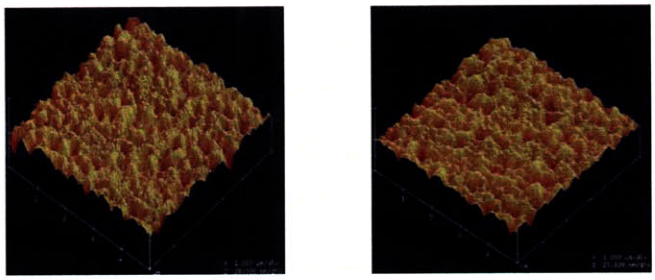
growth, the Ge layers have largely relaxed, and the Ge islands that have nucleated on the silicon substrate begin to coalesce. As the islands coalesce, a surface energy driven reaction to maximize the number of satisfied bonds for the Ge atoms leads to atoms preferentially adsorbing at "pits" formed at the boundary of coalescing Ge islands [42]. Thus, as the films become thicker, the overall Ge surface becomes smoother.

3.2.5 Effect of a temperature ramp layer on film morphology

The effect of having a temperature-ramp layer deposited during the temperature transition between the seed layer and the cap layer was also studied. Depositing this ramp layer by flowing GeH_4 in the epitaxial growth chamber during the temperature transition yields a slightly lower surface roughness of 1.9 nm compared to the RMS value of 2.2 nm measured for temperature ramps without GeH_4 flow. This is shown in the AFM micrographs in Figure 3.5.

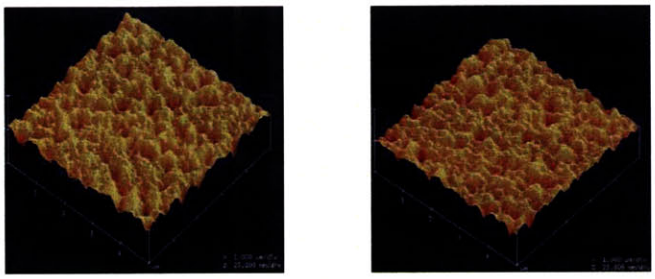
The effect of the temperature ramp time during the transition from the seed layer to the cap layer was also examined. As shown in Figure 3.6, it was found that for a 60 nm-thick seed, there was little effect on the surface roughness when the ramp time was varied between 30 and 295 seconds.

In summary, the deposition of germanium during the temperature transition, as opposed to annealing, was found to only slightly improve the Ge film surface roughness.



(a) (b)

Figure 3.5 5 μm x 5 μm AFM scans for 60 nm-thick seeds with varying GeH_4 flow in a 30 second temperature ramp transition:
(a) No GeH_4 flow during the ramp: RMS of 2.2 nm
(b) 100 sccms of GeH_4 during the ramp: RMS of 1.9 nm.
AFM measurements are courtesy of David Danielson.



(a) (b)

Figure 3.6 5 μm x 5 μm AFM scans for 60 nm-thick seeds after a temperature ramp transition to the cap (GeH_4 is flowing):
(a) A 295 second ramp: RMS of 2.1 nm.
(b) A 30 second ramp: RMS of 1.9 nm.
AFM measurements are courtesy of David Danielson.

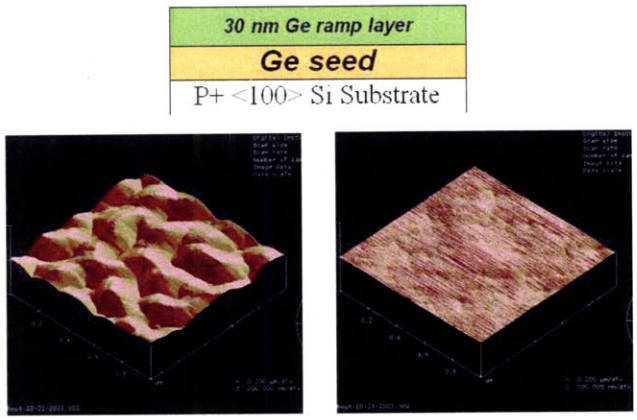
3.2.6 Effect of initial seed layer thickness on Ge film morphology

The effect of the initial seed thickness on the surface roughness after a temperature ramp transition was found to be significant. The ramp time for the transition between 335°C and 650°C was set at 295 seconds, and two Ge films, with initial seed layer thicknesses of 30 and 60 nm respectively, were heated to the cap temperature. The results are shown in the AFM micrographs in Figure

3.7. For the Ge film with an initial 30 nm-thick seed, there was an increase in the RMS surface roughness of ~10x (1.5 to 14.7 nm), while the Ge film with the initial 60 nm-thick seed had a slight increase in RMS roughness of 1.8x (1.2 to 2.1 nm). It is hypothesized that at or below a 30 nm seed thickness, the Ge islands have not fully coalesced, and thus have a stronger tendency to form islanded surfaces during the transition to the cap deposition temperature.

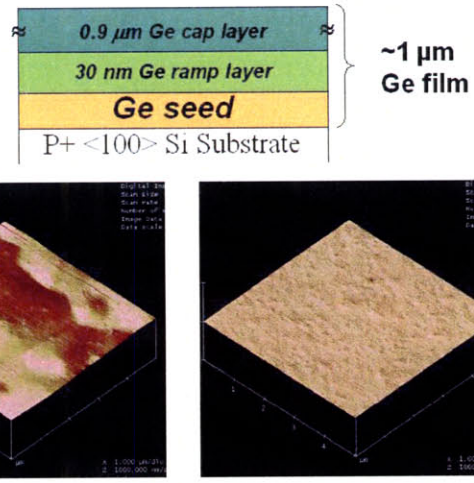
There is still a significant difference in surface roughness for a Ge film with an initial 30 nm-thick seed, (henceforth termed Ge film 1) and a Ge film with an initial 60 nm-thick seed (henceforth termed Ge film 2) which is apparent after depositing a 0.9 um-thick Ge cap layer at 650°C. Essentially, as shown in Figure 3.8 (a), Ge film 1 continues to roughen after the temperature ramp, with a final RMS surface roughness of 29 nm, an increase of 2x with respect to the after ramp roughness shown in Figure 3.7 (a). On the other hand, the RMS surface roughness of Ge film 2 decreases by ~2x after the ramp, to 0.9 nm. This leads to a 30x decrease in surface roughness for Ge film 2 relative to Ge film 1 for approximately the same overall film thickness. A sufficiently thick seed layer (e.g. 60 nm) is thus required to obtain smooth overall Ge surface morphology.

It has also been demonstrated that a sufficiently thick Ge seed layer (>75 nm) can survive the temperature ramp step without the need for an intermediate Ge ramp layer. The seed roughness increases from approximately 0.9 nm prior to the ramp to 1.8 nm after the temperature ramp layer for a 90 nm thick Ge seed layer without an intermediate Ge ramp layer.



(a) (b)

Figure 3.7 5 μm x 5 μm AFM scans of Ge films after temperature-ramp deposition with Ge seed thicknesses of (a) 30 nm (RMS of 14.7 nm), and (b) 60 nm (RMS of 2.1 nm). 60 nm-thick seed survives the temperature ramp without significant islanding. AFM measurements are courtesy of David Danielson.



(a) (b)

Figure 3.8 5 μm x 5 μm AFM scans of Ge films after cap deposition with initial seed thicknesses of (a) 30 nm (RMS of 29 nm), and (b) 60 nm (RMS of 0.9 nm). 60 nm-thick seed yields a much smoother overall Ge film. AFM measurements are courtesy of David Danielson.

3.2.7 Boron doping effect on seed growth

For the fabrication of vertical pin Ge-on-Si photodiodes, it was expected that it would be advantageous to dope the Ge seed layer to be p-type. This doping was introduced to remove the highly defected Ge seed layer from the photodiode

depletion region. Boron doping of the Ge seed layer using diborane (B_2H_6) during growth was thus investigated.

For low temperature epitaxy, the germanium growth rate was found to be significantly increased by boron doping on the order of 10^{19} cm^{-3}. The increase in the germanium seed growth rate has been observed to scale linearly for boron doping levels up to 10^{20} cm^{-3}. This trend is captured in Figure 3.9. The source of the increase in Ge growth rate with high levels of boron doping is theorized to be similar to the lattice contraction associated with high levels of boron doping in Si and $Si_{1-x}Ge_x$ films [43-44]. A decrease in the lattice constant of Ge will lower the lattice mismatch with the silicon substrate and reduces the activation energy for germanium atoms to adsorb onto the silicon substrate, increasing the initial growth rate of the Ge seed.

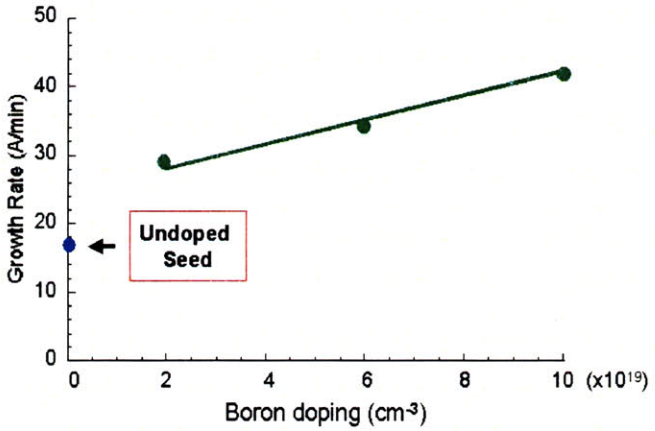


Figure 3.9 Effect of Boron doping on seed growth rate. The diborane (B_2H_6) flow was between 75 – 300 sccms. Above $10^{19}cm^{-3}$ doping levels, the seed growth rate is increased by boron. Between 10^{19} – 10^{20} cm^{-3} boron doping levels the seed growth rate is linearly proportional to the boron doping. RBS measurements are courtesy of Cait Ni Chleirigh.

To verify the existence of the Ge lattice contraction with high boron doping, two 6" P+ (100) Czchoralski wafers with 86 nm-thick Ge seed layers

were deposited at 335°C, 30 Torr. One wafer was a Ge seed with a 5 x 10^{19} cm^{-3} boron doping and the other wafer was an intrinsic Ge seed without boron doping. X-ray diffraction (XRD) θ/2θ scans were performed around the symmetric 004 reflection, and glancing-incident asymmetric 224 reflections were performed by Meekyung Kim using a Bede D3 diffractometer. The diffraction curves were interpreted using the RADS simulation program based on the dynamical diffraction theory [45]. Using the 004 and 224 data, both the out of plane and in plane lattice constants of the Ge seeds were estimated. Both Ge seeds appears to have an out of plane lattice constant of 0.563 nm, but as suggested in Figure 3.10, the boron doped Ge seed layer appears to have a slightly lower in plane lattice constant of 0.561 nm relative to the 0.562 nm in plane lattice constant of the undoped Ge seed layer.

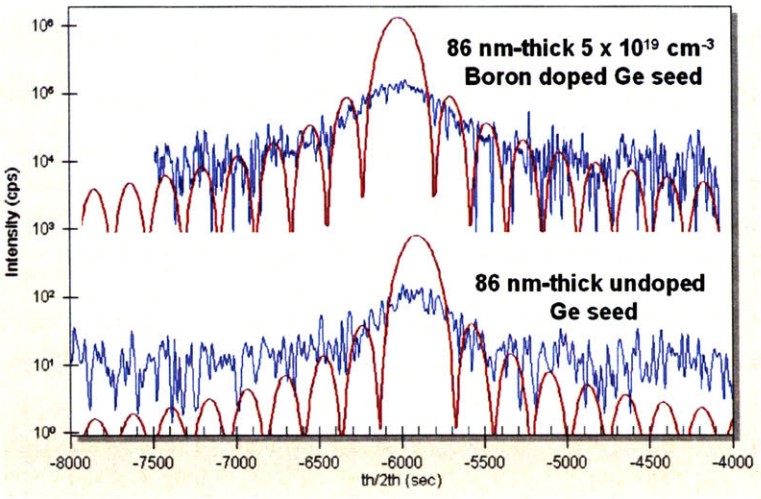


Figure 3.10 XRD analysis of 86 nm-thick doped and undoped Ge seed layers (blue line) in the 004 reflection scan. The RADS simulation fit to the data is overlaid in solid red. This data does not reproduce the fringes predicted by the simulations due to the high threading dislocation density (~10^{9} cm^{-2}) of the Ge seeds. The relaxation for the 86 nm-thick undoped seed layer in the bottom scan is 85.5%, while the relaxation for the 86 nm-thick 5 x 10^{19} cm^{-3} boron doped Ge seed layer is 83%. The corresponding in-plane lattice constants for the undoped and doped seeds extracted from the best simulation fit are 0.562 nm and 0.561 nm respectively. The out-of-plane lattice constant derived from asymmetric 224 reflection measurements was 0.563 nm for both Ge seed layers. XRD measurements and analysis are courtesy of Meekung Kim.

The increase in the seed growth rate with high boron doping is associated with a decrease in the oxygen that is incorporated at the Ge/Si heterointerface. Secondary Ion Mass Spectrometry (SIMS) plots of this phenomenon is shown in Figure 3.11. This effect is hypothesized to be due to a shorter growth time until complete germanium coverage of the silicon substrate is achieved. Oxygen has been observed at the Ge/Si heterointerface and is below the SIMS detection limit in the bulk region of the Ge films grown in this work. It is interesting to note that in RPCVD growth, no effect of boron doping has been seen on the growth rate of the Ge seed layer [46].

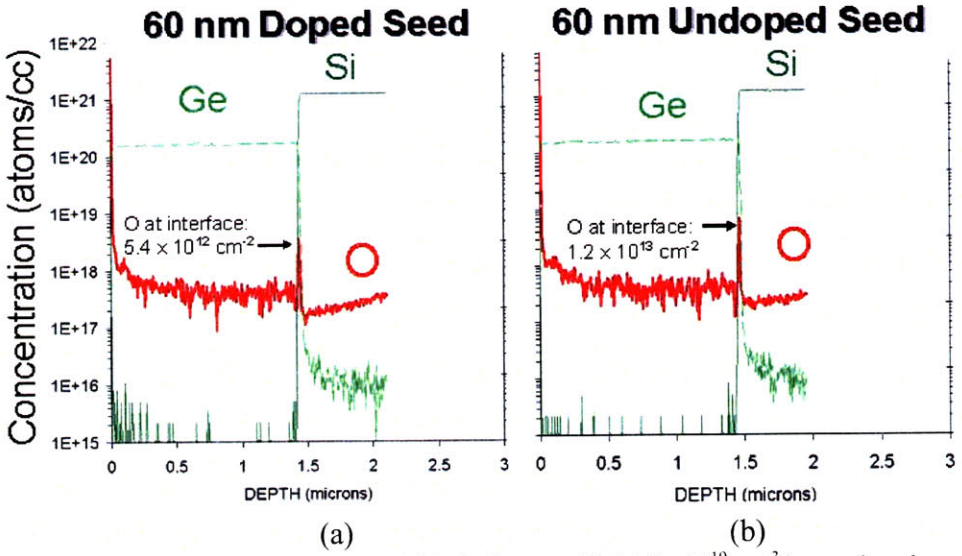


Figure 3.11 SIMS profiles of 1.5 μm-thick Ge layers with (a) 2 x 10^{19} cm^{-3} boron doped seed layer and (b) undoped seed layer. The 60% increase in growth rate for this boron doping level leads to a lower oxygen content at the Ge/Si heterointerface. In the bulk of the Ge film, the oxygen signal is below the SIMS detection limit.

3.2.8 Phosphorus doping in the germanium cap growth

For certain *pin* photodiode configurations, in-situ growth of an n-type Ge region is desirable. Thus, several samples were used to investigate phosphorus doping of Ge utilizing phosphine (PH_3) gas during epitaxial growth. In the literature, in-situ phosphorus doping levels above 10^{18} cm^{-3} have not been demonstrated in germanium films. This poor phosphorus incorporation efficiency is explained by surface segregation of phosphorus in the growing Ge film, similarly to what occurs for P-doped Si and $Si_{1-x}Ge_x$ [47-48]. Indeed for Reduced Pressure Chemical Vapor Deposition methods at 850°C, it was found that the phosphorus doping fluctuated between $1x10^{17}$ to $4x10^{17}$ cm^{-3}, independent of the phosphine flow (PH_3) [46]. In the RPCVD growth, the phosphorus doping did not affect the cap growth rate as might be expected for a surface segregation process, and there was no retardation of the growth rate as seen when phosphorus doping is introduced for $Si_{1-x}Ge_x$ films [46].

In the present work, the cap growth was conducted at 650°C, at a pressure of 30 Torr, and a hydrogen flow of 30 slpm on six inch p-type (Boron doped) Czchoralski wafers. The phosphorus doping was from a phosphine (PH_3) source with the flow range of interest being between 0 – 300 sccms. Under these conditions, the undoped Ge cap growth rate was ~60 nm/min. The thickness of the doped Ge cap layers was determined by spectroscopic ellipsometry and the resistivity of the film by a four point probe measurement. Hence, only the electrically active carriers were extracted from these measurements. The extracted doping levels ranged from $1 \times 10^{17} cm^{-3}$ to $8 \times 10^{18} cm^{-3}$.

As demonstrated in Figure 3.12, there is an almost linear increase in the number of electrically active phosphorus atoms as the phosphine flow is increased from 2 to 300 standard cubic centimeters per minute (sccms). The phosphine flow also did not have an appreciable affect on the Ge cap growth rate, which stayed a constant value of ~60 nm/min, throughout the entire range of phosphine flow. Moreover, as shown in Figure 3.13, the surface roughness of the Ge cap layer was not impacted by the incorporation of phosphorus, remaining in a tight range between 0.65 – 0.7 nm throughout the entire range of phosphine flow. It is hypothesized, that relative to prior published results, a higher growth rate and a lower Ge cap deposition temperature might have led to the lower segregation of the phosphorus atoms to the growing Ge surface, leading to the order of magnitude increase in the n-type doping that has been demonstrated for these Ge films.

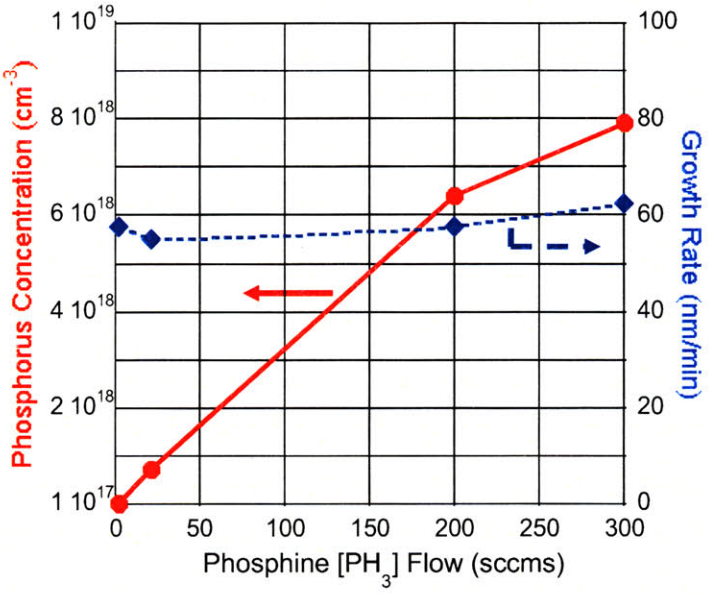
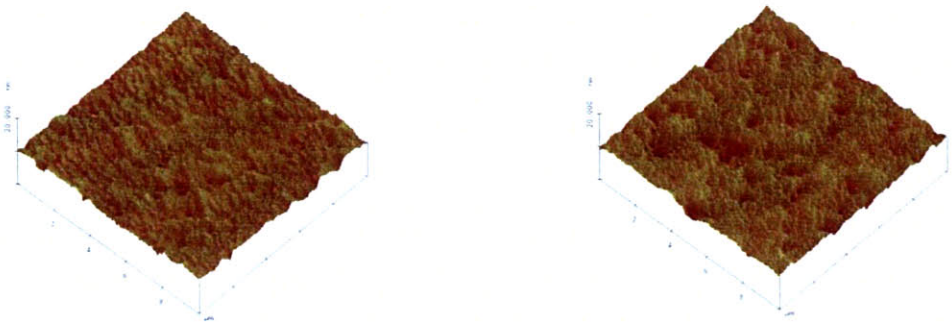


Figure 3.12 A plot of the electrically active phosphorus concentration (solid red) in the germanium cap layer as a function of phosphine flow. The phosphorus concentration is extracted from spectroscopic ellipsometry thickness measurements and four point probe resistivity measurements. The active phosphorus concentration is almost a linear function of the phosphine flow. The growth rate (dashed blue) of the germanium cap layer stays essentially constant at ~ 60 nm/min as a function of the phosphine flow.



(a) (b)

Figure 3.13 10 μm x 10 μm AFM scans of phosphorus doped ~0.24 μm-thick Ge cap films. (a) RMS roughness of 0.65 nm with an extracted doping level of $1x10^{17}cm^{-3}$. (b) RMS roughness of 0.7 nm with an extracted doping level of $8x10^{18}cm^{-3}$. There is essentially no effect of the phosphorus doping on the surface roughness of the germanium films in the doping range studied. AFM measurements are courtesy of Meekyung Kim.

3.2.9 Material characterization of blanket Ge-on-Si films

Low resolution XRD scans of the blanket Ge film were performed around the 004 symmetric reflection angle. As evident in Figure 3.14, there is only one peak for the Ge and Si films for the 2θ scan, indicating the Ge film is single crystal.

Ge films were grown to a thickness of 1 to 2 μm, under the preferred growth conditions determined in Section 3.2.2 and Section 3.2.3. These samples were annealed at 900°C for 30 minutes, and the dislocation density of the Ge films was estimated by Etch Pit Density (EPD) measurements. The EPD solution and analysis procedure is outlined in Appendix B, and to ensure that at least 0.5 microns of Ge was etched to ensure defect delineation, the etch depths were measured by a surface profilometer (Dektak) in the Exploratory Materials Laboratory (EML). Nomarski micrographs of defect etched 2 μm-thick Ge-on-Si films annealed at 900°C for 30 minutes are shown in Figure 3.15. The annealed films were found to have a threading dislocation density of ~2×10^7 cm^{-2}. Prior to annealing the films have a threading dislocation density higher than 10^8 cm^{-2} Upon annealing, as displayed in Figure 3.16, it was found that the RMS roughness

of 2 μm Ge-on-Si films increased from 0.6 nm to 1.6 nm. These dislocation densities and surface roughness results are comparable to those obtained using the UHVCVD growth process, and the Reduced Pressure CVD high temperature (850°C) growth of Ge films without annealing [25, 35, 49].

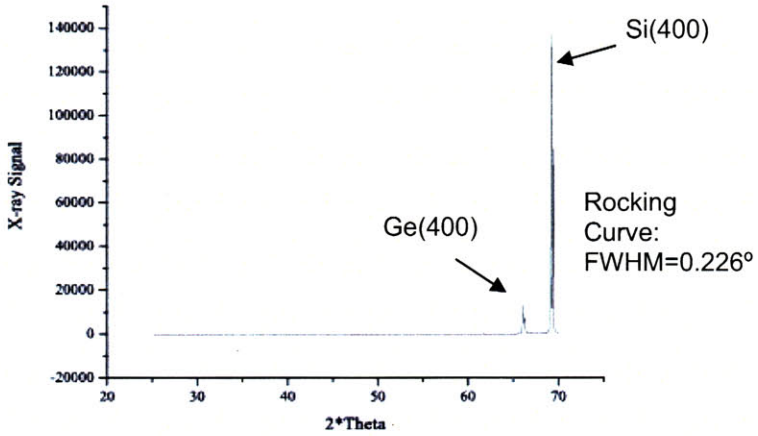
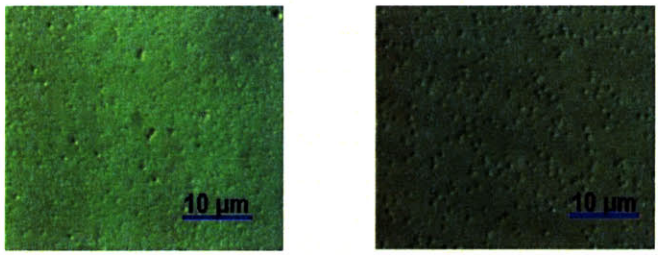


Figure 3.14 XRD analysis of a ~0.5 μm-thick Ge-on-Si film at a 004 symmetric reflection angle. There is only one peak for the Ge and Si films for the 2θ scan, indicating the Ge film is epitaxial. XRD measurement courtesy of David Danielson.

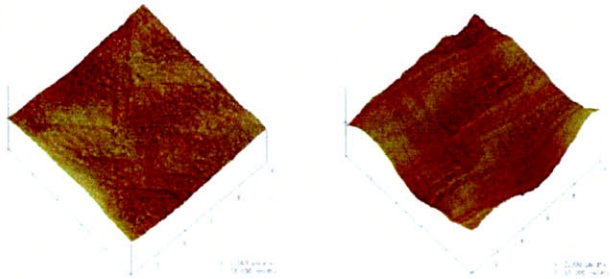


(a) (b)

Figure 3.15 Nomarski micrographs of *in-situ* annealed Ge films etched in an Iodine-based defect etch solution. *In-situ* anneals at: (Measurements are courtesy of David Danielson)

(a) 850°C for 30 minutes for a 1 μm-thick film yields a dislocation density of ~ 5 x 10^7 cm^{-2};

(b) 900°C for 30 minutes for a 2 μm-thick film yields a dislocation density of ~ 2 x 10^7 cm^{-2}.



(a) (b)

Figure 3.16 10 μm x 10 μm AFM scans of 2μm-thick Ge films (a) as grown (RMS of 0.6 nm), and (b) post anneal (RMS of 1.6 nm). AFM measurements are courtesy of Meekyung Kim.

3.3 Selective Epitaxial Growth (SEG) of Germanium on Silicon

[1] Although the majority of the devices fabricated in this work utilized blanket Ge films, there is interest in the use of selective deposition of Ge in oxide-patterned windows. The SEG epitaxial experiments were designed to suppress germanium nucleation on the oxide field regions of the mask pattern. With the mask pattern used, approximately 1% of the wafer surface was exposed Si for epitaxial growth. The growth parameters examined were the effect of HCl flow, deposition temperature, and chamber pressure.

Six inch p-type Czochralski Si (100) substrates are used in this study with ~1 μm-thick patterned thermal and DCVD oxide films as shown in Figure 3.17. The wafers were cleaned in an RCA clean process with an additional HF dip, DI water rinse, and spin-rinse dry step at the end. After loading the wafers into the LPCVD chamber, residual contaminants were removed with a short 5 minute bake in H_2 at

[1] The author would like to acknowledge the extensive measurement assistance of Meekyung Kim in the SEG study.

900°C. GeH_4 diluted at 30% in H_2 was used as the Ge source. The presence of germanium nucleation on the oxide surface was verified with a Nomarski microscope at a visual magnification of 110 - 1100x as demonstrated in Figure 3.18.

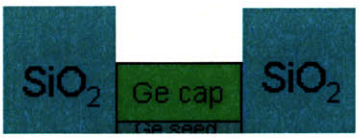


Figure 3.17 Schematic of the structure of SEG wafers. SiO_2 sidewalls were ~1um deep. 99% of the wafer surface was covered by SiO_2.

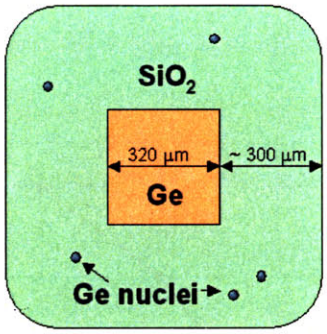


Figure 3.18 The field nucleation was counted around 320 μm square trench, by visually counting the numbers using a Nomarski microscope at a magnitude of 440x. Six to ten regions were scanned to get statistics. This method gives only a rough estimate with nucleation density varying by up to 100% depending on the location. Schematic illustration courtesy of Meekyung Kim.

3.3.1. SEG growth development of Ge-on-Si

The nominal Ge-on-Si deposition process developed for Blanket Ge-on-Si was utilized for SEG deposition. There was a ~5x increase in the germanium cap growth rate relative to the blanket epitaxial growth, due to a macroscopic loading effect for the 1% exposed Si surface area. At the growth pressure of 30 Torr,

there was also a microscopic loading effect as a function of trench widths, with a 1.6x increase in the deposition rate for 70 x 70 um^2 exposed silicon window relative to 320 x 320 um^2 exposed window, as shown in Figure 3.19. When the pressure is reduced to 10 Torr, the microscopic loading effect is reduced to ~7% for a 70 x 70 um^2 exposed window relative to a 320 x 320 um^2 exposed window. The reduction in the microscopic loading effect as the pressure is lowered is the expected result from prior Si SEG growth studies [50]. Moreover, it was noted that although the process in nominally selective, there is noticeable germanium nucleation on the oxide (on the order of 10^5 nuclei/cm^2) for germanium growth at 650°C, 30 Torr.

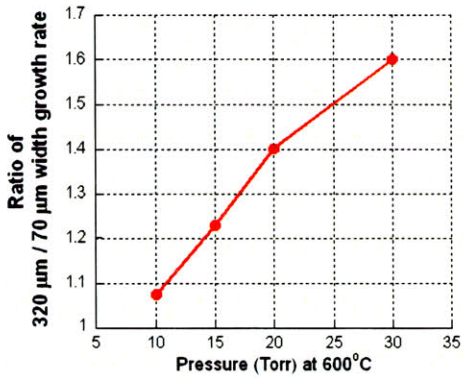
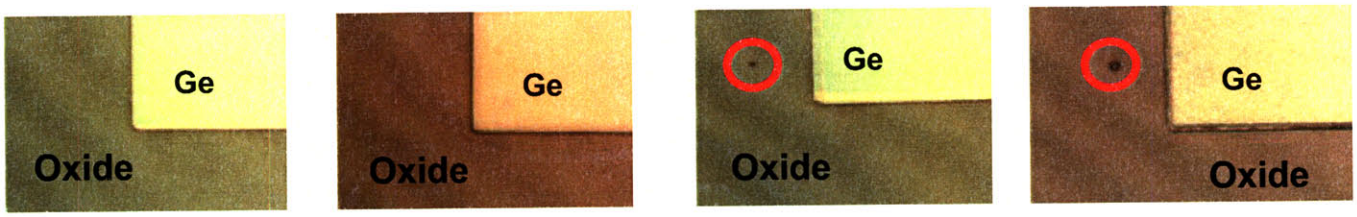


Figure 3.19 Relative Ge cap growth rate for 320 µm trench widths versus 70 µm trench widths as a function of pressure at 600°C. The microscopic loading effect drops almost linearly as a function of the pressure.



(a) (b) (c) (d)

Figure 3.20 Nomarski micrographs of SEG Ge-on-Si films highlighting the onset of germanium nucleation on the field oxide. Nuclei are marked by a red circle. Analysis courtesy of Meekyung Kim.

(a) No nucleation visually apparent after depositing a 63 nm-thick seed layer
(b) No nucleation visually apparent after depositing a 30 nm-thick ramp layer
(c) Nucleation visually apparent after depositing a 1.7 μm-thick cap layer for 320 μm trench widths
(d) Nucleation visually apparent after etching any nucleation sources in seed or ramp layer in HCl prior to 1.7 μm-thick cap layer deposition for 320 μm trench widths

In order to determine the onset of germanium nucleation on the oxide, three germanium wafers were grown, a seed only wafer, a seed and ramp layer wafer, and a seed, ramp, and cap layer as shown in Figure 3.20 (a) – (c).

The nucleation was visually identified only for the third wafer, with the cap layer present. In order to ascertain if the nucleation occurs in the cap layer, one more wafer was grown, as shown in Figure 3.20 (d). A standard seed, ramp, and cap layer was grown, then 150 sccms of HCl was flown in the chamber for 5 minutes to etch the Ge nuclei on the field oxide. At the end of the etch step, there was no more nucleation present on the oxide field. Finally, a Ge cap layer was re-deposited and then the wafer was examined for germanium nucleation on the oxide. It was noted that there was still nominally 10^4 nuclei/cm^2 when the wafer was examined as per the procedure outlined in Figure 3.18. Thus, based on six to ten randomly located ~ 1 mm^2 areas examined across the wafer, it was concluded

that visual germanium nucleation on the field oxide occurs during the cap deposition step. It was noted that since the nucleation density dropped during the cap only process and the germane partial pressure is highest during the ramp step that the ramp layer might contribute significantly to the nucleation process. Therefore, germane flow was discontinued during the temperature ramp step.

In order to ensure smooth film morphology, the Ge seed thickness was increased to 75 nm. Following these modifications to the standard blanket Ge-on-Si growth process, the growth parameters for nucleation suppression were studied solely during the deposition of the cap layer.

3.3.2 Effect of HCl flow on Ge nucleation density

HCl flows above 150 sccms during the cap layer growth led to complete suppression of germanium growth on both the oxide and silicon surface. As displayed in Figure 3.21, flows of HCl from 100 to 150 sccms created Ge-on-Si surfaces with RMS roughness values greater than 50 nm while failing to suppress germanium nucleation on the oxide surface. As shown in Table 3.1, it has been experimentally verified that DCVD oxide films, that have an 11x higher RMS surface roughness relative to thermal oxide films, also have a 2x increase in the Ge nucleation density. The increase in surface area and density of bond sites for rough surfaces is postulated to account for the increased nucleation density on DCVD oxide films.

To account for the increased nucleation for HCl flows smaller than 100 sccms shown in Figure 3.21, AFM studies were also performed to ascertain whether the

HCl flow roughened the oxide surface. As displayed in Table 3.2, the HCl flow does not appear to affect the surface roughness of the oxide film. Thus, it is postulated that HCl flow below 100 sccms has a chemical effect that increases the Ge nucleation on the oxide by at least 2.5x. At the germanium cap growth conditions examined of 650°C and 30 Torr, the use of HCl does not appear to be a viable approach to suppress germanium nucleation on the oxide surface since it results in either undue roughening of the Ge-on-Si films or a very low germanium growth rate.

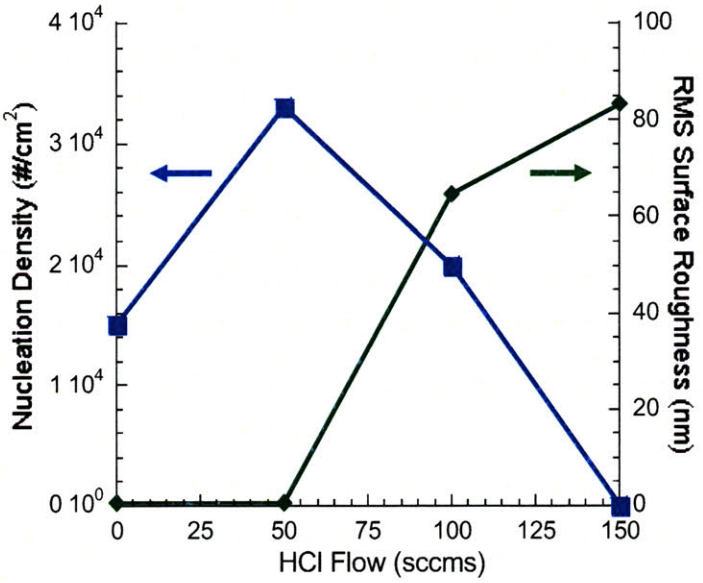


Figure 3.21 A plot of the effect of HCl flow during the germanium cap growth on the nucleation density (blue) and the surface roughness of the cap layer (green). There is no regime in which there is both a reduction of germanium nucleation on oxide and minimal surface roughness. Measurements are courtesy of Meekyung Kim.

Oxide	Growth Temp (°C)	Pressure (Torr)	Growth Rate (320 μm trench)	Ge Cap RMS (nm) 10 x 10 μm scan	Oxide RMS (nm) 10 x 10 μm scan	Nucleation Density (#/cm²)
Thermal	650	30	83 nm/min	Smooth/0.79	0.24	15,000
DCVD	650	30	82.5 nm/min	Smooth/0.83	2.75	25,000

Table 3.1 Nucleation density for Thermal and DCVD oxide films with identical growth conditions. The 11x greater oxide surface roughness of the DCVD field oxide relative to the thermal field oxide is hypothesized to lead to the 1.7x increase in germanium nucleation density on the DCVD field oxide. Measurements and analysis are courtesy of Meekyung Kim

HCl Flow (sccms)	Thermal Oxide RMS (nm) 10x10 μm scan
200	0.276
100	0.287
0	0.298

Table 3.2 Thermal field oxide roughness as a function of HCl flow. The HCl flow does not appear to roughen the surface, in fact it might smoothen the field oxide surface, although the AFM measurements are also near the detectable limit. AFM measurements are courtesy of Meekyung Kim.

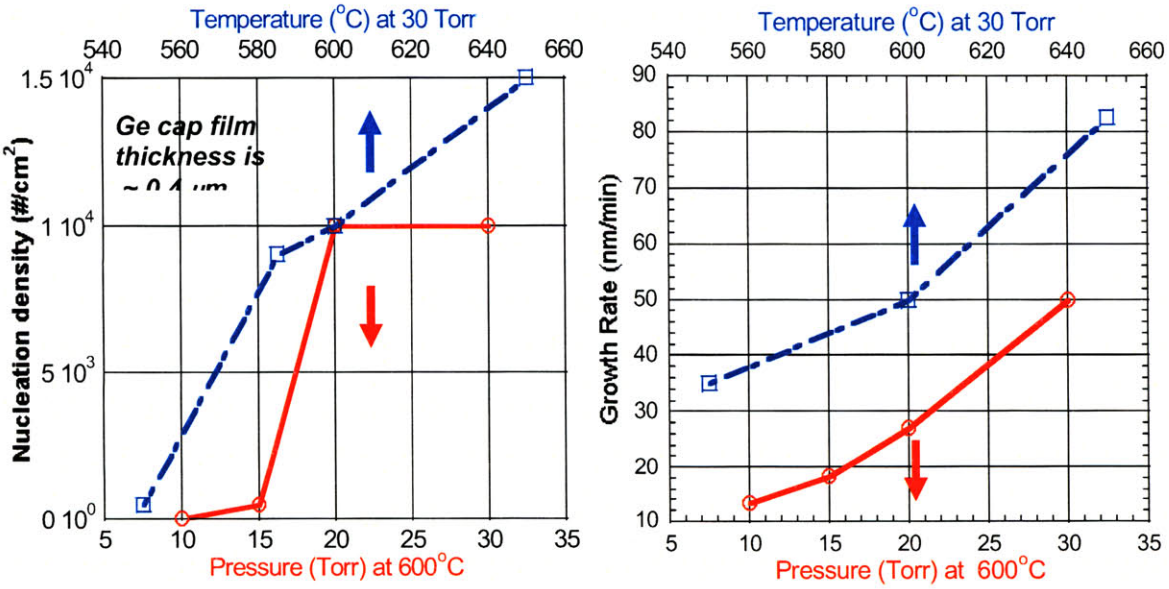
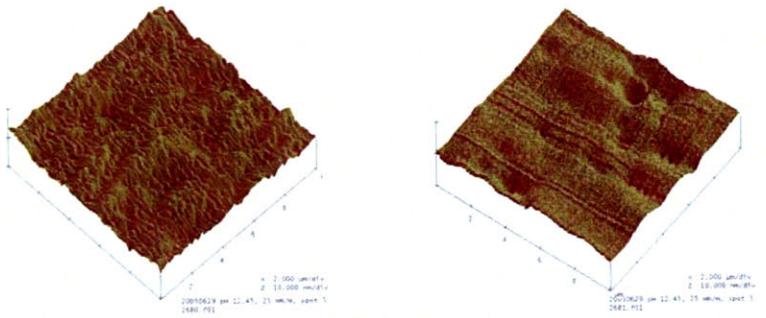


Figure 3.22 (a) Nucleation density as a function of chamber pressure and temperature. Lowering the chamber temperature (dashed blue) and chamber pressure (solid red) reduces the nucleation density. Minimal nucleation occurs at 600°C, 10 Torr. (b) Reducing the chamber temperature (dashed blue) and chamber pressure (solid red) also significantly reduces the germanium cap growth rate. Measurements are courtesy of Meekyung Kim.

3.3.3 Effect of temperature and pressure on Ge nucleation density

The Ge cap deposition temperature was varied from 550 to 650°C, and as is evident in Figure 3.22 (a), it is found that as the temperature decreased, the nucleation density of germanium on the oxide film dropped proportionally. For temperatures below 585°C, the germanium film grown in the Si windows develops pyramidal defects similar to those observed for blanket Ge-on-Si films at 575°C. In this temperature range, some Ge nucleation on the oxide surface is still evident. Thus, lowering the cap deposition temperature cannot be utilized as the sole approach to suppressing germanium nucleation on oxide surfaces. A germanium cap deposition temperature of 600°C was selected for continuing experiments to minimize the germanium nucleation on oxide while retaining reasonable growth rates and surface morphology.

At 600°C, the cap growth pressure was systematically reduced from 30 to 10 Torr, and there was no change observed in the nucleation density until the pressure dropped below 20 Torr. From 20 to 10 Torr, the germanium nucleation density is proportional to the growth pressure and drops to virtually zero at 10 Torr for six to ten random 1 mm^2 areas selected across the wafer as shown in Figure 3.18. The Ge nucleation on the oxide was not observed for Ge film thickness up to 0.8 μm, but germanium nucleation becomes evident for 1.3 μm-thick films grown under the same conditions [51]. As evident in Figure 3.22 (b), generally a reduction in the germanium nucleation density comes at the cost of significantly lower germanium cap growth rate.



(a) (b)

Figure 3.23 10 μm x 10 μm AFM scans of 1.7μm-thick SEG Ge-on-Si films (a) as grown (RMS of 1 nm), and (b) post 800°C blanket anneal (RMS of 1 nm). AFM measurements are courtesy of Meekyung Kim.

3.3.4. Material characterization of annealed, SEG Ge-on-Si films

After annealing the SEG Ge films with thicknesses of 1.3 and 1.7 μm at 800°C for 30 minutes, the films are found to have a threading dislocation density of ~2 x 10^7 cm^{-2}. As shown in Figure 3.23, 1.7 μm-thick annealed films had an RMS roughness of ~1 nm, for germanium surface areas of 1 mm^2. These dislocation densities and surface roughness results are comparable to the annealed, blanket Ge films described above. Furthermore, when the SEG Ge-on-Si films are cyclically annealed for 8 cycles between 450°C and 830°C with a 2 minute anneal time at each temperature per cycle, as the germanium trench size decreases, the threading dislocation density drops. This reduction in dislocation density is particulary evident for trench openings below 220 μm.

For an anneal at a constant temperature, the drop in nucleation density as a function of trench width noted for the cyclic anneal is not observed. This behavior is captured in Figure 3.24. For squares of dimension 30 μm x 30 μm, dislocation densities of 10^6 cm^{-2} are observed. These dislocation density trends are similar to those observed in UHVCVD SEG Ge-on-Si films [33].

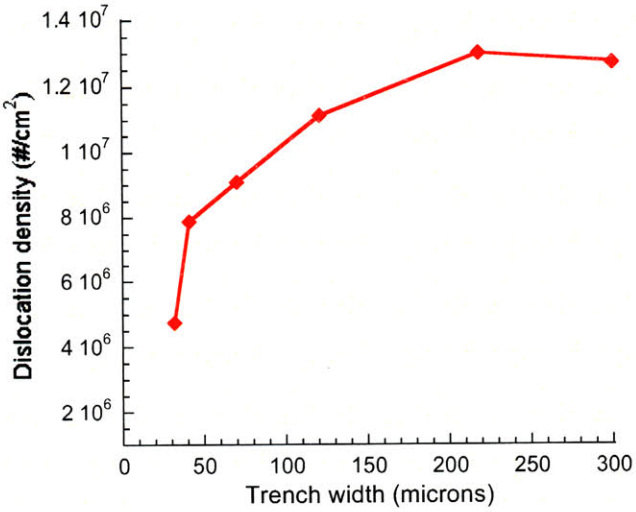


Figure 3.24 Dislocation density as a function of square trench opening after an *in-situ* cyclic anneal between 450°C and 830°C for ~32 minutes. Prior to the cyclic anneal, the dislocation density was higher than 10^8 cm^{-2}. Eight cycles were performed with a 2 minute residence time at 450°C or 830°C. The error bar is approximately ±10% for these measurements. For blanket anneals, the dislocation density did not vary as a function of trench opening. EPD measurements are courtesy of Meekyung Kim

3.4 Germanium passivation

Germanium is a much more reactive material than silicon, making passivation of the germanium surface very important in the fabrication process. Many approaches have been attempted to passivate germanium films. For example, a GeO_2 film can be reactively grown on the Ge surface. To further improve the thermal stability and passivation qualities, often the GeO_2 film is converted into GeO_xN_y films via thermal or plasma nitridation. Besides growing the germanium dielectrics, several deposited dielectrics ranging from SiO_2, SiO_2 on a thin Si cap, SiO_xN_y, Si_3N_4, Ge_3N_4, Al_2O_3, AlN, AlP_xO_y, to utilizing sulfides and chlorides have been investigated over the past forty years [52]. A few of the CMOS compatible germanium passivation methods are outlined below.

One of the simplest CMOS compatible methods of passivating germanium films is to deposit SiO_2 films on top of the germanium film. This method of

passivation generally leads to a density of interface traps (D_{it}) greater than 10^{12} cm^{-2} eV^{-1}. By introducing a Si interlayer on top of the Ge surface, then depositing an SiO_2 film, the formation of germanium oxides are avoided. This approach generally leads to D_{it} values between $10^{11} - 10^{12}$ cm^{-2} eV^{-1} [53]. Amorphous Ge_3N_4 passivating films deposited at 550°C in RF furnaces were also found to generally lead to D_{it} values around 10^{12} cm^{-2} eV^{-1} [54]

The other major approach to CMOS compatible germanium passivation films is to reactively grow a passivation film onto the germanium surface. Germanium oxides are generally very weak, being soluble in water or HF. Germanium oxides can be grown in a wet chemical oxidation reaction in a peroxide/HF solution that has high thermal and chemical stability. These GeO_2 films have been measured to have a D_{it} of 10^{12} $cm^{-2}eV^{-1}$ [55].

In order to further improve the quality of germanium oxide films, germanium oxide films are generally nitrided. GeO_xN_y films grown by oxidation at ~550°C and subsequent nitridation at temperatures of ~600°C in a vacuum furnace have been found to be promising passivation approaches for germanium films. Germanium oxynitride films that have been nitridated in the manner above for one to two hours have been found to lead to a D_{it} level of $5x10^{10}$ cm^{-2} eV^{-1}, some of the lowest values published in the literature [56-57].

A limited evaluation of various methods of passivating germanium films was conducted in this work via the direct deposition of passivating films in a dielectric chemical vapor deposition (DCVD) chamber and reactively growing native germanium insulating films in a rapid thermal processor (RTP) tool. In Chapter

4, more extensive passivation studies were indirectly evaluated via the effect of various dielectrics on the leakage currents of Ge-on-Si *pin* photodiodes. In the following sections, the passivation quality of various dielectrics on the germanium interface states is presented via capacitance versus frequency measurements on fabricated capacitors.

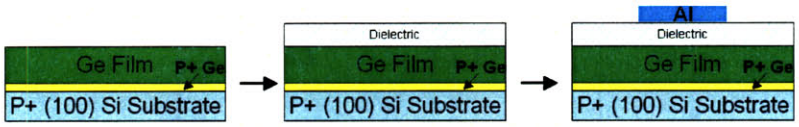


Figure 3.25 The generic fabrication sequence for Ge-on-Si capacitors. The Ge film is first deposited in the LPCVD chamber, followed by depositing and patterning the passivating film, and then the Al film is deposited and patterned.

3.4.1 Ge-on-Si capacitor fabrication

The first process step in fabricating the Ge-on-Si capacitors was depositing a Ge-on-Si film with a 5 x 10^{19} cm^{-3} boron doped 60 nm-thick Ge seed, and a 1.7 μm-thick intrinsic Ge cap layer as shown in Figure 3.25. Photoresist is spun and hardbaked onto the Ge-on Si film. Then the wafer backside is etched in order to remove the $Si_{1-x}Ge_x$ film that is currently created in the Ge-on-Si deposition process. A sample RBS spectrum illustrating an undesirable 0.26 um-thick $Si_{1-x}Ge_x$ region in the wafer backside from a 2 μm-thick unannealed Ge-on-Si deposition process is shown in Figure 3.26. The $Si_{1-x}Ge_x$ film on the wafer backside is removed in the LAM490 tool using a chlorine and helium based plasma chemistry. The $Si_{1-x}Ge_x$ film on the wafer backside is etched away in order to avoid germanium cross contamination in further processing steps. The

photoresist is then stripped from the frontside of the wafer and the Ge-on-Si film is cleaned with the Ge RCA clean detailed in Appendix D. Then the Ge

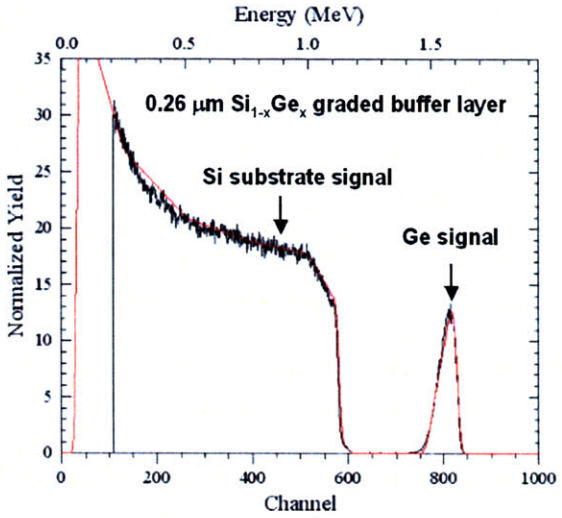


Figure 3.26 RBS spectrum showing the effect of undesirable Ge deposition on the wafer backside. The germanium deposits on the backside of the wafer and diffuses into the silicon during the Ge-on-Si growth process. After depositing one micron of germanium on the wafer frontside, the backside $Si_{1-x}Ge_x$ region linearly varied in composition from x =0.19 at the backside surface to zero at 0.26 μm into the wafer backside. This 2 μm-thick Ge-on-Si wafer did not have an *in-situ* anneal which is expected to extend the $Si_{1-x}Ge_x$ region deeper into the silicon. RBS analysis is courtesy of Cait Ni Chleirigh.

passivation layer is grown and/or deposited. The grown passivation layer is Germanium Oxynitride (GeO_xN_y), which is grown in an RTP either in an oxygen ambient, followed by an ammonia ambient, or just by reacting the native germanium oxide on the Ge-on-Si film in an ammonia ambient. As shown in Figure 3.27, the GeO_xN_y film thickness varies between 1.5 – 7 nm, depending

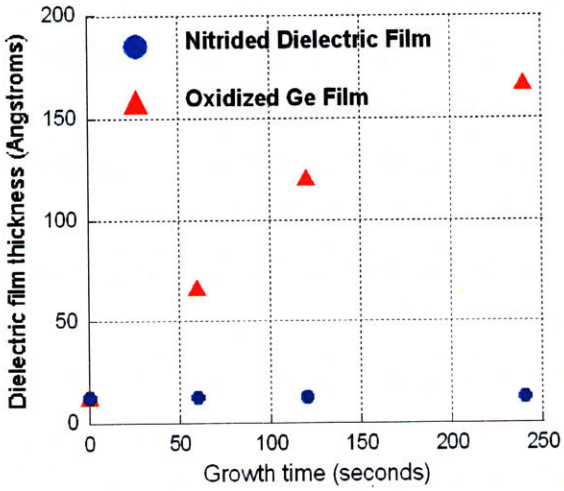


Figure 3.27 Plot of the dielectric film thickness as a function of the oxidation or nitridation time. Oxidation, creating a GeO film, leads to a linear increase in the growth rate, while nitridation, creates a GeON film, with a constant dielectric film thickness but an increased nitrogen content.

solely on the oxidation time. In lieu of growing a GeO_xN_y film, a SiO_2 film can also be deposited in the Dielectric Chemical Vapor Deposition (DCVD) tool. An aluminum film is then deposited in the Physical Vapor Deposition tool and patterned to form the top contact to the capacitors.

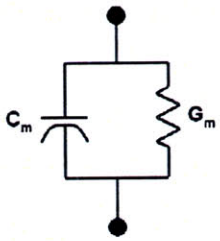


Figure 3.28 Equivalent circuit diagram that models the effect of D_{it} on capacitance vs voltage measurements. The conductance represents the trap capture and emission of carriers. From Schroder, *et al* [53].

3.4.2 D_{it} measurements

The capacitance and conductance of the fabricated capacitors was measured as a function of voltage with an HP4294A precision impedance analyzer. The top aluminum contacts and the bottom p+ silicon substrates were contacted with probes and stage contacts respectively. The capacitance and

conductivity of various devices were measured as a function of frequency from $10^3 - 10^7$ Hz. Using these measurements the density of interface states was determined using the conductance method introduced by Nicollian and Goetzberger [54]. This D_{it} measurement method yields the D_{it} in the depletion and weak inversion regimes and potentially the capture cross section for majority carriers and surface potential flunctuation.

The conductance method is based upon measuring the capacitance and conductance as a function of frequency. In this case, the conductance represents the current due to interface trap capture and emission of carriers, and thus can be used as a measure of the interface trap density. The equivalent circuit diagram for the conductance method is shown in Figure 3.28. The trap conductance and density of interface states are defined as:

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \qquad \text{(Equation 3.1)}$$

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{\max} \qquad \text{(Equation 3.2)}$$

where G_P is the trap conductance, ω is the measurement frequency, G_m is the measured conductance, C_m is the measured capacitance, and C_{ox} is the oxide capacitance [58].

As shown in Table 3.3, after the initial passivation process, Rapid Thermal Nitridation (GeO_xN_y) of Ge films gives the lowest D_{it} measurements in the 10^{11} cm^{-2} range. On the other hand, after thermal annealing in forming gas (50% N_2 / 50% H_2) at or above 325°C, the mid-gap density of states of the nitrided germanium film rapidly degrades to ~ 2 x 10^{12} cm^{-2}.

A Rapid Thermal Oxidation and Nitridation (GeO_xN_y) cycle gives more thermal stability to the annealing process, possibly due to the increased passivating film thickness, but increases the initial D_{it} level to ~10^{12} cm^{-2} eV^{-1} as illustrated in Figure 3.29 (b). The RTON germanium films actually improve after sintering at 325°C to match the D_{it} results from purely nitrided films without an intermediate oxidation step. As the sinter temperature is increased above 325°C, the RTON D_{it} results degrade, similarly as to the RTN results.

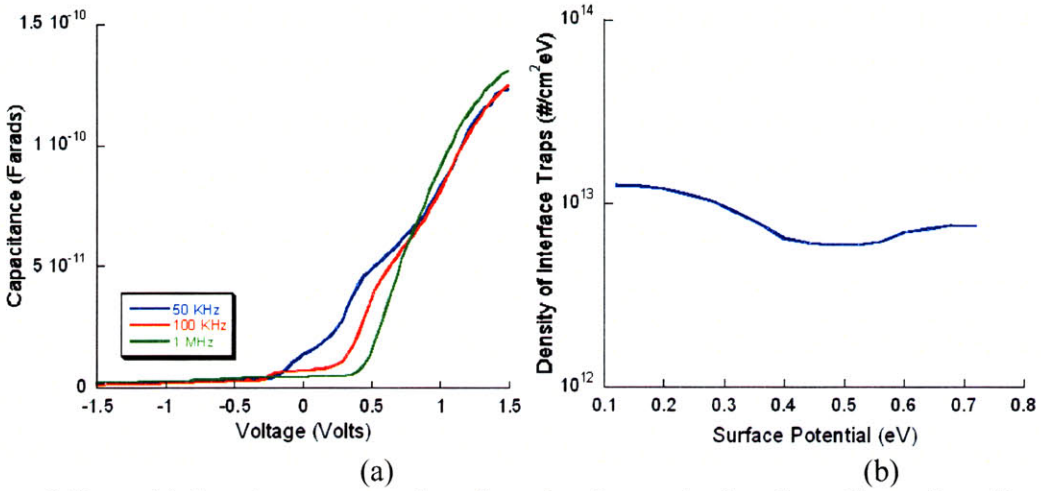


Figure 3.29 (a) Capacitance versus voltage for various frequencies for a Ge-on-Si capacitor with a 7 nm-thick GeO_xN_y dielectric film created by a 60 second oxidation step followed by a 120 second nitridation time in an ammonia ambient. The surface area of the aluminum contact was 2.25 x 10^4 cm^{-2}. The presence of interface traps in seen in the kink around 0.5 volts. At a frequency of 1 MHz, the capacitance curve becomes smooth due to the inability of the interface traps to follow the signal. (b) From the capacitance versus frequency measurements, the density of interface traps (D_{it}) is extracted using Equations 1 – 2 as a function of the surface potential. For this Ge-on-Si capacitor, the midgap D_{it} value is 6 x 10^{10} $cm^{-2}eV^{-1}$.

Oxidation time (sec)	Nitridation time (sec)	SiO_2 deposition	Thickness (nm)	Refractive Index	Sinter Temp (°C)	Bandedge D_{it} ($cm^{-2}eV^{-1}$)	Mid-gap D_{it} ($cm^{-2}eV^{-1}$)
60	60	No	7	1.3	0	3.00E+14	2.00E+12
60	60	No	7	1.3	325	2.00E+12	1.00E+11
60	60	No	7	1.3	425	8.00E+14	3.00E+12
60	120	No	7	1.3	0	1.00E+13	6.00E+12
0	60	No	1	1.5	0	1.00E+12	2.00E+11
0	60	No	1	1.5	325	1.00E+14	2.00E+12
0	60	No	1	1.5	425	1.00E+13	2.00E+12
0	0	Yes	66	1.3	0	1.00E+15	1.00E+13

Table 3.3 Density of Interface Traps (D_{it}) as a function of various dielectrics and processing conditions. Purely nitrided germanium films give the best passivation, but due to the thin nature of the film, the least thermal stability. Oxidized and nitrided germanium films give better thermal stability and the D_{it} lowers to match the best results from pure nitrided films after sintering at 325°C. Deposited SiO_2 films give the highest D_{it} measurements.

SiO_2 dielectric films give the highest D_{it} values ($10^{13} - 10^{14}$ $cm^{-2}eV^{-1}$) independently of whether the Ge-on-Si capacitor has been been sintered. It therefore appears that including as much nitrogen passivation as possible at the germanium interface is key to achieving good passivation results. In addition, in order to enjoy the full benefits of passivation, careful attention must be given to post-passivation thermal budgets.

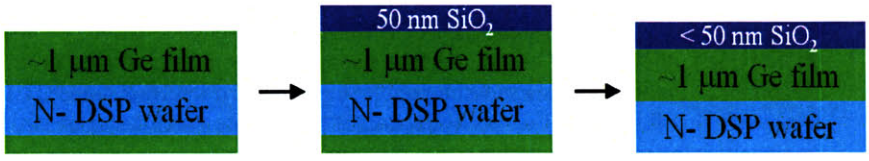


Figure 3.30 The generic fabrication sequence for Ge-on-Si absorption coefficient measurement. The Ge film is first deposited in the LPCVD chamber, a thin, transparent SiO_2 film is deposited to protect the Ge surface, and then the backside $Si_{1-x}Ge_x$ film is removed.

3.5 Ge film absorption coefficient measurement

A study of the absorption coefficient of Ge-on-Si films was also performed. The measurements were performed on a Cary spectrophotometer with a wavelength range between 175 – 3300 nm. The general fabrication process is shown in Figure 3.30. The germanium was deposited on an N- double side polished (DSP) wafer in order to ensure transmission through the entire wafer without backside roughness induced scattering loss and to minimize loss due to free carrier absorption. Two wafers were prepared for measurement, one control wafer, without germanium deposition, and the other wafer with an unnannealed ~1 micron Ge-on-Si film deposited at 650°C, 30 Torr. Both wafers then had a 50 nm SiO_2 film deposited on the surface. The backside SiO_2 and Ge film were then etched off in a Buffered Oxide Etch (BOE) solution and the LAM490 respectively. The wafer without Ge went through the same wet and dry etch processes in order to serve as a control for the wafer with the Ge-on-Si film. Theoretically, the measurement system was assumed to have no loss once the absorption, transmission, and reflection was accounted for (i.e. $1 = T + R + A$). The total reflection loss could not be completely accounted for, especially the loss contribution due to reflections from the Si/Ge interface. In order to further account for any loss in the Si film due to free carrier absorption and backside

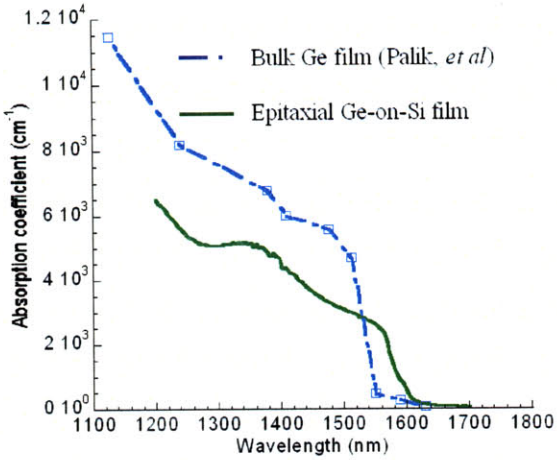


Figure 3.31 Absorption coefficient from bulk Ge film (dashed blue), and tensilely strained Ge-on-Si film (solid green). The wavelength cutoff for the bulk Ge film is 1.55 μm, while the wavelength cutoff for the Ge-on-Si film is 1.6 μm, showing the bandgap of the Ge-on-Si film has been reduced due to tensile strain from thermal stress, as observed by Cannon [60]. The absorption coefficient for the Ge-on-Si film is 2x less than expected, possibly due to silicon diffusion into the germanium film. Bulk Ge data from Palik, *et al* [59]

roughness induced scattering, the control wafer was also measured and used as a calibration for the system loss. The measured Ge film absorption coefficient is shown in Figure 3.31. Below the cut-off wavelength, the extracted absorption coefficient is approximately 2x less than expected for bulk germanium [59]. The reduction in the absolute value of the absorption coefficient might be due to a lower germanium film thickness than expected, possibly due to Si and Ge interdiffusion or to a lower germanium cap growth rate than expected. The lower than expected absorption coefficient will be discussed further in Section 4.3.1.

Although the calculated absorption coefficient is below the expected value, the effect of the tensile strain due to the mismatch of thermal expansion and contraction between the Ge film and the silicon substrate when cooling down from the deposition at 650°C is evident. Relative to the expected absorption coefficient cutoff at 1.55 microns for bulk Ge, the cutoff for Ge-on-Si films occurs at a wavelength of 1.6 microns, showing a 25 meV reduction in the Ge bandgap upon cooling down from 650°C [59]. This ~25 meV reduction in the Ge

bandgap upon cooling down from temperatures between 600 – 850°C has also been seen in prior UHVCVD work [60].

3.6 Chapter Summary

In this chapter, the effect of growth conditions such as pressure, temperature, and seed thickness on the material quality of epitaxially grown blanket LPCVD Ge-on-Si films has been examined. An optimum Ge seed layer growth temperature window of 335°C to 365°C has been identified. Seed layer depositions below 320°C lead to crystallographic defect formation, while depositions above 365°C produce surface roughening due to the increased surface mobility of germanium.

It has also been demonstrated that in this process, a Ge seed layer thickness of at least 45 nm is required in order to maintain smooth morphology as the temperature is ramped for the high-temperature portions of the growth process. For seed layers at or below 30 nm-thicknesses, the Ge film islands during the temperature transition to the cap temperature, leading to increasingly rougher surface morphology during the remainder of the deposition process. 60 nm-thick seed layers are sufficiently thick to withstand the temperature ramp and produce smooth Ge films.

A process window for smooth Ge cap layer growth has also been demonstrated. Smooth cap layers have been deposited from 600 to 700°C, and at 650°C, chamber pressures from 30 to 90 Torr are shown to lead to smooth film morphologies. 2 μm-thick Blanket Ge-on-Si films annealed at 830 to 900°C for

30 minutes have been shown to have threading dislocation densities of ~2 x 10^7 cm^{-2} with an associated RMS roughness of 1.6 nm.

Boron doping above 10^{19} cm^{-3} has been found to enhance the growth rate of Ge seed layers and lower the oxygen incorporation at the Ge/Si heterointerface. It is hypothesized that the enhancement in the growth rate is due to the lattice contraction from high boron doping. Phosphorus doping of the cap layer has also been demonstrated up to ~10^{19} cm^{-3}, without adversely affecting the germanium film growth rate and surface morphology.

The effect of HCl flow, growth pressure, and temperature on nucleation density for SEG LPCVD Ge-on-Si films is also examined. HCl does not appear to strongly suppress germanium nucleation on the oxide surface without causing undue roughening or a low growth rate for the Ge-on-Si film. Using GeH_4 and H_2, an optimal cap deposition condition of 600°C, 10 Torr has been identified for suppression of germanium nucleation on the field oxide of the wafer pattern. At higher temperatures or pressures, Ge nucleates readily on the oxide surface. 1.7 μm-thick selective Ge-on-Si films cyclically annealed between 450 and 830°C for 30 minutes have been shown to have threading dislocation densities that depend on the trench width, decreasing from ~1 x 10^7 cm^{-2} for 320 μm square trenches to ~4 x 10^6 cm^{-2} for 30 μm square trenches. The annealed films generally had an associated RMS roughness of 1 nm.

Passivation of the germanium films was studied using metal oxide semiconductor capacitance versus voltage measurements for various frequencies and it was found that reactively grown GeON films, either from a nitridation in

ammonia or an oxidation then nitridation step leads to mid-gap D_{it} values in the range of $10^{11} - 10^{12}$ cm^{-2}. Deposited silicon dioxide layers as passivation films led to a D_{it} values greater than 10^{13} cm^{-2}.

The absorption coefficient of Ge-on-Si films was also measured as a function of wavelength. Although the extracted absorption coefficient of our film was ~ 2x lower than expected, the expected bandgap narrowing due to tensile strain was observed, with the Ge-on-Si film demonstrating a wavelength cutoff of 1.6 μm versus the 1.55 μm wavelength cutoff of bulk germanium films. Further studies of the extracted absorption coefficient will be presented in Section 4.3.1.

Chapter 4: LPCVD Ge-on-Si *pin* photodiode fabrication and characterization results

Introduction

In this chapter, the fabrication and characterization results for blanket, mesa-isolated, and selective Ge-on-Si *pin* photodiodes are discussed. First, the electrical, optical, and material characteristics of polysilicon contacted *pin* photodiodes fabricated in blanket epitaxial Ge films are introduced. From these results comes the motivation for fabricating in-situ-doped, mesa-isolated Ge-on-Si *pin* photodiodes without polysilicon contacts. The optical and electrical characteristics of the mesa-isolated Ge-on-Si *pin* photodiodes are also investigated. Finally, the electrical characteristics of *pin* photodiodes fabricated in selective Ge-on-Si are discussed.

Motivation

Ge-on-Si films have many plausible applications, for example, as the channel material in Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) due to the high mobility of electrons and holes in Ge [61]. Moreover, Ge can be utilized in the source and drain material of MOSFETs to induce strain in the Si channel in order to increase the hole mobility. Current applications of such strained silicon channels involve selective epitaxial growth of $Si_{0.8}Ge_{0.2}$ [62].

One of the most promising applications of Ge-on-Si films leverages the high absorption coefficient of germanium in the near infrared region to create CMOS

compatible photodetectors that function in the low loss silica fiber wavelength range of 1.3 to 1.6 μm [63]. In order to fabricate a good photodiode, the Ge-on-Si film must have a high absorption coefficient in the wavelength range of interest, a long carrier lifetime, and the device should be designed for a short photogenerated carrier transit time [64].

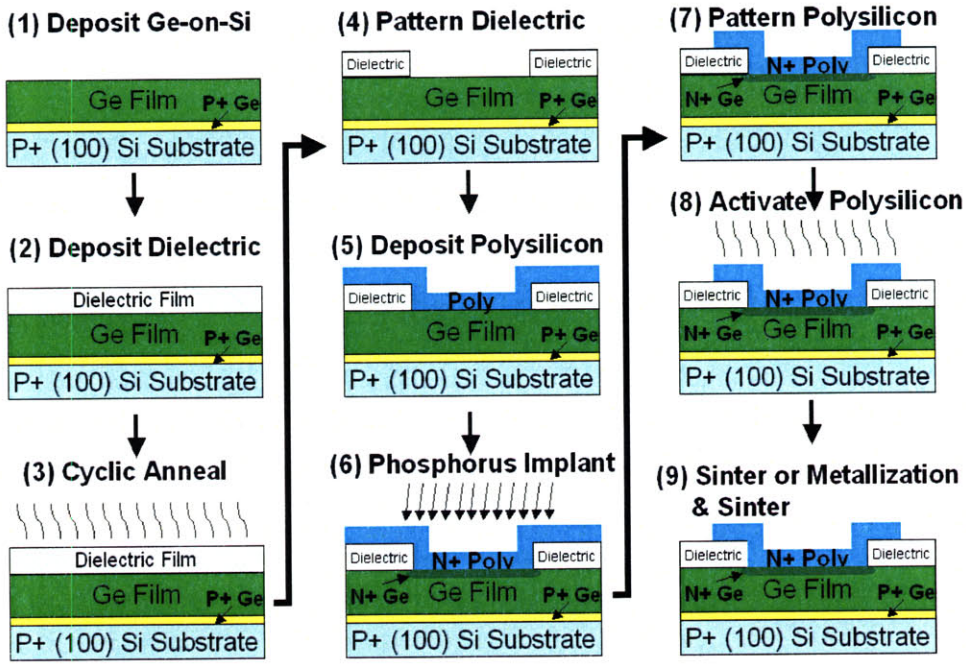


Figure 4.1 Generic fabrication process for blanket Ge-on-Si *pin* photodiodes. The metallization steps are not included in the schematic illustration above.

4.1 Blanket Ge-on-Si *pin* photodiode fabrication process

As has been demonstrated in Chapter 3, the surface roughness and dislocation density of the LPCVD Ge-on-Si films in this work match those of UHVCVD and RPCVD Ge-on-Si films. In order to further examine the optical and electrical qualities of the LPCVD Ge-on-Si films, *pin* photodiodes were also fabricated. This process is based upon a mask set developed at Analog Devices, Inc. for use in the Microsystems Technology Laboratories (MTL) cleanroom at MIT.

The first process step was depositing a Ge-on-Si film with a 5 x 10^{19} cm^{-3} boron doped 60 nm-thick Ge seed, and a 1.7 to 2 μm-thick intrinsic Ge cap layer in the Epi Centura™ chamber as shown in Figure 4.1. Photoresist is spun and hardbaked onto the Ge-on-Si film. Then the wafer backside is dry etched in a LAM490B in order to remove the $Si_{1-x}Ge_x$ film as discussed in Chapter 3. The photoresist is stripped from the frontside of the wafer and the Ge-on-Si film is cleaned with the "Ge RCA clean" process in Appendix D.

Next, the Ge passivation layer is grown and/or deposited. Most photodiodes only had a 300 nm-thick deposited passivation layer. This passivation layer is deposited in either a Plasma Enhanced CVD (PECVD) process (DCVD tool) or in a CVD process (low temperature oxide, 6C-LTO, tube). The majority of the deposited films were silicon nitride, silicon oxynitride (index of 1.7), or silicon dioxide films. For some of the photodiodes, there was a grown passivation layer inserted between the deposited passivation. The photodiodes with a reacted passivation layer was grown in a Rapid Thermal Processor system (RTP) either in an oxygen (O_2) ambient, followed by an ammonia (NH_3) ambient, or by reacting the native germanium oxide on the Ge-on-Si film in an ammonia ambient. This process created a Germanium Oxynitride (GeO_xN_y) film. As discussed in Section 3.4, the GeO_xN_y film thickness varies from 1.5 nm to 7nm, depending solely on the oxidation time.

If the Ge films are not *in-situ* annealed in the epitaxial reactor, an ex-situ anneal, shown in step 3 of Figure 4.1 is performed at this point in the process. The purpose of either of these anneals is to reduce the dislocation density. Most

wafers were subjected to "cyclic annealing," generally consisting of 8 cycles with each cycle including a minimum temperature of 650°C and a maximum temperature of 850°C with a 30 second duration at each temperature per cycle.

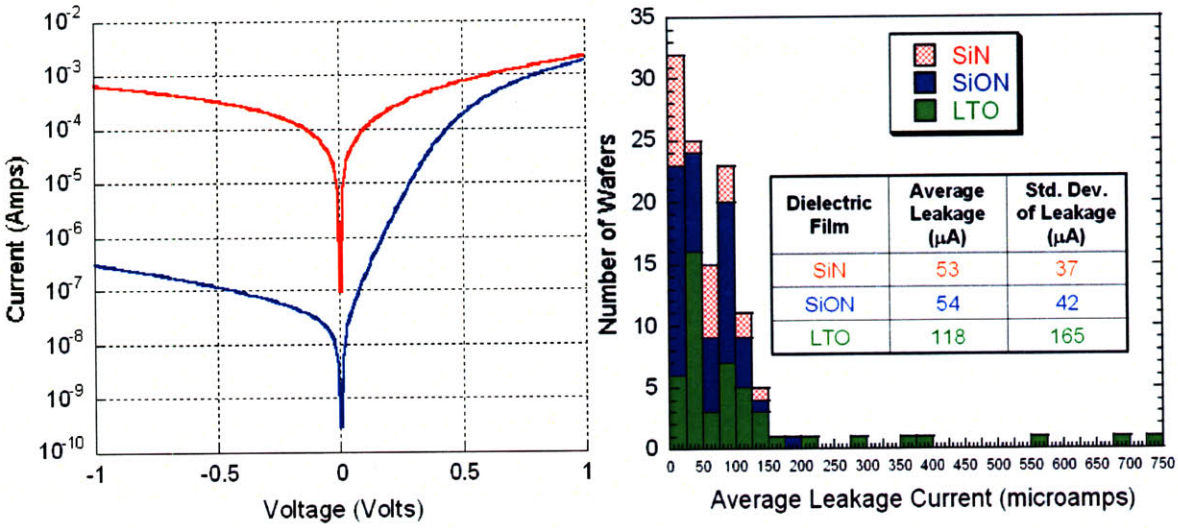
The passivation layer is then patterned as shown in step 4 of Figure 4.1 to expose the underlying Ge, and the wafer goes through a Ge RCA clean in order to prepare for the intrinsic 0.2 μm-thick polysilicon deposition. After the polysilicon is deposited, the wafers are sent out for ion implantation at Innovion, Inc. The standard implant conditions are 5×10^{15} cm^{-2} dose of phosphorus at an implant energy of 90 to 100 KeV. This leads to a chemical doping level of 1×10^{20} cm^{-3} in the polysilicon and an approximate 0.2 μm deep n-type Ge doping region beneath the polysilicon.

After the implant, the N+ polysilicon film is patterned, with the phosphorus diffused and activated at temperatures between 700°C to 750°C for 60 to 300 seconds in the RTP tool.

At this point, the basic components of a *pin* photodiode have been fabricated, and the wafer can either be sintered or the wafer can be metallized and then sintered to facilitate ease of device measurement. If the metallization step is skipped, the sintering is performed in a forming gas ambient (50% N_2 and 50% H_2 composition) at a temperature between 325 °C and 425°C for 30 minutes.

If the metallization process is to be completed, the wafer is subsequently patterned to open contacts to the p+ Si substrate. The passivation film is dry etched in the AME5000, and then the Ge film is etched in H_20:H_20_2:HCl in a ratio of 4:3:1. A 0.5 μm-thick field oxide film that also serves as an insulating layer

for the metal contact to the Si substrate is then deposited. Contact openings are etched in the oxide film and 0.1 μm-thick titanium and 0.75 μm-thick aluminum layers are deposited and subsequently patterned. Finally, the metallized photodiode is sintered in a forming gas ambient at a temperature between 325 °C to 425°C for 30 minutes.



(a) (b)

Figure 4.2 (a) Current-Voltage relationships of 50 μm x 50 μm *pin* photodiodes illustrating the orders of magnitude difference possible between some of the highest (solid red) and lowest (solid blue) reverse bias leakage currents for blanket Ge-on-Si photodiodes. (b) Average leakage current measured at –1 volt for 50 μm x 50 μm *pin* photodiodes for a majority of the blanket Ge-on-Si wafers fabricated in the course of this study. To generate this average, between 6 – 30 photodiodes were measured per wafer. The wafers are also segregated as a function of the passivating films used in the course of the blanket photodiode fabrication process.

4.2 Overview of blanket Ge-on-Si *pin* photodiode results

In the span of 3 years, over 200 wafers, and thousands of photodiodes were fabricated utilizing the steps discussed in Section 4.1. Approximately 150 of the wafers were fabricated with the assistance of Analog Devices, Inc., and ~50 wafers were fabricated by the author. All the wafers were fabricated at MTL.

In general, the reverse bias leakage current or dark current was utilized to assess the quality of the fabricated photodiodes. The rationale behind using the dark current to assess the photodiode quality is that it is a fast and convenient measurement method that yields a great amount of information about the photodiode [65]. The voltage dependence of the dark current also provides a good indication of the Ge-on-Si material quality and the impact of various fabrication steps on the photodiode electrical characteristics. Furthermore, as has been discussed in Chapter 2, the photodiode dark current is an important characteristic for circuit applications of these devices. For instance, the dark current is a key factor in determining the required power to achieve a given signal to noise ratio. Moreover, the dark current also plays a crucial role in the static power dissipation of a photodetector, since the device is usually operated in reverse bias [66].

The current-voltage characteristics of the photodiodes were measured with a HP4156C semiconductor parameter analyzer. In Figure 4.2 (b), a chart summarizing the reverse bias leakage current for a majority of the fabricated diodes is displayed. The majority of the fabricated wafers had 50 μm square photodiodes with reverse bias leakage currents between 10 and 30 μA at a bias of –1 volt. As discussed in Section 2.3, the maximum leakage current target for 50 x 50 μm^2 photodiodes was desired to be less than 7.5 μA. Thus, there was a strong desire to reduce the average reverse bias leakage current of the Ge-on-Si *pin* photodiodes.

The study to reduce the reverse bias leakage current values of the Ge-on-Si *pin* photodiodes was conducted in four major stages. The four main variables studied were the germanium dislocation anneal conditions, the polysilicon etch conditions, the polysilicon activation anneal conditions, and the germanium passivation conditions. Each of the four variables will be discussed in greater detail in the following sections. It should be noted that due to the presence of a large standard deviation among the photodiodes in a given lot, there is some difficulty in drawing conclusions from the processing splits.

4.2.1 Effect of the dislocation anneal on the photodiode dark current

These experiments were conducted to ascertain the impact of the dislocation anneal conditions on the reverse bias leakage current. The general parameters varied were the conditions of the *in-situ* and ex-situ anneal conditions. It was found that using an ex-situ anneals for temperatures between 650°C to 900°C and times from 8 to 60 minutes versus *in-situ* anneals at temperatures from 830°C to 900°C for 30 minutes appeared to reduce the reverse bias leakage current. In a comparison between in-situ and ex-situ germanium annealed wafers with identical growth and fabrication conditions, the five *in-situ* annealed wafers gave an average reverse bias leakage current of 13.7 μA for 50 x 50 μm^2 photodiodes biased at –1 volt, while the six ex-situ cyclically annealed wafers gave an average reverse bias leakage current of 6.5 μA for 50 x 50 μm^2 photodiodes biased at –1 volt, suggesting that the ex-situ anneal conditions were

better on average by approximately a factor of two. Furnace tube anneals at 900°C, for 30 to 60 minutes were also compared to RTP anneals and on average the RTP cyclic anneals gave slightly lower leakage than the tube anneals by approximately 20%. Thus, the majority of the dislocation anneals utilized in the course of processing the Ge-on-Si blanket wafers were cyclic anneals performed in an RTP tool.

4.2.2 Effect of Ge surface preparation and polysilicon etch conditions on the photodiode dark current

The etch studies were performed to quantify the impact of the germanium surface preparation prior to polysilicon deposition, and polysilicon etch conditions on the reverse bias leakage current. The major focus was on the germanium clean process and the dielectric dry and wet etch processes that define the polysilicon and germanium interface. There were two germanium cleans considered, one with a 1:1 hydrogen peroxide:water mixture and the second a dilute 1:6 hydrogen peroxide:water mixture. The dilute germanium clean was developed to reduce the germanium loss during the clean process from an etch rate greater than 15 nm/second to less than 5 nm/second as shown in Figure 4.3. It was determined in a comparison between the dilute germanium clean and the original germanium clean, that there was no clear dependence of the reverse bias leakage current on the Ge clean process. The more dilute germanium clean was adopted to minimize the germanium loss.

The dielectric etch condition was varied between a dry dielectric etch or a combined dry and wet dielectric etch. There was essentially no effect noted of this difference in processing conditions. A combination of a dry and wet etch was selected in order to minimize the possible impact of plasma damage to the germanium film prior to the polysilicon deposition [67].

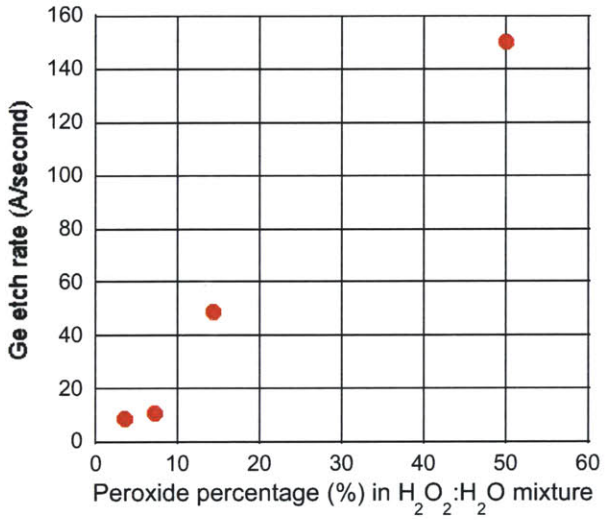


Figure 4.3 Germanium etch rate in as a function of the hydrogen peroxide concentration. A more dilute 14.3% hydrogen peroxide solution was selected to lower the germanium loss during the germanium clean process.

4.2.3 Effect of the polysilicon activation anneal on the photodiode dark current

The polysilicon activation anneal conditions were varied in order to quantify the effect of the activation anneal on the germanium surface material quality, and thus on the reverse bias leakage current. This study was performed for phosphorus implanted or in-situ doped polysilicon films. For phosphorus implanted polysilicon films, it was investigated whether performing the activation anneal before or after patterning the polysilicon had a strong effect on the reverse

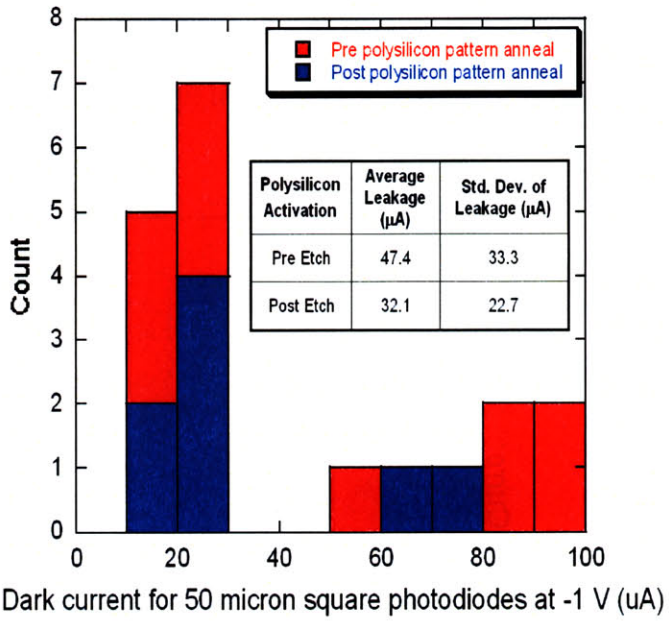


Figure 4.4 Number of wafers with an average reverse bias leakage at –1 volt for 50 μm x 50 μm Ge-on-Si *pin* photodiodes. The wafers are segregated as function of whether the polysilicon films were activated before (red) or after (blue) the polysilicon patterning step. A post patterning step polysilicon activation anneal led to a 33% lower leakage current than a pre patterning polysilicon activation anneal.

bias leakage current. As shown in Figure 4.4, it was found that a post-etch polysilicon pattern anneal lowered the average leakage current by ~33% relative to annealing prior to patterning the polysilicon. Furthermore, the thermal budget of the activation anneal was varied from 700°C (1 to 5 minutes) to 750 °C (1 to 5 minutes). It was found that below 700 °C, the dopants in the polysilicon film did not consistently activate. Between 700 and 850 °C, it appeared that the leakage current stayed constant and did not seem to be a function of the activation anneal thermal budget. It is worth noting that for anneals around 850 °C, the leakage current was somewhat higher at magnitudes of reverse bias higher than 2 volts, suggesting the possibility of a greater density of traps introduced due to the high temperature anneal process.

In-situ doped polysilicon films were also investigated due to their ability to lower the activation anneal thermal budget [68]. The polysilicon films were deposited on *in-situ* annealed germanium films with 3 to 7 nm silicon epitaxial

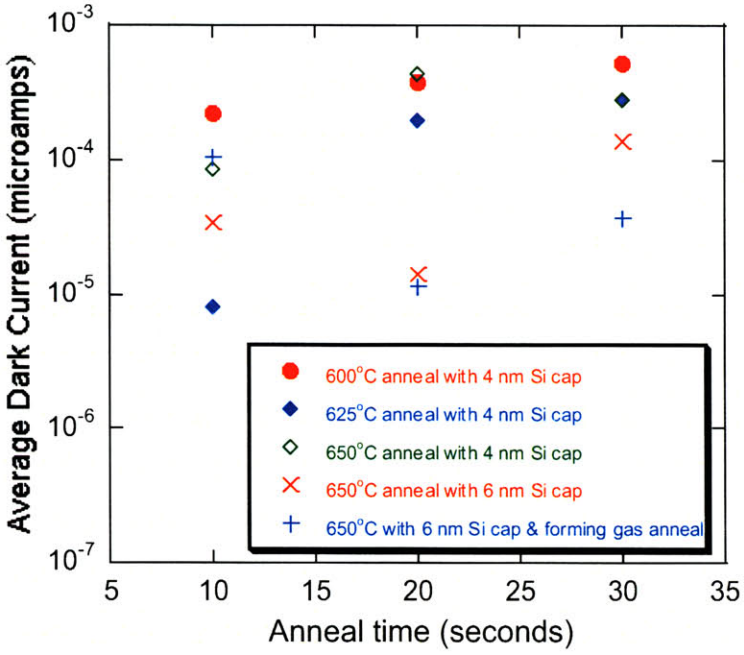


Figure 4.5 Average reverse bias leakage current at –1 volt of 50 μm x 50 μm blanket Ge-on-Si *pin* photodiodes as a function of the activation conditions for in-situ phosphorus doped polysilicon. Although the dark current appears to be reduced as the thermal budget decreases, the scatter in the data makes interpretation difficult. Measurements are courtesy of Nicole DiLello.

capping layers that were deposited after the anneal. The germanium films were *in-situ* annealed prior to depositing the silicon cap, because it has been reported that annealing germanium films after the silicon deposition inhibited the germanium dislocation anneal efficacy, leading to a 5 to 10x increase in the resulting dislocations [33]. Wafer pieces were cleaved and annealed in a Rapid Thermal Anneal (RTA) tool in order to determine an optimal thermal budget for polysilicon activation. Below 600°C, the polysilicon film did not activate reliably, hence the temperature range was limited to 600 to 650°C. As shown in

Figure 4.5, although the dark current does appear to decrease with the thermal budget, it appears that results are not reproducible, and the overall scatter in the data makes interpretation difficult. The difficulty in determining an optimal temperature and time could be attributed to either the large temperature variation in the RTA tool or the fact that the silicon passivation layer had relaxed, leading to a higher density of surface states. The only consistent trend that was extracted from this lot of photodiodes was that the reverse bias leakage current was perimeter dependent.

4.2.4 Effect of the germanium passivation film on the photodiode dark current

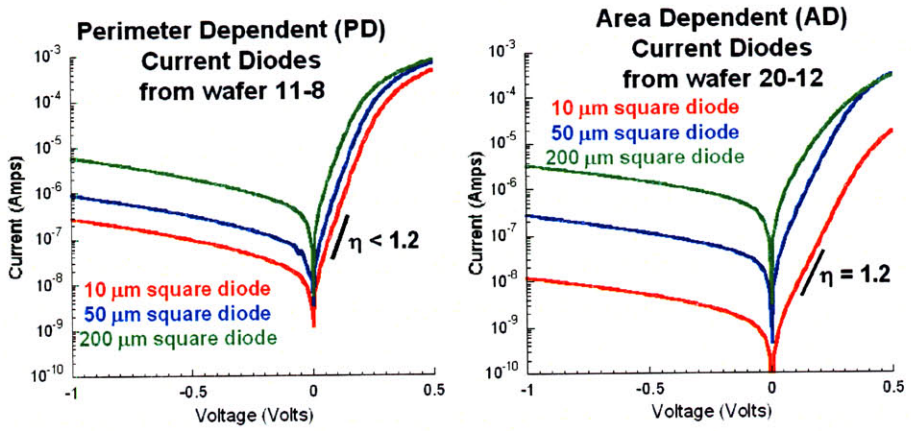
Figure 4.2 (b) shows the dark current as a function of the dielectric utilized to passivate the Ge film. It is clear that the SiN/SiON passivation films and the SiON films consistently yield the "lower" average leakage current values in the range of 1 to 25 μA for 50 μm x 50 μm photodiodes biased at –1 volt, while the Low Temperature Oxide (LTO) and DCVD SiO_2 films generally yield "higher" average leakage values in the range of 1 to greater than 100 μA for 50 μm x 50 μm photodiodes biased at –1 volt. On average, it was found that the SiN and/or SiON gave at least a 2x reduction in the dark current values relative to the LTO or DCVD SiO_2. It was also noted that as the nitrogen content of the passivation film increased, the leakage current dropped. This impact of the nitrogen content on the passivating dielectric is possibly due to either nitrogen passivation of

surface states, or lowered interdiffusion of Si, O, or Ge atoms between nitrogen rich dielectrics and Ge films [69-70].

To verify the effect of nitrogen passivation, a sinter experiment was performed. In this experiment, wafers were cleaved in half prior to the sinter step, and subjected to either no sintering or a sinter in a forming gas ambient at 425°C, for 30 minutes. It was observed that sintering the photodiodes generally led to a reduction in the leakage current relative to unsintered photodiodes from the same wafer. The effect of the sinter was particularly evident for SiON passivating films that showed a reduction of 2 to 3x in the dark current after a forming gas sinter relative to unsintered photodiodes.

Thin (2 to 6 nm) silicon films were also deposited on top of *in-situ* annealed germanium films prior to the deposition of SiON or LTO passivating films. It was also found that for identically processed 50 μm x 50 μm photodiodes with dark currents greater than 20 μA at –1 volt, the Si/SiON and Si/LTO combination tended to reduce the dark current by a factor of 2 to 3x relative to SiON and LTO only layers respectively. This effect has also been identified in the literature as a method to help reduce the leakage current [71].

Unfortunately, dark current values less than 5 μA for 50 μm x 50 μm photodiodes biased at –1 volt could not be demonstrated with a silicon interlayer between the dielectric and the germanium film. A possible explanation for this limitation will be further developed in Section 4.4.



(a) (b)

Figure 4.6 Electrical measurements for lowest leakage photodiodes fabricated with ideality factors of ≤1.2.
(a) Perimeter dependent current photodiodes with leakage of 1 μA for 50 μm x 50 μm photodiodes at –1 volt.
(b) Area dependent current photodiodes with leakage of 0.3 μA for 50 μm x 50 μm photodiodes at –1 volt.

4.2.5 Lowest dark current blanket Ge-on-Si *pin* photodiodes

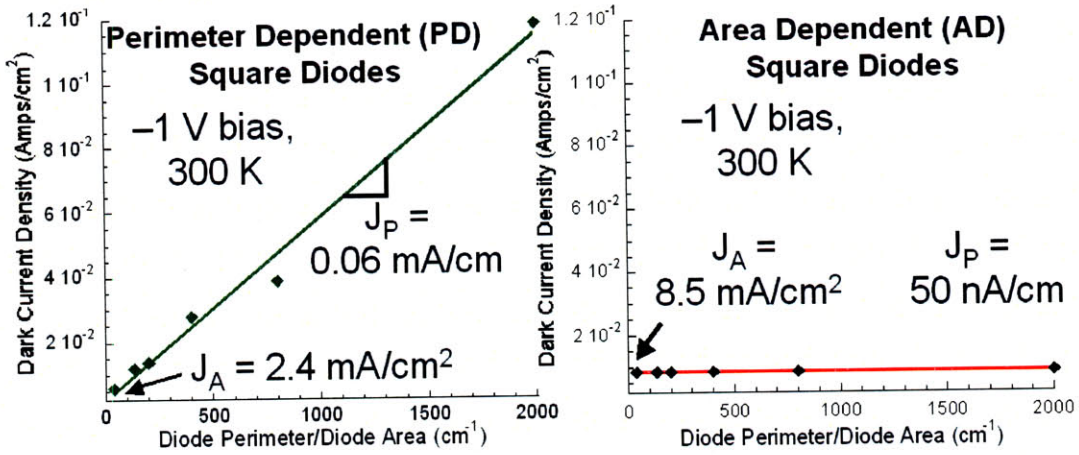
At this point, the focus will shift to analyzing the source of the reverse bias leakage current for the lowest leakage or "best" photodiodes fabricated. The lowest leakage blanket Ge-on-Si *pin* photodiodes from the last 3 years were perimeter dependent (PD) current photodiodes from wafer 11-8, and area dependent (AD) current photodiodes from wafer 20-12 as shown in Figure 4.6. Both the PD and AD photodiodes also have an extracted ideality factor of 1.1 to

1.2, which is quite reasonable for these process conditions. The ideality factor, η, is calculated from the diode equation under forward bias [72]:

$$I_F = I_S\left(e^{\frac{qV_F}{\eta kT}} - 1\right) \qquad \text{(Equation 4.1)}$$

$$\eta = \frac{V_1 - V_2}{(kT/q)}\left[In\frac{I_1}{I_2}\right]^{-1} \qquad \text{(Equation 4.2)}$$

where I_S is the reverse saturation current and I_X, V_X stand for the diode current at a given forward bias voltage. By simplifying Equation 4.1 for bias points above 50 millivolts and rearranging the equation for two bias points, η, is extracted as shown in Equation 4.2. In this thesis the quoted ideality factor is generally evaluated at voltages between 0.05 to 0.2 volt forward bias. Wafer 11-8 had a SiON passivation film with an ex-situ dislocation anneal, and wafer 20-12 had a GeON/SiO_2 passivation film with an *in-situ* dislocation anneal. The perimeter and area dependent behavior of these photodiodes can be determined by plotting the dark current density as a function of the photodiode perimeter divided by the photodiode area at a specific voltage as shown below [58]:



(a) (b)

Figure 4.7 Extraction of Perimeter and Area components of the photodiode reverse bias leakage current at a bias of –1 volt.

(a) Perimeter dependent current photodiodes have a dark current density of ~2.6 mA/cm^2, and are perimeter dependent for photodiodes less than 1 x 1 mm^2 in size. Photodiodes are from wafer 11-8.

(b) Area dependent current photodiodes have a dark current density of 8.5 mA/cm^2 and are area dependent for photodiodes down to the smallest size measured of 10 μm square. Photodiodes are from wafer 20-12.

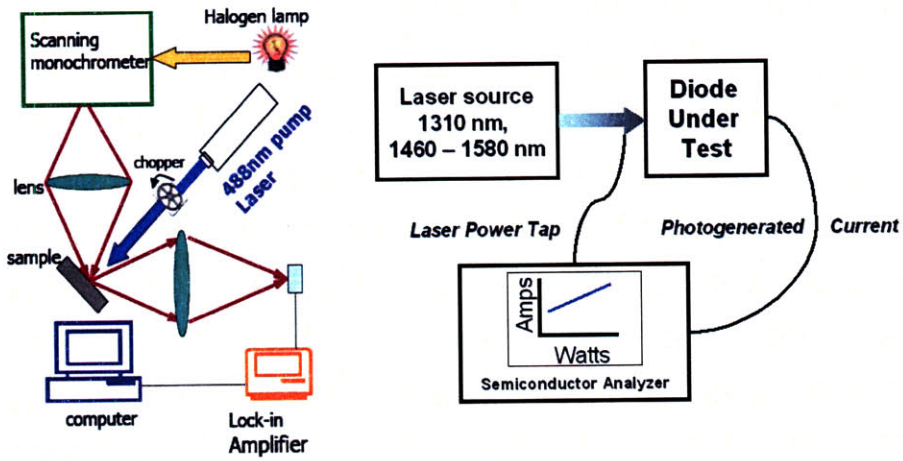
$$I_D(V) = J_P(V) * Perimeter + J_A(V) * Area \qquad \text{(Equation 4.3)}$$

$$J_D(V) = J_P(V) * \frac{Perimeter}{Area} + J_A(V) \qquad \text{(Equation 4.4)}$$

where I_D is the dark current, J_D is the dark current density, J_P stands for the perimeter coefficient in mA/cm and is the slope of Equation 4.4 and J_A is the area coefficient in mA/cm^2, and is the y-intercept of Equation 4.4. As shown in Figure 4.7, the reverse bias leakage current from wafer 11-8 is perimeter dependent for photodiodes less than 1 x 1 mm^2 in size. On the other hand, the reverse bias leakage current from wafer 20-12 is observed to be area dependent for photodiodes sizes down to the smallest dimensions fabricated of 10 x 10 μm^2. The PD photodiodes had an area dependent leakage value of ~2.4 mA/cm^2 at a –1

volt bias and the AD photodiodes had an area dependent leakage of ~8.5 mA/cm^2 at a –1 volt bias. Please see Appendix G for a further discussion of the source of the difference between the area dependent leakage values for these two types of photodiodes.

From the data in Figure 4.7, it is clear that the leakage current for the photodiodes in wafer 20-12 are area dependent, primarily because the perimeter coefficient, J_P, is so small. Specifically, the perimeter coefficient, J_P, is reduced by three orders of magnitude for wafer 20-12 relative to wafer 11-8, while the area coefficient, J_A, is within a factor of four for the photodiodes on both wafers. Thus, it appears that the processing on wafer 20-12 led to a significantly reduced perimeter leakage, relative to all other wafers analyzed in this work. The analysis in Section 4.3.3 attempts to explain the physical origin of this large difference in the perimeter leakage coefficients for these two wafers. A more accurate area coefficient for the PD photodiode will also be extracted in Appendix G.



(a) (b)

Figure 4.8 Various responsivity measurements setups (Images are courtesy of Jifeng Liu and Jason Orcutt):
(a) Overfill measurements using a broad spectrum halogen lamp source covering 1 to 1.7 μm wavelengths
(b) Underfill and overfill measurement setup using a 1310 nm CATV laser and a 1460 to 1580 nm tunable laser. In underfill operation, this setup was used to perform responsivity scans across the photodiode surface.

4.3 Material and Optical Measurements

Detailed optical and material measurements were performed on the best photodiodes from PD wafers 11-7, 11-8, and AD wafer 20-12 mentioned in the prior section. These include responsivity measurements, photoemission studies, Scanning Electron Microscopy (SEM), and Cross Sectional Transmission Electron Microscopy (XTEM). Secondary Ion Mass Spectroscopy (SIMS) and Spreading Resistance Profiling (SRP) were also performed for wafer 11-7.

4.3.1 Photodiode responsivity measurements

For the sake of clarity, responsivity measurement nomenclature will be defined at this stage. During the responsivity measurement, if the illumination spot size is less than the photodiode active area, this is specified to be an underfill measurement. Conversely, if the illumination spot size is greater than the photodiode active area, the responsivity measurement is an overfill measurement. As shown in Figure 4.8 (a) the responsivity of the PD photodiode without antireflection coating was measured by a broad spectrum halogen lamp that is filtered to a specific wavelength, with a 3 mm diameter illumination region. Thus, the halogen lamp setup tends to be an overfill measurement because the photodiode sizes range between 10 to 1000 μm in their widest lithographically defined dimension. Using this overfill measurement for a 100 x 100 μm^2 Ge-on-Si *pin* PD photodiode, the responsivity was extracted as a function of the wavelength, with a 0.5 A/W responsivity at 1550 nm wavelength. In order to conduct an underfill measurement, the same set of 100 x 100 μm^2 photodiodes.

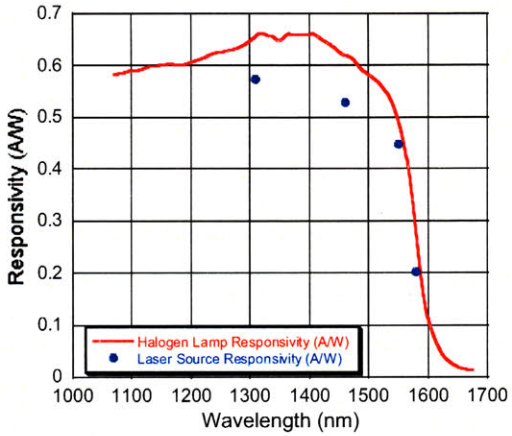


Figure 4.9 Responsivity data for 100 μm x 100 μm photodiodes biased at –1 volt using an overfill halogen lamp illumination with a 3 mm diameter spot size (solid red line) and an underfill laser illumination with a 2.5 μm diameter spot size (blue circles). The dark current for the diode measured by lamp illumination was 1.6 μA and for the diode measured by laser illumination was 10 μA. The halogen lamp responsivity values are 45 – 92 mA/W higher than the laser lamp responsivity values. Measurements are courtesy of Jifeng Liu (halogen lamp) and Jason Orcutt (underfill fiber laser).

were illuminated at 1550 nm wavelength with a laser source with a 2.5 to 5 μm illumination diameter as shown in Figure 4.8 (b). In this underfill measurement, the responsivity for a 100 x 100 μm^2 Ge-on-Si *pin* PD photodiode was extracted to be between 0.4 to 0.45 A/W at 1550 nm. Generally, as shown in Figure 4.9, at the wavelengths measured in the laser setup of 1310, 1460, 1550, and 1580 nm, the halogen lamp illumination responsivity measurements had a 45 to 92 mA/W greater responsivity value.

To further correlate these two measurements, overfill measurements were performed with the laser source by vertically displacing the laser lens fiber upwards from the focal point, thereby increasing the illumination diameter. This measurement showed that the responsivity *actually* dropped as the diameter of the laser illumination reached the size of the photodiode active area and stabilized to

around 0.32 to 0.36 A/W for a 1550 nm wavelength at illumination diameters above 100 microns as shown in Figure 4.10 (a). Thus, there appeared to be a 40

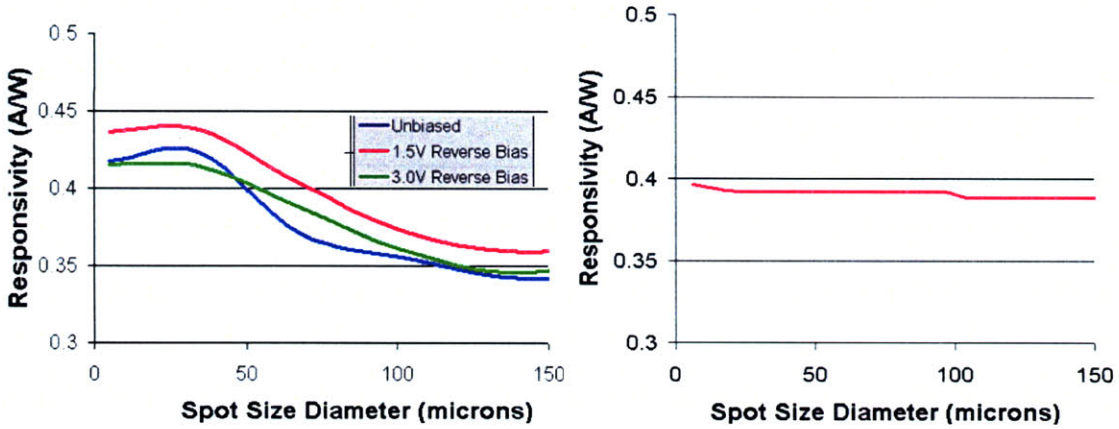


Figure 4.10 Responsivity measurements of 100 μm x 100 μm photodiodes laser illumination with a variable illumination diameter. Measurements are courtesy of Jason Orcutt.
(a) PD photodiode responsivity results show a decrease in the responsivity from 0.44 A/W to 0.36 A/W as the photodiode active area becomes overfilled.
(b) AD photodiode responsivity results show a constant responsivity of 0.39A/W throughout the active area.
The photodiode is biased at –1 volt.

to 50 % discrepancy between the halogen lamp illumination and the laser illumination overfill measurements.

To verify the accuracy of the overfill laser illumination measurements, the existence of a responsivity "dead zone" implied by the drop in the measured responsivity as the photodiode approached overfill illumination was tested by performing spatial measurements of the photodiode responsivity with a 5 μm diameter laser illumination at a 1545 nm wavelength. These measurements led to the confirmation of an ~5 to 7 μm responsivity "dead zone" around the perimeter of 20 x 100 μm^2, 40 x 100 μm^2 and 100 x 100 μm^2 photodiodes as shown in Figure 4.11. These spatially dependent laser measurements also confirmed that

the halogen lamp overfill illumination measurements overestimated the photodiode responsivity. It is possible that the halogen lamp illumination

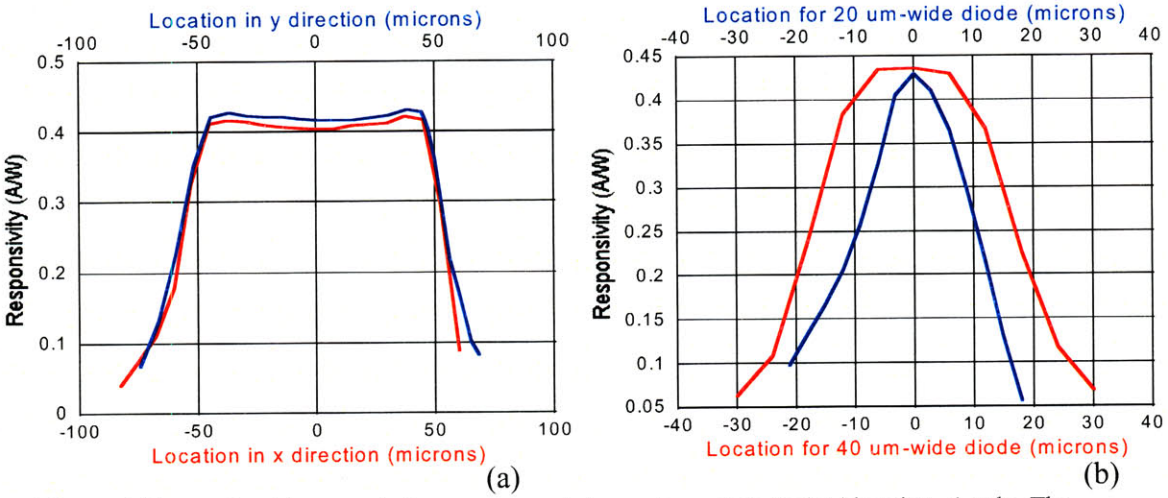


Figure 4.11 Spatial responsivity measurements for various photodiodes biased at –1 volt. The photodiodes were illuminated with a 2.5 μm diameter spot size at a wavelength of 1545 nm. The center of the photodiode is designated to be located at the origin of the cartesian plane for these measurements. A ~ 5 to7 μm responsivity "dead zone" was seen around the perimeter of all the PD photodiodes. Measurements are courtesy of Jason Orcutt.

(a) PD photodiode responsivity results for 100 μm x 100 μm photodiode show symmetric dead zones in the x (red) and y (blue) directions.

(b) PD photodiode responsivity results for 20 μm x 100 μm (blue) and 40 μm x 100 μm (red) photodiodes show a similar responsivity dead zone. For the smaller diodes, the responsivity dead zone actually appears larger than in larger photodiodes.

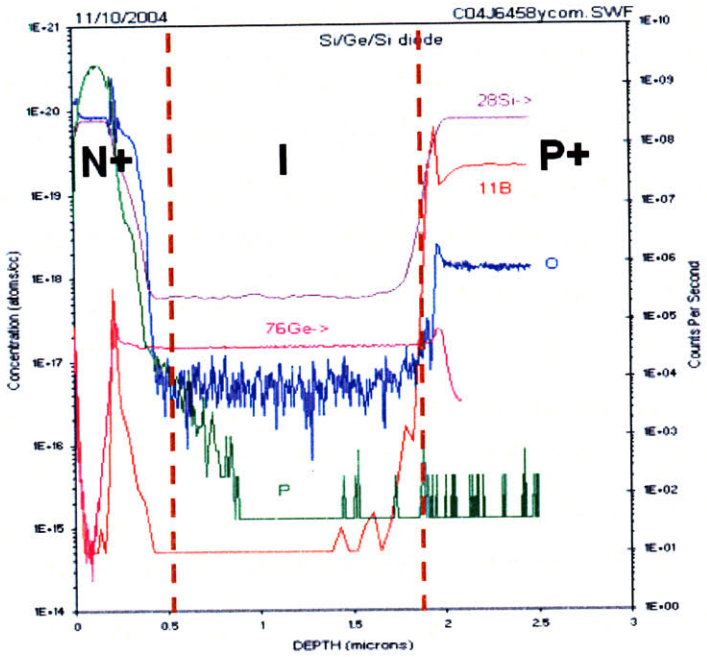
method does not accurately calibrate for the optical power being delivered to the photodiode, leading to the overestimate in the responsivity measurements.

Since the current for the PD photodiode is perimeter dependent, it is hypothesized that this perimeter "dead zone" is probably due to a trap mediated generation/recombination zone, and is also the source of the dark current due to the combination of high traps and a high electric field [73].

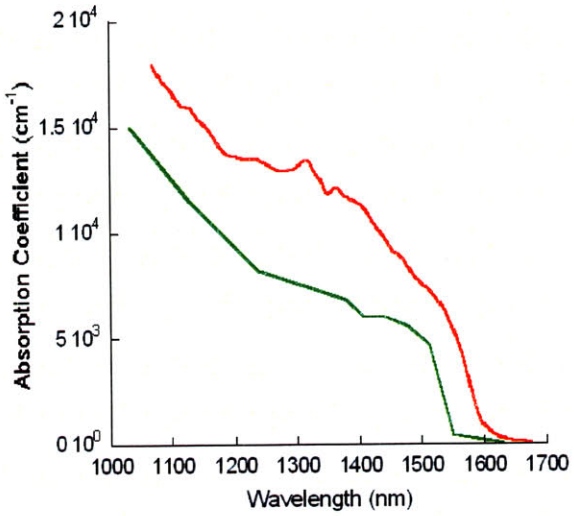
As shown in Figure 4.10 (a), the responsivity measurements of the PD photodiode did not show a strong variation of the responsivity as a function of

voltage. Under zero bias the responsivity was within 7% of the –1.5 volt bias responsivity, showing the built in fields in the photodiodes are quite high. As the photodiode bias is increased to –3 volt, the responsivity drops down to the zero bias condition. This reduction in responsivity might be associated with the exposure of the Ge/Si heterointerface as the width of the depletion region increases under reverse bias. The exposure of a valence band barrier in Ge-on-Si heterojunction photodiodes leads to an impeded flow of photogenerated carriers to the contacts, lowering the observed photoresponse [74]. Similar responsivity measurements were performed for an AD photodiode without an antireflection coating on the laser measurement setup. The responsivity in the center of the photodiode was found to be 0.4 A/W at 1545 nm wavelength when the photodiode is biased at –1 volt. As shown in Figure 4.10 (b), when the illumination spot size of the laser source was varied during measurements, there was no evidence of an associated responsivity "dead zone" for the AD photodiode.

Using the responsivity measurements from Figure 4.9 and the SIMS measurements of the PD photodiode shown in Figure 4.12 (a), the absorption coefficient versus wavelength curve shown in Figure 4.12 (b) was extracted. The reflection loss was determined to be between 0.3 to 0.4 for the wavelengths of interests from transmission matrix simulations by Jason Orcutt and Jifeng Liu, and the depth of the Ge film from the SIMS measurement was found to be 1.4 μm. A collection efficiency of 0.9 was assumed from bias dependent responsivity



(a)



(b)

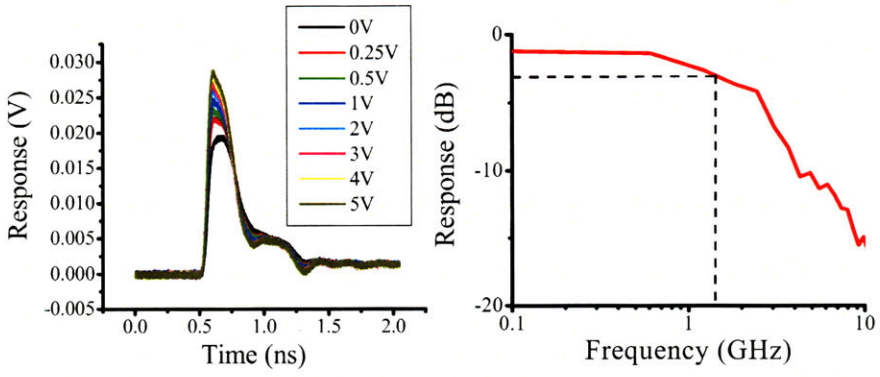
Figure 4.12 (a) SIMS plot of a PD photodiode with the P+, I, N+ regions highlighted. (b) Extracted absorption coefficient for the PD photodiode versus wavelength at zero bias (solid red), and the bulk germanium absorption coefficient (solid green). Bulk Ge data from Palik, *et al* [59].

measurements shown in Figure 4.10 (a). The absorption coefficient at 1550 nm for the PD photodiodes is ~ 5.5 x 10^3 cm^{-1}, with an associated quantum efficiency of ~50%. The wavelength cutoff of 1.61 μm corresponds to a ~ 30 meV shrinkage of the direct bandgap of Ge (from 0.8eV to 0.77eV). The extracted absorption coefficient of these germanium films is 2.5x higher than the directly measured absorption coefficient estimated from measurements on experimental

wafers described in Section 3.5. Part of the improved absorption coefficient can be attributed to the accurate intrinsic film thickness of 1.4 μm that can be extracted from the SIMS data on the photodiodes in Figure 4.12 (a). The SIMS data also shows the existence of a 0.4 μm-thick $Si_{1-x}Ge_x$ region near the Ge epi/Si substrate interface, that when factored into the results from the absorption coefficient study in Section 3.5 would increase the absorption coefficient for longer wavelengths. The remaining deviation between the two studies can be ascribed to differences in tensile strain due to the ~ 200°C higher annealing temperatures the PD photodiode wafers are exposed to.

4.3.2 Frequency measurements

High speed measurements were also performed on the PD photodiode. Two experimental methods of determining the 3-dB frequency were implemented, along with a third approach that is based upon a simple RC time constant calculation. The first 3-dB frequency measurement method was an impulse response measurement, followed by a Fast Fourier Transform (FFT) to extract the 3-dB frequency point. The second 3-dB frequency measurement method was via the magnitude of the measured photocurrent generated by frequency dependent illumination from a vertical cavity surface emitting laser (VCSEL). Finally, a rough estimate of the 3-dB frequency was obtained by measuring the series



(a) (b)

Figure 4.13 (a) Impulse response measurement versus bias for a 20 x 100 μm photodiode illuminated at 1.04 μm with a 1 picosecond pulse. The photoresponse exhibits a fast carrier generation time of ~100 ps, but a 7x longer carrier collection time. (b) Fast fourier transform of the photoresponse shows a 3-dB frequency of ~1.2 GHz. Measurements and analysis are courtesy of Jifeng Liu.

resistance and capacitance of the photodiodes and calculating the associated bandwidth due to the RC delay from Equation 2.10.

For the high-speed impulse response measurement, a Tektronix 11801C digital oscilloscope with a SD-32 50 GHz sampling head was used to measure the temporal response of the photodiodes to a mode-locked Yb-fiber laser at 1040 nm. The laser produces chirped pulses, with a 1 picosecond duration utilized for these measurements. A 50 GHz ground-signal-ground probe, with a 50 GHz bias-T, and 3.5 mm microwave cables were used in the measurement circuit.

Utilizing the impulse response method, the impulse response of a 20 x 100 μm^2 photodiode is shown in Figure 4.13 (a). At a –5 volt bias, the photodiode is measured to have a 3-dB frequency of 1.2 GHz as shown in the fast fourier transform in Figure 4.13 (b). The impulse response shows the 100 ps rise time of the photodiode that is 7 times faster than the fall time of 700 ps. The periodic

ripples in the long fall time may be associated with interfacial trap states at the N^+-polysilicon, dielectric, and Ge boundaries [75]. The ripples in the fall time of

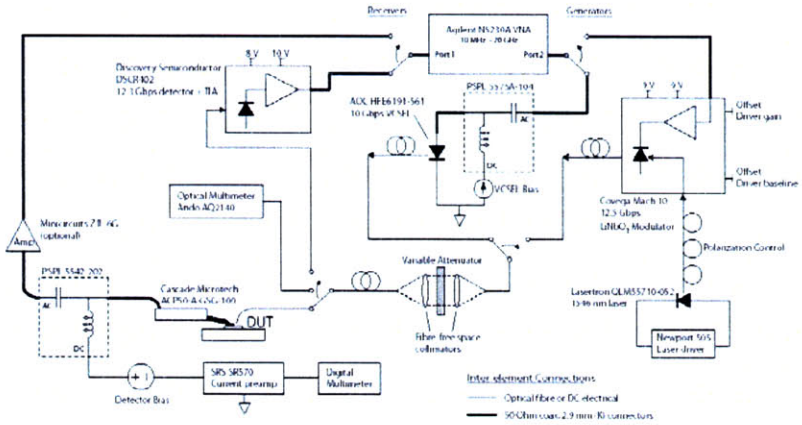


Figure 4.14 VCSEL high speed measurement setup. The frequency of the incoming 850 nm laser source is swept from 1 MHz to 5 GHz. The magnitude of the generated photocurrent is measured and used to extract the 3-dB frequency. Sketch is courtesy of Wojciech Giziwieciz.

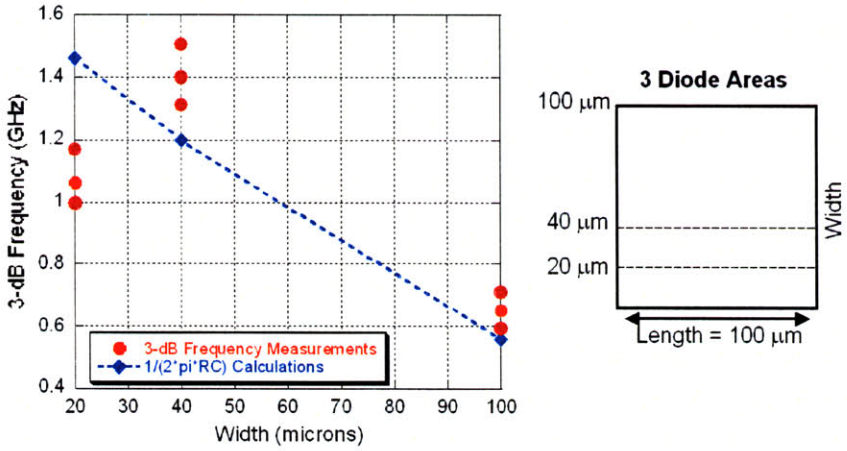


Figure 4.15 Comparison of measured 3-dB frequency measurements and estimated time constant calculations. As the area of the device decreases, it is expected that the measured frequency response increases or stays constant. This trend holds constant for all the time constant measurements and is borne out in the 3-dB frequency measurements for the 100 µm x 100 µm and 40 µm x 100 µm photodiodes. The measured 3-dB frequency response drops for the 20 µm x 100 µm photodiodes, which is possibly attributed to high concentration of trap states shown in Figure 4.13 (a) that introduce additional delay in the carrier collection time. Measurements are courtesy of Wojciech Giziwieciz.

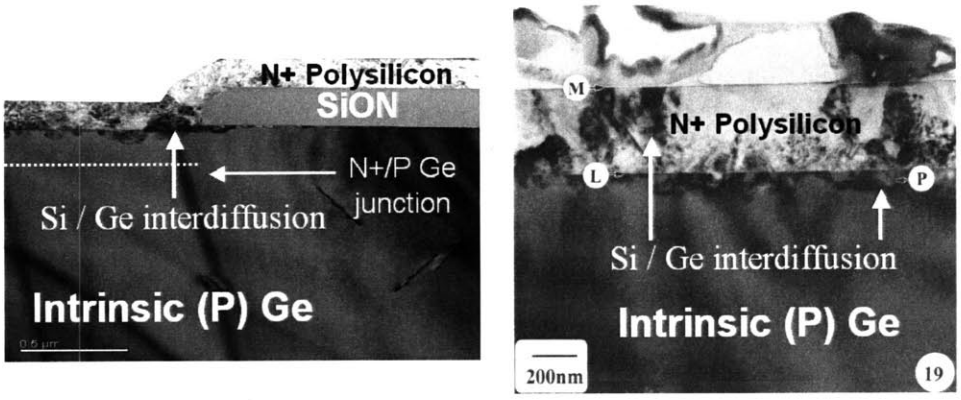
the unit impulse response appear to have a period of 350 picoseconds. This long fall time is believed to be the limiting factor in the frequency response of the photodiodes.

To further investigate the frequency response of these photodiodes, the 3-dB frequency of various photodiodes were measured using the VCSEL measurement setup, shown in Figure 4.14 at a wavelength of 850 nm, and were also estimated using their RC time constants. As shown in Figure 4.15, a 40 μm x 100 μm photodiode biased at –5 volts was measured to have a 3-dB frequency of 1.5 GHz. The measured 3-dB frequency of the 100 μm x 100 μm and the 40 μm x 100 μm photodiodes scale with the area of the photodiode, indicating that they are RC limited, but the measured 3-dB frequency of the 20 μm x 100 μm photodiodes actually drops relative to that of the 40 μm x 100 μm photodiodes. The RC time constant for all three photodiode sizes indicates that the 3-dB frequency should increase as the area decreases. Thus, it appears that the intrinsic transit time delay of the 20 x 100 μm^2 photodiode is the limiting factor, not the parasitic RC delay. It is hypothesized that since 55 to 75% of the 20 μm x 100 μm photodiode surface area is associated with a trap dominated zone, apparent in the responsivity measurements, it is likely that the transit time limitation is imposed by the trap mediated process shown in the impulse response measurement. This recombination/generation region could lead to the lowered measured 3-dB frequency for the 20 μm x 100 μm photodiodes relative to the 40 μm x 100 μm photodiodes. Thus it appears that the transit time limitation might

be due to carriers generated close to or in the trap dominated region around the perimeter of the PD photodiode.

4.3.3 Transmission Electron Microscopy Analysis

In order to further examine the material quality of the polysilicon, germanium, and dielectric interfaces, samples were sent to an outside analysis firm for cross sectional TEM analysis. TEM analysis was performed on both the PD and AD photodiodes, though in different studies and at different outside



(a) (b)

Figure 4.16 (a) TEM analysis of a PD photodiode. There are Si/Ge interaction regions along the polysilicon/germanium interface and also extend at least 0.3 μm underneath the SiON dielectric film. (b) TEM analysis of an AD photodiode. There are similar Si/Ge interactions as the PD photodiode at the polysilicon/germanium interface, but there was minimal extension of the Si/Ge interaction below the dielectric film (not shown in figure). TEM analysis courtesy of Analog Devices, Inc.

analysis firms. As shown in Figure 4.16 (a), a cross sectional TEM micrograph from a PD photodiode, there are regions of silicon and germanium (Si/Ge) interaction at the polysilicon and germanium interface. These Si/Ge nodules are hypothesized to be due to weak regions in the native germanium oxide passivation

film through which the Si and Ge diffused [76]. The Si/Ge regions appear to extend at least 25 nm, and up to a maximum value of approximately 100 nm, below the surface of the germanium film. The Si/Ge regions also appear to extend laterally at least 0.3 microns under the silicon oxynitride passivating layer. The existence of the Si/Ge region under the dielectric might be due to the dielectric etch step. The final step of the etch process is a wet etch of an approximate 50 nm-thick dielectric layer, with a 100% overetch time, thus easily leading to a 50 nm undercut. Approximately 60% of the polysilicon and germanium interface was found to be capped by the Si/Ge particles.

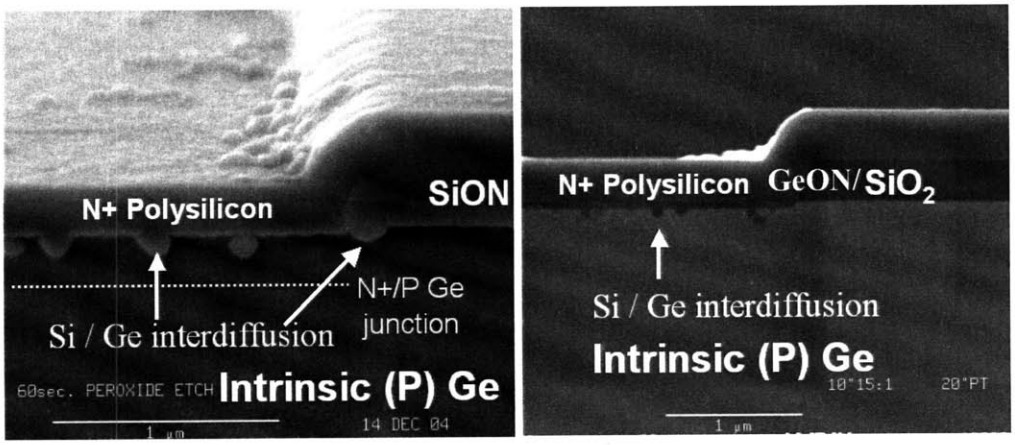
Electron Diffraction Spectrometry (EDS) analysis was also performed on the perimeter dependent photodiode active region. It was found that the Ge diffused up to 150 nm into the polysilicon cap layer, and that there were silicon and oxygen signals in the germanium film down to a depth of at least 150 nm.

TEM analysis was also performed on the AD photodiodes, on a sample from the low leakage (8.5 mA/cm^2) section of wafer 20-12 and a sample from the high leakage section of wafer 20-12 (4 A/cm^2). Both samples examined have been found to be generally similar to one another with the polysilicon and germanium interface being notable for containing a high density of Si/Ge particles that are characteristically faceted in the <111> direction and exhibit a tendency to have porous cores. Similarly to the PD photodiode, the Si/Ge formation extends to a maximum depth of some 150 nm beneath the surface of the germanium film. As shown in Figure 4.16 (b), ~65% of the surface of the polysilicon and germanium

interface was found to be capped by Si/Ge particles, which tended to have higher defect content in the immediate region surrounding them.

Unlike the PD photodiodes, both the high and low reverse bias leakage regions of the AD wafer show evidence that very little (≤ 50 nm lateral extent) Si/Ge interaction has taken place between the germanium layer and the GeON/LTO layer overlying it. The only significant differences between the high and low leakage samples is the tendency for the Ge surrounding the Si/Ge particles to be of higher dislocation content in the high leakage than the low leakage sample.

Thus, in a comparison between the PD and AD photodiode TEM analysis, it appears that the Si/Ge particles occur at the germanium and polysilicon interface



(a) (b)

Figure 4.17 (a) SEM analysis of a PD photodiode. There are Si/Ge interaction regions along the polysilicon/germanium interface and also underneath the SiON dielectric film. (b) SEM analysis of an AD photodiode. There are similar Si/Ge interactions as to the PD photodiode at the polysilicon/germanium interface, but there was no evidence of an extension of the Si/Ge interaction below the dielectric film. SEM analysis courtesy of Analog Devices, Inc.

for both types of photodiodes. On the other hand, Si/Ge particles extend significantly under the passivating film only for the PD photodiode. These conclusions have also been confirmed by Scanning Electron Microscopy (SEM) analysis with hydrogen peroxide (H_2O_2) etching to highlight the Si and Ge interaction regions as shown in Figure 4.17. The AD photodiodes did not show evidence of Si/Ge interaction underneath the dielectric while the PD photodiodes again show that there is a Si/Ge interaction region under the passivation layer. Moreover it is hypothesized that the Si/Ge region directly underneath the polysilicon and germanium interface is in a quasi neutral phosphorus implanted region without a high electric field, and hence does not contribute significantly to the leakage current, unlike the perimeter Si/Ge region that is outside the quasi neutral phosphorus implanted region [77]. This perimeter Si/Ge interaction zone is in the presence of a high electric field that exists at the N+/P germanium metallurgical junctions. Finally, it appears that the higher clusters of dislocations around the Si/Ge interaction regions might play a role in increasing the leakage current as seen in the TEM analysis for the AD low and high leakage photodiodes.

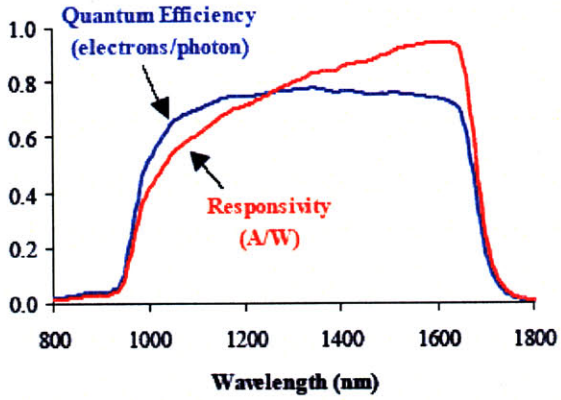


Figure 4.18 Spectral response of InGaAs photodetector utilized in the photoemission study.

4.3.4 Photoemission study

In order to gain an idea of the spatial current distribution of the photodiodes, near infrared images were taken of the PD and AD photodiodes under high reverse or forward bias, in the laboratory of Professor Mark Somerville at Olin College. The detector utilized for the study was a hyperspectral InGaAs photodetector. As shown in Figure 4.18, the photodetector had a responsivity of 0.5 to 0.9 A/W for the wavelength range between 950 nm to 1700 nm. Wavelength specific filters were also utilized. These filters had a 100 nm window allowing fifty to seventy-five percent transmission at the desired wavelengths. Eight filters were used to examine 100 nm windows between 950 to 1750 nm.

For the PD photodiodes with high reverse bias, a 3 to 5 μm wide spatial photoemission region at the perimeter of the photodiodes and within the polysilicon overlap with the dielectric region was observed. A representative image is shown in Figure 4.19. Using the filters, it was determined that the photoemission exists between 0.95 to 1.65 μm (1.31 to 0.75eV). In forward bias

the photoemission region existed primarily around the polysilicon and metal contact regions. Using the filters it was noted that there is a sharp dropoff at 1.31 eV and at 0.75 eV. In reverse bias for the AD photodiode, photoemission exists below 1.65 micron (energies greater than 0.75 eV), with a sharp dropoff at 0.75 eV, probably due to the InGaAs detector cutoff. In forward bias for the AD photodiode, emission exists only between 1.35 to 1.65 μm (0.92 to 0.75 eV). Outside this range, no photoemission was detected and thus the photoemission can be primarily attributed to the Ge bandgap.

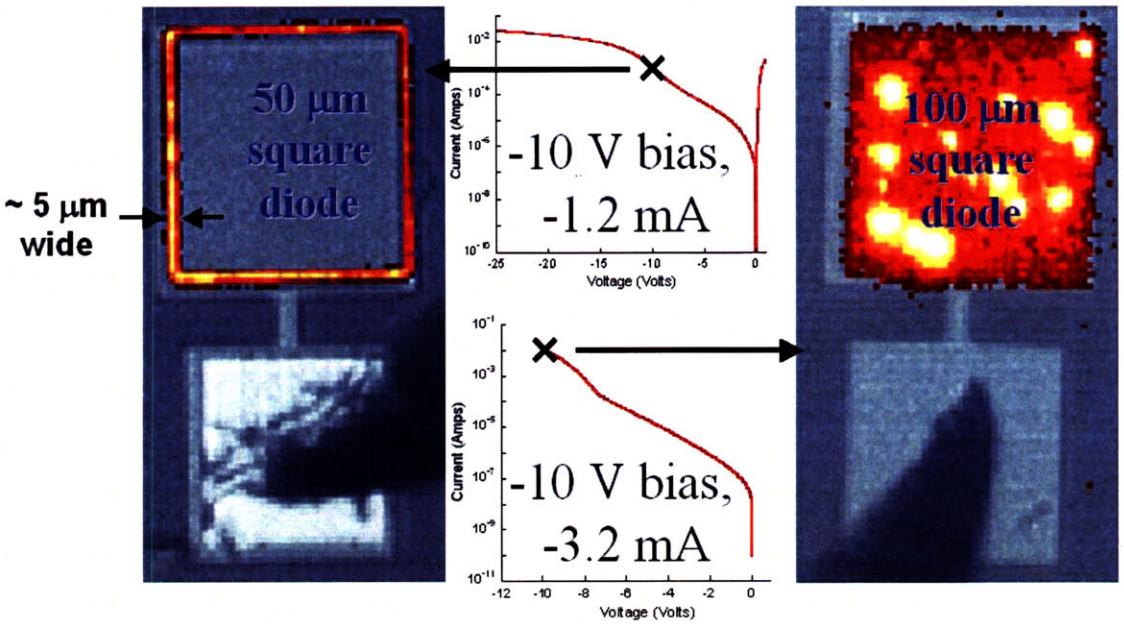


Figure 4.19 (a) Photoemission spectrum for a 50 μm x 50 μm PD photodiode. The photodiode was biased at –10 volts with a reverse bias leakage current of 1.2 mA. The reverse bias leakage current is located in a 3 – 5 μm continuous band around the perimeter of the photodiode. (b) Photoemission spectrum for a 100 x 100 μm^2 AD photodiode. The photodiode was biased at –10 volts with a reverse bias leakage current of 3.2 mA. The reverse bias leakage current is distributed evenly throughout the photodiode. Nominal I-V curves for both photodiode types are shown, with markers to show bias region for photemission measurements. Measurements are courtesy of Professor Mark Somerville.

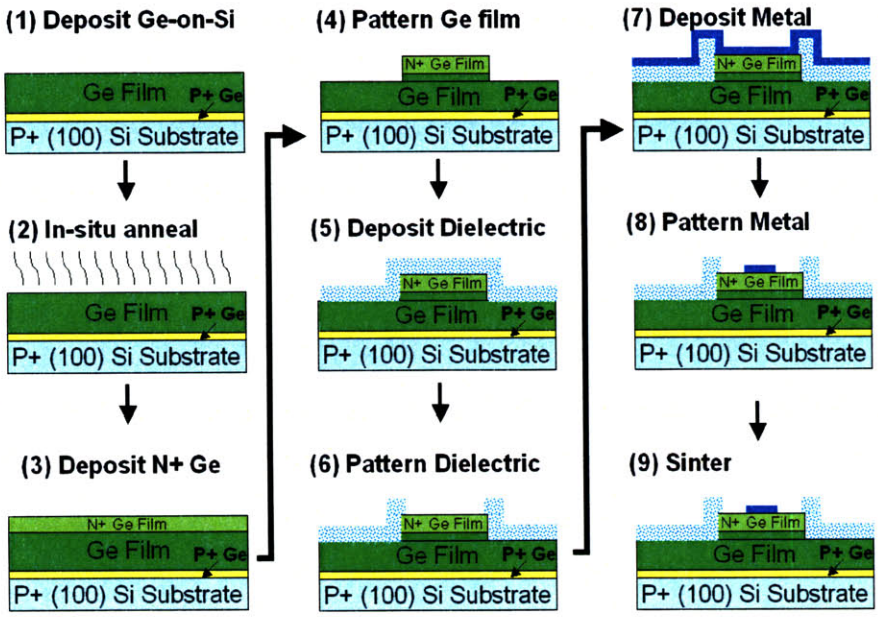


Figure 4.20 Generic fabrication process for mesa isolated Ge-on-Si *pin* photodiodes.

4.4 Mesa isolated Ge-on-Si *pin* photodiode

Due to the overlap of the Si/Ge interaction zone with the photoemission region and responsivity dead zone for the perimeter dependent photodiodes, it was hypothesized that the combination of polysilicon and a high thermal budget might be the source of the photodiode leakage current. To verify the effect of a low thermal budget and not having polysilicon as an N+ contact layer, *in-situ* annealed germanium films composed of 0.1μm p+, 1.5 μm intrinsic, and 0.2 μm n+ regions were deposited and mesa isolated photodiodes were fabricated.

4.4.1 Mesa isolated Ge-on-Si *pin* photodiode fabrication

As shown in Figure 4.20, the first process step was depositing a Ge-on-Si film with a 5 x 10^{19} cm^{-3} boron doped 60 nm-thick Ge seed, followed by a 1.5

μm-thick intrinsic Ge cap layer. The film was then *in-situ* annealed at 830°C for 30 minutes and an 8 x 10^{18} cm^{-3} phosphorus doped 0.2 μm-thick layer was deposited. The phosphorus layer was deposited after the *in-situ* anneal in order to avoid excessive phosphorus diffusion into the germanium intrinsic region during the anneal process [78].

Following the germanium deposition steps, photoresist was spun and hardbaked onto the Ge-on Si film. Then the wafer backside was etched in order to remove the $Si_{1-x}Ge_x$ film from the germanium film that has deposited onto and then diffused into the backside of the wafer. The photoresist was then removed from the wafers in an oxygen plasma and an image reversal photoresist was deposited. The mesa isolated photodiode active region was then defined with a wet etch to remove the N+ germanium layer. Following this step, the photoresist was ashed, and the passivation layer was reacted and/or grown onto the germanium film. Photoresist was patterned and metal contact vias to the N+ active region are then created, using a dry then wet etch process into the passivating film. The contact metal was then deposited onto the germanium film and the metal layer was patterned. At this stage the mesa isolated *pin* photodiode fabrication is complete, but an optional sintering step to ensure a low series resistance could be included.

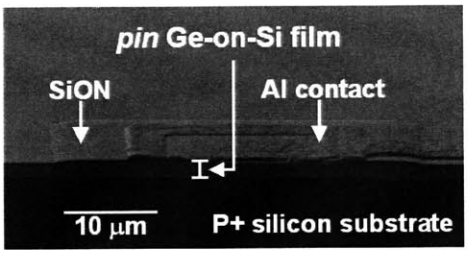


Figure 4.21 Cross sectional SEM image of a mesa isolated 40 μm x 40 μm *pin* photodiode.

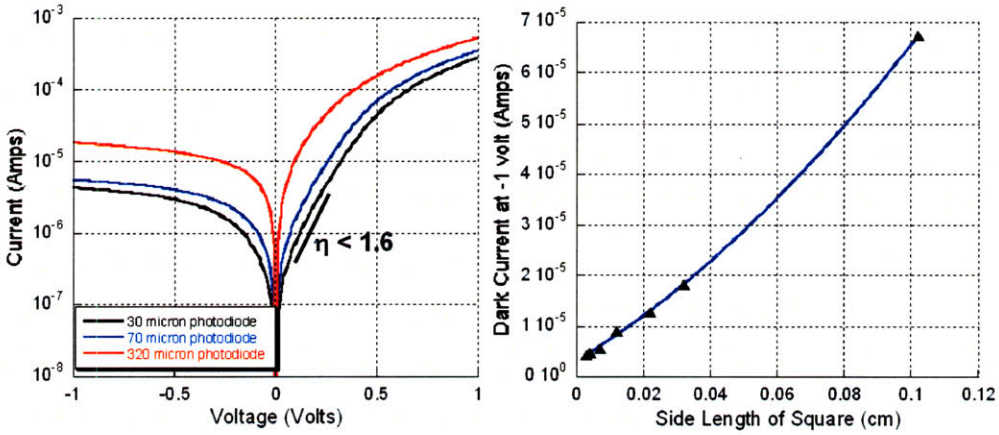
4.4.2 Electrical, optical, and material measurements on mesa isolated photodiodes

One mesa isolated *pin* photodiode wafer, with a representative SEM image shown in Figure 4.21, was successfully fabricated. The photodiode passivation layer was a GeO_xN_y layer grown by an RTP system using a 240 second nitridation process followed by a 0.3 μm-thick SiON film deposited in the DCVD system. The sidewall of the mesa was defined to be 0.4 microns deep, terminating in the intrinsic germanium film. The top contact was defined using a 0.75 μm-thick aluminum film. The current-voltage measurements showed that the ideality factor of the diodes was less than 1.6 for bias between 0.05 to 0.1 V. The series resistance of the diodes was generally in the range of 25 to 75 ohms, depending on the fraction of the N+ Ge active region contacted by the aluminum. The reverse bias leakage current appears to scale with the perimeter. Since the leakage current for circles and squares of comparable surface area generally had lower leakage for the circles, it was postulated that the corners of the mesa also had an effect on the leakage. Thus, the complete version of Equation 4.3 was utilized to analyze the dark current as shown below [58]:

$$I_D(V) = J_P(V) * Perimeter + J_A(V) * Area + I_C(V) * Corners + I_U(V) \quad \text{(Equation 4.5)}$$

where $I_C(V)$ stands for the current from one corner of a photodiode; Corners stands for the number of corners on the photodiode; $I_U(V)$ stands for the anomalous sources of dark current, such as the high leakage point shown on the left boundary of the photoemission spectrum in Figure 4.24 (a); and the remaining parameters have the same prior designations.

After performing this analysis at –1 volt, J_P was determined to be 0.1 mA/cm, J_A was determined to be 2.18 mA/cm^2, I_C was determined to be 0.25 μA, and I_U was determined to be 2.04 μA. Thus, for square photodiodes, the perimeter leakage dominates for photodiodes less than 1.8 x 1.8 mm^2 in size, and the total current density is ~2.6 mA for a 1 cm^2 area. The reverse bias leakage current also had a square root dependence on the applied bias, showing that without the Si/Ge interaction, the reverse bias leakage current did not have a tunneling characteristic. Looking at the description of dark current components discussed in Chapter 2, the behavior of the mesa isolated dark current is ascribed to surface



(a) (b)

Figure 4.22 (a) I-V measurements for various sized mesa isolated Ge-on-Si *pin* photodiodes. The reverse bias current scales as a function of the square root of the magnitude of the voltage. The forward current scales as a function of the metal contact perimeter and reverse bias current scales a function of the perimeter of the photodiode active area.
(b) Reverse leakage analysis of square mesa isolated Ge-on-Si *pin* photodiodes. Using equation 4.5 and the calculated parameters of J_P=0.1mA/cm, J_A=2.2 mA/cm^2, I_C=0.25 μA and I_U = 2.04 μA, an excellent fit (blue line) to the measured data (black triangles) is generated. Perimeter leakage dominates for square photodiodes less than 1.8 x 1.8 mm and the total current density is ~2.6 mA/cm^2.

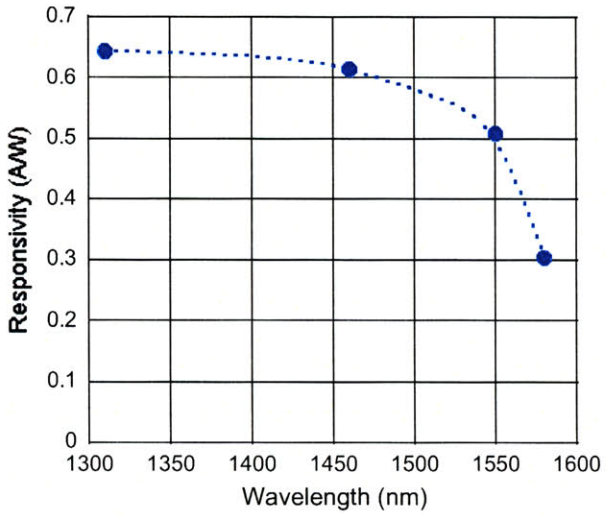
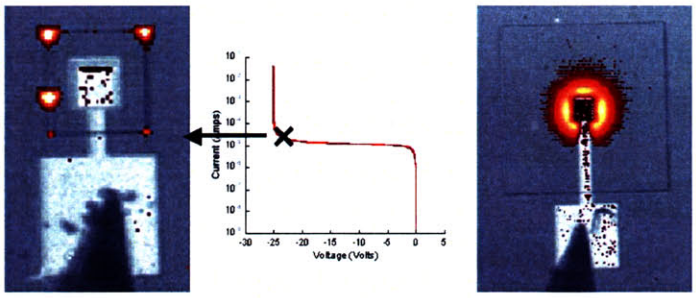


Figure 4.23 Responsivity measurements of 120 μm x 120 μm photodiodes biased at –1 volt with a 10.2 μA dark current illuminated with a 2.5 μm diameter spot size (blue circles). Measurements are courtesy of Jason Orcutt.

or bulk generation components. As shown in Figure 4.24 (b), the forward bias current was also found to scale with the perimeter of the metal contact area.

Responsivity measurements using the laser setup are shown in 4.23. These responsivity measurements yield a value of 0.51 to 0.55 A/W at a wavelength of 1.55 um and a bias of –1 volt. The higher responsivity value for the mesa isolated *pin* photodiodes is due to a 13% reflectance loss, relative to the 37% reflectance loss for the blanket Ge-on-Si *pin* photodiode. When this lower reflectance loss is factored into the calculations, the mesa isolated *pin* photodiode has an absorption coefficient of ~5.5 x 10^3 cm^{-1} and an external quantum efiiciency of ~50%, similar to the PD photodiodes. In order to ascertain the physical location of the reverse bias leakage current, photoemission studies of the mesa-isolated photodiode were conducted. As Figure 4.24 shows, the location of the reverse bias leakage current, near the breakdown of the device, appears to be

around the perimeter and corner regions of the active device area. These locations are the regions where there is an exposed sidewall with the possibility of



(a) (b)

Figure 4.24 (a) Photoemission spectrum in reverse bias for a 70 μm x 70 μm mesa isolated Ge-on-Si *pin* photodiode. The photodiode was biased at –24 volts with a reverse bias leakage current of 0.14 mA. The reverse bias leakage current is located in at the corners and the perimeter of the photodiode. Nominal representative I-V curve for mesa isolated photodiode is shown, marker shows photoemission measurement is taken at a bias prior to breakdown. (b) Photoemission spectrum in forward bias for a 220 x 220 μm mesa isolated Ge-on-Si *pin* photodiode. The photodiode was biased at 5 volts with a current of 11.3 mA. The forward current is distributed around the metal contact of the photodiode. Measurements are courtesy of Professor Mark Somerville.

increased surface states and also regions with the highest electric fields [79]. In both forward and reverse bias photoemission exists only in the wavelength range between 1.35 to 1.65 μm (0.92 to 0.75 eV), as is expected for a *pin* photodiode structure composed purely in a germanium film.

4.5 Selective Ge-on-Si *pin* photodiode fabrication process

In order to integrate Ge-on-Si photodiodes onto the silicon CMOS process, it is desired to selectively deposit epitaxial Ge-on-Si films in trenches etched into a masking layer. Moreover, as has been demonstrated in Section 3.3.4, as the trench widths drop, after a cyclic anneal, the dislocation density in

the Ge-on-Si film drops dramatically, greatly improving the material quality. This reduction in dislocation density is an additional benefit of utilizing SEG films for fabricating Ge-on-Si photodiodes.

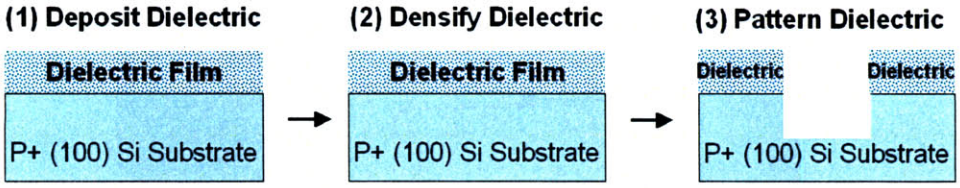
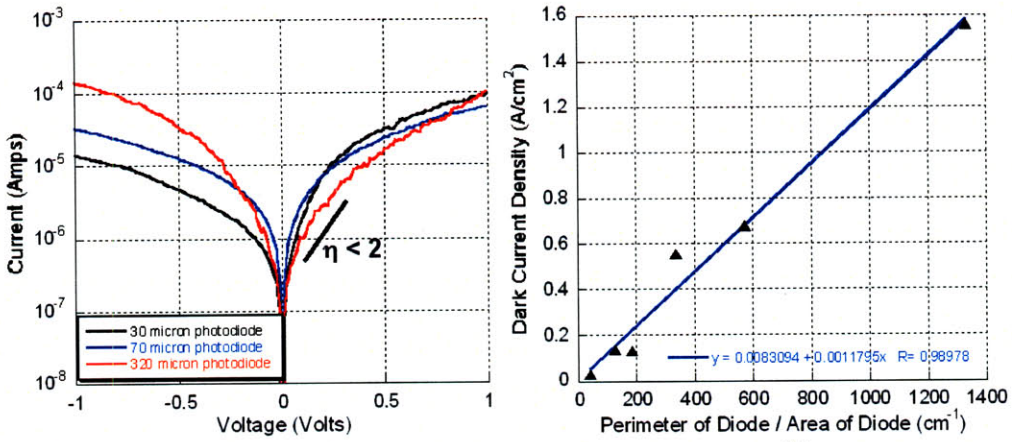


Figure 4.25 Initial fabrication process for selective Ge-on-Si *pin* photodiodes. The remainder of the selective photodiode process flow follow the blanket Ge-on-Si process flow described in Figure 4.1.

4.5.1 Selective Ge-on-Si *pin* photodiode fabrication process

As shown in Figure 4.25, starting with a P+ doped six-inch wafer, a 0.5 μm-thick SiO_2 film is deposited in the DCVD tool, and then densified in the ICL furnace tube at 1000°C for 90 minutes. Photoresist was then spun and hardbaked onto the wafer, and then backside oxide from the tube densification step was removed in a BOE solution. The first photoresist coat was removed, and a new photoresist layer was spun onto the film. The photoresist was then patterned, developed, and the field oxide and silicon substrate was dry etched to create 1.7 μm deep trenches. The photoresist was then ashed and the wafers went through a piranha clean.

After this step, the process was identical to the blanket *pin* photodiode process steps discussed earlier in Section 4.3.1, with the edge of the photodiode active region being 10 μm away from the selective Ge-on-Si sidewall for all the photodiodes.



(a) (b)

Figure 4.26 (a) I-V characteristics for various sized selective Ge-on-Si *pin* photodiodes. The reverse bias current scales exponentially with the applied bias. The reverse bias current scales as function of the photodiode perimeter. The photodiodes are barely rectifying in this due to the extremely high series resistance (~10^4 ohms).
(b) Perimeter area analysis of the selective Ge-on-Si *pin* photodiode, with J_P = 1.18 mA/cm and J_A = 8.31 mA/cm^2, with an associated combined current density of 13 mA/cm^2.

4.5.2 Electrical measurements

Eight selectively grown Ge-on-Si films were fabricated into photodiodes. The passivating films were either 0.3 μm-thick DCVD SiO_2 or SiON films. The wafers were not metallized, hence only electrical measurements were performed on these wafers. Generally, the reverse bias leakage current was found to be perimeter dominated with leakage density of 10 to 50 mA/cm^2, without significant difference between the photodiodes fabricated with DCVD SiO_2 and SiON passivating films. The photodiode measured in Figure 4.26 has a SiON passivating film. As shown in Figure 4.26, the reverse leakage current also has an exponential relationship with the magnitude of the reverse bias, implying a tunneling based source for the leakage current. In view of the results from the blanket and mesa isolated *pin* photodiodes, the tunneling behavior for the

selective *pin* photodiodes is not surprising since a 0.2 μm polysilicon cap layer was deposited to form an N+ contact layer. It is believed that activating this polysilicon layer led to the same type of Si/Ge interaction that is postulated to be the source of the tunneling based leakage current in blanket Ge-on-Si *pin* photodiodes. The high ideality factor for the selective Ge-on-Si *pin* photodiodes is ascribed to the high series resistance of ~10^4 ohms.

4.6 Chapter Summary

In this chapter the electrical, optical, and material characteristics of blanket, selective, and mesa-isolated *pin* photodiodes were discussed. It was found that most of the photodiodes had a perimeter dependent reverse bias leakage current that varied exponentially with applied bias. The reverse bias leakage current for a majority of the diodes was less than 50 μA for 50 μm x 50 μm photodiodes. Based upon all of the evidence gathered on the processed wafers, it is suspected that an unidentified process dependent variable is the source of the leakage current. This is consistent with the fact that the reverse bias leakage current for a majority of the photodiodes was perimeter dependent. Various photodiode processing changes were investigated with modest improvements in the dark current value. The photodiodes with the lowest dark currents for photodiodes with surface areas less than 4 x 10^{-4} cm^2 (200 x 200 μm^2) were a perimeter dependent wafer with a dark current density of 2.6 mA/cm^2 (~7 mA/cm^2 after further analysis in Appendix G) and an area dependent wafer with a dark current density of 8.5 mA/cm^2. The important difference between the PD and AD

photodiodes, however, is the fact that the observed perimeter coefficient for diodes on wafer 20-12 is three orders of magnitude lower than that extracted for the lowest leakage perimeter dependent photodiodes fabricated in this study, from wafer 11-8. Cross sectional TEM image comparisons of the lowest leakage area dependent and perimeter dependent blanket *pin* photodiodes were performed and Si/Ge interaction regions were identified as the possible source of the tunneling based reverse leakage current. Significantly, Si/Ge interaction regions were not noticed under the dielectric in wafer 20-12, but were found under the field dielectric in wafer 11-8.

Mesa isolated Ge-on-Si *pin* photodiodes without polysilicon contacts were fabricated and the leakage current took on a square root dependence on the magnitude of the reverse bias, a further indication that the Si/Ge interaction might contribute to the exponentially bias dependent dark current seen for many polysilicon contacted blanket and selective *pin* photodiodes. Responsivity measurements were performed on blanket and mesa isolated *pin* photodiodes, with measured values ranging from 0.4 to 0.55 A/W at a wavelength of 1.55 μm for photodiodes biased at –1 volt. For the perimeter dependent blanket *pin* photodiodes, a responsivity "dead zone" was identified near the photodiode perimeter.

Photoemission studies at high reverse bias were also performed on blanket and mesa isolated Ge-on-Si *pin* photodiodes. The photoemission zone for perimeter dependent blanket photodiodes was a continuous band that aligned with the responsivity "dead zone"; while for the area dependent blanket photodiodes

the photoemission zones appeared as discrete spots distributed evenly throughout the active area. Photoemission studies of mesa-isolated photodiodes showed the physical location of the dark current was primarily at the perimeter and corners of the photodiodes, where there exist higher electric fields and possibly higher surface state densities due to the etched sidewalls.

High speed measurements were performed on blanket Ge-on-Si *pin* photodiodes with perimeter dependent currents. The fastest photodiodes had a 3-dB frequency of 1.5 GHz at –5 volt bias. It is believed that a trap mediated process leads to a longer transit time delay in the perimeter dependent photodiode frequency response.

Shown in Table 4.1 is a summary table of the results for photodiodes fabricated in this work. The results for the fabricated photodiodes compare favorably for the reverse bias leakage current and the responsivity between the LPCVD and UHVCVD 2 step growths. The leakage current for both deposited material is essentially the same, while the absorption coefficient for LPCVD Ge-on-Si films appears to be slightly higher than UHVCVD Ge-on-Si films. On the other hand, the frequency response for the fabricated LPCVD photodiodes is ~6x lower than comparable UHVCVD devices. This difference in the frequency response is currently believed to be due to the photodiode fabrication process and not the deposited quality of the LPCVD Ge-on-Si films.

Source	Deposition Method	Deposition type	Intrinsic Layer thickness (μm)	Leakage Current at -1V (mA/cm^2)	Responsivity at 1.55 μm (A/W)	3-dB Frequency (GHz)
J.L. Liu, *et al*	Sb & Graded Buffer (4 μm)	Blanket Epi	0.9	**0.15**	<0.56	2.3
J.F. Liu, *et al*	2 step growth	Blanket Epi	2.35	12	**0.56**	8.5
Jutzi, *et al*	MBE growth at 300 °C	Blanket Epi	0.3	100	~0.03	**39**
J. F. Liu, *et al*	2 step growth	Selective Epi	1.7	12	0.4	2.5
This work	*2 step growth*	*Blanket Epi*	*~1.4*	*8.5*	*0.4*	*NA*
This work	*2 step growth*	*Blanket Epi*	*1.4*	*~7*[g]	*0.45*	*1.5*
This work	*2 step growth (mesa)*	*Blanket Epi*	*~1.5*	*~3**	*0.55*	*NA*
This work	*2 step growth*	*Selective Epi*	*~1.5*	*~13**	*NA*	*NA*

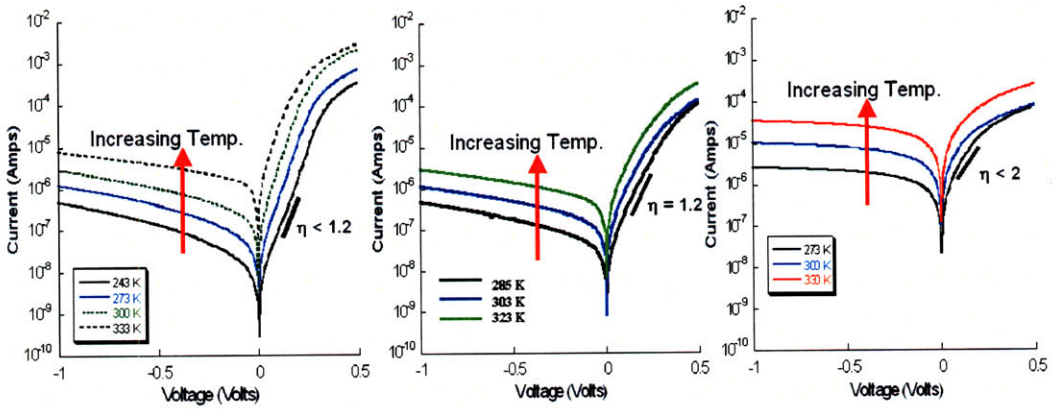
Table 4.1 Summary of various Ge-on-Si deposition methods and associated results from fabricated vertically illuminated *pin* photodiodes. The best results for each parameter are highlighted in bold. The asterisk for certain photodiodes is to note that the measured photodiodes have perimeter dependent leakage for active surface areas less than 1 mm^2. [g] refers to values extracted from Appendix G.

Chapter 5. Origins of the photodiode reverse bias leakage current

Introduction

In this chapter the sources of the reverse bias leakage current for the perimeter dependent (PD), area dependent (AD), and mesa isolated *pin* photodiodes presented in Chapter 4 are investigated. As discussed in Chapter 3, the reverse bias leakage current of photodiodes is important due to the detrimental effect high values of dark current has on the static power dissipation and the bit error rate (BER) of a photodetector. Thus, understanding the source of the dark current is an important objective for fabricating useful photodiodes.

The source of the reverse bias leakage current for the polysilicon-contacted (ion implanted) and metal contacted (in-situ doped) Ge-on-Si *pin* photodiodes were analyzed using temperature dependent current – voltage measurements. For the PD photodiodes, two-dimensional Medici simulations were also matched to the observed bias and temperature dependence of the reverse bias leakage current.



(a) (b) (c)

Figure 5.1 Temperature dependent IV curves for various photodiodes. (a) 100 x 100 μm^2 perimeter dependent (PD) and (b) area dependent AD photodiodes show an exponential relationship of the dark current with the applied bias and the temperature. (c) 120 x 120 μm^2 mesa isolated photodiode shows a square root dependence of the dark current on the applied bias and also an exponential relationship with the temperature. Series resistance of ~10^3 ohms is believed to cause high ideality factor in the measurements.

5.1 Temperature dependent reverse bias leakage current modeling

All the three types of Ge-on-Si *pin* photodiodes were measured on a temperature controlled stage with a range of –40°C to 200°C. The current-voltage characteristics at several temperatures for the perimeter dependent, area dependent, and mesa isolated photodiodes are shown in Figure 5.1. When plotted on a log-log scale both the PD and AD photodiodes exhibit an exponential dependence of the reverse leakage current on the applied bias and the temperature, while the mesa isolated photodiodes display a square root dependence on the magnitude of the applied bias and an exponential dependence on the temperature. This difference in voltage dependence (exponential versus

square root) may indicate a difference in the dominant leakage mechanisms, as discussed in Sections 5.1.1 to 5.1.4 below.

5.1.1 Tunneling and emission based reverse bias leakage current

Since the PD and AD photodiodes both have an exponential dependence on the applied bias, from the equations discussed earlier in Chapter 2, it is hypothesized that tunneling or emission mechanisms are the dominant sources of the reverse bias leakage current for these photodiodes. The source of the reverse bias leakage current could be the Poole-Frenkel effect, phonon assisted tunneling, or band-to-band tunneling as shown in Figure 5.2 (a). Utilizing the temperature dependent measurements, the specific tunneling and/or emission mechanism(s) associated with the observed dark current behavior was investigated.

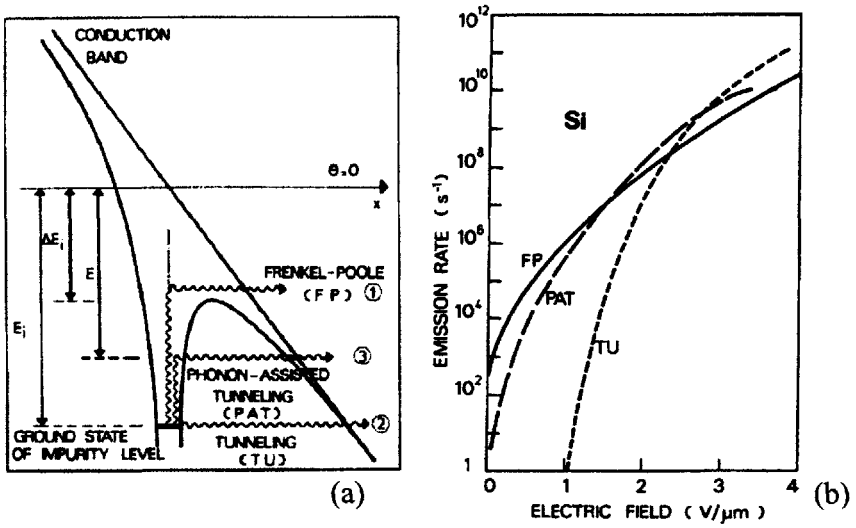


Figure 5.2 (a) Schematic showing the Poole-Frenkel effect in emission process 1, band-to-band tunneling in emission process 2, and the Phonon-Assisted Tunneling as emission process 3. (b) Emission rates as a function of the electric field for a Silicon bandgap. Poole-Frenkel (FP) and Phonon Assisted Tunneling (PAT) occur at much lower electric fields than band-to-band tunneling (TU). From Rosencher, *et al* [81].

At low electric fields, the reverse bias leakage current depends on the trap distribution, and hence the material quality and fabrication process [80]. At larger electric fields, the current becomes almost independent of the material quality and only depends on the bandgap due to the onset of band-to-band tunneling. As shown in Figure 5.2 (b), at low electric fields, the most dominant generation mechanisms are field enhanced thermionic emission by the Poole-Frenkel effect, and phonon assisted tunneling [85].

With regards to the Poole-Frenkel effect and phonon assisted tunneling (PAT), there are two kinds of trap states: Coulomb and Dirac centers [82]. For Coulomb centers, the electric field reduces the tunneling distance and also lowers the trap barrier height. In the case of Dirac centers, only the tunneling distance is affected, while the trap barrier height is unchanged [83]. For example, donor states act as Coulomb centers for the emission of an electron to the conduction band and can be thought of as Dirac centers for emission of a hole to the valence band. A reciprocal relationship holds for acceptor states emission to the valence band and conduction band respectively.

The theory for the Poole-Frenkel effect predicts an enhanced emission probability from Coulombic potential centers due to field-induced barrier lowering, as shown in Figure 5.2 (a), and can be modeled by [84]:

$$J_{PF} = CE_b \exp\left[-\frac{q\left(\phi_t - \sqrt{qE_b/\pi\varepsilon}\right)}{kT}\right] \propto \exp\left(\frac{-E_a}{kT}\right) \qquad \text{(Equation 5.1)}$$

$$E_a = q(\phi_t - \Delta\phi) \qquad \text{(Equation 5.2)}$$

$$\Delta\phi = \sqrt{qE_b/\pi\varepsilon} \qquad \text{(Equation 5.3)}$$

where E_b is the applied electric field, E_a is the activation energy of the Poole-Frenkel process, ε is the dielectric constant of the material, $\Delta\phi$ is the potential barrier lowering due to the electric field, and ϕ_t stands for the Coulombic barrier potential of the trap energy level. Examining Equations 5.2 and 5.3, if the activation energy of the leakage current is plotted as a function of $|V|^{1/2}$, where V is the applied reverse bias, and this plot appears linear, which is consistent with a Poole-Frenkel emission process.

At electric fields magnitudes that can stimulate the Poole-Frenkel effect, another effect that can occur is phonon assisted tunneling [85]. Phonon assisted tunneling occurs when multiphonon transitions from the ground state are followed by tunneling across a reduced barrier length. As the electric field increases, the barrier length decreases for a given carrier energy until tunneling may occur directly from the ground state.

The expression for the enhancement of the tunneling probability due to PAT is given by an integral over the trap depth of the product of a Boltzmann factor, that describes the multiphonon transistion probability to a particular energy level, and the tunneling probability from the trap to band state located at the same

energy level [82]. Thus, the enhancement of the generation/recombination rate due to PAT can be represented as [86-87]:

$$U_{SRH} = -\frac{pn - n_i^2}{\frac{\tau_p}{1+\Gamma_p}\left[n + n_i \exp\left(\frac{E_{trap}}{kT}\right)\right] + \frac{\tau_n}{1+\Gamma_n}\left[p + n_i \exp\left(\frac{-E_{trap}}{kT}\right)\right]} \quad \text{(Equation 5.4)}$$

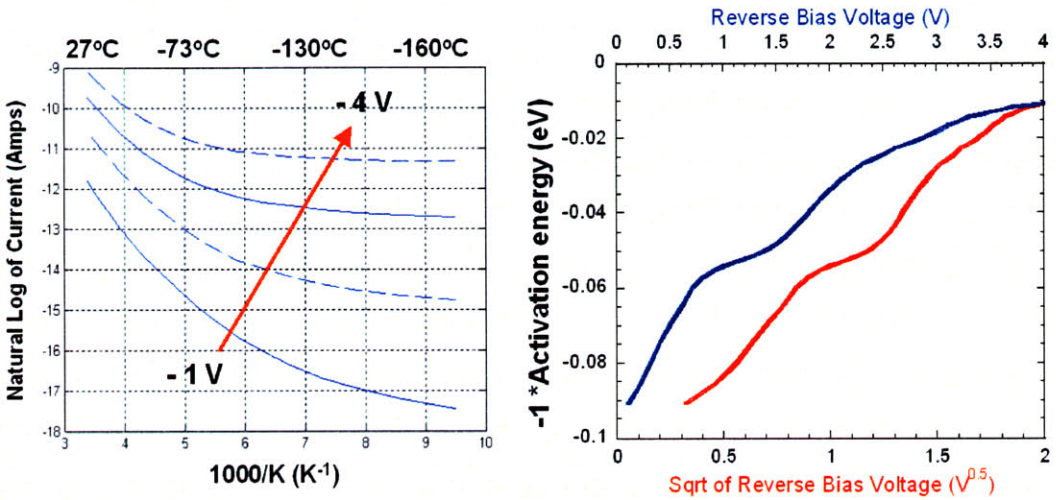
$$\Gamma_{n,p} = \frac{\phi_{tn,p}}{kT}\int_0^1 \exp\left[\frac{\phi_{tn,p}}{kT}u - \frac{4}{3}\frac{\sqrt{2m^*\phi_{tn.p}^3}}{q\hbar E_b}u^{3/2}\right]du \quad \text{(Equation 5.5)}$$

where U_{SRH} is the generalized Shockley-Read-Hall (SRH) generation rate, $\Gamma_{n,p}$ is the enhancement factor due to the electric field for electrons and holes, E_{trap} is the difference between the trap energy level and the Fermi energy level, and the remaining parameters have the standard meaning. Thus, PAT applies to both Dirac and Coulomb trap centers, while the Poole-Frenkel effect is limited to the Coulomb trap centers.

5.1.2 Source of Reverse Leakage Current for Perimeter Dependent Photodiodes

In order to investigate the apparent activation energy of the reverse bias leakage current, the log of the leakage current for PD photodiodes at several different voltages versus the inverse temperature (K^{-1}) is shown in Figure 5.3 (a). In this plot, the PD photodiode leakage current shows some non-linearity, indicating that the leakage mechanism does not appear to be described by a single-activation energy model. Figure 5.3 (b) is a plot of the PD photodiode leakage current apparent activation energy as a function of $|V|$ and $|V|^{1/2}$. Since the apparent activation energy does not appear linear as a function of $|V|^{1/2}$, it does

not appear that only a Poole-Frenkel effect is occurring. Thus, although the electric field affects the activation energy, implying that there are charged traps in the PD photodiodes, there probably is another factor, such as phonon assisted tunneling, which is contributing to the PD photodiode leakage current. The PD photodiode leakage current could therefore be due to a PAT process or combination of a Poole-Frenkel and PAT process.



(a) (b)

Figure 5.3 (a) Arrhenius plot of the temperature dependence for the PD photodiode reverse bias leakage current in Figure 5.1 (a). The curves are constant voltage curves at multiples of –1 volt. The nonlinear nature of the curve shows that the PD dark current does not have a single activation energy model. (b) Apparent activation energy as a function of $|V|$ (blue) and $|V|^{1/2}$ (red) for the PD photodiode extracted from Figure 5.1 (a). The fact that the activation energy changes as a function of bias shows that the electric field modulates the trap barrier. The nonlinear nature of the red curve means the PD photodiode emission process is not just Poole-Frenkel.

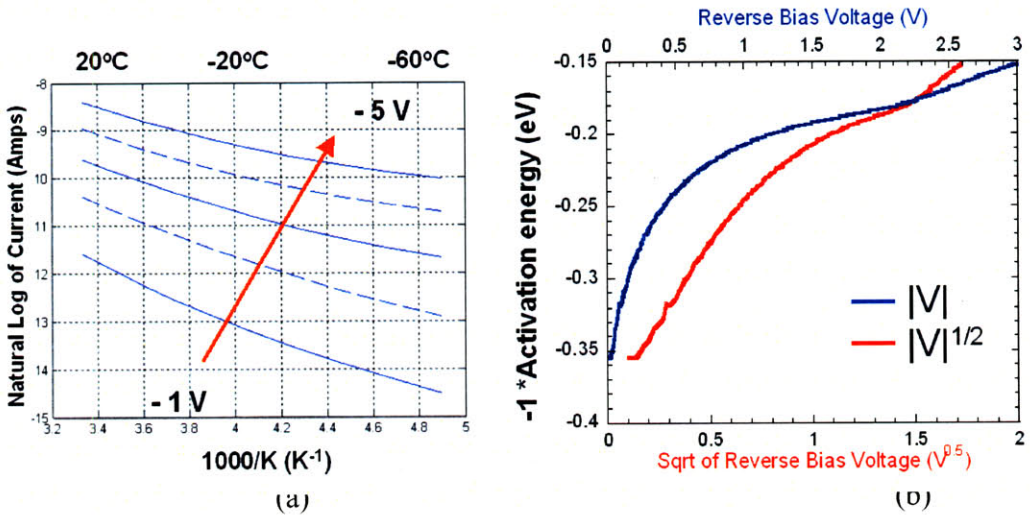


Figure 5.4 (a) Arrhenius plot of the temperature dependence of the reverse bias leakage current for a 300 μm x 300 μm PD photodiode from 100 K to 300 K. The voltage is swept between –10 volts and 1 volt. Transition in behavior of current appears to occur around 200 K. (b) Activation energy as a function of |V| (blue) and $|V|^{1/2}$ (red) for the PD photodiode for temperatures between 100 K to 200 K. The linearity of the red curve is consistent with a Poole-Frenkel emission process. Measurements are courtesy of Xiaochen Sun.

In order to confirm whether phonon assisted tunneling affected the reverse bias leakage current for the PD photodiodes, very low temperature current-voltage measurements were performed down to liquid helium temperatures (~20 K).. It is believed that if the temperature is sufficiently lowered, the PAT contribution to the leakage current should vanish, leaving only a Poole-Frenkel signature to the temperature dependence of the leakage current [88].

Using a Helium compressor and a vacuum chamber, a wire bonded sample of wafer 11-8 (PD photodiode) was cooled down from 300 K to 20 K. Shown in Figure 5.4 (a) is the associated current-voltage curve taken between –10 volts and 1 V at approximately 11 K increments. The data from the temperature dependent

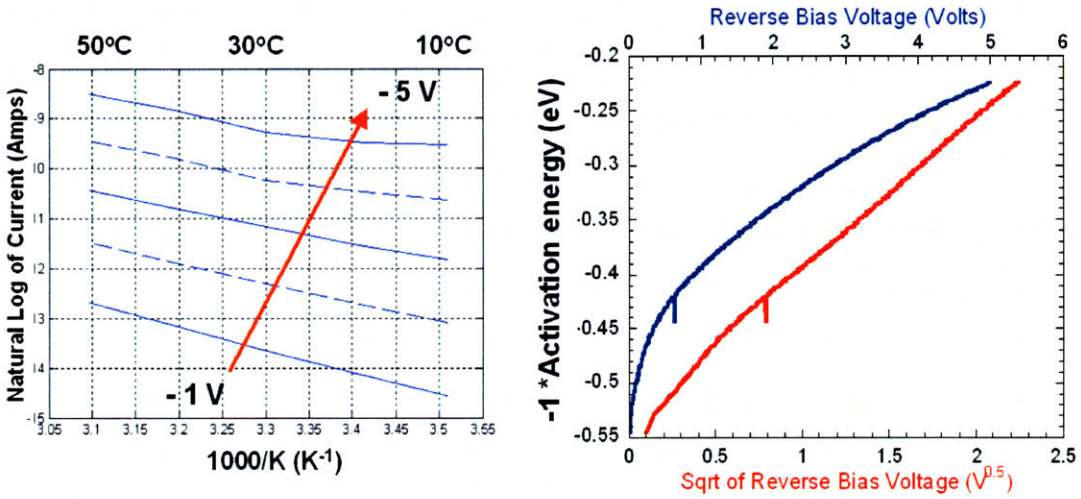
measurements were utilized to extract the activation energy as function of bias as shown in Figure 5.4 (b). It is found that for temperatures below 200 K, the plot of the activation energy versus $|V|^{1/2}$ had a fairly linear dependence, consistent with a Poole-Frenkel behavior. Thus it is hypothesized that both phonon assisted tunneling and the Poole-Frenkel effect contributes to the dark current above 200 K for the PD photodiodes, and the PAT contribution drops significantly for temperatures below 200 K. The physical source of the PD photodiode leakage current is believed to be due to the Si/Ge interaction regions located at the boundary of the device active area.

5.1.3 Source of Reverse Bias Leakage Current for Area Dependent Photodiodes

The log of the reverse bias leakage current for AD photodiodes at several different voltages versus the inverse temperature (K^{-1}) is shown in Figure 5.5 (a). In this plot, the AD photodiode leakage current does appear linear for voltages between –1 to –3 as functions of $|V|$ and $|V|^{1/2}$. Since the activation energy is linear as a function of $|V|^{1/2}$, it does appear that a Poole-Frenkel effect is occurring.

In order to assess whether the Si/Ge interaction regions that dominated the leakage current for the PD photodiodes affected the AD photodiodes, Equation 2.5 that models the bulk generation component (area dependence) of the reverse bias leakage current was re-examined. This equation can be rewritten to show the

explicit dependence of the minority carrier lifetime on the material quality as given by Equation 5.6 [33]:



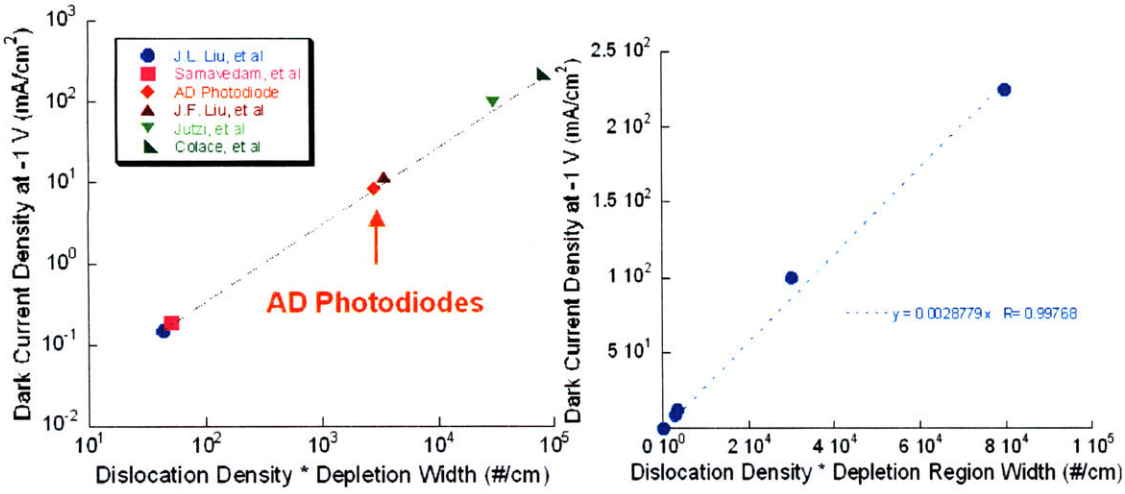
(a) (b)

Figure 5.5 (a) Arrhenius plot of the temperature dependence for the AD photodiode reverse bias leakage current in Figure 5.1 (b). The curves are constant voltage curves at multiples of –1 volt. Below –3 volts, the curves become nonlinear due to onset of band-to-band tunneling. (b) Activation energy as a function of |V| (blue) and $|V|^{1/2}$ (red) for the AD photodiode extracted from Figure 5.1 (b). The linear nature of the red curve means the AD photodiode emission process has a Poole-Frenkel signature.

$$J_g \approx -q\frac{n_i}{\tau_g}W = -qn_iWN_DN_{TD}\sigma V_{th} \qquad \text{(Equation 5.6)}$$

where N_D is the threading dislocation density, N_{TD} is the average number of traps for a given threading dislocation, σ is the trap capture cross section, V_{th} is the thermal velocity of the carriers, and the remaining parameters have the standard meaning. The only parameters in Equation 5.6 that can be simply adjusted once the photodiode material is selected are the depletion region width, W, and the dislocation density, N_D, with the majority of the remaining variables being intrinsic material parameters. Therefore, it was hypothesized that if the published

results in the literature of the dark current density for area dependent Ge-on-Si photodiodes were plotted as a function of the product of the depletion region width and dislocation density, the results should fit a straight line. As shown in Figure 5.6 (a), this is indeed the case for the published Ge-on-Si photodiodes with the relevant data available.



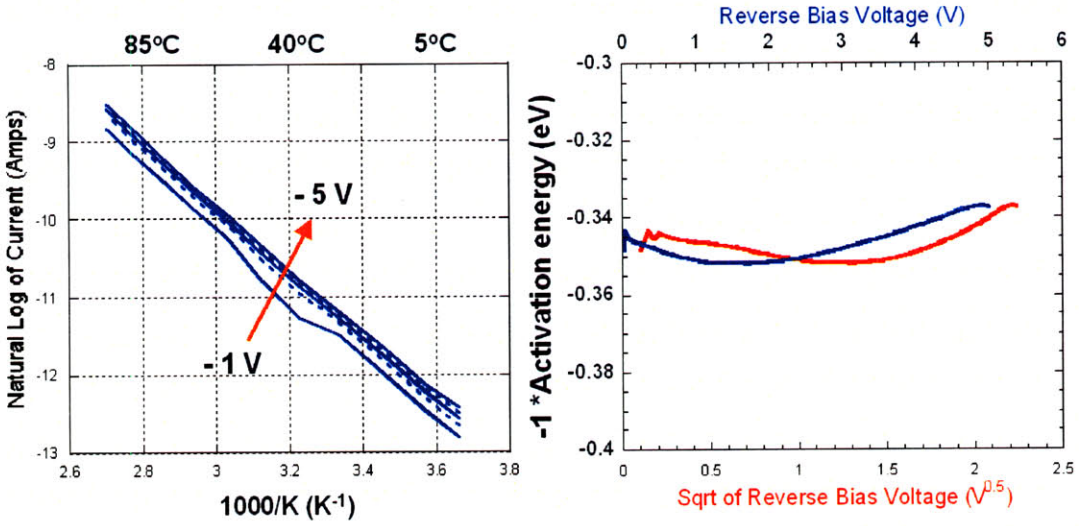
(a) (b)

Figure 5.6 (a) Published dark current density at –1 volt versus the product of the dislocation density and depletion width for area dependent Ge-on-Si photodiodes. AD photodiodes from this work have a good fit to the established line, showing that the dark current from these photodiodes is primarily generated in the bulk of the Ge-on-Si films from the threading dislocation density. It appears the Si/Ge interaction region does not significantly impact the dark current for these photodiodes. (b) Linear fit of dark current density at –1 volt to the product of the dislocation density and depletion width of published data shown in (a). Using the extracted slope of ~3 x 10^{-6} A/cm, the product of σ x N_{TD} in Equation 5.6 is determined to be 6.4 x 10^{-8} cm for these Ge-on-Si films.

Since the dark current density of the AD photodiodes as a function of the expected dislocation density and depletion width of these devices fits directly on the line established by the prior published data, it appears that the dark current density for the AD photodiodes is determined by the Ge-on-Si threading dislocation density. Finally, using the linear fit to the published data and the AD photodiodes shown in Figure 5.6 (b), as well as using germanium values for n_i of

2.3×10^{13} cm^{-3} and V_{th} of 1.2×10^{7} cm/s at 300 K, the value of the product of the average number of traps per dislocation and the capture cross section for Ge-on-Si traps is extracted to be 6.4×10^{-8} cm. If N_{TD} for Ge is assumed to be similar to that of Si at 10^{6} cm^{-1}, then the effective capture cross section of Ge-on-Si traps can be estimated to be 6.4×10^{-14} cm^{2} [89-90].

In summary, the source of the reverse bias leakage current for the AD photodiodes is consistent with bulk generation due to the threading dislocations in the Ge-on-Si film located in the intrinsic region of the *pin* photodiode. In addition, the generated dark current has a Poole-Frenkel characteristic.



(a) (b)

Figure 5.7 (a) Arrhenius plot of the temperature dependence for the mesa isolated photodiode reverse bias leakage current in Figure 5.1 (c). The curves are constant voltage curves at multiples of –1 volt. The mesa isolated photodiode dark current has an arrhenius relationship with the temperature. (b) Activation energy as a function of |V| (blue) and $|V|^{1/2}$ (red) for a mesa isolated photodiode extracted from Figure 5.1 (c). The activation energy is approximately -0.35 eV and is not dependent on the reverse bias voltage. From the activation energy, the most active traps appear to be located approximately in the middle of the germanium bandgap.

5.1.4 Source of Reverse Bias Leakage Current for Mesa Isolated Photodiodes

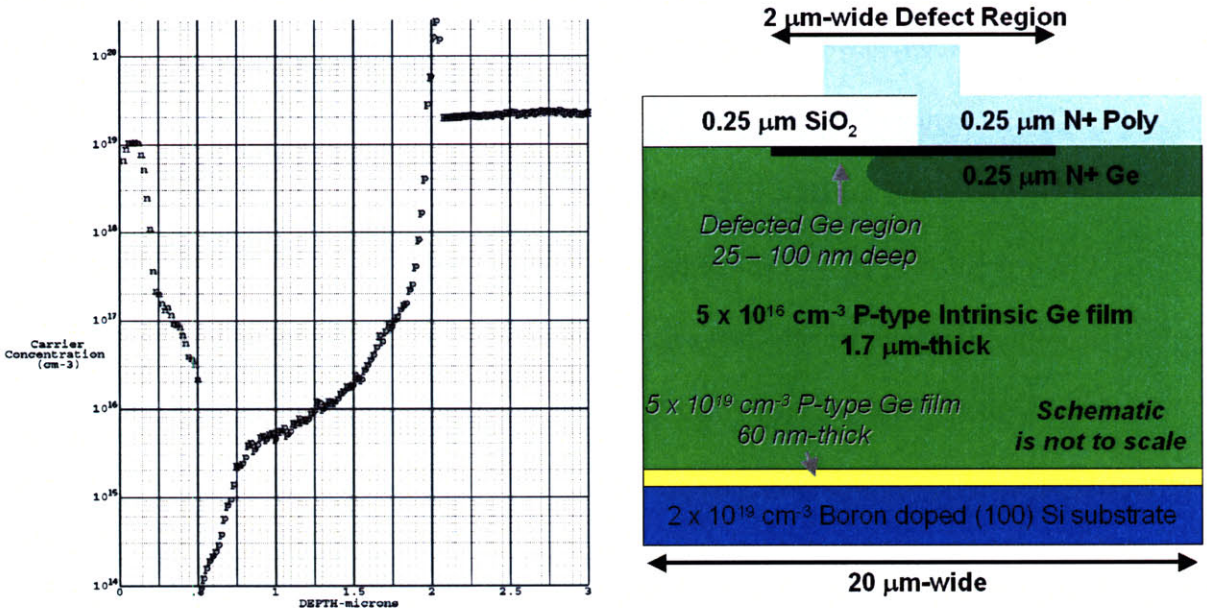
The apparent activation energy of the reverse leakage current was also measured for the mesa-isolated diodes, in the temperature range of 0 to 97°C. The results are shown in Figure 5.7, indicating a bias-independent, thermally activated generation process with an activation energy of roughly half the Ge bandgap. The data is consistent with a SRH generation process, with traps physically distributed in the depletion region of the diode, the width of which is modulated by the applied bias.

From Figures 5.1 and 5.7, and the theoretical background discussion in Chapter 2, it can be deduced that the leakage current for the mesa isolated *pin* photodiodes is associated with a surface or bulk generation source, with the most active defects located in the middle of the germanium bandgap. In order to distinguish between these two generation sources, a careful examination of Equations 2.5 and 2.6 shows that the surface generation component is dependent on the perimeter, while the bulk generation component is dependent solely on the area. As already mentioned in Section 4.4.2, the reverse bias leakage current for the mesa isolated *pin* photodiodes primarily scales with the perimeter for photodiodes less than ~1.8 x 1.8 mm^2 in size; thus the reverse bias leakage current for the fabricated photodiodes appears to be a surface generation mechanism. Therefore, it is expected that improved passivation of the germanium surface to lower the density of surface states will improve the reverse bias leakage current

for mesa isolated *pin* photodiodes. A summary table for the dark current analysis for all the photodiodes is shown in Table 5.1.

Wafer	Dark Current Dependence	Origin of Dark Current
11-8	Perimeter	Phonon Assisted Tunneling and Poole-Frenkel emission from Si/Ge interaction zones and threading dislocations
20-12	Area	Poole-Frenkel emission from Ge-on-Si threading dislocations
Mesa Isolated (1-2)	Perimeter	Surface generated from traps in the middle of the Ge bandgap

Table 5.1 Summary of reverse bias leakage current sources for various types of photodiodes.



(a) (b)

Figure 5.8 (a) Spreading Resistance Profile of a PD photodiode. This profile identifies the intrinsic region as being p-type with a doping between $10^{16} - 10^{17}$ cm^{-3}. (b) Two-dimensional Medici simulation structure created with information from SIMS, SRP, and TEM measurements.

5.2 Two-dimensional Medici simulations

In order to further examine the dependence of the reverse bias leakage current on various trap parameters such as trap density, lifetime, and location in the germanium film, two-dimensional Medici simulations were performed to model the voltage and temperature characteristics of perimeter dependent photodiodes. As shown in Figure 5.8 (b), only half of the diode structure was simulated due to the natural symmetry of the photodiode active area. This choice also conserved computer memory and considerably shortened the simulation time.

5.2.1 Perimeter dependent (PD) Medici simulations

For the PD photodiode, the doping levels and location of the Si/Ge interaction regions were extracted from Secondary Ion Mass Spectroscopy (SIMS) measurements shown in Figure 4.13 (a), Spreading Resistance Profile (SRP) measurements shown in Figure 5.8 (a), and Cross-sectional Transmission Electron Microscopy (XTEM) measurements shown in Figure 4.17 (a). The majority of the electrically active Si/Ge interaction nodes were concentrated around the interface of the germanium, silicon dioxide, and the polysilicon cap. From an examination of the cross sectional TEM images, a two micron wide highly defected germanium region was created to model the electrically active Si/Ge interaction regions. The trap distribution was assumed to be similar to that of a polycrystalline film, with an exponential trap density distribution in the bandgap as shown in Figure 5.9.

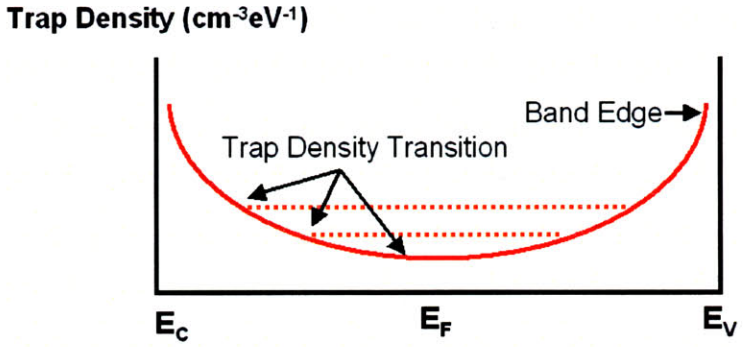


Figure 5.9 Trap distribution model used for Medici simulations. The three parameters used to describe the bandgap trap distribution are the band edge trap density, the midgap trap density, and the energy at which to transition to the midgap trap density.

The Medici models that were available for simulation were CONSRH or Concentration dependent Shockley-Read-Hall generation, AUGER, for auger generation, BTBT to represent band-to-band tunneling, and R.TUNNEL to represent the influence of both band-to-band tunneling and phonon-assisted tunneling. The parameters that were varied were the density and distribution of traps in the bandgap, the tunneling mass of the carriers in the germanium film, and the depth of the germanium defected region. The simulations were judged relative to the fit to the measured values as a function of the temperature dependence and the electrical dependence of the reverse bias leakage current. As shown in Figure 5.10 (a), only by utilizing the phonon-assisted tunneling model can the measured voltage dependence for the PD photodiode dark current be replicated in the simulations.

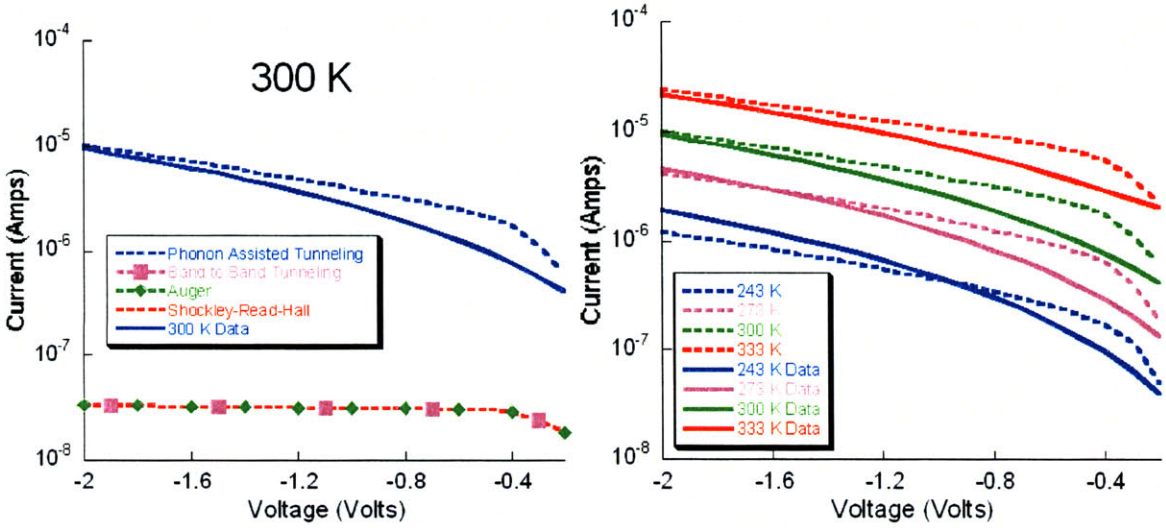


Figure 5.10 Two-dimensional Medici simulation fits to a 100 μm x 100 μm PD photodiode. (a) The effect of various Medici models are shown at 300 K. Only with the Phonon Assisted Tunneling model activated can the correct reverse bias leakage current dependence on the bias be achieved. (b) Temperature dependence for the Medici simulations also shows a good fit to the measured data between 243 – 333 K.

From the best simulation match to the measured voltage and temperature dependence of the PD photodiode dark current, the following parameters were extracted: At the band edge, the peak trap density was determined to be approximately $1x10^{19}cm^{-3}eV^{-1}$, and in the midgap region, the trap density was found to be approximately $3x10^{17}cm^{-3}eV^{-1}$, and a trap lifetime of 100 picoseconds was assumed. Initially, charged traps were included in the Medici simulation in order to simulate the Poole-Frenkel effect, since this mechanism is not explicitly included in the Medici simulation parameters. This unfortunately led to significantly less optimized results and thus all traps were made neutral. For the parameters mentioned above, the electrical and temperature dependence of the Medici simulation matches very well to the measured data in the temperature

range 243 K to 333 K as shown in Figure 5.10 (b). Unfortunately, Medici did not converge well below 240 K, so confirmation of the lowered contribution of the PAT below 200 K seen from the temperature dependent measurements could not be achieved within the Medici simulation environment.

Since many parameters could be varied in order to generate an acceptable fit to the dark current density as a function of temperature, a series of simulations were conducted to establish bounds within which the aggregate root mean square (RMS) error for the discrepancy between the simulated and measured values for the dark current density as a function of voltage and temperature would be less than 10%.

The major trap parameters considered in this study were the trap lifetime, the trap density and distribution through the bandgap, and the depth of the defected germanium region. In order to examine the effect of one parameter, for instance the trap lifetime, the trap lifetime was assigned a fixed value, and then the remaining parameters were varied in order to minimize the error between the simulated and measured data. Once a local minimum in the error has been determined, the assigned value of the trap lifetime was changed and a new minimum was found for the new trap lifetime value. This process was repeated until the minimum aggregate error for the simulation passes 10% or the assigned trap parameter values began to exceed reasonable physical bounds.

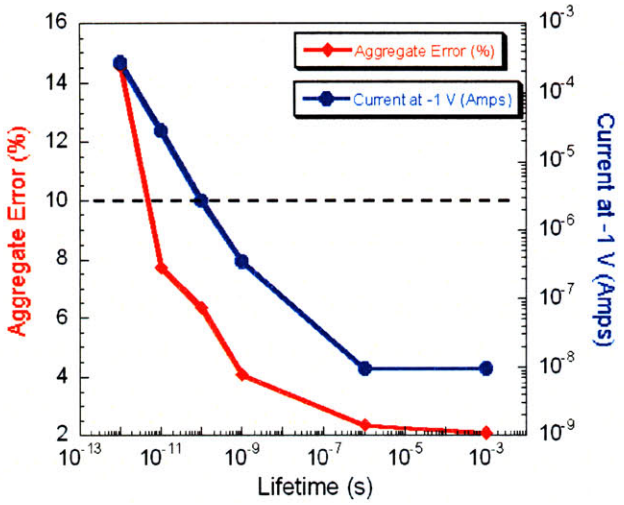


Figure 5.11 Two-dimensional Medici simulation aggregate error as a function of trap lifetime. The data is fitted for a 100 μm x 100 μm PD photodiode. The reverse bias leakage current increases linearly as the lifetime decreases until a trap lifetime of 1 microsecond is reached. The error is less than 10% at a trap lifetimes above 1 picosecond.

The first trap parameter studied in this fashion was the trap lifetime. The range of trap lifetimes examined was between one picosecond to one microsecond. As shown in Figure 5.11, it was found that the dark current density increased almost linearly as the trap lifetime decreased, as expected from purely Shockley-Read-Hall considerations of the carrier generation rate. As shown in Figure 5.11, as the trap lifetime dropped, the aggregate RMS error increased until it passed 10% at a trap lifetime around 1 picosecond. It appears that the error continues to decrease for longer trap lifetimes up to 1 microsecond, which constitutes a reasonable upper bound [91], especially in light of the 3.5×10^{-10} seconds period that is hypothesized to be the trap lifetime from the unit impulse measurements on the PD photodiode discussed in Section 4.3.2.

A second parameter examined was the effect of the peak trap density at the band edge, which correspondingly bounds the minimum trap density at the

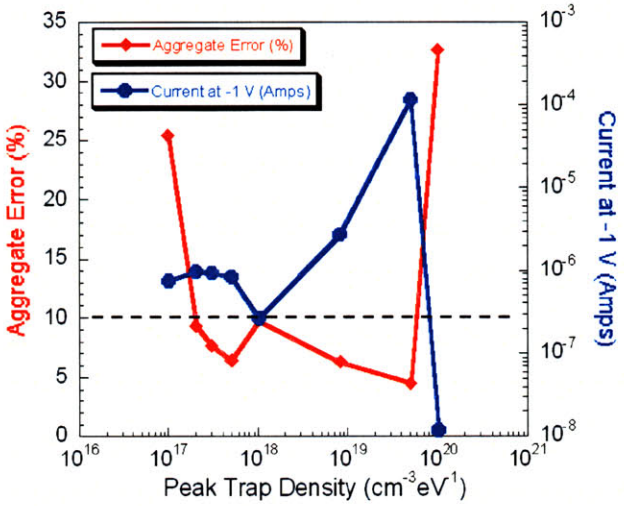


Figure 5.12 Two-dimensional Medici simulation aggregate error as a function of peak trap density. The data is fitted for a 100 μm x 100 μm PD photodiode. The reverse bias leakage current nominally increases as a function of the peak trap density at the band edge. Below 2 x 10^{17} $cm^{-3}eV^{-1}$ and above 5 x 10^{19} $cm^{-3}eV^{-1}$, the error increases past 10%.

Fermi level, and also impacts the trap distribution in the bandgap. The local minimum error of the peak trap density was mapped out for a range between 10^{17} $cm^{-3}eV^{-1}$ to 10^{20} $cm^{-3}eV^{-1}$. As shown in Figure 5.12, it was found that as the peak trap density in the bandgap increased, the magnitude of the reverse bias leakage current increased proportionally. Moreover, as shown in Figure 5.12, below 2 x 10^{17} $cm^{-3}eV^{-1}$ or above 7 x 10^{19} $cm^{-3}eV^{-1}$, the observed minimal error increased past 10%. At peak trap densities at or below 10^{17} $cm^{-3}eV^{-1}$, it was noted that no PAT effect was observed for reverse bias voltages above -1 volt, with the dark current density exhibiting a square root dependence with respect to the voltage. For peak trap densities above 7 x 10^{19} $cm^{-3}eV^{-1}$, the physical thickness of the defected region in the germanium begins to approach zero. If the depth of the physically defected region does not decrease, the dark current density would increase too rapidly with increases in the magnitude of the reverse bias.

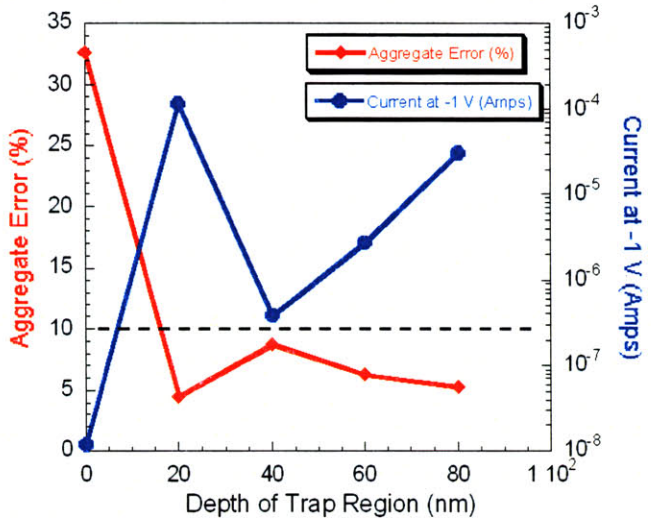


Figure 5.13 Two-dimensional Medici simulation aggregate error as a function of trap depth. The data is fitted for a 100 μm x 100 μm PD photodiode. The reverse bias leakage current nominally increases as the trap region depth into the germanium film increases. Below 20 nm trap depths, the aggregate error increases past 10%.

The depth of the germanium defected region was varied between 0 to 80 nm as in the prior simulations above. As shown in Figure 5.13, the observed minimal error increased past 10% for a germanium defected region thickness below 20 nm. Furthermore, as might be expected, as the germanium defected region thickness decreased, the peak trap density in the bandgap increased proportionally. It was found that as long as the highly defected Ge region overlapped a high electric field region, either due to the metallurgical junction or the applied bias, there was an appreciable generation current that led to a similar voltage dependence to the measured dark current behavior.

Although no definitive conclusions can be drawn from the two-dimensional Medici simulations, they provide an idea of nominal lower and upper bounds for some of the material parameters of interest. For the observed polysilicon and germanium interaction region that extends 50 to 150 nm into the germanium film, the peak trap density at the band edge of the germanium film

appears to be in the range of 10^{18} to 10^{19} $cm^{-3}eV^{-1}$, while the minimum trap density at the Fermi level appears to be between 10^{17} to 10^{18} $cm^{-3}eV^{-1}$. Finally, the trap lifetime of the PD photodiode appears to be greater than 10^{-12} seconds.

5.3 Chapter Summary

In this chapter the sources of the reverse bias leakage current for the perimeter dependent, area dependent and mesa isolated *pin* photodiodes were examined via temperature dependent current voltage measurements. The origin of the leakage current for the perimeter dependent photodiode could be associated with a combination of field enhanced thermionic emission (Poole-Frenkel effect) and phonon assisted tunneling (PAT). The area dependent photodiode leakage current is consistent with bulk generation from the Ge threading dislocation density. The AD photodiode leakage current also displays a Poole-Frenkel emission mechanism. The mesa isolated photodiode leakage current appears to be associated with surface generation mechanisms from traps located near the middle of the germanium bandgap.

Two-dimensional Medici simulations were performed for the perimeter dependent photodiodes. Due to limitations in the Medici simulation environment, PAT could be modeled accurately for the PD photodiode, but the Poole-Frenkel effect could not be modeled as readily. For the PD photodiode, applicable ranges for the trap lifetime, trap distribution in the bandgap, and extension of the trap region into the germanium surface were determined.

Chapter 6: Summary and Suggestions for Future Work

In this chapter, the major contributions of this thesis and suggested future studies are discussed.

6.1 Motivation

As digital systems become more ubiquitous, the high speed bit resolution limitations posed by purely electronic analog to digital converters (ADCs) has made combined electronic and photonic ADC architectures, which hold the promise for an order of magnitude increase in bit resolution, very attractive. In order to facilitate the integration of photonic systems onto an electronic chip, photodetectors targeted for the near infrared spectrum must be monolithically integrated onto the Si CMOS platform. Such near infrared photodetectors will require the integration of novel detecting materials, such as germanium films onto the silicon platform. Such near-infrared photodetectors can also be utilized for a plethora of applications such as optical interconnects, photonic integrated circuits, and near infrared cameras.

In this work, the major focus has been on investigating the possibility of utilizing a Low Pressure Chemical Vapor Deposition (LPCVD) Applied Materials Epi Centura™ system to deposit Ge-on-Si films that could then be fabricated into CMOS compatible *pin* photodiodes with low dark current, high speed, and high responsivity.

6.1.1 Epitaxial deposition of Ge-on-Si films: Blanket growth

In this thesis, the effect of growth conditions such as pressure, temperature, and seed thickness on the material quality of epitaxially grown LPCVD Ge-on-Si films have been examined. Ge-on-Si films were deposited in a two step process, first by growing a low temperature Ge layer (seed layer), followed by the deposition of a high temperature Ge layer (cap layer) with subsequent annealing to reduce the threading dislocation density to ~10^7 cm^{-2}. An optimum Ge seed layer growth temperature window of 335°C – 365°C has been identified. It has also been demonstrated that in this LPCVD process, a Ge seed layer thickness of 60 nm is required in order to maintain a smooth film morphology as the temperature is ramped for the high-temperature portions of the growth process. For seed layers at or below 30 nm-thicknesses, the Ge film islands during the temperature transition to the cap temperature, leading to increasingly rougher surface morphology during the remainder of the deposition process. A process window for smooth Ge cap layer growth has also been demonstrated. Smooth cap layers have been deposited from 600 to 700°C, and at 650°C, chamber pressures from 30 to 90 Torr are shown to lead to smooth film morphologies. 2 μm-thick blanket Ge-on-Si films annealed at 830 to 900°C for 30 minutes have been shown to have threading dislocation densities of ~2 x 10^7 cm^{-2} with an associated RMS surface roughness of 1.6 nm.

The effect of high levels of boron and phosphorus doping in the seed and cap layer growth respectively was also investigated. Boron doping above 10^{19} cm^{-3} has been found to enhance the growth rate of Ge seed layers and lower the oxygen

incorporation at the Ge/Si heterointerface. It is hypothesized that the enhancement in the growth rate is due to the lattice contraction from high boron doping. Phosphorus doping of the cap layer has also been demonstrated up to ~10^{19} cm^{-3}, without adversely affecting the germanium film growth rate and surface morphology.

Passivation of the germanium films was also studied and it was found that reactively grown GeON films, either from a nitridation in ammonia or an oxidation in an oxygen ambient followed by nitridation in an ammonia ambient leads to midgap D_{it} values in the range of 10^{11} to 10^{12} cm^{-2}. Post-deposition annealing tends to increase the density of interface states, however, indicating that careful attention must be paid to the thermal budget during Ge photodiode fabrication, in order to maintain passivation of the Ge surface by the dielectric overlayer. Deposited silicon dioxide layers as passivation films led to a D_{it} values greater than 10^{13} cm^{-2}.

6.1.2 Epitaxial deposition of Ge-on-Si films: Selective growth

The nominal Ge-on-Si deposition process developed for blanket Ge-on-Si epitaxy was utilized for the SEG deposition. Due to the reduction in the exposed silicon to 1% of the wafer surface area, there was an induced macroscopic loading effect that led to a ~5x increase in the germanium growth rate. Although the blanket Ge-on-Si growth process led to smooth germanium films, it was noted that there was noticeable germanium nucleation on the field oxide. The majority of the SEG epitaxial growth development was directed at lowering the nucleation

density of germanium on the field oxide, while retaining favorable germanium film characteristics.

The effect of HCl flow, growth pressure, and temperature on nucleation density for SEG LPCVD Ge-on-Si films was examined. HCl does not appear to strongly suppress germanium nucleation on the oxide surface without causing undue roughening or a low growth rate for the Ge-on-Si film. Using GeH_4 and H_2, an optimal cap deposition condition of 600°C, 10 Torr was identified for suppression of germanium nucleation on the field oxide of the wafer pattern. At higher temperatures or pressures, Ge nucleated readily on the oxide surface. In general, it has been found that suppressing the Ge nucleation density on oxide surfaces led to a corresponding reduction in the Ge-on-Si growth rate.

1.7 μm-thick selective Ge-on-Si films cyclically annealed between 450 – 830 °C for 30 minutes have been shown to have threading dislocation densities that depend on the trench width, decreasing from ~1 x 10^7 cm^{-2} for 300 μm square trenches to ~4 x 10^6 cm^{-2} for 30 μm square trenches. The annealed films generally had an RMS roughness of 1 nm.

6.1.3 Vertically illuminated Ge-on-Si *pin* photodiodes

After viably depositing Ge-on-Si films in a blanket and selective process in an LPCVD chamber, the next step was to fabricate vertically illuminated *pin* photodiodes to further evaluate the electrical, optical, and material characteristics of the Ge-on-Si films. Blanket, selective, and mesa-isolated *pin* photodiodes were fabricated and characterized. It was found that most of the blanket and all

the fabricated selective *pin* photodiodes had a perimeter dependent reverse bias leakage current with current densities generally less than 100 μA for photodiodes sizes of 50 x 50 μm^2. Most of the blanket and selective photodiodes also had a dark current with an exponential relationship to the applied reverse bias. Since the reverse bias leakage current was very difficult to reproduce from wafer-to-wafer and a majority of the photodiodes were perimeter dependent, it is believed that an unidentified process dependent variable is the responsible for the introduction of the defects causing the leakage current. Various photodiode processing changes were investigated with modest improvements in the dark current density. The photodiodes with the lowest dark currents for active areas less than 4 x 10^{-4} cm^2 (200 x 200 μm^2) come from a wafer with perimeter dependent photodiodes (wafer 11-8) with a dark current density of ~7 mA/cm^2, and a wafer with area dependent photodiodes (wafer 20-12) with a dark current density of 8.5 mA/cm^2. More importantly, the area dependent photodiodes on wafer 20-12 have perimeter coefficients for the reverse bias leakage current that are three orders of magnitude lower than those on the best photodiodes from wafer 11-8. In other words, wafer 20-12 has unusually low perimeter leakage currents. This led to photodiodes on wafer 20-12 with leakage currents as low at 10 nA at –1 volt for areas of 10 x 10 μm^2.

Samples were sent for cross sectional TEM images comparisons of the lowest leakage area dependent and perimeter dependent blanket *pin* photodiodes, and Si/Ge interaction regions were identified as the possible source of the reverse bias leakage current. TEM and SEM imaging indicates that the low leakage

photodiodes on wafer 20-12 did not display Si/Ge interaction regions underneath the field dielectric, while these regions were observed under the dielectric on wafer 11-8, which also showed a strong perimeter dependence to the leakage current. Mesa isolated *pin* photodiodes without polysilicon contacts were fabricated and the leakage current took on a square root dependence on the magnitude of the reverse bias. This bias dependence is quite different from the exponential dependence of the dark current on applied bias seen for many blanket and selective *pin* photodiodes.

Responsivity measurements were performed on blanket and mesa isolated *pin* photodiodes, with measured values ranging from 0.4 – 0.55 A/W at a wavelength of 1.55 μm for photodiodes biased at –1 volt. For the perimeter dependent blanket *pin* photodiodes, a responsivity "dead zone" was identified near the boundary of the active area of these photodiodes.

Photoemission studies at high reverse bias were also performed on blanket and mesa isolated Ge-on-Si *pin* photodiodes. The photoemission zone for perimeter dependent blanket photodiodes was a continuous band that aligned with the responsivity "dead zone" while for the area dependent blanket photodiodes the photoemission zones appeared as discrete spots distributed throughout the active area. Photoemission studies of mesa-isolated *pin* photodiodes showed the primary physical location of the dark current was at the perimeter and corners of the photodiodes, where there exists higher electric fields and possibly higher surface states due to the etched sidewalls.

High speed measurements were performed on blanket Ge-on-Si *pin* photodiodes with perimeter dependent currents. The fastest photodiodes had a 3-dB frequency of 1.5 GHz at bias of –5 volts for an illumination wavelength of 1.04 μm. It is believed that a trap mediated process leads to a longer transit time delay in the perimeter dependent photodiode frequency response.

Temperature dependent measurements of the perimeter dependent, area dependent and mesa isolated photodiodes were performed. The measurements and analysis are consistent with a combination of field assisted thermionic emission (Poole-Frenkel effect) and phonon assisted tunneling from the surface Si/Ge interaction region as the source of the reverse bias leakage current for the PD photodiodes. For the AD photodiodes, the reverse bias leakage current was consistent with bulk generation from the Ge-on-Si threading dislocations in the intrinsic region of the *pin* photodiode, and had a Poole-Frenkel signature. The mesa isolated photodiodes had a surface generation dominated leakage current, with the most active traps located in the middle of the germanium bandgap. It is expected that improved surface passivation techniques will lower the reverse bias leakage current for the mesa isolated photodiodes. Two-dimensional Medici simulations were carried out for the PD photodiodes. The characteristics of the measured data for the PD photodiode could only be matched with the phonon assisted tunneling model. Due to simulation limitations, the contribution of the Poole-Frenkel effect to the leakage current for the PD photodiode could not be accurately modeled. The general material ranges under which the simulated behavior matched the observed photodiode measurements were also evaluated.

6.2 Major contributions of this thesis

The contributions of this work are divided into two main sections, (1) Research on Epitaxial Deposition of Ge-on-Si films in an LPCVD chamber, and (2) Research on CMOS compatible Vertically Illuminated Ge-on-Si *PIN* Photodiodes

Research on Epitaxial Deposition of Ge-on-Si films in an LPCVD chamber

1. Developed an epitaxial blanket Ge-on-Si deposition process for a Low Pressure Chemical Vapor Deposition Applied Materials Epi Centura™ chamber.
    a. Identified process windows to deposit low temperature Ge-on-Si epitaxy of 335 to 365°C, and 30 to 60 Torr.
    b. Identified process windows to deposit high temperature Ge-on-Si epitaxy of 600 to 700°C, and 30 to 90 Torr.
2. Developed an epitaxial selective Ge-on-Si deposition process for a Low Pressure Chemical Vapor Deposition Applied Materials Epi Centura™ chamber.
    a. Identified the onset of Ge-on-Si nucleation in the epitaxial growth process.
    b. Identified the undesirable effects of including HCl to suppress Ge-on-Si nucleation on field oxide.

c. Identified chamber conditions of 600°C and 10 Torr to suppress Ge-on-Si nucleation on field oxide.

3. Investigated the effect of boron doping in low temperature Ge-on-Si epitaxy
   a. Identified increased growth rate of Ge-on-Si films possibly due to Ge lattice contraction at greater than 10^{19} cm^{-3} boron doping levels.
   b. Measured the reduction in contaminants such as oxygen at the Ge/Si interface due to the effect of high levels of boron doping.
4. Investigated the effect of phosphorus doping in high temperature Ge-on-Si epitaxy.
   a. Incorporated an order of magnitude greater phosphorus (~10^{19} cm^{-3}) in Ge-on-Si films than had been previously reported in the literature.
   b. Noted no adverse effects of high phosphorus doping in high temperature Ge-on-Si growth on the surface morphology and growth rate.

Research on CMOS compatible Vertically Illuminated Ge-on-Si *PIN* Photodiodes

1. Fabricated blanket Ge-on-Si *pin* photodiodes in collaboration with John Yasaitis of Analog Devices, Inc. These photodiodes demonstrated 0.25 – 1 μA reverse bias leakage current at –1 volt for photodiodes of dimension 50 x 50 μm, 1.5 GHz frequency response at –5 volts and a wavelength of 1.04 μm, and 0.4 – 0.45 A/W responsivity at 1.55 μm wavelength illumination.

a. Performed measurements and analysis that identified the origin of the reverse bias leakage current as field assisted thermionic emission and phonon assisted tunneling for PD photodiodes.
b. Performed measurements and analysis that identified the origin of the reverse bias leakage current as a bulk generation Poole-Frenkel emission mechanism consistent with Ge-on-Si threading dislocations in the intrinsic region of the *pin* photodiode.
c. Identified Si/Ge interaction regions as sources of lowered responsivity and also lowered effective carrier velocity.

2. Fabricated mesa isolated Ge-on-Si *pin* photodiodes without a polysilicon cap.
   a. These photodiodes had a square root dependence of the reverse bias leakage current on the applied bias
   b. Photodiodes had an external quantum efficiency of 47 to 51% at 1.55 μm, with high responsivity values of 0.51 to 0.55 A/W due to lowered reflectance loss relative to PD and AD photodiodes.

6.3 Suggestions for future work

The work presented in this thesis has just begun to scratch the surface of the possible applications of Ge-on-Si films, which range from being utilized as performance enhancers in MOSFETs to leveraging the integration of III-V materials onto the Si CMOS platform. In this section, suggestions for future work based on questions raised by the work performed in this thesis and the natural evolution of Ge-on-Si films are addressed. This section is partitioned into

suggestions for further research into (1) epitaxial development of Ge-on-Si films, and (2) CMOS compatible Ge-on-Si photodiodes.

Research in Epitaxial Deposition of Ge-on-Si films in an LPCVD chamber

1. Investigating Ge-on-Si cap deposition temperatures between 700 – 900°C and the effect on surface morphology and the dislocation density.
2. Investigating the effect of boron doping in the high temperature growth regime and the phosphorus doping in the low temperature growth regime.
3. Investigating further methods to suppress Ge nucleation on masking fields while retaining reasonable surface morphology and germanium growth rate.
    a. Exploring alternatives to SiO_2 as the selective masking field material
    b. Exploring various chamber deposition conditions
    c. Investigating effect of wafer backside oxide on deposition conditions
4. Investigating the activation and diffusion of dopants in germanium films
5. Further investigation of passivation materials and methods for germanium films.
    a. Exploring depositing GeON films in vacuum and the effect on the density of surface states
    b. Exploring atomic layer deposition of passivating films
6. Lifetime measurements should also be performed on the germanium material.

Research on CMOS compatible Ge-on-Si *PIN* Photodiodes

1. Further development into achieving reproducible, area dependent, low reverse bias leakage current photodiodes is needed.
    a. Photodiodes without polysilicon contacts, but an implanted N+ Ge active region should be fabricated at least in part to elucidate the effect of the sidewalls in the mesa isolated photodiodes on the photodiode characteristics.
2. The effect of threading dislocation regions on the leakage currents needs to be fully investigated and understood.
    a. The effect of the Si/Ge interaction regions in tandem with the threading dislocations should also be investigated.
    b. Implanting the perimeter regions of the photodiode to move the depletion regions away from the Si/Ge interaction regions should be investigated.
3. Further development of metrology methods such as Electron Beam Induced Current (EBIC), and Deep Level Transient Spectroscopy (DLTS) measurements should be pursued.
4. Further development of a selective *pin* photodiode fabrication process
    a. Investigating effect of the sidewall material and germanium deposition conditions on the reverse bias leakage current, responsivity, and frequency response.

5. Designing and fabricating a waveguide coupled Ge-on-Si *pin* photodiode structure to simultaneously achieve high frequency response (between 10 to 100 GHz) and high responsivity ($\geq$ 0.3 A/W).
6. Temperature dependent measurements of the responsivity and the frequency response should be conducted.
7. Further investigation of methods to improve the spur free dynamic range (linearity) of Ge-on-Si photodiodes should be performed.

Appendix A: Introduction to the Applied Materials Epi Centura™ System

A.1 Introduction

This appendix deals with the epi deposition process in general and provides details related to epi deposition using the Centura tool and epi film characterization.

A.2 The Epitaxial Deposition Process

Epitaxial deposition is a process in which a crystalline film is grown on a substrate. The following sections discuss epitaxial deposition fundamentals and the mechanisms for introducing dopants into epitaxial films.

A.2.1 Epitaxial Film Growth

Epitaxial film growth generally utilizes a Chemical Vapor Deposition (CVD) process. The epitaxial CVD process can be broken up into the following sequences:

1. Transportation of reactants to the wafer surface.

   (Some processes include reactions in the gas phase that generate film precursors before step 1.)

2. Adsorbtion of reactants on the wafer surface.
3. A chemical reaction at the surface producing the desired epitaxial film and undesirable reaction products.
4. Reaction products are desorbed from the surface.

5. Reaction products are transported from the wafer surface.

Rigorous mathematical modeling of these steps is nontrivial, and a simplified model (the Grove model) involving steps 1 and 3 is often used [92]. Despite the simplification of the Grove model, it captures many of the observed epitaxial CVD characteristics. A steady state deposition rate of

$$V = \frac{k_S h_g}{k_S + h_g} \frac{C_T}{N_1} Y \qquad \text{(Equation A.1)}$$

is predicted. V is the growth rate, k_S is the chemical surface reaction rate constant, h_g is the gas-phase mass transfer coefficient, C_T is the total number of molecules per unit volume in the gas, N_1 is the number of silicon atoms incorporated per unit volume in the film, and Y is the mole fraction of the reaction species in the gas. This model predicts a linear change in growth rate with changes in Y, which matches observations for typical industrial growth conditions where Y is quite small ($Y < 0.1$).

Another important feature of the Grove model is the implication of a surface reaction limited regime and a mass transfer limited regime. When surface reaction limiting criteria are in effect, or the gas-phase transfer coefficient is much greater than the surface reaction rate, the growth rate operates independently of h_g and is given by

$$V = k_S C_T Y \qquad \text{(Equation A.2)}$$

During the mass transfer limited regime where h_g, the gas-phase transfer coefficient is much less than k_s, the chemical reaction rate, the growth rate operates independently of k_s resulting in the following growth rate model:

$$V = h_g C_T Y \qquad \text{(Equation A.3)}$$

It is useful to understand what process conditions and factors contribute to the epitaxial growth rate. C_T should be a function of pressure and temperature, while Y is a function of the various reactant gas concentrations and the relative flow rates of each. The chemical surface reaction rate and gas-phase mass transfer constants, however, require further analysis. Assuming the reactions are of an Arrhenius type (meaning they are thermally activated), k_s is a function of a temperature independent frequency factor ($k0$), the activation energy of the reaction (Ea), Boltzmann's constant (k), and the process temperature (T):

$$k_S = k_o e^{-\left(\frac{E_a}{kT}\right)} \qquad \text{(Equation A.4)}$$

Assuming the process is not in a mass transfer limited regime, the chemical surface reaction rate should mainly be limited by the process temperature. At a constant temperature, the epitaxial growth rate can increase until the mass flow of reactants limits the process. The Grove model does generally predict the experimental results for typical process conditions. A number of models have been used for deriving gas-phase mass transfer coefficients. Boundary layer theory provides a reasonably accurate estimate of hg for reactant gases flowing over a surface [92]. A boundary layer is defined to be

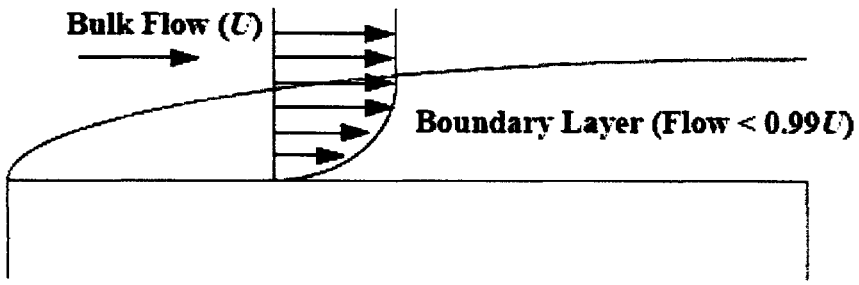


Figure A.1 Schematic of the thickness of boundary layer for laminar gas flow [92].

the region above a surface where the drag due to that surface lowers the gas flow rate below 99% of the bulk gas flow rate (U). The theory enforces a zero velocity constraint at the surface and a gradual rise in flow rate until the bulk flow is reached. This results in a boundary layer that expands along the surface in the flow direction.

$$h_g = \frac{3D_g}{2L}\sqrt{\mathrm{Re}_L} \qquad \text{(Equation A.5a)}$$

$$\mathrm{Re}_L = \frac{dUL}{\mu} \qquad \text{(Equation A.5b)}$$

where D_g is the diffusion coefficient for the active species, L is the length of the surface, and Re_L is the Reynolds number for the gas. The Reynolds number depends on the gas density (d), the bulk flow (U), the surface length (L), and the gas viscosity (μ). Assuming a fixed chemistry, h_g (and the deposition rate for a mass transfer limited process) is primarily driven by a square root dependence on U. Theory and experimental results display the growth rate's lack of dependence on temperature when in the mass flow limited regime.

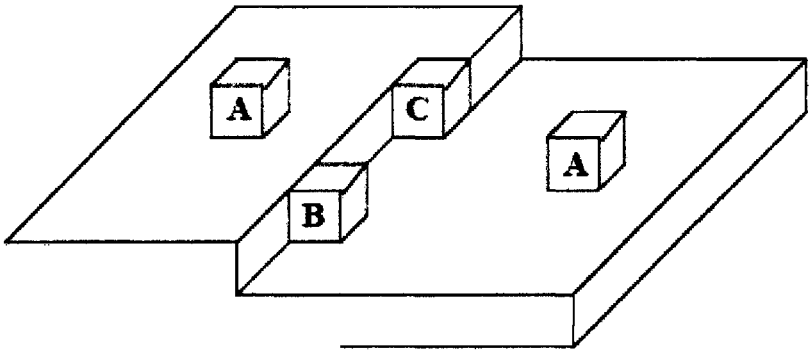


Figure A.2 Atomistic model of epitaxial growth. A adsorption is the least energeticly favorable location, with B being an improved adsorption site, and C being the best adsorption site due to the increased number of bonds available [92].

A.2.2 Atomistic Model of Epitaxial Growth

The atomistic model for epitaxial growth will be illustrated via silicon epitaxial growth on a silicon substrate. It is believed that silicon epitaxial film growth occurs via adatom migration. The adatoms attach to the silicon surface and migrate to kink positions at boundary steps between monolayers. A corner kink position provides the most energetically favorable position for stable attachment because half of the silicon lattice bonds are linked to the crystal. The epitaxial growth progresses via the lateral extension of the monocrystalline step layers.

A maximum monocrystalline growth rate can be determined for a given temperature with higher deposition rates resulting in polycrystaline films. It is believed that adatoms do not have sufficient time to migrate to kink positions when growth rates exceed a certain bound. Thus, higher temperatures provide more energy, increasing the velocity of migration, and therefore increasing the maximum growth rate as a function of the temperature.

A.3 Doping During Epitaxial Growth

Epitaxial growth provides the ability to precisely control film doping levels and thus the electrical characteristics of the deposited material. Silicon dopants are typically introduced with the reaction gases through the use of their hydrides [93]:

- Boron: Diborane (B_2H_6)
- Phosphorus: Phosphine (PH_3)
- Arsenic: Arsine (AsH_3)

The dopant delivery gases are usually heavily diluted with hydrogen to prevent dissociation of the dopant material [92]. There is currently no analytical model that accurately relates the ratio of the dopant concentration in the deposited film to the process conditions and generally empirical solutions of the doping levels must be found for each set of deposition parameters.

Fortunately the repeatability of the film doping concentration is very good for typical target doping concentrations and processing settings. A few scenarios are worth mentioning during the epitaxial doping process. Some epitaxial growth processes call for a lightly doped silicon layer to be added to a heavily doped wafer substrate. This situation results in dopant flux into the deposited film by two methods. First, there is direct solid state diffusion of dopant atoms from the substrate into the growing film that can lead to a wide transition layer between the bulk substrate and the steady state deposition doping levels. The thickness of the transition layer depends on the epitaxial deposition time and temperature, which higher temperatures and time leading to a wider transition layer thickness.

A second mechanism for substrate dopants to enter the growing epitaxial film is through vapor phase autodoping. Vapor phase autodoping occurs when a dopant atom from the wafer edge and/or backside evaporates into the gas stream, changing the dopant concentration in the process chamber, and subsequently in the growing film. Autodoping effects are typically noticeable as "tails" at the end of the diffused transition layer between substrate and final steady state doping levels. Solid state diffusion and autodoping can therefore impose restrictions on the minimum epitaxial thickness required to reach a given doping level.

A.4 Applied Materials Centura Epitaxial Deposition System

The Applied Materials Epi Centura system is a cluster tool to which single wafer processing chambers are attached. A single Centura system may have as many as three epi deposition chambers. The Epi Centura system can be configured for deposition at atmospheric pressure or reduced pressure, but switching between these configurations requires component changes in the processing chambers. The epi chamber is basically composed of upper and lower quartz domes. Process control parameters primarily include setpoints for chamber pressure, temperature, gas flows, and processing time.

The following sections first describe the various process settings that are available, then present a standard process recipe and some of the most important factors for process control.

A.4.1 Process Settings

Chamber pressure and gas flows into the chamber are regulated by Mass Flow Controllers (MFC's), that are set in the process recipe. Flows of the carrier gas to set the boundary layer conditions, and the reactant gases are controlled as part of the process recipe. The gas injection lines are divided into two flows prior to entering the chamber, one line supplies the outer edges of the chamber while the other supplies the chamber's center. Control of the radial edge and center gas flow ratio is enabled through valves whose set points are configured externally, through an Accusett system The ratio of the reactant gas flow to the radial center and edge flows help determine the uniformity of the growing epitaxial film.

The chamber temperature is controlled by radiant lamp modules on the top and bottom of the chamber. Each module is divided into inner and outer rings of lamps. Chamber temperature is monitored via two optical pyrometers, one focused near the bottom of the susceptor and one focused on the center of the wafer's surface. The bottom pyrometer is often used to control the temperature setpoint, since the top pyrometer readings are a function of the wafer surface emissivity, which depends on the growing epitaxial film composition and thickness. The chamber temperature is maintained by Proportional, Integral, Derivative (PID) controllers that use feedback from the optical pyrometers to vary the power delivered to the lamp modules. On the other hand, the lamp power can be set to a constant and the temperature allowed to consequently vary. The percentage of the heating power directed to the lower and upper modules, upper inner and upper outer rings, and lower inner and lower outer rings are also part of

the process recipe. These lamp power percentages are another important factor in tuning the wafer deposition rate uniformity control because the internal temperature feed-back loop can only maintain the temperature of at most the two locations where the pyrometers are focused.

A.4.2 The Standard Epi Deposition Recipe

A standard epitaxial depositon process on an Epi Centura tool nominally includes the following recipe steps [94]:

1. The lamps uniformly raise the chamber temperature to the appropriate bake temperature.
2. Native oxide on the wafer is reduced through a 30 second (or longer) bake in hydrogen gas. Reactamt gases are purged at this time to stabilize their flows before deposition.
3. The lamps uniformly lower (or sometimes raise) the chamber temperature to the appropriate process temperature.
4. Process gases are flowed to the chamber through the deposit manifold.
5. Epitaxial growth on the substrate surface and the front of the susceptor continue during the deposition step. Products from the chemical reaction are exhausted from the chamber. The chamber pressure, temperature, and reactant gas composition can change during the deposition process.
6. A short hydrogen gas purge clears the process gases from the chamber.
7. The wafer is cooled to a temperature to which it can be removed.

After removing the wafer an etch-back process is performed to clear material that was deposited on the chamber during the growth step. The frequency of the chamber clean varies, based on the deposition parameters. Generally the etch process should be performed once every one to three epi wafers.

In summary, the flexibility, low cost, and high throughput of the Epi Centura systems makes them a very useful tool for examining the kinetics and deposition possibilities of epitaxial manufacturing systems.

Appendix B: Germanium Etch Pit Density Procedure

Etch Solution Preparation:

(1) Clean glassware

(2) Etch Chemistry:

1. 35 mg of iodine
2. 65 ml of Acetic Acid
3. 20 ml of Nitric Acid
4. 10 ml of HF

(3) Measure out 35 mg iodine, grind with mortar and pestle

(4) Get medium sized plastic bottle

(5) Gown up: (Gown, Under Gloves, Over Gloves, Face Shield)

(6) Get all chemicals from Chemical Chase

(7) Add etch constituents to plastic bottle in the following sequence using a Teflon 100 ml graduated cylinder: Iodine, Acetic Acid, Nitric Acid, and HF

(8) Swirl etch solution for maximum iodine dissolution

(9) Let sit for between 1 – 24 hours until iodine is completely dissolved. The solution will be viable from a few weeks to a few months.

Pre-Etch Cleaning Procedures:

(1) Break sample into pieces

(2) Gown up: (Gown, Under Gloves, Over Gloves, Face Shield)

(3) Get chemicals: TCE, Acetone, and Methanol

(4) Get 3 100 ml beakers: Fill 1 with Trichlorethane, 1 with Acetone, 1 with Methanol.

   a. Note: Trichlorethane (TCE) and water might make a 2 phase mixture, so make sure the TCE beaker is completely dry before adding TCE.

(5) Put beakers into a sonicator and turn on

(6) Place samples into TCE beaker, let them sit for 10-20 minutes

(7) Place samples into Acetone beaker, let them sit for 10-20 minutes

(8) Place samples into Methanol beaker, let them sit for 10-20 minutes

Etch Procedures

(1) Take Methanol beaker with samples out of sonicator

(2) Fill 2 clean 1000 ml beakers with distilled water

(3) Remove sample from Methanol beaker with tweezers,

   a. Rinse in beaker #1 with distilled water
   b. Dip into etch solution for 10 seconds with continuous agitation
      i. If sample is underetched, no dislocation pits will be visible
      ii. If sample is overetched, there will be a variation in color (brown to blue)
   c. Rinse in beaker #2 with distilled water

(4) Iterate steps 3 b-c until dislocation pits are visible

a. Optionally, for SEG films, or patterned blanket Ge films, the etch depth can be checked with a surface profilometer to ensure that at least 0.5 microns of material has been etched.

(5) Dry samples with Nitrogen and inspect using an optical microscope.

(6) Count a small area (typically 10 x 10 microns): # of pits / area in cm^2 = Etch Pit Density

a. Take an average of 4 or more 10 x 10 micron areas for a reliable EPD value

b. Rule of thumb: Sparse pits density is ~10^7 cm^{-2} and high pit density is ~10^8 cm^{-2}

Accuracy of the defect count generated by this process is generally order of magnitude.

Appendix C: ICL Oxide Metal Contamination Study

C.1 Motivation and Background

Prior to allowing patterned SEG oxide wafers into the Applied Materials Epi Centura™ Deposition reactor, the contamination potential of the oxide sources was assessed. The focus of this experiment is to study the metal contamination potential of oxides and oxynitrides generated in ICL.

The first study assessed the contamination potential of the oxides generated by the DCVD, the 6C-LTO, the anneal tube 5B, and the thermal oxide tube 5D. This was a combined TXRF and SIMS study, with all materials analysis performed at Evans Analytical Group (EAG) at the location in Sunnyvale, CA. The TXRF analysis was used to measure the amount of metal contaminants from the DCVD Chamber C handling process. TXRF was performed on the polished side of the wafer which was face down in the system. TXRF was not performed on the deposited oxide. This includes contaminants from the robot handler and the susceptor. There was no control for the TXRF analysis. The SIMS analysis was used to quantify the common metallic contaminants in the DCVD, DCVD + anneal tube 5B, 6C-LTO + anneal tube 5B, and the thermal oxide tube 5D The control for the SIMS analysis was the thermal oxide grown in tube 5D.

The second study assessed the contamination potential of oxides and oxynitrides generated by the Concept1 reactor and the thermal oxide tube 5D. This was a combined TXRF and SIMS study. The TXRF analysis was used to measure the amount of metal contaminants from the Concept1 handling process, and the metal contaminants on the surface of the Concept1 oxide, and the thermal

oxide from tube 5D. A pre-epi cleaned* wafer served as a control for the TXRF analysis. The SIMS analysis was used to quantify the common metallic contaminants in Concept1 oxide and oxynitride, and the thermal oxide from tube 5D. The control for the SIMS analysis was the thermal oxide grown in tube 5D.

C.2 Oxide Study

***Nomenclature:**
Pre-epi clean: SC1 and Dump Rinse 1, HF dip for 15 seconds and Dump Rinse 1, SC2 and Dump Rinse 2, HF dip for 15 seconds and Dump Rinse 1. This is followed by a wet + dry SRD cycle. Unless specified otherwise, all wafers saw a pre-epi clean before deposition. [Note: normally the pre-epi clean is followed by a dry SRD cycle]
Standard clean: Standard rca clean with wet + dry SRD cycle
Wafer: 6" P+ Si (100) wafer

Study 1:
(1) Thermal oxide: 0.5 micron of oxide grown in tube 5D (ICL), pre-epi rca clean before cleaving
(2) LTO oxide (an): 1 micron of oxide grown in 6C-LTO and then annealed at 950C for 1 hour in tube 5B (ICL), pre-epi rca clean before cleaving
(3) DCVD oxide (an): 1 micron of oxide grown in Ch. C of DCVD, annealed at 950C for 1 hour in tube 5B (ICL), pre-epi rca clean before cleaving
(4) DCVD oxide: 1 micron of oxide grown in Ch. C of DCVD. No clean before cleaving.
(5) DCVD Handler wafer: Wafer with polished side down during 1um Ch. C oxide deposition. 6 – 16 Angstroms of oxide was deposited on the downward facing polished side during the 1um of oxide non-polished side deposition.

Wafers 1 - 4 received SIMS Cameca analysis for Na, Mg, Al, K, Cr, Fe, Ni, Zn
Wafer 5 received a tungsten source TXRF analysis for all transition metals.

Study 1-intermediate:
(1) DCVD oxide_3: This wafer received the standard rca clean. 1 micron of oxide grown in Ch. C of DCVD, annealed at 950C for 1 hour in tube 5B (ICL). This wafer was used to quantify the amount of Na, K from the prior Study 1-3 wafer, these are the results in Table 1.
(2) DCVD oxide_4: This wafer received the standard rca clean. 1 micron of oxide grown in Ch. C of DCVD. Cleaned with standard rca clean then annealed at 950C for 1 hour in tube 5B (ICL).

Wafers 1 - 2 received SIMS Quad analysis for Na, K

Study 2:

(1) Concept1 Handler wafer: Wafer with polished side down during 1um oxide deposition (Slot 1)
(2) TXRF control: Pre-epi cleaned wafer (Slot 4)
(3) Concept1 Oxide: Wafer with 1 um of Concept1 Silicon dioxide (Slot 7)
(4) Study 2 Thermal Ox: Wafer with 0.7 um of tube 5D Thermal oxide (Slot 10)
(5) Concept1 Oxynitride: Wafer with 1 um of Concept1 Silicon oxynitride (Slot 13)
(6) DCVD oxide_5: Wafer with 1um of DCVD Ch C. Silicon dioxide (Slot 16)
(7) DCVD oxide_6: This wafer received a standard rca clean. Wafer with 1um of DCVD Ch C. Silicon dioxide. (Slot 19)

Wafers 1 - 4 received tungsten source TXRF analysis for all transition metals
Wafers 3 - 5 received SIMS Cameca analysis for Na, Mg, Al, K, Cr, Fe
Wafers 3 - 7 received SIMS Quad analysis for Na, K

Measurement:

SIMS

The SIMS absolute error bar for these measurements is 2x, according to the engineers at Evans Analytical Group. Sample to sample, it is expected that there will be minimal variation. For Cameca analysis, archival SIMS oxide relative sensitivity factor (RSF) values were used for determine the concentration of the metals in this analysis. It is well known that Cameca analysis in oxides leads to charging and movement of the mobile Na ions to the oxide/silicon interface (snowplowing). This means that all the sodium Cameca data is inconclusive. For Quad analysis, oxide control samples were used to determine RSF values.

SIMS background levels for each element (cm^{-3}):
Cameca: Na: 5e13; Mg: 3e13; Al: 2e13; K: 5e13; Cr: 1-2e13; Fe: 3e14; Zn: 5e14; Ni: 2e15
Quad: Na: 7e13; K: 1e14

TXRF

A tungsten source was used for analyzing the contamination of wafers with transition elements. Sodium and Aluminum could not be measured by this method.

C.2.1 SIMS Data Summary

Study 1 summary:

All wafers cleaved with clean tools in a HEPA filtered section of 39-530b by Gary Riggott

Metal	Thermal Oxide [cm^{-3}]	LTO oxide (an) [cm^{-3}]	DCVD oxide (an) [cm^{-3}]	DCVD oxide [cm^{-3}]
Na	-	-	< 7E+13*	-
Mg	< 2E+13	6 ± 4 E+13	< 2E+13	< 2E+13
Al	< 3E+13	< 3E+13	< 3E+13	< 3E+13
K	< 2E+13	2 ± 1 E+14	< 2E+13	< 2E+13
Cr	< 2E+13	< 2E+13	< 2E+13	< 2E+13
Fe	< 3E+14	< 3E+14	< 3E+14	< 3E+14
Ni	< 5E+14	< 5E+14	< 5E+14	< 5E+14
Zn	< 2E+15	< 2E+15	< 2E+15	< 2E+15

Table C.1 Metal contamination from 0.3 μm – 0.7 μm into the films, except for Thermal oxide (0.2 – 0.4 μm). "<" means the measurement was detection limited whereas "±" refers to the average value of the SIMS measurement plus/minus the range of the data. "-" means the data is inconclusive.
* Data from Study 1-intermediate

Study 2 summary:

Whole wafers were sent for this analysis to avoid cleaving contamination

Metal	Study 2 Thermal Ox [cm^{-3}]	Concept1 Oxide [cm^{-3}]	Concept1 Oxynitride [cm^{-3}]	DCVD Oxide_5 [cm^{-3}]	DCVD Oxide_6 [cm^{-3}]
Na	< 7E+13	< 1E+13	3 ± 2 E+14	< 2E+14	< 2E+14
Mg	1.4 ± 1 E+14	< 2E+13	< 5E+13	*NA*	*NA*
Al	< 3E+13	< 3E+13	< 7E+13	*NA*	*NA*
K	*	< 2E+14	< 4E+13	< 7E+13	< 7E+13
Cr	< 3E+13	< 3E+13	< 8E+13	*NA*	*NA*
Fe	< 4E+14	< 4E+14	< 8E+14	*NA*	*NA*

Table C.2 Metal contamination from 0.3 μm – 0.7 μm into the films, except for Thermal oxide (0.2 – 0.6μm). "<" means the measurement was detection limited whereas "±" refers to the average value of the SIMS measurement plus/minus the range of the data. *NA* means the data was not available. Higher detection limit values for oxynitride film are due to the lower SIMS Cameca energies needed to profile this film.
* There was possible interference with Boron due to the heavily doped P+ substrate

C.2.2 TXRF Data Summary

Oxide surface contaminant study:

Whole wafers were sent to EAG for this analysis

Element	Units	Pre-epi cleaned wafer (no handling)	Study 2 Thermal Ox	Concept1 Oxide
S	10^{10} atoms/cm^2	63	310	550
Cl	10^{10} atoms/cm^2	240	60	430
K	10^{10} atoms/cm^2	*ND*	*ND*	*ND*
Ca	10^{10} atoms/cm^2	*ND*	*ND*	*ND*
Ti	10^{10} atoms/cm^2	*ND*	2.6	*ND*
V	10^{10} atoms/cm^2	*ND*	*ND*	*ND*
Cr	10^{10} atoms/cm^2	*ND*	*DL*	*ND*
Mn	10^{10} atoms/cm^2	*ND*	*ND*	*ND*
Fe	10^{10} atoms/cm^2	0.8	1.2	1.7
Co	10^{10} atoms/cm^2	0.6	*ND*	*ND*
Ni	10^{10} atoms/cm^2	0.6	*ND*	0.4
Cu	10^{10} atoms/cm^2	*ND*	0.5	1.5
Zn	10^{10} atoms/cm^2	0.8	1.1	1.3

Table C.3 TXRF maximum tables without ± deviations. *ND* stands for none detected. *DL* stands for possibly present near TXRF detection limit.

Handling Study:

Whole wafers were sent for this analysis

Element	Units	Pre-epi cleaned wafer (no handling)	DCVD	Concept1
S	10^{10} atoms/cm^2	63	74	225
Cl	10^{10} atoms/cm^2	240	58	320
K	10^{10} atoms/cm^2	*ND*	*ND*	*ND*
Ca	10^{10} atoms/cm^2	*ND*	*ND*	31
Ti	10^{10} atoms/cm^2	*ND*	*ND*	4.2
V	10^{10} atoms/cm^2	*ND*	*No data**	1.9
Cr	10^{10} atoms/cm^2	*ND*	*ND*	62
Mn	10^{10} atoms/cm^2	*ND*	*ND*	8.8
Fe	10^{10} atoms/cm^2	0.8	0.4	107
Co	10^{10} atoms/cm^2	0.6	0.3	1.7
Ni	10^{10} atoms/cm^2	0.6	0.5	19
Cu	10^{10} atoms/cm^2	*ND*	*ND*	14
Zn	10^{10} atoms/cm^2	0.8	*DL*	16

Table C.4 TXRF maximum tables without ± deviations. *ND* stands for none detected. *DL* stands for possibly present near TXRF detection limit.
* Vanadium was included in the Study 2 TXRF report, but was missing in the Study 1 TXRF report.

C.3 DISCUSSION

SIMS Oxide films conclusions:

- From Table 1, the 6C-LTO tube appears to be contaminated with Magnesium
    - Possibly contaminated with Potassium and Sodium also, although this could be due to cleaving contamination.
- From Table 2, it is possible that tube 5D is contaminated with Magnesium although the integrated dose is below the lab limits of $3x10^{10}cm^{-2}$.
    - From the integrated dose data, it appears that tube 5D might be contaminated with Aluminum
- From Table 2, the Concept1 oxynitride film appears to be contaminated with Sodium

TXRF Oxide surface and Handling experiment conclusions:

- From Table 3, it is appears that the oxides from the Concept1 and Thermal Oxide tube 5D are comparable, with Iron and possibly Chromium appearing only on the Thermal oxide surface and Nickel appearing only on the Concept1 oxide surface. Both oxides are comparable in surface contaminants to the pre-epi cleaned wafer.
- From the Table 4 data, there are small amounts of Iron, Cobalt, and Nickel detected from the wafer handler and/or the Ch. C susceptor in the DCVD tool. The DCVD handling compares favorably to the pre-epi cleaned wafer, the amount of Iron, Cobalt, and Nickel detected after the DCVD handling process is equal or lower to that of a freshly cleaned wafer surface.
- Looking at Table 4, the Concept1 Handling adds somewhere between 3 - 300x higher contamination than the DCVD handling in all the TXRF elements analyzed except for Potassium, which is difficult to measure with TXRF analysis.

C.4 CONCLUSION

Wafer	Study	Lab Processes	Analysis	Analysis Location	Element	Detected Level (10^{10} at/cm^2)	ICL Acceptable Limit (10^{10} at/cm^2)
LTO Oxide	1	Pre-epi clean (rca, ICL) -> 1 μm oxide deposition (**Tube 6C-LTO**, ICL) -> 950°C, 1 hour anneal (Tube 5B-Anneal, ICL)	SIMS	1 μm of oxide	Mg	9.7	3
					Na *	470	3
					K *	7.5	3
Concept1 Handler Wafer	2	Pre-epi clean (rca, ICL) -> 1 μm oxide *on backside* (**Concept1**, ICL)	TXRF	Polished front side that saw Concept1 handling	Ti	4.2	3
					Cr	62	3
					Fe	107	3
					Ni	19	3
					Zn	16	3
					Cu	14	3
Concept1 Oxynitride	2	Pre-epi clean (rca, ICL) -> 1 μm oxynitride deposition (**Concept1**, ICL)	SIMS	1 μm of oxynitride	Na	6.1	3
Thermal Oxide	1/2	Pre-epi clean (rca, ICL) -> 0.5/0.7 μm thermal oxide deposition (**Tube 5D-Thick Ox**, ICL)	SIMS	0.5/0.7 μm of thermal oxide	Al	7/19	3

Table C.5 The major contamination points found in the ICL Oxide study are above. The presumed source of contamination is highlighted in bold in the Lab Processes column. All wafers were P+ <100> Si substrate wafers.

* There was no followup SIMS study for the 6C-LTO tube after Study 1 (unlike for the Thermal Oxide and DCVD Oxide) so although the sodium and potassium values are suspected to be due to cleaving contamination, they are included for completeness.

Oxides deposited in the DCVD and the 6C-LTO tools were found to have low enough contamination potential for further processing in the Applied Materials Epi Centura reactor. The Concept1 tool has too high a metal contamination level to allow wafers into the Epi Centura tool.

Appendix D: Germanium RCA Clean Procedure

Ge RCA clean:

Note that the 50:1 HF:H_2O is dilute enough to etch SiO_2 very slowly (~5nm/min).

All steps are performed at room temperature

1. NH_4OH:H_2O 1:4 (tank 1) for 5 minutes to etch native oxide
2. Rinse (rinser 1)
3. H_2O_2:H_20 1:6 for 15 seconds to grow about 20A of GeO_2 (tank 1)
4. Rinse (rinser 1)
5. 50:1 HF for 30 seconds
6. Rinse (rinser 1)
7. HCl:H_2O 1:4 for 30 seconds (tank 2)
8. Rinse (rinser 2)
9. Dry in Spin Rinse Dryer (SRD)

Appendix E: TSCAP measurements on PD photodiodes

Thermally Stimulated Capacitance (TSCAP) measurements were performed in a helium cooled vacuum chamber on wirebonded perimeter dependent (PD) photodiodes by Xiaochen Sun in Professor Kimerling's laboratory. The photodiode was cooled under zero bias (filled traps) and reverse bias (unfilled traps). The small signal capacitance of the reverse biased PD photodiode was then measured as the photodiode warmed up. The difference in the small signal capacitance of these two conditions and the doping profile of the photodiode was then utilized to calculate density and bandgap location of the traps in the material as shown in Equation E.1 (a) and E.1 (b) [95]:

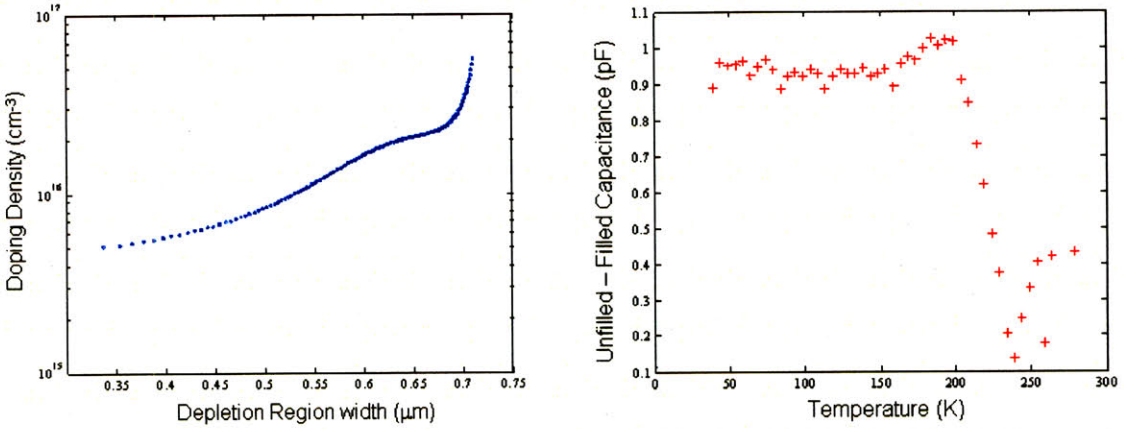
$$N_T = \frac{2(C_{unfilled} - C_{filled})}{C_{unfilled}} N_A \qquad \text{(Equation E.1a)}$$

$$X = \frac{E_p}{K_B T_{1/2}} \cong Ln\left(A_P T_{1/2} / BLn(2)\right) - Ln(X) \qquad \text{(Equation E.1b)}$$

where N_A is the doping concentration in the intrinsic region, E_P is the bandgap location of the trap, $T_{1/2}$ is the temperature at which the difference in unfilled and filled capacitance has dropped by half, A_P is a value that varies between $10^{12\pm1}$, and B is the linear ramp rate of the temperature in units of K/seconds. Figure E.1 shows the doping profile and TSCAP measurements for a 200 x 200 μm^2 PD photodiode. For values of N_A of 10^{16} cm^{-3}, $T_{1/2}$ of 225 K, B of 0.1 K/seconds, N_T is calculated to be 2 x 10^{15} cm^{-3} and a trap location of 0.63 eV is determined relative to the valence band.

Although these TSCAP measurement results are tentative, they do indicate that there is a very high density of traps in the photodiode under reverse bias.

These traps are also electrically active and can possibly contribute to the leakage current.

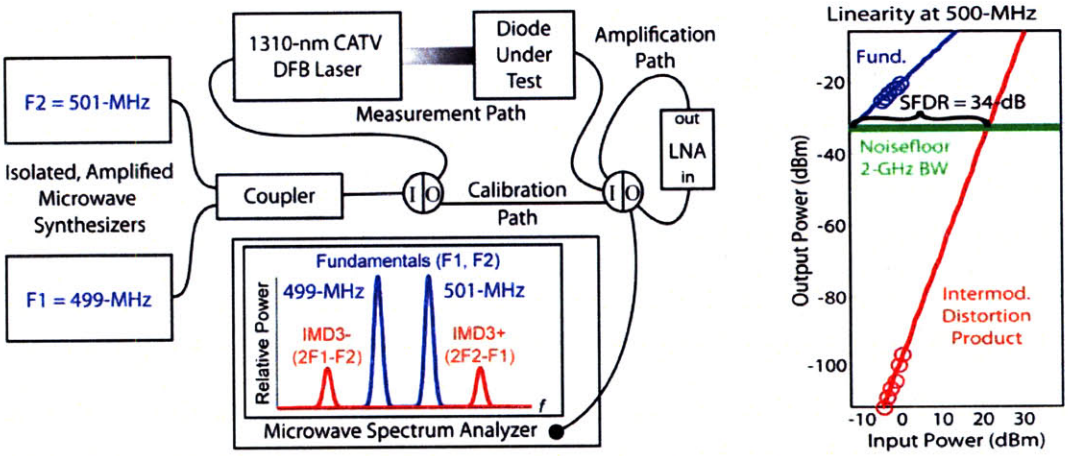


(a) (b)

Figure E.1 (a) Doping Diagram of a 200 x 200 μm^2 PD photodiode extracted from CV measurements, yielding an approximate intrinsic region p-type doping of 10^{16} cm^{-3} (b) TSCAP measurement showing the difference between unfilled and filled state capacitance as a function of temperature between 30 – 270 K. The photodiode was biased at –1 volt. The extracted trap density is 2 x 10^{15} cm^{-3}, with a trap bandgap location of 0.63 eV relative to the valence band edge. Measurements courtesy of Xiaochen Sun.

Appendix F: PD Photodiode (Wafer 11-8) Linearity Measurements

The linearity of the PD photodiode was measured. The photodiodes are required to translate pulse amplitude information into an electrical signal with sufficient linearity for a specified Effective Number Of Bits (ENOB). To characterize the linearity, the spur-free dynamic range (SFDR) of the diodes was measured by Jason Orcutt using the test setup shown in F.1 (a). To calculate the SFDR, the spectrum of the photodiode response to a two-tone RF-modulated input is measured as a function of modulation amplitude. As shown in the microwave spectrum analyzer screen inset to F.1 (a), third-order nonlinearities produce in-band intermodulation distortion products (IMD3) that limit the dynamic range of the detector. To ensure that observed nonlinearities are caused by the diodes, the output of the link laser was examined by using a lightwave front-end to the microwave spectrum analyzer and by replacing the Ge photodiodes with industry-standard Epitaxx InGaAs p-i-n photodiodes designed for CATV applications. To complete the data required to calculate SFDR, the noise floor of the link was measured, roughly integrating over a 2-GHz bandwidth with the microwave spectrum analyzer. This data and the calculated SFDR are shown in F.1 (b). The demonstrated 34-dB SFDR of this link would currently allow for 5.6 effective bits for an ADC at a bias of –3 V.



(a) (b)

Figure F.1 (a) Diagram showing the SFDR measurement setup. The I/0 blocks are microwave switches that enable switching between the measurement path and the calibration path, as well as the insertion of the optional amplification path. The block labeled LNA in the amplification path is a low-noise amplifier. (b) Spur-free dynamic range measurement on a 100 μm x100 μm^2 Ge photodiode. The diode was biased at -3 volts. Measurement courtesy of Jason Orcutt.

Appendix G: Resolving J_A difference between PD and AD Ge-on-Si Photodiodes

This appendix addresses the 3.7x difference in the area coefficient values for the perimeter dependent photodiodes from wafer 11-8 and the area coefficient values for the area dependent photodiodes from wafer 20-12. The 10 μm square PD photodiode essentially has the entire diode surface area covered by the 5 – 7 μm wide "perimeter" trap dominated zone in Figure 4.19 (a), and the 20 μm square photodiode has 75 - 91% of its surface area covered by the trap dominated zone. When the 10 and 20 μm square PD photodiodes are removed, J_A increases to 6.7 – 6.9 mA/cm2, while J_P stays at ~ 0.05 mA/cm. This is within ~20% of the J_A value of 8.5 mA/cm2 for the AD photodiodes, and is within acceptable ranges of variation for these photodiodes. The J_P value for the PD photodiodes changes very slightly from 0.06 mA/cm to ~0.05 mA/cm.

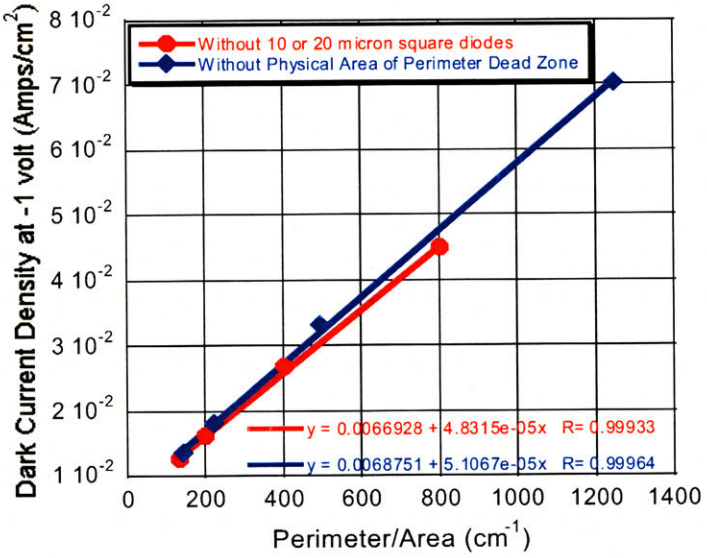


Figure G.1 Plot of Dark Current Density versus Active Perimeter / Active Area for the PD photodiodes. This plot leads to an increase in the extracted PD photodiode J_A coefficient of ~3x relative to Figure 4.7 (a). The new value of J_A coefficient is 6.7 – 6.9 mA/cm^2 and more closely matches the value of 8.5 mA/cm^2 extracted for the AD photodiodes. The J_P coefficient for the PD photodiodes changes slightly relative to Figure 4.7 (a), dropping from 0.06 mA/cm to ~0.05 mA/cm.

Appendix H: Design of Waveguide Coupled Ge-on-Si Photodiodes for Optical Interconnect Applications

H.1 INTRODUCTION

This appendix will address one of the next steps in incorporating Ge-on-Si photodiodes onto the VLSI platform via waveguide coupling of the light to the photodetector. An overview and analysis of various factors affecting waveguide and photodetector design is presented.

H.2 MOTIVATION

Silicon chips are now an essential part of the global technological infrastructure, with uses ranging from cell phones to pacemakers. This explosion of chip usage has been largely driven by Moore's law, which states that the feature size of chips will reduce exponentially and the processing speed of chips will be double every 18 months, leading to an exponential drop in price for ever faster devices. Unfortunately, the scaling trend captured in Moore's law is becoming more and more difficult to maintain. One of the main problems that will have to be overcome to maintain Moore's law in the next few generations of silicon chip design is the growing inability of electrical interconnections to keep up with device scaling. This looming problem has been highlighted by the roadmaps created by the Semiconductor Industry Association (SIA). These roadmaps show that on semiconductor chips themselves, where interconnects are short and numerous, interconnects will soon become very difficult. It is already

the case for electrical interconnections between chips that the performance is dominated by the interconnection medium rather than the devices at either end; it is expected that sometime in the next decade, this trend will migrate down to many connections on chips [96].

There are many approaches to solve the interconnect challenge, for instance the design architecture and system layout can be modified to minimize interconnect latency and distance [96]. The approach that will be focused on in this appendix is to remove the interconnection problem by changing the physical means of communicating between devices. Optical interconnection is emerging as a viable candidate that addresses most, if not all, of all the problems with the next generation of electrical interconnects. For example, electrical interconnects have aspect ratio limitations, as dimensions are shrunk, the resistance increases, increasing the latency of the line. This aspect ratio dependence is not the case with optical interconnects. Moreover, optical signal do not have the requirement for impedance matching, or signal degradation due to cross talk at small dimensions and high frequencies, or the inductance difficulties that plague electrical interconnections. A smaller, but rather significant point is that optical interconnects are virtually independent of the clock frequency for short distances, such as those for on-chip applications, unlike electrical interconnects that can only function within a very narrow bandwidth window. This makes the design of optical interconnects potentially easier and tremendously simplifies redesign of layouts.

Optical interconnection will require three main components, a light generator (laser), a waveguide to channel the light, and a photodetector. The topic of this appendix will not be the laser portion of the optical interconnect package, but will focus on the waveguide and the secondarily, the photodetector. In analyzing the waveguide design, the main criteria will be selecting between a silicon waveguide or a deposited waveguide in a CMOS silicon compatible process, and secondarily how this material choice impacts the performance of the photodetector.

The major difference between using a silicon waveguide and utilizing a deposited waveguide will be the significant change in the index of refraction for the core layer. The index of refraction for silicon is 3.5, while that for a deposited waveguide can range between 1.45 for silicon dioxide to 2.01 for a silicon nitride layer. The higher index of refraction for silicon leads to challenges for low loss coupling to either a fiber or to a photodetector, while also making sidewall roughness (scattering loss increases as a function of Δn^3) a significant issue. On the other hand, the high index of refraction for silicon minimizes the size of the waveguide and enhances the ability to have bends or curves along the length of the waveguide, potentially significantly lowering the footprint of this waveguide.

Deposited waveguides such as silicon dioxide and silicon nitride core waveguide boast low loss and easy coupling to fibers or photodetectors, potentially enhancing the signal to noise ratio (SNR) and lowering the size of the required photodetector. The low index of refraction for these films though, leads to larger footprints for the waveguide, so there is more use of the on-chip real

estate. In the sections below we will discuss in more detail the advantages and disadvantages of utilizing in-silicon waveguides versus utilizing on-silicon waveguides.

H.3 IN-SILICON PHOTONICS

H.3.1 Waveguide design

One advantage of silicon for the integrated optical applications is the availability of high quality substrate material at low costs. In addition there is a wealth of processing expertise that is readily applicable to the fabricating silicon waveguides. For this application, the core of the waveguide will be silicon and the cladding will be considered to be silicon dioxide. One of the reasons for this material choice is that atomically smooth Silicon On Insulator (SOI) is commercially available, thus making the bottom cladding material and core material readily available in one step. Moreover, for the top cladding material, silicon dioxide can either be grown or deposited. If grown on the silicon core layer, the interfacial roughness between the silicon and silicon dioxide film will have a roughness on the order of ≤ 3 nm [97] that is generally better than a deposited film. Silicon oxynitrides or silicon nitrides layers will have to be deposited and the interface will therefore be rougher than the grown silicon dioxide film. One issue with having a silicon core and a silicon dioxide cladding is the high index difference, Δn, of 2.05. This leads to the need for a smaller

waveguide, on the order of 100 nanometers in width, at the telecom wavelength ranges of 1.3 and 1.55 μm in order to facilitate single mode operation.

This high index contrast, though also leads to high coupling loss when coupling light from an optical fiber into the waveguide. The general approach to solving this problem has been to taper the waveguide, with a wide or narrow initial waveguide facet coupling to the optical fiber, that tapers into the waveguide channel. Tapers allow for a reduction in coupling loss through an adiabatic modal transformation and can also be used to increase the alignment tolerance of other optical devices, such as III-V lasers. Several taper methods have been proposed and have demonstrated efficient coupling from a relatively large silicon waveguide into an optical fiber. Tapers from the waveguide dimensions to the fiber dimensions for improving coupling efficiency between optical-fiber and waveguide modes have been suggested. However, to avoid excessive coupling to radiation modes in the taper, the required typical taper length must be of the order of millimeters [98]. In addition, unless carefully designed, these tapers can suffer from strong back reflections at the facet of the coupler. Complicated tapers have been suggested based on high-refractive-index materials in order to decrease the length to ~5.5 μm [99]. Quarter-wavelength plates are embedded at the curved facet of the coupler to prevent back reflections, whereas layered structures with a graded index variation are introduced in the vertical direction. However, fabrication of such a structure requires several steps, and the theoretical coupling losses were estimated to be ~1 dB. Inverse tapers, from the waveguide dimensions to the dimensions of a small tip, have been proposed for coupling laser diodes to

optical fibers [100]. These structures rely on the evanescent field at the tip to increase the mode size of the waveguide to that of the fiber. However, these structures are hundreds of microns long, and their coupling losses are fundamentally limited to ~1.3 dB. This is mostly a result of a high-effective-index mismatch between the optical fiber and the waveguide that lead to relatively strong back reflections [101]. In summary, it appears that tapers on the order of millimeters, although wasteful of real estate, minimize the coupling loss to ~0.4 dB/facet. If on-chip real estate is considered to be more important, nanotapers on the order of 40 μm in length can give a coupling loss of ~ 6 dB/facet [101].

Most of the propagation losses in the high index contrast waveguides have been found to be due to the interfacial sidewall roughness between the core and cladding regions. The propagation losses are a strong function of the sidewall roughness once the size of the waveguide drops below 4 μm [102]. This is captured in Figure H.1 below.

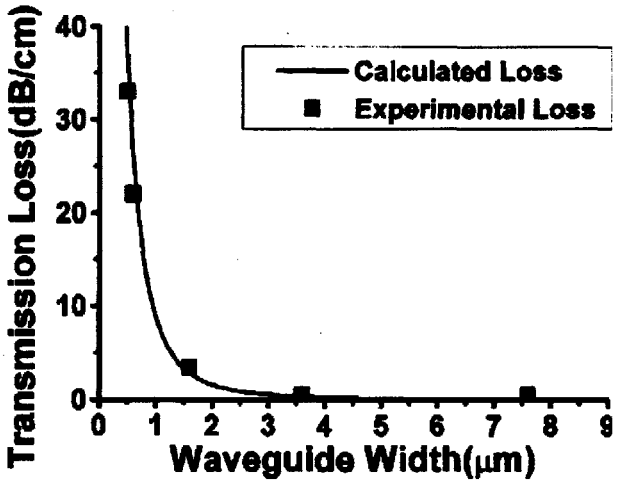


Figure H.1 Once the silicon core width drops below 4 μm, the transmission loss increases almost exponentially due to the effect of sidewall roughness [102]

It has been theoretically demonstrated that if the interfacial sidewall roughness is reduced below 0.5 nm, the optical propagation loss can be reduced to 0.1 dB/cm [102]. Recently, for submicron sized silicon waveguides, optical propagation losses between 0.4 – 0.8 dB/cm has been demonstrated [103, 104].

On a positive note, the high index contrast for this material system leads to very low bending loss. For a bending radius of 1 μm, it has been demonstrated that the bending loss is below 0.1 dB/cm [105]. For a bending radius of 2 μm and above the propagation loss associated with the bend drops below 0.05 dB/cm. This implies that the high index waveguide can have an extremely small footprint and save on a significant amount of on-chip real estate.

In the design under consideration in this appendix, the waveguide material choice was silicon for the core material of thickness 0.25 μm and silicon dioxide cladding thickness of 3 μm. The vertical confinement factor for this design is 0.86. In order to couple to the outside world, the silicon core region was expanded to 12 x 12 μm^2, which has been demonstrated to have losses of 0.4 dB/facet when connecting to standard optical fibers at 0.8 – 1.55 μm wavelengths [98]. The taper structure is formed by selective, single-crystal epitaxial silicon overgrowth on a 3 μm SOI substrate followed by etching to leave an adiabatic tapered waveguide structure that has a uniform height but varying width, as depicted in Figure H.2. The propagation loss for this design is expected to be on the order of 0.5 dB/cm.

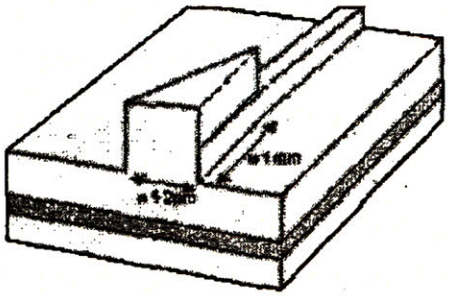


Figure H.2 The waveguide coupling is 12 x 12 μm^2 square for fiber coupling losses on the order of 0.5 dB/facet and the length of the taper region is approximately 1.5 mm to reduce propagation losses [98].

H.3.2 Photodetector design

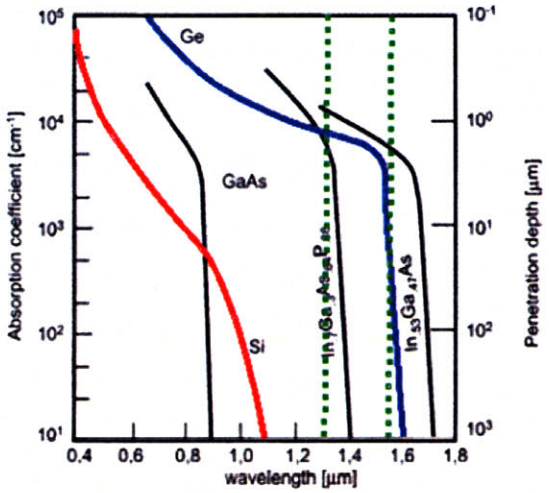


Figure H.3 Replot of Figure 1.2 (a) of absorption coefficient versus wavelength for different materials, the wavelengths of interest, 1.3 and 1.55 µm are marked by green dashed lines [10].

The high index for the silicon core region should lead to the requirement of a long waveguide and photodetector overlap region in order to extract the majority of the optical power from the waveguide. This is generally the case when working with $Si_{1-x}Ge_x$ films as the photodetecting material. Unfortunately, $Si_{1-x}Ge_x$ films do not have a high absorption coefficient at wavelengths between

1.3 to 1.5 μm desired in our application. Increasing the germanium composition in the film can improve the absorption coefficient, but also lowers the thickness limit of the $Si_{1-x}Ge_x$ film prior to relaxation, leading to a tradeoff between responsivity and absorption coefficient [10]. Generally, pure germanium films have not been utilized in the past due to the expected high number of defects that increase the dark current and thus decrease the SNR. It has recently been demonstrated that cyclically annealed Ge films have threading dislocation densities (TDD) on the order of ~ $10^7 cm^2$ and thus for an area of ~ 10 μm^2, few defects are expected [25]. Therefore, if the size of a Ge photodetector is carefully designed, there should be little impact of Ge TDD on the expected SNR.

H.3.3 Simulation results

Under these conditions, the photodetector material was selected to be a germanium film deposited on a silicon substrate, due to the high index of refraction of this material and the absorption coefficient >10^3 cm^{-1} at the wavelengths between 1.3 to 1.55 μm. As shown below in Figure H.4, the absorption between the waveguide and a 0.5 μm-thick Ge photodetector is approximately 1.62 dB/μm at a wavelength of 1.55 μm. In order to absorb 99% of the incoming light, the photodetector region therefore has to be at least 12 μm long. Another important consideration is to minimize the capacitance and the appearance of TDD's, hence the width of the photodetector region is selected to be 0.75 μm, leading to an area of 9.25 μm^2. Plugging all these values into Equation 2.11, the maximum frequency that the photodetector can operate is

determined to be 51 GHz, with the major contribution to the 3-dB roll-off being the transit time limited movement of the holes. In this estimate, the series resistance R is assumed to be 100 Ω (Nominal series resistance measurements from fabricated Ge photodetectors is 70 Ω), the capacitance was found to be 3.1 fF, the depletion region width of the detector is assumed to be 0.5 μm, and the saturation velocity of holes in germanium was assumed to be 6.7 x 10^6 cm/s [32].

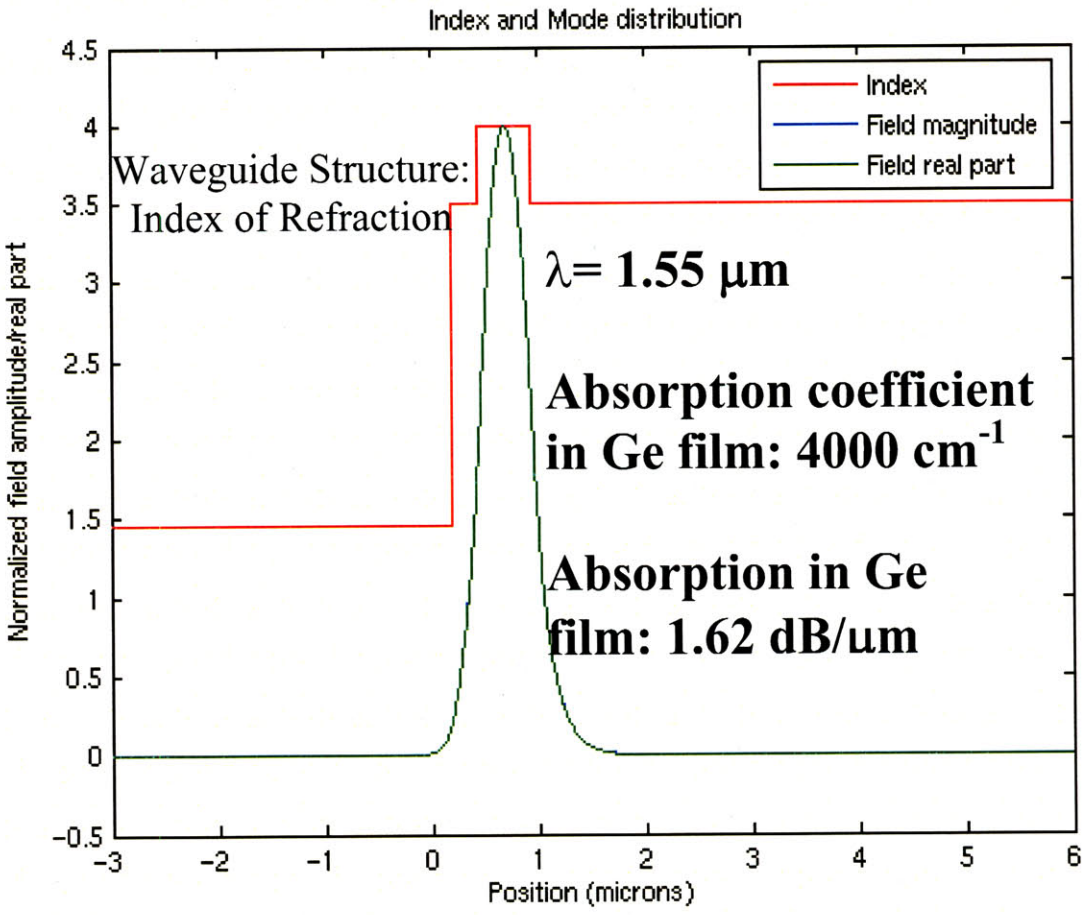


Figure H.4 Simulation results for coupling of in-silicon waveguide to the Ge photodetector. As is evident, the Ge with index of 4, essentially becomes the core of the waveguide, after the Si with the index of 3.5 couples to the Ge photodetector. The simulation also shows the absorption in Ge is 1.62 dB/μm at a wavelength of 1.55 μm.

H.4 ON-SILICON PHOTONICS

H.4.1 Waveguide design

On-silicon deposition methods generally utilize low contrast waveguides, hence have much less problems coupling to standard fiber optics. This also means that long tapers are not generally required, thus it is possible to use microns, instead of millimeters to couple with low loss from the fiber to the waveguide. The coupling loss for these low contrast waveguides is generally less than 1 dB/facet, if they are carefully designed. Furthermore, standard CMOS compatible process can be used to define the cladding and core regions on a standard silicon substrate without using a SOI substrate. The material choices for the core layers are Si_3N_4 (n = 2.01) and SiO_xN_y (n = 1.45 [SiO_2] – 2.01 [Si_3N_4]) with the cladding layers being a selection between air (n = 1) and SiO_2 (n = 1.45). In general, for reasonable confinement of the light, the index contrast should be greater than 0.3. Controlling the index of SiO_xN_y layers across the wafer also takes careful control of the deposition conditions [106]. Thus, the least complicated fabrication choices for the core/cladding materials are between SiO_2/air and Si_3N_4/SiO_2. In order to choose between these materials, the proposed structure for the waveguide should also be examined. The generic structures for on-silicon waveguides are rib waveguides, channel waveguides, and strip waveguides. The different representations for all 3 waveguide designs are illustrated below in Figure H.5.

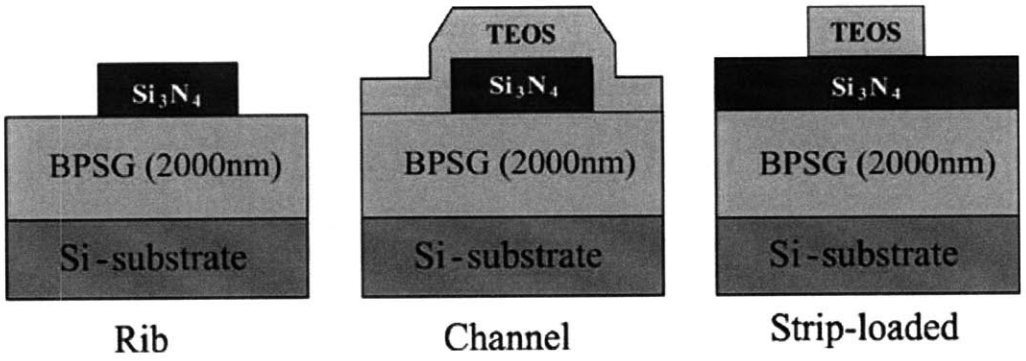


Figure H.5 Three different waveguide structures analyzed for channel (propagation) loss at 700 nm. The channel waveguide gave the lowest propagation losses at 0.1 dB/cm [108].

These 3 different structures have been evaluated by Daldosso [107]. All the structures were examined had a Si_3N_4 core waveguide and a SiO_2 cladding layer. The propagation losses were found to be lowest for the channel structure at 780 nm wavelength. The propagation loss is expected to be higher at the wavelengths of interest between 1.3 – 1.55 μm, but from prior experimental studies should be ~0.8 – 1.4 dB/cm, in part due to vibrational losses in the Si_3N_4 layer. It is expected that using LPCVD deposition of the Si_3N_4 layer will suppress the vibrational absorption losses at higher wavelengths associated with the Si-H and N-H bonds seen in prior studies [107, 108].

Utilizing SiO_2 and air as the core and cladding material implies the bottom buffer layer has to be greater than 9 μm to minimize loss due to substrate leakage to the high index of refraction silicon film. The requirement for such thick layers ensures that single mode operation will be difficult to ensure. Moreover, air as the cladding material can lead to impurity incorporation over time, slowly degrading the waveguide characteristics [108]. Thus it appears that a Si_3N_4 core channel waveguide with a SiO_2 cladding layer gives one of the best combinations of characterisitics for the desired application.

The bending loss for a Si_3N_4 core channel waveguide with a SiO_2 cladding layer is below 0.1 dB/cm for bending radii of 2 – 3 mm, and for 20 μm bends, the loss is between 1 – 2 dB/cm [115]. Hence, the taper real estate gain for low contrast waveguides relative to high contrast waveguides are compensated for if bends are required in the waveguide layout, such as for y-splitting.

In this section, the waveguide material choice is silicon nitride for the core material with a thickness of 0.6 μm and silicon dioxide for the cladding with a thickness of 3 μm. The vertical confinement factor for this design is 0.86. In order to couple to the outside world, the silicon nitride core region was kept at 0.6 x 0.6 μm^2, which has been demonstrated to have losses less than 0.5 dB/facet when connecting to standard optical fibers at 0.8 – 1.55 μm wavelengths in structures similar to those as used to generate the curve in Figure H.6. The propagation loss for this design is expected to be on the order of 1 dB/cm.

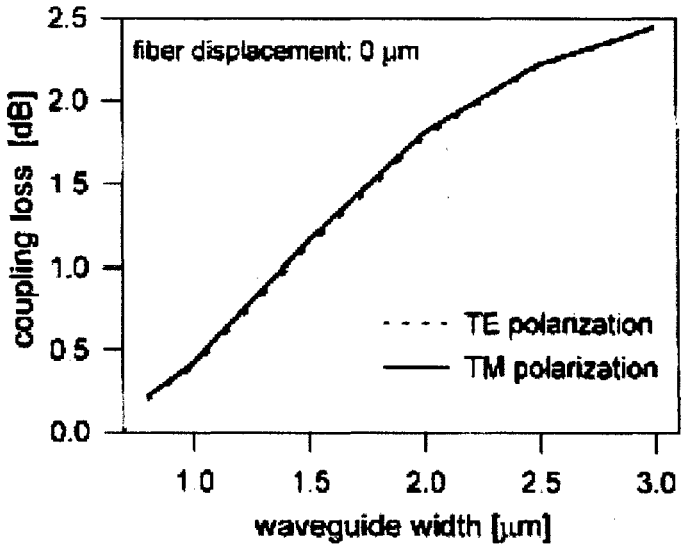


Figure H.6 As the waveguide width decreases for a SiON waveguide, the coupling losses to an optical fiber drops almost linearly. Small changes in fiber displacement also do not appreciably increase the coupling loss [106].

H.4.2 Photodetector design

The prior argument proposed in the section dealing with the choice of materials for in-silicon photodetector still applies for this waveguide structure, hence the photodetector material will again be germanium.

H.4.3 Simulation results

As shown below in Figure H.7, the absorption between the waveguide and a 0.5 μm-thick Ge photodetector is approximately 1.67 dB/μm at a wavelength of 1.55 μm. In order to absorb 99% of the incoming light, the photodetector region therefore has to be at least 12 μm long. Another important consideration is to minimize the capacitance and the appearance of TDD, hence the width of the photodetector region is selected to be 1 μm, leading to an area of 12 μm^2. Plugging all these values into Equation 2.11 and utilizing the standard values defined in Section H.3.3, the maximum frequency that the photodetector can operate at is determined to be 50.9 GHz, with the major contribution to the 3-dB roll-off being the transit time limited movement of the holes.

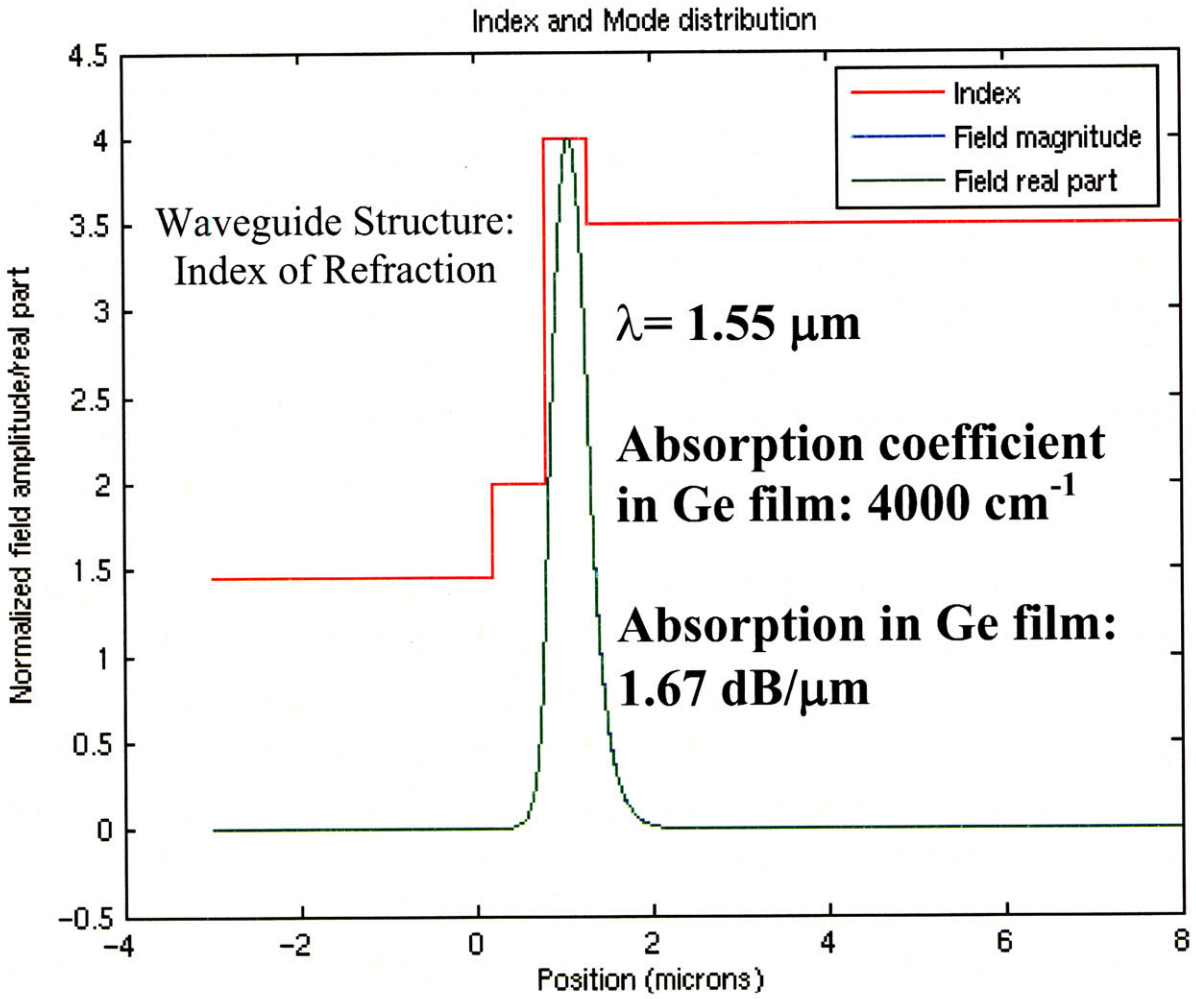


Figure H.7 Simulation results for coupling of on-silicon waveguide to the Ge photodetector. As is evident, the Ge essentially becomes the core of the waveguide versus the Si_3N_4 core waveguide material. The simulation also shows the absorption in Ge is 1.62 dB/μm at a wavelength of 1.55 μm.

H.5 CONCLUSION

Parameter	In-silicon design	On-silicon design
Substrate	SOI	Silicon
Fiber coupling depth x width	12 μm x 12 μm	0.6 μm x 0.6 μm
Fiber coupling loss	0.5 dB/facet	0.5 dB/facet
Taper Length	1.5 mm	0
Core material	Si (n = 3.5)	Si_3N_4 (n = 2.01)
Core depth x width	0.25 μm x 0.5 μm	0.6 μm x 0.6 μm
Cladding material	SiO_2 (n = 1.45)	SiO_2 (n = 1.45)
Top Cladding depth	3 μm	3 μm
Bottom Cladding depth	3 μm	3 μm
Index contrast	Δn = 2.05	Δn = 0.55
Vertical Confinement	0.86	0.86
Channel loss	0.5 dB/cm	1 dB/cm
Bending Loss	<0.1 dB/cm in 1 μm bend	0.1 dB/cm in ~2 mm bend
Detector Length	12.3 μm	12 μm
Detector Width	0.75 μm	1 μm
Detector depth	0.5 μm	0.5 μm
F_{3dB}	51 GHz	50.9 GHz

Table H.1 Summary of results for In-silicon and On-silicon waveguide and photodetector design

The waveguide properties for in-silicon and on-silicon waveguides are fairly similar. The major weaknesses of the in-silicon waveguide are the difficulty of coupling to the fiber, but if on-chip real estate is sacrificed, the losses are comparable or lower than that of low contrast (on-silicon) waveguides. The roughness of the on-silicon deposition process makes it difficult to control the propagation losses, and if there is any fan out of the waveguide required (bends), for losses comparable to in-silicon waveguides, the turns have to very wide, again using valuable real estate. Another subtle point is in-silicon results are best for SOI substrates that are more expensive relative to the silicon substrates used for

the on-silicon analysis. On the other hand, the cost of SOI wafers will drop if the manufacturing volume increases, so the current cost advantage for the on-silicon approach could be temporary. Looking at both waveguides, the fabrication cost and complexity is approximately equal for both, and the in-silicon waveguides can currently yield slightly lower propagation channel loss due to better control of the sidewall roughness and fabrication processes, and also minimally higher photodetector frequency, due to the smaller capacitance associated with a smaller waveguide. The above two factors, channel loss and smaller photodetector area, also yield better signal quality, and thus slightly better Bit Error Rates for the in-silicon waveguide coupled with a Ge photodetector. In conclusion, in-silicon is currently the better technological option, but it is easily foreseeable that with slightly better fabrication techniques and/or novel approaches, on-silicon could become the desired industrial choice.

Appendix I: Unique Simulation Code

I.1 INTRODUCTION

This appendix gives a sample of the Medici and Matlab code used to generate some of the figures and results shown in this thesis. The code shown in this section is unique to the equipment and devices utilized and fabricated in the course of completing this thesis. Thus, the majority of the code not shown in this section can be easily replicated by following well known optical theory and/or semiconductor physics.

I.2 Medici Code for Photodiode Dark Current Simulation

```
TITLE Ge PHOTODETECTOR

$ This code uses the optimize function to modify Ge material parameters to match
$ observed voltage dependence of the 11-8 PD photodiode.

MESH

x.MESH node=1 location=0
x.mesh node=3 location=2.25
x.mesh node=5 location=2.75
x.mesh node=8 location=5
y.mesh node=1 location=-0.2
y.mesh node=2 location=0
y.mesh node=10 location=0.2
y.mesh node=80 location=0.4
y.mesh node=90 location=4

region number=1 x.min=0   x.max=2   y.min=-0.2 y.max=0   oxide
region number=2 x.min=2   x.max=5   y.min=-0.2 y.max=0   Polysilicon
region number=3 x.min=0   x.max=2.5 y.min=0   y.max=0.2 oxide
region number=4 x.min=2.5 x.max=5   y.min=0   y.max=0.2 Polysilicon
region number=5 x.min=0   x.max=5   y.min=0.2 y.max=2.2 germanium
region number=6 x.min=0   x.max=5   y.min=2.2 y.max=4   Silicon

ELECTRODE NAME=Anode bottom x.min=2.875 x.max=4.625
ELECTRODE NAME=Cathode top  x.min=2.875 x.max=4.625
```

```
PROFILE P-TYPE N.PEAK=1E10 UNIF X.MIN=0 X.MAX=2.5  Y.MIN=0
Y.MAX=0.2
PROFILE p-TYPE N.PEAK=1E15 UNIF X.MIN=0 X.MAX=5  Y.MIN=0.2
Y.MAX=2.1
PROFILE impurity=p N.PEAK=3E20  X.MIN=2 X.MAX=2.5 Y.MIN=-0.1
Y.MAX=-0.1 Y.CHAR=0.055 X.CHAR=0.055
PROFILE impurity=p N.PEAK=3E20  X.MIN=2.5 X.MAX=5 Y.MIN=-0.1
Y.MAX=0.1 Y.CHAR=0.055 X.CHAR=0.055
PROFILE P-TYPE N.PEAK=2E19 UNIF X.MIN=0 X.MAX=5  Y.MIN=2.1
Y.MAX=2.2
PROFILE P-TYPE N.PEAK=2E20 UNIF X.MIN=0 X.MAX=5  Y.MIN=2.2
Y.MAX=4

assign name=bandgap n.val=0.77

loop optimize
assign name = traphigh up=5e19  low=1e18 n.val=8.1776e18   optimize
assign name = traplow  up=1e19  low=1e17 n.val=3.4072e17 optimize
assign name = bandend  up=0.37  low=0.01 n.val=0.1404   optimize
assign name = tunnelm  up=2     low=1e-2 n.val=3.5412e-2 optimize
assign name = trapreg  up=0.26  low=0.21 n.val=0.25   optimize

$assign name = traphigh n.val=1e20
$assign name = traplow  n.val=2.0941e18
$assign name = bandend  n.val=0.001
$assign name = tunnelm  n.val=0.1023
$assign name = trapreg  n.val=0.19

material germanium m.rtun=@tunnelm eg300=@bandgap

ASSIGN NAME=EV N.VAL=-0.5*@bandgap
ASSIGN NAME=EC N.VAL=0.5*@bandgap
COMMENT Calculate characteristic length for hole states
ASSIGN NAME=PCHR N.VAL=(-1*@bandend-
@EV)*LOG(@traphigh/@traplow) PRINT
COMMENT Generate hole traps
TRAP DISTR TAUN="1E-10" TAUP="1E-10" N.LEVEL=20 N.TOT="-
(@traplow+@traphigh*EXP(-(@FENER-@EV)/@PCHR))"
+ COND="@x>1&@x<2.75&@y>0.19&@y<@trapreg"
+ out.file=testp x.plot=4.65 y.plot=0.48

COMMENT Calculate characteristic length for electron states
ASSIGN NAME=NCHR N.VAL=(@EC-
@bandend)*LOG(@traphigh/@traplow) PRINT
COMMENT Generate electron traps
```

```
TRAP DISTR TAUN="1E-10" TAUP="1E-10" N.LEVEL=20
N.TOT="(@traplow+@traphigh*EXP((@FENER-@EC)/@NCHR))"
+ COND="@x>1&@x<2.75&@y>0.19&@y<@trapreg"
+ out.file=testn x.plot=4.65 y.plot=0.48
$ measured region of Si/Ge interdiffusion from Lot 11-7 is 25 - 50 nm deep
solve
sym newt carr=2
log      ivfile="PIN_IV"
Models consrh r.tunnel temp=300
method itlimit=100
SOLVE V(Cathode)=0 V(Anode)=-0.2
extract name=i02300 exp="abs(@i(Anode))" cond="@V(Anode)=-0.2" now
SOLVE V(Cathode)=0 V(Anode)=-1.0
extract name=i1300  exp="abs(@i(Anode))" cond="@V(Anode)=-1.0" now
extract name=slope300 exp="@i1300/@i02300" now target= 6.79 tartol=0.5
tarrel=0.01
echo @i1300
stop
```

I.3 Matlab Code for Photoemission Image Extraction and Superimposition

```
function [result] = SUextract(picture);
% Function that extracts the image from Sensor Unlimited's camera
c=fopen(picture);
b=fread(c,[640,240],'uint8');
m=b(1:2:end,:); % pick out leading 4 bits
l=b(2:2:end,:); % pick out remaining 8 bits
result=m*256+l; % calculate full 12 bit image
%imagesc(result);
axis equal

function [result,new_map] =
superimpose(Suextract(background),Suextract(picture));

%% created by Jim Fiorenza & modified by Oluwamuyiwa Olubuyide
% This MATLAB program superimposes light emission data onto a
% background image.  It first loads a background
% image and a picture image.  It then removes the low intensity pixels in
% the picture and superimposes the truncated picture on top of the
% background. The program manipulates the color tables such that the
% picture is displayed using different colors than the background.

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
```

```
% Inputs to control program       %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
% Setting to control the portion of the picture that is truncated
% For example: a setting of 1/4 means that the pixels that are in the
% lowest quarter of intensity in the picture are removed.

pic_blank_portion=1/4;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%


% Crop picture and background
bk = background;
pic_crop=picture;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Set up a new color map where the lower part of the map is black and
% white and the upper part is colored
colormap('default');

blank_num=1/pic_blank_portion;
% Set up the color map to be the right size for the background (64)
bk_colormap=bone;

% Set up the color map to be the right size for the picture (variable) and
%generate the color map for the picture
pic_map_size=64*(blank_num-1)+20;
map_resize=zeros(pic_map_size,3);
colormap(map_resize);
pic_colormap=hot(pic_map_size);



colormap('default');

% Construct color map with lower portion for the background and upper
% portion for the picture.

total_map_size=(blank_num)*64;
new_colormap=zeros(total_map_size,3);
new_colormap(1:64,:)=bk_colormap;
new_colormap(65:total_map_size,:)=pic_colormap(21:64*(blank_num-
1)+20,:);
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

blank_num=1/pic_blank_portion;


% Scale picture and background so that minimum is zero
min_bk=min(min(bk));
min_pic=min(min(pic_crop));
bk=bk-min_bk;
pic_crop=pic_crop-min_pic;

% Find out what is the maximum intensity in the picture and the
%background
max1_bk=max(bk);
max_bk=max(max(bk));
%max_pic=2000;
max_pic=max(max(pic_crop));

% Normalize the background and picture to a maximum intensity of 1
bk_norm=bk/max_bk;
pic_norm=pic_crop/max_pic;
pic_norm=pic_norm/max(max(pic_norm));

%set lower quarter of the picture intensity range to zero
%min intensity is 1 max intensity is 4
% cut off lower 25% to avoid "smear"
pic_temp=pic_norm-0.4;
pic_temp=pic_temp*4;
pic_temp=max(pic_temp,0);
pic_temp(find(pic_temp>0))=pic_temp(find(pic_temp>0))+1.001;
pic_show=pic_temp;

%Erase all elments in the background that have elements in the picture
%that aren't zero
bk_temp=bk_norm.*(pic_temp==0);
%pic_show;
%bk_show=(bk_temp+abs(bk_temp))/2;

% Scale the background so that the maximum background pixels don't
%appear as the minimum picture pixels
bk_show=bk_temp*0.99;

bk_show=bk_show;
pic_show=pic_show;
```

```
%Create the final image with the picture on top of the image
pic_final=pic_show+bk_show;


%plot and adjust the picture
result=pic_final;
new_map=new_colormap;
colormap(new_map);
imagesc(result);
axis equal
```

I.4 Matlab Code for Modes in a Leaky Waveguide

```
2D modesolver: 1D problem with straight leaky waveguide
% Created by Milos Popovic, Mar 9, 2002; modified by Oluwamuyiwa Olubuyide
% Example from W.P. Huang et al, "PML BC for Modal Analysis", IEEE PTL
% Vol.8, No.5, May 1996
%
% Notes: Works well with xmin = -2e-6, xmax = 12e-6, dPML = 4e-6, sigmamax
% = 40000.

clear all; close all;

% Problem (Leaky Mode Waveguide)

% Waveguide Setup

lam = 1550E-9;                          % Wavelength
abscoefficient = 10*100;                % Absorption coefficient in meter^-1
nI = abscoefficient/(2*2*pi/lam);
n1 = 1.46;  n2 = 3.5; n3=1.46;          % Index for waveguide core/cladding region
x1 = 0E-6; x2 = x1+0.25E-6; x3 = x2+4E-6; % Thickness of layers
xmin0 = -3e-6; xmax0 = 6e-6; h = 0.005E-6; % Region to be analyzed
neff_guess = n2;
dPML = 3E-6;  %6E-6;                    % Thickness of PML layer (meters)
sigmaMAX = 1e5; %40000; %10000; %6853;                                  % Max
conductivity in absorbing boundary (PML Layer), 1/(ohm meters)


x = [xmin0 : h/2 : xmax0].';            % Set up computational domain grid in
x, twice as dense as discretization pixel size h
n = ones(length(x),1) * n3;             % Create a vector containing index
distribution vs. x
   n(find(x<x3)) = n3;
```

```
   n(find(x<x2)) = n2;
   n(find(x<x1)) = n1;
   % Dielectric constant averaging between pixels for more accurate (O(h^2))
answers [MP] Oct 15, 2002
   n(3:2:end-2,:) = sqrt( (n(2:2:end-3,:).^2 + n(4:2:end-1,:).^2)/2 );
N.x = x(:); N.y = [-2:2].' * h/2; N.n = (n * [1 1 1 1 1]);  % For 1D problem, the y-
grid is not important but must have at least 5 points (i.e. 2 "pixels").

% Analysis Section:

OPTS.coordmode = 'C'; OPTS.eigmode = 'b'; OPTS.fieldmode = 'MY'; OPTS.BC
= [0 0 0 0];                    % Set up modesolver (see "help m2wcyl")

[beta,F] = m2wcyl(N, 2*pi/lam, 2*pi/lam * neff_guess, OPTS, 1, [1 0 0 0] *
dPML, sigmaMAX * [1 1]);    % Call modesolver

neff = beta/(2*pi/lam)        % Convert real beta to effective index
dBpermicron_guide = -10*log10(exp(-2*imag(beta)*1e-6))   % Convert
imaginary beta to dB/micron

% Plot section:

figure;
plot(x/1e-6, real(n),'r');
title('Index and Mode distribution');
hold;    % Plot mode field vs x, on top pixel of the 2-pixel domain in the y-
direction.
ii = find(abs(F.Ey(:,1)) == max(abs(F.Ey(:,1))));
Eypeak = F.Ey(ii,1);
plot(F.Rz/1e-6, [abs(F.Ey(:,1)/((1/n3)*Eypeak))
real(F.Ey(:,1)/((1/n3)*Eypeak))]);
xlabel('Position (microns)');
ylabel('Normalized field amplitude/real part');
legend('Index','Field magnitude','Field real part',1);


simulation1:
lam = 1550E-9;                    % Wavelength
abscoefficient = 4000*100;              % Absorption coefficient in meter^-1
nI = abscoefficient/(2*2*pi/lam);
n1 = 1.46;  n2 = 3.5; n3 = 4+j*nI; n4 = 3.5;
% From Huang paper "PML for 1D Leaky Mode Calculations"
x1 = 0.2E-6; x2 = x1+0.25E-6; x3 = x2+0.5E-6; x4 = x3+1E-6;
xmin0 = -3e-6; xmax0 = 6e-6; h = 0.005E-6;
neff_guess = n3;
dPML = 3E-6;  %6E-6;                    % Thickness of PML layer (meters)
```

```
simulation2:
n1 = 1.46;  n2 = 2; n3 = 4+j*nI; n4 = 3.5;
% From Huang paper "PML for 1D Leaky Mode Calculations"
x1 = 0.2E-6; x2 = x1+0.6E-6; x3 = x2+0.5E-6; x4 = x3+1E-6;
xmin0 = -3e-6; xmax0 = 8e-6; h = 0.005E-6;
neff_guess = n3;
dPML = 3E-6;  %6E-6;                    % Thickness of PML layer (meters)

waveguide2:
n1 = 1.46;  n2 = 2; n3=1.46;
% From Huang paper "PML for 1D Leaky Mode Calculations"
x1 = 0E-6; x2 = x1+0.6E-6; x3 = x2+4E-6;
xmin0 = -3e-6; xmax0 = 6e-6; h = 0.005E-6;
neff_guess = n2;
dPML = 3E-6;  %6E-6;                    % Thickness of PML layer (meters)
```

Modesolver code:

```
%---------.---------.---------.---------.---------.---------.---------.--------|
%
% Created June 18, 2002 by Milos Popovic, Modified by Oluwamuyiwa
Olubuyide
% Cylindrical-PML 2D mode solver for arbitrary index distributions.
%
% function [mu, F, {V, D, Pr, Pz, Rmtx}] = m2wcyl(S, nu_index, mu_guess,
OPTS, nmodes, dPML, sigmaPML)
%
% ** WARNING **    Modal fields returned [Ex Ey Ez Hx Hy Hz] are defined
%                  along a left-handed Cartesian coordinate system, in
%                  order to stay consistent with rho-phi-z cylindrical
%                  coordinates. I know this is stupid but using [Ex Ez
%                  Ey..] would be just as confusing. Thus if you are using
%                  Cartesian coords, on a right-handed (standard) coord
%                  system, the field values are really [Ex -Ey Ez Hx -Hy
%                  Hz].
%
% OUTPUT:
% mu            = ('w'-mode) energy-mode complex resonant frequencies, w/c
(highest Q first, then lowest frequency first)
%                 ('b'-mode) power-mode complex propagation constants, gamma
=def= beta*R (lowest loss first, then highest eff. index first)
%                 NOTE: for adjoint computations, modes are sorted by largest loss
first
% F             = data structure containing fields of computed modes
% V,D           = exact eigenvalue (D)/eigenvector (V) matrices returned by eigs
without post-processing
% Pr, Pz, Rmtx  = PML complex coordinate stretching factors Pr, Pz and
complex radial coordinate Rmtx
%
% INPUT:          ("pixel" grid is (M-1)x(N-1))
% S             = structure: S.n, S.x(:), S.y(:) = (2M-1 x 2N-1, 1x2M-1, 1x2N-1)
% nu_index      = index of eigenvalue eqn:
%                 # lambda's around in w-mode, frequency w/c in b-mode
% mu_guess      = eigenvalue guess: w guess in w-mode, beta*R (gamma) guess
in b-mode
%   NOTE: mu_guess is converted to w/c ('w'-mode) or gamma (beta*R = beta in
cartesian coords, 'b'-mode) inside the function!
% OPTS.coordmode = cylind'R'ical or 'C'artesian
% OPTS.eigmode   = 'w' or 'b' eigenvalue
% OPTS.fieldmode = 'V'ector or se'MX'ivector (or 'MY' for y-polarization)
% OPTS.BC       = [OPTIONAL] default = [0 0 0 0]; [left right bottom top]
boundary conditions, 0 = PEC, 1 = PMCh.
```

```
% OPTS.adjoint  = [OPTIONAL] default = 0; 0 = normal ([Ex Ey]), 1 = adjoint
([Hy -Hx])
% OPTS.eigsfcn  = [OPTIONAL] default = 'eigs'; can use to set custom sparse
eigenvalue solver
% nmodes        = number of modes to find/compute
% dPML          = pml thickness [left right down up]
% sigmaPML      = max conductivity [horizontal vertical]

% Known Issues: - Omega_tilde, Gamma_tilde/Gamma_hat offsets not yet
% ------------  implemented for proper phase offsets in discrete time/z (FDTD).
%         - Must fix H-field (maybe also E-field) computation at the
%         end to work for PMC boundary conditions!
%         - [Nov272003] Need to fix 'MY' semivector mode to be able to keep only
%           one-pixel-tall domain for TE slab calculations (TM already works).
%
% Updates:
% --------
% Jun 18, 2002 - First version.
% Sep 22, 2002 - Completing ability to compute for beta-eigenvalues.
%           - NOTE: Ez is still *always* calculated assuming cartesian
%           coordinates! This needs to be fixed.
%           - Lparam (nu_index) definition changed from w^2 to k0 for 'b'-mode
%           operation.
% Oct  1, 2002 - Lparam renamed to nu_index; eigguess renamed to mu_guess.
%           - Set VMODE = 1 to display textual debug info; VMODE = 2 plots
%figures also (all mode field plots..)
% Oct  3, 2002 - Changed EOPTS options structure for "eigs" to OPTS so that
%options for eigs can be passed IN to m2wcyl, such as
%           a starting eigenvector. Raw V and D (eigenvalues and eigenvectors)
are also an available output).
% Nov 20, 2002 - Proper calculation of third E-field (Ez, i.e. Ephi) added; H-field
%calculation?
% Nov 26, 2002 - Proper calculation of H-field (for radial or Cartesian coords)
%added.
% Dec 11, 2002 - Added optional parameter OPTS.adjoint = 0 (default) or 1
%(adjoint),
%           allowing one to compute the modes of the adjoint system.
%           *NOTE* that for modes of the adjoint system, [Ex Ey] -> [Hy -Hx],
ie.
%           the output fields are different ones.
% Feb 23, 2003 - MOPTS changed to match new version of m2dpmloper, to pass
%           fieldmode/eigmode instead of fmode/emode.
% Jun  7, 2003 - Added Pr, Pz, Rmtx as optional output variables (for leaky mode
%           overlap integrals without adjoint).
%           - FIXED calculation of Ez from Ex and Ey to be properly
%           computed using Pr, Pz in the PML; also now works in
```

```
%           'w'-mode! The E-field should now be exactly correct. Still
%           need to fix H calculation, at least for 'w'-mode (check).
% Jun  9, 2003 - FIXED to pass OPTS not MOPTS to m2dpmloper so that BC's
%           get passed. This was fixed in the /workFeb16/ directory version of
%           m2wcyl, so that version and this one must be made consistent ASAP!!
% Jul 23, 2003 - ADDED ability to pass in a user-set "eigs" function in the
%           OPTS.eigsfcn variable.
% Jul 28, 2003 - *** MAJOR UPDATE & SYNCHRONIZATION BETWEEN
% MULTIPLE VERSIONS OF m2wcyl.m ***
%          --Inserted updates of other m2wcyl versions:--
%           **Jun  9, 2003 - quick fix: can now pass on BCs (done in other
%              versions of
%           m2wcyl better).
%           Jun 25, 2003 - FIXED calculation of Hx, Hy, Hz fields for beta-mode
%            for
%           cylindrical, leaky modes. (still need to do for
%           omega-modes).
%           ---------------------------------------------
%           - Renamed w to mu
%           - Cleaned up commented out lines
%           - **Changed input argument mu_guess from w-units to have
%            k0-units (w/c)
%           - **Changed wI to be <0 as it should be for loss!
%           - Verified and cleaned up output field calculations
%           - Fixed Omega_tilde to have negative sign (this isn't used yet though)
%           - Corrected H-field computation in 'w'-mode (the guess
%            frequency was being used!! must use computed complex frequency).
% Aug  1, 2003 - Corrected H-field computation for PMC boundary conditions.
%           Still have to check whether this works for cylindrical modes!
% Aug 11, 2003 - Fixed H-field computation to include PML factors (Pr, Pz).
%           It should now be exactly right everywhere (domain + PML).
% Oct 23, 2003 - Added option OPTS.sigma = [] to search for closest
%           eigenvalue (DEFAULT), or 'SR','SI','LR', ...
% Oct 27, 2003 - Added default setting of OPTS.BC to [0 0 0 0] in case it
%           is not set at input. This was done just for compatibility
%           with older script files.
% Nov 21, 2003 - Updates: Adding field capture for PMCh BCs (different size)
%

% Simulation section

function [mu, F, V, D, Pr, Pz, Rmtx] = m2wcyl(S, nu_index, mu_guess, OPTS,
nmodes, dPML, sigmaPML)
PEC = 0; PMCh = 1; PBC = 2; PMC = 3;                % [MP-21nov2003] Define
boundary condition identifiers
c = 299792458; u0 = 4e-7*pi; e0 = 1/c^2/u0;         % Physical Constants
```

```
global VMODE;  if isempty(VMODE) VMODE = 0; end        % [VMODE]
Default value for debug flag.
if ~isfield(OPTS,'adjoint') OPTS.adjoint = 0; end      % Default "adjoint-
computation" flag is FALSE (0).
if isempty(OPTS.adjoint) OPTS.adjoint = 0; end
if ~isfield(OPTS,'eigsfcn') OPTS.eigsfcn = 'eigs'; end  % Default sparse-matrix
eigenvalue solver function.
if isempty(OPTS.eigsfcn) OPTS.eigsfcn = 'eigs'; end
if ~isfield(OPTS,'sigma') OPTS.sigma = []; end         % Eigenvalue choice: shift-
invert = [], or 'LM','SI',etc
if isempty(OPTS.sigma) OPTS.sigma = 1; end             % Guess not needed for
direct modes.mu_guess = 1;
if ~isfield(OPTS,'BC') OPTS.BC = [0 0 0 0]; end        % Default boundary
conditions
if isempty(OPTS.BC) OPTS.BC = [0 0 0 0]; end
BCl = OPTS.BC(1); BCr = OPTS.BC(2); BCd = OPTS.BC(3); BCu =
OPTS.BC(4); % Macros [MP-21nov2003]

t0 = clock;                                    % Begin timing the code (for debug)

R = S.x; Z = S.y; nn = S.n;                % [MPREM] Import parameters for now...
L = nu_index; % l0 = mu_guess;    % [MPREM] [MP] removed Sep 22, 2002
sigmaRMAX = sigmaPML(1); sigmaZMAX = sigmaPML(2);

if VMODE > 1                                   % [VMODE] Plot refr. index distribution
  figure; imagesc(R, Z, (nn.' - min(nn(:))) * 1000); axis image;
  if (OPTS.coordmode == 'C') xlabel('x'); ylabel('y');
  elseif (OPTS.coordmode == 'R') xlabel('\rho'); ylabel('z'); end
  title('2D Index Profile'); filestampplot(gcf, mfilename, 'I'); % Label w/ filename
end

NR = (length(R)+1)/2; NZ = (length(Z)+1)/2;
if OPTS.eigmode == 'w'     % For 'w'-eigenvalue case...
disp('Warning: new version of modesolver uses mu_guess = k0 = w/c as
frequency guess value, NOT w as before\n.');
%   mu_guess = mu_guess/c;         % [MP] need to change the guess value later
to k0! (now it is w0)
  w0 = c*mu_guess;
else                    % For 'beta'-eigenvalue case...
  w0 = c*nu_index;         % [MP] Sep 20, 2002
end

% Generate PML matrices

[Pr, Pz, Rmtx] = m2dpmlmatx(w0, nn.^2, R, Z, [sigmaRMAX sigmaZMAX],
dPML);  % w0 is exact in 'b'-mode or the guess value in 'w'-mode
```

```
% Generate "vector-Helmholtz" operator matrix for 'w'- or 'b'-eigenvalue problem

dR = R(3) - R(1); dZ = Z(3) - Z(1);                % Grid spacing in R, Z is dR/2,
dZ/2!
if (OPTS.coordmode == 'C') Rmtx = ones(size(Rmtx)); end % [MP] Oct 01, 2002
- For Cartesian mode, set Rmtx=all 1's.
H = m2dpmloper(nn.^2, Pr, Pz, Rmtx, dR, dZ, L^2, OPTS); % Works for 'w'- and
'b'-mode operation
H = H / mu_guess^2;  % Normalize matrix for modal (k/k0)^2 as eigenvalue in
'w'-mode
pack;                                  % [MPREM] MEMORY Pack.

t1 = clock;

oxL = 1*(BCl == PMCh); oxR = 1*(BCr == PMCh); oxD = 0; oxU = 0; % [MP-
21nov2003] Index offsets for Ex field
oyL = 0; oyR = 0; oyD = 1*(BCd == PMCh); oyU = 1*(BCu == PMCh); % [MP-
21nov2003] Index offsets for Ey field
MxSIZE = (NR-1-(oxL+oxR))*(NZ-2-(oxD+oxU)); MySIZE = (NR-2-
(oyL+oyR))*(NZ-1-(oyD+oyU)); % Size of Ex and Ey parts of the solution vector
if OPTS.fieldmode(1) == 'M'                    % Reduce matrix to single
polarization!
  if OPTS.fieldmode(2) == 'X'                  % Semi-vectorial operator for Ex
modes
    H = H(1:MxSIZE,1:MxSIZE);
  elseif OPTS.fieldmode(2) == 'Y'              % Semi-vectorial operator for Ey
modes
    H = H(MxSIZE+(1:MySIZE),MxSIZE+(1:MySIZE));
  else
    error([mfilename ': For semi-vectorial calculations, solvertype must '...
        'be "MX" or "MY".']);
  end
end

if (OPTS.adjoint) H = H'; end;                 % For adjoint system computation,
take adjoint of operator.
asgn = (-1)^OPTS.adjoint;                      % Sign flag for normal (1) and
adjoint (-1) system.

% Solve eigenvalue problem by Arnoldi algorithm in shift-invert mode
OPTS.tol = eps;1e-10;
OPTS.disp = VMODE;
%[V,D] = eigs(H,nmodes,1,OPTS);                % normal Matlab solver
%[V,D] = feval(OPTS.eigsfcn, H, nmodes, 1, OPTS);    % general Matlab eigs
solver (allows user-set eigs function)
```

```
[V,D] = feval(OPTS.eigsfcn, H, nmodes, OPTS.sigma, OPTS);       % general
Matlab eigs solver (allows user-set eigs function)
%[V,D] = feval(OPTS.eigsfcn, H, nmodes, 'LR', OPTS);       % general Matlab
eigs solver (allows user-set eigs function)
pack;                                   % [MPREM]
mu = sqrt(diag(D)) * mu_guess;                  % mu eigenvalue = w/c ('w'-
mode) or gamma ('b'-mode)

% Sort solved modes by lowest imaginary part of propagation constant!
if (OPTS.eigmode == 'w')    % For 'w'-eigenvalue case...
%    X = sortrows([-imag(w)*asgn -real(w) V.']);  % [MPREM] -ve imaginary
part since exp(-i*w*t): w =def= wR - i wI  (1/tau =def= wI)
   X  = sortrows([-imag(mu)*asgn +real(mu) V.']);     % -ve imaginary part since
exp(-i*w*t): w =def= wR - i wI  (1/tau =def= wI)
        % Sort second by LOWEST frequency first.
%    mu = +X(:,2) + i*X(:,1)*asgn;  % [MPREM] swap columns wrt top part of
this "if"-statement.
   mu = +X(:,2) - i*X(:,1)*asgn;  % keeping wI < 0, swap columns wrt top part of
this "if"-statement.
else                    % ...and for beta-eigenvalue case.
   % If betas have imaginary parts, sort by lowest loss (highest in adjoint case)...
   % ... otherwise, sort by highest modal index (best confined mode first)
   X = sortrows([+imag(mu)*asgn -real(mu) V.']);      % +ve imaginary part since
exp(+i*beta*z): beta =def= bR + i bI  (alpha =def= bI)
   mu = -X(:,2) + i*X(:,1)*asgn;  % swap columns wrt top part of this "if"-
statement.
end
V = X(:,3:size(X,2)).';                         % [MP030728] Resort V,D raw
matrices to match above sorting.
D = diag( (mu/mu_guess).^2 );

t2 = clock;                                % End timing the eigenvalue solver
(ARPACK)
if VMODE ~= 0                                % Print elapsed time
   fprintf(['Timing of the code:\n' ...
         '-----------------------------------------\n']);
   fprintf('"Vector-Helmholtz" operator setup: %5.2f sec\n',etime(t1,t0));
   fprintf('ARPACK (double) eigenvalue solver: %5.2f sec\n',etime(t2,t1));
   fprintf('-----------------------------------------\n');
   fprintf('TOTAL:                    %5.2f sec\n',etime(t2,t0));
   if VMODE > 1
      figure; plot( real(sqrt(diag(D))) ); title('Normalized eigenvalue real parts');
      xlabel('Mode number'); ylabel('Re(\mu)');      % Plot real part of mu
(=neff*k0 in 'b'-mode case)
   end
end
```

```
% OUTPUT MODE FIELDS
if nargout > 1                          % Extracting mode patterns from
eigenvector
  NX = NR; NY = NZ;                     % [MPREM] [MP] temporary..
  F.Rr = R(2:2:2*NR-2); F.Zr = Z(3:2:2*NZ-3);
  F.Rz = R(3:2:2*NR-3); F.Zz = Z(2:2:2*NZ-2);

  er = nn.^2;                           % [MPREM]
  for k = 1:size(V,2)                   % Extract fields from eigenvectors ...
    if(OPTS.fieldmode == 'V')           % ... based on solver type.
      % [MP-21nov2003] Extract sizes according to boundary condition
      % type!
      Ex(:,:,k) = [zeros(oxL,NY-2); zeros(NX-1-(oxL+oxR),oxD), ...
                   reshape(V(1:MxSIZE,k),NX-1-(oxL+oxR),NY-2-(oxD+oxU)), ...
                   zeros(NX-1-(oxL+oxR),oxU); zeros(oxR,NY-2)];
      Ey(:,:,k) = [zeros(oyL,NY-1); zeros(NX-2-(oyL+oyR),oyD), ...
                   reshape(V(MxSIZE+1:MxSIZE+MySIZE,k),NX-2-
(oyL+oyR),NY-1-(oyD+oyU)), ...
                   zeros(NX-2-(oyL+oyR),oyU); zeros(oyR,NY-1)];
    elseif(OPTS.fieldmode == 'MX')
      Ex(:,:,k) = [zeros(oxL,NY-2); zeros(NX-1-(oxL+oxR),oxD), ...
                   reshape(V(1:MxSIZE,k),NX-1-(oxL+oxR),NY-2-(oxD+oxU)), ...
                   zeros(NX-1-(oxL+oxR),oxU); zeros(oxR,NY-2)];
      Ey(:,:,k) = zeros(NX-2,NY-1);
    elseif(OPTS.fieldmode == 'MY')
      Ex(:,:,k) = zeros(NX-1,NY-2);
      Ey(:,:,k) = [zeros(oyL,NY-1); zeros(NX-2-(oyL+oyR),oyD), ...
                   reshape(V(1:MySIZE,k),NX-2-(oyL+oyR),NY-1-(oyD+oyU)), ...
                   zeros(NX-2-(oyL+oyR),oyU); zeros(oyR,NY-1)];
    else
      error('m2dchew: solvertype invalid; must be "V", "MX" or "MY".');
    end

    % Set propagation constant along phi/"z" direction
    if (OPTS.eigmode == 'b')
      betaR(k) = mu(k); omega(k) = w0;
    else
      betaR(k) = nu_index; omega(k) = c*mu(k);    % [MP030728] Fixed field
derivation for 'w'-mode
    end
    % Derive Ez from Gauss' Law
    % (here imaginary unit 'i' uses the exp(-i w t), exp(+i beta z)
    % convention (physics convention). When EE j is used, it is
    % explicitly written as j, NEVER as i below.
    erxx = er(2:2:2*NX-2,3:2:2*NY-3); eryy = er(3:2:2*NX-3,2:2:2*NY-2);
```

```
    erzz = er(3:2:2*NX-3,3:2:2*NY-3);
    rxx = Rmtx(2:2:2*NX-2,3:2:2*NY-3); ryx = Rmtx(3:2:2*NX-3,3:2:2*NY-
3);
    Ax = rxx .* (erxx).*[Ex(:,:,k)]; Ax = Pr(3:2:2*NX-3,3:2:2*NY-3) .*
(Ax(2:NX-1,:) - Ax(1:NX-2,:))/dR;  % d/dx exx Ex
    Ay = (eryy).*[Ey(:,:,k)]; Ay = Pz(3:2:2*NX-3,3:2:2*NY-3) .* ryx .*
(Ay(:,2:NY-1) - Ay(:,1:NY-2))/dZ;  % d/dy eyy Ey
    deltaphi = 0; Gammah(k) = betaR(k) * exp(-i*deltaphi);  % Define delta-phi
and Gamma-hat-prime; [MP030728] Verified eqn
    warning off MATLAB:divideByZero                    % [MP] Added July 26,
2003
    if( Gammah(k) == 0 ) disp('Warning: Ez improper as betaR = 0; Ez should
be =def= 0 here.'); end % [MP030728]
    Ez(:,:,k) = i./(Gammah(k)*erzz) .* (Ax + Ay);

% [MP020728] Verified eqn warning on MATLAB: divideByZero clear erxx
eryy erzz;                    % [MP030728] Added for memory conservation

% Derive H fields from Faraday's Law  ([MP030728] eqns verified again)

    if(OPTS.adjoint) disp('Warning: computation of other 4 field components
not supported in "adjoint" mode.'); end;  % [MP] Jul 15, 2004
    deltat = 0; Omegat(k) = omega(k) * exp(-i*deltat);    % Defining delta_t and
Omega_tilde, CHANGED SIGN [MP030728]
    C = -i/(Omegat(k) * u0);
    Gammat(k) = betaR(k) * exp(+i*deltaphi);       % Define delta-phi and
Gamma-tilde, [MP030728]
    ryy = Rmtx(3:2:2*NX-3,2:2:2*NY-2); rzz = Rmtx(3:2:2*NX-3,3:2:2*NY-
3);
%     Hx(:,:,k) = C * (i*Gammat(k).*Ey(:,:,k)./ryy - ...
%             ([Ez(:,:,k) zeros(NX-2,1)] - [zeros(NX-2,1) Ez(:,:,k)])/dZ );
%     Hz(:,:,k) = C * (([Ex(:,:,k) zeros(NX-1,1)] - [zeros(NX-1,1) Ex(:,:,k)])/dZ -
...
%             ([Ey(:,:,k); zeros(1,NY-1)] - [zeros(1,NY-1); Ey(:,:,k)])/dR);
%     Hy(:,:,k) = C * (1./rxx .* ...
%             ([rzz .* Ez(:,:,k); zeros(1,NY-2)] - [zeros(1,NY-2); rzz .*
Ez(:,:,k)])/dR - ...
%             i * Gammat(k) * Ex(:,:,k)./rxx);
%     Taking care of BCs... Recall: PEC = 0; PMC = 1; % IF MORE BCS ARE
%     TO BE ADDED, MUST CHANGE LINES BELOW TO COMPUTE
%       SEPARATELY BASED ON WHICH BC IS ACTIVE...
%     Hx(:,:,k) = C * (i*Gammat(k).*Ey(:,:,k)./ryy - ...
%             ([Ez(:,:,k) Ez(:,NY-2,k)*OPTS.BC(4)] - [Ez(:,1,k)*OPTS.BC(3)
Ez(:,:,k)])/dZ );
%     Hz(:,:,k) = C * (([Ex(:,:,k) Ex(:,NY-2,k)*OPTS.BC(4)] -
[Ex(:,1,k)*OPTS.BC(3) Ex(:,:,k)])/dZ - ...
```

```
%               ([Ey(:,:,k); Ey(NX-2,:,k)*OPTS.BC(2)] - [Ey(1,:,k)*OPTS.BC(1);
Ey(:,:,k)])/dR);
%       Hy(:,:,k) = C * (1./rxx .* ...
%               ([rzz .* Ez(:,:,k); rzz(NX-2,:) .* Ez(NX-2,:,k) * OPTS.BC(2)] - ...
%                [rzz(1,:) .* Ez(1,:,k) * OPTS.BC(1); rzz .* Ez(:,:,k)])/dR - ...
%               i * Gammat(k) * Ex(:,:,k)./rxx);
      Hx(:,:,k) = C * (i*Gammat(k).*Ey(:,:,k)./ryy - ...
            Pz(3:2:2*NX-3,2:2:2*NY-2) .* ([Ez(:,:,k) Ez(:,NY-
2,k)*OPTS.BC(4)] - [Ez(:,1,k)*OPTS.BC(3) Ez(:,:,k)])/dZ );
      Hz(:,:,k) = C * (Pz(2:2:2*NX-2,2:2:2*NY-2) .* ([Ex(:,:,k) Ex(:,NY-
2,k)*OPTS.BC(4)] - [Ex(:,1,k)*OPTS.BC(3) Ex(:,:,k)])/dZ - ...
            Pr(2:2:2*NX-2,2:2:2*NY-2) .* ([Ey(:,:,k); Ey(NX-
2,:,k)*OPTS.BC(2)] - [Ey(1,:,k)*OPTS.BC(1); Ey(:,:,k)])/dR);
      Hy(:,:,k) = C * (1./rxx .* ...
            Pr(2:2:2*NX-2,3:2:2*NY-3) .* ([rzz .* Ez(:,:,k); rzz(NX-2,:) .*
Ez(NX-2,:,k) * OPTS.BC(2)] - ...
             [rzz(1,:) .* Ez(1,:,k) * OPTS.BC(1); rzz .* Ez(:,:,k)])/dR - ...
            i * Gammat(k) * Ex(:,:,k)./rxx);

      if( VMODE > 1 )   % For guided modes, Ex/Ey=real, Ez=imag (90° out of
phase!).
         V1=Ex(:,:,k); i1=find(abs(V1) == max(abs(V1(:)))); A1 = V1(i1(1));
         figure; imagesc(F.Rr, F.Zr, real(Ex(:,:,k).'/A1)); axis image; % E^X
         title(strcat('E^X (Mode ',num2str(k),')')); xlabel('x'); ylabel('y');

         V1=Ey(:,:,k); i1=find(abs(V1) == max(abs(V1(:)))); A1 = V1(i1(1));
         figure; imagesc(F.Rz, F.Zz, real(Ey(:,:,k).'/A1)); axis image; % E^Y
         title(strcat('E^Y (Mode ',num2str(k),')')); xlabel('x'); ylabel('y');

         V1=Ez(:,:,k); i1=find(abs(V1) == max(abs(V1(:)))); A1 = V1(i1(1));
         figure; imagesc(F.Rz, F.Zz, real(Ez(:,:,k).'/A1)); axis image; % E^Z
         title(strcat('E^Z (Mode ',num2str(k),')')); xlabel('x'); ylabel('y');
         clear V1 i1;        % [MP030728] Added for memory conservation
      end
   end
end

% Display elapsed time
if( VMODE ~= 0 )  fprintf('Elapsed time: %6.2f sec\n', etime(clock,t0));  end

% mu already defined; putting fields into data structure F
F.Ex = Ex; F.Ey = Ey; F.Ez = Ez; F.Hx = Hx; F.Hy = Hy; F.Hz = Hz;
%---------.---------.---------.---------.---------.---------.---------.--------|
```

References

[1] F. Coppinger, A. S. Bhushan, and B. Jalali, "Photonic time stretch and its application to analog-to-digital conversion," IEEE. Transactions of Microwave Theory and Technology, Vol 47 #7, pp.1309 (1999).

[2] F. X. Kärtner, S. Akiyama, G. Barbastathis, T. Barwicz, H. Byun, D. T. Danielson, F. Gan, F. Grawert, C. W. Holzwarth, J. L. Hoyt, E. P. Ippen, M. Kim, L. C. Kimerling, J. Liu, J. Michel, O. O. Olubuyide, J. S. Orcutt, M. Park, M. Perrott, M. A. Popović, P. T. Rackich, R. J. Ram, H. I. Smith, and M. R. Watts, "Electronic Photonic Integrated Circuits for High Speed, High Resolution, Analog to Digital Conversion," Proceedings of SPIE, 6125 (03), (2006).

[3] P.W. Juodawlkis, J. C. Twichell, G. E. Betts, J. J. Hargreaves, R. D. Younger, J. L. Wasserman, F. J. O'Donnell, K. G. Ray, and R. C. Williamson, "Optically sampled analog-to-digital converters," IEEE Transactions of Microwave Theory and Technology, Vol. 49 #10, pp. 1840, (2001).

[4] T. R. Clark, J. U. Kang, and R. D. Esman, "Performance of a time- and wavelength-interleaved photonic sampler for analog-digital conversion," IEEE Photonics Technology Letters Vol. 11 #9, pp. 1168, (1999).

[5] J. A. Bell, M. C. Hamilton, D. A. Leep, H. F. Taylor, and Y. –H. Lee, "Optical sampling and demultiplexing applied to A/D conversion," Devices for Optical Processing, 1562, pp. 276, (1991).

[6] M. Y. Frankel, J. U. Kang, and R. D. Esman, "High-performance photonic analogue-to-digital converter," Electronic Letters Vol. 33 #25, pp. 2096, (1997).

[7] C. Gunn, "10 Gb/s CMOS Photonics Technology," Proceedings of SPIE, Vol. 6125, pp. 612501, (2006).

[8] L. Colace, G. Masini, F. Galluzzi, G. Assanto, G. Capellini, L. Di Gaspare, E. Palange, and F. Evangelisti, "Metal–semiconductor–metal near-infrared light detector based on epitaxial Ge/Si," Applied Physics Letters, Vol. 72, #24, pp. 3175 (1998).

[9] M. Jutzi, M. Berroth, G. Wöhl, M. Oehme, and E. Kasper, "Ge-on-Si Vertical Incidence Photodiodes with 39-GHz Bandwidth," IEEE Photonics Technology Letters, Vol. 17, #7, pp. 1510, (2005).

[10] M. Salib, L. Liao, R. Jones, M. Morse, A. Liu, D. Damara-Rubio, D. Alduino, M. Paniccia, "Silicon Photonics," Intel Technology Journal, Vol. 8, #2, pp. 143, (2004).

[11] Chuang, Shun Lien. Physics of Optoelectronic Devices. New York: John Wiley & Sons, Inc., 1995.

[12] T P. Pearsall and M.A. Pollack, "Compound semiconductor photodiodes," in Semiconductors and semimetals, R.K. Williardson and A.C. Beer, Eds., Vol. 22, Lightwave communications technology, Part D, Photodetectors, W.T. Tsang, Vol. Ed. New York: Academic, pp. 173, (1985).

[13] Y. Murakami and T. Shingyouji, "Separation and analysis of diffusion and generation components of pn junction current in various silicon wafers," Journal of Applied Physics Vol. 75, #7, pp. 3548 (1994).

[14] D. Braun, "Electronic Injection and Conduction Processes for Polymer Devices," Journal of Polymer Science: Part B: Polymer Physics, Vol. 41, pp. 2622, (2003).

[15] M. Takayanagi and S. Iwabuchi., "Theory of band-to-band tunneling under nonuniform electric fields for subbreakdown leakage currents," IEEE Transactions on Electron Devices, Vol. 38, #6, pp. 1425, (1991).

[16] M. B. Das, "Optoelectronic Detectors and Receivers: Speed and Sensitivity Limits," pp. 15, (1999).

[17] K.P. Roenker and P. Mushini, "Dynamic formation of a parasitic barrier to electron flow in SiGe HBTs operating at high current densities", Microelectronics Journal, Vol. 31, #5, pp. 353 (2000).

[18] J.C. Bean, "Silicon-Based Semiconductor Heterostructures", Chapter 11, in "Silicon-Molecular Beam Epitaxy, Volume II", edited by Kasper and Bean, CRC Press, pp. 93 (1988).

[19] S.R. Forrest, "Sensitivity of avalanche photodetector receivers for high-bit-rate long-wavelength optical communication systems," in Semiconductors and semimetals, R.K. Williardson and A.C. Beers, Eds., Vol 22, Lightwave communication technology, Part D, Photodetectors, W.T. Tsang, Vol. Ed. New York: Academic, pp. 329, (1985).

[20] G. Masini, L. Colace, and G. Assanto, "2.5 Gbits/s polycrystalline germanium-on silicon photodetector operating from 1.3 to 1.55 μm", Applied Physics Letters, Vol 82, #15, pp. 2524, (2003).

[21] S. B. Samavedam, M. T. Currie, T. A. Langdo, and E. A. Fitzgerald, "High-quality germanium photodiodes integrated on silicon substrates using optimized relaxed graded buffers," Applied Physics Letters, Vol. 73, #15, pp. 2125 (1998)

[22] G. Masini, L. Colace, F. Petulla, G. Assanto, V Cencelli, and F. DeNotaristefani, "Monolithic and hybrid near infared detection and imaging based on poly-Ge photodiode arrays", Optical Materials, Vol. 27 pp. 1079, (2005).

[23] Y.-H. Xie, E.A. Fitzgerald, P.J. Silverman, A.R. Kortan, and B.E. Weir, "Fabrication of Relaxed GeSi Buffer Layers on Si(100) with Low Threading Dislocation Density," Materials Science and Engineering B, #14, pp. 332, (2004)

[24] J.L. Liu, S. Tong, Y.H. Luo, J. Wan, and K.L. Wang, "High-quality Ge films on Si substrates using Sb surfactant-mediated graded SiGe buffers", Applied Physics Letters, Vol. 79, #21, pp. 3431 (2001).

[25] H.-C Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling, "High-quality Ge epilayers on Si with low threading-dislocation densities," Vol. 75, #19, pp. 2909, (1999).

[26] J. Liu, J. Michel, W. Giziewicz, D. Pan, K. Wada, D. D. Cannon, S. Jongthammanurak, D. T. Danielson, L. C. Kimerling, J. Chen, F. Ö. Ilday, F. X. Kärtner, and J. Yasaitis, "High-performance, tensile-strained Ge *p-i-n* photodetectors on a Si platform," Applied Physics Letters Vol. 87, pp. 103501 (2005).

[27] P.D. Agnello, T.O. Sedgwick, M.S. Goorsky, J. Ott,; T.S. Kuan, and G. Scilla, "Selective growth of silicon-germanium alloys by atmospheric-pressure chemical vapor deposition at low temperatures" Applied Physics Letters, Vol. 59, #12, pp. 1479, (1991).

[28] J. Liu, J. Michel, D.D. Cannon, W. Giziewicz, D. Pan, D.T. Danielson, S. Jongthammanurak, J.Yasaitis, K. Wada, C.G. Fonstad, and L.C. Kimerling, "High Speed Ge Photodetectors on Si Platform for GHz Optical Communications in C+L Bands", Material Research Society Symposium Precedings, Vol. 829, B6.9.1, (2005).

[29] F. Kärtner, "MIT Gigahertz High-resolution Optical Sampling Technology (GHOST)," Cambridge, MA: Massachusetts Institute of Technology, (2004)

[30] Einarsson, Goran. Principles of Lightwave Communications, John Wiley & Sons, Inc, 1995.

[31] Arya, Vivek. Analysis, Design, and Performance Evaluation of Optical Fiber Spectrum-Sliced WDM Systems. Department of Electrical Engineering, Blacksburg, VA: Virginia Polytechnic Institute and State University, (1997).

[32] http://www.ioffe.rssi.ru/SVA/NSM/Semicond/Ge/electric.html: New Semiconductor Archive of Material Parameters at the Ioffe Physico-Technical Institute.

[33] H.-C. Luan, "Ge Photodetectors for Si Microphotonics", in Department of Material Science and Engineering. Cambridge, MA: Massachusetts Institute of Technology, (2001).

[34] E. Mateeva, P. Sutter, J.C. Bean, M. G. Lagally, "Mechanism of organization of three-dimensional islands in SiGe/Si multilayers," Applied Physics Letters, Vol. 71, #22, pp. 3233 (1997)

[35] J.M. Hartmann, A.M. Papon, P. Holliger, G. Rolland, T. Billon, M. Rouvière, L. Vivien, and S. Laval, MRS Symposium Proceedings B4.3, Vol. 809 (2004)

[36] M. Halbwax, D. Bouchier, V. Yam, D. Debarre, and L.H. Nguyen, "Kinetics of Ge growth at low temperature on Si(001) by ultrahigh vacuum chemical vapor deposition", Journal of Applied Physics, Vol. 97, p. 064907-1 (2005).

[37] A. Sakai and T. Tatsumi, Applied Physics Letters, Vol. 64, #52 (1994).

[38] S. J. Kahang, J.Y. Park, K.H. Booth, J. Lee, Y. Khang, and Y. Kuk, Journalof Vacuum Science Technology, Vol 15, pp. 927, (1997).

[39] D. Dentel, J.L. Bischoff, T. Angot, and L. Kubler, Surface Science, Vol. 211, pp. 402, (1998).

[40] Meekyung Kim private communication

[41] M. Halbwax, D. Bouchier, V. Yam, D. Debarre, Lam H. Nguyen, Y. Zheng, P. Rosner, M. Benamara, H.P. Strunk, C. Clerc, Journal of Applied Physics, Vol. 97, 064907 (2005)

[42] F. Liu, F. Wu, M. G. Lagally, "Effect of Strain on Structure and Morphology of Ultrathin Ge Films on Si (001)," Chemical Reviews, Vol. 97, pp. 1045, (1997).

[43] H. Holloway, and S. L. McCarthy Journal of Applied Physics, Vol. 73, #1 pp. 103, (1993).

[44] B. Tillack, P. Zaumseil, G. Morgenstern, D. Kruger, and G. Ritter, Applied Physics Letters, Vol. 67, #8, pp. 1143, (1995).

[45] D. K. Bowen, N. Loxley, B.K. Tanner, L. Cooke and M. A. Capano, Proceedings of Material Research Society, Vol. 208, pp. 113 (1991).

[46] J.M. Hartmann, J.-F. Damlencourt, Y. Bogumilowicz, P. Hollinger, G. Rolland, and T. Billon, "Reduced pressure-chemical vapor deposition of intrinsic and doped Ge layers on Si(001) for microelectronics and optoelectronics purposes", Journal of Crystal Growth, Vol. 274, pp. 90, (2005).

[47] J.M. Hartmann, V. Loup, G. Rolland, P. Hollinger, F. Laugier, C. Vannuffel, and M.N. Semeria, Journal of Crystal Growth, Vol. 236, pp. 10, (2002).

[48] J.M. Hartmann, L. Clavelier, C. Jahan, P. Hollinger, G. Rolland, T. Billon, and C. Defranoux, Journal of Crystal Growth, Vol. 264, pp. 36, (2004).

[49] J.M. Hartmann, A. Abbadie, A.M. Papon, P. Holliger, G. Rolland, T. Billon, J.M. Fedeli, M. Rouviere, L. Vivien, and S. Laval, Journal of Applied Physics, Vol. 95, #10 (2004).

[50] C. Ratsch and J.A. Venables, Journal of Vacuum Science and Technology A - Vacuum Surfaces and Films 21 (2003) 96.

[51] J.M. Hartmann, Y. Bogumilowicz, F. Andrieu, P. Holliger, G. Rolland, and T. Billon, "Reduced pressure-chemical vapor deposition of high Ge content $Si_{1-x}Ge_x$ and high C content $Si_{1-y}C_y$ layers for advanced metal oxide semiconductor transistors", Journal of Crystal Growth, Vol. 277, #1-4 pp. 114 (2005).

[52] C.O. Chui, F. Ito, and K.C. Saraswat, "Nanoscale Germanium MOS Dielectrics-Part I: Germanium Oxynitrides", IEEE Transactions on Electron Devices, Vol. 53, #7 pp. 1501 (2006).

[53] G.G. Fountain, R.A. Rudder, S.V. Hattangady, D.J. Vitkavage, R.J. Markunas, "Electrical and microstructural characterisation of an ultrathin silicon interlayer used in a silicon dioxide/germanium-based mis structure", Electronics Letters, Vol 24, #16, pp. 1010 (1988).

[54] T. Yashiro, "Determination of Trap Levels in Ge_3N_4 and Barrier Energies at the Ge3N4-Ge Interface by C-V Characteristics", Japanese Journal of Applied Physics, Vol. 10, #12 pp. 1691, (1971).

[55] O.J. Gregory, L.A. Pruitt, E.E. Crisman, C. Roberts, P.J. Stiles, "Native Oxides Formed on Single-Crystal Germanium by Wet Chemical Reactions", Journal of the Electrochemical Society (Solid-State Science and Technology), pp. 923, (1988).

[56] D.J. Hynes and J.J. Rosenberg, "Growth and Materials Characterization of Native Germanium Oxynitride Thin Films on Germanium", Journal of Electrochemical Society: Solid-State Science and Technology, Vol. 135, #4, pp.961, (1988).

[57] J. J. Rosenberg and S. C. Martin, "Self-Aligned Germanium MOSFET's Using a Nitrided Native Oxide Gate Insulator," IEEE Electron Device Letters, Vol. 9, #12, pp. 639, (1988)

[58] Schroder, Dieter K. Semiconductor Material and Device Characterization 3rd edition, John Wiley & Sons, Wiley Interscience, Inc., Hoboken, New Jersey, 2006.

[59] Handbook of Optical Constants of Solids, edited by Edward D. Palik, Academic Press, NY, 1985.

[60] D. D. Cannon, "Strain-engineered CMOS-compatible Ge Photodetectors" in Department of Material Science and Engineering. Cambridge, MA: Massachusetts Institute of Technology, (2001).

[61] C. Werkhoven, C. Arena, M. Bauer, P. Brabant, M. Meurls, T. Valentina, and L. Sourlau, "Ge epitaxy on Si: an enabling high-performance CMOS platform", Semiconductor International, Vol. 29, #11, pp. 67, (2006).

[62] G. Eneman, P. Verheyen, R. Rooyackers, F. Nouri, L. Washington, R. Schreutelkamp, V. Moroz, L. Smith, An De Keersgieter; M. Jurczak, and Kristin De Meyer, "Scalability of the $Si_{1-x}Ge_x$ source/drain technology for the 45-nm technology node and beyond," IEEE Transactions on Electron Devices, Vol. 53, #7, pp. 1647 (2006).

[63] H.-R. Muller, J. Kirchhof, V. Reichel, and S. Unger, "Low loss silica fiber optics: Fibers for high-power lasers and amplifiers," Academie des Sciences. Comptes Rendus, Physique, Vol. 7, #2, pp. 154, (2006).

[64] J. D. B. Bradley, P.E. Jessop, and A.P. Knights, "Requirements for photodetectors: Infra-red photo-detectors monolithically integrated with silicon-based photonic circuits," Materials, Integration and Technology for Monolithic Instruments (Materials Research Society Symposium Proceedings), Vol. 869, pp. 65, (2005).

[65] A. Ruzin and S. Marunko, "Current mechanisms in silicon PIN structures processed with various technologies", Nuclear Instruments & Methods in Physics Research, Section A (Accelerators, Spectrometers, Detectors and Associated Equipment), Vol. 492, #3, pp. 411 (2002).

[66] G.A. Davis, R.E. Weiss, R.A. LaRue, K.J. Williams, R.D. Esman, "A 920-1650-nm high-current photodetector", IEEE Photonics Technology Letters, Vol. 8, #10, pp. 1373, (1996).

[67] J.P. McVittie, "Plasma charging damage: An overview," Proc. 1st International Symposium Plasma Process Induced Damage, pp. 7 (1996).

[68] T. Kobayashi, S. Iijima, and A. Hiraiwa, "P-type polysilicon processing temperature reduction using in situ boron-doped amorphous silicon", Japanese Journal of Applied Physics, Part 2 (Letters), Vol. 32, # 5A, pp. L638 (1993).

[69] M. Nowakowski, J. Bandaru, L.D. Bell, and S. Nikzad, "Preparation of Ge (100) substrates for high-quality epitaxial growth of group IV materials", Self-Organized Processes in Semiconductor Heteroepitaxy Symposium (MRS Symposium Proceedings), Vol.794, pp. 71, (2004).

[70] M.S. Carroll, Y.S. Suh, and R. Levy, "Suppressed boron diffusion in bulk silicon below strained (100) $Si_{1-x}Ge_x$ surfaces during nitrogen annealing," 207th Meeting of the Electrochemical Society - Meeting Abstracts, pp. 675 (2005).

[71] W.P. Bai, N. Lu, and D. –L Kwong, "Si interlayer passivation on germanium MOS capacitors with high-K dielectric and metal gate", IEEE Electron Device Letters, Vol. 26, #6, pp. 378, (2005).

[72] Roger T., and Sodini, Charles G., Microelectronics: An Integrated Approach, Prentice Hall Electronic and VLSI Series, Upper Saddle River, New Jersey, 07458, 1997.

[73] G.C. Chi, J.K. Sheu, M.L. Lee, C.J. Kao, Y.K. Su, S.J. Chang, and W.C Lai, "Reduction of dark current in AlGaN/GaN Schottky barrier photodetectors with a low-temperature-grown GaN cap layer," Materials Research Society Symposium – Proceedings: GaN and Related Alloys, Vol. 798, pp. 353, (2003).

[74] E.A. Kraut, "The effect of valence-band offset on potential and current distributions in HgCdTe heterostructures", Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films), Vol. 7, #2, pp. 420, (1989).

[75] R. Rheinlander, G. Grummt, J. Kovac, H. Haefner, and R. Heilmann, "Minority-carrier generation and recombination in 1.35 μm InGaAsP/InP double heterostructures diodes," Physica Status Solidi (A) Applied Research, Vol. 107, #1, pp. 405, (1988).

[76] L.Yan, S.H. Olsen, M. Kanoun, R. Agaiby, A.G. O'Neill, "Gate leakage mechanisms in strained Si devices", Journal of Applied Physics, Vol. 100, #10, pp. 104507 (2006).

[77] G. Khanduri and B. Panwar, "A study of the effects of the base doping profile on SiGe heterojunction bipolar transistor performance for all levels of injection", Semiconductor Science and Technology, Vol. 21, # 4, pp. 486, (2006).

[78] M. Carroll and R. Koudelka, "Accurate modelling of average phosphorus diffusivities in germanium after long thermal anneals", 2006 International SiGe Technology and Device Meeting, pp. 20, (2006).

[79] R. Bashir, T. Su, J.M. Sherman, G.W. Neudeck, J. Denton, and A. Obeidat, "Reduction of sidewall defect induced leakage currents by the use of nitrided field oxides in silicon selective epitaxial growth isolation for advanced ultralarge scale integration", Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures), Vol. 18, #2, pp. 695, (2000).

[80] V.P. Markevich, A.R. Peaker, V.V. Litvinov, L.I. Murin, and N.V. Abrosimov, "Electric field enhancement of electron emission from deep level traps in Ge crystals", Physica B: Condensed Matter (Proceedings of the 23rd International Conference on Defects in Semiconductors), Vol. 376-377, #1, pp. 200 (2006).

[81] E. Rosencher, V. Mosser, G. Vincent, "Transient-current study of field-assisted emission from shallow levels in silicon," Physical Review B, Vol. 29, #3, pp. 1135, (1984).

[82] H.C. De Graaf, M. Huybers, and J.G. De Groot, "Grain boundary states and the characteristics of lateral polysilicon diodes", Solid State Electronics, Vol. 25, #1, pp. 67, (1982).

[83] L. Colalongo, M. Valdinoci, and G. Baccarani, "Investigation on Anomalous Leakage Currents in Poly-TFT's Including Dynamic Effects," IEEE Transactions on Electron Devices, Vol. 44, #11, pp. 2106, (1997).

[84] H. Zhang, E. J. Miller, and E. T. Yu, "Analysis of leakage current mechanism in Schottky contacts on GaN and $Al_{0.25}Ga_{0.75}N$/GaN grown by

molecular-beam epitaxy," Journal of Applied Physics, Vol. 99, pp. 023703-1, (2006).

[85] P. Pipinys, A. Rimeika, and A. Pipiniene, "Analysis of reverse current-voltage characteristics of Schottky diodes based on phonon-assisted tunneling including Frenkel emission mechanism", Solid State Electronics, Vol. 46, #9, pp. 1283 (2000).

[86] E.J. Miller, E.T. Yu, P. Waltereit, and J.S. Speck, "Analysis of reverse-bias leakage current mechanisms in GaN grown by molecular-beam epitaxy", Applied Physics Letters, Vol 84, #4, pp. 535 (2004).

[87] Medici User Guide, Version V-2003.12, Synopsys, Inc. (2003)

[88] P. Pipinys and V. Lapeika, Journal of Applied Physics, Vol. 99, #9, pp. 93709-1 (2006)

[89] L. C. Kimerling, J. R. Patel, J. L. Benton, and P. E. Freeland, Institute of Physics Conference Series, Vol. 59, pp. 401 (1981).

[90] J. R. Patel, and L. C. Kimerling, Crystal Research and Technology, Vol. 16, pp. 187, (1981)

[91] E. Gaubas, and J. Vanhellemont, "Dependence of carrier lifetime in germanium on resistivity and carrier injection level," Applied Physics Letters, Vol. 89, pp. 142106-1, (2006).

[92] S. Wolf and R. Tauber, "Silicon Processing for the VLSI Era (Volume 1 – Process Technology)," Lattice Press, (1986).

[93] "Epi Centura Process Manual," Applied Materials, Inc., (1995).

[94] A. Gower-Hall, "Integrated Model-Based Run-to-Run Uniformity Control for Epitaxial Silicon Deposition," in Department of Electrical Engineering and Computer Science. Cambridge, MA: Massachusetts Institute of Technology, (2001).

[95] C. T. Sah, W.W. Chan, H. S. Fu, and J.W. Walker, "Thermally Stimulated Capacitance (TSCAP) in p-n Junctions," Applied Physics Letters, Vol. 20, #5, (1972).

[96] D. Miller, "Rationale and Challenges for Optical Interconnects to Electronic Chips," Proceedings of the IEEE, Vol. 88, pp. 728, (2000).

[97] L. Lai, and E.A. Irene, "Limiting Si/SiO_2 interface roughness resulting from thermal oxidation," Journal of Applied Physics, Vol. 86, pp. 1729, (1999).

[98] I. Day, I. Evans, A. Knights, F. Hopper, S. Roberts, J. Johnston, S. Day, J. Luff, H. Tsang, and M. Asghari, "Tapered Silicon Waveguides for Low Insertion Loss Highly-Efficient High-Speed Electronic Variable Optical Attenuators," OFC, pp. 249, (2003).

[99] C. Manolatou, H. Haus, IEEE Digest of the LEOS Summer Topical Meetings pp. 31 (2001).

[100] I. Moerman, P. P. Van Daele, and P. M. Demeester, IEEE Journal Selected Topics in Quantum Electronics, Vol. 6, pp. 1308, (1997).

[101] V.R. Almeida, R. R. Panepucci, and M. Lipson, "Nanotaper for compact mode conversion," Optics Letters, Vol. 28, pp. 1302, (2003).

[102] K. K. Lee, D. R. Lim, H. Luan, A. Agarwal, J. Foresi, and L. C. Kimerling, "Effect of size and roughness on light transmission in a Si/SiO_2 waveguide: Experiments and model," Applied Physics Letters, Vol. 77, pp. 1617, (2000).

[103] K. K. Lee, D. R. Lim, and L. C. Kimerling, "Fabrication of ultralow-loss Si/SiO_2 waveguides by roughness reduction," Optics Letters, Vol. 26, pp. 1888, (2001).

[104] S. Lardenois, D. Pascal, L. Vivien, E. Cassan, S. Laval, R. Orobtchouk, M. Heitzmann, N. Bouzaida, and L. Mollard, "Low-loss submicrometer silicon on insulator rib waveguides and corner mirrors," Optics Letters, Vol. 28, pp. 1150, (2003).

[105] Y. A. Vlasov, and S. J. McNab, "Losses in single-mode silicon-on-insulator strip waveguides and bends," Optics Express, Vol. 12, pp. 1622, (2004).

[106] R. M. de Ridder, K. Worhoff, A. Driessen, P. V. Lambeck, and H. Albers, "Silicon Oxynitride Planar Waveguiding Structures for Application in Optical Communication," IEEE Journal of Selected Topics in Quantum Electronics, Vol. 4, pp. 930, (1998).

[107] N. Daldosso, M. Melchiorri, F. Riboli, M. Girardini, G. Pucker, M. Crivellari, P. Bellutti, A. Lui, and L. Pavesi, "Comparison Among Various Si_3N_4 Waveguide Geometries Grown Within a CMOS Fabrication Pilot Line," Journal of Lightwave Technology, Vol. 22, pp. 1734, (2004).

[108] D. A. P. Bulla, W. Li, C. Charles, R. Boswell, A. Ankiewicz, and J. D. Love, "Low-loss Silica-Based Optical Film Waveguides Deposited by Helicon-Activated Reactive Evaporation," Journal of Lightwave Technology, Vol. 23, pp. 1302, (2005).

[109] E. Brab, U. Hilleringmann, and K. Schumacher, "System Integration of Optical Devices and Analog CMOS Amplifiers," IEEE Journal of Solid-State Circuits, Vol. 29, pp. 1006, (1994).

[110] K. Misiakos, E. Tsoi, E. Halmagean, and S. Kakabakos, "Monolithic Integration of Light Emitting Diodes, Detectors, and Optical fibers on a silicon wafer: A CMOS compatible optical sensor," IEDM, pp. 25, (1998).

[111] L. Pavesi, "Will silicon be the photonic material of the third millennium?," Journal of Physics: Condensed Matter, Vol. 15, pp. 1169, (2003).

[112] G. Masini, V. Cencelli, L. Colace, F. de Notaristefani, and G. Assanto, "Linear Array of Si-Ge Heterojunction Photodetectors Monolithically Integrated with Silicon CMOS Readout Electronics," IEEE Journal of Selected Topics in Quantum Electronics, Vol. 10, pp 811, (2004).

[113] A. Splett, T. Zinke, K. Petermann, E. Kasper, H. Kibbel, H.-J. Herzog, and H. Presting, "Integration of Waveguides and Photodetectors in SiGe for 1.3 μm Operation," IEEE Photonics Technology Letters, Vol. 6, pp. 59, (1994).

[114] R. Baets, W. Bogaerts, P. Dumon, G. Roelkens, I. Christiaens, K. De Mesel, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman, D. Van Thourhout, V. Wiaux, J. Wouters, and S. Beckx, "Integration of Photonic Functions in and with Silicon," IEEE, pp. 57, (2004)

[115] A. Yamada, M. Sakuraba, J. Murota, K. Wada, and L. C. Kimerling, "Propagation Characteristics of Si Nitride Optical Waveguide Integrated with Si p-i-n Diodes for Light Emitter and Detector," IEEE Conference on Group IV Photonics, pp.142, (2004).

[116] B. R. Murthy, M. T. Doan, and D. R. Lim, "Si_3N_4 Film Etching to Form Fine Tapered Structures for Photonics Applications," IEEE Conference on Group IV Photonics, pp.101, (2004).

[117] K. Kapser, C. Wagner, and P. P. Deimel, "Rapid Deposition of High-Quality Silicon-Oxinitride Waveguides," IEEE Transactions Photonics Technology Letters, Vol. 3, pp. 1096, (1991).

[118] A. Splett, K. Petermann, "Low Loss Single-Mode Optical Waveguides with Large Cross-Section in Standard Epitaxial Silicon," IEEE Photonics Technology Letters, Vol. 6, pp. 425, (1994).

[119] S. Janz, A. Delage, A. Bogdanov, D. Dalacu, B. Lamontagne, and D.-X. Xu, "Graded index waveguide couplers for silicon-based microphotonics," IEEE Conference on Group IV Photonics, pp.148, (2004).

[120] L. Wosinski, "Silica-on-Silicon Technology for Photonic Integrated Devices," ICTON, pp. 274, (2004).

[121] B. Jalali, P. D. Trinh, S. Yegnanarayanan, F. Coppinger, "Guided-wave optics in silicon-on-insulator technology," IEEE Proceedings of Optoelectronics, Vol. 143, pp. 307, (1996).

[122] L. Eldada, "Telecom optical componentry: past, present, future," Proceedings of SPIE, Vol. 4604, pp. 1, (2001).

[123] A. L. Coldren and S.W, Corzine, "Diode Lasers and Photonic Integrated Circuits," John Wiley and Sons, Inc., New York, 1995.

[124] Class notes for MIT Course 6.973: Semiconductor Optoelectronics: Theory and Design, (2004).