Parallel Integrated Receivers for Multiple Antenna Wireless LAN Systems

by

Lunal Khuon

B.S., Illinois Institute of Technology (1994)
M.S., Illinois Institute of Technology (1998)

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering and Computer Science

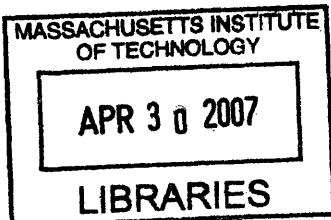at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 2007

© Massachusetts Institute of Technology 2007. All rights reserved.

Author . . . .
Department of Electrical Engineering and Computer Science
October 30, 2006

Certified by. . . . .
Charles G. Sodini
Professor
Thesis Supervisor

Accepted by . . . .
Arthur C. Smith
Chairman, Department Committee on Graduate Students

Parallel Integrated Receivers for Multiple Antenna Wireless LAN Systems

by

Lunal Khuon

Submitted to the Department of Electrical Engineering and Computer Science
on October 30, 2006, in partial fulfillment of the
requirements for the degree of
Doctor of Philosophy

Abstract

This thesis focuses on the design of power- and area-efficient parallel integrated receivers for multiple antenna wireless LAN systems. These receivers are part of an indoor parallel radio system that achieves 1 gigabit per second data rates and enables high bandwidth wireless communication between portable user devices and a high speed wired internet connection.

Since a critical aspect for efficiency is that an optimal number of transceivers be used to meet system requirements, this thesis first considers power dissipation and area consumption for parallel integrated transceivers. It develops parallel transceiver power dissipation and area consumption models that are functions of distance, data rate, and noise figure and incorporate the behavior of a multiple-input, multiple-output channel and power dissipation and area consumption values for typical RF circuits. These models properly balance benefits of multiple antennas with drawbacks due to parallel radio overhead. Their application shows that the combined transceiver power dissipation can actually decrease with more antennas and also provides a circuits-based number of antennas upper bound that has not been established previously. The thesis then proposes a solution that applies multiple antenna signal-to-noise ratio (SNR) gain at the receiver to reduce its power dissipation and area consumption. SNR gain trades noise figure for power- and area-efficient circuits. The implementation of a single chip 5.22-GHz area-efficient parallel receiver RFIC that shows practical application of these models, SNR gain, and area-efficient circuits is demonstrated. The context of this design comes from the Wireless Gigabit Local Area Network (WiGLAN). It's system characteristics such as a wide 150 MHz bandwidth and parallel radios uniquely determine a WiGLAN parallel receiver design.

Thesis Supervisor: Charles G. Sodini
Title: Professor

To Monita and Alexander

Acknowledgments

the definitive answer when it comes to circuit noise but, as ex-industry employees, we spend more time sharing "fond" memories of our previous working lives. I thank Albert Jerng, fellow dad, for sharing his parental knowledge and also for the many conversations we had on parenthood, engineering, and life in general. I thank John Fiorenza, the group's cultural ambassador, for all the left field conversations on the American culture and world history. If there's something to be known, engineering or otherwise, John is already there asking the questions.

I thank Rhonda Maynard for all her help. Rhonda handles all requests with the utmost care and efficiency and does everything with a smile! I thank Marilyn Pierce for taking care of many institution requirements on my behalf. Marilyn has been a lifesaver when it comes to making sure that I didn't miss any department requirements.

Finally, this work would not be possible without the love and support of my dearest wife, Monita. I thank Monita, with all my heart, for her patience, encouragement, understanding, and especially humor throughout the years at MIT. She has given me the little bursts of sunshine on even the cloudiest days. I thank Alex, our little baby, for bringing me so much happiness and love and providing that final push to wrap everything up. I thank my parents, Mr. and Mrs. Kandien and Sieklim Khuon, for their love and support. I thank my new parents, Mr. and Mrs. Bun Thong and Ly Keang Var, for their love and understanding. I thank Monida Var and Dr. Roger Fan for their quick wits and hilarous pokes that bring humor to life. Both Monida and Roger are passionate individuals that have the warmest hearts and the deepest love. It is truly wonderful to have them in my life. I thank my cousin and his wife, Timothy and Jenny Khuon, for always looking out for me while I was in Massachusetts. I've enjoyed the many South Shore and Costco shopping trips. Tim and Jenny's home was always open to me.

Contents

List of Figures

15

17

19

List of Tables

Chapter 1

Introduction

Investigations into the benefits of parallel radios, especially in the case of multiple transmit, multiple receive systems for broadband communications, tie heavily to a characterization of a multiple-input-multiple-output (MIMO) channel [1] and developments of space-time processing [2, 3, 4] and smart antennas [5, 6]. As these endeavors begin to mature, a next step considers the associated radio frequency (RF) hardware designs [2].

To begin, it is necessary to understand that power dissipation and area consumption for transceiver circuits are important concerns for multiple antenna systems. Table 1.1 lists percent power dissipation for an integrated 802.11a single radio chipset [7, 8, 9, 10]. The table shows that a transmitter and local oscillator consumes 75% of total radio power dissipation in transmit mode while a receiver and local oscillator consumes nearly 50% of total radio power dissipation in receive mode. The radio uses a transmitter that consists of programmable gain amplifiers, a pair

Transmit Mode:		Receive Mode:	
Transmitter	61%	Receiver	28%
Local Oscillator	14%	Local Oscillator	20%
Digital-to-Analog Converter	5%	Analog-to-Digital Converter	24%
Digital Signal Processor	20%	Digital Signal Processor	27%
Total	100%	Total	100%

Table 1.1: Percent power dissipation for a typical 802.11a radio [7, 8, 9, 10]

23

Transmitter	10%
Receiver	15%
Local Oscillator	7%
Analog-to-Digital Converter	5%
Digital-to-Analog Converter	5%
Digital Signal Processor	58%
Total	100%

Table 1.2: Percent area consumption for a typical 802.11a radio [7, 8, 9, 10]

Process(nm)	Cell Size(μm^2)	Memory Size(Mbit)	Chip Size(mm^2)	Release
130	2.45	18	103	March 00
90	1.0	50	109	February 02
65	0.57	70	110	April 04
45	0.346	153	119	January 06

Table 1.3: Intel SRAM test chips. The cell size trend shows roughly a 50% size decrease every 2 years [11].

of intermediate frequency image-reject mixers, radio frequency mixer, and a power amplifier and a receiver that consists of a low noise amplifier, radio frequency mixer, intermediate frequency quadrature mixers, and programmable gain amplifiers. These circuits along with the local oscillator form a transceiver and their power dissipation represent significant portion of total radio power dissipation. If an approximation for a multiple antenna system represents some multiple of these percentages, a first step to reduce radio power dissipation for multiple antenna systems then begins with minimization of transceiver power dissipation.

Table 1.2 lists percent area consumption for the same 802.11a single radio. Unlike percent power dissipation, the digital signal processor consumes the most chip area at 58%. A transmitter, receiver, and local oscillator together occupy 32% the total area. In terms of area, it seems that multiple antenna systems should focus on the processor. To do so, however, neglects recent trends in technology scaling that shrink digital circuits and increase transistor density. As an example, Table 1.3 lists physical cell, memory, and chip sizes for Intel's SRAM test chips that are forerunners for their processors [11]. The data shows roughly a 50% cell size decrease every 2 years. Given a recent release for a 153 Mbit SRAM that uses 0.346 μm^2 cell and has more than

24

one billion transistors, it is likely that processor area is not a cost driver for future multiple antenna systems [12].

The situation is quite different for transceiver circuits. A technology roadmap observes that obstacles to future passive integration are roadblocks to successful RF, analog, and mixed signal implementations [13]. A key point is that large value inductors and capacitors, as energy storage devices, require large area to achieve a high quality factor, or Q and therefore circuits that use them are inherently large [14]. Simply put, this implies that technology scaling does not shrink RF circuits. Therefore, similar to power dissipation, a significant step for multiple antenna systems minimizes area consumption for transceiver circuits.

This thesis takes steps to reduce power dissipation and area consumption for RF circuits in multiple antenna systems. Specifically, it investigates the design of power- and area-efficient parallel integrated receivers for a gigabit wireless LAN system. Since this design exploits the parallelism of the radio channel, the implementation allows the development of design methods specific to parallel radios and incorporates considerations for single chip integration and radio system design. This thesis proposes a system solution that utilizes multiple antenna signal-to-noise ratio (SNR) gain to minimize power dissipation and area consumption for parallel integrated receivers. To illustrate its application, it first develops power dissipation and area consumption models that incorporate SNR gain. The thesis also introduces circuits that trade SNR gain for lower power dissipation and area consumption. In the sections to follow, a brief overview of the main ideas of the thesis is given. More detailed discussions are found in the respective chapters.

1.1 WiGLAN Parallel Receiver System

The Wireless Gigabit Local Area Network (WiGLAN) is a current research project at the Massachusetts Institute of Technology that explores various techniques and approaches at the system and circuit levels that would allow indoor wireless communication at data rates of 1 gigabit per second [15]. In particular, it uses parallel
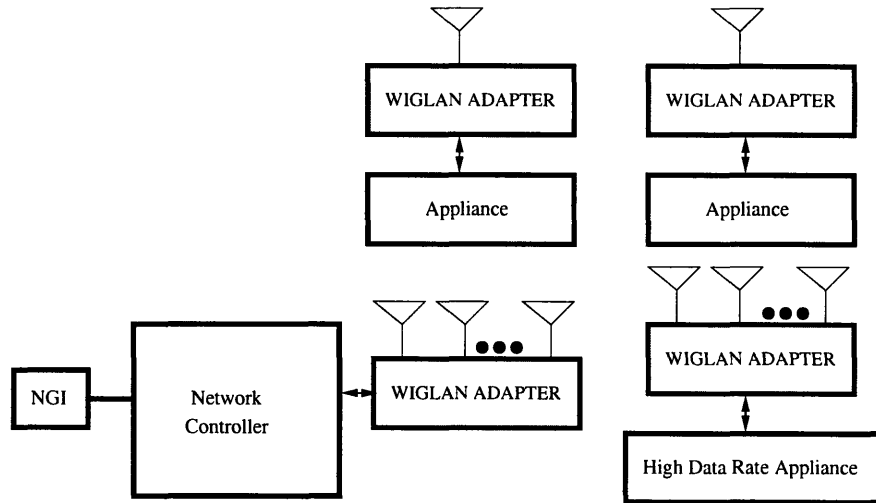
Figure 1-1: Wireless Gigabit Local Area Network

radios, 150 MHz bandwidth at 5.22 GHz, Orthogonal Frequency Division Multiplexing (OFDM), and adaptive modulation. WiGLAN's parallel radios exploit spatially independent multi-path signal propagation to relax necessary SNR for low bit error rates. OFDM allows more efficient use of a wide bandwidth while adaptive modulation seeks to efficiently use a time-varying fading channel.

As shown in Fig. 1-1, WiGLAN consists of a network controller that is connected by wire to the Next Generation Internet (NGI). The controller communicates wirelessly with various appliances that exist throughout the indoor home or office environment using an attached multiple antenna WiGLAN adapter. Application of OFDM allows the controller to determine and allocate a number of sub-carriers to each appliances depending on their rate requirements. At the appliances, low and high data rate devices use single and multiple antenna WiGLAN adapters, respectively.

Chapter 2 examines a WiGLAN parallel receiver system. It determines that a digital intermediate frequency (IF) receiver best meets the requirements for parallel receivers. A digital IF receiver architecture avoids analog quadrature downconversion and eliminates IQ mismatch. However, since the WiGLAN receiver uses a heterodyne architecture, it must reject an image signal before performing frequency translation. An integrated Q-enhanced filter rejects this image signal and provides for a fully inte-

grated solution. The WiGLAN receiver also implements singular value decomposition (SVD) in its digital processor to exploit the benefits of multiple antennas for spatial diversity. SVD decomposes the MIMO channel matrix into equivalent parallel channels but requires that the transmitter knows the channel. WiGLAN parallel receivers characterize and send back channel information to the transmitters to meet this need.

1.2 Power and Area Models

Considering a probabilistic channel alone, it appears that more antennas are always better for multiple antenna systems. An uncoded MxN antenna system in a rich-scattering Rayleigh fading environment has maximum diversity MN and a bit error rate that is proportional to SNR^{-MN} [16]. Each additional antenna favorably increases diversity and lowers bit error rate for a given SNR though there is less incremental diversity gain with each additional antenna. To determine a lower bound, [17] considers a system that operates in this rich-scattering channel and determines the minimum number of antennas that is sufficient to support various data and error rates. To determine an upper bound, [18] considers both the scattering condition for the channel and the area constraints for the transmit and receive antenna arrays. More clusters of scatterers increase the number of parallel subchannels while for a given wireless device's area, as the number of antennas increases, spacings between antennas decreases and the antennas eventually become correlated and degrade channel parallelism.

The first part of Chapter 3 develops a power dissipation model that adds transceiver power dissipation to the results from [17] to determine the optimal number of antennas for a multiple antenna system. This represents the most effective efficiency as it proposes to use only the number of antennas that is necessary to meet system requirements. Similar to [17], this thesis assumes a rich-scattering channel in order to focus on implementation tradeoffs. A method that considers the channel condition to determine the number of antennas is given in [18]. This chapter adapts a transceiver energy model presented in [19] for a wireless microsensor network to a general multiple

27

antenna wireless LAN system by considering equal time operation for transmitter and receiver and incorporating a multiplication constant N that represents the number of antennas. The model determines an optimal number of antennas by capturing a decrease in RF transmit power due to increasing diversity with the increase in overhead power from each additional transceiver.

This part of the chapter also develops an area consumption model. This model simply adds area consumption for all the individual transceiver circuits to give a total. An area consumption model ensures that an optimal number of antennas that satisfies power dissipation and system requirements does not exceed available chip area.

1.3   SNR Gain and Its Application

SNR gain represents a relaxation in necessary SNR for a multiple antenna system given the same data and bit error rates and operating conditions as a single transmit, single receive (1x1) antenna system. An advantage of SNR gain is that it increases transmission range for a wireless system without additional transmit signal power. This aspect has been thoroughly exploited by transceiver [20, 21] and receiver [22, 23] designers.

The second part of Chapter 3 proposes applying portions of SNR gain to lower power dissipation and area consumption for parallel transceivers as shown in Fig. 1-2. At the transmitter, SNR gain is applied to lower RF transmit signal power. Less RF power lowers power dissipation for a power amplifier (PA) which then lowers transceiver power dissipation. Since PA power dissipation represents a large portion of transceiver power dissipation, the reduction is significant. For the situation when RF transmit signal power generation dominates transceiver power dissipation, combined power dissipation for multiple transceivers decreases with more antennas. This implies, for example, that total power dissipation for two or more transceivers can actually be less than the power dissipation for one transceiver. At the receiver, SNR gain is applied to relax noise figure. This allows usage of receive circuits that trade power dissipation and area consumption for noise. This latter portion of the thesis is

```
        ┌─────────────────────────────────────┐
        ┊        Multiple Antenna System      ┊
        ┊        Signal–to–Noise Ratio Gain   ┊
        └─────────────────────────────────────┘
                                        │
                                        ▼
                        ┌────────────────────────────────┐
                        │  Relax circuit noise: Noise Figure │
                        └────────────────────────────────┘

┌──────────────────────┐   ┌──────────────────────┐   ┌──────────────────────┐
│ (1) Reduce Transmit  │   │ (2) Reduce Receiver  │   │ (3) Reduce Chip Area  │
│     Power            │   │     Power Consumption│   │                       │
└──────────────────────┘   └──────────────────────┘   └──────────────────────┘
```
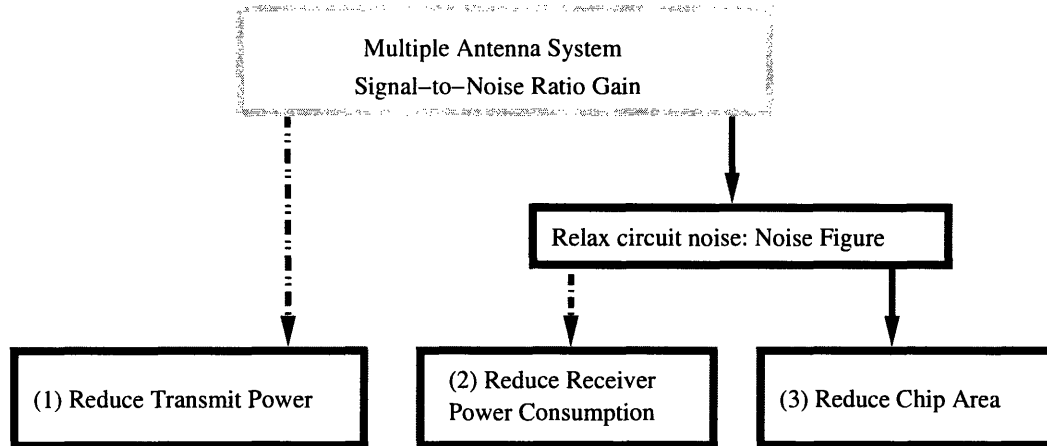
Figure 1-2: Application of SNR gain

also reported in [24, 25].

Since the parallel transceiver power dissipation model includes multiple antenna SNR in its calculation, it inherently incorporates SNR gain to reduce the RF transmit signal power. To account for the other two SNR gain parameters, minor modifications to both power dissipation and area consumption models are necessary. Application of SNR gain to reduce receiver operating power requires that the power dissipation model incorporates the resulting higher noise figure and lower receiver operating power. Similarly, application of SNR gain to reduce receiver area consumption requires that the power dissipation model incorporates the resulting higher noise figure and that the area consumption model captures the lower receiver area consumption. These requirements simply imply introducing multiplication factors for power dissipation and area consumption and associating appropriate noise figures with them.

Embedding SNR gain within power dissipation and area consumption models allows its proper application. For example, at short distances, RF transmit power generation represents a small portion of transceiver power dissipation. In this situation, where transmit signal power is not dominant, a transceiver power dissipation model shows that it is better to apply SNR gain to relax noise figure and lower receiver operating power. In another situation, available chip area may be insufficient to support the optimal number of antennas. A transceiver area consumption model,

for this case, suggests application of SNR gain to lower chip area while a transceiver power dissipation model assesses the impact.

1.4 Minimal Power and Area Circuits

SNR gain application at the receiver requires circuits that are able to trade noise for lower power dissipation and area consumption. Chapter 4 introduces a variable power low noise amplifier (VPLNA) and area-efficient low noise amplifier (LNA) to answer this need. A VPLNA lowers its power dissipation when there is sufficient SNR gain to support a resulting higher noise figure. Lower power dissipation results from using a lower bias current either through adaptively controlling the current source or switching to an amplifier gain branch that consumes less current. Lower current yields less gain which then degrades noise figure for a VPLNA with adaptive current source while a lower gain branch has higher noise figure for multiple gain branch VPLNA. An area-efficient LNA consumes little chip area since it uses on–chip resistors instead of physically large on–chip inductors in its design. However, as resistors contribute additional noise, an area-efficient LNA also requires sufficient SNR gain to support its higher noise figure.

1.5 Area-efficient Parallel Receiver RFIC

Application of power dissipation and area consumption models, SNR gain, and area-efficient circuits produces an area-efficient single-chip parallel receiver RFIC test chip for WiGLAN. Chapter 5 presents this chip that has four parallel receivers and their shared circuits. Each receiver has a low noise amplifier, Q-enhanced image reject notch filter, mixer, and local oscillator amplifier but shares a global local oscillator amplifier and distribution circuits for bias and filter tuning. Measurement shows that one receiver occupies an active area less than 1 mm^2, provides 14 dB gain, and consumes 50 mW. On–chip image filters have rejections better than 30 dB at the image frequency. This portion of the thesis is also reported in [26].

30

1.6 Thesis Outline

For the rest of the thesis, brief descriptions for the chapters are as follow.

- Chapter 2 presents a parallel receiver system that uses digital IF and integrated Q-enhanced image filters and implements SVD within its digital processor to achieve spatial diversity gain.

- Chapter 3 develops the consumption models for parallel transceivers. It begins first with a single transceiver models and extends to parallel transceiver models based on spatial diversity. Using these models, this chapter examines in greater detail power and area tradeoffs for SNR gain and show their relationships to number of transceivers, distance, and noise figure.

- Chapter 4 presents variable power and area-efficient circuits. A variable power LNA lowers its power dissipation to lower transceiver power dissipation. An area-efficient LNA cost effectively enables parallel transceiver implementation on–chip. Both circuits applies SNR gain to relax noise figure requirements.

- Chapter 5 applies power dissipation and area consumption models together with area-efficient circuits to implement a parallel receiver chip with minimal transceiver power dissipation.

- Chapter 6 reviews the thesis contributions and discusses possible future research directions.

Chapter 2

WiGLAN Parallel Receiver System

This chapter introduces the WiGLAN parallel receiver system. It consists of multiple antennas, parallel radio frequency (RF) receivers, analog-to-digital converters (ADCs), and a MIMO-OFDM digital signal processor (DSP) as shown in Fig. 2-1. With multiple antennas, each WiGLAN parallel receiver experiences spatially independent fading. It is through this independence that WiGLAN exploits the parallelism of an indoor wireless channel. Each antenna has a digital intermediate frequency (IF) receiver to convert signals from RF to a low IF and a time-interleaved ADC array to digitize an entire 150 MHz bandwidth [27]. This maintains the parallelism on–chip and also avoids analog quadrature downconversion. Inputs from each receiver then feed a MIMO-OFDM DSP that applies singular value decomposition (SVD) to achieve SNR gain [17]. In the sections to follow, this chapter discusses the
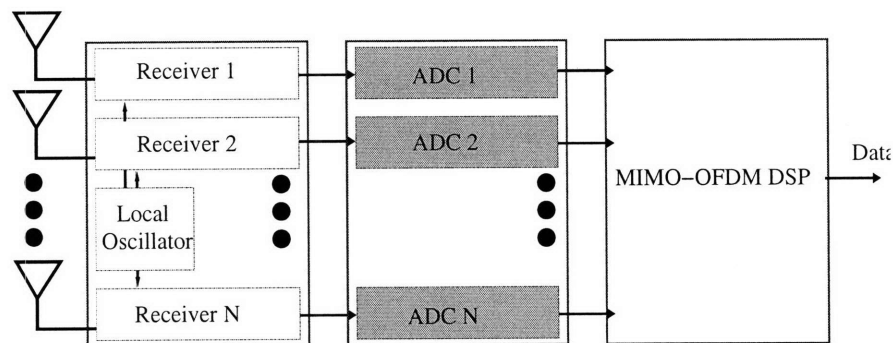
Figure 2-1: Parallel receiver system

33

characteristics of an indoor wireless channel, presents WiGLAN digital IF receiver, ADC, and DSP. and concludes with baseband bit error rate (BER) simulation results [17] that become critical inputs to the power dissipation and area consumption models.

2.1 Wireless Channel

WiGLAN operates in an indoor wireless channel as typically found in home and business office environments. Characteristics of these environments include multiple partitions that prevent line of sight communication, small objects that scatter signals throughout, and people whose movements create motion in the channel. In such environments, WiGLAN uses multiple antennas to improve its link quality and applies OFDM so that it may operate at 5.22 GHz with a wide 150 MHz bandwidth. Since both of these techniques tie closely to the nature of the channel, the following discussion begins with a description of a wireless channel and then shows how WiGLAN uses this channel to achieve reliable high data rate wireless communication.

2.1.1 Multipath Propagation and Fading

In addition to a direct path, radio waves propagate from the transmitter to the receiver by reflection, diffraction, and scattering. Fig. 2-2 shows these mechanisms between a single transmitter and two receivers. Reflection occurs when a wave encounters a large object when compared to its wavelength. Depending on the properties of the object and angle of incidence, portions or all of the wave reflect back. For example, if the wave impinges on a perfect conductor, total reflection occurs. On the other hand, if it encounters a dielectric, then part of the wave reflects while the other part refracts into the dielectric. Diffraction occurs when there is a sharp obstruction along the path. The wave bends around the corner of the obstruction such that a receiver in the shadow of the obstruction can detect the signal. Scattering occurs when the wave either encounters a rough surface or small objects compared to its wavelength. The resulting reflected waves spread out in all directions. Due to these propagation
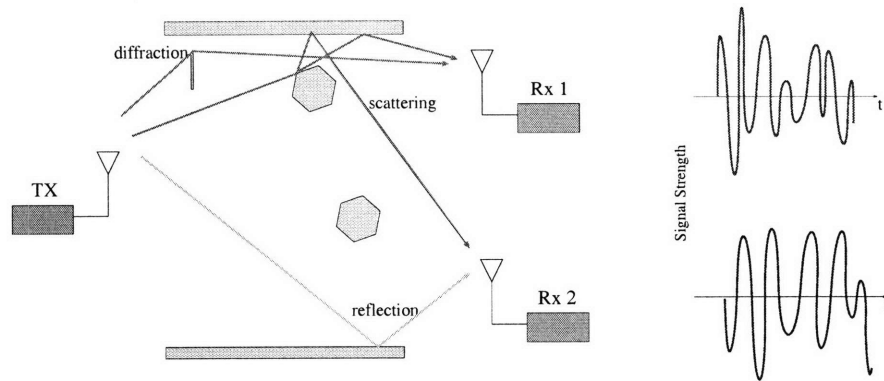
Figure 2-2: Multi-path propagation and fading for two receivers

mechanisms, a receiver at one location detects a signal that is a combination of waves that travelled different paths of varying lengths from the transmitter to the receiver. This type of propagation is known as multipath propagation [28].

As a result of multipath propagation, multiple versions of the transmitted signal arrive at the receiver with various time delays and attenuations. This results in the spreading of the modulation symbol in time and is referred to as time dispersion. The standard deviation of the time spread is termed rms delay spread. In addition, movements within the channel produce a time varying channel that spreads the frequency components of the signal. This effect is known as frequency dispersion and the spread is specifically called the Doppler spread. The Doppler spread expands a single frequency tone into a spectrum and is a function of the velocity of motion and the signal wavelength.

Fading is a rapid fluctuation in the instantaneous received signal amplitude over a small travel distance or time. The right side of Fig. 2-2 shows the signal amplitudes for the two receivers that experience independent fading versus time. The impact of fading on a wireless system is a function of both the channel characteristics and the transmitted signal. If the modulation bandwidth is less than the coherence bandwidth, that is, the bandwidth for which the channel affects all the signal frequencies equally, the signal experiences flat fading. Viewed in the time domain, flat fading implies that the symbol period is greater than the rms delay spread. If the modulation bandwidth exceeds the coherence bandwidth, the signal experiences fre-

quency selective fading and the channel affects the signal frequencies unequally and produces intersymbol interference. Viewed in the time domain, frequency selective fading implies that the symbol period is less than the rms delay spread. In a separate phenomenon, if the symbol period is less than the channel coherence time, that is, the period of time for which the channel affects all portions of the signal equally, the signal experiences slow fading. Viewed in the frequency domain, slow fading implies that the modulation bandwidth is greater than the Doppler spread. If, on the other hand, the symbol period is greater than the channel coherence time, the signal experiences fast fading. A fast fading channel is a channel that changes faster than the signal and results in distortion seen in time as unequal effects on the symbol during its period. Viewed in the frequency domain, fast fading implies the modulation bandwidth is less than the Doppler spread.

In a rich scattering environment, there exist parallel subchannels in space that create multiple inputs and multiple outputs for the channel. This allows parallel radios to implement spatial multiplexing and diversity. Due to multipath, each transmit antenna sees effectively a different channel and simultaneously transmits with the same frequency band. At the receivers, the channel matrix allows the receivers to extract the spatial signatures of the transmitted signals. Spatial multiplexing exploits the parallel subchannels to achieve high data rate transmissions by dividing a high rate data stream into several lower rate parallel data streams that transmit through a different antenna element separated by physical distance. At the parallel receivers, linear combinations of the received signals are spatially equalized, processed to retrieve the sub-streams, and then combined to recover the original data stream. For spatial diversity, parallel subchannels also exist between the parallel transmitters and receivers as in spatial multiplexing. However, space-time coding encodes the same signal differently and transmits each coded stream through a different antenna. Therefore, for a MIMO system, as shown in Fig. 2-3, if the parallel streams consist of different data, spatial multiplexing is achieved. On the other hand, if the same streams are redundantly transmitted as shown in Fig. 2-4, then spatial diversity is achieved. In order to exploit a MIMO channel, the receivers must be able to deter-
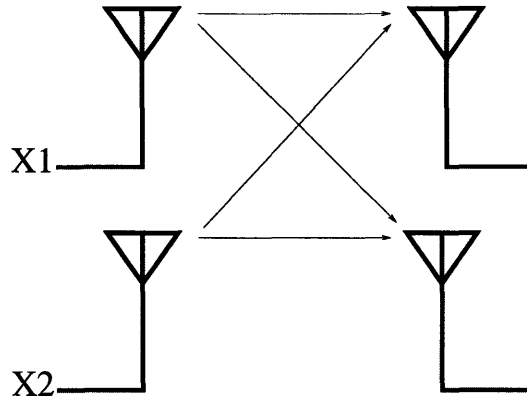
Figure 2-3: Spatial multiplexing example using 2x2 system with two separate data streams X1 and X2
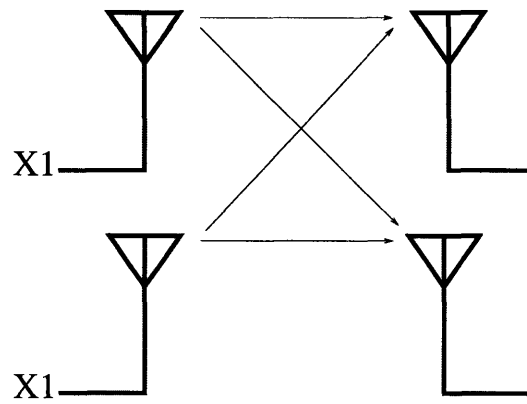
Figure 2-4: Spatial diversity example using 2x2 system with redundant data stream X1

mine the spatial signatures of the transmitted signals. As will be shown later, this is accomplished through the application of singular value decomposition (SVD).

Although a spatial multiplexing or diversity system uses an array of antennas, it is not a beamforming system. Certainly the individual antennas themselves could be similarly isotropic. However, a beamforming system uses an array of antennas to create a strong radiation pattern in the desired direction. A beamforming system also works relatively well in line-of-sight communication systems such satellites and point-to-point microwave links. Its antenna array does not need to exploit multipath signal propagation since the system enhances the line-of-sight transmit signal itself. This implies that a beamforming system does not depend on a MIMO channel. On the other hand, multiple antennas for spatial multiplexing and diversity systems require multipath signal propagation and normally operate in non line-of-sight situations.

2.1.2   WiGLAN System in a Fading Channel

At 5 GHz in an indoor environment, WiGLAN operates in a frequency selective but slow fading channel. It accounts for this channel behavior to achieve high data rate reliable communication as follow.

- **Fading**: WiGLAN uses multiple antennas to apply spatial diversity and overcome deep fades. Multiple antennas at antenna spacings greater than half wavelengths experience independent fading [1, 3]. Therefore, for multiple receive antennas, it is possible that while one receive antenna experiences a deep fade, another captures a strong signal. As the number of antennas increases, the chances that all receive antennas experiencing a deep fade significantly decreases. While it is certainly possible to achieve similar gains using time or frequency diversity, with multiple antennas, WiGLAN reaps the benefits of diversity without increasing time delay and frequency bandwidth. In time diversity, a data repeats its transmission with time spacings exceeding the coherence time. Although this allows each transmission to experience a different fading, a receiver using time diversity must wait for all transmissions to complete. In

frequency diversity, data repeats its transmission on different carriers that are more than a coherence bandwidth apart. Similar to time diversity, each frequency transmission experiences a different fading. However, using frequency diversity without decreasing data rates requires more frequency spectrum.

Since WiGLAN applies spatial diversity instead of multiplexing, it sacrifices multiple antenna capacity for diversity gain. In [17], it was shown that at high SNR, the change in capacity, ΔC, is given as

$$\Delta C \approx 0.33k\Delta SNR, \tag{2.1}$$

where k represents the number of parallel subchannels and is equivalent to N antennas for an NxN system and ΔSNR is given in dB. The relation implies that every 3 dB decrease in the SNR requirements due to spatial diversity costs k b/s/Hz in capacity. It is important to note that WiGLAN is a high diversity system that achieves gigabit per second data rates by using a wide frequency bandwidth and does not implement spatial multiplexing.

- **Frequency selective fading**: With its wide 150 MHz bandwidth, a WiGLAN transmission at 5.22 GHz experiences frequency selective fading. To overcome this impairment, WiGLAN applies OFDM and breaks its band into 1 MHz frequency bins. This bandwidth is well below the 4 MHz coherence bandwidth for 5-GHz non-line of sight [29] so that effectively, each modulated OFDM subcarrier experiences flat fading.

- **Slow fading**: An indoor environment has little motion and results in a slow fading channel. WiGLAN takes advantage of this situation and applies adaptive modulation for each OFDM subcarrier. With adaptive modulation, the receive node characterizes the channel for each subcarrier and transmits this information back to the transmit node. The transmit node then adjusts modulation order for each subcarrier corresponding to the SNR that the channel supports. WiGLAN does not use a subcarrier with very poor SNR in order to reduce errors

due to outage. For a subcarrier with good SNR, WiGLAN applies higher order modulation in order to increase data rates. Since the channel changes slowly, a transmit node can use a particular rate for some time before another channel measurement is necessary. This minimizes overhead for adaptive modulation. Near 5 GHz, the coherence time is around 24 ms with actual transmission time for WiGLAN set at 10 ms [30].

2.2   Digital IF Receiver

WiGLAN uses a digital IF receiver that simplifies and removes many analog impairments. A digital IF receiver recovers in-phase (I) and quadrature (Q) components after digitization and avoids analog gain and phase matching issues for wide bandwidth and between parallel receivers. However, a digital IF receiver has an image problem that requires filtering. An integrated Q-enhanced image filter eliminates usage of an off-chip image filter and provides a fully integrated solution without resorting to direct conversion.

2.2.1   IQ Mismatch

A direct conversion receiver converts a signal at RF directly to baseband frequency. It simplifies RF receiver integration because it has no image and uses low pass filters at its outputs that are amenable to integration. However, a direct conversion receiver implements analog quadrature downconversion and therefore inherently has IQ mismatch. Fig. 2-5 shows an analog quadrature downconverter that uses quadrature LO signals and two separate branches with each branch consisting of a mixer and low pass filter. The top branch retrieves a I signal while a bottom branch retrieves a Q, or 90° out of phase, signal. These two components together provide amplitude and phase information that are sufficient to reconstruct the transmitted signal. An amplitude error ϵ and phase error $\Delta\phi$ arise through LO paths and between the two branches and cause shift and rotation, respectively, as shown in Fig. 2-6, and given

Gain and Phase Error

Gain and Phase Error

Gain and Phase Error
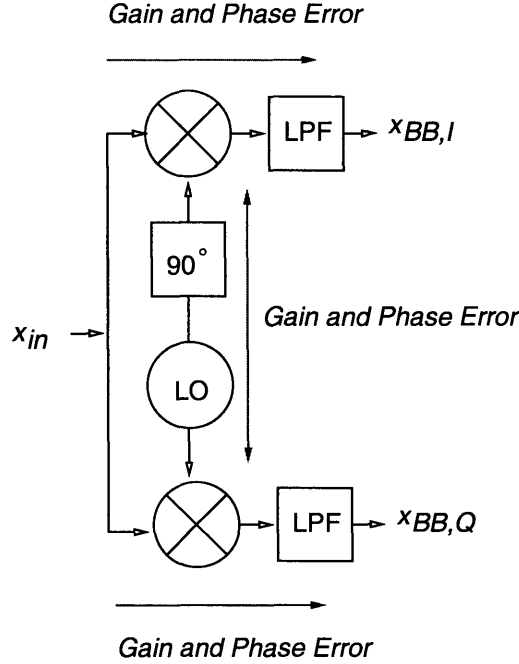
Figure 2-5: Analog quadrature downconversion with gain and phase error paths

as [31]

$$x_{BB,I}(t) = a\left(1 + \frac{\epsilon}{2}\right)\cos\frac{\Delta\phi}{2} - b\left(1 + \frac{\epsilon}{2}\right)\sin\frac{\Delta\phi}{2} \qquad (2.2)$$

$$x_{BB,Q}(t) = -a\left(1 - \frac{\epsilon}{2}\right)\sin\frac{\Delta\phi}{2} + b\left(1 - \frac{\epsilon}{2}\right)\cos\frac{\Delta\phi}{2}, \qquad (2.3)$$

where received signal $x_{in} = a\cos\omega_C t + b\sin\omega_C t$ and a and b are either -1 or +1. Simulations for a direct conversion receiver that uses 64-QAM modulation in an OFDM WLAN system show that IQ mismatch at ϵ=1% and $\Delta\phi$=1° has a 2 dB SNR degradation at bit error rate of 10^{-5} [32]. An IQ mismatch of ϵ=10% and $\Delta\phi$=10° produces a bit error rate floor of 10^{-1} independent of higher SNR.

A digital IF receiver eliminates IQ mismatch since, as shown in Fig. 2-7, quadrature downconversion comes after analog-to-digital conversion [33]. A digital sinewave generator produces quadrature LO signals for the I and Q branches and digital multipliers replace mixers. There are no gain and phase errors through either digital LO paths or the two branches so that $\epsilon \approx 0$ and $\Delta\phi \approx 0$ and (2.2) and (2.3) become $x_{BB,I} = a$ and $x_{BB,Q} = b$. Additionally, since a digital IF receiver is a heterodyne

Gain Error
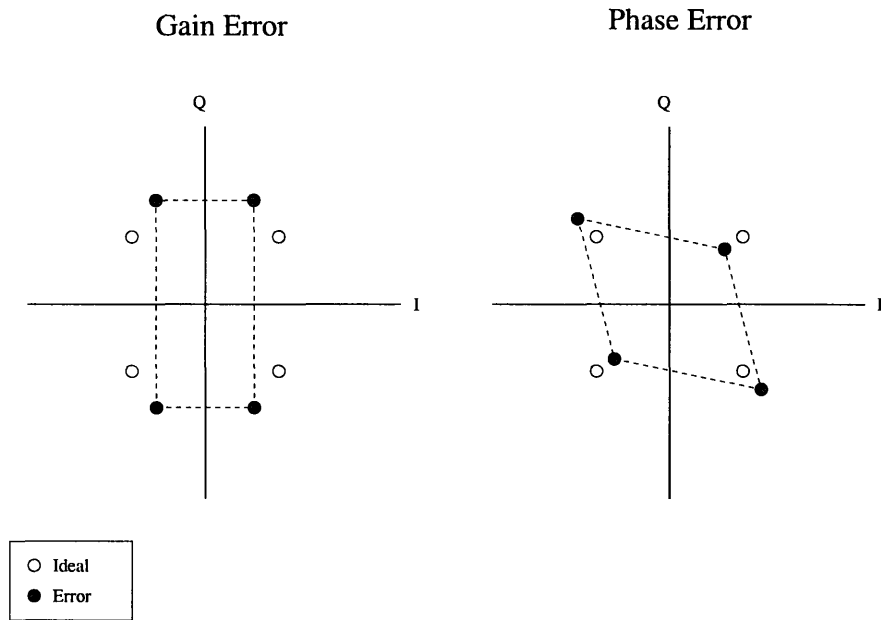
Phase Error

Figure 2-6: Constellation plots demonstrating gain and phase errors for simple 4 QAM
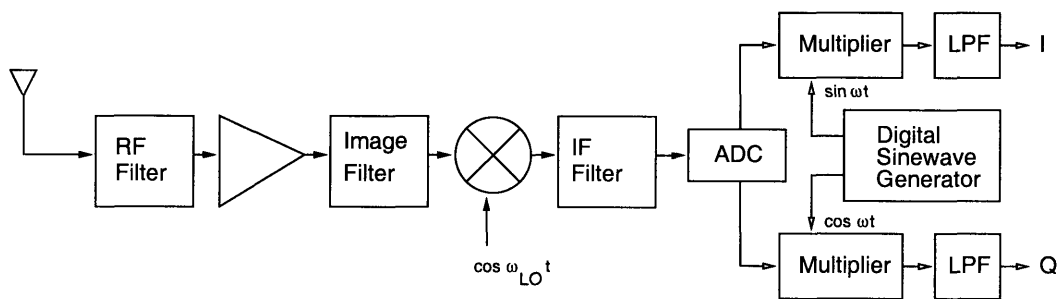
Figure 2-7: A digital IF receiver and digital IQ retrieval.

receiver, it solves or eliminates other problems unique to a direct conversion receiver that include dc offset, 1/f noise, and LO feedthrough [34].

2.2.2 Integrated Q-enhanced Image Filter

A conventional heterodyne receiver uses off-chip filters for its RF, image, and IF filtering needs (see filters in Fig. 2-7). Discrete components such as low loss ceramic filters and high Q surface-acoustic-wave (SAW) filters provide a proper balance of minimum insertion loss and high selectivity [35] and their utilization increases as the the wireless industry grows [36]. For WiGLAN parallel receivers, however, to use an off chip filter for the image rejection requires that the signal be taken off chip after a low noise amplifier (LNA) and then brought back on–chip before the mixer. High frequency operation along with board parasitics makes off–chip impedance matching difficult [37]. The level of difficulty further increases with parallel receivers, as multiple matches must be made per receiver. This latter requirement also increases chip power dissipation and area consumption due to matching and driver circuits.

To avoid these complications, a WiGLAN receiver uses an integrated Q-enhanced notch filter to reject the image frequency. An integrated Q-enhanced notch filter applies active circuits to overcome losses for on–chip inductors and improves its Q. Additionally, it enables high image rejection with a low IF by placing a notch directly at the image frequency. With low IF and since a WiGLAN receiver digitizes its entire bandwidth, an anti-alias filter that is part of the ADC becomes a sufficient IF filter. A WiGLAN receiver can still use an off-chip RF filter before the LNA since its inputs come from off-chip antennas. An off-chip RF filter does not add complexity but requires that the LNA presents a correct terminal impedance for the filter.

In general, a choice for a receiver's output frequency considers a trade between the capabilities to perform image rejection and IF channel selection. Fig. 2-8 illustrates this trade. An image signal at ω_{IM} and a desired RF signal at ω_{RF} are symmetric with respect to the LO signal at ω_{LO}. Frequency downconversion implies a translation
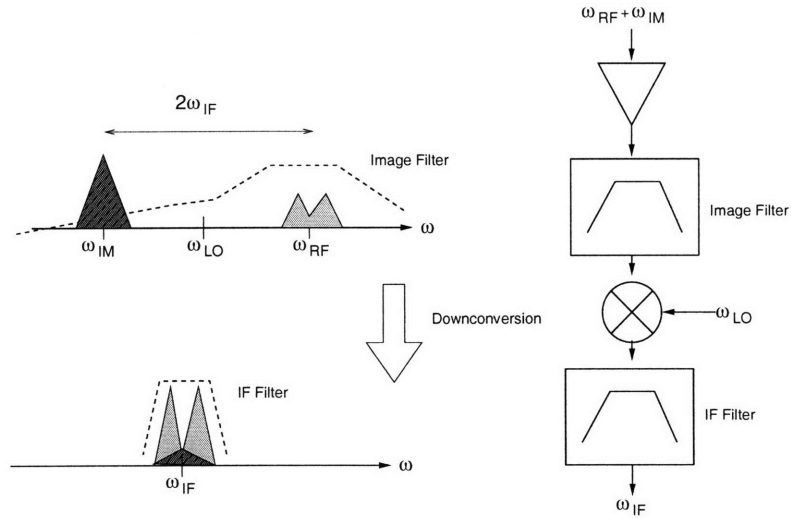
Figure 2-8: Single conversion (heterodyne) receiver

for these two signals to a lower frequency ω_{IF} given as

$$\omega_{IF} = |\omega_{RF} - \omega_{LO}| = |\omega_{IM} - \omega_{LO}|. \tag{2.4}$$

By symmetry, an image signal exists at two times IF away from a desired RF signal. A higher IF implies that an image is farther away from the desired RF signal and experiences greater attenuation from a bandpass image filter. However, at higher IF, the filter requires a larger Q to select the same channel bandwidth. As an example, consider a simple one resonator bandpasss filter whose bandwidth W is given as

$$W = \frac{\omega_{IF}}{Q}, \tag{2.5}$$

where ω_{IF} is the IF center frequency and Q represents its quality factor. Increasing ω_{IF} requires that filter's quality factor to increase proportionally in order to maintain W. High Q inductors and therefore high Q filters are difficult to achieve on–chip. To improve IF channel selection, it would be better to lower the IF frequency so that a lower Q still achieves W. For this latter situation, however, the image moves closer to a desired RF signal and the image filter provides little attenuation.

A double conversion receiver, as shown in Fig. 2-9, breaks the relation between

44
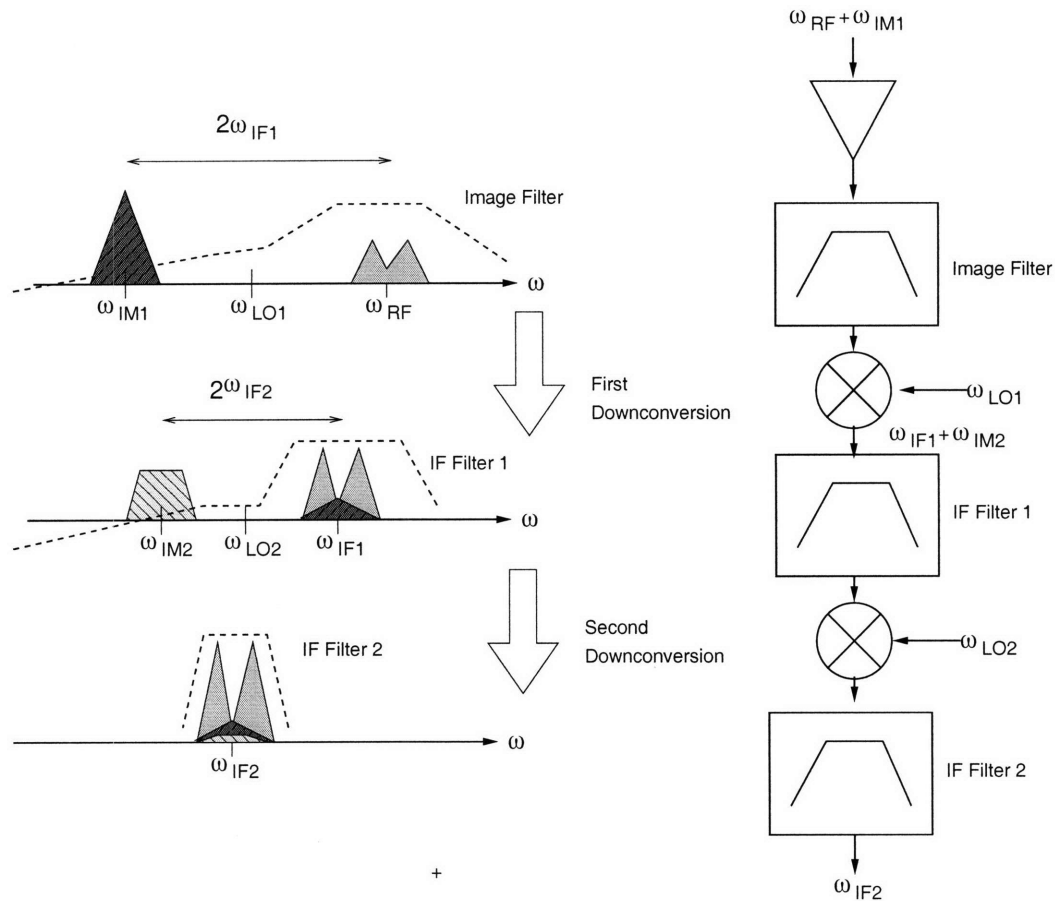
Figure 2-9: Double downconversion receiver

image rejection and IF channel selection. Its first frequency downconversion uses a high IF at ω_{IF1} that maximizes image rejection at ω_{IM1}. A second downconversion to a low IF at ω_{IF2} allows a low Q IF Filter 2 to perform IF channel selection or, in the WiGLAN case, a low pass filter to select an entire bandwidth. However, this receiver requires two mixers and two distinct LO signal frequencies and adds an additional IF filter that can be a challenge to integrate. In [38], the authors demonstrate a third order Q-enhanced LC bandpass filter chip at 2140 MHz with 60 MHz bandwidth and 0 dB insertion loss [38]. Unfortunately, this single-ended filter consumes 2 mm^2 chip area and is not favorable for area-efficient parallel receivers.

An image reject receiver also provides image rejection with a low IF. It does so by cancelling an image through quadrature mixing, as shown in Fig. 2-10. Including

45
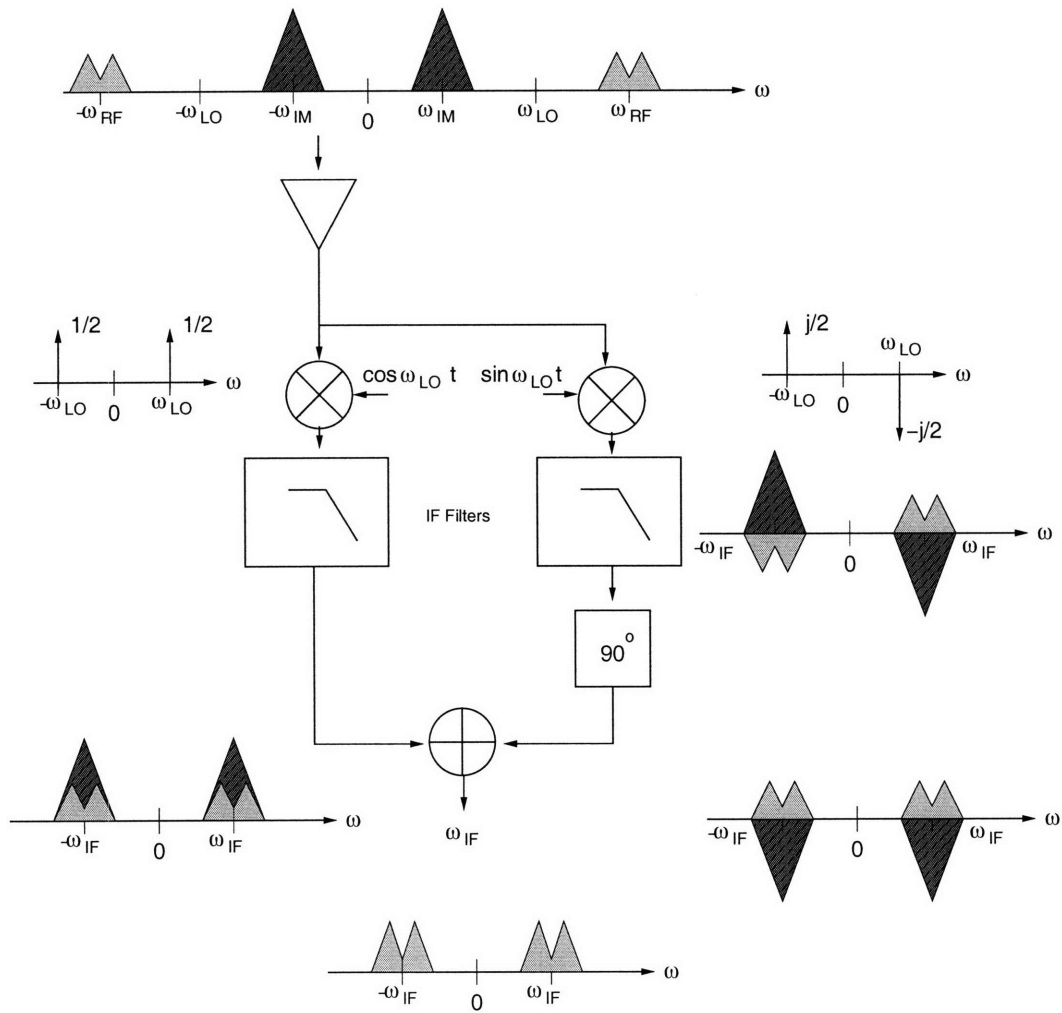
Figure 2-10: Image reject receiver

negative frequency components, an input consists of an image at ω_{IM} and $-\omega_{IM}$ and a desired RF signal at ω_{RF} and $-\omega_{RF}$. Quadrature LO signals $\cos\omega_{LO}t$ and $\sin\omega_{LO}t$ produce tones at ω_{LO} and $-\omega_{LO}$ whose amplitudes are evident by rewriting the LO signals as sums of exponential functions as follow.

$$\cos\omega_{LO}t = \frac{1}{2}e^{j\omega_{LO}t} + \frac{1}{2}e^{-j\omega_{LO}t} \tag{2.6}$$

$$\sin\omega_{LO}t = \frac{-j}{2}e^{j\omega_{LO}t} + \frac{j}{2}e^{-j\omega_{LO}t} \tag{2.7}$$

Mixing with these LO signals translates input signals to ω_{IF} and $-\omega_{IF}$. For $\sin\omega_{LO}t$, frequency translation also results in a negative amplitudes for the desired signal at $-\omega_{IF}$ and image signal at ω_{IF}. If inputs are cosines, trigonometry verifies this result. For example, a translated desired signal is given as

$$(\sin\omega_{LO}t)(\cos\omega_{RF}t) = \frac{1}{2}\sin\left(\omega_{LO} + \omega_{RF}\right)t + \frac{1}{2}\sin\left(\omega_{LO} - \omega_{RF}\right)t. \tag{2.8}$$

A first term with $\omega_{LO} + \omega_{RF}$ disappears with low pass filtering while a second term becomes negative, that is, $\sin(\omega_{LO} - \omega_{RF})t = -\sin(\omega_{RF} - \omega_{LO})t$ since $\omega_{RF} > \omega_{LO}$. Similarly, processing an image signal produces $\frac{1}{2}\sin\left(\omega_{LO} - \omega_{IM}\right)t$. These signals then pass through a 90° phase shift that flips signs for components at $-\omega_{IF}$. A summer adds this result with the result from cosine branch and mathematically cancels the unwanted image but reinforces the desired signal. This architecture has been shown to contribute 36 dB image frequency rejection with a 5-GHz RF signal and a low 250 MHz IF frequency [39]. However, the quadrature mixing operation suffers from the same IQ mismatch as an analog quadrature downconverter. In fact, [31] notes that IQ mismatch degrades the performance of an image reject receiver architecture more than even a direct conversion receiver. The WiGLAN digital IF receiver avoids using an image reject receiver architecture for the same reasons it does not use a direct conversion receiver.

A Q-enhanced notch filter provides high image rejection and allows usage of a low IF receiver without using a double conversion or image reject receiver. Fig. 2-11
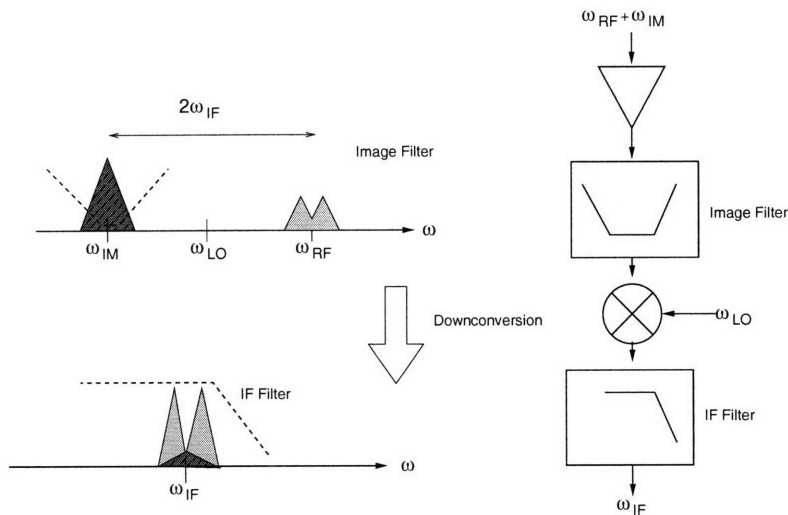
Figure 2-11: Receiver with Q-enhanced notch filter for image rejection

shows a receiver with a Q-enhanced notch filter that simply places a notch at the image frequency and a low pass filter at IF that allows selection of an entire band. A Q-enhanced notch filter has been shown to achieve over 50 dB image rejection at the image frequency of 2.5 GHz for a 1.9-GHz receiver [40]. This filter uses a series LC resonator in-between two transistors in cascode amplifier configuration to create a notch. With the LC resonant frequency set at the image frequency, a low impedance short-circuits an undesired image to ground but passes a desired RF signal. The amount of image rejection, or the depth of the notch, depends heavily on the Q of the LC resonator. Therefore, Q-enhancement maximizes rejection. This filter and its variation appear as part of an LNA [41], [42], [43] and in 5-GHz wireless LAN receivers [44], [45], [46]. Chapter 5 gives design details for a cross-coupled PMOS Q-enhanced notch filter that produces image rejection for the WiGLAN digital IF receiver.

2.3 Analog-to-Digital Converter

A WiGLAN digital IF receiver takes advantage of a high performance, wide bandwidth, massively parallel time-interleaved ADC array [27]. This array consists of 128
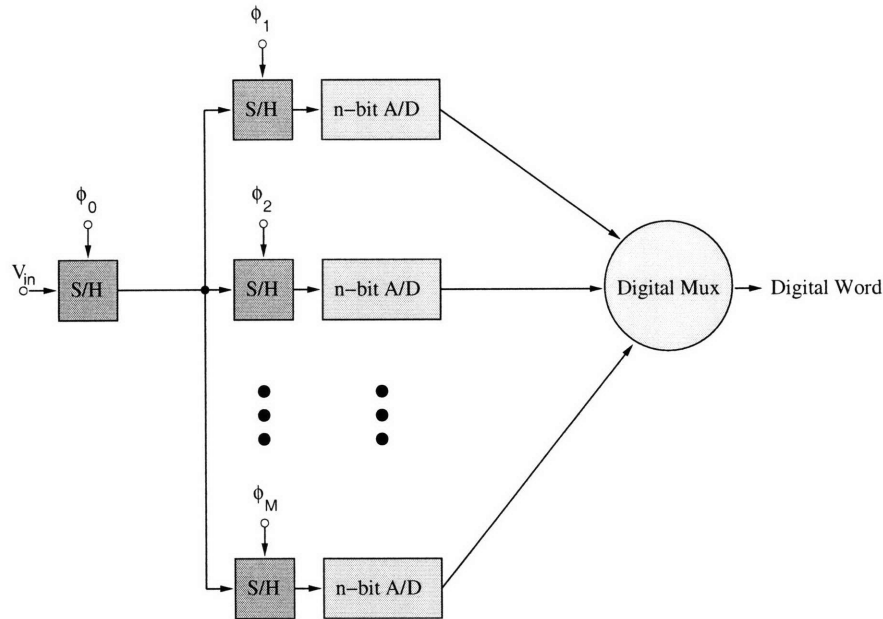
Figure 2-12: An M-channel time-interleaved ADC array [47]

14-bit pipeline ADCs, a continuous background digital calibration for gain, offset, and timing skew errors, and a back-end digital interpolation to cancel timing skew. A time-interleaved converter array achieves high speed analog-to-digital conversion similar to a flash converter but is significantly more area efficient because it does not require 2^n comparators for n-bit conversion [47]. Fig. 2-12 shows the operation of an M-channel time-interleaved ADC [48]. A main sample-and-hold (S/H) circuit samples and holds an input signal V_{in} at rate ϕ_0. The array consists of S/H and n-bit ADC channels 1 through M with clocks ϕ_1 to ϕ_M that use a rate $1/M$ of ϕ_0 and a respective delay to each other equal to the period of ϕ_0. Essentially, each converter gets a successive sample such that effectively it appears as a single converter is operating at rate of ϕ_0. The issues for large channel time-interleaved ADC array are mismatches between ADC channels and clock and signal interconnects. To counter these issues, WiGLAN ADC splits the array into 16 blocks of 8 ADC channels and calibrates per block. Additionally, it uses signals multiplexed onto a single line for each block to reduce signal interconnect and a single master clock with distributed local gating scheme to reduce clock interconnect.

49
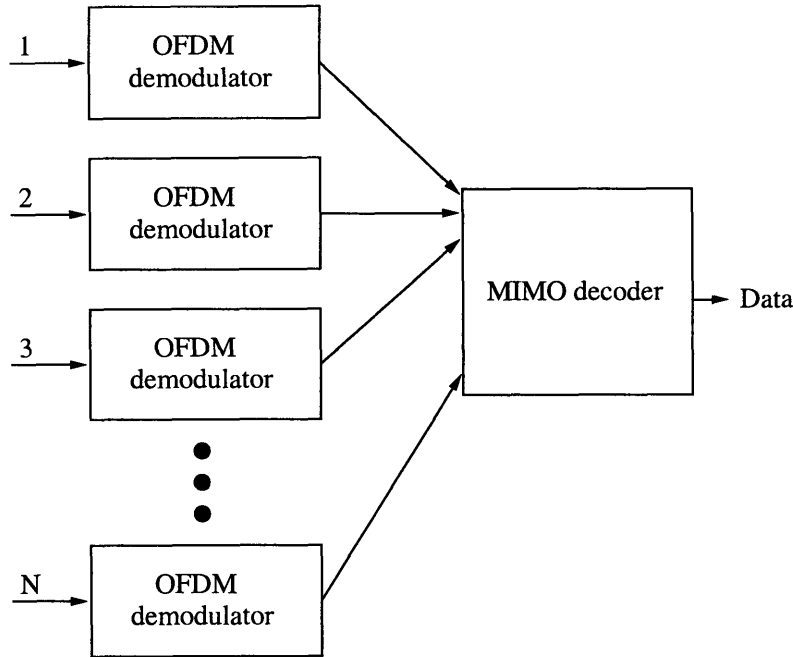
Figure 2-13: Simplified diagram for WiGLAN receive digital processor

2.4 Multiple Antenna Digital Processor

WiGLAN parallel receivers utilize a digital processor that processes multiple OFDM symbols from each antenna and performs SVD for each OFDM subcarrier. Fig. 2-13 shows a simplified block diagram for the digital processor. The processor consists of N OFDM demodulators to support N parallel receivers and a single MIMO decoder that compares outputs from these demodulators and produces an output data stream. The discussions to follow present an overview of OFDM and SVD and conclude with results from [17] that specify bit error rate performance for WiGLAN.

2.4.1 Orthogonal Frequency Division Multiplexing

WiGLAN uses OFDM as a multi-carrier modulation and multiple access technique to accomplish frequency multiplexing and enable adaptive modulation per subcarrier. Dependent upon the rates and quality of service requirements for individual appliances, WiGLAN allocates a number of subcarriers to each appliance. In an OFDM
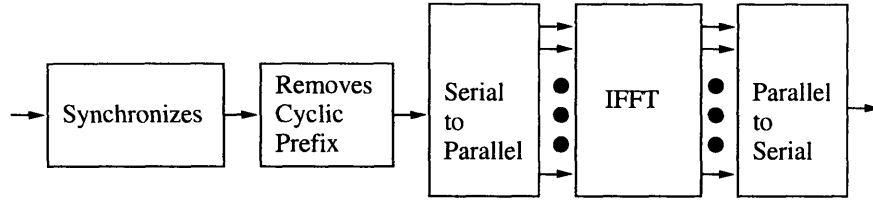
Figure 2-14: An OFDM demodulator

system, a digital signal processor through a Discrete Fourier Transform generates multiple carriers and eliminates the need for multiple carrier generation with analog techniques [49]. The orthogonality of the carriers avoids frequency guardbands and achieves spectral efficiency. However, a time guardband is necessary to maintain orthogonality and shows up in the form of a cyclic prefix that appends the data stream. This guardband is chosen to be larger than the rms delay spread to eliminate intersymbol interference but its use decreases the effective data rates. An off the shelf single-input, single-output (SISO) WiGLAN implementation uses a time guardband that is 25% of the OFDM symbol period [50]. At 1 MHz subcarrier spacings, this gives a 1 μs period and a 250 ns time guardband that represents several times the delay spread of a typical office environment at 40 to 70 ns [49]. For this implementaion, with 128 subcarriers and 256-QAM, the time guardband shrinks the data rate from 1.024 Gb/s to 819.2 Mb/s.

An OFDM demodulator is shown in Fig. 2-14. It takes a serial output from the ADC and performs synchronization for timing and frequency offsets. Afterwards, it removes the cyclic prefix and applies serial to parallel conversion. The set of parallel data streams feed an Inverse Fast Fourier Transform (IFFT) which is an efficient implementation for an Inverse Discrete Fourier Transform. The IFFT extracts the transmit data for each subcarrier and then outputs to a parallel to serial converter that then sends out a serial data stream.

In order to successfully implement OFDM at the receivers, the subcarriers must remain orthogonal. Loss of orthogonality results if the transmitters and receivers do not use exactly the same frequencies [49]. This implies that carrier phase noise and frequency offset degrade orthogonality and produce intercarrier interference (ICI).

Besides selecting a crystal oscillator pair at the transmitter and the receiver that closely match in frequencies [50], an OFDM system uses cyclic extension, training symbols, and pilots to synchronize and maintain orthogonality [49, 50].

2.4.2 Singular Value Decomposition

WiGLAN applies SVD to achieve SNR gain. Since SVD works for any configuration of antennas, it provides system design flexibility. Additionally, it allows immediate packet decoding. This implies less memory usage and computation for WiGLAN digital processor. The following discussion extends results from [12, 16, 51] to decompose a MIMO channel using SVD for one OFDM subcarrier:

A received signal vector $\mathbf{y}$ for OFDM subcarrier k is given as

$$\mathbf{y}(k) = \mathbf{H}(k)\mathbf{x}(k) + \mathbf{w}(k), \tag{2.9}$$

where $\mathbf{x}(k)$ and $\mathbf{w}(k)$ are transmit signal and additive Gaussian noise vectors and channel matrix $\mathbf{H}(k)$ is given as

$$\mathbf{H}(k) = \begin{bmatrix} h_{11}(k) & \cdots & h_{1M}(k) \\ \vdots & \ddots & \vdots \\ h_{N1}(k) & \cdots & h_{NM}(k) \end{bmatrix}. \tag{2.10}$$

A channel response $h_{ij}(k)$ exists between receiver i and transmitter j for OFDM subcarrier k in an M-transmit, N-receiver system.

With SVD, $\mathbf{H}(k)$ decomposes to

$$\mathbf{H}(k) = \mathbf{U}(k)\mathbf{\Lambda}(k)\mathbf{V}^*(k), \tag{2.11}$$

where $\mathbf{U}(k)$ and $\mathbf{V}(k)$ are NxN and MxM unitary matrices, respectively, and $\mathbf{V}^*(k)$ represents the conjugate transpose of $\mathbf{V}(k)$. Columns of $\mathbf{U}(k)$ are eigenvectors of $\mathbf{H}(k)\mathbf{H}^T(k)$ and columns of $\mathbf{V}(k)$ are eigenvectors of $\mathbf{H}^T(k)\mathbf{H}(k)$. NxM diagonal matrix $\mathbf{\Lambda}(k)$ consists of singular values $\lambda_1(k)$ through $\lambda_{n_{min}}(k)$ of $\mathbf{H}(k)$ with $n_{min} =$
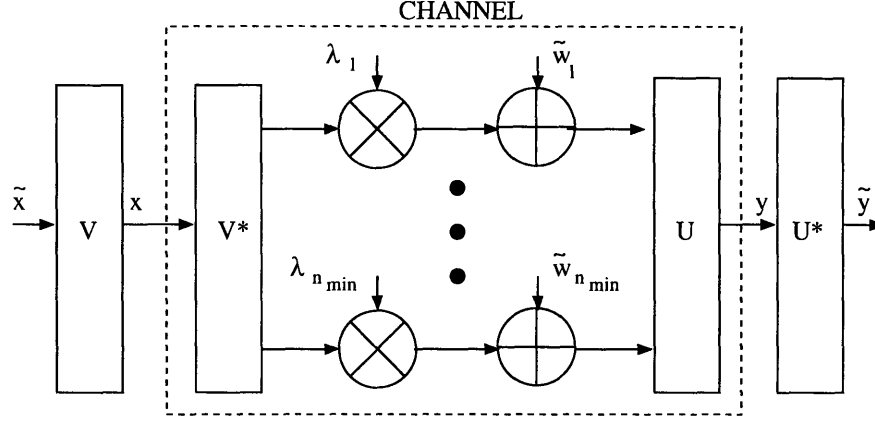
Figure 2-15: Baseband SVD system with parallel subchannels [16]. Noise $\tilde{\mathbf{w}}$ is included in the channel.

$\min(M, N)$. These values are square roots of nonzero eigenvalues of both $\mathbf{H}(k)\mathbf{H}^\mathbf{T}(k)$ and $\mathbf{H}^\mathbf{T}(k)\mathbf{H}(k)$ and represent n_{min} parallel channels. Rewriting $\mathbf{y}(k)$ as $\tilde{\mathbf{y}}(k)$ gives

$$\tilde{\mathbf{y}}(k) = \mathbf{\Lambda}(k)\tilde{\mathbf{x}}(k) + \tilde{\mathbf{w}}(k), \tag{2.12}$$

where

$$\tilde{\mathbf{y}}(k) = \mathbf{U}^*(k)\mathbf{y}(k), \tag{2.13}$$

$$\tilde{\mathbf{x}}(k) = \mathbf{V}^*(k)\mathbf{x}(k), \tag{2.14}$$

$$\tilde{\mathbf{w}}(k) = \mathbf{U}^*(k)\mathbf{w}(k). \tag{2.15}$$

With SVD, a MIMO vector channel becomes parallel, independent scalar subchannels, or eigenmodes, as shown in Fig. 2-15 [16] and given as

$$\tilde{y}_i(k) = \lambda_i(k)\tilde{x}_i(k) + \tilde{w}_i(k), \tag{2.16}$$

for $i = 1 \ldots n_{min}$.

Pre-filter $\mathbf{V}$ for transmit and post-filter $\mathbf{U}$ for receive are necessary to implement SVD. A pre-filter $\mathbf{V}$ requires the transmitter to know the channel. This means that the transmit node knows amplitude and phase response for each OFDM subcarrier [12]. A transmit node can estimate channel state information (CSI) from

the packets it receives from the particular receive node. This is known as implicit feedback and requires a reciprocal channel. However, with MIMO-specific gain and phase mismatches between analog transmitters and receivers, reciprocity suffers and circuit calibration is necessary [52, 53]. Such calibrations are challenges to MIMO transceiver RFIC design [20]. To avoid these issues, WiGLAN receive node measures and sends channel information back to the transmit node. Although this explicit feedback requires additional packets or fields to carry CSI [52], it may be possible to incorporate CSI within the WiGLAN adaptive modulation routine.

Through $\Lambda(k)$, SVD generalizes a maximal ratio combiner. This allows WiGLAN parallel receivers to avoid using analog approaches such as LO phase shifter [22], multi-phase LO and phase selectors [54], and Cartesian combining with invertible variable gain amplifiers [23]. These analog approaches combine signals before the digital processor and thus limit multiple antenna systems to spatial diversity applications. Furthermore, they are applicable for narrowband systems to counter flat fading but not applicable for wide bandwidth systems such as WiGLAN with its frequency selective fading. Most importantly, though, these analog approaches increase complexity for RF circuits and add significant chip area and power consumption. Due to wide bandwidth and a desire to implement a power- and area-efficient design, an analog combiner approach is not suitable for WiGLAN parallel receivers.

2.4.3 Bit Error Rate Performance

Essential inputs to the power dissipation and area consumption models are WiGLAN bit error rate (BER) performances versus SNR. These inputs come from [17] which performs a baseband BER simulation in Matlab. This simulation generates a bit-stream using a pseudo random binary sequence (PRBS) generator as its data source, sends this stream through WiGLAN baseband system and channel models, and compares the output of the demodulator at the receiver with the output of the data source. It calculates BER as the number of error bits received divided by the total number of bits sent. For any NxN system, the simulation repeats the output of the data source through all N transmitters. This BER simulation uses a Monte Carlo analysis

which, for large number of bits, produces a steady state BER. It determines BER for various SNR values by sweeping noise power but fixing signal power. Additional considerations and assumptions for the baseband BER simulation are as follow.

- The indoor channel is rich in scatterers and the number of parallel subchannels is given by n_{min} where n_{min}=min(M,N) for a M-transmit, N-receive antenna system.

- Simulation uses only one OFDM bin and assumes it experiences flat fading. The system data rate is equivalent to data rate for one bin times the number of bins within the bandwidth. In [17], there are 150 bins in 150 MHz bandwidth. An implementation that uses only 128 bins, or has 128 MHz for signal bandwidth and 22 MHz for analog filter roll-off, has lower data rates but does not affect simulation validity.

- Each uncorrelated channel coefficient h_{ij} (as given in section 2.4.2) has Rayleigh distributed amplitude and uniformly distributed phase. This is a normal assumption for wireless systems in a non line-of-sight Rayleigh fading channel.

- Independent fades occur on a per packet basis. This assumption simplifies the simulation or otherwise it becomes intractable to account for different fades within the packet period. Given a certain coherence time, it is certainly possible to choose a packet length that meets this assumption.

Fig. 2-16 plots BER simulation results for a four-transmit, four-receive (4x4) and a single-transmit, single-receive (1x1) antenna system. These systems use 64-QAM modulation and uncoded transmissions. The 4x4 system applies maximum diversity by repeating the same data stream on all four parallel channels. E_S/N_O represents average signal energy over noise variance and is equivalent to SNR when the symbol rate is set to bandwidth. At very low SNR, both systems have high BER because noise dominates the transmission and many decision errors result. In a 1x1 system, a very high SNR is necessary to achieve low BER because deep fades in the channel cause outages. In a 4x4 system, a combination of transmit and receive spatial diversity add
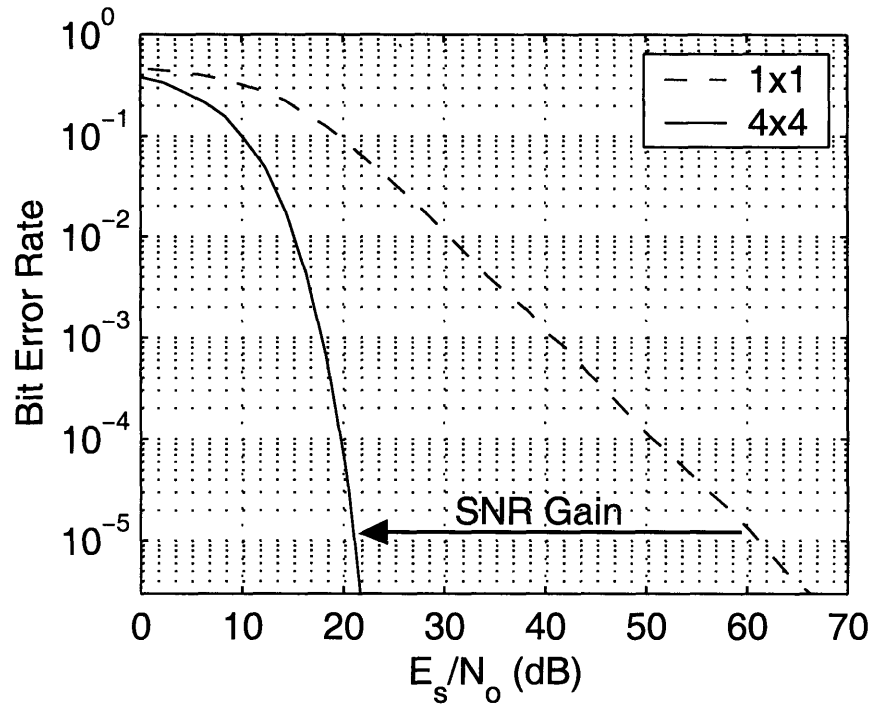
Figure 2-16: Bit error rates versus signal-to-noise ratio in terms of signal energy E_S over noise variance N_O for 1x1 and 4x4 uncoded systems in Rayleigh channel with 64-QAM. 4x4 system uses maximum spatial diversity. SNR gain is the difference in SNR between a 1x1 and any M transmit, N receive (MxN) antenna for a specific bit error rate.

NxN	Rate (Mb/s):		
	1000	900	540
1x1	48.30	45.96	39.26
2x2	31.30	28.89	21.57
3x3	27.62	25.19	17.80
4x4	25.76	23.33	15.90
5x5	24.50	22.07	14.63
6x6	23.51	21.09	13.67
7x7	22.76	20.33	12.85

Table 2.1: E_S/N_O values in dB for BER=10^{-3}, uncoded, and with adaptive modulation [17]

NxN	Rate (Mb/s):		
	1000	900	540
1x1	68.61	66.35	59.99
2x2	37.09	34.68	27.35
3x3	31.06	29.16	21.64
4x4	29.17	26.74	19.27
5x5	27.70	25.25	17.68
6x6	26.70	24.25	16.62
7x7	25.40	23.01	15.74

Table 2.2: E_S/N_O values in dB for BER=10^{-5}, uncoded, and with adaptive modulation [17]

redundancy to the system and lower the outage probability such that a low BER is achievable without high SNR. A comparison of the 4x4 and 1x1 systems at BER=10^{-5} shows that a 4x4 system requires about 40 dB less SNR to achieve the same BER as a 1x1 system. Redefining this difference as a gain, then a 4x4 maximum diversity system with 64-QAM and uncoded transmission has 40 dB SNR gain at BER=10^{-5}. In this thesis, SNR gain is defined as the amount of SNR relaxation a M-transmit, N-receive (MxN) antenna system achieves with spatial diversity over a 1x1 antenna system at the same BER and data rate.

Tables 2.1 and 2.2 list simulated E_S/N_O in dB for NxN antenna systems with BER=10^{-3} and BER=10^{-5}, respectively [17]. The tables present only uncoded transmissions. Coded transmissions are complex to analyze since coding adds overhead and varies with the optimality of the code. Reported data rates result from multi-

plying an adaptive modulation average throughput by bandwidth. As an example, WiGLAN requires an average throughput of 6.67 b/s/Hz to achieve 1 Gb/s with 150 MHz [17]. For 256, 64, 16, and 4-QAM, the rates are 8, 6, 4, and 2 b/s/Hz. Therefore, this average throughput requires either a channel with high SNR or significant SNR gain such that adaptive modulation chooses mostly 256-QAM. The BER simulation uses a normalized average power for each QAM modulation [17] and produces SNR values that consist of an average symbol energy over noise variance. This fits well with the power dissipation model which uses averages in its calculation such as average transmit power and path loss. The tables report SNR values only for NxN systems, that is systems with the number of transmitters set equal to the number of receivers, or M=N. For these systems, parallel radios fully exploit all parallel channels. In all discussions to follow in this thesis, N antennas or transceivers are part of a NxN antenna system.

Fig. 2-17 plots SNR gain using values from the two tables for 540 and 1000 Mb/s data rates. As evident in this figure and the previous Fig. 2-16, lower BER has higher SNR gain values. Specifically, SNR gains at BER=10^{-5} are about 16 dB more than gains at BER=10^{-3} for N>1. The selection of a BER target for WiGLAN is dependent upon the details of the system design. In [17], a multiple antenna WiGLAN operates with 1% packet error for packets with a size of 1000 bits. This gives system bit error rate at 10^{-5}. Implementations [30, 50] use BER at 10^{-3} for their single antenna designs. For multiple antenna systems, it is advantageous to choose lower BER for larger SNR gain since this is where the benefits from multiple antennas become significant. In the chapters to follow, this thesis choose BER=10^{-5}, but it must be noted that the models developed in this thesis are valid and applicable for any BER.

2.5   Summary

This chapter presents a WiGLAN parallel receiver system. It discusses the design for the digital IF receiver, a high speed, massively parallel analog-to-digital converter,

58
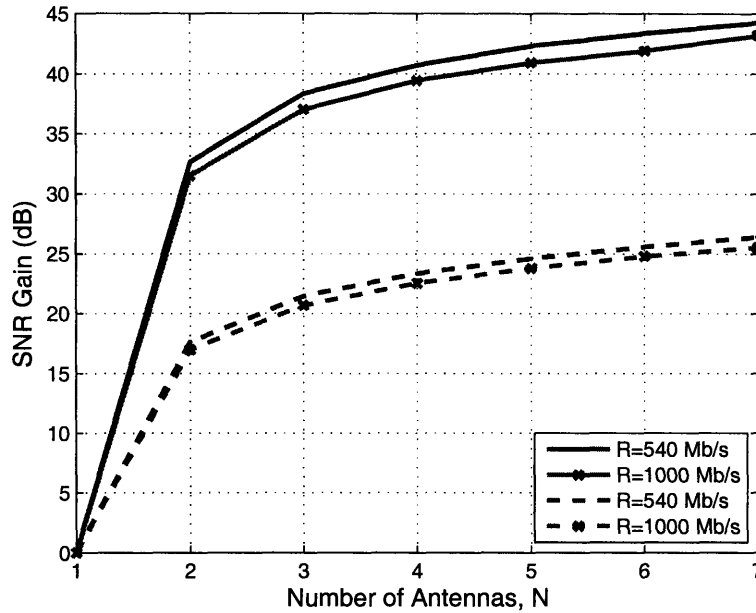
Figure 2-17: SNR gain at BER=10^{-5} (SOLID) and BER=10^{-3} (DASH) for N antennas and data rates 540 and 1000 Mb/s

and a multiple antenna digital signal processor. In moving forward, three major points to keep in mind are:

- WiGLAN uses a digital IF receiver that eliminates IQ mismatch. This receiver incorporates an integrated Q-enhanced image reject notch filter that avoid tradeoffs between RF and IF filters without resorting to direct conversion, double conversion or image reject receivers. Later it will be shown that its first circuit, the low noise amplifier, enables SNR gain application at the receiver.

- WiGLAN uses a very wide bandwidth at 5.22 GHz. It applies OFDM for multi-carrier modulation and multiple access by allocating a variable number of bins per user. OFDM simplifies equalization, achieves spectral efficiency, accomplishes frequency multiplexing, and enables adaptive modulation per subcarrier.

- WiGLAN uses multiple antennas and applies SVD to achieve SNR gain. With SNR gain, WiGLAN achieves very low BER without high SNR. In the chapters to follow, SNR gain is shown to be an integral part of the power dissipation

model. Lower power dissipation and area consumption for parallel transceivers become possible with SNR gain.

Chapter 3

Power Dissipation and Area Consumption Models

This chapter shows how to apply SNR gain to reduce transceiver power dissipation and area consumption. It begins by developing models for a single transceiver and then extends them to parallel transceivers. It incorporates spatial diversity into these models and describes the relations between power dissipation and various system parameters such as distance, receive noise figure, and number of antennas before applying them to reduce transmit signal power, receiver operating power, and receiver chip area. Additionally, this chapter shows that similar models are applicable to parallel radios on a single chip.

3.1 Single Transceiver Models

A single RF transceiver consists of three main sections: local oscillator, transmitter, and receiver as shown in Fig. 3-1. The receiver takes as an input an RF signal from an antenna and filters, amplifies, and frequency translates to either a baseband frequency (homodyne or direct conversion receiver) or intermediate frequency (heterodyne receiver) signal. The transmitter, on the other hand, takes as an input a baseband or intermediate frequency signal and frequency translates to an RF signal, amplifies and filters before it outputs to an antenna. The local oscillator provides a signal to both

61
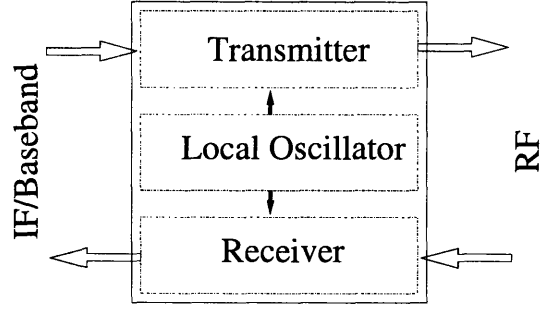
Figure 3-1: Single radio frequency transceiver model.

the receiver and transmitter to allow frequency translation.

An area consumption model for a single transceiver is given by (3.1), where A_{LO}, A_{TX}, and A_{RX} are the area consumption for a local oscillator, transmitter, and receiver, respectively.

$$A_{1,TRX} = A_{LO} + A_{TX} + A_{RX} \tag{3.1}$$

The total transceiver area consumption is simply the summation of the individual area consumptions. The power dissipation model, as given by (3.2) for a single transceiver assumes that the transmitter and receiver operate equally half-time and therefore contribute 50% of its individual power dissipation to the total transceiver power dissipation.

$$P_{1,TRX} = \frac{2P_{LO} + P_{TX} + P_{PA} + P_{RX}}{2} \tag{3.2}$$

In this model, P_{LO}, P_{TX}, P_{RX}, and P_{PA} correspond to the LO, transmitter without power amplifier (PA), receiver, and PA power dissipation. Equal time operation is a valid assumption for the time division duplex WiGLAN system which shares the same frequency band for transmit and receive functions. The local oscillator operates during both functions and therefore contributes all of its power dissipation to the total. The power dissipation for a power amplifier, though part of the transmitter, is considered separately so that, as will be shown later, its power dissipation can be tied directly to RF transmit signal power.

62

3.2 Parallel Transceiver Models

An initial model for parallel transceiver area consumption adapts (3.1) and is given by

$$A_{N,TRX} = A_{LO} + N\left(A_{TX} + A_{RX}\right),\tag{3.3}$$

where the number of transceivers N multiplies areas for the transmitter and receiver sections.[1] Parallel transmitters and receivers are necessary to maintain the channel parallelism on–chip. However, these transceivers share one local oscillator (LO) since parallelism is necessary only along the signal path. Similarly, an initial model for a parallel transceiver power dissipation adapts (3.2) and is given by

$$P_{N,TRX} = P_{LO} + N\left(\frac{P_{TX} + P_{PA}/N + P_{RX}}{2}\right).\tag{3.4}$$

where, again, the number of transceivers N multiplies power dissipation for transmitter and receiver sections but not LO power dissipation. The PA power dissipation is rescaled by $1/N$ in order to keep RF transmit signal power constant for fair comparisons between N parallel transceiver systems. This will become clearer after establishing a relationship between PA power dissipation and RF transmit signal power in the discussions to follow.

One LO for all transceivers instead of one LO per transceiver minimizes area consumption and power dissipation and additionally, for certain closed-loop MIMO systems, improves synchronization [20] and phase noise [55]. Ignoring routing considerations, area consumption and power dissipation for an LO do not increase with the number of antennas. Fig. 3-2 shows a parallel transceiver model. One LO supplies a signal to all transceivers with each transceiver consisting of a transmitter and receiver.

To develop these models, this thesis takes as inputs published chip data from a set of papers [7, 8, 9, 10]. While the models can use any similar published wireless LAN RF transceiver chip data, this particular set fully describes a RF transceiver,

---

[1]Please note that, in this thesis, N represents both the number of transceivers and the number of antennas since there is exactly one transceiver per antenna.
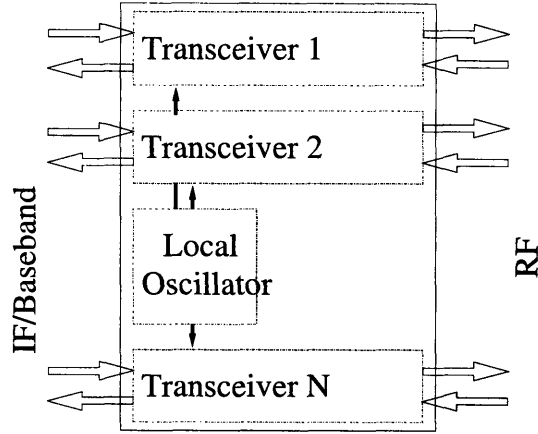
Figure 3-2: Parallel radio frequency transceiver model. Each transceiver consists of a transmitter and a receiver. All transceivers share one LO.

	Area(mm²)	Power(mW)
Transmitter (TX)	4.4	160 (P_{TX}) 627 (P_{PA})
Receiver (RX)	7.1	250
Local Oscillator (LO)	3.1	180

Table 3.1: Wireless LAN RF transceiver active area consumption and reported power dissipation. Values are estimates based on published results for a 802.11a WLAN chipset [7, 8].

baseband processor, and radio chipset that altogether provides a complete picture for one radio system. In the present development for power dissipation and area consumption models, it is the intuition and methodology that is of prime importance and not the exact power or area values. An exact application of these models for WiGLAN appears in Chapter 5 for an area-efficient WiGLAN parallel receiver design.

Table 3.1 lists the approximate area consumption and power dissipation from the published data set for a transmitter, receiver, and LO section. To simplify, the approximation divides published shared logic and bias areas equally among the three sections. The transmit section separates the PA power dissipation from the rest of the transmit electronics. This PA power dissipation is a derived value based on a data comparison between [7, 8]. Fig. 3-3 plots parallel transceiver area consumption as given by (3.3) versus N transceivers using Table 3.1. The figure shows that chip area consumption for parallel transceivers increases with increasing number of transceivers
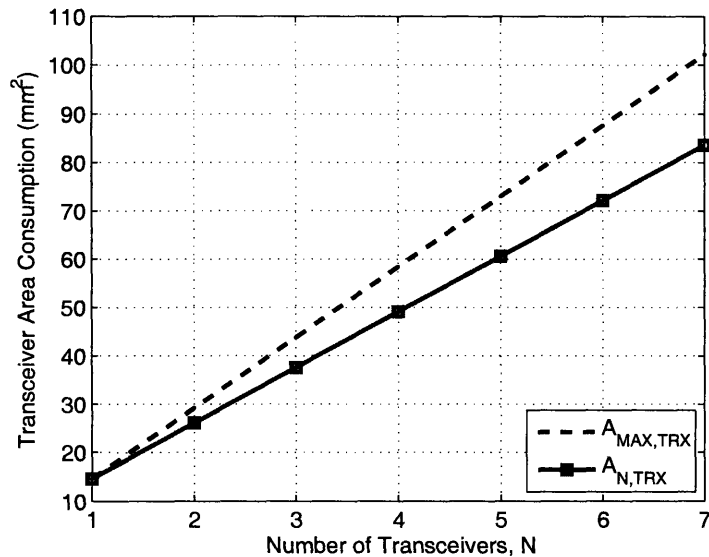
Figure 3-3: Area consumption for parallel transceivers versus number of transceivers N without SNR gain applied. $A_{MAX,TRX}$ represents the situation where the LO is not shared.

but has a slower increase with LO sharing. Fig. 3-4 plots parallel transceiver power dissipation as given by (3.4) versus N transceivers also using Table 3.1. The figure shows that chip power dissipation for parallel transceivers increases with the number of transceivers but by sharing LO and keeping RF transmit signal power constant, the increase is less.

The previous models predict that a direct extension from single transceiver to parallel transceivers increases area consumption and power dissipation as the number of transceivers increases. For example, at N=4, the models predict that the active chip area consumption increases by three and one half times to about 50 mm^2 and total chip power dissipation nearly doubles to 1.3 W. These increases make multiple antenna systems less desirable for low-cost portable applications. According to Table 3.1, the PA power dissipation is more than half the transmitter's power dissipation. Per [7], this is necessary to achieve P_{out}=22 dBm. With multiple antennas, there exists significant SNR gain that can reduce P_{out} and thus transceiver power dissipation.

To incorporate SNR gain, a relationship between SNR and transceiver power
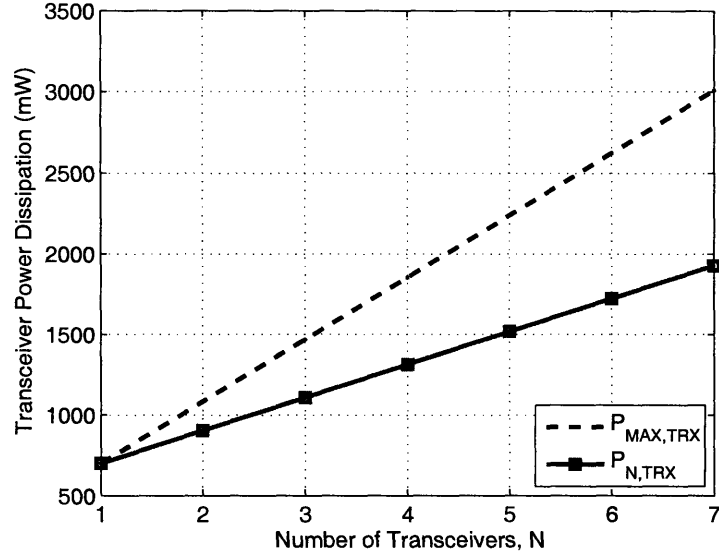
Figure 3-4: Power dissipation for parallel transceivers versus number of transceivers N without SNR gain applied. $P_{MAX,TRX}$ represents the situation where the LO is not shared. For both $P_{N,TRX}$ and $P_{MAX,TRX}$, total RF transmit signal power is kept constant for all N transceiver systems.

dissipation becomes necessary. This comes from relating RF transmit signal power to PA power dissipation as

$$P_{PA} = \frac{P_T}{\eta_{PA}}, \tag{3.5}$$

where P_T, P_{PA}, and η_{PA} are RF transmit signal power, PA power dissipation, and PA power efficiency, respectively. A substitution of (3.5) into (3.4) results in

$$P_{N,TRX} = P_{LO} + N\left(\frac{P_{TX} + P_{RX}}{2}\right) + \frac{P_T}{2\eta_{PA}}, \tag{3.6}$$

that relates power dissipation for parallel transceivers to RF transmit signal power. The RF transmit signal power necessary is given as

$$P_T = LP_R, \tag{3.7}$$

66

where P_R is an input signal to a receiver and path loss L is given by [56]

$$L = \frac{(4\pi)^2 \, (d/d_O)^n}{G_T G_R \lambda^2}. \tag{3.8}$$

Path loss consists of a loss at some fixed distance d_O, for example, at one meter for an indoor environment. This loss comes from either calculations using the free space propagation or measurements. To account for actual receiver distance, the model includes distance variable d and determines the impact of distance through a path loss exponent n, which comes from measurements. Path loss exponent varies from two to five or higher [56]. Using $d_O=1$ m and isotropic antennas (antenna gains G_T $=G_R=1$), distance d, path loss exponent n, and signal wavelength λ fully determine path loss. The receiver's input signal power P_R is given as

$$P_R = F R_S N_O \, (E_S/N_O)_N\,, \tag{3.9}$$

where F represents noise factor and is a unitless ratio of an input SNR to output SNR and $(E_S/N_O)_N$ represents the SNR at a decoder input for a NxN antenna system. Multiplication of $(E_S/N_O)_N$ with noise density N_O and then symbol rate R_S gives average symbol power. Substitution of (3.7), (3.8), and (3.9) into (3.6) gives a parallel transceiver power dissipation model as

$$P_{N,TRX} = P_{LO} + N \frac{(P_{TX} + P_{RX})}{2} + \frac{1}{2\eta_{PA}} \frac{(4\pi)^2 \, (d/d_O)^n}{G_T G_R \lambda^2} F R_S N_O \, (E_S/N_O)_N\,, \tag{3.10}$$

which relates multiple antenna SNR $(E_S/N_O)_N$ for any N transceiver system to transceiver power dissipation $P_{N,TRX}$. For this model, its first term is constant and comes from sharing LO. The second term increases proportionally with the number of transceivers N and represents the additional overhead for using multiple antenna systems. The third term represents power dissipation necessary to generate an RF transmit signal and decreases with N through $(E_S/N_O)_N$. This last term incorporates the power saving benefits from SNR gain.

Variable	Value	Units	Reference
η_{PA}	0.25		[7, 8, 9]
F	6.31		[7]
N_O	4.00e-21	J/Hz	Standard
d_O	1	m	Standard
G_T, G_R	1		WiGLAN
n	3		WiGLAN
λ	5.75	cm	WiGLAN
R_S	150	Msymbols/s	WiGLAN

Table 3.2: Additional model inputs not including $(E_S/N_O)_N$ and previously given transmitter, receiver, and LO power dissipation values

3.3 Observations for Power Dissipation

With a parallel transceiver power dissipation model, it becomes possible to examine relationships between power dissipation and various variables. Indeed, this power dissipation model is a general model and a study that includes, for example, relationships between power dissipation and PA efficiency, carrier frequency, and antenna gains are possible. However, this thesis focuses mainly on the number of transceivers N, receive noise factor F, and transmission distance d because it seeks a general but fundamental behavior for parallel transceiver power dissipation. As will be shown, investigations for N, F, and d sufficiently show the tradeoff between increased power dissipation due to multiple antenna overhead and decreased power dissipation due to SNR gain.

Additionally, limiting the study to an indoor 5-GHz wireless LAN system sets many variables. Table 3.2 lists these variables, their values and sources. PA efficiency η_{PA}, like PA power dissipation, results from comparisons between [7, 8, 9]. A noise factor F at 6.31 represents a noise figure of 8 dB and also comes from [7]. These two values come from the same chip that had provided area consumption and power dissipation for Table 3.1. Noise density N_O and distance d_O take standard values set by a temperature of 290 K and 1 m, respectively. The rest of table applies values from WiGLAN. In particular, it uses isotropic antennas for transmit and receive antennas such that antenna gains $G_T = G_R = 1$ and sets path loss n at 3 to represent a typical
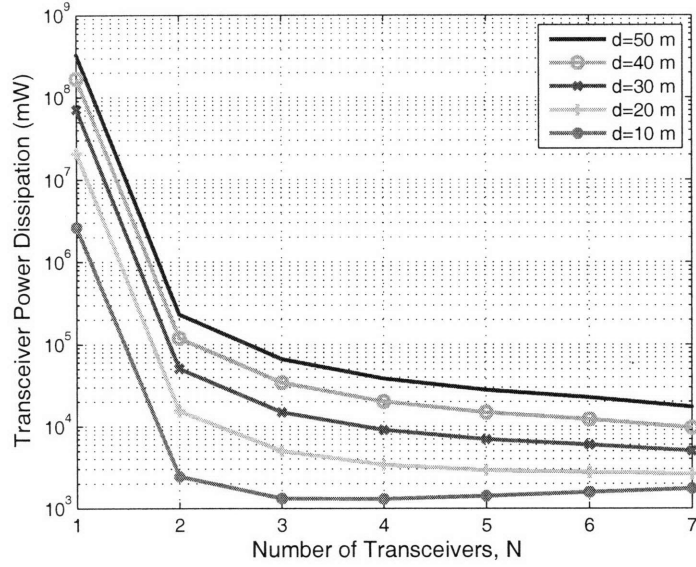
Figure 3-5: Power dissipation for parallel transceivers versus number of transceivers N for various distances and applying SNR gain. NF is kept constant at 8 dB.

indoor environment [17]. A wavelength λ at 5.75 cm implies an operation at 5.22 GHz while symbol rate R_S at 150 Msymbols/s equals frequency bandwidth for WiGLAN. This sets $(E_S/N_O)_N$ to be the receive SNR for N number of transceivers.

3.3.1   Number of Transceivers, N

Using power dissipation values from Tables 3.1, additional model inputs from Table 3.2, and SNR values from Table 2.2, Fig. 3-5 plots parallel transceiver power dissipation as given by (3.10) versus the number of transceivers N at different distances d for 1 Gb/s data rate with 10^{-5} bit error rate.[2] To achieve these rates requires an excessive transceiver power dissipation for a single transceiver system. This is due to a need to generate a large RF transmit signal power to meet SNR requirements at the receiver. Using two transceivers contributes SNR gain and lowers the transceivers' power dissipation by many orders of magnitude. Additional transceivers beyond two further decreases power dissipation but with diminishing returns as higher N provides

---

[2]For all plots in this thesis, the transceiver power dissipation for any N refers to the combined power dissipation for all N parallel transceivers.
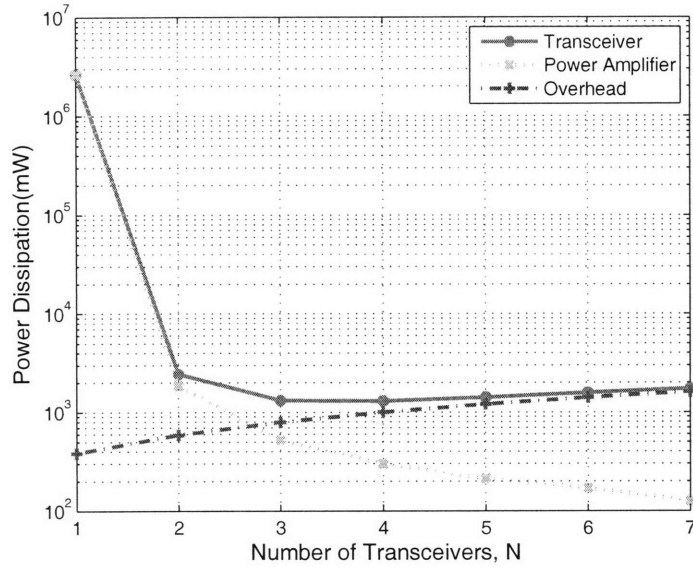
Figure 3-6: Power dissipation for d=10 m. Minimum transceiver power dissipation occurs between N=3 and 4. Further increasing N will increase transceiver power dissipation since overhead power dissipation has become greater than PA power dissipation.

less incremental SNR gain. For long distances, such as d=50 m, where transmit signal power is a major component of a transceiver power dissipation, using additional transceivers translates to lower transceiver power dissipation. To be clear, this says that the combined power dissipation for seven transceivers is less than six transceivers which is then less than five transceivers and so forth. This non-intuitive result implies that using more antennas decreases total transceiver power dissipation and becomes apparent only with the application of the power dissipation model with SNR gain. For short distances, such d=10 m, after reaching a minimum, using additional transceivers increases total transceiver power dissipation. To understand how this is possible, Fig. 3-6 considers the distance d at 10 m and examines how overhead power dissipation, as given by the first two terms of (3.10), and PA power dissipation, the third term, relate to N. As N increases, PA power dissipation decreases due to larger SNR gain but overhead power dissipation increases due to additional transceivers. The minimum transceiver power dissipation occurs when additional overhead power dissipation roughly equals the reduction in PA power dissipation. For d=10 m, an
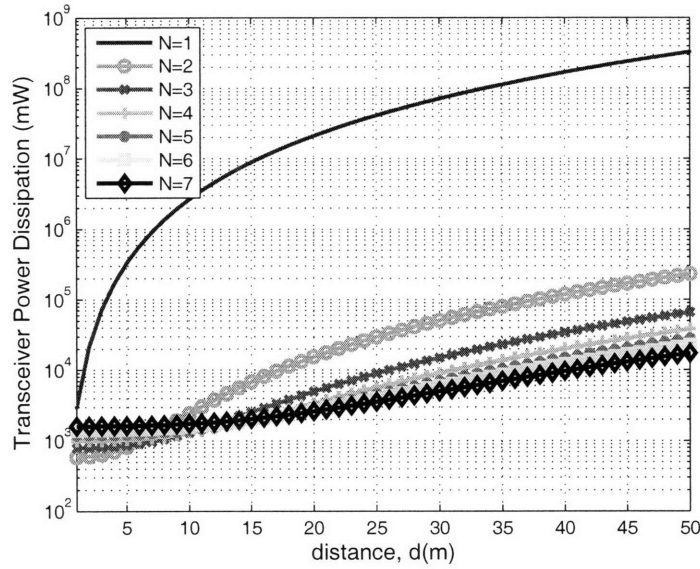
Figure 3-7: Power dissipation for parallel transceiver systems versus distance d. NF is kept constant at 8 dB. A single transceiver system requires excessive transceiver power dissipation to achieve both BER=10^{-5} and 1 Gb/s. Figs. 3-8 and 3-9 provide zoom-in views for this figure.

optimal number of transcievers occurs between N=3 and 4.

3.3.2 Distance, d

The optimal number of transceivers to use for any particular distance can be determined by examining Fig. 3-7 which plots the transceiver power dissipation for 1 through 7 transceivers for BER=10^{-5} and 1 Gb/s. With an excessive transmit signal power requirement, it is evident again that a single transceiver system cannot achieve the desired data and error rates. As an example, given the receivers' -92 dBm input noise power for 150 MHz bandwidth and path loss of 77 dB for d=10 m, a single transceiver requires an overwhelming 251 W RF transmit signal power to achieve its $(E_S/N_O)_1$=69 dB. Comparatively, for the same distance, a two transceiver system requires only 0.16 W transmit signal power to achieve its $(E_S/N_O)_2$=37 dB.

For short distances, or d=1 to 20 m, Fig. 3-8 shows that the bottom envelope gives number of transceivers N that minimizes parallel transceiver power dissipation. As
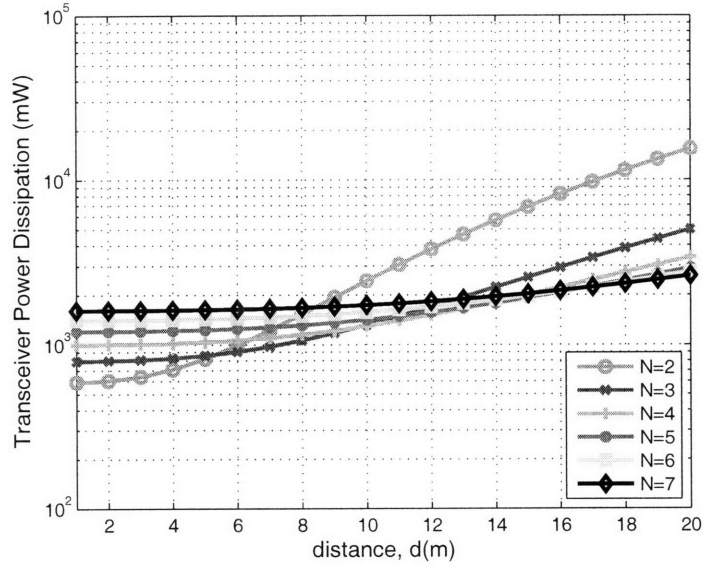
Figure 3-8: Zoom in view no.1: Power dissipation for parallel transceiver systems (except a single transceiver system) at short distances. Bottom envelope of plots gives N transceiver system with lowest power dissipation.

distance increases, minimal power dissipation occurs for larger N. For example, from d=1 to 5 m, a N=2 system provides the lowest parallel transceiver power dissipation while from d=5 to 9 m, it is a N=3 system. For long distances, as shown in Fig. 3-9, the largest system, in this case N=7, provides the lowest parallel transceiver power dissipation. The tradeoff is again a balance between RF transmit signal power and overhead power dissipation. To explain the previous three figures, Fig. 3-10 plots transceiver, overhead and PA power dissipation versus distance d for N=4. Ignoring a single transceiver case, at short distances, overhead power dissipation dominates transceiver power dissipation. As distance increases, more RF transmit signal power is necessary to meet SNR requirements and eventually PA power dissipation dominates transceiver power dissipation. Adding more transceivers will lower parallel transceiver power dissipation at long distances since it lowers RF transmit signal power.
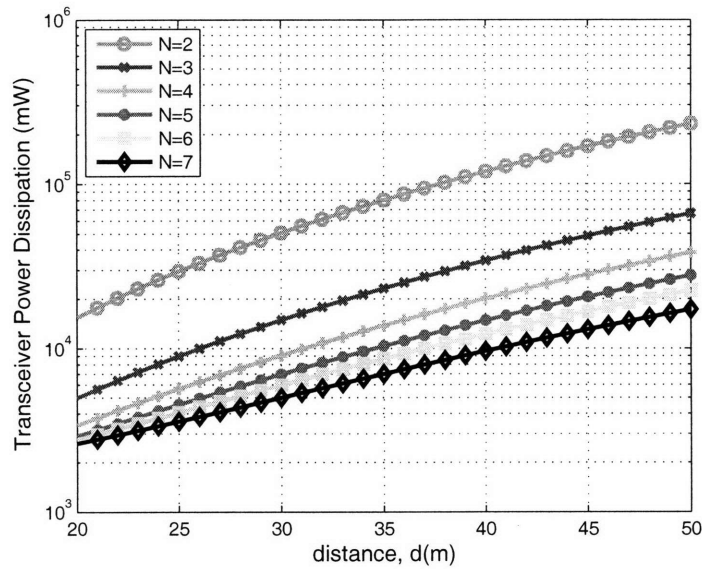
Figure 3-9: Zoom in view no.2: Power dissipation for parallel transceiver systems (except a single transceiver system) at long distances. For long transmission distance, using the largest N possible minimizes power dissipation for parallel transceivers.
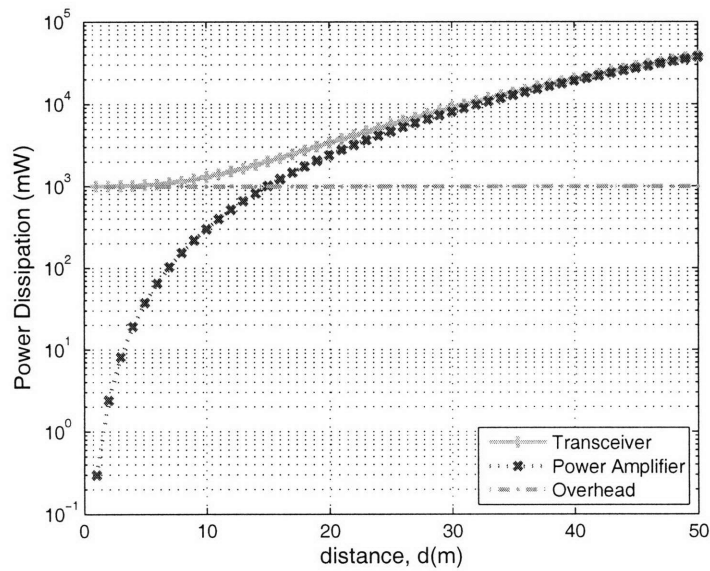
Figure 3-10: Power dissipation for $N=4$ transceivers versus distance d. NF is kept constant at 8 dB. Power dissipation is dominated by overhead electronics at short distances and PA at long distances.
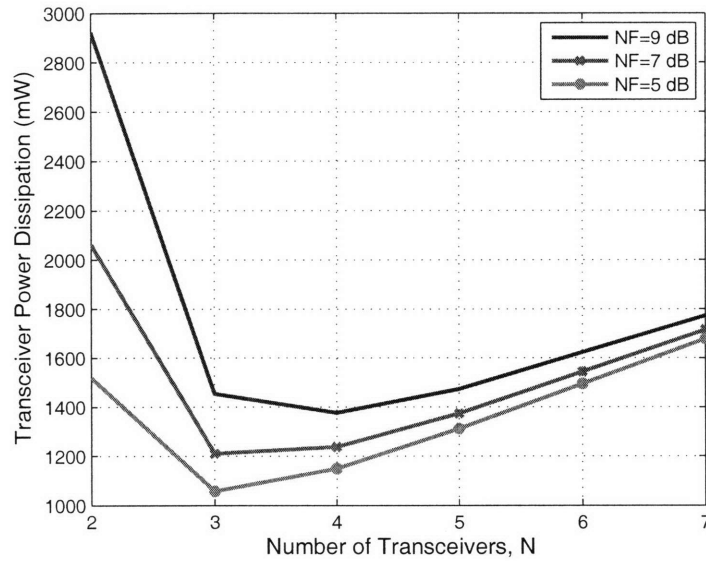
Figure 3-11: Power dissipation for parallel transceivers versus number of transceivers N at various noise figure (NF) values (note: power is plotted on linear scale). Distance d is kept constant at 10 m. Increasing NF increases power dissipation for parallel transceivers and also shifts minimum power dissipation to larger N transceivers. That is, $N=3$ for NF=5 dB shifts to $N=4$ for NF=9 dB.

3.3.3 Noise factor, F

Noise factor for a receiver indirectly indicates how much noise it adds to its output. A receiver system with a large noise factor severely degrades SNR and requires a larger input signal to maintain the same output SNR as a low noise system. With all other factors held constant, this system requires a larger RF transmit signal power and therefore increases transceiver power dissipation. Fig. 3-11 plots parallel transceiver power dissipation for different noise figures (NFs, noise factor in dB units) at $d=20$ m. As NF increases from 5 to 9 dB, the corresponding parallel transceiver power dissipation shifts upwards and in certain situations gives an optimal number of transceivers at larger number of transceivers N as seen for $N=3$ at NF=5 dB and $N=4$ for NF=9 dB. The shift in RF transmit signal power is 1 dB power for every 1 dB increase in noise figure. This is best seen by plotting the RF transmit signal power in dBm, either versus distance as in Fig. 3-12 or versus number of transceivers N as in Fig. 3-13.
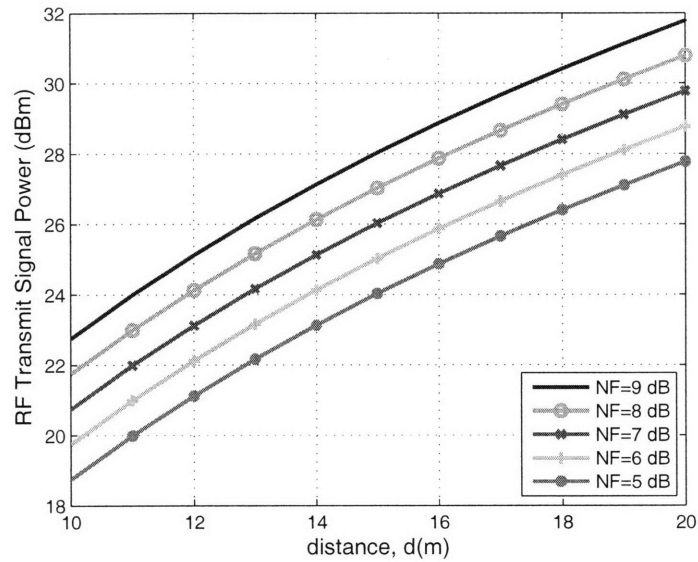
Figure 3-12: RF transmit signal power versus distance d for various NF values. Number of transceivers N is kept constant at 4. Transmit signal power increase 1 dB per 1 dB increase in noise figure.
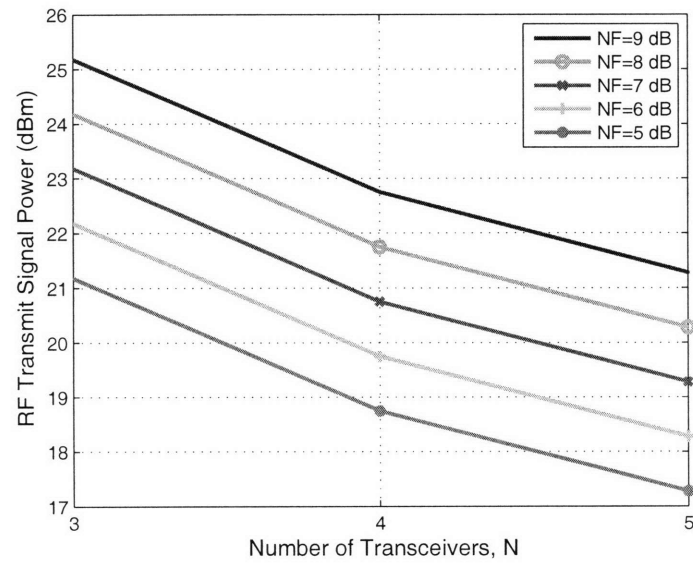
Figure 3-13: RF transmit signal power versus number of transceivers N for various NF values. Distance d is kept constant at 10 m. Transmit signal power increase 1 dB power per 1 dB increase in noise figure.

3.4 SNR Gain Applications

The primary purpose for developing power dissipation and area consumption models is to show how to apply SNR gain to reduce power and area consumption. Therefore, this section presents three applications for SNR gain using these models. A first application examines the balance between dissipation for overhead and RF transmit signal power. It details an optimal number of antennas that sets an upper bound based on transceiver power dissipation. A second application focuses on the situation when RF transmit signal power is small and a reduction in transceiver power dissipation comes from reducing operating power at the receivers. A third and last application shows how SNR gain resolves an area constraint for parallel receivers. In the last two applications, slight modifications to power dissipation and area consumption models are necessary to account for lower receiver operating power and area and a larger noise factor.

3.4.1 Optimal Number of Antennas

Previous observations show that the balance between increasing dissipation due to multiple antenna overhead and decreasing dissipation due to SNR gain gives an optimal number of transceivers. Since there is one transceiver per antenna, this gives an optimal number of antennas. Plots in Figs. 3-6 and 3-10 verify these observations and, through reading the bottom envelopes of Figs. 3-7 through 3-9, Table 3.3 lists an optimal number of transceivers that minimizes power dissipation at any transmission distance. For example, if WiGLAN uses a similar design as [7, 8] to build its parallel transceivers, then it should use four transceivers in a 4x4 system to achieve 1 Gb/s and BER=10^{-5} at transmission distances up to 13 m.

Finding an optimal number of transceivers allows for an efficient use of multiple antennas and is an important result. With an optimal number, it is certain that there is enough antennas to meet a minimum SNR and achieve a specific data and bit error rate and, at the same time, that the overhead to achieve these rates are minimal. A minimum SNR comes built-in with $(E_S/N_O)_N$ which specifies a minimum number of

distance(m)	N
1-5	2
6-9	3
10-13	4
14-16	5
16-17	6
≥ 18	7

Table 3.3: Choosing N to minimize power dissipation for parallel transceivers based on maximum transmission distance for NxN systems and Figs. 3-7, 3-8, and 3-9.

antennas to meet data and bit error rate requirements [17]. It is multiple antenna overhead power dissipation that determines the maximum number of antennas.

Previously, before considerations for overhead power dissipation, [18] sets an optimal number of antennas based on physical constraints for antenna arrays using the size of a wireless device and a propagation channel that incorporates clusters of scatterers. With respect to a wireless device, it shows that packing more and more antennas eventually does not increase the number of parallel channels. Due to an area constraint, antennas spacings would eventually decrease and fades between antennas become correlated. As an example, a wireless device the size of a notebook that operates in a 5-GHz indoor channel has three parallel subchannels and can fit ten antennas at half-wavelength spacings. This shows that, in terms of parallel subchannels, the channel not the device limits a useful number of antennas to three. The constraint on the number of parallel subchannels comes from an assumption that uses a channel consisting of three clusters with 20° cluster solid angles. A slight change in cluster angle to 24° allows support for four parallel subchannels. Invariably, the physical channel also limits the validity for a parallel transceiver power dissipation model as the model uses BER simulation results that assumes a rich scattering channel to achieve SNR gain.

3.4.2 Lower Operation Power

When the transmit signal power does not dominate parallel transceiver power dissipation, relaxing noise requirements at the receivers reduces power dissipation. A new

design-dependent noise factor F_α defines noise factor for a receiver with its operating power reduced through α and given as αP_{RX}. Considering these modifications in (3.10) results in

$$P_{N,TRX} = P_{LO} + N\frac{(P_{TX} + \alpha P_{RX})}{2} + \frac{1}{2\eta_{PA}}\frac{(4\pi)^2 (d/d_O)^n}{G_T G_R \lambda^2} F_\alpha R_S N_O \left(E_S/N_O\right)_N, \quad (3.11)$$

which modifies both the overhead power dissipation and transmit signal power terms. Since lower power operation implies that receiver power dissipation decreases and its noise figure increases, the limits for the new variables are $0 < \alpha \leq 1$ and $F_\alpha \geq F$. Additional noise figure for lower power operation increases the RF transmit signal power, as shown from previous discussions, 1 dB power for every 1 dB increase in noise figure. A decrease in overhead power dissipation due to the receivers is given as

$$\Delta P_{OH} = (N/2)(1 - \alpha) P_{RX}. \quad (3.12)$$

It's important to note that applying SNR gain to offset additional noise due to reducing operating power is applicable only for a parallel transceiver system. A single transceiver has no SNR gain and therefore (3.11) and (3.12) are valid for $N > 1$. Fig. 3-14 plots overhead power dissipation versus number of transceivers N for $\alpha=1$ and 0.5. Since (3.12) is proportional to N, as N increases, the difference in overhead power dissipation between $\alpha=1$ and $\alpha=0.5$ widens. Therefore, relaxing noise figure to lower operating power is most effective with more transceivers. Fig. 3-15 plots parallel transceiver power dissipation versus distance d for $N=4$ transceivers with and without applying SNR gain to reduce receiver operating power. By reducing receiver operating power, parallel transceiver power dissipation is lower at short distances due to lower overhead power dissipation. However, since a larger transmit signal power is necessary to offset an increased noise figure, at long distances where transmit signal power is dominant, reducing receiver operating power hurts parallel transceiver power dissipation. The drawn conclusion is that receivers should not reduce their operating power unless parallel transceiver overhead power dissipation is dominant.
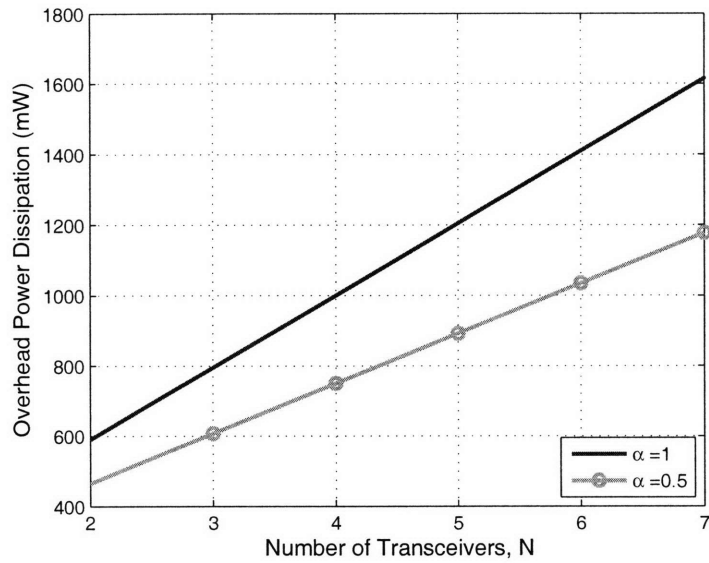
Figure 3-14: Overhead power dissipation for parallel transceivers versus number of transceivers N with α=1 and α=0.5. Reducing receiver operating power is valid for $N > 1$ when there is SNR gain available. Impact for a smaller α on overhead power dissipation increases with more transceivers.
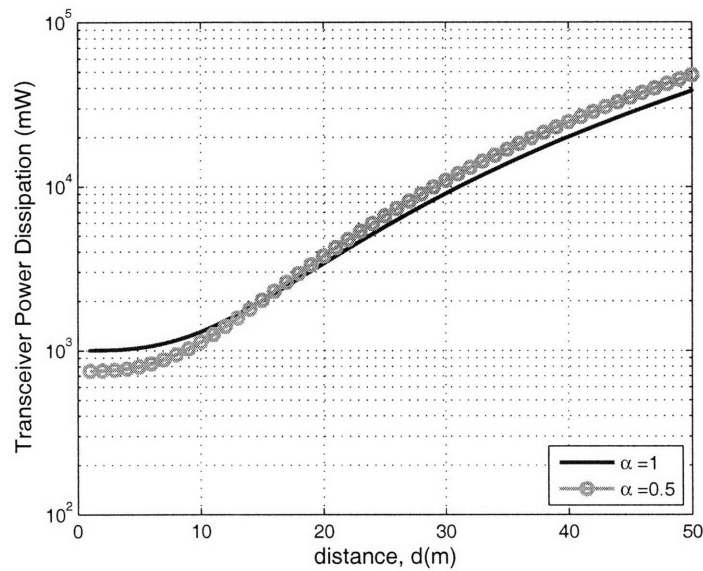
Figure 3-15: Power dissipation for N=4 transceivers versus distance d with α=1 and α=0.5. Corresponding NF values are 8 dB for α=1 and 9 dB for α=0.5. Reducing receiver operating power is best applied when overhead power dissipation is dominant.
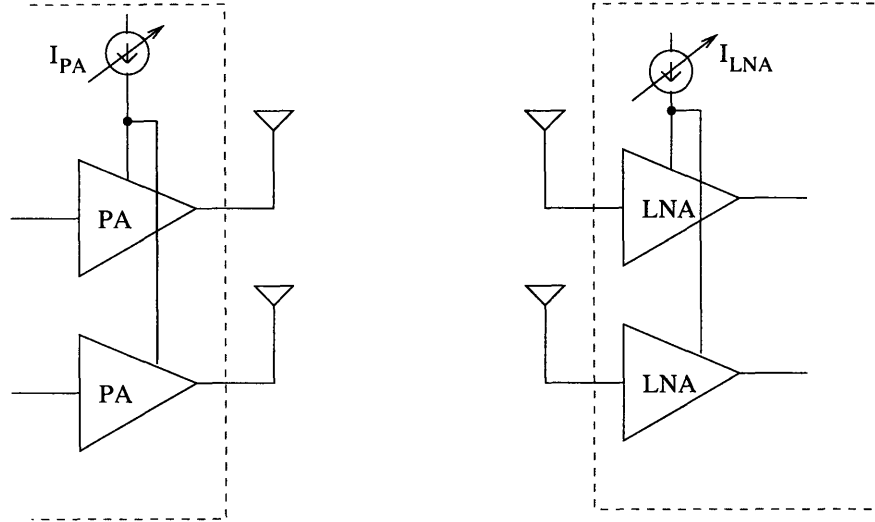
Figure 3-16: A variable power 2x2 system with variability applied to the PAs and LNAs.

To illustrate, Fig. 3-16 shows a variable power 2x2 parallel transceiver system that applies variable current sources I_{PA} and I_{LNA} to vary the power dissipation for the PAs and LNAs. At the system's maximum transmission distance, both the PAs and the LNAs operate at some nominal current values in order to meet the SNR requirements for a 2x2 system at 1 Gb/s data rate and 10^{-5} BER. As the receivers physically move closer to the transmitters, the transmit signal experience less path loss and more signal power is detected at the receiver. Since the noise power at the receivers' inputs is fixed by the bandwidth and unaffected by distance, the SNR at their inputs increases. This provides a margin in necessary SNR that allows the transmitter to lower its RF transmit signal power and as a result the system reduces I_{PA} and lowers power dissipation for the PAs. As the transmission distance between transmitters and receivers becomes small, even lower path loss exists in-between and significant margin in SNR exists that allows the system to tremedously lower RF transmit signal power and effectively reduce PA power dissipation to a minimal value. At this point, further reduction in transceiver power dissipation is possible if the

system also reduces I_{LNA}. As will be shown in Section 4.2, at lower bias currents, a variable power LNA exhibits higher noise figure and exploits the excess margin in SNR.

The adjustments for the currents I_{PA} and I_{LNA} occur at the same rate as the change in transmission distance. A likely scenario is a WiGLAN appliance that is carried by a person walking towards the network controller. The individual's walking speed determines the change in distance. Since WiGLAN measures the channel SNR as part of its adaptive modulation routine, this measurement is also available to adjust the operation power. However, the channel changes on the order of miliseconds while normal walking speed changes distance in seconds. It would be appropriate to average the channel SNR measurements over time to remove the effect of small-scale fading though the averaging period itself must not be longer than the inverse of the walking speed. For example, given a channel coherence time of 25 ms and walking speed at 5 m/s, it would be appropriate to time average 8 measurements.

3.4.3   Area Constraint

When chip area is a major constraint, relaxing noise figure also reduces chip area usage. This relationship will be shown later in Section 4.3. For the moment, assume that there are area-efficient circuits which introduce a higher noise factor F_γ but trade SNR gain to reduce a receiver's area consumption correspondingly by γ. This gives the power dissipation model for parallel transceivers as

$$P_{N,TRX} = P_{LO} + N\frac{(P_{TX} + P_{RX})}{2} + \frac{1}{2\eta_{PA}}\frac{(4\pi)^2 (d/d_O)^n}{G_T G_R \lambda^2} F_\gamma R_S N_O (E_S/N_O)_N. \quad (3.13)$$

A modified area consumption model is given as

$$A_{N,TRX} = A_{LO} + N\left(A_{TX} + \gamma A_{RX}\right), \quad (3.14)$$

where a factor γ reduces a receiver's area consumption. As with reducing operating power, the constraints for F_γ and γ are $F_\gamma \geq F$ and $0 < \gamma \leq 1$, respectively. The shift
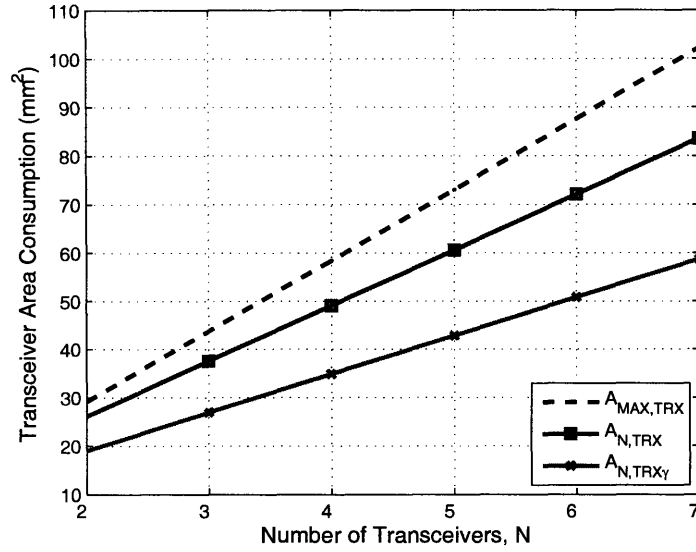
Figure 3-17: Area consumption for parallel transceivers versus number of transceivers N. Trading SNR gain for reduced area consumption is valid for $N > 1$ when there is SNR gain available. $A_{MAX,TRX}$, $A_{N,TRX}$, and $A_{N,TRX\gamma}$ represent area consumption for parallel transceivers with no LO sharing, no SNR gain ($\gamma = 1$), and SNR gain trade for area (arbitrary $\gamma = \frac{3}{8}$), respectively. Unlike power dissipation for parallel transceivers, area consumption for parallel transceivers always increases with additional transceivers.

in transmit signal power due to a larger noise figure is similar to previous discussions. Fig. 3-17 appends a parallel transceiver area consumption with $\gamma = 3/8$ to a graph from Fig. 3-3. Again, for a single transceiver, there is no SNR gain available to lower area consumption so (3.13) and (3.14) are valid for $N > 1$. As N increases, area increases. However, area for a parallel transceiver system that trades SNR gain for area-efficiency increases at a slower rate. Unlike parallel transceiver power dissipation versus number of transceivers N, using more transceivers always increases area consumption. Applying SNR gain only slows the rate of increase.

3.5 Parallel Radio Models

It is possible to extend models for area consumption and power dissipation to a parallel radio system itself. Parallel radio models do not contribute insight into SNR
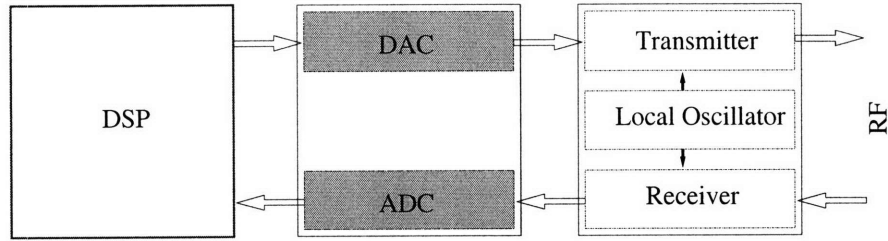
Figure 3-18: A single radio model.
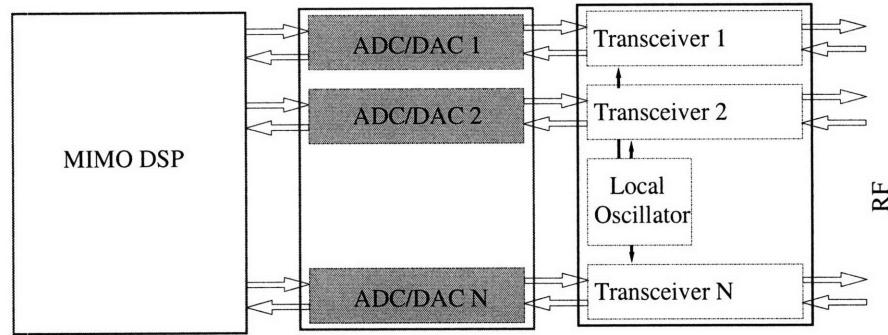
Figure 3-19: Parallel radio model.

gain application as SNR gain itself is built within the parallel transceiver models. Yet these models cast a spotlight on a need to understand how other sections of a single radio system extend to a parallel radio system. In particular, it seems appropriate that analog-to-digital and digital-to-analog converters should increase their power dissipation and area consumption with the number of antennas. It is less clear how power dissipation or area consumption for a digital signal processor changes with the number of antennas. It is very possible that as the number of antennas increases, a DSP uses a different algorithm for each NxN system such that its area consumption and power dissipation is an unknown function of the number of antennas. In this situation, a simplified assumption becomes necessary.

As shown in Fig. 3-18, in addition to the RF transceiver, a single radio system consists of an ADC, digital-to-analog converter (DAC), and a DSP. ADC and DAC are mixed signal circuits that translate signals between their analog and digital representation while a DSP processes these signals only in digital form. Fig. 3-19 shows the model for parallel radios. It consists of parallel transceivers that share one LO,

parallel ADCs and DACs, and a MIMO DSP. To maintain the parallelism in a channel throughout analog processing requires that each transceiver has a respective ADC and DAC. As a result, power dissipation and area consumption for these mixed-signal circuits increase per antenna.

For a MIMO DSP, it is less clear how its power dissipation and area consumption will change with increasing number of antennas. An upper bound suggests that with parallel transceivers, complexity increases by N^2 [18]. This assumption considers processing that went from a scalar channel for a single transceiver system to a matrix channel for N transceiver systems. In comparing a MIMO decoder from Section 2.4 to other decoders for the same data and bit error rate, [17] argues that implementing SVD uses less area and power consumption. This consideration, along with consideration for a multiple antenna processor that uses N parallel OFDM demodulators, suggests that complexity increases by N. In terms of an actual implementation, a 4x4 1900-MHz MIMO WLAN system that uses a field programmable gate array (FPGA) shows that it has a baseband complexity eight times that of current 802.11 modems [12]. This implies a complexity increase by $2N$.

Area consumption and power dissipation models for parallel radios capture the above variations in complexity by defining multiplicative constants for the processor's area and power consumption. An area consumption model for parallel radios is given as

$$A_{N,Radio} = A_{N,TRX} + \epsilon A_{DSP} + N\left(A_{ADC} + A_{DAC}\right), \tag{3.15}$$

where individual areas for ADC, DAC, and MIMO DSP are given by A_{ADC}, A_{DAC}, and A_{DSP}, respectively, and append a parallel transceiver area consumption model $A_{N,TRX}$. Area consumption contributions from ADC and DAC increase with N. Area consumption contribution from a DSP has a multiplicative constant ϵ that varies from slightly above unity for no significant increase to N^2, that is $1 < \epsilon \leq N^2$. A power dissipation model for parallel radios is given as

$$P_{N,Radio} = P_{N,TRX} + \kappa P_{DSP} + N\left(\frac{P_{ADC} + P_{DAC}}{2}\right), \tag{3.16}$$

	Area(mm^2)	Power(mW)
Digital Signal Processor (DSP)	26.5	258 (TX mode)
		241 (RX mode)
Analog-to-Digital Converter (ADC)	2.43	211
Digital-to-Analog Converter (DAC)	2.43	68

Table 3.4: Wireless LAN baseband and MAC processor area consumption and power dissipation. Values are taken from published results for a 802.11 a WLAN chipset [10].

where similar to an area consumption model, power dissipation for ADC, DAC, and DSP are given by P_{ADC}, P_{DAC}, and P_{DSP}, repectively, and append a parallel transceiver power dissipation model $P_{N,TRX}$. Like ϵ, DSP power dissipation contributes to parallel radio power dissipation through a multiplicative constant κ that varies from slightly above unity to N^2, that is $1 < \kappa \leq N^2$.

Table 3.4 lists area consumption and power dissipation values for a baseband processor [10]. This processor corresponds to the RF transceiver previously given in Table 3.1. With this table, Fig. 3-20 plots parallel radio area consumption as given by (3.15) versus N transceivers for ϵ equal to N^2, N, and 1. This corresponds to a quadratic, linear, and constant DSP area consumption, respectively. Similarly, Fig. 3-21 plots parallel radio power dissipation as given by (3.16) versus number of transceivers N for κ equal to N^2, N, and 1. This corresponds to a quadratic, linear, and constant DSP power dissipation, respectively. These two figures for parallel radios are equivalent to Figs. 3-3 and 3-4 which did not apply SNR gain. Increases for DSP area consumption and power dissipation by N^2 produces unacceptably high parallel radio area consumption and power dissipation values and makes this system impractical. At four transceivers, this model shows a parallel radio area of 492 mm^2 and a power dissipation near 6 W. In comparison, at four transceivers, a parallel radio system that uses $\epsilon = \kappa = N$ consumes 175 mm^2 and under 3 W and a system with ϵ and κ set to unity uses 95 mm^2 and a little over 2 W.

To consider SNR gain, Fig. 3-22 plots parallel radio power dissipation as given by (3.16) versus number of transceivers N for various distance d. The figure assumes $\kappa = N$ and applies parallel transceiver power dissipation $P_{N,TRX}$ as given by (3.10) for 1 Gb/s, 10^{-5} BER, and NF=8 dB. Note that, although the baseband processor and
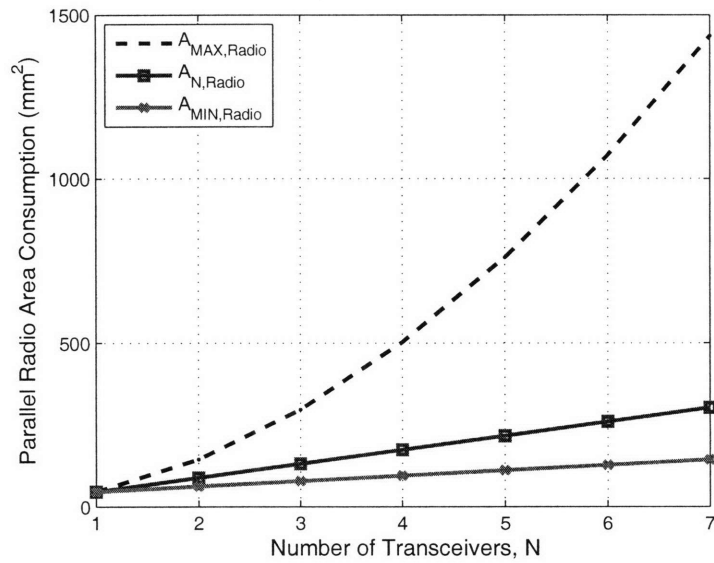
Figure 3-20: Area consumption for parallel radios versus number of transceivers N without SNR gain applied. An increase in area consumption for a DSP is bounded by N^2 ($A_{MAX,Radio}$) and unity ($A_{MIN,Radio}$) but is likely to be closer to N ($A_{N,Radio}$).
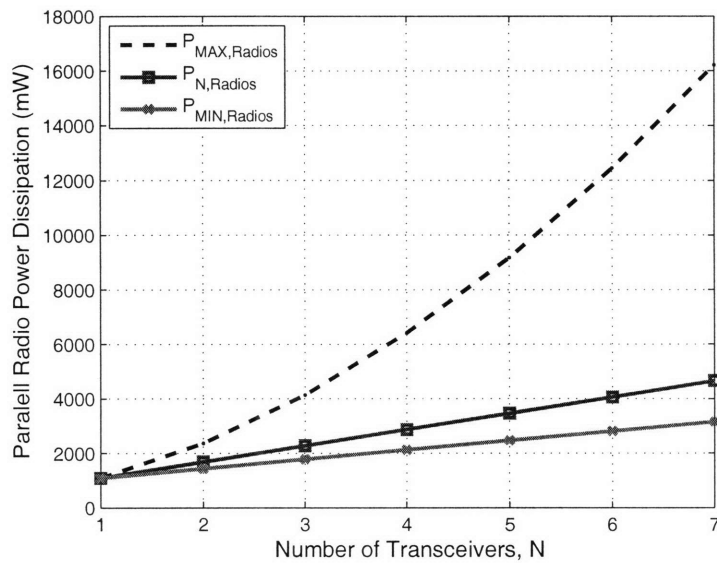
Figure 3-21: Power dissipation for parallel radios versus number of transceivers N without SNR gain applied. An increase in power dissipation for DSP is bounded by N^2 ($P_{MAX,Radio}$) and unity ($P_{MIN,Radio}$) but is likely to be closer to N ($P_{N,Radio}$).
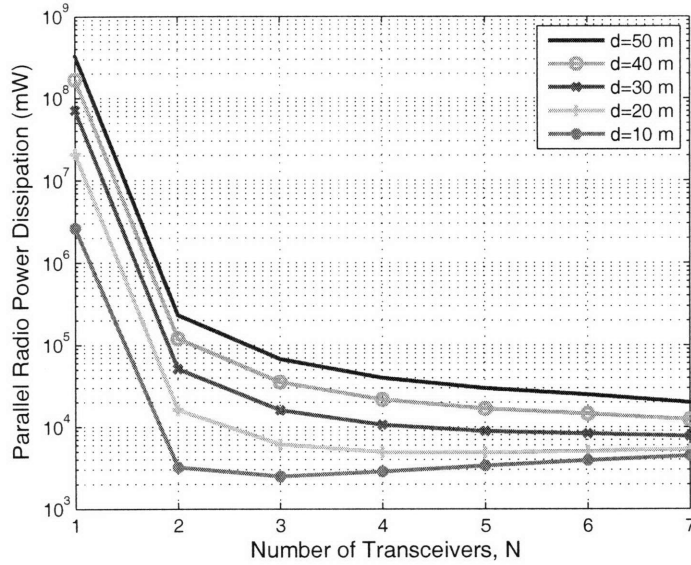
Figure 3-22: Power dissipation for parallel radios versus number of transceivers N for various distances d. Plots assume SNR gain application, $\kappa = N$, and NF=8 dB for 1 Gb/s and 10^{-5} BER.

converters contribute additional overhead, this figure is similar to the plot for parallel transceiver power dissipation as shown in Fig. 3-5 and all the previous discussions on overhead power dissipation, RF transmit signal power, and noise figure are equally valid here for parallel radios as they are for parallel transceivers.

3.6 Coded Transmission

The application of forward error correction, or coding, improves the BER for a multiple antenna system (see Fig. 3-12 of [17]). As an example, a (255,241) Reed-Solomon (RS) code achieves an encoded 10^{-5} BER with an uncoded BER at 10^{-3} while a (255,187) RS code achieves an encoded 10^{-5} with an uncoded BER at 10^{-2}. These RS codes are (n,k) block codes that take k-bit input, append n minus k check bits to enable error detection and correction, and form an n-bit output codeword. The additional check bits provide redundancy in the bitstream that reduces the error probability. Table 3.5 lists the simulated E_S/N_O for multiple antenna systems that apply

NxN	Uncoded	(255,241)
1x1	68.61	50.08
2x2	37.09	33.12
3x3	31.06	29.44
4x4	29.17	27.58
5x5	27.70	26.32
6x6	26.70	25.33
7x7	25.40	24.58

Table 3.5: Simulated E_S/N_O values in dB for uncoded and (255,241) RS code to achieve 1 Gb/s data rate with BER=10^{-5} and applying adaptive modulation [17].

uncoded and (255,241) RS coded transmissions to achieve 10^{-5} BER at an effective 1 Gb/s data rate [17]. The table shows that coding reduces the systems' SNR requirements for any NxN system. The (255,241) RS code reduces the necessary E_S/N_O for a 1x1 system from 68.61 to 50.08 dB. This represents a coding gain of 8.53 dB. However, with more antennas, coding gain decreases so that a 7x7 system with (255,241) RS code has a coding gain of only 0.82 dB when compared to a 7x7 uncoded system. This implies that coding has a greater impact for systems that use fewer number of antennas since, at low BER, using many antennas already produces significant SNR gain.

Fig. 3-23 plots the transceiver power dissipation for parallel transceivers using uncoded and (255,241) RS coded transmissions. At low N, it shows that the application of coding further lowers the transceiver power dissipation beyond the values achieved from using multiple antenna SNR gain alone. Coding lowers SNR requirements as compared to no coding and therefore reduces the necessary transmit signal power. This reduces the dominant PA power dissipation. Similar to previous observations for power dissipation, as N increases, overhead power dissipation for the coded systems becomes significant and dominates total transceiver power dissipation. However, since coding adds more bits, it adds overhead only in the DSP and does not itself produce additional overhead power dissipation within the RF transceivers. With coding, less SNR gain from using multiple antennas is necessary and the optimal number of transceivers shifts to a lower value. The figure shows that, for (255,241) RS coded systems, the optimal number of transceivers occurs at $N=3$ as opposed to
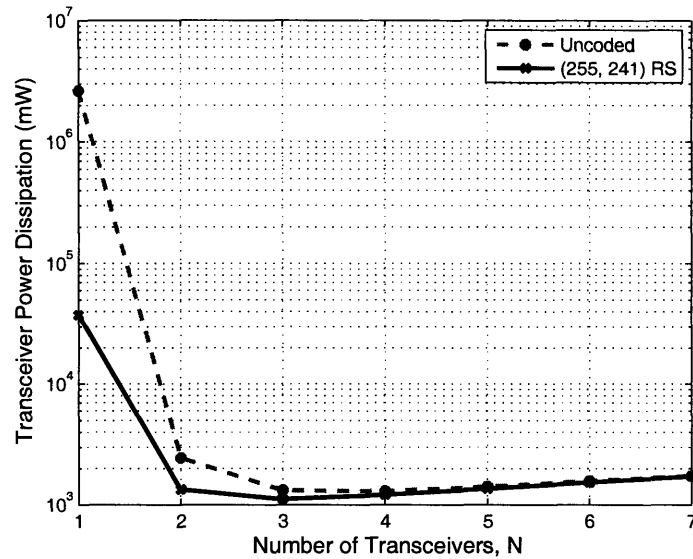
Figure 3-23: Power dissipation for parallel transceivers versus number of transceivers N for uncoded and (255,241) RS coded transmissions. Transmission distance is 10 m. Receivers have 8 dB NF and the systems achieve a 1 Gb/s data rate with 10^{-5} BER.

N=4 for uncoded systems. This suggests the possibility of a single transceiver system that has a large coding gain and therefore it is able to avoid using multiple antennas. This system applies coding to achieve similar SNR gain as would result from using multiple antennas but demands tremendous computation and memory resources and adds significant delay due its usage of codes with very long block lengths [17]. A more practical implementation chooses multiple antennas to achieve significant SNR gain and then applies coding so that the total minimum transceiver power dissipation occurs at a lower number of antennas.

Since coded systems add complexity to the analysis due to the details of the specific codes but do not offer additional insights with respect to SNR gain tradeoffs, the rest of this thesis considers uncoded transmissions. With an uncoded system, SNR gain comes only from using multiple antennas and a tightly coupled relationship exists between the benefits from using multiple antennas and the drawbacks due to its overhead. Certainly, as shown above, the application of coding does impact the transceiver power dissipation but similar to the models for parallel radios, major

model insights inherently come from the balance between SNR gain and overhead and are equally valid for uncoded and coded systems.

3.7 Summary

As this chapter presents many new ideas, it is important to point out the major results before continuing to the next topic on circuits that trade SNR gain. First, it is necessary to recognize that a balance exists between a decrease in parallel transceiver power dissipation due to SNR gain and an increase in power dissipation due to multiple antenna overhead. This balance gives an optimal number of transceivers and it has been shown that an optimum exists for different distances and noise figures. Next, in situations when overhead power dissipation dominates parallel transceiver power dissipation, it is better to apply SNR gain to lower the operating power for a receiver. A lower power receiver has a higher noise figure but increasing an already small RF transmit signal to offset this additional noise figure does not significantly impact overall transceiver power dissipation. Similarly, an area constraint design takes portion of SNR gain to reduce its area consumption but increases its receive noise figure as a consequence. The point to keep in mind here is that discussions for power dissipation or system performance matter little if the design simply does not fit available chip area. Finally, the models can extend beyond transceivers and uncoded systems and shed light on other parts of a parallel radio and on coded systems but, in terms of SNR gain, the major results can be found within the transceiver models for uncoded transmissions.

Chapter 4

Minimal Power and Area Circuits

This chapter presents LNA circuits from the literature that have variable power dissipation or low area consumption but possess relatively high noise figure. These types of circuits enable SNR gain application at the receiver to reduce its power dissipation and area consumption. The chapter defines a variable power LNA as an LNA that varies its operating power. This amplifier uses an external control to vary its bias current [57] or selects amplifier branches with variable power dissipation [58]. At lower operating power, a variable power LNA has higher noise figure. The chapter defines an area-efficient LNA as an LNA that uses on-chip resistors instead of on-chip inductors. The resistors add thermal noise and increase noise figure but save considerable area. The chapter uses a broadband LNA from [46] as an area-efficient LNA.

4.1   Power and Area for a Low Noise Amplifier

An LNA is a critical block within a receiver. It must adequately amplify an input signal for further processing downstream and contribute minimal noise itself. Its input and output impedance must be matched in order to provide proper terminal impedances for the RF and image reject filters. Given that it has sufficient gain, noise figure for an LNA dominates a receiver's noise figure. Therefore, trading SNR gain for relaxed receive noise figure is a tradeoff made essentially with an LNA design.

Power dissipation for an LNA can represent a significant portion of the total

power dissipation for a WLAN RF receiver. As an example, a 5-GHz HIPERLAN RF receiver that consists of an LNA, passive RF mixer, image reject filter, image reject PLL/VCO, and bias circuits has 58% of its power dissipation due to the LNA [44]. Similarly, a direct conversion 5-GHz RF receiver in [59] integrates an LNA, a pair of I/Q downconversion mixers, quadrature VCO, and a set of LO buffers and has power dissipation for an LNA that represents 42% of its power dissipation while a 5.2-GHz 802.11a/HIPERLAN double conversion receiver that includes a baseband has 30% of its power dissipation due to the LNA [60]. These examples show that, in both heterodyne and direct conversion designs, an application of SNR gain to lower LNA power dissipation has the potential to significantly impact power dissipation for a receiver.

In comparison to power dissipation, area consumption for an LNA represents a smaller but still appreciable portion of total area consumption for a WLAN RF receiver. In the reference receivers [44, 59, 60], this author approximates that the LNA consumes roughly one quarter of total active area. However, the story is quite different for on–chip inductors. The double conversion receiver uses two inductors for the LNA but six inductors in total that nearly consume all of its active area [60]. The direct conversion receiver uses six inductors for the LNA but has a total of fourteen inductors that occupies somewhere between 70-80% of the active area [59] while the remaining receiver uses four inductors for the LNA but has eight inductors in total that occupies nearly 70% of the active area [44]. The application of SNR gain to reduce area consumption for an LNA represents one step towards minimal usage for on-chip inductors.

4.2   Variable Power Low Noise Amplifier

A variable power LNA (VPLNA) is an LNA that lowers its power dissipation when there is sufficient SNR gain to offset the additional noise that results. Previously, in Section 3.4.2, it was shown that using two VPLNAs allows a 2x2 system to lower its power dissipation at short transmission distance. To lower its power, a VPLNA can
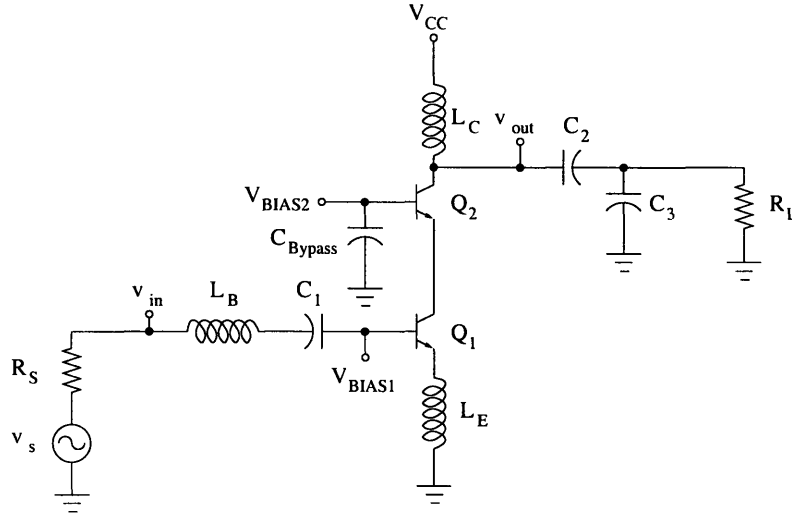
Figure 4-1: Conventional single-ended narrowband cascode low noise amplifier. Input impedance is matched to source impedance R_S and output impedance is matched to load R_L.

lower its operating power or simply use amplifiers that have less power dissipation. As such, the first VPLNA uses a variable current source that changes bias current for the LNA while the second VPLNA has separate amplifier branches. Both VPLNAs are adaptations of a conventional narrowband LNA. In the discussions to follow, the section first reviews a conventional narrowband LNA and then presents a VPLNA that uses variable bias network or an additional amplifier branch.

4.2.1 Narrowband Cascode LNA

Fig. 4-1 shows a single-ended conventional narrowband cascode LNA with its input and output matched to source resistance R_S and load resistance R_L, respectively. A cascode topology allows DC current reuse and therefore saves power consumption. Excellent reverse isolation results from cascode transistor Q_2 providing a low impedance input to driver transistor Q_1. This lowers Q_1's gain and minimizes the Miller effect on its base-collector capacitance.

Assuming a very large C_1, the amplifier's input impedance is given as [61]

$$Z_{in} = j\omega L_B + r_{b1} + \frac{1}{j\omega \left(C_{\pi 1} + 2C_{\mu 1} \right)} + j\omega L_E + \frac{g_m L_E}{\left(C_{\pi 1} + 2C_{\mu 1} \right)}, \quad (4.1)$$

where L_B and L_E are base matching and emitter degeneration inductors, g_m is intrinsic transconductance, and $C_{\pi 1}$, $C_{\mu 1}$, and r_{b1} are Q_1's base-emitter and base-collector capacitances and input base resistance, respectively. Transconductance g_m is given as

$$g_m = \frac{I_C}{V_T}, \quad (4.2)$$

where I_C is collector current and V_T is thermal voltage which is normally taken to be 25-26 mV around room temperature. At low base currents, the same DC current flows through Q_1 and Q_2. This current is equivalent to I_{C1} and I_{C2} so that $g_{m1}=g_{m2}=g_m$. The term $2C_{\mu 1}$ in (4.1) comes from a capacitance across Q_1's base-collector junction and, by Miller effect, is given as

$$C_{MILLER} = \left(1 - A_V \right) C_{\mu 1} = \left(1 + g_{m1} \frac{1}{g_{m2}} \right) C_{\mu 1} = (1 + g_m/g_m)C_{\mu 1} = 2C_{\mu 1}. \quad (4.3)$$

To power match requires a source impedance that equals a complex conjugate of an amplifier's input impedance, that is, $Z_S = Z_{in}^*$. However, since the source impedance is purely real, that is, $Z_S = R_S$, this requires $Re\{Z_{in}\} = R_S$ and $Im\{Z_{in}\} = 0$ and using (4.1) gives

$$R_S = R_{in} = r_{b1} + \frac{g_m L_E}{\left(C_{\pi 1} + 2C_{\mu 1} \right)}, \quad (4.4)$$

$$0 = \omega L_B + \omega L_E + \frac{-1}{\omega \left(C_{\pi 1} + 2C_{\mu 1} \right)}. \quad (4.5)$$

The relationship in (4.5) holds true at resonant frequency ω_O that is given as

$$\omega_O = \frac{1}{\sqrt{\left(L_B + L_E \right) \left(C_{\pi 1} + 2C_{\mu 1} \right)}}, \quad (4.6)$$

94

where all reactances cancel and $Z_{in} = R_{in}$. With (4.4) and (4.6), R_{in} is given as

$$R_{in} = r_{b1} + g_m w_O^2 L_E \left(L_B + L_E \right).$$ (4.7)

Some important points to note here are that input impedance matching is narrowband and centered at ω_O and a reactive component L_E generated a noiseless resistor (second term of (4.4)). Additionally, through g_m, the input impedance match is a function of bias. An input reflection coefficient S_{11} quantifies input impedance match and, in terms of source impedance Z_S and input impedance Z_{in} at resonance, it is given by

$$S_{11} = \frac{Z_{in} - Z_S}{Z_{in} + Z_S} = \frac{R_{in} - R_S}{R_{in} + R_S}$$ (4.8)

With a cascode, transistor Q_2's output impedance is high. Therefore, amplifier output impedance is approximately given by L_C's real impedance as

$$R_{LC} = L_C \omega_O Q_{LC},$$ (4.9)

where Q_{LC} is quality factor for inductor L_C. Tapped-capacitor network $C2$ and $C3$ along with L_C form a matching network to match R_{LC} to load resistor R_L.

A passband transducer power gain G_T is given as [61]

$$G_T \approx g_m^2 \left(\frac{\omega_O L_B}{2R_S} \right)^2 R_S \left(L_C \omega_O Q_{LC} \right).$$ (4.10)

Note that the power gain is proportional to g_m^2. Passband noise factor for this LNA is given as [61]

$$F \approx 1 + \frac{r_{b1} + 2g_m R_S^2 \left(\frac{C_{\pi 1} \omega_O}{g_m} \right)^2 + \frac{g_m}{2\beta_O} \left[\left(R_S + r_{b1} \right)^2 + \left(L_B + L_E \right)^2 \omega_O^2 \right]}{R_S},$$ (4.11)

where β_O is DC current gain.

As an example, an LNA that operates at 5.22 GHz and matches to R_S=50 Ω uses inductors L_B=1.3 nH, L_E=0.25 nH, and L_C=0.96 nH (Q_{LC}=20) and a transis-
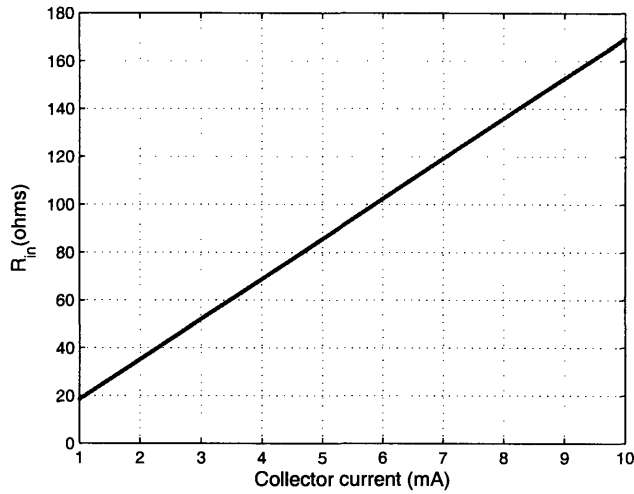
Figure 4-2: Real input impedance R_{in} as a function of collector current for a 5.22-GHz narrowband cascode LNA. Increasing current increases g_m which then increases R_{in}. Input values are L_B=1.31 nH and L_E=0.960 nH for a transistor with r_{b1}=1.69 Ω.

tor Q_1 that has r_{b1}=1.69 Ω, $C_{\pi1}$=588 fF, and β_O=100. Applying expressions given in (4.7), (4.8), (4.10), and (4.11) for 3 mA collector current and at resonance, this LNA has Z_{in}=52 Ω, S_{11}=-34 dB, G_T=19.5 dB, and a noise figure that equals 1.5 dB.

4.2.2 LNA with Variable Bias

At a constant supply voltage, one way to reduce operating power for an LNA is to lower its bias current. As bias current varies, however, input impedance match, gain, and noise figure also vary and it is possible that at some bias values, these parameters no longer meet system requirements. Using an LNA from the previous example, Fig. 4-2 plots the real input impedance R_{in} as given by (4.7) versus collector current. This plot and the next set of plots to follow assume that collector current approximates bias current. This is true for low base current. The plot shows that sweeping collector current from 1 mA to 10 mA gives R_{in} that increases linearly from 20 Ω to approximately 170 Ω. To match to R_S=50 Ω requires collector current I_C to be approximately 2.9 mA. To quantify the input impedance match, Fig. 4-3 plots S_{11} at resonance as given by (4.8) versus collector current. The figure shows S_{11} in
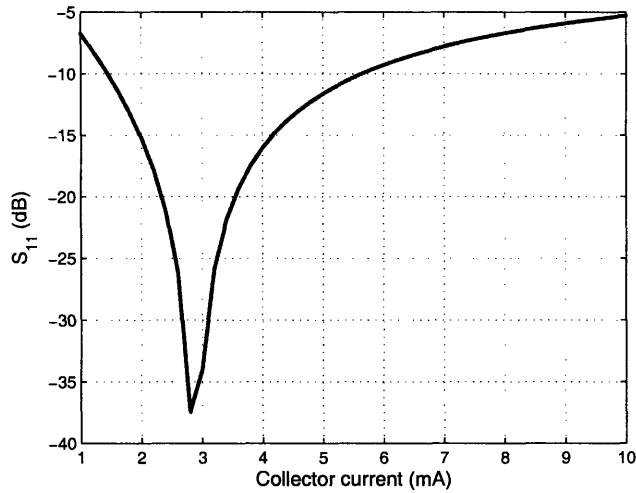
Figure 4-3: S_{11} as a function of collector current for a 5.22-GHz narrowband cascode LNA with R_S=50 Ω. Plot assumes an input impedance match at resonance such that S_{11} consists only of R_S and R_{in}. To keep S_{11} less than -10 dB limits collector current values to between 1.4 and 5.6 mA.

decibels which is given as $(S_{11})_{dB} = 20log_{10}S_{11}$. As R_{in} approaches R_S, S_{11} gets closer to zero and its decibel equivalent dips towards infinity. The plot stops short near -40 dB simply due to its collector current step size which was set at 0.1 mA. Low values for S_{11} indicate a good match as they imply that the input absorbs all the signal power and very little signal reflects back to the source. In general, a typical LNA specification for S_{11} requires it be less than -10 dB. This limits the present LNA to operate between 1.4 to 5.6 mA.

Fig. 4-4 plots transducer power gain using (4.10) in decibel versus collector current. As current increases, G_T increases through g_m^2 and gives a quadratic relationship between power gain and bias current. The limits set by input impedance match constrain gain to be between 12 to 25 dB. Fig. 4-5 plots noise figure using (4.11) versus collector current. At small collector currents, collector shot noise, which is represented by the second numerator term in (4.11), dominates noise figure due to a small gain. Graphically, this is shown by a decrease in noise figure as collector current increases beyond 1 mA. At high collector currents, base shot noise, which is represented by a third numerator term of (4.11), dominates and increases with
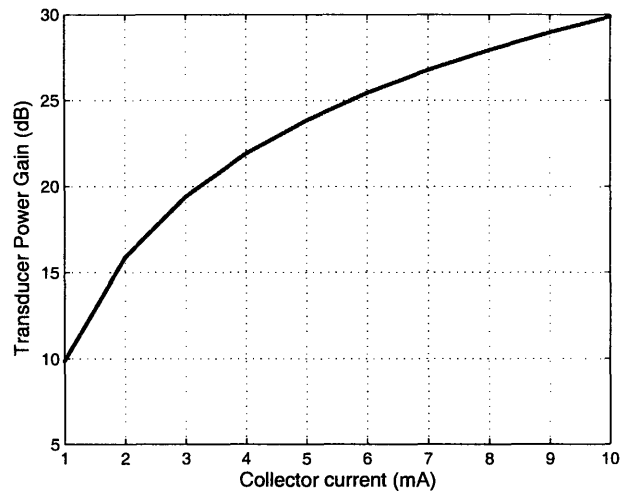
Figure 4-4: Narrowband cascode LNA's transducer power gain versus collector current. Increasing current increases g_m which then increases gain. Design values are as follow: $L_B = 1.31$ nH and L_C=0.960 nH with Q_{LC}=20. Source impedance R_S is taken to be 50 Ω and operation frequency is at 5.22 GHz.
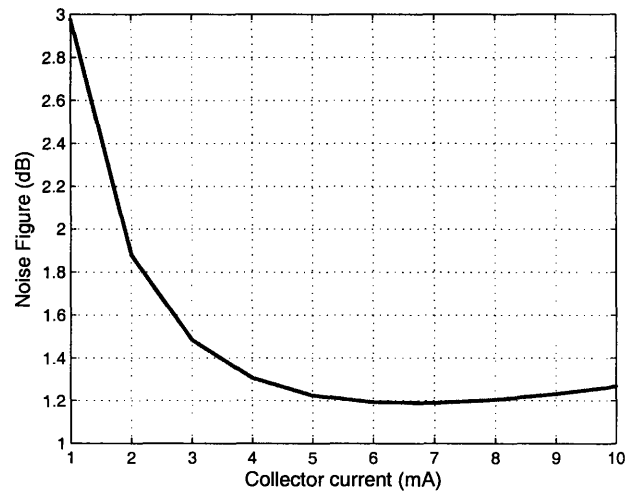
Figure 4-5: Narrowband cascode LNA's noise figure versus collector current. Collector shot noises increases noise figure at low current while base shot noise increases noise figure at high current. In addition to values given for G_T plot, transistor parameters r_b is 1.69 Ω, $C_{\pi 1}$ is 588 fF, β_O is 100. To match input, emitter inductor L_E is 0.25 nH.
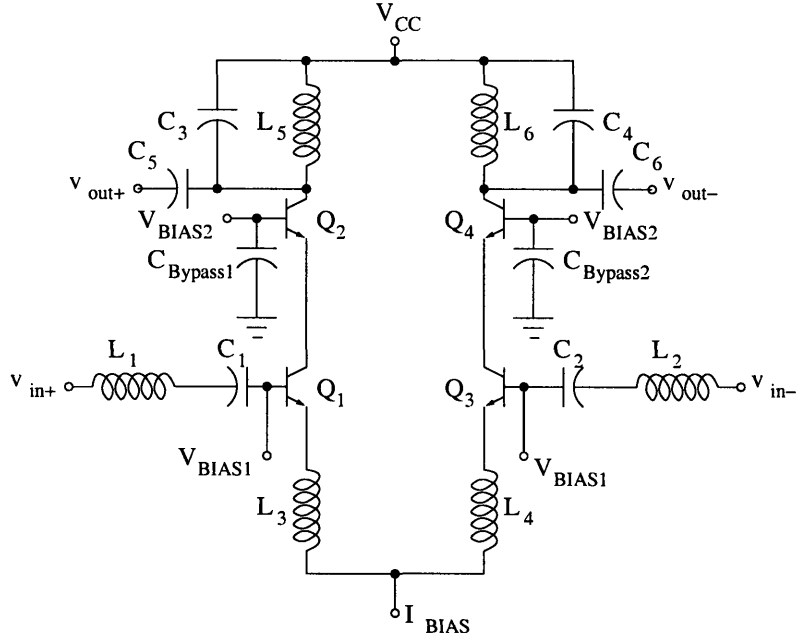
Figure 4-6: Differential cascode narrowband low noise amplifier with input control current I_{BIAS} [57]. Lowering I_{BIAS} lowers amplifier's power consumption but increases noise figure.

increasing current. This balance produces a minimum which for this LNA occurs at 1.2 dB near 6 mA. This current is slightly beyond the limits set by input impedance match. Noise figure for collector current values from 1.4 to 5.6 mA goes from 2.4 dB to slightly above 1.2 dB. It is possible to shift the minimum noise figure to a lower current but, to do so, $C_{\pi 1}$ in the second term of (4.11) must decrease. Using less transistor stripes for a bipolar transistor lowers $C_{\pi 1}$ but increases r_{b1} and additionally changes input impedance match [61]. While, in theory, it is certainly possible to power and noise match the input, discrete values for input inductors L_B and L_E set by geometry limit practical realizations.

Given the previous discussions, Fig. 4-6 shows one possible VLPNA design. It is a differential version for a coventional narrowband cascode LNA with an additional input I_{BIAS} that sets its bias current. This circuit is the bipolar equivalent for the CMOS LNA that is given in [57]. At small base currents, the sum of collector currents through Q_1 and Q_3 approximates I_{BIAS}. If this VPLNA initially operates at a
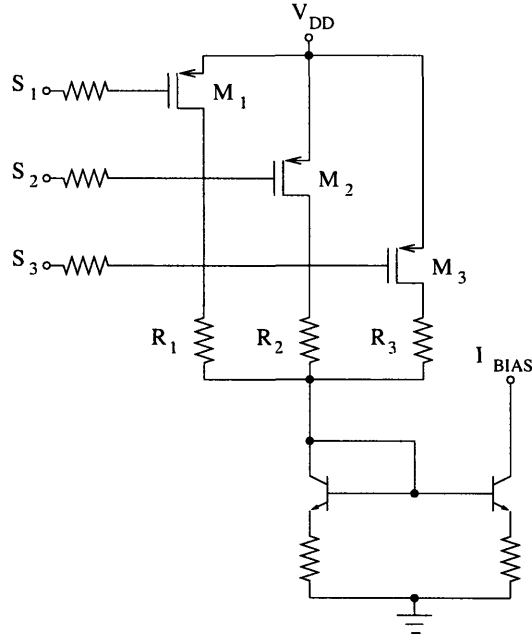
Figure 4-7: Externally programmable bias current network [57]. Three-bit control S_1, S_2, S_3 selects a desired combination of resistors R_1, R_2, and R_3 to set the reference current.

minimum noise figure point as shown in Fig. 4-5, lowering I_{BIAS} increases its noise figure and decreases its gain. Lowering I_{BIAS} improves the input impedance match as R_{in} approaches R_S at first but degrades as current is further reduced.

To use this LNA requires an externally programmable bias network that provides an input control current. Such a network is shown in Fig. 4-7 [57]. It uses three control bits S_1, S_2, and S_3 to achieve eight different values for power dissipation. The network is a current source with a variable reference resistance. Depending on the control bits, resistors R_1, R_2, and R_3 switch in and establish a particular resistance that then sets the reference current. Table 4.1 lists reported simulation results for bias current, gain, and noise figure for a 5.2-GHz CMOS LNA that incorporated this network [57]. Shutting off all three PMOS switches M_1, M_2 and M_3 shuts the current source down and puts the amplifier in sleep mode. Noise figure increases from 2.1 to 3.3 dB as current decreases from 8.0 mA to 3.4 mA while gain, for this range, decreases from 15.0 to 13.0 dB.

3-bit control	I_{BIAS}(mA)	NF(dB)	Gain(dB)
111	0	sleep	sleep
110	3.4	3.3	13.0
101	5.8	2.2	14.3
100	8.0	2.1	15.0
011	9.0	2.1	15.5
010	10	2.1	16.0
001	12	2.2	16.2
000	13	2.3	16.5

Table 4.1: Simulated values of bias current, noise figure, gain, and input for a 5.2-GHz differential CMOS LNA with all possible combinations of control bits S_1, S_2, and S_3 [57]

4.2.3   LNA with Multiple Branches

A convential narrowband cascode LNA has an optimal noise figure at one particular current density. As a result, at other bias currents, noise figure increases. A design that optimizes at each power dissipation is shown in Fig. 4-8 [58]. It uses one output configuration but two amplifier branches. A high gain branch is a conventional narrowband cascode LNA that consists of transistors Q_1 and Q_2 and degeneration inductor L_E. Its input impedance is previously given by (4.1). A low gain branch uses transistors Q_3 and Q_4, resistors R_1 and R_2, and capacitors C_1 and C_m. The input impedance for the low gain branch is given as

$$Z_{inLG} = j\omega L_B + \frac{1}{j\omega C_1} + R_1 + \frac{1}{j\omega \left(C_{\pi3} + C_M \right)}, \qquad (4.12)$$

where r_{b3} has been ignored, L_B is the inductor shared by both branches, and Miller capacitance C_M is given as

$$C_M = (1 + g_{m3}R_2) C_m. \qquad (4.13)$$

To input impedance match both branches to R_S requires that the real impedance be set as

$$R_S = \frac{g_{m1}L_E}{(C_{\pi1} + 2C_{\mu1})} = R_1, \qquad (4.14)$$

101
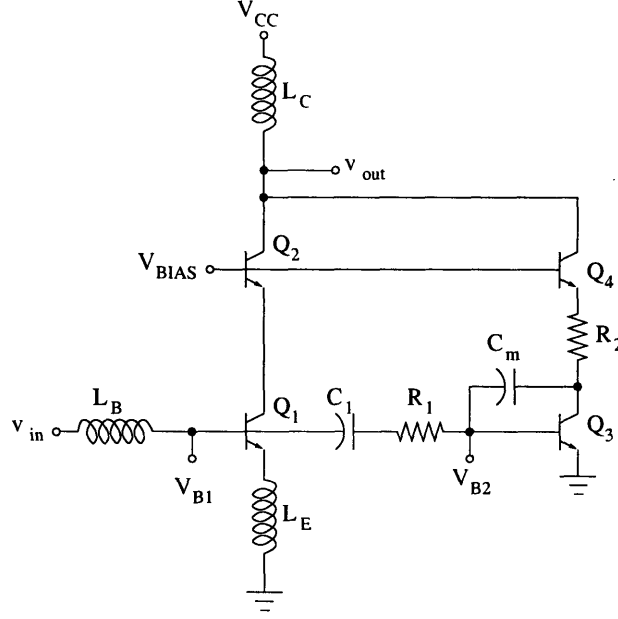
Figure 4-8: VPLNA with low and high gain branches [58]. Applying either VB1 or VB2 selects either branch for use.

where negligible base resistances r_{b1} and r_{b3} have been ignored such that degeneration inductor L_E in the high gain branch and resistor R_1 in the low gain branch match the respective input impedance for each branch. R_1 also attenuates large input signals for the low gain branch and saves silicon area by eliminating an input impedance matching degeneration inductor. However, it is in series with Q_3 and contributes noise directly to the amplifier [58]. Capacitor C_m, which can be set comparatively larger than $C_{\mu3}$, linearizes Q_3. Resistor R_2 establishes voltage gain for Q_3 and help sets C_M through (4.13).

Similar to (4.5) with $Im\{Z_{in}\}=0$, the imaginary impedance is given by

$$0 = \omega L_B + \omega L_E + \frac{-1}{\omega\left(C_{\pi1} + 2C_{\mu1}\right)} = \omega L_B + \frac{-1}{\omega C_1} + \frac{-1}{\omega\left(C_{\pi3} + C_M\right)}. \qquad (4.15)$$

Cancelling L_B on both sides and multiplying by -1 give

$$\frac{1}{\omega\left(C_{\pi1} + 2C_{\mu1}\right)} - \omega L_E = \frac{1}{\omega C_1} + \frac{1}{\omega\left(C_{\pi3} + C_M\right)}. \qquad (4.16)$$

102

Branch	I_{CC}(mA)	NF(dB)	Gain(dB)	S11(dB)
High Gain	3.0	3.5	16.3	< -10
Low Gain	2.0	8.3	5.8	< -12

Table 4.2: Reported measurement results for current consumption, noise figure, gain, and S_{11} at high and low gain branches [58]

Applying either V_{B1} or V_{B2} selects either branch for use. An off-state branch does load an on-state branch. However, capacitance C_1 reduces loading of a high gain branch by a low gain branch while a combination of small transistors Q_1 and Q_3 and $R_1 > R_S$ minimizes the impact of loading on the low gain branch from the high gain branch [58]. Table 4.2 shows reported measurement results for a 5-GHz LNA that has two branches [58]. Reducing current consumption by 50% from 3 to 2 mA increases noise figure by about 5 dB and decreases gain by a little over 10 dB. Input impedance match, in terms of an input S-parameter S_{11}, is less than -10 dB for both branches.

4.3 Area-efficient Low Noise Amplifier

An area-efficient LNA design is shown in Fig. 4-9. This LNA is the differential version of a single-ended broadband amplifier that is given by [46]. It is a shunt-series amplifier with an additional cascode transistors Q_3 and Q_4 to improve frequency response and more importantly provide a low impedance load for a Q-enhanced notch filter [41]. An area-efficient LNA achieves its area-efficiency by not using on-chip inductors. To appreciate this characteristic, Fig. 4-10 shows physical sizes for typical on-chip active and passive devices for a 5-GHz LNA. An on–chip 1 nH spiral inductor consumes three hundred times the size of a bipolar transistor with emitter area of 3.05 μm^2 and one hundred times the size of a 100 Ω polysilicon resistor. An area-efficient LNA performs all the functions of an LNA as discussed in Section 4.2.1 that include providing sufficient gain and input and output impedance match and contributing minimal noise. Although with multiple antenna systems, SNR gain relaxes the last requirement.

As shown in Fig. 4-9, shunt-series feedback resistors R_{F1} and R_{F2} provide input
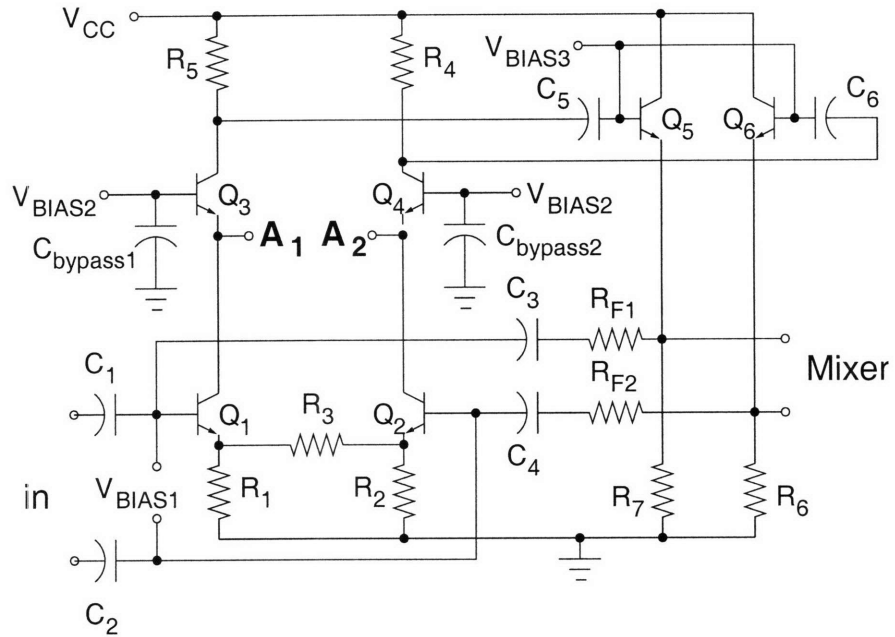
Figure 4-9: Area-efficient low noise amplifier. LNA is an area-efficient shunt-series amplifier with additional cascode and buffer circuits. Resistors R_{F1} and R_{F2} provide input impedance matching.

Dual Metal–Insulator–Metal
Capacitor, 1 pF (10.8)

Polysilicon Resistor,
100 Ω (3.6)

Bipolar Transistor, Ae = 3.05 sq um (1)

NMOS Transistor, W/L = 200/0.54 (1.3)

Octagonal Spiral Inductor, 1 nH (333)
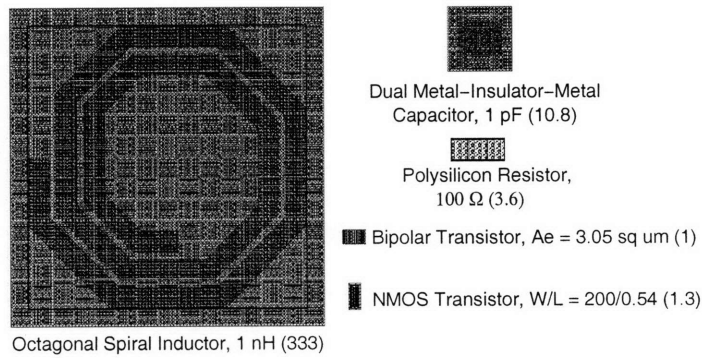
Figure 4-10: On-chip passive and active components. The sizes in parentheses are relative to the shown bipolar transistor that has an emitter area of 3.05 μm and occupies 172 μm^2 of chip area.

impedance matching to 50 Ω while resistors R_1 and R_2 set the bias currents through the cascode amplifier. To set bias current and apply series feedback, or emitter degeneration, separately, this author uses an additional resistor R_3 that ties to the emitters of driver transistors Q_1 and Q_2 and effectively lowers the resistances seen by the emitters. The approximate input resistance for the half circuit is given as [46]

$$R_{in} \approx R_{F1} / \frac{R_5}{R_{E1} + 1/g_m}, \qquad (4.17)$$

where resistor R_5 sets the unloaded output voltage swing for the cascode amplifier and R_{E1} is given as

$$R_{E1} = R_1 || \frac{R_3}{2}. \qquad (4.18)$$

An emitter follower voltage buffer prevents loading the amplifier's output. It consists of transistors Q_5 and Q_6 and resistors R_6 and R_7 to set its current. With this buffer, the half circuit voltage gain for the LNA is given as [46]

$$A_V = \frac{R_5}{R_{E1} + 1/g_m} A_{EF}, \qquad (4.19)$$

where A_{EF} is the voltage gain for the emitter follower and is typically near unity. Comparing (4.17) with (4.19) shows that the input resistance is approximated as the feedback resistor divided by the gain of the amplifier.

Noise figure for the area-efficient LNA is dominated by the shunt feedback resistors R_{F1} and R_{F2} and series feedback resistors R_1, R_2, and R_3. The shunt feedback resistors contribute a noise current power that is given as

$$\overline{i_{R_F}^2} = \frac{4kT\Delta f}{R_F}, \qquad (4.20)$$

where R_F represents R_{F1} or R_{F2} and k, T, and Δf are Boltzmann's constant at 1.38×10^{-23} J/K, temperature at 290 K, and frequency bandwidth, respectively. The series feedback resistors contribute a noise voltage power that is given as

$$\overline{v_{R_E}^2} = 4kTR_E\Delta f, \qquad (4.21)$$

105

Parameter	Narrowband	Area-Efficient
NF(dB)	1.4	4.5
Area(mm^2)	0.6	0.23
Power Dissipation (mW)	10.3	19
Power Gain, G_P(dB)	13	12.2
S_{11}(dB)	<-10	<-10

Table 4.3: Simulated results for differential narrowband and area-efficient LNA

where R_E represents R_{E1} or R_{E2} with $R_{E2} = R_2||\frac{R_3}{2}$. These expressions indicate that using larger shunt feedback resistors R_{F1} and R_{F2} and smaller series feedback resistors R_1, R_2, and R_3 reduces their noise contribution. However, as given in (4.17), as R_{F1} increases, more gain is necessary to maintain R_{in}. Similarly, as the resistances at the emitter decrease, more collector current is necessary to maintain the same voltage at the emitter node. Both situations increase power dissipation and lead to a design tradeoff between resistor noise and LNA power dissipation.

This area-efficient LNA design does not necessarily need to be broadband and uses capacitors C_1 and C_2 at its input to set a low frequency cutoff for the amplifier's frequency response. This attenuates unncessary low frequency gain and also helps minimize input noise power. Capacitors C_3-C_6 provide DC blocking between driver and buffer stages while common base cascode transistors Q_3 and Q_4 require bypass capacitors $C_{bypass1}$ and $C_{bypass2}$. Not shown are individual simple resistor divider networks that generate voltages V_{BIAS1}, V_{BIAS2}, and V_{BIAS3} to bias the bases for common emitter, cascode, and buffer circuits, respectively. Terminals A_1 and A_2 provide a connection for a Q-enhanced image reject notch filter (to be discussed in Chapter 5).

Table 4.3 compares the simulated results between a 5.22-GHz differential narrowband LNA that was shown in Fig. 4-6 and the area-efficient LNA. This author designed and simulated these circuits using a 0.18μm SiGe BiCMOS process and SpectreRF, respectively. The area-efficient LNA has a simulated noise figure that is about 3 dB higher than the narrowband LNA but occupies a chip area that is about one-third the estimated area necessary to implement the narrowband LNA. This lower area consumption comes from the elimination of six on-chip inductors. The area-efficient

LNA consumes 19 mW DC power with most of the power dissipation from the emitter follower that consumes 11 mW. High power dissipation at the buffer is necessary to provide a low impedance output to drive the mixer's transconductor. The area-efficient LNA has a simulated gain that is similar to that of the narrowband LNA and an input S_{11} that is below -10 dB. Chapter 5 considers these two LNA circuits for parallel receiver implementations and provides additional results.

4.4 Summary

This chapter defines a variable power LNA and an area-efficient LNA as circuits that enable SNR gain application at the receiver to reduce its power dissipation and area consumption, respectively. It presents circuits from the literature that support these definitions. A variable power LNA uses either a lower bias current or lower power amplifier branch to lower its power dissipation. An area-efficient LNA uses on–chip resistors instead of on–chip inductors to reduce its area consumption. Both circuits contribute more noise and require a small portion of available SNR gain as compensation.

To consider how much SNR gain is necessary to offset the higher noise figure for the LNA, it is necessary to consider not only the gain and noise figure of the LNA but also the noise figure of the electronics that follow it in the receiver. This is similarly true for receiver power dissipation and area consumption as the impact from a variable power LNA and an area-efficient LNA depends on the power dissipation and area consumption from the other circuits in a receiver (see section 4.1). The next chapter discusses these other circuits that make it possible to determine necessary SNR gain and the percent power dissipation and area consumption for the LNA.

Chapter 5

An Area-Efficient 5.22-GHz Parallel Receiver RFIC

This chapter presents the first multiple antenna parallel receiver RFIC that has been optimized for area consumption. This area-efficient 5.22-GHz parallel receiver test chip implements four parallel WiGLAN digital IF receivers. Each receiver consists of area-efficient low noise amplifier, mixer, and local oscillator amplifier, uses a Q-enhanced image reject notch filter, and shares a global local oscillator amplifier and bias and control signals. The design and implementation of these receivers illustrate the application of previously developed models, SNR gain, and area-efficient circuits.

5.1 Single WiGLAN Receiver

A single WiGLAN parallel receiver is shown in Fig. 5-1. It is a digital IF receiver that consists of a low noise amplifier (LNA), Q-enhanced image reject notch filter, mixer, and local oscillator (LO) amplifier. The receiver first amplifies a radio frequency (RF) signal at 5.22 GHz using an LNA. It then down converts the signal to an intermediate frequency (IF) at 580 MHz. At this frequency, it is possible to replace inductor-capacitor (LC) pass band filtering with resistor-capacitor (RC) low pass filtering at the mixer's output to minimize its area. With a low side LO signal frequency at 4.64 GHz, the image is at 4.06 GHz where only a weak satellite downlink signal exists.
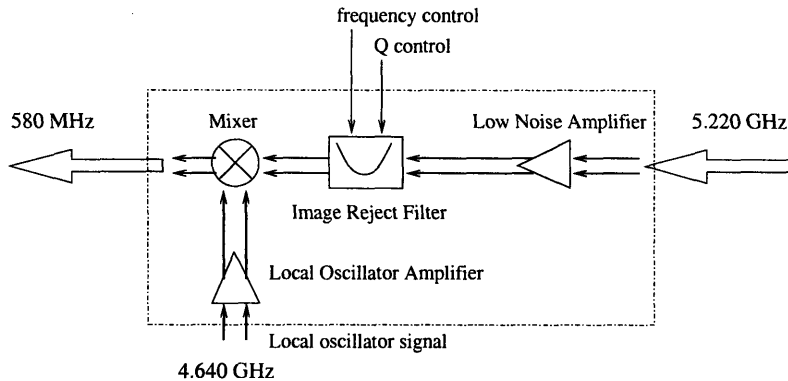
Figure 5-1: A single WiGLAN RF receiver. Differential receiver consists of an LNA, Q-enhanced image reject filter, mixer, and local oscillator amplifier. Integrated filter requires both frequency and Q tuning control signals to set its center frequency and rejection.

This allows the usage of a minimal order Q-enhanced LC notch filter before the mixer to perform image rejection. A low order LC filter minimizes the number of resonators and thus minimizes area for the filter. The receiver also requires two input control signals to set center frequency and rejection for the integrated filter and is differential in order to reject common mode noise. The following sections discuss the notch filter, mixer, and LO amplifier circuits. A discussion for the differential area-efficient LNA was previously given in Section 4.3.

5.1.1   Q-enhanced Notch Filter

An integrated Q-enhanced image reject LC notch filter has become popular recently as a high rejection and more stable alternative to a Q-enhanced band pass filter [44], [62],and [63]. For the same order, a notch filter has a faster roll-off than a band pass filter. This translates to a minimum number of LC resonators and a smaller area necessary to perform filtering. However, a Q-enhanced notch filter is tuned to completely cancel resonator losses and must use an LNA's emitter (or source for MOS designs) as a load for stability. By inserting the filter in-between cascode and driver transistors for an LNA, a filter is loaded by an emitter of a cascode. Therefore a cascode design is necessary for most LNAs that utilize a Q-enhanced LC notch filter. For designs that do not use a cascode specifically with this filter type, area-inefficient

110
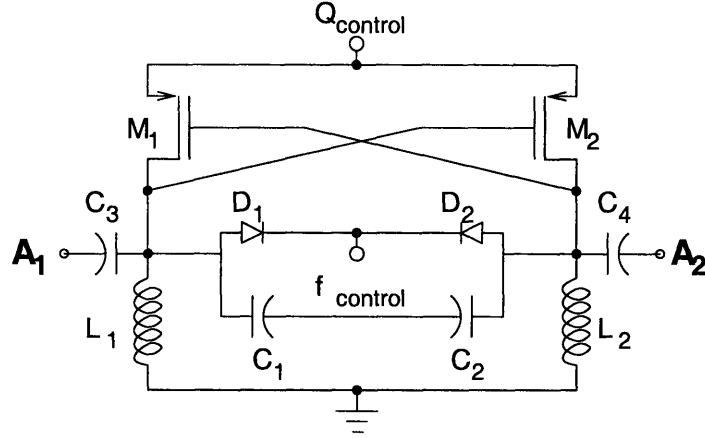
Figure 5-2: 3rd order Q-enhanced image reject notch filter

inductive transformers couple the filter to an LNA [63]. A third order Q-enhanced LC notch filter is shown in Fig. 5-2. It consists of cross-coupled PMOS transistors M_1 and M_2 that generate the negative conductance and voltage variable capacitors D_1 and D_2, capacitors C_1-C_4, and inductors L_1 and L_2 that altogether set the filter's center frequency. The filter exists between points A_1 and A_2 of an area-efficient LNA (see Fig. 4-9) and requires control signal inputs $Q_{control}$ and $f_{control}$.

To understand how the notch filter rejects the image frequency but leaves the desired RF signal unaffected, half of the first stage of the LNA with a filter equivalent circuit is redrawn in Fig. 5-3. Looking into the notch filter, the filter's impedance is given as

$$Z_F = \frac{1}{j\omega C_3} + \frac{1}{j\omega C_T}||j\omega L_1||R_{eff},\qquad(5.1)$$

where

$$R_{eff} = R_p||\frac{-1}{g_{m_{PMOS}}} = \frac{-R_p/g_{m_{PMOS}}}{R_p - \frac{1}{g_{m_{PMOS}}}},\qquad(5.2)$$

and

$$C_T = C_1 + C_{D1}.\qquad(5.3)$$

R_p represents losses of L_1 and C_T. Negative-G_m generator produces $\frac{-1}{g_{m_{PMOS}}}$ and C_{D_1} is effective capacitance for varactor D_1. After expansion and some manipulations, Z_F

111
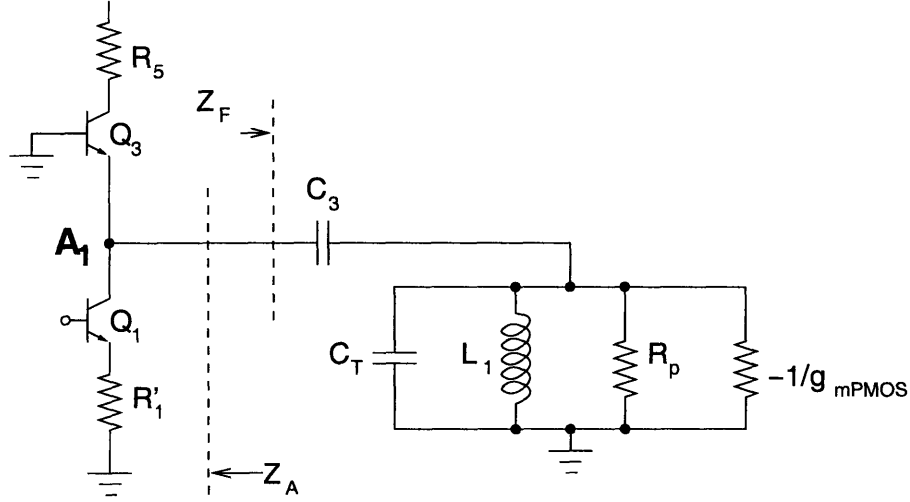
Figure 5-3: Equivalent circuit for Q-enhanced image reject notch filter at point A1.

is written as

$$Z_F = \frac{\left(\frac{C_T+C_3}{C_T C_3}\right)\left(s^2 + \frac{1}{R_{eff}(C_T+C_3)}s + \frac{1}{L_1(C_T+C_3)}\right)}{s\left(s^2 + \frac{1}{R_{eff}C_T}s + \frac{1}{L_1 C_T}\right)}. \tag{5.4}$$

Since the amplifier's impedance at point A_1 loads the filter, a Q-enhanced notch filter sets $g_{m_{PMOS}}$ to $1/R_p$ without fear of instability [64]. When this is done, R_{eff}, as given by (5.2), becomes infinite and the filter's impedance is given as

$$Z_F = \begin{cases} 0 & \text{for } \omega^2_{z_1,z_2} = \frac{1}{L_1(C_T+C_3)} \\ \infty & \text{for } \omega^2_{p_1,p_2} = \frac{1}{L_1 C_T}, \omega_{p_3} = 0 \end{cases} \tag{5.5}$$

where ω_{z_1} and ω_{z_2} are zero frequencies and ω_{p_1}, ω_{p_2}, and ω_{p_3} are pole frequencies of Z_F. When $Z_F=0$, a signal from collector of driver transistor Q_1 shorts to ground. This occurs because C_3 series resonates with C_T and L_1. When Z_F is infinite, the same signal passes to an emitter of Q_3 as in a normal LNA operation. This occurs because C_T parallel resonates with L_1 and produces an open circuit at one end of capacitor C_3. With $\omega_{p_3}=0$, capacitor C_3 acts as a DC blocking capacitor. With these relations in mind, to reject the image but not passband, it is necessary to set the

112
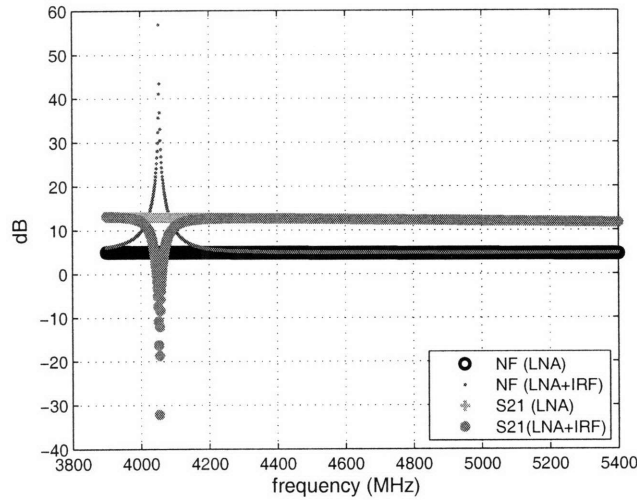
Figure 5-4: Simulated noise figure and gain versus frequency for an area-efficient LNA with and without Q-enhanced image reject notch filter. Noise figure and gain remain constant at 4.6 dB and 12 dB, respectively over frequency except at image frequency where a notch in the gain response produces a spike in noise figure. This spike "hides" true filter noise contributions at the image band.

image and passband frequencies as follow

$$\omega_{IMAGE}^2 = \omega_{z_1,z_2}^2, \tag{5.6}$$

$$\omega_{RF}^2 = \omega_{p_1,p_2}^2. \tag{5.7}$$

Considering (5.5), (5.6), and (5.7), this notch filter requires the image frequency to be less than the RF signal frequency since $C_3 > 0$ in (5.5). Fig. 5-4 plots in decibels simulated noise figure and gain for the previous area-efficient LNA with and without the additional Q-enhanced notch filter. In a 50 Ω system, gain $|S_{21}|^2$ is equivalent to transducer power gain G_T. Gain and noise figure for both cases remain constant over frequency except with an image filter, at 4.06 GHz, a large notch appears in the gain response to reject the image. This notch heavily attenuates an input signal and causes an artificially high peak to appear for noise figure. This behavior hides the true noise contributions at the image band.

113
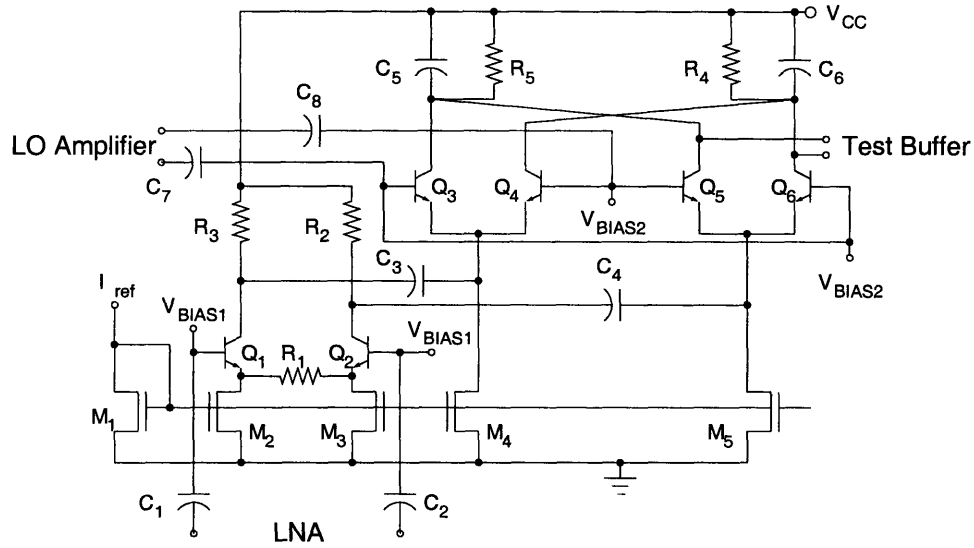
Figure 5-5: Area-efficient folded BiCMOS mixer. Area-efficiency comes from using RC as opposed to LC circuits at mixer's output. Folded design allows separate bias currents for RF transconductor and switching core, which maximizes both transconductance and voltage swing.

5.1.2 Mixer and LO Amplifiers

An area-efficient double-balanced folded mixer is shown in Fig. 5-5. The mixer uses RC low pass circuits consisting of resistors R_4 and R_5 and capacitors C_3 and C_4 at its output instead of LC bandpass circuits to achieve area-efficiency. A folded design maximizes transconductance and voltage swing by allowing separate bias currents to be used at the RF transconductor and the switching core. Bipolar transistors Q_1 and Q_2 are used for the transconductor and Q_3-Q_6 for the switching core to achieve a higher transconductance per unit current (g_m/I) when compared to MOS transistors. For the switching core, a higher g_m/I translates to a lower required LO power to switch. This put less demand on the individual receiver's local oscillator amplifier. Capacitors pairs C_1-C_2, C_3-C_4 and C_7-C_8 are DC blocking capacitors that simplify inter-stage biasing between LNA and mixer, transconductor and switching core, and LO amplifier and switching core, respectively. Similar to the area-efficient LNA, simple resistor divider networks (not shown in the figure) provide individual bias voltages to each bipolar transistor. Voltage V_{BIAS1} biases transconductor transistors

114
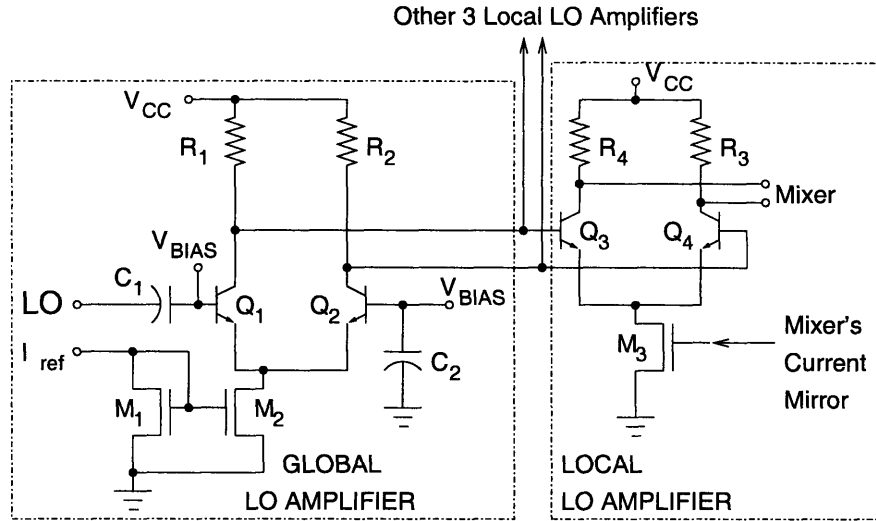
Figure 5-6: Global and local LO amplifiers. Two stage amplification allows a low power LO signal distribution.

Q_1 and Q_2 while voltage V_{BIAS2} biases switching core transistors Q_3-Q_6. The mixer uses NMOS transistors M_1-M_5 as current mirrors with an input reference current I_{ref}. These NMOS transistors do not have a gate current and thus exhibit good current match.

An LO signal that drives the mixer's core is applied externally to two amplifier stages before reaching the mixer as shown in Fig. 5-6. In the first stage, a single-ended input-differential output global LO amplifier converts and distributes a signal generator's input to all four parallel receivers. This global amplifier consists of a differential amplifier with one input AC coupled through capacitor C_1 to an external LO signal and another input bypassed by capacitor C_2. The differential amplifier consists of transistors Q_1 and Q_2, current mirror transistors M_1 and M_2, and resistors R_1 and R_2. An external reference current I_{ref} supplies the mirror circuit. At each receiver, a local LO differential amplifier consisting of transistors Q_3 and Q_4, resistors R_3 and R_4, and current source transistor M_3, amplifies the signal to a proper level in order to switch the mixer. The current source shares its gate bias with all other NMOS transistors of a local mixer.

Using two stages allows an LO signal to distribute with minimum power and

115

minimizes its undesired coupling into other parts of the receiver. To hard-switched the mixer's core requires a minimum of about 5 times thermal voltage, or about 100 mV peak. Improvements in noise are possible with stronger LO signals up to 300 mV [46]. If an external 50 Ω LO source drives the mixer directly, this means an LO input power of -10 dBm to 0 dBm is necessary. This is comparably large when considering RF and IF signal powers. With two stage LO amplification, a global LO amplifier provides a simulated voltage gain of 3.5 while a second local LO amplifier provides a simulated voltage gain of 2. As a result, a -27 dBm, or 14 mV, external LO signal then produces 50 mV peak distributed LO signal to each receiver that becomes 100 mV peak at the mixer.

5.2 Power and Area Estimates for WiGLAN Parallel Receivers

To determine power dissipation and area consumption for WiGLAN parallel receivers, it is necessary to find an optimal number of transceivers. This implies an application of the parallel transceiver power dissipation model. Total power dissipation and area consumption for parallel receivers then simply become a multiplication of this number with the power dissipation and area consumption for a single WiGLAN parallel receiver. A parallel transceiver power dissipation model that was previously given by (3.10) is given as

$$P_{N,TRX} = P_{LO} + N \frac{(P_{TX} + P_{RX})}{2} + \frac{1}{2\eta_{PA}} \frac{(4\pi)^2 (d/d_O)^n}{G_T G_R \lambda^2} F R_S N_O (E_S/N_O)_N. \quad (5.8)$$

This model requires power dissipation values for local oscillator, transmitter, and receiver. However, actually finding an optimal number of transceivers does not require knowing power dissipation for the local oscillator. An optimal number results from a balance between increasing power dissipation due to overhead that is given in the second term and decreasing power dissipation due to increasing SNR gain that is given in the third term as the number of transceivers N increases. The first term that

116
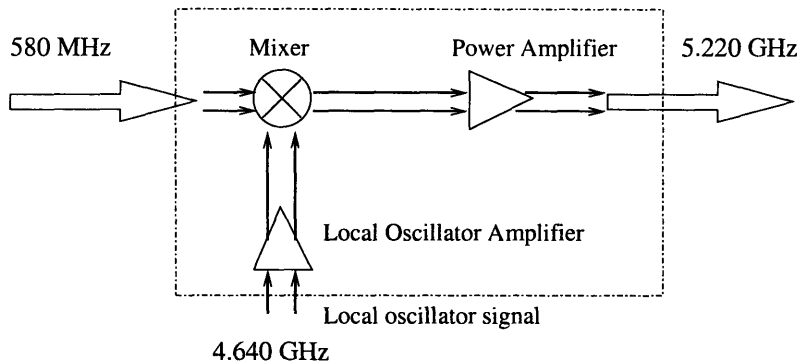
Figure 5-7: A single WiGLAN RF transmitter. It consists of a mixer, local LO amplifier, and power amplifier.

represents LO power dissipation is a constant that does not vary with N. Although LO power dissipation is necessary to determine parallel transceiver power dissipation, it is not necessary to determine N itself. Since the objective is to find N, the discussion to follow neglects P_{LO} in the transceiver power dissipation.

Power dissipation for a single transmitter and receiver come from the power dissipation values of their respective RF blocks. A single WiGLAN receiver that was shown in Fig. 5-1 has a power dissipation that is given as

$$P_{RX} = P_{LNA} + P_{IRF} + P_{MIXER} + P_{LOAMP}, \tag{5.9}$$

where P_{LNA}, P_{IRF}, P_{MIXER}, and P_{LOAMP} are the power dissipation for the LNA, image reject filter, mixer, and local LO amplifier, respectively. Fig. 5-7 shows a block diagram for a simple WiGLAN parallel transmitter. It consists of a mixer, local LO amplifier, and power amplifier. The power dissipation for a single WiGLAN transmitter is given as

$$P_{TX} = P_{MIXER} + P_{LOAMP}, \tag{5.10}$$

where P_{MIXER} and P_{LOAMP} are power dissipation for mixer and local LO amplifier, respectively, and power dissipation for a power amplifier is absent. This missing power dissipation has already been captured by the third term of the parallel transceiver power dissipation model that is given in (5.8). This term relates RF transmit signal

117

Circuit	Power(mW)
Receiver:	
LNA	19
Image Filter	≈ 0
Mixer	24
LO Amplifier	7
Transmitter:	
Mixer	24
LO Amplifier	7

Table 5.1: RF circuits power dissipation for WiGLAN receiver and transmitter. Power dissipation for receiver circuits are simulation results. Power dissipation for transmitter circuits assume that the transmitter uses a mixer and local LO amplifier with similar power dissipation to those of the receiver. Power amplifier power dissipation is absent as it is already part of the transceiver power dissipation model.

power necessary to achieve a certain SNR at the detector to power dissipation for a power amplifier through its power efficiency η_{PA}.

Table 5.1 lists power dissipation for the WiGLAN receiver and transmitter circuits. Power dissipation for receiver circuits come from Spectre DC simulations of circuits that were presented in Sections 4.3 and 5.1. On the other hand, power dissipation values for transmitter circuits assume a transmitter that uses a mixer and local LO amplifier with similar power dissipation to those of the receiver. The power amplifier power dissipation is captured in the transceiver model and therefore is not listed. Summing up listed values using the expressions for the WiGLAN single receiver and transmitter power dissipation as given by (5.9) and (5.10) gives $P_{RX}=50$ mW and $P_{TX}=31$ mW, respectively.

As mentioned previously, the third term of the parallel transceiver power dissipation model gives the power amplifier's contribution to transceiver power dissipation. To determine this term, Table 5.2 gives the values for the term's variables except for $(E_S/N_O)_N$ which was already given by Table 2.2 at 1 Gb/s data rate and 10^{-5} bit error rate. Power amplifier efficiency comes from [65] which had implemented a WiGLAN power amplifier. The noise factor value for F represents a simulated SpectreRF noise figure of 8.8 dB for a WiGLAN area-efficient parallel receiver. The rest of the listed values are standard noise density at room temperature, typical offset distance at 1 m,

Variable	Value	Units	Reference
η_{PA}	0.47		[65]
F	7.59		SpectreRF Simulation
N_O	4.00e-21	J/Hz	Standard
d_O	1	m	Standard
d	10		WiGLAN
GT,GR	1		WiGLAN
n	3		WiGLAN
λ	5.77	cm	WiGLAN
R_S	150	Msymbols/s	WiGLAN

Table 5.2: Additional inputs for WiGLAN parallel transceiver power dissipation model

WiGLAN transmission distance at 10 m for 1 Gb/s, and WiGLAN assumptions that were previously discussed in Section 3.3. With these values, Fig. 5-8 plots the parallel transceiver power dissipation as given by (5.8) versus N transceivers. Inherent in the power dissipation model, these transceivers applies SNR gain available through a rich-scattering channel to reduce RF transmit signal power. The plot shows that four transceivers give a transceiver power of 377 mW while five transceivers give a slightly lower consumption at 363 mW. The latter is a minimum transceiver power dissipation for WiGLAN parallel transceivers that use area-efficient parallel receivers. The parallel receivers themselves consume 200 mW for four receivers and 250 mW for five receivers.

With optimal number of antennas and receiver power dissipation out of the way, the next step is to estimate the area consumption for the WiGLAN parallel receiver test chip. Dropping the transmitter area in the parallel transceiver area consumption model as given by (3.3), a WiGLAN parallel receiver area consumption model is given as

$$A_{N,RX} = A_{LO} + NA_{RX}, \quad (5.11)$$

where A_{LO} and A_{RX} represent area consumption for LO and receiver circuits and N represents the number of transceivers. The area consumption for a single WiGLAN parallel receiver is given as

$$A_{RX} = A_{LNA} + A_{IRF} + A_{MIXER} + A_{LOAMP}, \quad (5.12)$$

119
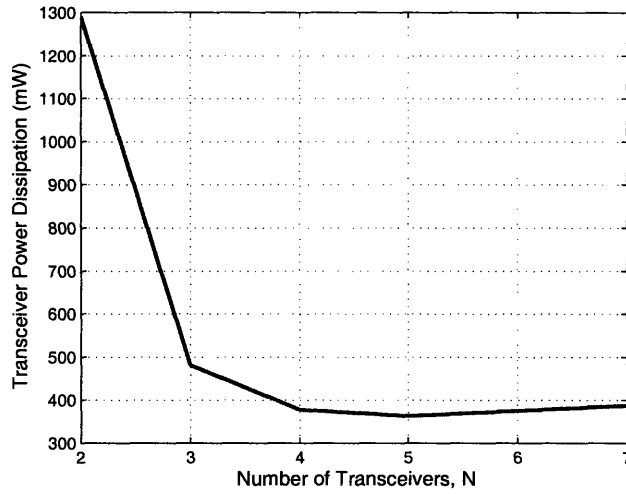
Figure 5-8: Power dissipation for parallel transceivers that use area-efficient parallel receivers. Minimum power of 363 mW occurs at five transceivers. Using four transceivers consume 377 mW. Note that plot does not account for LO power dissipation since it is not necessary when seeking N.

where A_{LNA}, A_{IRF}, A_{MIXER}, and A_{LOAMP} represent the areas for LNA, image reject filter, mixer, and local LO amplifier. Table 5.3 lists estimated area consumption values for a single WiGLAN parallel receiver and its shared circuits. Area consumption values for receiver circuits come from an initial layout. These values altogether gives 0.7 mm^2 for a single receiver. Floorplanning reserves 1.5 mm^2 for LO, its global amplifier, bias and distribution circuits. Using these values, Fig. 5-9 plots the WiGLAN parallel receiver area consumption as given by (5.11) versus N transceivers. Four

Circuit	Area(mm^2)
Receiver:	
LNA	0.23
Image Filter	0.15
Mixer	0.2
LO Amplifier	0.12
Shared circuits	1.5

Table 5.3: Area consumptions for receiver and shared circuits. The shared circuits include LO, bias, and distribution circuits. Values are estimates based on floorplanning and initial layout.

120
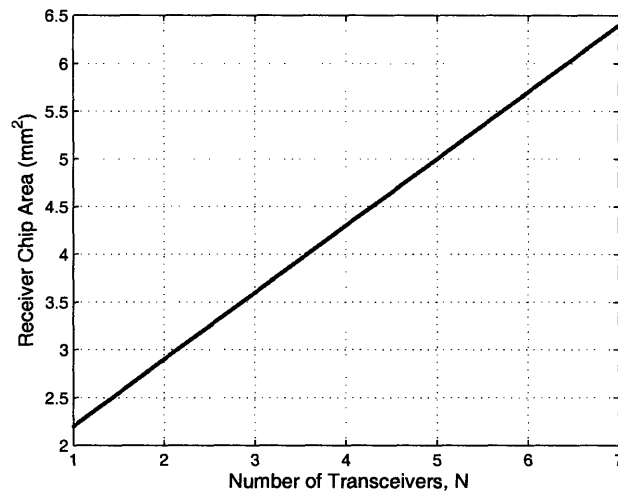
Figure 5-9: Area consumption for area-efficient parallel receivers. At $N=4$, the receivers consume 4.3 mm^2.

receiver consumes 4.3 mm^2 while five receivers consumes 5.0 mm^2. Since power consumptions for four and five transceivers are nearly similar, it is better to choose four receivers and save some chip area. This choice then gives a four parallel receivers that, in total, consume 4.3 mm^2 active area and 200 mW power dissipation.

A floorplan for a four receivers chip is shown in Fig. 5-10. A receiver occupies each corner of the chip and shares bias, control, and LO signals. Bias and distribution and global LO amplifier circuits exist in a center area and takes roughly 0.5 mm^2. The floorplan saves 1 mm^2 chip area for an eventual drop-in LO design. Frequency control and Q control signals come from off-chip. A simple wire then connects all the receivers' voltage variable capacitor terminals together while a current mirror circuit distributes a Q control current signal to the various PMOS devices. A second current mirror circuit distributes a reference current to mixer and LO amplifier circuits.

Before moving on to the next section, it is appropriate to estimate the impact on parallel receivers for the area-efficient LNA as well as the conventional and variable power LNA. The conventional LNA is the differential narrowband cascode LNA that was previously shown in Fig. 4-6. The variable power LNA is the same conventional LNA but it operates at lower bias current. This LNA occupies an estimated 0.6
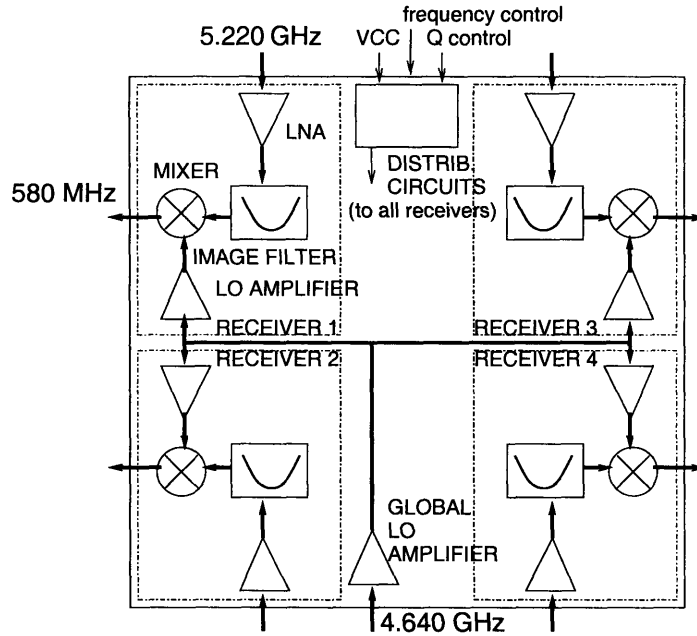
Figure 5-10: Floorplan for parallel receiver RFIC. Four receivers and support circuits consume 4.3 mm². A receiver at each corner consumes 0.7 mm². It is expected that shared circuits will occupy 1.5 mm² in the center area.

mm² area and operates at 10.3 mW (conventional) and 3.6 mW (variable power). A receiver that uses this LNA but keeps its other circuits the same as the WiGLAN area-efficient parallel receiver allows a fair comparison of the benefits from SNR gain alone. This receiver consumes 1.07 mm² chip area and uses 41.3 mW for conventional and 34.6 mW for variable power LNA. Fig. 5-11 plots the area consumption for parallel receivers that use a conventional or variable power LNA and an area-efficient LNA versus the number of transceivers N. At four receivers, the receivers that use an area-efficient LNA consume 1.5 mm² less area than the receivers that uses the conventional LNA. This gap nearly doubles for seven receivers. Table 5.4 compares the power dissipation and area consumption for these parallel receivers. At four receivers, an area-efficient LNA approach has 35 mW more power dissipation than a conventional LNA approach but uses 1.5 mm² less area. This increases the receivers' power dissipation by 21% but reduces their chip area by 25%. This implies that a design that faces a critical area constraint must sacrifice some power dissipation to

122
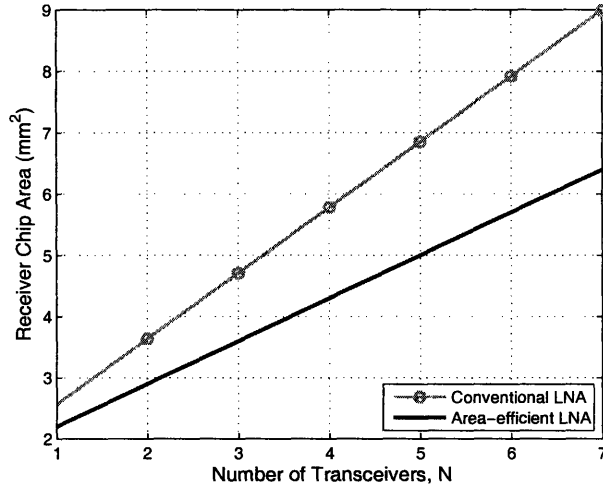
Figure 5-11: Area consumption for parallel receivers that use conventional and area-efficient LNA. At $N=4$, receivers that use the conventional LNA consume an additional 1.5 mm^2 over receivers that use an area-efficient LNA.

LNA Approach	P_{LNA}(mW)	$P_{4,RX}$(mW)	$A_{4,RX}$(mm^2)
Area-efficient	19	200	4.3
Conventional	10.3	165	5.8
Variable Power (Low Power)	3.6	138	5.8

Table 5.4: Estimated power dissipation and area consumption for 4 parallel receivers that use either an area-efficient, conventional, or variable power LNA. LNA power dissipation are simulated values.
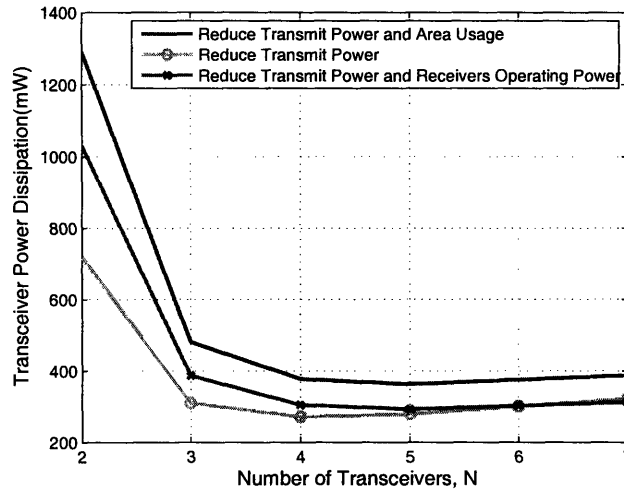
Figure 5-12: Transceiver power dissipation for parallel receivers that use three different LNA approaches. An area-efficient LNA approach applies SNR gain to reduce transmit power and area usage. A conventional LNA approach applies SNR gain to reduce transmit power only and a variable or low power LNA approach applies SNR gain to reduce transmit power and receiver operating power.

gain area savings. Four receivers that use a low power LNA approach has 27 mW less power dissipation than the same number of receivers that uses a conventional LNA approach. This saves receiver power dissipation by 16%. The power savings are less than area since the conventional LNA power dissipation represents only 25% of a parallel receiver's power dissipation while its area represents 56% of a parallel receiver's area consumption.

A broader consideration that includes the transmitter is shown in Fig. 5-12. This figure plots transceiver power dissipation versus the number of transceivers for all three approaches and is similar to Fig. 5-8 as it neglects LO power dissipation. The legend for this figure describes how the transceivers apply SNR gain. Transceivers that use an area-efficient LNA approach apply SNR gain to reduce transmit power and area usage. Transceivers that use a conventional LNA approach apply SNR gain to reduce transmit power only. Transceivers that use a variable or low power LNA approach apply SNR gain to reduce transmit power and receiver operating power. At small N, the difference in power dissipation between the approaches come from

the difference in receiver noise figure. The receiver that uses a conventional LNA has simulated 6 dB noise figure. When it operates the LNA at low power dissipation, its noise figure becomes 7.8 dB. This requires 1.8 dB SNR gain at the receiver to offset the additional noise. For the receiver that uses an area-efficient LNA, it has a simulated 8.8 dB noise figure and therefore needs 2.8 dB SNR gain at the receiver to cover its additional noise. As the transceivers apply more SNR gain at the receivers, less is available to reduce RF transmit signal power at the transmitters. This causes transmitter power dissipation to increase. At low N, RF transmit signal power is significant and the differences in applied SNR gain are apparent. The transceivers that use a conventional approach have the lowest power dissipation since it applies all of the SNR gain to reduce RF transmit signal power. As the number of transceivers increases, there is enough SNR gain available to sufficiently make RF transmit signal power small. The power dissipation differences between the approaches then are due to the power dissipation of the LNA themselves. However, when compared to the conventional approach, the variable or low power approach only saves power dissipation at high number of transceivers N when there are many LNAs.

5.3 Chip Characterization for WiGLAN Parallel Receivers

Using the circuits given in Sections 4.3 and 5.1 and the results predicted by the models, this thesis implements four parallel receivers on a single chip. The discussions to follow present this area-efficient parallel receiver chip, its test board, measurement setups, and measurement results.

5.3.1 Receiver Chip and Test Board

A WiGLAN parallel receiver test chip is shown in Fig. 5-13. It is fabricated in a 0.18 μm SiGe BiCMOS IBM 7WL process. The chip has a total area that is 2.26 mm by 2.5 mm and uses an active area that is approximately 4 mm^2. Similar to its floorplan,

125
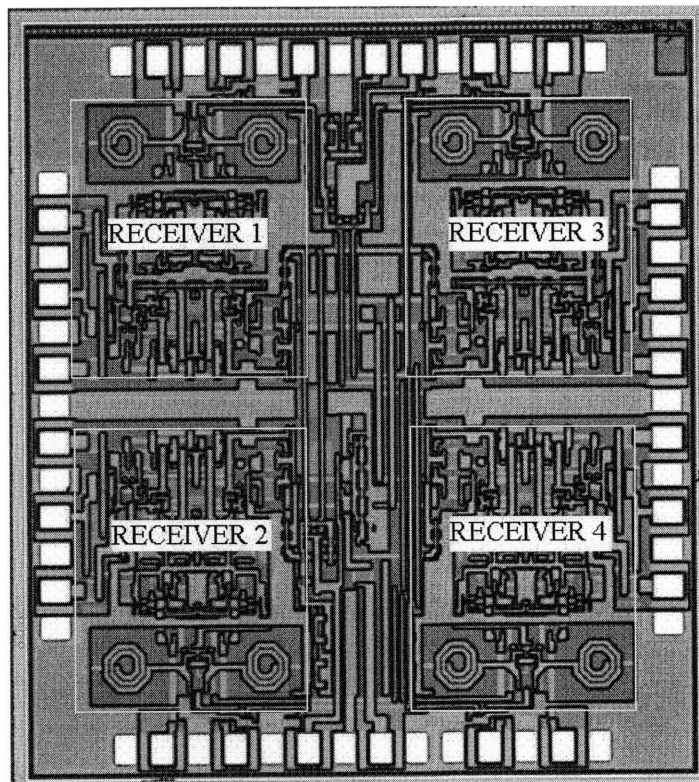
Figure 5-13: WiGLAN parallel receiver RFIC die photo. Chip area is 5.65 mm^2 (active area=4 mm^2). Process is IBM 0.18 μm SiGe BiCMOS 7WL.
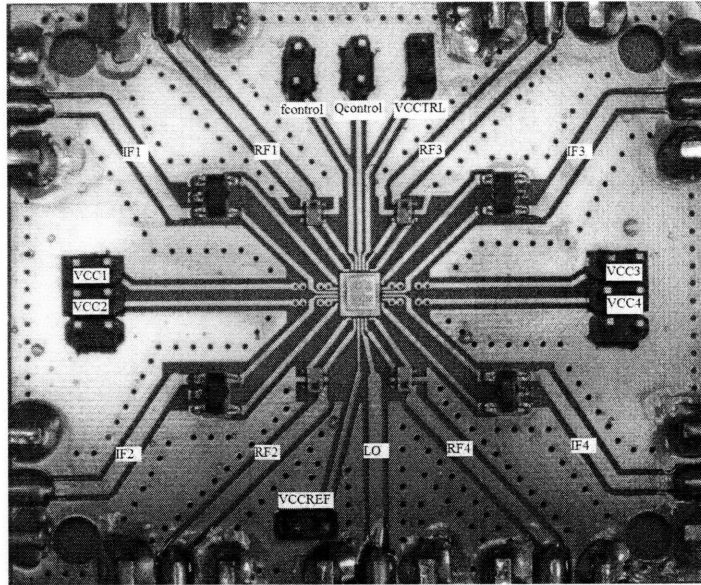
Figure 5-14: Test printed circuit board (PCB) with direct die attachment at center.

it has a parallel receiver at each of its four corners. Each receiver uses two spiral inductors to implement its Q-enhanced notch filter. This filter is the only parallel receiver circuit that uses on–chip inductors. The parallel receiver circuits that include the LNA, mixer, and LO amplifiers, as previously discussed, are all resistor-based. In total, this chip has 54 bondpads with 29 bondpads for signal and 25 bondpads for ground connections. Except for two DC signals, every signal bondpad has adjacent ground bondpads on either side to isolate its signal.

For measurement, the parallel receiver chip mounts directly to a printed circuit board (PCB) at its center as shown in Fig. 5-14. This test board avoids soldermask and solder tinning and instead uses an immersion gold plating that facilitates the die attachment to the PCB. After attachment, ground bondpads downbond to a PCB ground paddle. Bondwires attach input and output high frequency differential signals to on-board baluns which then convert them to single-ended signals that are more suitable for single-ended test equipment. After these baluns, 50 Ω coplanar waveguide lines carry the signals to SMA connectors. Bondwires also attach bondpads for DC signals to lines on the PCB that go to pin connectors.

127
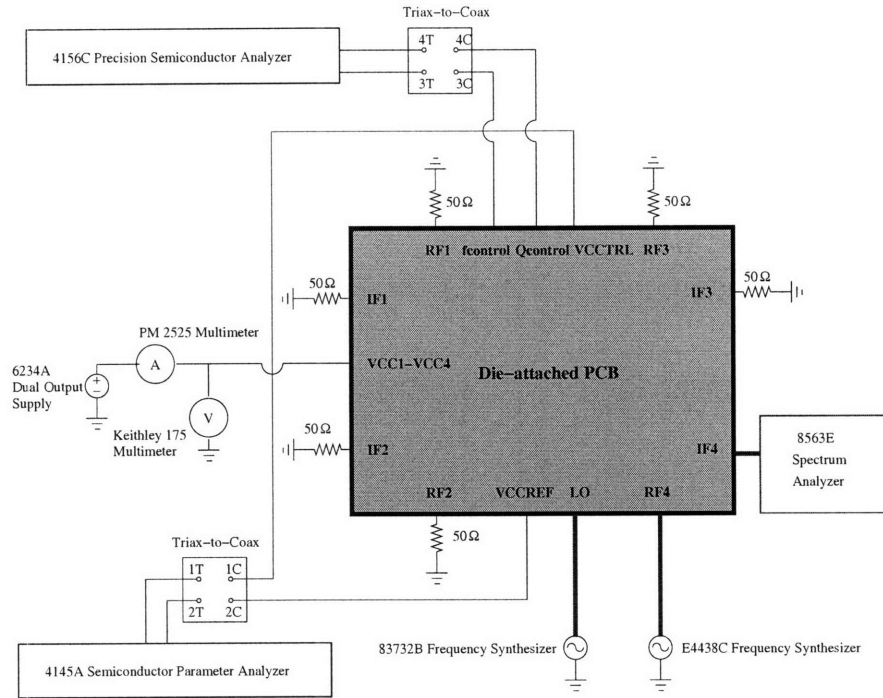
Figure 5-15: Test setup for receiver power dissipation and gain measurements

5.3.2   Test Setup

A board level test diagram that is suitable to measure receiver power dissipation, passband gain, image rejection, and gain compression is shown in Fig. 5-15. This diagram considers receiver number 4 as the receiver under test. R_{F1} through R_{F4} and I_{F1} through I_{F4} are inputs and outputs, respectively, for receivers 1 through 4. Measurements for other receivers require a simple swap of R_{F4} for R_{F1}, R_{F2}, or R_{F3} and correspondingly I_{F4} for I_{F1}, I_{F2}, or I_{F3}. Supply voltages V_{CC1} through V_{CC4} supply receivers 1 through 4. Separate voltages V_{CCREF} and V_{CCTRL} provide supply voltage for reference and Q control current mirrors. In this particular setup, receiver number 4 receives an RF input from a frequency synthesizer and outputs to a spectrum analyzer. A separate frequency synthesizer supplies an LO signal input. With an LO signal, the receiver frequency translates its high frequency RF input to a low frequency IF output. SMA connectors and low loss RF cables connect these board inputs and outputs to test equipment. All unused high frequency board inputs and

128
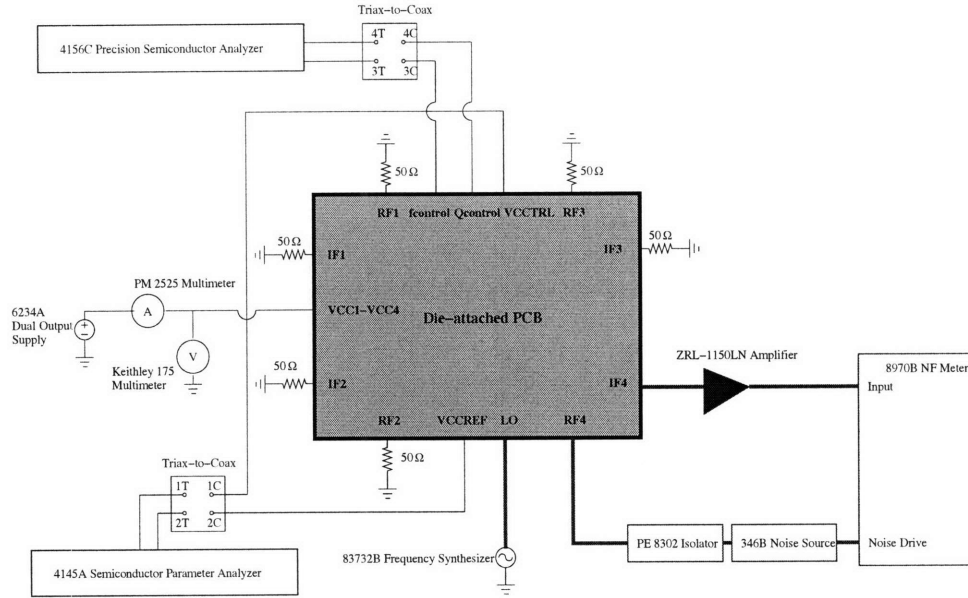
Figure 5-16: Test setup for noise figure measurements.

outputs terminate with 50 Ω to avoid reflections. A precision semiconductor analyzer supplies $f_{control}$ voltage and $Q_{control}$ current signal and allows for fine resolution control of signal levels. Another semiconductor analyzer provides voltage supplies to V_{CCREF} and V_{CCTRL}. These analyzers also act as multimeters and measure voltage and current outputs to simplify the test setup. With semiconductor parameter analyzers, triax-to-coax conversion is necessary and so a simple custom converter box converts between connector types. Since current consumption for all four receivers exceed the current limit of a parameter analyzer, a general purpose power supply provides a supply voltage for each receiver and uses a voltmeter and ammeter to monitor its voltage and current outputs, respectively.

A board level noise figure measurement setup is shown in Fig. 5-16. Similarly to the previous setup, this diagram considers receiver number 4 as the receiver under test. The setup removes the frequency synthesizer at the RF input and replaces it with a broadband noise source. At the output, a noise figure meter input replaces a spectrum analyzer. As before, characterization for another receiver requires swapping RF and IF ports to that receiver. An 8970B Noise Figure Meter uses a Y-factor method to measure noise figure. This method requires a driver to switch on and off

129
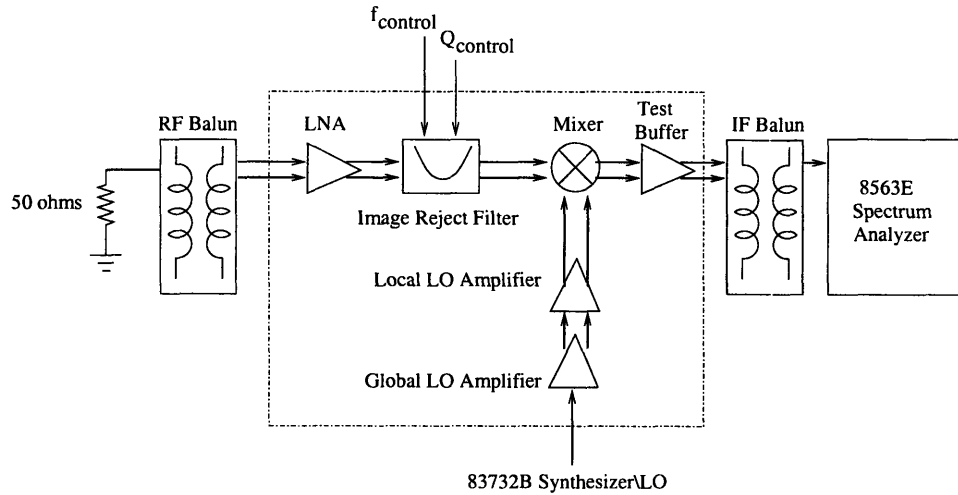
Figure 5-17: Filter frequency range measurement setup for a receiver

a pre-calibrated noise source that feeds an input of a device under test. To minimize reflections at a receiver's input due to mismatches between it and a noise source, a low loss (0.6 dB IL maximum) 4-8 GHz isolator separates noise source and receiver. A low noise amplifier module amplifies the receiver's output before feeding the meter's input. This amplifier also exists in a calibration setup and therefore becomes part of the measurement system. Both isolator and amplifier modules are precautionary additions in a noise figure measurement setup to deal with possible issues of poor input match, low gain device under test, and appreciable cable loss after device under test. These additions help reduce the uncertainty of a noise figure measurement [66].

Frequency tuning range measurements for a Q-enhanced notch filter do not require an RF input [67]. A test setup diagram is shown for this measurement in Fig. 5-17. DC supply voltages for this measurement are not shown as they are the same as the previous two setups. Since the receiver does not need an RF input, its input terminates to a 50 Ω SMA load through the on–board RF balun. The test increases $Q_{control}$ current signal to force the notch filter to become unstable and oscillate at the filter's center frequency. This produces a signal that drives the transconductor input for the mixer. An external synthesizer supplies an LO signal that frequency translates the oscillation signal to a lower frequency. This is necessary given that an IF balun

Connection	Input/output value
V_{CC1}-V_{CC4}	1.8 V
V_{CCREF}	1.8 V
V_{CCTRL}	3.3 V
R_{F1}-R_{F3}	50 Ω
I_{F1}-I_{F3}	50 Ω
$f_{control}$	Variable voltage
$Q_{control}$	Variable current
LO	4.64 GHz, -20 dBm RF signal
R_{F4}	Variable frequency, -40 dBm RF signal; 50 Ω
I_{F4}	Input to Spectrum Analyzer; Ext. Amplifier

Table 5.5: Setup values corresponding to previous test diagram for receiver number 4

at the output has a passband range between 2-800 MHz and the center frequency for the filter is near 4 GHz. This translation merely implies that the filter frequency is the measured output frequency plus a constant equal to the LO frequency.

Table 5.5 provides the setup values for each signal. While V_{CC1} through V_{CC4} and V_{CCREF} use 1.8 Volts, V_{CCTRL} uses 3.3 Volts to give greater range for $Q_{control}$. Unused RF inputs R_{F1} through R_{F3} and IF outputs I_{F1} through I_{F3} terminate to 50 Ω SMA loads. With two on–chip LO amplifier stages, the chip uses a relatively low LO input at -20 dBm. Passband and image band gain characterizations requires RF input signals that vary within the passband from 5.145 GHz to 5.295 GHz and within the image band from 3.985 GHz to 4.135 GHz, respectively. A passband gain compression measurement steps a 5.22-GHz RF input power upwards at 1 dB increments until gain compresses by 1 dB. Frequency tuning measurement for the Q-enhanced notch filter forces the filter to oscillate using $Q_{control}$ and then varies $f_{control}$ to determine its frequency range. This tuning measurement requires R_{F4} to terminate to 50 Ω. A noise figure measurement replaces the input RF signal at R_{F4} with a input noise source and removes the spectrum analyzer from I_{F4} and replaces it with an external amplifier that feeds a noise figure meter.

Chip:	
Technology	0.18 μm SiGe BiCMOS
Total area	2.26x2.5 mm^2
Active area	4 mm^2
Power Dissipation, 4 receivers (includes test buffer)	225 mW
Power Dissipation, Shared circuits (excludes LO)	56 mW
Receivers:	
(IF=580 MHz and LO power=-20 dBm)	
Power Conversion Gain	14 dB
Minimum rejection at 4.06 GHz	36 dB
Filter frequency tune ($f_{control}$=0.9 V)	270 MHz/V
Input 1-dB Gain Compression Point	-33 dBm
NF (Q-enhancement OFF/ON)	7/15 dB

Table 5.6: Chip Summary

5.3.3 Measurement Results

Table 5.6 summarizes results for an area-efficient parallel receiver RFIC test chip. The chip has 4 mm^2 active area for its four receivers and shared circuits. This value is similar to the 4.3 mm^2 area consumption estimated by the parallel receiver area consumption model. The difference of 0.3 mm^2 comes from the shared circuits area consumption which actually has an area of 1.2 mm^2 as opposed to the predicted 1.5 mm^2. Measured power dissipation for the four receivers at 225 mW is also similar to the 200 mW parallel receiver power dissipation predicted by the parallel transceiver power dissipation model. It is slightly greater because it includes power dissipation for a test buffer that follows the mixer. This buffer shares the same supply as the rest of the receiver circuits to avoid additional DC inputs for the chip. These area consumption and power dissipation results confirm the validity of the power dissipation and area consumption models. The chip also consumes 56 mW for its shared circuits that include current mirrors for the distributed reference current and control current $Q_{control}$ and the global LO amplifier. The chip did not implement an on–chip LO and excludes its power dissipation from the measured power dissipation for shared circuits.

A WiGLAN parallel receiver converts a signal at 5.22 GHz to 580 MHz with 14 dB power conversion gain. It uses a Q-enhanced image reject notch filter that has a
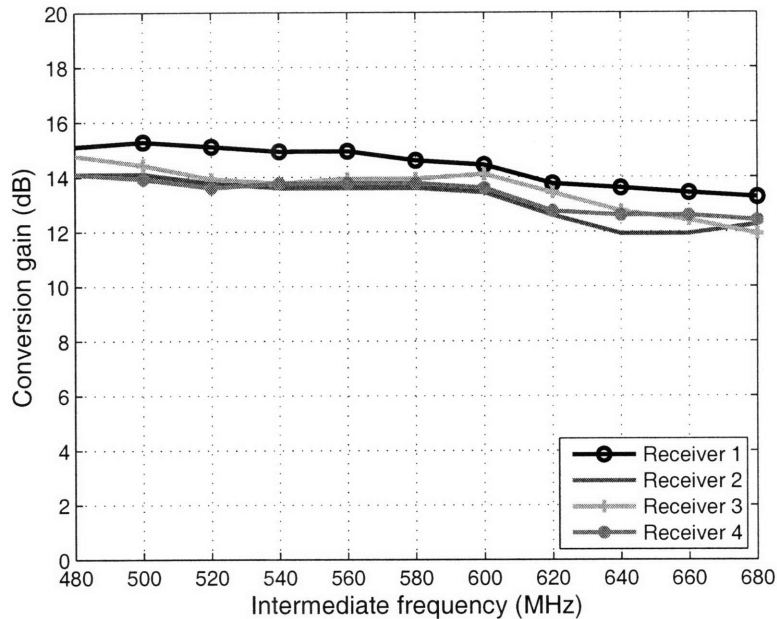
Figure 5-18: Pass band conversion gains

tuning constant of 270 MHz/V at $f_{control}$=0.9 Volts and allows the receiver to achieve a minimum 36 dB rejection for an image at 4.06 GHz. The receiver exhibits two noise figure values dependent on the application of Q-enhancement. It has a 15 dB noise figure when the image reject notch filter uses Q-enhancement and 7 dB noise figure when the same filter does not use Q-enhancement. The receiver has a 1 dB gain compression point at -33 dBm input power. The discussions to follow provide more details for these measured results.

Passband Gain and Image Rejection

The measured passband conversion gain for all four parallel receivers is shown in Figs. 5-18. Comparing gain between receivers shows that the maximum difference is 1.67 dB and it occurs between receiver number 1 and number 2 at an output frequency of 640 MHz. If the figure neglects receiver number 1, gain difference between the other three receivers is well under 1 dB for the entire output frequency range. It is likely that these gain differences as well as the gain slope at higher output frequency result
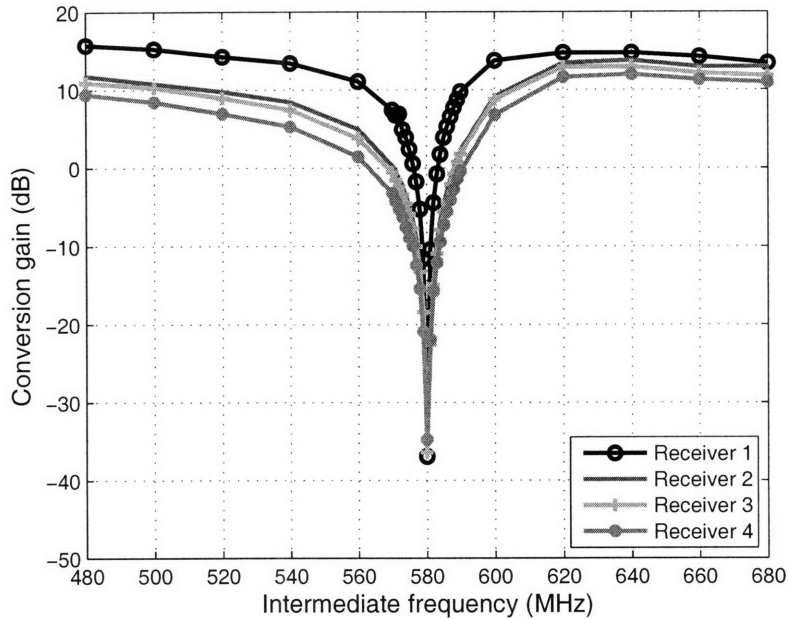
Figure 5-19: Image frequency conversion gains

from the test board IF baluns. These IF baluns possess a 2 dB slope for insertion loss at higher frequency and their unit-to-unit insertion loss vary by about 1 dB.

The measured image band conversion gain for all four receivers is shown in Fig. 5-19. With Q-enhanced image reject notch filters, the receivers achieve greater than 36 dB image rejection at 580 MHz output frequency. Since the LO frequency is at 4.64 GHz, this output frequency corresponds to an image that exists at 4.06 GHz. The filters for all four receivers have a center frequency that is tunable from 3.9 GHz to 4.2 GHz for $f_{control}$ values from 0.45 Volts to 1.8 Volts as shown in Fig. 5-20. At 0.9 Volts, the filters achieve a 270 MHz/V tuning constant.

Compression Point

Measured output power versus input power for all four receivers is shown in Fig. 5-21. The relationship between these two powers remain linear to within 1 dB for input powers less than -33 dBm. The parallel receiver test chip did not include a test port in-between the LNA and mixer so it is not possible to determine by

134
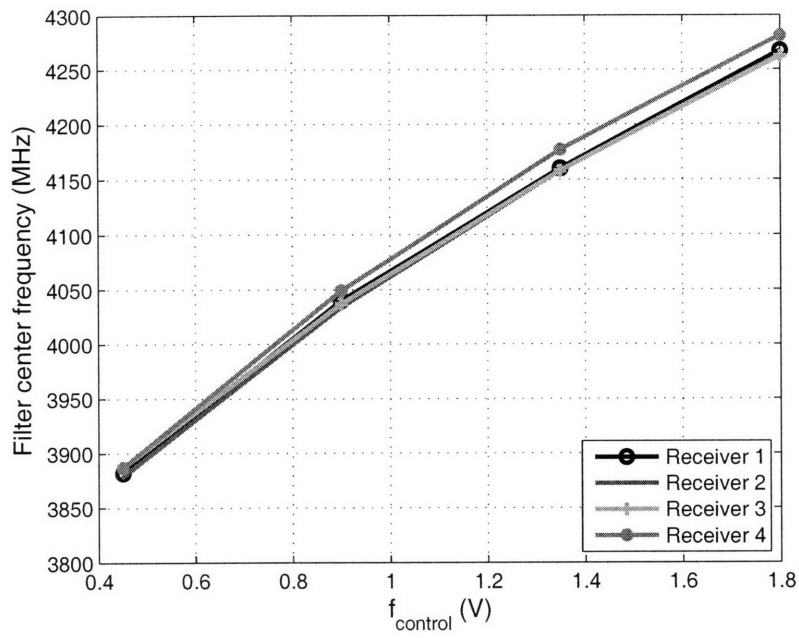
Figure 5-20: Notch filters' center frequency tuning ranges
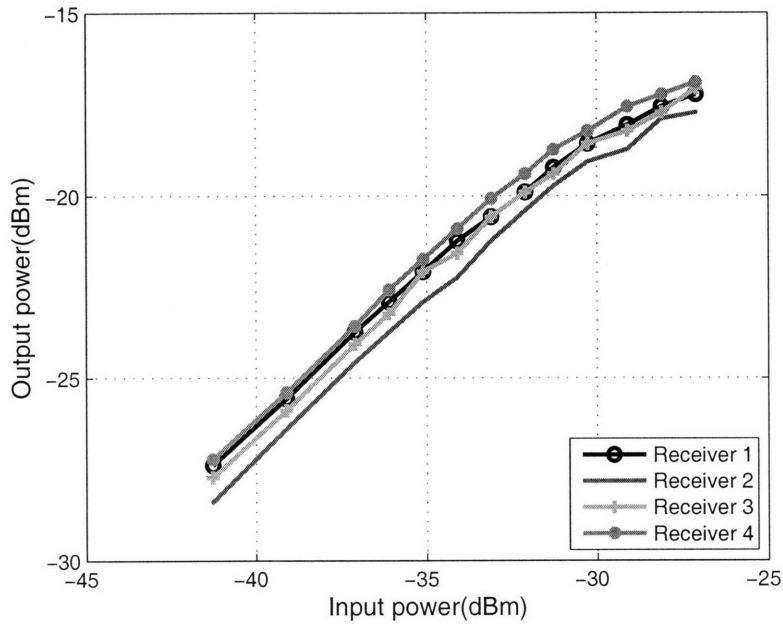
Figure 5-21: Output powers versus swept input powers for 5.22-GHz RF input signal. Input 1 dB compression point occurs at approximately -33 dBm.
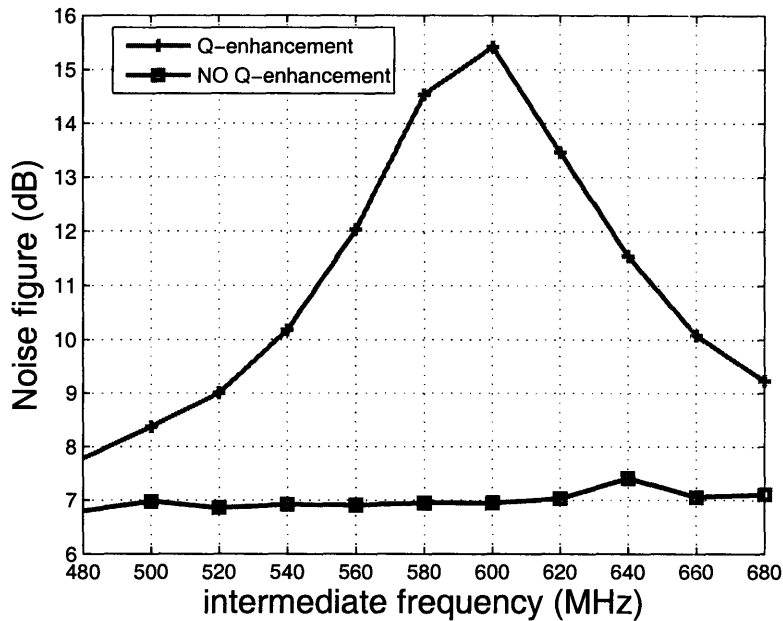
Figure 5-22: Receiver noise figure with and without Q-enhancement applied for image reject notch filter. Q-enhancement produces a large peak in noise figure near the center frequency for the notch filter.

measurement the circuit that limits compression point. However, simulation shows that this compression point is set by the mixer and not the area-efficient LNA. While the area-efficient LNA has a simulated -19 dBm input 1-dB compression point, the mixer has a simulated -24 dBm input 1-dB compression point. Since the mixer's input comes after signal amplification and its compression point is lower than the LNA, the mixer sets the receiver compression point. As an example, if the power gain of the area-efficient LNA that precedes the mixer is just 9 dB, this gives the receiver input compression point set by mixer at -33 dBm as measured.

Noise Figure

Measured noise figure shows a large noise figure peak for the WiGLAN parallel receiver. As shown in Fig. 5-22 for the curve labeled "Q-enhancement," this peak appears near the center of the output passband at 580 MHz. The figure shows that the receiver has a 15 dB noise figure peak when its applies Q-enhancement to its filter

136
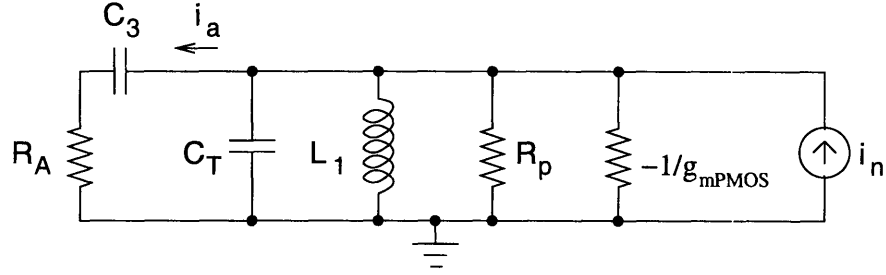
Figure 5-23: Circuit for noise analysis at desired pass band frequency.

but 7 dB noise figure when it does not. Since the receiver uses an LO frequency at 4.64 GHz and translates both image band at 4.06 GHz and passband at 5.22 GHz to this output passband, it is unclear which input band is responsible for the large peak in noise figure although it is certain that using Q-enhancement produces it. The next section shows through analysis, simulation, and measurement that image noise due to the notch filter degrades the receiver noise figure.

5.3.4 Q-enhanced Notch Filter Noise

Examination of the filter circuit shows that it contributes noise to the area-efficient LNA through its coupling capacitor. As previously shown in Fig. 5-3, this is capacitor C_3. A more simplified equivalent circuit for noise analysis is shown in Fig. 5-23. In this circuit, a resistor R_A represents the amplifier as a load for the filter. The noise current i_a that flows to the amplifier is then given by current division as

$$i_a = \left(\frac{Y_3}{Y_3 + sC_T + \frac{1}{sL_1} + \frac{1}{R_{eff}}} \right) i_n, \qquad (5.13)$$

where

$$Y_3 = \frac{1}{\frac{1}{sC3} + R_A}, \qquad (5.14)$$

and i_n represents an equivalent noise source for the filter and $R_{eff}=R_p||\frac{-1}{g_{mPMOS}}$. From (5.7), at the center frequency of the receiver passband, L_1 resonates with C_T. In addition, the application of Q-enhancement sets $g_{mPMOS} = \frac{1}{R_p}$. As a result, the last three terms in the denominator of (5.13) disappear and i_a equals i_n. Therefore,

137
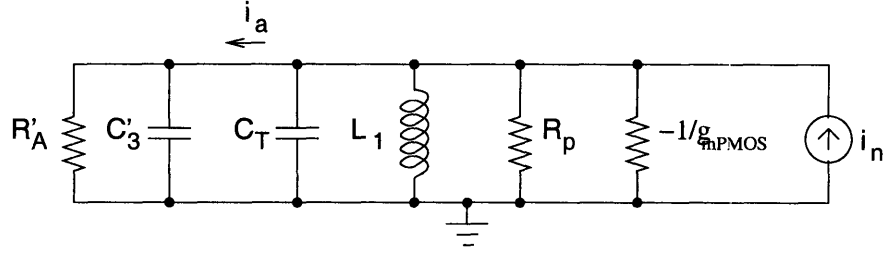
Figure 5-24: Circuit for noise analysis at image frequency.

a Q-enhanced image reject notch filter contributes all of its noise current i_n to the amplifier circuit at the receiver passband.

At the notch frequency, which coincides with the image frequency as given by (5.6), L_1 resonates with C_T and C_3. The expansion of (5.13) to determine i_a that flows into the amplifier at the notch frequency is cumbersome and yields no intuition. Instead, the admittance Y_3 is first converted to a parallel equivalent RC circuit as shown in Fig. 5-24. New resistor R'_A and capacitor C'_3 are given as

$$R'_A = R_A(Q_3^2 + 1), \tag{5.15}$$

$$C'_3 = C_3 \left(\frac{Q_3^2}{Q_3^2 + 1} \right), \tag{5.16}$$

where the quality factor Q_3 is given by

$$Q_3 = \frac{1}{\omega R_A C_3}. \tag{5.17}$$

The current i_a is the sum of the currents that flow through R'_A and C'_3. It is given as

$$i_a = i_{R'_A} + i_{C'_3}. \tag{5.18}$$

At $\omega^2 = \frac{1}{L_1(C_T + C'_3)}$, and $g_{mPMOS} = \frac{1}{R_p}$, all of i_n flows through R'_A so that $i_{R'_A} = i_n$. To determine $i_{C'_3}$, note that the voltage magnitude across the resonator, $|V|$, is given as

$$|V| = |i_n|R'_A. \tag{5.19}$$

138

Then the current that flows through C_3' is $|V|\omega C_3'$. Combining results from (5.15), (5.16), (5.17), (5.18), and (5.19) gives the current through $i_{C_3'}$ as

$$\begin{aligned} |i_{C_3'}| &= |i_n|R_A'\omega C_3' \\ &= |i_n|Q_3. \end{aligned} \tag{5.20}$$

With this result, the current to the amplifier becomes

$$i_a = i_n(1 + Q_3). \tag{5.21}$$

The last equation implies that the Q-enhanced image reject notch filter contributes more noise at its notch frequency and suggests the noise figure peak that appeared in Fig. 5-22 must come from the image band.

A noise simulation for an area-efficient LNA that uses a Q-enhanced image reject notch filter illustrates this analytical result. Fig. 5-25 plots the simulated output noise for this circuit along with the output noise components due to the filter and the input source resistance. Output noise components due to the LNA itself are not shown. Near the RF pass band, the noise contributed from the filter is well below the noise contributed by an input source resistance. However, as the plot approaches the center frequency for the Q-enhanced image reject notch filter, the filter's noise contributions rise. At the same time the noise contributions by the input dramatically decrease since the notch filter significantly attenuates any input signal at its center frequency. For noise figure, this notch in gain "hides" true noise contributions from a Q-enhanced notch filter (see Fig. 5-4).

Noise contributions from a Q-enhanced notch filter impact the receiver most when the filter's center frequency is the same as the image frequency since the receiver folds the image in-band. Fig. 5-26 plots measured receiver noise figure versus output frequency for the receiver that uses a Q-enhanced image reject notch filter and operates with two different image frequencies. The curve that has a large noise figure peak has an image frequency that is the same as the notch frequency at 4.06 GHz. The curve
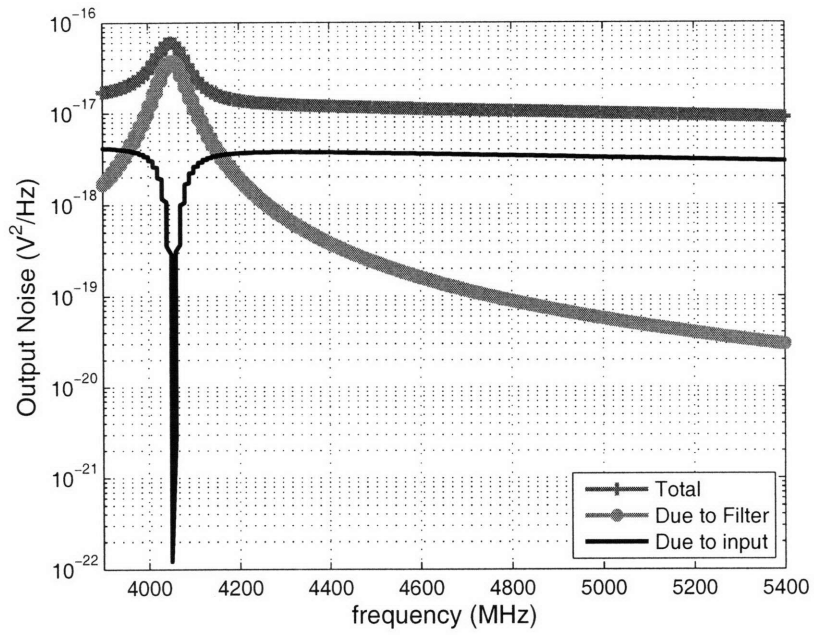
Figure 5-25: Simulated output noise of LNA with Q-enhanced image reject notch filter. Note that the output is plotted on a logarithmic scale.
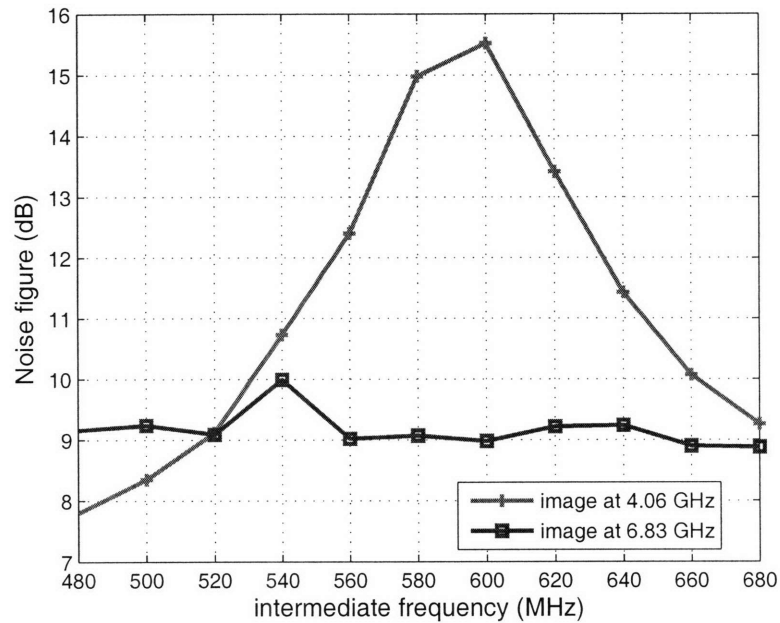

Figure 5-26: Measured receiver noise figures at an intermediate frequency for notch frequency at 4.06 GHz and images centered at 4.06 GHz and 6.83 GHz.

that does not possess a similar peak has an image that is not at the notch frequency. This latter curve comes from an image at 6.83 GHz that experiences less receiver gain. This reduces its SNR and increases receiver noise figure to around 9 dB.

The Q-enhanced notch filter provides a deep but narrow notch at the image band. This allows the WiGLAN parallel receiver to reject interferers that may fold in-band and cause signal distortions. This notch filter also rejects input image noise but since its notch bandwidth is narrow, a good portion of this noise still folds in-band. However, it is not this input noise but the image noise contributions from the Q-enhanced notch filter itself that severely degrade the receiver noise figure. Given this realization, it would be best to avoid using a Q-enhanced notch filter. Without this filter, certainly a little more input image noise folds in-band but a lot of filter image noise goes away. The noise measurements without Q-enhancement approximate this situation and predict that the receiver noise figure without a notch filter to be around 7 dB. Without the Q-enhanced notch filter, the receiver is once again susceptible to image band interferers. However, since WiGLAN uses an image band that contains the spectrum for a weak satellite signal, it is unlikely that any image interferer exists.

5.4   Summary

This chapter presents an area-efficient WiGLAN parallel receiver test chip. The chip represents the application of the concepts presented in this thesis that include power dissipation and area consumption models, SNR gain, and minimal power and area circuits. The chapter gives an overview of the test chip and various measurement setups. It then presents measured power dissipation and area consumption for the test chip that validate the power dissipation and area consumption models and also demonstrate the feasibility of an area-efficient LNA. Measurement results also indicate that the Q-enhanced image reject notch filter contributes significant noise at the image band. This image noise folds in-band and severely degrades the receiver noise figure. Without interferers in the image band, removal of this filter should improve the noise figure and not produce any signal distortion.

Chapter 6

Conclusion and Future Work

This chapter reviews the major thesis contributions. These contributions confirm that the thesis represents the first work to reduce power dissipation and area consumption for multiple antenna RF circuits. Possible future research directions follow this consideration and are extensions of SNR gain into other parts of the radio.

6.1 Thesis Contributions

This thesis presents an approach that applies SNR gain to reduce power dissipation and area consumption for parallel receivers. The contributions from this thesis are as follow.

- *It develops parallel transceiver power dissipation and area consumption models that illustrate the first effort to quantify the relationship between number of antennas and power dissipation and area consumption for multiple antenna systems.*

  The models incorporate propagation loss, RF circuit parameters that include power dissipation, area consumption and noise, and bit error rate simulation results for a multiple antenna wireless LAN system. These models are general and applicable to any multiple antenna system that exploits parallel subchannels.

- *It shows that the combined transceiver power dissipation can actually decrease*

with more antennas.

This situation occurs when RF transmit signal power generation dominates transceiver power dissipation and using additional transceivers increases SNR gain. This observation is a surprising and non-intuitive result that comes from the application of the power dissipation model with SNR gain.

- *It determines an optimal number of antennas that represent the first multiple antenna optimization based on transceiver power dissipation.*

A balance exists between a decrease in parallel transceiver power dissipation due to SNR gain and an increase in power dissipation due to multiple antenna overhead. This produces a minimal point that reaps the benefits from multiple antennas without wasting overhead. The model builds in a lower bound as it uses bit error rate simulation results that specify a minimum number of antennas necessary for a particular data and bit error rate. It adds an upper bound when it includes overhead power dissipation. Together, these two bounds produce an optimal number.

- *It introduces concurrently with [17] the idea to apply SNR gain at the receiver to lower power dissipation and area consumption but separately develops circuits that enable this application.*

Inherent in the balance is an application of SNR gain to lower RF transmit signal power. When the transmit signal power is large, this tremendously lowers parallel transceiver power dissipation by lowering power dissipation at the transmitter. When RF transmit signal power is already small or an area constraint limits a parallel transceiver design, the thesis applies a portion of SNR gain to lower operating power and area consumption, respectively, for parallel receivers, and does so through variable power and area-efficient low noise amplifiers. Depending on their percent consumption within a receiver, lowering power dissipation and area consumption for these circuits has the potential to considerably reduce power dissipation and area consumption for a receiver.

- *It implements the first multiple antenna parallel receiver RFIC that has been optimized for area consumption.*

  SNR gain application for WiGLAN parallel receivers produces a 5.22-GHz test chip that implements four independent receivers. Each area-efficient receiver is less than 1 mm^2 and consists of a resistor-based low noise amplifier, mixer, and local oscillator amplifier to reduce area consumption and uses a Q-enhanced notch filter to reject the image frequency. Bias and control circuits along with a global local oscillator amplifier supplies signal to all four receivers.

6.2 Future Research Directions

In addition to the discussions presented in this thesis, it is appropriate to consider how SNR gain is applicable to other parts of a receiver. Afterall, SNR gain offsets noise figure for an entire receiver and its application actually encompasses other receiver circuits. It is desirable then to develop a variable power receiver that consists of a low noise amplifier, mixer and other amplifiers that can lower its operating power. The challenges for this approach include not only understanding how the parameters for each circuit vary with power consumption but also how the interactions between the circuits change at lower operating power. On the other hand, an area-efficient receiver strictly based on SNR gain may not be possible. This thesis demonstrates a receiver that achieves area-efficiency through the application of SNR gain and the selection of receiver architecture and its input and output frequencies. In terms of noise figure, besides the low noise amplifier, there is no direct relationship between using on-chip inductors and noise for other circuits in a receiver.

At the transmitter, in a similar fashion to the receiver, it is desirable to lower power dissipation for other circuits beside the power amplifier. In this situation, it is necessary to develop a variable power transmitter. Such a transmitter most likely will have the same concerns as that of a variable power receiver in terms of how circuit parameters behave at lower power dissipation.

It is also desirable to lower area consumption at the transmitter. Similar to
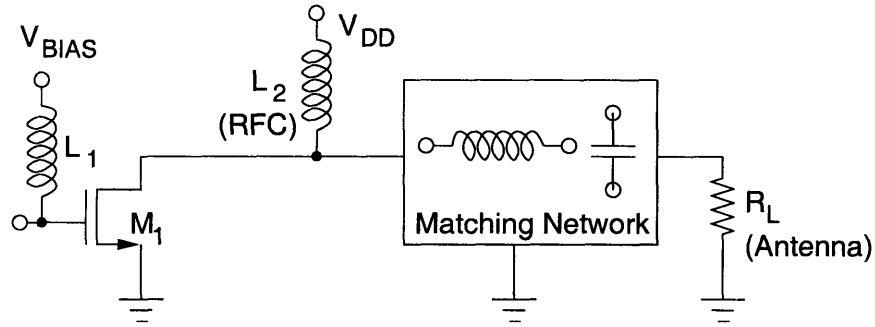
Figure 6-1: General power amplifier model [65]

a low noise amplifier, a power amplifier uses on-chip inductors. Fig. 6-1 shows a general power amplifier that is given in [65]. It consists of a common source amplifier with its DC gate voltage and drain current supplied through inductors L_1 and L_2. The inductors, especially L_2, are large in order to choke off RF signal to the power supply. An output matching network that consists of reactive components matches the amplifier's output to a load resistance R_L that represents the antenna. If the amplifier replaces its bias inductors with resistors, it increases its power dissipation and decreases the signal power to the load as a portion of RF signal leaks to supply. If it replaces inductors in the matching network, it degrades its power efficiency as harmonics in addition to the fundamental signal power reach the load [65]. As a result, the replacement of inductors decreases the efficiency for a power amplifier such that at the same power dissipation, there is less generated RF transmit signal power. SNR gain is applicable to offset this difference and its application has the potential to reduce area consumption at the transmitter.

Bibliography

[1] R. Stridh and B. Ottersten, "Spatial characterization of indoor radio channel measurements at 5 GHz," in *Proc. IEEE Sensors Array and Multichannel Signal Processing Workshop*, pp. 58–62, Mar. 2000.

[2] H. Sampath, S. Talwar, J. Tellado, and et al., "A fourth generation MIMO–OFDM broadband wireless system: design, performance, and field trial results," *IEEE Communications Magazine*, vol. 40, pp. 143–149, Sept. 2002.

[3] D. Gesbert, L. Haumonte, H. Bolcskei, and et al., "Technologies and performance for non-line-of-sight broadband wireless access networks," *IEEE Communications Magazine*, vol. 40, pp. 86–94, Apr. 2002.

[4] S. Catreux, V. Erceg, D. Gesbert, and R. W. H. Jr., "Adaptive modulation and MIMO coding for broadband wireless data networks," *IEEE Communications Magazine*, vol. 40, pp. 108–115, June 2002.

[5] M. Reudink and D. Reudink, "Smart antennas for broadband wireless access," in *IEEE Emerging Technologies Symposium: Broadband Wireless Internet Access*, pp. 1–5, Apr. 2000.

[6] R. L. Haupt, "The development of smart antennas," *IEEE Antennas and Propagation Society International Symposium*, vol. 4, pp. 48–51, July 2001.

[7] M. Zargari, D. Su, C. Yue, and et al., "A 5-GHz CMOS transceiver for IEEE 802.11a wireless LAN systems," *IEEE J. Solid–State Circuits*, vol. 37, pp. 1688–1694, Dec. 2002.

[8] D. Su, C. Yue, S. Rabii, and et al., "A 5GHz CMOS transceiver for IEEE 802.11a wireless LAN systems," *IEEE Internat'l Solid States Circuits Conference*, vol. 1, pp. 92–449, Feb. 2002.

[9] T. Meng, B. McFarland, D. Su, and J. Thomson, "Design and implementation of an all-CMOS 802.11a wireless LAN chipset," *IEEE Communications Magazine*, vol. 41, pp. 160–168, Aug. 2003.

[10] J. Thomson, B. Baas, E. Cooper, and et al., "An integrated 802.11a baseband and MAC processor," *IEEE Internat'l Solid States Circuits Conference*, vol. 1, pp. 126–451, Feb. 2002.

[11] M. Bohr, "Intel first to demonstrate working 45nm chips," *Press Release. www.intel.com/technology*, Jan. 2006.

[12] S. Nanda, R. Walton, J. Ketchum, M. Wallace, and S. Howard, "A high-performance MIMO OFDM wireless LAN," *IEEE Communications Magazine*, vol. 43, pp. 101–109, Feb. 2005.

[13] ITRS, "International technology roadmap for semiconductors," 2005. http://public.itrs.net.

[14] G. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, Apr. 1965.

[15] A. P. Chandrakasan, H. Lee, and C. G. Sodini, "Wireless gigabit local area network." Microsystem Technology Laboratories Annual Report, Cambridge, Massachusetts, 2002.

[16] D. Tse and P. Viswanath, *Fundamentals of Wireless Communication*. Cambridge University Press, draft ed., 2004.

[17] E. W. Huang, *Circuit-Aware System Design Techniques for Wireless Communication*. PhD dissertation, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, Feb. 2006.

[18] A. S. Y. Poon, *Use of Spatial Dimension for Spectrum Sharing.* PhD dissertation, University of California, Berkeley, Department of Electrical Engineering and Computer Science, 2004.

[19] A. Y. Wang, *Low Power RF Transceiver Modeling and Design for Wireless Microsensor Networks.* PhD dissertation, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, June 2005.

[20] D. G. Rahn, M. S. Cavin, F. F. Dai, and et al., "A fully integrated multiband MIMO WLAN transceiver RFIC," *IEEE J. Solid–State Circuits*, vol. 40, pp. 1629–1641, Aug. 2005.

[21] G. Chien, P.-B. Leong, S. W. Son, M. Tsai, and L. Tse, "A fully integrated dual band MIMO transceiver IC," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 99–102, June 2006.

[22] T. Yamaji, D. Kurose, O. Wanatabe, S. Obayashi, and T. Itakura, "A four-input beam-forming downconverter for adaptive antennas," *IEEE J. Solid–State Circuits*, vol. 38, pp. 1619–1625, Oct. 2003.

[23] J. Paramesh, R. Bishop, K. Soumyanath, and D. Allstot, "A 1.4V 5GHz four-antenna cartesian-combining receiver in 90nm CMOS for beamforming and spatial diversity applications," in *IEEE ISSCC Digest of Tech. Papers*, pp. 210–211, Feb. 2005.

[24] L. Khuon, E. Huang, C. Sodini, and G. Wornell, "Integrated transceiver arrays for multiple antenna systems," in *Proc. 61st IEEE Veh. Tech. Conf.*, pp. 892–895, May 2005.

[25] E. Huang, L. Khuon, C. Sodini, and G. Wornell, "An approach for area- and power-efficient low-complexity implementation of multiple antenna transceivers," *IEEE Radio and Wireless Symposium*, pp. 495–498, Jan. 2006.

[26] L. Khuon and C. Sodini, "An area efficient 5-GHz multiple receiver RFIC for MIMO WLAN applications," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 107–110, June 2006.

[27] M. Spaeth and H. S. Lee, "Massively parallel background calibrated high speed ADC for WiGLAN." MIT Center for Integrated Circuits and Systems Research Review, Cambridge, Massachusetts, May 2002.

[28] A. Y. Wang, "Base station design for a wireless microsensor system," master's thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, Sept. 2000.

[29] I. Cuiñas and M. G. Sánchez, "Measuring, modeling, and characterizing of indoor radio channel at 5.8 GHz," *IEEE Trans. Vehicular Technology*, vol. 50, pp. 526–535, Mar. 2001.

[30] J. K. Tan, "An adaptive orthogonal frequency division multiplexing baseband modem for wideband wireless channels," master's thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, May 2006.

[31] B. Razavi, "Design considerations for direct–conversion receivers," *IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing*, vol. 4, pp. 428–435, July 1997.

[32] W. Eberle, J. Tubbax, and B. C. et al., "OFDM-WLAN receiver performance improvement using digital compensation techniques," *IEEE Radio and Wireless Conference*, pp. 111–114, Aug. 2002.

[33] B. Razavi, *RF Microelectronics*. Prentice Hall PTR, 1998.

[34] J. K. Cavers and S. P. Stapleton, "A dsp–based alternative to direct conversion receivers for digital mobile communications," *IEEE Global Telecommunications Conference*, vol. 3, pp. 2024–2029, Dec. 1990.

[35] Sawtek, "Fundamentals of SAW transversal filters," *www.sawtek.com.*

[36] G. Riha, "SAW filters for radio communication systems," *Proc. IEEE International Symposium on Circuits and Systems*, pp. 1389–1394, June 1988.

[37] P. R. Gray and R. G. Meyer, "Future directions in silicon ICs for RF personal communications," *IEEE Custom Integrated Circuits Conference*, pp. 83–90, May 1995.

[38] T. Soorapanth and S. S. Wong, "A 0-dB IL 2140 ±30 MHz bandpass filter utilizing Q-enhanced spiral inductors in standard CMOS," *IEEE J. Solid–State Circuits*, vol. 37, pp. 967–977, May 2002.

[39] J. R. Long, "A low–voltage 5.1-5.8–GHz image–reject downconverter RF IC," *IEEE J. Solid–State Circuits*, vol. 35, pp. 1320–1328, Sept. 2000.

[40] J. Macedo, M. Copeland, and P. Schvan, "A 2.5 GHz monolithic silicon image reject filter," *IEEE Custom Integrated Circuits Conference*, pp. 193–196, May 1996.

[41] J. W. Rogers and C. Plett, "A completely integrated 1.8 Volt 5GHz tunable image reject notch filter," in *IEEE RFIC Symp. Dig.*, pp. 75–78, June 2001.

[42] F. Svelto, G. Montagna, S. Deantoni, and et al., "Solutions for image rejection CMOS LNA," *IEEE International Symposium on Circuits and Systems*, pp. 49–52, May 2000.

[43] H. Samavati, H. R. Rategh, and T. H. Lee, "A 12.4mw CMOS front–end for a 5GHz wireless-LAN receiver," *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 87–90, June 1999.

[44] H. Samavati, H. Rategh, and T. Lee, "A 5-GHz CMOS wireless LAN receiver front end," *IEEE J. Solid–State Circuits*, vol. 35, pp. 765–772, May 2000.

[45] S. P. Voinigescu, M. A. Copeland, D. Marchesan, and et al., "5GHz HBT mono-lithic radio transceiver with tunable filter," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 131–134, June 1999.

[46] J. Rogers and C. Plett, "A 5GHz radio front-end with automatically Q tuned notch filter," *IEEE Proc. Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 69–72, Sept. 2002.

[47] J. Willaim C. Black and D. A. Hodges, "Time interleaved converter arrays," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 1022–1029, Dec. 1980.

[48] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley & Sons, Inc., 1997.

[49] R. V. Nee and R. Prasad, *OFDM for Wireless Multimedia Communications*. Artech House Publishers, 2000.

[50] N. Matalon, "An implementation of a 5.25GHz transceiver for high data rate wireless applications," master's thesis, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, July 2005.

[51] G. Strang, *Linear Algebra and Its Applications*. Harcourt Brace Jovanovich, third ed., 1988.

[52] W.-J. Choi, Q. Sun, and J. M. Gilbert, "Circuit implications of MIMO technology for advanced wireless local area networks," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 185–188, June 2005.

[53] J. Liu, G. Vandersteen, J. Craninckx, M. Libois, and et al., "A novel and low-cost analog front-end mismatch calibration scheme for MIMO-OFDM WLANs," *IEEE Radio and Wireless Symposium*, pp. 219–222, Jan. 2006.

[54] H. Hashemi, X. Guan, and A. Hajimiri, "A fully integrated 24GHz 8-path phased-array receiver in silicon," *IEEE International Solid-State Circuits Conference*, pp. 390–391,534, Feb. 2004.

[55] Y. Palaskas, A. Ravi, S. Pellerano, B. Carlton, and et al., "A 5GHz 108Mb/s 2x2 MIMO transceiver with fully integrated +16dbm PAs in 90nm CMOS," *IEEE International Solid–State Circuits Conference*, pp. 362–363,659, Feb. 2006.

[56] T. S. Rappaport, *Wireless Communications*. Prentice-Hall PTR, 1996.

[57] F. Plessas and G. Kalivas, "A 5-GHz, variable gain, SiGe low noise amplifier," *Proc. 24th International Conf. on Microelectronics*, vol. 2, pp. 609–612, May 2004.

[58] M. Liu and J. Craninckx, "A 5-GHZ BiCMOS variable-gain low noise amplifier with inductorless low-gain branch," *Proc. of ESSCIRC*, pp. 223–226, Sept. 2005.

[59] T.-P. Liu and E. Westerwick, "5-GHz CMOS radio transceiver front-end chipset," *IEEE J. Solid–State Circuits*, vol. 35, pp. 1927–1933, Dec. 2000.

[60] B. Razavi, "A 5.2-GHz CMOS receiver with 62-dB image rejection," *IEEE J. Solid–State Circuits*, vol. 36, pp. 810–815, May 2001.

[61] K. O, "RF integrated circuits and technology," 2002. MIT class notes 6.976.

[62] S. Voinigescu, M. Copeland, D. Marchesan, P. Popescu, and M. C. Maliepaard, "5GHz HBT monolithic radio transceiver with tunable filter," in *IEEE RFIC Symp. Dig.*, pp. 131–134, June 1999.

[63] J. Rogers and C. Plett, "A 5GHz radio front-end with automatically Q tuned notch filter," in *IEEE Bipolar/BiCMOS Circ. and Tech. Mtg.*, pp. 69–72, Sept. 2002.

[64] J. Macedo and M. Copeland, "A 1.9-GHz silicon receiver with monolithic image filtering," *IEEE J. Solid–State Circuits*, vol. 33, pp. 378–386, Mar. 1998.

[65] A. D. Pham, *Outphase Power Amplifiers in OFDM Systems*. PhD dissertation, Massachusetts Institute of Technology, Department of Electrical Engineering and Computer Science, Sept. 2005.

[66] Agilent, "Noise figure measurement accuracy-the y-factor method," 2001. Application Note 57-2.

[67] X. He, *Fully Integrated Transceiver Design in SOI Process.* PhD dissertation, Kansas State University, Department of Electrical Engineering and Computer Engineering, 2004.