Development of the Recess Mounting with Monolithic Metallization Optoelectronic Integrated Circuit Technology for Optical Clock Distribution Applications

by

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Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

ELECTRICAL ENGINEER in ELECTRICAL ENGINEERING

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
[February 2007]
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Abstract

Recess mounting with monolithic metallization, or RM^3 integration, is used to integrate $In_{0.47}Ga_{0.53}As/InP$ based lattice-matched high quantum efficiency p-i-n photodetectors on silicon chips to build high performance optoelectronic integrated circuits [1]. In RM^3 integration, partially processed heterostructure devices are placed in recesses formed in the dielectric layers covering the surface of an integrated circuit chip, the surface is planarized, and monolithic processing is continued to transform the heterostructures into optoelectronic devices monolithically integrated with the underlying electronic circuitry.

Two different RM^3 techniques have been investigated, Aligned Pillar Bonding (APB) and OptoPill Assembly (OPA). APB integrates lattice mismatched materials using aligned, selective area wafer bonding at reduced temperature (under 350°C), which protects the electronic chips from the adverse effects of high temperatures, and reduces the thermal expansion mismatch concerns. In the OPA technique, optoelectronic heterostructures are processed into circular pills of 8 μm height and 45 μm diameter, the pills are released from the substrate, and collected through a process that involves decanting. The pills are then assembled into recesses on silicon chips using manual pick & place techniques, and they are bonded to the metal pads on the bottom surface of the recesses using a Cu-AuSn solder bond. A new magnet assisted bonding technique is utilized to obtain clamping pressure to form the solder bond. The gap between the pill and the surrounding recess is filled using BCB, which also provides good surface planarization.

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Chapter 1

Introduction

As the integrated circuit technology is being driven beyond the VLSI regime, transistor performance and integration density are no longer the primary limitations on the performance of digital systems. Rather, the electrical wires that interconnect the transistors within electronic systems determine the performance. Electrical interconnect limitations arise from the finite resistance, capacitance and inductance of the electrical conductors. For example, the electrical bus lines that carry data between chips on a multi-chip module (MCM) have to be operated at clock frequencies much lower than the on-chip clock rate due to the parasitics associated with the long metallic wires. As the clock frequencies are moving into the gigahertz regime, the on-chip global interconnects are also becoming very difficult to implement for similar reasons.

The electrical interconnect problems were first observed in long-distance communication systems in 1960s. After the invention of the semiconductor laser and the development of optical fibers, optical communication links that offer higher bandwidth and lower loss than electrical interconnects have become the backbone of long-distance communication channels replacing the electrical coaxial cables and copper wires. As it once revolutionized the long-distance communications, the use of optics can now offer solutions for several electrical interconnect performance limitations at shorter length scales that include the on-chip, chip-to-chip and board-to-board scales. In Section 1.1,

some of the motivations for the use of optical interconnects in digital systems are reviewed.

Unlike long-distance communication links where a single optical fiber, a discrete laser, a discrete photodetector, and separate driver and receiver electronics are well suited to the task, optics will be successful at small size scales only if the optical interconnect, the optical emitter and detector, and the electronics can be constructed together, i.e. integrated. Therefore, a key technology needed to realize such optical interconnects is the means of fabricating optoelectronic integrated circuits (OEICs), which closely couple VLSI-complexity electronics with large numbers of optoelectronic devices such as semiconductor lasers, light emitting diodes (LEDs), optical modulators and photodetectors. The central theme of this thesis is the development of an optoelectronic integration technology that is termed **R**ecess **M**ounting with **M**onolithic **M**etallization (RM^3). Section 1.2 surveys various optoelectronic integration techniques to understand the advantages and limitations of the OEICs made with RM^3 technologies in the context of optical interconnect system performance.

1.1 Electrical and Optical Interconnects

Low power dissipation, small latency, small physical size, and the ability to integrate with mainstream silicon electronics in large numbers are all required of optoelectronic devices for dense optical interconnects at the chip-to-chip and on-chip levels. To start the discussion of the benefits of optical interconnects to electronic chips in digital systems, it is important to understand some of the physical limitations to the scaling of electrical interconnections.

Conventional electrical interconnects possess resistance and capacitance, which determine the rise time of the signals. The finite rise times limit the rate at which the signals can be sent down the wire. If the bits are sent too close in time, they will overlap because of this finite rise time. An important issue here is that the rise times do not scale with the shrinking size of the electrical interconnects in VLSI systems [2]. The shrinkage of an electrical line in all dimensions by some factor makes no change in the RC time

constant of the line, and the lines cannot keep up with the transistors, which get faster as the feature sizes get smaller.

A similar problem arises for the longer inductive-capacitive (LC) lines such as the electrical interconnects at the chip-to-chip and board-to-board levels. The rise times on such lines are limited by skin-effect resistance, which becomes worse at high frequencies. The form of the rise time has a much longer tail for LC lines than the RC case, leading to worse problems with overlapping of successive bits. This particular form of tail arises from the frequency dependence of the effective resistance that results from the skin effect. For high-speed systems nearly all lines other than on-chip lines are LC lines. There is a drop by as much as a factor of 10 in the number of bits per second that can be transmitted by an LC line compared with an RC line for a certain interconnect cross-sectional area. Hence, the bandwidth limitation is a more urgent problem for off-chip electrical interconnects [3].

Optical interconnects do not suffer from this aspect ratio limit. The physics of loss and signal distortion in optical interconnection is completely different. Loss in optical media is essentially independent of the modulation bit rate, even into the terahertz regime. Optical attenuation can be relatively very small; it is negligible in free-space propagation over scales of meters, and in optical fibers over kilometers (e.g., 0.2 dB/km loss at 1550 nm wavelength). Optical systems readily exceed the electrical scaling limit derived here by multiple orders of magnitude. For example, a single-mode optical fiber, 125 μm in diameter and 15 km in length, would have only 3 dB of distance dependent loss. Sending signals at, for example, 100 Mb/s is simple and routine in such a system. A simple electrical interconnect with the same length and cross section would, according to the scaling analysis of this paper, be able to carry less than 0.1 bit/s of data [3]. More sophisticated optical systems can handle much greater distances and bit rates, with 160 Gb/s transmitted over 232 km of optical fiber.

The distance-dependent loss and distortion in an optically interconnected digital system is much easier to model and take into account. An optical interconnect can be taken over any distance in a digital electronic system without degradation. On the other hand, with electrical interconnects, connecting over any substantial distance is

increasingly difficult. Hence with optics, it is possible to take architectures and continue to scale them to higher clock speeds without having to deal with the problem of aspect ratio.

The cross-sectional area of an electrical interconnect largely determines its performance, and the aspect ratio limit constrains the maximum interconnect density that can be achieved with electrical interconnects. Fiber optical interconnects have an important advantage in this regard. Optical fibers are very compact (typical fiber outer diameter is 125 μm) and flexible and may be densely packed in one- and two-dimensional arrays. Fiber optic connectors are also more compact than electrical connectors, thus providing another advantage in density. Another aspect of optical interconnections that lead to a higher density is the ability to intersect optical paths. For example, in planar lightwave circuits, waveguides may intersect orthogonally without cross-talk. In free-space optics, where a transmission medium is not required, optical paths can be crossed arbitrarily.

The delay on optical signal or clock paths is not strongly dependent on temperature, and signal edges do not degrade substantially over tens of meters. By contrast, the effective delay in electrical lines depends on the temperature because the resistivity of metal depends on temperature. The rise time on electrical lines is proportional to resistance of the line, and the signal delay on RC lines is proportional to the resistance. In addition, gate delay varies with fabrication and temperature. In the case of optics, the propagation delay due to the finite velocity of light can still not be avoided, but the arrival time of optical signals is likely to be reliable and predictable.

There is also variability in delay from the driver and receiver circuits in both the electrical and optical cases. With the use of small optoelectronic devices integrated well with their electrical drive circuits, the optical circuits should have the same or fewer numbers of stages than their electrical counterparts, and hence comparable or better delay variation.

In general, in optics, the power consumption does not depend on the distance of signal propagation. By contrast, the power required to distribute signals or clocks with electrical interconnects will depend on the total length of the distribution lines. Optics

could eliminate the need for high-power clock driver circuits on chips. Telecommunication receivers, which are usually designed with large input capacitance and minimum detectable power, are too large and consume too much power for use in optical interconnections. With integration of relatively small photodetectors, relatively low power dissipation and small size are possible in optical interconnect receiver circuits. Optical output devices, such as quantum well modulators and Vertical Cavity Surface Emitting Lasers (VCSELs), must operate at relatively low power so that the transmitter circuits do not dissipate too much power. With quantum well modulators, total power dissipation in the range of a few milliwatts is also possible for transmitter circuits [4].

Conventional electrical interconnects suffer from mutual electromagnetic coupling effects. These effects become more severe as the signal bandwidth increases since the mutual coupling is proportional to the signal frequency. Photons do not generate stray electric and magnetic fields. With proper design, optical interconnects can offer communication links with extremely low cross-talk.

In conclusion, optics is a promising technology for high-density, high-speed interconnects typically required in modern computation and communication systems. However, the realization of optical interconnects can only be possible with high-density, high-speed and low-power optoelectronic integrated circuits.

1.2 Optoelectronic VLSI Technologies

The development of optoelectronic integrated circuits (OEICs) that combine large numbers of optoelectronic devices with VLSI-complexity electronics is the key technological challenge associated with the implementation of optical interconnects. The choice of specific optoelectronic and electronic devices to combine the high transmission bandwidth of optical signals and the information processing capacity of electronic circuits is the central theme in the development of an optoelectronic integration technology. Fundamental incompatibilities between the III-V compound semiconductors that are commonly used for optoelectronic devices (GaAs, InP, etc.), and silicon, the dominant electronic semiconductor material, have been an obstacle in the realization of OEICs. These incompatibility issues have resulted in the development of a number of

different optoelectronic integration technologies that can be broadly categorized as either monolithic or hybrid.

1.2.1 Monolithic Optoelectronic Integration

In the monolithic approach the optics and electronics are inherently proximal. The close proximity aspect of the monolithic optoelectronic integration can reduce the parasitics associated with contacts and interconnects, thus improving the performance of the optoelectronic circuits. The power dissipation of the optoelectronic circuit is also reduced since integrating all systems on the same chip eliminates the need for buffer electronics that drive off-chip output signals. In most applications, the production cost can also be reduced since the monolithic integration enables the easy packaging of the optoelectronic circuits [5].

Monolithic integration employs a common semiconductor substrate on which both electrical and optical devices are formed. Monolithic integration has proven difficult due to fundamental material incompatibilities as mentioned before. For example, VLSI complexity electronic circuits are often fabricated from silicon, which is a poor light emitter due to its indirect bandgap. On the other hand, semiconductor optical sources and detectors can readily be made from III-V compound semiconductors such as indium phosphide (InP) and gallium arsenide (GaAs) that are direct bandgap and have much better optical emission properties. The problem is that these two materials systems (silicon and the III-V's) are quite different and thus are difficult to integrate on the same chip. The lattice mismatch between different semiconductor materials can cause dislocations that often introduce deep-levels, which degrade the device performance. The dimensional change due to the heterogeneous thermal expansion not only induces large stress on a microscopic scale, but also makes it impossible to maintain macroscopic alignment of patterns. Coefficients of thermal expansion (CTE) and lattice constants of some of the materials used in this research are shown in Table 1-1.

Table 1-1: Material parameters of important semiconductors and dielectrics

Parameter	Si	GaAs	InP	$In_{0.53}Ga_{0.47}As$	SiO_2
Lattice constant (A°)	5.43095	5.65330	5.86860	5.86860	N/A
CTE (x 10^{-6} °C^{-1})	2.60	6.86	4.75	5.67	0.50

The recent progress in compound semiconductor VLSI fabrication has made it possible to build very high speed GaAs and InP based optical transmitter and receiver circuits. The availability of both electronic circuits and optoelectronic components such as lasers, LEDs and detectors in InP and GaAs based material systems is an important achievement towards the full monolithic integration of optoelectronic systems. However, the processing constraints of optoelectronic devices are typically inconsistent with standard VLSI fabrication even when the same kind of substrate is used to fabricate both the electronic circuits and the optoelectronic devices. For example, the optimum conditions demanded by the high quality epitaxial growth are often not compatible with the processing requirements of electronics. GaAs VLSI circuits using aluminum based metal interconnections cannot sustain any elongated processing at temperatures above 470°C [6].

For silicon-based electronics, thermal cycle above 550°C is also detrimental due to dopant diffusion and the degradation of ohmic contacts and metallization layers [7]. On the other hand, the temperatures required for optimal growth can be as high as 550°C-600°C for InP and 600°C-700°C for GaAs, and it is generally very difficult to grow high quality epitaxial layers on pre-processed electronic circuits without degrading the functionality of the electronic circuit [8].

Most commercial optoelectronic applications rely on hybrid integration, but there is considerable research effort to develop monolithic optoelectronic integration techniques because of the higher performance, lower packaging cost and lower power dissipation of monolithic OEICs. There are a number of approaches to monolithic optoelectronic integration.

1.2.1.1 Common epi-layers

In this technique, both the optical and the electrical devices are fabricated in the same epitaxial layers. For example, since HBT and laser diode heterostructures are similar, selected areas of the wafer can be processed into HBTs and other areas into laser diodes. Unfortunately, this approach does not allow for the independent optimization of both optical and electronic devices. In addition, poor planarity and electronic device uniformity restrict this technique to small to medium scale integration [8].

Alternatively, the optical and electrical device epitaxial heterostructures can be separated to avoid compromising optical and electrical device performance. Optical device layers, which are typically quite thick (3-8 μm), can be grown beneath the electrical device layers, which are typically thin (~1 μm), and this allows the independent optimization of the electrical and optical devices. A thin layer of material is removed to gain access to the thick layers in the lateral areas where optical devices are to be formed. The improved surface planarity of this process also allows the use of monolithic processing to complete the fabrication of the devices after the epitaxial growth is done. One drawback of this approach is that the electronic devices do not take advantage of the commercial electronics infrastructure [8].

1.2.1.2 Epitaxy-on-Electronics (EoE)

Epitaxy-on-Electronics is based on epitaxially growing the optoelectronic device layers on the host substrate of electronics, which are typically III-V compound semiconductors, in recesses opened down to the underlying wafer surface [8]. Removing the polycrystalline material, which is deposited on the surface of the chip during the epitaxy, leaves behind photonic epitaxial islands intermixed with the electronic devices. After the removal of the polycrystalline material, the top surface of the electronic chip is highly planar, and monolithic processing can be used to finish the optoelectronic device fabrication, and to interconnect with the pre-existing electronics on the chip. The EoE process is illustrated in Figure 1-1.

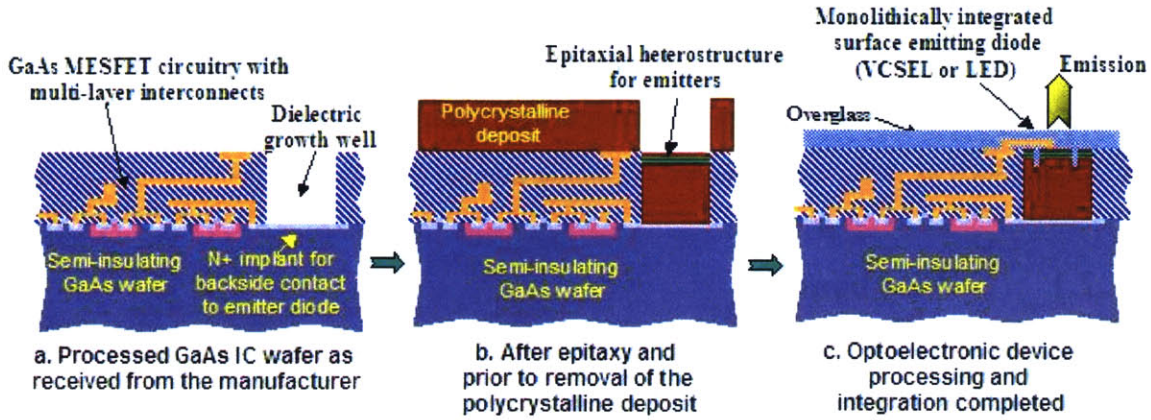

Figure 1-1: The Epitaxy-on-Electronics Process: a) Dielectric growth wells are opened on the back-end of the GaAs wafer, b) optoelectronic device epitaxy and the removal of the polycrystalline deposit from the surface of the chip, and c) after completing device processing and integration

The difficulty of obtaining very clean surfaces, required for high quality epitaxial growth, on the bottom of the dielectric growth window is an important limitation of Epitaxy-on-Electronics. The substrates used for electronic circuits are not as high quality as those used for optoelectronic devices, the ion implantation needed to form the back contact area introduces damage, and the growth surface can easily be damaged by the etch processes employed during the opening of the dielectric windows. Furthermore, Epitaxy-on-Electronics is restricted to GaAs and InP integrated circuits, and it is not suitable for CMOS chips due to lattice mismatch and heterogeneous thermal expansion when the electronic substrate used is silicon. EoE is also limited by degradation of the electronic circuits at elevated temperature, which limits the epitaxy temperature to under 500°C. These limitations of the EoE technology make it necessary to consider other RM^3 processes that do not require growing optoelectronic epitaxial layers on electronic substrates.

1.2.2 Hybrid Optoelectronic Integration

Monolithic integration offers a reduction in cost, an increase in functionality and an improvement in performance over hybrid circuits, but due to the limitations of the monolithic integration technologies described so far, most commercial optoelectronic

systems rely on hybrid integration. In the hybrid approach, the optics and the electronics are formed separately but are then packaged in close proximity. Hybrid integration brings together separately optimized optoelectronic and electronic parts through a variety of techniques such as wafer bonding, wire bonding and flip-chip bonding.

1.2.2.1 Wire bonding

The wire bonding technique involves the bonding of gold or aluminum wires between contact pads on different chips or assembly boards [10]. Die on the carrier or the substrate are moved through a wire bonder, and each bond is individually produced. The machine's pattern recognition system identifies the die, transforms and corrects the taught locations for each bond, and individually moves to each location to produce an interconnection. This makes wire bonding a costly operation for large-scale integration. For high frequency applications, this technique is also limited by the wire bond inductance. It may be possible to use the wire bond inductance to build noise-matching or inductive-peaking networks to improve the performance of the optoelectronic circuit, but this is more the exception than the rule, and lead inductance is in general a major limitation. An illustration of a wire-bonded optoelectronic device is shown in Figure 1-2.

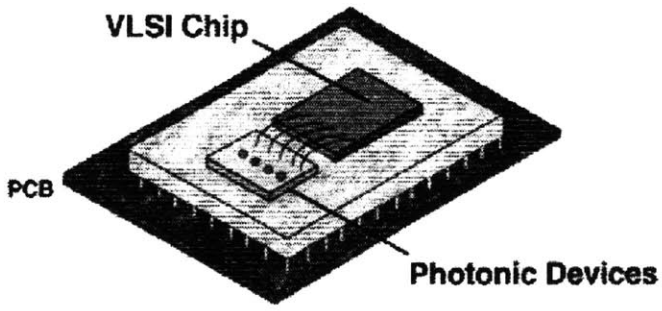

Figure 1-2: An illustration of a wire-bonded optoelectronic device

1.2.2.2 Flip-chip bonding

Currently, flip-chip bonding is the most mature technology for the combination of III-V optoelectronics with silicon integrated circuits. Like most other hybrid integration techniques, it allows the independent optimization of electronics and optoelectronic

devices. The basic technique of flip-chip bonding has been used for over thirty years as an alternative to the wire bonding of integrated circuits. In the basic flip-chip bonding technique, solder balls are applied to the IC bondpads, and the chip is brought into rough alignment with a package. The solder is then reflowed by heating, and the IC and package are pulled into proper alignment by the surface tension of the molten solder. The flip-chip bonding technique is preferred over wire bonding because of the reduced parasitics and a shorter assembly time [9-11].

While this basic technique is very well suited to the packaging of electronic die, two significant modifications have been made in applying it to OEIC fabrication. First, unlike conventional flip-chip packaging, the substrates of the optoelectronic die which are flip-chip bonded to form OEICs are typically removed, leaving individual free-standing devices. This is done in order to address the issues arising from the large thermal expansion mismatch between silicon and compound semiconductors. Second, suitable bondpads must be prepared on the optoelectronic sample. Common optoelectronic devices are highly non-planar. Producing contacts to both sides of the optoelectronic device is a challenging fabrication task, particularly given the high device densities that are desired and the bondpad co-planarity required for successful flip-chip bonding. Recently, three different techniques have been reported that address the co-planarization problem in the flip-chip optoelectronic integration process [12].

In the first technique, optoelectronic devices are fully processed before bonding, and the n- and p-contacts are formed in such a way that they are on the same plane as illustrated in Figure 1-3. In order to accomplish this, Au is electroplated on the n-contact to a height that is level with the p-contact. In addition to this, 5 μm of Au is deposited onto both the electroplated Au post and the p-contact. On the IC chip, Ti-Au-InSn is deposited onto the Al bonding pads. The bonding is done at 180°C, which melts the InSn contacts and bonds the two chips together. It is believed that the alloying of InSn with Au occurs during the bonding phase. After the bonding, the optoelectronic substrate is removed, leaving individual optoelectronic devices locally bonded to pads on the electronic chips.

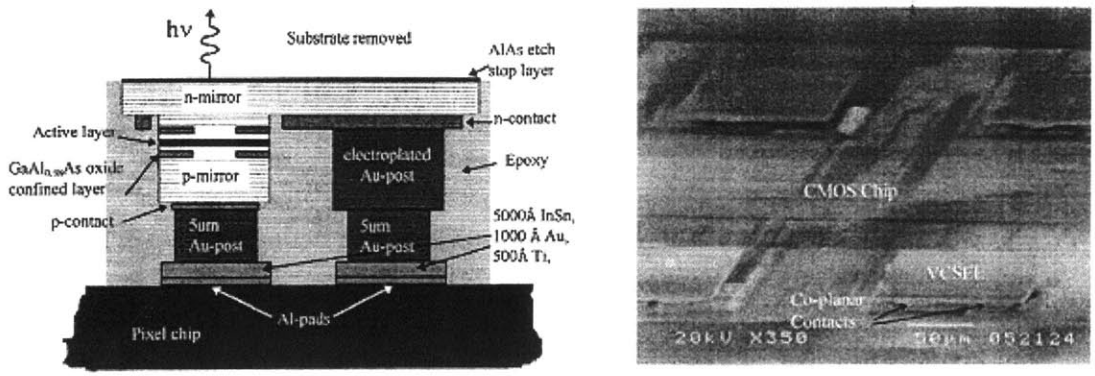

Figure 1-3: Illustration (left) and SEM (right) image of a coplanar bonded VCSEL on an electronic chip [12]

Electroplating for co-planarization of the solder bonds can be avoided by depositing Au posts onto pads on the electronic chip to the approximate height of the optoelectronic device in order to form part of the top contacts as can be seen in Figure 1-4. After the bonding, epoxy is flowed between the two chips, the optoelectronic substrate is removed, and the n-contact of the optoelectronic device and the metal trace between the n-contact and Au posts are deposited and annealed. Step coverage is not a serious problem since the epoxy provides a bridge between the optoelectronic device and the Au post.

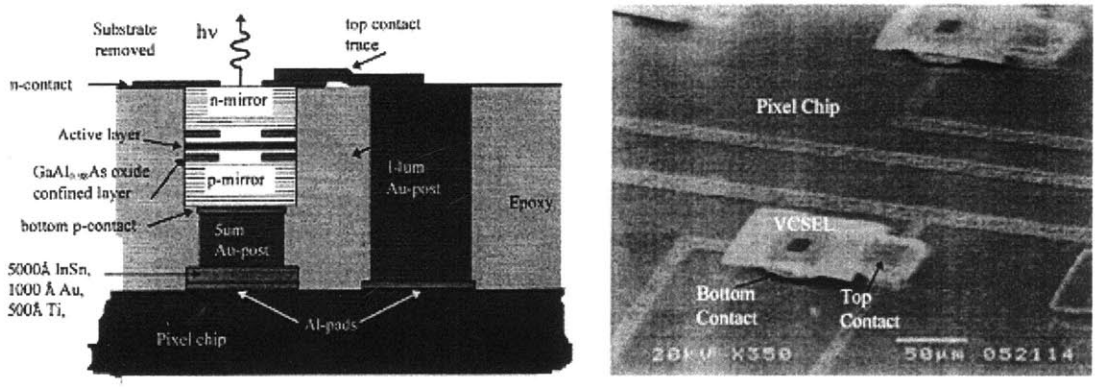

Figure 1-4: Illustration (left) and SEM image (right) of a top-bottom bonded VCSEL on an electronic chip [12]

Both of the methods described so far use tall metallic posts to achieve a level of co-planarity for generating electrical contacts to both sides of the optoelectronic device. The Au posts are usually electroplated and the height variations cannot be avoided. Beyond this, the electrical parasitics associated with these posts can limit the performance of the OEICs at high frequencies. The use of metallic bonding posts is eliminated in a third technique by attaching the optoelectronic wafer to the electronic chip by the help of an epoxy. After the attachment, the optoelectronic wafer substrate is removed and the remaining epitaxial layers are processed into optoelectronic devices as illustrated in Figure 1-5. The contacts are made to each side of the optoelectronic device, and polyimide is spun on and patterned to provide an insulating layer. Au is then deposited and patterned into traces that connect the p- and n-contacts to their corresponding bondpads on the electronic chips. However, the yield in this process is very low, and the non-planar top surface of the integrated complete OEIC prevents the fabrication of dielectric waveguides on top of the chip.

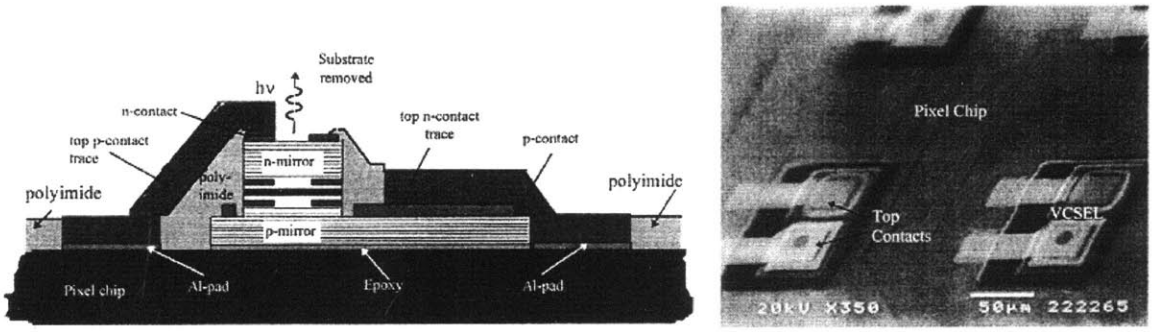

Figure 1-5: Illustration (left) and SEM image (right) of a top-contact bonded VCSEL on an electronic chip [12]

1.2.2.3 Wafer Fusion

In wafer fusion bonding, the surfaces of two mirror-polished wafers are prepared for the bonding process, and then brought into contact for bonding at room temperature in a sufficiently clean environment in order to avoid particles between the wafers. Directly after room temperature bonding, Van der Waals interactions or hydrogen bridge bonds

determine the adhesion between the two wafers. Higher bond energy, required for most practical applications, may be obtained by an appropriate heating step [13]. For compound semiconductor bonding, at temperatures as high as 1100°C, the Group III atoms diffuse along the two surfaces, and when the materials are cooled, they form the original compounds with the Group V elements on the other side of the interface resulting in a very strong covalent bond [14]. Lattice matching is not an issue for wafer bonding, but stress due to thermal expansion coefficient mismatch can lead to deformation of bonded wafers. Higher temperatures required for the covalent bonding can result in dopant diffusion and the degradation of ohmic contacts and the metallization layers; hence the two wafers must be fused together before the fabrication of the electronic circuits, requiring the development of a new VLSI technology. Therefore, wafer fusion is not a cost-effective way of building an optoelectronic integrated circuit technology.

1.3 Recess Mounting with Monolithic Metallization

The Recess Mounting with Monolithic Metallization (RM^3) technology overcomes most of the limitations of the flip-chip bonding techniques mentioned so far by bonding the individual optoelectronic devices into recess openings on the silicon integrated circuits. Modern integrated circuits have several layers of metallization, and in the RM^3 process, the top and bottom contacts of the optoelectronic devices can be made at different levels of IC metallization since the optoelectronic device mesas are placed into recesses etched in the dielectric back-ends of the electronic chips. This allows the use of vertical optoelectronic devices and avoids the tedious manufacturing process flow for making contacts to both sides of the optoelectronic device. In addition, it reduces the parasitics associated with the Au posts that are used for co-planarization before the bonding of the devices can take place. An illustration of an recess mounted optoelectronic device is shown in Figure 1-6.

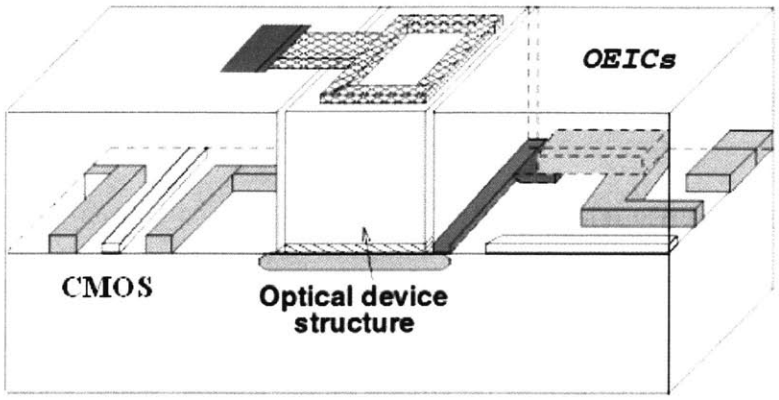

Figure 1-6: Illustration of an OEIC fabricated by Recess Mounting with Monolithic Metallization (RM^3) process

RM^3 allows the use of compound semiconductor based optoelectronic devices such as lasers and photodetectors on silicon chips. Although it is possible to make some of these optoelectronic devices, such as photodetectors, from silicon processes, the performance of the InP and GaAs based photodetectors are much better than the performance of silicon based photodetectors. In Chapter 2, it will be shown the performance of high-speed optical clock distribution can be significantly improved by using InGaAs/InP based photodetectors instead of integrated silicon photodetectors.

The major advantage of RM^3 over the flip-chip bonding technique illustrated in Figure 1-5 is the planar surface obtained by the RM^3 process. Both processes use metal traces to form the electrical interconnect to the top terminal of the device, and the bottom interconnect is fabricated using a larger pad. Therefore, the interconnect parasitics are comparable. However, the approach in Figure 1-5 results in a highly non-planar surface, and no further processing can be done on the wafer after the bonding of the optoelectronic device. In RM^3, the planar surface achieved after the integration allows the continuation of monolithic processing that can be used to fabricate integrated optical waveguides on the top surface of the chip to distribute the light signals.

In conclusion, RM^3 is a modified flip-chip bonding technique, which has advantages over the conventional optoelectronic flip-chip bonding techniques described in this section. Among these advantages are a simplified process flow, very good

planarization that leads to reduced top contact parasitics and lower packaging costs. In addition, the planar top surface of the OEICs fabricated by the RM^3 processes is very suitable for making integrated optical waveguides on top of the electronic chips.

1.4 Thesis Organization

The main concern of this thesis is the processing technology development for the Recess Mounting with Monolithic Metallization optoelectronic integration technology to integrate InP based heterostructures on silicon chips. Besides being a key component in the development of optical interconnects, an optoelectronic integration technology can also find applications in sensor arrays, wireless infrared local area networks and fiber-optical communications. In this thesis, the emphasis is on the development of the RM^3 optoelectronic integration technology to build optical interconnects. More specifically, the RM^3 concept is used for studying the integration of indium phosphide based lattice-matched photodetectors at 1550 nm wavelength with silicon chips for optical clock distribution applications. The issues regarding the conventional electrical clock distribution in modern digital CMOS chips are reviewed in Chapter 2, and the advantages offered by using an RM^3 process for optical distribution of the clock signals across a chip is examined. Chapter 2 includes a detailed analysis of the physics and operation of the p-i-n photodiode used in the integration work. This discussion includes the effect of using heterojunctions in the device layers, the derivation of the current voltage characteristics, responsivity, quantum efficiency and the frequency response. Two dimensional device simulations of the InGaAs/InP based p-i-n photodetectors are used to support the analysis of the photodetector.

Chapter 3 is the main chapter of the thesis, and it focuses on the technology development for the RM^3 process. RM^3 technology is an "exotic" process, and a series of new processing technologies were developed for the RM^3. Two major RM^3 processes researched in this thesis are the Aligned Pillar Bonding and OptoPill Assembly. Aligned Pillar Bonding is derived from the conventional flip-chip bonding techniques, and it utilizes an RDA M8 Flip-Chip Bonder instrument. OptoPill Assembly is based on manual assembly of OptoPills of p-i-n heterostructures on recesses opened on silicon chips. A

new solder bonding method using magnetic interaction forces is developed. Magneto-static simulations are used to quantitatively analyze this technique. Bonding experiments were carried out with the help of Mindy Teo [39c].

Chapter 2

Analysis of 1550 nm $In_{0.47}Ga_{0.53}As$/InP based p-i-n Photodetectors for RM^3 Applications

RM^3 integration techniques can be utilized in numerous optoelectronic applications including optical interconnects for on-chip and chip-to-chip clock and data distribution. This chapter starts with a discussion of the motivations for on-chip optical clock distribution, and it reviews the problems with the present clock distribution schemes. It then highlights how RM^3 can be used to advance the optical clock distribution concept by monolithically integrating high quantum efficiency, low capacitance, 1550 nm $In_{0.47}Ga_{0.53}As$/InP based p-i-n photodetectors on silicon chips. An analytical discussion of the photodetector is supported by ATLAS 2D device simulations that compute various electrical and optical characteristics of the photodetector.

2.1 Review of Conventional Clock Distribution on ICs

Clock distribution is a specific application of global signal distribution. The distinct characteristics of a clock signal are that it is periodic and predictable. However, in practical systems, clock signals do not arrive precisely at the same time everywhere on the chip. A clock signal that arrives slightly out of phase at different locations is skewed. Similarly, jitter refers to variation of arrival of the clock signal relative to an average

arrival time (clock period) from cycle to cycle. Skew and jitter are often due to static variation in circuit, device and interconnect parameters, dynamic variation in temperature and power supply fluctuation, and other sources, such as noise.

Reliable global clock distribution in high-speed microprocessors and ASIC circuits via electrical interconnects is becoming a serious issue with deep sub-micron CMOS processes. Clock signals in silicon VLSI circuits must be distributed to each flip-flop within the IC. The dense population of flip-flops leads to a complex clock distribution network, thus to increased relative device and interconnect variation resulting in clock skew and jitter across the chip. This problem is amplified by higher clock frequencies resulting in lower absolute skew and jitter budgets. On the other hand, parasitics such as high resistance of the interconnection combined with the capacitance due to decreasing wire dimensions and fringing fields imposes a significant RC delay factor for the long clock lines, limiting clock rates. The large current required to rapidly charge and discharge the total capacitance of the clock network along with the increasing numbers of repeater insertion limit the maximum clock rate due to power dissipation.

A number of methods have been developed to achieve low skew clock distribution with electrical interconnects. Existing schemes for electrical clock distribution such as H-trees and matched delay lines rely on symmetry to achieve minimal skew (difference in signal arrival times) across all leaf nodes on the chip. In principle, if all clock paths to flip-flops were of equal length and of equal impedance load, the clock skew would be zero (or minimal). However, even with balanced H-trees, process variability leads to significant amounts of skew. Furthermore, the clock signal received at different flip-flops is influenced by the routing of the clock interconnections among a dense set of data interconnections, switching increasingly rapidly as data rates evolve to Gbits/s on ICs. These neighboring, high-speed data lines couple a significant amount of cross-talk onto the clock lines. The specific cross-talk appearing at any single flip-flop depends on the specific path of the clock line to that flip-flop as well as the specific activity of data lines that couple to that path. As a result, large amounts of statistical modeling and optimization are required to design balanced H-Tree distribution schemes that achieve desired clock frequencies where skew and jitter budgets occupy a small, constant fraction of the clock cycle.

H-Trees are no longer sufficient to meet skew budgets with clock rates in excess of 1 GHz as process variability increases relative to shrinking process technologies. New designs utilize active deskew mechanisms, which operate by comparing distributed clocks with a carefully balanced reference clock. Distributed clocks are then adjusted through delay elements such that they are in phase with the reference clock, and the global skew has been reduced from 110ps to 28ps [15]. However, these mechanisms do not compensate for environmental (temperature and power supply) variation or noise, and they do little to mitigate jitter.

2.1.1 Optical Clock Distribution

Optical clock distribution to ICs has been studied for several years. As was mentioned in Chapter 1, the potential benefits optics has to offer include lack of parasitics (such as RC delays and crosstalks), higher potential frequencies due to lack of frequency dependent signal loss or distortion, lower power interconnects [2,3]. The use of optics to globally distribute a clock signal can help to reduce skew and jitter so long as the optical receiver circuitry is robust to the sources of variation mentioned before. Optical clocks can be transmitted in a tree using waveguides or in free space. Light can be distributed to multiple areas of the chip with very low skew. If this light can be reliably converted to an electrical clock signal, this method could serve as a good replacement for current electrical clock distribution techniques.

Up to the present, there has been not yet been a demonstration of completely integrated on-chip optical clock distribution networks. General approaches for on-chip optical clock distribution are illustrated in Figure 2-1 [16]. In the optical H-tree approach shown in Figure 2-1(a), optical waveguides replicate the H-Tree topology. The chip is divided into smaller sections, and each section consists of a photodetector and a receiver module. The externally applied global clock signal is distributed from the optical source to each section through waveguides. Once reaching the detector in each section, the optical pulses are converted into an electrical square wave matching the digital voltage levels on the IC, and conventional electrical interconnects continue the distribution of the clock.

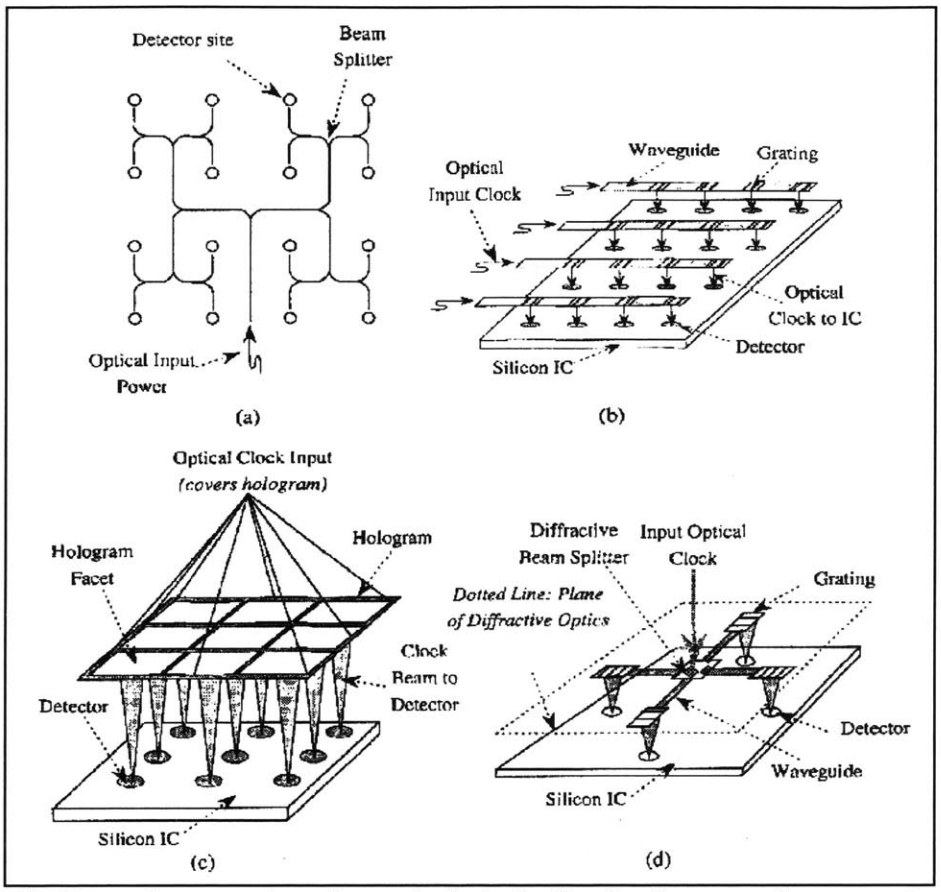

Figure 2-1: General approaches for optical clock distribution over the area of an IC: (a) Waveguide emulating H-tree, (b) Tapped waveguides, (c) Hologram distribution of clock, (d) Planar diffractive optics providing vertically optical clocks [16].

In Figure 2-1(b), a set of parallel waveguides traverse the IC, with diffractive elements redirecting a portion of the light onto underlying detectors. The resulting array of detectors looks like the approach in Figure 2-1(a), but with the condition of precisely equalized paths removed since the distance that light travels before reaching a photodetector depends on the layout of the optoelectronic chip and not the length of the waveguide [16].

In Figure 2-1(c), the optical clock signals are applied vertically (avoiding the need for fabricating waveguides on the IC surface) through use of a hologram. A restriction is that the hologram must be separated from the IC surface by approximately 1 cm, adding significant volume to the basic IC. In Figure 2-1(d), a planar optical unit (with diffractive optics, mirrors, etc.) is used to first distribute light in the plane of the unit, and then direct it vertically to the IC (with zero skew along the optical paths) [16].

Keeler et al. demonstrate a free-space distribution scheme, where femtosecond pulses are used for skew and jitter removal [17]. The impulse nature of femtosecond pulses make them ideal candidates for wavelength division multiplexing due to the large spectrum of frequencies contained in such a pulse. Additionally, as early as 1991, Delfyett et al. demonstrated optical clock distribution to 1024 ports via optical fiber [18]. Jitter between any two end-nodes in this system was measured below 12ps. Both of these systems may be applicable at a board-to-board or chip-to-chip level communication, but not for intra-chip communication. Optical fiber cores are on the order of 5 μm in diameter and are thus not practical for on-chip optical distribution.

At MIT, the research has focused on integrated on-chip silicon CMOS distribution networks. Sam designed a first-generation clock receiver circuit, which utilizes modified inverters as a primary means of amplification in 0.35 μm MOS process and silicon p-i-n photodetectors [19]. However, integrated silicon p-i-n photodetectors have small absorption coefficients, and thus they require a very thick intrinsic region or large areas due to their low responsivities. Lum designed a second-generation clock receiver circuit with a completely different architecture by using a bandgap reference and voltage regulator in a 0.18 μm CMOS process, which proved valuable in increasing robustness to environmental variation [20]. Lum's design uses Indium Phosphide (InP) based photodetectors, which are RM^3 integrated to a CMOS die. InGaAs/InP based photodiodes can be built with large responsivities using thinner (~1 μm) intrinsic regions, and they also allow for smaller photodetector areas (30 μm x 30 μm) and thus smaller diode capacitance.

2.2 Analysis of 1550 nm $In_{0.47}Ga_{0.53}As$/InP based p-i-n Photodetectors

All of these approaches for optical clock distribution favor a significant number of clock lines into the IC, requiring an optoelectronic integration technology that can be used to integrate large numbers of photodetectors with silicon VLSI circuits. The photodetector either must be made of silicon or be made in such as way that it can be integrated with a silicon die. Photodetectors made of silicon have the advantage of easy integration on a CMOS process. However, the low absorption coefficient of silicon at fiber-optic wavelengths makes it necessary to use a much thicker absorption region to obtain

sufficient photocurrent for efficient conversion into an electrical signal. Since the area of the photodetector is directly proportional to its capacitance, a large area photodetector also has high capacitance, which degrades the frequency response of the detector. A thick absorption region is also undesirable since it is hard to implement on a conventional CMOS process, and the transit times of carriers are proportional to the thickness of the absorption zone in a p-i-n photodiode. Beyond this, long minority carrier lifetimes degrade the bandwidth of silicon photodiodes in comparison with III-V semiconductors such as InP and GaAs.

The p-i-n photodiode made up of compound semiconductor materials has become the most widely deployed photodetector for all optoelectronic applications including OEICs. The quantum efficiency and the frequency response of a p-i-n photodiode can be optimized by changing the thickness of the depletion region, resulting in high quantum efficiency and low dark current devices most suitable for monolithic OEICs. High quantum efficiency leads to smaller acceptable device areas, and the capacitance of the III-V p-i-n photodetectors are very low compared with silicon photodetectors that provide the same photocurrent as output.

The study in this thesis involves an $In_{0.47}Ga_{0.53}As$/InP based lattice-matched p-i-n photodetector designed for operation at 1550 nm wavelength. The active region of the photodetector is a 1.1 μm-wide undoped (intrinsic) $In_{0.47}Ga_{0.53}As$[1] layer, which has bandgap energy of 0.74 eV at 300°K. The InGaAs layer is sandwiched between p-type and n-type InP buffer regions, thus forming a double heterojunction structure. This formation has the advantages of a higher breakdown voltage and a smaller reverse leakage current compared with a homojunction structure made up of narrow bandgap materials. When a heterostructure material is used, the incident optical power is mostly absorbed in the intrinsic region, and the wide bandgap buffer layers work merely as transparent windows. In this scheme, the InGaAs layer is depleted under the typical reverse-biased operation of the photodiode, and the carriers generated in this high field region are swept away by the electric field. The intrinsic region is encapsulated by two 0.05 μm spacer layers of intrinsic InP that serve as dopant diffusion barriers between the doped window layers and the intrinsic region. When a relatively thin top window layer is

[1] The InGaAs material referred in this document always has the composition $In_{0.47}Ga_{0.53}As$.

utilized, the light incident on the photodiode can penetrate this layer with minimum absorption. However, a thin window layer also results in a large sheet resistance. The thickness of the top window layer is chosen as 0.25 μm, a thickness that provides a good trade-off between sheet resistance and light absorption. The bottom window is thicker (5 μm) since it serves as a support base when the photodiode pill is released from the substrate.

The photodiode structure is encapsulated with a pair of InGaAs layers of 0.2 μm thickness. The narrow bandgap InGaAs exhibits low Schottky barrier heights for both n-type and p-type material, and for this reason, heavily doped InGaAs is often incorporated as a contact layer for InP based devices. Low Schottky barrier height of InGaAs makes non-alloyed contacts possible, which is desirable for RM^3 processes. The growth cross-section of the p-i-n heterostructure used in this thesis is shown in Figure 2-2.

0.2 μm p+ InGaAs contact (5E18 cm^{-3})
5 μm P+ InP buffer (5E18 cm^{-3})
0.05 μm InP spacer (un-doped)
1.1 μm InGaAs I-layer (un-doped)
0.05 μm InP spacer (un-doped)
0.25 μm N+ InP upper window (5E18 cm^{-3})
0.2 μm n+ InGaAs contact/etch stop (5E18 cm^{-3})
2.5 μm N+ InP buffer (5E18 cm^{-3})
N+ InP (100) substrate

Figure 2-2: The growth cross-section of the InP/InGaAs p-i-n heterostructure

The discussion in this chapter starts with a review of the heterojunction physics that governs the operation of the p-i-n photodiode. The electrical mobility and carrier generation-recombination models used in the simulations are presented. This is followed by an analytical discussion of the p-i-n photodiodes, which includes the derivations of the

DC photocurrent and the frequency response of the photodiode. Finally, two-dimensional ATLAS device simulations are used to characterize the electrical and optical response of the photodiode. First, energy-band diagrams are studied at different bias conditions. This is followed by DC bias sweep simulations that reveal the dark current and the turn-on voltage of the photodiode. AC small signal analysis is used to extract the device capacitance. LUMINOUS optical simulator is used in conjunction with ATLAS to calculate the DC photocurrent, intrinsic cut-off frequency and the optical transient response of the photodiode.

2.2.1 Semiconductor Physics for Heterojunctions

The physics of semiconductor devices are governed by the Poisson's equation, the continuity equations and the transport equations. Poisson's equation relates variations in electrostatic potential to local charge densities:

$$div(\varepsilon \nabla \varphi) = -\rho \tag{2.1}$$

where φ is the electrostatic potential, ε is the local permittivity, and ρ is the local space charge density. The electric field is obtained from the gradient of the potential:

$$\vec{E} = \nabla \varphi \tag{2.2}$$

The continuity equations describe the way the electron and hole densities evolve as the result of transport processes, generation processes and recombination processes:

$$\frac{\partial n}{\partial t} = \frac{1}{q} div \vec{J}_n + G_n - R_n \tag{2.3}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} div \vec{J}_p + G_p - R_p \tag{2.4}$$

In this set of equations, n and p are the electron and hole concentration, $\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the magnitude of the charge on an electron.

Derivations based upon the Boltzmann transport theory have shown that the current densities in the continuity equations may be approximated by a drift-diffusion

model, which is appropriate for most devices. In this case, the current densities are expressed in terms of the quasi-Fermi levels E_{fn} and E_{fp} as:

$$\vec{J}_n = \mu_n n \nabla E_{fn} \tag{2.5}$$

$$\vec{J}_p = \mu_p p \nabla E_{fp} \tag{2.6}$$

where μ_n and μ_p are the electron and hole mobilities. The quasi-Fermi levels are then linked to the carrier concentrations and the potential through the two Boltzmann approximations:

$$E_{fn}(x) = E_c(x) + kT \ln\left(\frac{n(x)}{N_c(x)}\right) \tag{2.7}$$

$$E_{fp}(x) = E_v(x) - kT \ln\left(\frac{p(x)}{N_v(x)}\right) \tag{2.8}$$

where $E_c(x)$ is the energy of the conduction band edge, $E_v(x)$ is the energy of the valence band edge, and N_c and N_v are the effective density of states in the conduction and valence bands, respectively. Conduction and valence band energies can be written as:

$$E_c(x) = -q\phi(x) - \chi(x) \tag{2.9}$$

$$E_v(x) = -q\phi(x) - \chi(x) - E_g(x) \tag{2.10}$$

where χ is the electron affinity and E_g is the bandgap energy. Substituting Eq. 2.9 into Eq. 2.7 yields:

$$J_n(x) = -n\mu_n q \frac{\partial \varphi}{\partial x} - n\mu_n \frac{\partial \chi}{\partial x} + \mu_n kT \frac{\partial n}{\partial x} - \mu_n kT \frac{n}{N_c} \frac{\partial N_c}{\partial x} \tag{2.11}$$

The last term is usually small, and it can be neglected. Identifying an effective electric field for electrons:

$$\vec{E}_{ex} = -\frac{1}{q} \frac{\partial E_c}{\partial x} \tag{2.12}$$

Using this last equation and the Boltzmann-Einstein relation, the transport equation for electrons can be written as:

$$J_n(x) = qn\mu_n \vec{E}_{ex} + qD_e \frac{\partial n}{\partial x} \tag{2.13}$$

Similarly for holes:

$$J_p(x) = qp\mu_p \vec{E}_{hx} - qD_h \frac{\partial p}{\partial x} \tag{2.14}$$

where the effective electric field for holes is given by:

$$\vec{E}_{hx} = \frac{1}{q}\frac{\partial E_v}{\partial x} \tag{2.15}$$

Finally, it should be noted that for homojunction materials:

$$\vec{E} = \vec{E}_{ex} = \vec{E}_{hx} \tag{2.16}$$

since the bandgap energy and the electron affinity are not dependent on the position variable. On the other hand, for heterojunction materials, the effective electric fields for holes and electrons can be different and this should be taken into account for the calculations. A more detailed discussion of heterojunction energy band diagrams is given in Section 2.2.5.1.

2.2.2 Electrical Mobility Model for InGaAs/InP Material System

The carrier mobilities μ_n and μ_p account for scattering mechanisms in electrical transport. In optoelectronic devices such as p-i-n photodiodes and modulators, electrons and holes travel with their saturation velocity, v_{sat}, under the influence of the applied bias. For compound semiconductors, the electron velocity, instead of monotonically attaining a saturation value, first reaches a peak value and then decreases and attains a saturation value. The negative differential mobility model is used to account for certain devices where the carrier drift velocity peaks at some electric field before reducing as the electric field increases [21, 22]:

$$\mu_n(E) = \frac{\mu_{no} + \dfrac{v_{satn}}{E}\left(\dfrac{E}{E_{critn}}\right)^{\gamma_n}}{1 + \left(\dfrac{E}{E_{critn}}\right)^{\gamma_n}} \tag{2.17}$$

$$\mu_p(E) = \frac{\mu_{po} + \dfrac{v_{satp}}{E}\left(\dfrac{E}{E_{critp}}\right)^{\gamma_p}}{1 + \left(\dfrac{E}{E_{critp}}\right)^{\gamma_p}} \tag{2.18}$$

where v_{satn} and v_{satp} are electron and hole saturation velocities, E_{critn} and E_{critp} are the critical electric field values where the mobility peaks, and μ_{no} and μ_{po} are the low-field electron and hole mobilities. Table 2-1 enlists the values of these parameters for the InGaAs/InP material system [23, 24] with a doping level of $5x10^{18}$ cm^{-3}, which is the doping of the heterostructure layers employed in this thesis. In Figure 2-3, carrier drift velocity is plotted as a function of the electric field for this material system.

Table 2-1: Electrical mobility model parameters for the InP/InGaAs material system

	μ_n (cm^2/Vs)	μ_p (cm^2/Vs)	$v_{sat,n}$ (cm/s)	$v_{sat,p}$ (cm/s)	E_{critn} (kV/cm)	E_{critp} (kV/cm)
InP	$4.6x10^3$	$1.5x10^2$	$6.7x10^6$	$5x10^6$	10	70
$In_{0.47}Ga_{0.53}As$	$2.1x10^4$	$4.3x10^2$	$8.2x10^6$	$5x10^6$	2.5	35

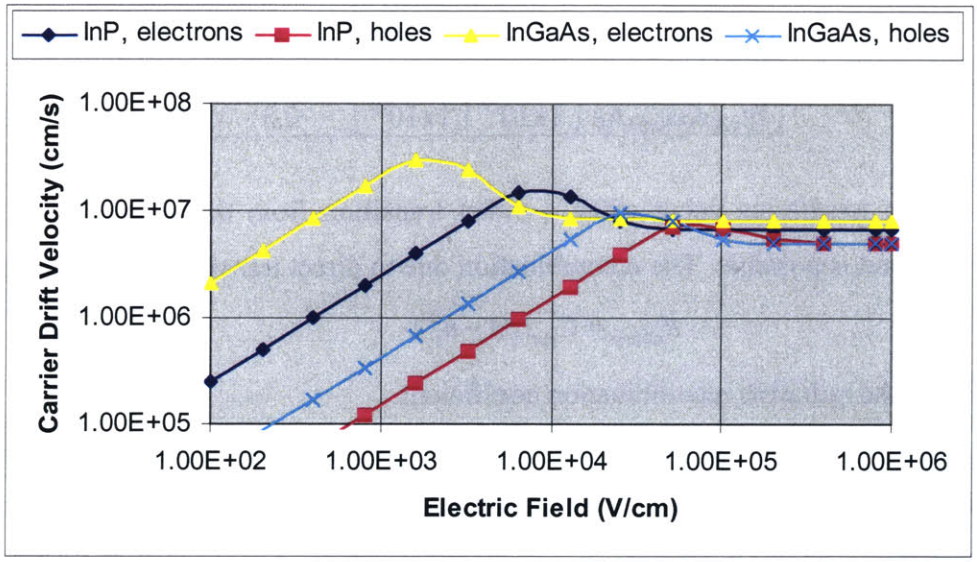

Figure 2-3: Velocity-field characteristics for carriers in the InGaAs/InP material system

2.2.3 Carrier Recombination Models

Carrier generation-recombination is the process through which the semiconductor material attempts to return to equilibrium after being disturbed from it. The most important processes responsible for carrier recombination in optoelectronic photodiodes are phonon transitions, photon transitions and Auger transitions.

Phonon transitions occur in the presence of a trap (or defect) within the forbidden gap of the semiconductor. Deep levels essentially act as carrier recombination or trapping

centers and adversely affect device performance. Deep levels can be produced by a variety of defects that include substitutional and interstitial impurity atoms, lattice vacancies, or complex defects formed by a combination of two types of defects. The recombination due to these defects is first derived by Shockley-Read-Hall, and it can be modeled as:

$$R_{SRH} = \frac{np - n_i^2}{\tau_{po}\left(n + N_c e^{-(E_c - E_T)/kT}\right) + \tau_{no}\left(p + N_v e^{-(E_T - E_v)/kT}\right)} \tag{2.19}$$

where E_T is the trap energy level, τ_{no} and τ_{po} are the electron and hole lifetimes. It should be noted that this model assumes only one trap level. The values of these parameters for the lattice-matched InP/InGaAs material system are shown in Table 2-2 [25].

Table 2-2: SRH recombination parameters for the InP/InGaAs material system

	T_{po} (s)	T_{no} (s)	E_{trap} (eV)
InP	$2x10^{-8}$	$1x10^{-8}$	0.3
$In_{0.47}Ga_{0.53}As$	$1x10^{-9}$	$1x10^{-9}$	0.3

Photon transitions occur when a direct transition from the valence band to the conduction band is possible. The recombination due to direct transitions is modeled as:

$$R_{direct} = C_{opt}(pn - n_i^2) \tag{2.20}$$

where C_{opt} is the radiative recombination coefficient.

Auger recombination occurs through a three-particle transition whereby a mobile carrier is either captured or emitted. Auger recombination is commonly modeled using the expression:

$$R_{Auger} = A_n(pn^2 - n_i^2 n) + A_p(np^2 - pn_i^2) \tag{2.21}$$

where A_n and A_p are the Auger coefficients. Table 2-3 lists the direct combination and the Auger recombination parameters of the lattice-matched InP/InGaAs system [26].

Table 2-3: Direct and Auger recombination parameters for InP/InGaAs material system

	C_{opt} (cm^3/s)	A_n (cm^6/s)	A_p (cm^6/s)
InP	$1.2x10^{-10}$	$9x10^{-31}$	$9x10^{-31}$
$In_{0.47}Ga_{0.53}As$	$0.96x10^{-10}$	$7x10^{-29}$	$7x10^{-29}$

The semiconductor equations that describe the carrier densities and current flow can be used in conjunction with the mobility model and the recombination models described so far to fully analyze the electronic and optical behavior of the p-i-n photodiode used in this thesis.

2.2.4 Analysis of Reverse Biased p-i-n Photodiode

The junction photodiode is always operated under reverse-biased conditions to form a wide depletion region at the heterojunction interface. This section includes the analytical derivation of the dc photocurrent and the frequency response of a p-i-n photodiode under reverse bias conditions.

2.2.4.1 DC Photocurrent

Light absorbed in different regions of a photodiode produce electron-hole pairs. In general, the photocurrent is the sum of two components. One is the current due to generation in the intrinsic region and within a diffusion length of it where almost all carriers generated are separated by the electric field, and their motion leads to current flow in the external circuit. The second one is the current due to the diffusion of holes and electrons generated in the quasi-neutral regions. In the case of an InGaAs/InP p-i-n photodetector, the generation in the n- and p- type InP quasi-neutral regions is very small due to the low absorption coefficient of InP at 1.55 μm wavelength. Therefore, the photocurrent is mostly determined by generation of hole-electron pairs in the intrinsic region. The pair generation rate, assuming η_i=1, is given by [21]:

$$G(x) = \varphi_o \alpha\, e^{-\alpha x} = \frac{P_{inc}(1-\theta_R)}{A\,h\,v}\,\alpha\, e^{-\alpha x} \tag{2.22}$$

where φ_o is the incident photon flux (photons/sec/cm^2), α is the absorption coefficient, P_{inc} is the power of the incident light wave, θ_R is the reflectivity of the top surface, A is the area of the diode, and hv is the energy associated with a single photon. The absorption coefficient and the reflectivity can be calculated from the real and imaginary components of the refractive index, respectively. The drift current can then be expressed as:

$$J = -q\int_0^W G(x)\,dx = -q\phi_o(1-e^{-\alpha W}) \tag{2.23}$$

where W is the width of the intrinsic layer.

The external quantum efficiency (η_{ext}) of the diode can be expressed as:

$$\eta_{ext} = \frac{\left|J/q\right|}{P_{inc}/Ah\nu} = \frac{\phi_o(1-e^{-\alpha x})}{\phi_o/(1-\theta_R)} = (1-\theta_R)(1-e^{-\alpha W}) \tag{2.24}$$

It is desirable to have a large depletion layer width so that all or most photons incident on the device can be absorbed in the intrinsic region ($\alpha W >> 1$). However, when the depletion region width is made too large, the transit time of carriers across this region will increase, thus increasing the response time of the photodiode. There is a trade-off between the responsivity of the photodiode, which is a measure of the photocurrent produced, and the bandwidth, which is related to the transit time of carriers, the junction capacitance, and the resistance of the diode and the circuit.

A low reflection coefficient at the top surface is desirable to attain high quantum efficiency. This can be realized by anti-reflection dielectric coatings, which have $\theta_R \approx 0$, but this method is not utilized in this thesis.

2.2.4.2 Frequency response

If the photodiode is designed to be sufficiently small, and still has the desired responsivity, then the frequency response, or bandwidth, is determined by transit time effects. This is because the photogenerated carriers require a finite time to traverse the depletion layer. The frequency response can be analyzed by making use of the continuity equations and current density equations from Section 2.2.1.

It is usually valid to assume that the transit time of carriers is much shorter than the bulk recombination lifetime, so that the recombination term can be neglected from the continuity equations. Another assumption is that due to the large electric field, the diffusion current can be neglected.

The incident photon flux is assumed to be of the form $\phi_{inc} = \phi_o + \phi_1 e^{j\omega t}$ and it is assumed that each photon produces one electron-hole pair (high internal efficiency). Then the generation rate and the carrier densities are given by:

$$\hat{G}(x,t) = G_o(x) + \hat{G}_1(x)e^{j\omega t} \tag{2.25}$$

$$p(x,t) = p_{dc}(x) + p_1(x)e^{j\omega t} \tag{2.26}$$

$$n(x,t) = n_{dc}(x) + n_1(x)e^{j\omega t} \tag{2.27}$$

where the subscript 1 denotes the incremental ac quantities and the subscript dc denotes dc quantities. With these assumptions, the continuity equations for ac quantities can be written as

$$\frac{\partial J_{e1}}{\partial x} - j\omega\frac{J_{e1}}{v_e} = -q\hat{G}_1 \tag{2.28}$$

$$\frac{\partial J_{h1}}{\partial x} + j\omega\frac{J_{h1}}{v_h} = q\hat{G}_1 \tag{2.29}$$

where v_e and v_h are the electron and hole saturation velocities and $\hat{G}_1 = \alpha\phi_o e^{-\alpha x}$. Solving for $J_{e1}(x)$ and $J_{h1}(x)$ and using the boundary condition $J_{e1}(0)=0$ and $J_{h1}(0)=0$ yields

$$J_{h1}(x) = -\alpha\, q\,\phi_o\left[\frac{e^{-\alpha x} - e^{-\alpha W + \frac{j\omega(W-x)}{v_h}}}{(\alpha - j\omega/v_h)}\right] \tag{2.30}$$

$$J_{e1}(x) = -\alpha\, q\,\phi_o\left[\frac{e^{\frac{jwx}{v_e}} - e^{-\alpha x}}{(\alpha + jw/v_e)}\right] \tag{2.31}$$

Solving for the short-circuit current, one can obtain:

$$J(w) = \frac{1}{W}\int_0^W (J_{e1}(x) + J_{h1}(x))\,dx \tag{2.32}$$

which by substitution of Eqs. 2.30 and 2.31 give

$$\begin{aligned} J(w) = {} & q\phi_o\alpha W\left[\frac{e^{-\alpha W} - 1}{\alpha W(\alpha W - jwt_{tr}^h)} + \frac{e^{-\alpha W}(e^{jwt_{tr}^h} - 1)}{jwt_{tr}^h(\alpha W - jwt_{tr}^h)}\right] \\ & + q\phi_o\alpha W\left[\frac{1 - e^{jwt_{tr}^e}}{jwt_{tr}^e(\alpha W + jwt_{tr}^e)} + \frac{1 - e^{-\alpha W}}{\alpha W(\alpha W + jwt_{tr}^e)}\right] \end{aligned} \tag{2.33}$$

where t_{tr}^e and t_{tr}^h are the electron and hole transit times, respectively. The transit times are determined by the thickness of the intrinsic region and the drift velocity of the carriers in the depletion region. The drift velocity of the carriers depends on the strength of the

electric field in the intrinsic region, which is set by the reverse bias applied on the photodiode and the thickness of the intrinsic region. Figure 2-4 shows the frequency response of the normalized current density as calculated from Eq 2.33. The thickness of the intrinsic region is 1.1 μm, and a reverse-bias of 1V is applied across the photodiode.

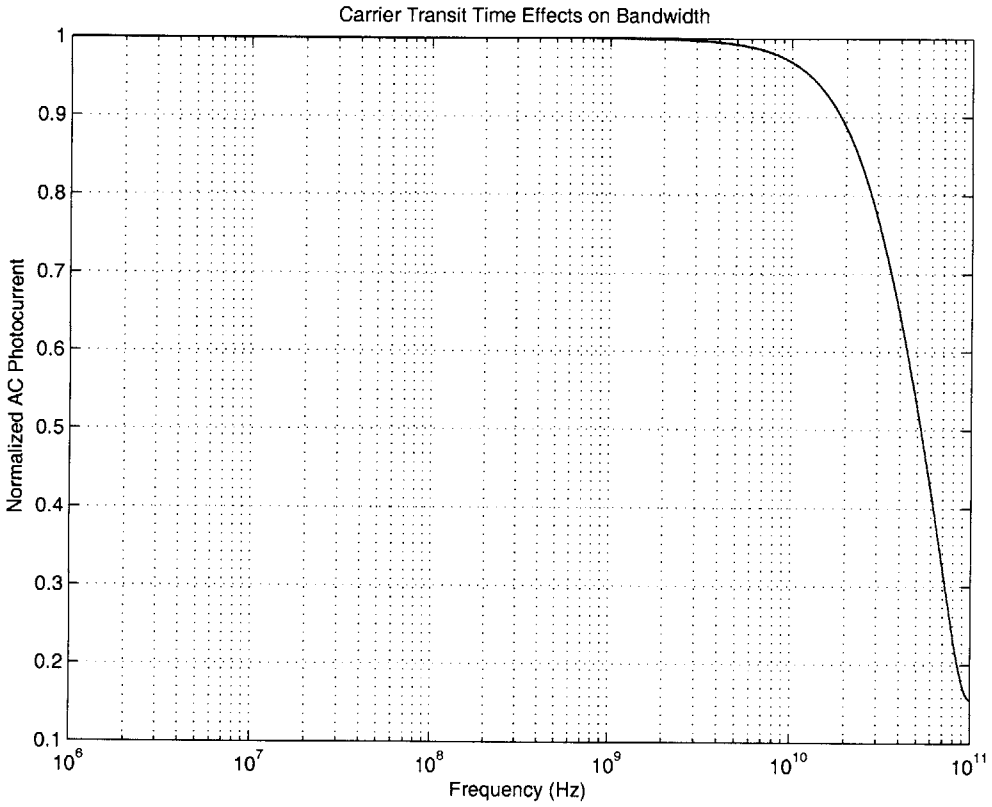

Figure 2-4: Bandwidth due to finite carrier transit time across the depletion region in the p-i-n photodetector (from Eq. 2.33)

The 3dB-down cut-off frequency is calculated to be 52 GHz from Eq. 2.33. This is much higher than the clock frequencies used in modern digital chips. Typically, the front-end circuits are designed to operate at a few GHz, and thus the bandwidth-limiting factor is not the intrinsic response of the photodiode. The current expressed in Eq. 2.33 gives the intrinsic frequency response of the photodiode. If the diode capacitance and other circuit parameters shown in Figure 2-5 are taken into account, the frequency response of these can be included in a transfer function H(ω) and the output current can be expressed as

$$J_o(\omega) = J(\omega)H(\omega) \tag{2.34}$$

where $J_o(\omega)$ is the output current across the load and $H(\omega)$ is the transfer function of the equivalent circuit, which can be derived as

$$H(\omega) = \frac{R_D}{a + j\omega b - d\omega^2} \tag{2.35}$$

where

$$a = R_s + R_D + R_L$$

$$b = R_s R_L C_p + (R_s + R_L) R_D C_j + R_L R_D C_p \tag{2.35}$$

$$d = R_s R_L C_p R_D C_j$$

In the equivalent circuit, C_j is the junction capacitance originating from the depletion region. R_D is the diode shunt resistance to model the dark current of the photodiode. It has a large value at zero and reverse biases and a very small value under forward bias. R_s is termed the series resistances of the diode, which is the sum of the contact resistances on each side and the undepleted regions of the photodiode. The RM^3 related parasitic is Cp, which is the parasitic capacitance between the metal bonding plate at the bottom of the recess and the substrate. R_L is used to represent the load.

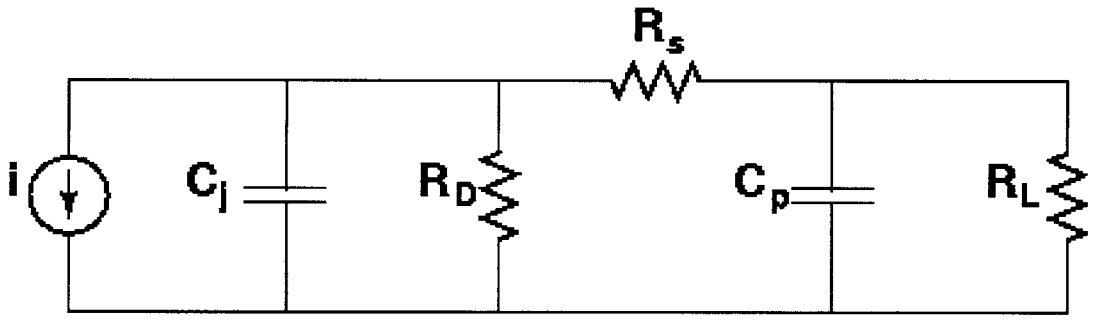

Figure 2-5: Equivalent circuit of a p-i-n photodiode

The contact resistance is estimated by using the data for InGaAs with the specific doping. The contact resistance is estimated as $1x10^{-4}$ Ω-cm^2 for p-type InGaAs with $5x10^{18}$ cm^{-3} doping, and it is $7x10^{-6}$ Ω-cm^2 for n-type InGaAs with $5x10^{18}$ cm^{-3} doping [27]. The ohmic contact on the p-side cover the entire bottom surface of the pill, and has a total area of 1590 μm^2, which results in a contact resistance of ~6 Ω. The ohmic contact

on the n-side is a square-shaped ring with a total surface area of 240 μm^2, which results in a contact resistance of ~3 Ω. Therefore, the total series contact resistance is estimated around 9 Ω. The resistances of the undepleted regions of the photodiode are very small (<1 Ω). The parasitic capacitance between the recess bond-pad and the ground plate, C_p, is estimated at 12 fF using the parasitic extraction tool of the Cadence IC design kit. This capacitance is very small compared with the as-designed capacitance of the p-i-n photodiode (~108 fF).

Figure 2-6 shows the 3dB frequency of H(ω) as the value of the load resistance varies. For load resistances above 500 Ω, the 3dB frequency is smaller than 5 GHz. Therefore, if a clock frequency of 5 GHz is desired, the transimpedance stage where the photodiode is connected to in an optical receiver circuit should exhibit an input impedance of less than 500 Ω in order to meet the bandwidth requirement.

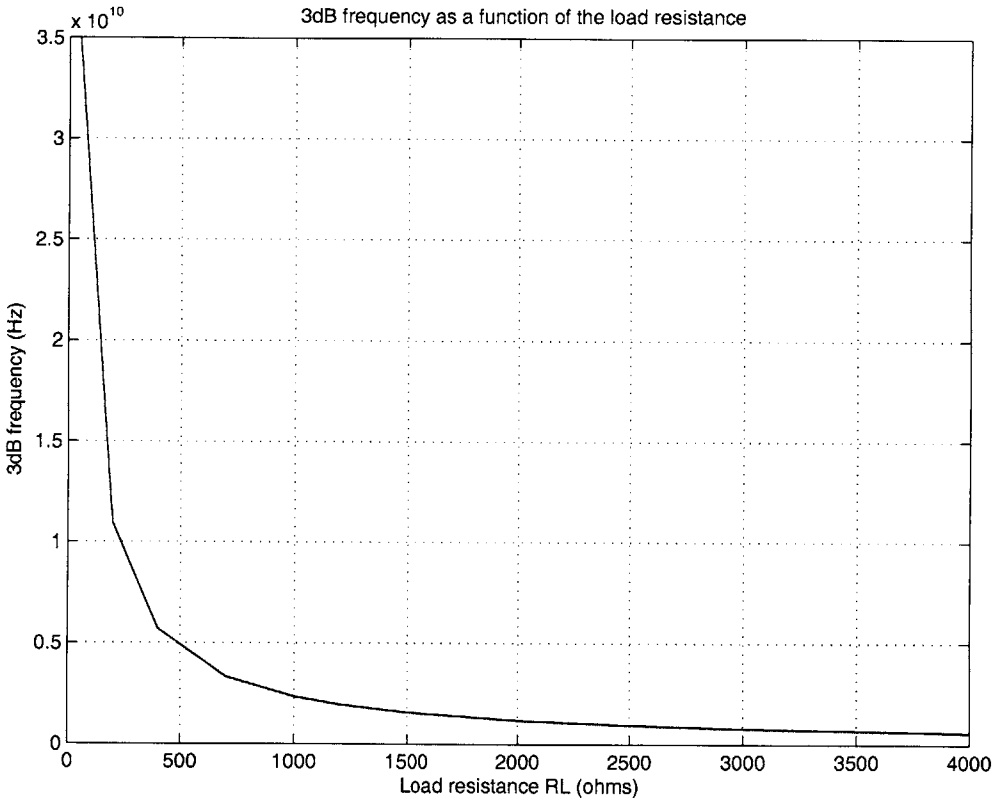

Figure 2-6: 3dB frequency as a function of the load resistance for the p-i-n equivalent circuit shown in Figure 2-5.

2.2.5 ATLAS Two-Dimensional Device Simulations

ATLAS is a physically based two-dimensional device simulator [28]. For the p-i-n simulations, a device structure is constructed using the ATLAS command language. First, a mesh is defined by a series of horizontal and vertical lines and the spacing between them. The regions within this mesh are allocated to different materials such as InGaAs and InP. After the regions are defined, the location of the electrodes is specified. In the final step, the doping profile in each region is specified.

2.2.5.1 Physical Definition of the Heterostructure

A two-dimensional mesh is defined to cover the physical simulation domain of the p-i-n photodiode. A finer mesh is constructed in and around the intrinsic region for numerical accuracy. The mesh is defined coarser in regions away from the intrinsic region to avoid convergence problems and to obtain a faster simulation. The mesh is a rectangle of 30-μm length and 6.35-μm height. The third dimension, the width of the device, is taken into account by using a scaling factor, which multiplies the current obtained from the 2D simulation of the mesh structure. The mesh structure is shown in Figure 2-7.

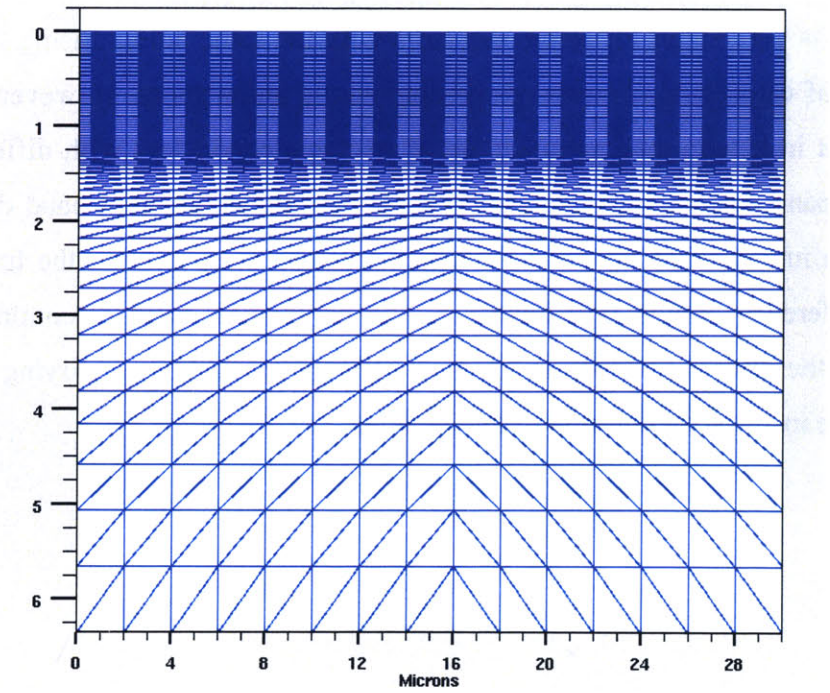

Figure 2-7: The ATLAS mesh structure of the p-i-n photodetector

After the mesh is specified, every part of the mesh is assigned to be a particular material type. For the p-i-n photodiode, this is either InP or InGaAs. The doping concentration is $5x10^{18}$ cm^{-3} for the buffer regions and $5x10^{15}$ cm^{-3} for the intrinsic region. All doping profiles are uniform. Two electrodes are defined on the top surface of the mesh to resemble a ring structure, which is the shape of the top contact to the actual photodiode. These two electrodes are electrically connected, i.e. shorted. The other electrode is placed along the bottom surface of the mesh. The contact resistances are specified as part of the ATLAS electrode definition.

For a heterojunction material, the difference in the two material bandgap energies creates conduction and valence band discontinuities as shown in Figure 2-8. The way that the bandgap difference is distributed between the conduction and valence bands has a large impact on the charge transport in these devices. The model proposed by Anderson assumes an ideal interface free of interfacial defect states. According to Anderson's model, the conduction band offset is equal to the difference between the two materials' electron affinities. In general, band offsets measured experimentally are very different from those obtained from the electron affinity rule. The common anion rule, which was proposed to explain the experimental data, states that the valence band discontinuity at the interface is very small for semiconductors with the same anion arising from the fact that the top of valence band states are predominantly anion states. However, it has been observed that in heterojunctions made up of two semiconductors with different anions, the valence band discontinuity is usually larger than the conduction band discontinuity. This is taken into account for the p-i-n heterostructure by specifying the fraction of the bandgap difference, which will appear as the conduction band discontinuity. In the simulations, the desired conduction bandgap offset is created by modifying the electron affinity of the material on one side of the junction.

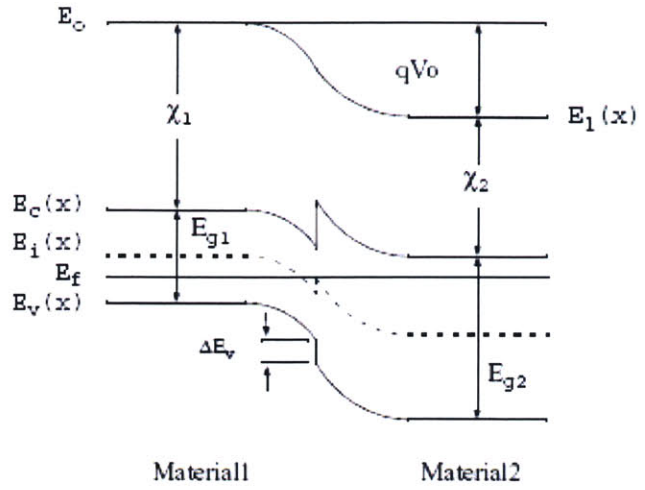

Figure 2-8: Energy band diagram of a pn heterojunction

For the InGaAs/InP material system, 43% of the bandgap difference is assigned to the conduction band discontinuity [29]. With this assumption, the energy band diagram of the p-i-n heterostructure under zero bias conditions is shown in Figure 2-9. The n-type region is on the left side of this figure and the p-type region is on the right side. Intrinsic region lies in the middle of these two buffer layers.

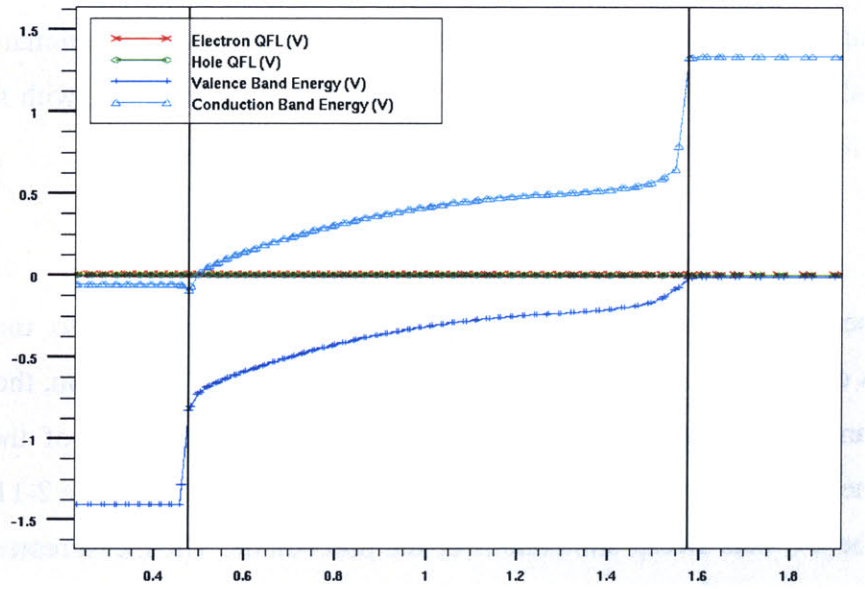

Figure 2-9: Energy band diagram of the p-i-n photodiode at thermal equilibrium

The energy band diagram under 1V reverse bias is shown in Figure 2-10. The large electric field that is formed in the depletion layer can easily sweep the carriers

generated in the depletion region into the buffer regions where they can diffuse towards the contacts. The quasi-fermi level splitting due to disturbance from the thermal equilibrium is evident in the intrinsic region.

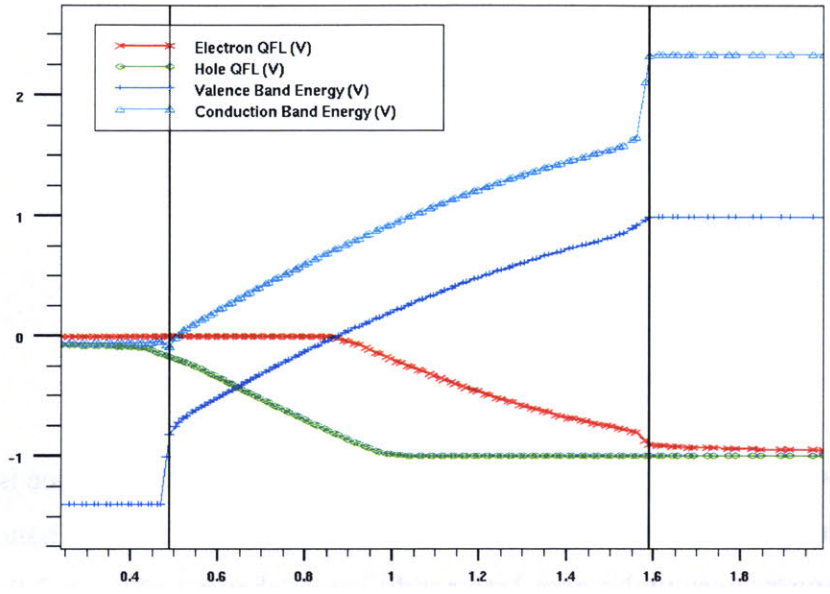

Figure 2-10: Energy Band Diagram of the p-i-n photodiode under 1V reverse bias

After the structure is completely defined, the simulation models are specified, which include the electrical mobility models, photogeneration and recombination models. The physical models previously defined in this chapter are used along with the material parameters for the InGaAs/InP system as tabulated before.

2.2.5.2 Electrical characterization

ATLAS uses the mesh structure along with the physical models to run electrical simulations of the device. This is done by solving the Poisson's equation, the continuity equations and the transport equations simultaneously at each point of the mesh by imposing the boundary conditions from the adjacent mesh points. Figure 2-11 shows the results of the DC bias sweep simulations of the photodiode. The measurements reveal a dark current of ~5×10^{-13} Amps, and a turn-on voltage of 0.7 V.

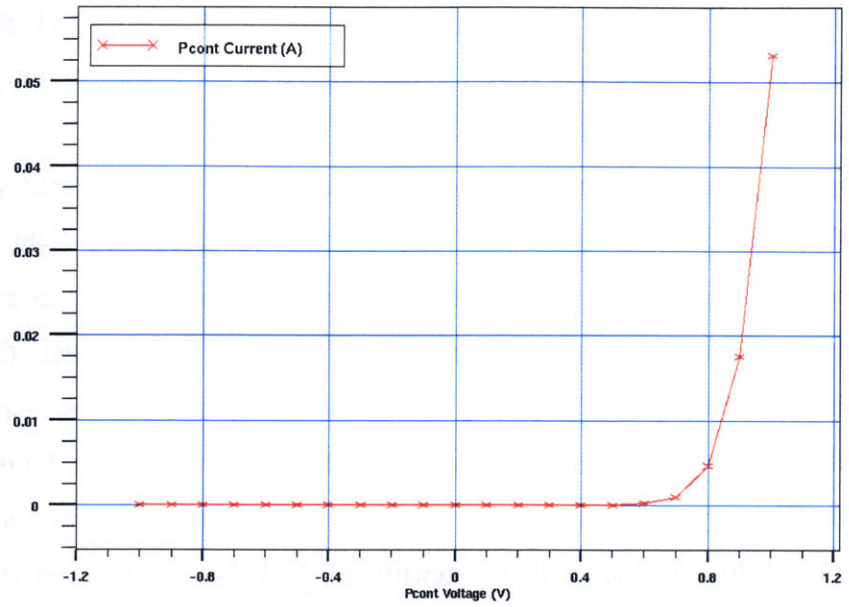

Figure 2-11: Current-voltage characteristics of the p-i-n photodiode

The capacitance of the p-i-n photodiode is evaluated by considering an ac small signal simulation. Under reverse bias conditions, the dominant capacitance is expected to be the depletion region capacitance, which can be written as

$$C = \frac{\varepsilon A}{d} \tag{2.36}$$

where A is the area of the photodiode and d is the thickness of the intrinsic region. With a photodiode area of 900 μm^2, and an intrinsic region thickness of 1.1 μm; the photodiode capacitance is 108 fF. This result is confirmed by the ac small signal simulations. ATLAS returns a conductance and capacitance matrix as the result of the ac simulations. This matrix is used to extract the C-V characteristics of the photodiode at 1 GHz

2.2.5.3 Optical characterization

The photocurrent output of the photodiode is determined by a light source simulation. ATLAS uses LUMINOUS, a ray trace and light absorption program, for optical simulations [27]. Luminous calculates optical intensity profiles within the semiconductor device and converts them into photogeneration rates in the device simulator. In general, optoelectronic simulation is split into two parts. The optical intensity profiles within the semiconductor device are calculated using optical ray trace with the real component of

the refractive index. Photogeneration models using the imaginary part of the refractive index is utilized to calculate a new carrier concentration at each point in the grid. This is followed by an electrical simulation.

An optical beam is defined as a collimated source, and it is split into rays as defined in the optical beam statement. The cumulative effects of light absorption, reflection and transmission are saved for each ray, and this is used to calculate the photogeneration rate at each point in the grid. From this information, the quantum efficiency, photocurrent, optical frequency and transient responses can be extracted.

The light source is defined as a single ray that originates from 1 μm above the photodetector. The ray spans the entire width of the device. The ray has a single wavelength (1550 nm) and an optical intensity of 1 W/cm^2. Reflection from the top surface of the photodiode is taken into account by using the real part of the refractive index to calculate the reflected and transmitted components of the incident optical ray.

After the optical source had been defined, the photocurrent was calculated by simulating an I-V measurement in the presence of the light source. A photocurrent of 7.5 μA is revealed for 1V reversed-bias condition. This bias is typical for the circuit nodes where the photodiode will be connected. Current-voltage characteristics of the photodiode under illumination are shown in Figure 2-12. The increase in the current in the reverse bias regime is due to the photogeneration in the depletion region.

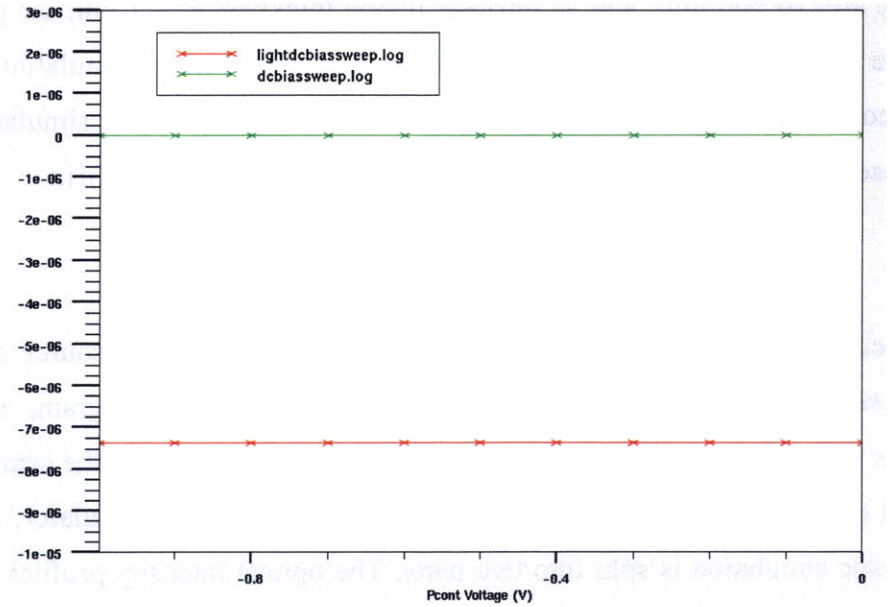

Figure 2-12: DC Photocurrent of the p-i-n photodiode

The quantum efficiency was calculated by dividing the measured photocurrent with the source photocurrent. Source photocurrent is readily available in the simulation output of ATLAS. ATLAS calculates the source photocurrent by if every photon eminent from the source would create exactly one electron-hole pair. The source photocurrent for the photodiode is 11.22 μA, which results in a quantum efficiency of 66%. This is high compared with the quantum efficiency of silicon-based photodiodes (4-5%).

The cut-off frequency of the photodiode was calculated using an AC optical source simulation, which revealed 4.5 GHz intrinsic cut-off frequency with a 500 Ω load resistance, which is the same as the input impedance of the TIA stage used by Lum [20]. The simulated frequency response of the p-i-n photodiode is shown in Figure 2-13.

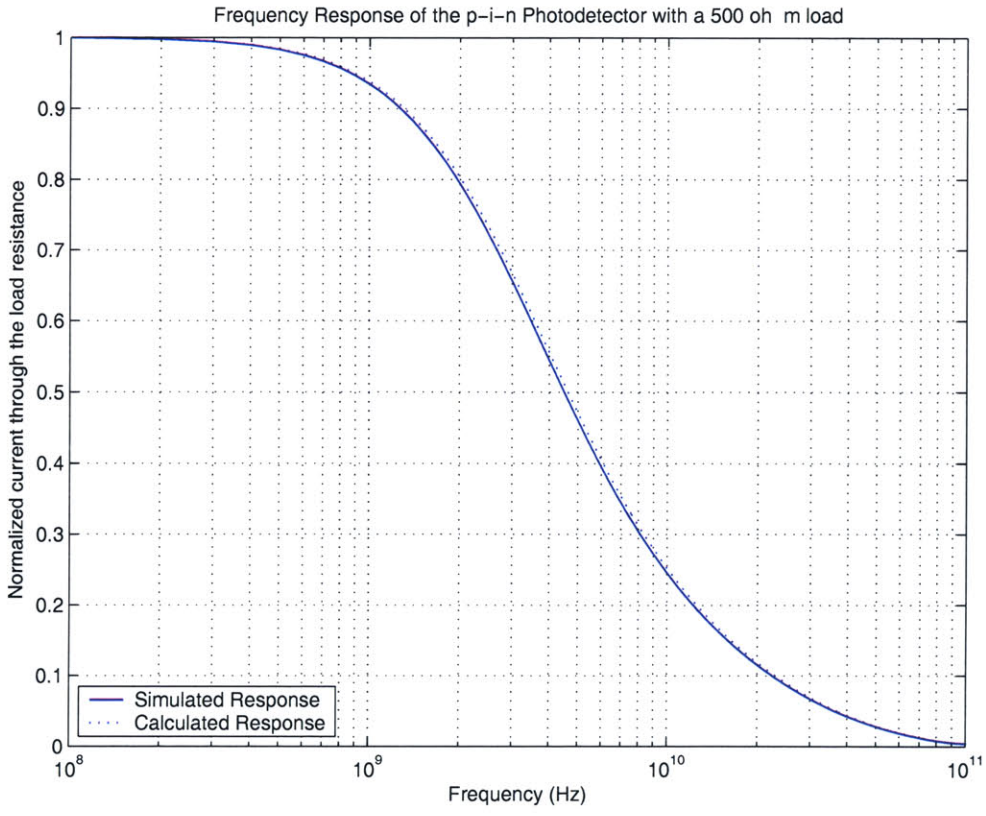

Figure 2-13: Optical frequency response of the p-i-n photodiode

In the final step, the transient characteristics of the photodiode were studied. The transient response shows the rise and fall times of the current in response to an optical

square wave input source. The optical transient response of the photodiode is shown in Figure 2-14. The simulated input light source has 50% duty cycle. The input source is displayed in the upper half of the figure. The simulated output current through a 500 Ω load resistor connected to the photodetector is shown in the lower half of the figure. The output of the photodiode has a rise and fall times of 100 ps. The rise and fall times are defined as the time it takes for the output to go from 10% to 90% of its final value.

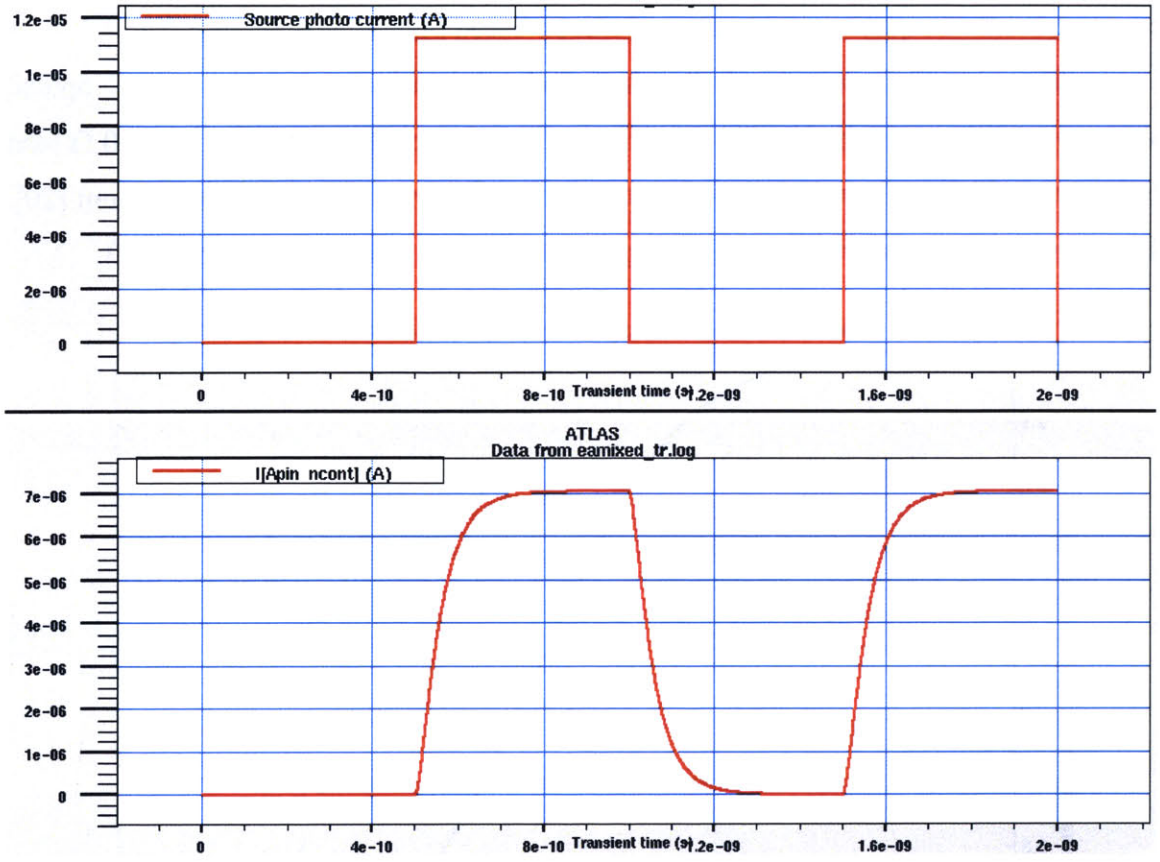

Figure 2-14: Optical transient response of the p-i-n photodiode: The top plot shows the source photocurrent and the bottom plot shows the output current of the photodiode in response to this optical input.

In general, the cut-off frequency (f_{3dB}) can be related to the rise time (t_r) through:

$$f_{3\,dB} = \frac{\Gamma_d}{2\,\pi\,t_r} \tag{2.37}$$

where Γ_d has the value 2.8 [21]. This result is obtained using Fourier transforms [21]. This result is in agreement with the 4.5 GHz cut-off frequency and the 100 ps rise/fall times obtained with the simulations.

2.2.5 Summary of the Results

The goal of this chapter is to provide background information on the physics and operation of the InGaAs photodetector used in this research work. Analytical calculations and device simulations are used to identify the photocurrent, the 3dB bandwidth, the quantum efficiency, and the transient response of the photodetector. As expected from an InGaAs based photodetector, a high quantum efficiency of 66% is obtained. Silicon based photodetectors usually have much lower quantum efficiencies (<10%), but it should be noted that the advances in optoelectronic silicon research such as the use of germanium doping, strained silicon and silicon nanocrystals can result in higher quantum efficiencies for silicon based photodetectors.

As it was shown in this chapter, the 3dB bandwidth of the photodetector is determined by the device area and the thickness of the intrinsic region. The use of a higher quantum efficieny photodetector results in an improved bandwidth as the device area can be reduced to obtain the same photocurrent.

The photodector has a transient response that is characterized by 100 ps rise/fall times. For digital applications, rise/fall times should be small compared with the clock period. A factor of 10 is considered good, which corresponds to a 1 GHz clock rate. For faster clock rates, the photodetector's bandwidth should be improved according to Eq. 2.37. For example, for a modern CPU with 5 GHz clock speed (i.e. 200 ps clock period), the rise/fall times of the clock signal should be at most 20 ps, which corresponds to a photodetector bandwidth of ~22 GHz, which is roughly five times the RC bandwidth of the photodetector designed in this thesis. As it is mentioned in Section 2.2.4.2, the RC bandwidth of the photodetector is mainly determined by the junction capacitance and the load resistance. The RC bandwidth can be improved either by making the junction capacitance small or by lowering the load resistance. The sensitivity specification of the front-end circuit can be used to derive the total photocurrent that the photodetector should supply, and a higher output current usually necessicates a larger area photodetector as the other two parameters, the quantum efficiency and the thickness of the intrinsic region, are more difficult to control than the device area. The photodetector used in this thesis has a very high quantum efficiency (66%), and it is hard to make the intrinsic region 5 times

thicker to lower the junction capacitance by the same factor. This is because the total thickness of the photodetector is constrained in an RM^3 process as it is discussed in Chapter 3. Therefore, both the area of the photodetector, which determines the output current, and the load resistance are to be controlled by the circuit designer to meet with the specifications of the clock receiver circuit in hand.

It can be concluded that the InGaAs/InP based p-i-n photodetector described in this chapter is suitable for use in an RM^3 process due to its high quantum efficiency, large bandwidth and fast transient response.

Chapter 3

Recess Mounting with Monolithic Metallization Technology Development

Monolithic OEICs offer performance and cost advantages over hybrid optoelectronic integration techniques such as wire bonding and flip-chip assembly. However, fundamental incompatibilities between III-V compound semiconductors and silicon have been an obstacle in the realization of OEICs based on silicon integrated circuits, and a number of heterogeneous monolithic optoelectronic integration technologies have been developed. Some of these techniques were mentioned in Chapter 1.

A new optoelectronic integration technology, recess mounting with monolithic metallization, or RM^3 integration, is developed to integrate III-V photodiodes on silicon chips for optical clock distribution applications. In RM^3 integration, partially processed heterostructure devices are placed in recesses formed in the dielectric layers covering the surface of an integrated circuit chip, the surface is re-planarized, and monolithic processing is continued to transform the heterostructures into optoelectronic devices monolithically integrated with the underlying electronic circuitry. At present, two different RM^3 techniques exist: Aligned Pillar Bonding, and OptoPill Assembly. This chapter presents the processing technology development for Aligned Pillar Bonding and OptoPill Assembly.

3.1 Aligned Pillar Bonding (APB)

Aligned Pillar Bonding overcomes some of the limitations of Epitaxy-on-Electronics by integrating lattice mismatched materials using aligned, selective area wafer bonding at reduced temperature (~ 300°C - 350°C). APB involves bonding of an epitaxially grown wafer with the desired optoelectronic device layer onto another wafer with VLSI density electronic circuits on it. APB inherits the advantages of flip-chip bonding techniques in that the optoelectronic and the electronic components are fabricated under their optimal conditions, and integrated by reduced temperature metal assisted bonding. Low temperature bonding protects the circuits and optoelectronic devices from thermally induced damage, and reduces the thermal expansion mismatch concerns.

A schematic illustration of the APB technique is given in Figure 3-1. The optoelectronic heterostructure is grown on a lattice-matched substrate under optimal epitaxial conditions, and the structure is patterned into relatively tall mesas that are called "pillars", hence the term Aligned Pillar Bonding. Pillars can be prepared with metal cap layers on the top when solder bonding is utilized for bonding the pillars onto the electronic wafer. The pattern of these pillars across the wafer is the mirror image of the recess openings on the dielectric surface of the electronic circuit chip. The bottom of the recesses is metallized for bonding. Next, the pillar wafer and the electronics wafer are oriented face-to-face, the pillar and recess patterns are aligned, and the two wafers are brought into contact and bonded by applying pressure. If the bonding is successful, an epoxy is flowed between the chips and allowed to harden. The purpose of this epoxy is to protect the front face of the electronic chip from the subsequent optoelectronic substrate removal etch. Furthermore, an epitaxial etch stop layer is utilized within the optoelectronic device to protect the actual device layers from the wet etch. After the optoelectronic substrate is removed, the excess epoxy is etched in oxygen rich CF_4 plasma, and the OEIC fabrication is completed monolithically as in EoE. This section will continue with a discussion of the process modules developed for the APB.

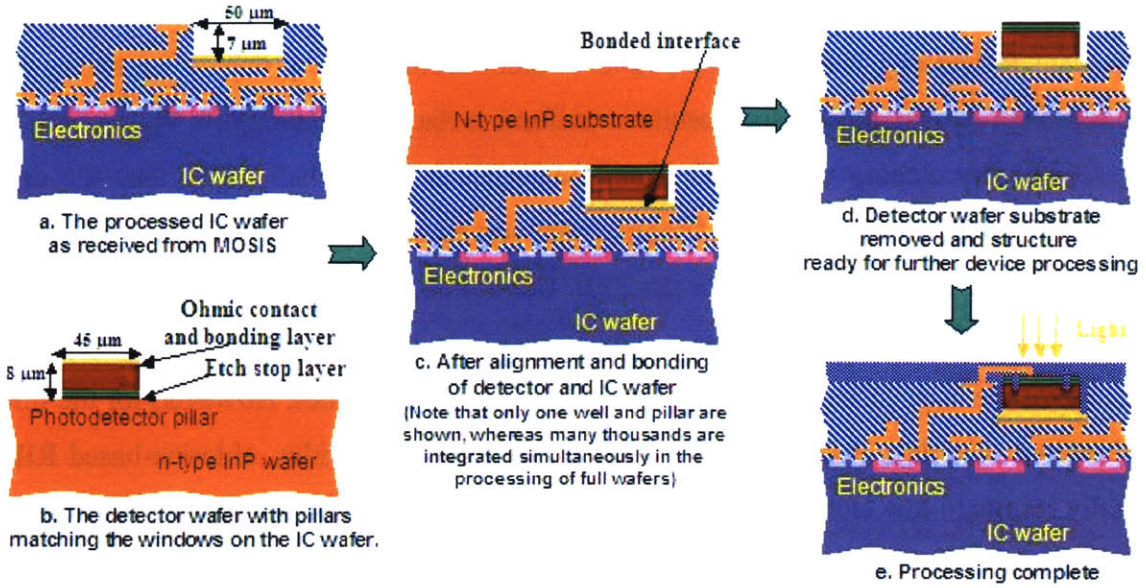

Figure 3-1: The APB process: (a) Recesses are opened on the processed IC wafers received from the manufacturer, (b) the n-side down detector wafers with pillars etched to match the windows on the IC wafer; (c) after bonding of the detector and the IC wafer; (d) after removal of the substrate of the detector wafer leaving p-i-n heterostructures bonded in the windows; and (e) after completing device processing and integration

3.1.1 Reactive Ion Etching of InP Based Materials

In this thesis, PlasmaQuest PECVD-RIE tool[1] was used for etching InP based heterostructures. In an ECR enhanced reactive ion etching system, the plasma is generated inside a dielectric vessel and flows out of the source into a material-processing chamber. The microwave power is coupled to the plasma across a dielectric window, rather than by direct connection to an electrode immersed in the plasma. The electrons are kept inside the chamber by an applied DC magnetic field, and the electron flux to the chamber wall is minimized. This in turn produces a lower sheath voltage so that the energy loss due to ions bombarding the walls is reduced. The reduced energy loss and the smaller etching chamber area due to the confinement provided by the magnetic field results in higher ion density. In addition, an RF source is used to bias the substrate so that

[1] PlasmaQuest is an electron cyclotron resonance (ECR) enhanced reactive ion etching system available in the Technology Research Laboratory of MIT.

the ion flux and the ion energy can be varied independently. ECR plasma etching is an important technology for III-V compound semiconductor etching due to its ability to produce high-density plasma that results in uniform surface morphology [6, 7].

The dry etching of InP and related materials is more challenging than the dry etching of GaAs based materials. Chlorine-based ion etching can be successfully used for the dry etching of GaAs based materials [30]. Controllable etch rates and smooth surface morphology are often obtained over a wide range of gas mixtures and process conditions because of the high volatility of the gallium and Group V chlorides. However, for the InP and related materials, due to the low volatility of indium chlorides, chlorine-based RIE usually results in low etch rates and leads to rough surfaces. Niggebrugge was the first to demonstrate the CH_4-H_2 chemistry for the RIE processing of In-based III-V compound semiconductors as a good alternative to the chlorine-based chemistry [31]. Operated at room temperature, hydrocarbon-based plasmas provide anisotropic profiles and etch rates of a few tens of nanometers per minute, thus the CH_4 based recipes gained acceptance for the anisotropic dry etching of InP [32, 33]. According to Hayes [34], in CH_4-H_2 plasma etching of InP, the phosphorus volatilizes in the form of PH_3, and the most likely reactants for indium volatilization are organo-indium compounds such as $(CH_3)_3In^+$ and $(CH_3)_2In^+$.

3.1.1.1 Development of Silicon Dioxide Etch Mask for InP Etching

The quality of the etch mask is very important to obtain a highly anisotropic etch profile in deep dry etching. The properties of a good etch mask are resistance to mask erosion during etching, an easy deposition, patterning and removal. Silicon dioxide (SiO_2) is a promising mask material for deep dry etching of III-V semiconductors. It has the advantage that it can easily be patterned in the same dry etch system using a CF_4/He plasma, and can be removed in the same way after the etching is complete. Alternatively, it may be removed in buffered hydrofluoric acid (BOE), which does not attack InP and most related materials.

The SiO_2 mask must be thick enough so that it can remain intact during the etching without undergoing significant erosion. The thickness of the SiO_2 film depends

on the desired pillar height. Typically, it was found that the oxide mask thickness should be at least 0.8-μm for defining 10-μm tall pillars. SiO_2 films were deposited in an ECR-PECVD chamber using SiH_4-O_2 plasma. The flow rates were 80 sccm for SiH_4 and 12 sccm for O_2. The deposition took place under 50 mTorr pressure, and the microwave power setting was 300W. The chuck temperature was set at 80°C in the first series of runs. However, during the deposition of the SiO_2 mask, an adhesion problem was observed between the deposited oxide film and the InGaAs top contact layer on the InP wafer. It has proven to be very difficult to deposit SiO_2 films even at moderately high temperatures on InGaAs using the ECR-PECVD chamber. The difference in thermal expansion coefficients of InGaAs and SiO_2 results in the cracking and flaking of the oxide film when the wafer is cooled down to room temperature after the deposition. Therefore, a low temperature oxide deposition technique is necessary to produce a good quality oxide film that can be patterned as an etch mask.

As an alternative, oxide deposition using an e-beam depository tool was explored presuming that the wafer temperature can be kept low during the process by using several cooling intervals. However, the high kinetic energy of the e-beam evaporated silicon dioxide molecules results in the heating of the wafer as they fall on its surface, and similar thermal expansion related cracking problems were observed.

Ultimately, the same ECR-PECVD chamber was used for oxide deposition at a reduced temperature. At lower temperatures, the oxide deposition rate is higher because of the improved sticking coefficient of the wafer surface. The low temperature deposition eliminates thermally induced cracking problems, and the oxide film adheres well to the InGaAs surface. However, the lowered surface kinetic energy reduces the mobility of the silicon atoms on the wafer surface, and because of this, the deposited film is less uniform as it is revealed by the color gradients on surface of the oxide due to thickness variation. Fortunately, the uniformity of the film is still good enough for it to be used as an etch mask. A processing temperature of 45°C was used, which is the highest temperature that yields an oxide film adhering well to the substrate.

The SiO_2 film was patterned in CF_4/He plasma using a photoresist mask, resulting in a high sidewall aspect ratio etch mask (~10:1) compared with a wet chemical etching

process. As in most etching systems, the sidewall profile of the etch mask plays an important role in determining the sidewall profile of the material being etched, and therefore anisotropic plasma etching of the oxide mask film improves the sidewall aspect ratio of the InP pillars. The erosion of the photoresist mask may become a problem while etching very thick oxide films. To preserve photoresist mask integrity during the SiO_2 mask patterning, 4 μm of AZP4620 thick resist was used as the etch mask for the dry etching of the oxide film. In this way, oxide masks thicker than 1 μm were patterned. The disadvantage of using thick resist is the reduced sidewall aspect ratio, but the sidewall aspect ratios are still much better than what the wet chemical etching can accomplish.

The dry etching of the oxide film was carried out in the same chamber at room temperature under 20 mTorr pressure. The flow rates were 15 sccm for CF_4 and 5 sccm for He. The microwave power was 100W, and the RF power was 20W. Under these conditions, the average etch rate was 4 A° per second.

3.1.1.2 CH_4-H_2 Plasma Etching of InGaAs/InP p-i-n Detectors

CH_4-H_2 plasma etching was used for etching InGaAs/InP p-i-n structures into pillars of 10 μm height for integration on silicon chips. The InP photodetector wafer was cleaved into a square chip 1 cm on a side. A SiO_2 mask of 0.8 μm thickness was deposited on this chip using the low temperature SiO_2 deposition process. Following this step, 4 μm thick resist was spun on the chip, the pillars were patterned using photolithography, and the oxide mask was dry etched in CF_4-He plasma. Once the mask transfer had been completed, the remaining photoresist on the pillars was removed using oxygen plasma. The InP based p-i-n structure was then etched in CH_4-H_2 plasma at room temperature under 18 mTorr pressure. The flows rates were 15 sccm for both CH_4 and H_2. The microwave power was 275W, and the RF power was 35W. The etching of 10 micron tall pillars was completed in about 2 hours. After the etching of the pillars, the remaining dielectric mask was removed in CF_4-He plasma. The process flow for the InP/InGaAs p-i-n heterostructure pillar fabrication is illustrated in Figure 3-2.

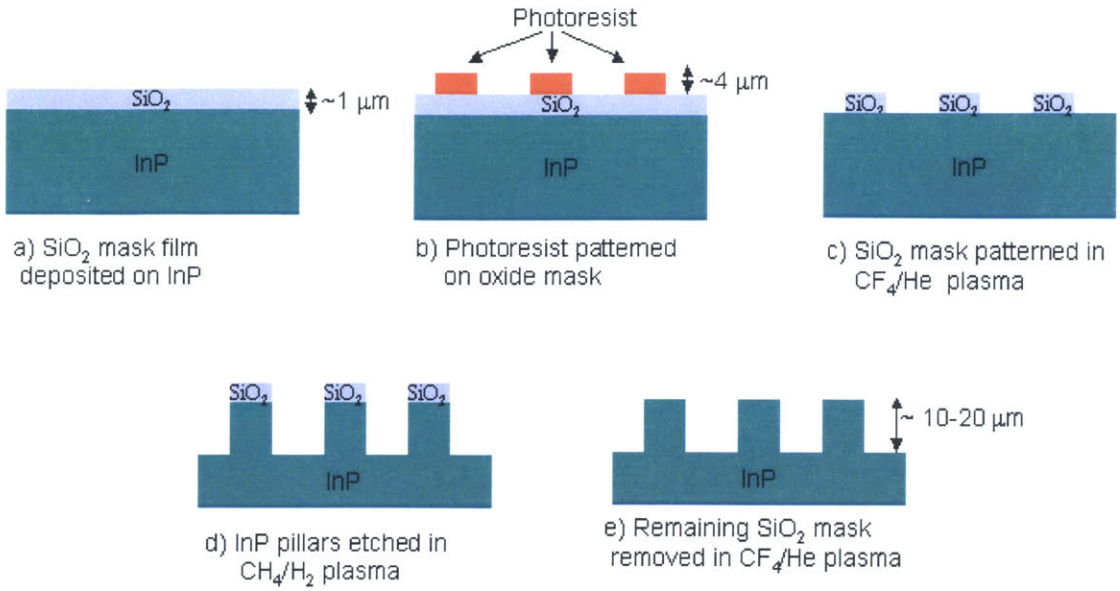

Figure 3-2: APB process flow for the InP/InGaAs pillar fabrication

Figure 3-3 is the SEM image of a 10-μm tall InGaAs/InP pillar[2]. The high sidewall aspect ratio refers to a highly anisotropic etch process. The roughness on the bottom surface is caused by polymer deposition. It is known that the formation of polymer films can take place under certain conditions of RIE with carbon-containing gases [35]. Since the polymer films cover the surface of the InP wafer, the plasma-wafer surface reaction area is reduced, and this in turn can limit the etch process. Often, the optimization of the methane/hydrogen etch involves identifying conditions where the gas pressure or input power is sufficiently high to produce a reasonably rapid etch rate, and yet low enough to avoid polymer deposition onto the surface which is being etched. Even under conditions where clean and rapid etching of InP substrate takes place, polymer deposition will occur on the unetched, masked regions. This is presumably because the chemically reactive species are not depleted in those regions, and they take an alternative reaction path, forming the polymers. For the etch recipe used in this work, polymer deposition was observed on the unmasked surface of the InP wafer, which resulted in a rough surface morphology, but the polymers did not obstruct the completion of the etch to the desired depth, and pillars with 20 μm height were defined. For RM[3] processes, the

[2] There is an AuSn cap layer on the top surface of this pillar.

InP substrate is eventually removed, thus the rough unmasked portions of the InP wafer are separated from the pillars.

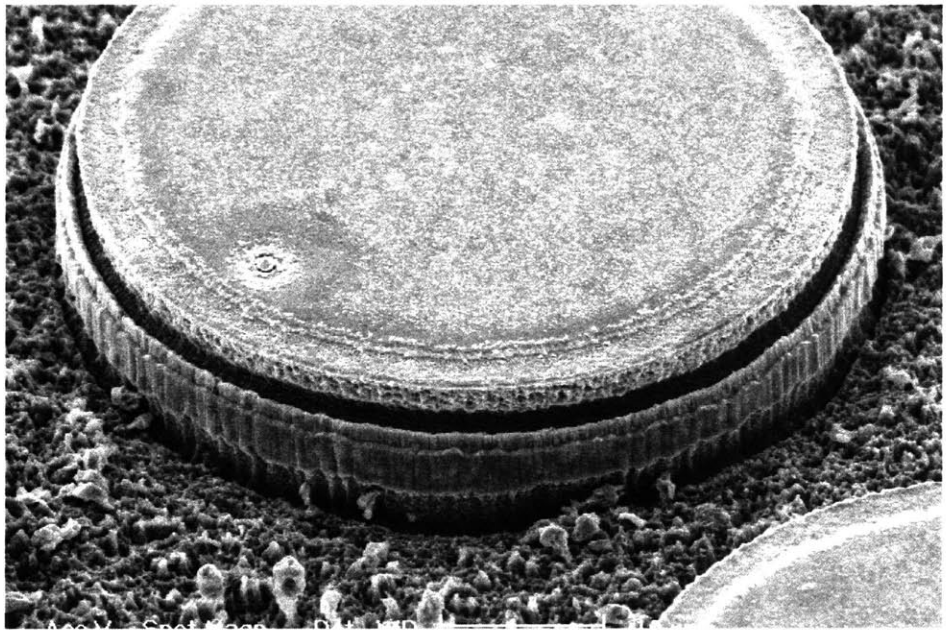

Figure 3-3: Scanning Electron Microscope Image of ECR-RIE etched InP pillars

The sidewall roughness is also a common problem for the deep dry etching of InP based materials. During the substrate removal etch, the sidewalls of the pillar are slightly trimmed by the HCl wet etchant, thus reducing the sidewall roughness originating from deep dry etching of InP. This is discussed in more detail in Section 3.2.1.2. If the rough sidewalls of the pillar degrade the performance of the optoelectronic device, the optoelectronic device can be redefined after being bonded onto the silicon chip by utilizing a groove etching technique on the surface of the pillar. This approach is discussed in Section 3.2.4.

The most widely employed technique for polymer removal is argon ion milling [35]. If argon is included in the plasma, argon ions can remove the polymers as they are being deposited on the surface of the wafer, thereby reducing the polymer deposition. On the other hand, argon will also sputter-etch the oxide etch mask, and for deep dry etching (~ 10 μm), like in RM^3 processes, the etch mask can erode during the etch, thereby not allowing the completion of the etch. The unavailability of argon in the PlasmaQuest

ECR-RIE plasma etching system used in this research work did not allow the investigation of this technique for polymer removal.

Polymers can also be reduced by using a very short dip in sulfuric acid (H_2SO_4), which etches most organic materials. This technique was employed in this thesis with plain InP wafers. However, the actual photodetector structures include InGaAs layers, and sulfuric acid can attack InGaAs, which makes it hard to use this technique on the heterostructure wafers. Very short sulfuric acid dips were employed to avoid the damage to the epi-layers, but this did not result in the removal of polymers since the etch times in sulfuric acid were short to avoid damage to heterostructures.

3.1.2 Metal Deposition on InP Pillars

As mentioned in the previous section, it may be necessary to deposit metal on the top surface of the InP/InGaAs pillars depending on the specific pillar-to-recess bonding technology utilized. In this thesis, two different types of metal assisted bonding techniques have been investigated. The first one is a semiconductor-to-palladium bond. The goal of this process is to form a strong bond between the Pd film, which is deposited on the bottom surface of the recess etched on the silicon chip, and the InGaAs layer, which is on the top surface of the p-i-n pillar. A more detailed discussion of palladium-to-semiconductor bonding is given in Section 3.1.4.2. When this technique is utilized, pillar surfaces are not metallized since palladium should react directly with the semiconductor.

The other bonding technique utilizes low temperature AuSn (80% Au, 20% Sn) eutectic solder alloy, which is resistant to oxidation, hence can be applied without the use of a flux, significantly simplifying the bonding process. Typically, solder is deposited on the pillar surface above an under-bump metallization (UBM) layer, which provides adhesion to both the solder and the pillar surface to prevent AuSn from de-wetting the surface. This layer also blocks AuSn from diffusing into the pillar during bonding. Specifics of AuSn solder bonding are discussed in Section 3.1.4.3.

Solder bonding technique requires that the pillar preparation must be altered so that the solder and the UBM pads can be deposited on the surface of the pillars. Two different methods have been investigated for this purpose. In the first one, the metal stack

was patterned on the plain surface of the epitaxial InP wafer using the lift-off technique. After this step, an oxide film was deposited on the metallized surface of the InP wafer, but the oxide film adhesion was poor even with the reduced temperature mask deposition technique mentioned before. The oxide film peeled off the surface of the wafer preventing further processing. Moreover, even if the oxide deposition succeeded, this approach would still require another step of lithography to pattern the oxide mask, which can easily result in the metal stack to be off-centered with the pillars.

The other method started with the deposition of a continuous film of metal on the plain surface of the epitaxial substrate. An oxide film was deposited on top of the metal film, and it was patterned in a plasma chamber using photoresist as an etch mask. The oxide mask was then used as a hard mask to etch the metal film and the semiconductor underneath it in a plasma chamber. This method was also utilized for the preparation of OptoPillars in OptoPill Assembly, and it is discussed in more detail in Section 3.2.1.1.

3.1.3 Recess Preparation via Dry Etching on CMOS Chips

The recess bonding pads are initially covered with a thick stack of dielectric layers that serves as the insulation barriers between the different levels of metallization on an integrated circuit. The dielectrics in the recesses are usually not removed during the foundry run. The goal of the recess cleaning process is to expose the bonding pads covered originally by the dielectric stacks produced in the foundry run. Recess cleaning is a rather delicate process, and it should be tailored to accommodate the specific back-end technology of the foundry utilized. The electronic circuits on the chip must be preserved while removing the thick layer of dielectrics on the bondpads.

The final passivation layer covering the top surface of the CMOS chips is PECVD silicon nitride. This film is difficult to etch with wet chemical etchants. Hydrofluoric acid can etch it, but the etch rate is quite low, and the process is not selective with respect to SiO_2 which is underneath the nitride layer. Boiling phosphoric acid at 80°C is commonly used to etch silicon nitride, but this etchant often lifts off the photoresist masks, thus a hard mask has to be used, requiring its own masking and etching steps. Room

temperature phosphoric acid can also etch the nitride layers, but the etch rate is very low, and the etch is isotropic possibly damaging the dielectric coating around the recesses.

Figure 3-4 shows the SEM image of a partially cleaned CMOS recess after an attempt to clean it by wet chemical etchants. The inter-metal dielectric layers (IMDs) are indicated by the arrows on the figure. Up to five layers of IMDs can be seen in the figure. The top layer is a silicon nitride (SiN) passivation layer, and there is another passivation layer between this nitride layer and the IMDs. The smooth surface in the areas where the etch could be completed is the METAL2 layer. The two stripes in the center of the METAL 2 layer, which can be seen on the lower right corner of Figure 3-4 and more clearly on Figure 3-5 and Figure 3-6, were utilized for compliance with the CMOS design rules during the silicon lay-out. The metal layer for the 0.18 μm TSMC process is a copper-doped aluminum layer sandwiched between TiN diffusion barriers. The smooth and shiny surface of this layer can be used to tell it from the dielectric layers.

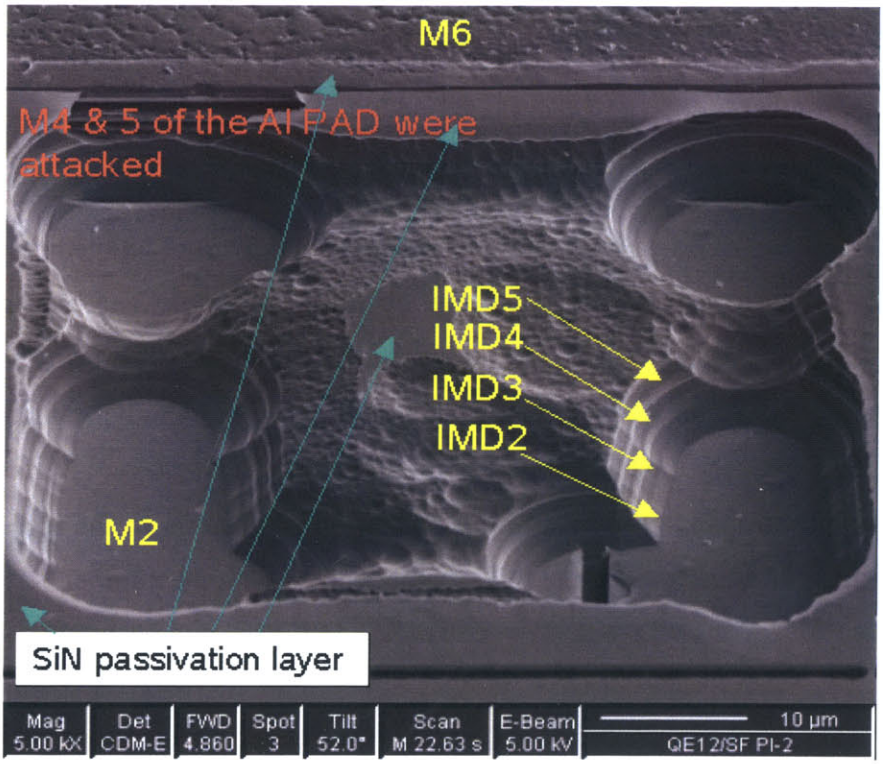

Figure 3-4: SEM image of a CMOS recess after an attempt to clean it by wet etching

Figure 3-5 shows further SEM/EDS analysis of a CMOS recess that was subjected to a wet etch. 2 μm of thick photoresist was patterned on the chip to expose the recesses, and the chip was immersed in room temperature phosphoric acid and BOE in alternating steps. As it can be seen, the etch could not be completed uniformly, and a square shaped pillar-like region was formed in the center of the recess, about the region defined by the two stripes. An EDS analysis of the chip as shown on the right side of Figure 3-5 suggests that the incomplete etching of the final nitride passivation layer is responsible for the formation of the pillar and the non-uniform and incomplete etching of the recess. The nitride layer, which could only be partially removed by the phosphoric acid etch, behaved as an etch mask during the buffered oxide etching of the silicon dioxide IMD layers underneath it. To overcome this problem, the chip was immersed in phosphoric acid for a long time to completely etch away the nitride layer, but it has been observed that some portion of this nitride layer still remained, precluding the uniform etching of the recess. Furthermore, immersing the chip for long times in BOE and H_3PO_4 can induce severe damage to the surrounding bondpads and to the Ti/Al layer underneath the recess dielectrics since BOE can also attack aluminum.

An electron diffraction spectroscopy (EDS) analysis of the partially cleaned recess (using wet etching) is shown on the right side of Figure 3-5. As was mentioned before, the top dielectric layer on the un-etched pillar-like region (denoted by "1" on the SEM image) is SiN as can be seen from the top-left EDS graph. The top layer on the surrounding dielectric stack (denoted by "4" on the SEM image) is also SiN as shown in the EDS graph with the corresponding number. There is another silicon dioxide passivation layer between the top nitride layer and the IMDs. This layer is denoted by "2" on the SEM image and the corresponding EDS graph. The bottom of the recess is a TiN metallic layer as can be seen from the EDS graph denoted with the number "3".

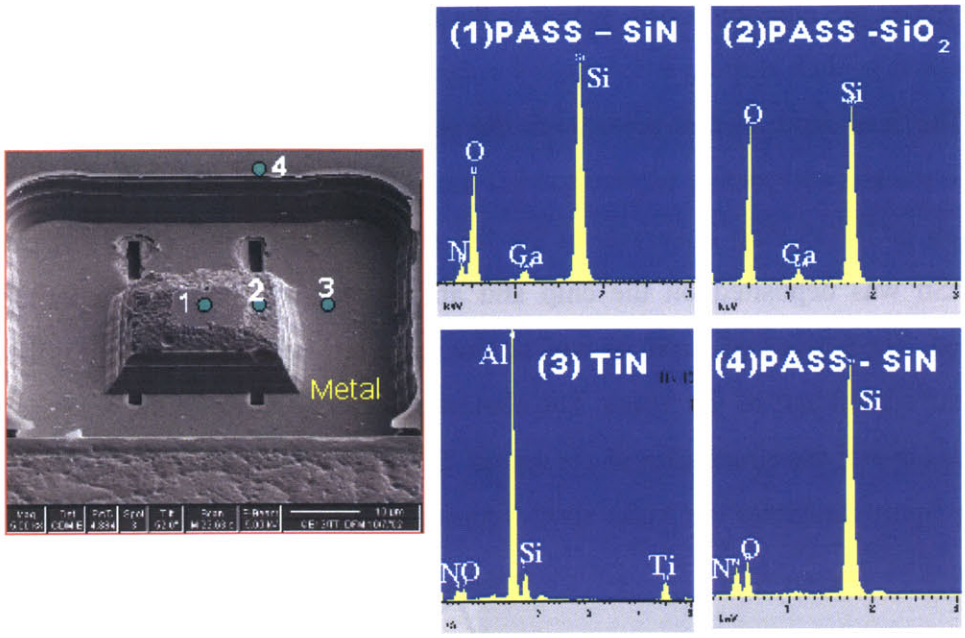

Figure 3-5: SEM and EDS analysis of the CMOS recess

Since the wet etching did not produce good results for the CMOS recess cleaning process, and a better etch process was sought. Using CF_4-O_2 plasma, atomic fluorine is produced which etches the nitride film much more easily. The recesses were exposed by patterning 7 μm thick photoresist on the chips, which is a reasonably good etch mask for fluorine based dry etch plasmas as was mentioned before. The silicon nitride etch was performed at room temperature under 20 mTorr pressure. The flow rates were 15 sccm for CF_4, 15 sccm for He, and 5 sccm for O_2. The microwave power was 100W, and the RF power was 20W. The silicon nitride final passivation layer, which was around 0.5 μm thick, could be completely removed in 1000 seconds using this plasma etching system. Dry etching of the interlayer dielectrics, which were made of silicon dioxide, followed the removal of the silicon nitride layer. The same silicon dioxide plasma etch recipe developed for the pillar mask etching was utilized for this step.

Another advantage of using fluorine based plasma etching over hydrofluoric acid wet etching is that the METAL 1 aluminum pad underneath the dielectric stack has a low etch rate with fluorine based chemistries since the by-product, AlF_3, is not very volatile

[7]. Therefore the aluminum pad, which is the bottom contact layer for the p-i-n diode, also serves as an etch stop layer for the dry etching of the dielectrics in the recess.

The final depth of the recess, after the aluminum surface underneath the removed dielectric stack is completely exposed, is 7.2 μm. The SEM image of a dielectric window opened on a CMOS chip is shown on the left side of Figure 3-6. The SEM was taken after AuSn was deposited on the chip and an unsuccessful bonding experiment was performed. The residue of AuSn as well as the mark left behind by the InP pillar can be seen in the central part of the figure. The aluminum layer underneath the AuSn is flat and it extends beyond the boundaries of the recess. The micro-photograph on the right side of the same figure illustrates the AuSn alloy deposited in a CMOS recess.

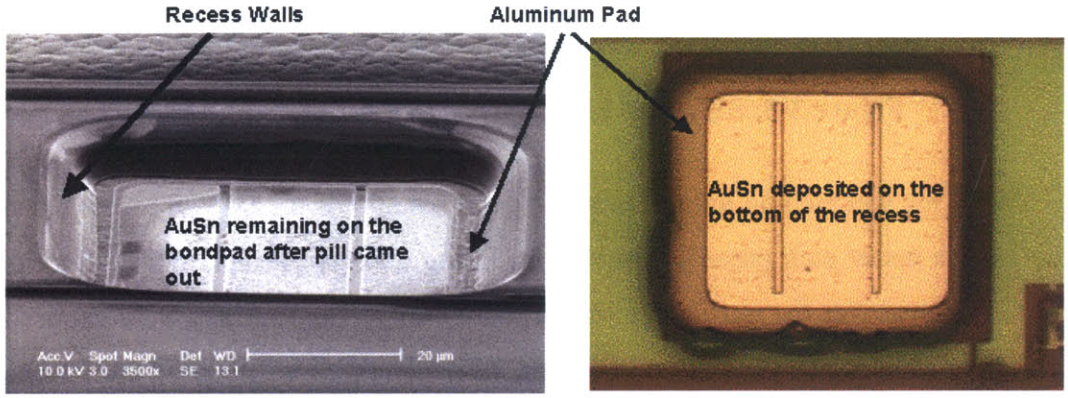

Figure 3-6: Left: SEM image of the metal pad exposed on the bottom of a dielectric window on a CMOS chip. The two stripes originate from the CMOS design rules.
Right: Micro-photograph of an AuSn deposited CMOS recess.

The sidewall slope of the recess is most likely due to the lithography process used for the plasma etch. Typically, it takes 4 hours in the plasma chamber to etch down to the aluminum pad, and removing the photoresist mask afterwards proved hard even with organic photoresist strippers such as micro-strip. As a result of this, the process was divided into two steps, and the photoresist was stripped and re-patterned between the two steps. The re-patterning of the photoresist between the two steps is challenging since the recess is already etched down by 4 μm after the first step, and it is difficult to obtain a sharp photoresist pattern along the edges of the recess since there is always some etching of the edges of the recess during plasma etch. Therefore, when the same size mask is used

to re-expose the already etched recesses, the recess size is typically a little larger than the size of the mask, resulting in a non-sharp resist pattern in the edge area, which can lead to reduced sidewall slope.

3.1.4 Metal Assisted Bonding for RM^3

The primary function of the bond is to provide a mechanical connection between the optoelectronic device and the bonding pad at the bottom of the recess opened on the surface of the CMOS chip. Bonding of dissimilar materials to construct mechanical structures on the micro-scale is an area of limited research. However, the area of packaging micro-devices and die-attach techniques is a rich subject and is closely related to the task at hand. Thus, the techniques that were considered for the current application were based on die-attach and packaging techniques.

A significant problem with the wafer bonding methods such as wafer fusion and glass frit bonding is the difficulty of obtaining a good electrical connection between the two substrates at the bonding interface due to the presence of native oxides on the semiconductor surface. Metal assisted bonding, which utilizes an intermediate metal layer between the two substrates, can provide a good electrical connection and a robust mechanical bond between the optoelectronic device pillars and the CMOS chip.

3.1.4.1 RDA M8 Flip-Chip Bonder

A Research Devices Automation M8 flip-chip bonder in the Microelectronics Laboratory of the Northeastern University was used in the experiments. This bonder has less than 2 μm pattern-to-pattern alignment tolerance. The pillar wafer and the electronics wafer were placed on the two chucks of this bonder, and the pillar and recess patterns were aligned using front-side optical plane alignment. The two wafers were then secured (i.e. brought into contact), and bonded by applying uniaxial pressure at temperatures under 350°C. The force applied during the bonding was 50 grams which translates into 18 MPa pressure for a chip with 17 pillars of 40 μm x 40 μm size each. Only the bottom chuck of

the bonder could be heated, and the InP chip was placed on this chuck due to the high thermal conductivity of InP.

Alignment is very critical for the proper operation of M8. The first type of alignment is the in-plane alignment, which is done by the help of an optical probe plane inserted between the two chips when the chips are placed face-to-face on the two chucks. The in-plane alignment is used to simultaneously align all pillar-recess pairs on the two chips. The optical plane is removed after the in-plane alignment is completed. The second phase is the co-planar alignment of the two wafer surfaces so that the surfaces of the recesses and the pillars are parallel to each other. Without co-planar alignment, it is not possible to have contact between pillars and recesses uniformly across the entire chip.

The co-planar alignment is usually accomplished optically by the help of an auto-collimator, but the manual pitch & roll mechanism of the M8 that was available for this work did not allow the use of the autocollimator, and the co-planar alignment was done by using a process which involved bringing two flat, polished wafers into contact and then releasing them to allow for their self co-alignment through pitch & roll. The success of this procedure varied from run to run, and it has not been possible to obtain a high yield and reliable alignment and bonding procedure using the M8 flip-chip bonder. The issues regarding the co-planar alignment problem will be addressed in Section 3.1.6.

3.1.4.2 Palladium-to-Semiconductor Bond

One of the two bonding metallurgies investigated in this thesis is palladium-to-semiconductor bonding. Palladium (Pd) forms a good ohmic contact with semiconductors, and the high malleability of Pd accommodates the stress due to lattice mismatch and the difference in the thermal expansion coefficients of the electronic and the optoelectronic substrates [36]. Another valuable property of palladium as a bonding agent is that it can displace and disperse native oxide layers on the semiconductors, while resisting oxidation itself [36]. On GaAs, a deposited film of Pd diffuses through the typical native oxide layer at room temperature. The driving force for this diffusion is a solid-state reaction that forms the compound Pd_4GaAs. The formation of this compound results in the mechanical dispersion of the native oxide layer, and this allows the

complete coverage of the interface with the reaction product. The formation of Kirkendall voids in the un-reacted Pd at the interface shows that Pd is the dominant moving species in this reaction. Furthermore, the native oxides, which are mechanically dispersed, move into these voids resulting in an interface that is free of native oxides. This ability of Pd to penetrate and disperse native oxides on semiconductor surfaces at low temperatures allows building highly conductive bonding interface at low temperatures, and it results in good ohmic contacts with both n-type and p-type compound semiconductors such as GaAs and InP [36]. The surface diffusivity of Pd on Pd is very high, allowing Pd to fill in the cracks and humps on the surface of the semiconductor, creating a smoother interface desirable for wafer bonding [36].

Pd bonding of GaAs and InP, materials with significantly different lattice constants, was shown finding that a Pd layer is sufficiently malleable to accommodate the stress resulting from the thermal expansion coefficient mismatch [37]. Typically, a Pd/Sn/Pd sandwich layer is deposited on one of the substrates, and the bonding takes place between this metal layer and the other substrate [38]. The relatively small diffusion of palladium and tin has the significance that palladium on both sides of the bonding interface are separated by tin, and the palladium can alloy with the semiconductor on either side of the interface. Sn has a low melting point, 232°C, and it is molten at the bonding temperature (~300°C). Thus it can serve as a cushion layer to accommodate non-planarity or surface curvature of the bonded surfaces. This is expected to improve the bond working with the malleability of Pd.

In APB recess metallization process, a sandwich layer of Pd/Sn/Pd (300nm/100nm/300nm) was e-beam deposited onto the aluminum bonding pads inside the recesses opened on the CMOS chip. An SEM image of Pd/Sn/Pd layer deposited onto a recess bonding pad is shown in Figure 3-7. Underneath this film is the aluminum bonding pad. When this metal layer is brought into contact with the InGaAs surface layer of the pillars at an elevated temperature under uniaxial pressure, a bond can form at the interface. Alternatively Pd can also be deposited on both substrates, and the bonding can occur between the two Pd layers, but this metal-to-metal bond will be harder to form than

the metal-to-semiconductor bond at the desired low temperatures, so the Pd-semiconductor bond approach was pursued [39a].

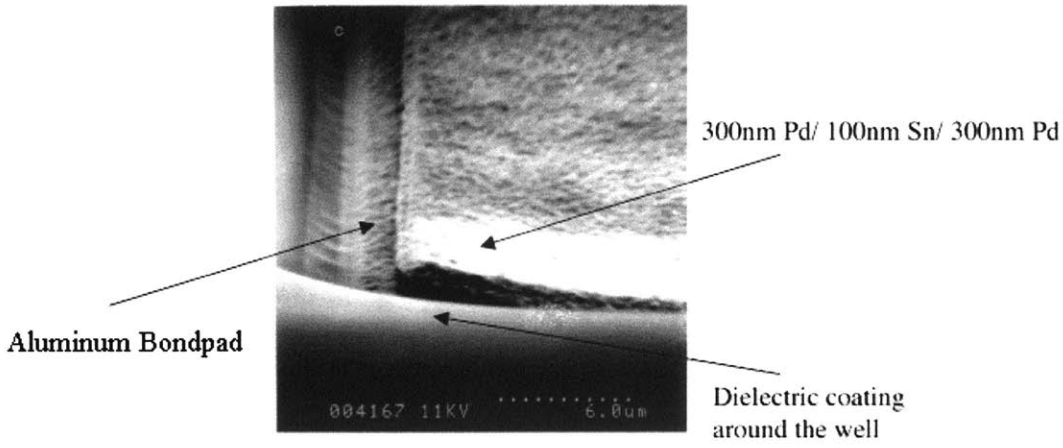

Figure 3-7: Pd/Sn/Pd metallization of a VLSI recess

The palladium-to-semiconductor bond approach was investigated under a clamping pressure of 20 MPa at 300 °C. The bonding duration was 30 minutes and the heating/cooling ramps were 20 °C/min. However, the two chips came apart easily after being removed from the bonder. This was mostly due to the co-planar alignment problems with the bonder. To investigate this issue further, a silicon wafer piece of 1 cm^2 area was coated with the same Pd/Sn/Pd stack for being bonded to a same-size, flat InGaAs/InP wafer piece. After the two wafers were supposedly brought into full contact using the co-planar alignment procedure, there was still a tiny gap between the wafers, and the wafers touched only at one edge and not the opposite one. Trying to bond the two wafers using a clamping force of 500 grams[3] at 300 °C for 30 minutes did not yield a good result, and the chips came apart easily after they were removed from the bonder. This was expected since the chips were not parallel at the time of bonding. Due to these limitations, palladium-to-semiconductor bond approach was not pursued.

[3] This was the maximum force applicable by the bonder, and it translates into a pressure of 0.05 MPa if they were in full contact.

3.1.4.3 AuSn Eutectic Solder Alloy Bond

Solder bonding technique is also limited by the same co-planar alignment problem of the flip-chip bonder for the APB process, but it has important advantages for the OptoPill Assembly process. A typical solder process consists of heating the bond material, which is typically a metal alloy, above its melting temperature, allowing it to wet the surfaces to be bonded, and then cooling to solidify. Solders are prevalent in microelectronics packaging applications, because the lower processing temperatures prevent damage of sensitive electronics.

In general, solders are divided into two basic categories, soft and hard. Soft solders such as Sn-Pb typically have melting temperatures below 200°C, have low yield strengths, and are more susceptible to thermal fatigue and creep. Device layers bonded using soft solders are not subject to high stress because the bonding layers would deform plastically to relax the stress developed. The capability of plastic deformation, however, makes soft solders subject to thermal fatigue and creep rupture, causing long-term reliability problems.

Commonly used hard solders include eutectic compositions of gold-silicon (97wt.%Au - 3wt.%Si), gold-germanium (87.5wt.%Au - 27.5wt.%Ge), and gold-tin (80wt.%Au - 20wt.%Sn), which have melting temperatures (eutectic points) of 363, 361 and 278°C, respectively. Due to higher melting temperatures and yield strengths, hard solders are used more frequently in packaging applications.

The gold-based eutectic solders have good mechanical properties and are electrically conductive, which make them attractive for RM^3 processes. In addition, the bonds can be completed in a reducing atmosphere without the use of flux. They have good thermal conductivity and are free from thermal fatigue because of their high strength resulting in elastic rather than plastic deformation under stress.

AuSn has the lowest melting temperature, highest yield strength, and lowest modulus of the gold-based eutectic solders discussed [40]. The room temperature values of thermal expansion coefficient, elastic modulus and strength are listed in Table 3-1 [40]. The principal disadvantages of the AuSn solder are the large thermal expansion coefficient, which can lead to large residual stress, and the high gold content, which

makes the bonding method expensive. Despite these drawbacks, the advantages of the AuSn lead it to its selection to bond optoelectronic device pillars to silicon CMOS chips.

Table 3-1: Room temperature mechanical properties of 80 wt.% Au - 20 wt.% Sn alloy

Young's Modulus	59.2 GPa
CTE	15.93 μm/m°C
Yield strength	275 MPa
Ultimate Strength	275 MPa

The equilibrium phase diagram of the gold-tin binary system is shown in Figure 3-8 [40]. It is one of the more complicated binary systems with two eutectic points. The common eutectic composition of 80 wt.% Au and 20 wt.% Sn melts at 278 °C. Alloys of the second eutectic composition, 10 wt.% Au and 90 wt.% Sn melt at 217 °C. Virtually all applications of the gold-tin system as a solder utilize the 80/20 eutectic composition.

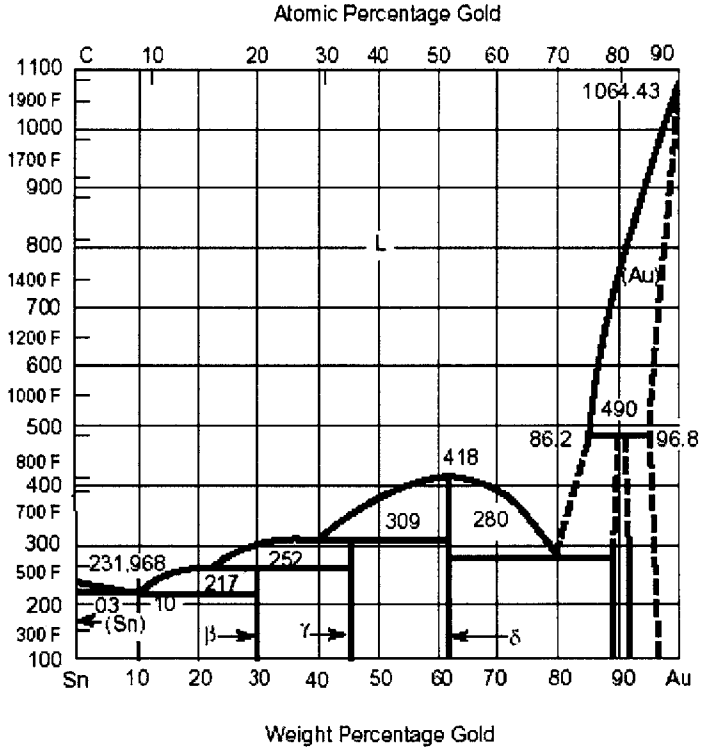

Figure 3-8: Gold-tin equilibrium phase diagram [41]

For RM^3 processes, the bonding takes place inside a recess opening, and it is necessary to deposit the solder alloy directly on one or both of the components to be bonded using a monolithic deposition technique such as e-beam. This can be done by depositing a eutectic AuSn premix (commercially available) on one or both of the components. If AuSn is deposited on both surfaces, the bonding occurs by the inter-mixing of the molten AuSn alloys upon heating. If AuSn is deposited on one surface only, the other surface is coated with an AuSn wettable pad, and the bonding takes place when the solder wets this bonding pad. Both of these approaches utilize the AuSn eutectic solder premix that is e-beam deposited onto the desired component.

Bouwstra reported an alternative approach for AuSn bonding by depositing a gold/tin/gold multi-layer on one of the components to be bonded [41]. The component that mates with the layer containing the gold-tin composite was also metallized with a chromium adhesion layer followed by a gold capping layer to promote wetting. The total layer thickness of the two opposing surfaces was designed to fit the eutectic composition of the gold-tin system. A static clamping pressure of 0.07 MPa was used to achieve a tensile bond strength of 2.0 MPa at 350 °C with two silicon wafers, one coated with 100 nm Cr/ 100 nm Au/ 1000 nm Sn/ 100 nm Au, and the other coated with 100 nm Cr/ 1000 nm Au [41]. It should be noted that this multiplayer concept is only effective because of the fact that tin melts at 232 °C, which is lower than the melting temperature of the 80/20 eutectic alloy. Upon heating, tin melts and inter-diffuses with gold to form a gold-tin alloy at the eutectic composition as determined by the as-deposited total layer thickness. The formation of tin-oxide on the surface is prevented by depositing the gold and tin layers such that gold is the final layer deposited.

The results reported by Bouwstra demonstrate that it is possible to form a strong bond using thin solder layers and a small clamping pressure, which is crucial for the OptoPill Assembly process. However, the success of the multi-layer technique depends on the precision of the thickness of the metal layers in order to achieve the eutectic composition upon heating. Due to the variations in the metal deposition rates, AuSn alloys with different compositions may form, significantly lowering the bond strength. This problem is reduced when an AuSn eutectic solder premix is used.

The solder will not readily wet and bond to aluminum bonding pads on CMOS, thus the bonding surfaces need to be metallized prior to bonding. The under bump metallization (UBM) typically consists of three layers. The first one is an adhesion and diffusion barrier layer, which forms a strong bond with bonding pad metallization, and prevents diffusion between bonding pad metallization and solder bumps. Chromium (Cr), titanium (Ti) and titanium/tungsten (Ti/W) are typically used for this purpose. The second layer is a solder wettable layer, which provides a surface for solder bump to adhere to. Copper (Cu), nickel (Ni) and palladium (Pd) with a thickness of ~1-5 μm are examples of wettable pads. The final layer is an oxidation barrier layer to protect the UBM structure from oxidation, and a thin layer of gold can be used for this purpose.

There are many possible combinations of thin film layers for UBM such as Ti/Cu/Au, Ti/Cu, Ti/Cu/Ni, TiW/Cu/Au, Cr/Cu/Au, Ni/Au, Ti/Ni/Pd, and Mo/Pd [ref]. The structure of UBM affects greatly the reliability of UBM itself. For example, Ti/Cu/Ni UBM has better adhesion strength than Ti/Cu UBM. UBM structure also has effects on reliability of connections between UBM and bonding pad and between the UBM and the solder bumps. To achieve reliable connection between UBM and solder bumps, UBM must be compatible with the solder alloys used for solder bump. UBM suitable for high lead solders may not work well with high tin solders (eutectic solders). For example, Cu is a good solder wettable layer for high lead solder with 3-5% of tin, but it is not suitable for high tin solder since Sn reacts rapidly with Cu and forms Sn-Cu inter-metallic compound. If Cu is completely consumed, solder will dewet from the bondpads.

In RM^3 processes, the aluminum pads on the recesses were metallized with a UBM consisting of 30 nm thick Cr adhesion layer and diffusion barrier, 300 nm thick Cu solder-wettable pad and 10 nm thick Au oxidation barrier. UBM on the pillar side was comprised of a Au film to provide an ohmic contact to the optoelectronic device and a nickel diffusion barrier of 300 nm thickness. AuSn solder of 0.6-1.0 μm was deposited on top of the Ni film in the same vacuum cycle.

To complete the bond, AuSn layer on the pillars was brought into contact with the UBM on the CMOS bonding pads after the proper alignment, and the combination was heated to 350°C to melt the solder. M8 flip-chip bonder utilized in APB (see Section

3.1.5) did not allow the use of a forming gas ambient to prevent oxidation during heating. The magnitude of the clamping pressure used in the APB process was in the range of 0.1 MPa [41]. However, due to the problems of the M8 flip-chip bonder, the yield of the APB AuSn solder bonding experiments was also low. However, a successful bond was achieved using this metallurgy in the OptoPill Assembly process as discussed in Section 3.2.3. The results of APB AuSn bonding experiments are discussed in Section 3.1.6.

An alternative method for applying the AuSn layer was also considered. AuSn solder was deposited onto both the pillars and the recesses (using the same pillar UBM on both sides). It was expected that in molten form the solder on both sides of the interface would inter-mix, and form into a single solder layer upon cooling. However, this method did not yield a good bond in neither the OPA or the APB processes.

3.1.5 APB InP Substrate Removal

If the bonding is successful, the bonded wafer pair is transferred on a glass slide for easy manipulation, and TRA-BOND 2113 epoxy is flowed between the chips and allowed to harden. The purpose of this epoxy is to protect the front surfaces of the chips from the subsequent substrate removal etch. The epoxy is applied from one side of the chips, and it flows into the gap between the two chips by capillary action. TRA-BOND 2113 is a clear, low viscosity epoxy adhesive that can cure at room temperature, and has very good flowability and wetting characteristics. Fully cured TRA-BOND 2113 is a good electrical insulator and provides excellent resistance to acids like HCl, which is used during the substrate removal etch. The epoxy is transparent, and it has a viscosity of 300 cps at room temperature when mixed. The epoxy can be cured in 24 hours at room temperature, or in 4 hours at 65 °C. The room temperature cure with a short pre-heating for outgassing is the preferred curing method for this application.

As the epoxy moves into the gap flowing towards the center of the chips, it can trap the air that was in between the two chips, resulting in the formation of air bubbles in the cured epoxy. As it can be seen from Figure 3-9, these air bubbles can cause the undercutting of the pillars since the substrate removal etchant can reach the device layers

through these bubbles. As a result, the pillars can be significantly undercut in the extent that all InP buffer layers can be removed by the substrate etchant.

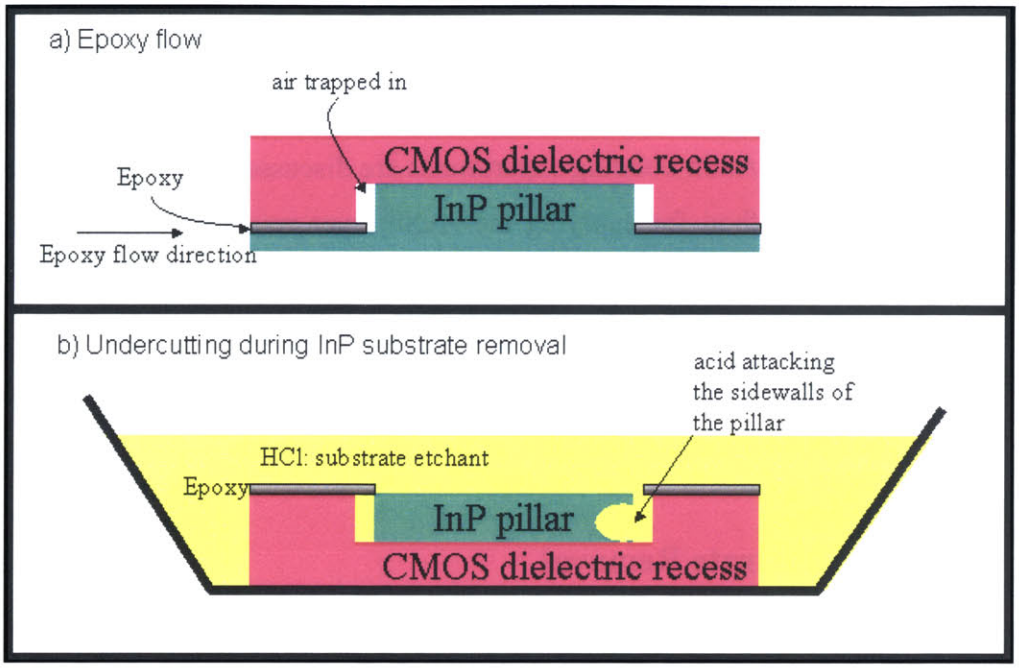

Figure 3-9: Illustration of the under-cutting problem during InP substrate removal due to the air bubbles trapped in the epoxy

In order to reduce the effects of this problem, the bonded pair of chips was placed on a plastic stand inside a semispherical glass chamber, which was brought under vacuum by the help of an O-ring and a vacuum pump. The top opening of the chamber was covered with a rubber cork that had a needle inserted through it as shown in Figure 3-10. Once the chamber was vacuumed down, the epoxy was dropped through this needle onto the stand to come into contact with the edges of the chips, and flow in between the two chips. After the epoxy was flown, the chamber was brought into atmospheric pressure, the bonded chips were carefully taken out of the vacuum chamber, and they were placed on a 65°C hot plate for 10 minutes to allow for the outgassing of the epoxy. After this step, the epoxy was allowed to cure at room temperature for 24 hours. After the epoxy had been cured, the bonded pair was mounted on a glass cover-slide using molten black wax, which is very resistant to etchants, and the wax was cooled down to solidify. The

only surface of the bonded pair, which was not immersed in wax, was the back side of the pillar wafer. The wax is used to protect the electronic substrate and the actual device layers during the substrate removal phase.

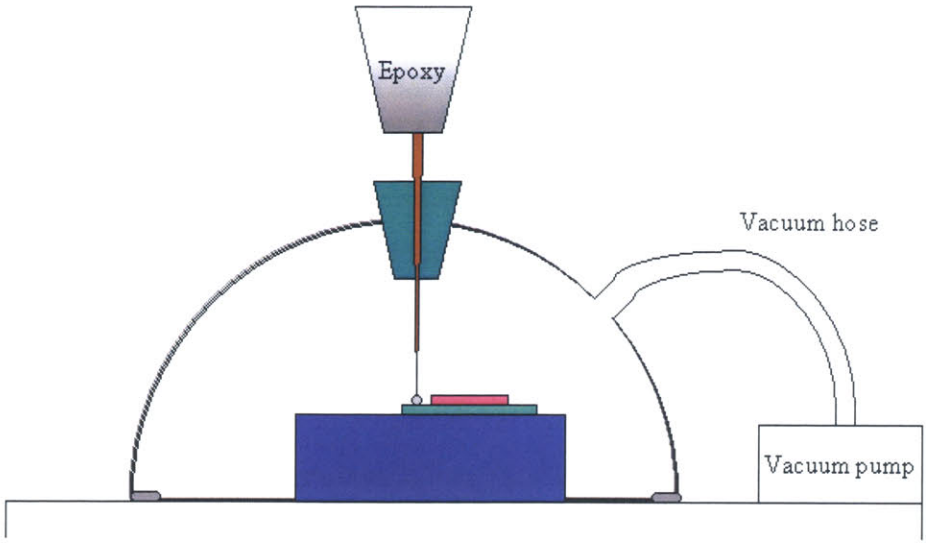

Figure 3-10: Epoxy flow under vacuum to prevent the air bubbles

Next, the chips were immersed in a solution of HCl, which etches the InP substrate starting from the uncovered back side. An InGaAs epitaxial etch stop layer is utilized to protect the actual device pillars from HCl. Figure 3-11 shows InP detector pillars on a CMOS after the substrate removal.

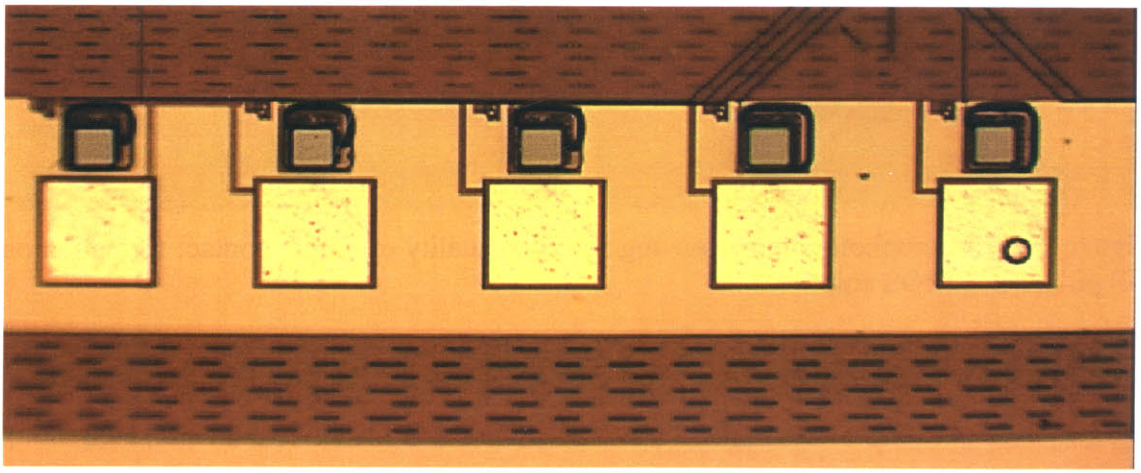

Figure 3-11: Micrograph of InP pillars on a CMOS chip after substrate removal.

3.1.6 Summary of APB Results and Process Limitations

APB post-fill processing starts with etching away the excess epoxy on top of the chip in CF_4/O_2 plasma. However, if the epoxy chars during this process due to overheating, removal of the epoxy can no longer be feasible. The chip should be placed on a good heat sink material during the plasma etch to avoid the charring problem due to overheating. Furthermore, the etch process should be divided into several short intervals to allow the cooling of the chip between the successive etching steps. However, the charring of the epoxy could still occur in spite of these precautions.

If the epoxy is removed successfully, the next step is to form a metallic ohmic ring on the top surface of the bonded pillars using the lift-off technique. However, the roughness created by the epoxy residue on the edges or on the back surface of the chip can significantly lower the quality of the photolithography process on the CMOS chip. It is hard to completely remove this epoxy by scrapping it off the back side and the edges of the chip since this procedure can damage the chip. Figure 3-12 shows the microphotographs of two pillars transferred on a CMOS chip. The poor quality of the ohmic contact metal rings is due to the lithographical problems mentioned above.

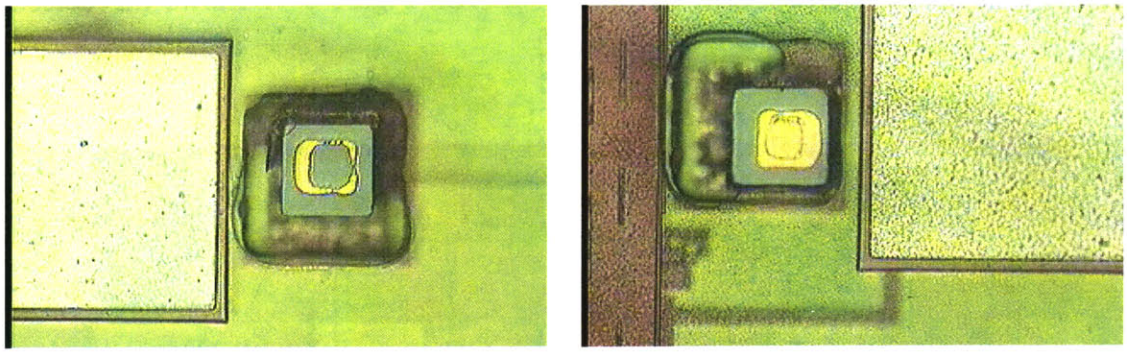

Figure 3-12: Microphotographs showing the poor quality of ohmic contact formation on InP pillars on CMOS chip.

A closer examination of the InP pillars transferred onto CMOS recesses revealed that the pillars actually stood higher than they should have inside the recesses, suggesting that the pillar was not actually bonded to the bonding pad inside the recess. The origin of this problem was traced to the co-planar alignment issues of the M8 flip-chip bonder.

More specifically, if the two chips do not have the proper co-planar alignment, they will come into contact at a surface other than the designated bonding interface, thus preventing the pillars from coming into contact with the bonding pads inside the recesses. Occasionally, the two chips can be attached together at this surface after an attempt of bonding, and it may not be possible to distinguish this from a real bond at the desired interface. If the process is continued, the epoxy will flow into the gap between the pillar and the bottom surface of the recess, and upon curing, the pillars will be stuck on the cured epoxy, instead of being bonded to the bonding pad. This is undesirable since the epoxy is not conductive and it forms an insulator between the electronic interconnects and the bottom of the pillar. For example, the pillar shown in Figure 3-13 is stuck on a layer of epoxy covering the bonding pad surface.

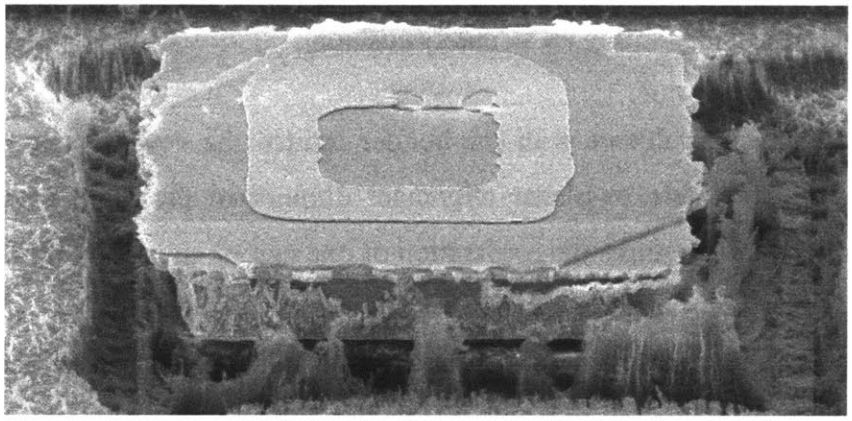

Figure 3-13: SEM image showing an InP pillar on a CMOS chip and a metallic ring formed on the pillar. The pillar is stuck on the epoxy, and it is not bonded to the pad.

The epoxy around the pillar is more visible in Figure 3-14. This is a close-up SEM image of the sidewall of an InP pillar transferred to a CMOS recess. The SEM is taken after the epoxy is etched away, but the remains of the epoxy still remain on the sidewalls of the pillar. It is this epoxy that prevented the under-cutting of the pillar layers during the substrate removal etch. However, the epoxy sits as a cushion under the pillar, isolating the pillar from the metallic bonding pad on the bottom of the recess.

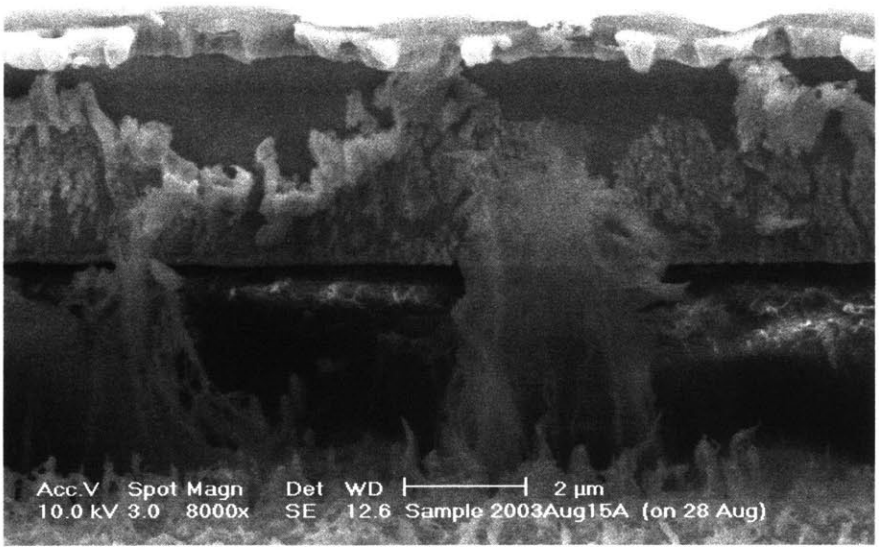

Figure 3-14: Close-up SEM of an InP pillar transferred on a CMOS chip. SEM taken after the epoxy etch process. The remains of the epoxy are visible on the sidewalls of the pillar and pillar is actually sitting on an epoxy cushion.

The alignment problems with the bonder limited the development of the APB technology. The unreliable co-planar alignment diminished the yield of the bonding experiments. Each trial requires the preparation of one pair of chips, and it is not possible to re-use the pillar chip again if the bonding is not successful. Figure 3-15 shows the micrograph of a pillar chip after a failed attempt of bonding. As can be seen from the figure, the metal on the top surface of the pillar has lost its uniformity after the bonding (due to re-flow and contact with the other substrate). Each pillar chip is 1 cm^2 in area, and only 10 or so such chips can be cleaved from an InP epitaxy wafer of 5 cm diameter. Because of the need of an epitaxial etch stop layer, the typical epitaxial thickness is 6-8 microns, and thus the development of the APB process is very wasteful of the epitaxial material.

Figure 3-15: Micrograph showing the poor condition of the AuSn alloy on the top surface of an InP pillar after an unsuccessful bonding attempt.

It was concluded that a new RM^3 technology that does not depend on aligned bonding should be sought. It is very likely that the results of APB would be more successful with a higher performance flip-chip bonder that had more advanced alignment features. Commercially available flip-chip bonders are designed to utilize solder bumps, and with solder bumps the co-planar alignment is not as crucial as it is for APB. Therefore it may be wise to work with a flip-chip bonder equipment manufacturer to have them custom-design a product that is suitable for pillar-to-recess bonding. However, the funding limitations at the time of this research work did not allow for the purchase of a custom-designed flip-chip bonder. As a result of this, the APB approach was not pursued any further, and a new RM^3 technique named OptoPill Assembly was proposed and implemented. Some of the process modules developed for the APB process were applied to OptoPill Assembly with minor modifications. These include the plasma etching procedures and bonding metallurgies.

3.2 OptoPill Assembly (OPA)

The OptoPill Assembly is a new RM^3 technology that offers several important advantages over the APB technique. OPA is suitable for CMOS integration, makes efficient use of epitaxial material, and does not require aligned wafer bonding. Optoelectronic heterostructures are processed into circular pills of 8 μm height and 45 μm diameter; the pills are released from the substrate, and collected. The OptoPills are then assembled into recesses on silicon chips using manual pick & place techniques, and they are bonded to the metal pads on the bottom surface of the recesses using AuSn solder bond. The gap between the pill and the surrounding recess walls is filled using benzocyclobutene (BCB), which also provides good surface planarization. Finally, the interconnect metallization can be carried out using conventional monolithic processing, like in other RM^3 technologies. OPA process flow is illustrated in Figure 3-16.

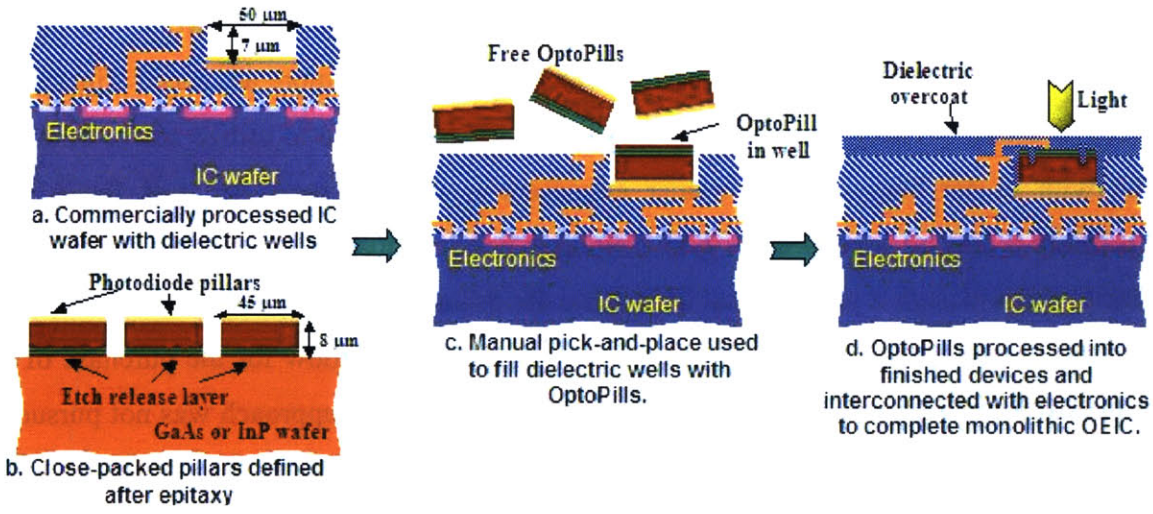

Figure 3-16: Schematic illustration of OptoPill Assembly

The following discussion can be divided into three parts: (a) OptoPill fabrication, (b) pill assembly and bonding; and (c) a series of post-fill processing steps.

3.2.1 OptoPill Fabrication

The process of making the OptoPills is comprised of three main parts. The first part is the fabrication of OptoPillars on the InP detector wafer. The second part is the InP substrate

removal process to release the OptoPills from the InP wafer. The final part is the collection of OptoPills in a clear methanol solution, which allows the easy manipulation of the OptoPills for the following manual assembly process.

3.2.1.1 Fabrication of OptoPillars

OptoPillar fabrication starts on a III-V wafer with heterostructures epitaxially grown on it, and continues with the deposition of a metal stack on this wafer. The metal stack is typically composed of three layers. The first layer is used to form an ohmic contact with the p-type InGaAs cap layer on the pillars. This will be discussed in more detail in Section 3.2.4. The second layer is a 300 nm film of nickel. The nickel layer serves two purposes. First, it provides a diffusion barrier against the AuSn solder deposited above the nickel layer itself. Due to the relatively large thickness of the solder, gold in the composition of this AuSn alloy can diffuse into the semiconductor, degrading the device performance, if no barrier layer is present between the AuSn and the semiconductor surface. Furthermore, nickel is a soft magnetic material, and the magnetic force of attraction between the nickel layer and a cobalt-samarium magnet placed under the chip during the bonding phase is used to obtain a clamping pressure for bonding the pillars into recesses. This magnet assisted bonding technique is discussed in Section 3.2.3.

The third and the final layer is a 600 nm AuSn solder. All metal layers were deposited in a single e-beam run on the planar epitaxial surface of the InP wafer, and a short buffered oxide etch dip was utilized immediately before the e-beaming of the metals to remove the native oxides on the surface of the InGaAs layer.

After the metal stack was e-beamed onto the heterostructure wafer, a hard mask (typically SiO_2) was deposited on top of the metal stack using chemical vapor deposition. The thickness of the oxide mask is 2 μm, which is thicker than the oxide masks used in APB since the oxide mask in OPA must be thick enough to withstand the etching of both the semiconductor and the metal stack. The oxide hard mask was patterned into a dense 2D array of circular shaped mesas with 45 μm diameter by using negative photoresist as an etch mask. The patterning of the oxide mask was done with dry etching in a plasma chamber as was mentioned before.

After the hard mask was patterned, the photoresist was removed, and the metal stack was etched using the patterned oxide as an etch mask. The etch employed the RF-sputtering technique in an argon plasma with an argon flow of 50 sccm and an RF power of 100KW. Under these conditions, the etching of the metal stack was completed in 100 minutes. The oxide mask is thick enough so that it stands during the RF-sputter etch and the following semiconductor etch.

After this step, the semiconductor pillars were etched in CH_4/H_2 plasma as was discussed in Section 3.1.1.2. The typical pillar height is 8-10 μm. After the etching of the semiconductor pillars was completed, the oxide mask was removed in CF_4/O_2 plasma. With a typical pillar array period of 100 μm, several thousand pills can be obtained from an epitaxial wafer of 1 cm^2 area, and this helps to reduce the use of the epitaxial material and processing costs. The OptoPillar fabrication process is illustrated in Figure 3-17.

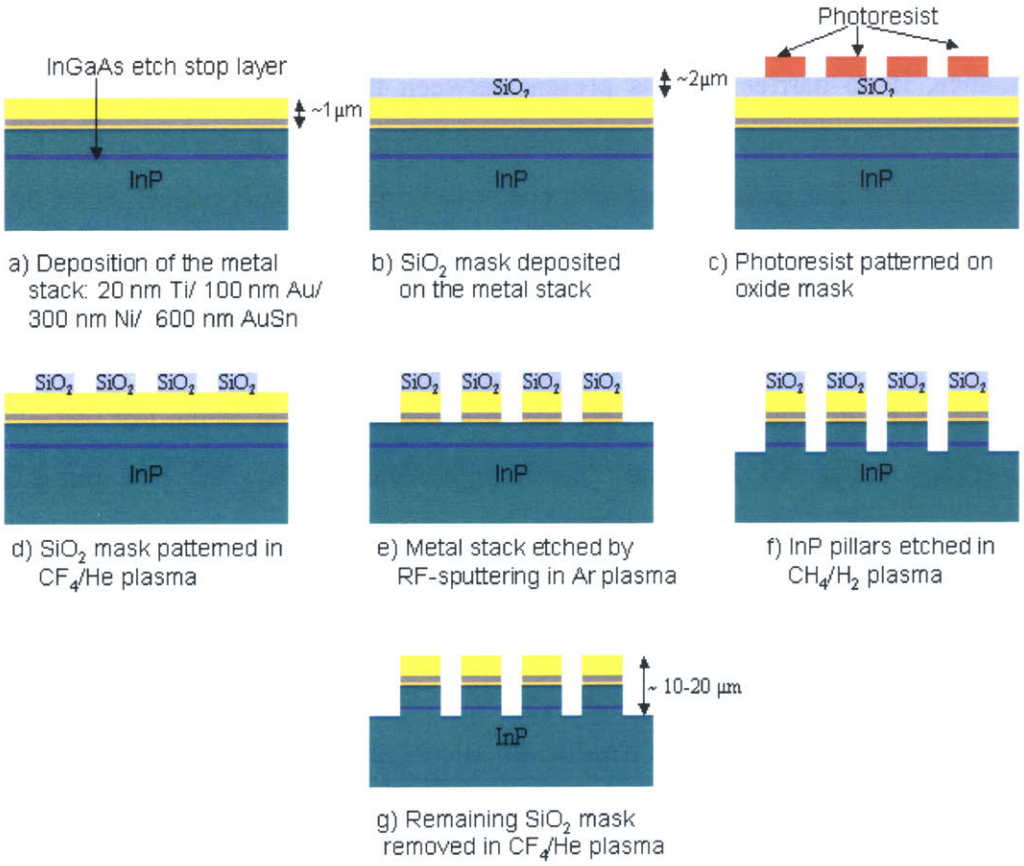

Figure 3-17: Illustration of the OptoPillar definition process

3.2.1.2 OPA InP substrate removal

After the OptoPillar processing is complete, the OptoPills must be released from the InP substrate. First, two layers of AZP4620 photoresist (~20 μm in total thickness) were spun on the front surface of the InP pillar wafer, and hard baked. This photoresist layer helps to protect the pillars from the substrate etchant, and it provides an easy way of collecting the pills after the substrate is etched away. Next, the pillar chip was dropped front-side down in molten wax (heated at 125°C on a piece of teflon), which covers the front surface and the edges of the chip. Special care is taken to prevent the molten wax from coming into contact with the back-side of the pillar wafer because even a thin layer of wax is very resistant to the substrate etchant, and it can block the substrate etch. Once the chip was immersed in wax (except its back surface), the chip and the wax were cooled down to room temperature to allow the solidification of the wax. The photoresist and the wax help to protect the front surface and the edges of the chip during the substrate removal etch which starts from the back surface of the InP pillar chip, and proceeds towards the front surface until it reaches the InGaAs etch stop layer of the OptoPillars.

The selective wet etchant that is used to remove the InP substrate is hydrochloric acid (HCl) with a concentration of HCl:H_20 (1:6). HCl can etch InP very rapidly, but its etch rate of InGaAs is extremely low (less than 10 nm/hour); thus it is a good substrate removal selective etchant for this material system. As the substrate etch nears completion, the circular shaped pills become visible embedded in photoresist and wax. When the pills become completely visible in the wax (with no residue of InP substrate left around them), the chip is taken out of the etchant, and the pills are collected using a process that involves decanting until the pills are in a clear methanol solution. The OptoPill collection technique is discussed in more detail in the next section. The substrate removal process is illustrated in Figure 3-18.

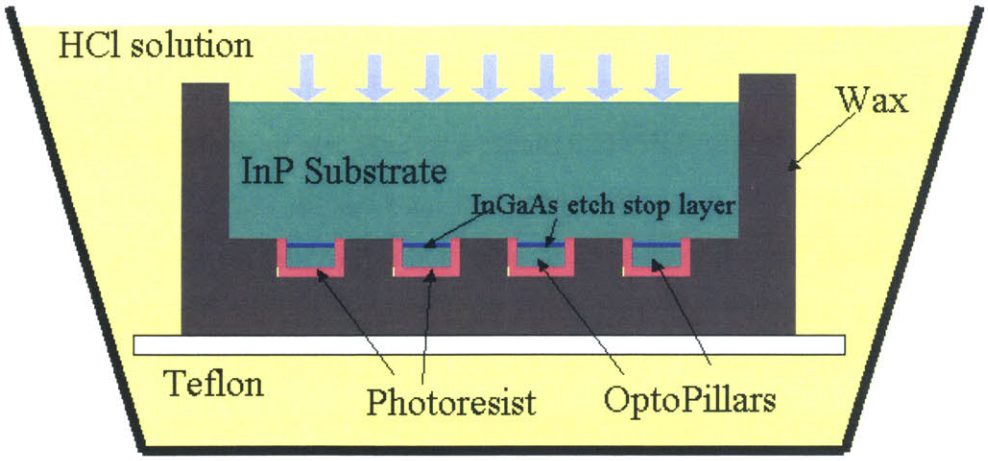

Figure 3-18: OPA InP substrate removal

During the substrate removal, the front sides of the pills are protected with photoresist and wax and the back side is the InGaAs etch-stop layer which is resistant to InP etching. However, it has been observed that undercutting of the InP buffer layers of the photodetector structure can occur in some of the OptoPills. The undercutting is easily detectable with the help of a microscope since HCl etches InP anisotropically, thus trimming the sides of the circular pills to turn them into squares, and the thin InGaAs etch stop layer on the top is transparent enough to view the square shaped InP buffer regions under the top InGaAs etch-stop layer. This undercutting can be significantly reduced if the substrate etching completes at the same time across the sample so that the sample can be taken out of the etchant immediately after the etch completes. As it will be discussed next, a procedure to improve the etch uniformity was implemented, and it significantly reduced the undercutting, but slight undercutting, which looked more like edge trimming, was still observed. However, the trimming of the sidewalls of the pill by a wet etchant can be advantageous since it can reduce the sidewall roughness due to deep dry etching.

The substrate etch rate along the back-surface of the InP wafer can vary if there is a residue of wax or photoresist left on the back-surface of the InP wafer from the processing prior to the substrate etch. This residue can initially block the etch on one part of the chip, causing the etch to complete later on that part of the chip. This problem was reduced by protecting the back-side of the chip with water-soluble tape when it is

immersed in molten wax. After the wax solidifies, the tape was removed in DI water. The photoresist residue in the back was cleaned by applying acetone using a Q-tip.

The negative effects of the non-uniform etching across the surface of the wafer can be reduced if the chip is immersed partially in the etchant when an etch non-uniformity becomes visible. Immersing only one part of the chip (the part that is etching more slowly) in the etchant is rather tricky since it requires human interaction (to hold the chip right above the surface of the etchant) and can result in an hazardous situation.

3.2.1.3 Collection of OptoPills in Clear Methanol Solution

After the InP substrate is removed, the next step is to collect the pills, which are embedded in wax and photoresist, in a clear solution so that the pills can be used in the assembly. This was done by placing the chip just above the opening of a cylindrical glass tube, and spraying acetone onto the chip. Acetone dissolves photoresist, but it is inactive against the wax. Since the pills are completely embedded in photoresist with no direct contact with the wax, pills can flow into the test tube along with the dissolved photoresist in an acetone solution while the solid black wax remains behind on the teflon substrate. After all pills are collected in the tube, the tube is filled up with acetone to dilute the dissolved photoresist solution. This process is illustrated in Figure 3-19.

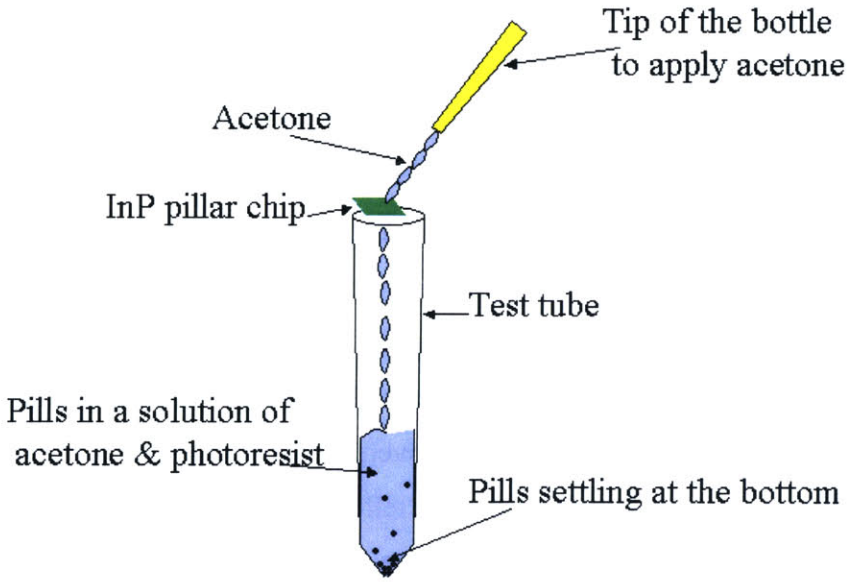

Figure 3-19: OptoPill collection inside a test tube

The tube is rested in vertical position for an hour to allow for the pills to settle at the bottom of the test tube. After the pills settle, the acetone solution in the test tube is decanted by using a pipette to suck the solution from the top surface of the tube all the way down to the bottom (approximately 2 cm above the bottom of the tube) where all the pills reside. The tube is then filled up with fresh acetone to decant the solution.

This process is repeated as many times as needed to completely wash the photoresist off the pills, and then the pills are transferred in a solution of methanol using the same technique. Methanol washes off acetone, which leaves behind significant residue as it evaporates due to its low vapor pressure. The pills are subjected to minimal damage during the application of this decanting procedure.

3.2.2 Micro-Scale Pick-and-Place (MPAP) Assembly Technique

There are two techniques that are being used to fill the recesses with OptoPills: micro-scale pick-and-place (MPAP), and magnetically assisted statistical assembly (MASA) [2]. MASA is a novel advanced version of what is often termed a "self-assembly" process. The research reported here concerns the first technique, MPAP. MPAP is viewed simply as a means to do assembly so the necessary post-assembly technologies could be developed in parallel with the MASA assembly process. MPAP involves dispersing OptoPills on a flat substrate, and picking them up using a micromanipulator like those commonly found on manual probe stations. The pills are then placed one at a time in the recesses on the CMOS chip, and they are bonded using an AuSn solder alloy.

The process developed begins by first dispersing a small quantity of pills on a copper-coated silicon substrate, and by then selecting those pills that have their metal coated side facing the substrate. The selection is carried out with the help of a microscope. The selected pills should not have visible undercutting. It is more difficult to pick the pills up if the AuSn side is up. Moreover, the AuSn layer is not transparent, and it is not possible to see through this layer to tell the undercutting of the pill under the probe tip. Pills that have significant undercutting are avoided since they can be broken easily during the pick and place assembly, and their active device area is reduced.

For the pills that settle with the AuSn side down, the undercutting can be inspected with the help of a microscope during the pick and place assembly. Figure 3-20 shows OptoPills dispensed on a silicon substrate to illustrate the pill selection process. Only the pills with the InGaAs side up and negligible undercutting are selected for the manual assembly process.

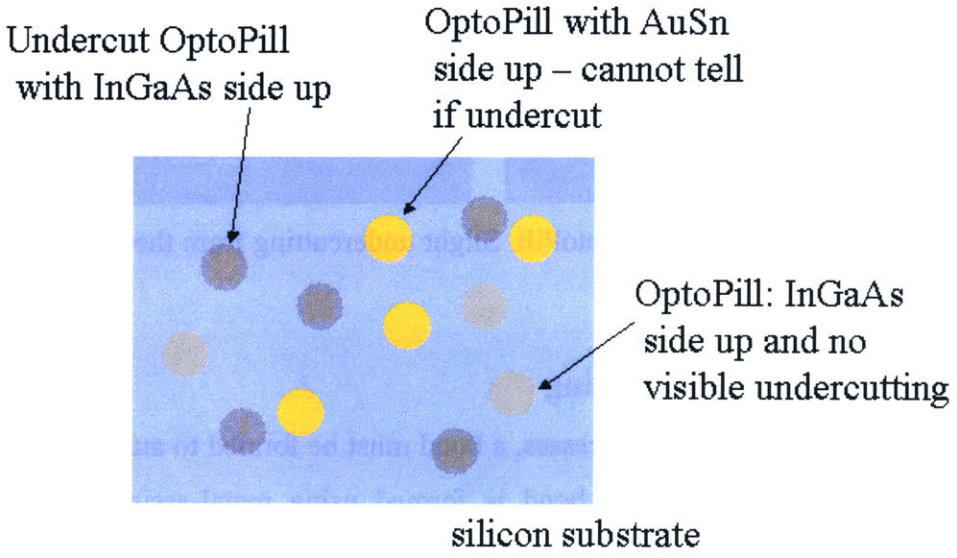

Figure 3-20: OptoPills dispensed on a silicon substrate for MPAP. Only the OptoPills with InGaAs side up and no visible undercutting are selected for the assembly process.

A fine probe tip wet with a thin coat of liquid solder flux was used to pick up the pills and place them in their recesses. The process was carried out by Mindy Teo, who developed the probe tip pick & place processes [39b]. The processing on the silicon substrate is very similar to the APB technique. Plasma etching is used to define the recesses, and the bottom surface of the recesses is then metallized for pill assembly and bonding using the lift-off technique. The typical metal stacks on the recess bottom include a UBM layer or a UBM layer along with AuSn solder much like in the APB process.

A close-up SEM of one of these OptoPills in a CMOS recess is shown in Figure 3-21. Clearly visible features are the UBM pad under the pill, the slight undercutting of the pill due to anisotropic InP substrate removal etch, and some damage on the top surface of the pill most likely due to the MPAP technique.

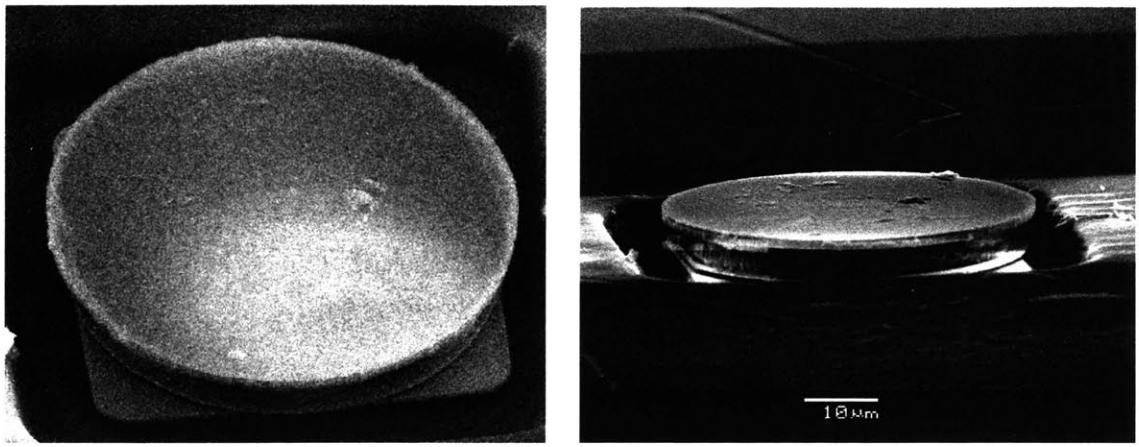

Figure 3-21: SEMs showing an OptoPill. Slight undercutting from the edges can be seen by close inspection.

3.2.3 Magnet Assisted Bonding

Once the pills are located in the recesses, a bond must be formed to attach the pills to the recesses. In RM^3 processes, this bond is formed using metal-assisted bonding. The metallic bond should keep the pill in the recess. Metallic bonds are formed by metal-to-semiconductor reaction or by soldering. The first method requires a high clamping pressure. It is not suitable for the OPA process where the pills are released from the handle wafer before the assembly, and thus it is difficult to apply high clamping pressure on the pills. Therefore, eutectic solder alloying is the preferred method for OPA.

As was mentioned before, the two surfaces must be in contact during the solder bonding, and furthermore, some clamping pressure must be applied in order to break the native oxide layers at the interface and provide a homogeneous contact between the to-be-bonded surfaces. In APB, much like in the other flip-chip technologies, a high clamping pressure can be provided by the flip-chip bonder, and it is simple to apply the desired pressure with this scheme so long as this pressure does not result in damage to the chips.

In OPA, on the other hand, it is not possible to utilize a flip-chip bonder since the pills are not attached to a handle substrate, and hence it is not as trivial to apply clamping pressure at the solder joints. Along with Mindy Teo [39b] and Vivian Lei [39c], two

different methods have been investigated for providing the clamping pressure required during the bonding phase of OPA. The first method utilizes the force of gravity. After the OptoPills are assembled into the recesses using the Pick & Place technique, the CMOS chip is placed on a graphite annealer strip. A thin stack of glass cover-slides is placed on top of the CMOS chip. In the current design of the optoelectronic device and the CMOS chip, the top surfaces of the assembled OptoPills are higher (~1 μm) than the final passivation surface of the CMOS chip; hence, it is expected that when placed on the chip, the glass cover-slides will be in contact with the surfaces of the OptoPills only and not with the surface of the CMOS chip. A drawback of this technique is that the cover-slides are much larger than the OptoPills, and it is difficult to balance the weight of the cover-slides on the OptoPills uniformly across the chip. The poor weight balance may result in a torque that can tilt the pills around one edge, and make it very difficult to obtain a flat bonding interface for all pills at the same time. Another disadvantage of applying this technique is in an RM^3 process where the OptoPills cannot be higher than the surface of the wafer. In this case, the weight will balance on the chip and not on the OptoPills. However, this was not a concern in the current application.

The second method, magnet assisted bonding, is a new technique which relies on the use of magnetic forces to obtain the clamping pressure needed for solder bonding. As before, the silicon chip with the OptoPill filled recesses was placed on a graphite annealer strip in a forming gas ambient. This time, a cobalt-samarium high temperature magnet was placed under the annealer strip as illustrated in Figure 3-22. A tiny gap was left between the magnet and the annealer strip to avoid direct thermal contact to the magnet. The magnetic attraction force between this hard magnet and the soft magnetic nickel film on the OptoPills causes the pills to get attracted downward towards the magnet, and hence the clamping pressure at the solder interface. Section 3.2.3.1 includes a discussion of the estimation of this clamping pressure.

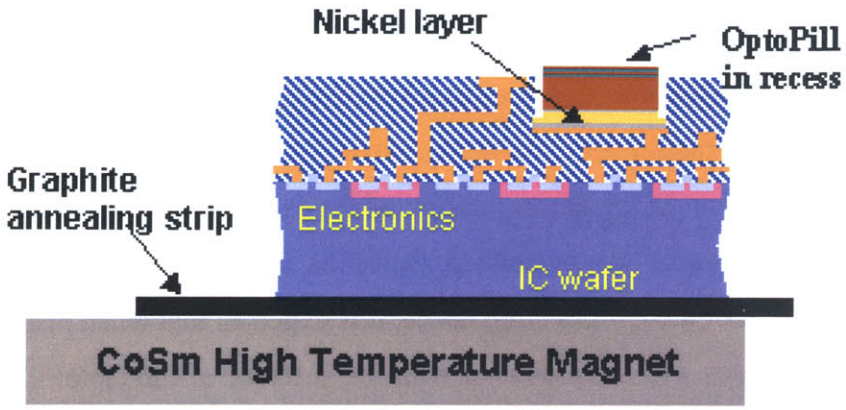

Figure 3-22: The chip and the magnet during the magnetically assisted bonding

A magnetic material is characterized by its hysteresis loop (Figure 3-23). This is a plot of B, the magnetic flux density, as a function of H, the applied magnetic field. In general, $\vec{B} = \mu_O(\vec{H} + \vec{M})$, where $\vec{M}$ is the magnetization. The main parameters that can be extrapolated from Figure 3-23 are the coercivity, H_c, the remanence, B_r, the saturation induction, B_s, and the permeability μ. The remanence is the flux density remaining when the applied magnetic field is reduced to zero. The coercivity is the magnetic field required to demagnetize the sample, or bring the magnetic flux density to zero. The saturation induction is the maximum value of magnetic flux density attainable in an external magnetic field. The saturation of the flux density results from the saturation of the magnetization, M_s, and is related by the equation $\overrightarrow{B_s} = \mu_O(\vec{H} + \overrightarrow{M_s})$.

The response of a material to an applied magnetic field is described by the magnetic permeability, μ. This quantity relates the magnetic field, H, and magnetic induction, B, through the equation, $\mu = \frac{B}{H}$. Materials with high magnetic permeability produce a high magnetic induction when placed in a field H.

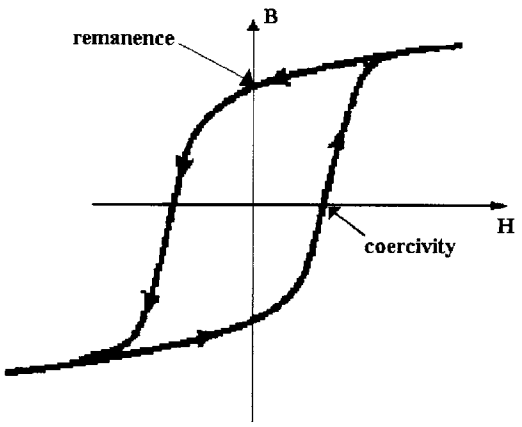

Figure 3-23: Typical magnetic hysteresis loop

Properties such as the saturation magnetization, M_s, depend only on what material is used. For instance, all bulk nickel samples should have the same M_s. Properties such as coercivity, remanence, and permeability however depend on sample shape, stress, crystal structure, grain size, and other physical properties.

Magnetic materials can be classified as either hard or soft. Hard magnetic materials typically have high coercivity and high remanence. These materials require larger applied magnetic fields to magnetize them than do soft magnetic materials. Moreover, once magnetized, hard magnetic materials are more difficult to demagnetize than soft magnetic materials. Therefore, hard magnetic materials are used to produce permanent magnets. Soft magnetic materials have lower remanence, lower coercivity, and higher permeability. These soft materials are relatively easy to magnetize and demagnetize.

The normalized in-plane and out-of-plane magnetic characteristics of a sputtered film of nickel on GaAs substrate die are shown in Figure 3-24 (re-printed from [42]). The data extracted from this plot is shown in Table 3-2. This data was collected at room temperature. Since the thickness of the nickel film is much smaller than the length and width of the substrate, it is expected that the shape anisotropy should be significant. Due to large shape anisotropy, the easy direction for magnetization is in-plane. Furthermore, magnetocrystalline anisotropy is low since the nickel film polycrystallizes as it was sputtered, and the nickel film is not thin enough to exhibit significant surface anisotropy.

Therefore, it is expected that the shape anisotropy is the dominant anisotropy, and magnetization is mostly in-plane. However, some out-of-plane magnetization is also observed as exhibited by the non-zero remanence of the out-of-plane hysteresis loop. The most likely cause of this non-zero remanence is the magnetoelastic anisotropy due to the stress resulting from the cooling of the nickel upon sputtering. In the simulations, the saturation of the out-of-plane and in-plane magnetization was ignored. This approximation was justified by calculating the magnitude of the field around the OptoPills. It was shown that the field was not strong enough to saturate the nickel films.

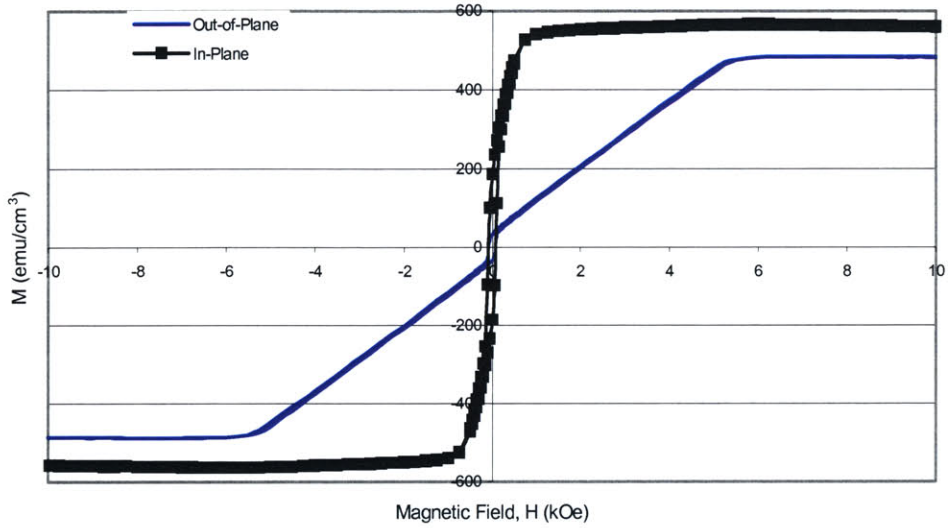

Figure 3-24: Magnetic hysteresis loop of a 0.38 micron sputter deposited nickel film on a GaAs substrate [42]

3.2.3.1 Estimation of the Magneto-Static Clamping Pressure

The magnetic attraction force between the OptoPills and the CoSm high temperature magnet is studied using two-dimensional magneto-static simulations. The simulation software used is Maxwell SV 2D Electromagnetic Simulator.

A mesh is defined to represent the geometry of the problem. The cobalt-samarium magnet used in the bonding experiments is disk-shaped with 0.75" diameter and 0.25" height. In the simulations, this magnet was represented with a rectangle that has 0.75" length and 0.25" height. The nickel layers on the OptoPills are also disk shaped (as the

OptoPills themselves) with 45 μm diameter and 300 nm height. In the simulations, the nickel films were represented with rectangles that have 45 μm width and 500 nm height. A film with thickness less than 500 nm could not be defined as it was not accepted by the simulations software. The thickness of the annealer strip is 1 mm and the thickness of the CMOS chip itself is 0.5 mm, thus the minimum separation between the surface of the magnet and the nickel film on the OptoPills is 1.5 mm. The geometry of the problem is illustrated in Figure 3-25.

The problem is defined using a rectangular coordinate system. As part of the software, a cylindrical coordinate system is also available for axisymmetric problems. A comparison was made between the results obtained for the same problem with these two different coordinate systems. The problem studied was the clamping pressure on the nickel pills located above the center of the magnet. Since this problem is axisymmetric, it can be modeled by both the cylindrical and the rectangular coordinate systems. It was shown that the force calculated with the cylindrical coordinate system does not deviate more than 2% from the force calculated with the rectangular coordinate system.

Another verification experiment was also performed. It is possible to calculate the pull force between a disk-shaped magnet and a metal film that are separated by a desired distance using online software tools [43]. Analytical and empirical results exist for the calculation of this pull force, and the computational methods used by the online software tools are derived from these results. It was shown that the 2D magneto-static simulator yields the same attraction force as the online tools when this problem was modeled and simulated in the Maxwell 2D simulator using the same strategy as in the OptoPill problem.

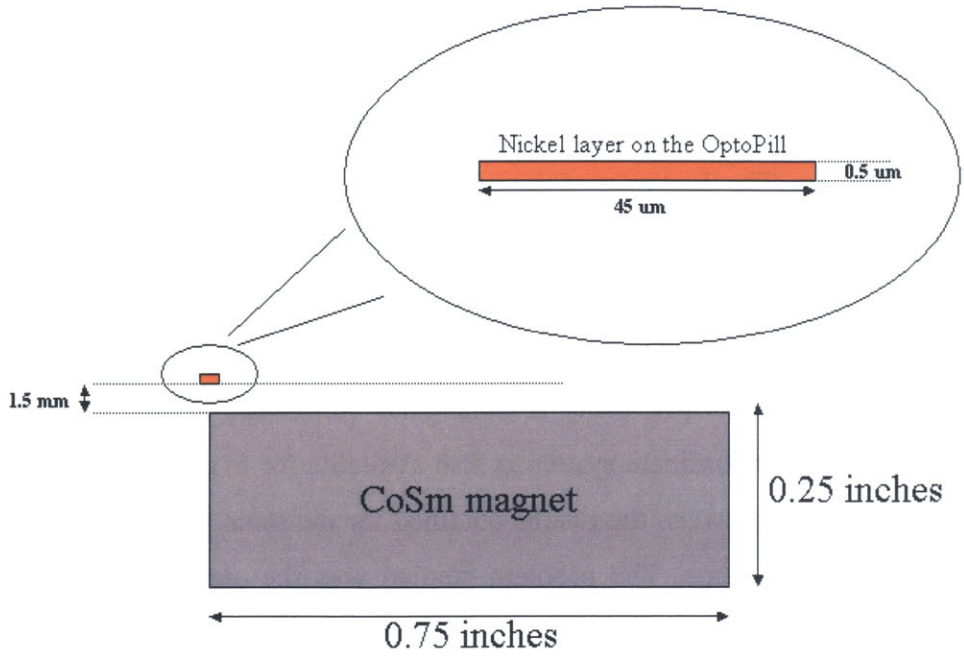

Figure 3-25: Problem geometry for 2D magneto-static simulations

After the geometry of the problem was specified, the magnetic properties of CoSm and thin film nickel were entered to the simulation software. The CoSm data was obtained from the simulation software itself, and it was checked against the references obtained from the vendor. B-H data for the nickel films was extrapolated from the data in Figure 3-24. The data used in the simulations is tabulated in Table 3-2.

Table 3-2: Magnetic B-H data used in the magneto-static simulations

	Permeability	H_c (A/m)	B_R (T)	M_p (A/m)
SmCo	1.04	820,000	1.07	850,000
Ni (in-plane)	3.33	55,000	0.23	183,000
Ni (out-of-plane)	0.58	55,000	0.04	32,000

Figure 3-26 shows the magnitude of the magnetic flux density around the CoSm magnet. As it was expected, the magnitude of the flux density becomes smaller further away from the magnet, and it is much larger around the edges of the magnet due to the fringing fields around the edges of the magnet.

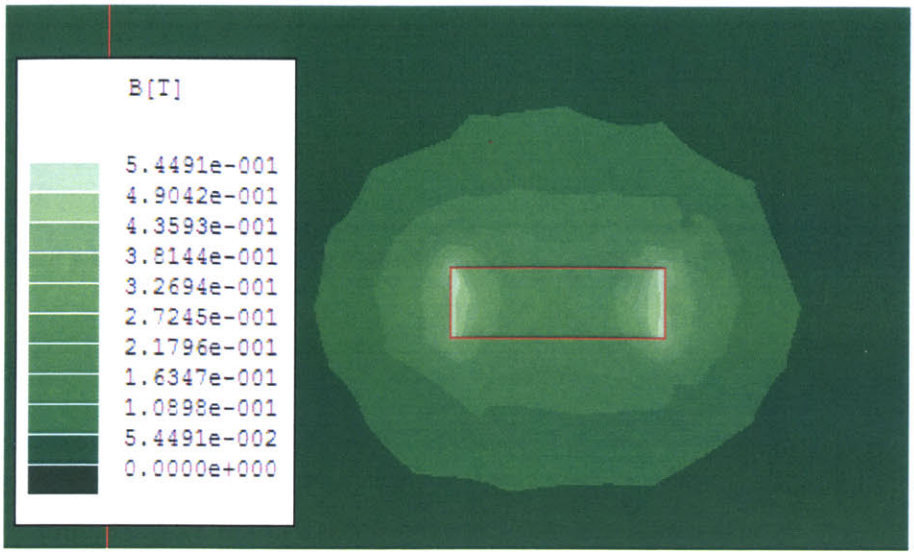

Figure 3-26: The magnitude of the magnetic flux density is shown around the CoSm magnet. CoSm magnet is indicated with the rectangle in the center of the figure.

The magneto-static simulations were used to calculate the force on the OptoPills. Due to the existence of stronger fields around the edges of the magnet, it was expected that the magnetic force on the OptoPills would be higher if the pills were placed close to the edges of the magnet. Figure 3-27 shows the variation of clamping pressure with horizontal distance from the center of the magnet. During these simulations, the distance between the OptoPills and the magnet was kept at 1.5 mm, which is the minimum distance that can be obtained using the apparatus in the lab. As it can be seen from this figure, the clamping pressure is the highest at the edge of the magnet, which corresponds to 9.5 mm on the graph.

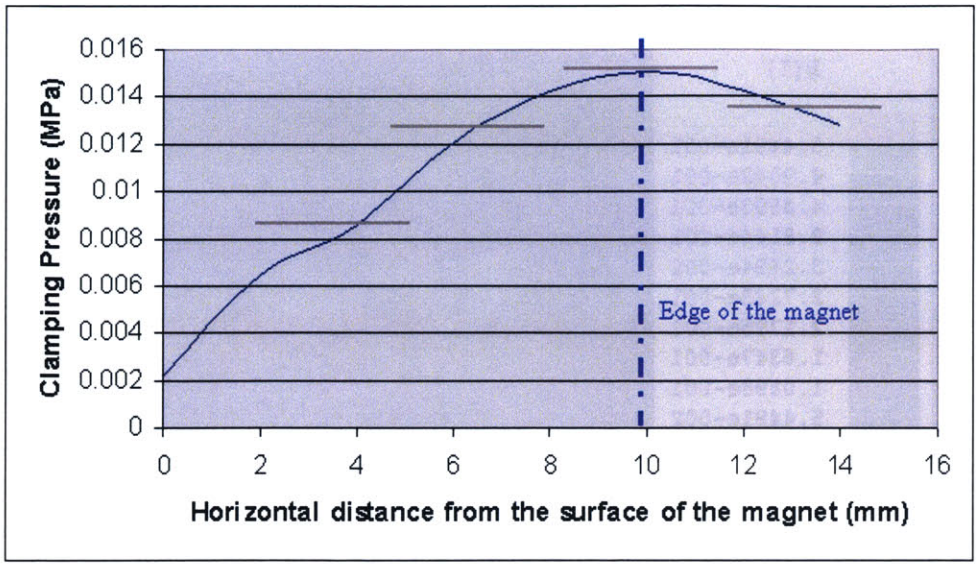

Figure 3-27: Clamping pressure on the OptoPill is shown as a function of the horizontal distance from the center of the magnet. The vertical separation between the magnet and the pills is kept at 1.5 mm.

The OptoPills on a CMOS chip occupy a square-shaped area with 3 mm on a side. Therefore, if the CMOS chips is located roughly centered on the edge of the magnet, the pills will take up the space from 8 mm to 10.5 mm along the horizontal axis shown in Figure 3-27, and the maximum deviation from the highest clamping pressure will be less than 10%. Hence, if the CMOS chip is located along the edge of the magnet, there will be close reasonably uniform clamping pressure on the OptoPills.

Next, the effect of the distance between the OptoPills and the magnet is investigated. This is done by analyzing the clamping pressure as a function of distance between the OptoPills and the surface of the magnet. The OptoPills are placed on the edge of the magnet as suggested by the previous simulation. Figure 3-28 shows the clamping pressure on the OptoPills as a function of the separation from the surface of the magnet.

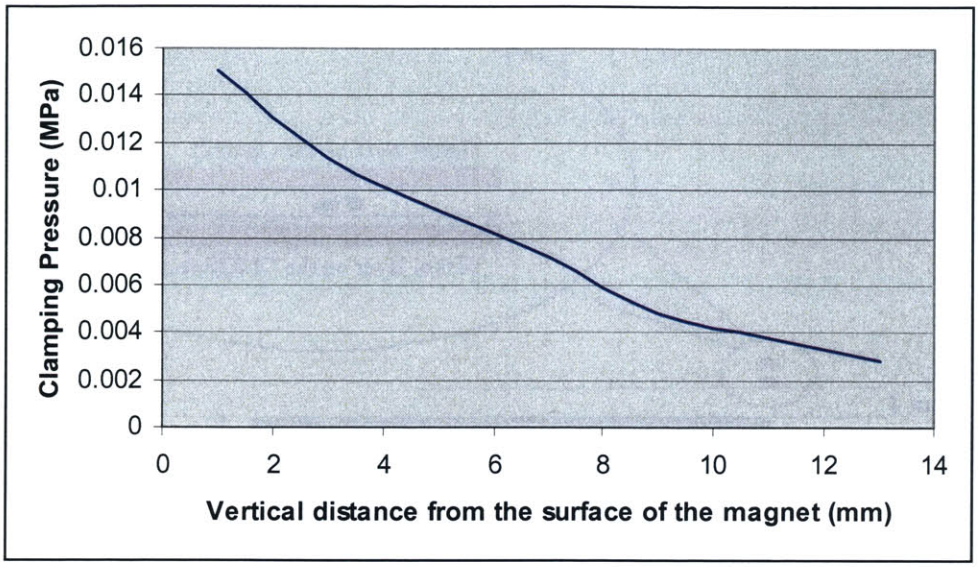

Figure 3-28: Clamping pressure on the OptoPills is shown as a function of the distance from the surface of the magnet. The pills are placed along the edge of the magnet.

The results of these simulations showed that significant clamping pressure can be obtained by using the magnet assisted bonding technique. Moreover, a method to further improve the clamping pressure during the magnetic bonding was also considered. Including a second layer of nickel in close proximity to the nickel layer on the OptoPill can improve the magnetic force of attraction by converging more of the magnetic flux lines towards the OptoPill area. The physical implementation of this is carried out by including nickel in the UBM stack on the recess. As it was previously discussed, including nickel as part of the UBM on the recess was considered in order to form a diffusion barrier between the aluminum bondpads and the AuSn solder. Thus, the same nickel film can serve two purposes at the same time.

To investigate this idea, 2D simulations were made by including a second layer of nickel as the bondpad nickel with identical geometry and material properties. In the actual assembly, there is a layer of solder and a wettable pad between the OptoPill nickel layer and the bondpad nickel layer. The total thickness of this intermediate metal stack is 1 μm, and thus the bondpad nickel layer is placed 1 μm below the OptoPill nickel layer to simulate the actual physical situation. The geometry of this problem is illustrated in Figure 3-29.

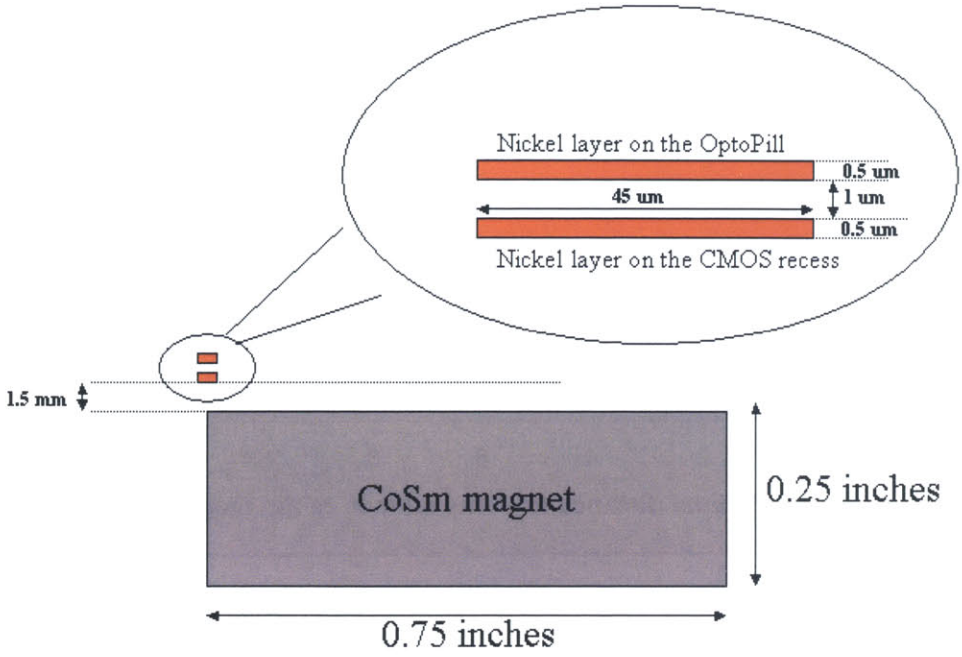

Figure 3-29: The problem geometry for 2D magneto-static simulations. The simulations are made with a secondary layer of nickel in the recess.

Inclusion of this secondary nickel layer has increased the clamping pressure on the OptoPill by 34%. The horizontal component of the magnetic force is small, thus the torque on the pills is small. Furthermore, the magnetic attraction force is enhanced by including a layer of nickel as part of the recess bondpad UBM, which results in a higher magnetic flux density around the OptoPill nickel layers.

Figure 3-30 shows the clamping pressure on the OptoPills when a nickel layer is utilized in the CMOS recess. If the chip is centered along the edge of the magnet, the clamping pressure varies at most 10% from the center of the chip towards its edge.

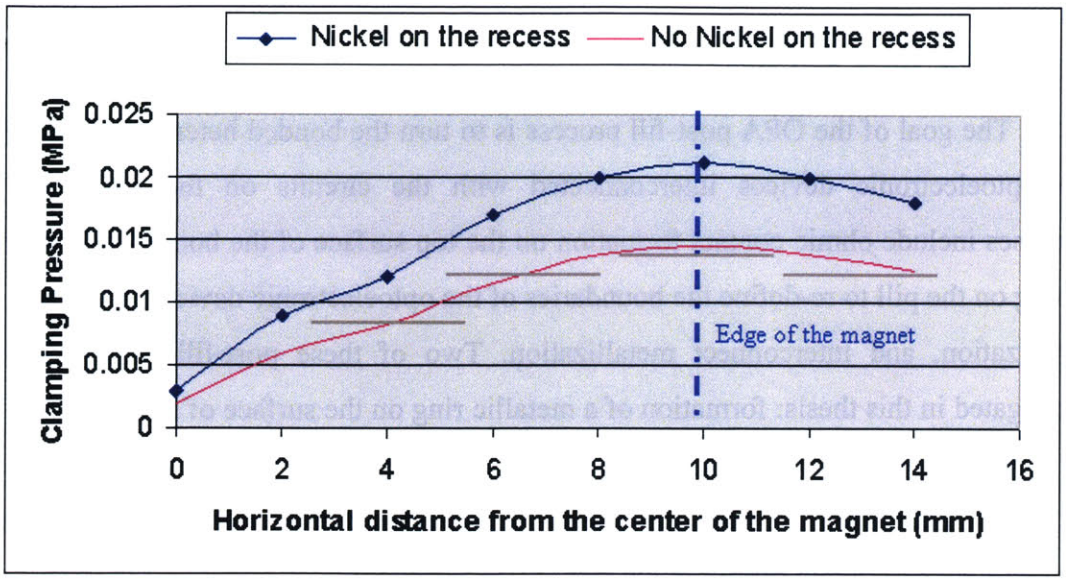

Figure 3-30: Magnetic clamping pressure as a function of vertical distance from the surface of the CoSm magnet. The OptoPills are placed on the edge of the magnet and the simulations include another layer of nickel under the OptoPills.

As the simulation results suggest, it is possible to obtain a clamping pressure more than 0.02 MPa using the magnetic interaction if the OptoPill is placed 1.5 mm above the surface of the magnet. That separation is closest to the achievable with the current setup where the thickness of the annealer strip is 1 mm and the CMOS chip itself is 0.5 mm thick. Results show that the magnetic force interaction can provide 0.02 MPa clamping pressure desired for the solder bonding if the magnet is placed in a way to maximize the force of attraction. As mentioned before, Bouwstra, et. al, demonstrate AuSn bonding with a clamping pressure of 0.07 MPa, which is in the same range with the 0.02 MPa pressure estimated by the magneto-static simulations.

In another experiment, the separation between the two nickel layers was varied from 0.25 μm to 2 μm, and the clamping pressure was calculated. The clamping pressure did not change more than 4% with the separation. The size of the recess nickel layer was also varied from 25 μm to 100 μm, and this did not yield a pressure change more than 2.5%. A ring patterned bottom nickel layer was defined in the cylindrical coordinate system to investigate the effects of the shape of the bottom nickel layer on the pressure. The result was only 3% different from the nominal case.

3.2.4 OPA Post-Fill Processing

The goal of the OPA post-fill process is to turn the bonded heterostructure pillars into optoelectronic devices interconnected with the circuits on the chip. Post-fill processes include ohmic contact formation on the top surface of the bonded pill, groove-etching on the pill to re-define the boundaries of the optoelectronic device, gap filling and planarization, and interconnect metallization. Two of these post-fill processes were investigated in this thesis: formation of a metallic ring on the surface of the OptoPills and gap filling and planarization using benzocyclobutene (BCB). These two processes are discussed in more detail in this section, and the patterning of the BCB and groove-etching processes are mentioned briefly in the end.

3.2.4.1 Ohmic Contact Formation on the OptoPill

After the pills are bonded into the recesses, the OPA Post-Fill process should proceed with the formation of an ohmic contact on the top surface of the pill. In this thesis, e-beam deposition with the lift-off technique was used to form square-shaped metallic ohmic contact rings on the top surface of the OptoPills. Figure 3-31 shows the micro-photograph of a metallic ring formed on the surface of an OptoPill. Using the MPAP technique, this pill was located in a recess opened on a silicon wafer, and it was bonded using the magnet assisted AuSn-to-Cu bonding process that was mentioned before. This bonding experiment was carried out with the help of Mindy Teo [39b].

An electrical testing of the device was performed by probing the contact ring on the OptoPill and the back surface of the silicon wafer. The measurement did not reveal diode characteristics as would be expected from the device (Chapter 2). The reason for this is the problems related with ohmic contact formation on the OptoPills. When the OptoPills were fabricated, Au was used to form an ohmic contact with the p-type InGaAs cap layer, which was the top surface of the epitaxial wafer. However, contact resistance measurements carried out with a calibration sample that had the same InGaAs doping profile revealed that Au does not form an ohmic contact with the device even after

alloying. Along with Vivian Lei [39c], it was shown that an alloyed ohmic contact can be formed using AuZn on p-type InGaAs with the particular doping ($5x10^{18}$ cm^{-3}). However, this contact must be annealed at 405°C, which is much higher than the melting temperature of the AuSn alloy (278°C). Therefore, it is essential to deposit the AuZn alloy and anneal it at this temperature before proceeding with the deposition of the other metal layers on the OptoPill such as nickel and the AuSn solder. Otherwise, AuSn can melt and re-flow, which can result in a rough metal surface prior to bonding.

The top surface of the OptoPill is n-type InGaAs ($5x10^{18}$ cm^{-3} doping level), and Ti/Au was used to form the ohmic contact ring on this surface of the bonded OptoPill. Unlike the p-side of the pillar, there is not a way of independently verifying the ohmic contact formation on the n-side since this side is only exposed after the substrate removal. However, it is predicted that Pd/AuGe can be used to form a non-alloyed ohmic contact on the n-type surface of the OptoPill [27]. Alloyed ohmic contacts should be avoided since typical alloying temperatures for this type of contact are higher than the melting temperature of AuSn, and heating the chip beyond this temperature can result in damage to the bond at the bottom of the recess.

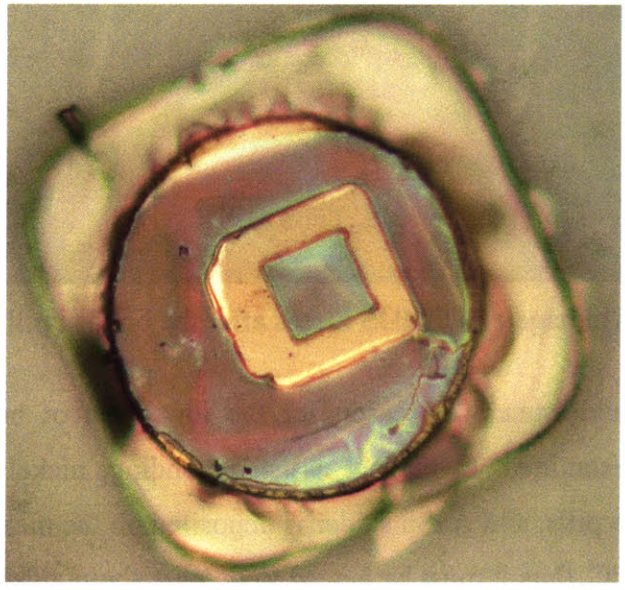

Figure 3-31: Metallic ring formed on the surface of the OptoPill after it was bonded onto a CMOS recess using the AuSn-to-Cu bond.

The experiments would be repeated using these new ohmic contact layers, but another problem regarding the bond strength needed further investigation since the yield of the bonding experiments were very low, and the OptoPills came out of the recesses during the lift-off process employed in ohmic contact deposition. For example, the same bonding experiment that resulted in the pill shown in Figure 3-31 was repeated using the same conditions, but this time the OptoPills came out of the recesses, not allowing the completion of the process. The OptoPill bonded onto the CMOS recess shown in Figure 3-32 was lost during the metal lift-off in acetone. In this experiment, AuSn inter-mixing technique was used, and the re-flow of the AuSn solder can be seen from the SEM. It is also interesting to note that de-wetting of the recesses or the pills was not observed suggesting good adhesion of the solders and the UBM pads onto the CMOS recess bonding pads and OptoPills.

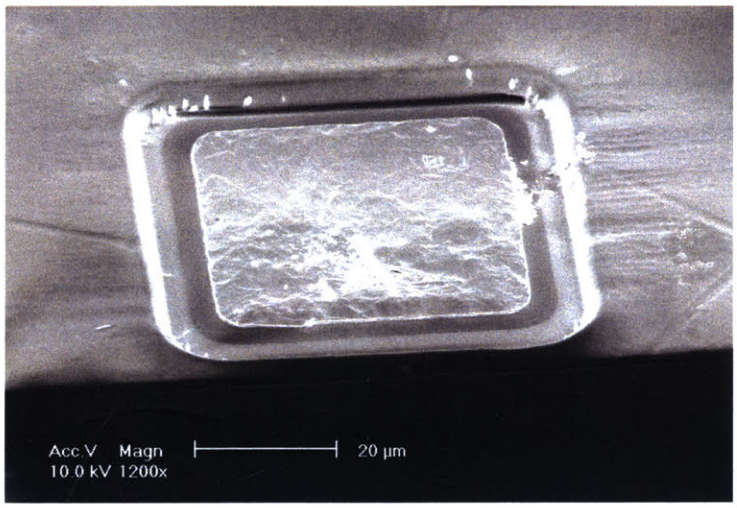

Figure 3-32: SEM image of a CMOS recess after the bonded pill has broken away

In order to understand the reason for the low yield of bonding, the bonding conditions were re-examined. In magnet assisted bonding, nickel is used as the soft magnetic layer on the pills, and AuSn solder is deposited on the nickel layer. AuSn has a melting point of 278°C, thus it must be heated to at least above this temperature to make the bond. The AuSn thin film bonding reported by Bouwstra was achieved at a temperature of 350°C using a clamping pressure of 0.07 MPa [41]. During the bonding

experiments carried out in this thesis using the magnet assisted bonding technique, the bonding temperature was varied between 280°C and 350°C. Nickel has a Curie temperature of 358°C. Looking at the magnetization vs. temperature plot for nickel in Figure 3-33, it can be seen that nickel's magnetization starts to degrade at 280°C, and it has very small magnetization left at temperatures around 350°C. In the lower end of the temperature range, nickel can retain its ferromagnetism, but the temperature is too low compared with the temperatures reported for thin film AuSn solder bonding. In the higher end of the temperature range, nickel loses its ferromagnetism. Because of the heat conduction across the silicon chip where the pills are assembled, the temperature of the nickel layers on different pills may vary during the bonding, thus resulting in the low yield of bonding that was observed.

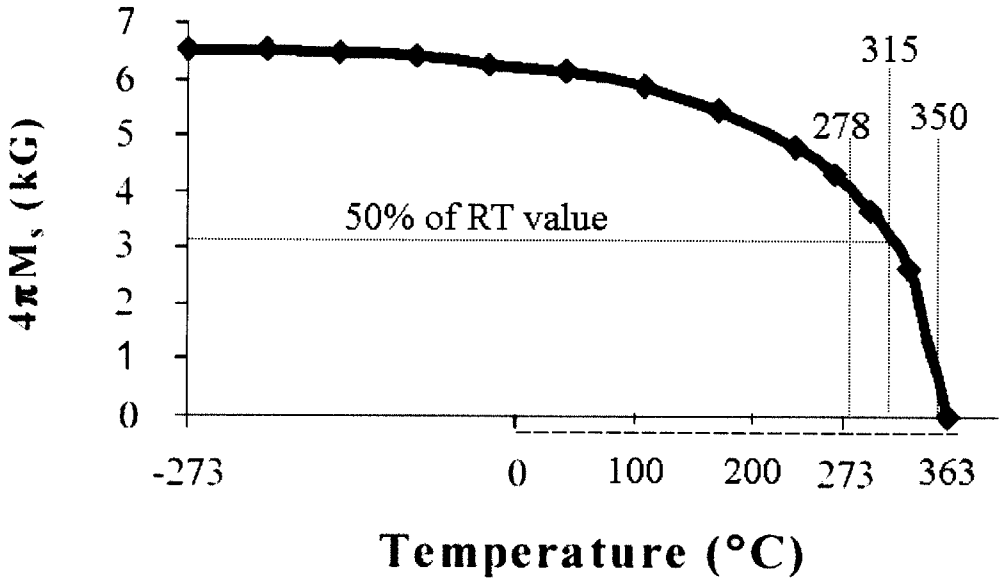

Figure 3-33: Magnetization of nickel as a function of temperature

The two other ferromagnetic metals that have higher Curie temperatures than nickel are iron (770°C) and cobalt (1170°C). The magneto-static force simulations yield similar results with these materials (assuming their bulk permeability), and the same clamping pressure can be expected. But since their Curie temperatures are higher, they can be heated up to 350°C without losing their ferromagnetism.

The actual physical implementation using these materials is challenging. Cobalt is a hard magnetic material, and using cobalt on the pills (instead of nickel) can result in the pills clumping together before the assembly. Depositing cobalt on the samples is a challenge since cobalt heats up very fast, and breaks the depository vacuum. Sputter etch may not work to pattern these materials because of the heating problems (and iron is too hard to sputter with our technique), so the current process is not applicable with these new metals.

3.2.4.2 Gap Filling and Planarization using BCB

To monolithically interconnect the OptoPills with the circuits on the chip, an interconnect should be formed between the ohmic contact ring on the surface of the OptoPills and an aluminum pad adjacent to the each pill. The aluminum pad is electrically connected to the circuitry using chip's own interconnects. However, the OptoPills are surrounded by a gap, which is 7 μm deep and 3 μm wide on each side. This gap must be filled and the top surface of the filling material must be planar enough to continue the monolithic interconnect processing. In the OPA processes, Dow Chemical's 3022-35 Dry-Etch Cyclotene benzocyclobutene (BCB) resin was used for this purpose as illustrated in Figure 3-34. This resin can be deposited with a minimum cured film thickness of 1 μm.

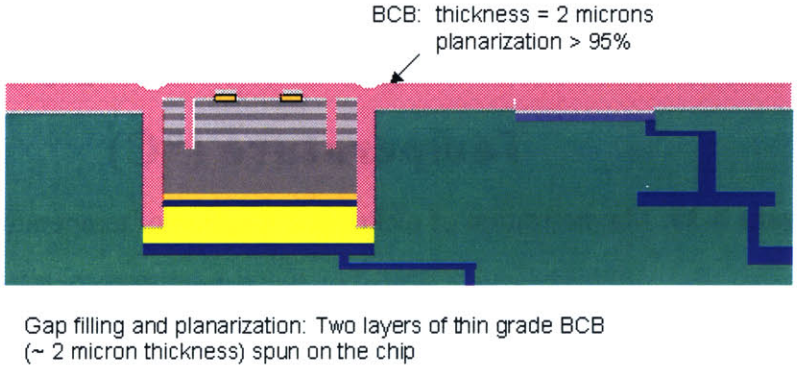

Figure 3-34: Illustration of the BCB gap filling and planarization for RM^3 processes

Along with Vivian Lei [39c], gap filling and planarization using BCB was demonstrated on a simulation sample prepared on a silicon substrate. A square-shaped groove ring was fabricated by plasma etching on a silicon substrate as shown on the left side of Figure 3-35. The ring is 40 μm on a side with 6 μm width and 8.5 μm depth. This structure was designed and fabricated to resemble a OptoPill bonded on a recess in the actual RM^3 process. Two layers of the BCB resin was coated on this simulation sample to fill the grooves and re-planarize the top surface.

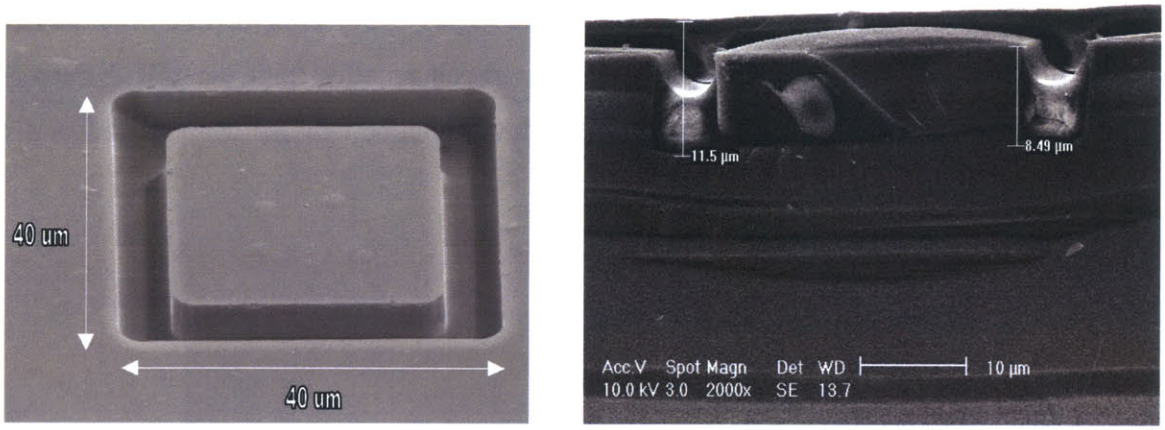

Figure 3-35: SEMs demonstrating the gap filling and planarization achieved with BCB: a) Groove ring etched in silicon (depth = 8.5 microns); b) Sideview of the same groove after 2 layers of BCB coating

The SEM image on the right-side of Figure 3-35 shows a side-view of the groove after two layers of thin grade BCB coating. As it can be seen from the picture, the first layer of BCB fills the gap almost to a half of its depth as only a very thin layer of BCB gets deposited on the planar surfaces of the chip. The second layer of BCB, which gets coated on the first layer following a short soft-cure, fills up the rest of the gap, and it provides more than 95% of planarization on the top surface. After the gap filling, the final thickness of the BCB on the top surface of the chip was 2 μm.

BCB should be patterned to open vias for fabricating the electrical interconnects between the OptoPills and the adjacent pads on the silicon chip. The Dow Chemical's 3022-35 Dry-Etch Cyclotene BCB is a dry etch grade resin, as discussed in [44], its plasma etching can be carried out using a photoresist etch mask. AZP4620 photoresist exhibits a BCB/resist selectivity of 0.7 at an etch rate of 0.7 μm/min when etched in a 9:1

oxygen:CF_4 plasma under 200 mTorr pressure with an RF power of 300W [44]. The thickness of the BCB on the top surface is only 2 μm, thus 3 μm of AZP4620 photoresist can be used as an etch mask.

3.2.4.3 Other Post-Fill Processes

After the fabrication of the ohmic contacts, the boundaries of the optoelectronic device can be re-defined by etching a groove on the pills that is deep enough to penetrate the heterostructure layers (~2 μm) as illustrated in Figure 3-36. This may be necessary if the desired size of the optoelectronic device is much smaller than the pill diameter. Moreover, the boundaries of the optoelectronic device can be isolated from the sidewalls of the OptoPills.

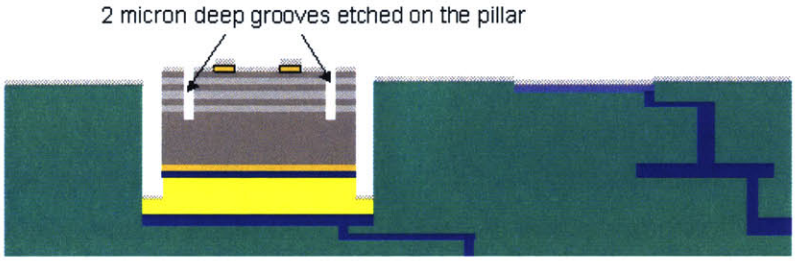

Figure 3-36: Illustration of the optoelectronic device definition process by groove-etching.

3.2.5 Summary of OPA Results

The four important constituents of the OPA technique are the OptoPill fabrication, the Pick & Place manual assembly technique, the magnetic force assisted bonding and the post-fill process utilizing the BCB. In this section, the findings of this thesis on these parts will be reviewed.

The fabrication of OptoPills in the InGaAs/InP material system was demonstrated as mentioned in Section 3.2.1. Partial undercutting of the OptoPills was observed, which is suspected to occur during the substrate removal phase. There are a number of ways to improve the quality of the OptoPills. The first one is to use a commercial foundry to grow the hetererostructures to reduce the risks due to possible defects within the material

system, more specifically the InGaAs etch stop layer. A defected InGaAs etch stop layer can cause the undercutting problem observed here. The second method is to develop a more advanced dry etching process designed for OptoPillar fabrication. The sidewall roughness of the OptoPillars should be reduced to help the photoresist to protect the front surfaces of the OptoPills from the substrate etchant. Finally, the substrate etching process can be improved by designing a new wet etchant system.

The Pick & Place manual assembly technique can be hazardous for the OptoPills as it involves the manipulation of the OptoPills with probe tips. In IC manufacturing plants, it is common practice to prevent the wafers to come into contact with any sharp object during the entire process flow. Manipulating the OptoPills with probe tips is essentially a violation of this rule. The Pick & Place technique can be used for demonstrational purposes in the context of a thesis work, but an automated pill assembly technique needs to be developed if OPA is ever to be employed in full-wafer-scale fabrication.

Magnetic force assisted bonding was proposed because a method is needed to exert clamping pressure on the OptoPills that are then assembled into recesses etched into IC chips. Though it is a promising, new technique; the magnetic force assisted bonding experiments that are carried out here did not reveal preliminary success. As it is discussed in Section 3.2.4.1, nickel, the soft magnetic material used in OptoPill fabrication, does not have a Curie temperature that is high enough to preserve its ferromagnetism during the bonding process. However, there are a number of methods that can be used to improve the magnetic force assisted bonding technology. The first one is to use a different magnetic material system, which has a higher Curie temperature. Iron and cobalt are two of the candidates as mentioned in Section 3.2.4.1. The second way is to devise a magnetostatic bonding apparatus through a more advanced analysis of the magnetostatic force fields with the goal of maximizing the clamping pressure on the OptoPills.

It should be noted that magnetostatic force assisted bonding can find use in a number of applications where micron-sized free-standing structures need to be bonded onto larger wafers. In author's opinion, it is a technique which is certainly worth exploring further.

Finally, it was shown that the BCB can be used as a good gap filling and planarization agent during the post-fill processes as discussed in Section 3.2.4.2. The processing of BCB is well-understood, and in this work, it was shown that BCB is suitable for the post-fill processing of the OPA technique.

3.3 Summary of the RM^3 Process Development

In this chapter, the research efforts on two different RM^3 processes are mentioned: APB and OPA. APB aims to utilize a flip-chip bonder to do optoelectronic integration. As it is discussed in Section 3.1.6, the challenge of pillar-to-recess bonding with a conventional flip-chip bonder that is designed to utilize solder bumps makes it difficult to obtain a good bond at the pillar-to-recess interface. In order to evaluate the success of a flip-chip bond, one must first carry out the substrate removal process as described in Section 3.1.5. An epoxy was utilized in the substrate removal process, and cleaning the epoxy from the surface of the chip could be problematic due to the charring of the epoxy.

OPA does not need a flip-chip bonder as it was described in Section 3.2. OptoPills of semiconductor heterostructures are released from their substrate, and then they are manipulated with probe tips and placed in recesses etched on IC chips. The bonding has to be performed with free-standing pills, and the conventional wisdom of applying the bonding force via the substrates does not hold. All of this makes the OPA a truly "exotic" process, which requires more time and resource allocation to research more thoroughly.

One should also mention that neither of these processes can be trivially applied to IC fabrication at the wafer scale. For the APB, one needs to devise a stepper-like flip-chip bonder that will move across the IC wafer to do the bonding one-chip-at-a-time. However, the execution of the substrate removal process at the full-wafer scale remains a challenge. For the OPA, one needs to replace the manual Pick & Place technique with a more automatic method to fill up the recesses with OptoPills. Fluidic self-assembly methods are being researched for this purpose, but these are low yield techniques, and they are not to be employed on a semiconductor wafer after the IC fabrication procedure is completed. This is because the IC manufacturer will first have to carry out the IC fabrication process to completion, which is costly, and then the low-yield self-assembly

techniques can be employed to utilize OPA. Using a low-yield procedure in the end of a costly fabrication cycle are usually avoided.

As a conclusion, the APB technique requires a custom-designed flip-chip bonder, and for the OPA, more work needs to be done to improve the OptoPill fabrication, the OptoPill assembly, and the magnet-assisted bonding processes.

Chapter 4

Summary and Conclusion

This thesis was concerned with the development of the Aligned Pillar Bonding and OptoPill Assembly optoelectronic integration technologies. The initial focus of the research was the APB technique. A series of processing modules have been developed, and they have been implemented along with several process refinements in the context of the APB research. However, the insufficient co-planar alignment capacity of the particular flip-chip bonder utilized did not allow the successful bonding of the pillar and recess pairs. The alignment problems with the bonder, and more specifically the unreliable co-planar alignment diminished the yield of the bonding experiments. As mentioned in Section 3.1.6, it has been observed that if the two chips do not have the proper co-planar alignment, they will come into contact at a surface other than the designated bonding interface, thus preventing the pillars from coming into contact with the bonding pads inside the recesses. Occasionally, the two chips can be attached together at this surface after an attempt of bonding, and it may not be possible to distinguish this from a real bond at the desired interface. As a result of this, the processing efforts were shifted towards OPA.

OPA does not require the use of a flip-chip bonder, and it makes very efficient use of the epitaxial wafer. However, OPA needs a reliable mechanism to locate the OptoPills in recesses etched on the silicon chips. A new technique named Micro-scale Pick and

Place (MPAP) was investigated along with Mindy Teo [39b]. This technique is based on picking the OptoPills dispersed on a substrate with the help of a probe tip, and locating them in the recesses prepared on silicon chips. After the OptoPill is located in a recess, it is bonded to the bonding pad in the bottom of the recess utilizing an AuSn solder bond. A new bonding technique termed magnet assisted bonding is used to provide clamping pressure for during the formation of the AuSn solder bond. In magnet assisted bonding, the magnetic force of attraction between the nickel layer on the OptoPill and a CoSm magnet placed under the chip during the bonding is used to obtain a clamping pressure on the pill to assist during the bonding. An estimation of the magnetic clamping pressure was made using magneto-static simulations, which revealed a clamping pressure in the order of the ones used in AuSn thin film bonding experiments [41]. The bonding procedure was carried out using the AuSn-to-Cu bonding technique, and after the bonding of the OptoPill, the post-fill processing was continued to form a metallic contact ring on the surface of the OptoPill. However, the electrical measurements did not yield the response that was predicted in Chapter 2 due to an ohmic contact problem with the InGaAs cap layers used in the work. As is is discussed in Section 3.2.4.1, the OptoPills were fabricated with an Au layer to form an ohmic contact to the p-type InGaAs cap layer of the heterostructure, but contact resistance measurements carried out on a different sample have revealed that it is not possible to form an ohmic contact in this way, even after alloying. A set of new ohmic contact metals has been identified for the OptoPills. Along with Vivian Lei [39c], it was shown that an alloyed ohmic contact can be formed using AuZn on p-type InGaAs with the particular doping ($5x10^{18}$ cm^{-3}). However, this contact must be annealed at 405°C, which is much higher than the melting temperature of the AuSn alloy (278°C). Therefore, it is essential to deposit the AuZn alloy and anneal it at this temperature before proceeding with the deposition of the other metal layers on the OptoPill such as nickel and the AuSn solder. Otherwise, AuSn can melt and re-flow, which can result in a rough metal surface prior to bonding.

For the p-type InGaAs layer, an ohmic contact was achieved using alloyed AuZn. However, for the n-type InGaAs, no investigations were possible with the current heterostructures since the n-type InGaAs layer is on the substrate side, and it is not

exposed until the pills are fabricated. It is predicted that Pd/AuGe can form a non-alloyed ohmic contact with the n-type InGaAs layer of the particular doping used in this work.

The major factor that limited the further investigation of this problem is the low yield of bonding. During the ohmic contact formation, the OptoPills came out of the recesses where they were bonded to. The origin of this problem is the demagnetization of nickel in the bonding temperature range used with AuSn solder bonds. Typically, AuSn thin film bonds are made at temperatures around 350°C, and nickel loses most of its ferromagnetism above 300°C, diminishing the magnetic force on the OptoPill.

One solution to this problem is the use of ferromagnetic metals such as cobalt or iron that have higher Curie transition temperatures. However, cobalt is a hard magnetic material, and its permanent magnetization can cause the OptoPills to clump together in the process of OptoPill collection, making it very hard to separate them to locate them in recesses using the micro-scale Pick and Place technique. The application of the current OptoPill process using these materials can also be more challenging than nickel. E-beam deposition of cobalt does not have a good rate of success since it heats up very fast during the e-beam deposition, and damages the e-beam deposition monitor crystal.

4.1 Directions for Future Research

As is is discussed in Section 3.1.6, it is very likely that the results of APB would be more successful with a higher performance flip-chip bonder that had more advanced alignment features. Commercially available flip-chip bonders are designed to utilize solder bumps, and with solder bumps the co-planar alignment is not as crucial as it is for APB. Therefore it may be wise to work with a flip-chip bonder equipment manufacturer to have them custom-design a product that is suitable for pillar-to-recess bonding.

A new soft ferromagnetic layer can be investigated for the OptoPill fabrication. This layer should have a high Curie transition temperature so that it can retain its ferromagnetism at the temperatures used in AuSn soldering (~350°C). In this way, the desired clamping pressure can be obtained using the magnet assisted bonding technique. Easy deposition and etching (with RF-sputtering) along with electrical conductivity are the other desired features of such a soft ferromagnetic layer. It is also advantageous if this

layer can be utilized without a need for a significant modification in the OptoPill fabrication process. Alloys of nickel and other metals can be investigated for this purpose.

A magnetostatic bonding apparatus can be designed and built through a more advanced analysis of the magnetostatic force fields with the goal of maximizing the clamping pressure on the OptoPills. In this thesis, a two-dimensional magnetostatic simulator is used to estimate the strength of the magnetic clamping pressure between the OptoPills and the recesses. The geometry that is used is the most trivial "chip-on-a-magnet" geometry. A more advanced magnetic force generator can be designed that will give the best results for the magnetic force assisted bonding.

The Pick & Place manual assembly technique can be used for demonstrational purposes in the context of a thesis work, but an automated pill assembly technique needs to be developed if OPA is ever to be employed in full-wafer-scale fabrication. Fluidic self-assembly is one alternative [53]. A more automated version of Pick & Place can also be implemented, where a sensory system is used to select the pills, and then move them into the recesses. Both of these technologies are difficult to implement, but they are not really needed in the context of a thesis research, where the processing is limited to chips but not to full wafers.

It is also imperative to separate the bonding experiments from the electrical characterization of the OptoPill to minimize the problems regarding ohmic contact formation. This can be done by using a more simple resistive pill structure as shown in Figure 4-1. This pill is made up of a highly doped n-type InP layer sandwiched between two n-type InGaAs layers. If the InGaAs layer is grown with a doping level of 10^{19} cm^{-3}, it is possible to use non-alloyed ohmic contacts as mentioned in [27]. Furthermore, if the same InGaAs layer is utilized on both sides of the pillar, the same ohmic contact metallization can be used for the bottom plate and the top ring. As was mentioned before, the current p-i-n heterostructure does not allow the independent testing of the ohmic contact formation on the n-type InGaAs layer. Another possible solution to this problem would be to grow a calibration sample along with the p-i-n heterostructure in the same

chamber. If the calibration sample is grown with the same n-type InGaAs layer on the top then that layer can be used to independently verify the ohmic contact formation.

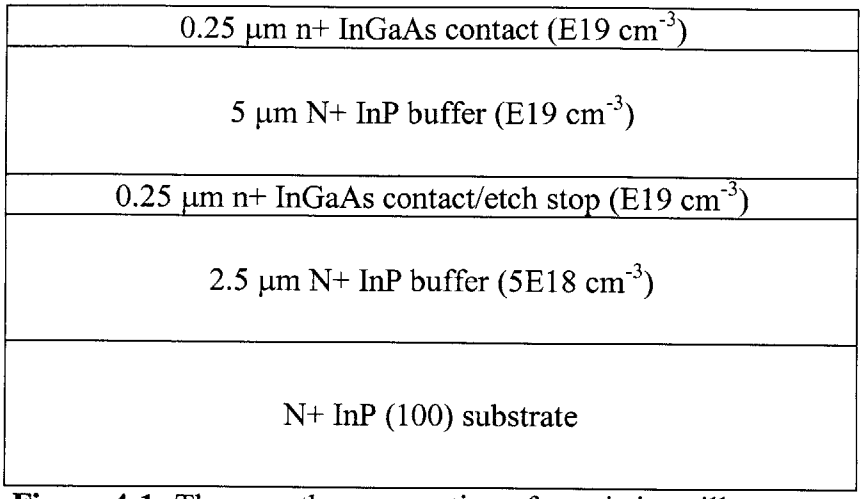

Figure 4-1: The growth cross-section of a resistive pill structure

As it is discussed in Section 3.2.5, there are a number of ways to improve the quality of the OptoPills. The first one is to use a commercial foundry to grow the hetererostructures to reduce the risks due to possible defects within the material system, more specifically the InGaAs etch stop layer. The second method is to develop a more advanced dry etching process designed for OptoPillar fabrication. The sidewall roughness of the OptoPillars should be reduced to help the photoresist to protect the front surfaces of the OptoPills from the substrate etchant. Finally, the substrate etching process can be improved by designing a new wet etchant system.

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