

Comparator Design and Analysis for Comparator-Based Switched-Capacitor Circuits

by

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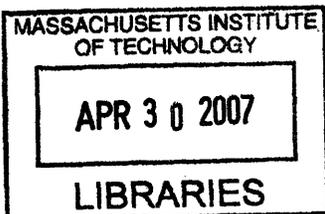
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Abstract

The design of high gain, wide dynamic range op-amps for switched-capacitor circuits has become increasingly challenging with the migration of designs to scaled CMOS technologies. The reduced power supply voltages and the low intrinsic device gain in scaled technologies offset some of the benefits of the reduced device parasitics. An alternative comparator-based switched-capacitor circuit (CBSC) technique that eliminates the need for high gain op-amps in the signal path is proposed. The CBSC technique applies to switched-capacitor circuits in general and is compatible with most known architectures. A prototype 1.5 b/stage pipeline ADC implemented in a 0.18 μm CMOS process is presented that operates at 7.9 MHz, achieves 8.6 effective bits of accuracy, and consumes 2.5 mW of power.

Techniques for the noise analysis of comparator-based systems are presented. Non-stationary noise analysis techniques are applied to circuit analysis problems for white noise sources in a framework consistent with the more familiar wide-sense-stationary techniques. The design of a low-noise threshold detection comparator using a preamplifier is discussed. Assuming the preamplifier output is reset between decisions, it is shown that for a given noise and speed requirement, a band-limiting preamplifier is the lowest power implementation. Noise analysis techniques are applied to the prototype CBSC gain stage to arrive at a theoretical noise power spectral density (PSD) estimate for the prototype pipeline ADC. Theoretical predictions and measured results of the input referred noise PSD for the prototype are compared showing that the noise contribution of the preamplifier dominates the overall noise performance.

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Dedication

I dedicate this thesis to my Grandmother Beulah T. Fleming (January 6, 1912–August 11, 2006) who passed away during my final days at MIT. Her letters and phone calls were always a welcome respite from life as a graduate student. I could always count on her being awake at all hours of the night, eager to hear about recent events in my life, and willing to share her thoughts on current events or memories of days gone by.

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Chapter 1

Introduction

1.1 Motivation

The design of switched-capacitor circuits in scaled CMOS technologies is becoming increasingly difficult. Although parasitic capacitances are reduced at each successive technology node allowing for faster or lower power operation of analog circuits, other factors such as reduced power supply voltages, lower device output resistance, increased flicker noise, and charge leakage paths present challenges to switched-capacitor circuit designers.

Charge storage in scaled CMOS technologies is a looming problem. In the past, only reverse biased diode leakage at the source and drain junction were of concern, but sub-threshold drain current leakage and gate current leakage are becoming significant¹. Existing solutions to this problem involve controlling the bias voltages on devices in their off state to minimize the leakage current [3] [4] [5]. Another alternative is to operate the circuits faster than otherwise necessary to minimize leakage charge error ($\Delta Q \propto I_{leak}/f_s$).

Unfortunately, the pocket (halo) implant [6] routinely used in scaled technologies to prevent punch-through and control short channel threshold voltage effects has

¹For a good overview of leakage sources in scaled technologies see [1] [2].

the unintended side effect of increasing the flicker noise in scaled technologies [7]. Using devices with a larger gate area WL does reduce the input referred flicker noise PSD, but it requires an increase in power consumption to maintain the same speed of operation. Traditional techniques such as correlated double sampling or chopper stabilization can be used to eliminate flicker noise [8], but larger amounts of flicker noise may require performing these functions at frequencies higher than the required Nyquist sampling rate for the input signal bandwidth.

Lower supply voltages reduce the amount of voltage headroom available for the output voltage swing of op-amps. To maintain the same dynamic range, the input referred noise of the op-amp must be reduced. Reducing the op-amp noise requires an increase in the compensation capacitor C_c , but the power consumption must also be increased to maintain the same speed of operation G_m/C_c .

Another major difficulty in op-amp design for scaled CMOS technologies is the ability to obtain the required DC gain. Devices with shorter channel lengths are expected to have lower output resistance (r_o) and intrinsic device gain ($g_m r_o$), but the pocket (halo) implant [6] also causes a drain-induced threshold shift (DITS) that does not disappear at longer channel lengths [9] [10]. The result is a lower than expected device output resistance even at longer device lengths where DIBL effects are expected to be negligible. Traditionally, the method of obtaining large DC gains with devices that have low output resistance has been to cascode the transistors connected to high impedance nodes in the op-amp. However, cascoding exacerbates the reduced supply voltage problem. The alternative to cascoding is to cascade multiple gain stages, but stabilizing a cascade of amplifiers in feedback is difficult. Techniques such as nested Miller compensation [11] can be used to stabilize the op-amp in feedback, but an increase in power consumption is required to maintain the same speed of operation².

To address the issues of low intrinsic device gain and lower supply voltages, a new comparator-based switched-capacitor circuit (CBSC) technique is proposed that eliminates the need for high gain op-amps in the signal path. The proposed tech-

²For a good overview on sophisticated op-amp compensation techniques see [12].

nique is compatible with most known switched-capacitor architectures, but it is more amenable to design in scaled technologies.

1.2 Thesis Organization

Chapter 2 provides an introduction to the comparator-based switched-capacitor technique. This chapter covers the basic principle of operation and a brief discussion of accuracy limitations.

Chapter 3 covers the noise analysis techniques for comparator-based circuits that are used throughout the thesis. The different noise analysis techniques are demonstrated with a series of examples.

Chapter 4 discusses the design of efficient low-noise threshold detection comparators. Design equations are presented for a low noise preamplifier for threshold detection comparators. Basic threshold comparator design is reviewed, and the unique requirements for threshold comparators in CBSC systems are discussed.

Chapter 5 presents the details and results of the CBSC prototype 1.5 b/stage pipeline ADC.

Chapter 6 covers the detailed noise analysis of the CBSC pipeline ADC. The general noise power spectral density (PSD) results for both thermal and flicker noise sources are derived, and the mean-squared noise results for thermal noise sources are also presented.

Chapter 7 presents a comparison between the theoretical noise PSD derived in Chapter 6 and measured results from the prototype.

Finally, Chapter 8 summarizes the contributions of this thesis and suggests areas for future work.

Chapter 2

Comparator-Based Switched-Capacitor Circuits

2.1 Overview

The basic operation of comparator-based switched-capacitor circuits (CBSC) is introduced. After establishing the basics, a more practical comparator-based charge transfer phase is described. Accuracy limitations are introduced, where a further discussion of noise is deferred to later chapters. Finally, a summary of the known limitations and potential advantages of the CBSC technique is given.

2.2 CBSC Basic Principle of Operation

Although the CBSC technique is applicable to a wide range of switched-capacitor circuits, a simple switched-capacitor gain stage is used to illustrate the basic principle of operation. A traditional op-amp based switched-capacitor gain stage is compared to the proposed comparator-based implementation. Both circuits use the same input sampling circuit. The difference is in the method of achieving the virtual ground condition during the charge transfer or amplification phase.

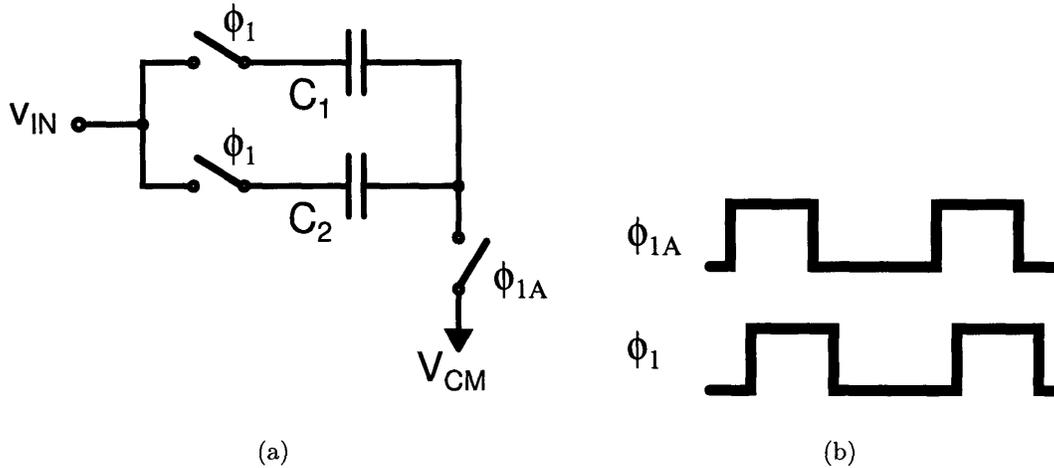


Figure 2-1: Bottom plate open-loop sampling (a) Sampling circuit. (b) Sampling clocks. ϕ_{1A} defines sampling instant to minimize input dependent charge injection.

2.2.1 Sampling Circuit

Assume that both circuits use the same open-loop input sampling circuit shown in Figure 2-1. During the sampling phase ϕ_1 , the input voltage is sampled onto both C_1 and C_2 . The opening the bottom plate switch to V_{CM} at the falling edge of ϕ_{1A} defines the sampling instant. The clock ϕ_{1A} is an advanced version of the sampling phase clock ϕ_1 . This sampling method minimizes signal dependent charge injection from the sampling switch [13] [14].

2.2.2 Op-amp Based Charge Transfer Phase

In the traditional op-amp based charge transfer phase, the capacitors C_1 and C_2 are reconfigured as shown in Figure 2-2. The op-amp then forces a virtual ground condition at node v_X . This forces all the charge sampled onto C_2 to transfer to C_1 . During the charge transfer, both the output voltage v_O and the virtual ground node v_X exponentially settle to their steady-state values. In Figure 2-2, the exponential settling neglects slew rate limitations and the effects of higher order poles in the op-amp that would increase the required settling time. After a number of time-constants

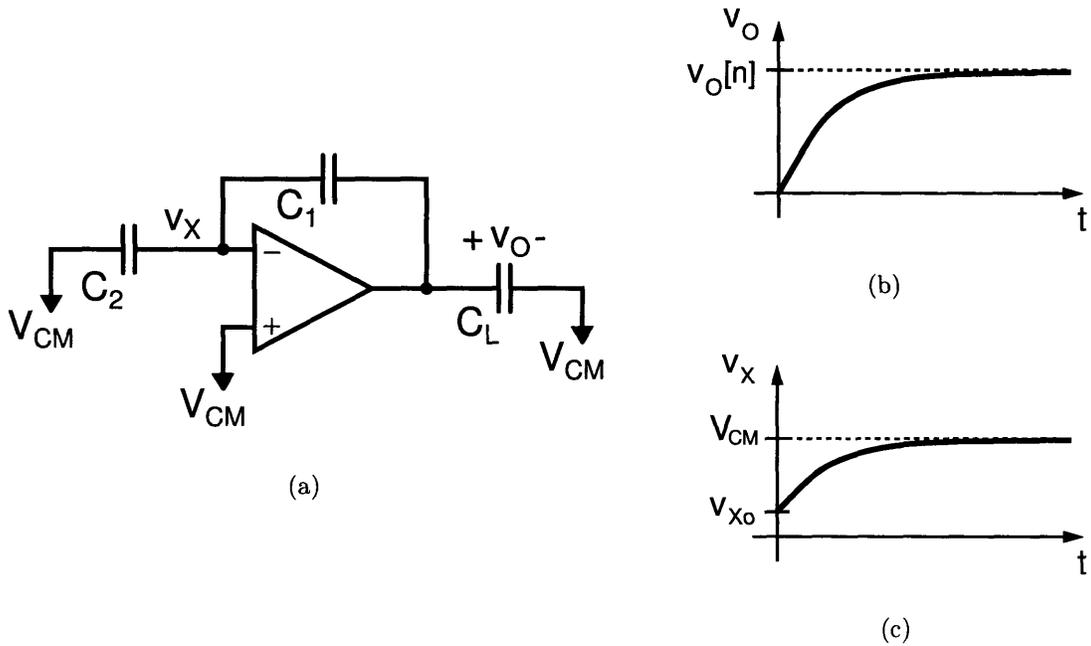


Figure 2-2: Op-amp based switched-capacitor gain stage charge transfer phase. (a) Switched-capacitor circuit (b) The output voltage exponentially settles to the final value. (c) The summing node voltage exponentially settles to the virtual ground condition.

have passed to achieve the desired output voltage accuracy, the output of the stage can be sampled. The relationship between the input and output samples is

$$v_O[n] = \left(\frac{C_1 + C_2}{C_1} \right) v_{IN}[n - \frac{1}{2}] \quad (2.1)$$

and the capacitor ratio (C_2/C_1) determines the gain of the amplifier.

Note that during the charge transfer phase, the accuracy of the output voltage directly depends on the accuracy of the virtual ground condition. In conventional designs, the op-amp forces the virtual ground in a continuous-time manner, but in switched-capacitor circuits, an accurate virtual ground condition is only required at the sampling instant. Therefore, it should be possible to detect the virtual ground condition at a single time point using a threshold-detection comparator rather than force it with an op-amp. Also, detecting the virtual ground condition should be more

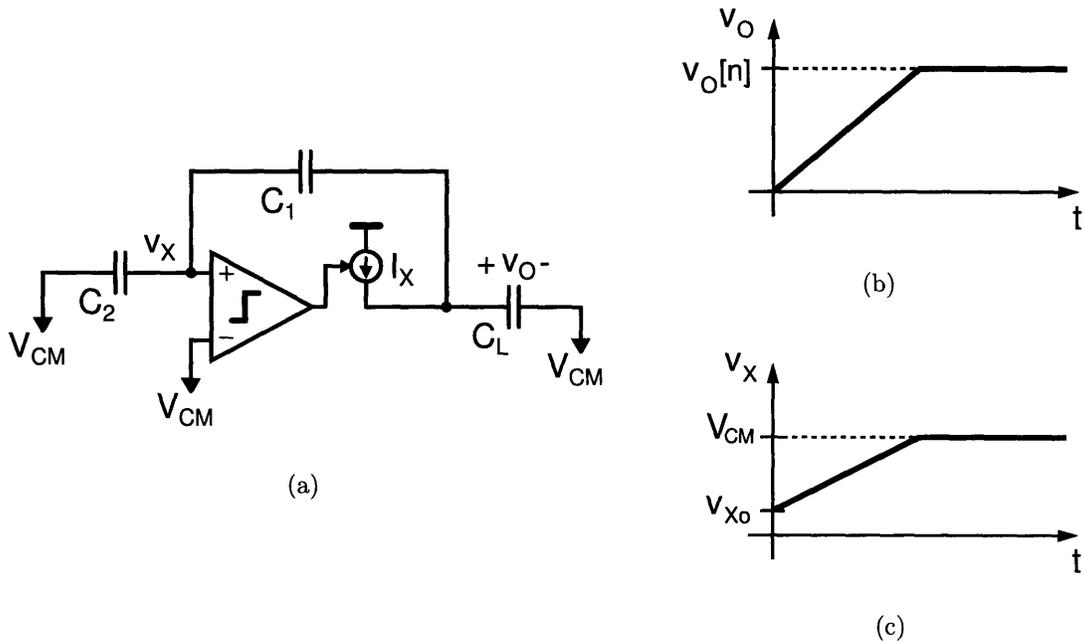


Figure 2-3: Comparator-based switched-capacitor gain stage charge transfer phase. (a) Switched-capacitor circuit with an idealized zero delay comparator. (b) The output voltage ramps to the final value. (c) The summing node voltage ramps to the virtual ground condition.

energy efficient than forcing it.

2.2.3 Comparator-Based Charge Transfer Phase

Detecting the virtual ground condition is the approach taken in the comparator-based charge transfer phase. The procedure for implementing a comparator based charge transfer phase is now presented.

Again, assuming the input was sampled just like in the op-amp case, and the capacitors C_1 and C_2 are reconfigured in a similar manner; the result is the circuit in Figure 2-3. The op-amp has been replaced with a virtual-ground threshold-detection comparator and a current source I_x . Assuming for the moment that something has been done to ensure that v_X always starts below the virtual ground condition ($v_{Xo} < V_{CM}$), the current source I_x turns on at the beginning of the charge transfer

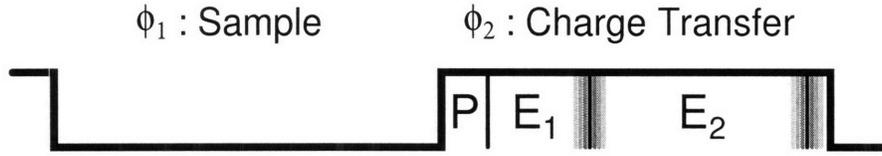


Figure 2-4: CBSC charge transfer phase timing.

phase and charges up the capacitor network consisting of C_1 , C_2 and C_L . The ramp voltage waveforms shown in Figure 2-3 result. The voltage v_X continues to increase until it equals V_{CM} . At this point, the comparator detects the virtual ground condition and turns off the current source I_x . Therefore, the comparator defines the sampling instant. The state of the circuit is identical to that of the op-amp based implementation, and the relationship between the input and output samples is identical to (2.1).

2.3 Practical CBSC Gain Stage Charge Transfer

Now that the basic principle of operation has been established, a more practical version like that used in the prototype system is described. The first issue that must be addressed is to ensure the initial condition in the charge transfer phase. The second issue is maximizing the accuracy of the charge transfer phase. To minimize the noise in the comparator decision, it is desirable to maximize the time available to the comparator to do noise averaging when making its decision. The noise averaging property of the comparator is discussed in detail in Chapters 3 and 4. It is also desirable to minimize the final overshoot to minimize the sensitivity to nonlinearity in the ramp rate.

To address these requirements, the charge transfer phase for the prototype was divided into three sub-phases: preset phase (P), coarse charge transfer phase (E_1), and fine charge transfer phase (E_2). The time available for each sub-phase is as illustrated in Figure 2-4. The time spent on coarse and fine charge transfer are signal dependent because of the self-timed nature of the comparator-based circuit.

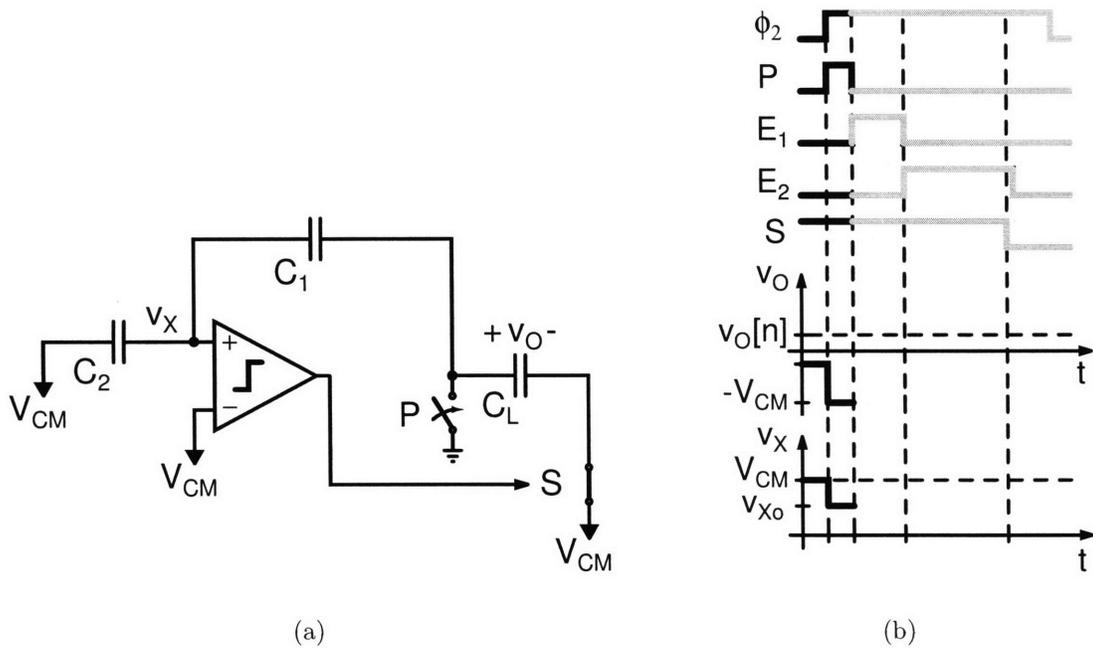


Figure 2-5: Preset phase (P). (a) Switch P closes. (b) v_O grounded and v_X set below V_{CM}

2.3.1 Preset Phase

To ensure the voltage v_X starts out below the virtual ground condition V_{CM} , a brief preset phase is used. Assuming the input has just been sampled onto C_1 and C_2 , the summing node voltage v_X starts at V_{CM} . If at the same time C_2 is connected to V_{CM} , the output node is also switched to the lowest voltage in the system (ground), then a negative step results at the summing node v_X through the capacitive divider C_1 and C_2 . This negative step can be used to ensure the preset voltage for v_X is less than the common-mode voltage over a range of input voltages.

To derive the valid input range for the given preset method, the preset value of the summing node voltage v_{Xo} is found from its initial voltage V_{CM} and the superposition of the voltage steps at v_X from closing the switches at C_2 and C_1 to V_{CM} and ground

respectively¹

$$v_{X_o} = V_{CM} + \left(\frac{C_2}{C_1 + C_2} \right) (V_{CM} - v_{IN}) - \left(\frac{C_1}{C_1 + C_2} \right) v_{IN} \quad (2.2)$$

Therefore, the preset value for the summing node is

$$v_{X_o} = \left(2 - \frac{C_1}{C_1 + C_2} \right) V_{CM} - v_{IN}. \quad (2.3)$$

Using the constraints that the summing node voltage v_{X_o} must be greater than zero and less than V_{CM} results in the following valid input range for a gain of two stage

$$\frac{1}{2}V_{CM} \leq v_{IN} \leq \frac{3}{2}V_{CM}. \quad (2.4)$$

Assuming that V_{CM} is halfway between the supply rails, this is exactly the same input range required to keep the output within the supply rails.

During the preset phase, the output sampling switch S is also closed after the preset switch to ground has been closed. Therefore, the preset state also resets the load capacitance before charge transfer begins.

2.3.2 Coarse Charge Transfer Phase

To obtain a quick, rough estimate of the output and virtual ground condition, a relatively fast ramp-rate is used in the coarse charge transfer phase. The coarse phase ramp is generated with current source I_1 in Figure 2-6. Because of finite delay of the comparator, the output of the gain stage overshoots the correct value

$$V_{ov1} = \frac{I_1}{C_E} t_{d1} \quad (2.5)$$

¹The same result can be derived using charge conservation at the summing node before and after the switches are closed.

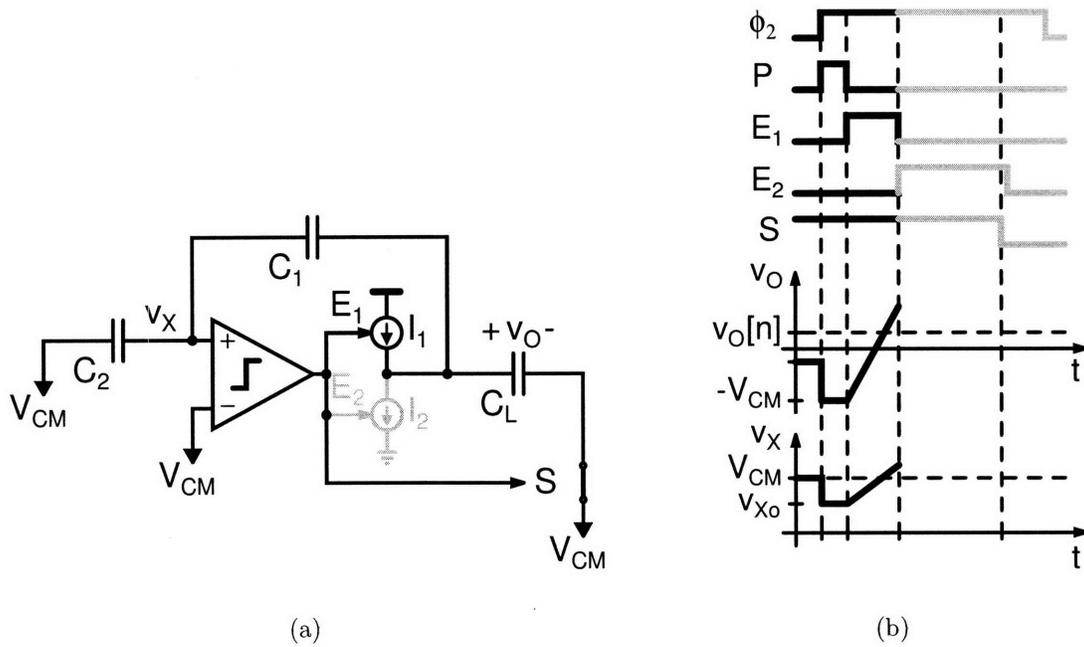


Figure 2-6: Coarse charge transfer phase (E_1). (a) Current source I_1 charges output. (b) v_O and v_X ramp and overshoot their ideal values.

where I_1 is the coarse charging current, t_{d1} is the comparator delay for the coarse charge transfer phase

$$C_E = C_L + C_x \quad (2.6)$$

and $C_x = C_1 C_2 / (C_1 + C_2)$ is the series combination of C_1 and C_2 . The overshoot of the virtual ground condition is

$$V_{ovx1} = f_o V_{ov1} \quad (2.7)$$

where

$$f_o = \frac{C_1}{C_1 + C_2} \quad (2.8)$$

is the feedback factor.

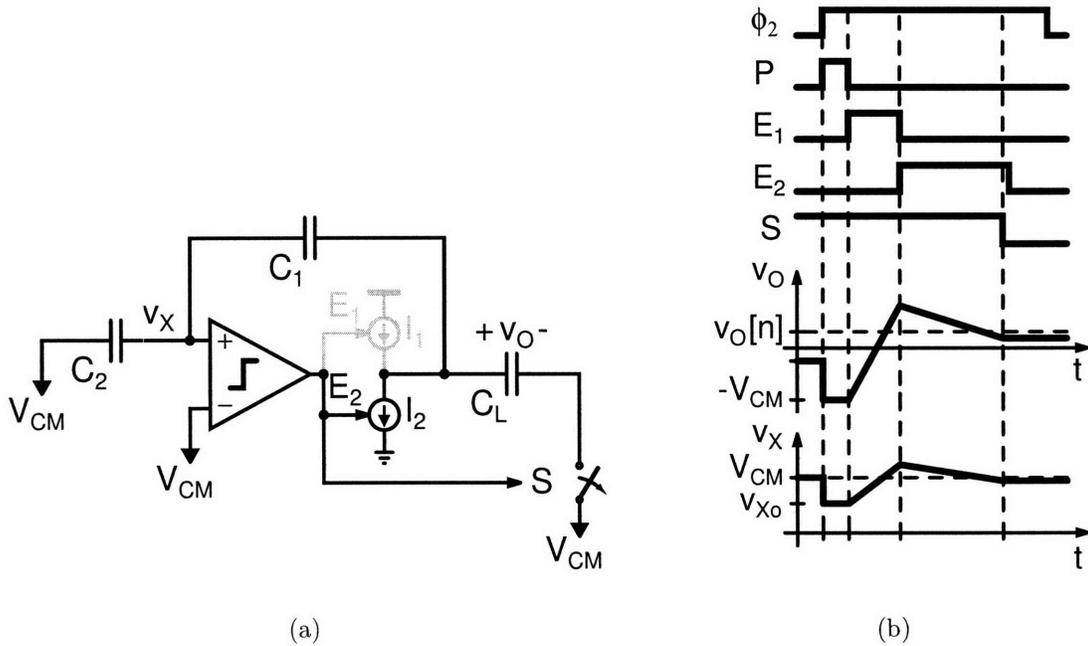


Figure 2-7: Fine charge transfer phase (E_2). (a) Current source I_2 discharges output. (b) v_O and v_X ramp to their final values.

2.3.3 Fine Charge Transfer Phase

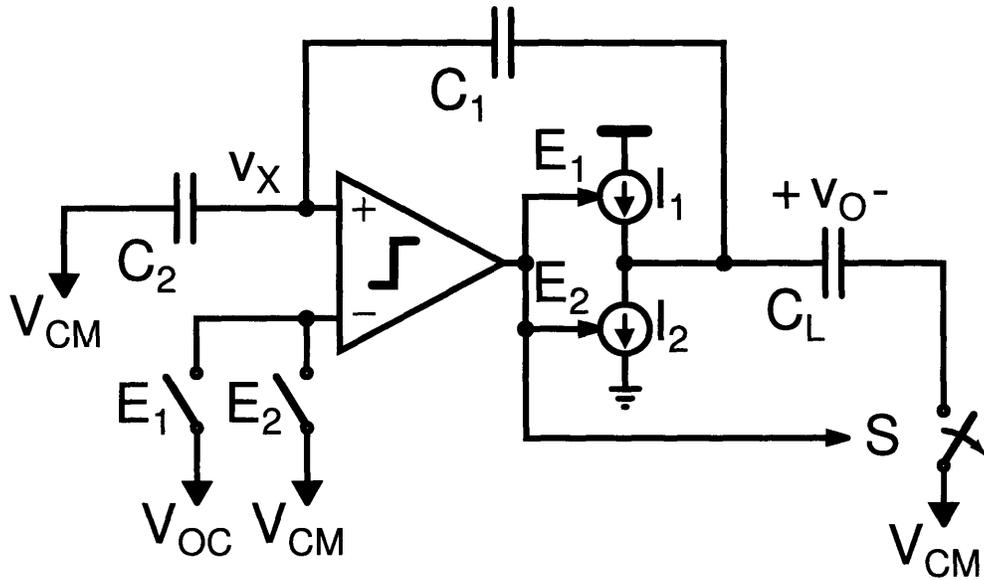
To obtain a more accurate virtual ground condition, a fine charge transfer phase with a significantly more gradual ramp rate is used. The fine charge transfer ramp is generated with current source I_2 in Figure 2-7. The use of the fine charge transfer phase also erases any noise and nonlinearity from the first comparator decision and overshoot. It is the final overshoot that determines the offset and nonlinearity of the stage. If the ramp rate is perfectly constant over the full-scale output range of the stage, then the final overshoot would only be an offset, and in many systems, it could be easily be corrected. Unfortunately, the overshoot is not constant in a real system. Therefore, the second overshoot must be kept small enough to meet the linearity requirements of the stage.

2.3.4 Overshoot Correction

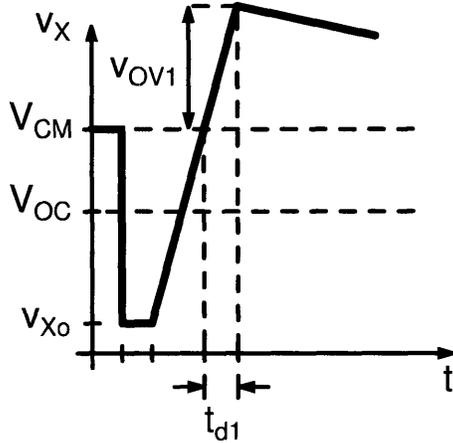
To maximize the time available for the comparator decision in fine charge transfer phase without placing excessive speed requirements on the comparator during the coarse charge transfer phase, it becomes necessary to implement some sort of overshoot correction in the coarse charge transfer phase.

Consider the coarse phase decision shown in Figure 2-8(b). If the comparator has a total delay time of t_{d1} for the coarse charge transfer phase, and the reference voltage on the comparator is the common-mode voltage V_{CM} , then the overshoot v_{OV1} of the true virtual condition is relatively large. The fine phase charge current must discharge the summing node voltage back to V_{CM} before the comparator can make its second decision in the fine charge transfer phase. Therefore, the overshoot of V_{CM} limits how much the ramp rate can be reduced for the fine charge transfer phase while maintaining the same speed of operation. However, if the coarse phase ramp rate is constant, then the overshoot v_{OV1} is the same every time, and it is possible to use a comparator reference voltage V_{OC} that is slightly below V_{CM} to anticipate the threshold crossing as shown in Figure 2-8(c). The circuit implementation for the overshoot correction used in the prototype is shown in Figure 2-8(a), where two different references are switched to the comparator for the coarse and fine charge transfer phases.

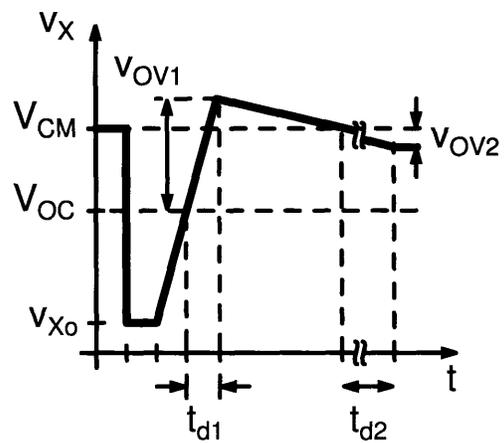
For a perfectly constant ramp rate, the coarse phase overshoot could be completely canceled, but ramp rate variation and noise in the coarse phase comparator decision place a limit on the amount of overshoot correction. The supply voltages also place a constraint on the possible amount of overshoot correction.



(a)



(b)



(c)

Figure 2-8: Overshoot cancellation. (a) CBSC stage with overshoot cancellation. (b) v_X node voltage during the charge transfer phase without overshoot correction. The large overshoot during the coarse phase prevents the charge transfer operation from finishing in allowed time. (c) CBSC stage with overshoot cancellation.

2.4 Noise Analysis

If the comparator is thought of as a finite time integrator,² then the input referred noise voltage of the comparator is inversely proportional to the square-root of comparator integration time

$$v_{nRMS} \propto \frac{1}{\sqrt{t_i}}. \quad (2.9)$$

This is because the output noise voltage of the integrator preamplifier grows with the square-root of integration time (random-walk)

$$v_{oRMS} \propto \sqrt{t_i}, \quad (2.10)$$

but the signal grows proportional to the integration time

$$v_o(t) \propto t_i. \quad (2.11)$$

Noise analysis techniques are covered in Chapter 3. Comparator noise analysis is covered in more detail in Chapter 4 in the context of threshold detection comparator design. Chapter 6 presents the detailed noise analysis of a CBSC gain stage.

2.5 Ramp Linearity

Ramp linearity has an effect similar to finite gain in op-amp based systems. Therefore, careful design of constant ramp generators is key to designing CBSC systems with a high degree of linearity.

²It is shown in Chapter 4 that an integrating preamplifier for the comparator results in the lowest power consumption for a given speed and noise requirement.

In op-amp based designs, the output of a gain stage is

$$v_O = \frac{1}{f_o} \left(\frac{1}{1 + \frac{1}{f_o A_o}} \right) (v_{IN} - V_{os}) \quad (2.12)$$

$$\approx \frac{1}{f_o} \left(1 - \frac{1}{f_o A_o} \right) (v_{IN} - V_{os}) \quad (2.13)$$

where $f_o = C_1/(C_1 + C_2)$ is the feedback factor, V_{os} is the input referred offset for the op-amp, and A_o is the op-amp DC gain.

For the CBSC case, assuming the fine charge transfer phase current source I_2 has a constant finite output resistance R_o over the full-scale output range of the stage, I_2 can be expressed as

$$I_2 = I_{2o} + \frac{1}{R_o} v_O \quad (2.14)$$

$$= I_{2o} \left(1 + \frac{v_O}{I_{2o} R_o} \right). \quad (2.15)$$

The output ramp rate for the fine charge transfer phase is

$$\frac{dv_O}{dt} = \frac{I_2}{C_E} \quad (2.16)$$

$$= \frac{I_{2o}}{C_E} \left(1 + \frac{v_O}{I_{2o} R_o} \right) \quad (2.17)$$

where C_E as defined above (2.6) is the net capacitance the current source is charging and is assumed to be constant here. For a comparator delay of t_d seconds, the final output value is

$$v_O \approx \frac{1}{f_o} v_{IN} - \left. \frac{dv_O}{dt} \right|_{v_O} t_d \quad (2.18)$$

$$= \frac{1}{f_o} \left(1 - \frac{t_d}{C_E R_o} \right) (v_{IN} - V_{os}) \quad (2.19)$$

where

$$V_{os} = f_o \frac{I_{2o}}{C_E} t_d \quad (2.20)$$

is the part of the overshoot that is signal independent and looks like an input referred offset voltage. This offset is in addition to the offset of the comparator. Completing the analogy to the op-amp case (2.13), the effective open-loop gain is

$$A_o \leftrightarrow \frac{C_E R_o}{f_o t_d}. \quad (2.21)$$

The finite output resistance of the fine charge transfer phase current source behaves similar to finite gain in the op-amp case. Note that the gain can be increased in a couple of ways. Shorter comparator delay results in a higher effective gain, but it will trade off with noise performance. Increasing the current source output resistance directly increases the effective gain, and increasing the signal capacitances also helps. Finally, note that unlike the op-amp case, the finite gain term

$$A_o f_o \leftrightarrow \frac{C_E R_o}{t_d} \quad (2.22)$$

does not depend of the feedback factor used.

2.6 Summary

The basic principle of a comparator-based charge transfer phase has been explained. Its operation parallels that of an op-amp based system, but it takes advantage of the fact that an accurate virtual ground is only needed at the sampling instant. A brief overview of accuracy limitations was given.

2.6.1 Limitations

Because CBSC systems lack an output amplifier, they can only drive switched-capacitor loads. This is expected since it was one of the drawbacks stated above

for op-amp systems that continuously force the virtual ground and output voltages. Only being able to drive switched-capacitor loads does not severely limit the applicability of the CBSC approach. If a continuous load needs to be driven, then an output buffer could be used.

A related limitation is that CBSC designs cannot drive both sides of the sampling capacitor simultaneously. This makes the technique incompatible with conventional closed-loop offset cancellation where the input sampling capacitors sample with reference to a driven virtual ground node. The comparator is still free during the sampling phase, and other techniques should be possible to perform offset cancellation if necessary.

As discussed above, finite output resistance of the ramp current sources have an effect similar to finite op-amp gain. However, designing a constant current source in scaled technologies should be easier than designing a high-gain op-amp because the current source is not directly in the signal path, and therefore it has fewer design constraints.

To be sure, the above list of limitations is incomplete. Because this is a new design method, further investigation is required to determine a more complete list of limitations.

2.6.2 Advantages

Comparator-based systems have the potential for significant power reduction compared to op-amp based designs because of the differences in the noise-bandwidth and speed requirements of op-amp and comparator-based designs. See Chapter 4 and [15] for details.

In addition, comparator-based systems are more amenable to design in scaled technologies than op-amp based systems because of differences in the requirements for the comparator and current sources compared to the op-amp. The big difference is that feedback and stability concerns have been removed for comparator-based systems, and the high output resistance current sources are not directly in the signal

path.

Finally, the CBSC design method should be applicable to a wide range of switched-capacitor circuits and compatible with most known architectures. In sampled data systems, circuit designs that traditionally use feedback to force a virtual ground should be compatible with the proposed virtual ground detection scheme. Switched-capacitor filter, integrators, DACs and ADCs should all be compatible with the CBSC technique. Because the CBSC approach utilizes architectures similar to traditional op-amp based designs, with some notable exceptions made above, the wealth of the design techniques and architectures from op-amp designs should transfer to CBSC designs.

Chapter 3

Noise Analysis

Because of the transient nature of comparator circuits, the usual steady-state analysis that is performed on amplifiers is not appropriate. To determine the transient response of a circuit, differential equations or Laplace transform methods must be employed. These methods are well documented and widely used in electrical engineering. Methods for handling transient responses of noise inputs, which are random processes, exist [16] [17], but are not widely known or applied in the electrical engineering circuit design community. Two exceptions are the areas of charge transfer devices [18] [19] [20] and relaxation oscillators [21]. The work on charge transfer devices actually addresses the more complicated case where device parameters are also allowed to vary with time. This approach is also appropriate for the dynamic circuits discussed here because of their large signal behavior. The linear analysis approach presented in this thesis is only approximate, but it is significantly less complicated than the analysis with time-varying coefficients. The differential equation analysis presented for the relaxation oscillator jitter calculation in [21] is identical in principle to that presented in this chapter. The benefit of the approach presented here is that it generalizes to arbitrary linear, time-invariant (LTI) systems. The time-domain method presented parallels the usual frequency-domain approach. Finally, a set of simple results for the special case of a white noise step input is given with both time-domain and frequency-domain interpretations.

Recently, interest in charge-based sampling circuits [22] that periodically integrate the input signal for a fixed amount of time has resulted in a series of papers applying this technique for sub-sampling [23] [20] [24] [25] [26]. The sampling model and resulting mathematics also apply to the analysis of comparator-based systems if the periodic integration is extended to periodic filtering. While the non-stationary noise analysis examines the details of noise behavior over a single period of operation, a periodic filtering analysis is presented that examines a series of sampled outputs. The sampled values form a wide-sense stationary (WSS) sequence with PSD properties that can be calculated using the traditional frequency domain aliasing model for both thermal and flicker noise sources. Flicker noise is not strictly WSS because the integral of the noise PSD is not bounded on the low frequency limit. However, a finite duration measurement of a flicker noise process is WSS and non-overlapping measurements are independent [27] [28]. This chapter concludes with a brief summary of the key results from noise aliasing theory for both white and flicker noise sources.

3.1 Noise Analysis Overview

Like all signal processing problems, noise analysis can be viewed in the time-domain and the frequency-domain. Both viewpoints tend to offer unique insights to the signal or the system. Figure 3-1 shows a generic system $H(f)$ or $h(t)$ and the input and output quantities associated with frequency-domain and time-domain noise analysis. The quantities shown in the Figure 3-1 and the relationships between them are explained in the following sections. A simple transconductance amplifier example is used to illustrate each analysis method. To keep complexity to a minimum, the series of examples only solve for the output noise voltage. The issues of gain and input referred noise are addressed later in the chapter.

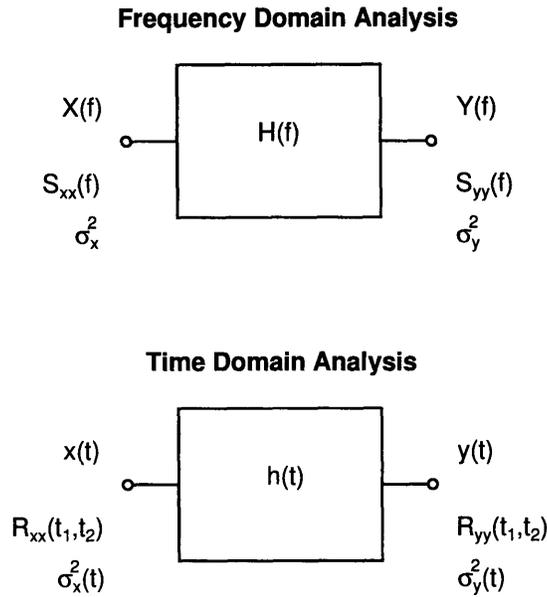


Figure 3-1: Overview of time-domain and frequency-domain analysis.

3.2 Wide-Sense-Stationary Noise Analysis

Much like sinusoidal-steady-state signal analysis, steady-state noise analysis methods assume an input $\mathbf{x}(t)$ of infinite duration, which is a Wide-Sense Stationary (WSS) random process¹. A WSS random process has a mean

$$\mu_x = E[\mathbf{x}(t)] \quad (3.1)$$

and variance

$$\sigma_x^2 = E [(\mathbf{x}(t) - \mu_x)^2] \quad (3.2)$$

that are independent of time. Therefore, the input noise waveform has an ill-defined amplitude, but it has a constant root-mean-square (RMS) value. In other words, it has a constant noise power. The RMS value of the noise is commonly measured as a time average. In circuit analysis, a noise signal is always defined to have zero mean

¹Bold variables are used to denote random processes.

($\mu_x = 0$) to separate the deterministic or average response from the noise.

3.2.1 WSS Frequency-domain Analysis

The output $\mathbf{y}(t)$ of a linear time-invariant (LTI) system with transfer function $H(f)$ to a noise input can be calculated using the Power Spectral Density (PSD) of the input signal $S_{xx}(f)$. The output PSD $S_{yy}(f)$ for the system $H(f)$ can be calculated as

$$S_{yy}(f) = |H(f)|^2 S_{xx}(f) \quad (3.3)$$

and the average noise power of the output signal is

$$\sigma_y^2 = \int_{-\infty}^{+\infty} S_{yy}(f) df. \quad (3.4)$$

Notice that a two-sided PSD has been assumed in this definition. Because the two-sided PSD $S_{yy}(f)$ is symmetric around zero frequency, a one-sided PSD is customarily used

$$S_x(f) = 2 S_{xx}(f) \quad (3.5)$$

$$S_y(f) = 2 S_{yy}(f) \quad (3.6)$$

$$S_y(f) = |H(f)|^2 S_x(f) \quad (3.7)$$

and the integral limits are taken from 0 to $+\infty$

$$\sigma_y^2 = \int_0^{+\infty} S_y(f) df. \quad (3.8)$$

As a final point, the output noise signal also has zero mean and a constant RMS value which means that the output noise is also WSS.

Example 3.1 Transconductance Amplifier: WSS Frequency-domain Analysis

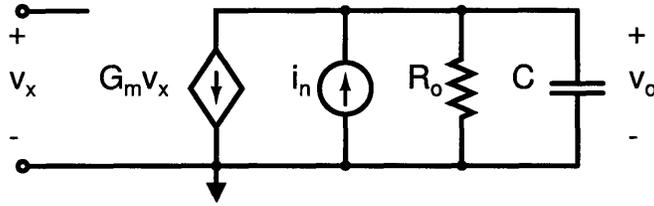


Figure 3-2: Transconductance Amplifier.

For comparison to the other analysis methods, the WSS frequency-domain noise analysis of the simple transconductance amplifier in Figure 3-2 is presented. The input noise signal i_n is the white noise current source associated with the transconductance device and has a one-sided PSD

$$S_{i_n}(f) = S_{i_n}(0) = 4kTG_n \quad (3.9)$$

where G_n is the noise conductance for the current noise source i_n . The transfer function from the noise current to the output voltage is simply the impedance that the current source drives

$$H(f) = \frac{R_o}{1 + j2\pi f\tau_o} \quad (3.10)$$

where $\tau_o = R_o C$. The output voltage PSD for the amplifier is

$$\begin{aligned} S_{v_o}(f) &= |H(f)|^2 S_{i_n}(f) \\ &= 4kTG_n \left(\frac{R_o^2}{1 + (2\pi f)^2 \tau_o^2} \right) \end{aligned} \quad (3.11)$$

The usual method to determine the integral for the output noise voltage (3.8) for a white noise input is to define an effective noise bandwidth NBW for the transfer function $H(f)$

$$\text{NBW} = \frac{1}{|H(0)|^2} \int_0^\infty |H(f)|^2 df \quad (3.12)$$

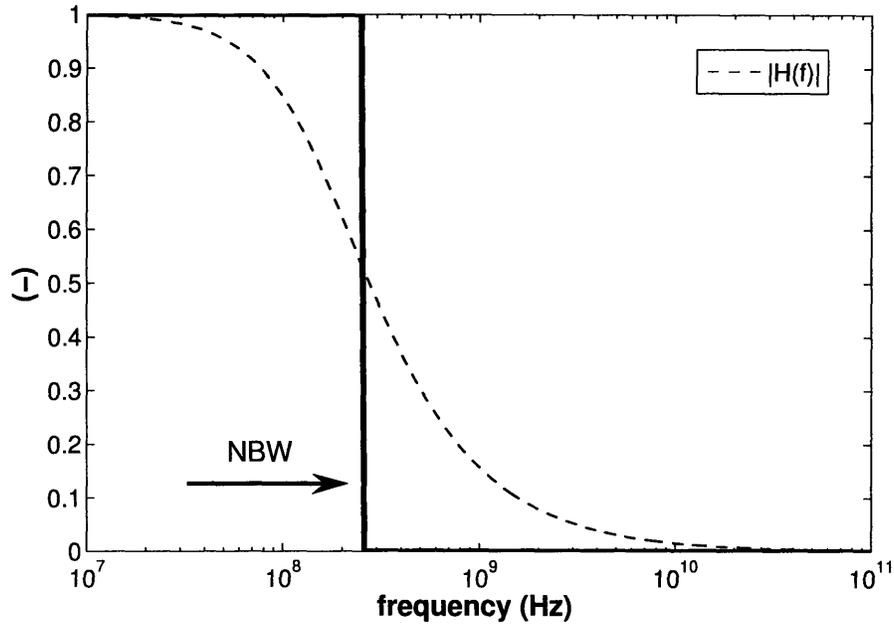


Figure 3-3: Noise Bandwidth (NBW) for a one-pole system.

which has the well known result for a single pole transfer function

$$\text{NBW} = \frac{\pi}{2} f_{3dB} = \frac{1}{4\tau_o} \quad (3.13)$$

The NBW is shown graphically in Figure 3-3, and it can be thought of as the equivalent brick-wall filter bandwidth. The output noise voltage is then

$$\begin{aligned} \overline{v_o^2} &= S_{i_n}(0) |H(0)|^2 \text{NBW} \\ &= 4kTG_n R_o^2 \frac{1}{4R_o C} \end{aligned} \quad (3.14)$$

$$\overline{v_o^2} = \left(\frac{G_n}{G_m} \right) \frac{kT}{C} (G_m R_o) \quad (3.15)$$

□

3.2.2 WSS Time-domain Analysis

The problem can also be solved in the time-domain using the autocorrelation² of the noise instead of the PSD. Autocorrelation is defined as the correlation between the value of a random process at two different time instants

$$R_{xx}(t_1, t_2) = E [\mathbf{x}(t_1)\mathbf{x}(t_2)]. \quad (3.16)$$

For a WSS random process, the autocorrelation is only a function of the time difference $\tau = |t_2 - t_1|$

$$R_{xx}(\tau) = E [\mathbf{x}(t + \tau)\mathbf{x}(t)]. \quad (3.17)$$

This property is the result of the mean and variance of $\mathbf{x}(t)$ being independent of time. The Einstein-Wiener-Khinchin Theorem [29] states that the two-sided PSD and the autocorrelation are related through the Fourier transform $\mathcal{F}\{\}$ with respect to τ

$$R_{xx}(\tau) \xleftrightarrow{\mathcal{F}} S_{xx}(f). \quad (3.18)$$

To calculate the response of an LTI system $h(t)$ to $\mathbf{x}(t)$, the multiplication in the frequency domain by the transfer function is replaced by convolution with the impulse response

$$R_{yy}(\tau) = R_{xx}(\tau) * [h(\tau) * h(-\tau)] \quad (3.19)$$

and the output noise variance is

$$\sigma_y^2 = R_{yy}(0). \quad (3.20)$$

²In general, autocovariance ($C_{xx}(t_1, t_2)$) should be used for random processes with nonzero mean, but since all noise random processes are defined to be zero mean, the autocovariance and the autocorrelation are equal.

$$C_{xx}(t_1, t_2) = R_{xx}(t_1, t_2) - \mu_x^2$$

The autocorrelation of a WSS white noise process is the inverse Fourier Transform of its PSD, which is constant over all frequencies. Therefore, the WSS white noise autocorrelation is

$$R_{xx}(\tau) = S_{xx}(0) \delta(\tau). \quad (3.21)$$

For a WSS white noise input the two convolutions simplify to a single integral

$$\sigma_y^2 = S_{xx}(0) \int_{-\infty}^{+\infty} |h(\alpha)|^2 d\alpha. \quad (3.22)$$

Because the time-domain analysis requires two convolutions in general and the frequency domain analysis only requires multiplication and one integration, the time-domain method is very rarely used.

Example 3.2 Transconductance Amplifier: WSS Time-domain Analysis

For the same transconductance amplifier in the previous example (Figure 3-2), the impulse response from the noise source to the output voltage is

$$h(t) = \frac{1}{C} e^{-t/\tau_o} u(t). \quad (3.23)$$

The autocorrelation for the current noise is

$$R_{i_n i_n}(\tau) = \frac{1}{2} S_{i_n}(0) \delta(\tau) \quad (3.24)$$

where $S_{i_n}(0)$ is the same as defined in Example 3.1. Substituting these values into (3.22), the output noise voltage variance can then be calculated as

$$\begin{aligned} \overline{v_o^2} &= 2kTG_n \int_0^{\infty} \frac{1}{C^2} e^{-2\alpha/\tau_o} d\alpha \\ \overline{v_o^2} &= \left(\frac{G_n}{G_m} \right) \frac{kT}{C} (G_m R_o) \end{aligned} \quad (3.25)$$

which is identical to the result found in the previous example (3.15) using frequency-

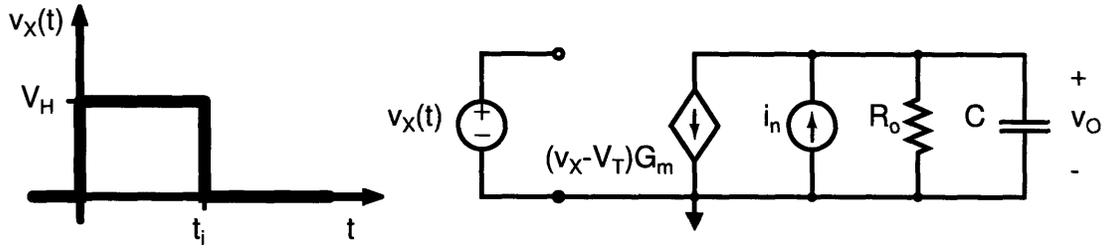


Figure 3-4: Transconductance amplifier operating as an integrator ($V_H > V_T$).

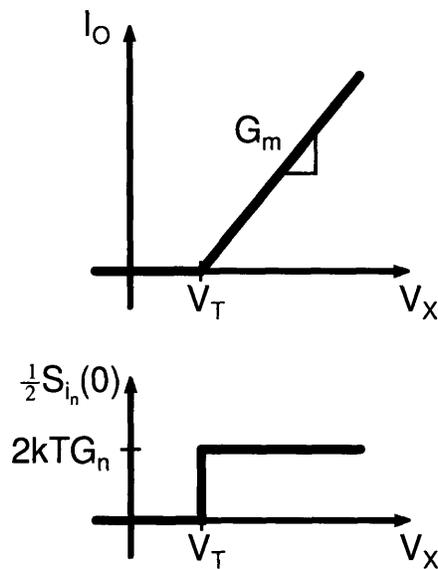


Figure 3-5: Large signal response of transconductance device with noise.

domain analysis.

□

3.3 Non-stationary Noise Analysis

As motivation for non-stationary noise analysis, consider the case of the example transconductance amplifier operating as an integrator ($R_o \rightarrow \infty$). If the transconductance device has the device characteristics shown in Figure 3-5 and is driven with the $v_s(t)$ waveform shown in Figure 3-4, the noise i_n is applied at time zero and re-

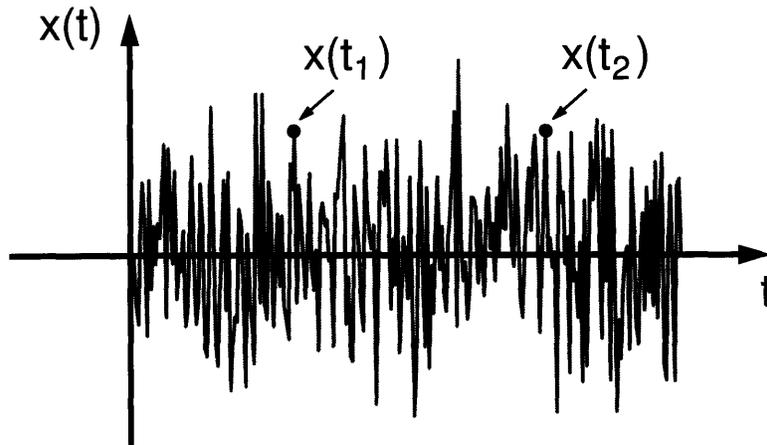


Figure 3-6: Step noise signal $\mathbf{x}(t)$. Underlying WSS noise process $\nu(t)$ applied at $t = 0$. For t_1 or t_2 less than zero, the autocorrelation for $\mathbf{x}(t)$ is zero, and for t_1 and t_2 greater than zero, the underlying WSS autocorrelation $R_{\nu\nu}(t_1, t_2)$ defines the autocorrelation of $\mathbf{x}(t)$.

moved at time t_i . Assuming that the time the noise is applied t_i is much less than the time constant at the output τ_o , the output voltage does not reach steady-state and WSS noise analysis does not apply. This section presents the techniques for analyzing non-stationary noise problems given in [16] [17] in the context of circuit analysis problems.

3.3.1 Non-stationary Time-domain Analysis

In order to determine the response of an LTI system to a step noise input, the problem is more conveniently solved in the time-domain. Assume the input is constructed from an underlying WSS process $\nu(t)$ applied at time zero

$$\mathbf{x}(t) = \nu(t)u(t) \quad (3.26)$$

where $u(t)$ is the unit step function. An example step noise waveform is given in Figure 3-6. This is a non-stationary random process; the mean and variance of $\mathbf{x}(t)$

are functions of time. The autocorrelation is then

$$R_{xx}(t_1, t_2) = E [\mathbf{x}(t_1)\mathbf{x}(t_2)] \quad (3.27)$$

$$= E [\boldsymbol{\nu}(t_1)\boldsymbol{\nu}(t_2)u(t_1)u(t_2)]$$

$$= E [\boldsymbol{\nu}(t_1)\boldsymbol{\nu}(t_2)] E [u(t_1)u(t_2)]$$

$$= R_{\nu\nu}(t_1, t_2) u(t_1)u(t_2) \quad (3.28)$$

which is the autocorrelation of the underlying random process when both time points are after the noise input was applied. In order to simplify the non-stationary autocorrelation expressions, it is always assumed that $(0 \leq t_1 \leq t_2)$. For a white noise step input

$$R_{\nu\nu}(t_1, t_2) = S_{xx}(0) \delta(t_2 - t_1) \quad (3.29)$$

where $S_{xx}(0)$ is again the two-sided white noise PSD. The transient response of an LTI system with impulse response $h(t)$ to a step noise input can be calculated by convolving the input autocorrelation function with the impulse response once for each time index to obtain the output autocorrelation³

$$\begin{aligned} R_{xy}(t_1, t_2) &= R_{xx}(t_1, t_2) * h(t_2) \\ &= \int_{-\infty}^{+\infty} R_{xx}(t_1, \tau) h(t_2 - \tau) d\tau \end{aligned} \quad (3.30)$$

$$\begin{aligned} R_{yy}(t_1, t_2) &= R_{xy}(t_1, t_2) * h(t_1) \\ &= \int_{-\infty}^{+\infty} R_{xy}(\tau, t_2) h(t_1 - \tau) d\tau. \end{aligned} \quad (3.31)$$

The procedure is similar to the WSS time-domain analysis except that the absolute value of each time index is important for a non-stationary signal, and only the time difference was important for WSS signals. Setting the two time indexes equal to each

³The intermediate result $R_{xy}(t_1, t_2)$ is known as the cross-correlation.

other gives the variance of the output as a function of time

$$\sigma_y^2(t) = R_{yy}(t_1, t_2) \Big|_{t_1=t_2=t} \quad (3.32)$$

where $t_1 = t_2$ is the same as $\tau = 0$ in the WSS case. For a white noise step input, the two convolutions again simplify to a single integral

$$\sigma_y^2(t) = S_{xx}(0) \int_{-\infty}^t |h(\tau)|^2 d\tau. \quad (3.33)$$

The output variance changes over time and has a transient and steady-state solution that depend on the system to which the noise was applied. Notice the similarities between (3.33) and (3.22). The only difference is in the upper limit of integration, infinity in (3.22) and time in (3.33). Because stable systems have impulse responses that decay to zero as time goes to infinity, the output noise variance approaches the WSS result as time approaches infinity.

Example 3.3 Transconductance Amplifier: Non-stationary Time-domain Analysis

Again, the impulse response from the noise current to the output voltage for the circuit in Figure 3-4 is

$$h(t) = \frac{1}{C} e^{-t/\tau_o} u(t). \quad (3.34)$$

The autocorrelation for the step current noise is

$$R_{\nu\nu}(t_1, t_2) = \frac{1}{2} S_{i_n}(0) \delta(t_2 - t_1) \quad (3.35)$$

$$R_{xx}(t_1, t_2) = 2kTG_n \delta(t_2 - t_1) u(t_1) u(t_2). \quad (3.36)$$

The output noise voltage variance from (3.33) is

$$\begin{aligned}\overline{v_o^2}(t_i) &= 2kTG_n \int_0^{t_i} \frac{1}{C^2} e^{-2\alpha/\tau_o} d\alpha \\ \overline{v_o^2}(t_i) &= \left(\frac{G_n}{G_m}\right) \frac{kT}{C} (G_m R_o) \left[1 - e^{-2t_i/\tau_o}\right] u(t)\end{aligned}\quad (3.37)$$

which is valid for all values of the amplifier response time t_i . Two limiting cases are of interest: $t_i \ll \tau_o$ and $t_i \gg \tau_o$.

For times much shorter than the time-constant at the output of the amplifier ($t_i \ll \tau_o$), the transconductance amplifier operates as an integrator. Using the first two terms of a Taylor approximation for the exponential

$$e^{-2t_i/\tau_o} \approx 1 - \frac{2t_i}{\tau_o} \quad \text{for } t_i \ll \tau_o/2 \quad (3.38)$$

and (3.37) is approximately,

$$\overline{v_o^2}(t_i) = \frac{2kTG_n}{C^2} t_i u(t) \quad \text{for } t_i \ll \tau_o/2. \quad (3.39)$$

In this case, the output noise voltage is a Weiner process, also commonly referred to as a random walk or Brownian motion. Think of the current noise source as either adding or removing a packet of noise charge to the capacitor at each instant of time, and the probability of doing so at each time instant is independent of what happened at all previous times. The average charge added to the capacitor is zero, but the variance grows with time. It should be noted that this result is not obtainable using traditional WSS frequency-domain analysis.

The other case of interest is what happens for times much longer than the system time constant ($t_i \gg \tau_o$), in other words the steady-state solution. For this case, the exponential term in (3.37) goes to zero, and the output noise voltage variance is

$$\overline{v_o^2}(t_i) = \left(\frac{G_n}{G_m}\right) \frac{kT}{C} (G_m R_o) \quad (3.40)$$

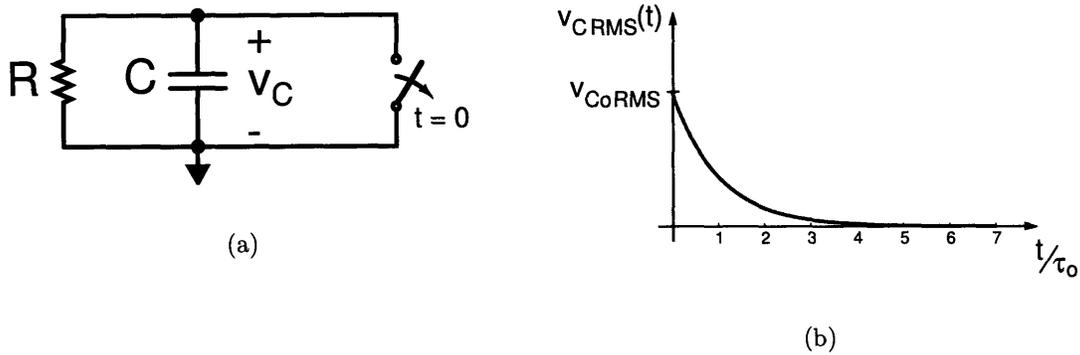


Figure 3-7: Noise initial condition example: capacitor reset noise. (a) RC circuit with capacitor reset noise ($R \gg R_{\text{switch}}$). (b) Capacitor RMS noise voltage from initial condition for $t > 0$.

but (3.40) is recognized to be the same as (3.15) and (3.25), the WSS solution.

□

3.3.2 Noise Initial Conditions

Another issue with time domain noise analysis is the handling of initial conditions on capacitors and inductors. The above method determines the noise response for zero initial conditions, also known as the zero state response. Assuming the initial condition is statistically independent of the noise input, the system can be analyzed for zero state and initial condition responses separately. Consider the parallel RC circuit in Figure 3-7 with a reset noise initial condition on the capacitor. For the initial condition response, assume a zero average initial condition with some variance (kT/C noise)

$$v_C(0) = \begin{cases} \overline{v_C}(0) = 0 & \text{Initial condition mean} & (3.41a) \\ \overline{v_C^2}(0) = \overline{v_{Co}^2} & \text{Initial condition variance} & (3.41b) \end{cases}$$

and assume that the initial condition is independent of other noise. For each trial in the ensemble, the system response to an initial condition is

$$v_C(t) = v_C(0) e^{-t/\tau_o} u(t) \quad (3.42)$$

where $\tau_o = RC$. Then, the ensemble average is

$$\overline{v_C}(t) = \mathbb{E}[v_C(0)] e^{-t/\tau_o} u(t) = 0 \quad (3.43)$$

and the ensemble variance is

$$\overline{v_C^2}(t) = \mathbb{E}[v_C^2(0) e^{-2t/\tau_o}] u(t) \quad (3.44)$$

$$= \overline{v_{C_o}^2} e^{-2t/\tau_o} u(t). \quad (3.45)$$

The standard deviation of the noise voltage decays at the same exponential rate as an average initial condition. Because the initial condition response is assumed independent of the zero state response, the variances simply add.

3.3.3 Non-stationary Noise Interpretation

To understand the meaning of a time-varying variance (or standard deviation), it is necessary to discuss more precisely the averages used to define the statistics of random processes. When dealing with non-stationary random processes, it is important to realize that ensemble averages and not time averages are being used. The random process $\mathbf{x}(\zeta, t)$ represents a collection of many $x(t)$ realizations, and each one is associated with a specific value $\zeta = \zeta_i$, where ζ is a random variable. An ensemble average is taken over all realizations ζ at a fixed time t_i . In contrast, time averages are an average over time for a fixed realization ζ_i . The two are equivalent in the case of a stationary random process because the mean and variance are independent of time. While it is convenient to think of random process statistics as time averages

for the WSS case, the results of a non-stationary analysis require the interpretation of the statistics as ensemble averages. For example, consider a noisy current source charging a capacitor, the capacitor voltage is shown in Figure 3-8. Because the system is linear and superposition applies, the composite waveform can be separated into the average ramp that the DC current causes and a noise voltage that the noise current integrating on the capacitor causes. At any point in time, the possible values of the noise waveform are given by a statistical distribution. A time varying noise variance implies that the standard deviation of the voltage distribution is changing with time. Therefore, the noise voltages and currents calculated represent the standard deviation of the signal taken over many experiments.

3.3.4 Non-stationary Frequency-domain Analysis

Because the definition of the PSD assumes that the variance of the noise process is independent of time, the PSD of a non-stationary process is not very meaningful. However, a slight reformulation of the problem allows for a frequency domain interpretation to the non-stationary noise problem for a white noise input. First, rewriting (3.33) as

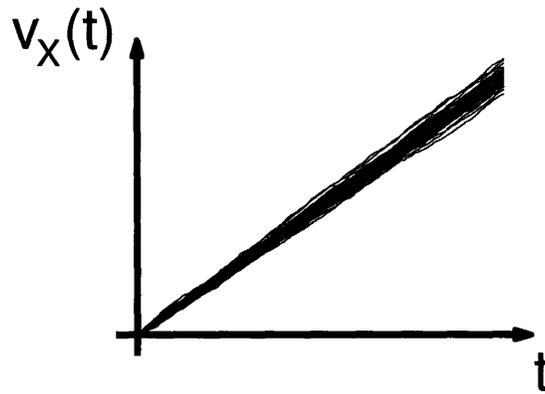
$$\sigma_y^2(t_i) = S_{xx}(0) \int_{-\infty}^{+\infty} |h_w(\alpha)|^2 d\alpha \quad (3.46)$$

where

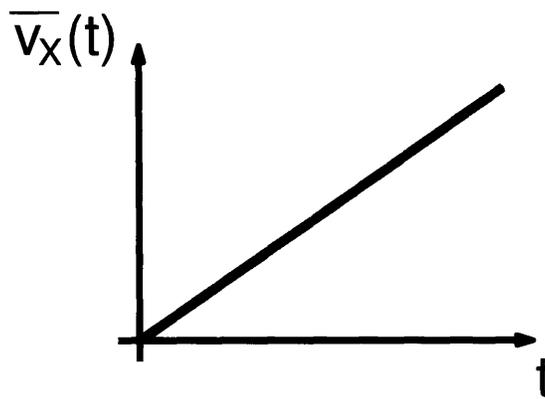
$$h_w(t) = h(t)w(t) \quad (3.47)$$

and $w(t)$ is a rectangular window from 0 to t_i . An example of a windowed impulse response is shown in Figure 3-9. Next, Parseval's Theorem can be used to rewrite (3.46) in the frequency domain

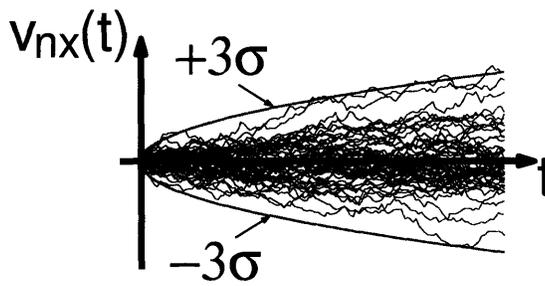
$$\begin{aligned} \sigma_y^2(t_i) &= S_{xx}(0) \int_{-\infty}^{+\infty} |H_w(f)|^2 df \\ &= S_x(0) \int_0^{\infty} |H_w(f)|^2 df \end{aligned} \quad (3.48)$$



(a)



(b)



(c)

Figure 3-8: In transient noise analysis, it is ensemble averages and not time averages that are most important. (a) Ramp voltage plus random walk noise. (b) Average ramp voltage. (c) Random walk noise voltage showing 3σ bounds.

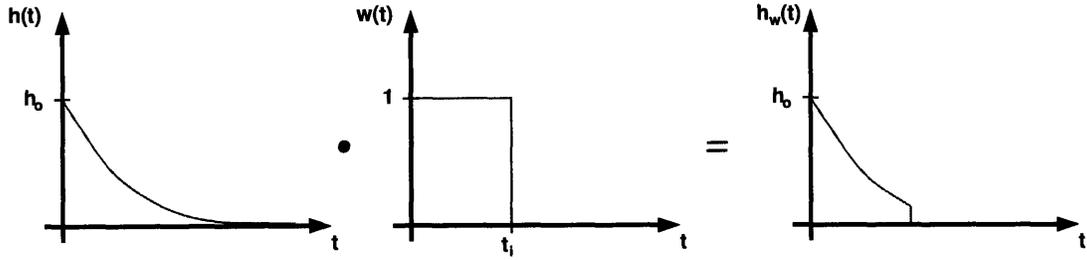


Figure 3-9: Windowed impulse response.

where again $S_x(0) = 2S_{xx}(0)$. Because multiplication in the time-domain is convolution in the frequency-domain, the time-dependent transfer function $H_w(f)$ is calculated as

$$W(f) = t_i \left(\frac{\sin(\pi f t_i)}{\pi f t_i} \right) e^{-j2\pi f t_i/2} = t_i \operatorname{sinc}(f t_i) e^{-j2\pi f t_i/2} \quad (3.49)$$

$$H_w(f) = H(f) * W(f) = \mathcal{F}\{h_w(t)\}. \quad (3.50)$$

Upon examination of (3.48) and review of the WSS frequency-domain analysis, it is possible to define a generalized effective noise bandwidth that is a function of time

$$\text{NBW}(t_i) = \frac{1}{|H_w(0)|^2} \int_0^\infty |H_w(f)|^2 df \quad (3.51)$$

$$= \frac{1}{\left| \int_0^{t_i} h(t) dt \right|^2} \int_0^{t_i} |h(t)|^2 dt \quad (3.52)$$

Figure 3-10 shows what happens to $H_w(f)$ as t_i increases for a one-pole system. For small t_i , NBW is larger, but the amplitude is lower. Because the input PSD is being amplified by a gain proportional to t_i^2 , and the NBW is inversely proportional to t_i , the output noise voltage variance is proportional to t_i . As t_i gets to be much larger than τ_o of the system, the transfer function approaches $|H(f)|$. Therefore, the NBW also approaches the steady-state NBW for large t_i .

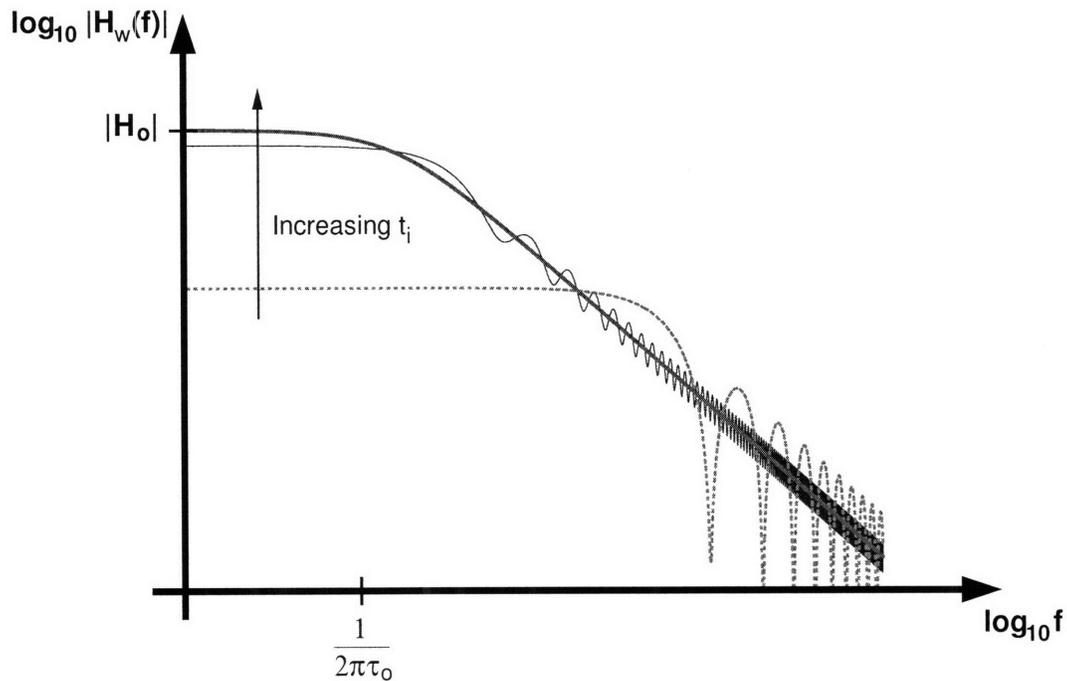


Figure 3-10: Frequency Domain: Transfer function for different window widths (t_i)

Example 3.4 Ideal Integrator: Frequency-domain Analysis

Consider the ideal integrator from the previous example that integrates the input white noise current i_n onto the output capacitor C . The impulse response is a step function

$$h(t) = \frac{1}{C}u(t). \quad (3.53)$$

To determine the windowed response transfer function, it is easier to perform the multiplication in the time-domain first and then take the Fourier transform

$$H_w(f) = \frac{t_i}{C} \text{sinc}(ft_i) e^{-j2\pi ft_i/2}. \quad (3.54)$$

Recalling the definition of NBW (3.12), it is possible to define the NBW for the

transfer function $H_w(f)$ where

$$|H_w(0)| = \frac{t_i}{C} \quad (3.55)$$

$$|H_w(f)| = \frac{t_i}{C} \left| \frac{\sin(\pi f t_i)}{\pi f t_i} \right|. \quad (3.56)$$

Substituting into (3.51)

$$\begin{aligned} \text{NBW}(t_i) &= \int_0^\infty \frac{\sin^2(\pi f t_i)}{(\pi f t_i)^2} df \\ &= \frac{1}{(\pi t_i)^2} \int_0^\infty \frac{\sin^2(\pi f t_i)}{f^2} df \\ \text{NBW}(t_i) &= \frac{1}{2t_i}. \end{aligned} \quad (3.57)$$

Using the frequency-domain method to determine the output noise voltage (3.14)

$$\overline{v_o^2}(t_i) = S_{i_n}(0) |H_w(0)|^2 \text{NBW}(t_i) \quad (3.58)$$

$$= 4kTG_n \left(\frac{t_i^2}{C^2} \right) \left(\frac{1}{2t_i} \right) \quad (3.59)$$

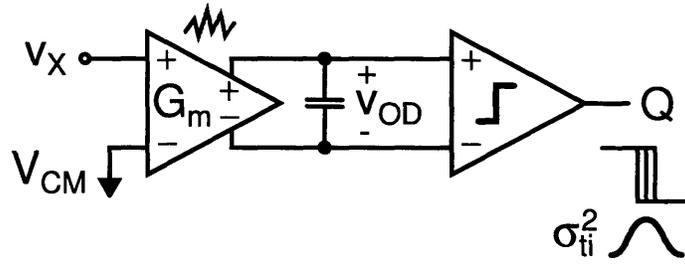
$$\overline{v_o^2}(t_i) = \frac{2kTG_n}{C^2} t_i \quad (3.60)$$

which is the same result obtained for the integrator using the non-stationary time-domain method (3.39).

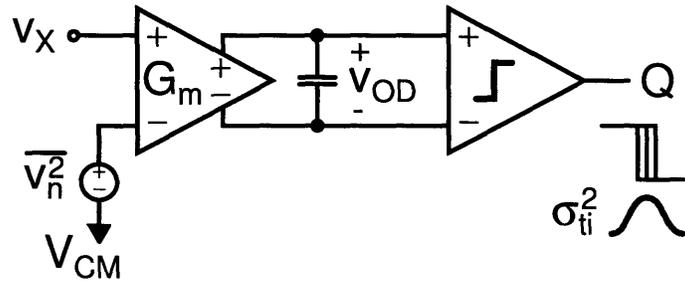
□

3.4 Input Referred Noise

All the examples in the previous sections calculated the output noise voltage for transconductance amplifier, but the input referred noise is more useful for evaluating amplifier performance. The reason is that input referred noise allows a direct comparison of the input signal to the noise the amplifier adds. If only the noise at the



(a)



(b)

Figure 3-11: Input referred noise comparator model (a) Noisy comparator results in timing jitter σ_{tj} . (b) Noiseless comparator with input referred noise $\overline{v_n^2}$ resulting in the same timing jitter.

output was examined, it would appear that a better amplifier can be made by lowering the transconductance and hence the output noise, but lowering the transconductance lowers the signal gain faster than it lowers the amplifier output noise. Therefore, it turns out to be better to increase the transconductance because the signal gain increases faster than the amplifier output noise increases. In this section, the noise gain for a comparator is defined and then used to find the input referred noise of the comparator.

3.4.1 Noise Gain

The output noise voltage of the amplifier results in jitter of the output threshold crossing through the rate of change of the amplifier output voltage as shown in Fig-

ure 3-11(a). To refer the output voltage noise to the input of the amplifier, it is desired to have an input noise voltage that results in the same comparator jitter when the input voltage ramp crosses the input threshold voltage as shown in Figure 3-11(b). Determining the noise gain requires a discussion of noise voltage to timing jitter conversion and timing jitter to noise voltage conversion. The result is that the appropriate noise gain is defined as a ratio of the output to input time derivatives at the output and input threshold crossings respectively.

Noise Voltage to Timing Jitter Conversion

The conversion of noise voltages to timing jitter happens when a noisy signal is sensed by a threshold detection device [30]. To see how this occurs, consider Figure 3-12. The signal crosses the threshold V_M at some average rate $\overline{dv_X/dt}$ and has a noise voltage distribution at the average crossing time t_i as shown on the right. Assuming the noise voltage variations are small over the range of possible crossing times, the standard deviation of the noise voltage projects back to the threshold with the average slope,

$$\sigma_{t_i}^2 = v_{xn}^2 \left| \frac{dv_X}{dt} \right|^{-2} \quad (3.61)$$

defining the standard deviation of a distribution of times the threshold is crossed. The variation in time is the jitter in the threshold crossing.

In some sense, the above description is an oversimplification of what actually occurs. If the noise was a high frequency signal superimposed on the average signal, the noise would consistently cause early threshold crossings. However, in the transconductance amplifier, the output noise voltage is the integration of the white noise current which is random walk noise. Amplitude variations in random walk noise are much slower than for white noise. For example, consider the signal plus noise waveform shown in Figure 3-8(a). Superimposing a threshold voltage on this waveform shows that the noise does result in a distribution of times about the average crossing time as described in the model above.

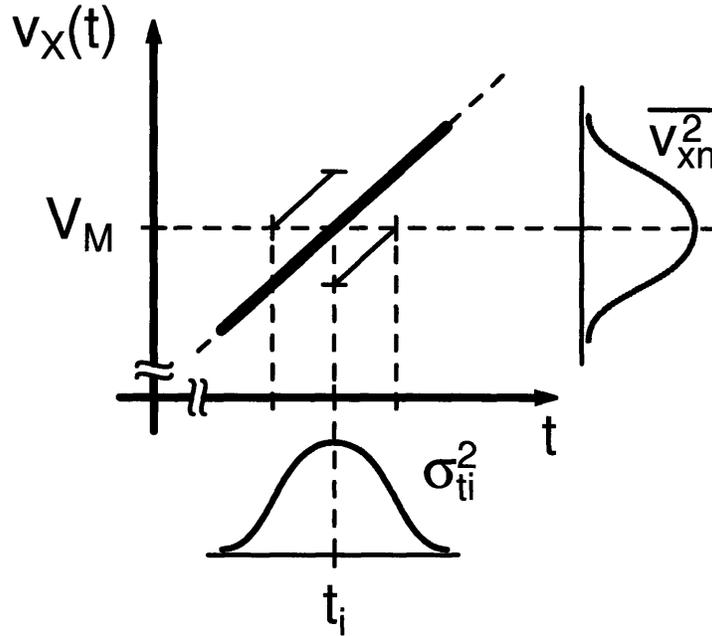


Figure 3-12: Transformation of voltage noise to timing jitter in the comparator decision.

Timing Jitter to Noise Voltage Conversion

The conversion of jitter back to a noise voltage is commonly invoked in the clock jitter analysis of sampling circuits [31] [32]. The idea is that for some input signal rate of change, random variation in the sampling instant results in a random error in the sampled value

$$\overline{v_{nx}^2} = \left| \frac{dv_X}{dt} \right|^2 \sigma_{ti}^2 \quad (3.62)$$

where σ_{ti} is the RMS timing jitter of the sampling clock. Referring again to Figure 3-12, the transformation of timing jitter into a sampled noise voltage is just the reverse of the noise voltage to timing jitter conversion.

Input Referred Noise and Noise Gain

Using the above results, the amplifier introduces a jitter at the output

$$\sigma_{ti}^2 = \overline{v_{on}^2} \left| \frac{dv_O}{dt} \right|_{v_O=V_{Mto}}^{-2} \quad (3.63)$$

where V_{M_o} is the threshold voltage at the output (input threshold of next stage). For an input referred noise voltage $\overline{v_n^2}$, the jitter calculated at the input is

$$\sigma_{ti}^2 = \overline{v_n^2} \left| \frac{dv_X}{dt} \right|_{v_X=V_{CM}}^{-2} \quad (3.64)$$

where V_{CM} is the threshold at the amplifier input in Figure 3-11. Setting the jitter from the output noise equal to the jitter from the input referred noise, the input referred noise is

$$\overline{v_n^2} = \frac{\overline{v_{on}^2}}{|A_N|^2} \quad (3.65)$$

where the noise gain is

$$|A_N| = \left(\left| \frac{dv_O}{dt} \right|_{v_O=V_{M_o}} \right) / \left(\left| \frac{dv_X}{dt} \right|_{v_X=V_{CM}} \right) \quad (3.66)$$

which is the ratio of the rate the output threshold is crossed to the rate the input threshold is crossed.

Example 3.5 Transconductance Amplifier: Input Referred Noise

Consider the amplifier shown in Figure 3-4 with a step ramp input

$$v_X(t) = Mt u(t) \quad (3.67)$$

shown in Figure 3-13 where M is the slope of the ramp. For simplicity, assume the threshold voltage for the transconductance device is zero ($V_T = 0$). The response of the amplifier to a ramp input is

$$v_O(t) = A_o M \left[t - \tau_o (1 - e^{-t/\tau_o}) \right] u(t) \quad (3.68)$$

where $A_o = G_m R_o$ is the DC gain of the amplifier. Using (3.66), the input slope is a

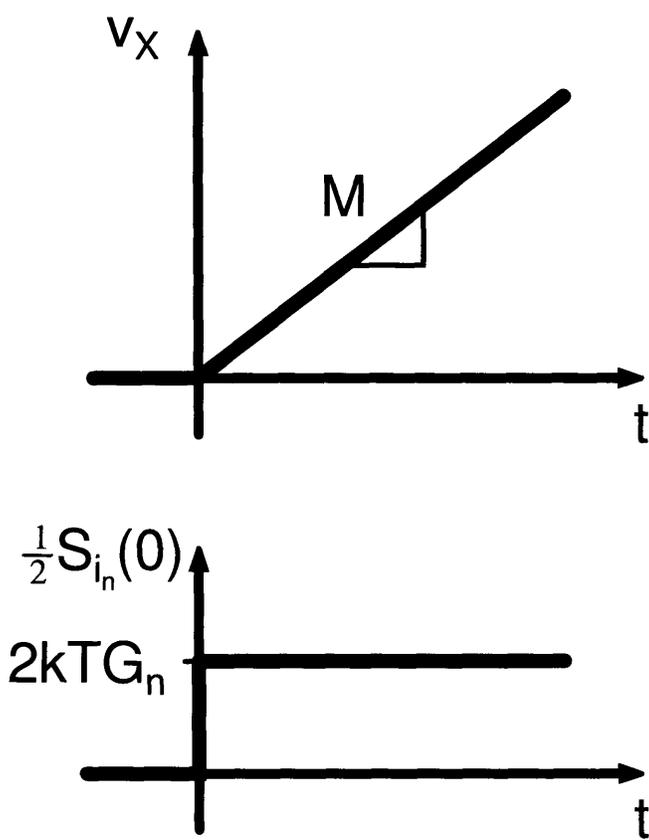


Figure 3-13: Step ramp input and corresponding step noise input.

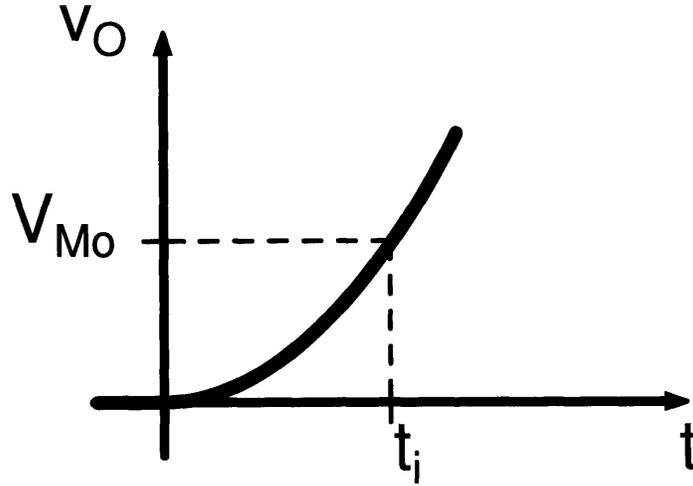


Figure 3-14: Response time t_i for amplifier to reach output threshold V_{Mo} .

constant M , and the output slope is

$$\left. \frac{dv_O}{dt} \right|_{v_O=V_{Mo}} = MA_o [1 - e^{-t_i/\tau_o}] u(t_i) \quad (3.69)$$

where t_i is the response time for the output to cross its threshold V_{Mo} as shown in Figure 3-14. The noise gain is

$$|A_N(t_i)| = A_o [1 - e^{-t_i/\tau_o}] u(t_i). \quad (3.70)$$

Using the expression for the output voltage noise (3.37) derived in Example 3.3, the input referred noise is

$$\begin{aligned} \overline{v_n^2}(t_i) &= \frac{\overline{v_o^2}(t_i)}{|A_N(t_i)|^2} \\ &= \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{C} \right) \left(\frac{1}{A_o} \right) \left[\frac{1 + e^{-t_i/\tau_o}}{1 - e^{-t_i/\tau_o}} \right] u(t_i) \\ \overline{v_n^2}(t_i) &= \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{C} \right) \left(\frac{1}{A_o} \right) \coth \left(\frac{t_i}{2\tau_o} \right) u(t_i). \end{aligned} \quad (3.71)$$

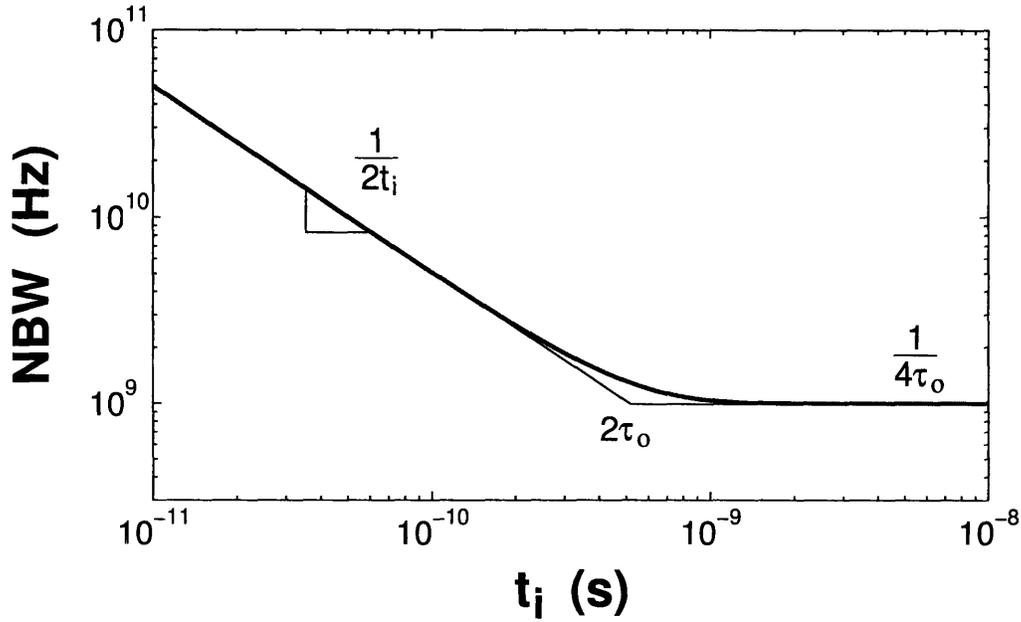


Figure 3-15: Noise Bandwidth versus response time t_i . $\tau_o = 250$ ps

The noise bandwidth can be factored out of (3.71)

$$\overline{v_n^2}(t_i) = 4kTR_n \text{NBW} \quad (3.72)$$

$$\text{NBW}(t_i) = \frac{1}{4\tau_o} \coth\left(\frac{t_i}{2\tau_o}\right) u(t_i) \quad (3.73)$$

where $R_n = G_n/G_m^2$ is the usual input referred noise resistance of a transconductance amplifier. Figure 3-15 shows a plot of NBW versus response time t_i . The limiting behavior of these expression are now presented for $t_i \ll \tau_o$ and $t_i \gg \tau_o$.

For times much shorter than the time-constant at the output of the amplifier ($t_i \ll \tau_o$), the transconductance amplifier operates as an integrator. Using the first two terms of a Taylor approximation for the exponential (3.38), the output voltage grows quadratically with time

$$v_o(t) = \frac{1}{2} \left(\frac{G_m}{C} \right) M t^2 u(t) \quad (3.74)$$

and the noise gain grows with time

$$|A_N| = \frac{G_m}{C} t_i. \quad (3.75)$$

The output random walk voltage noise expressed in terms of the noise bandwidth is

$$\overline{v_o^2} = 4kTG_n \left(\frac{t_i}{C} \right)^2 \text{NBW} \quad (3.76)$$

and the input referred noise is

$$\overline{v_n^2} = 4kTR_n \text{NBW} \quad (3.77)$$

where the noise bandwidth is

$$\text{NBW} = \frac{1}{2t_i}. \quad (3.78)$$

The noise bandwidth is inversely proportional to the response time t_i as shown in Figure 3-15.

The other limiting case of interest is the steady-state solution ($t \gg \tau_o$). For this case, the exponential terms in (3.71) go to zero. The output voltage is a delayed version of the input with the slope scaled by the DC gain

$$v_o(t) = A_o M [t - \tau_o] u(t). \quad (3.79)$$

The noise gain is then just the DC amplifier gain

$$|A_N| = A_o \quad (3.80)$$

and the output noise voltage is

$$\overline{v_o^2} = 4kTG_n \frac{1}{4\tau_o} = \left(\frac{G_n}{G_m} \right) \frac{kT}{C} (G_m R_o). \quad (3.81)$$

The input referred noise voltage is the expected kT/C noise

$$\overline{v_n^2} = \left(\frac{G_n}{G_m}\right) \left(\frac{kT}{C}\right) \left(\frac{1}{A_o}\right) \quad (3.82)$$

and the noise bandwidth in this case is

$$\text{NBW} = \frac{1}{4\tau_o} = \frac{\pi}{2} f_{3\text{dB}} \quad (3.83)$$

which is the familiar fraction of the 3dB bandwidth.

The shape of the NBW versus response time plot in Figure 3-15 is determined by the hyperbolic cotangent function. Because the input referred noise is the input referred white noise PSD times the NBW, the input referred noise voltage has the same shape as the plot in the figure. In addition, Figure 3-15 shows that the intersection of the steady-state and band-limiting asymptotes is $t_i = 2\tau_o$.

□

3.5 Periodic Filtering Frequency Domain Model

While the non-stationary analysis of noise sources describes the circuit response to the step noise input in detail, in most cases the final value is sampled and the system operates on a series of discrete-time samples. Therefore, it is the statistics of the series of samples that are of interest. Even though the details of the processing during each period results in non-stationary noise voltages and currents, the same operation is performed each clock cycle, and the signals have the same statistics each clock cycle. This means that the process is wide-sense cyclo-stationary (WSCS). The periodically sampled values then all have the same statistics and form a WSS discrete-time series. First, the periodic filtering sampler model is described, and the filter transfer function is defined. Then, well known noise aliasing techniques can be applied to obtain a noise PSD estimate for the series of samples.

The derivation for the model of a periodic filtering sampler follows that presented

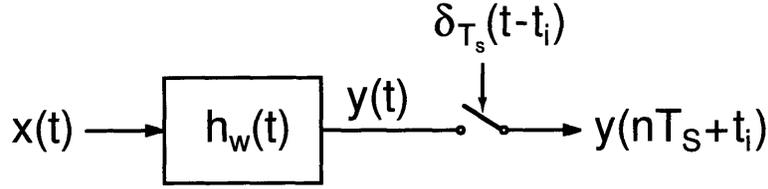


Figure 3-16: Periodic filtering sampler model: the output samples can be modeled as the impulse train sampling of the input filtered by Fourier transform of the windowed impulse response.

in [20] for a periodic integrating sampler. The value of the n^{th} -sample of the output $y(t)$ for a system that integrates the input $x(t)$ from time nT_s to $nT_s + t_i$ is

$$y(nT_s + t_i) = \int_{nT_s}^{nT_s + t_i} x(\tau) d\tau \quad (3.84)$$

$$= \int_{-\infty}^{+\infty} x(\tau) w(nT_s + t_i - \tau) d\tau \quad (3.85)$$

where $w(t)$ is the rectangular window function of unit height and duration t_i . Realizing that the second integral is just the convolution of the input $x(t)$ to a time-shifted impulse response of a finite duration integrator $w(t)$, the procedure is easily extended to finite duration filtering of an arbitrary impulse response

$$y(nT_s + t_i) = \int_{-\infty}^{+\infty} x(\tau) h_w(nT_s + t_i - \tau) d\tau \quad (3.86)$$

where $h_w(t) = h(t)w(t)$ is the windowed impulse response. It should be noted that it is the zero-state response that is found from the convolution of the input with an impulse response. Therefore, this procedure assumes the output is reset between operations. Continuing with the model derivation, the series of periodically filtered samples can be expressed as the infinite sum of samples

$$\sum_{n=-\infty}^{+\infty} y(nT_s + t_i) \delta(t - nT_s - t_i) = y(t) \sum_{n=-\infty}^{+\infty} \delta(t - nT_s - t_i) \quad (3.87)$$

which is an impulse train sampling of the output. Using the usual short-hand for the sampling impulse train

$$\delta_{T_s}(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT_s) \quad (3.88)$$

the output samples of the periodic filtering system can be modeled as shown in Figure 3-16 according to

$$y(t) \delta_{T_s}(t - t_i) = [x(t) * h_w(t)] \delta_{T_s}(t - t_i) \quad (3.89)$$

where the filter function $H_w(f)$ is the Fourier transform the the windowed impulse response.

$$H_w(f) = \int_0^{t_i} h(t) e^{-j(2\pi f)t} dt. \quad (3.90)$$

The model in Figure 3-16 reduces to that originally suggest in [22] and used in [24] [25] for a period integrating system. The periodic filtering model also works to describe the classic RC sampling circuit. Because the switch and capacitor are assumed to reach steady-state, the filter function is just the RC low-pass filter of the switch and capacitor.

The advantage of generalizing the periodic integration model to handle periodic filtering is that the variation in output samples from periodic filtering of noise sources can be analyzed using well established noise aliasing theory where the transfer function for the noise sources is the $H_w(f)$ from the noise source to the output. The procedure for determining the filter transfer function is to find the Laplace s-domain transfer function from the noise source to the output. The inverse Laplace transform yields the system impulse response, which is then windowed by $w(t)$ from 0 to t_i . The Fourier transform of the windowed impulse response produces the desired filter

function. Summarizing mathematically,

$$H(s) \xrightarrow{\mathcal{L}^{-1}} h(t) \quad (3.91)$$

$$h_w(t) = h(t)w(t) \quad (3.92)$$

$$h_w(t) \xrightarrow{\mathcal{F}} H_w(f). \quad (3.93)$$

The noise PSD of the sampled output can then be found from the sum of the filtered and shifted input noise PSD [33] [34] [35] [36] [16]

$$S_{yy}(f) = \sum_{n=-\infty}^{+\infty} |H_w(f - nf_s)|^2 S_{xx}(f - nf_s) \quad (3.94)$$

which is valid over the two-sided Nyquist range $(-f_s/2 \leq f \leq f_s/2)$. Alternatively, the one-sided aliased noise PSD $S_y(f)$ valid from $0 \leq f \leq f_s/2$ can be calculated as

$$S_y(f) = \sum_{n=-\infty}^{+\infty} |H_w(f - nf_s)|^2 2S_{xx}(f - nf_s) \quad (3.95)$$

where $2S_{xx}(f)$ is the same as assuming a two-sided input noise PSD with the one-sided PSD magnitude. The limits of summation can be truncated to a finite value from knowledge of the effective noise bandwidth of $H_w(f)$ [34]. A more extensive review of key noise aliasing proprieties are given in Section 3.6.

Example 3.6 Periodic Filtering Sampler: Periodic Integration

Consider the simple case of periodic integration of a noise current $i_x(t)$ onto a capacitor C_s for t_i seconds every T_s seconds. The s-domain transfer function from i_x to v_o is

$$H(s) = \frac{1}{sC_s}. \quad (3.96)$$

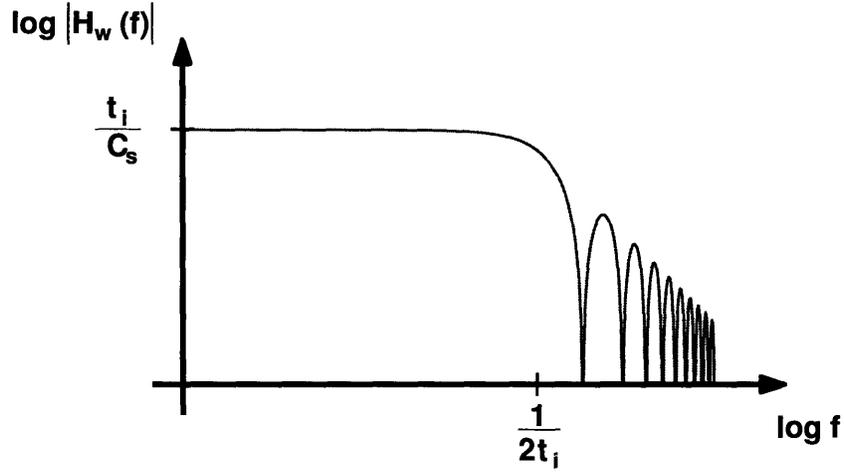


Figure 3-17: Periodic integration filter $H_w(f)$. DC gain $|H_w(0)| = t_i/C_s$ and one-sided noise bandwidth $\text{NBW} = 1/(2t_i)$.

Taking the inverse Laplace transform results in

$$h(t) = \frac{1}{C_s}u(t) \quad (3.97)$$

for an infinite duration integrator. Truncating the impulse response at t_i gives the windowed impulse response

$$h_w(t) = \frac{1}{C_s}w(t), \quad (3.98)$$

and finally, the periodic integration filter is

$$H_w(f) = \left(\frac{t_i}{C_s}\right) \frac{1 - e^{-j(2\pi f)t_i}}{j(2\pi f)t_i}. \quad (3.99)$$

Simplifying and calculating the magnitude squared of the filter function

$$|H_w(f)|^2 = \left(\frac{t_i}{C_s}\right)^2 \text{sinc}^2(ft_i) \quad (3.100)$$

which is a simple sinc filter with a one-sided noise bandwidth of $1/(2t_i)$. A plot of

$H_w(f)$ is given in Figure 3-17. The aliased output spectrum then is

$$S_{v_o v_o}(f) = \sum_{n=-\infty}^{+\infty} |H_w(f - n f_s)|^2 S_{xx}(f - n f_s) \quad (3.101)$$

which if the current source noise i_x has a white noise PSD $S_{xx}(0)$, the one-sided output voltage PSD simplifies to

$$S_{v_o}(f) = S_x(0) \left(\frac{t_i}{C_s} \right)^2 \left(\frac{1}{2t_i} \right) \frac{1}{f_s/2}. \quad (3.102)$$

The output PSD is the expected random walk noise with a white PSD over the Nyquist range. Because the integration time must be less than sampling period $t_i \leq T_s$,

$$\frac{f_s}{2} \leq \text{NBW} \quad (3.103)$$

which means that the noise aliases for all integration times and has an essentially white noise PSD.

□

3.6 Noise Aliasing

Aliasing theory of noise is reviewed highlighting key results that are used in the noise analysis of the prototype CBSC pipeline ADC. The aliasing of white noise and flicker noise are addressed along with useful approximations. Finally, a discussion on the number of terms that must be included in the aliasing summation to include some percentage of the total noise power given the system noise bandwidth.

3.6.1 White Noise Aliasing

The simplest way of thinking about white noise aliasing is in terms of the conservation of noise power. For a stationary signal, the RMS value of a sampled signal must be the same as the RMS value of the original signal. More generally, the ensemble variance of

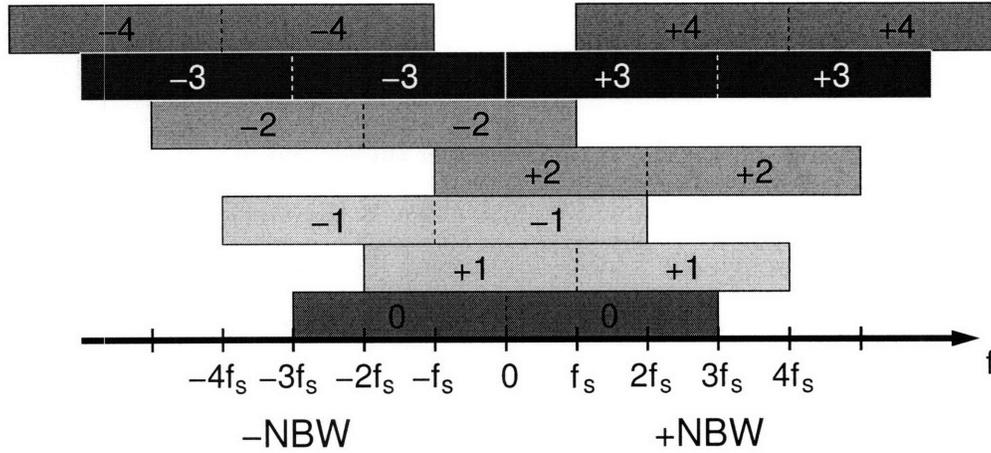


Figure 3-18: White noise aliasing $NBW = 3f_s$ [34].

the original signal at the sampling instant must be the same as the ensemble variance of the sampled value

$$\sigma_x^2 = |H(0)|^2 S_{x_o} NBW = \sigma_y^2 \quad (3.104)$$

where $S_x(f) = S_{x_o}$ is the white noise input PSD. The noise in the original bandwidth has been aliased to the baseband frequency range from 0 to $f_s/2$ such that [34] [35] [33] [37] [38]

$$S_y(0) \approx |H(0)|^2 S_{x_o} \left(\frac{NBW}{f_s/2} \right) \quad (3.105)$$

which means that the aliased spectrum is approximately the original white noise with a multiplier of $NBW/(f_s/2)$. The multiplier is approximately the number of aliased spectra that fall into the baseband frequency range of $-f_s/2 \leq f \leq f_s/2$ as shown in Figure 3-18 [34].

In contrast to sampled signals where the signal bandwidth is always contained within a single Nyquist band, the noise bandwidth of a sampling system is always greater than or equal to $f_s/2$. Therefore, noise aliasing is the norm in sampled systems.

3.6.2 Flicker Noise Aliasing

Flicker noise aliasing can also be examined under the assumption of the conservation of noise power; however, it is more often instructive to decompose the aliased spectra into its direct feed-through and folded components. The results can then be examined in terms of noise power or as a PSD. Both approaches yield different insights to the aliasing of flicker noise and both are considered below. Only the case of unity flicker exponent $1/f$ is considered for mathematical simplicity.

The pre-sampled one-sided noise PSD for flicker noise is

$$S_x(f) = \frac{S_x(1)}{f} \quad (3.106)$$

where an example PSD is shown in Figure 3-19(a). The total noise power is found by integrating the noise PSD

$$\sigma_{total}^2 = \int_{f_L}^{f_H} |H(0)|^2 \frac{S_x(1)}{f} df \quad (3.107)$$

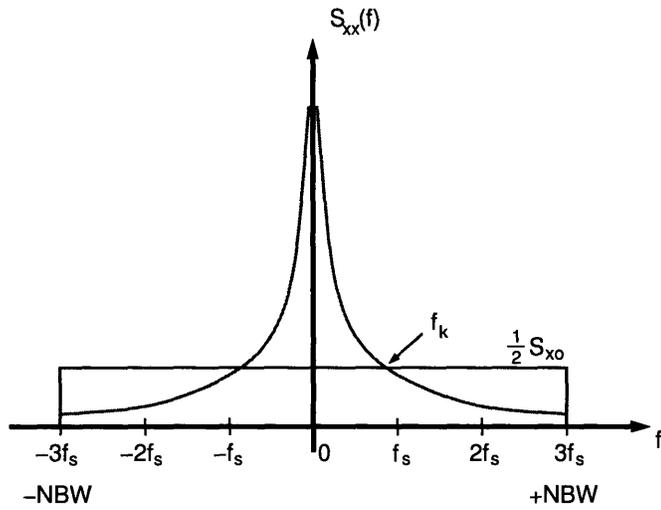
$$= |H(0)|^2 S_x(1) \ln \left(\frac{f_H}{f_L} \right) \quad (3.108)$$

where $S_x(1)$ is the flicker noise at 1Hz, f_H is the upper frequency limit (NBW), $f_L = 1/(2T_o)$ is the lower frequency limit, and T_o is the duration of the measurement. The interpretation for the lower frequency limit is that for a given measurement duration very low frequency variations appear as a DC offset. Decomposing the total noise power into its direct and folded components results in

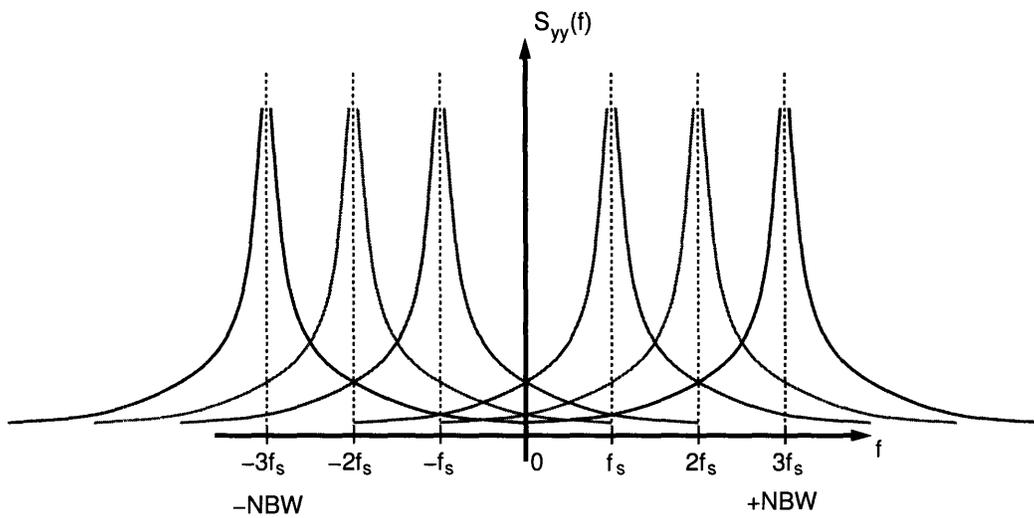
$$\sigma_{total}^2 = \sigma_{direct}^2 + \sigma_{fold}^2 \quad (3.109)$$

where

$$\sigma_{direct}^2 = |H(0)|^2 S_x(1) \ln \left(\frac{f_s/2}{f_L} \right) \quad (3.110)$$



(a)



(b)

Figure 3-19: Flicker noise aliasing (a) Original pre-sampled PSD with flicker and thermal noise. (b) Folded flicker noise.

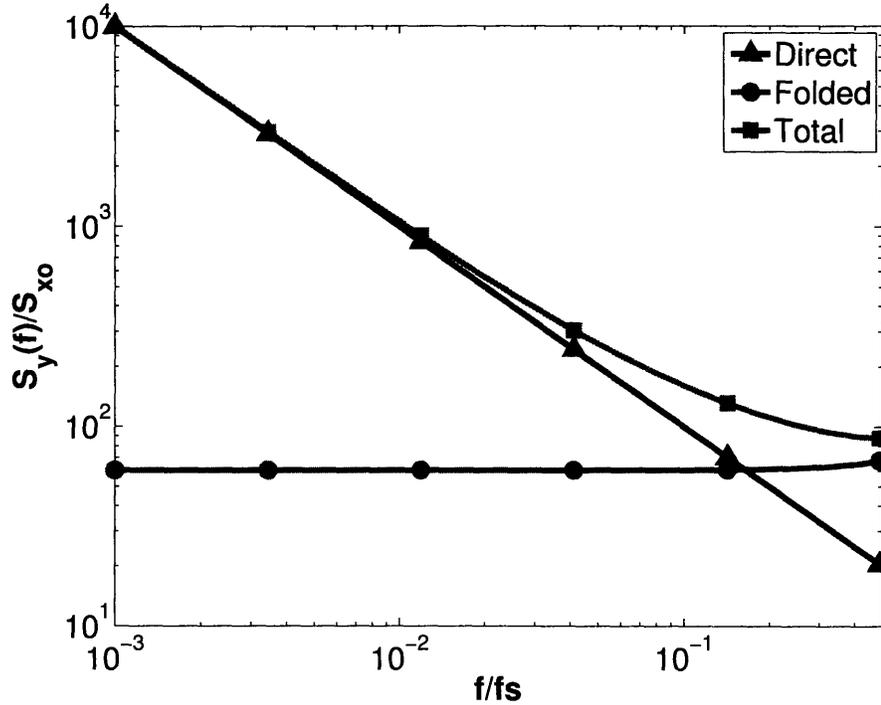


Figure 3-20: Total sampled flicker noise PSD showing direct feed-through contribution and apparent white folded flicker noise.

and

$$\sigma_{fold}^2 = |H(0)|^2 S_x(1) \ln \left(\frac{f_H}{f_s/2} \right). \quad (3.111)$$

It is interesting to note that the folded flicker noise power is independent of the measurement duration T_o , but for a fixed sampling frequency, the direct feed-through flicker noise contribution depends on the measurement duration.

Figure 3-19(b) shows how the folded aliases combine to make up the folded flicker noise PSD. It is evident from Figure 3-19(b) that the folded flicker noise PSD is approximately constant over the Nyquist band $-f_s/2 \leq f \leq f_s/2$. The white noise approximation is discussed below. Assuming the folded flicker noise is essentially white,

$$S_{y,fold}(0) \approx |H(0)|^2 \frac{S_x(1)}{f_s/2} \ln \left(\frac{f_H}{f_s/2} \right) \quad (3.112)$$

and neglecting the logarithmic term, the amount of folded noise is inversely proportional to the sampling frequency. In addition, the PSD originally contained in the Nyquist band feeds directly through to the output

$$S_{y,direct}(f) \approx |H(0)|^2 \frac{S_x(1)}{f}. \quad (3.113)$$

Therefore, the total aliased flicker noise PSD is approximately the sum of direct feed-through component and an essentially white folded component

$$S_{y,total}(f) \approx |H(0)|^2 \left[\frac{S_x(1)}{f} + \frac{S_x(1)}{f_s/2} \ln \left(\frac{f_H}{f_s/2} \right) \right] \quad (3.114)$$

where an example aliased flicker noise PSD showing the direct and folded contributions is given in Figure 3-20 The significance of the folded flicker noise is discussed more below.

A PSD approach to the aliasing problem is now presented that justifies the apparent white noise approximation for the folded flicker noise and gives a useful closed form approximation for its value.

The spectral aliasing summation (3.94) can also be decomposed into its direct and folded components. The direct feed-through component is the case where $n = 0$ in the summation

$$S_{y,0}(f) = |H(f)|^2 S_x(f). \quad (3.115)$$

For the noise originally contained in the Nyquist range, the sampler filters the noise PSD, but otherwise leaves it unchanged.

The folded flicker noise is all the other terms in the summation

$$S_{yy,fold}(f) = \sum_{\substack{n=-\infty \\ n \neq 0}}^{+\infty} |H(f - nf_s)|^2 S_{xx}(f - nf_s). \quad (3.116)$$

Simplifying the summation to handle one-sided PSDs

$$S_{y, \text{fold}}(f) = \sum_{n=1}^{+\infty} |H(nf_s - f)|^2 S_x(nf_s - f) + |H(nf_s + f)|^2 S_x(nf_s + f) \quad (3.117)$$

which is valid from $0 \leq f \leq f_s/2$.

Useful closed form results for the folded flicker noise can be obtained assuming a simple one-pole filter with unity gain

$$|H(f)|^2 = \frac{1}{1 + (f/f_c)^2} \quad (3.118)$$

where f_c is the 3 dB frequency of the filter. The filter serves to bound the flicker noise at high frequencies. Then, the folded noise summation can be approximated by its first term and the contribution from the rest of the terms bound using the Integral Test from calculus [39]. For example, if the first term of (3.117) is written as the sum of the $n = 1$ term and the remaining terms

$$\sum_{n=1}^{\infty} \frac{1}{nf_s - f} \left[\frac{1}{1 + (f/f_c)^2} \right] = \frac{1}{f_s - f} + \sum_{n=2}^{\infty} \frac{1}{nf_s - f} \left[\frac{1}{1 + (f/f_c)^2} \right] \quad (3.119)$$

then an upper and lower bounds can be placed on the remaining summation

$$\sum_{n=2}^{\infty} \frac{1}{nf_s - f} \left[\frac{1}{1 + (f/f_c)^2} \right] \approx \int_a^{+\infty} \frac{1}{nf_s - f} \left[\frac{1}{1 + (f/f_c)^2} \right] dn \quad (3.120)$$

where a is 1 for the upper bound and 2 for the lower bound. Enz [35] approximated the summation using an intermediate lower bound of $3/2$

$$\sum_{n=2}^{\infty} \frac{1}{nf_s - f} \left[\frac{1}{1 + (f/f_c)^2} \right] \approx \int_{\frac{3}{2}}^{+\infty} \frac{1}{nf_s - f} \left[\frac{1}{1 + (f/f_c)^2} \right] dn. \quad (3.121)$$

Carrying out the approximation for both terms in (3.117) and adding the results gives

$$S_{y, \text{fold}}(f) \approx \frac{S_x(1)}{f_s/2} \left[\frac{f_s^2}{f_s^2 - f^2} + \frac{1}{2} \ln \left(\frac{f_c^2}{\left(\frac{3}{2}f_s\right)^2 - f^2} \right) \right] \quad (3.122)$$

which is (8) in [35].

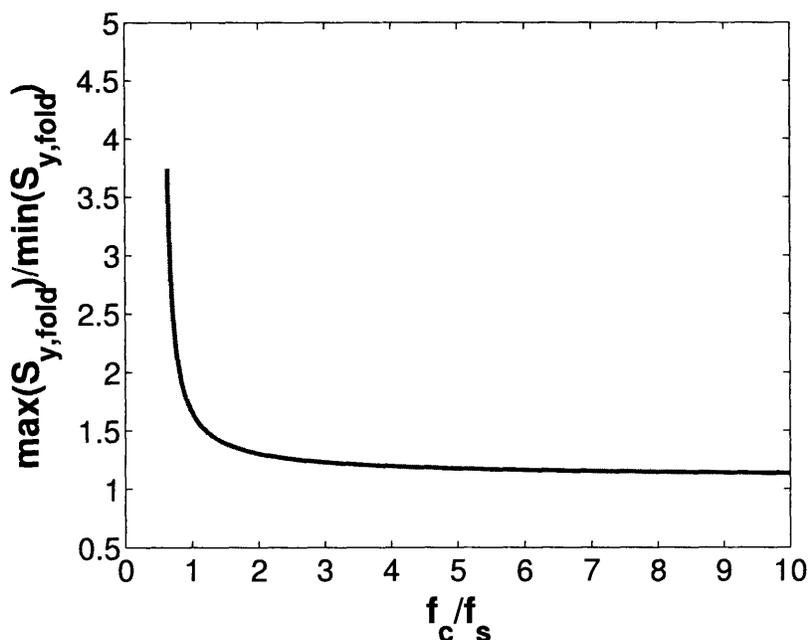


Figure 3-21: Maximum to minimum PSD ratio for folded flicker noise $S_{y, \text{fold}}(f_s/2)/S_{y, \text{fold}}(0)$.

Figure 3-21 plots the maximum to minimum ratio of (3.122) for different ratios of filter bandwidth to sampling frequency. Figure 3-21 shows that the apparent white noise approximation is reasonable for filter bandwidths greater than twice the sampling frequency. Assuming the folded flicker noise has a roughly constant value of $S_{y, \text{fold}}(f_s/2)$ from 0 to $f_s/2$, the final approximation in [35] is

$$S_{y, \text{fold}}(f) \approx \frac{S_x(1)}{f_s/2} \left[1 + \ln \left(\frac{f_c}{f_s} \right) \right]. \quad (3.123)$$

Expressing the flicker noise at 1 Hz $S_x(1)$ in terms of the white noise S_{xo} and the corner frequency f_k

$$S_x(1) = S_{xo}f_k \quad (3.124)$$

the folded flicker noise is proportional to the unsampled white noise PSD

$$S_{y,old}(f) = S_{xo} \left(\frac{f_k}{f_s/2} \right) \left[1 + \ln \left(\frac{f_c}{f_s} \right) \right]. \quad (3.125)$$

Comparing (3.125) and (3.105), the folded flicker noise contribution is equal to the aliased white noise when

$$\text{NBW} \approx f_k \left[1 + \ln \left(\frac{f_c}{f_s} \right) \right] \quad (3.126)$$

or for reasonable (f_c/f_s) ratios, $\text{NBW} \approx 3f_k$.

3.6.3 Finite Summation Approximation of Aliased Noise

For more complicated filter functions and non-unity flicker noise exponent, the evaluation of the integral for the closed-form approximation of the aliasing sum becomes difficult to solve. Therefore, it is often more convenient to find the aliased spectra from numerical evaluation of the aliasing summation (3.94). The difficulty in this approach is determining the number of terms in the summation to use to achieve a desired accuracy. A method analogous to the cumulative distribution function (CDF) from statistics is used to determine the number of terms required to achieve a certain percentage of the total.

Intuitively, it should be possible to approximate the infinite sum (3.117) using a finite number of terms if the filter has a finite noise bandwidth

$$S_{y,old}(f) = \sum_{n=0}^N |H(nf_s - f)|^2 S_x(nf_s - f) + |H(nf_s + f)|^2 S_x(nf_s + f). \quad (3.127)$$

The question is how large does N need to be to account for some percentage of the total folded noise power. The required number of terms is related to the noise

bandwidth NBW of $H(f)$

$$N = k\eta \quad (3.128)$$

where η is the noise bandwidth normalized to half the sampling frequency

$$\eta = \left\lceil \frac{\text{NBW}}{f_s/2} \right\rceil \quad (3.129)$$

and $k\eta$ terms are required to get the desired accuracy.

Consider the white noise aliased from a one-pole transfer function. A one-pole transfer function should be a conservative case since most other filters have lower noise bandwidths. A CDF like plot can be made of the fraction of the total noise power versus k referred to here as the cumulative aliasing function (CAF). Figure 3-22 shows the plot of the CAF. Note that using $k = 1$ is equivalent to assuming that 100% of the noise power is contained within the noise bandwidth. However, Figure 3-22 and Table 3.1 show that only 80.6% of the noise is accounted for with this approximation. Table 3.1 shows the required number of η for higher accuracy. Note that the CAF noise power fraction approaches one slowly, but for $k = 4$ the sum would contain 95% of the total noise power.

3.7 Summary

A comprehensive series of noise analysis methods have been presented for linear circuit analysis. Their basic application has been illustrated through a series of examples. In addition, a definition of noise gain for large signal systems has been presented assuming an amplifier with noise and a noiseless amplifier with input referred noise produce the same jitter. Next, a periodic filtering analysis method has been presented that allows for the analysis of periodic samples in terms of well-known aliasing theory. A brief review of aliasing theory is presented focusing on the lesser known effect of aliased flicker noise. The techniques and concepts presented in this chapter are used in later chapters to analyze comparators and their preamplifiers. The results

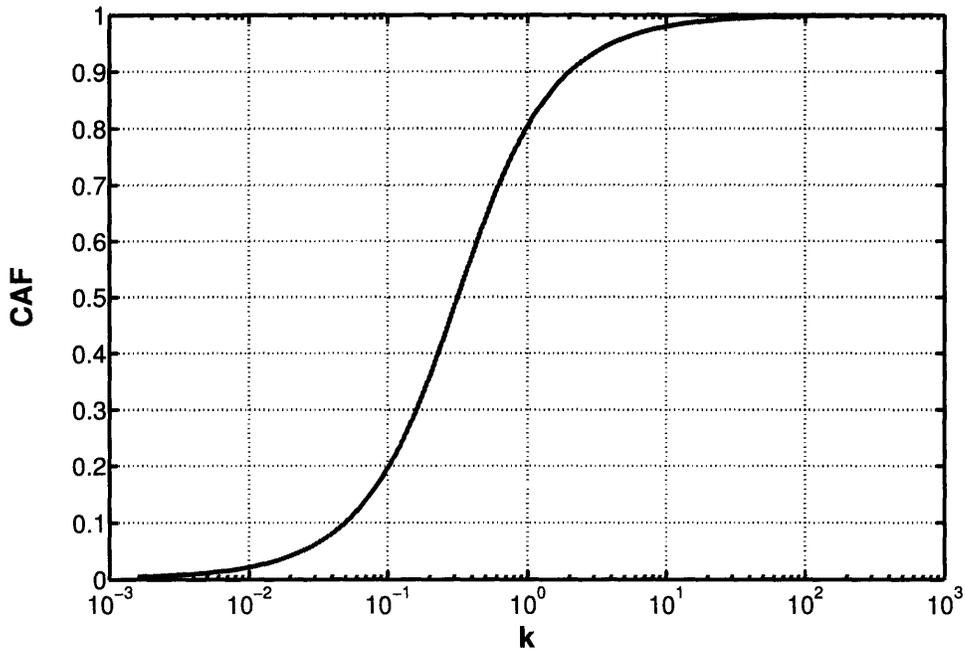


Figure 3-22: Cumulative aliasing function (CAF): fraction of total noise power as a function of the number k of normalized noise bandwidths η .

k	% of Total Noise Power
1	80.6%
4	95%
20	99%
200	99.9%

Table 3.1: Fraction of total noise power as a function of the number k of the normalized noise bandwidths $\eta = \lceil \text{NBW}/(f_s/2) \rceil$.

summarized in Example 3.5 for a ramp input will be used extensively.

Chapter 4

Threshold Detection Comparator Design

4.1 Overview

Threshold comparator design for comparator-based switched capacitor circuits is presented. First, threshold comparator specifications are reviewed and contrasted with latched based comparators that are ubiquitous in mixed-signal design. Because the threshold comparator in the CBSC charge transfer phase determines to a large extent the noise accuracy, considerations for low noise threshold comparator design are addressed. A band-limiting preamplifier placed in front of a traditional threshold detection comparator is recommended, and a noise analysis of the resulting comparator plus preamplifier is presented drawing on the non-stationary noise analysis from Chapter 3. A design procedure for the band-limiting preamplifier is proposed. Finally, the design of the threshold detection comparator is discussed.

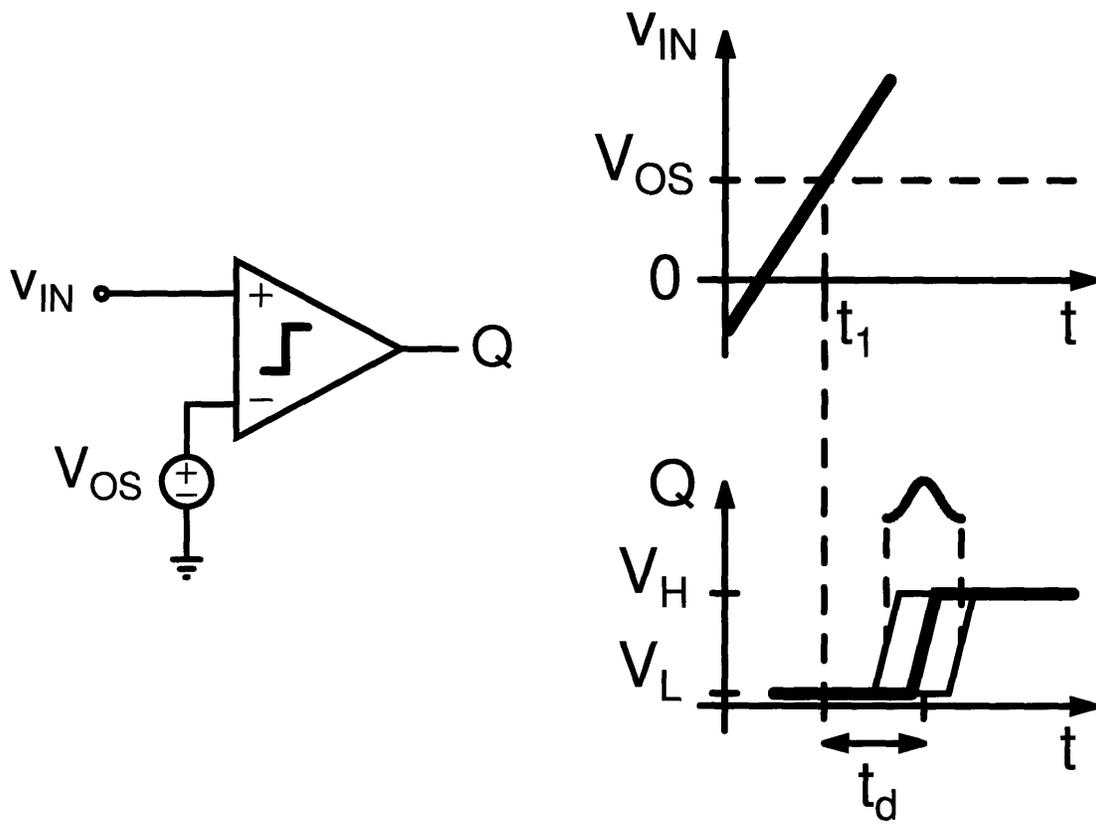


Figure 4-1: General definition of threshold detection comparator performance.

4.2 Threshold Detection Comparators

4.2.1 Specifications

Unlike traditional latch-based clocked comparators that determine whether its input voltage is positive or negative at a specific instant in time, threshold detection comparators must determine the time at which the input crosses zero. A generic schematic of a threshold detection comparator with its key parameters is shown in Figure 4-1. In simplistic terms, if the input voltage is positive, the output must be a logic high, and if the input voltage is negative, the output must be a logic low. A comparator offset (V_{os}) causes a systematic error in the threshold, which for a ramp input can also be viewed as a timing skew (t_1) in the threshold detection. The comparator has a finite delay (t_d) from the point of crossing the offset adjusted threshold to the logic transition. This delay varies due to thermal and flicker noise sources in the devices used in the comparator and appears as jitter in the comparator decision. The jitter can also be input referred and expressed as a noise voltage superimposed on the reference voltage. The transformation of jitter to voltage noise and voltage noise to jitter was discussed in Chapter 3.

As mentioned in Chapter 2, the role of the virtual ground threshold detection comparator is of critical importance to the accuracy of the CBSC charge transfer accuracy. Offset and delay errors in the decision can be tolerated in most systems, but jitter in the threshold detection results in a noise voltage sampled onto the load capacitance. When referred to the input, this voltage noise can be equivalently modeled as an input referred voltage noise at the input of the virtual ground threshold detection comparator. Methods for analyzing non-stationary threshold detection systems to determine their input referred noise voltage for white noise were presented in Chapter 3. The previously obtained results for a transconductance amplifier with finite output resistance are briefly reviewed and are used to discuss the design of low noise threshold detection comparators. Only thermal noise is considered here to simplify the discussion. The impact of flicker noise is addressed in Chapter 6 when

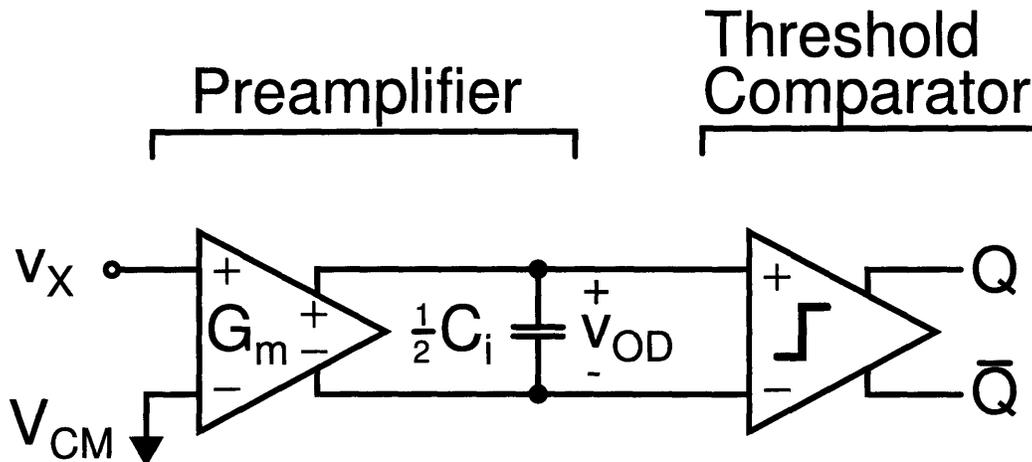


Figure 4-2: Ideal threshold detection comparator with band-limiting preamplifier.

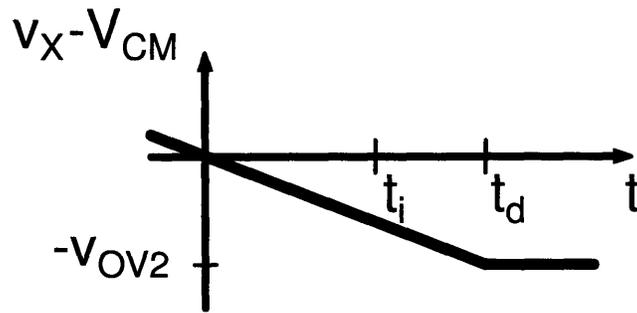
the analysis of the entire CBSC gain stage is performed.

4.2.2 Low Noise Comparator Design

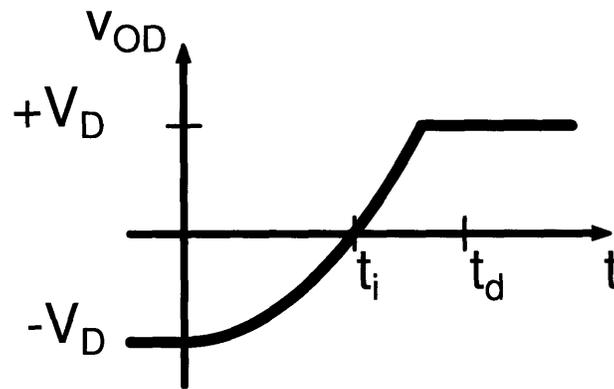
A threshold detection comparator is usually thought of as a wide-bandwidth high-gain amplifier possibly implemented as a cascade of low-gain amplifiers [40] [41]. The first stage of the cascaded amplifier typically dominates its input referred noise PSD and approximately sets the comparator noise bandwidth. Because the capacitance at the output of the first stage is kept as small as possible to maximize the speed at a given power consumption, the input referred noise of such an amplifier can be rather large.

One possible solution to lower the input referred noise of the comparator is to add a preamplifier in front of the threshold detection comparator as shown in Figure 4-2. The sensitivity of the comparator is improved if the preamplifier has lower input referred noise than the threshold comparator alone and if the preamplifier has enough gain to dominate the input referred noise performance of the comparator.

In small-signal amplifiers, the frequency of the transfer function poles of the amplifier determine speed, but in threshold detection systems, the time it takes the output to reach a threshold voltage determines speed. This difference in speed defi-



(a)



(b)



(c)

Figure 4-3: Ideal timing for comparator with preamplifier. The preamplifier output voltage is clamped at $\pm V_D$. (a) Preamplifier input voltage where the summing node voltage v_X has crossed the virtual ground condition at time zero. (b) Preamplifier output voltage showing the response time t_i it takes for the preamplifier output to reach the comparator threshold. (c) Output logic signal changes stage after total comparator delay t_d .

nitions is a consequence of comparators not necessarily operating under small-signal steady-state conditions. If the band-limiting preamplifier output always starts with the same initial condition, for the same load capacitance C_L and transconductance G_m , the fastest way to the output logic threshold is the amplifier with the highest small-signal gain [42].

The general ramp response of a transconductance amplifier was derived in Chapter 3 (3.68), and is repeated here for convenience

$$v_O(t) = A_o M \left[t - \tau_o (1 - e^{-t/\tau_o}) \right] u(t) \quad (4.1)$$

where the small-signal steady-state gain is $A_o = G_m R_o$, the preamplifier time constant is $\tau_o = R_o C_i$, and $M = dv_X/dt$ is the input ramp rate. Figure 4-3 shows the response of the preamplifier and threshold comparator assuming the output of the preamplifier is clamped to $|V_D|$ between decisions. The time it takes the output of the preamplifier to reach the threshold V_M is defined as the preamplifier response time t_i . Holding the transconductance G_m and the load capacitance C_i constant, Figure 4-4(a) shows a plot of the ramp response for increasing values of output resistance demonstrating that the preamplifier with the highest output resistance has the fastest ramp response.

Figure 4-5(a) is a graph of preamplifier response time (t_i) versus preamplifier output resistance R_o for constant G_m and C_i . Since it is not possible to solve (4.1) explicitly for the response time t_i in the general case, consider the limiting behavior

$$v_O(t_i) = \begin{cases} \frac{1}{2} \left(\frac{G_m}{C_i} \right) M t_i^2 & \text{Ideal integrator } (t_i \ll \tau_o) \\ G_m R_o M t_i & \text{Steady-state } (t_i \gg \tau_o). \end{cases} \quad (4.2a)$$

$$(4.2b)$$

To find the response time for the limiting cases, set the output voltage equal to the threshold voltage V_M and solve for the response time t_i . For the steady-state case when R_o is small (4.2b), the response time is inversely proportional to R_o

$$t_{i,ss} = \left(\frac{V_M}{M G_m} \right) \frac{1}{R_o}. \quad (4.3)$$

As the output resistance approaches infinity $R_o \rightarrow \infty$, the preamplifier becomes an ideal integrator, and the time to reach the threshold approaches its minimum value and becomes independent of R_o

$$t_{i,int} = \left(\frac{2V_M C_i}{MG_m} \right)^{\frac{1}{2}}. \quad (4.4)$$

Using the above relationships, it can be shown that the point at which these two asymptotes intersect is where $\tau_o = t_{i,int}/2$. This point represents a point of diminishing returns for increasing output resistance and is noted as $R_{o,dim}$ in Figure 4-5(a).

Intuitively, a band-limiting stage should be lower noise than a broadband stage, but as was shown in Chapter 3, care must be taken in applying knowledge of small-signal amplifier noise behavior to systems that do not necessarily reach steady-state. From Example 3.5, the input referred noise of a transconductance amplifier was shown to be proportional to the noise bandwidth (3.73), which is a function of the preamplifier response time t_i . The key results from that discussion are the input referred noise voltage

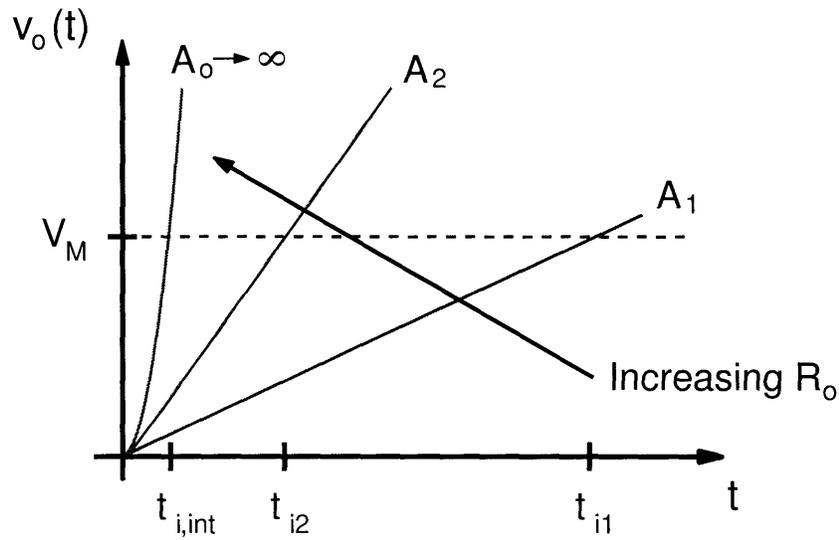
$$\overline{v_n^2}(t_i) = 4kTR_n \text{NBW} \quad (4.5)$$

and the noise bandwidth

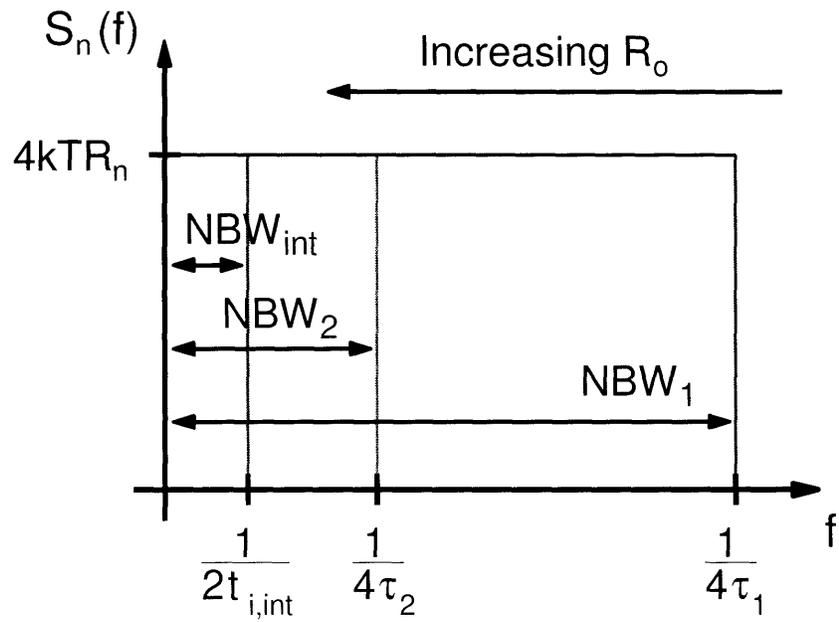
$$\text{NBW}(t_i) = \frac{1}{4\tau_o} \coth \left(\frac{t_i}{2\tau_o} \right) u(t_i) \quad (4.6)$$

where the noise resistance of the preamplifier $R_n = G_n/G_m^2$. As shown in Figure 4-4(b), for a constant G_m and C_i , the preamplifier noise bandwidth decreases as the output resistance is increased as expected. However, at some point the preamplifier begins to behave like an integrator, and the noise bandwidth does not decrease below that defined by the random walk noise

$$\text{NBW} \geq \frac{1}{2t_{i,int}} \quad t_i \ll \tau_o. \quad (4.7)$$

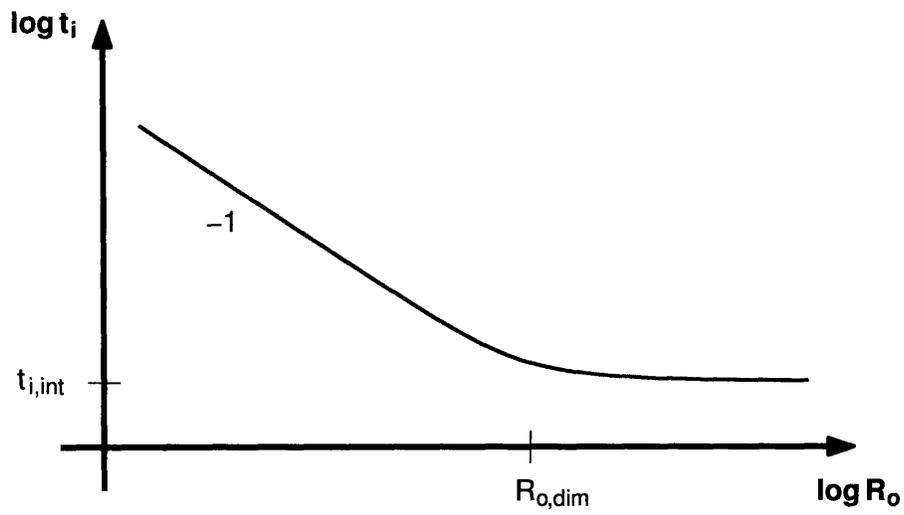


(a)

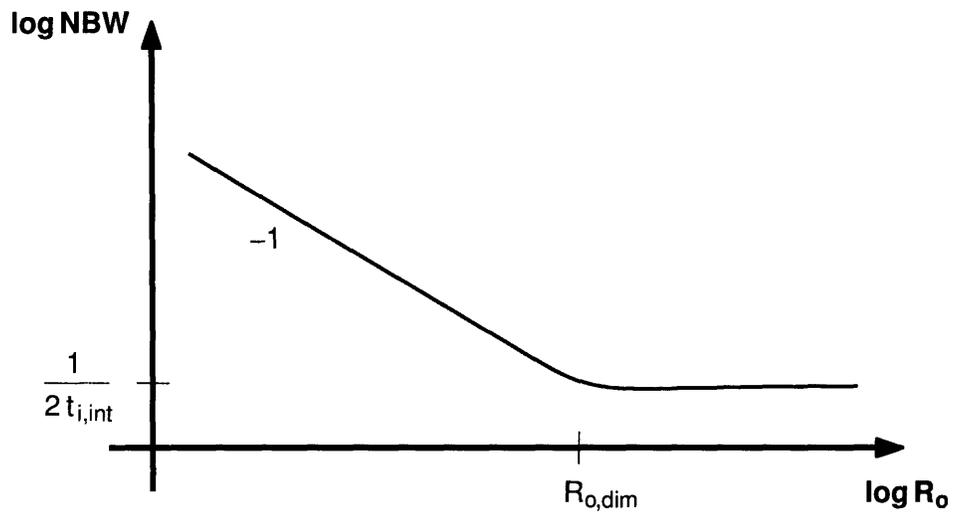


(b)

Figure 4-4: Holding G_m and C_L constant, R_o is swept, the ramp response to a given threshold V_M is faster for high R_o and the total mean-square noise is lower for high R_o (a) Ramp response. (b) Noise bandwidth.



(a)



(b)

Figure 4-5: Holding G_m and C_i constant, R_o is swept. (a) Ramp response: time to a given threshold V_M is faster for larger R_o . (b) Noise bandwidth: reduces for larger R_o

The graph in Figure 4-5(b) also shows that the noise bandwidth decreases inversely proportional to the preamplifier output resistance

$$\text{NBW} = \frac{1}{4R_o C_i} \quad t_i \gg \tau_o. \quad (4.8)$$

As the preamplifier output resistance approaches infinity, the noise bandwidth becomes independent of the output resistance

$$\text{NBW} = \frac{1}{2t_{i,int}} \quad (4.9)$$

and the point at which these two asymptotes intersect is when $\tau_o = t_{i,int}/2$. Therefore, the noise also has a point of diminishing return that is the same as for speed considerations.

Noise from the clamped state of the circuit does results in a kT/C_i reset noise initial condition on the preamplifier load capacitor C_i , but the clamp noise is at the output of the preamplifier. Therefore, its contribution to the input referred noise is small if the preamplifier has a relatively large noise gain or has time for the initial condition to decay to zero. The noise contribution from the clamp stage of the preamplifier is addressed in the CBSC gain stage noise analysis in Chapter 6.

4.2.3 Preamplifier Design

The goal in this section is to derive a set of approximate design equations for the preamplifier. Given a noise requirement $\overline{v_n^2}$, a speed requirement $f_s = 1/T_s$, and some information about the linearity requirements of the system, determine the required power consumption $G_m = f(I_D)$, the required capacitance C_i and the required output resistance R_o . Again, only thermal noise is addressed. First, a general set of design equations are presented. Then, three special cases are addressed. The two limiting cases of a wide bandwidth preamplifier and an ideal integrator preamplifier are considered, and the point of diminishing return is discussed.

Analysis Equations

Before deriving the design relationships, the relevant analysis equations for the preamplifier are summarized. In the following discussion, the preamplifier response time t_i is assumed to dominate the total comparator delay. The speed of the system places some constraint on amount of time that the preamplifier can spend integrating, which is captured in the following relation

$$mt_i = \frac{T_s}{2} \quad (4.10)$$

where m is the number of t_i 's that can fit into $T_s/2$. The linearity constraint determines the amount of time allowed for the final preamplifier response time [43]. The number of response times m is analogous to the number of time constants required for settling in an op-amp based system ($n\tau_o = T_s/2$). The equation that determines the response time is

$$V_M = MA_o \left[t_i - \tau_o (1 - e^{-t_i/\tau_o}) \right]. \quad (4.11)$$

As discussed in Chapter 2, ramp rate variation results in an overshoot that is a function of the input voltage. This signal dependent overshoot introduces non-linearity in the sampled output voltage of the CBSC stage. For a given ramp rate variation over the full-scale output range, the linearity requirement for the stage places a constraint on the allowable overshoot at the output V_{ov} which when referred to the input of the comparator is

$$V_{ovx} = V_{ov} \left(\frac{C_1}{C_1 + C_2} \right) = Mt_i. \quad (4.12)$$

The input referred noise of the comparator can then be written as

$$\overline{v_n^2} = \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{C_i} \right) \left(\frac{1}{A_o} \right) \coth \left(\frac{t_i}{2\tau_o} \right) \quad (4.13)$$

where terms from the noise bandwidth and noise resistance have been rearranged to obtain a result that is proportional to kT/C_i . Solving (4.11) for A_o , the input referred

noise can be expressed as

$$\overline{v_n^2} = \left(\frac{G_n}{G_m}\right) \left(\frac{kT}{C_i}\right) \left(\frac{V_{ovx}}{V_M}\right) \left[1 - \frac{\tau_o}{t_i} \left(1 - e^{-t_i/\tau_o}\right)\right] \coth\left(\frac{t_i}{2\tau_o}\right). \quad (4.14)$$

Equations (4.10), (4.11), (4.12) and (4.14) complete the set of analysis equations for the preamplifier.

Design Equations

Given the linearity constraints (m, V_{ovx}), the threshold voltage V_M of the threshold comparator following the preamplifier, and the topology dependent G_n/G_m ratio, the input referred noise of the comparator is only a function of the preamplifier load capacitance C_i and the preamplifier response time t_i relative to the preamplifier time constant $x = t_i/\tau_o$. Solving (4.14) for C_i

$$C_i = \left(\frac{G_n}{G_m}\right) \left(\frac{kT}{\overline{v_n^2}}\right) \left(\frac{V_{ovx}}{V_M}\right) \left[1 - \frac{1}{x} \left(1 - e^{-x}\right)\right] \coth\left(\frac{x}{2}\right) \quad (4.15)$$

sets the required preamplifier load capacitance. The speed of the preamplifier can then be related to G_m/C_i

$$\frac{G_m}{C_i} = (2mf_s) \left(\frac{V_M}{V_{ovx}}\right) \left(\frac{x}{1 - \frac{1}{x}(1 - e^{-x})}\right) \quad (4.16)$$

where (4.11), (4.10) and the output resistance for $t_i = x\tau_o$

$$R_o = \frac{t_i}{xC_i} = \frac{1}{x(2mf_s)C_i} \quad (4.17)$$

have been combined. The speed requirement combined with the value of C_i calculated above for noise determines the required transconductance

$$G_m = (2mf_s) \left(\frac{G_n}{G_m}\right) \left(\frac{kT}{\overline{v_n^2}}\right) \left[x \coth\left(\frac{x}{2}\right)\right] \quad (4.18)$$

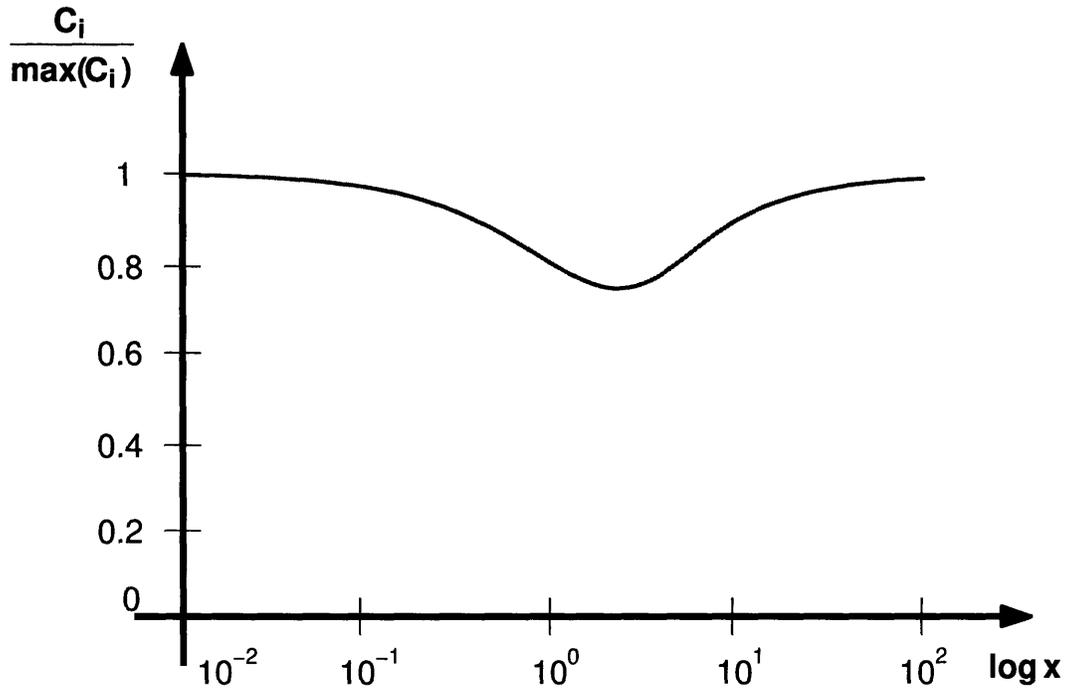


Figure 4-6: Relative preamplifier band-limiting capacitance C_i versus response time relative to preamplifier time constant $x = t_i/\tau_o$ for a given noise and speed requirement. Because C_i is relatively constant, the relative amount of response time is approximately only a function of output resistance R_o ($x \sim 1/R_o$).

The preamplifier power can be found from the G_m/I_D relationship for the input devices of the preamplifier.

The general design equations above depend on the amount of time it takes the preamplifier to reach the threshold V_M relative to the preamplifier time constant. This relative amount of response time defined above as

$$x = \frac{t_i}{\tau_o} = \frac{1}{(2mf_s)R_oC_i} \quad (4.19)$$

where the constant speed requirement (4.10) and $\tau_o = R_oC_i$ have been substituted. The relative response time is a function of both R_o and C_i . Figure 4-6 shows a plot of the relative magnitude of C_i versus x for a constant noise, speed, and linearity requirements. The required capacitance is essentially independent of whether the preamplifier has a wide bandwidth or is an ideal integrator. The reason for the

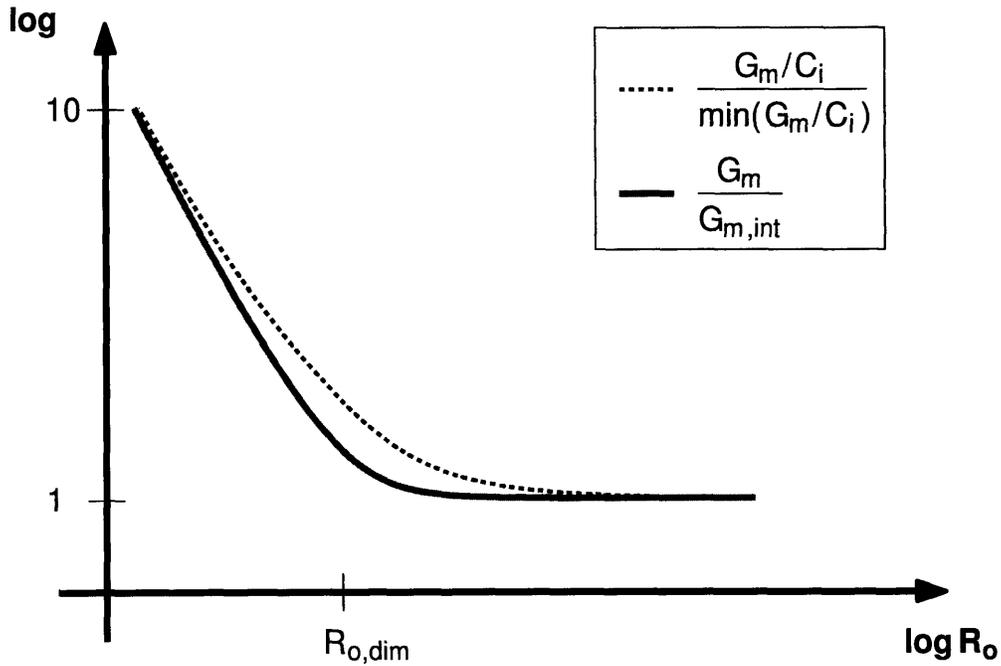


Figure 4-7: Relative preamplifier speed G_m/C_i and transconductance G_m versus output resistance R_o . Transconductance approaches the ideal integrator result versus R_o more quickly than speed.

minimum in the required capacitance near $t_i = 2\tau_o$ can be understood as follows: for a constant G_m and C_i , Figure 4-5 shows that the noise bandwidth improves more quickly than the speed (t_i). For the design equations, the noise and speed are held constant. Therefore, the improvement in noise can be traded for lower capacitance C_i and lower G_m to keep the noise and speed the same. The implications of the faster improvement in noise versus R_o for the design equations can be seen in Figure 4-7 where the required relative transconductance G_m approaches its minimum value more quickly than the relative speed G_m/C_i .

The limiting behavior versus output resistance of the design equations (4.15), (4.16), and (4.18) is now explored.

The limiting behavior of the required capacitance for large and small output re-

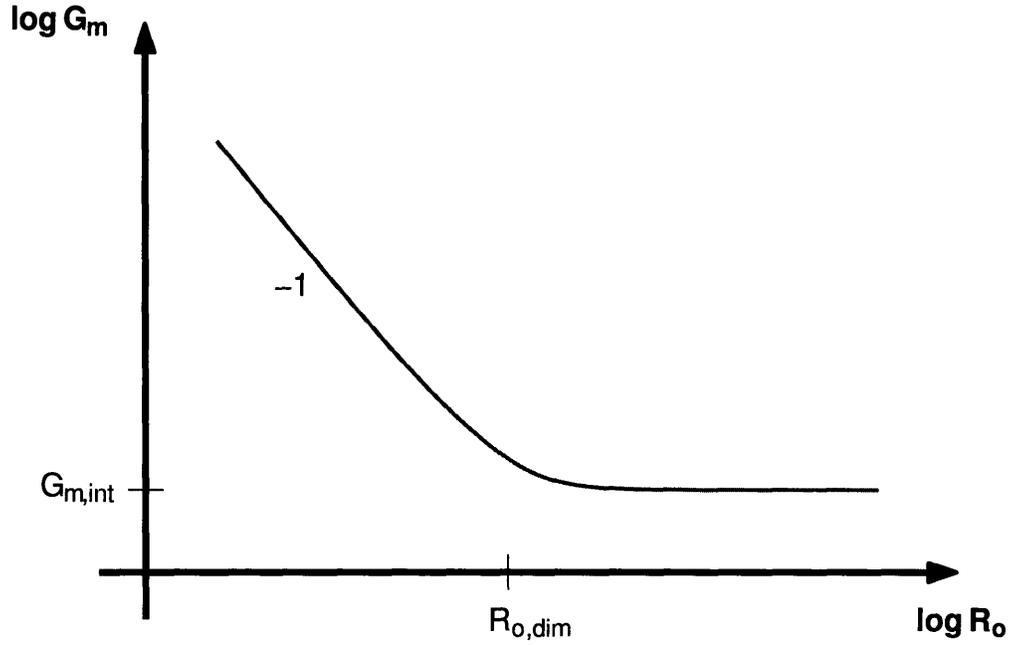


Figure 4-8: Required preamplifier transconductance versus output resistance for constant noise, speed and linearity requirements. Minimum transconductance ($G_{m,int}$) design is an ideal integrator ($R_o \gg R_{o,dim}$).

sistance equivalently large and small x is

$$C_i = \begin{cases} \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{v_n^2} \right) \left(\frac{V_{ovx}}{V_M} \right) & t_i \ll \tau_o \quad (4.20a) \\ \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{v_n^2} \right) \left(\frac{V_{ovx}}{V_M} \right) & t_i \gg \tau_o \quad (4.20b) \end{cases}$$

which turn out to be identical as expected from Figure 4-6. Taking the derivative of (4.15) with respect to x and setting equal to zero, the minimum required capacitance versus x can be solve for numerically and is

$$\frac{C_i}{\max(C_i)} \approx 0.7443 \quad (4.21)$$

at $x \approx 2.209$. Therefore, the minimum capacitance point is near $t_i = 2\tau_o$, the significance of which is explained below.

Assuming the preamplifier is an ideal integrator, the speed of the preamplifier is

$$\frac{G_m}{C_i} = 2(2mf_s) \left(\frac{V_M}{V_{ovx}} \right) \quad t_i \ll \tau_o \quad (4.22a)$$

which is independent of the output resistance (Figure 4-7). For the case of a wide-bandwidth preamplifier, the required speed is

$$\frac{G_m}{C_i} = \frac{1}{R_o C_i} \left(\frac{V_M}{V_{ovx}} \right) \quad t_i \gg \tau_o \quad (4.22b)$$

which is inversely proportional to R_o . The point at which these two limiting cases intersect is $t_i = 2\tau_o$. The output resistance at this point is

$$R_{o,dim} = \frac{1}{4mf_s C_{i,int}} \quad (4.23)$$

where $C_{i,int}$ is the capacitance required for an integrator (4.20a). The point where $t_i = 2\tau_o$ represents a point of diminishing return. For output resistances below $R_{o,dim}$, an increase in R_o yields a proportional improvement in speed, but the speed approaches a minimum for output resistance greater than $R_{o,dim}$.

The point of diminishing return also carries over into the required transconductance for a given noise and speed requirement. The limiting behavior for the transconductance (4.18) is

$$G_m = \begin{cases} 2(2mf_s) \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{v_n^2} \right) & t_i \ll \tau_o \\ \frac{1}{R_o} \left(\frac{V_M}{V_{ovx}} \right) & t_i \gg \tau_o \end{cases} \quad (4.24a)$$

$$\quad (4.24b)$$

where the transconductance approaches its minimum value

$$G_{m,int} = 2(2mf_s) \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{v_n^2} \right) \quad (4.25)$$

when the preamplifier becomes an ideal integrator and is inversely proportional to R_o

for a wide bandwidth preamplifier (Figure 4-8). The intersection of these two limiting equations is the same $R_{o,dim}$ as above which occurs when $t_i = 2\tau_o$.

Because $t_i = 2\tau_o$ represents the point of diminishing return for increasing R_o , it is useful to quantify how much additional transconductance savings can be obtained in the limit of infinite output resistance. Assuming $t_i = 2\tau_o$ and $R_o = R_{o,dim}$, the required transconductance from (4.18) with $x = 2$ is

$$G_{m,dim} = G_{m,int} \coth(1) \approx 1.313 G_{m,int} \quad (4.26)$$

where $G_{m,int}$ is defined in (4.25). Therefore, the additional transconductance savings from increasing R_o beyond $R_{o,dim}$ is less than 25 %.

The final conclusion from this discussion is that it is not efficient to force the use of a wide-bandwidth preamplifier that has time to settle to many time constants. It should be noted that the preamplifier design procedure presented does not consider the impact of other noise sources in the CBSC charge transfer. The role of the preamplifier noise in the CBSC gain stage is addressed in Chapter 6.

4.2.4 Threshold Detection

The actual threshold detection is also an important part of the overall threshold comparator design. Ultimately, small differential inputs must generate rail-to-rail or near rail-to-rail outputs in a short amount of time. If care is not used in the design, the threshold detection circuit can consume more power than the preamplifier. In theory, the only required power consumption for threshold detection is the CV^2f power to charge and discharge the node capacitances. Comments are made on possible threshold comparator implementations. The actual threshold comparator used in the prototype is described in Chapter 5. Finally, differences in the requirements of a threshold comparator for CBSC are enumerated pointing output potential ideas to explore in future CBSC comparator designs.

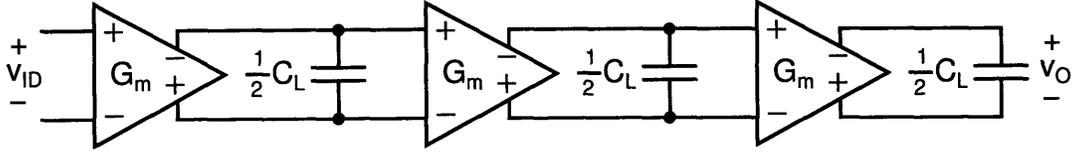


Figure 4-9: Cascade of three amplifier stages.

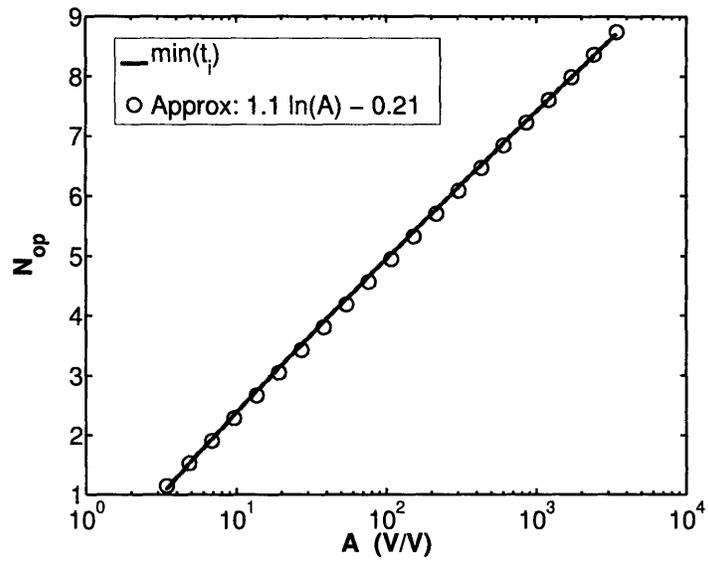
Cascaded Amplifiers

The simplest implementation of a threshold comparator is to use an open-loop amplifier with high gain and a wide bandwidth [40] [44] [41]. This was the model assumed when the argument was made to use a band-limiting preamplifier in front of the threshold comparator. Again, assuming that the threshold comparator is reset between decisions, what is actually important for a fast response is not the actual bandwidth, but the unity gain frequency G_m/C_L [42]. The argument for a band-limiting preamplifier also holds for threshold comparator stages.

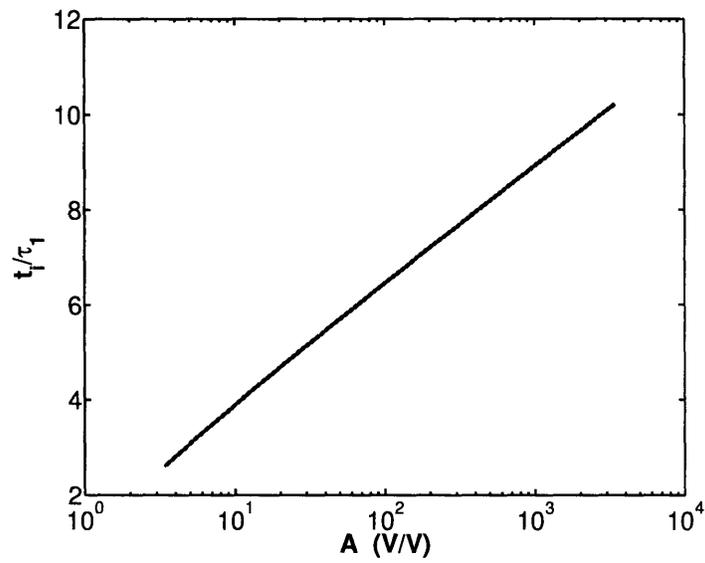
An optimum design strategy has been considered for preamplifiers in clocked comparators [45] that minimizes the delay of a cascade of N identical, ideal band-limiting amplifiers for a step input. It is assumed that the transconductance amplifiers all start from a state such that they immediately respond to changes in their inputs, and the transconductance amplifiers have no slew-rate limitations. Given the G_m/C_L of the amplifiers, the design specifies the optimum number of stages to minimize the delay for a required gain, where the gain is the ratio of the required output voltage to the step input size. It is possible to duplicate this analysis for step ramp inputs. The output voltage response for a step ramp input $v_{ID}(t) = Mt u(t)$ is

$$v_O(t) = \frac{1}{(N+1)!} (M\tau_1) \left(\frac{t}{\tau_1}\right)^{N+1} \quad (4.27)$$

where M is the input ramp rate, $\tau_1 = C_L/G_m$ is the unity gain time constant for the amplifier, and N is the number of stages. The response time t_i it takes the cascade



(a)



(b)

Figure 4-10: Optimum cascade of amplifiers. (a) Optimum number of stages N_{op} versus the required gain A for minimum response time t_i . Approximation that the gain is a linear function of the natural logarithm of the required gain [45]. (b) Relative delay (t_i/τ_1) versus required gain A assuming the optimum number of stages N_{op} is used.

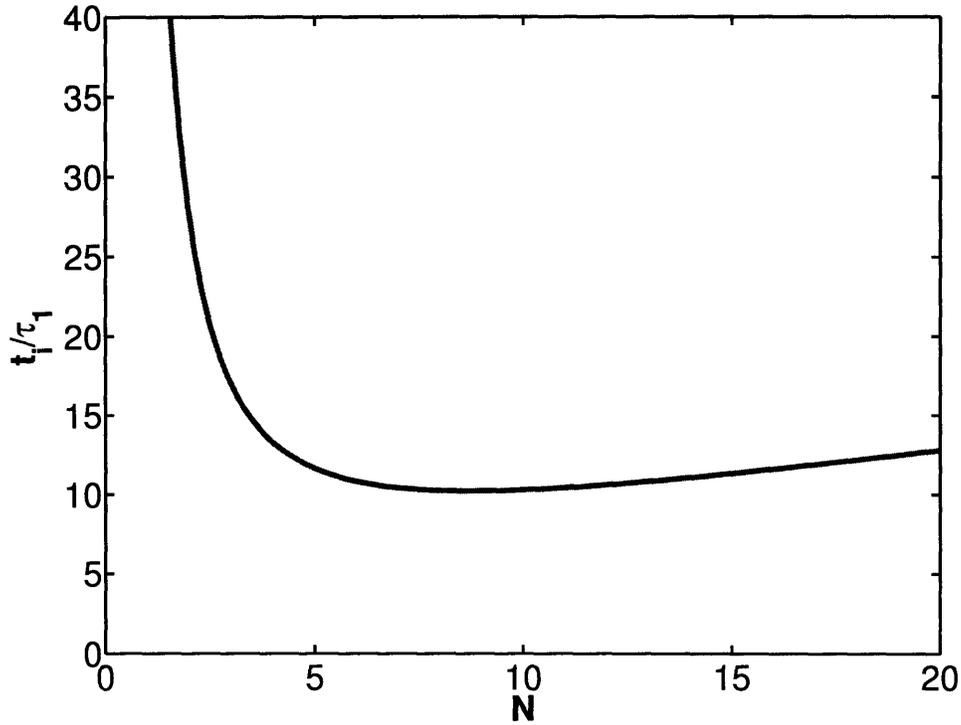


Figure 4-11: Relative delay versus number of stages for a given gain requirement A .

of amplifiers to reach the output threshold V_M is

$$t_i = \tau_1 \left[A(N+1)! \right]^{\frac{1}{N+1}} \quad (4.28)$$

where $A = V_M/(M\tau_1)$ is required gain. The optimum number of stages versus required gain is plotted in Figure 4-10(a) along with a rough approximation for the optimum number of stages [45]

$$N_{op} \approx 1.1 \ln(A) - 0.21. \quad (4.29)$$

Figure 4-10(b) shows a plot of the relative response time t_i/τ_1 versus the required gain A assuming the optimum number of stages N_{op} is used.

However, the suggested optimum number of stages is rather large and has a broad minimum as shown in Figure 4-11. Only a small penalty in terms of delay is paid for significantly reducing the number of stages used and the amount the power consump-

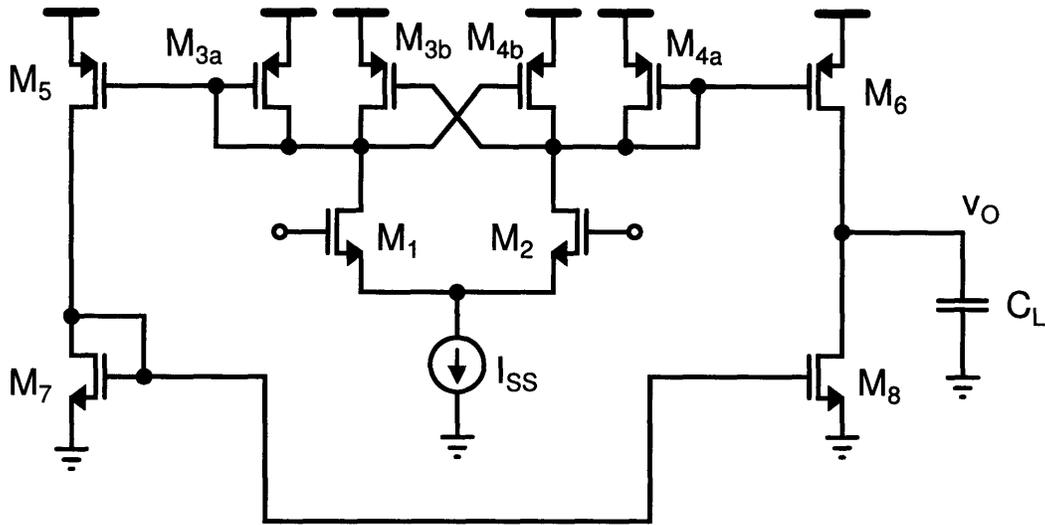


Figure 4-12: Current mirror op-amp as a comparator.

tion. For example, in Figure 4-11, the optimum number of stages is approximately 8, and the relative delay is 10. If the number of stages is halved to 4, the relative delay is only increased to roughly 13, but the power consumption is halved.

While a cascade of differential amplifiers can be used to generate output decisions with several hundred millivolts of voltage swing, it is not amenable to the generation of rail-to-rail signals needed to control CMOS logic and sampling switches.

Current Mirror Op-amp

A simple single stage implementation of a threshold comparator is the current mirror op-amp [40] [41] shown in Figure 4-12. The cross-coupled transistors M_{3b} and M_{4b} serve two important purposes. First, they speed up the completion of the decision at the output of the differential amplifier. If they are not present, the transient operation is slow because transistors M_{3a} or M_{4a} enter weak inversion and do not shut off M_5 or M_6 quickly. The second purpose is that the cross coupled devices can be used to add a small amount of hysteresis to the comparator.

Two important design issues exist for this comparator topology. The first is the trade-off between output slew rate and static power dissipation and the second is the

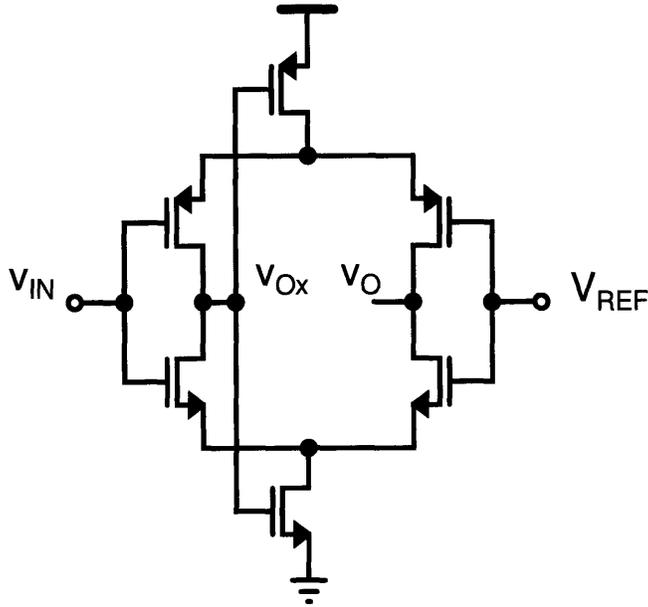


Figure 4-13: Bazes comparator based on a self-biased differential amplifier.

asymmetry in the design.

Because the current mirror op-amp essentially just steers the tail current I_{SS} to charge or discharge the load capacitance, its output slew rate trades off linearly with the amount of static power dissipation. For example, the current required to charge 5 fF from 0 to 1.8 V with a 100 ps rise time is 90 μ A. The situation is problematic since the jitter in the output decision is a function of the output slew rate.

The other problem is the asymmetry of the amplifier and the slow transient in shutting off transistor M_7 . Because the pull-up and pull-down paths are different, the response of the amplifier is different depending on the direction of the decision. Pull-down transitions are fast because the cross-coupled device turns off M_6 quickly and allows transistor M_8 to discharge C_L unopposed. However, for the pull-up transition, the transistor M_6 turns on quickly, but it has to supply the current being sunk by M_8 during the slow turn off of transistor M_7 .

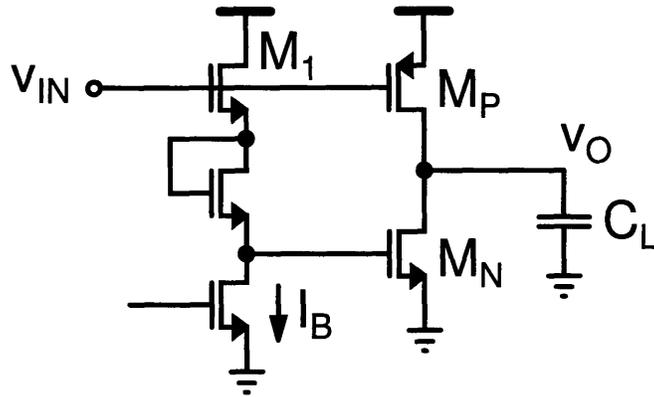


Figure 4-14: Inverter with split NMOS and PMOS drive. A source follower is used as a DC level shifter to drive the NMOS device.

Bazes Comparator

An interesting idea that can break the link between the static power consumed to the output slew rate is the self-biased CMOS differential amplifier [46] shown in Figure 4-13. This differential amplifier has a bias current that behaves similar to an inverter. For large differential inputs, the amplifier draws little or no static current, and draws large amounts of current when the differential input is near zero. This situation is the exact opposite of a Class AB differential amplifier that has a larger bias current for large differential inputs to address slew rate limitations in op-amp settling.

The comparator shown is not fully differential because it has a singled-ended output. A fully-differential implementation has been proposed [47]. These comparators require a common-mode input voltage near $V_{DD}/2$, but they are not suited to be a single stage comparator for CBSC because of the large current draw for a zero differential input. This comparator design could work well for later stages to turn a low swing differential signal into a rail-to-rail signal, but the output of the differential preamplifiers would require a common-mode level shift.

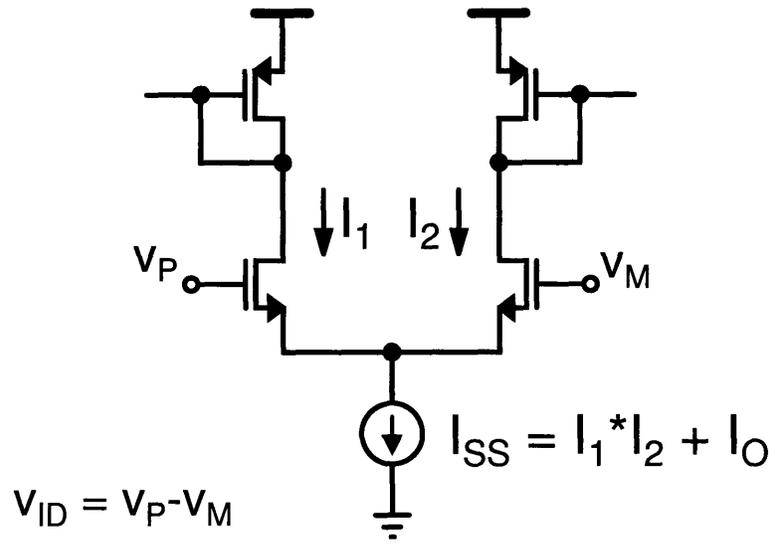
Inverter-Based Level Converter

From the discussion of the previous comparator designs, it is clear that a circuit with a high slew rate but low static power consumption is required. An inverter meets these requirements, but requires a near rail-to-rail input that is centered around $V_{DD}/2$. Assuming at least one stage of differential amplification with an output voltage that swings from the positive rail down to about mid-rail, the single-ended circuit shown in Figure 4-14 can convert the signal into to a rail-to-rail signal. Because the circuit is based on an inverter, it has a large dynamic current available for generating fast edge rates, but it only draws static power in the source follower. The input capacitance of the source follower is relatively small, approximately C_{gd} of M_1 . The static bias current of the follower can be relatively small because it only drives a minimum sized NMOS device and its internal parasitics.

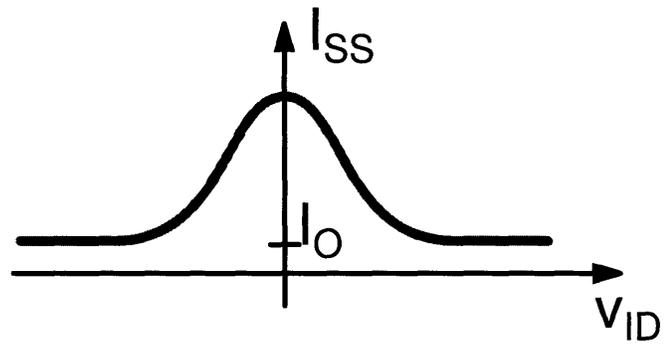
Although this design has a fairly good dynamic to static power consumption ratio, it still consumes static power. In addition, the minimum size inverter driven with a half V_{DD} drive limits the output slew rate to some extent. Finally, the minimum sized inverter can not drive very large capacitive loads, and buffering the logic output with a series of inverters adds to the total comparator delay.

Adaptively Biased Differential Amplifier

The final threshold comparator circuit idea to be discussed is to apply the idea of a larger current for zero differential input to an adaptively biased differential amplifier. A simplified schematic is shown in Figure 4-15. The tail current is the product of the current in each leg of the differential amplifier plus a small static current ($I_{ss} = I_1 * I_2 + I_O$). This circuit is a simple extension of the more common Class AB like adaptive bias where $I_{SS} = I_1 - I_2 + I_O$ [48]. One possible method of obtaining the product of the currents I_1 and I_2 is to use translinear circuits techniques [49]. The challenges are getting a large ratio between $I_1 I_2$ and I_O , and implementing a fast and efficient multiplier for $I_1 I_2$.



(a)



(b)

Figure 4-15: Adaptively biased differential amplifier. (a) Simplified schematic. (b) Required bias current variation. When $v_{ID} = 0$, $I_1 = I_2$.

Threshold Detection for CBSC

In comparator-based switched-capacitor circuits, the threshold detection comparator does not need to meet all the requirements of a traditional threshold detection comparator. Removal of these constraints should allow for more design flexibility and improved efficiency. Three key differences in CBSC systems are that the direction of each decision is known, each decision has different speed and accuracy requirements, and the comparator can be reset or reconfigured between decisions.

First, because the direction of each decision is known, the design can be optimized for one direction, and an asymmetric circuit could be used. For example, a circuit with asymmetric positive feedback that has a weak pull-up device that must be overcome but enables a strong pull-down device that never has to be overcome by the weak pull-up is possible.

Second, because each decision has different speed and accuracy requirements, it is possible to either reconfigure the comparator between stages to vary speed and accuracy or use different comparators for each decision. For example, one simple modification would be to change the preamplifier load capacitance C_i between the coarse and fine charge transfer phase decision. A small C_i during the coarse phase allows for a fast but noisy decision, and a large C_i during the fine phase allows for a slower but lower noise decision.

Finally, a general purpose comparator must be able to make decisions in either direction and be able to recover quickly after making a decision, but because the comparator can be reset or reconfigured between decisions in CBSC, the comparator does not need to be designed for fast recovery. The state of the comparator can either be reset with switches between decisions or a different comparator can be used.

The proof of concept pipeline ADC did not take advantage of the unique requirements of a CBSC virtual ground threshold detection comparator. Future work should explore the possibility of exploiting these differences.

4.3 Summary

The specifications of threshold detection comparators have been described, and their operation contrasted with that of the more common clocked comparator. The non-stationary noise analysis techniques from Chapter 3 were used as the basis for a discussion on low noise threshold comparator design. It was found that it is advantageous to band-limit the preamplifier to improve both its speed and noise performance at a given power consumption. A set of simplified design equations for the preamplifier were derived. The capacitance required for a given noise performance requirement was found to be relatively independent of whether the preamplifier was severely band-limited or not. The difference is that the band-limited design can be made to consume less power while operating at the same speed. Finally, the issues related to the design of the actual threshold comparator were briefly discussed concluding with a summary of the potential design flexibility for virtual ground threshold detection comparators in comparator-based switched-capacitor circuits.

Chapter 5

CBSC Prototype Pipeline ADC

5.1 Overview

Although the CBSC technique is a general approach that can be applied to most switched-capacitor circuits, for the demonstration of the concept, a prototype pipeline ADC was constructed [50] [15]. A brief description of the overall pipeline ADC is given. The details of the bit-decision comparator and the threshold comparator used in the prototype are emphasized. The experimental results from the prototype converter are presented along with comments on testing procedures and equipment.

5.2 1.5-bit/stage CBSC Pipelined ADC

A schematic of the first two stages of the prototype pipeline ADC is shown in Figure 5-1. To simplify the design of the prototype, a single-ended circuit design was used as shown. A fully-differential design should be possible, but it would require the design of a common-mode feedback circuit to equalize the differential pull-up and pull-down currents. The pipeline was implemented as a cascade of identical stages with sampling capacitors $C_s = C_{1a} + C_{1b} = 500$ fF. No threshold comparator sharing between adjacent stages or comparator duty-cycling for lower power consumption was performed. The system clock directly controls the sampling and bit decision timing of

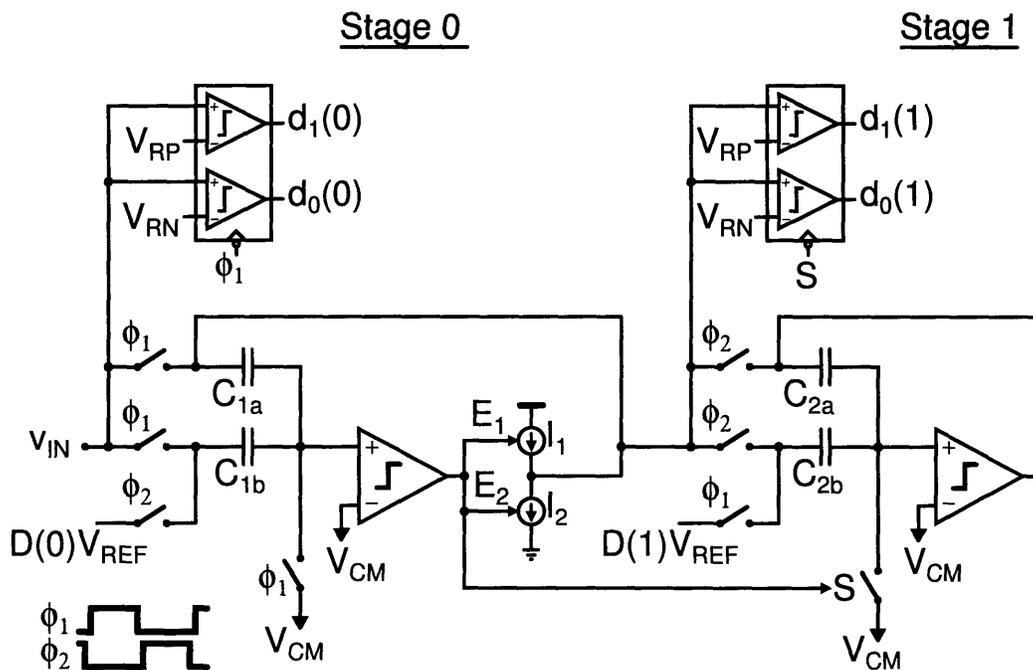


Figure 5-1: First two stages of Pipeline ADC. Note that the first stage sampling and bit-decision clocking are controlled by the system clock, but for the second and subsequent stages, the sampling and bit-decision clocking are controlled by the comparator of the previous stage.

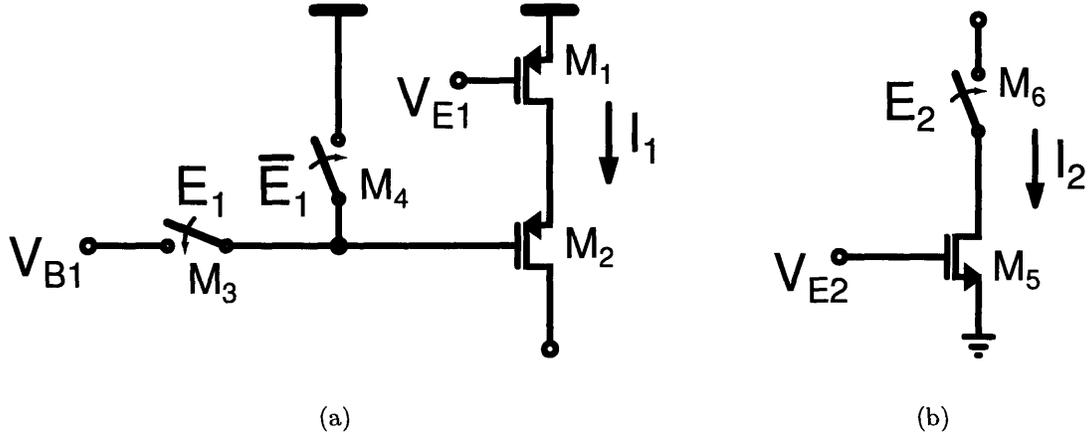


Figure 5-2: Coarse and fine phase current sources. Bias voltage generation not shown. (a) Coarse phase current source $I_1 = 70 \mu\text{A}$. (b) Fine phase current source $I_2 = 3 \mu\text{A}$.

the first stage of the pipeline, but the previous stage comparator decision controls the sampling and bit decision timing for the second and subsequent stages. However, the overall pipeline process is not self-timed. The operation of each stage of the pipeline operates under the control of the system clock. The circuits used to implement the coarse and fine charging current sources, the bit-decision comparators, and the virtual ground threshold detection comparator are described below.

5.2.1 Charging Current Sources

To allow for the majority of the coarse phase overshoot to be canceled as discussed in Chapter 2, a constant ramp rate for the coarse charge transfer phase is required across the full-scale output range. One straightforward method of reducing the ramp rate variation is to use a cascoded current source. Therefore, the coarse phase charging current source I_1 was implemented as a cascoded PMOS current source (M_1, M_2) as shown in Figure 5-2(a), where the bias voltage on the cascode device is used to turn on (M_3) and off (M_4) the current source. For lower supply voltage operation, alternative methods of keeping the ramp rate constant are required.

Because the fine phase current is more than an order of magnitude lower than the

coarse phase charging current ($70\ \mu\text{A}/3\ \mu\text{A}$), the output resistance of a single device of the same length should also be an order of magnitude larger. According to the simulation models used at design time, the output resistance of a single device would be adequate to keep the fine phase overshoot variation small enough for 10 b linearity. Therefore, the fine phase current source I_2 was implemented as a single transistor current source (M_5) as shown in Figure 5-2(b), where a series NMOS switched (M_6) was used to turned on and off the current source. It was later realized that the series switch (M_6) behaves like a cascode device at the high end of the full-scale range. The large increase in output resistance at the high end of the output range results in a signal dependent overshoot and ultimately INL in the ADC transfer characteristic.

5.2.2 Bit Decision Comparators

The two bit-decision comparators shown in Figure 5-1 are traditional latch-based clocked comparators. At the falling edge of ϕ_1 or S , these comparators determine if their inputs are greater than or less than the two reference voltages V_{RP} and V_{RN} according to the 1.5 b/stage algorithm [51] [52]. The core of the bit-decision comparator is the latch circuit shown in Figure 5-3(b). The latch used in Figure 5-3(b) is a slight modification of the well-known cross-coupled inverter latch [53] shown in Figure 5-3(a). The reason for splitting the transistor M_P into two separate devices with their drains not connected is to minimize signal dependent current required at the input of the latch during the charge transfer phase.

Consider the traditional latch in Figure 5-3(a), the reference voltage V_{REF} is somewhere near the middle of the supply range, and the input v_{IN} is always pulled to $V_{SS} = 0$ during preset. At the beginning of the charge transfer phase, the transistors M_2 and M_3 are off and transistors M_4 and M_1 are on. Therefore, the drain of M_N starts at V_{SS} and the drain of M_P (node X) starts at V_{REF} . As the input voltage ramps up during the charge transfer phase, transistor M_1 turns off when $v_{IN} \geq V_{REF} - V_{TN}$, and transistor M_4 turns off when $v_{IN} \geq V_{REF} - V_{TP}$. However, when $v_{IN} \geq V_{REF} + V_{TP}$, transistor M_3 turns on with node A acting as the source

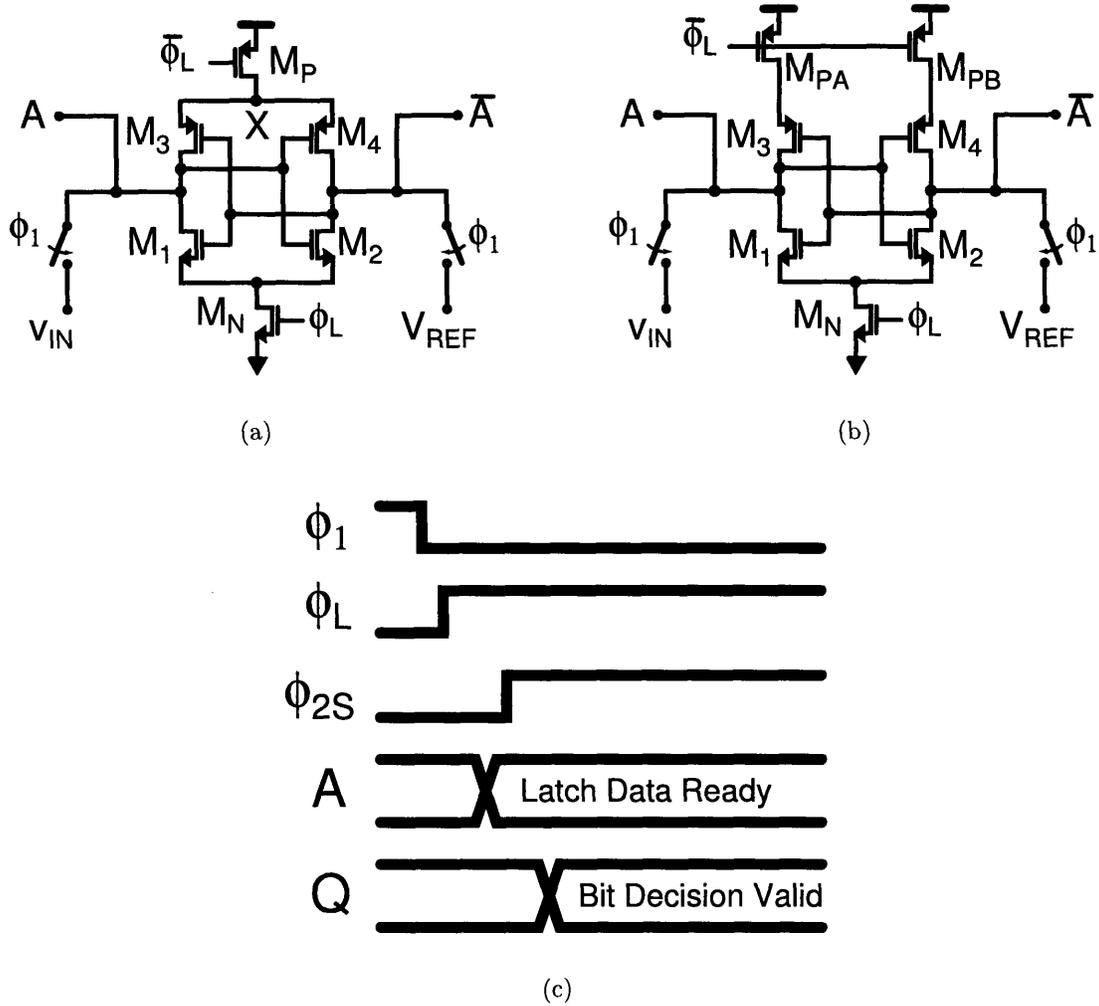


Figure 5-3: Bit decision comparators. (a) Typical cross-coupled inverter based clocked latch. (b) Cross-coupled inverter based clock latch used in prototype. Addresses the problem of having to charge node X at the drain of M_P . (c) Latch timing diagram.

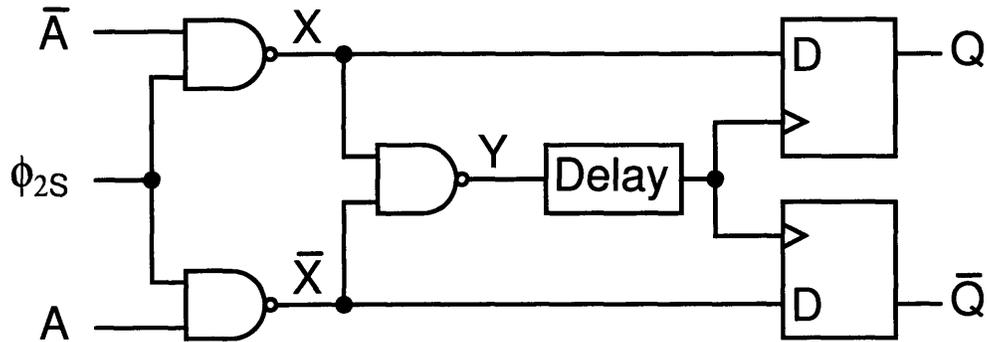


Figure 5-4: Bit decision comparator data valid and storage registers.

terminal because the gate of M_3 is at V_{REF} and the input voltage pulls node A a threshold voltage above V_{REF} . When M_3 turns on, more current is needed from the input to charge the capacitance at node X from V_{REF} to $V_{REF} + V_{TP}$. This large change in the input current causes ramp variation at the output of the CBSC gain stage, which can cause non-linearity in the overshoot.

The modified latch in Figure 5-3(b) eliminates this problem because the drain of transistor M_{PA} is discharged to $V_{REF} + V_{TP}$ during preset, which is exactly the voltage at where transistor M_3 turns on. However, the extra drain and source capacitance of transistors M_{PA} and M_3 still become visible to the input when $v_{IN} \geq V_{REF} + V_{TP}$. If less ramp variation is needed, alternative comparator designs could be used.

An additional consideration for the design of the latch is the trade-off between input referred offset and speed. The matching between the two inverters determines the input referred offset of the latch. The offset requirement for a pipeline converter using the 1.5 b/stage algorithm is greatly reduced [51] [52], but longer devices can be used to improve the input referred offset if required. However, the speed of the latch is reduced and the input capacitance is increased.

The additional supporting circuitry for the bit-decision comparators is shown in Figure 5-4. A fixed set of inverter delays are used to self-time the enable signal ϕ_{2S} on the output decision circuit. The rest of the logic detects when the comparator has made a valid decision (Y) and stores the bit decisions in static D-type flip-flops (DFF) [54].

5.2.3 Virtual Ground Threshold Detection Comparator

In contrast to the bit-decision comparators that make a magnitude decision at a specific instant in time, the virtual ground threshold detection comparator must determine the time at which the node v_X equals V_{CM} . The schematic of the threshold detection comparator used in the prototype is shown in Figure 5-5. Following the discussion in Chapter 4, the threshold comparator can be thought of as a band-limiting preamplifier stage followed by a broad-band amplifier cascade plus level shifter.

The band-limiting preamplifier was implemented as a differential amplifier with active loads. The output is clamped with back-to-back diode connected NMOS transistors. The clamp devices provide an effective reset state for the output between decisions and keeps all devices in their active regions to minimize recovery time. The details of the preamplifier with a continuous-time common-mode feedback circuit is shown in Figure 5-6 [55]. The tail current for the preamplifier is nominally $16\ \mu\text{A}$. To maximize the unity gain frequency of the preamplifier, the input devices use short gate lengths $W_1/L_1 = 3.2\ \mu\text{m}/0.26\ \mu\text{m}$. From simulations including parasitic extraction, the preamplifier has a transconductance (G_m) of $166\ \mu\text{S}$, an output resistance of $130\ \text{k}\Omega$, and an equivalent load capacitance (C_i) of $25\ \text{fF}$.

The two low-swing gain stages are differential amplifiers with resistive loads where the resistors were implemented using triode PMOS devices with their gates tied to V_{SS} . The nonlinearity introduced from using triode devices as loads is unimportant for comparator amplifier stages. The single-ended output swing of the low-swing gain stages is roughly $400\ \text{mV}$, and it is DC level shifted down with a diode connected PMOS device. The DC level shift allows the final gain stage, which also has triode PMOS loads, to have a larger swing while still keeping its differential input devices in saturation. Each half of the final gain stage swings about half the supply voltage ($900\ \text{mV}$) and is converted to a rail-to-rail signal with the inverter based level converter shown in Figure 5-5. One advantage of the level converter shown is that because it is based on an inverter, it has a peak transition current that is significantly larger than the static current $I_{B4} = 5\ \mu\text{A}$ in the source follower as discussed in Chapter 4. This

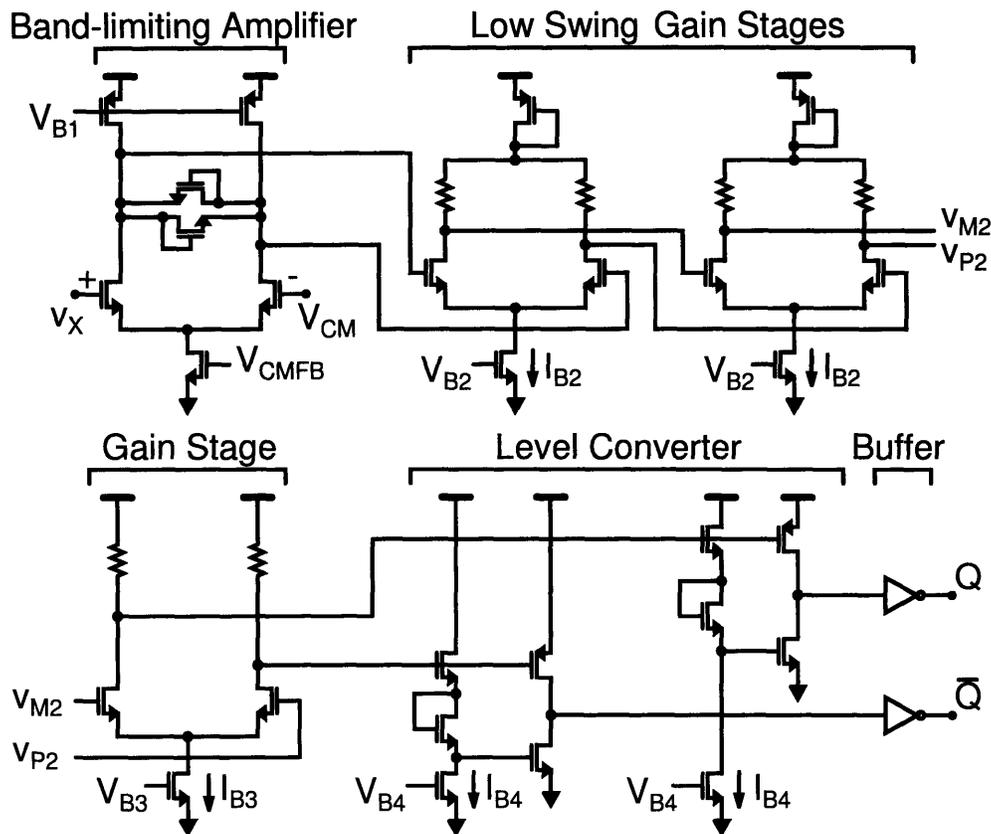


Figure 5-5: Schematic of prototype threshold-detection comparator with band-limiting preamplifier. The total parasitic capacitance at the output of the band-limiting amplifier determines the bandwidth. Resistors shown in the schematic are implemented as PMOS devices with grounded gates operating in the triode region. Each comparator has a power consumption of roughly $200 \mu\text{W}$.

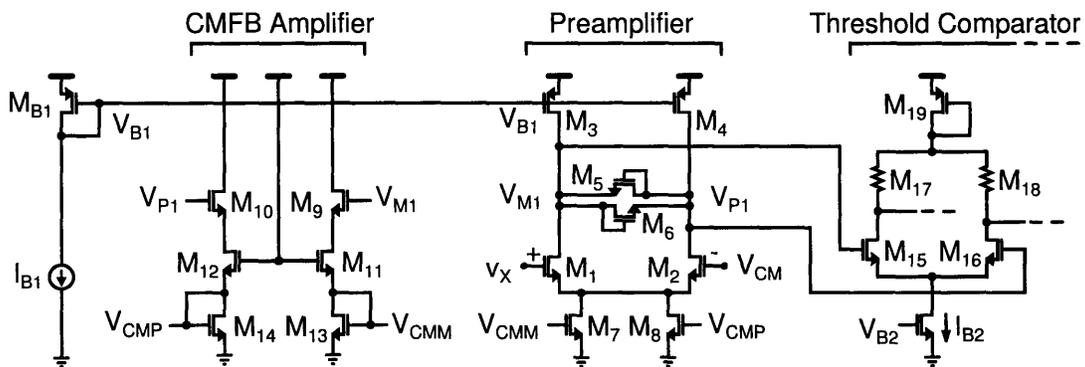


Figure 5-6: More detailed schematic of comparator preamplifier for prototype showing the common-mode feedback circuit.

Bias Current	Value
$I_{M14} + I_{M15}$	$16 \mu\text{A}$
$I_{M7} + I_{M8}$	$16 \mu\text{A}$
I_{B2}	$13 \mu\text{A}$
I_{B3}	$24 \mu\text{A}$
I_{B4}	$5 \mu\text{A}$
Total Static Bias	$92 \mu\text{A}$

Table 5.1: Threshold-detection comparator static bias currents.

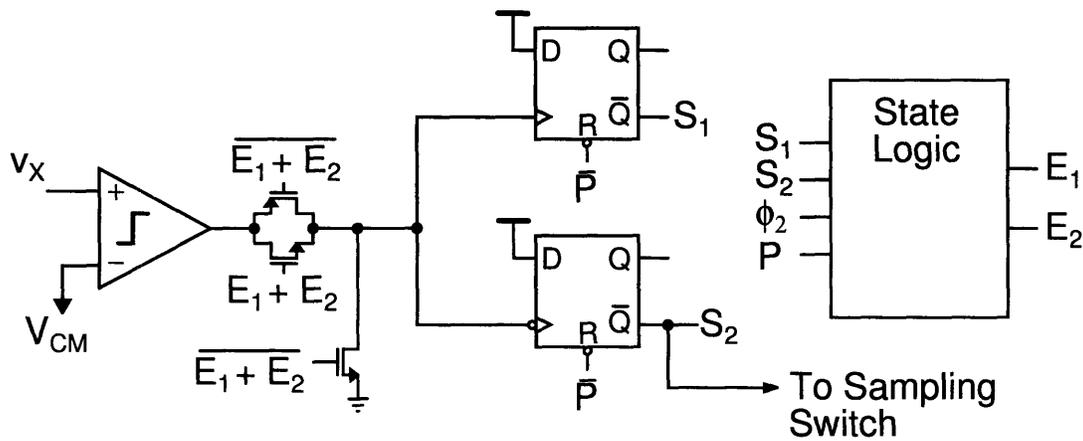


Figure 5-7: Current source and sampling logic and CBSC state machine.

behavior allows for fast rise/fall times resulting in lower jitter sensitivity in the later stages of the comparator. Table 5.1 gives the bias currents for the different stages.

5.2.4 CBSC State Machine

A finite state machine is used to control the coarse and fine charge transfer phase operation as shown in Figure 5-7. The state machine consists of two fully static DFFs [54] and some combinational state logic to generate the control signals E_1 and E_2 from the current state and the system clock.

During the sampling and preset phases, the clock inputs to the DFFs are disconnected from the comparator output and held low. During the preset phase, the DFFs are reset, which sets their \bar{Q} outputs high. Therefore, the signal S_2 is high and the

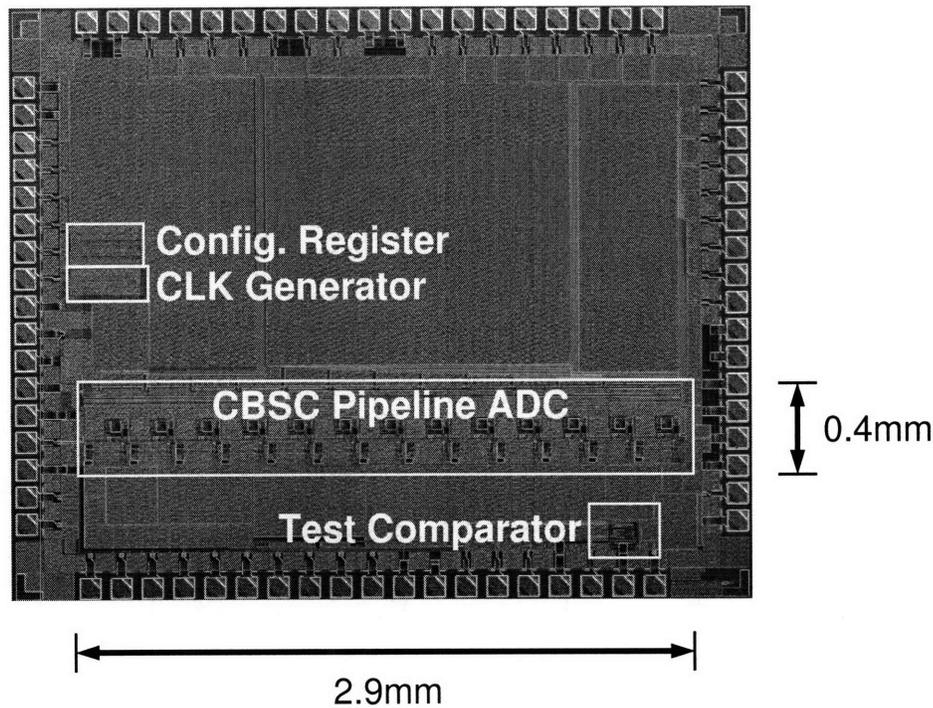


Figure 5-8: Die photograph. 0.18 μm CMOS process. Pipeline Area: 1.2 mm^2 .

sampling switch is closed during preset.

During the charge transfer phases E_1 and E_2 , the output of the comparator is connected to the clock input of the DFFs. When the comparator input makes its first decision for the coarse charge transfer phase, the signal S_1 falls low. The state logic then shuts off the coarse phase charging current I_1 and turns on the fine phase current I_2 . Upon the fine phase threshold crossing decision, the signal S_2 falls low and opens the sampling switch. The signal E_2 falls low after the state logic propagation delay.

5.2.5 Prototype Test Chip

A die micrograph of the prototype pipeline ADC is shown in Figure 5-8. The prototype was fabricated in a 0.18 μm CMOS process. All the bit decision for the 12 pipeline stages are sent off chip for post-processing. For the ADC performance data in this chapter, the output was truncated to 10 bits, but 12 bits of output were used for the noise characterization of the pipeline in order to reduce the effect of quantization

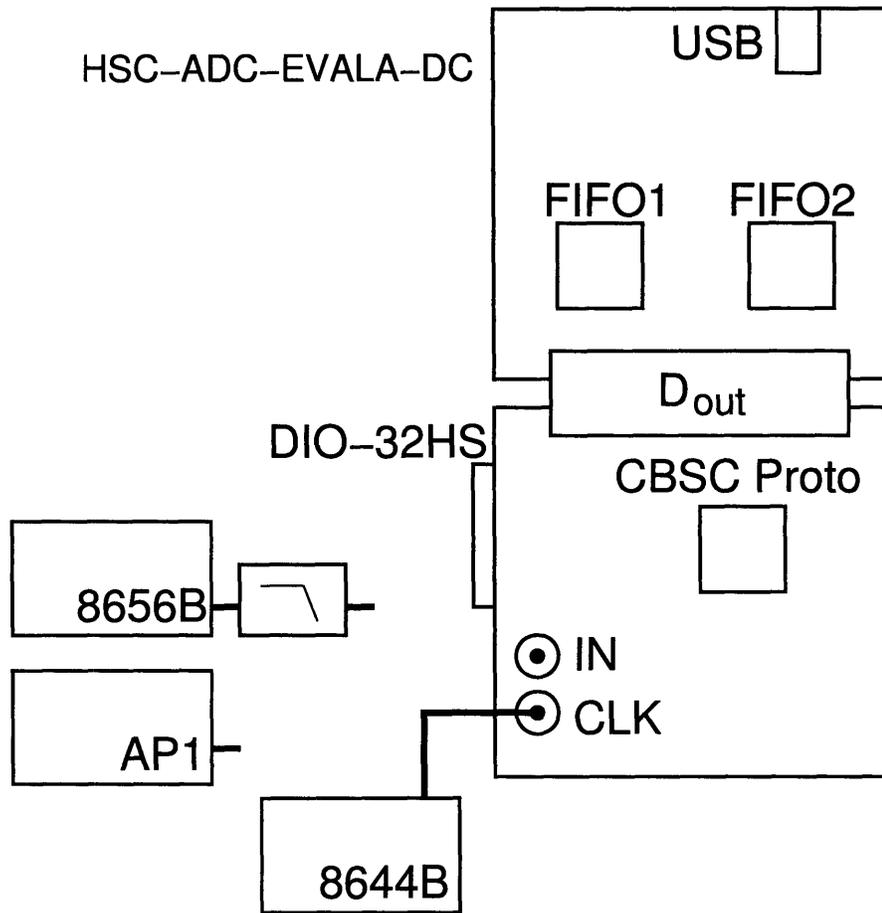


Figure 5-9: Simplified diagram of the prototype test setup.

noise. The prototype had an on-chip non-overlapping clock generator to generate all the required timing edges from a single input reference clock. The relative timing of the clock edges was controllable through a 32 b serial configuration register. All comparator bias currents and the coarse and fine phase currents were applied externally for maximum testing flexibility. The reference voltages for the ADC were also generated off chip [43].

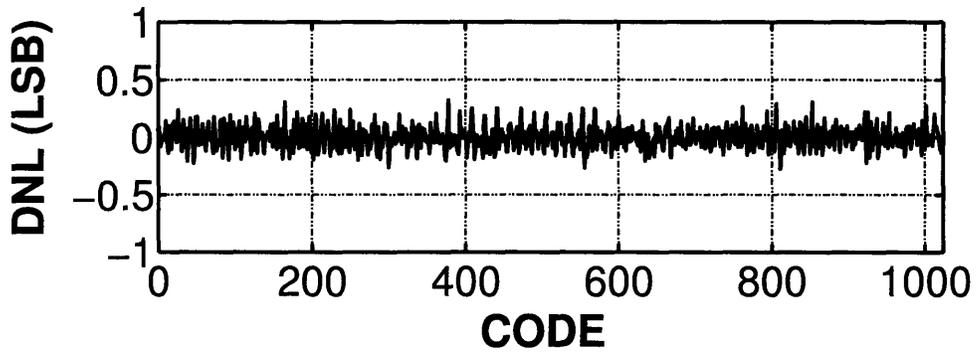
5.3 Experimental Results

Measured results of the prototype pipeline ADC are presented. Testing results are reported in accordance with the IEEE standards on ADC test methods [56].

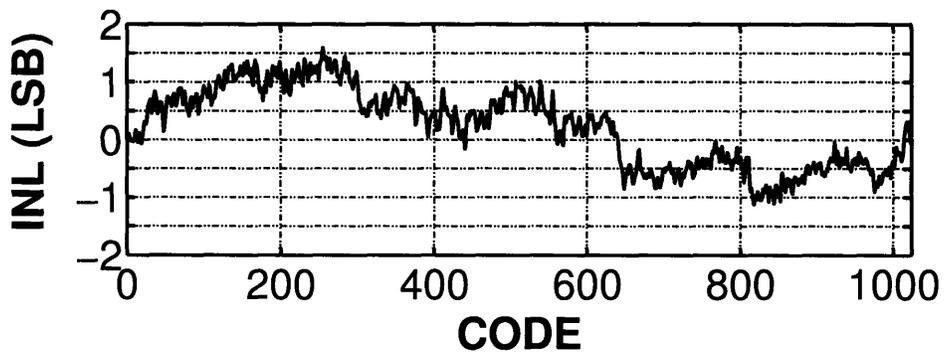
A simplified diagram of the test setup is shown in Figure 5-9. The Agilent 8644B signal generator was used to supply the reference clock for the prototype. The output data from the prototype converter could be acquired using either the HSC-ADC-EVALA-DC data acquisition board from ADI with 256 kS deep FIFOs (IDT-72V2113) or the TLA715 logic analyzer. The data acquisition board has a USB interface and comes with a driver and software to control the board. Labview was used to control a National Instruments PCI-DIO-32HS data acquisition board for programming the configuration register in the prototype to set timing options for the clock edges generated on chip. The DIO-32HS connects to the test board with a 68-pin cable and connector on the PCB.

The INL and DNL performance of the prototype converter operating at approximately a 7.9 MHz sampling rate are shown in Figure 5-10. The INL and DNL measurements were made using the sine wave histogram test [57] where the Audio Precision AP1 was used to generate the low frequency sine wave input. It is important to select the input and sampling frequencies such that exactly an integer number of periods are recorded and samples do not repeat periodically during the data record. This special selection of frequencies is often referred to as coherent sampling. A useful adaptation of this concept to testing with finite precision signal sources has been suggested in Maxim Application Note 3190 [58].

The FFT testing results for a single tone input are given in Figure 5-11 for an input frequency near $f_s/2$ and an input amplitude of -1 dBFS. The output of a HP8656B signal generator was low-pass filtered to provide a spectrally pure input sine wave for FFT testing. The filters used for testing were a series of low-pass filters from Mini-Circuits and TTE. All harmonic distortion components of the input sine wave should be at least 20 dB below the magnitude of the distortion components under investigation [56]. Again, the the input frequency and the sampling frequency should be selected according to coherent sampling requirements. For FFT testing, coherent sampling results in all signal and harmonic tones falling in their own FFT bins. The



(a)



(b)

Figure 5-10: ADC 10 b INL and DNL for a 7.9 MHz sampling frequency. (a) DNL. (b) INL.

FFT Test: $f_s = 7.9\text{MHz}$, $f_{in} = 3.8\text{MHz}$, $A_{in} = -1.0\text{dBFS}$

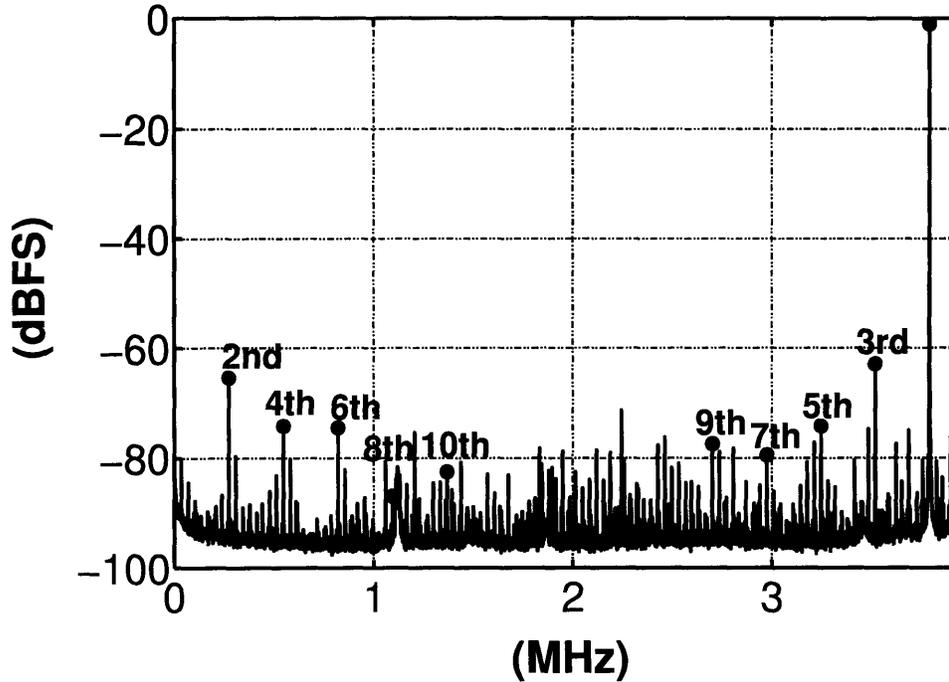


Figure 5-11: Output FFT for $f_s = 7.9\text{MHz}$ sampling rate and a -1dBFS input at $f_{in} = 3.8\text{MHz}$.

spectral plot shown is the average square magnitude of 60 FFTs of 2^{14} samples¹. The spectral averaging makes the higher-order low level distortion products visible in the FFT spectrum shown in Figure 5-11.

Figure 5-12 shows the signal-to-noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) versus input frequency f_{in} for the prototype. The SNDR performance is essentially constant up to the Nyquist rate ($f_s/2$). This result demonstrates that input sampling circuit was not limiting the linearity performance of the

¹Note: Equation (87) in [56] is incorrect. It should be [59]

$$X_{avm}[f_m] = \frac{1}{K} \sum_{k=1}^K |X[f_m]|^2. \quad (5.1)$$

FFT averaging and spectral estimation are discussed in more detail in Chapter 7.

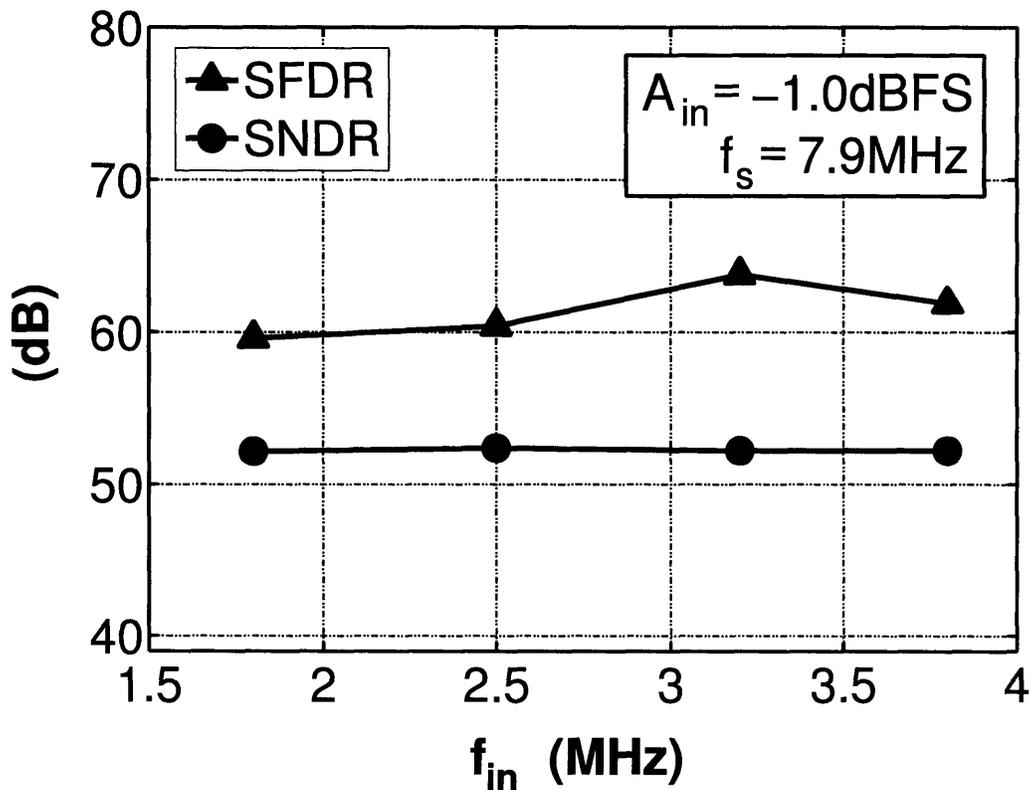


Figure 5-12: SNDR and SFDR versus input frequency.

prototype.

Recall that the SFDR is defined as the ratio between the largest harmonic component and the input tone. From Figure 5-12, the SFDR appears to improve with input frequency. However, variation in the SFDR performance versus input frequency is reasonable because the amplitude of the dominant harmonic component can vary versus input frequency due to the cancellation of competing effects for a single harmonic component.

Table 5.2 gives a summary of the performance of the prototype pipeline ADC. Operating at a 7.9 MHz sampling frequency, the converter achieves 8.6 effective bits of accuracy, and consumes 2.5 mW of power resulting in a 0.8 pJ/b figure of merit [60]. The 2.5 mW power consumption does not include the power consumption from the clock generation circuits or the pad drivers for the output bits. In addition, the time-

f_s	7.9 MHz
V_{FS}	1 V (single-ended)
DNL	+0.33/-0.28 LSB ₁₀
INL	+1.59/-1.13 LSB ₁₀
SFDR	62 dB
SNDR	52 dB
SNR	53 dB
ENOB	8.6 b
Power	2.5 mW
$\text{FOM} = \frac{P}{2f_{\text{in}} 2^{\text{ENOB}}}$	0.8 pJ/step

Table 5.2: ADC Performance Summary

alignment and 1.5 b/stage correction algorithm were also not implemented on-chip.

5.4 Summary

The circuits used in the implementation of the CBSC prototype pipeline ADC were described. Details of the bit decision and threshold detection comparators were emphasized. The bit decision comparator used was a slight modification of the standard cross-coupled inverter based latch to address the signal dependent load problem of the original design. The threshold detection comparator used in the prototype was described focusing on the preamplifier implementation. The basic test setup for the prototype was described, and measured results from the prototype were presented. The key results were summarized in Table 5.2.

Chapter 6

CBSC Noise Analysis

6.1 Overview

The noise analysis of a CBSC pipeline ADC stage is presented. The analysis is based on the prototype implementation described in Chapter 5. Noise from the virtual ground threshold detection comparator, the charging current, and the switches are analyzed separately. The results can then be combined with the noise from the input sampler to form a total input referred noise PSD estimate for the prototype. The theoretical estimate is compared with measured results in Chapter 7.

6.2 Total Input Referred Noise of Pipeline ADC

For the purposes of analyzing the input referred noise of the ADC, a single pipeline stage can be represented as a gain-of-two amplification shown in Figure 6-1 that resolves 1.5 effective bits [51]. The input referred noise of the i -th stage of residue calculation is $\overline{v_n^2(i)}$, and the noise in the residue calculation for the i -th stage does not affect the i -th stage bit decision.

The input referred noise PSD of the ADC can be measured by examining the output codes for a zero input signal, but the measured value also contains quantization noise from the ADC. Because the prototype pipeline was implemented as a cascade

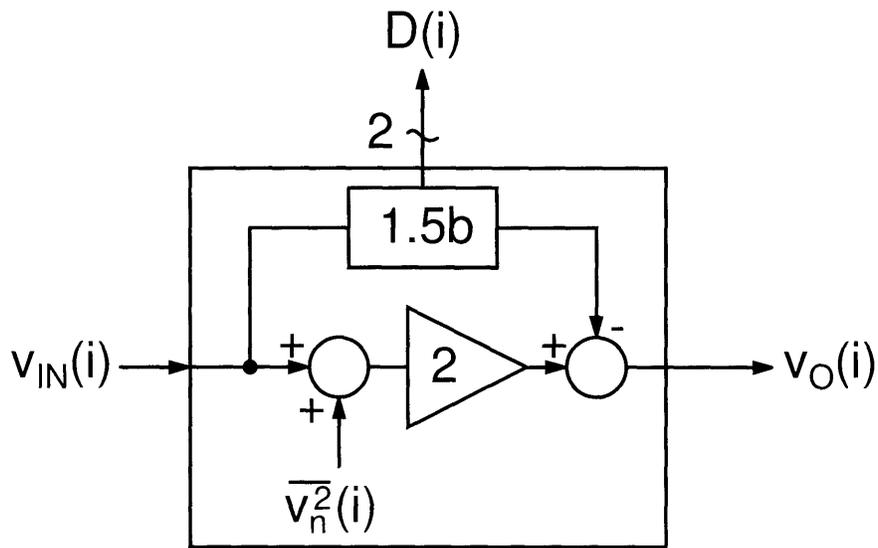


Figure 6-1: Single 1.5b/stage model for noise analysis.

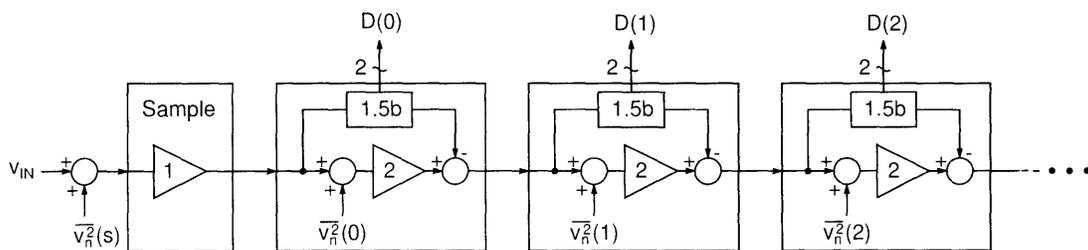


Figure 6-2: Pipeline ADC model noise model.

of identical stages, the total input referred noise from the residue amplifiers has a particularly simple form. Referring to Figure 6-2, the input referred noise PSD of an N -bit ADC due to noise in the residue calculations is

$$\begin{aligned}
 S_{n,ADC}(f) &= \frac{S_{n0}(f)}{1} + \frac{S_{n1}(f)}{2^2} + \dots + \frac{S_{n(N-2)}(f)}{2^{2(N-2)}} \\
 &= S_{n0}(f) \sum_{i=0}^{N-2} \left(\frac{1}{4}\right)^i \\
 S_{n,ADC}(f) &= \frac{4}{3} \left[1 - \left(\frac{1}{4}\right)^{N-1} \right] S_{n0}(f) \tag{6.1}
 \end{aligned}$$

$$S_{n,ADC}(f) \approx \frac{4}{3} S_{n0}(f) \tag{6.2}$$

where $S_{n0}(f)$ is the input referred noise PSD of a single stage and the final approximation in (6.2) is true for a large number of bits ($N \gg 1$) and converges to $4/3$ quickly. The kT/C noise of the input sampler and the ADC quantization noise add to the input referred noise PSD to give the total input noise PSD. In total,

$$S_{n,total}(f) = S_{sample}(f) + S_{n,ADC}(f) + S_q(f) \tag{6.3}$$

where $S_{sample}(f) = kT/C_s/(f_s/2)$ is the noise PSD from the input sampler over the Nyquist range and $S_q(f) = V_{LSB}^2/12/(f_s/2)$ is the ADC quantization noise PSD.

6.3 Single Pipeline Stage Input Referred Noise

The goal of this section is to derive the input referred noise PSD for a single pipeline stage $S_{n0}(f)$. The interpretation of the periodic filtering model with aliasing is used to calculate the input referred noise PSD for each of the noise sources in the gain stage. The total input referred noise from a pipeline stage consists of contributions from the virtual ground threshold detection comparator, the fine phase charging current source, and the switches in the gain stage.

6.3.1 Periodic Filtering Model

Most of the noise sources in the CBSC charge transfer phase result in a non-stationary noise response. For example, the fine phase charging current integrates noise onto the capacitance network and clearly does not reach steady-state. As another example, the response of the preamplifier for the threshold detection comparator may not reach steady-state before reaching the output threshold voltage. The non-stationary noise analysis presented in Chapter 3 can be used to analyze both of these cases for a single charge transfer phase. While analyzing a single charge transfer phase does yield insight into the noise voltage behavior versus time over the duration of the charge transfer, ultimately, the output value is sampled and the statistics on the series of samples are of more interest. The periodic filtering noise model from Chapter 3 addresses the spectral analysis of the series of periodic samples allowing for the inclusion of both thermal and flicker noise sources. The focus of the analysis then becomes the Fourier transform of the windowed transfer function from the noise source to the output of the gain stage which is referred to the input by the stage gain. Because both approaches yield different insights into the performance of the system, they are both presented. However, only results for the white noise sources using the non-stationary noise analysis are presented under the assumption that the preamplifier is an ideal integrator. These results are simpler and allow for an easier comparison of the different noise contributions.

6.3.2 Threshold Detection Comparator Noise

The schematic of the ideal threshold detection comparator with a band-limiting preamplifier is shown in Figure 6-3. As discussed in Chapter 4, the output of the preamplifier is assumed to be clamped after each decision so that $\frac{1}{2}C_i$ has either $\pm V_D$ across it. When the voltage on the output capacitance is clamped, it does not begin to discharge until the differential input voltage to the transconductance preamplifier is greater than the input referred clamp voltage ($|v_{ID}| > |V_D|/A_o$). An approximate

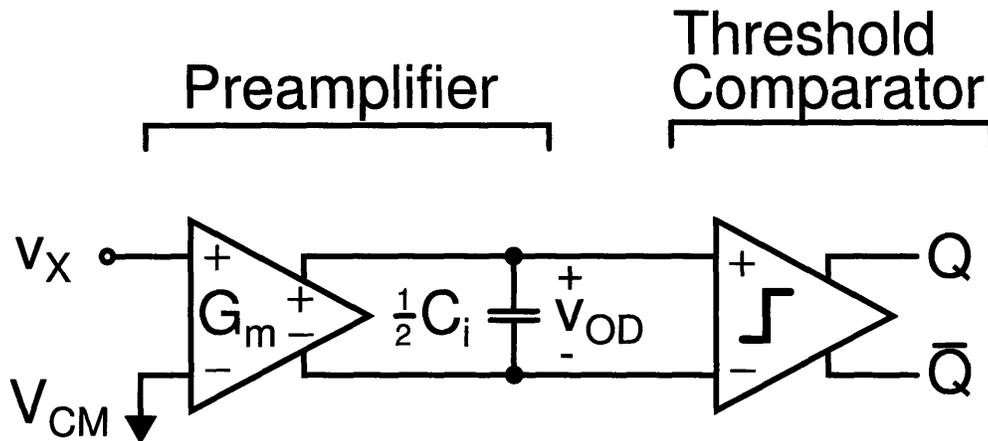
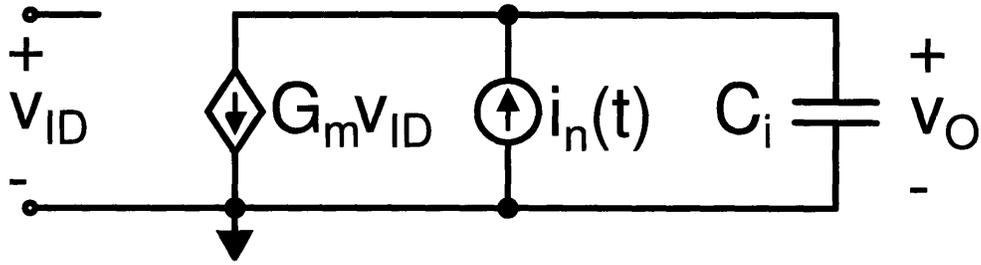


Figure 6-3: Ideal threshold detection comparator with band-limiting preamplifier.

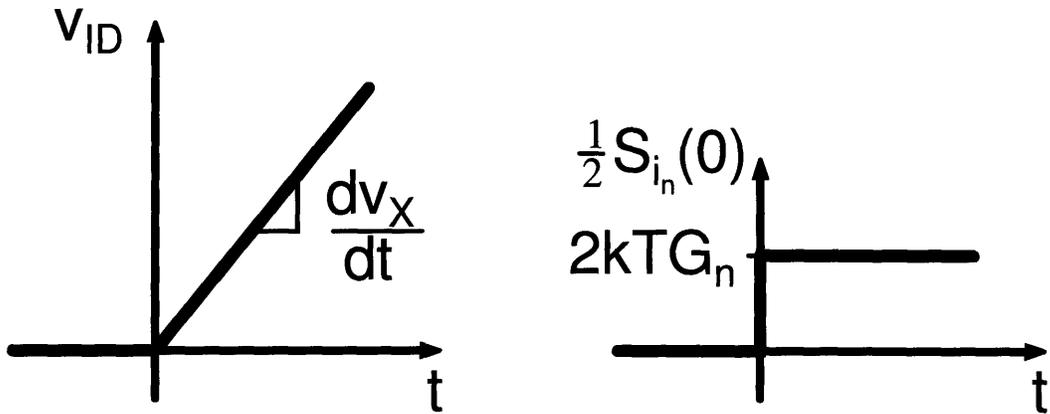
linear half-circuit model for the ideal preamplifier that neglects slew rate limitations is shown in Figure 6-4(a) where its differential input voltage is modeled as a step ramp waveform and the noise from the transconductance device starts integrating onto the output capacitance at time zero (Figure 6-4(b)). The noise from the preamplifier consists of noise on the band-limiting capacitance $\frac{1}{2}C_i$ from the clamped output after the coarse charge transfer phase and noise current integrated onto the band-limiting capacitance during the fine phase response time t_i . The noise contribution from the threshold comparator following the preamplifier is assumed to be small when referred to the input, which is equivalent to assuming the preamplifier has a reasonably large noise gain.

Clamp State Noise

The noise from the clamped state is a noise initial condition on the band-limiting capacitance ($\frac{1}{2}C_i$). Assuming the NMOS diode has a relatively low on-resistance compared to the output resistances of the current source loads and input pair devices (M_1 - M_4) in Figure 6-5, only noise from the clamp device and the current passing through the clamp (M_3 or M_4) feed noise to the band-limiting capacitor. The transfer function from these two noise sources to the output is the low-pass filter at the output of the preamplifier in the clamp state. Assuming the preamplifier reaches steady-state



(a)



(b)

Figure 6-4: Half-circuit model for band-limiting preamplifier. (a) Linear half-circuit model. (b) Waveforms for linear half-circuit model.

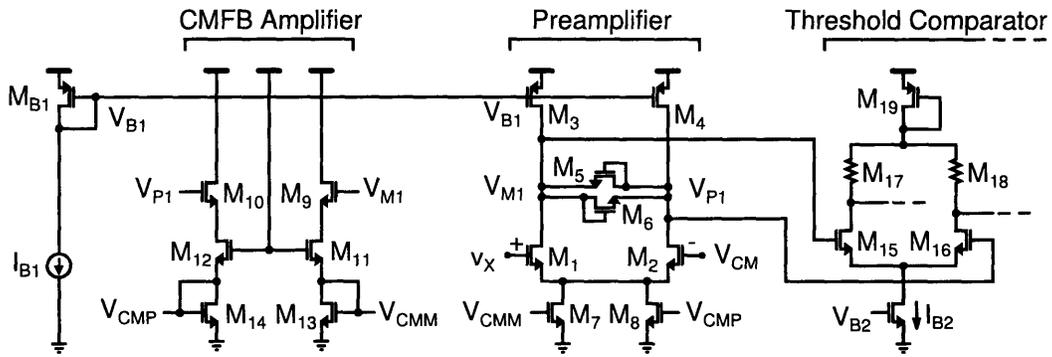


Figure 6-5: Comparator preamplifier for prototype.

during its time in the clamped state, the transfer function is

$$|H_{w,clamp}(f)|^2 = \frac{1}{G_m^2} \left(\frac{G_D^{-2}/R_o^2}{1 + (2\pi f)^2 \left(\frac{C_i}{2G_D}\right)^2} \right) \left(\frac{e^{-t_i/\tau_o}}{1 - e^{-t_i/\tau_o}} \right)^2 \quad (6.4)$$

where G_D is the diode clamp conductance, the noise has been referred to the input of the preamplifier using (3.70), and the exponential decay occurs during the preamplifier response time. If the response time t_i is much longer than the high impedance time constant $\tau_o = R_o C_i$ during the response time, the clamp noise decays to zero and does not contribute to the input referred noise. The one-sided input referred aliased noise contribution from the clamp state can be found using the transfer function (6.4) in aliasing summation (3.94)

$$S_{n,clamp}(f) = \sum_n |H_{w,clamp}(f - n f_s)|^2 S_{i_n,clamp}(f - n f_s) \quad (6.5)$$

where $S_{i_n,clamp}(f)$ is the twice the two-sided noise current PSD applied to C_i during the clamp state.

However, because the preamplifier is assumed to reach steady-state during the clamp state, the non-stationary noise analysis is not necessary to calculate the output noise voltage from the clamp and current source load thermal noise sources. The noise at the output is simply the kT/C noise at the output

$$\overline{v_{n,clamp}^2} = 2 \left(\frac{G_{nD}}{G_D} \right) \left(\frac{kT}{C_i} \right). \quad (6.6)$$

If the response for an ideal integrator is being calculated, the noise initial condition from the clamp state does not decay, and the input referred noise is

$$\overline{v_{n,clamp}^2} = 2 \left(\frac{G_{nD}}{G_D} \right) \left(\frac{kT}{C_i} \right) \frac{1}{|A_N(t_i)|^2} \quad (6.7)$$

where $|A_N(t_i)| = G_m t_i / C_i$ (3.75) is the noise gain of an ideal integrator operating for t_i seconds before reaching the threshold at the output of the preamplifier.

Preamplifier Response Time Noise

During the preamplifier response time, the noise current from the transconductance amplifier adds noise to the output voltage of the preamplifier. The general transfer function from the output noise current of the transconductance amplifier referred to the input is

$$|H_{w,resp}(f)|^2 = \left(\frac{1/G_m^2}{1 + (2\pi f \tau_o)^2} \right) \left(\frac{1 - 2e^{-t_i/\tau_o} \cos(2\pi f t_i) + e^{-2t_i/\tau_o}}{1 - 2e^{-t_i/\tau_o} + e^{-2t_i/\tau_o}} \right) \quad (6.8)$$

where the noise has been referred to the preamplifier input with (3.70), and the preamplifier response time t_i is that defined in Figure 4-3. The preamplifier response time noise simplifies into two interesting special cases for a broad-band preamplifier and an ideal integrator preamplifier

$$|H_{w,resp}(f)|^2 = \begin{cases} \frac{1/G_m^2}{1 + (2\pi f \tau_o)^2} & t_i \gg \tau_o \\ \frac{1}{G_m^2} \text{sinc}^2(ft_i) & t_i \ll \tau_o. \end{cases} \quad (6.9a)$$

$$(6.9b)$$

For the broad-band case, the transfer function simplifies to the expected steady-state result which is independent of the response time t_i and has a constant noise bandwidth. For the case of an ideal integrator preamplifier, the transfer function simplifies to a sinc function with a noise bandwidth that is inversely proportional to the response time. These two results are identical to the cases (3.83) and (3.78) described in Example 3.5. Figure 6-6 show a plot of $|H_{w,resp}(f)|^2$ for three cases where the output resistance of the preamplifier was varied. The one-sided input referred aliased noise contribution from the preamplifier during its response time is

$$S_{n,resp}(f) = \sum_n |H_{w,resp}(f - n f_s)|^2 S_{i_n,resp}(f - n f_s) \quad (6.10)$$

where $S_{i_n,resp}(f)$ is twice the two-sided noise PSD applied to C_i during the preamplifier response time.

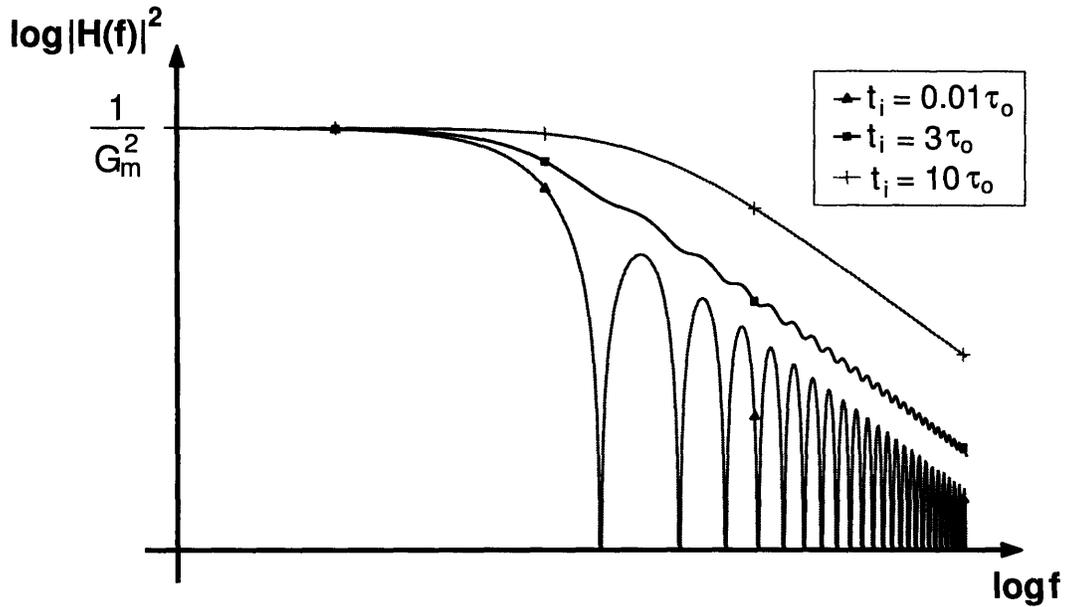


Figure 6-6: Preamplifier response time filter $|H_{w,resp}(f)|^2$ for different output resistances causing variation in t_i relative to τ_o .

The input referred noise of a transconductance amplifier with infinite output resistance was derived in Example 3.5 as a special case when $t_i \ll \tau_o$. From (3.77) and (3.78)

$$\overline{v_{n,resp}^2} = 4kTR_n \frac{1}{2t_i} \quad (6.11)$$

where $R_n = G_n/G_m^2$ is the usual input referred noise resistance for the preamplifier. For easier comparison with the clamp state noise, the input referred noise can be reformulated into a kT/C noise expression

$$\overline{v_{n,resp}^2} = 2 \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{C_i} \right) \frac{1}{|A_N|} \quad (6.12)$$

where again, the definition of the integrator noise gain (3.75) has been used.

Total Preamplifier Noise

The total aliased noise contribution from the preamplifier is the sum of the clamp state and response time noise

$$S_{n,preamp}(f) = S_{n,clamp}(f) + S_{n,resp}(f). \quad (6.13)$$

To gain some insight into the relative contribution of the magnitude of these two noise sources, consider the sum of the input referred noise voltages (6.7) and (6.12)

$$\overline{v_{n,preamp}^2} = 2 \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{C_i} \right) \frac{1}{|A_N|} \left[1 + \left(\frac{G_m}{G_n} \right) \left(\frac{G_{nD}}{G_D} \right) \frac{1}{|A_N|} \right]. \quad (6.14)$$

Assuming the preamplifier has a relatively large noise gain

$$|A_N| \gg \left(\frac{G_m}{G_n} \right) \left(\frac{G_{nD}}{G_D} \right) \quad (6.15)$$

the second term in (6.14) from the clamp noise contribution is small, and the response time noise dominates the input referred noise of the preamplifier

$$\overline{v_{n,preamp}^2} \approx 2 \left(\frac{G_n}{G_m} \right) \left(\frac{kT}{C_i} \right) \frac{1}{|A_N|} \quad (6.16)$$

$$= 4kTR_n \frac{1}{2t_i}. \quad (6.17)$$

6.3.3 Charging Current Noise

The second source of noise to be considered during the charge transfer phase is the contribution from the fine phase charging current source I_2 shown in Fig. 6-7. The noise from the charging current I_2 only adds noise to the final sampled output value after the preamplifier input threshold crossing. The noise added to the capacitor network before this time does not effect the final value, and only changes the time it takes to reach the preamplifier input threshold. The noise contribution from the

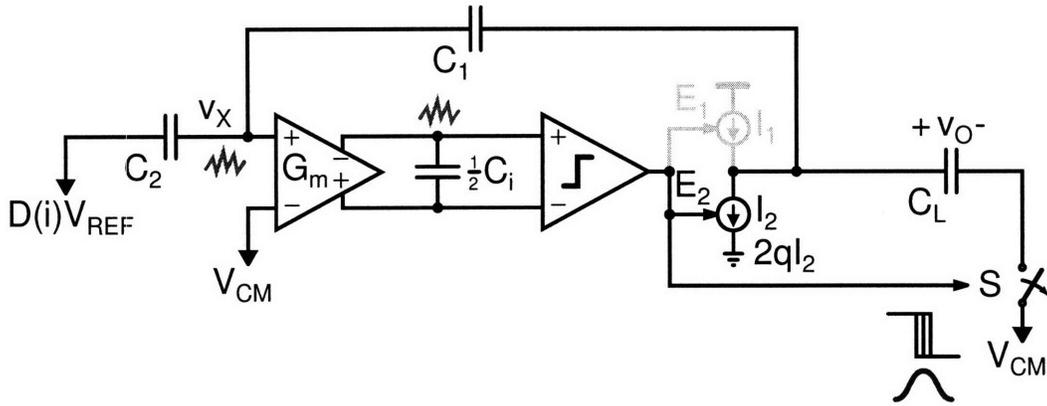


Figure 6-7: Noise contribution from fine phase charging current I_2 .

charging current consists of the random walk noise on the external capacitor network during two independent time intervals. The first interval is the preamplifier response time t_i from Fig. 4-3, and the second interval is the delay time from the threshold detection to the sampling switch opening $t_d - t_i$ in Fig. 4-3.

Preamplifier Filtered Noise

The random walk at the preamplifier input during the preamplifier response time generates a jitter that is negatively correlated with the noise voltage at preamplifier input and partially cancels the noise during this time. Referring to Figure 6-7, consider a larger than average random walk deviation at the preamplifier input. This larger than average deviation results in a larger than average preamplifier output, and a shorter than average time to reach the comparator threshold voltage. Therefore, the shorter than average comparator delay cancels the larger than average random walk deviation.

To derive a transfer function for the noise that takes into account the correlation between the comparator jitter and the output random walk, consider the following procedure: analyze the circuit as two open-loop voltages referred to the input of the gain stage. The first is the open-loop random walk voltage at the output of the gain stage referred to the input $y(t)$, and the second is the voltage error at the output referred to the input $z(t)$ that results from the jitter in the comparator decision from

the preamplifier filtered random walk voltage. The true input referred noise voltage is then the difference of these two voltages

$$v_{I_{2i}}(t) = y(t) - z(t). \quad (6.18)$$

The two-sided noise PSD is then a function of the PSDs of $y(t)$ and $z(t)$ as well as their cross-power spectral densities

$$S_{nn,I_{2i}}(f) = S_{yy}(f) - S_{yz}(f) - S_{zy}(f) + S_{zz}(f) \quad (6.19)$$

$$= |H_y(f) - H_z(f)|^2 S_{xx}(f) \quad (6.20)$$

where $H_y(f)$ is the open-loop transfer function from the current source noise to the output, $H_z(f)$ is the open-loop transfer function from the current source to output error due to the jitter in the comparator decision from the preamplifier filtered noise, and $S_{xx}(f)$ is the two-sided noise PSD of the current source I_2 . The open-loop transfer function for the random walk referred the input of the gain stage during t_i is

$$H_y(f) = \left(\frac{t_i}{C_E} \right) \left(\frac{C_1}{C_1 + C_2} \right) \text{sinc}(ft_i) e^{-j(2\pi f)t_i/2}. \quad (6.21)$$

The open-loop transfer function due to the jitter in the comparator decision is more complicated. The s-domain transfer function from the charging current I_2 to the preamplifier output referred to the input of the gain stage is

$$H_z(s) = \frac{1}{|A_n(t_i)|} \left(\frac{1}{sC_E} \right) \left(\frac{C_1}{C_1 + C_2} \right) \frac{A_o}{1 + s\tau_o}. \quad (6.22)$$

The infinite duration impulse response is the inverse Laplace transform

$$h_z(t) = \left(\frac{A_o}{|A_n(t_i)|} \right) \left(\frac{1}{C_E} \right) \left(\frac{C_1}{C_1 + C_2} \right) (1 - e^{-t/\tau_o}) u(t) \quad (6.23)$$

and the Fourier transform of the windowed impulse response is the desired noise

transfer function

$$H_z(f) = \mathcal{F}\{h_z(t)w(t)\}. \quad (6.24)$$

The transfer function for the charge current noise accounting for the correlated jitter is

$$|H_{w,I_2}(f)|^2 = |H_y(f) - H_z(f)|^2. \quad (6.25)$$

The one-sided input referred aliased noise contribution from the charging current during the preamplifier response time is

$$S_{n,I_{2i}}(f) = \sum_n |H_{w,I_2}(f - nf_s)|^2 2S_{xx}(f - nf_s) \quad (6.26)$$

To understand the properties of this transfer function, two special cases are considered, a wide-bandwidth preamplifier and an ideal integrator preamplifier. Plots of the transfer function $H_{w,I_2}(f)$ are shown for three values of preamplifier output resistance R_o in Fig. 6-8. For a wide-bandwidth preamplifier $R_o = 10 \text{ k}\Omega$, the noise at the output of the preamplifier is proportional to the noise at the input of the preamplifier at low frequencies. For an infinite bandwidth preamplifier, they would be proportional at all frequencies and the jitter would completely cancel the open-loop random walk deviation and would have a correlation coefficient of $c_{yz} = -1$. For a finite bandwidth, higher frequencies have a phase delay resulting in less than complete cancellation. In the other extreme, an ideal integrating preamplifier $R_o = 100 \text{ M}\Omega$ still has a correlated jitter, but it is the minimum. Using the open-loop transfer functions, it can be shown that the correlation coefficient for an ideal integrator is $c_{yz} = -\sqrt{3}/2 \approx -0.866$.

Using a procedure that parallels the frequency domain approach above, the white noise voltage response including correlation can be expressed in a form similar to (3.33)

$$\overline{v_{n,I_{2i}}^2} = S_{xx}(0) \int_{-\infty}^t |h_y(\tau) - h_z(\tau)|^2 d\tau \quad (6.27)$$

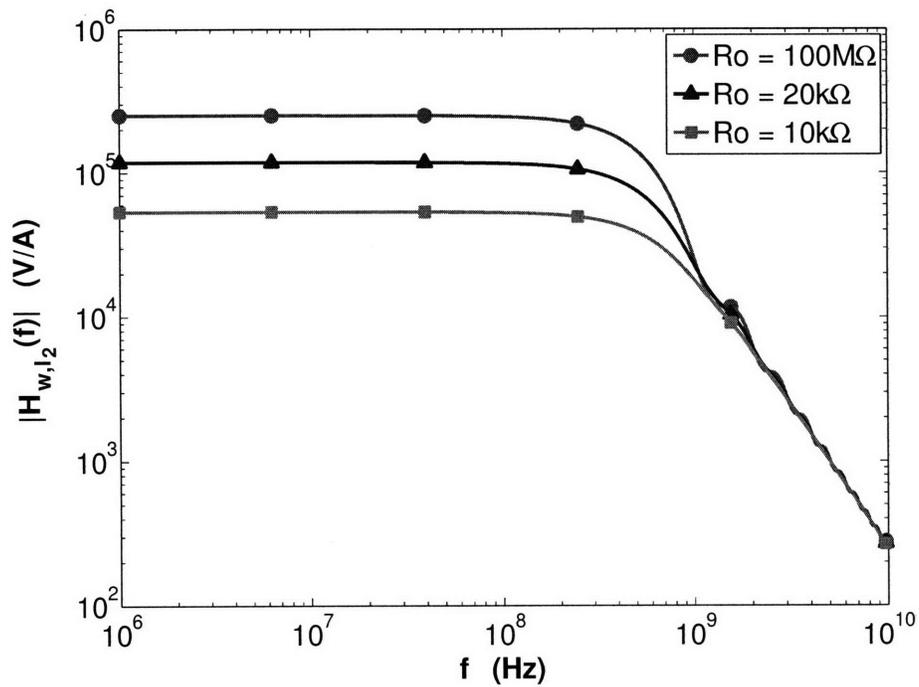


Figure 6-8: Charging current transfer function during preamplifier response time. Preamplifier output swept for a constant G_m and C_i . A broad-band preamplifier, lower output resistance, results in more noise cancellation and therefore, lower transfer function gain.

where

$$h_y(t) = \left(\frac{1}{C_E} \right) \left(\frac{C_1}{C_1 + C_2} \right) u(t) \quad (6.28)$$

is the impulse response from the charging current noise to the output voltage referred to the input of the gain stage and the general form of $h_z(t)$ is define in (6.23). The expression for $h_z(t)$ simplifies to

$$h_z(t) = \left(\frac{1}{C_E} \right) \left(\frac{C_1}{C_1 + C_2} \right) \left(\frac{t}{t_i} \right) u(t) \quad (6.29)$$

for the case where the preamplifier is an ideal integrator. Substituting (6.28) and (6.29) into (6.27) to calculate the input referred noise from the charging current including the effects of the negatively correlated comparator jitter results in

$$\overline{v_{n,I2i}^2} = \frac{1}{3} \left(\frac{S_{xx}(0)}{C_E^2} t_i \right) \left(\frac{C_1}{C_1 + C_2} \right)^2. \quad (6.30)$$

The input referred noise is 1/3 of the open-loop random walk voltage at the output referred to the input. The factor of 1/3 is a result of the partial cancellation of noise for an ideal integrator preamplifier. For a wide bandwidth preamplifier, this factor approaches zero.

Noise During Threshold Comparator Delay

During the second interval, the threshold comparator delay, the random walk noise also accumulates on the external capacitor network until the output sampling switch is opened. The noise transfer function is

$$|H_{w,I2c}(f)|^2 = \left(\frac{t_c}{C_E} \right)^2 \left(\frac{C_1}{C_1 + C_2} \right)^2 \text{sinc}^2(ft_c) \quad (6.31)$$

where $t_c = t_d - t_i$ is the threshold comparator delay. The one-sided input referred aliased noise contribution from the charging current during the threshold comparator

delay is

$$S_{n,I_{2c}}(f) = \sum_n |H_{w,I_{2c}}(f - nf_s)|^2 2S_{xx}(f - nf_s). \quad (6.32)$$

Because the preamplifier does not filter the noise added to the output during the threshold comparator delay, the noise added during this time is not correlated with the comparator jitter. The noise contribution referred to the input during this time is

$$\overline{v_{n,I_{2c}}^2} = \left(\frac{S_{xx}(0)}{C_E^2} t_c \right) \left(\frac{C_1}{C_1 + C_2} \right)^2. \quad (6.33)$$

which is simply a random walk noise voltage.

Total Charging Current Noise

The total one-sided input referred noise PSD from the charging current noise is

$$S_{n,I_2}(f) = S_{n,I_{2i}}(f) + S_{n,I_{2c}}(f). \quad (6.34)$$

The total input referred noise from the charging current is the sum of the preamplifier filtered (6.30) and threshold comparator delay (6.33) contributions

$$\overline{v_{n,I_2}^2} = \frac{1}{3} \left(\frac{S_{xx}(0)}{C_E^2} t_i \right) \left(\frac{C_1}{C_1 + C_2} \right)^2 \left[1 + \frac{3t_c}{t_i} \right]. \quad (6.35)$$

For the case of an ideal integrator preamplifier, the noise accumulated during the preamplifier response time dominates this input referred noise contribution if

$$t_i \gg 3t_c. \quad (6.36)$$

However, for a general preamplifier bandwidth, it is difficult to say *a priori* which of the two terms is more important.

Assuming that the preamplifier response time is much larger than the threshold comparator delay ($t_i \gg t_c$) and the charging current source has shot noise $S_{xx}(0) = qI_2$, the expression for the noise contribution from the charging current

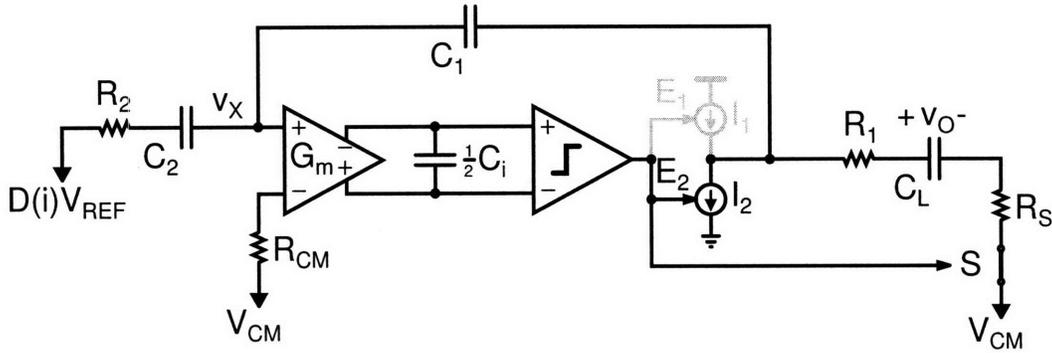


Figure 6-9: Noise contribution from sampling and configuration switches.

can be rewritten as

$$\overline{v_{n,I_2}^2} = \frac{1}{3} \left(\frac{qV_{ovx}}{C_E} \right) \quad (6.37)$$

where V_{ovx} is the input referred overshoot of the fine charge transfer phase. Therefore, for a constant overshoot requirement for linearity, the only way to lower the noise contribution from the charging current noise is to increase the total capacitance used in the sampling and feedback networks.

6.3.4 Switch Noise

During the charge transfer phase, two switches are connected in series with the load capacitance and one in series with capacitor C_2 to the appropriate reference voltage as shown in Fig. 6-9. The noise from these switches is white and results in two sources of noise for the CBSC charge transfer phase. The first source is the noise present at node v_x that the preamplifier filters during its response time. The second source is the noise present on the load capacitance at the output sampling instant. These two voltages result from the same resistor noise, but they are uncorrelated because they occur at different times due to the finite threshold comparator delay.

Preamplifier Filtered Noise

The noise present at node v_X at the threshold detection point is a white noise PSD determined by the resistance and capacitor network

$$S_{R_{neq}}(0) = 4kTR_{neq} \quad (\text{one-sided}) \quad (6.38)$$

where

$$R_{neq} = R_{CM} + (R_1 + R_S) \left(\frac{C_{1L}}{C_{1L} + C_2} \right)^2 + R_2 \left(\frac{C_2}{C_{1L} + C_2} \right)^2 \quad (6.39)$$

and C_{1L} is the series combination of C_1 and C_L . This formulation assumes that the RC time-constant of the switch and capacitor network is much smaller than the preamplifier time constant. The preamplifier filters the switch noise resulting in jitter in the comparator decision. The transfer function to refer this noise source to the input of the stage is similar to the preamplifier response noise

$$|H_{w,filter}(f)|^2 = \left(\frac{1}{1 + (2\pi f\tau_o)^2} \right) \left(\frac{1 - 2e^{-t_i/\tau_o} \cos(2\pi f t_i) + e^{-2t_i/\tau_o}}{1 - 2e^{-t_i/\tau_o} + e^{-2t_i/\tau_o}} \right). \quad (6.40)$$

The one-sided input referred aliased noise contribution from the switch noise during the preamplifier response time is

$$S_{n,filter}(f) = \sum_n |H_{w,filter}(f - n f_s)|^2 S_{R_{neq}}(f - n f_s). \quad (6.41)$$

where $S_{R_{neq}}(f - n f_s)$ is twice the two-sided noise PSD from the equivalent switch noise resistance R_{neq} .

Because the the noise bandwidth of the preamplifier filters the switch noise at v_X in a manner similar to the input referred noise of the preamplifier

$$\overline{v_{R,filter}^2} = 4kTR_{neq} \frac{1}{2t_i} \quad (6.42)$$

for an ideal integrator preamplifier. Therefore, this noise contribution from the

switches can be minimized through appropriate design of the switch resistances so that R_{neq} is much less than the input referred noise resistance R_n of the preamplifier.

Sampling Noise

The noise sampled onto the load capacitance from the switch and capacitor network assuming that the threshold detection comparator was not present is just the kT/C noise of the equivalent total capacitance

$$C_{eq} = \frac{C_x C_L}{C_x + C_L} \quad (6.43)$$

where C_x is the series combination of the feedback capacitances C_1 and C_2 . The noise voltage on C_L is the kT/C noise of C_{eq} through the voltage divider from v_{eq} to the load capacitance

$$\begin{aligned} \overline{v_{oR,sample}^2} &= \frac{kT}{C_{eq}} \left(\frac{C_x}{C_x + C_L} \right)^2 \\ &= \frac{kT}{C_L} \left(\frac{C_x}{C_x + C_L} \right). \end{aligned} \quad (6.44)$$

Therefore, the input referred noise is

$$\overline{v_{R,sample}^2} = \frac{kT}{C_L} \left(\frac{C_x}{C_x + C_L} \right) \left(\frac{C_1}{C_1 + C_2} \right)^2 \quad (6.45)$$

where $(C_1 + C_2)/C_1$ is the stage gain. Because this is a white noise source, its one-sided noise PSD is constant over the Nyquist range is

$$S_{n,sample}(f) = \frac{\overline{v_R^2}}{f_s/2} \quad (6.46)$$

Note, this result could also have been obtained using the steady-state transfer function for the switch and capacitor network and the aliasing summation.

Total Switch Noise

The total one-sided input referred noise from the switches during the charge transfer phase is sum of the noise voltage variances of the kT/C noise of the load and the switch noise error in the threshold detection

$$S_{n,R}(f) = S_{n,filter}(f) + S_{n,sample}(f). \quad (6.47)$$

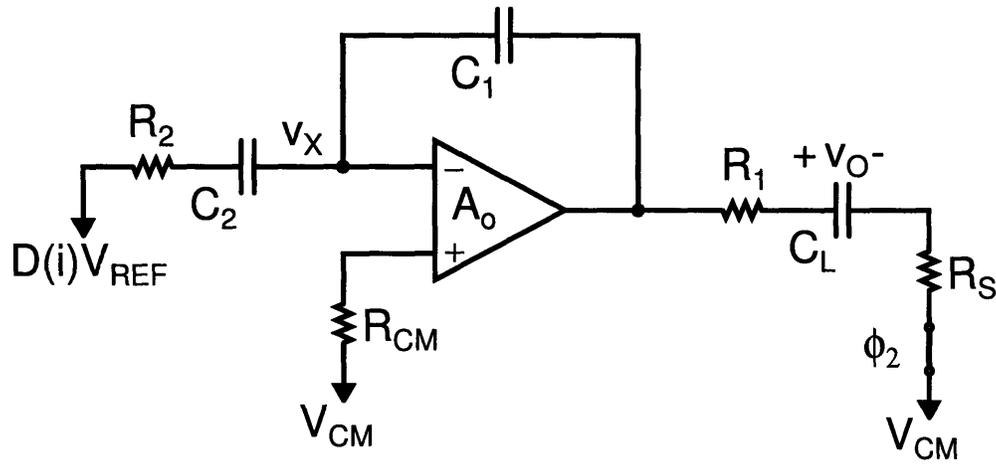
The total noise contribution from the switches for an ideal integrator preamplifier is the sum of the noise voltage variances for the two independent noise contributions (6.42) and (6.45). The filtered switch noise can be managed through appropriate sizing of switch resistances, but the sampling kT/C noise represents a fundamental noise limitation that depends on the size of the capacitances used. Unlike the usual kT/C limitation, the noise here is not solely defined in terms of C_L . For example, consider a gain of two stage $C_1 = C_2 = C_s/2$ where the load capacitance is scaled by a factor of two $C_L = C_s/2$. Then, the input referred noise contribution from sampling at the output is

$$\overline{v_{R,sample}^2} = \frac{1}{6} \frac{kT}{C_s}. \quad (6.48)$$

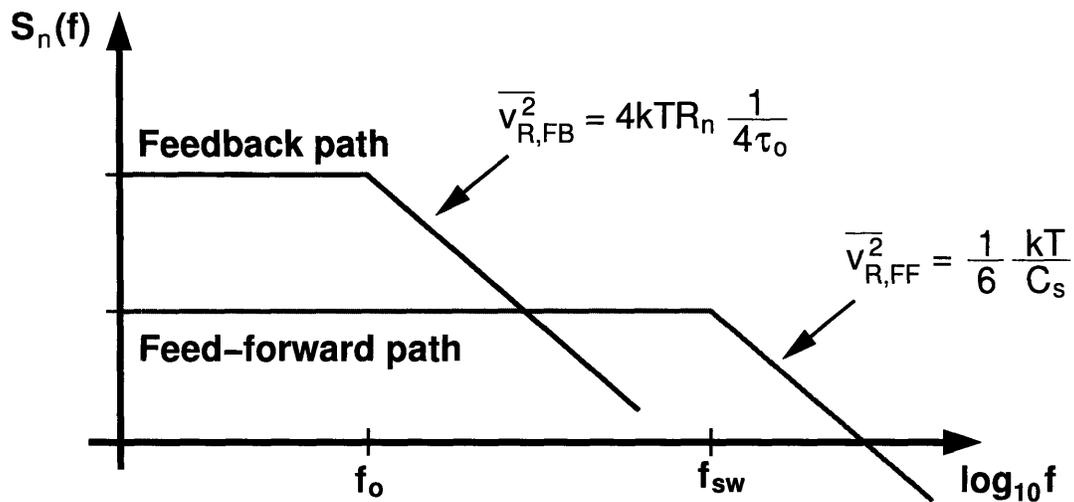
It should also be pointed out that the traditional op-amp based charge transfer implementations have similar contributions from the switch noise (Figure 6-10). In an op-amp based system, the switch and capacitor network has a wider bandwidth than the op-amp feedback loop. Therefore, the feedback loop filters a portion of the switch noise, but some also reaches the output through a feed-forward path. These two contributions are similar to those in the comparator-based charge transfer, but the two contributions in the op-amp based system are not independent.

6.4 Putting It All Together

This section discusses how to combine the filter results above to determine the total input referred noise PSD of the CBSC gain stage and prototype ADC. The thermal



(a)



(b)

Figure 6-10: Op-amp based charge transfer switch noise contribution for a gain of two stage. Op-amp noise bandwidth is $1/(4\tau_o) = \frac{\pi}{2}f_{3dB}$, $C_1 = C_2 = C_s$, and the load capacitance has been scaled by a factor of two $C_L = C_s/2$. (a) Schematic of op-amp based gain of two stage with switch resistances shown. (b) Input referred noise PSD highlighting feedback $\overline{v_{R,FB}^2}$ and feed-forward $\overline{v_{R,FF}^2}$ noise paths.

noise contributions for CBSC designs with ideal integrator preamplifiers are compared to similar contributions in op-amp based designs and to each other.

6.4.1 Complete Noise PSD Estimate

The noise transfer functions for the periodic filter model derived in the previous section can be combined to determine the input referred noise PSD estimate for the switched-capacitor gain stage. Numerical techniques for calculating the noise PSD from the transfer function, the input noise PSD, and the aliasing summation were presented in Chapter 3. For the prototype, a cascade of identical stages was used for the pipeline ADC, and the total input referred noise of the ADC can be calculated using (6.2) and (6.3). In Chapter 7, the results of the theoretical model presented here are compared to noise measurements from the prototype CBSC pipeline ADC.

6.4.2 Comparison of White Noise Voltage Contributions

Based on the mean-squared noise voltage results presented above, relative comparisons about the importance of the different thermal noise source are made. Emphasis is placed on the noise sources that are unique to CBSC designs compared to op-amp based designs. The importance of folded flicker noise is also addressed.

Thermal Noise

Assuming that both the op-amp and CBSC designs use the open-loop input sampler, they both suffer equally from the kT/C_s noise of the sampling capacitors. As discussed in Section 6.3.4 and shown in Figure 6-10, the switch noise contributions for a CBSC gain stage have similar contributions in op-amp based designs. However, the sampling noise and filtered noise in a CBSC system are independent because of the finite delay of the threshold detection comparator and logic that follow the preamplifier. In the op-amp based gain stage, the feedback loop filters the switch noise within the loop bandwidth, but at frequencies beyond the loop bandwidth, the switch noise feeds

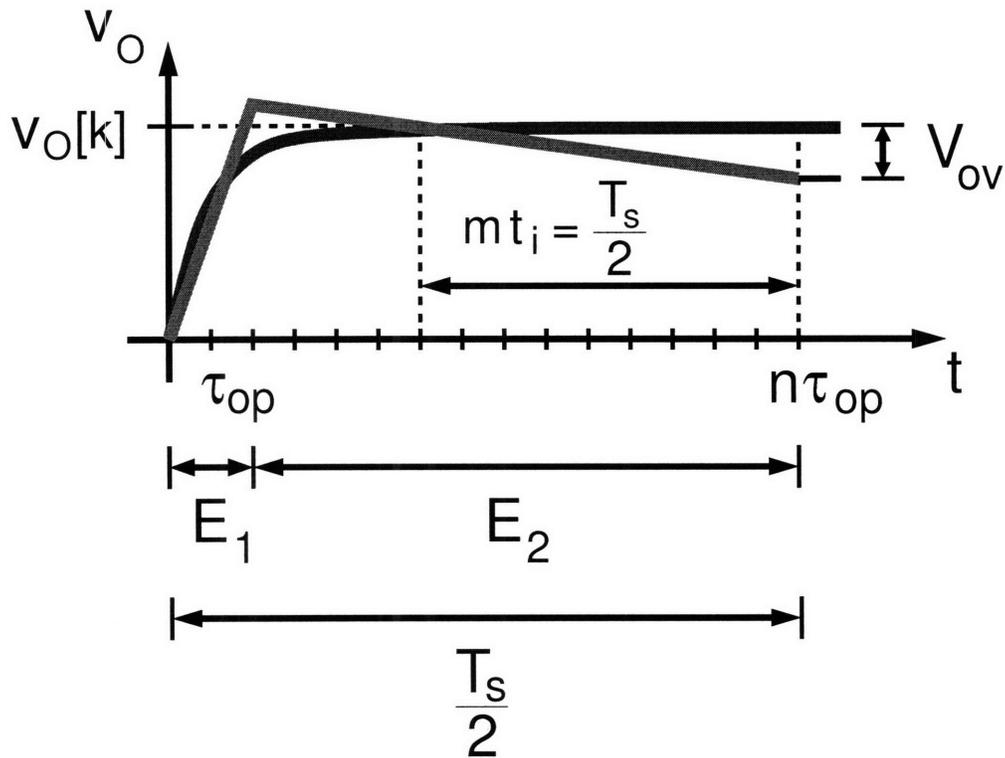


Figure 6-11: CBSC versus op-amp based charge transfer timing. Because t_i can potentially be made a larger fraction of $T_s/2$ than the op-amp closed-loop time constant τ_{op} can be, for the same power consumption and speed, the comparator-based design has lower noise bandwidth.

directly to the output capacitance.

The most significant difference in the noise performance of comparator-based and op-amp based switched capacitor systems is the noise contribution of the op-amp versus the virtual ground threshold detection comparator and charging current source. First, the charging current noise is assumed to be significantly smaller than the preamplifier noise. The preamplifier noise is then compared to the op-amp noise. Finally, the conditions for when the charging current noise is significantly smaller than the preamplifier noise are determined.

From (6.11), the input referred noise for the preamplifier is the expected noise PSD and the noise bandwidth is inversely proportional to the response time t_i . For an op-amp based system, the input referred noise PSD may be larger than the threshold comparator and preamplifier due to architectural differences in the op-amp that are

necessary to achieve high gain and make the op-amp stable in feedback. In an op-amp based system, the closed-loop bandwidth of the system determines the noise bandwidth

$$\text{NBW}_{op} = \frac{\pi}{2} f_{3dB} = \frac{1}{4\tau_{op}} \quad (6.49)$$

where the op-amp based system is modeled with a single pole. The number of closed-loop time constants in a half clock-cycle for an op-amp based system is relatively large and the desired accuracy determines the required number of time constants. In a CBSC system, potentially, the preamplifier response time of the fine charge transfer phase can be made a larger fraction of $T_s/2$ than τ_{op} . This situation is illustrated in Figure 6-11. It should be possible to trade the noise advantage of comparator based designs for lower power consumption at the same speed of operation. Therefore, CBSC designs have the potential to achieve the same noise accuracy and speed of operation at a lower power consumption than their op-amp based counterparts.

The preceding argument assumed that the noise contribution from the charging current is negligible, but in reality, the charging current noise also places a limit on the minimum value of capacitances that can be used to achieve a given accuracy for a specified overshoot requirement. In order for the charging current noise to be smaller than the preamplifier noise

$$C_E > \frac{1}{3} \left(\frac{G_m}{G_n} \right) \left(\frac{V_M}{kT/q} \right) C_i \quad (6.50)$$

where V_M is the change in preamplifier output voltage to reach the threshold comparator trip point and G_n/G_m is total input referred noise conductance relative the transconductance of the preamplifier input pair. Given a noise requirement, the preamplifier integration capacitance can be determined as discussed in Chapter 4.

Folded Flicker Noise

As discussed in Chapter 3, folded flicker noise appears white in the aliased spectrum. Using the conservation of noise power expressions for flicker noise aliasing (3.111),

the folded flicker mean squared noise can be estimated as

$$\sigma_{fold}^2 = |H(0)|^2 S_x(1) \ln \left(\frac{\text{NBW}}{f_s/2} \right) \quad (6.51)$$

where an ideal brick-wall filter with gain $|H(0)|$ and noise bandwidth NBW have been assumed. The folded flicker noise contribution is significant compared to the aliased thermal noise unless

$$\frac{\text{NBW}}{f_s/2} \ll \exp \left(\frac{\text{NBW}}{f_k} \right) \quad (6.52)$$

which implies that the noise bandwidth of the system is greater than the flicker noise corner frequency. Unfortunately, this folded flicker noise contribution is present even when correlated double sampling is used [35].

If the preamplifier response time noise dominates, the folded flicker noise contribution using (6.51) is

$$\overline{v_{n,preamp}^2} = \left(\frac{2S_{i_n,resp}(1)}{G_m^2} \right) \ln \left(\frac{T_s}{t_i} \right) \quad (6.53)$$

where $S_{i_n,resp}(1)$ is the two-sided flicker noise current PSD at 1 Hz from the preamplifier. The noise is only a function of input referred flicker noise of the preamplifier and depends logarithmically on the ratio of T_s and t_i , which is greater than or equal to 2 for the limiting case of $t_i = T_s/2$. Assuming that the relationship between t_i and the sampling period is fixed, the main factor determining the magnitude of the folded flicker noise contribution is the input referred flicker noise density at 1 Hz ($2S_{i_n,resp}(1)$). Lowering the contribution of the folded flicker noise in a given technology, requires increasing the area of the devices used in the preamplifier, especially the input differential pair. However, increasing the transistor sizes increases the parasitic capacitances and possibly the required power consumption.

An approximate expression for the folder flicker noise contribution from the charging current source I_2 can also be found. Assuming the noise during preamplifier

response time dominates the charging current noise

$$\overline{v_{n,I_2}^2} \approx \frac{1}{4} V_{ovx}^2 \left(\frac{S_x(1)}{I_2^2} \right) \ln \left(\frac{4 T_s}{3 t_i} \right) \quad (6.54)$$

where V_{ovx} is the overshoot at the output of the gain stage referred to the input, and $S_x(1)$ is the one-sided flicker noise current PSD at 1 Hz from the charging current source I_2 .

The folded flicker noise contribution is not unique to comparator-based designs. Op-amp designs would also suffer from the effects of folded flicker noise in a similar manner. However, the larger noise bandwidths of op-amp based systems means that flicker noise corner frequencies need to be that much higher for folded flicker noise to be significant compared to the aliased thermal noise.

6.5 Summary

The periodic filtering analysis for a series of samples from a possibly non-stationary underlying random process presented in Chapter 3 was applied to the CBSC charge transfer phase to derive a set of noise transfer functions than can be used to obtain a noise PSD estimate for a given CBSC design. In addition, noise voltage expressions were derived for the simplified case of an ideal integrator preamplifier. These simplified expressions were used to comment on the relative importance of each noise source and compare it to the similar noise source in an op-amp based implementation. As a final note, parasitic capacitances at the virtual ground summing node and the output node have been ignored in the equations given in this chapter to avoid unnecessarily complicating the discussion. However, the effect of these capacitances can be significant. It is relatively straight forward to extend the expressions presented here to include their effect, and the theoretical estimate given in Chapter 7 does include the effects of these parasitics.

Chapter 7

Measured Results of Noise in CBSC

7.1 Overview

Measured results of the noise performance of the prototype CBSC pipeline ADC are presented. The theoretical PSD estimates from Chapter 6 are compared with measured results for a variety of sampling frequencies. It is found that the two dominant sources of noise for the prototype are the flicker and thermal noise from the preamplifier of the comparator.

7.2 Measurement Method

A measurement of the input referred noise PSD of the prototype ADC can be made from the measurement of ADC output codes for a zero DC input. These output codes can then be mapped into the equivalent input noise voltage that would be used to generate them for a noiseless ADC

$$V_{Do}(nT_s) = D_o(nT_s) V_{LSB12} \quad (7.1)$$

where $D_o(nT_s)$ is the measured output code of sample n and V_{LSB12} least significant bit voltage for the prototype converter using all 12 b of output. A periodogram estimate [59] of the noise PSD can then be made from the series of samples

$$S_{T_o}(f) = 2 \left| \mathcal{F} \{ T_s V_{D_o}(nT_s) \} \right|^2 df \quad (7.2)$$

where $T_s = 1/f_s$ is the sampling period, $df = 1/T_o$ is the FFT bin width, $T_o = NT_s$ is the duration of the data record and N is the number of samples in the data record and the length of the FFT. The factor of 2 in (7.2) is because the one-sided PSD estimate is calculated.

Because a single periodogram measurement has a large variance, spectral averaging techniques are required to make an unbiased, low variance spectral estimate [59]. A simple method for achieving the spectral averaging is to average a large number K of independent periodogram measurements

$$\bar{S}_{T_o}(f) = \frac{1}{K} \sum_{k=1}^K S_{T_o,k}(f). \quad (7.3)$$

The expected value of the average periodogram estimate is the same as that of the original periodogram [59]

$$E\{\bar{S}_{T_o}(f)\} = 2S(f) * \left| T_o \text{sinc}(fT_o) \right|^2 df \quad (7.4)$$

which is the actual PSD $S(f)$ convolved with the magnitude squared of the Fourier transform of a rectangular window of duration T_o . From the discussion of noise bandwidth in Chapter 3, the two-sided noise bandwidth of the sinc filter is $1/T_o = df$. Therefore, if the actual noise PSD is constant over the noise bandwidth of the sinc filter, the periodogram estimate is approximately unbiased. In the limit of $T_o \rightarrow \infty$, the noise bandwidth goes to zero, and the periodogram is an unbiased estimate of $S(f)$ [59].

The standard deviation of the average periodogram estimate is [59]

$$\text{Std}\{\bar{S}_{T_o}(f)\} \approx \frac{1}{\sqrt{N}} [2S(f)] \quad f \neq 0. \quad (7.5)$$

For example, for an average of 100 periodogram measurements, the standard deviation is roughly 10% of the mean. The data presented here uses $K = 30$, which results in a standard deviation of approximately 18% of the mean.

The advantage of the average periodogram spectral estimation technique is that it achieves smoothing of the periodogram PSD estimate without loss of frequency resolution. The disadvantage is that large amounts of data are required to obtain a low variance PSD estimate.

Because investigation of the low frequency flicker noise is desired, the minimum frequency of the periodogram is of interest. The lowest frequency bin in the FFT depends on the length of the data record

$$df = \frac{1}{T_o} = \frac{f_s}{N}. \quad (7.6)$$

Therefore, the only way to measure very low frequency noise is to increase the duration of the data record either through the collection of more continuous samples (increase N) or increasing the time between samples (decrease f_s). The minimum frequency FFT bin has a width of df centered around df Hz, which extends from $\frac{1}{2}df \leq f \leq \frac{3}{2}df$. All noise from frequencies less than $\frac{1}{2}df$ is lumped into the DC FFT frequency bin and appears as an time-varying offset between the datasets.

7.3 Results

The measured PSD estimates using the average periodogram method are compared with theoretical estimates made using the analysis from Chapter 6. Device parameters for prototype design are determined from simulations and parasitic extraction of the layout.

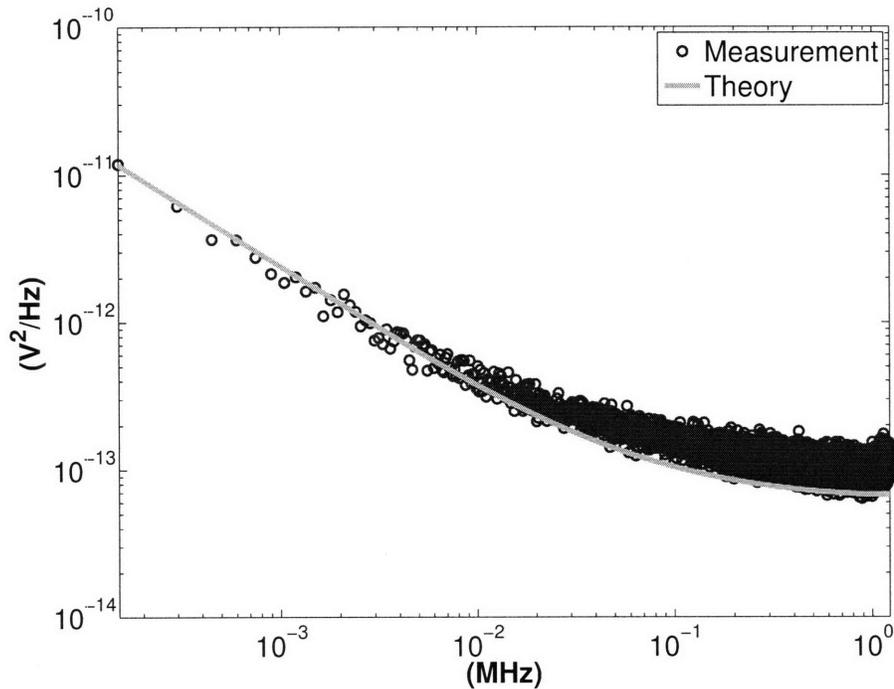
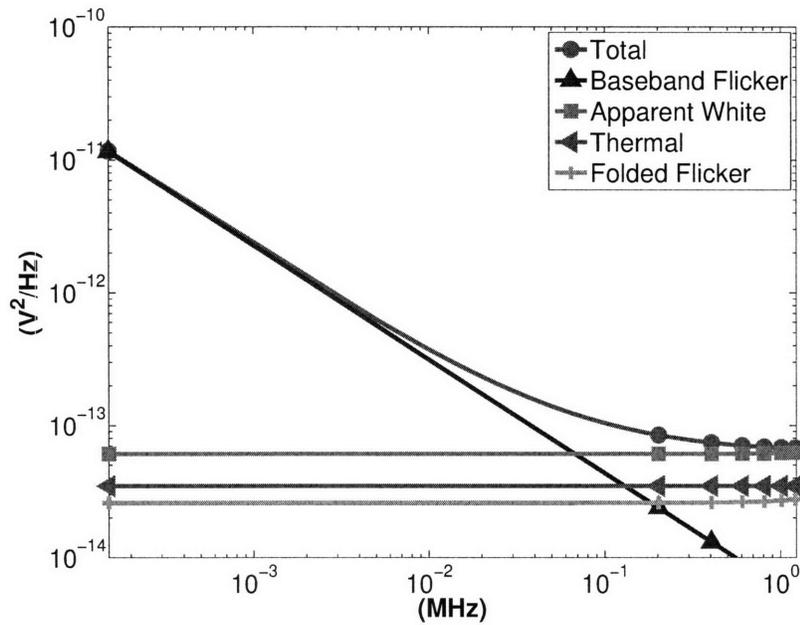


Figure 7-1: Theoretical and measured noise PSD $f_s = 2.4576$ MHz, $K = 30$

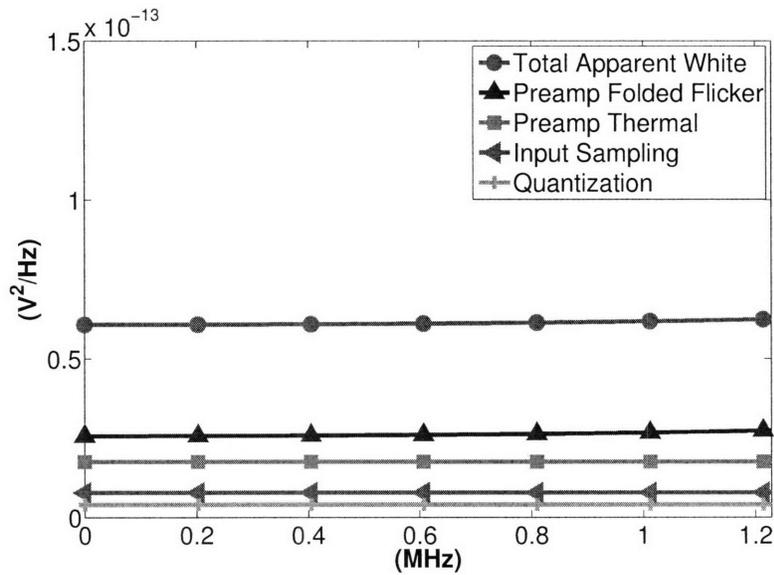
7.3.1 ADC Input Referred Noise PSD

For a sampling frequency of 2.4576 MHz, both the measured and theoretical noise PSD estimates are shown in Figure 7-1 in a log-log graph. The theoretical estimate and measured PSD match to within knowledge of the device flicker noise parameters and output resistance of preamplifier devices. Sensitivity of the theoretical prediction to these parameters is investigated in Section 7.3.2.

The theoretical breakdown of the noise contributions for the 2.4576 MHz sampling frequency data is given in Figure 7-2(a). This plot shows the contributions of the direct baseband flicker noise, the folded flicker noise, the total aliased thermal noise, and their contribution to the total noise PSD. The apparent white noise is the sum of the aliased thermal noise and the folded flicker noise PSDs. It is clear from this graph that the folded flicker noise contributes significantly to the apparent white noise of the ADC. Figure 7-2(b) plots the top four contributors to the apparent white noise of the ADC and shows that the folded flicker noise of the preamplifier dominates.



(a)



(b)

Figure 7-2: Theoretical breakdown of PSD noise for $f_s = 2.4576$ MHz (a) Theoretical breakdown of aliased components. (b) Theoretical breakdown of apparent white noise sources.

Rank	PSD (V ² /Hz)	% of Total	Source
1	2.62×10^{-14}	42.8%	Preamp Folded Flicker
2	1.75×10^{-14}	28.6%	Preamp Thermal
3	7.79×10^{-15}	12.7%	Input Sampler
4	4.04×10^{-15}	6.60%	Quantization Noise
5	3.36×10^{-15}	5.49%	Switch Noise Preamp Response
6	1.12×10^{-15}	1.84%	Output Sample
7	7.36×10^{-16}	1.20%	Charging Current Thermal: t_c
8	2.26×10^{-16}	0.37%	Charging Current Thermal: t_i
9	1.83×10^{-16}	0.30%	Charging Current Folded Flicker: t_c
10	5.77×10^{-17}	0.09%	Charging Current Folded Flicker: t_i
11	8.46×10^{-19}	0.00%	Preamp Clamp Thermal
12	5.75×10^{-19}	0.00%	Preamp Clamp Folded Flicker

Table 7.1: Ranking of apparent white noise sources in ADC PSD estimate for sampling frequency $f_s = 2.4576$ MHz.

Specifically, it is the flicker noise of the input pair devices that represents the dominant contribution to the folded flicker noise. Table 7.1 shows a complete breakdown of all possible apparent white noise sources from their theoretical estimates and their relative contribution to the total apparent white noise.

Figure 7-3 and Figure 7-4 compare the theory and measurements for two additional sampling frequencies of 983.04 kHz and 327.68 kHz. Over the three sampling frequencies shown, the apparent white noise level varies over almost an order of magnitude and still matches the theoretical prediction reasonably well.

7.3.2 Sensitivity of Theoretical Prediction

The sensitivity of the theoretical prediction to key parameters is investigated. Because the flicker noise of the preamplifier input devices dominate the noise performance of the prototype ADC, the theoretical results are particularly sensitive to the preamplifier flicker noise parameters $S_{i_n}(1)$ and α . In addition, the output resistance R_o determines the steady-state bandwidth of the preamplifier. Therefore, the accuracy of the output resistance can have a noticeable effect on the thermal noise contribution

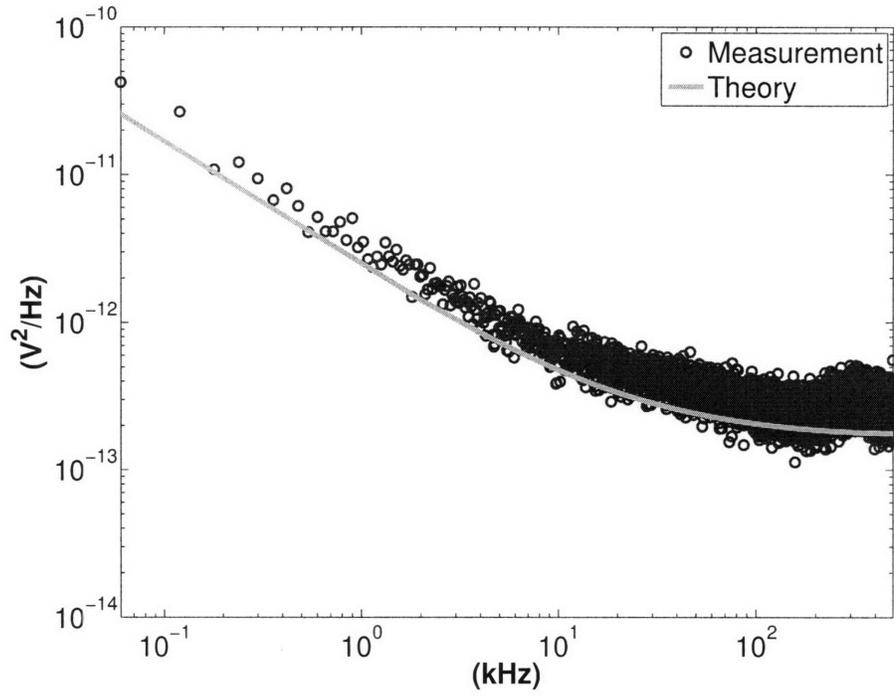


Figure 7-3: Theoretical and measured noise PSD $f_s = 983.04$ kHz, $K = 30$.

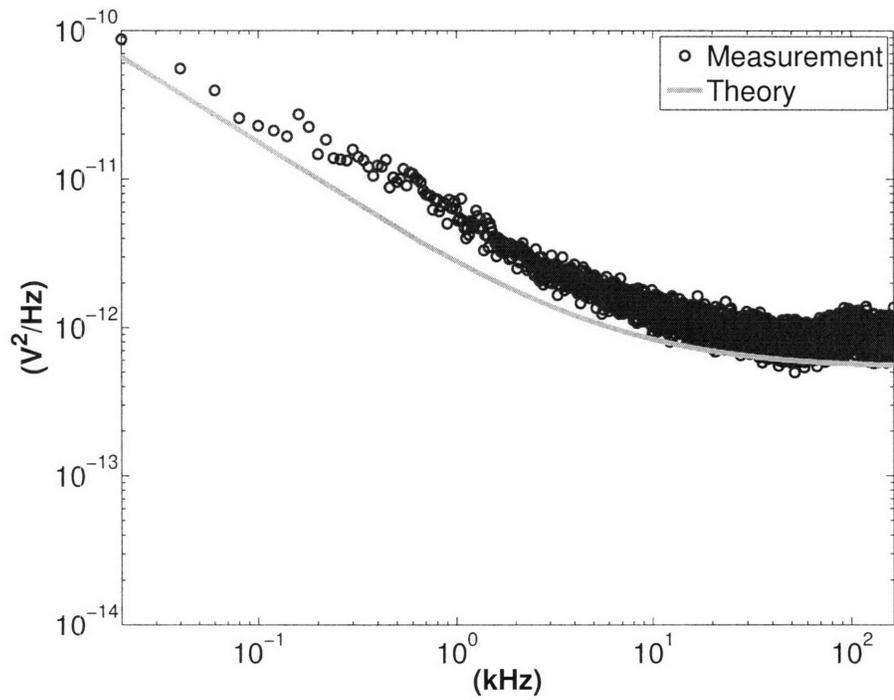


Figure 7-4: Theoretical and measured noise PSD $f_s = 327.68$ kHz, $K = 30$.

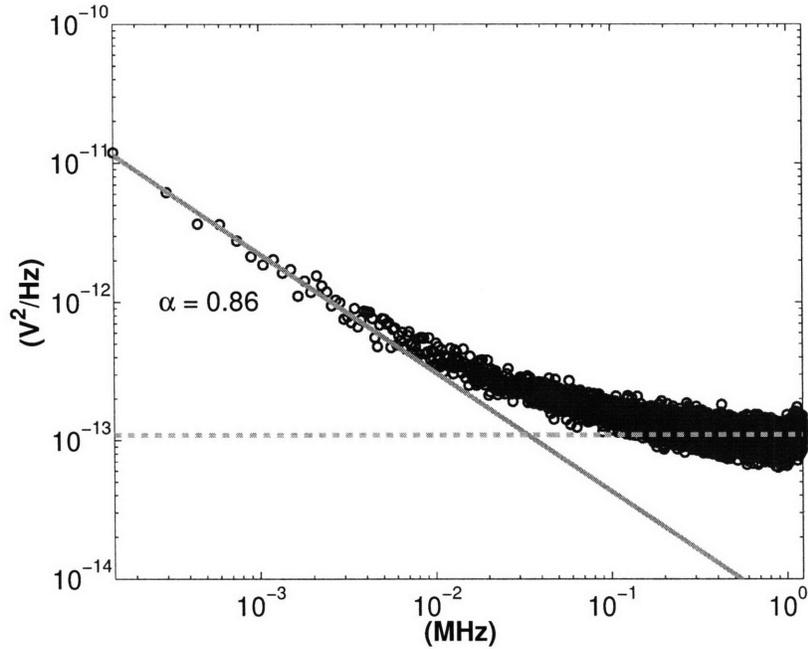


Figure 7-5: Fit of ADC input referred noise PSD to determine preamplifier flicker noise parameters. The flicker noise exponent $\alpha = 0.86$ and the flicker noise PSD for a single preamplifier at 1 Hz $S_{i_n}(1) = 1.3 \times 10^{-17} \text{ A}^2$.

of the preamplifier. Holding everything else in the theoretical calculations constant, the effect of variations in each of these parameters are investigated.

Because the preamplifier input devices dominate the input referred flicker noise of the prototype ADC, the baseband flicker noise can be interpreted as a measurement of the flicker noise of the sum for all the of the preamplifiers in the pipeline. A linear regression on the logarithm of the PSD measurements versus the logarithm of frequency at frequencies significantly below the corner frequency of the aliased spectrum can be used to make a measurement of the flicker noise parameters $S_{i_n}(1)$ and α in the general flicker noise equation

$$S_{i_n}(f) = \frac{S_{i_n}(1)}{f^\alpha}. \quad (7.7)$$

The fit used is shown in Figure 7-5, where the flicker noise exponent $\alpha = 0.86$ and the flicker noise at 1 Hz $S_{i_n}(1) = 1.3 \times 10^{-17} \text{ A}^2$. These flicker noise parameters imply

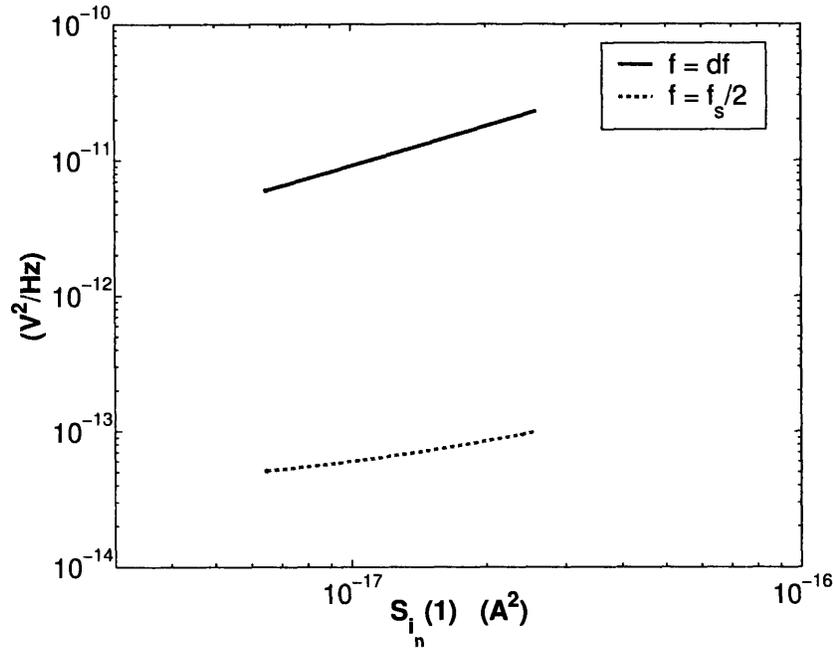


Figure 7-6: ADC input referred noise PSD at $f = f_s/2$ and $f = df$ versus flicker noise of preamplifier at 1 Hz $S_{i_n}(1)$.

a flicker noise corner frequency for the preamplifier before sampling of $f_k = 41$ MHz. The extracted flicker noise parameters are consistent with simulation and measured data for the process.

Since the predicted theoretical value for the noise PSD depends directly on the accuracy of the extracted flicker noise coefficients, the sensitivity of the theoretical noise PSD prediction to the flicker noise coefficients is examined. Figure 7-6 shows a plot of the ADC input referred PSD versus $S_{i_n}(1)$ at $f_s/2$ and df . The PSD at $f_s/2$ is a measure of the apparent white noise, and the PSD at the first FFT bin df is a measure of the baseband flicker noise. Figure 7-6 shows that variation in $S_{i_n}(1)$ has a strong effect on both the baseband and folded flicker noise contributions as expected.

The flicker noise exponent α is the log-log slope of the flicker noise and is defined above (7.7) where α is typically between 0.8 and 1.2 and ideally has a value of 1. Figure 7-7 shows a plot of the ADC input referred noise PSD versus the flicker noise exponent of the input devices of the preamplifier at $f_s/2$ and df . The flicker noise

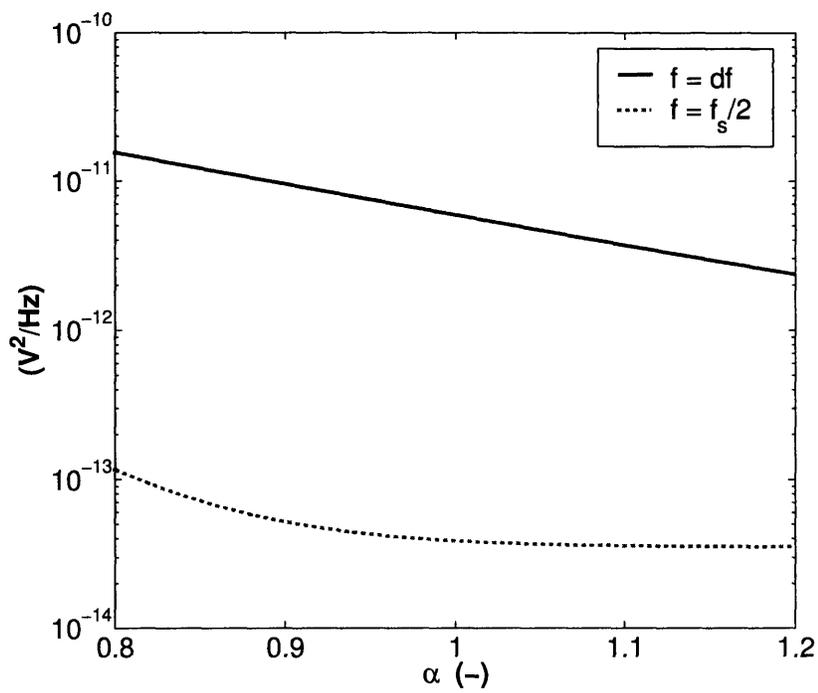


Figure 7-7: ADC input referred noise PSD at $f = f_s/2$ and $f = df$ versus flicker noise exponent α .

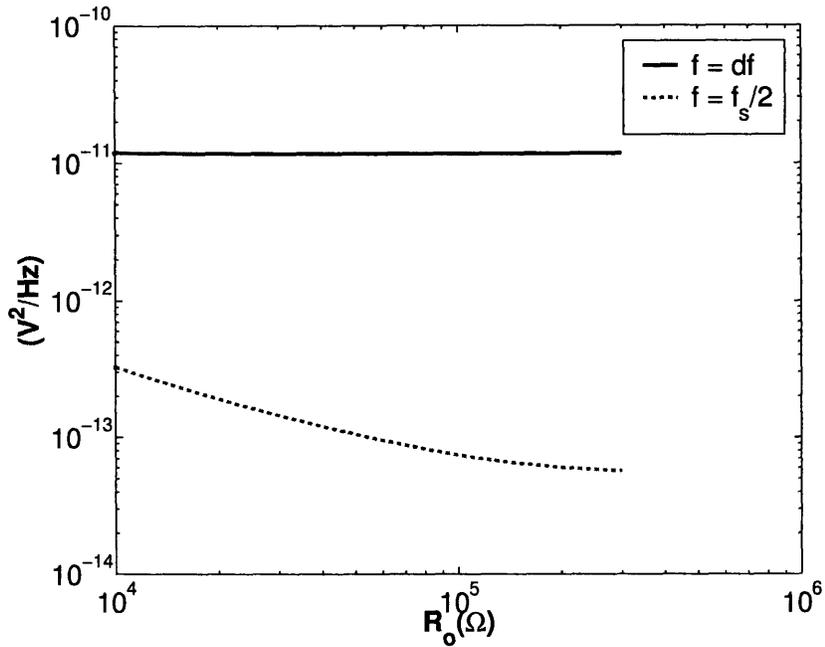


Figure 7-8: ADC input referred noise PSD at $f = f_s/2$ and $f = df$ versus output resistance R_o of preamplifier.

exponent does have a noticeable effect on the magnitude of the folded flicker noise contribution, but an exponent in the range of 0.8 to 0.9 is consistent with simulation models and measured data for the process. For $f_s = 2.4576$ MHz, the frequency of the lowest FFT bin df is 150 Hz for 2^{14} samples, so the baseband flicker noise does change some as α is varied.

The theoretical noise estimate is also sensitive to the noise bandwidth of the preamplifier. The preamplifier response time in the prototype was several time constants, and the output resistance defines the noise bandwidth of the preamplifier. Figure 7-8 shows the plot of ADC input referred noise PSD versus the preamplifier output resistance R_o over a range of values. The output resistance value used from simulation was 130 k Ω . The BSIM3v3 simulation models used to determine the output resistance do not take into account the effects of the pocket halo doping on output resistance, which would tend to result in a lower than predicted output resistance [9] [10] and wider noise bandwidth.

7.4 Discussion

Because the folded flicker noise, preamplifier thermal noise and input sampling noise components dominated the noise over all possible sampling frequencies for the prototype, detailed measurements of the other noise sources in the CBSC gain stage were not possible. The contributions of the other noise sources have been verified with behavioral simulations, but further investigation is needed to verify each of these noise contributions independently with measured results.

It should be pointed out that the preamplifier in the prototype design had too low of an output resistance to behave as an integrator for the fine charge transfer phase. The required output resistance was underestimated when the prototype was designed. One reason for the underestimation was the original assumption that the preamplifier response time was equivalent to the zero-cross delay of the preamplifier. As discussed in Chapter 4, the correct definition is the time which the preamplifier noise is integrated onto its load capacitance. This time can be significantly longer than the zero-crossing delay for a finite gain preamplifier with a slow input ramp. In addition, the comparator was designed to be fast enough to control the coarse phase overshoot without consuming excessive amounts of power. Because the noise analysis was not completely understood at design time, no serious prediction of the noise performance was possible. The goal was a functioning prototype.

The input devices of preamplifier are relatively short and small in area

$$\frac{W}{L} = \frac{3.2 \mu\text{m}}{0.26 \mu\text{m}}. \quad (7.8)$$

Flicker noise could have been lowered and output resistance increased if longer and wider devices were used. However, if device parasitic capacitances are a significant contributor to the preamplifier integration capacitance, additional power would be required to maintain the same speed of operation.

A flicker noise exponent of less than one ($\alpha < 1$) is clearly evident from the measured input referred noise of the ADC. Flicker noise measurement in scaled tech-

SNR	ENOB	Description
65 dB	10.5 b	Thermal noise: Theory
63 dB	10.1 b	Apparent white noise: Theory
62 dB	10.0 b	Apparent white noise with 12 b quantization noise: Theory
59 dB	9.6 b	Apparent white noise with 12 b quantization noise: Measured
58 dB	9.3 b	Apparent white noise with 10 b quantization noise: Measured
53 dB	8.7 b	SNR from FFT test with 10 b quantization noise
52 dB	8.6 b	SNDR from FFT test with 10 b quantization noise

Table 7.2: SNR and ENOB for prototype converter for different combinations of noise sources and harmonic distortion.

nologies have also shown NMOS devices to have flicker noise exponent consistently less than one. Either a non-uniform trap density in the oxide or correlated mobility fluctuations can explain this behavior [61] [62].

Table 7.2 presents the performance of the prototype ADC in terms of SNR and ENOB assuming different combinations of noise sources and harmonic distortion. The first row of Table 7.2 gives the SNR and ENOB of the prototype converter for thermal noise sources only without quantization noise. The SNR and ENOB given in the second row is for the apparent white noise (thermal noise + folded flicker noise), which shows a degradation of 0.4 b in ENOB and 2 dB in SNR. Adding 12 b quantization noise results in a 0.1 b degradation of ENOB. The fourth row in Table 7.2 is from the measured apparent white noise of the converter including 12 b quantization noise. The 3 dB difference in SNR from the theoretically predicted value occurs for the same reasons as discussed above for the difference in measured and predicted noise PSD. The fifth row in Table 7.2 is the measured apparent white noise for 10 b quantization noise which results in a 0.3 b lower ENOB. The last two rows in Table 7.2 are from the FFT test results in Chapter 5. The SNR from the FFT test includes all higher order harmonic distortion (first 9 harmonics removed) and shows a 5 dB reduction in SNR compared to the measured apparent white noise with 10 b quantization noise. The 5 dB reduction in SNR is equivalent to a 0.6 b reduction in ENOB. As can be seen in Figure 5-11, significant harmonic distortion exists across the frequency spectrum.

For the SNDR, the first 9 harmonic components are included, which results in an additional 0.1 b degradation in ENOB.

7.5 Summary

The measurement technique used to extract the comparator noise from the CBSC prototype pipeline ADC was presented. Measured results of the noise performance of the prototype were compared with the theoretical model presented in Chapter 6. It was found that folded flicker noise from the preamplifier was the dominant noise source in the converter. Because of the inaccuracies of modeling parameters, the sensitivity of the theoretical results to key parameters was explored. The results were found to be most sensitive to the flicker noise at 1 Hz for the preamplifier input devices. The flicker noise exponent can also cause significant differences in the amount of folded flicker noise, but the measured noise of the ADC confirms the low flicker noise exponent. The shortcomings of the prototype design were discussed, and the need for further investigation to verify the theoretical models given in Chapter 6 with measured data was highlighted. Finally, the impact of the different noise sources and distortion components had on the performance of the prototype ADC was discussed.

Chapter 8

Conclusion

8.1 Thesis Contributions

The comparator-based switched-capacitor circuit technique proposed in [50] [15] was reviewed, including the description and results of the the prototype 1.5 b/stage pipeline ADC. The proposed technique eliminates the need for high gain op-amps in the signal path, and should be applicable to a wide range of switched-capacitor circuits.

In order to analyze the noise behavior of comparator-based switched capacitors circuits, a set of non-stationary noise analysis techniques were applied to circuit analysis problems in a framework similar to well-known stationary noise analysis methods. A periodic filtering analysis method was used to analyze the noise power spectral density of a series of periodic samples in CBSC systems. The key result is the definition of the appropriate filter for the non-stationary noise source that is periodically sampled. Impulse sampling of the filtered noise can then be analyzed using preexisting noise aliasing methods.

The design of efficient low noise preamplifiers for threshold detection comparators was discussed, and a design methodology was presented. This discussion showed that an ideal integrator represents the lowest power preamplifier implementation for a given speed and noise requirement. In addition, the requirements of threshold detection comparators used in CBSC designs were discussed.

The noise analysis techniques were applied to the analysis of a CBSC gain stage for the prototype. The relative contribution of the noise sources from the switches, the charging current and the comparator were detailed and comparisons were made.

Finally, the periodic filtering analysis of a series of WSS samples of a system was used to generate a theoretical noise estimate for prototype pipeline ADC. It was found that the noise from the preamplifier for the comparator dominated the input referred noise performance of the prototype pipeline ADC. In addition, the folded flicker noise contribution was significant because the flicker noise corner frequency of the preamplifier was greater than half the sampling frequency.

8.2 Future Work

Some suggestions for future work:

- A fully-differential design implementation for CBSC charge transfer. A differential design would require a common-mode feedback circuit to equalize the pull-up and pull-down currents to maintain a constant output common-mode for the stage.
- An offset correction or correlated double sampling method that allows for the removal of constant offsets and low frequency flicker noise.
- Develop methods for constant ramp generation at lower supply voltages where cascoding of current sources is not possible.
- Additional optimization of threshold comparator designs based on the unique threshold comparator requirements outlined in Chapter 4.
- Determine practical limits of potential power reduction for CBSC designs. Explore the possibilities of making the preamplifier integration time t_i much longer than an op-amp settling time constant τ_o for the same linearity requirement.

- Test the CBSC approach in other ADC design spaces (eg. high speed or high accuracy) and switched capacitor applications.

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