A PN Encoded Spread-Spectrum Microwave Radar Based Backing and Parking Aid

by

Charles Campbell Hardy

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of
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Author_ _____

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Certified by____ _____

Anantha Chandrakasan
Thesis Supervisor

Accepted by_ _____

F.R. Morgenthaler
Chairman, Department Committee on Graduate Theses

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Abstract

The pseudo-noise (PN) direct sequence bi-phase shift key (BPSK) modulated microwave radar sensor provides a test platform for radar engineers to explore the feasibility of a commercial automotive backing and parking aid based on this technology. Emitter coupled logic (ECL) digital components are utilized in the construction of the PN code generator and delay units. These are integrated with a microwave transceiver composed of catalog microwave mixers. Laboratory test equipment is used for all microwave, clock, and power sources. Such a system is capable of operating with a clock frequency of beyond 600 MHz and provides detection and ranging of objects with a range resolution of better than 25 cm. It is shown that 25 cm is the finest range resolution any practical backing and parking aid is likely to be able to utilize. Functionality of the system is shown.

Thesis Supervisor: Anantha Chandrakasan

Title: Assistant Professor, EECS

John C. Reed
H.E. Microwave
P.O. Box 23340
Tucson, AZ 85734

January 12, 1996

Professor F.R. Morgenthaler
Department of Electrical Engineering and Computer Science
Room 38-476 M.I.T.
Cambridge, MA 02139

Subject: Master of Engineering Thesis of Charles C. Hardy

Dear Professor Morgenthaler:

I have reviewed the attached thesis of Charles C. Hardy on behalf of H.E. Microwave. The thesis is within the scope of the thesis proposal as previously approved and does not contain any material that is objectionable to H.E. Microwave. It is also approved for technical content.

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I am deeply indebted to many people for making this paper possible.

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It would have been impossible to arrive at this point in my life without the love and support of my family. I am grateful to my mother for her years of encouragement and telling me I could achieve anything I wanted to. I am also especially grateful to my brother and sister-in-law, David and Teri Hardy for the hospitality and support they have shown me over the past years. They have provided me with a place to call home and the encouragement to get through the tough times.

Finally, I must give credit where credit is due for any of my success. I am indebted beyond words to my Lord and Savior for all that my life has been. He has not only preserved my life and provided me the means of achieving, but is also the reason such achievement is even worth pursuing. He truly blesses me far beyond anything I deserve.

Dedicated to the principles of individual Liberty, Freedom, and Sovereignty embodied in the United States Declaration of Independence and Constitution which allow man to rise or fall according to his own industry and the blessing of Providence upon him. May we be wise stewards of that blood-won Freedom.

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1. Background

There is growing interest in the automotive industry in various collision early warning devices suitable for use on over-the-road tractor-trailer rigs, recreational vehicles, and automobiles. At the heart of any collision warning device is a detection and ranging sensor capable of determining whether there are any obstacles in a vehicle's path of travel and whether any such obstacles are in close enough proximity to be of concern. While there is interest in lane-changing aids based on side looking sensors for cars and trucks and collision avoidance or adaptive cruise controls systems based on forward looking sensors, automotive manufacturers are particularly interested at this time in devices which will provide detection, ranging, and appropriate notification to the driver of obstacles located behind his vehicle. Such a device would be valuable as a backing and parking aid. The reasons for the interest in such devices are not hard to find.

1.1 The Dangers of Backing

According to one warning device company's advertising literature, an accident involving a backing vehicle occurs every 1.6 minutes in the United States [1]. According to their literature, many companies report that low-speed, backing accidents account for 20 to 90 percent of all accident costs. Nationally, backing accidents cost over $1.3 billion annually. Most of these accidents are caused by the simple fact that the driver cannot see what is behind his vehicle. Professional drivers operating large trucks with poor rearward visibility are at special risk due to the frequency with which they must back their vehicles up to loading platforms and because of the crowded conditions which almost always exist around such platforms. Even at very low speeds, any collision involving a ten ton truck is likely to be very costly or, if a human is involved, even fatal.

Commercial trucks are not the only vehicles at risk of backing accidents. Large recreational vehicles are subject to very similar backing challenges to those of commercial trucks. Ever increasingly popular recreational vehicles have an added risk in that the drivers of such vehicles usually do not have the same level of driving expertise as drivers of commercial rigs. Even standard passenger cars are not immune to backing accidents as every vehicle has less visibility to the rear than it does to the front. At least one major automobile manufacturer is, in fact, at this time engaging in initial searches for a backing and parking aid to be included on their high-priced, luxury passenger cars.

Manufacturer's and driver's of tractor-trailer trucks and recreational vehicles have long recognized the need for something to ease the challenge of backing large vehicles. Video camera/monitor combinations have been utilized on select recreational vehicles for quite some time in an effort to increase rear visibility [1]. However, commercial drivers have found that an audible warning, supplemented with some sort of simple range indicator, is much more helpful as it does not require their constant visual attention—visual attention which must already be split between both sides and the front of their vehicles—in order to alert them to danger.

1.2 The Advantages of Radar

There are three primary competing technologies that appear capable of providing this type of early warning: laser, sonar, and microwave radar detection and ranging sensors. Microwave radar devices offer certain advantages over the other two technologies. Most importantly, both sonar and laser systems suffer serious performance degradation under

wet, foggy, or icy conditions—the very conditions when driver visibility is at its lowest and system performance is most critical. In contrast, radar sensors are much less susceptible to foul weather interference. The required use of electro-mechanical transducers in sonar systems also reduces reliability compared to microwave systems which do not employ any moving parts. The fact that these transducers must be open to the environment in order to function raises additional concerns. Radar units, on the other hand, may be environmentally sealed safely behind mechanically robust, yet microwave transparent material.

The ability to seal microwave units in environmentally secure fixtures gives them another advantage—aesthetics. Laser units require some type of optically transparent material to transmit and receive through. As already discussed, sonar units require some type of physical opening to function. Neither of these situations lend themselves well to the commercial car market. Designers and owners of the type of expensive cars likely to first have such warning systems incorporated would rather have those systems hidden from view than to interrupt the stylish lines of their cars. A radar unit may be completely hidden behind the plastic bumpers used on modern cars or within a plastic tail light fixture.

1.3 Why Pseudo-noise Encoded Spread Spectrum

A pseudo-noise (PN) encoded, spread-spectrum type of microwave radar system is investigated herein because it has potential for low cost precision ranging. Due to the auto-correlation properties of PN sequences, precision ranging is possible with very little or no signal processing beyond simple correlation, which is accomplished with a single mixer. Coupled with the ease with which PN sequences may be generated using standard digital

components, the ability to avoid expensive signal processing makes such systems very attractive from an economic point of view.

Another advantage of PN encoded spread-spectrum systems is their wide bandwidth. It is a well proven fact that the range resolution obtainable in a fixed amount of operation time is directly proportional to the bandwidth of the waveform incident on the target [2]. Traditional ranging systems use either high slew rate, variable frequency oscillators or devices capable of launching wave pulses of extremely short and well controlled time duration in order to achieve the bandwidth required for the desired range resolution. In the case of a practical parking aid, the required bandwidth is on the order of a GHz. PN encoding offers a much simpler and more economical way to achieve this bandwidth. In addition, such a system provides for a 100 percent duty cycle (continuous wave) target illumination whereas a pulsed system illuminates the target for only a fraction of the operation time. The radar "detectability" of a target is directly proportional to the total energy imparted to the target during a given observation time [2]. Continuous wave transmissions produce the maximum energy on target in a given time. This translates to greater sensitivity at a given transmit power level, or to lower transmit peak power levels for a given sensitivity.

Finally, as ironic as it may seem, the properties of spread-spectrum systems offer real advantages as the electro-magnetic spectrum becomes increasingly crowded. Spread-spectrum systems are relatively immune to interference from standard narrowband devices operating in the same frequency range. Any received narrowband interference energy is effectively spread over a wide spectrum in the spread-spectrum receiver by the same process that collapses the system's own returning spread-spectrum signal into a narrow-band signal. Nor do spread-spectrum systems normally interfere with the operation of

narrowband devices since the radiated energy in any narrow band is very low (often in a narrowband receiver's noise floor) compared to the energy radiated by conventional transmitters. Through judicious choices of encoding methods, it is also possible to minimize or avoid interference between other spread-spectrum devices. Even two or more devices using the same code may be operated without cross-interference under certain conditions discussed in Chapter 4.

2. Scope

The purpose of this project is the design, construction, and functionality verification of a PN encoded, spread-spectrum radar system suitable for use as a test platform. Preliminary tests and data collection on transceiver behavior will also be conducted. This test platform is intended to be used by radar engineers for conducting real world studies into the practicality of implementing such systems in a commercial backing and parking aid. The primary focus of the project is the high speed digital circuitry required to implement the PN code generator and variable delay units. This circuitry was to be designed and constructed using off-the-shelf digital components. All microwave components for this project were to be furnished as lab sources or else purchased as off-the-shelf, catalog items.

3. System Overview

It is worthwhile to begin by examining the actual system requirements for a practical backing and parking aid. However, we must first determine exactly what is meant by the terms 'backing' and 'parking' in the context of vehicles moving in reverse.

3.1 Backing and Parking Defined

Up to this point it the terms 'backing' and 'parking' have been used mostly interchangeably. However there are distinct differences in the situations which each term denotes and the resultant system requirements. The term 'backing' is used to imply a transitory move to position the vehicle for ultimate forward motion. Consequently, specific vehicle position is of very little concern so long as collisions are avoided. Common examples of 'backing' include pulling out of driveway or an angle parking stall in reverse prior to assuming forward motion.

The term 'parking' , on the other hand, is used to denote motion intended to position the vehicle for relatively long-term placement. In this case, specific vehicle position is of prime concern since it is some specific positioning of the vehicle that the driver is seeking to obtain. Also, 'parking' often occurs in much closer quarters than does 'backing'. Three examples of 'parking' which are of most interest here are parallel parking between two vehicles, positioning a tractor-trailer directly in front of a loading dock, or positioning a recreation vehicle in a camping area.

The foregoing definitions are, admittedly, somewhat loose. However, they are sufficient for the purpose of illustrating the difference in system requirements between a device designed to aid in 'backing' a vehicle and one designed to assist with 'parking'. The two requirements affected by this difference in application are the range resolution and the maximum range at which a target may be detected.

A driver 'backing' out of a driveway or parking stall simply needs to be alerted as soon as possible that he is approaching a collision caused by either a course error or by an object

moving into his previously clear path of travel. He may then redirect his attention and take appropriate action to avoid any collision. In contrast, a driver engaged in 'parking' a vehicle is likely to be fully aware of the obstacle behind him, whether it be a loading dock, a parked car, or a picnic table. His goal is not necessarily to avoid these objects all together, but rather it is often to position his vehicle as close to them as possible, if only temporarily, without actually hitting them. Given that the driver is already aware that obstacles exist behind him and since those obstacles are likely to be in close proximity to his vehicle before he is at all concerned about them, he does not require a warning as quickly as he might when 'backing'. However, he does need to know their precise location relative to his vehicle—particularly when the objects are in his vehicle's blind spots.

It is clear that while a simple 'backing' aid may get by quite adequately with relatively course range resolution so long as it has a relatively long maximum detection range, a 'parking' aid must have much finer range resolution if it is to be of real assistance to the driver. However, it does not require as much maximum range. All else being equal, improved range resolution will not adversely affect a 'backing' aid and increased maximum range will not adversely affect a 'parking' aid. So long as both requirements may be met simultaneously, the two units may be combined into one. In as much as every vehicle engages in both 'backing' and 'parking' maneuvers, it is economically desirable to combine these functions rather than building and installing two separate units.

3.2 System Requirements

To be of benefit, a backing and parking aid system must be capable of detecting objects located behind the vehicle and providing information to the driver both quickly and

accurately enough for him to take corrective action. Clearly, the maximum range at which an object must be detected in order to provide adequate warning is directly proportional to the rate of closure between the vehicle and the obstacle. Since most backing accidents involve a vehicle backing into a stationary obstacle, the rate of closure may be assumed to be simply the vehicle's own velocity. Vehicle velocity during backing is quite low, not much more than 5 mph or about 8 kph. During tight parking maneuvers it is likely to be even lower.

At 5 mph or 8 kph, a vehicle travels just over 7 feet or about 2.25 meters each second. The National Highway Transportation Safety Board has estimated that at freeway speeds an early warning of even 1/2 second would eliminate almost 90% of all collisions. At the much slower speeds present during backing and parking, a one second warning would, therefore, be more than adequate. Further, any practical backing and parking aid must be able to detect targets even when the vehicle is moving extremely slowly or not moving at all. This means that any objects in the detectable range will activate the alarm immediately upon the unit being automatically armed by shifting the equipped vehicle into reverse. Thus, the driver will be alerted to these hazards before his vehicle has even begun moving. So two meters may be considered an adequate minimum length for the maximum detection distance even in a 'backing' aid.

The range resolution which is required is a little harder to determine. Ideally a driver 'parking' a vehicle would like to have as much resolution as possible so that he may accurately position his vehicle extremely closely to objects behind him. In fact, current practice for many drivers is to back slowly until they actually make contact with the object behind them and to then pull forward slightly. Clearly this practice is ripe for causing damage or injury, especially if some unseen and unintended object—such as a human

being—gets between the vehicle and the object. This very situation is of grave concern around the busy tractor-trailer loading docks previously mentioned. A parking aid should provide adequate range resolution to discourage this "bump and stop" approach.

However, before designing a sensor with extremely fine range resolution, another requirement bears some discussion. No driver is the least bit interested in the distance between the sensor and the object. The distance of concern is the distance between the object and the vehicle. Even with the sensor mounted directed to the vehicle's rear bumper, these two distances are not necessarily the same as illustrated in Figure 3-1. In the figure, both obstacles 1 and 2 are r cm from the sensor. However, while obstacle 2 is indeed r cm away from the vehicle, obstacle 1 is only r[cos(θ)] cm away. As r becomes smaller and θ becomes larger the discrepancy between the distance to the sensor and the actual distance to the vehicle grows until it reaches a maximum when θ equals 90°. This occurs as the vehicle's rear bumper comes into contact with the obstacle. At this point the obstacle is still w cm away from the sensor but 0 cm away from the vehicle. It is clear, in this case, that increasing the range resolution of the sensor to less than w cm results in absolutely no increase in system utility.

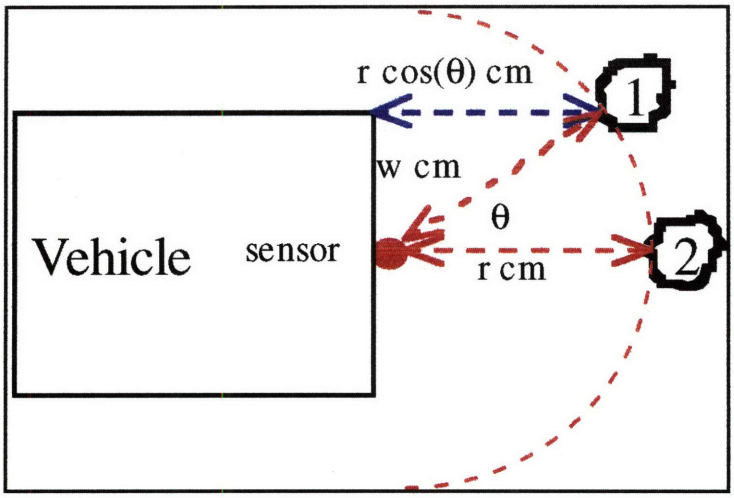

Figure 3-1: Single Sensor

A tractor-trailer rig or large recreational vehicle may be two meters or more in total width allowing w to reach 100 cm. This is not nearly fine enough range resolution for a practical parking aid. The immediate solution is to somehow decrease w. Decreasing the width of vehicles is not possible. However, an attainable solution is depicted in Figure 3-2. Here, the distance w has been cut in half by the addition of a second sensor.

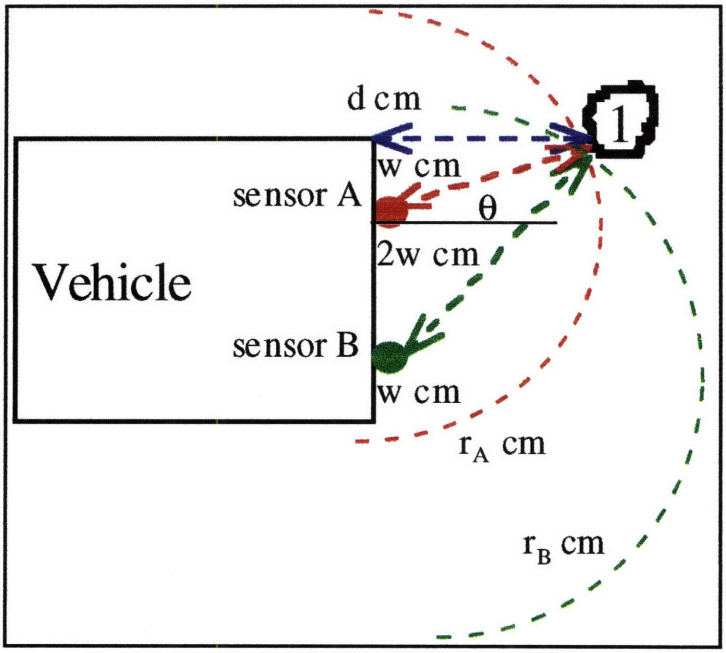

Figure 3-2: Multiple Sensors vs. Point Target

Sensor A measures a distance r_A cm to the obstacle. The actual distance between the obstacle and the vehicle is, once again, $r_A[\cos(\theta)]$ cm. However, with w halved, the amount of error between the actual distance and the measured distance as the obstacle is contacted is now only 50 cm rather than 100 cm. Range resolution of the sensors may now be set to 50 cm with realizable system benefits.

One might notice that multiple sensors offer an added benefit beyond simply decreasing the distance w. Not only does sensor A measure a distance to the obstacle, but sensor B also measures a distance to the obstacle, r_B cm. The obstacle is now constrained to lay on the intersection of two known circles defined by the simultaneous equations (assume the origin at sensor A), $x^2+y^2=r_A$ and $x^2+(y+2w)^2=r_B$. The exact position of the obstacle may be

readily computed from these two equations with an accuracy directly proportional to the accuracy with which r_A and r_B are known.

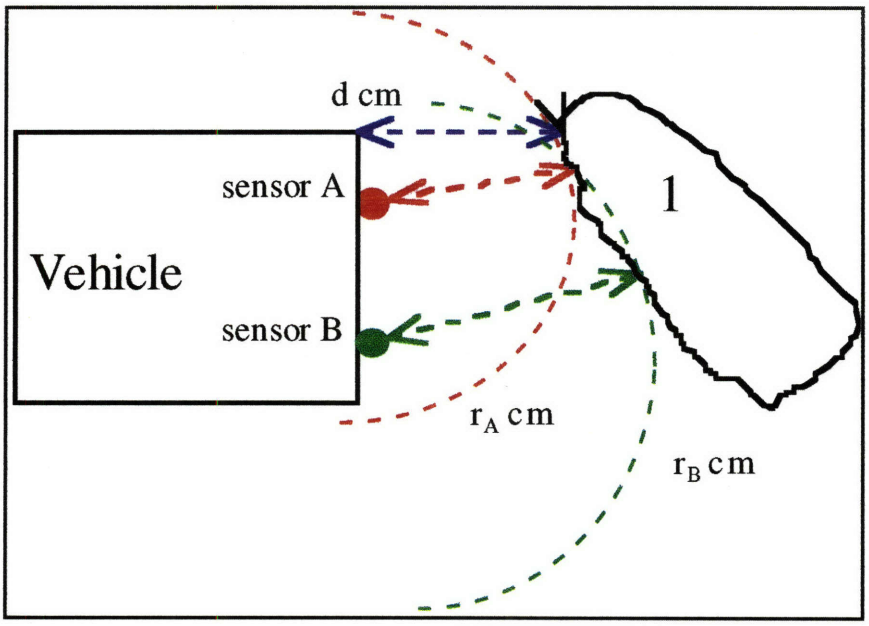

Figure 3-3: Multiple Sensors vs. Wide Target

It must be emphasized that the foregoing calculations may be properly applied only to an obstacle such as a fence post, power pole, or person, which approximates a single, discreet target. Figure 3-3 illustrates a scenario in which a vehicle is backing into a wide, distributed target at an oblique angle. Any number of very common obstacles from loading docks to other vehicles to sides of buildings may be thought of as such wide, distributed targets. The problem with such obstacles is in the fact that it is impossible to predict which portion of the obstacle the sensor is going to pick-up at any given moment. Here, sensor A and sensor B are picking up two different points of the obstacle and thus its exact location cannot be determined. Once again, the accuracy of the system is limited by the cosine error and the point of diminishing returns is quickly reached in striving for greater system range resolution. The finest range resolution obtainable is limited by the greatest distance, w, which any target may be from the nearest sensor when it comes into contact with the vehicle.

It should be feasible through proper placement of the individual sensors and alignment of the range gates to provide the driver with a "pre-contact" warning which, in the ideal case of a wide target approached perpendicularly, would indicate the target was less than some small distance, say 2 or 3 cm, from the vehicle. This would eliminate the need to "touch and stop" when backing directly into a loading dock or wall. It must be stressed again, however, that even this trick offers no help when the target is approached at an oblique angle as is often the case when parallel parking.

3.3 System Components

The various system components are depicted in Figure 3-4. The parking and backing aid is comprised of four main subsystems: The pseudo-noise code generator, the microwave transceiver, a code correlator, and the detector/display. The code generator is comprised of off-the-shelf Emitter Coupled Logic (ECL) digital components and is detailed in Chapter 4.

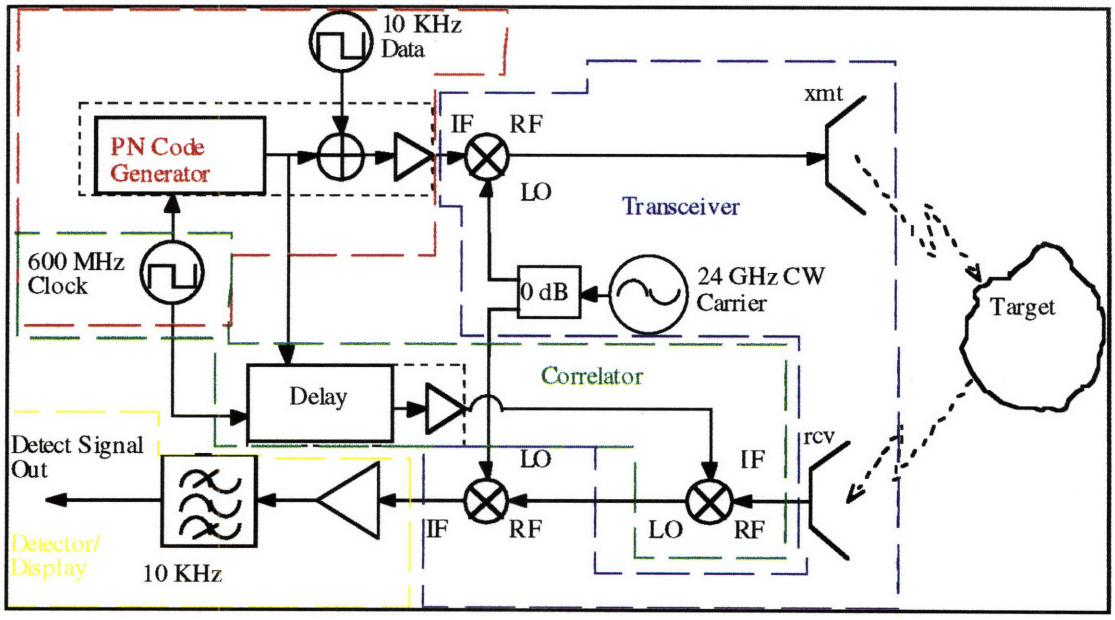

Figure 3-4: System Block Diagram

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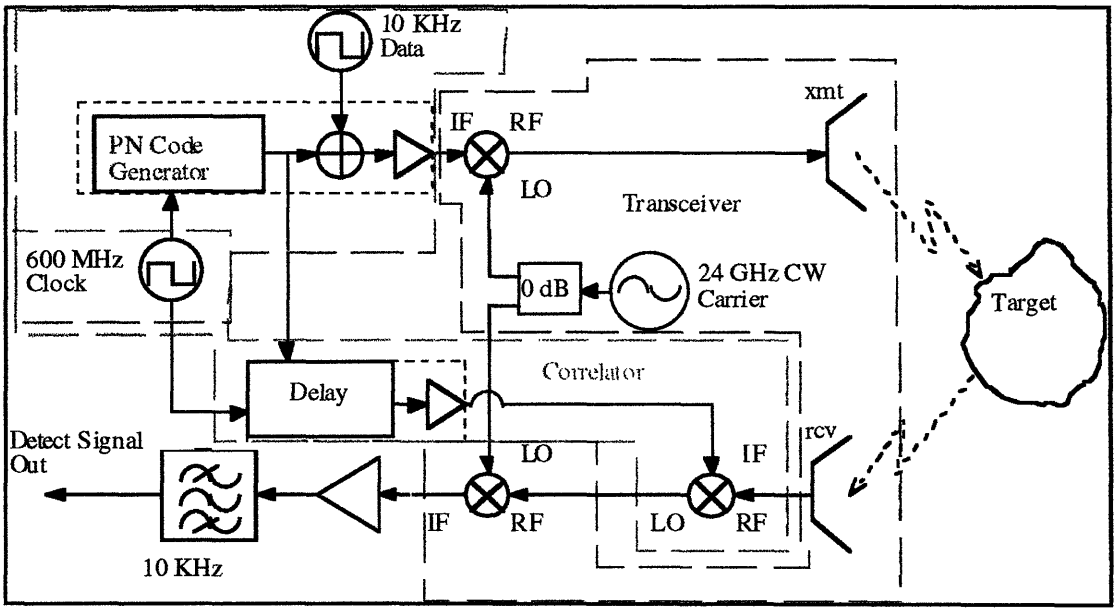


Figure 3-4: System Block Diagram

The PN code is used to directly Bi-phase Shift Key (BPSK) the microwave frequency continuous wave (CW) carrier. This BPS Keying results in a spectrum bandwidth which is twice the PN code rate.

The microwave transceiver is comprised of the microwave oscillator and two, off-the-shelf, or catalog mixers. The transmit mixer is driven by the CW carrier and switched by the PN code to produce the spread-spectrum wave. The receiver mixer, driven by the same CW carrier, comprises a coherent receiver and is used as a down converter from rf to baseband. A primary point under investigation is whether such a single channel coherent receiver would function acceptably without signal dropouts when used against real-world targets. A laboratory microwave source was used for the microwave oscillator. The transceiver is examined in Chapter 6.

The correlator is comprised of a delay unit and a catalog mixer. The delay unit is detailed in Chapter 5. The correlatot is discussed further in Chapter 6. The delay unit is composed primarily of ECL digital devices. The PN code is fed into the delay unit, delayed a specific time period, and is then used to switch the correlator mixer just as the non-delayed PN code is used to switch the transmit mixer. This time the switching results in a collapse of the received spread-spectrum waveform into a narrowband waveform whenever the incoming signal and the delayed PN code correlate. This narrowband wave is then down converted to baseband by the receiver mixer. When the incoming signal and the delayed PN code do not correlate, any received energy is spread over a wide spectrum and only low-level noise is down converted.

The detector/display is made up of a baseband amplifier, a bandpass filter, a peak detector, and a display unit. The baseband amplifier and bandpass filter are detailed in Chapter 7. The bandpass filter is used to isolate the fundamental harmonic of a 10 KHz square wave which is encoded on the transmitted waveform. Upon proper correlation of the received spectrum, this 10 KHz wave is recovered. Its presence and amplitude indicates the presence of a target. Triggering off this low frequency wave rather than a simple DC level eliminates ambiguities caused by DC bias fluctuations which are common in the receiver electronics. A cathode ray oscilloscope (CRO) is used for detection and display purposes.

4. PN Code Generator

The heart of a pseudo-noise (PN) encoded spread-spectrum system is a (PN) code generator. PN codes are attractive because of their auto-correlation properties and the ease with which they may be generated. Such codes are readily generated from standard digital components. In fact, the only components required for PN code generation are registers and exclusive or (XOR) gates. The block diagram of the PN code generator constructed is shown in Figure 4-1. The actual code generation portion of this circuit consist of three Motorola MC100EL30, Triple D-Flip-Flop chips and an MC100EL07 XOR gate. The second XOR gate and the microwave amplifier serve to drive the transmit mixer properly.

The nine flip-flops are wired serially with a common clock as a nine stage shift register. The output from the fourth and ninth stages are fed back through the XOR gate to the input of the first stage. This feedback configuration was taken directly from Dixon [3]. This constitutes a shift register maximal sequence generator. Computer simulation tools for

circuits or layouts were not readily available. Therefore, debugging was done at the board level for all designs throughout.

4.1 Maximal Sequence Codes

A maximal code is, by definition, the longest code which may be generated by a shift register of a given length. The length of such a sequence is 2^n-1 chips where n is the number of stages in the shift register—in this case nine. The term "chip" is used to denote the bits of the generated code and is traditionally used in spread-spectrum communication systems in lieu of the more familiar "bit" in order to avoid confusion between the bits of data being encoded and transmitted and the bits of the code sequence doing the encoding and spreading. The term derives from the fact that in spread-spectrum communication systems, the PN code rate is much higher than the data stream bit rate, thus the PN code is said to "chop" the data stream bits into small "chips" as those bits are encoded. This same terminology will be used throughout this paper to avoid confusion.

Maximal sequence codes have a number of well defined properties of interest in the system under investigation which are enumerated by Dixon. These include:

1. Every possible state, or n-tuple, except the all-zeros state, of the given shift register will occur once and only once during each cycle of the code. The all zero state does not occur and an inspection of the block diagram will immediately show that should it ever occur, it will never be exited, in effect turning off the code generator.
2. Autocorrelation of a maximal sequence is -1 for all values of phase shift except for the 0±1 phase shift area. In this area the correlation varies linearly from -1 to 2^n-1 (the sequence length) with the maximum value occurring at zero phase shift.

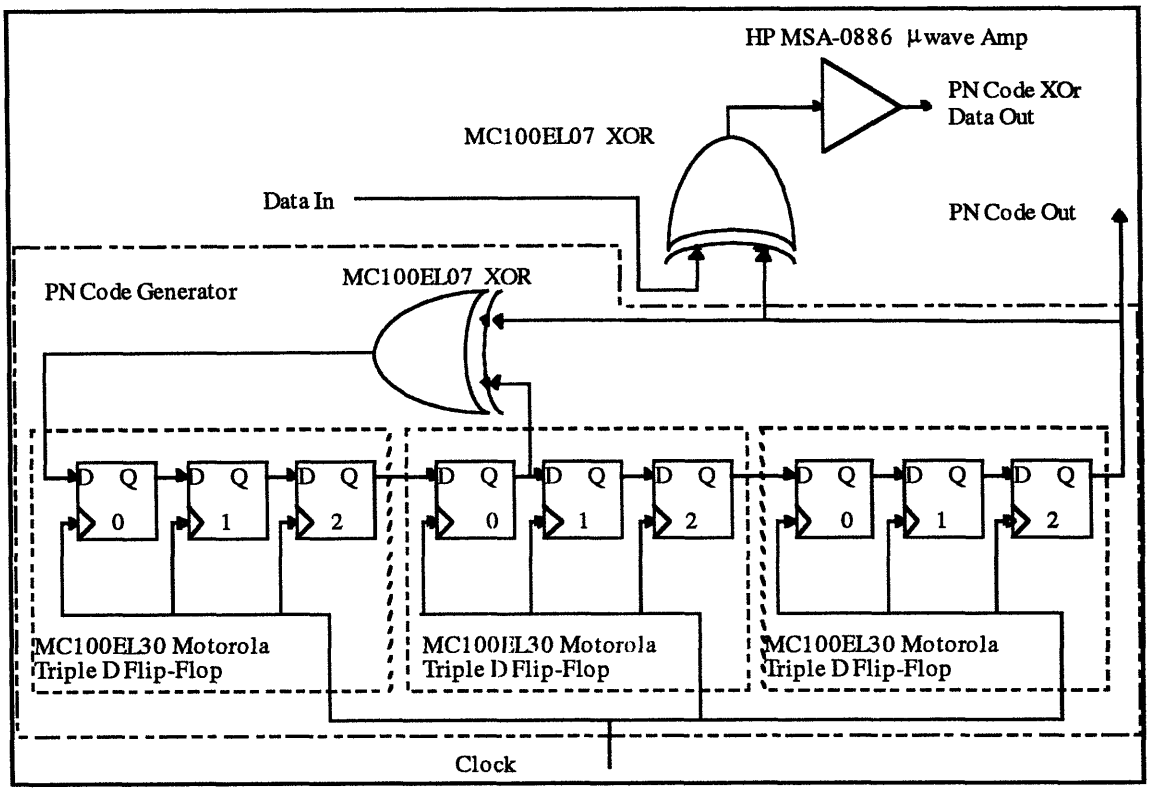


Figure 4-1: Code Generator Block Diagram

3. Even though the codes are known as pseudo-noise codes, the statistical distribution of ones and zeros is well defined and always the same.
4. There are exactly 2^{n-1} ones and exactly 2^{n-1}-1 zeros in a maximal code sequence.

There is another property of maximal code sequences which is very useful in communication systems and which is exploited in this system as well. Every communications system must have some means of encoding the data to be sent. While most of the standard modulation techniques may be carried out on the carrier wave prior to it being spread, the most useful technique for transmitting data in a spread-spectrum communications systems is through the use of code modification. Code modification means that the PN code used to BPSK the CW carrier is changed in such a way that the information being transmitted is embedded in it. This must be done while preserving the other properties of maximal codes. Fortunately, there is a simple method of doing this.

First the data is digitized. Then the digital data bit stream is modulo-two added (XORed) to the PN code. The XOR process has the effect of inverting the PN code each time a transition occurs in the data bit stream. The resultant PN code, which is now code ⊕ data, retains all of its desirable properties. The data may be extracted on the receiving end by modulo-two adding the received code with an unmodified replica of the original PN code. This modulo-two adding results in (code ⊕ data) ⊕ code which is equal to simply data since A⊕B⊕A=B.

This property is exploited by XOR-ing the PN code with a 10 KHz square wave (10 KHz alternating bit stream) prior to spreading the CW carrier. A non-modified copy of the original PN code is delayed and used to drive the correlator. Upon correlation, rather than a DC level being present, the 10 KHz square wave will be recovered. The 10 KHz signal will be referred to hereafter as the data wave since it is in the same position as a data stream in a communications system.

In a communications system, one would most likely have to take care to ensure that the data bit stream and the PN code are synchronized in some way so that an inversion of the code only takes place only on a valid clock transition. The possibility of an inversion taking place mid chip is fairly high if the PN code rate is only 10 or 20 times the data rate as is often the case in communication systems. However, given the data rate of 10 KHz and the case of a 600 MHz code rate present in this system, there are 60×10^3 chips for every bit of data. This means that over 117 cycles of the code are transmitted for every bit of data or 235 cycles of code for every period of the square wave. Even if the extremely unlikely worst case of inverting the code mid chip occurred every single time the data bit stream

changed, correlation would not be affected as it would only be one wrong value in every $60x10^3$.

Property 3 offers the potential of being able to operate multiple systems using the same code simultaneously without cross-interference so long as it may be guaranteed that any signal received from another unit is at least one full chip out of synchronization with the receiving unit's signal. If systems were stationary, their clock could be synchronized and their codes offset by appropriate amounts to ensure this. While this is not possible with mobile systems, further research may indicate that the probability of interference from another identical unit is too low to warrant concern. The probability that two systems will actually be aimed at each other in close enough proximity and with their codes properly aligned so as to result in interference does intuitively seem low for a system that only operates when the automobile is in reverse.

4.2 Code Requirements

There are two parameters of primary concern in selecting a PN maximal code: the code length and frequency. The code frequency determines the bandwidth of the transmitted waveform and thus, the range resolution of the system. The code length determines the maximum range which may be unambiguously measured by the system. Together, these two parameters also determine the code repetition rate.

Having gone through the discussion in Section 3.2 it was determined that a range resolution of 25 cm would be appropriate for this test radar. As will be shown in Chapter 6 the range resolution is determined by the frequency of the PN code according to, $resolution = \frac{c}{2f_{code}}$. Given a desired range resolution of 25 cm then, the required

frequency is given by, $f_{code} \approx \frac{300X10^6 m/s}{2*0.25m} = 600MHz$. A range resolution of 15 cm would require a code frequency of 1 GHz.

Target range is measured in spread-spectrum radar systems by correlating the signal returned from obstacles with an internally delayed version of the signal. The amount of internal delay required for peak correlation with the returned signal is equal to the two-way travel time of the returned signal. Given that electro-magnetic waves propagate through air at a known and constant velocity, the speed of light, c, the one way distance, or range to the target may be readily determined from the internal delay. This eliminates the need to measure the time interval between launching a wave pulse and its return to the system as is done in pulse radar systems. This allows the use of CW for 100% duty cycle target illumination while also providing for precision ranging.

However, it imposes a constraint on the maximum target range which may be measured without ambiguity. A pulse radar system must wait long enough between launching subsequent wave pulses to ensure that only one pulse is in transit between the radar and the target and back in order to accurately time the transit interval. Similarly, a PN encoded spread-spectrum radar system must provide that only one cycle of code is in transit to the target and back at any given moment. If more than one cycle of the code is permitted to be in transit at a time, the radar will have no way of determining which returning cycle is correlating with the internally delayed code and ranging ambiguities will occur.

The maximum range (two-way distance) that a single cycle of code will span is,

$$range_{\max} = \frac{chiplength * codelength}{2} = \frac{c * codelength}{2f_{code}}. \qquad (4\text{-}1)$$

However, the maximum range that may be determined without ambiguity is actually less

than this. There is no way to guarantee that there are no targets slightly beyond the maximum range spanned by a single cycle of the code. Any such target may be ranged ambiguously. The solution is to use a code length which is longer than the maximum range of interest. If the code is long enough, it may be arranged that any energy returned from targets beyond the code's maximum span will be sufficiently attenuated enough by the round trip to the target to be below triggering thresholds.

Given a maximum range of interest of 2 meters as determined in Section 3.2, the shortest code length which will span this range is readily determined from Equation 4.1. This length is: $codelength > \frac{2 f_{code} * range_{max}}{c} \approx \frac{2 * 600MHz * 2m}{300X10^6} = 8chips$. To prevent range ambiguities the code will need to be longer than this. In order to be absolutely certain that any targets located beyond the maximum span of the code would return no appreciable energy to the system an order of magnitude increase in code length was chosen.

A 7 bit shift register is the shortest one capable of exceeding 80 chips in length (2^7-1=127). However, the flip-flops used come three to a package. So long as three packages are required, all nine flip-flops might as well be used giving a 2^9-1=511 chip code. The appropriate feedback connections were obtained from commonly available tables reprinted in Dixon [3]. The connections were verified for proper operation using a software representation in a computer simulation prior to construction of the physical circuit. The test code in "Mathematica" and results are reproduced in Appendix 1.

The autocorrelation of the resultant maximal code was also verified using Mathematica. Autocorrelation is expressed as the number of agreements minus the number of disagreements when the code is compared chip by chip with a phase shifted version of itself. Once again, the code is printed in Appendix 1. The autocorrelation function, which

is a plot of the autocorrelation over all phase shifts is shown in Figure 4-2. The plot verifies the accuracy of the feedback connections by demonstrating the expected correlation function. An expanded view around the zero phase shift portion of the plot is shown in Figure 4-3.

Having selected the code frequency and length, the code repetition rate may now be determined. The code repetition rate is given by:

$$reprate_{code} = \frac{f_{code}}{codelength} = \frac{600MHz}{511} \approx 1.17MHz. \qquad (4\text{-}2)$$

4.3 PN Code Generator Circuit Design

The system being considered was designed and built to be a test platform for experiments

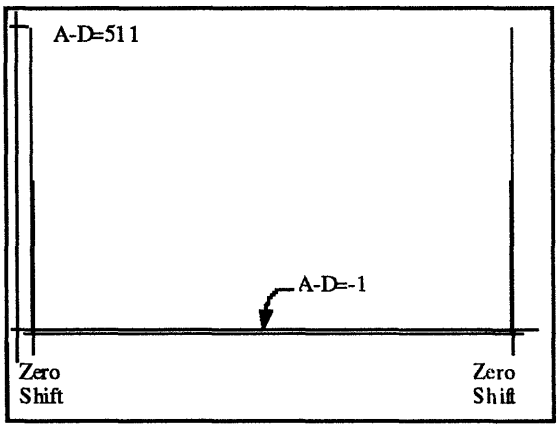


Figure 4-2: PN Code Autocorrelation

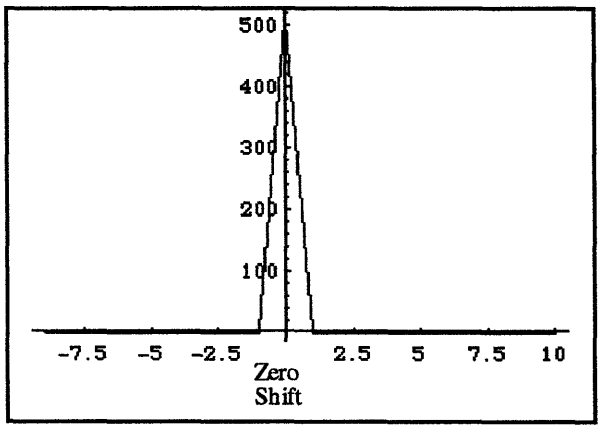


Figure 4-3: Autocorrelation Detail

on PN encoded spread-spectrum radar. One requirement was that it be built using existing, off-the-shelf components to keep both costs and construction time reasonable. Another requirement was to provide flexibility in both the code frequency and the carrier frequency. Even though an initial code frequency of 600 MHz was selected, an eye was kept on the

desirability of running the system at 800 MHz, 1 GHz, or faster. The only digital components that offered this operation speed were in the Emitter Coupled Logic (ECL) family. Motorola has an acceptable selection of ECL components which were readily available and promised operation frequencies in the 1 GHz plus range.

When compared to the TTL or CMOS logic families, ECL offers some unique design challenges. However, given that they were the only devices capable of the required operation frequency, there was really no alternative. A primary concern for many when considering ECL devices is their high power consumption. While it is true that the static power consumption of ECL devices is higher than for CMOS, ECL devices' power requirements remain constant over frequency. CMOS devices' power requirements, on the other hand, increase with frequency. At frequencies as low as 20 MHz, CMOS power consumption will begin to rise above ECL requirements [4].

ECL devices have low impedance outputs and high impedance inputs which are ideal for driving 50Ω to 130Ω controlled impedance lines. These lines are commonly fabricated on microwave substrates. Surface mount packages allow these devices to be integrated directly into a microwave circuit. While the boards built for this investigation were not integrated beyond the inclusion of a microwave amplifier for drive purposes, the ability to eventually include all components on a single board is an attractive feature.

Another novelty is the fact that ECL devices traditionally use a negative power supply. This is done because all voltage references are to the most positive rail, V_{CC}. Any noise on this rail couples directly, one-to-one onto the outputs. Since it is usually much easier to keep a ground plane quiet than it is a power supply, the ground plane is used as V_{CC} while a negative supply is used for V_{EE}. The Motorola devices used call for the most negative

rail, V_{EE}, to be nominally set at -5.2V. Logic swings are nominally between -0.7V for a high (1) and -1.6V for a low (0).

The most challenging requirement of ECL devices in terms of designing a layout is their need for a pull-down resistor on every driven line. The requirement to include some type of pull-down on every drive line conflicts with the desire to pack components as close as possible so as to minimize the lengths of such lines. At 600-1000 MHz, wavelengths are as short as 30 cm. This means that a wave transitions from its minimum to maximum values in 7.5 cm. The Motorola ECL application guide suggests that any line with a length over approximately 0.7 cm must be treated as a transmission line [4].

From transmission line theory we know that any wave traveling down a line will be partially reflected back down the line upon reaching any impedance mismatch. The magnitude of the reflection is described by the reflection coefficient, ρ.

$$\rho = \frac{(z_1 - z_0)}{(z_1 + z_0)} \qquad (4\text{-}3)$$

where z_1 = encountered impedance and z_0 = the characteristic line impedance.
The reflected wave will travel back down the line until encountering another impedance mismatch at which point it will be re-reflected back down the line. Such reflections will continue until a steady state signal value is reached. It is important, therefore, for the pull-down resistors to be properly matched to the line impedance.

A non-woven Teflon microwave substrate was chosen with an eye toward future microwave integration. The substrate is .031" thick with a relative dielectric constant of 2.94 and is plated on both sides with 1 oz/ft^2 copper. Therefore the copper plating is .0014" thick. The plating on one side of the substrate is left intact forming a ground plane.

The plating on the other side is etched to produce traces. With the ground plane separated by the substrate, these traces constitute microstrips. In an effort to minimize coupling between adjacent lines, line widths were kept to a minimum. The minimum microstrip line width recommended by the fabrication shop was .007". The characteristic impedance of a microstrip line is given by [4]:

$$z_0 = \frac{87}{\sqrt{(\varepsilon_r + 1.41)}} \ln\left[\frac{5.98 * h}{0.8w + t}\right] \qquad (4\text{-}4)$$

where:

ε_r = Relative Dielectric Constant of the Substrate

w = Width of the Signal Trace

t = Thickness of Signal Trace

h = Thickness of the Substrate (all dimensions in inches).

This equation is accurate to within ±5% when $0.1 < w/h < 3.0$ and $1 < \varepsilon_r < 15$. In addition, the ground plane is assumed to extend beyond the edge of the trace by at least the width of the trace. Although the first constraint is not met in this case, the formula will still give a workable estimate of line impedance as verified by a computer simulation. With the values above Equeation 4-4 gives a value of 136.7Ω for a line width of .007".

The propagation delay for a signal on a microstrip line is described by [4]:

$$T_{PD} = 1.016\sqrt{0.475\varepsilon_r + 0.67}\, ns/foot. \qquad (4\text{-}5)$$

For the substrate employed in this system then, the propagation delay is 1.46 ns/foot or 47.9 ps/cm. Compared to the 1 ns period of a 1 GHz wave, the importance of minimizing line lengths becomes clear. The capacitance per unit length is given by $C_0 = T_{PD}/Z_0$. Utilizing equation 4-4 and equation 4-5 the capacitance of these traces is found to be 350 fF/cm.

There are two primary methods of terminating a transmission line: series termination and parallel termination. Parallel termination allows the fastest circuit termination as RC delays are minimized. Parallel termination involves terminating the line to a voltage, V_{TT}, through a resistor with a value equal to the characteristic impedance of the line. A judicious choice of V_{TT} will minimize power dissipation. The Motorola ECL devices are designed to drive into a V_{TT} of -2V. The problem with this scheme is that it requires a second power supply, V_{TT}.

An alternate approach is to use Thevenin equivalent termination which consists of a resistor divider network comprised of two resistors, R_1 between V_{CC} and the terminated line, and R_2 between the line and V_{EE}, to bias the line to the desired voltage. If the resistance of the divider network, which is simply the parallel combination of the two resistors, is equal to the characteristic impedance of the line, no reflections will occur. The resistors must, therefore, satisfy two conditions:

$$R \,//\, R_2 = Z_0 \qquad (4\text{-}6) \qquad \text{and} \qquad V_{EE}\frac{R_1}{R + R_2} = V_{TT}. \qquad (4\text{-}7)$$

Solving equation 4-6 and equation 4-7 simultaneously for Z_0=130Ω and V_{TT}=-2V yields R_1=220Ω and R_2=360Ω.

An impedance of 100Ω was desired on the clock lines. Using equation 4-4 a line width of 0.020" was decided upon. To simplify the interface between the lab source that would act as the clock and the ECL components, AC coupling was decided upon. It was prudent

then to bias the clock lines to the midpoint between an input high level, V_{IH}, and an input low level, V_{IL}, or about -1.3V. Plugging these requirements into equations 4-6 and 4-7 yielded values of 130Ω for R_1 and 400Ω for R_2 on these lines.

Finally, adequate power lines had to be laid down. Each triple D flip-flop consumes 62 mA. The XOR gate uses 17 mA. This gives a total current of 203 mA through the integrated circuits. Every driven line also has a direct, resistive connection between V_{CC} and V_{EE}. This connection consists of a 220Ω resistor in series with a 360Ω resistor for a total resistance of 580Ω. There are a total of 14 such networks on the board in parallel between the supply rails. There are also three networks on the clock lines, each of which has an equivalent resistance of 530Ω. Therefore, the total resistance between the supply rails is: $\frac{1}{14\left(\frac{1}{580\Omega}\right)+3\left(\frac{1}{530\Omega}\right)} = 34\Omega$. These resistors draw 5.2V/34Ω = 153 mA. This gives a total current demand on the board of 356 mA.

One ounce microstip line will carry 53 mA per .001" of width while incurring a 10° C temperature increase above ambient according to ANSI standards. Trace widths of .020" were decided upon for the power lines to give a healthy margin of safety. As per Motorola's recommendation, the power line is bypassed with a .22 μF capacitor as it comes on board. The power line is further bypassed with a .01 μF capacitor as near as possible to each package's V_{CC} pin and as close as possible to the clock line termination resistors. Direct bypassing to each V_{EE} pin proved to be unnecessary.

A detail of the schematic of the PN Code Generator is shown in Figure 4-4. For simplicity, stages 1 though 6 are omitted since their interconnects are identical to those shown for stages 7 though 9. The figure also shows the feedback path through the XOR gate, the 10 KHz "data" signal input through the second XOR gate, and the output driver amplifier. The schematic omits the bypass capacitors.

The ECL components used all have differential outputs. Generally, these may be treated as simply the true and compliment of the output. However, it is advisable to terminate both outputs anytime either output is used. This is done in order to minimize switching current changes which may end up being translated to noise on the power line. Fortunately, properties number 1 and 4 of maximal codes, discussed in section 4.1 give some relief from this problem. Through most of the code sequence, when a given flip-flop transitions from one state to another, there is another flip-flop in close proximity which is making the opposite transition. This should minimize the changes in current load due to switching even without the termination on the unused half of output pairs. Thus, termination on the unused compliment outputs was omitted without introduction of problems.

It was found that the XOR gate input was very sensitive to variations in the voltage levels driving it. In particular, the V_{IH} levels could not vary by more than a few tens of millivolts or else gate performance was adversely affected. Such accuracy was a little more than the lab function generator could reliably and easily produce so a series resistor of 400Ω was added on the input line. This acts in conjunction with the termination resistors to form a voltage divider reducing the voltage variations from the function generator by a factor of 4. This allows the function generator to be set to give a 2 V_{p-p} wave rather than a 500 mV_{p-p} wave.

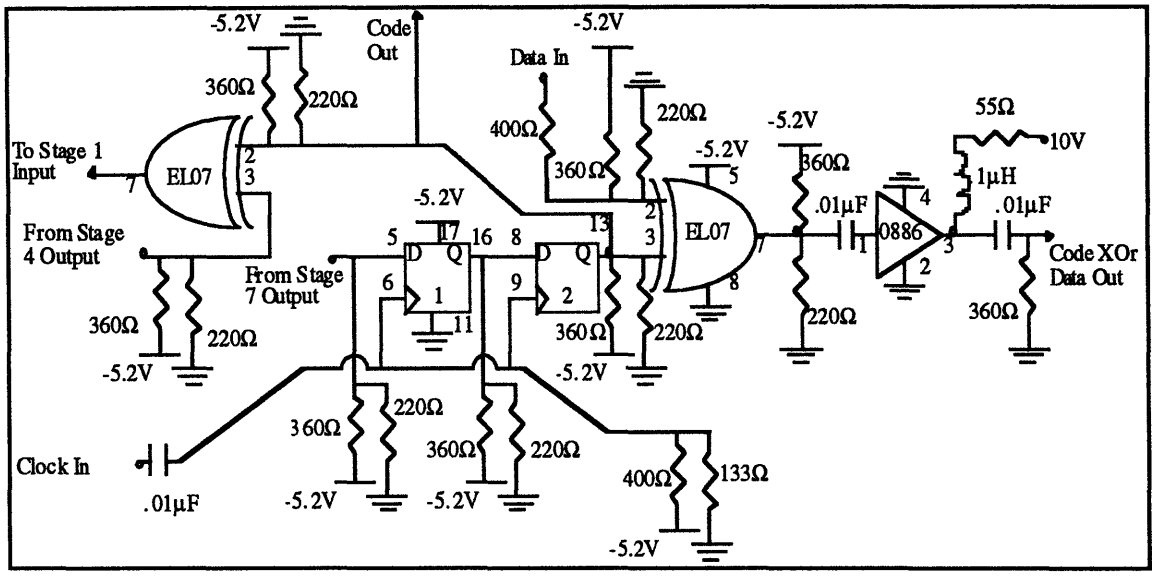


Figure 4-4: Code Generator Schematic Detail

The same Thevenin termination was used on this line as on the other lines to reduce the required offset on the data signal to 400 mV while still providing a valid low input to the XOR gate in the absence of any data wave. This logic low input to the XOR gate allows the gate to function properly and the PN code to be transmitted unmodified in the absence of any data signal. Using AC coupling rather than DC coupling on this line would have eliminated the need for offset altogether and is used on later versions. However, inasmuch as the extreme sensitivity of the XOR inputs was not known until after the board was built and testing was conducted, no capacitor was included on the board. It was easier to adjust the offset of the function generator than to resect the input line and add a capacitor.

The clock inputs on the flip-flops, on the other hand, showed very little sensitivity to variations in drive voltage levels. In fact, they are driven using a laboratory rf source which supplies a sine wave rather than a square wave. Power variations of over 4 dB on the clock caused no noticeable effect on circuit performance.

The 500-600 mV swings of the ECL logic devices is insufficient to switch the IF port of the mixers which require approximately +7 dBm of power for full switching. A microwave amplifier was added to provide the required voltage swings. In order to maintain the square edges of the PN code it is necessary to amplify the full spectrum of the code to at least the fifth harmonic. This required an amplifier capable of providing gain to at least 3 GHz. The Hewlett Packard MSA-0886 microwave amplifier is a convenient 50Ω gain block and offers 7 dB gain at 5.5 GHz. It has 30 dB of gain at 100 MHz. This provides too much power and over switches the mixers and some attenuation is required between the amps and the mixers.

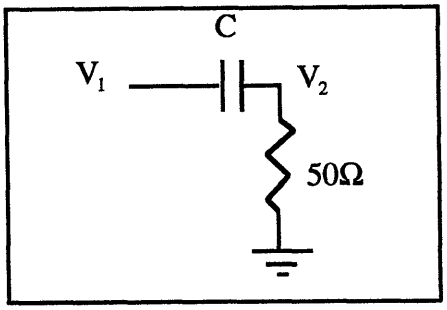


Figure 4-5: Amplifier Coupling

The amplifier requires AC coupling on both its input and output. Capacitors which would effectively pass the code had to be selected. Although the code is running at 600 MHz it has frequency components that are much lower than this. This is because the code has runs of chips which do not change value every time. This is no surprise since changing value every clock cycle would give a simple square wave rather than a PN code. The longest run between a chip changes is nine and occurs in the cycles following the all high state. This means the lowest frequency present is one-ninth that of the clock rate or about 65 MHz. The input and output of the amplifier, with their blocking capacitors, may both be represented by the equivalent circuit shown in Figure 4-5.

The minimum value of C which will pass the lowest frequency must be calculated. We must insure that the voltage at V_2 is at least 90% of the voltage at V_1 at the conclusion of the

longest run without the chips changing values. Since the slowest frequency is 65 MHz, the longest period is about 16 ns. This requirement may be expressed as $V = V_1 e^{-t/50\Omega C} > .9V_1 \mid_{t=16ns}$. Solving for C gives the requirement that C > 3 nF. Any value larger than this will work as well. Chip resistors of .01 μF were selected. Since the lowest frequency component present on the clock lines is 600 MHz, .01 μF was more than sufficient to pass the clock without distortion as well.

The bias for the amplifier is provided through a resistor and rf choke inductor. The output of the amplifier is at a nominal voltage of 7.8V. The specification sheet calls for a supply voltage of 10V and bias current between 20 and 40 mA. This range of bias current yields output power levels between +5 and +15 dBm. A 51Ω bias resistor provides a bias current of about 30 mA with a supply voltage of 9.5 V. A chip inductor of .1 μH, the largest chip inductor with length and width dimensions of .120" x .060" that could be found, was employed as the rf choke.

4.4 PN Code Generator Layout

The primary consideration in laying out the code generator circuit was interconnect length. The secondary consideration was to keep the layout as planer as possible so as to avoid the inclusion of too many jumpers over traces. Not only do such jumpers add complexity to the layout, they also have longer propagation delays than pure microstrip. The flip-flops are in dual-in-line, surface mount packages with "flow-through" pin-outs which place the inputs on one side of the package and the outputs on the other. A single connection to V_{EE} was required on each package. The flip-flops required three connections to V_{CC} while the

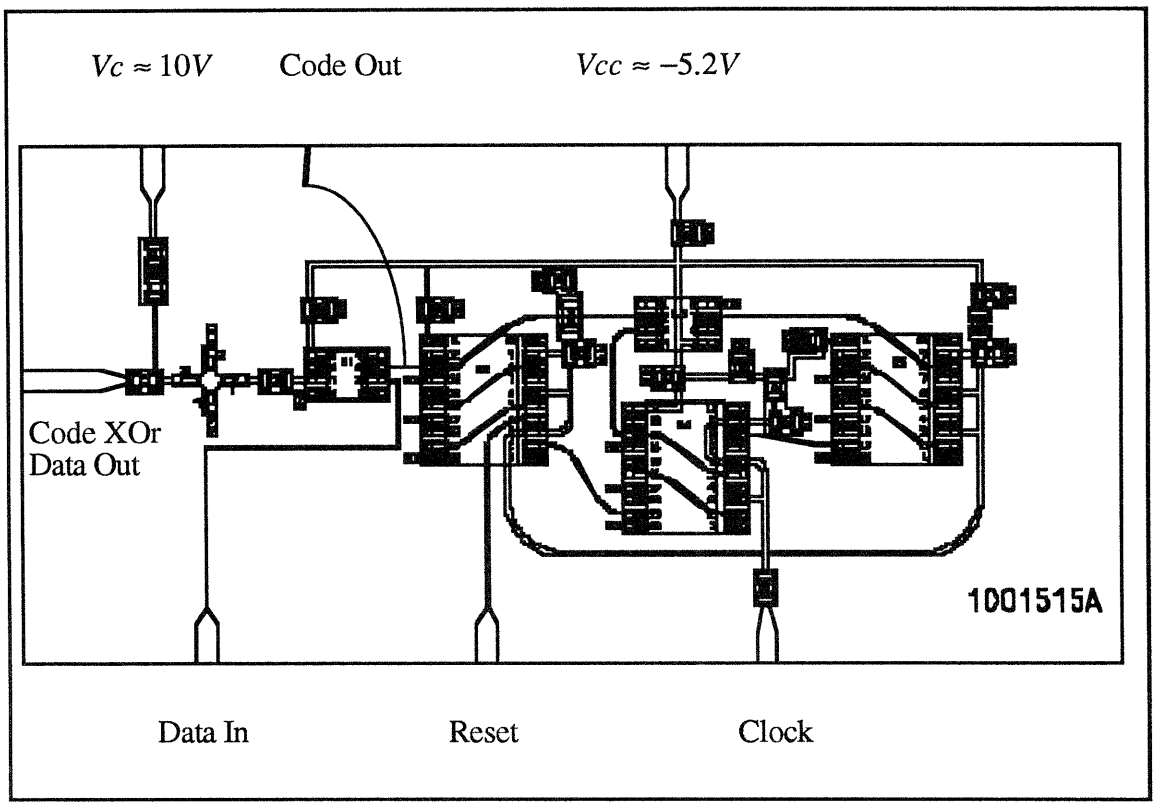


Figure 4-6: Code Generator Layout

XOR gate required a single V_{CC} connection. All V_{CC} connections are achieved with plated vias through the substrate to the ground plane. The layout is shown in Figure 4-6.

In order to minimize coupling between lines, care was taken to ensure that all lines are separated from one another by at least 3 times their own width. Further, clock and data lines were kept free of sharp corners which would have increased radiation. Power lines were allowed to have right angles.

The longest interconnect is the feedback path from stage 9, through the XOR gate, to the input of stage 1. As can be seen, the flip-flops were arranged side to side and slightly staggered. While not the absolutely tightest arrangement possible, it allowed the feedback path to be a total of about 3.8 cm in length with the XOR gate place directly in the middle.

The propagation delay over this length of microstrip is about 182 ps. The XOR gate has a worst case propagation delay of 395 ps.

This gives a total delay of about 577 ps. The flip-flops have a worst case set-up time of 150 ps and clock to valid output time of 710 ps. The total time involved in the longest delay path then is 577 ps + 150 ps + 710 ps = 1437 ps. This represents the shortest period that can be guaranteed to function in the system and translates to a maximum frequency of 695 MHz. This frequency will give a range resolution of 22 cm. The clock lines all have lengths that are close enough to one another that clock skew was not a limiting factor.

Dynamic input/output (I/O) on the board is accomplished through the use of SMA launches which were soldered to the wide portions of the traces at board's edge. These areas are .080" wide which provides adequate room to attach the launches. The impedance of these sections is 50Ω. This matches the impedance of the various lab equipment used. The traces taper smoothly from these areas down to the previously mentioned widths. The smooth taper helps reduce reflections over those which would be present with a direct connection between the wide areas and the narrower lines. DC power is supplied through a simple clip post soldered to the wide edge are of the power trace.

The finished board was screwed down to a metal back plate using machine screws for mechanical strength. The substrate material is quite flexible and was handled a lot in the course of the project so added physical durability was a must. The back plate provided a firm mounting point for the ground portion of the SMA connectors. System ground is connected through one of these SMA grounds.

Included in the layout, but not shown in the schematic, is a contact to one of the asynchronous set pins on one of the flip-flop packages. This is provided as a way to "jump start" the code generator in the event it powers up in, or otherwise enters, the all zero state. According to the specification sheet, asserting a logic high level on this pin is supposed to load a logic high into all three flip-flops. Unfortunately, rather than setting the three flip-flops, the pin acted to reset them. Consequently, starting the code generator usually involved asserting a logic high on one of the interconnects between the packages with a voltage probe set to -0.6V. This method worked fine as ECL devices are capable of using "wired-or" connections without damage. A finished product would employ some type of automatic startup feature. Such a feature was included in the next board and is discussed in chapter 8.

The layout is non-planer in only two places. In one case a required resistor is jumped over a data line to provide termination to a clock line. The second case is to correct an oversight in the layout which resulted in there not being a microstrip connection to the original, unmodified code which is required in the correlation process. This microstrip could have been run from the output of stage nine in the code generator to the bottom edge of the board without jumpers. However, by the time the mistake had been discovered, it was necessary to add a thin wire to the board to carry the code to the edge of board. It was easier to run this wire to the top edge of the board over the power line. It is insulated from the power line with a small piece of Teflon tape not shown in the figure. This worked surprisingly well and did not seem to degrade performance so long as the line was ultimately terminated by being connected to the delay board.

4.5 Code Generator Functionality Tests

The layout does not include any of the required termination resistors. One-eighth watt, wire leaded resistors were added after the other components were in place. This allowed for a little experimentation with the two forms of parallel termination. Single resistor termination to V_{TT} was experimented with first. A 130Ω resistor was added between each drive line and a second power supply set to -2V. The board was run at 100 MHz and the code output was viewed on a digital storage cathode ray oscilloscope (CRO). Once enough sections of the expected code were identified, the clock frequency was increased. Above 150 MHz the scope was unable to display the code. Above this frequency the output spectrum was viewed on a spectrum analyzer. In this configuration, the board provided an expected output spectrum up to 700 MHz.

These single resistors were then removed and replaced with the Thevenin termination discussed in the previous section. Once again, the code was viewed on the digital CRO and several runs of the code were positively identified before increasing the clock frequency. The board now provided the expected output spectrum up to 650 MHz. Inasmuch as a frequency of 600 MHz was decided upon for initial testing, this performance level was sufficient to proceed. A typical output spectrum is shown in Figure 4-7. This spectrum is of the PN code running at 600 MHz. The first null at 600 MHz is clearly visible. The spike within this null is a residue of the clock waveform. Similar spectra were observed with clock frequencies ranging from 60 MHz to 650 MHz with the first null always occurring at the clock frequency.

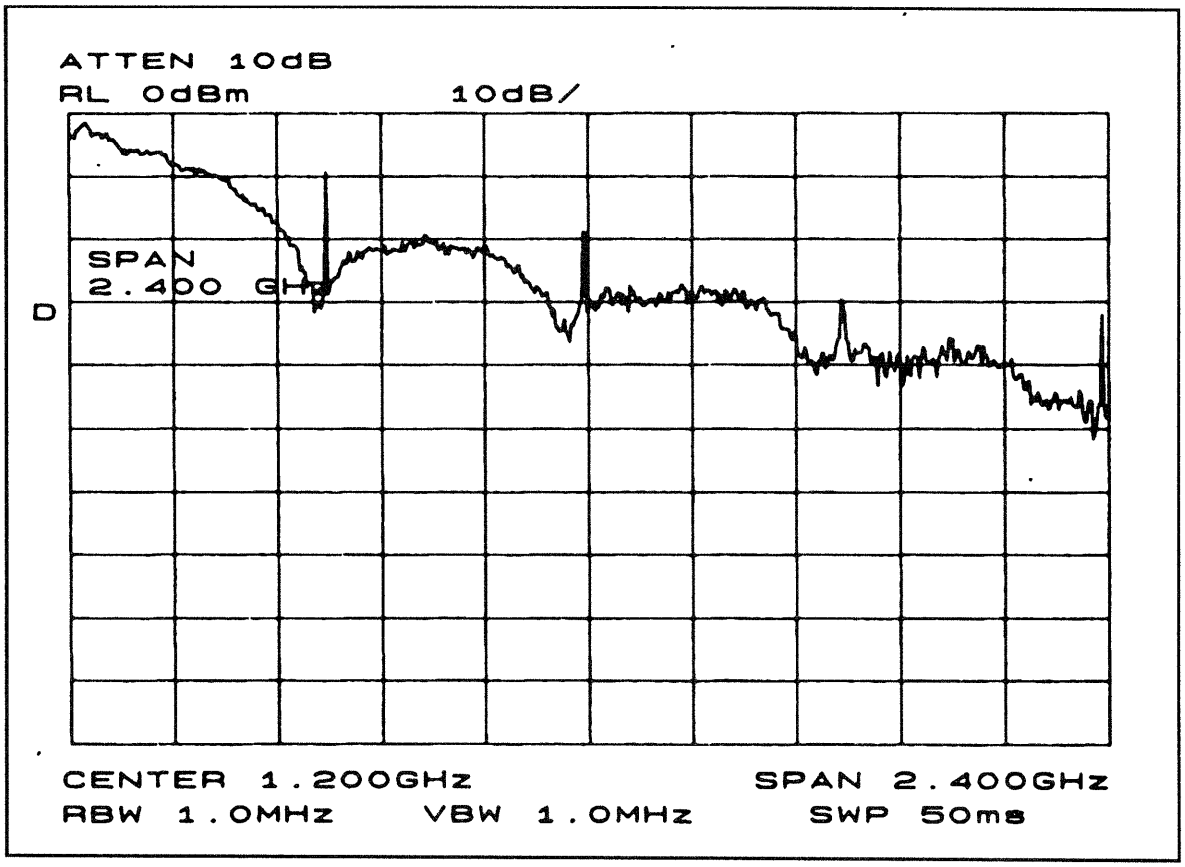


Figure 4-7: PN Code Spectrum

Having verified the proper operation of the code generator, initial tests were conducted on interfacing it with the transceiver. Those tests are outlined in chapter 6. Work was also commenced on the design and construction of the variable delay unit.

5. Delay Unit

The purpose of the variable delay unit is to delay the PN code by a specific number of chips. Each chip of delay represents one range bin or gate in the system. Each bin is one-half of the chip wavelength long and is the finest range resolution the system can measure. It is the delayed version of the code that is correlated with the received signal.

5.1 Delay Unit Circuit Design

There are only two real constraints on the design of the delay unit. First, it must be able to operate at sufficiently high code rates to support the system code generator. Second, it must be able to delay the code an integer number of chips without altering the code sequence itself. Added functionality of changing the position of the system range bin is accomplished if the delay integer may be readily changed. This accommodates target detection at numerous ranges and facilitates more extensive concept testing than possible with a single fixed range gate.

The most straightforward way to introduce an integer delay into a digital bit stream is to clock it through a series of registers. This will delay the bit steam an integer number of bits while not altering the bit stream itself. This certainly satisfies the second requirement. Since the PN code is originally generated using a series of registers, there is no difficulty in finding registers which will operate at the same clock frequencies as that at which the code is running. Identical part numbers could be used. However, Motorola MC100E151 6 Bit D Register, also in the ECL logic family were used instead.

These parts are in a 28 pin, square surface mount package rather than a dual-in-line as the triple D flip-flops used for the code generator. These parts offer faster propagation delays and require shorter setup times than the triple D flip-flops. Another consideration was the fact that there are twice as many registers in each package. With the code running at 600 MHz each range bin is 25 cm long as previously discussed. This means that a total of 8 range bins are required to obtain a maximum range of 2 m. These parts allow that to be achieved with 2 pieces rather than three. As the code rate is increased, and the length of the range bins decreases, even more delays will be required in order to maintain a maximum range of 2 m. At 1 GHz code, and 15 cm range resolution, 14 range gates are required.

Unfortunately, these parts are also 10% more expensive on a per flip-flop basis than the dual in line packages. Cost is not an issue for this test unit, however it will be a factor in determining the ultimate marketability of any system based on this concept.

The block diagram of the delay unit is shown in Figure 5-1. The flip-flops are arranged in shift register fashion just as they were for the code generator only this time there is no feed back path. Selectability of the integer unit of delay is provided by one side of a Motorola MC100E163 2 bit 8:1 multiplexer. The other side is unused. A microwave amplifier is included again to provide the necessary power to drive the IF port of the mixer used as a correlator. The smallest delay that can be selected is actually a 2 chip delay. This was done to compensate for the internal delays in the transceiver loop.

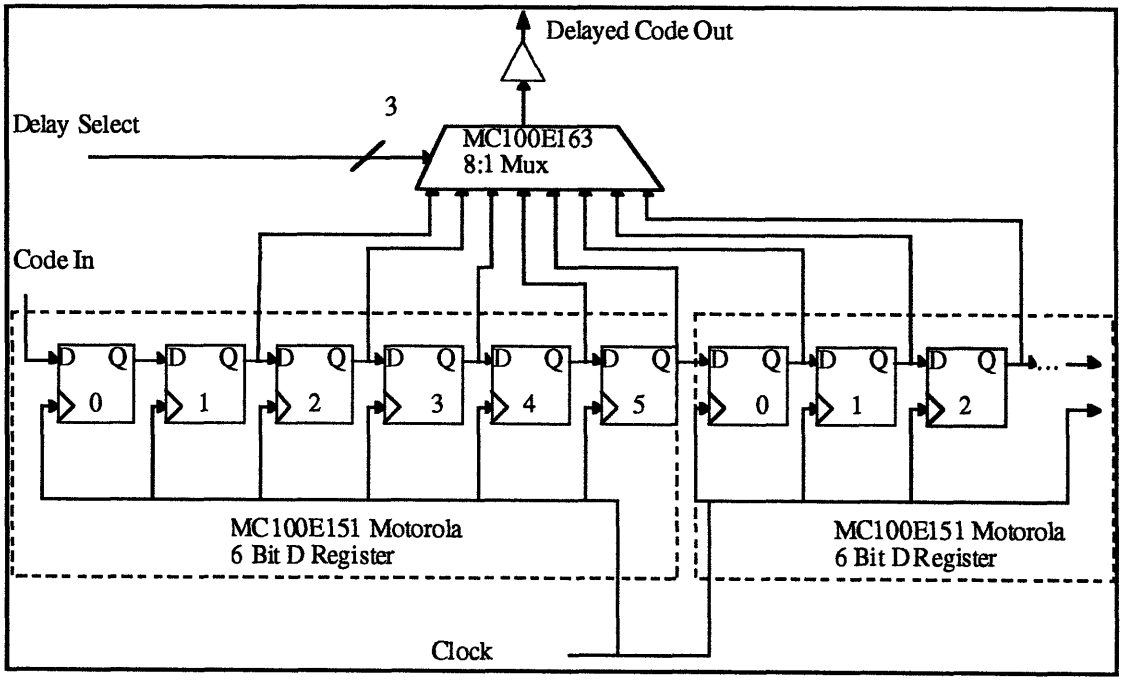


Figure 5-1: Delay Unit Block Diagram

The same microwave substrate was used for the delay unit as was used for the code generator. Upon verification that the code generator and delay unit both functioned

independently, a third board which integrated the two units together was planned. Microstrip lines of the same width as those used on code generator were used--namely .007" for data interconnects and .020" for clock and power lines. Thevenin termination was used again and all values are the same as they were on the code generator . As in the code generator, only the outputs used were terminated. Their compliments were left open. DC bypassing and AC coupling is as on the code generator as well.

The devices used all have internal pull down resistors of approximately 60 KΩ on the inputs which are capable of guaranteeing that any open inputs are pulled to a logic low state. This is exploited in the switching of the multiplexer. A surface mount, dual-in-line, four channel, single throw switch is used to assert the control lines. One side of the each switch is tied to the control lines. The other side is tied to a logic high voltage of -0.6V which is established by a resistive voltage divider. This divider uses a 510Ω and a 3.9 KΩ resistor. A control line is asserted by closing the proper switch and connecting the line to the voltage divider. Even with all three lines asserted at once, the 60KΩ internal resistors will not significantly alter the voltage divider. A line is de-asserted by opening the appropriate switch and allowing the line to float. Its own internal resistor pulls it to a logic low level.

Power consumption does have to be checked as different parts are being used. Each 6 bit register uses 90 mA. The mux also use 90 mA. This is a total of 270 mA through the integrated circuits. There are 19 resistor networks on the data lines, each equivalent to 580Ω, in parallel. There are also two networks on the clock lines, each equal to 530Ω. This is all in parallel with the logic high voltage divider which has an equivalent resistance of 4400Ω. So the equivalent resistance across the rails is:

$$\frac{1}{19\left(\frac{1}{580\Omega}\right)+2\left(\frac{1}{530\Omega}\right)+\frac{1}{4400\Omega}} = 27\Omega$$ and the total current draw of the resistors is 191 mA. The total current draw of the board, therefore, is 461 mA and .020" wide power traces still provide adequate capacity.

5.2 Delay Unit Layout

The delay unit layout is shown in Figure 5-2. As with the code generator, AC lines are kept at least 3 line widths away from all other lines and have no sharp corners.

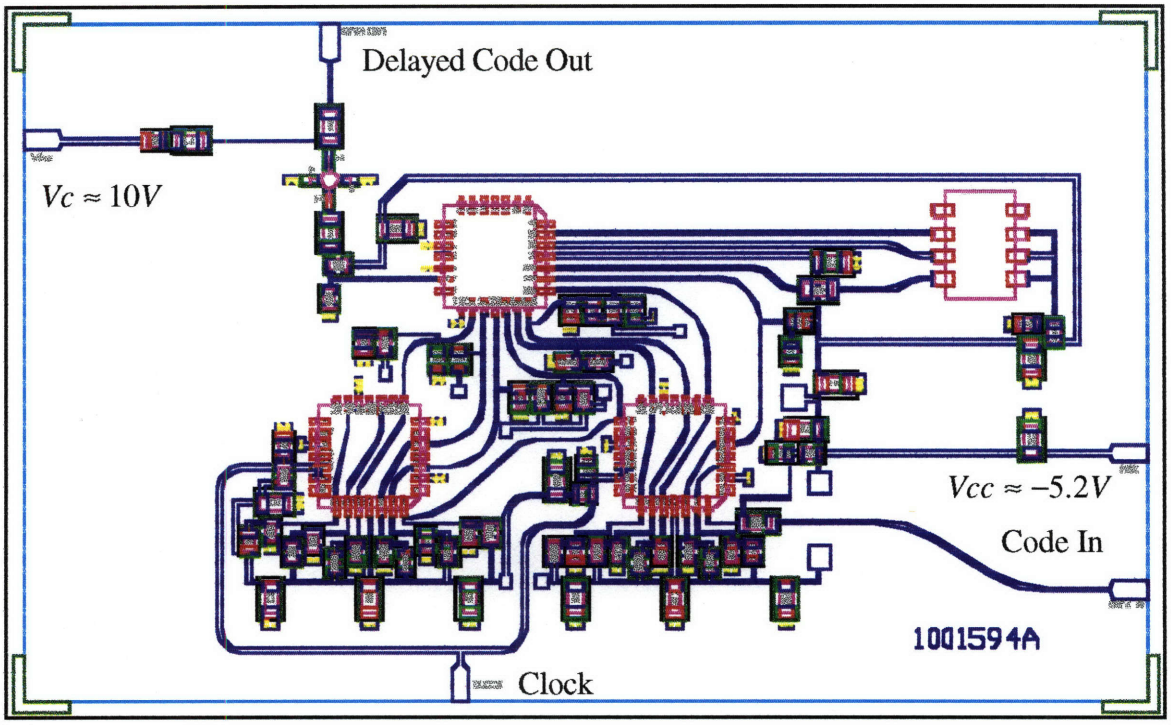


Figure 5-2: Delay Unit Layout

The longest interconnect on this board is approximately 4.4 cm long creating a delay of 214 ps. These registers have a worst case propagation delay of 800 ps, but a worst case

setup time of 0 ps. The total delay is, therefore, 1014 ps and guaranteed maximum frequency of 985 MHz can be achieved.

Having determined the desired termination scheme on the code generator layout, Thevenin termination resistors were included on the delay board. Surface mount chip resistors measuring .080"x.050" are used throughout. The capacitors and inductor are all .120"x060" surface mount parts.

The inclusion of the termination resistors on the board complicated the layout somewhat as compared to the code generator. Each termination network requires connections to both V_{EE} and V_{CC}. Connection to V_{CC} is easily accomplished with a plated through via to the ground plane on the back side of the board. The easiest way of running power to these networks is with short jumper wires connected to solder pads. This allows multiple lines to be crossed with a single wire rather than introducing multiple 0Ω jumper chips to make the same connection. Multiple jumper chips would have also required more room between individual traces being crossed to accommodate the mounting points.

In order to minimize the number of jumper wires needed, two termination networks are located next to each other between every second data line. This allows a single jumper to provide the required connection to V_{EE} to two sets of termination networks. In addition to the data lines between the registers and the multiplexer, there are two other places where jumper wires are required. The clock has to be crossed in one place and the incoming code has to crossed. A single 0Ω jumper is used to jump a multiplexer control line over the power line.

In planning this board, a coupling capacitor was allowed for on the incoming code line. This was done in case DC levels from one board to the next proved to vary too much, or if other difficulties necessitated ac coupling. After the difficulties encountered with the XOR gate on the code generator such difficulties seemed possible if not likely. However, AC coupling proved unnecessary so the break in the incoming code line was bridged with a 0Ω jumper.

Dynamic I/O and power connections onto the board were handled just as for the code generator. Coupling of the clock input and microwave amplifier, as well as bias current for the amplifier and bypassing of the power line near components and termination networks, were all handled as before. Once again, the finished board was mounted to a metal backplate using machine screws run down through the top of the board.

5.3 Delay Unit Functionality Tests

To verify proper operation of the variable delay unit it is initially tested with square waves. A square wave is fed into the code input lone through a 360Ω resistor. The resistor was added to provide the required stability of the voltage levels as is done on the data input of the XOR gate on the code generator board. This signal is viewed on channel 1 of a CRO and used to trigger the CRO sweep. The delayed output is viewed on channel 2 of the CRO.

The signal fed into the code input is run at various frequencies between 1 and 20 MHz. The board is clocked at frequencies ranging from 75 MHz to 1.52 GHz. The output waveform is then compared to the input signal at each of the eight possible settings on the multiplexer. Each setting represents a different amount of delay. We would expect to see

the output waveform trail the input signal by an amount equal to $(1 + delay_{selected}) * Period_{clock}$, where delay may range from one to eight.

With the clock set below about 100 MHz, it is possible to see the output code slip behind the input code by the expected amount at each setting of the mux. As the clock frequency is increased, the delay becomes too small to see effectively on the CRO. However, the output wave is still completely visible. Correct operation is assumed so long as the output wave clearly duplicates the input wave even when the expected delay becomes too small to see on the CRO. This is the case up to a clock frequency of 1.52 GHz, beyond which the output wave deteriorates. The fact that the circuit functions beyond the calculated maximum indicates the parts used are functioning with propagation delays and set up times not only better than the worst case values, but better even than the specified typical values. Specified typical propagation delays and set up times are 650 ps and -175 ps, respectively. These delays combined with the longest trace delay would indicate a maximum frequency of 1.45 GHz.

Interestingly, at code input rates of less than 10 MHz, the microwave amplifier inverts the output delayed code. Probing the various traces on the board verified that the amplifier is in fact inverting the signal rather than some other problem being present. Such inversion poses no problem to the system since phase shift is not considered and correlation between the returned and delayed codes will not be affected.

As a second verification of proper operation, the code input is next connected to the unmodified code output of the code generator board as it will be in actual operation. The resistor used previously is removed. The boards are clocked synchronously at 150 MHz. The data input on the code generator is left unconnected so it was set low by its bias

network. Thus the code leaving the code⊕data output of the generator board is simply code⊕0 which is equal to just code. The outputs of both boards are viewed on a digital storage CRO. The delayed code is found to be delayed by an integer number of chips with the integer ranging from two to nine as set on the mux control switches. At frequencies much above 150 MHz, the CRO cannot adequately display the waveforms. The spectra of both the delayed and nondelayed codes are viewed on a spectrum analyzer. Both spectra have the expected shape as shown in Figure 4-7 and are virtually identical to one another up to the maximum generating frequency of about 650 MHz.

Further testing of the delay unit involved interfacing with the transceiver and is detailed in chapter 6.

6. Transceiver

The transceiver is composed of a continuous wave (CW) microwave oscillator and two catalog, double-balanced mixers. A laboratory microwave source is used for the oscillator. A third catalog mixer acts as the system correlator. Two different sets of mixer/correlator mixers are experimented with. One set of mixers, Anaren #74129, is designed for operation around 16 GHz. The mixers in the other set, Miteq #M1826, are designed for use at 24 GHz. Two sets of standard gain horns are used for the transmit and receive antennas. One set of horns is specified for use at 24 GHz. The other set is designed for use around the 12 GHz band but is used at 16 GHz for some testing in this project. This constitutes two different transceivers operating at two different carrier frequencies.

Two transceivers were built and tested for several reasons. The system was originally envisioned to operate at a carrier frequency of 24 GHz. A high frequency carrier is

desirable for reason discussed in the following sections. However, a longer lead time was required to obtain the 24 GHz mixers than was required to obtain the 16 GHz mixers. Using the lower frequency mixers first and then moving on to the higher frequencies allowed testing to begin sooner and experience to be gained interfacing the digital components with microwave mixers. The lower frequency mixers also offered much better port-to-port isolation. The 16 GHz mixers provide a minimum of 28 dB of isolation between the LO port (the carrier port) and the RF port (the transmit port) while the 24 GHz mixers provide only 18 dB between these ports. Since it was not known how carrier leakage would affect system performance there was some question as to whether the 24 GHz mixers' isolation was adequate.

Both the range resolution and the maximum range that the system can measure are independent of carrier frequency. However, carrier frequency is still an important system consideration as it affects target dropout as discussed below. Given a PN code rate, it also determines the bandwidth the antennas must support as well as the physical size of the antennas. It is also a major factor in component costs. Further, carrier frequency is restricted by FCC band allocations. A specific band has not been determined for ultimate operation however both Ka (24 GHz) and X (10 GHz) band are being considered. A problem arises in that neither of these bands have any channel allocations that came close to being the required one GHz wide.

One of the wider channels available in the Ka band is 250 MHz wide from 24 to 24.250 GHz [5]. Within this channel the average electric field intensity may be 250,000 μV/m when measured at a distance of 3 meters from the radiating device. Any emissions outside of allocated bands must typically be below 500 μV/m when measured at 3 meters. There is some unwritten industrial precedence for allowing spread-spectrum devices to deliberately

radiate outside allocated bands so long as their average field intensity is below this FCC floor. FCC approval will be pursued as one of the early phases of the development program following this research.

For convenience, these field intensity levels may be converted to transmitted power (in watts) by using a form of the Friis Transmission Formula.

$$p = \frac{P_t G_t}{4\pi r^2} = \frac{E^2}{\eta} \tag{6.1}$$

Where:

p	=	power density (W/m^2)
P_t	=	Transmitted Power (W)
G_t	=	Gain of transmit antenna
r	=	Radius from antenna
E	=	Electric Field Intensity
η	=	Impedance of free space ($\approx 120\pi\Omega$).

If one assumes a horn with a gain of 10, solving for P_t gives about 1.9 mW of allowed transmitted power. The greatest power that may be transmitted outside allocated bandwidths is 7.5 μW. These figures are finally converted to dBm (decibels per milliwatt) for convenience and yield 2.7 dBm and -51.2 dBm for the allowable in and out of band transmitted power, respectively.

6.1 BPSK Modulation/Demodulation

The system under examination employs direct sequence, Bi-phase Shift Key (BPSK) modulation. BPSK modulation is carried out by phase shifting, by 180°, the carrier each

time the PN code transitions states. This phase shift is implemented by switching the IF port of a mixer with the PN code while the LO port is driven with the carrier. It is direct sequence because the PN code is used directly to carry out this switching. The baseband spectrum of the PN code has already been examined in section 4.5, Code Generator Functionality Tests. The spectrum of the CW carrier is simply an impulse. It is instructive to also examine the time domain waveforms in a BPSK modulated system. Representations of these waveforms are shown in Figure 6-1 [3].

The CW carrier, ω_c, is shown in the upper left corner of the figure. Directly below the carrier is a short segment of the PN code, Pn(t). At each transition of the PN code, the carrier is phase shifted by 180° and the resultant wideband signal is shown in the lower left corner. This signal (neglecting amplitudes) is either $\cos(\omega_c t)$ or $\cos(\omega_c t+\pi) = -\cos(\omega_c t)$ depending on which portion is examined. If the bits of the PN code are +1 for a logic level one and -1 for a logic level zero, then the transmitted signal may be written as simply $Pn(t)\cos(\omega_c t)$. In other words, it is simply the carrier multiplied by the PN code bit stream. This is exactly what we would expect at the output of a mixer. This wideband signal is transmitted, reflects off an obstacle, and is received by the system.

The received signal is reproduced in the upper right corner of the figure. A short segment of PN code, delayed by an appropriate amount to account for the flight time of the transmitted and recovered waveform, is shown directly below. Once again, the waveform's phase is shifted by 180° at each transition of the PN code yielding either $Pn(t-\tau)\cos(\omega_c(t-\tau))$ or $Pn(t-\tau)\cos(\omega_c(t-\tau)+\pi)$ where τ is the flight time delay. This is equal to $Pn^2(t-\tau)\cos(\omega_c(t-\tau))$, which, since $Pn(t) = \pm 1$, is equal to $\cos(\omega_c(t-\tau))$.

This phase shift constitutes correlating the delayed code with the received signal and is carried out by switching the IF port of the correlating mixer with the PN code while the wideband waveform is received through the RF port. This collapses the spread-spectrum signal back to a narrowband signal. The original carrier is recovered and is shown in the lower right corner of Figure 6-1.

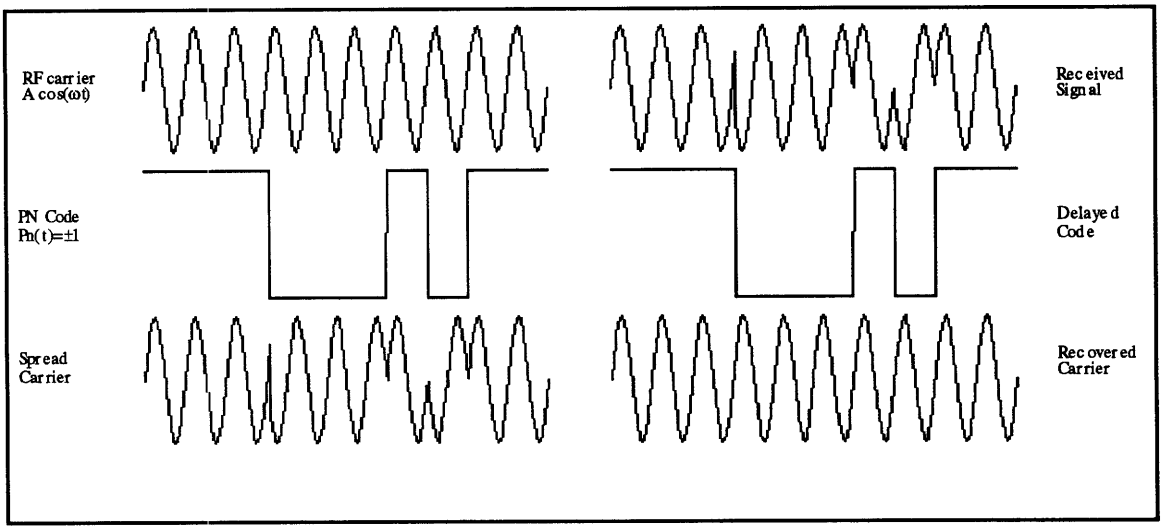


Figure 6-1: System Time Domain Waveforms

Clearly, unless the state transitions in the delayed code line up with phase shifts of the received signal the original carrier will not be recovered exactly. If the transitions of the delayed PN code are one full chip or more out of proper alignment with the phase shifts of the received signal the autocorrelation goes to a minimum value and no carrier is recovered. As discussed in chapter 4, the autocorrelation of a maximal PN code varies linearly from its maximum value to its minimum value in the region of 0±1 chip shift. Thus, if the misalignment between the delayed PN code and the received signal is less than one full chip, some fraction of the carrier's energy will be mapped into the desired narrowband while the rest of the carrier's energy will be spread. The distance to an obstacle is easily

determined then, to a resolution of one chip length by observing how much delay in the PN code is required to recover the narrowband carrier.

6.2 BPSK Ranging

This concept is illustrated in Figure 6-2 which shows three adjacent autocorrelation functions. The ticks along the ordinance represent the integer chip delays of the PN code as selectable from the delay unit. The peak of each autocorrelation function occurs when the range to the obstacle is such that one of these integer chip delays causes perfect correlation with the returning code. The autocorrelation value decreases linearly from this peak to its minimum value as the range to the obstacle moves away from this point. The minimum value of one autocorrelation function, or range gate, occurs at the peak of the adjacent autocorrelation function or range gate.

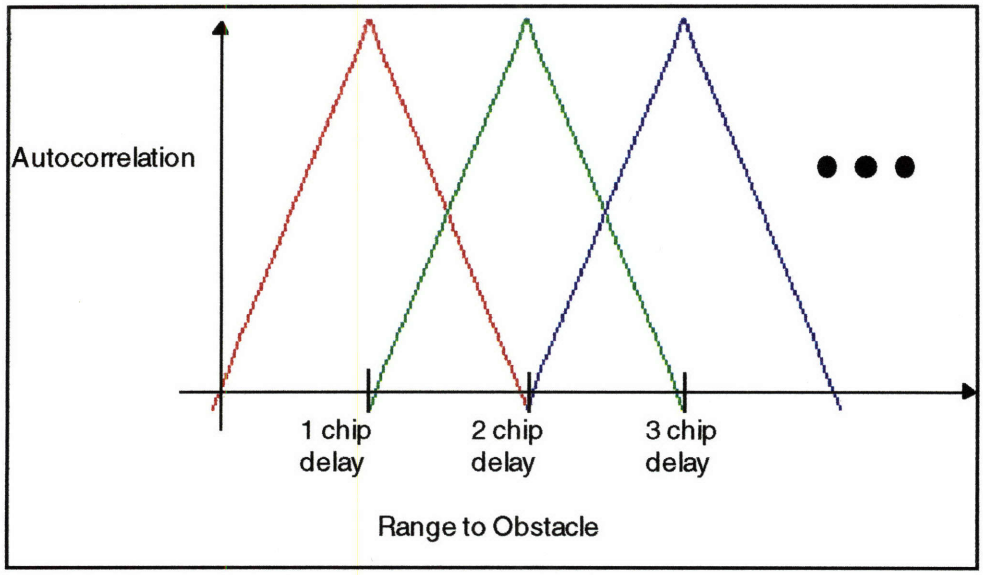


Figure 6-2: Range Gates

The resolution possible in such a system is clearly dependent on the physical length of the transmitted code chips. This is simply c/f_{code}. In other words, this means that phase changes in the transmitted spectrum occur c/f_{code} meters apart. However, since the code chips must travel round trip, they cover exactly twice the distance as that to the target. The transmitted code must be returned to be correlated after traveling only half of a chip length if it is to align with a one chip internal delay since the total round trip distance is then equal to one full chip. So every chip of internal delay translates to a half chip length of range. Thus the actual resolution possible is $\frac{c}{2f_{code}}$.

For clarity, the time domain waveforms in Figure 6-1 do not illustrate the encoding of the 10 KHz data signal onto the PN code. As discussed in chapter 4, the data signal is XORed with the PN code prior to the PN code switching the transmit mixer. This results in an inversion in the PN code bit stream each time the data signal changes state. An unmodified version of the PN code is then correlated with the received signal. In the simple case of perfect alignment between the received signal and the delayed code, the recovered carrier will be left with a 180° phase shift occurring at the data signal rate of 10 KHz. Thus we see the data is recovered as phase information on the carrier. The received and correlated signal may be represented as $\cos[\omega_c(t-\tau)+\phi[t-\tau]]$ where:

ω_c = CW carrier frequency,

$\phi[t]$ = $\begin{cases} 0, & 0<t<\frac{nP_d}{2} \\ \pi, & \frac{nP_d}{2}<t<nP_d \end{cases}$ n is any integer, P_d is the period of the data signal,

τ = round trip time delay.

When the delayed code and received signal do not align perfectly, but are less than one full chip out of alignment, some portion of the wideband signal's energy will be remapped into

the expected narrow bandwidth and the carrier, with its phase encoded data signal, will be recoverable although with a reduced amplitude. All of foregoing applies to a single range gate. In an actual system the sensors would be swept through all the range gates and every gate would be checked for a target.

6.3 Baseband Recovery and Target Dropout

After correlating the received signal with the delayed version of the PN code the data signal is available as phase inversions on the recovered carrier. This signal is down converted to baseband by multiplying it with the same carrier used on the transmit side of the transceiver using a mixer identical to those used for modulation and correlation. This constitutes a coherent, heterodyne receiver. While other forms of down-conversion offer some theoretical advantages, issues of power and the desire to avoid wideband, high-frequency amplifiers precludes their use. The resultant signal after multiplying these two signals is:

$$\cos(\omega_c t)\cos[\omega_c(t-\tau)+\phi(t-\tau)]$$

$$=\frac{1}{2}\left\{\cos\left[-\omega_c\tau+\phi[t-\tau]\right]+\cos\left[2\omega_c t-\omega_c\tau+\phi[t-\tau]\right]\right\}.$$

Neglecting the second order term which is easily filtered,

$$=\frac{1}{2}\left\{\cos(-\omega_c\tau)\cos(\phi[t-\tau)+\sin(-\omega_c\tau)\sin(\phi[t-\tau])\right\}.$$

However, since $\phi[t]$ equals either 0 or π, the second term in the above sum is always 0

and, neglecting the constant,

$$=\cos(-\omega_c\tau)\cos(\phi[t-\tau]). \qquad (6\text{-}8)$$

The second term in the product of equation 6-8 is the baseband data square wave. The first term contains no time varying elements and is a constant multiplier which, given a constant

CW carrier, varies between -1 and 1 depending on the time delay τ. This time delay is determined by the range to the target by the relation

$$\tau = \frac{2R}{c}. \tag{6-9}$$

The argument of the first term may be expressed as $2\pi f_c \tau$. In this form it is readily apparent that when τ is equal to $\frac{2n+1}{4f_c}$ the argument is equal to $\pi/2$ and, since cosine of $\pi/2$ equals zero, the amplitude of the mixer output is zero. At this point the receiver is said to be in quadrature and target dropout occurs. Substituting this value of τ into equation 6-9 reveals that the amplitude of the data signal will be zero whenever $R = \left(\frac{2n+1}{8}\right)\frac{c}{f_c} = \left(\frac{2n+1}{8}\right)\lambda_c$. Similar calculations show the data signal will be at a maximum amplitude when $R = \frac{n}{4}\lambda_c$.

Thus, as the range to an obstacle changes by a distance equal to 1/4 of the carrier wavelength, the amplitude of the recovered baseband data signal will vary from its maximum amplitude to zero amplitude and finally to an inverted maximum. The actual behavior of the system's range gates then is represented by a cosine multiplied by each triangular autocorrelation function of Figure 6-2. This situation is shown in Figure 6-3.

Virtually all radar systems employ some method of overcoming this inherent weakness of coherent heterodyne receivers. Super-heterodyne receivers which make use of an intermediate frequency and down convert in two stages are one common method. Two channel Quadrature receivers in which one channel is at a maximum amplitude whenever

the other channel is at zero are another. Clearly, both of these solutions come at increased system cost. The radar engineers for whom this system was designed and built desire to determine whether such costs can be avoided.

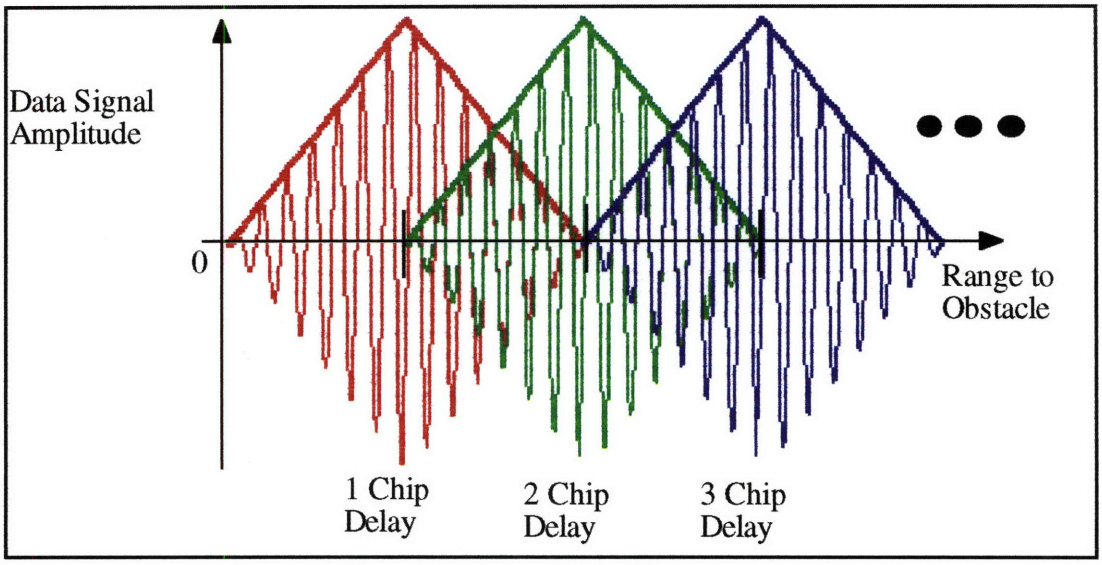


Figure 6-3: Range Gates with Quadrature

Certainly, given a coherent heterodyne receiver, there is no theoretical way around the signal dropouts. However, radar engineers theorize that if the distance between two peaks is small enough real world obstacles might not dropout. The reasoning is that if real world targets exhibit a radar depth greater than 1/8 λ_c then even if some of their returned signal is at a dropout point, some of the signal will always be at a peak. The smaller λ_c is the more likely that targets will have a radar depth which is greater than 1/8 λ_c. This is one of the motivations for using a high frequency carrier. A 24 GHz carrier has a wavelength of just 12 mm. This means that any target with a radar depth of greater than 1.6 mm will return energy with time delays, τ, which will span the entire region from zero to peak output of the receiver. On the other hand, with a carrier frequency of 16 GHz, targets will have to

have a radar depth of 2.3 mm to give the same result. Detailed testing of this theory is the job of radar engineers and is ongoing. Initial testing is detailed below.

6.4 Transceiver Functionality Tests

In order to verify the functionality of the PN code generator/Transceiver interface, the test setup shown in Figure 6-4 is constructed using the 16 GHz mixers. The output of the transmit mixer is fed to the input of the correlator mixer via a length of microwave delay line. Variable attenuators are placed on the LO port of the transmit mixer and the RF port of the correlator mixer to assist in ruling out any possibility of direct leakage from the transmit side of the system to the receiver. The 6 dB attenuator on the output of the code generator is required to prevent the microwave amplifier from over driving the mixer. The data signal is set to 100 KHz. A carrier frequency of 14.786 GHz is decided upon empirically as it produced the peak output with the delay line used. (Given a fixed τ, varying the carrier frequency will produce the same peaks and nulls from the receiver as was seen in section 6.3.) The carrier power is held constant.

The amplitude of the received data signal is recorded as attenuators A and B are varied between 0 and 20 dB. The power spectrum of the transmitted waveform is viewed on a spectrum analyzer in real time by using a -10 dB coupler on the transmit line. A representative spectrum is shown in Figure 6-5. The power level of the highest point on the spectrum, denoted by the arrow, which occurs at the carrier frequency is recorded. For simplicity, this quantity is referred to as the "peak power" throughout this report even though that term is normally associated with signals whose power levels vary over time. This value is recorded with two different settings, 2 MHz and 1 MHz, on the spectrum

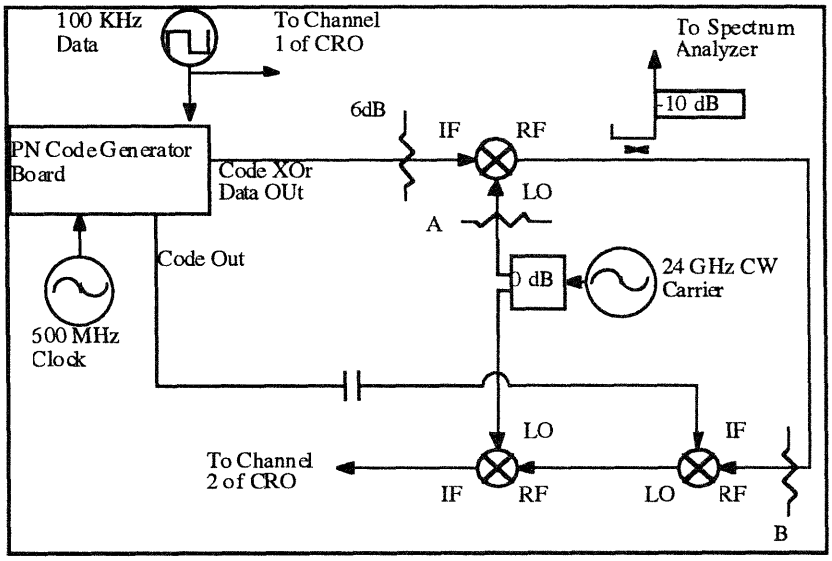


Figure 6-4: Code Generator Test Setup

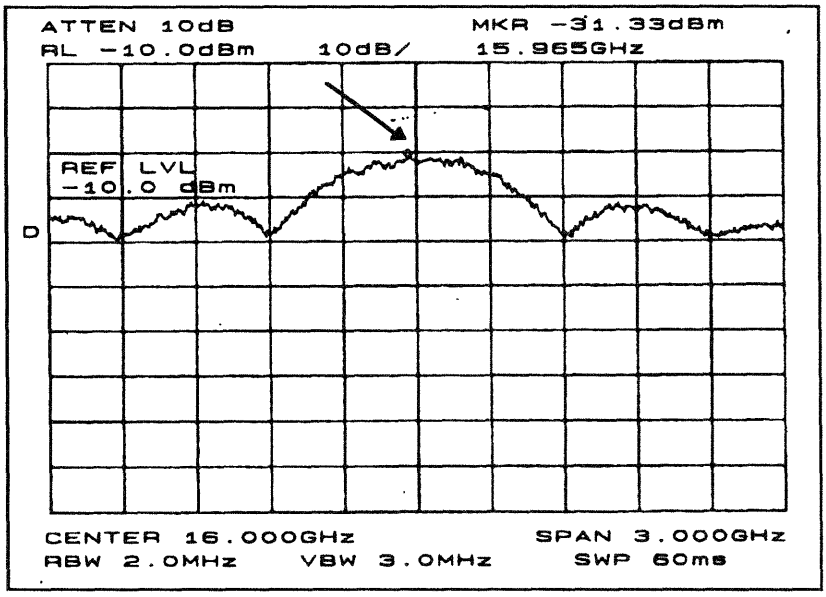


Figure 6-5: 16 GHz Transmit spectrum

analyzer's measurement bandwidth. The mainlobe width is twice the code clock frequency and the spectrum exhibits the expected $[\sin(x)/x]^2$ shape.

The results are shown in Figure 6-6. As can be seen, the transmit power level goes down just as we would expect when the carrier is attenuated prior to driving the transmit mixer. The measured transmit power is also cut roughly in half when the bandwidth of the spectrum analyzer is halved. This is the behavior that would be expected if noise were being measured. That the spread-spectrum transmitted waveform behaves similarly indicates it has certain noise-like properties as we hope a PN waveform would.

The data signal's amplitude also decreases as either the transmit power is decreased or the loss in the delay line is increased. This gives some reassurance that the system is actually correlating and down converting the transmitted signal as desired rather than allowing the baseband to leak directly through.

A(dB)	100 KHz signal output amplitude B(dB) 0	20	Peak Power Transmit BW=2MHz	BW=1MHz
0	110 mV	11 mV	-30 dBm	-32 dBm
10	20 mV	2 mV	-40 dBm	-43 dBm
20	8 mV	1 mV	-50 dBm	-54 dBm

Figure 6-6: Code Generator Interface Test Results

The carrier frequency is next varied to observe the quadrature phenomena of the receiver. As the carrier is varied over a range of roughly 200 MHz the amplitude of the recovered baseband data signal varies from 0 mV to 100 mV and back to 0 mV. A brief summary of these figures is presented in Figure 6-7.

CW f (GHz)	**14.701**	**14.706**	**14.800**	**14.895**	**14.904**
100 KHz signal amplitude	0 mV	20 mV	100 mV	20 mV	0 mV

Figure 6-7: Quadrature Test Results

6.5 Transmit Power Characterizations

Some of the characteristics of the transmitted waveform and the mixers are next determined. The test setup used for these characterizations is shown in Figure 6-8. The

carrier frequency is set to 15 GHz and the carrier power into the LO port is metered at 0 dBm. The PN code power into the IF port is metered at 10.7 dBm.

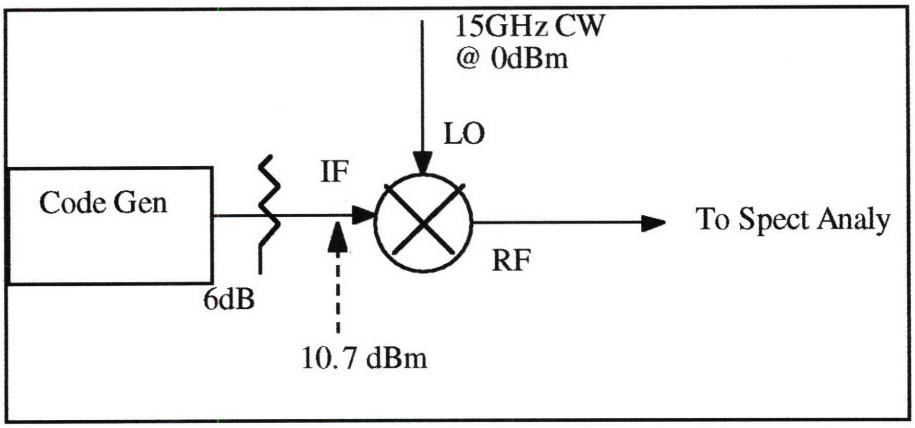


Figure 6-8: 16 GHz Mixer Characterization Test Setup

The code clock rate is varied between 50 and 600 MHz and the peak transmitted power is measured at both 1 and 2 MHz bandwidths on the spectrum analyzer. The results are plotted in Figure 6-9. As the clock rate is increased, the main and side lobes of the transmitted waveform spread wider. The first null occurs at $f_{carrier}+f_{code\ clock}$. Since the total

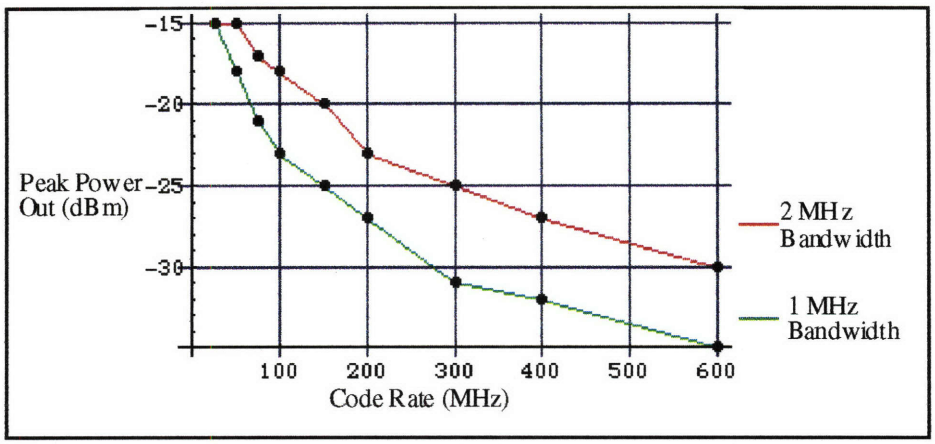


Figure 6-9: Peak Power Out versus Code Clock Rate

transmitted power must remain constant, the peak level decreases as the lobes spread. Figure 6-10 and Figure 6-11 show two such waveforms centered at 24 GHz. Figure 6-10

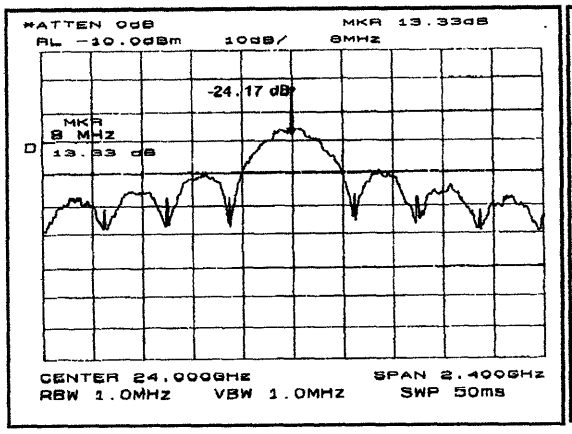


Figure 6-10: Transmit Spectrum, 300 MHz Code Rate

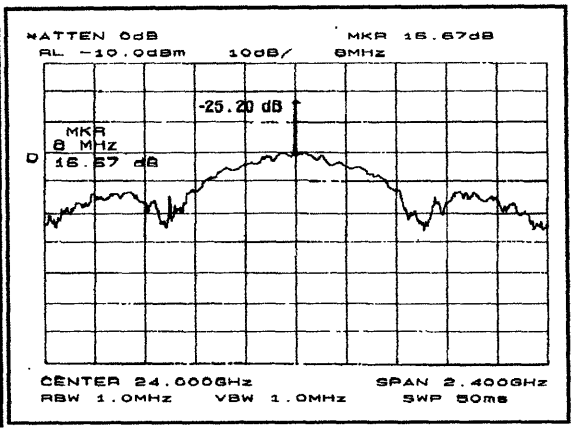


Figure 6-11: Transmit Spectrum, 600 MHz Code Rate

shows the transmit spectrum with a code rate of 300 MHz. Figure 6-11 shows the transmit spectrum with a code rate of 600 MHz.

Next, the code is held at 600 MHz and 10.7 dBm. The carrier power into the LO port is varied between -35 and 0 dBm. Once again, peak power measurements are taken with the

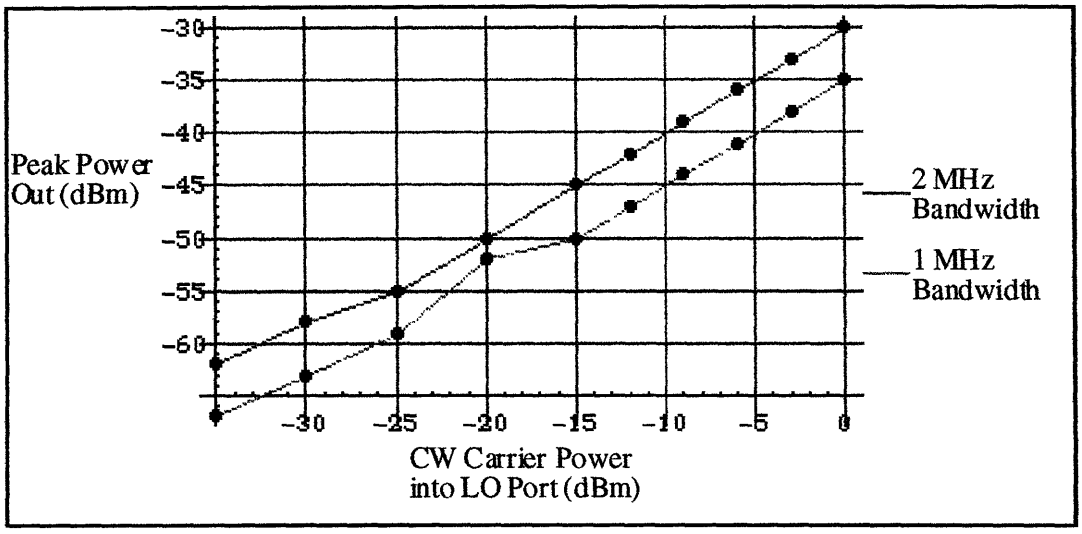


Figure 6-12: Peak Power Out versus Carrier Power In, 16 GHz mixeris

spectrum analyzer set to 1 and 2 MHz bandwidths. The results are plotted in Figure 6-12. Neglecting measurement inaccuracies, the curves are linear as expected.

Next, a 600 MHz square wave is fed into the IF port in place of the PN code. The carrier power is held constant at 15 GHz and 0 dBm. The expected spectrum when mixing a sine wave with a square wave is an impulse at the carrier frequency and impulses at the odd harmonics of the square wave including the fundamental. This is observed. The power of the upper and lower sidebands are equal. The power level of the square wave is varied between -7 and +12 dBm. An RF power meter indicates the total power out of the mixer remains constant at -9.0 dBm. However, the power level in the sidebands varies with the power of the switching square wave. Results are shown in Figure 6-13.

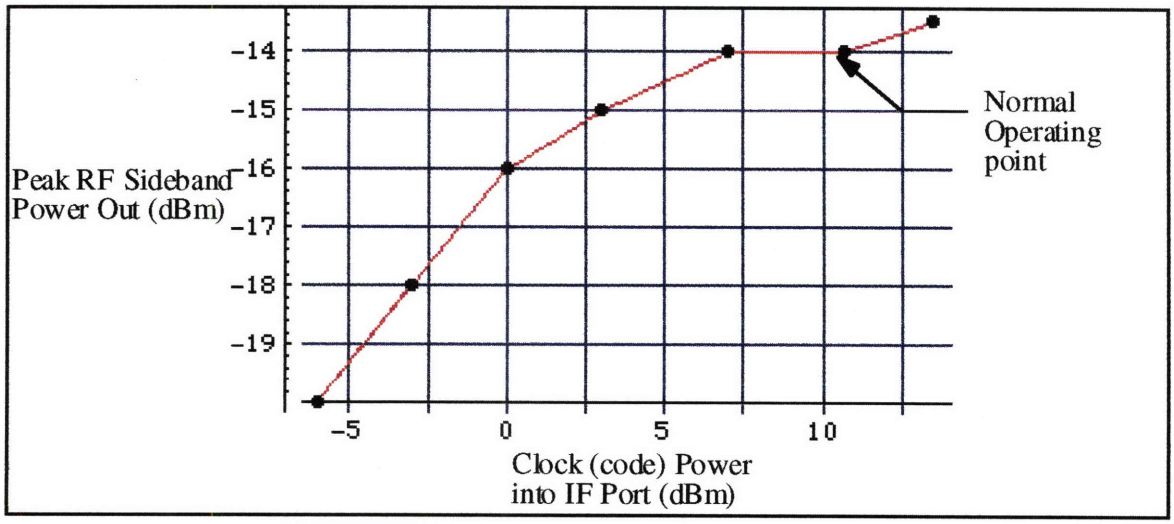


Figure 6-13: Peak Sideband Power Out vs. Code Power In, 16 GHz mixer

As can been seen, between approximately +7 and +11 dBm power into the IF port, the power in the sidebands remained constant. Experimentation shows that a power level of 10.7 dBm provides an output spectrum with the least amount of carrier or clock frequencies visible. In other words, this power level provides the best carrier balance and clock

balance to the mixer. Figure 6-5 shows no visible evidence of either carrier or code imbalance or leakage.

Finally, the 600 MHz square wave power into the IF port is held constant at 10.7 dBm. The 15 GHz carrier power is varied between -15 and 0 dBm. The total transmitted power is measured using a power meter. The power in the first sideband is measured using the spectrum analyzer. Results are shown in Figure 6-14 and indicate the mixers have about 9 dB of loss.

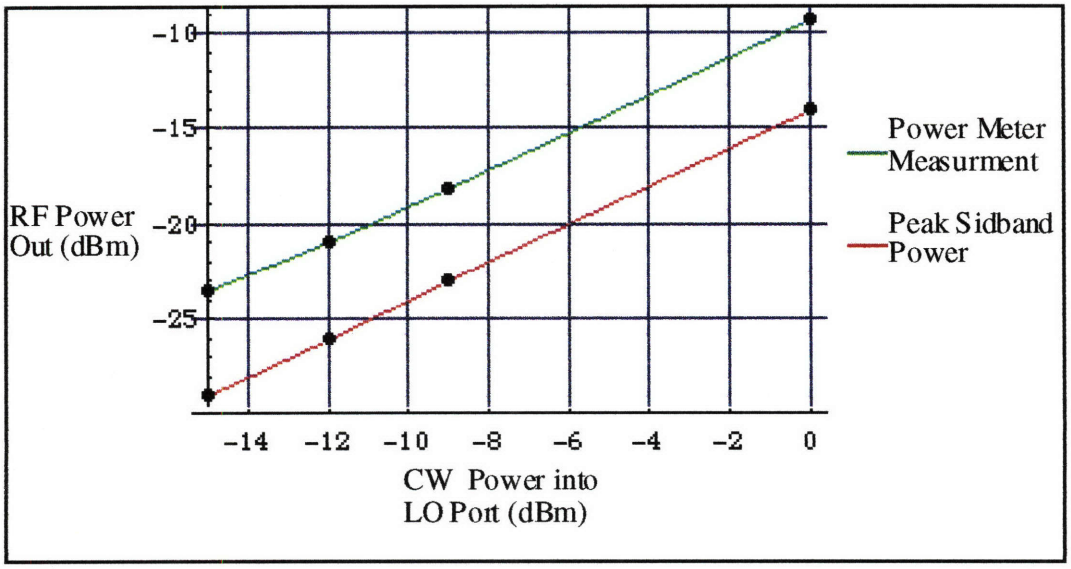


Figure 6-14: RF Power Out vs. Carrier Power In, 16 GHz mixer

Upon receipt of the 24 GHz mixers, the same tests were conducted on them. A typical output spectrum is shown in Figure 6-15. This spectrum show significant clock and carrier leakage. This is due to the poorer port-to-port isolation capabilities of the these mixers compared to their lower frequency counterparts. For the tests on these mixers two power measurements are typically taken on the spectrum analyzer. One, referred to as "peak spreading power", is the highest power level on the $[\sin(x)/x]^2$ curve. The other, called

"peak leakage power", is the highest power level of the carrier leakage. The best balance possible on the carrier and PN code driving the mixer results in the clock leakage always

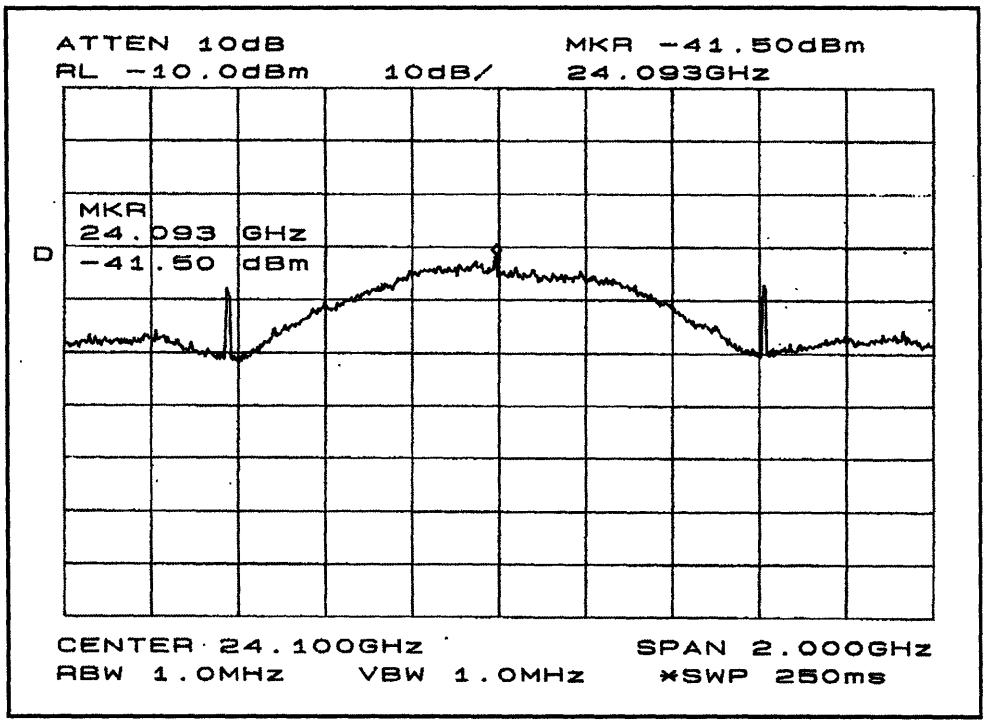


Figure 6-15: 24 GHz Transmit Spectrum

being lower than the "peak spreading power". For this project, we are only interested in the highest power levels transmitted so measurements on the clock leakage are not taken.

The results from these tests are shown in Figure 6-16 through Figure 6-19. These figures are presented without further comment except to note that for the first test on the 24 GHz mixers, measurements are taken at three bandwidth settings on the spectrum analyzer, 2 MHz, 1 MHz, and 100 KHz. As can be seen in Figure 6-16, 100 KHz simply is not enough bandwidth for the spectrum analyzer to make an accurate measurement of a noise-like signal whose bandwidth is on the order of one GHz.

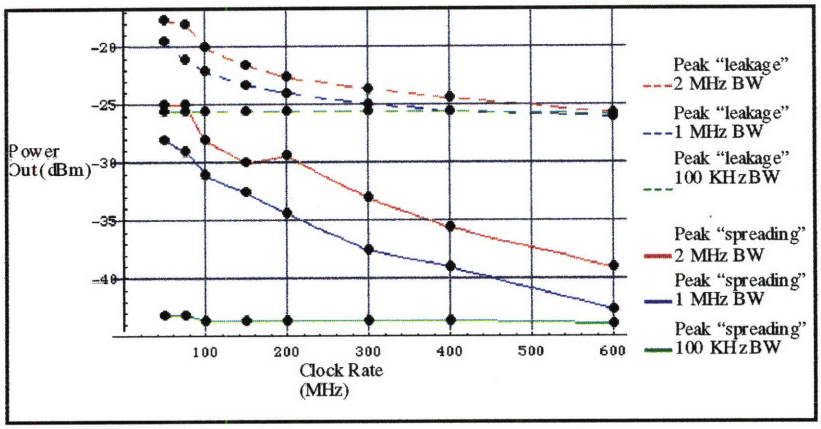


Figure 6-16: Power Out vs. Code Rate, 24 GHz mixer

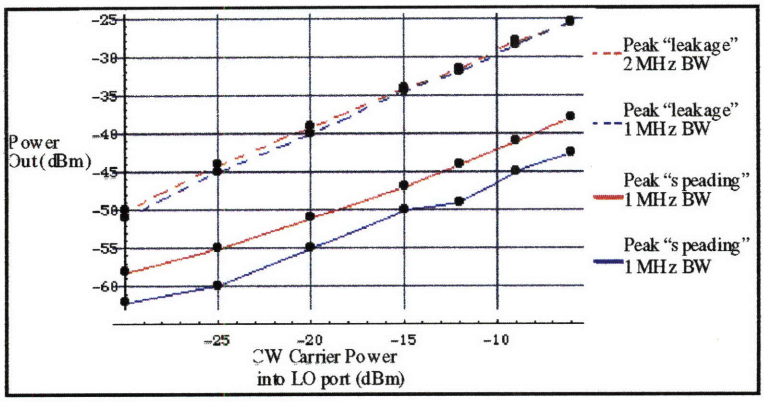


Figure 6-17: Power Out vs. Carrier Power In, 24 GHz mixer

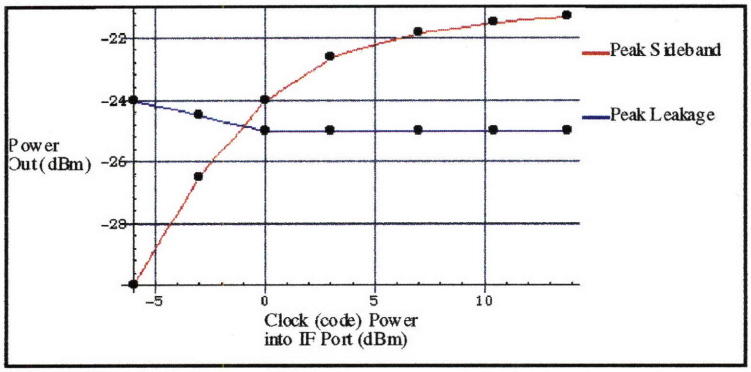


Figure 6-18: Power Out vs. Code Power In, 24 GHz mixer

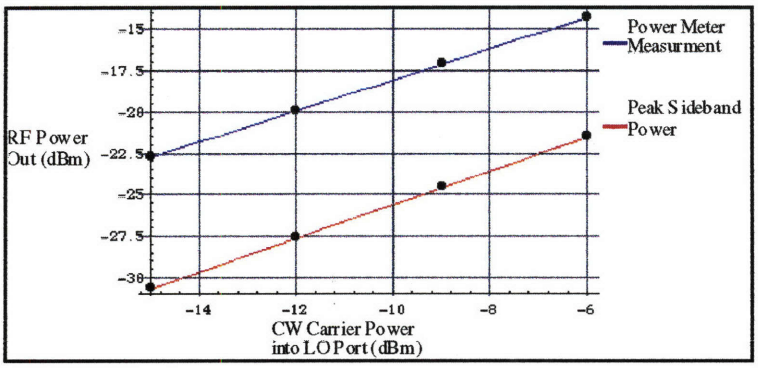


Figure 6-19: RF Power Out vs. Carrier Power In, 24 GHz mixer

6.6 Receiver Characteristics

The delay unit is now ready for integration into the system. The system is assembled as shown in Figure 6-20. Other than the baseband amplifier and detector/display components, this is now the complete system. The target is a tetrahedral corner reflector, 17 cm long per side, located 60 cm from the antennas. The spectral output of the correlator and the

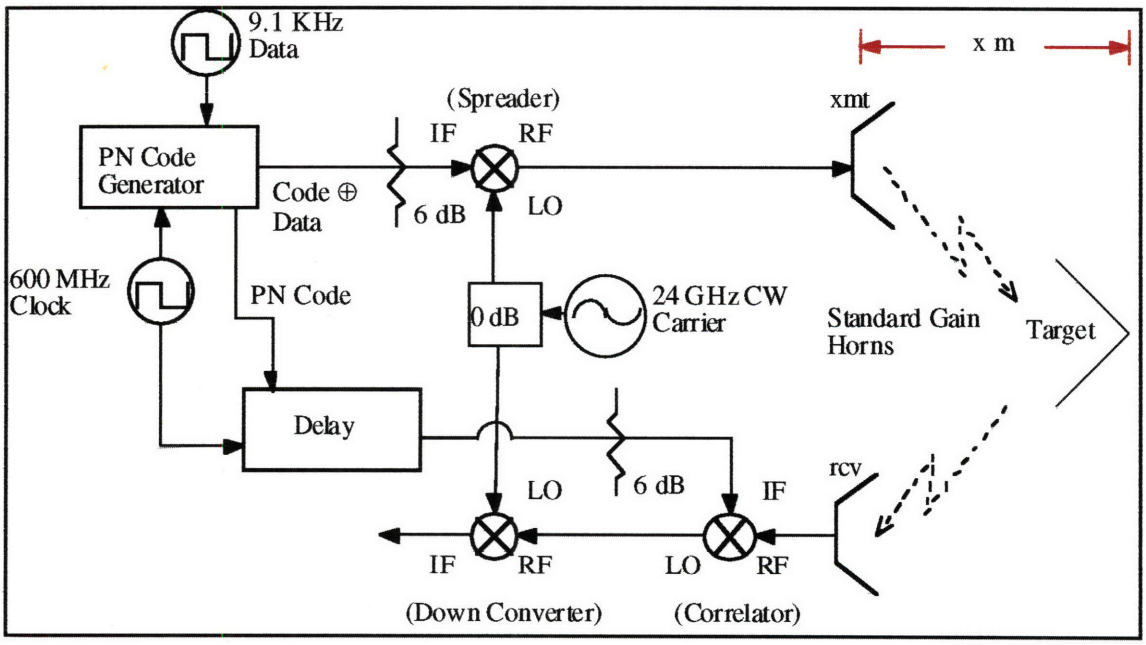


Figure 6-20: System Test Setup

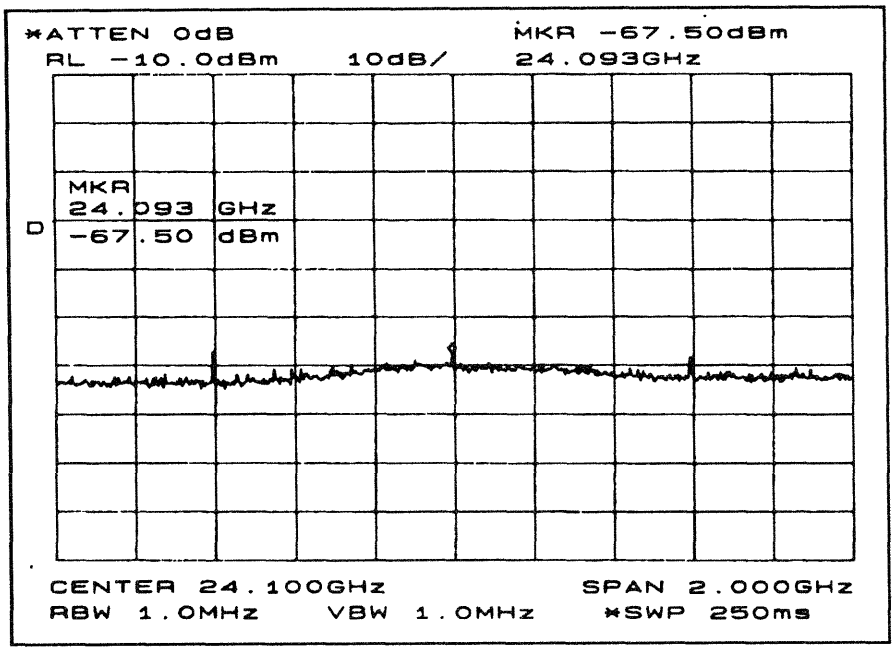


Figure 6-21: Gate 1 Microwave Spectrum

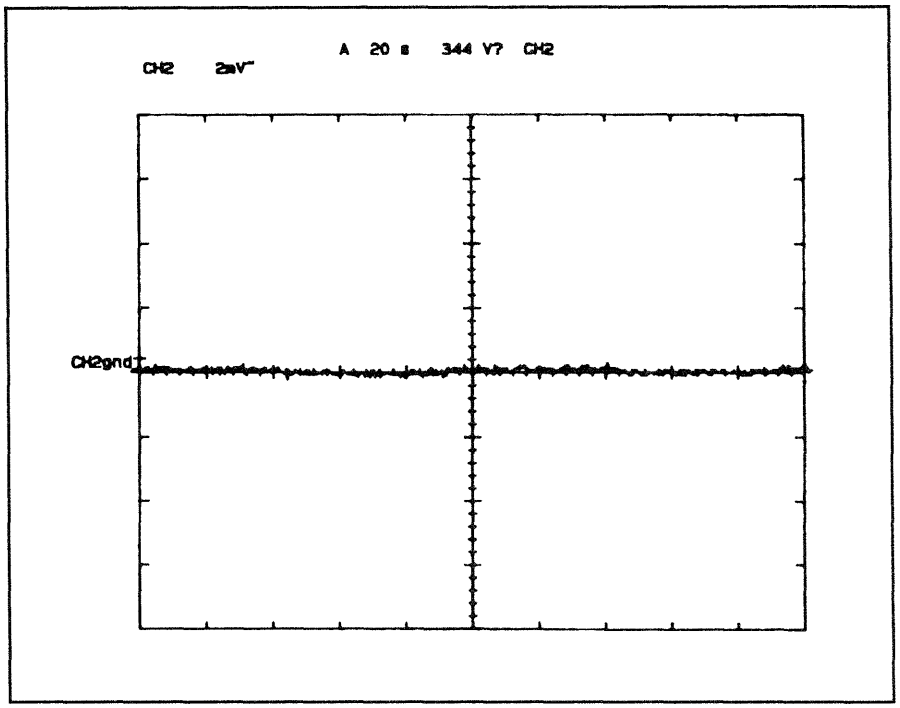
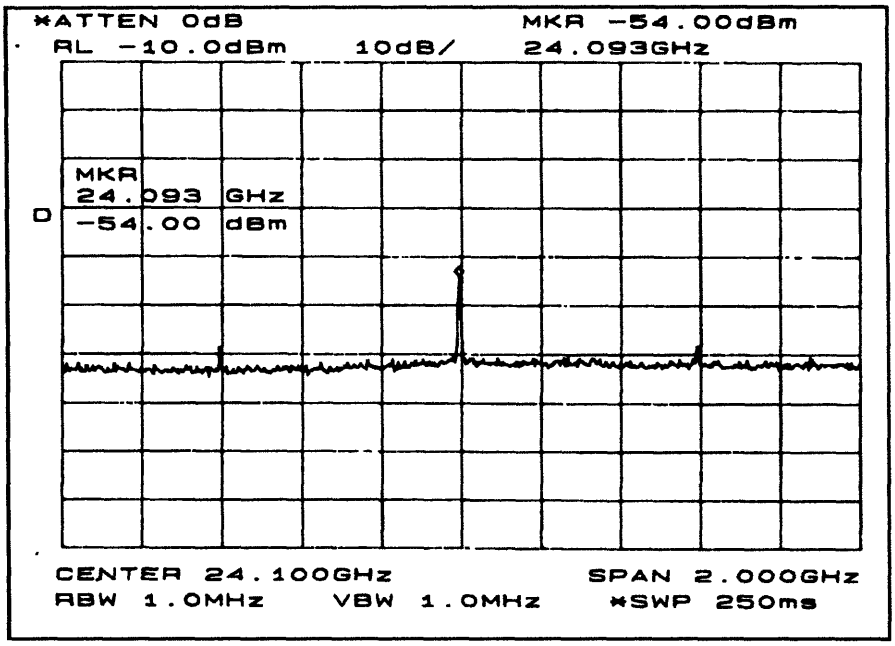


Figure 6-22: Gate 1 Baseband

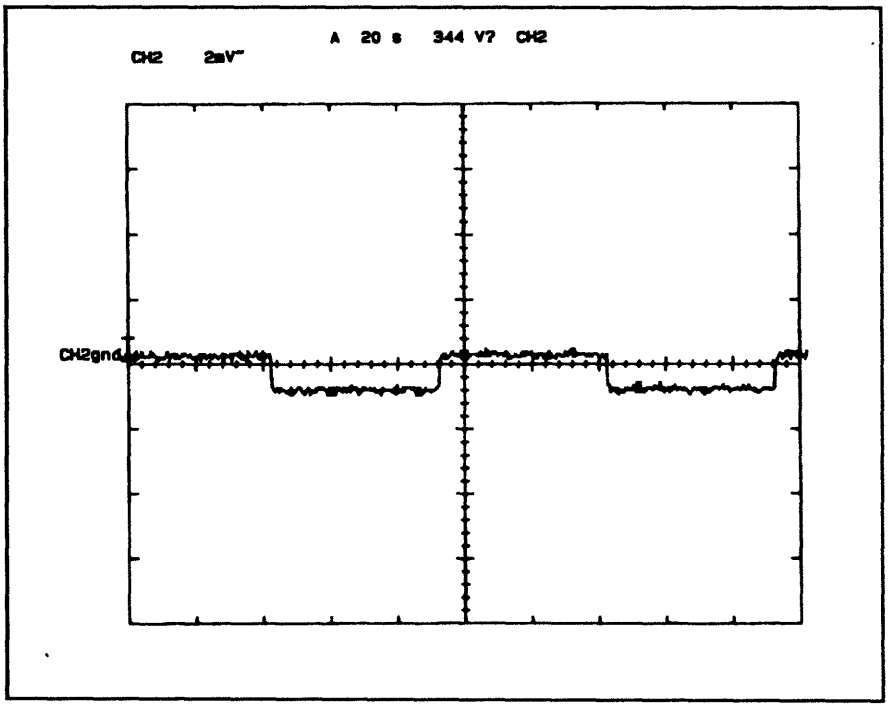
baseband output of the down converter are examined at each range gate setting.

The spectral output of the correlator and the baseband output of the down converter are shown in Figure 6-21 and Figure 6-22, respectively. Recall that this range gate represents a two chip delay in the PN code. Only very small energy components are visible in the spectrum with the majority of energy



below the noise floor of the analyzer. This indicates that the target is located in the outside tail of the range gate. No output is visible in the baseband signal.

Figure 6-23: Gate 2 Microwave Spectrum



When the delay unit is switched to the second range gate, which provides for 3 chips of delay, the outputs shown in Figure 6-23 and Figure 6-24 are observed. The spectral component at the carrier frequency is now 13.5 dB higher in power than before showing that the

Figure 6-24: Gate 2 Baseband

wideband signal is being correlated with the delayed code and remapped into the expected narrow bandwidth. This indicates the target is located near the center of this range bin. The baseband now contains the data signal square wave with an amplitude of roughly 2 mV_{p-p} which when filtered and amplified will trigger the detection circuitry. A DC offset of roughly -.75 mV is present on the detect signal. This offset level varies slightly from time to time. Since the detection circuitry which will eventually trigger off this signal will be designed to trigger off the AC rather than the DC component, the offset presents no concern.

The microwave spectral and the baseband outputs with the unit switched to the third range gate are shown in Figure 6-25 and Figure 6-26. This time no distinct spectral components are visible at the carrier frequency. Only a low amplitude, wideband spectrum, almost completely in the noise floor is visible. This indicates that the target does not lie anywhere within this range bin and virtually all the returned energy is being spread into wideband energy by the correlation process. In other words, the correlation function is at its minimum value. No output is visible in the baseband and no

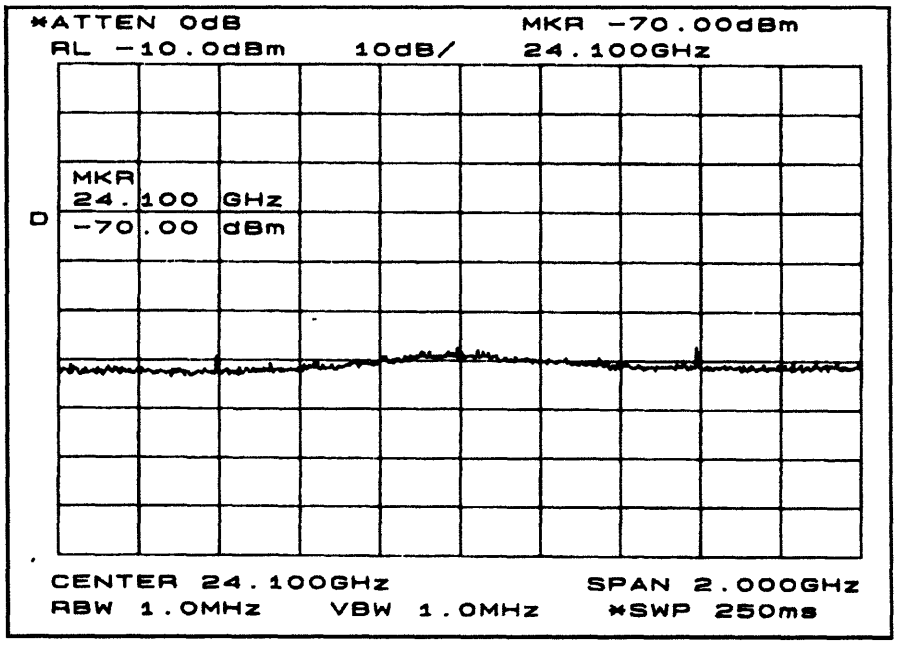


Figure 6-25: Gate 3 Microwave Spectrum

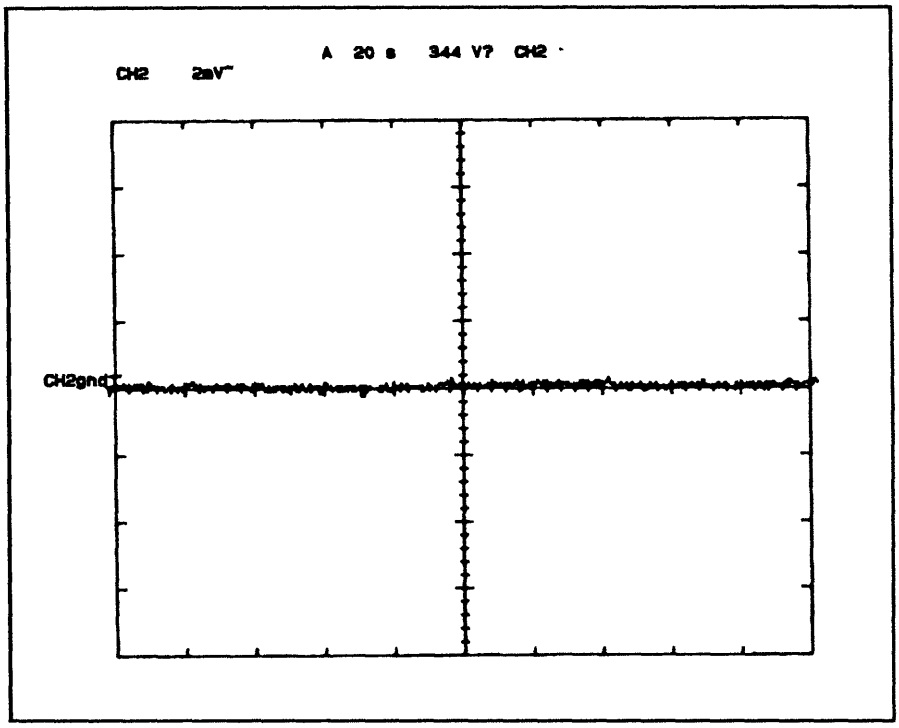


Figure 6-26: Gate 3 Baseband

detect would be triggered.

The outputs with the system set to range gates four through eight are all very similar to the outputs with at range gate three. The plots of those outputs is omitted for brevity. The target was moved through all eight range bins and the system was cycled through all bins with the target at each position to verify the full functionality of the delay unit and the overall system. The results are identical to those presented above with the outputs from the proper range bin being distinctly present while no output is present on the other bins. When the target is positioned midway between two adjacent range bins, the outputs of those two bins are similar to those of bin two above but at reduced amplitude as we would expect for a target positioned midway down the autocorrelation curve. All other bins give no response.

7. Baseband Amplifier

7.1 Amplifier Design

The baseband amplifier and bandpass filter depicted in Figure 3-4 on page 20 are combined in a single, two-stage amplified filter. The filter's schematic is shown in Figure 7-1.

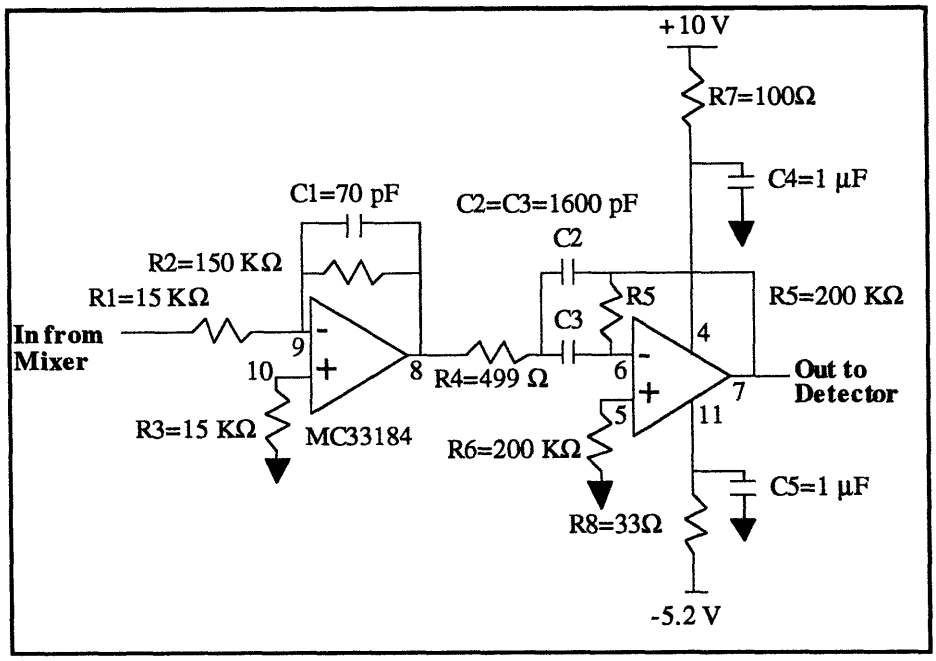


Figure 7-1: Baseband Amplifier Schematic

The baseband amplifier serves to amplify and filter the fundamental harmonic of the data signal square wave which is encoded on the PN waveform and pass the resultant sine wave on to the detection circuitry. A minimum gain of 40 dB is required to amplify the 1 to 2 mV_{p-p} square waves seen at the output of the down-converting mixer to a sufficient amplitude to be used by detector circuitry. The presence (of sufficient amplitude) of this

resultant sine wave at the input to the detector circuit indicates the presence of a target within a particular range gate.

Initially a single-stage, amplified, bandpass filter was built and tested. This amplifier consisted of what is shown as the second stage of the amplifier in Figure 7-1. The design of this bandpass filter was taken directly from Daryanani[6]. The voltage transfer function of this filter is seen to be:

$$T_{BP} = \frac{-s/R_4C_2}{s^2 + s\left(\frac{1}{R_5C_3} + \frac{1}{R_5C_2}\right) + \frac{1}{R_4R_5C_2C_3}} \qquad (7\text{-}1)$$

This is of the form:

$$K_1 \frac{s}{s^2 + \frac{\omega_p}{Q_p}s + \omega_p^2}. \qquad (7\text{-}2)$$

with pole frequency and Q given by:

$$\omega_p = \sqrt{\frac{1}{R_4R_5C_2C_3}}, \qquad (7\text{-}3) \qquad Q_p = \frac{\sqrt{\frac{1}{R_4R_5C_2C_3}}}{\frac{1}{R_5C_3} + \frac{1}{R_5C_2}} = \frac{\sqrt{\frac{R_5}{R_4}}}{\sqrt{\frac{C_2}{C_3}} + \sqrt{\frac{C_3}{C_2}}}. \qquad (7\text{-}4)$$

K is given by:

$$K = \frac{-1}{R_4C_2} = -2\omega_pQ_p. \qquad (7\text{-}5)$$

With $C_2 = C_3 = 1600$ pF, R4 = 499Ω, and R5 = 200KΩ, the Bode magnitude plot is shown in Figure 7-2.

As can be seen from equation 7-5, the pole frequency is affected by the value of R_4. It must be emphasized that this value is actually the total input impedance of the filter and is the sum of the value of R_4 and the output impedance of the circuit driving the filter. This was not anticipated to be a problem since the mixers are all specified to have 50Ω output impedance.

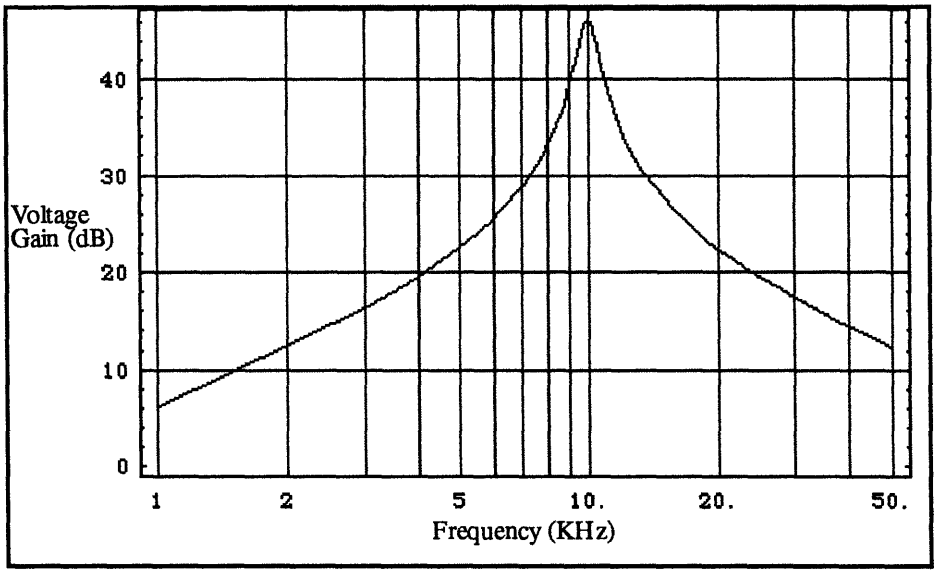


Figure 7-2: Bandpass stage Voltage Gain versus Frequency

However, driving the filter with the 24 GHz mixer shifted the pole frequency from the value of 9.4 KHz when driven with 50Ω lab equipment down to 4.1 KHz. Back calculations using equation 7-1 indicated the mixer had an output impedance of over 2KΩ. Further research into the mixer characteristics verified that at low frequencies the output impedance does increase significantly above the specifications at rf frequencies.

To alleviate this loading on the input of the filter, a buffer stage is added in front of the filter. The voltage transfer function of the lowpass filter stage is:

$$T_{BP} = \frac{-1/R_1}{\frac{1}{R_2} + j\omega C_1}. \qquad (7\text{-}6)$$

For this filter, the total input impedance, R_1 + the driving circuit output impedance, affects only the gain. The cutoff frequency is unaffected by variations in this term. Neither is the cutoff frequency terribly critical as the primary function of this stage is simply to buffer the input to the bandpass filter. The low output impedance of this filter provided by the op amp maintains the desired characteristics of the bandpass filter. The filter was designed as a lowpass rather than an all pass only to reduce the amount of high frequency noise passed to the bandpass stage. So long as the cutoff frequency is above the pole frequency of the bandpass, overall operation will not be adversely affected. For R_1 = 15KΩ, R_2 = 150KΩ, and C_1 = 70 pF, the Bode magnitude plot of the voltage transfer function is shown in Figure 7-3. The filter's gain is slightly less than that indicated when it is driven by the

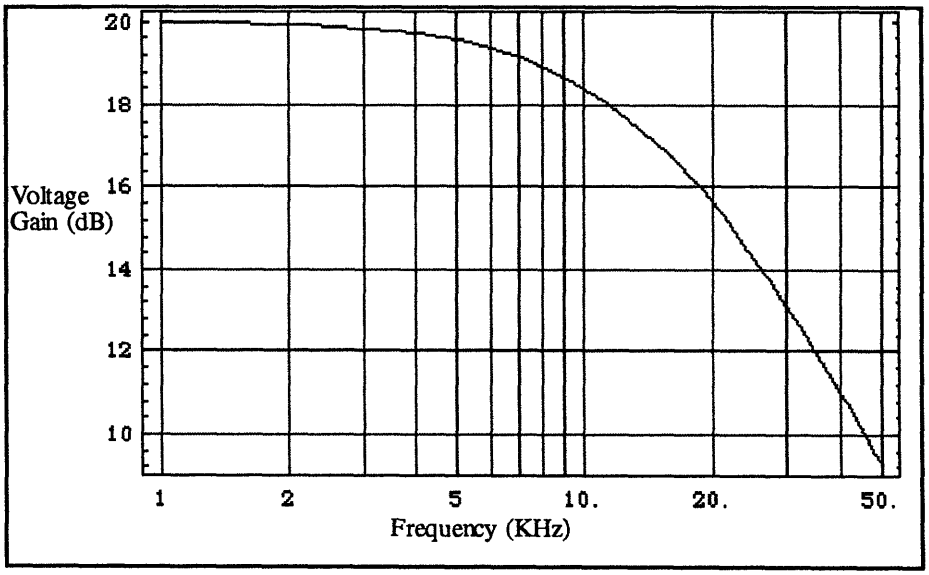


Figure 7-3: Lowpass stage Voltage Gain versus Frequency

mixer since the total input impedance is roughly 17KΩ rather than just the 15KΩ of R_1.

With these two filters cascaded the total transfer function is simply $T_{BP}T_{LP}$. This transfer function is plotted in Figure 7-4. The combined filter now exhibits its pole frequency at 9.4 KHz both when driven with a laboratory function generator as well as when driven with the 24 GHz down-converting mixer.

7.2 Integration and Functionality Tests

With the baseband amplifier in place, the system as shown in Figure 3-4 is complete. Two functionality tests were conducted at this point. First, the system was played against a corner reflector just as discussed in section 6.6, Receiver Characteristics. The amplifier

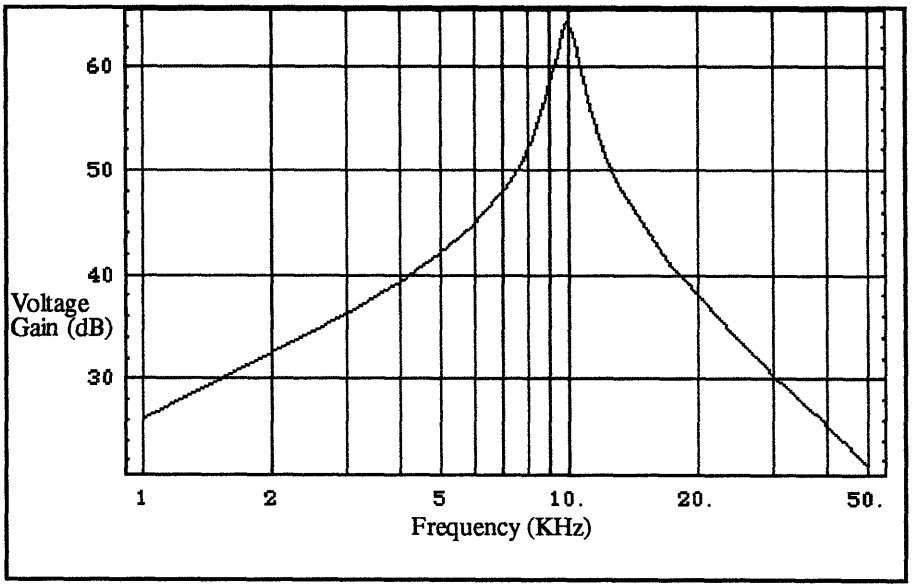


Figure 7-4: Combined Voltage Gain versus Frequency

provides a 250 mV_{p-p} sine wave when the target is in the center of the selected range bin. The amplitude decreases as expected to a minimum value of roughly 20 mV_{p-p} when the

target is completely outside the range bin. At this point the signal has large amounts of narrowband noise combined with the sine wave.

This figure is higher than desired and limits the smallest target, in terms of radar cross section, that can be detected. The antennas were removed and terminated to 50Ω to determine if coupling was occurring directly from one antenna to another. The minimum amplitude, hereafter referred to as the noise floor, did not decrease and the composition of the signal remained unchanged.

Next, the microwave feed to the transmit mixer was disconnected and terminated. The noise floor at the output was then composed of narrow band noise with a peak-to-peak amplitude of roughly 10 mV. No pure sine wave component was discernible. This indicates that the 10 KHz data signal is leaking directly through the transmit mixer and getting onto the microwave line driving the down converter.

A circulator between the 24 GHz power splitter and the transmit mixer was added and the microwave line was reconnected to the transmit mixer. The noise floor remained at roughly 10 mV_{p-p}, however, some sine wave component was discernible. This noise floor is low enough for the radar engineers to conduct their experiments and no further efforts were expended towards reducing if further.

Finally, the system and all necessary support hardware including power supplies, sources, and meters were place on a wheeled equipment cart. The transceiver was placed 990 cm (39 in) above the ground. This rolling test platform was taken outside to large, flat, paved area free of obstacles. The radar was tested, at oblique angles, against a vertical, square metal post, 2 cm per side. It was also tested against human beings. These tests were

conducted by varying the range to the target between 25 and 200 cm in increments of roughly 12 cm. At each range, the output of the baseband amplifier, the detection trigger signal, was examined at all eight range gates.

These fairly informal tests reveal that the radar easily detects these two common obstacles. The detection signal remains at the noise floor for all range gates except the gate or adjacent gates in which the obstacle is positioned. Even at the maximum range of interest, 2 m, both the human body and the metallic posts produced trigger signals of over 100 mV_{p-p}. Unfortunately, the quadrature dropout effect of the receiver was clearly visible. As the range to the obstacle varies by 1.5 mm, the output signal changes from 100 mV all the way down to the noise floor. It appears, that insofar as this radar is concerned, both these targets look very much point targets. The radar engineers will conduct more extensive tests to confirm or refute these initial findings.

8. Combined Code Generator/Delay Unit

With the system assembled and functional, a third circuit was designed which integrates the PN code generator and delay unit onto a single board. Placing both units on a single board reduces the area required. In addition to reducing the overall area, the combined unit has 16 rather than 8 range gates. This increases the maximum detectable range to 4 meters when the system is run at a code generation rate of 600 MHz. The combined board also has a self starting feature which is absent on the individual code generator. The self-starting circuitry will detect if the generator ever enters the all zeros state and will provide a signal to restart the system. The block diagram is shown in Figure 8-1. For clarity, clock lines have been omitted from the diagram. However, all D-registers are clocked synchronously just as before.

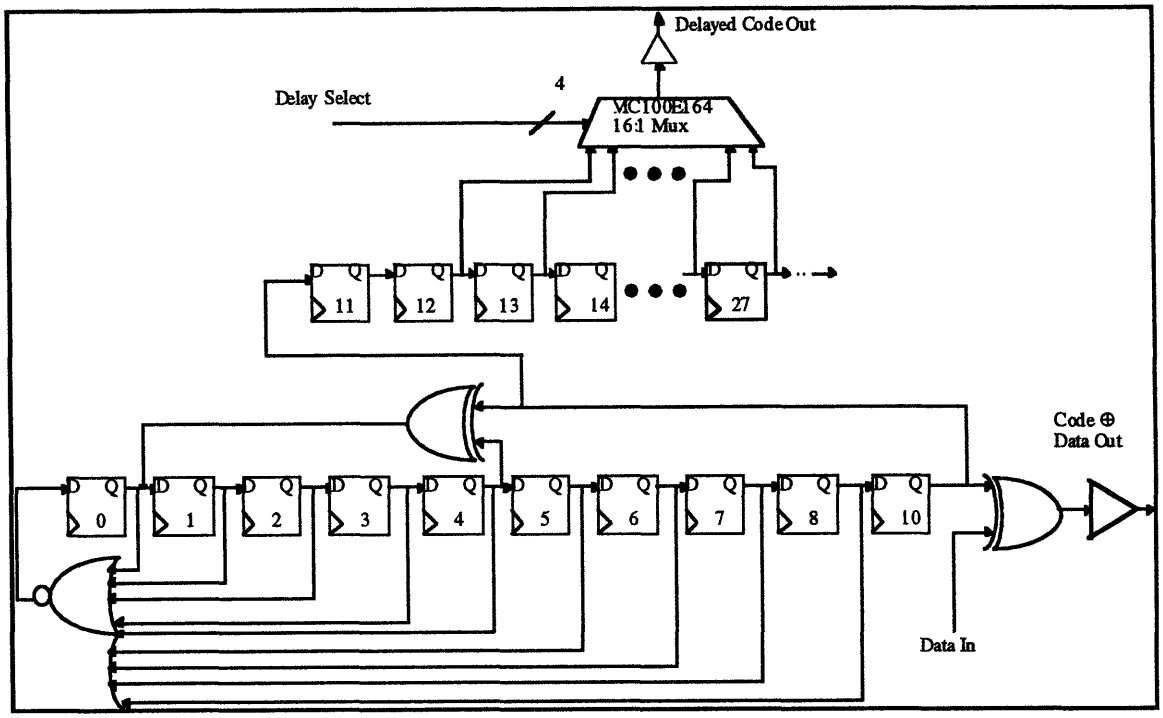


Figure 8-1: Combined Unit Block Diagram

Motorola MC100E151, 6 bit D-registers are used for both the code generator portion and the delay portion of the circuit. A Motorola MC100E164, 16:1 multiplexer allows any one of the 16 range gates to be selected. The same XOR gates and microwave amplifiers as used on the previous boards are used here. Line terminations are Thevenin equivalent just as before.

The self start feature is implemented by taking the NOR of the outputs of all nine code generation stages. Should all nine stages output a zero, the NOR gate produces a high level which is loaded into D-register 0 which acts as a buffer to prevent race conditions. On the next clock cycle, this high will be ORed with the feedback path level, which is zero, and clocked into the first stage of the code generator restarting the system. So long as the system is not in the all zero state the NOR gate will output a zero. Any signal ORed with zero is just the original signal so the system functions normally. The OR of the self start

and the feedback path is implemented using a wired-OR connection. The OR connection is not explicitly shown in the diagram.

There are no 9 input NOR gates in the Motorola ECL family. Three MC100E01, four bit OR/NOR chips were used to implement the required function. This introduces two gate delays along this path.

The same interconnect line widths of .007" and clock line widths of .020" were used just as before. Total current consumption of the board must be calculated to determine the required widths of the power lines. The five, 6-bit register use 90 mA each for a total of 450 mA. The multiplexer requires 80 mA. The two XOR gates and the three XOR gates use 20 mA each for a total of 100 mA. This makes a total of 630 mA required by the integrated circuits. This must be added to the current required by the various resistive networks.

There are five clock line termination networks in parallel. These networks have a resistance of 530Ω. There are 41 interconnect line terminations each equivalent to 580Ω. There is also a voltage divider to provide the required logic high for controlling the multiplexer which has a resistance of 4.4 KΩ. The total resistance across the rails is:

$$\frac{1}{5\left(\frac{1}{530\Omega}\right)+41\left(\frac{1}{580\Omega}\right)+\frac{1}{4400\Omega}} = 12.5\Omega$$ so the total current draw due to the resistors is 400 mA.

The total current draw of the board is, therefore, 1030 mA. As mentioned in section 4.3, given one once copper traces, ANSI standard allow 53 mA per every .001" of line width

while providing no more than 10° C temperature rise above ambient. Therefore, .020" lines will safely carry 1060 mA. Further, the layout of the board insures that no single power trace is carrying any more than 50% of the total current. This still provides a large margin of safety so .020" power traces were used once again.

The layout of the combined board is shown in Figure 8-2. The same microwave substrate used previously was used for this board. The longest delay path is in the self start circuitry. It is a total of 11.5 cm long and passes through two OR/NOR gates. The delay of this line is 551 ps. The gates add an additional 660 ps propagation delay. As before, the registers have a setup time of 0 ps and a propagation delay of 800 ps. The total delay then is 2.07 ns. The highest clock frequency with which the system can be guaranteed to function is about 500 MHz. This frequency provides a range resolution of 30 cm.

Initial functionality tests show the unit functions acceptably up to a clock frequency of 600 MHz indicating that the component on this board are also operating closer to their specified typical values than their guaranteed worst case values. The self-start circuitry also functions as expected and upon startup or momentary clock disruption code generation is resumed automatically.

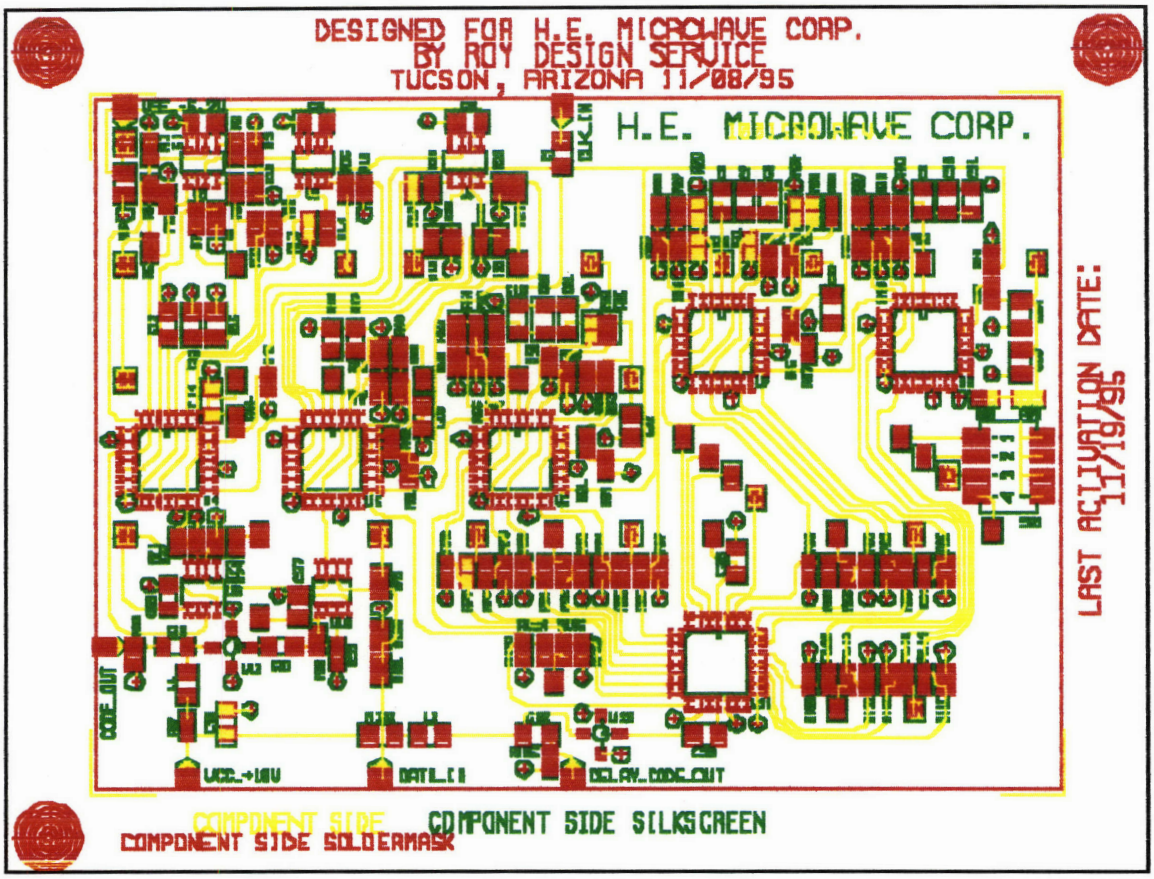


Figure 8-2: Combined Board Layout

9. Conclusions

The range resolution of any backing and parking aid is limited by the cosine error. This error occurs when an obstacle, or a portion thereof, lies off the center line of measurement. In such a situation, the object will be closer to the automobile's bumper than to the sensor making the measurement. The greatest resolution which any practical backing and parking aid may report is limited to the largest distance which an obstacle may be away from the sensing unit at the moment the automobile's bumper contacts the obstacle. If a single sensor is mounted in the middle of the rear bumper, this distance is equal to one-half the total width of the vehicle.

Adding multiple sensors across the rear of the automobile will reduce this distance and allow greater range resolutions to be reported. However, no practical backing and parking aid is likely to be able to report range resolutions greater than about 25 cm anytime in the near future. Therefore, individual sensors need not provide for any greater range resolution than 25 cm.

A pseudo-noise (PN) encoded, direct sequence bi-phase shift key (BPSK) modulated microwave radar sensor provides detection and ranging. The bandwidth of such a system is equal to twice the code rate. With a code generation rate of 600 MHz the sensor will provide the desired 25 cm of range resolution with no signal processing required beyond a simple binary level detection circuit. Greater resolution may be obtained by increasing the code generation rate or by increasing the level of signal processing performed. This type of system provides for 100% duty cycle on target illumination. This allows greater sensitivity at lower transmit power levels than pulsed radar systems.

The required maximal sequence PN code may be readily generated from digital registers and gates. Digital registers may also be used to form the required delay line. Emitter coupled logic (ECL) devices provide the required switching speed to allow operation at 600 MHz and beyond. However, ECL devices impose some challenging design requirements. Being current driven devices, they require pull down resistors on every driven line. The necessity of adding at least one, and often two, resistors to every driven line conflicts with the need to keep interconnect lengths as short as possible. Line lengths of more than a few inches quickly become the limiting factor in system speed.

The system designed using these components demonstrates proper functionality. Its ability to provide detection and ranging of two common obstacles encountered while backing or

parking a vehicle has been preliminary demonstrated. However, those obstacles -- a vertical metallic pole and a human being -- both appear to have no radar depth. Consequently, the single channel coherent receiver suffers target dropout even with a carrier frequency of 24 GHz. This suggests that a quadrature receiver will likely be required to guarantee stationary target detection when the vehicle is not moving. The cost of adding a second channel may be offset, however, by the ability to use a lower carrier frequency.

The system has been turned over to the radar engineers for whom it was designed and built. They will make future use of it as a test platform to investigate in depth the feasibility of building a cost effective backing and parking aid using PN encoded spread-spectrum microwave sensors.

10. References

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11. Appendix 1: Mathematica test of PN Code Generator

The code generator feedback paths were verified for correctness prior to construction using the Mathemaitca software package. The code was generated via this software simulation and verified to be maximal. Then the code was autocorrelated over all phase shifts.

11.1 PN Code Generation

The **Mathematica** code used to simulate the PN Code Generator prior to construction is printed below. It is a direct software representation of the hardware implementation. The nine registers of the hardware are represented by a list, named "dregs", of nine elements with the feed-forward dynamics represented by the "**RotateRight**" function. The feedback XOR gate is represented by the "**Xor**" function. Inasmuch as this was a one-time check to guarantee proper feedback connection, no effort was expended in optimizing the code.

Since the **Mathematica** function "**Xor**" operates only on the values "True" and "False", list "dregs" was set up using these variables and is the list on which all relevant calculations occur. List "output" was set up numerically and is used only for output purposes. After each calculation on "dregs", "output" is modified to reflect the current status of "dregs" by letting "1" and "0" represent "True" and "False", respectively. The list "output" is then printed. This was done simply because viewing lists of ones and zeroes was found to be easier than viewing lists of Trues and Falses.

Each output is a list giving the complete state of the hardware at each cycle. The last element in each list is what would be seen at the Code Generator output at that cycle. Thus,

by reading across each line, one sees the total state of the hardware and by reading down the last column one sees the Code Generator output over time.

The code is initiated with the list set to mimic the hardware in the all high state and is looped until the all high state is encountered again. A hard stop set at 550 cycles was inserted to stop the code in case some error prevented the all high state from being reached. Each line of output is numbered for convenience in ensuring that all 511 expected states are present. Clearly, due to the cyclical nature of the output, the code (and the hardware) may be initiated in any state except the all low state without affecting steady-state operation.

```
dregs={True,True,True,True,True,True,True,True,True};
output={0,0,0,0,0,0,0,0,0};
count=1;
While[count<550, For[w=1, w<10,w++,
If[dregs[[w]]==True, output[[w]]=1, output[[w]]=0]];
temp=Xor[dregs[[4]],dregs[[9]]];
dregs=RotateRight[dregs];
dregs[[1]]=temp;
Print[count," ", output];
If[output == {1,1,1,1,1,1,1,1,1} && count > 1, Break[]];
count++]
```

11.2 PN Code Generation Output

The output from the Mathematica test code is printed below and verifies the accuracy of the planned feedback connection in generating a maximal sequence code. Note that there are 511 distinct states (state 512 is the same as state 1 and is the beginning of the next cycle).

```
1  {1, 1, 1, 1, 1, 1, 1, 1, 1}
2  {0, 1, 1, 1, 1, 1, 1, 1, 1}
3  {0, 0, 1, 1, 1, 1, 1, 1, 1}
4  {0, 0, 0, 1, 1, 1, 1, 1, 1}
5  {0, 0, 0, 0, 1, 1, 1, 1, 1}
6  {1, 0, 0, 0, 0, 1, 1, 1, 1}
7  {1, 1, 0, 0, 0, 0, 1, 1, 1}
8  {1, 1, 1, 0, 0, 0, 0, 1, 1}
9  {1, 1, 1, 1, 0, 0, 0, 0, 1}
10 {0, 1, 1, 1, 1, 0, 0, 0, 0}
11 {1, 0, 1, 1, 1, 1, 0, 0, 0}
12 {1, 1, 0, 1, 1, 1, 1, 0, 0}
13 {1, 1, 1, 0, 1, 1, 1, 1, 0}
14 {0, 1, 1, 1, 0, 1, 1, 1, 1}
15 {0, 0, 1, 1, 1, 0, 1, 1, 1}
16 {0, 0, 0, 1, 1, 1, 0, 1, 1}
17 {0, 0, 0, 0, 1, 1, 1, 0, 1}
18 {1, 0, 0, 0, 0, 1, 1, 1, 0}
19 {0, 1, 0, 0, 0, 0, 1, 1, 1}
20 {1, 0, 1, 0, 0, 0, 0, 1, 1}
21 {1, 1, 0, 1, 0, 0, 0, 0, 1}
22 {0, 1, 1, 0, 1, 0, 0, 0, 0}
```

23 {0, 0, 1, 1, 0, 1, 0, 0, 0}
24 {1, 0, 0, 1, 1, 0, 1, 0, 0}
25 {1, 1, 0, 0, 1, 1, 0, 1, 0}
26 {0, 1, 1, 0, 0, 1, 1, 0, 1}
27 {1, 0, 1, 1, 0, 0, 1, 1, 0}
28 {1, 1, 0, 1, 1, 0, 0, 1, 1}
29 {0, 1, 1, 0, 1, 1, 0, 0, 1}
30 {1, 0, 1, 1, 0, 1, 1, 0, 0}
31 {1, 1, 0, 1, 1, 0, 1, 1, 0}
32 {1, 1, 1, 0, 1, 1, 0, 1, 1}
33 {1, 1, 1, 1, 0, 1, 1, 0, 1}
34 {0, 1, 1, 1, 1, 0, 1, 1, 0}
35 {1, 0, 1, 1, 1, 1, 0, 1, 1}
36 {0, 1, 0, 1, 1, 1, 1, 0, 1}
37 {0, 0, 1, 0, 1, 1, 1, 1, 0}
38 {0, 0, 0, 1, 0, 1, 1, 1, 1}
39 {0, 0, 0, 0, 1, 0, 1, 1, 1}
40 {1, 0, 0, 0, 0, 1, 0, 1, 1}
41 {1, 1, 0, 0, 0, 0, 1, 0, 1}
42 {1, 1, 1, 0, 0, 0, 0, 1, 0}
43 {0, 1, 1, 1, 0, 0, 0, 0, 1}
44 {0, 0, 1, 1, 1, 0, 0, 0, 0}
45 {1, 0, 0, 1, 1, 1, 0, 0, 0}
46 {1, 1, 0, 0, 1, 1, 1, 0, 0}
47 {0, 1, 1, 0, 0, 1, 1, 1, 0}
48 {0, 0, 1, 1, 0, 0, 1, 1, 1}
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50 {0, 0, 0, 0, 1, 1, 0, 0, 1}
51 {1, 0, 0, 0, 0, 1, 1, 0, 0}
52 {0, 1, 0, 0, 0, 0, 1, 1, 0}
53 {0, 0, 1, 0, 0, 0, 0, 1, 1}
54 {1, 0, 0, 1, 0, 0, 0, 0, 1}
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56 {0, 0, 1, 0, 0, 1, 0, 0, 0}
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58 {1, 0, 0, 0, 1, 0, 0, 1, 0}
59 {0, 1, 0, 0, 0, 1, 0, 0, 1}
60 {1, 0, 1, 0, 0, 0, 1, 0, 0}
61 {0, 1, 0, 1, 0, 0, 0, 1, 0}
62 {1, 0, 1, 0, 1, 0, 0, 0, 1}
63 {1, 1, 0, 1, 0, 1, 0, 0, 0}
64 {1, 1, 1, 0, 1, 0, 1, 0, 0}
65 {0, 1, 1, 1, 0, 1, 0, 1, 0}
66 {1, 0, 1, 1, 1, 0, 1, 0, 1}
67 {0, 1, 0, 1, 1, 1, 0, 1, 0}
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77 {1, 0, 0, 1, 0, 0, 1, 1, 1}
78 {0, 1, 0, 0, 1, 0, 0, 1, 1}
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81 {1, 1, 1, 0, 1, 0, 0, 1, 0}
82 {0, 1, 1, 1, 0, 1, 0, 0, 1}
83 {0, 0, 1, 1, 1, 0, 1, 0, 0}
84 {1, 0, 0, 1, 1, 1, 0, 1, 0}
85 {1, 1, 0, 0, 1, 1, 1, 0, 1}
86 {1, 1, 1, 0, 0, 1, 1, 1, 0}
87 {0, 1, 1, 1, 0, 0, 1, 1, 1}
88 {0, 0, 1, 1, 1, 0, 0, 1, 1}
89 {0, 0, 0, 1, 1, 1, 0, 0, 1}
90 {0, 0, 0, 0, 1, 1, 1, 0, 0}
91 {0, 0, 0, 0, 0, 1, 1, 1, 0}
92 {0, 0, 0, 0, 0, 0, 1, 1, 1}
93 {1, 0, 0, 0, 0, 0, 0, 1, 1}
94 {1, 1, 0, 0, 0, 0, 0, 0, 1}
95 {1, 1, 1, 0, 0, 0, 0, 0, 0}
96 {0, 1, 1, 1, 0, 0, 0, 0, 0}
97 {1, 0, 1, 1, 1, 0, 0, 0, 0}
98 {1, 1, 0, 1, 1, 1, 0, 0, 0}
99 {1, 1, 1, 0, 1, 1, 1, 0, 0}
100 {0, 1, 1, 1, 0, 1, 1, 1, 0}
101 {1, 0, 1, 1, 1, 0, 1, 1, 1}
102 {0, 1, 0, 1, 1, 1, 0, 1, 1}
103 {0, 0, 1, 0, 1, 1, 1, 0, 1}
104 {1, 0, 0, 1, 0, 1, 1, 1, 0}
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169 {0, 0, 0, 0, 0, 1, 1, 0, 1}
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171 {0, 1, 0, 0, 0, 0, 0, 1, 1}
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186 {1, 1, 1, 0, 0, 0, 1, 1, 1}
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189 {0, 0, 1, 1, 1, 1, 0, 0, 0}
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191 {1, 1, 0, 0, 1, 1, 1, 1, 0}
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197 {1, 1, 0, 0, 1, 0, 1, 1, 0}
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199 {1, 0, 1, 1, 0, 0, 1, 0, 1}
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201 {1, 0, 1, 0, 1, 1, 0, 0, 1}
202 {1, 1, 0, 1, 0, 1, 1, 0, 0}
203 {1, 1, 1, 0, 1, 0, 1, 1, 0}
204 {0, 1, 1, 1, 0, 1, 0, 1, 1}
205 {0, 0, 1, 1, 1, 0, 1, 0, 1}
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207 {1, 0, 0, 0, 1, 1, 1, 0, 1}
208 {1, 1, 0, 0, 0, 1, 1, 1, 0}
209 {0, 1, 1, 0, 0, 0, 1, 1, 1}
210 {1, 0, 1, 1, 0, 0, 0, 1, 1}
211 {0, 1, 0, 1, 1, 0, 0, 0, 1}
212 {0, 0, 1, 0, 1, 1, 0, 0, 0}
213 {0, 0, 0, 1, 0, 1, 1, 0, 0}
214 {1, 0, 0, 0, 1, 0, 1, 1, 0}
215 {0, 1, 0, 0, 0, 1, 0, 1, 1}
216 {1, 0, 1, 0, 0, 0, 1, 0, 1}
217 {1, 1, 0, 1, 0, 0, 0, 1, 0}
218 {1, 1, 1, 0, 1, 0, 0, 0, 1}
219 {1, 1, 1, 1, 0, 1, 0, 0, 0}
220 {1, 1, 1, 1, 1, 0, 1, 0, 0}
221 {1, 1, 1, 1, 1, 1, 0, 1, 0}
222 {1, 1, 1, 1, 1, 1, 1, 0, 1}
223 {0, 1, 1, 1, 1, 1, 1, 1, 0}
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225 {0, 1, 0, 1, 1, 1, 1, 1, 1}
226 {0, 0, 1, 0, 1, 1, 1, 1, 1}
227 {1, 0, 0, 1, 0, 1, 1, 1, 1}
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229 {1, 0, 1, 0, 0, 1, 0, 1, 1}
230 {1, 1, 0, 1, 0, 0, 1, 0, 1}
231 {0, 1, 1, 0, 1, 0, 0, 1, 0}
232 {0, 0, 1, 1, 0, 1, 0, 0, 1}
233 {0, 0, 0, 1, 1, 0, 1, 0, 0}
234 {1, 0, 0, 0, 1, 1, 0, 1, 0}

235 {0, 1, 0, 0, 0, 1, 1, 0, 1}
236 {1, 0, 1, 0, 0, 0, 1, 1, 0}
237 {0, 1, 0, 1, 0, 0, 0, 1, 1}
238 {0, 0, 1, 0, 1, 0, 0, 0, 1}
239 {1, 0, 0, 1, 0, 1, 0, 0, 0}
240 {1, 1, 0, 0, 1, 0, 1, 0, 0}
241 {0, 1, 1, 0, 0, 1, 0, 1, 0}
242 {0, 0, 1, 1, 0, 0, 1, 0, 1}
243 {0, 0, 0, 1, 1, 0, 0, 1, 0}
244 {1, 0, 0, 0, 1, 1, 0, 0, 1}
245 {1, 1, 0, 0, 0, 1, 1, 0, 0}
246 {0, 1, 1, 0, 0, 0, 1, 1, 0}
247 {0, 0, 1, 1, 0, 0, 0, 1, 1}
248 {0, 0, 0, 1, 1, 0, 0, 0, 1}
249 {0, 0, 0, 0, 1, 1, 0, 0, 0}
250 {0, 0, 0, 0, 0, 1, 1, 0, 0}
251 {0, 0, 0, 0, 0, 0, 1, 1, 0}
252 {0, 0, 0, 0, 0, 0, 0, 1, 1}
253 {1, 0, 0, 0, 0, 0, 0, 0, 1}
254 {1, 1, 0, 0, 0, 0, 0, 0, 0}
255 {0, 1, 1, 0, 0, 0, 0, 0, 0}
256 {0, 0, 1, 1, 0, 0, 0, 0, 0}
257 {1, 0, 0, 1, 1, 0, 0, 0, 0}
258 {1, 1, 0, 0, 1, 1, 0, 0, 0}
259 {0, 1, 1, 0, 0, 1, 1, 0, 0}
260 {0, 0, 1, 1, 0, 0, 1, 1, 0}
261 {1, 0, 0, 1, 1, 0, 0, 1, 1}
262 {0, 1, 0, 0, 1, 1, 0, 0, 1}
263 {1, 0, 1, 0, 0, 1, 1, 0, 0}
264 {0, 1, 0, 1, 0, 0, 1, 1, 0}
265 {1, 0, 1, 0, 1, 0, 0, 1, 1}
266 {1, 1, 0, 1, 0, 1, 0, 0, 1}
267 {0, 1, 1, 0, 1, 0, 1, 0, 0}
268 {0, 0, 1, 1, 0, 1, 0, 1, 0}
269 {1, 0, 0, 1, 1, 0, 1, 0, 1}
270 {0, 1, 0, 0, 1, 1, 0, 1, 0}
271 {0, 0, 1, 0, 0, 1, 1, 0, 1}
272 {1, 0, 0, 1, 0, 0, 1, 1, 0}
273 {1, 1, 0, 0, 1, 0, 0, 1, 1}
274 {1, 1, 1, 0, 0, 1, 0, 0, 1}
275 {1, 1, 1, 1, 0, 0, 1, 0, 0}
276 {1, 1, 1, 1, 1, 0, 0, 1, 0}
277 {1, 1, 1, 1, 1, 1, 0, 0, 1}
278 {0, 1, 1, 1, 1, 1, 1, 0, 0}
279 {1, 0, 1, 1, 1, 1, 1, 1, 0}
280 {1, 1, 0, 1, 1, 1, 1, 1, 1}
281 {0, 1, 1, 0, 1, 1, 1, 1, 1}
282 {1, 0, 1, 1, 0, 1, 1, 1, 1}
283 {0, 1, 0, 1, 1, 0, 1, 1, 1}
284 {0, 0, 1, 0, 1, 1, 0, 1, 1}
285 {1, 0, 0, 1, 0, 1, 1, 0, 1}
286 {0, 1, 0, 0, 1, 0, 1, 1, 0}
287 {0, 0, 1, 0, 0, 1, 0, 1, 1}
288 {1, 0, 0, 1, 0, 0, 1, 0, 1}
289 {0, 1, 0, 0, 1, 0, 0, 1, 0}
290 {0, 0, 1, 0, 0, 1, 0, 0, 1}
291 {1, 0, 0, 1, 0, 0, 1, 0, 0}
292 {1, 1, 0, 0, 1, 0, 0, 1, 0}
293 {0, 1, 1, 0, 0, 1, 0, 0, 1}
294 {1, 0, 1, 1, 0, 0, 1, 0, 0}
295 {1, 1, 0, 1, 1, 0, 0, 1, 0}
296 {1, 1, 1, 0, 1, 1, 0, 0, 1}
297 {1, 1, 1, 1, 0, 1, 1, 0, 0}
298 {1, 1, 1, 1, 1, 0, 1, 1, 0}
299 {1, 1, 1, 1, 1, 1, 0, 1, 1}
300 {0, 1, 1, 1, 1, 1, 1, 0, 1}
301 {0, 0, 1, 1, 1, 1, 1, 1, 0}
302 {1, 0, 0, 1, 1, 1, 1, 1, 1}
303 {0, 1, 0, 0, 1, 1, 1, 1, 1}
304 {1, 0, 1, 0, 0, 1, 1, 1, 1}
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306 {0, 1, 1, 0, 1, 0, 0, 1, 1}
307 {1, 0, 1, 1, 0, 1, 0, 0, 1}
308 {0, 1, 0, 1, 1, 0, 1, 0, 0}
309 {1, 0, 1, 0, 1, 1, 0, 1, 0}
310 {0, 1, 0, 1, 0, 1, 1, 0, 1}
311 {0, 0, 1, 0, 1, 0, 1, 1, 0}
312 {0, 0, 0, 1, 0, 1, 0, 1, 1}
313 {0, 0, 0, 0, 1, 0, 1, 0, 1}
314 {1, 0, 0, 0, 0, 1, 0, 1, 0}
315 {0, 1, 0, 0, 0, 0, 1, 0, 1}
316 {1, 0, 1, 0, 0, 0, 0, 1, 0}
317 {0, 1, 0, 1, 0, 0, 0, 0, 1}
318 {0, 0, 1, 0, 1, 0, 0, 0, 0}
319 {0, 0, 0, 1, 0, 1, 0, 0, 0}
320 {1, 0, 0, 0, 1, 0, 1, 0, 0}
321 {0, 1, 0, 0, 0, 1, 0, 1, 0}
322 {0, 0, 1, 0, 0, 0, 1, 0, 1}
323 {1, 0, 0, 1, 0, 0, 0, 1, 0}
324 {1, 1, 0, 0, 1, 0, 0, 0, 1}
325 {1, 1, 1, 0, 0, 1, 0, 0, 0}
326 {0, 1, 1, 1, 0, 0, 1, 0, 0}
327 {1, 0, 1, 1, 1, 0, 0, 1, 0}
328 {1, 1, 0, 1, 1, 1, 0, 0, 1}
329 {0, 1, 1, 0, 1, 1, 1, 0, 0}
330 {0, 0, 1, 1, 0, 1, 1, 1, 0}
331 {1, 0, 0, 1, 1, 0, 1, 1, 1}
332 {0, 1, 0, 0, 1, 1, 0, 1, 1}
333 {1, 0, 1, 0, 0, 1, 1, 0, 1}
334 {1, 1, 0, 1, 0, 0, 1, 1, 0}
335 {1, 1, 1, 0, 1, 0, 0, 1, 1}
336 {1, 1, 1, 1, 0, 1, 0, 0, 1}
337 {0, 1, 1, 1, 1, 0, 1, 0, 0}
338 {1, 0, 1, 1, 1, 1, 0, 1, 0}
339 {1, 1, 0, 1, 1, 1, 1, 0, 1}
340 {0, 1, 1, 0, 1, 1, 1, 1, 0}

341 {0, 0, 1, 1, 0, 1, 1, 1, 1}
342 {0, 0, 0, 1, 1, 0, 1, 1, 1}
343 {0, 0, 0, 0, 1, 1, 0, 1, 1}
344 {1, 0, 0, 0, 0, 1, 1, 0, 1}
345 {1, 1, 0, 0, 0, 0, 1, 1, 0}
346 {0, 1, 1, 0, 0, 0, 0, 1, 1}
347 {1, 0, 1, 1, 0, 0, 0, 0, 1}
348 {0, 1, 0, 1, 1, 0, 0, 0, 0}
349 {1, 0, 1, 0, 1, 1, 0, 0, 0}
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381 {0, 0, 0, 0, 0, 0, 0, 1, 0}
382 {0, 0, 0, 0, 0, 0, 0, 0, 1}
383 {1, 0, 0, 0, 0, 0, 0, 0, 0}
384 {0, 1, 0, 0, 0, 0, 0, 0, 0}
385 {0, 0, 1, 0, 0, 0, 0, 0, 0}
386 {0, 0, 0, 1, 0, 0, 0, 0, 0}
387 {1, 0, 0, 0, 1, 0, 0, 0, 0}
388 {0, 1, 0, 0, 0, 1, 0, 0, 0}
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473 {0, 0, 0, 0, 0, 1, 0, 0, 1}
474 {1, 0, 0, 0, 0, 0, 1, 0, 0}
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482 {1, 1, 0, 0, 1, 1, 0, 0, 1}
483 {1, 1, 1, 0, 0, 1, 1, 0, 0}
484 {0, 1, 1, 1, 0, 0, 1, 1, 0}
485 {1, 0, 1, 1, 1, 0, 0, 1, 1}
486 {0, 1, 0, 1, 1, 1, 0, 0, 1}
487 {0, 0, 1, 0, 1, 1, 1, 0, 0}
488 {0, 0, 0, 1, 0, 1, 1, 1, 0}
489 {1, 0, 0, 0, 1, 0, 1, 1, 1}
490 {1, 1, 0, 0, 0, 1, 0, 1, 1}
491 {1, 1, 1, 0, 0, 0, 1, 0, 1}
492 {1, 1, 1, 1, 0, 0, 0, 1, 0}
493 {1, 1, 1, 1, 1, 0, 0, 0, 1}
494 {0, 1, 1, 1, 1, 1, 0, 0, 0}
495 {1, 0, 1, 1, 1, 1, 1, 0, 0}
496 {1, 1, 0, 1, 1, 1, 1, 1, 0}
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498 {1, 1, 1, 1, 0, 1, 1, 1, 1}
499 {0, 1, 1, 1, 1, 0, 1, 1, 1}
500 {0, 0, 1, 1, 1, 1, 0, 1, 1}
501 {0, 0, 0, 1, 1, 1, 1, 0, 1}
502 {0, 0, 0, 0, 1, 1, 1, 1, 0}
503 {0, 0, 0, 0, 0, 1, 1, 1, 1}
504 {1, 0, 0, 0, 0, 0, 1, 1, 1}
505 {1, 1, 0, 0, 0, 0, 0, 1, 1}
506 {1, 1, 1, 0, 0, 0, 0, 0, 1}
507 {1, 1, 1, 1, 0, 0, 0, 0, 0}
508 {1, 1, 1, 1, 1, 0, 0, 0, 0}
509 {1, 1, 1, 1, 1, 1, 0, 0, 0}
510 {1, 1, 1, 1, 1, 1, 1, 0, 0}
511 {1, 1, 1, 1, 1, 1, 1, 1, 0}
512 {1, 1, 1, 1, 1, 1, 1, 1, 1}

11.3 PN Code Autocorrelation

The **Mathematica** code used generate the autocorrelation function of the PN code is printed below. The auto correlation function is generated in two steps. The first section of code calculates the PN code just as the previous section of code did. However, instead of outputing the complete state of the shift register at each cycle, this section of code only outputs the content of stage nine in the shift register -- the value that would be seen at the output of the code generator each cycle. These are the same values that would be obtained by reading vertically down the last column of the last section except that the low state which is represented by zeros in the previous section have been represented by -1 here. This is

done to simplify the calculation of the autocorrelation function. These values are output as a single list of 511 elements.

```
dregs={True,True,True,True,True,True,True,True,True};
a=1;
While[a<550,
      If[dregs==
            {True,True,True,True,True,True,True,True,True}
             && a > 1, Break[]];
      If[dregs[[9]]==True, drive[a]=1, drive[a]=-1];
      temp=Xor[dregs[[4]],dregs[[9]]];
      dregs=RotateRight[dregs];
      dregs[[1]]=temp;
      a++];
      pncode = Array[drive,511]
```

{1, 1, 1, 1, 1, 1, 1, 1, 1, -1, -1, -1, -1, 1, 1, 1, 1, -1, 1, 1, 1, -1, -1, -1, -1, 1, -1, 1, 1, -1, -1, 1, 1, -1, 1, 1, -1, 1, 1, 1, 1, -1, 1, -1, -1, -1, -1, 1, 1, 1, -1, -1, 1, 1, -1, -1, -1, -1, 1, -1, -1, 1, -1, -1, -1, 1, -1, 1, -1, 1, 1, 1, -1, 1, -1, 1, 1, 1, 1, -1, -1, 1, -1, -1, 1, -1, 1, 1, 1, 1, -1, -1, -1, -1, -1, -1, 1, 1, 1, -1, 1, 1, 1, -1, 1, -1, -1, 1, 1, 1, 1, -1, 1, -1, 1, -1, -1, 1, -1, 1, -1, -1, -1, -1, -1, -1, 1, -1, 1, -1, 1, -1, 1, -1, 1, 1, 1, 1, 1, -1, 1, -1, 1, 1, -1, 1, -1, -1, -1, -1, -1, 1, 1, -1, 1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, -1, 1, 1, -1, -1, -1, -1, -1, 1, -1, 1, 1, 1, -1, 1, 1, 1, 1, 1, -1, -1, -1, 1, 1, 1, 1, -1, -1, 1, 1, -1, 1, -1, -1, -1, -1, 1, -1, 1, 1, 1, 1, 1, 1, 1, -1, -1, -1, 1, -1, 1, 1, -1, -1, -1,1, -1,1, -1, -1, 1, 1, -1, -1, -1, 1, 1, -1, -1, -1, -1, -1, -1, -1, 1, 1, -1, -1, 1, 1, -1, -1, 1, -1, 1, -1, 1, 1, -1, -1, 1, -1, -1, 1, 1, 1, 1, 1, 1, -1, 1, 1, -1, 1, 1, -1, -1, 1, -1, -1, 1, 1, -1, 1, 1, 1, 1, 1, 1, -1, -1, 1, -1, 1, -1, 1, -1, -1, -1, 1, -1, -1, 1, 1, 1, -1, 1, 1, -1, -1, 1, -1, 1, 1, 1, 1, -1, 1, -1, -1, -1, -1, 1, 1, -1, 1, -1, 1, -1, 1, -1, -1, 1, -1, 1, -1, -1, -1, -1, 1, 1, -1, -1, 1, -1, -1, -1, -1, -1, -1, -1, -1, 1, -1, -1, -1, 1, -1, -1, -1, 1, 1, -1, -1, 1, -1, 1, -1, 1, -1, 1, 1, -1, 1, 1, -1, -1, -1, 1, 1, 1, -1, -1, -1, 1, -1, 1, -1, 1, -1, -1, 1, -1, 1, 1, -1, 1, 1, 1, 1, 1, -1, -1, 1, 1, 1, 1, -1, -1, 1, -1, 1, 1, -1, 1, 1, 1, -1, -1, 1, -1, 1, -1, -1, 1, -1, -1, -1, -1, -1, 1, -1, -1, 1, 1, -1, -1, 1, 1, 1, -1, 1, -1, -1, -1, 1, 1, 1, 1, 1, -1, 1, 1, 1, 1, -1, -1, -1, -1, -1}

The next section of code takes this list and computes and plots the discrete autocorrelation function. The discrete autocorrelation is defined as the number of agreements minus the number of disagreements when the PN code is compared, bit-wise, with a phase shifted copy of itself. With the high and low states represented by +1 and -1, respectively, the bit-wise comparison is easily implemented by bit-wise multiplication. Two bits that are the

same will always multiply to +1 while two bits that are different will multipy to give -1. The summation over all such products yields the autocorrelation value at the given phase shift. This entire procedure is carried out for every integer phase shift and the result from each such shift is appended into a single list. This list is then plotted yielding the discrete autocorrelation function plot.

```
r=1;
While[r<532, autocorrelate[r] =
      Apply[Plus, (pncode * RotateRight[pncode, -10+r])];
      r++];
corefunc=Array[autocorrelate, 531]
ListPlot[corefunc, PlotJoined->True, Axes->False];
```

12. Appendix 2: Mathematica Code for Baseband Amplifier

The Mathematica Code used to verify the baseband amplifier design and generate the voltage gain graphs of chapter 7 is included below.

This section of Code defines the low pass amplifier stage and generates the log-linear plot of its gain in dB.

```
g[f_] := -(1/Ra) / ((1/Rb) + (I 2 Pi f c))
Ra=15 10^3;
Rb=150 10^3;
c=70 10^-12;
LogLinearPlot[20 Log[10, Abs[g[f 1000]]], {f, 1, 50},
GridLines -> Automatic, Frame -> True];
```

This section defines the bandpass amplifier stage and generates the log linear plot of its voltage gain in dB.

```
h[f_] := -1/R1/C2 I 2 Pi f /((I 2 Pi f)^2 + I 2 Pi f
(1/R2/C1 + 1/R2/C2) + 1/R1/R2/C1/C2 )
R1 = 499;
R2 = 200 10^3;
C1 = C2 = 1600 10^-12;
LogLinearPlot[20 Log[10, Abs[h[f 1000]]], {f, 1, 50},
GridLines -> Automatic, Frame -> True]
```

Finally, this section of code generates the log linear plot of the cascaded system's voltage gain in dB.

```
LogLinearPlot[20 Log[10, Abs[h[f 1000] g[f 1000]]], {f, 1, 50},
Frame -> True, GridLines -> Automatic]
```