

RM³ Processing for In-plane Optical Interconnects on Si-CMOS and the Impact of Topographic Features on Losses in Deposited Dielectric Waveguides

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Abstract—This paper describes recent progress in a continuing program to develop and apply RM³ (recess mounting with monolithic metallization) technologies for heterogeneous integration. Particular emphasis is placed on the applicability of RM³ integration to in-plane geometries for on-chip optical clock and signal distribution and on the suitability of commercially processed IC wafers for use as substrates for rectangular dielectric waveguides.

Index Terms— optoelectronic integration, heterogeneous integration, hybrid assembly, in-plane laser diodes, rectangular dielectric waveguides.

I. INTRODUCTION

THE desirability of integrating compound semiconductor functionality, including very high speed operation and efficient light emission and detection, with silicon CMOS circuitry has been recognized for many years, and so too have the challenges of doing such integration monolithically. These challenges include (1) significant differences between the lattice periods of silicon, gallium arsenide, and indium phosphide, (2) large differences in the thermal expansion coefficients of these same materials, and (3) the unavailability of large diameter III-V substrate wafers matching the commonly used silicon wafer diameters (200 and 300 mm). Over the years, a variety of approaches have been proposed to overcome these challenges, but in fact the only practical methods available at present to combine III-V functionality with Si-CMOS are in reality only modest refinements of hybrid assembly and bump-bonding techniques first developed almost 40 years ago[1]. A monolithic solution does still not exist.

Integration technology is being studied and developed at MIT to meet this need and thereby to extend the wafer level, batch processing method of manufacture that has had such a major economic impact on integrated electronics, to optoelectronic integration and ultimately to all mixed-media, mixed-material integration. There are several variations of this technology which are being pursued, but they all share very important traits. First, they are all modular in nature in that they all add to, and build upon, an existing and established silicon integrated circuit foundation, and involve additional processing only after the silicon processing has been

essentially completed on a commercial process line.¹ Second, in all of these technologies, the device or devices to be integrated with the silicon IC are placed in recesses formed in the dielectric layers covering the semiconductor wafer as shown in Figure 1a.

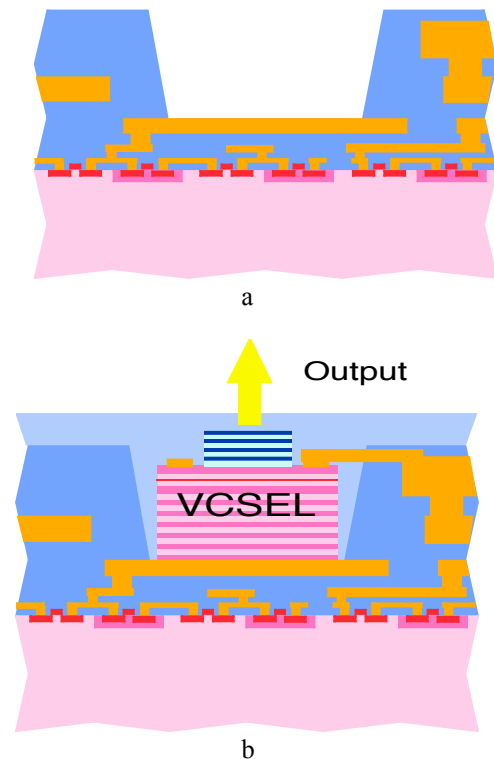


Figure 1 - The RM³ concept: a. A cross-section of one of the recesses formed in the dielectric layers covering a commercially-processed integrated circuit wafer. b. After compound semiconductor heterostructure devices (VCSELs in this illustration) have been put into position in the recesses, their processing has been completed, and they have been connected monolithically with the underlying electronics.

The depth of the recess and thickness of the device structure being integrated are coordinated so that the upper surfaces of the devices are coplanar with the top surface of the integrated

¹ "Essentially" because the additional processing occurs before the bond pads have been opened for bonding and before the wafer has been sawn into individual die.

circuit wafer. This facilitates subsequent processing because it results in a planar surface on which one can deposit continuous metal films and on which precision photolithographic patterning can be performed.

The processing of the wafer is then continued to complete any remaining processing of the devices and to connect them monolithically to the underlying silicon circuitry using photolithographically defined thin-film metal lines.² The resulting integrated unit is pictured in Figure 1b.

This type of integration is described as recess-mounting with monolithic metallization, RM³. Three RM³ technologies, EoE, APB, and MASA, which differ in the method used to do the placement or mounting in the recesses, have been described at previous SMA Annual Symposia [2-3]. Recently a fourth approach which relies on manual placement of heterostructure pills into the recesses has been developed.

In Section II a new application area for RM³ integration, in-plane optical clock and signal distribution through rectangular dielectric waveguides, will be described and in Section III an analysis of suitability of processed silicon IC wafers as substrates for these waveguides will be presented. Finally, the paper will be concluded in Section IV with an overview of the present status of RM³, and comments on future directions the technologies can be expected to take.

II. IN-PLANE, ON-CHIP APPLICATIONS

The primary focus of laser diode research in the past ten years has been on vertical cavity surface emitting lasers (VCSELs) like the one illustrated in Figure 1b, but as interest in chip-to-chip, and even on-chip, optical interconnect has grown dramatically in the past year, it has become clear to some researchers that in-plane lasers offer many advantages in this context. Their geometry and in-plane emission are better

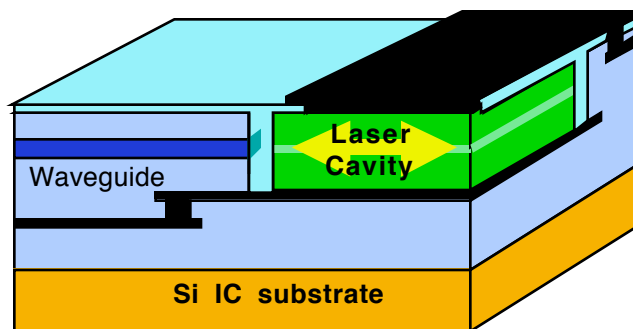


Figure 2 - Cross-sectional drawing illustrating an in-plane laser diode RM³ integrated on a CMOS integrated circuit chip with its output aligned with a planar waveguide for use in on-chip optical interconnect. The laser stripe and facet are formed after bonding to insure precise lateral alignment with the waveguides; vertical alignment is insured by accurate control when the heterostructure is grown.

² The importance of patterned thin film metal interconnects was first recognized by Robert Noyce in 1957 when he invented the monolithic silicon integrated circuit at Fairchild Semiconductor, and with Jack Kilby of TI started the silicon microelectronics revolution. The RM³ technologies recognize that this simple but profound concept is no less important to doing successful heterogeneous integration.

suited to this particular application, they can be modulated at much higher data rates than can VCSELs, and they can readily be fabricated with multiple contacts along the active layer [4] to reduce drive requirements and further increase the modulation frequency. Furthermore one can easily envision adding another layer (or layers) of interconnect to a back-end process sequence, this time for planar optical waveguides. RM³ integration will make it possible to easily align the active laser stripe vertically and laterally with these waveguides, as shown in Figure 2, forming a tightly and efficiently integrated unit. A program of research has been proposed to explore applying RM³ technology to integrating multi-contact in-plane laser diodes for inter- and intra-chip optical communications. As a first step the suitability of processed integrated circuit wafers as substrates for rectangular dielectric waveguides has been evaluated. This study is described in the next section.

III. DIELECTRIC WAVEGUIDES ON SI-IC WAFERS

A. Introduction to the Problem

Using processed silicon integrated circuit (IC) wafers as the foundation for forming optoelectronic integrated circuits (OEICs) has become an important approach to doing heterogeneous integration, and as was discussed in the introduction, several different technologies ranging from flip-chip surface mounting [5] to recess mounting with monolithic metallization, RM³ [1] have now been demonstrated. With these techniques, III-V light emitters and detectors can readily be integrated monolithically on high performance silicon ICs which have been fabricated on state-of-the-art commercial production lines.

The reported applications of OEICs fabricated on Si foundations are almost exclusively directed at surface-normal input and output of the optical signals. While this is the desired geometry for many applications, there is another broad collection of applications for which it would be desirable to direct and guide the optical signals in the plane of the wafer. This is particularly true for the on-chip optical interconnect applications described in Section II; this geometry is also attractive for some fiber-coupled applications. This section addresses the issue of adding monolithic dielectric waveguides to silicon IC wafers to provide thin film interconnect lines for optical signals similar to those which are formed for the electrical signals in the various metal layers.

The problem of forming dielectric waveguides on silicon wafers has been addressed by numerous groups [6], but this work has almost exclusively been done on unprocessed wafers, rather than on wafers which have gone through a complete IC fabrication process. The published work has thus addressed the issues of choosing cladding and core materials, of reducing side-wall losses, and of forming bends, couplers, splitters, etc., but not the issue of forming these guides and structures on the surface of a fully processed integrated circuit wafer.

An important additional complication is introduced when waveguides are deposited on a processed integrated circuit wafer as part of the back-end process because the upper surface

of the wafer is no longer perfectly planar. Thus, waveguide bending losses must be considered for bending in the direction perpendicular to the substrate in addition to the typical in-plane lateral bending losses. Even for processes using a chemical mechanical polishing (CMP) step, long range surface undulations exist on IC wafers that could potentially contribute to losses. In this section we examine these waveguide bending losses using the Marcuse equation [7] and the beam propagation method (BPM) [8] to develop a range of waveguide and process parameters for which these surface undulation losses may safely be ignored.

B. Estimating Wafer Surface Non-planarity

Figure 3 shows in more detail than Fig. 2 the possible structure of an OEIC in which the waveguides are deposited during the back-end processing after deposition and patterning of the metal layers. The waveguide core/cladding material system could be either a CVD or sputter deposited oxynitride or a low-loss polymeric material. Prior to the formation of the waveguide structure and most likely as part of each metal layer formation, the surface would have undergone a series of chemical-mechanical-polishing (CMP) steps to remove local microroughness and local structure left behind by patterning of the metal layers and via formation. CMP typically does a good job of removing local structure so that a high resolution scanning electron microscope (SEM) photomicrograph of the surface after CMP would show a nearly flat surface. However, long range or global planarity, loosely defined here as over a range on the order of 1 mm, is a function of the geometry of the underlying structure and the properties of the CMP pad [9]. In order to determine the bending losses resulting from these long-range surface variations, we approximated the surface as being made up of a series of arcs. If the arc radii

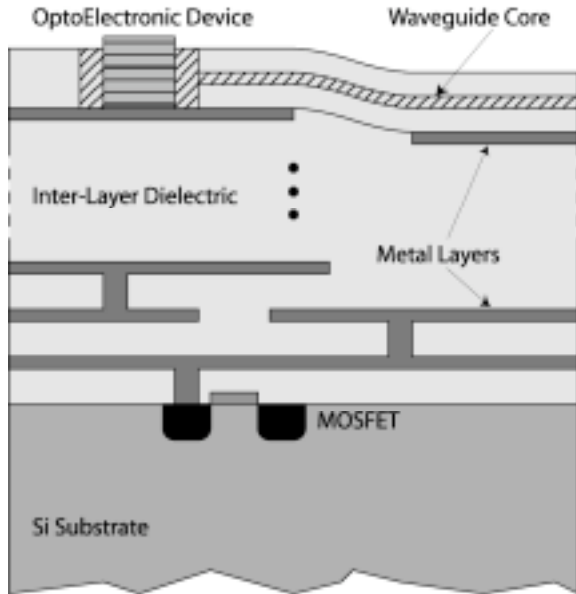


Figure 3 - Schematic cross section of a Si CMOS IC integrated with optoelectronic devices and dielectric waveguides.

can be determined, then an approximate loss per unit length can be calculated using existing knowledge of losses for perfectly circular bends.

Consider the typical case of an inter-layer dielectric (ILD) stack deposited over an area with metal traces. According to the model proposed by Stine *et al.*[10], the relationship between ILD thickness and pattern density can be expressed as [9]:

$$z = z_0 \square z_1 \square K t + \square z_1 \quad (1)$$

when $t > z_1/K$. Here z is the ILD thickness referenced from the top of metal regions, z_0 is the amount of dielectric deposited before CMP, z_1 is the as-deposited metal step height, K is the removal rate for blanket or unpatterned wafers, t is time, and \square is the pattern density. The pattern density for metal traces over some area is defined as the fraction of that area that is covered by the metal traces. For two points A and B on a wafer with the same z_1 and z_0 and different pattern densities \square_A and \square_B , the following applies

$$z_A = z_0 \square z_1 \square K t + \square_A z_1 \quad (2a)$$

$$z_B = z_0 \square z_1 \square K t + \square_B z_1 \quad (2b)$$

$$\square z = z_B \square z_A = z_1 (\square_B \square \square_A) \quad (3)$$

The as-deposited step height, z_1 , is the maximum $\square z$ for two points, A and B, corresponding to the case in which $\square_B = 1$, and $\square_A = 0$. An additional parameter called the planarization length or interaction distance is effectively the minimum distance between points A and B over which the full $\square z$ height difference will be realized from the CMP step. For two points, A and B, separated by less than the planarization length, a fraction of the full $\square z$ height will be realized. The planarization length is a function of the CMP pad type. In general a stiffer pad will have a longer planarization length while a more flexible pad will have a shorter planarization length. Typically, the planarization length falls in the range of 1 to 5 mm.

We now have a $\square z$ surface height variation and a distance (the planarization length) over which this surface height variation occurs. To first order, this surface profile can be approximated with two arcs as shown in Figure 4. The radius, R , is found from the following equation

$$R = \frac{l^2 + \square z^2}{2 \square z} \quad (4)$$

where l is the planarization length and $\square z$ is the height variation from Equation 3.

Based on Equations 1 to 4, a range of possible out-of-plane bending radii can be calculated for typical-to-worst case back-end process scenarios. The worst case scenario corresponds to the case with the tightest bends and consequently the largest bending losses. From Equation 4, clearly the minimum radius corresponds to the minimum l , or minimum planarization length. The minimum planarization

targeted application. It should be noted that not all of these waveguide material systems are necessarily compatible with post back-end processing usually because of the requirement of high annealing temperatures, or because they, by definition, require front-end processing. Nevertheless they represent typical waveguide designs and, therefore, provide some relevance to actual waveguides.

Core Clad	Indices	Application	Dimension Wavelength	Loss
$SiO_2 : Ge$	1.455	Passives,	$5.5 \mu m$	$0.063 dB/cm$
SiO_2	1.445	Fibercoupling	$1.3 \mu m$	
$SiO_2 : Ge$	1.465	Passives,	$3, 4 \mu m$	$0.042 \mu m$
SiO_2	1.445	Fibercoupling	$1.3 \mu m$	$0.23 dB/cm$
Si	3.45	SOI and poly	$< 1 \mu m$	$> 20 dB/cm$
SiO_2	1.45	Si guides	$1.3 \mu m$	
Si_3N_4	2.0	Guides on SiO_2	$1 \mu m$	$1 dB/cm$
SiO_2	1.45		$0.85, 1.3, 1.55 \mu m$	
SiO_xN_y	$1.46 \mu m$	Varied	$1 \mu m$	$0.1 \mu m$
SiO_2	1.45		$10 \mu m$	$1 dB/cm$
$SiO_2 : Ge$	1.46	Si Optical	$10 \mu m$	$< 0.1 dB/cm$
SiO_2	1.45	Bench		

Table I - Typical waveguide materials, parameters, applications, dimensions, and experimentally measured transmission losses [13].

The results of a typical simulation showing predicted bending losses versus bending radius for the two models are shown in Figure 5. The waveguide simulated in this example has a silicon oxynitride core with an index of 1.65, and a silicon dioxide cladding with an index of 1.45. The guide

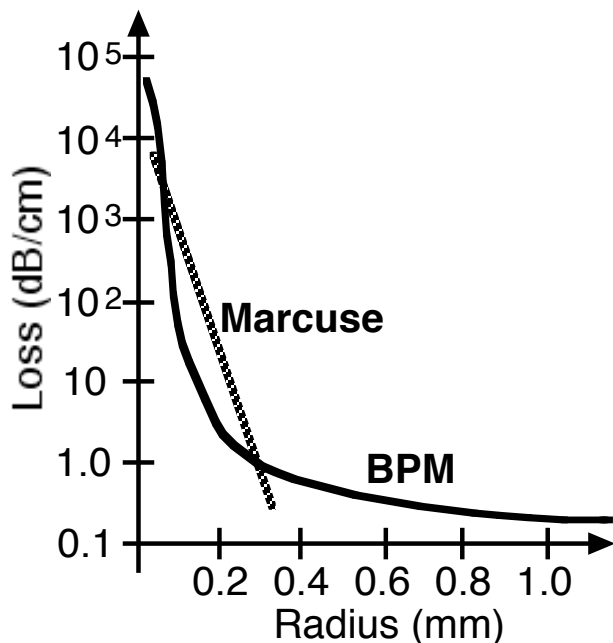


Figure 5 - Waveguide loss at $\lambda = 1.55 \mu m$ versus bending radius predicted by the Marcuse formula and by the BPM simulation in a guide with a $1 \mu m$ by $1 \mu m$ silicon oxynitride ($n = 1.65$) and silicon dioxide cladding ($n = 1.45$).

cross-section is $1 \mu m$ by $1 \mu m$, and the propagating radiation has a wavelength of $1.55 \mu m$. The effective index of the guide is 1.52.

Simulations like those illustrated in Figure 5 were performed for waveguides with silicon dioxide cladding (index = 1.45) and cores with indices yielding index steps of 0.05, 0.1, 0.2, 0.55, and 2.0. The plots of loss as a function of bending radius look qualitatively similar to those in Figure 5, but, of course, show large quantitative variations. An effective way of summarizing the results of these simulations is to compare the bending radii at which a given level of loss is observed for each index step; this comparison is presented in Table II. The values on this table are those found from the BPM simulations. In all cases the Marcuse model yields a far smaller level of loss at a given radius; an example of this behavior can be seen in Figure 5.

n	0.05	0.1	0.2	0.55	2.0
Radius (μm)					
@10 dB/cm	600	275	125	52	20
@ 1dB/cm	1550	610	315	140	50
@0.1dB/cm	4000	1800	1000	450	300

Table II - Bending radii corresponding to bending losses of varying orders of magnitude.

One important observation to make regarding the BPM simulations is that they become increasingly sensitive to round-off errors in the computation as the bending radius is increased and the accuracy of the modeling must be questioned and in particular the leveling off of the loss at large radii, which was seen in all cases, may be in part an artifact of the modeling and in reality the loss may be smaller than indicated. The calculation can be viewed as yielding a conservative estimate of the loss and in spite of this possible effect, still indicates that the loss is negligible;

E. Discussion and Conclusions on Waveguide Layers

It is clear from Table II that for radii of 5 cm or greater, the bending losses may be ignored. This is especially the case for large index contrast guides with higher mode confinement. This is entirely consistent with the fact that rectangular dielectric waveguides are designed so that low-loss lateral bends can be realized with them, and that in most cases bending radii considerably less than 5 cm are sought. The identification of 5 cm with the worst-case bending radius associated the surface undulations on processed IC wafers is clearly a key result of this study.

Using equations which govern the dependence of underlying pattern density on the removal rate of ILD oxide by CMP, a worst case wafer surface profile for a deposited waveguide has been calculated. This corresponds to the surface profile of a Si CMOS wafer after completion of the back-end processing including all metal layers. Given a minimum planarization length of 1mm and a maximum step height of $5 \mu m$, a deposited waveguide would see approximately a 5 cm out-of-plane bending radius. Simulations

using the Marcuse bending loss equation and Rsoft's BeamProp BPM software package, both indicated that for even the worst case scenario, out-of-plane bending losses may be safely ignored as they typically fall well below the range of absorption loss for the corresponding material systems. This implies that modern, CMP-processed integrated circuit wells can be used as low-loss substrates for the deposition of rectangular dielectric waveguides, and that addition of dielectric waveguide interconnect layers to the back-end process sequence is a viable approach to implementing intra-chip optical interconnects and optical clock distribution networks.

IV. CONCLUSION

In this paper we have reviewed the fact that recess mounting with monolithic metallization, RM³, techniques for mixed-material integration on silicon have been demonstrated in several variations and are already being used in research on a wide range of applications for complex optoelectronic integrated circuits in sensing, signal processing, and integrated circuit interconnects. Just as the electronic industry is facing the increasingly difficult challenge of making devices smaller and smaller, and the cost of doing so becomes greater and greater, it is clear that the ability to add III-V semiconductor functionality to silicon integrated circuits will play a larger and larger role in generating new applications and markets for integrated circuits, and will be increasingly important to the electronics industry. RM³ technologies promise to play a major role in providing this ability.

A new area of application for RM³ technologies, that being in-plane propagation geometries, was introduced and a key factor in its implementation, the impact of IC wafer surface topology on rectangular dielectric waveguide scattering losses, has been evaluated. It was found that modern CMP-processed IC wafers can be expected to be smooth enough that their surface topology will not add additional losses to waveguides formed on them.

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