

CHARGE STORAGE EFFECT IN A TRILAYER STRUCTURE COMPRISING GERMANIUM NANOCRYSTALS

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ABSTRACT

A metal-insulator-semiconductor (MIS) device with a trilayer insulator structure consisting of sputtered SiO₂ (~50nm)/evaporated pure germanium (Ge) layer (2.4nm)/rapid thermal oxide (~5nm) was fabricated on a p-type Si substrate. The MIS device was rapid thermal annealed at 1000°C. Capacitance-voltage (C-V) measurements showed that, after rapid thermal annealing at 1000°C for 300s in Ar, the trilayer device exhibited charge storage property. The charge storage effect was not observed in a device with a bilayer structure without the Ge middle layer. With increasing rapid thermal annealing time from 0 to 400s, the width of the C-V hysteresis of the trilayer device increased significantly from 1.5V to ~11V, indicating that the charge storage capability was enhanced with increasing annealing time. High-resolution transmission electron microscopy results confirmed that with increasing annealing time, the 2.4nm amorphous middle Ge layer crystallized gradually. More Ge nanocrystals were formed and the crystallinity of the Ge layer improved as the annealing time was increased. When the measurement temperature was increased from -50°C to 150°C, the width of the hysteresis of the MIS device reduced from ~10V to ~6V. This means that the charge storage capability of the trilayer structure decreases with increasing measurement temperature. This is due to the fact that the leakage current in the trilayer structure increases with increasing measurement temperature.

1. INTRODUCTION

The confinement of carriers in semiconductor nanocrystals has led to several significant observations of physical phenomena and demonstrations of the usefulness in electronic and optoelectronic devices. Recently, researches have been focusing on the charge storage effect and single electron effect of Si nanocrystals [1-9]. It was discovered that the device performance strongly depends on the ability

to control the nanocrystal particle size and distribution, crystallinity, oxide-passivation quality, and crystal-to-crystal isolation that prevents lateral charge conduction in the nanocrystal layer. Fukuda *et al.* [10] had fabricated SiO₂/Ge nanocrystal/SiO₂ structure by oxidizing the electron-beam evaporated Ge film. They attributed the flatband shift in the C-V characteristics of their devices to the charge storage of a single electron in a potential well. Hu *et al.* [11] demonstrated a novel technique of fabricating a Ge nanocrystal quasi-nonvolatile memory device by oxidation of the Si_{1-x}Ge_x layer. We have reported previously the structural characterization results of Ge nanocrystals synthesized by the rapid thermal annealing technique [12,13]. In this article, we report results of a novel trilayer structure fabricated using a combination of electron-beam evaporation and magnetron sputtering techniques to deposit the Ge and SiO₂ layers. We again used the rapid thermal annealing technique to form the Ge nanocrystals in the trilayer structure.

2. EXPERIMENT

The trilayer structures used in this work consist of the following: (i) a thin (~5nm) SiO₂ layer grown using rapid thermal oxidation (RTO) in a dry oxygen ambient at 1000°C for 50s on a p-type silicon substrate, (ii) a pure Ge layer (2.4 nm) deposited on the RTO layer by electron-beam evaporation at a base pressure of 3×10⁻⁷ Torr, and (iii) a top pure SiO₂ cap layer (~50nm) deposited by radio frequency (rf) magnetron sputtering at a rf power of 100W. A control sample with a bilayer structure (i.e., without the middle Ge layer) was also fabricated. The trilayer structure and the control sample were subjected to rapid thermal annealing in an argon ambient at 1000°C for 300s. The rapid thermal anneal ramp-up and ramp-down rates were fixed at 30°C/s.

High-resolution transmission electron microscopy (HRTEM) (Model: Philips FEG300CM) was used to observe the crystallization of the pure Ge layer in the

trilayer structure. The C-V measurements were carried out using a HP4284A precision LCR meter.

3. RESULTS AND DISCUSSIONS

Figure 1 shows the C-V characteristics of a trilayer device (device A) and a control bilayer sample (device B) that had been rapid thermal annealed at 1000°C for 300s. It can be seen from Figure 1 that: (i) both devices A and B have a counter-clockwise hysteresis, (ii) the width of C-V hysteresis of device A is about 10V, and (iii) device B shows very small hysteresis. The results of Figure 1 indicate that the middle Ge layer plays an important role in the charge storage property of the trilayer structure.

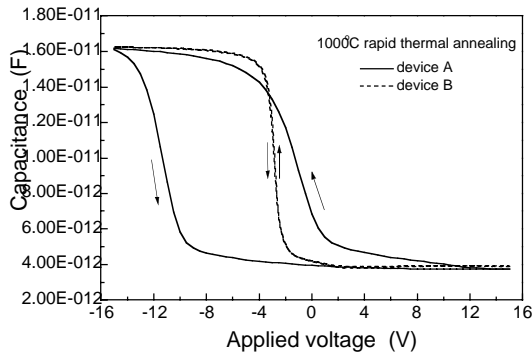


Figure 1: C-V curves of the trilayer structure (device A) and the control bilayer structure (device B). Both devices were rapid thermal annealed at 1000°C for 300s in argon.

We studied further how the charge storage capability of the trilayer structure changes with rapid thermal annealing time. Figure 2 shows the C-V curves of trilayer samples that were rapid thermal annealed for 0, 10, 50, 100, 200 and 400s, respectively. It can be seen that the hysteresis of the C-V curves for the as-prepared sample is very small (1.5V). However, after 10s of rapid thermal annealing, the width of the hysteresis increases to ~7V. This means that the trilayer structure exhibits charge-storage capability after 10s annealing. With increasing annealing time up to 400s, the width of the C-V hysteresis widens to ~11V. Note that the C-V curve shifts slightly to the left and the maximum capacitance of the C-V curves decreases from 18.5 to 14 pF with increasing annealing duration. We suggest that more Ge nanocrystals were formed with increasing annealing time. The increase in the Ge nanocrystals resulted in more charges being trapped. This accounts for the widening of the C-V hysteresis and the shifting of the C-V curve to the left. The reduction in the maximum capacitance of samples prepared with increasing annealing time may be due to the

fact that the dielectric constant of the film decreases with increasing annealing time due to the precipitation of Ge nanocrystals, or the increase in the oxide thickness by oxidation of the underlying Si substrate with increasing annealing duration.

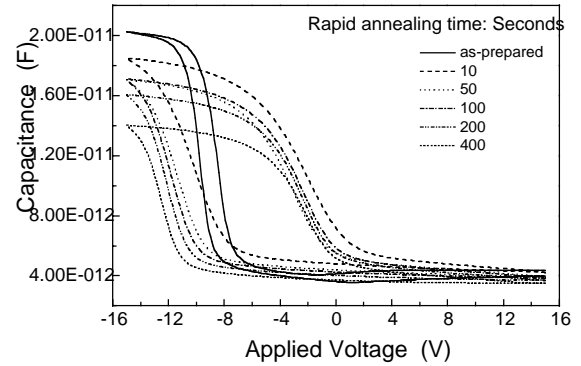


Figure 2: C-V curves, showing different amounts of hysteresis, of trilayer structures with a 2.4nm Ge layer that were rapid thermal annealed for duration of 0, 10, 50, 100, 200 and 400s in argon.

The effect of annealing time on the charge storage capability of the trilayer structure was also studied using the HRTEM. Figures 3(a), 3(b) and 3(c) show the cross-sectional HRTEM micrographs of the trilayer structures that were rapid thermal annealed at 1000°C for 0, 10 and 300s, respectively. Figure 3(a) shows that the as-prepared trilayer structure has distinguishable interfaces between the middle Ge layer with the RTO and top cap oxide layers, and that the Ge layer is amorphous. After rapid thermal annealing for 10s (see Figure 3(b)), the interfaces become less obvious and the Ge middle layer begins to shrink to form Ge nanocrystals. The number of Ge nanocrystals, however, is small and the lattice fringes are not very clear. This shows that the crystallinity of the Ge nanocrystals is not good. After rapid thermal annealing for 300s (Figure 3(c)), the Ge layer has shrunk to form Ge nanocrystals entirely embedded in the oxide. The size of the Ge nanocrystals is around 5nm. The distribution of the nanocrystals is nearly uniform. The density of the nanocrystals is estimated to be $\sim 9 \times 10^{11} \text{ cm}^{-2}$ by counting the numbers of nanocrystals from the plan-view TEM pictures directly (not shown here). The TEM observation also shows that most of the nanocrystals in Figure 3(c) are single crystals, as the lattice fringes can be clearly identified. This indicates that the nanocrystals have good crystallinity after annealing for 300s.

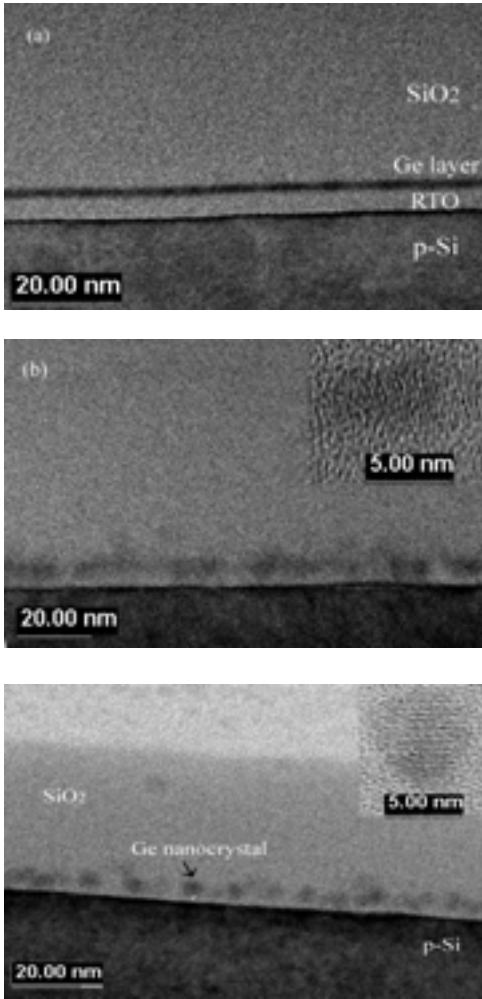


Figure 3: (a), (b) and (c) show the cross-sectional HRTEM images of trilayer structures that were rapid thermal annealed at 1000°C for 0, 10 and 300s, respectively.

In order to investigate the charge storage capability of device A at different temperatures, we measure the width of the C-V hysteresis from -50°C to 150°C, and the results are shown in Figure 4. It can be seen that at -50°C, the hysteresis loop is very large. This means that the charge storage capability is at its best. With increasing measuring temperature from -50 to 150°C, the width of the C-V hysteresis reduces gradually from 10V to 6V and the slope of the C-V curve for the charging branch (sweep from negative to positive gate voltage) becomes gentler. The hysteresis becomes very small at 200°C and this indicates that the device loses its charge-storage capability entirely. The reduction in the hysteresis may be related to the increasing leakage current with increasing measurement

temperature and/or the increase in the thermal energy as compared to the Coulomb charging energy.

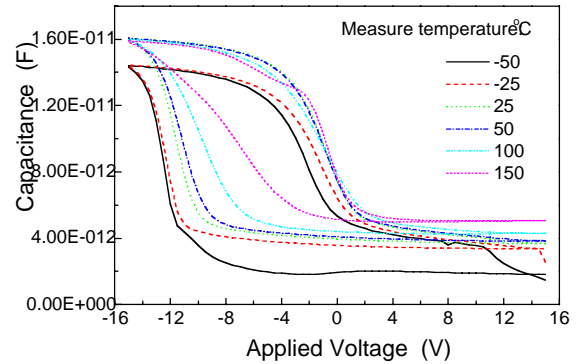


Figure 4: C-V curves measured at temperatures of -50, -25, 25, 50, 100 and 150°C, respectively, of the trilayer structure.

4. CONCLUSION

In conclusion, we have demonstrated a novel trilayer structure device comprising of Ge nanocrystals that has potential in memory applications. The Ge nanocrystals embedded in the oxide is formed by electron-beam evaporation of a thin 2.4nm Ge layer as the middle layer of a trilayer structure. The charge storage capability was improved significantly with increasing annealing time from 10s to 400s, but decreased gradually with increasing measurement temperature from -50°C to 150°C.

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