1. Consider a bipolar junction transistor with an emitter doping level of $10^{18} \text{ cm}^{-3}$, a base doping level of $10^{16} \text{ cm}^{-3}$, and a collector doping level of $10^{15} \text{ cm}^{-3}$. The cross-sectional area of this device is $10^{-7} \text{ cm}$. The width of the base is $W_B = 5 \text{ um}$, and $W_B < L_{DB}$ the minority carrier diffusion length in the base. Assume also that widths of the emitter and collector are much longer than minority carrier diffusion lengths in those regions.

(a) Sketch the equilibrium minority carrier concentration vs distance along the transistor from the emitter to the collector, in every region except for the depletion regions.

Voltages of $V_{EB} = .3 \text{ volts}$ and $V_{CB} = -2 \text{ volts}$ are applied to the device.

(b) What regime of operation is the device in? What will be the relative values of $I_E$, $I_B$, and $I_C$, compared to one another?

(c) Sketch minority carrier concentration vs distance within the device, given the applied biases. Quantitatively label maximum and minimum concentrations within the emitter, base, and collector.

(d) Neglecting the length of the depletion region within the base, determine the current density flowing from the collector to the emitter, $I_{CE}$.

(e) If the polarity of $V_{EB}$ were reversed, how would $I_{CE}$ change (qualitatively)?

2. In a pnp transistor connected to two power sources as shown below:

![Transistor Diagram]

a) A significant collector current can be obtained even for $V_{CB}=0$. Explain how a zero-biased collector-base junction can serve as a collector of minority carriers. Be sure to identify the roles that drift and diffusion might play.

b) Although the effect of increasing $V_{CB}$ from 0 to 10V is not large, it is real. Why does $I_C$ increase slightly for some fixed $I_E$ as $V_{CB}$ is increased?

c). A pnp transistor is used as a phototransistor (i.e. light falling on the device causes a base current which is amplified). How fast could such a device switch? The base width is $50 \mu\text{m}$; assume $D_p = 10 \text{ cm}^2/\text{s}$. 
3. A JFET has its bottom gate connected to the source and grounded. Voltage $V_D$ (positive) is applied to the drain, and voltage $V_G$ (negative) is connected to the top gate.

![JFET Diagram]

a) Sketch the shape of the depletion regions inside the device when $V_G$ is made large enough to pinch off the channel with $V_D = 0$.
b) You are told that the pinch-off gate voltage $V_p = -8V$ when $V_D = 0$ and the two gates are electrically connected together. Based on this, determine the pinch-off voltage $V_{PT}$ for the case shown above when $V_D = 0$. Assume that the built-in voltage $V_o = 1V$. Is this answer consistent with the sketch in part a)?
c) Assuming $V_{PT} < V_G < 0$, sketch the depletion regions when the drain voltage is increased to the pinch-off point.
d) Derive an expression for $V_{D,sat}$ in terms of $V_{PT}$, $V_o$, and $V_G$ when the bottom gate is tied to ground. (Your answer should contain only voltages).
e) In light of your answers for c) and d), will $V_{D,sat}$ for the case of the bottom gate tied to ground be greater or less than the $V_{D,sat}$ for the case when the two gates are tied to each other? Explain.

4. An ideal MOS junction is shown below. Band bending has caused the fermi level to touch the intrinsic level at the Si/SiO$_2$ interface.

a) Sketch the charge buildup, the electrostatic potential, and the electric field inside the semiconductor vs. position.
b) Do equilibrium conditions prevail inside the semiconductor? Sketch the electron concentration vs. distance inside the semiconductor.