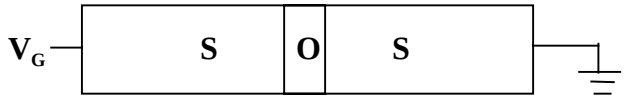
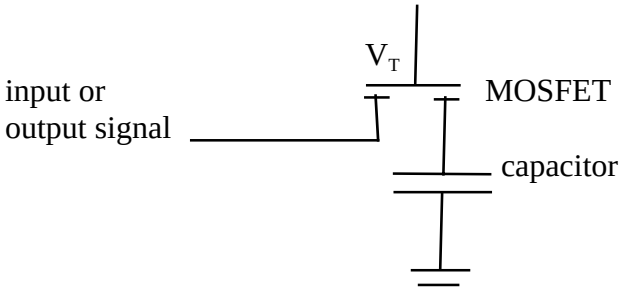
3.15 Electrical, Optical and Magnetic Materials and Devices
Prof. Caroline A. Ross
Fall 2003

Problem Set 4 MOS and photodevices Due: Tues Oct 21, 2003
Reference: Pierret chapers 9, 15, 16

1. In class we looked at a p-type semiconductor and examined what bias conditions lead to accumulation, depletion, and inversion in a MOS structure.
a) Go through the same exercise with an n-type material to show what voltage applied to the metal leads to accumulation, depletion, and inversion.
b) Now draw a MOSFET using an n-type material and explain what voltages are applied to the gate and drain to make it work like a transistor. Assume the source is grounded (zero voltage).
c) It is possible to build a structure consisting of semiconductor-oxide-semiconductor (SOS). This can be treated like a MOS structure except the semiconductor bands are pinned on both sides of the oxide. Assume that your SOS structure is ideal and the two semiconductor layers are identical and have n-type doping. Draw the band diagram for the structure under different V_G conditions (positive or negative) and explain whether you get accumulation, depletion, or inversion.



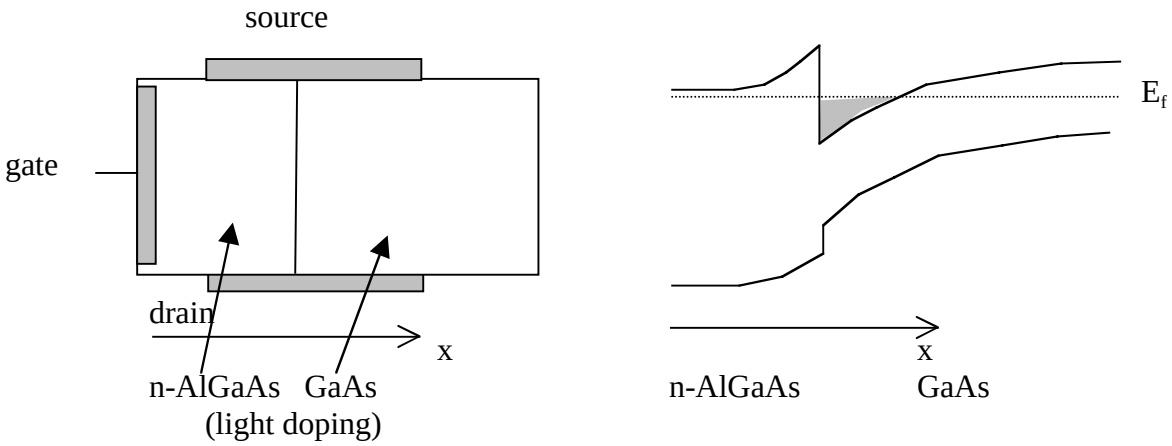
2. A dynamic random access memory (DRAM) stores one bit of data in a cell that consists of one capacitor and one MOSFET. The circuit of one cell is shown below.



When the MOSFET is turned on (by applying a voltage V_T), charge can flow between the input and the capacitor. A charged capacitor represents a '1' and an uncharged capacitor represents a '0'. To read the bit, we apply V_T and see whether charge flows out of the capacitor – if it does, the bit was a '1'. (The bit must then be rewritten.)
a) In the DRAM cell, estimate how long it takes to read or write a bit. Assume the capacitor has dimensions 10 x 10 μm, the thickness of the oxide is 50 nm and its relative permittivity is 4. It is charged up to 5V. The major resistance to current flow comes from the n-channel in the MOSFET, with length 1 μm, width 0.5 μm, thickness 0.5 μm, and 10^{16} carriers/cm^3.

b) Extremely fast FETs can be made using heterostructures as shown below. In the heterostructure, the high bandgap side is heavily doped while the low bandgap side is lightly doped. The heavily-doped side is connected to the gate. (x just represents depth into the device). What is the significance of the shaded region of the band structure? Note that this region connects

the source and drain together. What happens to the shaded region when a gate voltage is applied? Explain why this device can operate very quickly compared to a standard JFET or MOSFET.



3. This question concerns the solar panel which we examined in class.

a) Plot the I-V data which we measured on top of the manufacturer's curves from Handout 4.

b) How many times brighter would the light have to be compared to what we measured for the cell to be 'fully illuminated'? Is it reasonable to expect the panel to achieve full illumination at any time in the year?

c) How long would the cell have to operate in Boston in October to obtain 1kWh power (i.e. about 10c worth of electricity)?

d) What is the ideal resistance of the load for the cell to generate maximum power under full illumination? Is this consistent with typical loads presented by, for example, an electric light bulb or an electric motor?

e) The panel was made of 36 cells. Why were the 36 cells connected in series? What would the optimum resistive load be if they were connected in parallel?

f) Each cell passes about 60 mA under about 0.5 V forward bias in the dark. Previously we found that a typical pn junction allows about 1 mA to pass under about 0.5 V forward bias. What is the reason for this difference?

g) J_o for the cell in the dark is 2.5 10^{-12} A/cm^2. Given typical doping levels, what does this imply about the quality of the silicon needed for the cell, as compared to microelectronic-grade silicon?

4. Design a silicon *pin* photodiode of area 1 mm^2 with as fast a response time as possible when used in conjunction with a 50 Ω load resistor. Take ε_r = 11.8 and v_s, the electron saturation drift velocity, as 10^5 m/s. Address the following points:

- Determine the optimum thickness of each layer
- Describe an optimum doping arrangement
- Over what wavelength range would you expect the device to be most effective?
- Describe the expected frequency response
- Estimate the minimum detectable input light intensity

There is no one 'right' answer for this. To obtain credit, clearly explain your assumptions and reasoning.