Processing, Structure, Properties, and Reliability of Metals for Microsystems

Carl V. Thompson

Abstract-- **Research on the processing, structure, properties and reliability of metal films and metallic microdevice elements is reviewed. Recent research has demonstrated that inelastic deformation mechanisms of metallic films and microelements are a function of temperature, encapsulation, and dimension. Reduced dimension can lead to strengthening or softening, depending on the temperature and strain rate. These results will help in the analysis and prediction of the stress state of films and microelements as a function of their thermal history. Experimental characterization and modeling of stress evolution during film formation has also been undertaken. New microelectromechanical devices have been developed for in situ measurements of stress during processing, and experiments relating stress and structure evolution are underway for electrodeposition and reactive film formation as well as vapor deposition. Experiments relating current-induced stress evolution (electromigration) to the reliability of Cu based interconnects are also being carried out.**

Index Terms-- **interconnects, MEMS, stress, thin films**

I. Introduction

Our research program at MIT focuses on the relationships between processing, structure, properties and the reliability of polycrystalline metallic films used in microdevices and systems. This includes research on the evolution of the structure and mechanical properties of films during their formation and during post-formation processing, as well as research on the characterization and control of the mechanical properties and reliability of polycrystalline films and microelements used in microdevices and systems. SMA students constitute an integral part of our research team and interact extensively with students at MIT. Progress in our overall program will be briefly reviewed, with a focus on the contributions of SMA students and SMA-supported interactions with MIT students.

II. Mechanisms of Inelastic Deformation of Films and Microelements

We are studying three forms of film formation, physical vapor deposition, electrodeposition, and reactive film formation. In all three cases we are focusing on structure and stress evolution during film formation, and on the effects that each has on the other. Our goal is to develop quantitative and predictive models for stress and structure evolution, to provide the basis for engineering design of polycrystalline films and microelements with properties that are optimized for performance and reliability in a range of specific applications in microsystems.

As background for this work, we have studied inelastic deformation of continuous and patterned polycrystalline films of fcc metals. These materials are used for on-chip interconnections in integrated circuits and in an increasing variety of microelectromechanical devices and systems.

We use a number of techniques to characterize stresses during thermal cycling of films and microelements. One way in which we have characterized inelastic deformation in metal films on wafer substrates is through wafer curvature measurements made during thermal cycling [1-2]. Differential thermal expansion leads to the development of compressive biaxial strains in the films during heating, and biaxial tensilestrains during cooling. The resulting stress in the films causes a measurable curvature in wafer substrate. In addition to curvature measurements on film-coated Si wafers, we have also made micromachined single crystal Si membranes on which films have been deposited. The Si membranes are sufficiently thick and the metal films sufficiently thin that heating and cooling lead to the same stress states obtained during heating and cooling of full wafers. However, the membranes and films are sufficiently thin to allow observation of dislocation activity during in-situ heating and cooling in a high-energy transmission electron microscope [2-3]. We have also developed an analysis that allows characterization of the stress state in films patterned into lines using wafer curvature experiments [4].

From the experiments outlined above we have learned that there are two regimes of inelastic deformation in polycrystalline thin films. At relatively low temperatures, such as room temperature, inelastic deformation of films and microelements is dislocation- mediated. The flow stress in this regime depends on the dimensions of the microelements as well as on their thermal histories. Thinner films and narrower lines have high yield stresses. We have found that in at least some metals, the origin of this effect is related to dimension-dependent and thermal history dependent variations in dislocation densities, which are quite high, rather than dislocation pinning or drag associated with the microelement surfaces, as has been widely assumed in the past [5]. We have both direct microscopic evidence as well as evidence inferred from measured activation volumes for isothermal relaxation that the dislocation-mediated plasticity is inhibited by pinning sites whose spacing corresponds to those of forest dislocation spacings, rather than to the larger microelement and grain dimensions.

At higher temperatures, films and microelements can

This work was supported by the Singapore-MIT Alliance, the Semiconductor Research Corporation, MARCO, and the U.S. National Science Foundation.

C. V. Thompson is with the Massachusetts Institute of Technology, Cambridge, MA 02139 USA (telephone: 617-253-7652, e-mail: cthomp@mtl.mit.edu).

rapidly deform through diffusive-creep processes. In this regime the deformation rate increases and the flow stress decreases with increasing temperature. Also because the grain sizes of thin films and microelements generally scale with the spacial dimensions of films and microelements [6], diffusion distances decrease with decreasing dimension so that the deformation rate and flow stress *decrease* with decreasing film thickness and microelement dimension [1]. Because diffusive creep is more strongly temperature dependent than dislocation-mediated deformation, the temperature at which creep dominates decreases with decreasing film dimension. We therefore find that the basic inelastic deformation mechanism, and the dependence of mechanical properties on film and microelement dimension, depend on both temperature and dimension, as shown in figure 1. We have further demonstrated that encapsulation of films and microelements with materials that inhibit surface diffusion, and therefore diffusive creep, can shift the dominant deformation mechanism domains as schematically illustrated in figure 2.

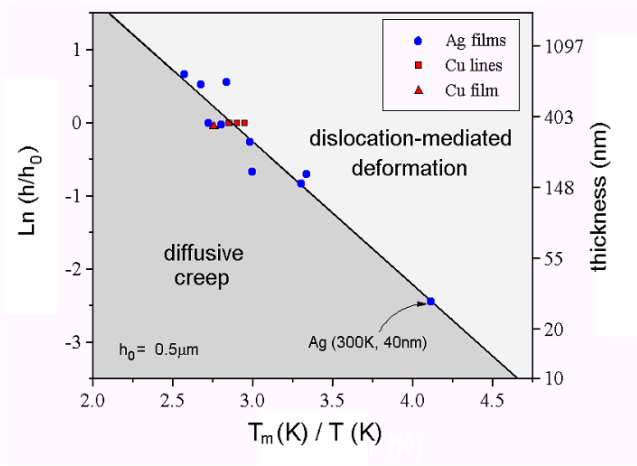

Figure 1. Deformation mechanism map for fcc metal films, based on measurements made while cooling unpassivated Ag and Cu films and Cu lines on Si substrates at 6C/min.

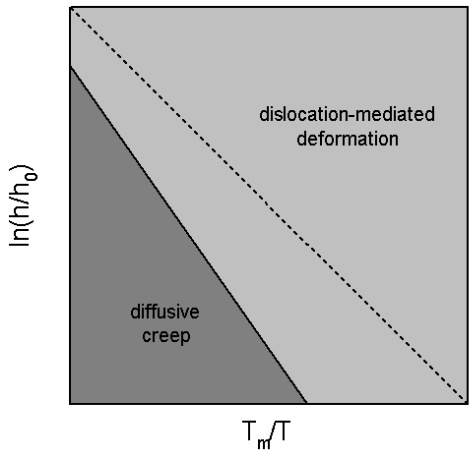

Figure 2. Schematic illustration of the effect of surface pasivation.

III. Stress Evolution During Film Formation

Polycrystalline films deposited using physical vapor deposition can be under tensile or compressive stresses of 1 MPa or more in the as-deposited state [7-8]. The origin of tensile stresses is thought to be related to the coalescence process [9]. Polycrystalline films form through nucleation of crystal islands, which subsequently grow into the vapor phase as well as in the plane of the substrate surface. When islands make contact, grain boundaries form through the elimination of some of the surface area of the two coalescing islands. This processes is highly energetically favored when the impinging islands are small, so that their surface to volume ratios are high. Boundary formation can occur most rapidly through straining of the islands to allow a boundary to "zip" up from the substrate surface. Quite high strain energies can be compensated for by the surface energy reduction, and it can be shown that the resulting tensile stresses are of the same magnitudes observed in experiments [10,11].

In the past year we have developed simulations of island nucleation, growth, impingement, and coalescence to form polycrystalline films [10]. We have also used finite element models to determine the coalescence stress as a function of the sizes of the coalescing islands, and as a function of their surface and grain boundary energies as well as of their mechanical properties. We have used film formation simulations with finite element stress calculations, and analytic models for diffusive creep as a stress relaxation mechanism, to reproduce experimental results obtained from in-situ measurements of film stress during film formation and growth [10,12]. We feel that our results allow quantitative explanation of the high tensile stresses observed in as-deposited refractory metals, as well as the transient tensile stresses that develops during coalescence of lower melting temperature fcc metals, but which is relaxed during continued growth or growth interruptions.

The origin of compressive stresses, especially in films formed through evaporative deposition, is less well understood. In sputter deposited films with large compressive stresses can result when deposition is carried out at low sputtering gas pressures. This effect is thought to be related to shot peening [7]. However, even in evaporatively deposited films, compressive stresses are observed prior to coalescence, and are often observed after coalescence in films in which the tensile coalescence stress is relaxed.

In order to develop a better understanding of the details of stress evolution, and the corresponding structural evolution that occurs during film formation, we have developed a number of microelectromechanical devices for in-situ and ex-situ characterization of stress during processing of polycrystalline films. These include electrostatic pull-in structures, 'poiezolevers', and buckled membrane devices.

IV. Microelectromechanical Devices for Characterization of Stress and Structure Evolution During Film Processing

Electrostatic pull-in structures consist of polycrystalline cantilever or doubly-supported beams that can be electrostaticaly pulled down to make contact with the

substrate (figure 3). As the micro-beam is pulled in to the substrate, there is a well-defined instability point at which the beam snaps down to the substrate. The voltage at which this occurs is a function of the geometric characteristics of the beam structure and of the stress and modulus of the beam. By measuring the pull-in voltage of beams of different lengths, the modulus and the stress of beams can be independently determined [14]. Once the beams themselves have been characterized, they can be used as substrates for deposited films. Devices have been developed which allow electrical detection of pull-in for in-situ thin film stress measurements made during deposition.

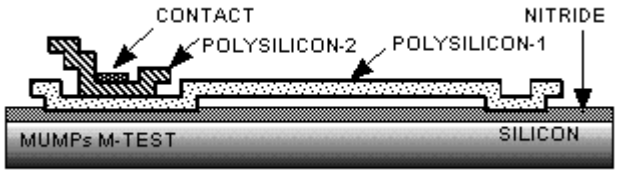

Figure 3. A doubly-supported beam that can be electrostatically pulled in to the snubstrate. By measuring the pull-in voltage for devices with different lengths (but otherwise identical geometries), the stress and modulus of the beam can be determined. The stress and modulus of films deposited on the beams can also be determined (after reference 14).

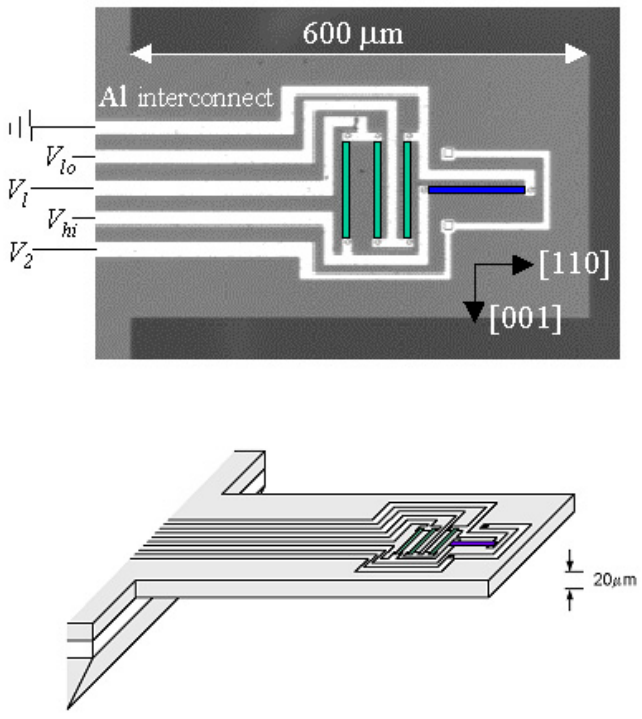

Figure 4. A microelectromechanical device for in-situ measurements of stress evolution during film deposition. A microcantilever is fabricated in a thinned (110) wafer bonded to a (100) Si wafer. Three resistors in a Wheatstone bridge are oriented to have zero piezoresistance and the fourth is oriented to have a large piezoresistance.

An alternative to pull-in devices is what we have called 'piezolevers' (see figure 4). These are devices made using bonded silicon-on-insulator wafers in which cantilevers are formed in the Si film and released through an oxide etch so that they are suspended over anisotropically etched holes in the underlying Si substrate. Before the release etch, four-resistor Wheatstone bridge structures are microfabricated in the cantilevers. The Si films are made using (110) wafers bonded to (100) wafers. The cantilevers therefore have (110) surface normals. The in-plane piezoresistivity for this orientation is highly anisotropic, so that three resistors of the Wheatstone bridge can be oriented so as to have essentially zero piezoresistivity, and the fourth can be oriented so as to have a high piezoresistivity. By monitoring the piezoresistivity of the fourth resistor during film deposition, the stress in the Si cantilever, and therefore the stress resulting from film growth, can be monitored with a high sensitivity. Figure 5 shows data acquired using one of these devices. This shows the development of a small compressive stress before coalescence, development of a tensile stress during coalescence, and development of a compressive stress again after calescence and during film thickening. High-sensitivity measurements of film stress are being made during film growth and during growth interrupts, and as a function of deposition temperature and deposition rate. This database will be used to further develop quantitative and predictive models for stress and structure evolution during processing of polycrystalline films.

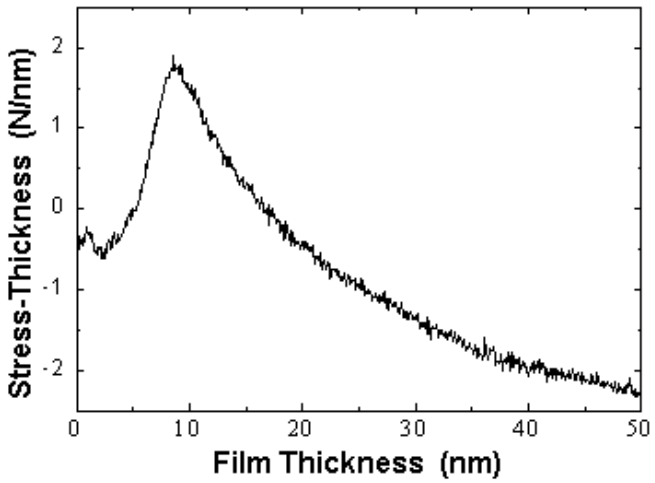

Figure 5. The stress-thickness product as a function of film thickness measured during deposition of Cu on a device of the type shown in figure 4.

A third very simple microelectromechical device has been developed for studies of stress evolution during chemical vapor deposition, and for studies of stress evolution during transmission electron microscopy. These consist of buckled membranes suspended over square holes produced by anisotropic etching of Si substrates (figure 6). These have been made by anisotropically etching bonded silicon-on-insulator wafers to create Si-SiO_2 membranes suspended over square holes in the Si substrates. Because the thermally grown SiO_2 is in a compressive stress state, membranes within specific thickness and area ranges will buckle in a single mode state. The detailed shape of the buckled membranes can be quickly and easily determined with sub-10nm z-axis resolution using automated optical profilometry based on optical interferometry. The buckle state can be characterized before and after film deposition, and given knowledge of the

geometric and mechanical properties of the membranes, the mechanical properties of the deposited films can be determined from measured differences in the buckled state. An advantage of this technique over beam-based techniques is that film deposition on both sides of the membrane does not detract from the measured property, but instead, amplifies it. This makes this technique useful for characterization of CVD processes, for which deposition on both sides of beams or membranes is difficult to avoid.

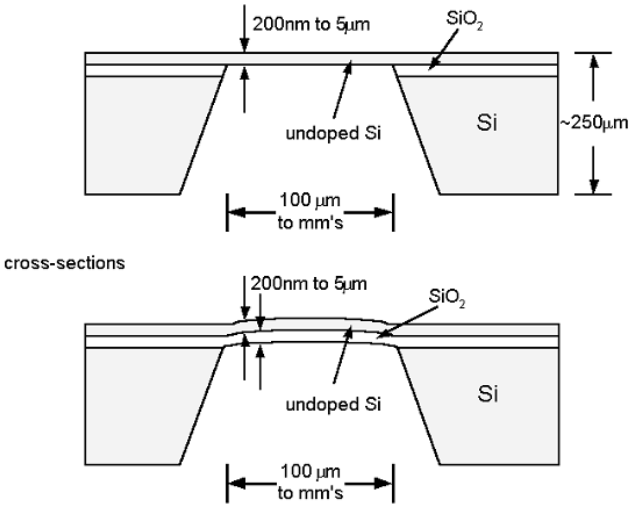

Figure 6. Micromachined buckled square membranes of single-crystal-Si/SiO_2 bilayers.

Membrane structures are also ideally suited for experiments carried out in transmission electron microscopes. We plan to carry out in-situ studies of film formation in collaboration with IMRE, using IMRE's TEM equipped for in-situ deposition. These studies will allow direct observations of coalescence processes, and may allow observation of dislocation-mediate relaxation processes during film formation.

V. Film Formation by Non-Vapor-Phase Processes

As our understanding of stress and structure evolution during vapor phase deposition of films improves, we will increasingly turn our attention to stress and structure evolution during film formation via other techniques. We specifically are equipping ourselves for studies of electrodeposition of metallic films, and solid state reactive formation of metal silicide films. In these studies we will use and build on the modeling and experimental tools developed for studies of vapor-deposited films.

Electrodeposition has become a critical process in fabrication of microelectronic circuits. It is used to deposit polycrystalline Cu films that are patterned into lines that interconnect devices in circuits. Electrodeposition is also widely used in the manufacture of micro-magnetic devices such as magnetic read-write heads and has potential use in fabrication of microelectromechanical devices, especially those fabricated using the LIGA process. During electrodeposition of polycrystalline films, the grain structure develops through nucleation, growth, impingement and coalescence processes similar to those that occur during vapor deposition. However, electrodeposition involves film growth from an aqueous solution with chemical additives that play complex roles in controlling nucleation and in controlling growth rates on both global and highly localized length scales [15]. The latter is often required to suppress growth instabilities associated with field intensification and accelerated growth at surface perturbations. Grain structure evolution is known to be strongly affected by additive concentrations as well as the deposition current and rate [16-17]. However, relatively little is known about stress evolution during electrodeposition, and its relationship to structure evolution, even though stress evolution has been linked to important post-deposition 'self-annealing processes in electrodeposited Cu films [18]. We have developed an electrodeposition system in which stress evolution during film formation can be monitored.

Reactive film formation is used to form both oxides and metal silicides, which play critical roles in the performance of microelectronic devices and systems. Metal silicides are used as low resistance diffusion barriers at metal-silicon contacts and as components of low resistance gates in metal-oxide-semiconductor field effect transistors. These silicide films are usually formed through deposition of pure metal films on Si, followed by heating to form silicides through reactions. Silicides formed in this way are usually polycrystalline. In most cases of reactive film formation, the structure of the resulting polycrystalline films forms through nucleation, growth, impingement, and coalescence of islands at the original interface between the reacting materials [19-21]. It has been demonstrated that reactive film formation leads to stress evolution that is readily measured [22], and it has also been suggested that small changes in the stress state of the Si surface can strongly affect the kinetics of reactive film formation [23].

The change in the metal molar volume that accompanies silicide formation during solid-state reactive film formation is large, and might be expected to lead to an unsustainably high stress in the newly formed films. That such high stresses are not observed suggests that mechanical deformation leading to stress relief occurs during reactive film formation. This deformation plays an unknown, but probably very important role in determining the final film structure and properties, and in governing the kinetics of film formation, which would, in turn, affect the temperature required for formation of different phases. SMA student Liew Kwan Pong has initiated studies of stress evolution during reactive film formation leading to formation of nickel silicide films. The current status of her studies will be reviewed in a separate abstract and presentation in this symposium.

Through development of unique experimental and modeling capabilities, we hope to develop quantitative and predictive modeling capabilities that can be used to engineer the structure and properties of polycrystalline films and microelements produced using a variety of techniques, and optimized for a variety of applications.

VI. Interconnect Reliability

One of the most important applications of polycrystalline metallic films is in formation of the thin-film wires that interconnect devices in integrated circuits (IC). As devices shrink and become more numerous, interconnect widths shrink, but the number of interconnect segments and total interconnect length increases. Interconnect widths are shrinking at an exponential rate, and the total length of interconnect segments is increasing at an exponential rate [24]. Both trends independently require reliability improvements at an exponential rate.

At the same time that reliability requirements are rapidly becoming more stringent, the materials and processes used for forming IC interconnects have entered a phase of rapid evolution. As devices are shrink, there switching speeds become faster. However, as the number of devices in an IC increases the number of wiring segments increases, and the total length of wiring increases, and already exceeds 1 km. Resistance-Capacitance (RC) delays in signal transmission in interconnects now limits the overall performance of integrated circuits [24]. The IC industry is therefore replacing Al-based interconnects with lower-resistance Cu interconnects as rapidly as possible, and is also beginning to introduce low-dielectric-constant alternatives to SiO_2, which is now used for electrical insulation and mechanical support for multilevel interconnect structures. Also because Cu generally diffuses through dielectric materials more readily than Al, very thin (10nm or less) refractory-metal films are used to line the trenches into which Cu is electrodeposited, to serve as diffusion barriers. Both the Cu films and the liners are polycrystalline and their grain structures and mechanical stress states affect their reliability.

The major reliability concern for metallic interconnects is voiding or extrusions due to processing-related tensile or compressive stresses, respectively, and voiding or extrusions caused by stresses that develop due to current-induced mass redistribution, known as electromigration. Our group at MIT has studied stress-induced and electromigration-induced voiding of interconnects for many years. Through the SMA program we have been able to now initiate studies of the reliability of Cu-based interconnects. SMA student Gan Chee Lip, and SMA Fellows Choi and Pey collaborated in the development of a variety of test structures to be used in characterization of stress-induced and electromigration-induced voiding of Cu interconnects. These structures include conventional test structures, as well as interconnect 'tree' structures needed to develop models and methodologies for accurate circuit and layout-specific reliability assessments [25-26]. These test structures have been fabricated at IME in Singapore, and are now also being fabricated at Sematach in the US. MIT students are characterizing these devices in collaboration with Gan Chee Lip, and in collaboration with researchers at Intel and Sandia National Laboratories in the US.

Gan Chee Lip will summarize some of his key findings in a separate abstract and presentation at this symposium. Gan and his MIT colleagues have shown that Cu-based interconnects have a wider variety of failure mechanisms than Al-based interconnects, and that the behavior of Cu-based trees is fundamentally different from Al-based trees. This requires the development of new reliability models and assessment methodologies, especially for circuit-level reliability assessments. Because, electromigration is current-induced mechanical creep, its rate depend on interface and grain boundary structures. The rate at which electromigration leads to failure also depends on the mechanical properties of the surrounding liner and dielectric materials, and on their initial stress states. As mentioned earlier, the latter can vary over wide ranges, depending on the method and conditions for deposition. A detailed, quantitative, and predictive understanding of the reliability of metallic interconnects will require a detailed understanding of the relationships among processing, structure and stress in all components of the metallization system, including not only the high conductivity metal (e.g., Cu or Cu alloys), but also refractory metal liners and low-k dielectrics.

VII. Summary

In summary, an interconnected research program on the processing of polycrystalline metallic films for applications in microdevices and microsystems is being supported, in part, through the SMA program. New devices and techniques for characterizing stress and structure evolution during processing of thin films have been developed, and are being using by both MIT and SMA students to characterize property evolution during formation of films via vapor deposition, electrodeposition, and solid-state reactive film formation. The understanding developed through these studies is being applied to ongoing studies by MIT and SMA students on the rapidly evolving technology of metallic interconnects for high performance integrated circuits. Research on characterization and modeling of stress and structure evolution during film processing is producing the tools needed to design and process materials with properties that have been optimized for a wide variety of applications in micro- and nano-systems.

References

[1] M.J. Kobrinsky and C.V. Thompson, Appl. Phys. Letts. **73**, p. 2429 (1998).

[2] M.J. Kobrinsky and C.V. Thompson, Acta Materialia **48**, p. 625 (2000).

[3] M.J. Kobrinsky, G. Dehm, C. V. Thompson, and E. Arzt, Acta Mater. **49**, pp. 3597-3607 (2001).

[4] M.J. Kobrinsky, C.V. Thompson, and M. Gross, J. Appl. Phys **89**, pp. 91-98 (2001).

[5] W. D. Nix, Met. Trans. A **20A**, p. 2217 (1989).

[6] C.V. Thompson, Solid State Physics **55**, pp. 269-314 (2000).

[7] M. Ohring, "The Materials Science of Thin Films", Academic Press, N.Y., N.Y., (1992).

[8] R. Abermann, Vacuum **41**, p. 1279 (1990).

[9] W. D. Nix and B. M. Clemens, J. Mater. Res. **14**, p. 3467 (1999).

[10] S.C. Seel, C.V. Thompson, S.J. Hearne and J.A. Floro, J. Appl. Phys **88**, pp. 7079-7086 (2000).

[11] L.B. Freund and E. Chason, J. Appl. Phys. **89**, p. 4866 (2001).

[12] J. A. Floro, S. J. Hearne, J. A. Hunter, and P. Kotula, E. Chason, S. C. Seel and C. V. Thompson, J. Appl. Phys. **89**, p. 4886 (2001).

[13] A. L. Shull and F. Spaepen, J. Appl. Phys. **80**, p. 6243 (1996).

[14] P. Osterberg and S. Senturia, *IEEE Journal of Microelectromechanical Systems* **6**, p. 107 (1997).

[15] J.O'M. Bockris and A.K.N. Reddy, "Modern Electrochemistry Vol. 2", Plenum Publishing, N.Y.,N.Y. (1970).
[16] R. Winand, Hydrometallurgy **29**, p. 567 (1992).
[17] J.W. Dini, Matreials and Manufacturing Processes **12**, p. 437 (1997).
[18] J.M.E. Harper, C. Cabral, Jr., P.C. Andricacos, L. Gignac, I.C. Noyan, K.P. Rodbell, and C.K. Hu, J.Appl. Phys. **86**, p. 2516 (1999).
[19] K.R. Coffey, L.A. Clevenger, K Barmak, D.A. Rudman, and C.V. Thompson, Appl. Phys. Letts. **55**, p. 852 (1989).
[20] E. Ma, C.V. Thompson and L.A. Clevenger, J. of Appl. Phys. **69**, p. 2211 (1991).
[21] C. Michaelsen, K. Barmak, and T. P. Weihs, J. Phys. D, **30**, 1 (1997).
[22] V. Svilan, J.M.E. Harper, C. Cabral, L.A. Clevenger, MRS Symp. Proc. **356**, 167 (1995).
[23] S.L. Cheng, H.Y. Huang, Y.C. Peng, L.J. Chen, B.Y. Tsui, C.J. Tsai, S.S. Guo, Appl. Phys. Letts. **74**, p. 1406 (1999).
[24] "International Technology Roadmap for Semiconductors," Semiconductor Industry Association, 2000 version: http://public.itrs.net/Files/2000UpdateFinal/2kUdFinal.cfm
[25] S.P. Riege and C.V. Thompson, IEEE Transactions on Electron Devices **45**, p. 2254 (1998).
[26] J.J. Clement, S.P. Riege, R. Cvijetic, and C.V. Thompson, IEEE Trans. on CAD of Integrated Circuits and Systems, **18**, p. 576 (1999).
[27] S.P. Hau-Riege and C.V. Thompson, J. Appl. Phys. **89**, pp. 601-609 (2001).