An Integrated Circuit Biosensor for Hyperthermia Cancer Treatment

by

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B.S., Massachusetts Institute of Technology (1994)

Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

Hyperthermia, in which the temperature of tumor cells is selectively elevated, is an important cancer treatment. An integrated circuit biosensor for use during these treatments is described. The first generation of this design was completed by Dr. Kenneth Szajda.

Each of the "smart sensor" chips contains a high resolution temperature sensor, preamplification circuitry, and a sigma-delta A/D converter. The temperature sensor is designed to have a dual use: 1) as a temperature monitor and 2) for use in perfusion (volumetric blood flow) measurement using thermal methods. Both temperature and perfusion are major determinants of treatment success as well as key variables needed for calculating temperature values at non-measured points in the tumor.

Key system requirements are high resolution, low area, and low power. This thesis focuses on reducing the area and power of the 1^{st} generation design, while maintaining the resolution of temperature measurements. A layout strategy to minimize area for a fixed width layout is introduced. Low power operational amplifier design is discussed. A common mode feedback method using no extra power dissipation is incorporated. On-chip biasing, complementing this common mode feedback structure, is used to provide a common mode voltage insensitive to component values or absolute currents. Control over the common mode voltage is critical for maintaining high output swing with a low voltage supply (3V). Changes in the sigma-delta A/D converter architecture also contribute to substantial power and area savings. The size of a single chip was reduced by 50% to 580 X 3930 microns. Static power consumption was reduced by 80% to .94 mW.

Other modifications to the system are discussed, including control circuitry, output drivers, electrostatic discharge protection, and off-chip signal processing.

Thesis Supervisor: Charles G. Sodini
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Acknowledgments

I would like to acknowledge my parents as the "Wind Beneath my Wings." Both my parents have made many sacrifices for my benefit, and their dedication is appreciated.

Every projects needs an advisor, but I have had the distinct pleasure of having several.

Professor Charlie Sodini has been my advisor in Electrical Engineering and has guided me through the design aspect of this system with excellent courses and individual meetings.

Dr. H. Frederick Bowman, a faculty member in HST, has contributed insight about the most important aspect of this project: it's use in hyperthermia treatment. Because of Dr. Bowman, my Electrical Engineering thesis experience was broadened to include a concern for clinical applications. In addition, I rely on his experience and knowledge in perfusion sensing systems.

Dr. Kenneth S. Szajda was not only responsible for the first generation of this design, but has also taken a very active role in advising me during this project. He has contributed throughout this project in uncountable ways, from answering my endless questions to contributing ideas for system improvements.

A special thanks you is extended to:

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Chapter 1

Introduction

Health care was voted as the area in which technology would most likely affect the average person in the next ten years, according to an IEEE poll taken in September of 1993.[1] With a 42 billion dollar medical technology industry and with worldwide use of medical devices growing at a rate of ten percent per year, the potential of incorporating new technology into medicine has never been greater.[2] Yet, with medical care comprising fourteen percent of the gross domestic product in the United States, and health care reform a top area of national concern, every effort should be made to deliver this technology at a reasonable cost.[3]

This thesis involves coupling modern biotechnology and advanced electronics. Specifically, this thesis implements circuit design improvements to a low noise, high resolution, biomedical integrated circuit temperature sensor that was first proposed and developed by Szajda as part of his "active needle" system.[4] Multiple (10-16) sensors fit inside a 22 gauge needle, allowing for use in medical applications. An advantage of the integrated circuit implementation is that chips can be mass produced at a low cost.

This sensor is being developed specifically for use in cancer patients during hy-

perthermia treatment. For thermometry, it will be used to monitor temperature distributions both in and immediately outside tumors. This circuit is also a step toward the development of a blood perfusion sensor. Although measurement of perfusion has many important applications, the immediate purpose of combined perfusion/temperature sensors will, again, be to provide multi-parameter monitoring during hyperthermia treatments.

The "active needle" potential is not limited to temperature and perfusion sensing. The concept and architecture of the system can be used for any number of sensors: such as oxygen, glucose, and radiation, etc. Therefore, a whole tissue characterization system is possible on a single needle.

1.1 Hyperthermia

The object of local hyperthermia is to selectively elevate tumor tissue to a therapeutic temperature level around 43 °C. At high temperatures, this heating can damage tumor cells. At more moderate temperatures, heating can enhance tumor perfusion, increasing the effectiveness of both radiation therapy and chemotherapy by increasing oxygen or drug delivery to the tumor. [5]

The first role of these circuits is to provide temperature feedback to the clinician while administering hyperthermia therapy. The quality of the hyperthermia treatment lies in the ability to heat tumor cells to therapeutic levels, while leaving normal tissue minimally heated, and thus undamaged. Temperature measurements are important in planning and administering hyperthermia treatments because they provide feedback to the clinician about the thermal dose applied to tumor cells. Small sized probes that allow dense thermometry are clearly required for monitoring treatments and evaluating heating equipment. [6]

The ultimate goal of this project is to combine the temperature sensor circuitry

developed in this thesis with an integral heat source in order to measure perfusion, or volumetric blood flow. Blood flow is a significant determinant of tissue temperature during hyperthermia. Blood flow varies widely depending on tumor type and size and is heterogeneous even within a given tumor. [7] Clinical data from patients shows that perfusion can vary much more than 5% from second-to-second with no external influence. Larger changes, such as a 60% drop, can result from a simple action such as an arm extension.[8] Perfusion is significantly modified by drugs and heat.

Perfusion values and their variations induced by hyperthermia are an important action of the treatment. Very low areas of perfusion, often in the center of a tumor, will be more susceptible to damage from heat treatment. Increases in perfusion induced by temperature elevation will increase chemical and oxygen delivery, enhancing the benefit of chemotherapy and radiation. Knowledge of perfusion levels help a physician plan and evaluate hyperthermia treatment.

Since safety concerns and placement constraints allow measurements only at a limited number of tumor sites, probe data is also used in thermal models that predict the temperature throughout tumor. This can provide treatment information about the whole volume of the tumor, not just the measured sites. Both perfusion and temperature are important parameters in this modeling. Dense and accurate temperature and perfusion measurements will make the thermal field predictions and treatment control more accurate.

1.2 Perfusion Measurement Methods

There are several possible methods of perfusion measurement. Magnetic resonance imaging (MRI) can image blood movement either by tracking tagged blood or by monitoring phase shifts in a varying magnetic field. [9] MRI is very complex and re-

quires expensive equipment. To date, this method only provides qualitative indicators of perfusion, but it may hold future promise. [10, 11]

PET, Positron Emission Tomography, tracks tracers labeled with positron-emitting isotopes. PET has extremely high sensitivity. It can measure as low as picomolar concentrations of the tracer. Resolution of 2 to 3 mm has been reached, but this is dependent on the stillness of the patient. In addition, oxygen utilization, pH and drug uptake may be imaged as well as blood flow. [12] Because these trace compounds have a half-life on the order of one half hour, an expensive on-site cyclotron is necessary to produce these isotopes.[9]

Doppler Flowometry is based on applying a wave and measuring its reflection. If the wave is reflected off a moving object, the velocity of the object can be measured due to the Doppler effect. [9, 13] Doppler Flowometry in animal studies has been validated against radioactive microspheres in normal tissue. [12] A disadvantage of Doppler Flowometry is that it is unlikely that a calibration standard can be determined. Differences between tissues, such as hematocrit, vascular geometry and tissue optical properties make it impossible to generalize a calibration scheme that could be used in different tissues.

Other imaging techniques rely on injecting a tracer into the blood and imaging the movement of this injection. The image may be scanned by a variety of methods, including Dynamic X-Ray Computed Tomography or MRI imaging. These techniques, along with PET, suffer from the fact that a tracer must be injected. Each injection of tracer will provide only a one shot measurement of perfusion. [9]

Radioactive microspheres require a biopsy of tissue and is therefore not acceptable for clinical use. It is, however, a popular verification technique. If a bolus of tracer is well mixed in the afferent blood supplying an organ, then it will be distributed to different parts of the organ in the same proportion as the blood transporting it. This is referred to as the indicator fractionation principle. Microspheres are chosen to be a

size (10-15 μm) that will be trapped in the capillaries. The concentration of trapped spheres is usually measured by taking biopsies of the tissues and measuring their radioactivity. With this information about relative activity throughout the tissue, along with a measurement of total activity in a reference sample of blood in the circulation, the perfusion at each location can be extracted. [12]

1.3 Perfusion Measurement by Thermal Methods

The sensor developed in this project will use thermal methods, similar to those developed in Dr. Bowman's laboratory for the Thermal Diffusion Probe (TDP), to quantify perfusion. [14, 15] The Thermal Diffusion Probe transducer is an electrically resistive thermistor bead that can be mounted at the tip of a needle or catheter probe.[1] The thermistor is used to sense the temperature of the tissue and is then heated by dissipating enough electrical energy in the bead to maintain fixed temperature step. In the presence of blood flow, more steady-state electrical power is required to maintain the temperature step. The volume average temperature increment of the bead, in the presence of perfusion is [14]:[2]

$$\Delta T = \frac{P_{ss}}{4\pi a k_b}\left[\frac{k_b}{k_m}\left(\frac{1}{\sqrt{\frac{\omega c_{bl} a^2}{k_m}} + 1}\right) + .2\right] \tag{1.1}$$

It is important to understand the relationship between the resolution of the temperature measurements and the accuracy of the extracted perfusion values. A sensitivity analysis on the above equationresults in the following relationship.[4]

[1] This project would incorporate a similar thermal system using integrated circuits.

[2] P_{ss} is the steady state power required to maintain the temperature increment (Watts), a is the sphere radius (cm), k_b is the thermal conductivity of the sphere $\frac{watt}{cmC}$, and k_m is the thermal conductivity of the medium $\frac{watt}{cmC}$, ω is the perfusion $\frac{ml}{100g-min}$ and c_{bl} is the blood heat capacity $\frac{watt-sec}{gmC}$.

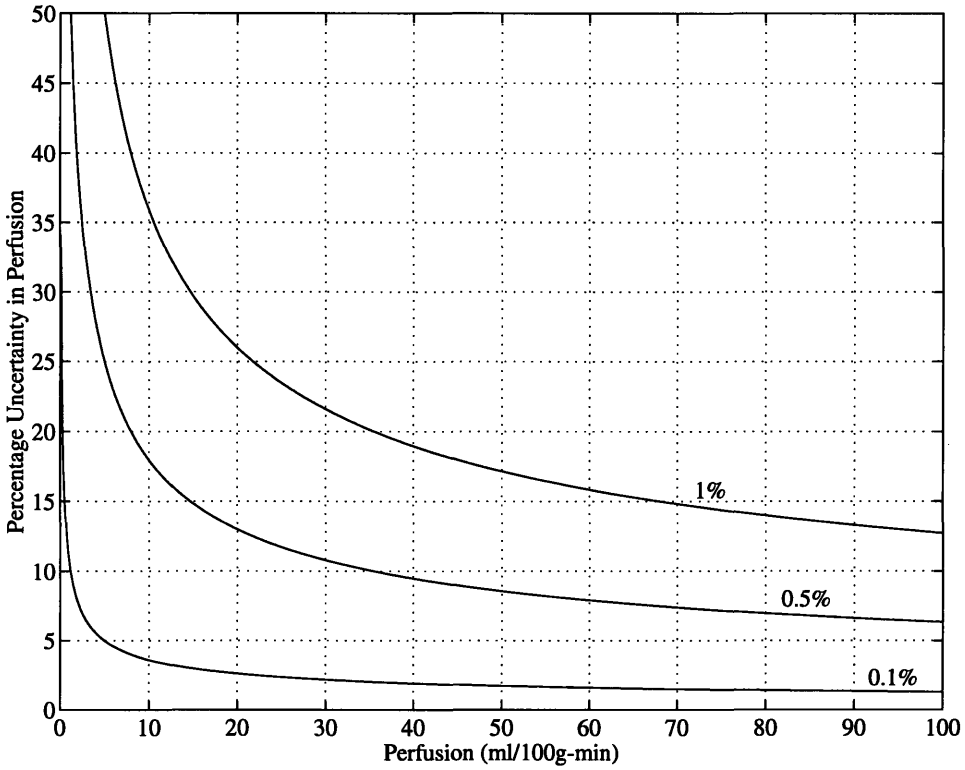

Figure 1-1: Relationship Between percentage uncertainty in temperature and percentage uncertainty in perfusion as a function of perfusion [1]

$$\frac{\partial\omega}{\omega} = 2[1 + \frac{1}{\sqrt{\frac{\omega c_{bl} a^2}{k_m}}}]\frac{\partial\Delta T}{\Delta T} \tag{1.2}$$

Figure 1-1 shows the percent uncertainty in extracted perfusion plotted as a function of perfusion. This is done at various uncertainty values of the measured temperature step. Large uncertainties in perfusion can result from small inaccuracies in the measured temperature step. For example, for blood perfusion on the order of 5ml/100g-min, which is a typical value for resting muscle tissue, uncertainty in temperature resolution must be less that 0.1% to measure perfusion to within 5% of its true value. Typical temperature steps used for measurement are 5 degrees Celsius, so this would correspond to a temperature resolution of 5 millidegrees Celsius. The

design goal of this project is a temperature resolution of 1 millidegree Celsius to be comparable to the best discrete systems.

1.4 Thesis Objectives

Szajda completed his Ph.D. project that included the design and fabrication of the temperature measurement system. This system includes a diode temperature sensor, a preamplifier, a fourth order sigma-delta A/D converter and the necessary control circuitry. [4]

The designed use of these temperature sensors is the measurement of perfusion. AS explained, perfusion will be quantified by measuring the power needed to maintain a fixed temperature increment at the sensor site. Therefore, the goal of this thesis is to optimize the temperature sensing system for this purpose.

The thesis objectives will focus the following important factors contributing to the accuracy of perfusion measurements:

1. Temperature resolution- The quantification of perfusion will rely on controlling a temperature step at the measurement site. Accuracy of the perfusion measurement is sensitive to the measurement of this temperature step. The design goal of this project is a temperature resolution of 1 m°C.

2. Number of temperature sensors- Obviously, the smaller the chip size, the greater spatial density of temperature sensor sites. In addition, with a smaller size, the chip will better model a point source, increasing the accuracy of the models used in the measurement. With smaller geometry, power deposition will spread more evenly, increasing the likelihood of uniform temperature across the chip. An isothermal heat source is ideal for perfusion measurement. Temperature sensors neighboring the perfusion sensor are used to monitor changes in baseline temperature throughout the measurement, so closely spaced sensors are very useful to monitor the thermal

gradients in the baseline temperature to predict the baseline temperature at the point of perfusion measurement.

3. Power dissipation- The power dissipated in the circuit results in a thermal artifact that changes with time. Its value, and in particular, the absolute variations in this value, must be kept to a minimum to maintain temperature resolution and simplify perfusion measurements. Steady state errors can be treated as on offset for temperature sensing. If the total power and temperature is measured both before and after an applied temperature step, an accurate perfusion calculation can be made. This also assumes that the artifact does not change during the measurement process. For any reduction in chip size, power dissipation must be reduced correspondingly to get the same thermal artifact.

In line with the objective for sensing perfusion, this thesis focuses on minimizing the area and power consumption of Szajda's system, while maintaining the temperature resolution.

1.5 Thesis Outline

Chapter 2 is a description of the overall "active needle" temperature sensing system, with results from prior experiments.

Chapters 3-5 cover design issues affecting the sensor goals. Chapter 3, Analog-to-Digital Conversion, and Chapter 4, the Operational Amplifier, covers methods of reducing power and area, while maintaining temperature resolution. Layout techniques used to minimize area are discussed in Chapter 5.

General improvements were made to improve the overall functionality of the system. Changes made to the control circuitry to simplify the system and ease fabrication of the needle are discussed in Chapter 6. Progress made on a decimation system, which will allow real-time measurement results, is summarized in Chapter 7.

Finally, Chapter 8 summarizes the accomplishments of this thesis, reports the current status of this work, and lays a plan for the next steps in this project.

Chapter 2

System Overview

This section describes the overall system, with results from Szajda's thesis.[4] Areas that are significant to thesis goals will be examined in detail in later chapters.

2.1 Overall System

Szajda designed and fabricated the first generation of the temperature measurement system and has been an active advisor during this project. The heart of the system fits on a small chip (8300 x 620 microns) (Figure 2-1). Each sensor chip contains a diode temperature sensor, a preamplifier, a sigma-delta A/D converter, as well as the control circuitry necessary to run the system. [4] The on-chip A/D conversion produces a noise-resistant, digital signal that can be processed off-chip. Future developments of the system include the addition of a heat source and power sensing circuitry necessary to facilitate perfusion measurements. Use of an integrated circuits allow a small chip and needle size, increases sensor density and patient comfort. The system also allows the flexibility of combining several different types of sensors in one needle.

Szajda's sensors have been tested on a needle, with a resulting temperature reso-

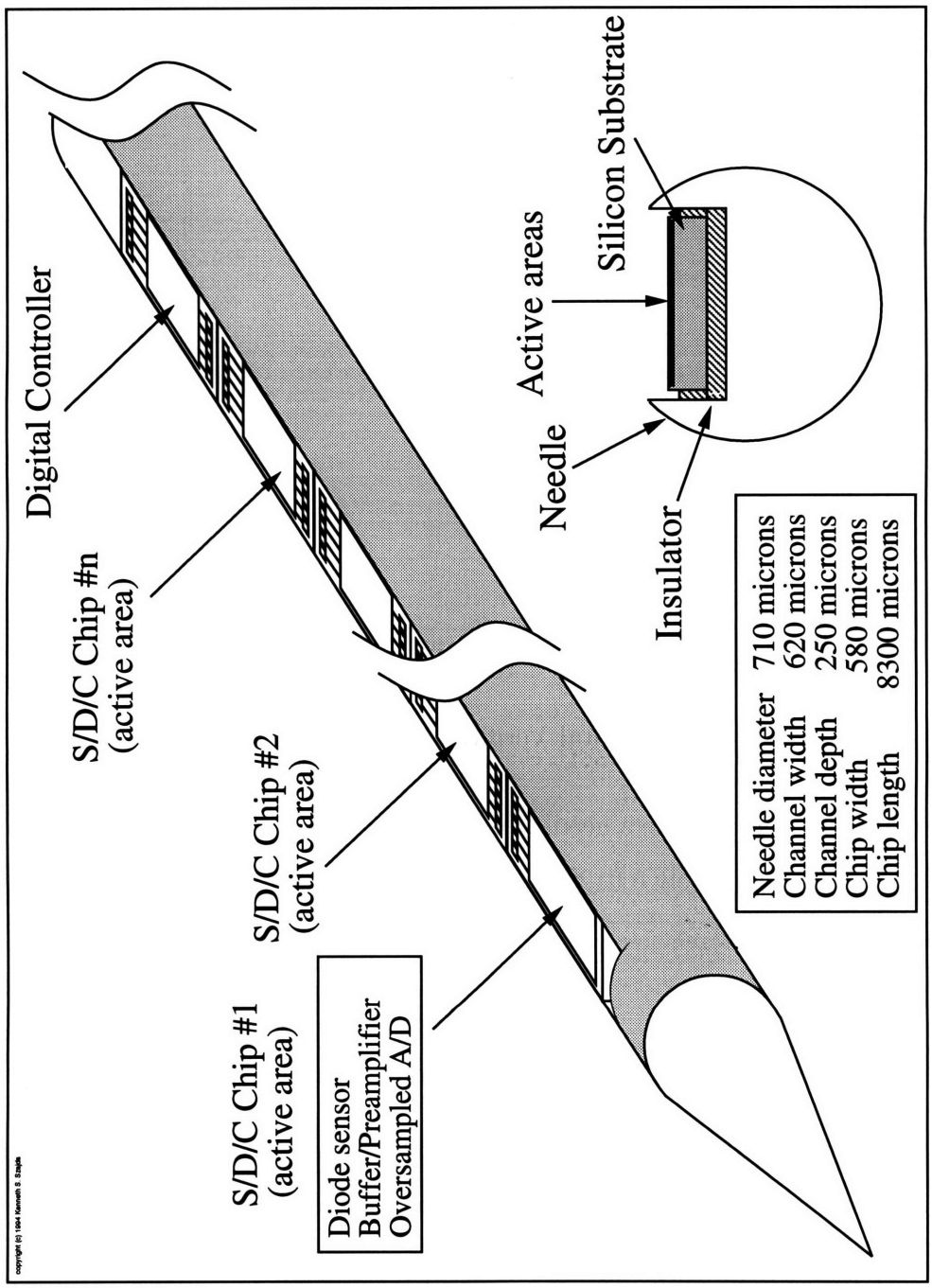

Figure 2-1: Active Needle Temperature Sensing System Developed by Dr. Szajda [1]

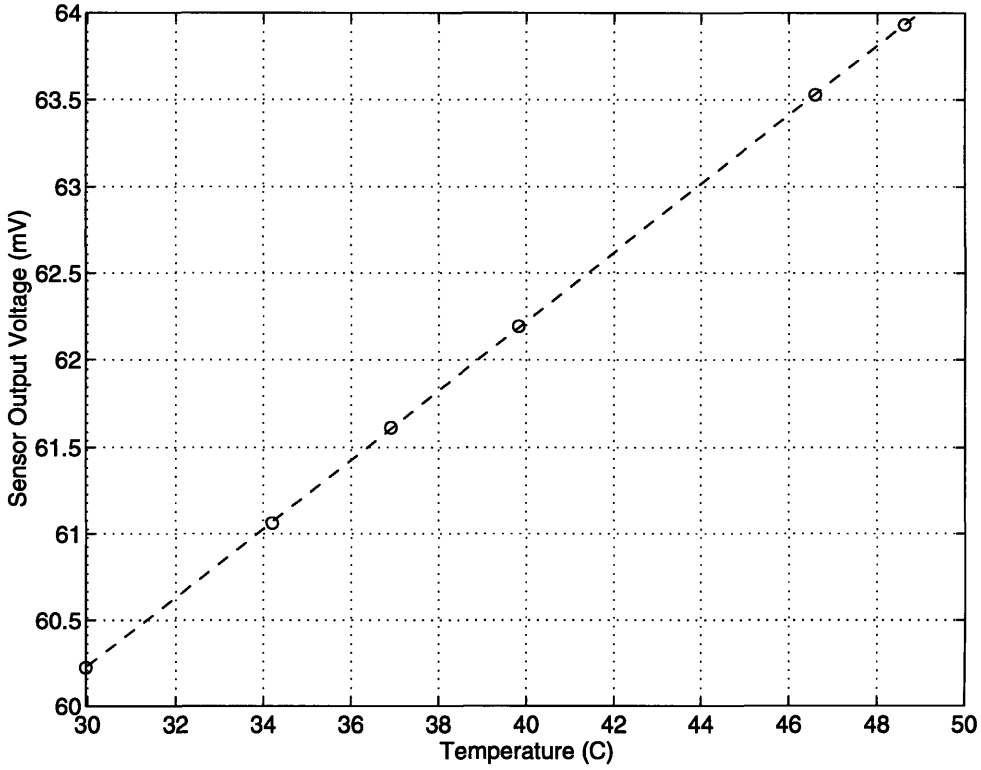

Figure 2-2: Experimental Verification of Temperature Sensors [1]

lution of at least 4m°C inside a needle and 3m° C in a testing apparatus.[1] Linearity of the system is approximately 0.012%. The extracted sensor output verses temperature is shown in Figure 2-2.

2.2 Temperature Sensor

The temperature sensor in this system was developed by Szajda (Figure 2-3). Szajda's thesis covers the development, implementation, and analysis of this sensor is much greater detail. [4]

[1]The measured resolution is largely limited by the capabilities of the test apparatus; the sensor may be able to resolve even smaller temperature changes. An improved testing setup is currently being designed so that the actual sensor resolution limit can be determined.

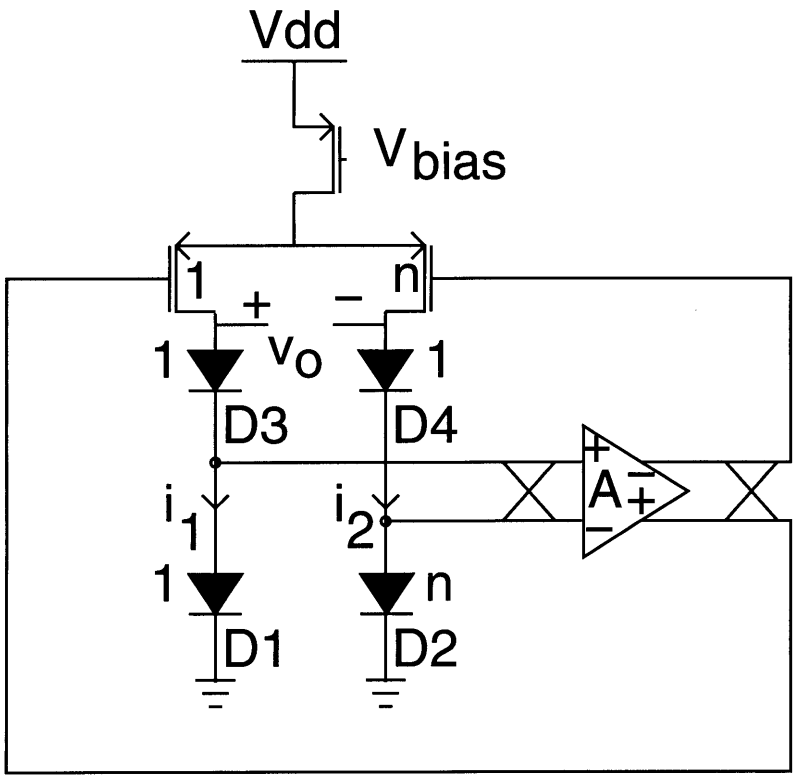

Figure 2-3: Temperature Sensor[1]

The operational amplifier, with the feedback loop, maintains a zero differential voltage at its inputs. This establishes a current ratio between the two legs of n. The output voltage is generated by running these two currents through identical diodes, D3 and D4. Do to these ratioed currents, a voltage difference is established at the output. This output is linearly related to temperature. [4][2]

$$v_o = \frac{kT}{q} ln(n) \tag{2.1}$$

[2] k is Boltzman's constant, T is the absolute temperature (K), and q is magnitude of charge on an electron

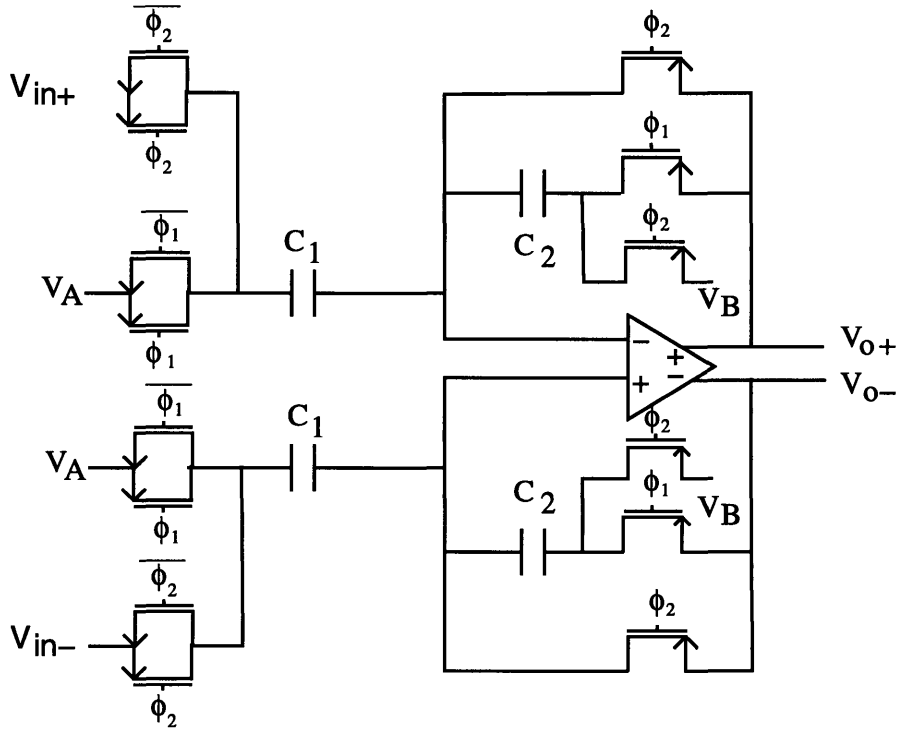

Figure 2-4: Preamplification Stage

2.3 Preamplification

With a current ratio (n) of 10, the output voltage of the sensor has a resolution of 198 nV per m°C. The signal is amplified to increase resistance to noise and ease the requirements of A/D conversion.

The signal processing is done with switch capacitor techniques.[16] Since the frequencies of interest are below 1 Hz, the clocks for the circuits, even running at very conservative speeds of tens of kHz, are many times faster than the signal. The system runs with non-overlapping clocks ϕ_1 and ϕ_2.

The output of the sensor is first amplified through a switched capacitor amplifier (Figure 2-4). Inputs V_A and V_B are used for correlated double sampling to suppress low-frequency noise. When ϕ_1 is high, a differential voltage is read from the inputs

onto the capacitors C_1. When ϕ_2 is high, the differential output voltage is an amplification of the differential input: [4][3]

$$V_{o+} - V_{o-} = \frac{C_1}{C_2}(V_{in+} - V_{in-}) \tag{2.2}$$

2.4 Further Signal Processing

The temperature range of interest in hyperthermia is 30-50 °C, which corresponds to about 300-323 Kelvin. Since the sensing methodology is referenced to absolute 0, the measurement range is 0 to 323 Kelvin. Therefore, one part in 323,000, or 18.3 bits is needed to resolve $1m$°C.[4] Signal frequencies of interest are 0-1 Hz.

A sigma-delta A/D converter is used to convert the analog signal into a digital bit stream. As will be explained in later chapters, this results in a one-bit digital representation of the signal that will be transported off chip. The oversampling ratio of the signal is very high (abot 30,000), with quantization noise shifted to higher frequencies as a result of the modulator architecture. An advantage of having the conversion on chip is that the output signal is digital and free from the corruption and interference that would be subjected to an analog signal.

The digital output stream is then fed into a DSP board to be low-pass filtered. Low-pass filtering removes the noise components that had been shifted to high frequencies. Temperature data can then be extracted from the filtered values.

A control chip on the needle is used to receive instructions from a PC. Appropriate signals are then sent to individual sensors. The only limitation on the number of sensors per needle is the number that physically fit along the length.

[3]See reference for full derivation.

[4]Another option would be to subtract voltages corresponding to undesired temperatures, and then amplify the signal to lower the requirement of the A/D converter. In this case, the subtraction would have to be accurate to 18.3 bits.

2.5 Thermal Artifact

Since the integrated circuits generate power, it is important to understand this effect on the sensor measurements. Simulations of power dissipation of the previous design resulted in a peak temperature elevation on the chip of about 46m°C. [5] If the sensor is used only to sense temperature, this accuracy is adequate for use in treatement. A reasonable accuracy requirement for this use is .1°C. The artifact will limit the accuracy of transient measurements to 46m°C. In steady state, this error could be subtracted as an offset if its value is known. When measuring perfusion, the presence of a thermal artifact will require careful measurement of the temperature and applied power both before and after the temperature step. If the artifact does not change during the measurement process, it does affect the accuracy of perfusion measurements. Since this thesis will make area reductions of the sensor chip, corresponding power reductions are necessary to keep the same thermal artifact.

[5] A full description of the simulation setup and simulation results are describe in Szajda's thesis. [4]

Chapter 3

Analog-to-Digital Conversion

3.1 Introduction

Analog-to-digital conversion is done on the sensor chip, in close proximity to the sensor, to prevent corruption from noise as the signal is moved off chip. This conversion is done at the expense of power and area consumption on the sensor chip, so design care is needed for these important parameters. In addition, the resolution of the temperature data, 18.3 bits, must be maintained.

Sigma-delta modulation is used for the analog-to-digital conversion. The modulator oversamples the signal, and using a noise shaping feedback loop, shifts quantization noise to high frequencies. The technique therefore capitalizes on the low frequency nature of the signal (0-1 Hz). In addition, the resolution of this conversion can be high with relatively coarse components.

This chapter will explain the principles of Sigma-delta A/D conversion, first from an intuitive approach in the time-domain and then quantitatively in the frequency domain. Design issues affecting power and area will be discussed, explaining changes in architecture from the first generation design. Finally, the specific design imple-

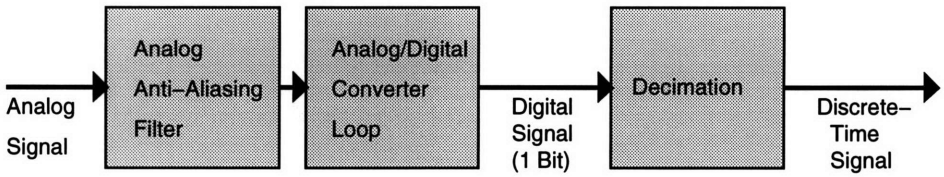

Figure 3-1: Sigma Delta A/D Conversion- Overall System

mentation will be described and important characteristics summarized.

3.2 Sigma-Delta A/D Conversion

Even with perfect implementation, any conversion from the analog to the digital domain has an inherent quantization error. This results from representing a continuous signal with a finite number of bits. A sigma-delta modulator reduces quantization error by making coarse conversions at a very high sampling rate, trading low frequency resolution for bandwidth. Signal processing techniques can then be used to extract accurate data at the lower frequencies. [17]

A typical system for sigma-delta analog/digital conversion is shown in Figure 3-1. According to Nyquist theorem, aliasing will occur unless the analog signal is limited to frequencies less than one half the sampling frequency. In a sigma-delta converter, the signal will be sampled at a much greater frequency than the signal of interest, so the requirements on the filter are relaxed due to the higher rate of sampling.

The A/D converter loop includes a quantizer inside a feedback loop. Typically, this quantizer contains very few bits, often 1. The clock rate in the loop is run many times faster than the required conversion rate as determined by the Nyquist criteria. The output of the modulator is a digital bit stream. The decimation, which is done in the digital domain, is responsible for removing high frequency components of the resulting

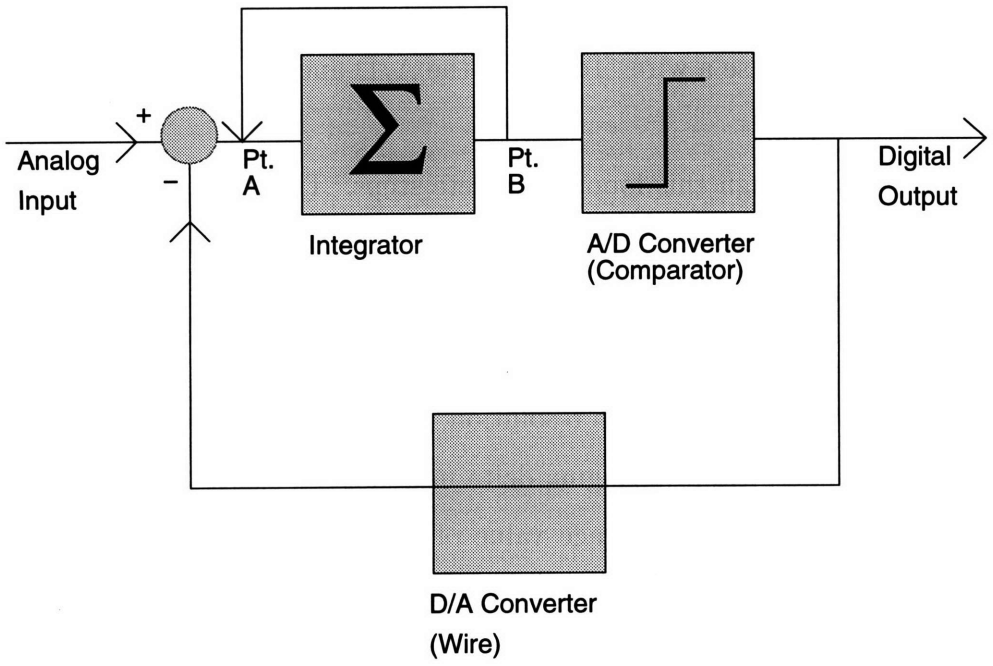

Figure 3-2: Sigma Delta A/D Converter Loop

signal. These high frequency components contain most of the quantization noise, since it has been shaped by the modulator. [17] Decimation of the digital output extracts the low-frequency components of the output, which contain signal information, and discards the quantization noise that has been shifted to high frequencies. This signal processing is done off-chip, and does not contribute to the power and area of the sensor.

3.2.1 Modulation

This section will describe a very simple sigma-delta modulator. A general model for more complicated (and more accurate) systems will then be introduced.

A simple A/D converter loop is shown in Figure 3-2. Incorporated in the feed-

forward path is a discrete-time integrator followed by an A/D converter. In this case, the A/D converter is one bit, and is therefore a comparator. The feedback loop has a D/A converter, in this case a wire. Together, the A/D and D/A converters are called a quantizer.

Table 3.1 steps through this loop in discrete steps. The reference voltage is +/- 5 Volts and the initial state is zero. The input is a DC value of 2 Volts. The same pattern repeats every ten cycles.[1] The average value of the output, over a large number of samples, is 2.[2] By sampling at a high rate, low frequency components of the signal can be converted with high resolution, despite the fact that A/D conversion is only 1 bit. This is typical of all sigma delta modulators. With the use of feedback and a high sampling rate, the average value of the digital output of the converter approximates the average value of the continuous-time, analog input.

A generalized case for a sigma-delta modulator appears in Figure 3-3 . In this case, the integrator is replaced by an arbitrary system function, H(z). If the signal at the input of the A/D converter is sufficiently random and uncorrelated with the input, the system can be represented by a linearized model (Figure 3-4). In this model, the quantizer is replaced by a random noise source. This noise source is the quantization noise introduced by converting a continuous signal into a one-bit representation.

Using this model, transfer functions can be derived from Black's formula.

$$\frac{Output}{Input} = \frac{H(z)}{1 + H(z)} \tag{3.1}$$

$$\frac{Output}{Noise} = \frac{1}{1 + H(z)} \tag{3.2}$$

[1]This is a typical problem with a low order loop. Repeating patterns add harmonic distortion. In designs higher than 2nd order, this problem is greatly reduced.

[2]Since the pattern repeats every ten time steps, the average value over a large number of time steps is the same as the average value of the first ten steps.

Input (Volts)	Integrator Input (Volts)	Integrator Output (Volts)	D/A Output (Volts)
2	-3	0	5
2	7	-3	-5
2	-3	4	5
2	-3	1	5
2	7	-2	-5
2	-3	5	5
2	-3	2	5
2	7	-1	-5
2	-3	6	5
2	-3	3	5
2	-3	0	5 *(repeats)
2	7	-3	-5
2	-3	4	5

Table 3.1: A/D Conversion Simulation

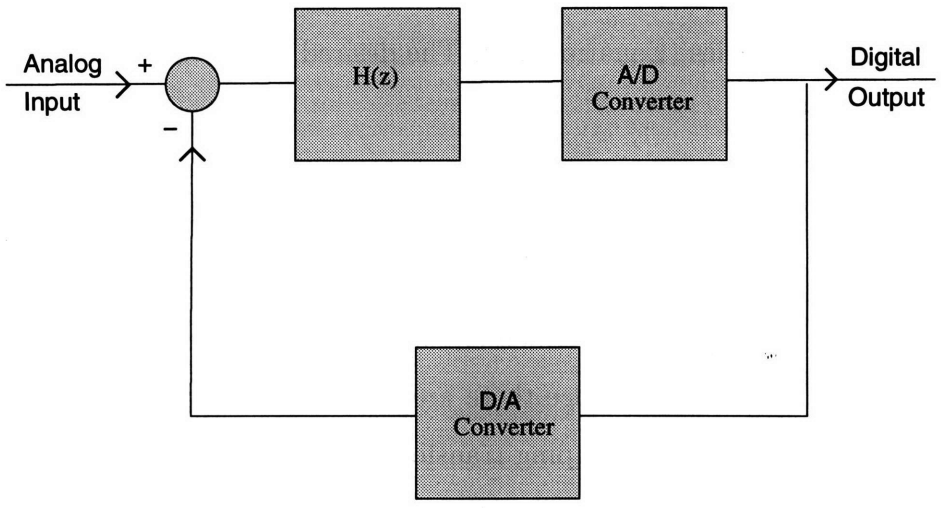

Figure 3-3: General Sigma/Delta Converter Loop

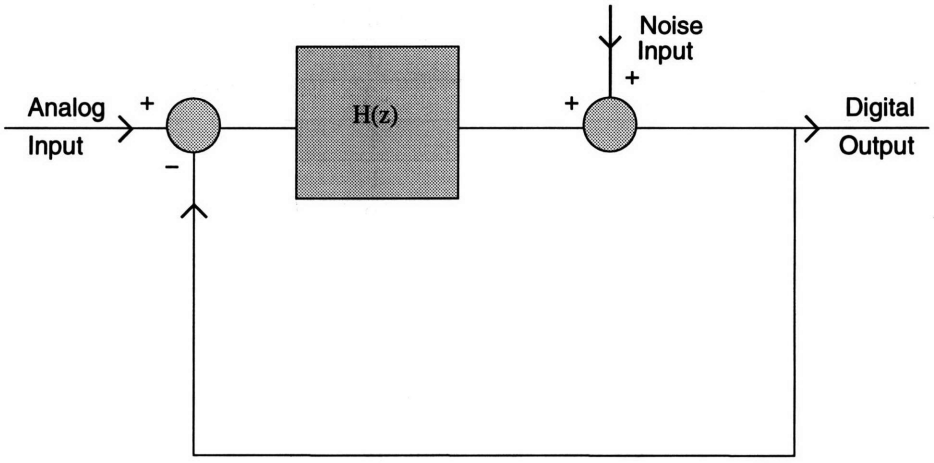

Figure 3-4: Linearized Model of Sigma/Delta A/D Converter Loop

H(z) is designed so low frequency components of the signal pass through the system (Equation 3.1), while the quantization noise is attenuated for low frequencies and passed at high frequencies (Equation 3.2). The desired characteristics are obtained if H(z) is a low pass filter.

3.2.2 Transfer Function Implementation

The transfer function, H(z) is implemented using a third order, distributed feedback architecture (Figure 3-5). [18] Since there are three integrators, the system is third order and will produce a noise shaping transfer function with three poles.

The output of the comparator is fed back to the input of each of the integrators with a gain of B1, B2, or B3. These coefficients, along with the integrator gains, C1, C2, C3, can be implemented with the same operational amplifier as the integration.

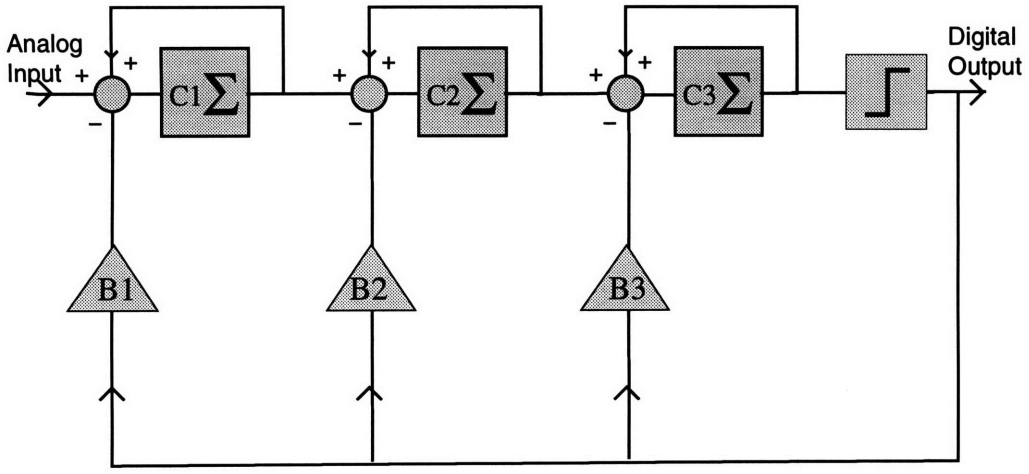

Figure 3-5: Sigma Delta Architecture

Therefore, this loop can be built with a total of three operational amplifiers.

As a comparison, the first generation design was fourth order, feed-forward implementation(Figure 3-6). Here, four integrators provide fourth order noise shaping. The output of each integrator is fed forward into a summer. This design requires five operational amplifiers: four for the integrators and one for the summer. Since the desired noise shaping can be implemented with a third order system and a distributed feedback architecture eliminates the necessity of a summer, two amplifiers are eliminated in the new design.

The transfer function from the input to output must pass signal frequencies while the transfer function from the quantized noise source to the output must attenuate low frequencies. After the architecture of the system is chosen, the coefficients (B's and C's) are designed to obtain these characteristics. First, the transfer functions are determined. The integrators are implemented in discrete time, with a one cycle

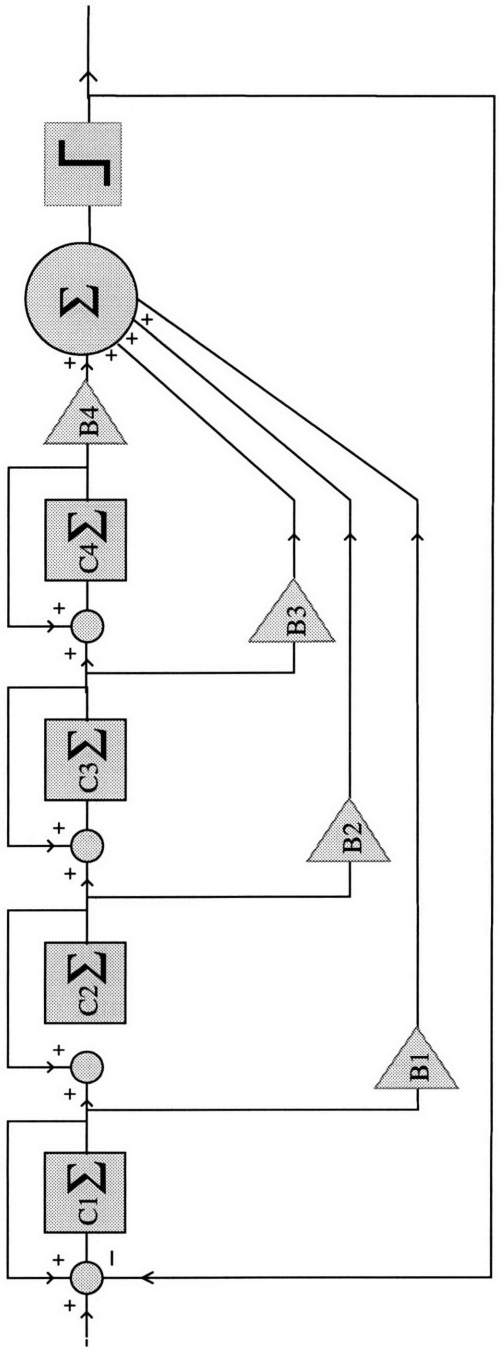

Figure 3-6: Previous Sigma Delta Architecture

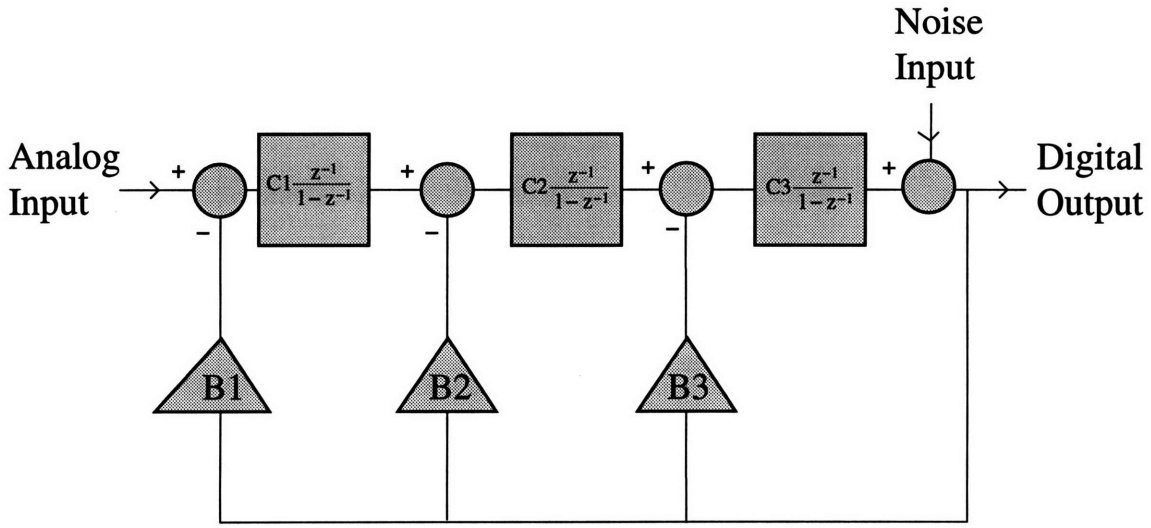

Figure 3-7: Z Transform Block Diagram

delay. The z transform of each integrator is:

$$\frac{Cz^{-1}}{1-z^{-1}} \tag{3.3}$$

Using the linear model of the system, the z-transform block diagram is shown in Figure 3-7.

Solving for the transfer functions:

$$\frac{Output}{Noise} = \frac{(1-z^{-1})^3}{1+a_1z^{-1}+a_2z^{-2}+a_3z^3} \tag{3.4}$$

$$\frac{Output}{Input} = \frac{C_1C_2C_3z^{-3}}{1+a_1z^{-1}+a_2z^{-2}+a_3z^3} \tag{3.5}$$

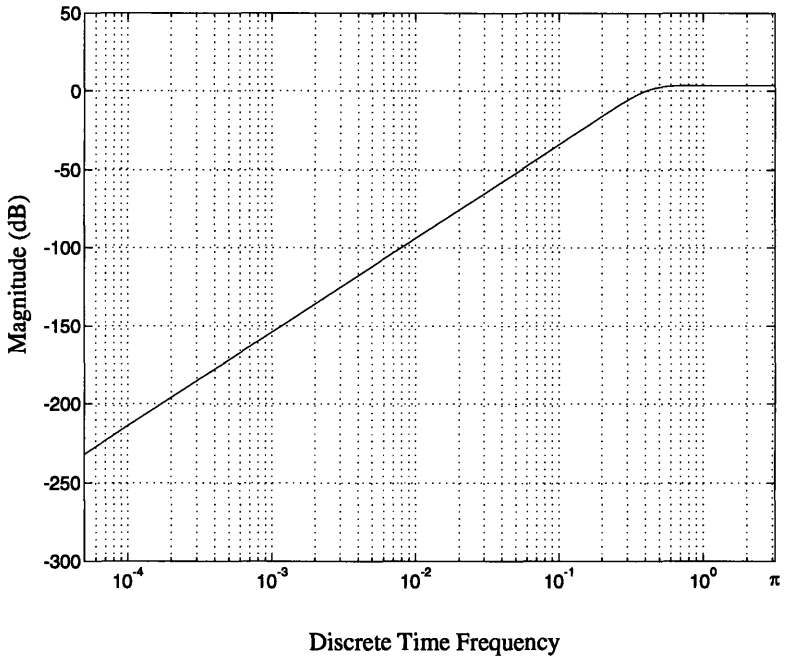

Figure 3-8: Noise Shaping Transfer Function

$$a_1 = B_3C_3 - 3 \tag{3.6}$$

$$a_2 = B_2C_2C_3 - 2B_3C_3 + 3 \tag{3.7}$$

$$a_3 = C_1B_1C_2C_3 + B_3C_3 - B_2C_2C_3 - 1 \tag{3.8}$$

The feedback coefficients (B_1, B_2, B_3) form the poles of the noise shaping transfer function. Although this design has three zeros at DC, it is also possible to move these zeros to obtain a wider stopband by adding feedforward coefficients as well. Due to size considerations, this will not be done since the extra noise shaping is not necessary.

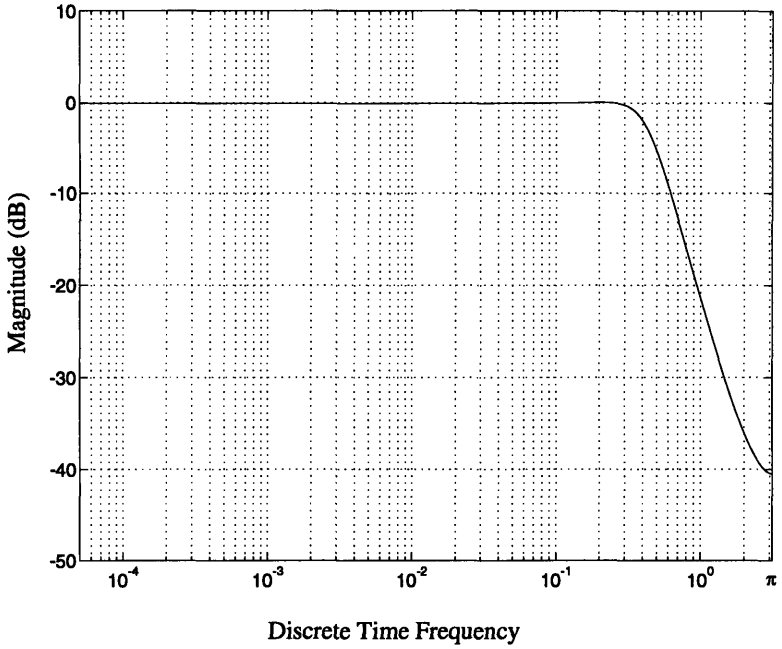

Figure 3-9: Input Transfer Function

The desired transfer function for the noise is a high pass filter. Using Matlab, the coefficients for a third order high pass filter were determined. The denominator of this equation was used to determine the poles of the desired noise shaping transfer function.

$$\frac{Output}{Noise} = \frac{(1-z^{-1})^3}{1+-2.17z^{-1}+1.65z^{-2}-.43z^{-3}} \tag{3.9}$$

The denominator of these equations, and thus the poles of the filter, are made to match the noise shaping transfer function. The corner frequency of the filter was chosen so the high frequency gain of the noise transfer function was 1.52. This gain has been empirically determined to be related to the stable operation of the modulator. [19] The coefficient values, (C's and B's) are then chosen to match this transfer function.

$$C_3B_3 - 3 = -2.17 \tag{3.10}$$

$$C_2C_3B_2 - 2B_3C_3 + 3 = 1.65 \tag{3.11}$$

$$B_2C_2C_3 - 1 = -.43 \tag{3.12}$$

This is an underconstrained problem with 3 equations and 6 unknowns. There is a fair deal of flexibility in choosing values. Another constraint is that the value B1, determines the gain of the signal transfer function and is chosen to be 1 for a gain of 1. After a first pass is made, the design process is iterative. A Sigma-Delta simulation program, SIM [20], was used to simulate these values. This was used to evaluate stability and the check the saturation of the amplifiers. The output of the amplifiers must remain within their differential output swing.

The simulations were also used examine the behavior of the comparator. Since the model used for the design is based on a linear behavior approximation of this non-linear element, the model is not valid when this approximation breaks down. This approximation is that the input to the comparator is a random and uncorrelated with the modulator input. As the DC input of the system approaches full scale, this approximation breaks down.

According to Parseval's theorem, the square of the integrated frequency output of the comparator must be a constant. Since the system is highly oversampled, the "average gain" of the comparator can be estimated by averaging the input and output. In the linear model described above, it was assumed that the gain was 1. If the gain is not 1, the noise shaping transfer function will be different than the linearized design. As the DC value of the input in increased, the "average gain" of the comparator becomes smaller, moving the poles of the transfer function outside the unit circle, leading to instability. As a method of design, the procedure illustrated in Robert

Adams' paper was followed.[18] This involves iteratively measuring the average gain of the comparator and making slight shifts in the corner frequency to obtain a gain of 1 for low DC inputs. This verifies stability of lower frequencies.

Following this argument, the actual value of C3 is not independent of the comparator gain. If gain of C3 is decreased, the "average gain" of the comparator will increased because the output is only dependent on the sign.[3]. C3 can therefore be reduced to keep its output within the amplifier output swing without changing the noise shaping characteristics of the system.[4]

The following coefficients values were used to determine the noise shaping:

B1	1
B2	.3864
B3	.2068
C1	.0620
C2	1.2
C3	4

Table 3.2: Modulator Coefficient Values

Simulations have verified that this feedback loop is stable for an input up to 60% of DAC reference. Figure 3-10 represents a sinusoidal input of 1 Volt at 1 Hz and a sampling frequency of 2.81 kHz. The signal at 1 Hz, as well as the quantization noise, is apparent in this output.

[3]This has been verified with simulation

[4]Following the above argument, C_3=.25 in circuit implementation.

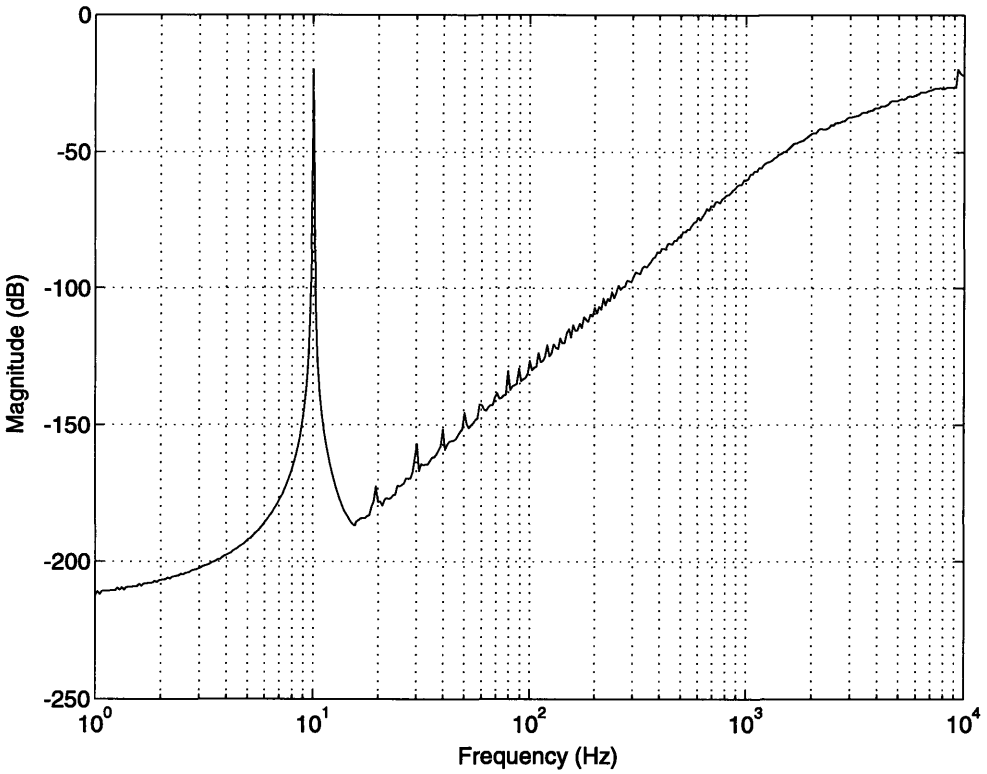

Figure 3-10: Simulation of Input

3.3 Oversampling Ratio

The noise shaping characteristics of the modulator can be seen in Figure 3-8. One bit is approximately 6dB. The requirement of the modulator is about 20 bits. [5] This corresponds to a noise shaping of 120 dB. A conservative design goal is to achieve noise shaping of 132 dB at the highest frequency of interest, 1 Hz.

The x-axis in Figure 3-8 is in discrete time frequency with value up to π. The desired noise shaping of 132 dB occurs at a discrete-time frequency of .00223. This discrete-time frequency should correspond to 1Hz in the original continuous time signal. The following formula can be used to calculate the minumimum sampling

[5] The full-scale input is about 1/4 of full scale, adding 2 bits to the 18.3 bit resolution requirement.

rate:

$$w_d = fT \tag{3.13}$$

where w_d is the discrete time frequency, f is the continuous time frequency, and T is the sampling period. For $f = 6.28\frac{1}{s}$ (1Hz), the minimum sampling frequency is 2.81 kHz. This is the minimum sampling rate required for the desired noise shaping characteristics of the sigma-delta modulation.

This sampling rate is also related to several sources of noise. Reduction of the sampling rate by a factor of n will increase each of these noise source by $\sqrt{n}$.

1. Thermal noise at the input of the preamplifier is aliased during correlated double sampling.

2. Switches contribute $\frac{kT}{C}$ noise. The total noise of the switch is divided by the square root of the oversampling ratio.[6]

3. Thermal noise from opamps and diodes is aliased when sampled with switched capacitors.

Reduction of the sampling rate from the previous value of 65.536 kHz to 2.81kHz will significantly increase the noise contributions from all three sources. Since this design must preserve the temperature resolution of the 1st generation sensor, the system components must function properly with a sampling rate as high as 65.536 kHz.

3.4 Additional Power Savings

Of the three operational amplifiers in the modulator, the characteristics of the first is the most critical since it is at the input. Therefore, the noise from the amplifier at this

[6]For a 1 pF capacitor, the total noise voltage at each switch is 4.15nV.

stage is directly reflected at the output. The noise at the input from the other stages, however, is shaped similar to the quantization. Thus, the noise from the second and third opamps can be much higher and not effect the design.

Lowering the current in the first stage of the amplifier lowers g_m and increases the equivalent input noise voltage. Because noise introduced at the inputs of the second and third amplifiers are shaped, the current in these operational amplifiers can be reduced, thereby reducing power.

3.5 Implementation

3.5.1 Switched Capacitor Integrator

Switched capacitor filters were used as the building blocks for the modulator. [16] Discrete time integration eliminates errors that are introduced by integrating different patterns of feedback because the integration reaches its final value at each discrete step. Because $\frac{kT}{C}$ noise is reduced by the square root of the oversampling ratio, the noise introduced by these switches is insignificant.

Each stage of the modulator was implemented with a two input, non-inverting, differential integrator, as shown in 3-11. To save area, rransmission gates are used only when the swing of the signal makes them necessary. Delayed clocking is used to prevent feedthrough nonlinearities.

The transfer function is obtained by first examining the charge balance on the top half of the circuit. When ϕ_2 is high, the charge on the capacitors is:

$$Q_{C1,2} = C_1(V_{in+} - V_{cm}) \tag{3.14}$$

$$Q_{C2,2} = C_2(Quan_- - V_{cm}) \tag{3.15}$$

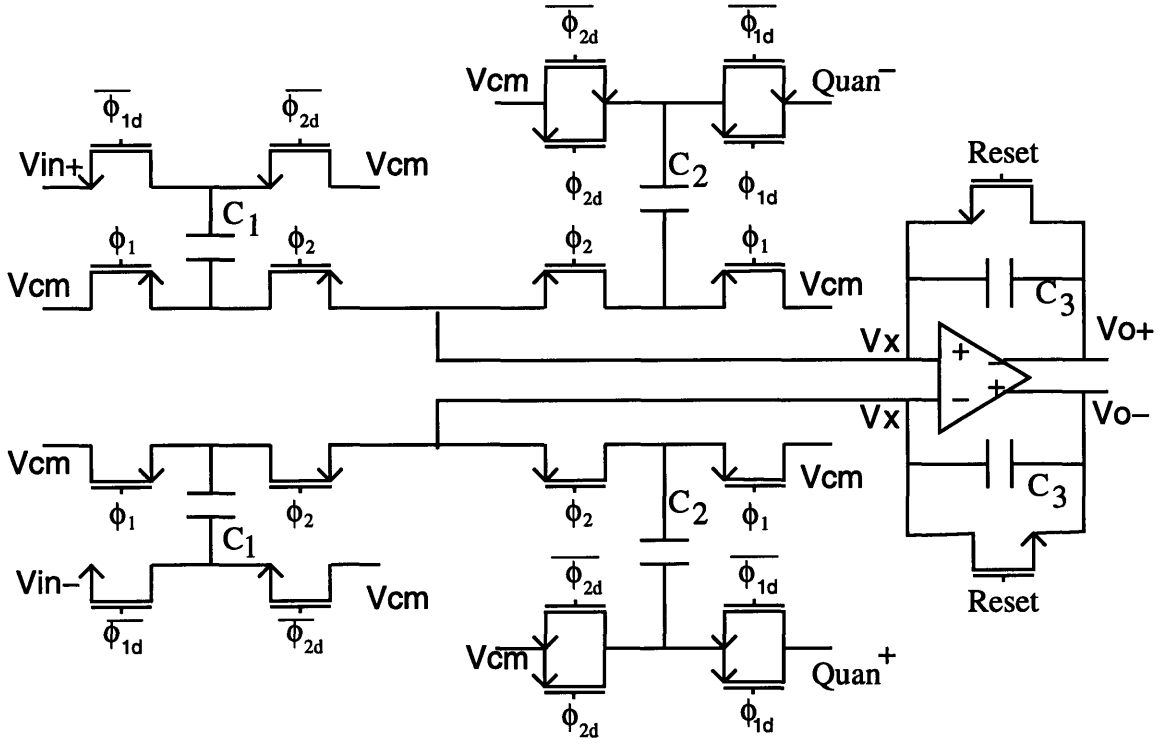

Figure 3-11: Two Input Integrator

$$Q_{C3,2} = C_3(V_{op+} - V_{x,2}) \tag{3.16}$$

where V_{op+} is the value of V_{o+} at the end of the previous cycle. $V_{x,2}$ is the voltage at the input terminals of the operational amplifier when $\phi 2$ is high. V_{in+} and $Quan\_$ are the two inputs to the integrated. V_{in+} is the positive output of the preamplifier or the previous integrator in the modulator and $Quan\_$ is the negative feedback from the quantizer.

When ϕ_1 is high, the charge on the capacitors:

$$Q_{C1,1} = C_1(V_{cm} - V_{x,1}) \tag{3.17}$$

$$Q_{C2,1} = C_2(V_{cm} - V_{x,1}) \tag{3.18}$$

$$Q_{C3,1} = C_3(V_{o+} - V_{x,1}) \tag{3.19}$$

$V_{x,1}$ is the voltage at the input terminals when ϕ_1 is high. By equating the total charge during the two cycles:

$$V_{o+} = \frac{C_1}{C_3}(V_{in+} - 2V_{CM} + V_{x,1}) + \frac{C_2}{C_3}(Quan_- - 2V_{CM} + V_{x,1}) + V_{x,1} + V_{op+} - V_{x,2} \tag{3.20}$$

Similarly, the same analysis can be done for the bottom half of the circuit. Since the operational amplifier has high gain, it is assumed that the input terminals are equal.

$$V_{o-} = \frac{C_1}{C_3}(V_{in-} - 2V_{CM} + V_{x,1}) + \frac{C_2}{C_3}(Quan_+ - 2V_{CM} + V_{x,1}) + V_{x,1} + V_{op-} - V_{x,2} \tag{3.21}$$

The differential output is:

$$V_{o+} - V_{o-} = \frac{C_1}{C_3}(V_{in+} - V_{in-}) + \frac{C_2}{C_3}(Quan_- - Quan_+) + (V_{op+} - V_{op-}) \tag{3.22}$$

This circuit accomplishes both integration and summation of the two inputs using one amplifier. The gain of the amplifier is $\frac{C_1}{C_3}$ and the feedback coefficient from the quantizer is $\frac{C_2}{C_1}$. The reset switch is provided to zero the output voltage if overload occurs.

3.5.2 Comparator

The quantizer in this design is one-bit, so a comparator is used for both the A/D and D/A converter. A clocked bistable latch is used (Figure 3-12). When ϕ_1 is high, the output voltages are charged to the output values of the third integrator. When ϕ_2 is high, the inputs are isolated from the circuit and the latch is connected to references. Positive feedback causes the outputs to be driven to the two rails; the output beginning at the higher voltage is drive to V_{dd}, while the other is grounded.

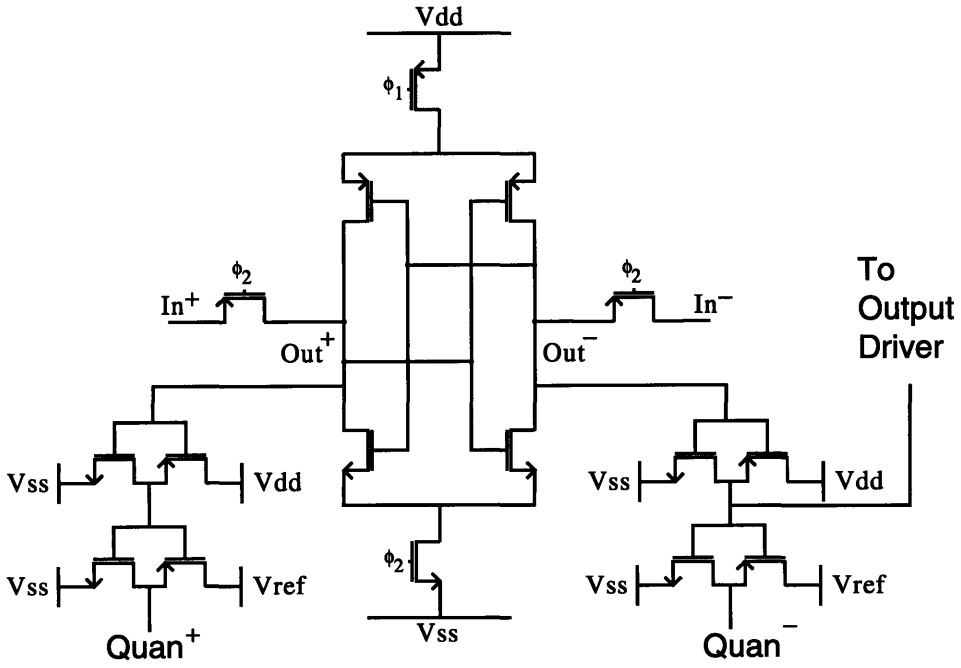

Figure 3-12: Comparator Schematic

The output of the comparator is fed directly into inverters, one for each output to ensures symmetrical loading. The output of one of these inverters is sent to the output driver. Another set of inverter buffers serves to drive the feedback voltage to V_{ref} or ground. V_{ref} must be constant over the frequencies of interest to the full scale of the desired A/D conversion because it feeds directly into the input of the modulator.

3.6 Summary

The following table summarized the characteristics of the sigma-delta modulator.

	Old Implementation	New Implementation
Order	4th	3rd
Oversampling Ratio	6554	6554
Clock Rate	32.768 kHz	32.768 kHz
Noise shaping at 1 Hz	250 dB	214 dB
Number of Amplifiers	5	3
Power Supply	6V	3V
Power Usage per OpAmp	560 μW	175 μW (1st Opamp) 100μW (2nd and 3rd Opamp)
Power Usage Total	2.8 mW	.375 mW
Space	610 x 5100 microns	610 x 1700 microns

Chapter 4

Operational Amplifier

The operational amplifier is one of the major building blocks of the system. One amplifier is used for temperature sensing, one for preamplification, and three for the sigma-delta A/D modulator. The operational amplifiers are the major source of static power consumption in the design, and are therefore the major source of power consumption. Since this basic building block is repeated five times, effort made in optimizing a single operational amplifier will be multiplied.

This chapter reviews specifications set on the operational amplifier and explains the basic amplifier design. A low power/area method of common mode feedback, along with complementary biasing is also introduced. Design considerations that relate to power consumption are considered.

4.1 Operational Amplifier Specifications

Although separate optimized designs could have been generated for each of the amplifiers, one basic topology was used to simplify the design and keep the project time reasonable. Since the operational amplifier is used for both the sensor and the signal

processing, the performance criteria is determined by the most stringent of the two needs. [1]

Open loop gain is most important in the front end sensor. The offset due to threshold differences and size mismatches of the differential pair transistors in the sensor is divided by the open loop gain of the amplifier.[2] If the offset voltage is constant, the error can be removed by calibration. However, there is drift in the offset with temperature, which results in measurement error. A gain of about $2x10^4$ is required to ensure that this error is less than 19.8 nV, or less than 10 % of the error budget.[4]

Settling time is critical for the signal processing. Full settling is necessary in the preamplifier so the input into the A/D converter is an accurate representation of the measured signal. Full settling is also necessary in the sigma-delta modulator.[3] With reference to full scale, the signal must settle to about 20.3 bits during one half the clock period (7.6 u).[4] With a worst case 1/10 feedback and 10% of the half clock cycle alloted to slewing, the required unity gain bandwidth is 3.26 MHz. The phase margin must be at least 60° to prevent ringing. To implement sigma-delta modulation, a reasonable differential output swing is at least 2 Volts is necessary.

To resolve 1 m°C, the sensitivity at the output of the sensor has to be at least 198 nV. The input referred noise at the operational amplifier of the sensor contributes directly to the signal. Because the operational amplifier is chopped, which removes low frequency offset and flicker noise, the major contribution is the broadband thermal noise. The preamplifier also contributes noise, although correlated double sampling

[1] An exception was made for the second and third amplifiers in the modulator because a simple change leads to substantial power reduction. This is explained in Chapter 3.

[2] The offset of the operational amplifier itself is nullified by the chopping circuitry.

[3] A guarantee of linear settling would relax this constraint, but this is not practical due to power constraints.

[4] This represents the 18.3 bits necessary for the temperature resolution plus another 2 bits because the signal is not the full scale.

does provide some reduction. The amplifier at the input of the sigma-delta modulator also has a noise contribution, with its relative contribution is divided by the gain of the preamplifier. To obtain the measurement resolution of the old implementation, the thermal noise contribution of the amplifier below the range of interest (1Hz), must be less than 12nV.

Other characteristics of the operational amplifier are not as critical. Since the critical sensing circuitry is isolated from moving digital signals, excessive power supply rejection ratios are not critical. The differential circuitry also relaxes the common mode rejection tolerance.

In line with these requirements, the design was best optimized to reduce the power and area.

4.2 Basic Topology

The basic structure of the operational amplifier is a folded cascode (Figure 4-1).[4] Typical results from a folded cascode topology are moderate in both gain and bandwidth and a high phase margin. The compensation capacitances are provided by the capacitive load already in the topology, eliminating the area of extra capacitors.

PMOS input devices are used because fully isolated PMOS devices are provided by the fabrication processes. Common-mode feedback (devices M9 and M10) is used to maintain the common mode level at the output and will be explained in detail later in this chapter. Although the cascoded output stage reduces the output swing, improved cascode biasing minimizes this reduction.[21] A self-biasing current source is used for biasing the on-needle circuitry.

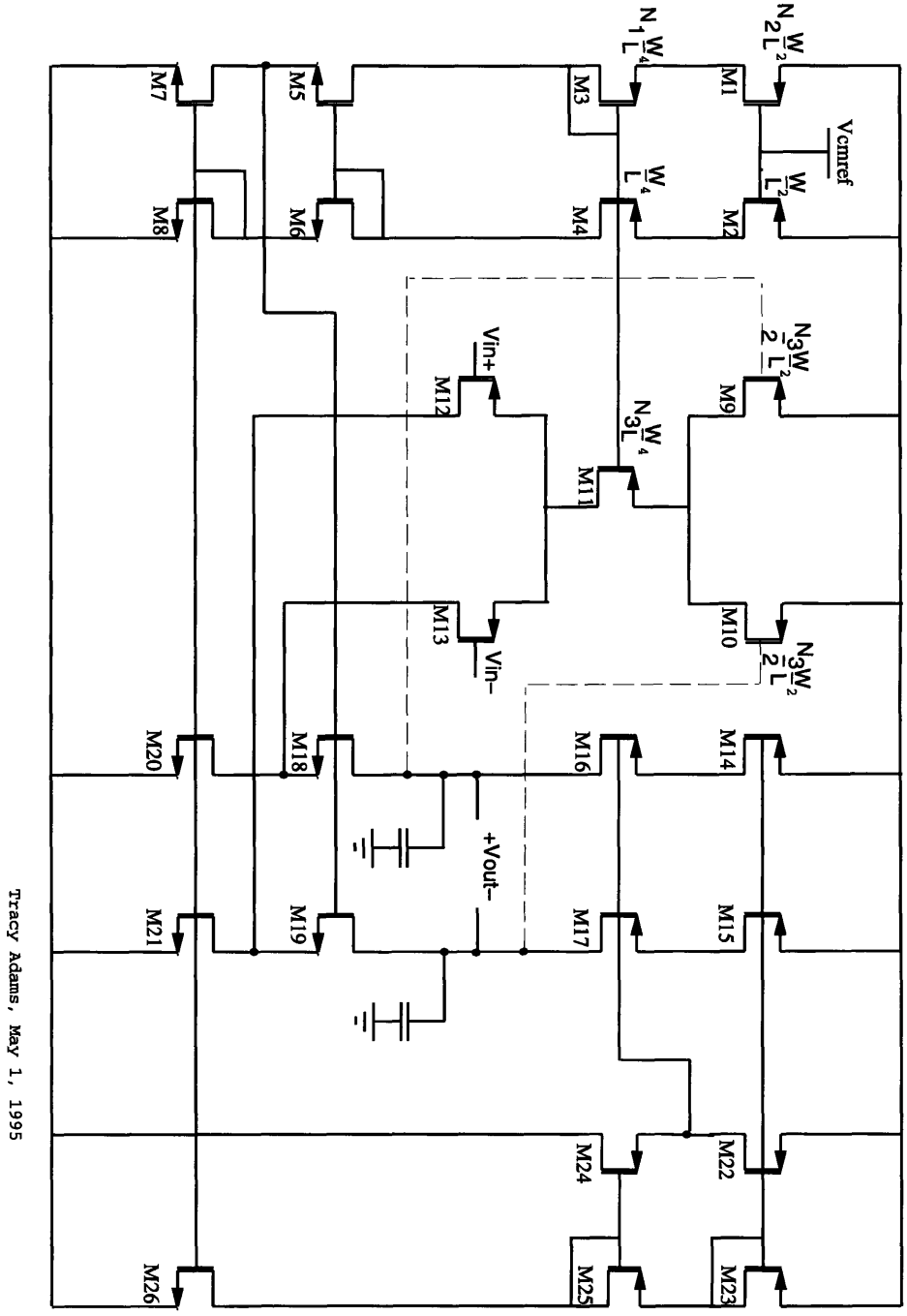

Figure 4-1: Operational Amplifier

4.3 Operational Amplifier Characteristics

4.3.1 Gain

Gain calculations of an operational amplifier are implified by first examining the small signal models of some typical MOSFET connections. The first case shows the gate and source grounded (Figure 4-2a). The small signal model is simply an output resistor, R_o. When a source resistor is present, the analysis is slightly more complicated(Figure 4-2b). Again, however, the result is a modified output resistance given by $R_e + R_o(1 + g_m R_e)$. When the gate and drain are grounded(Figure 4-2c) , the result is a resistor of value $\frac{1}{g_m}$. With a drain resistance present as well (Figure 4-2d), the resistor value is $\frac{(R_D+R_o)\frac{1}{g_m}}{\frac{1}{g_m}+R_o}$. When $R_D << R_o$ and $\frac{1}{g_m} << R_o$, the resistor value is approximately $\frac{1}{g_m}$. The heart of the folded cascode is shown in Figure 4-3. To find the DC gain, the Norton equivalent of the small signal model is evaluated. I_{SC} is found by solving for the short circuit output caused by a small signal voltage at the input. Using our simplifications, the small signal model for half of the circuit is shown in Figure 4-4 (upper left). Since the value for $\frac{1}{g_{m19}}$ is a few kΩ and R_{o20} is well over 100 kΩ, the short circuit current is $v_{in} g_{m12}$. The diagram on the right is used to find R_{out}. The Norton equivalent model appears in the lower left. The differential open circuit gain is $g_{m12,13} R_{out}$. The total gain is approximately:

$$A = g_{m12}[(R_{o12}||Ro20)g_{m18}R_{o18})||(R_{o14}g_{m16}R_{o16})] \tag{4.1}$$

$$A \propto (g_m R_o)^2 \tag{4.2}$$

The gain of the circuit is directly related to the intrinsic device voltage gain, or the $g_m R_o$ products of $M_{12,13}$, $M_{18,19}$ and $M_{16,17}$. To operate at the highest possible gain, devices should be biased at weak inversion, where this product is maximized.[22]

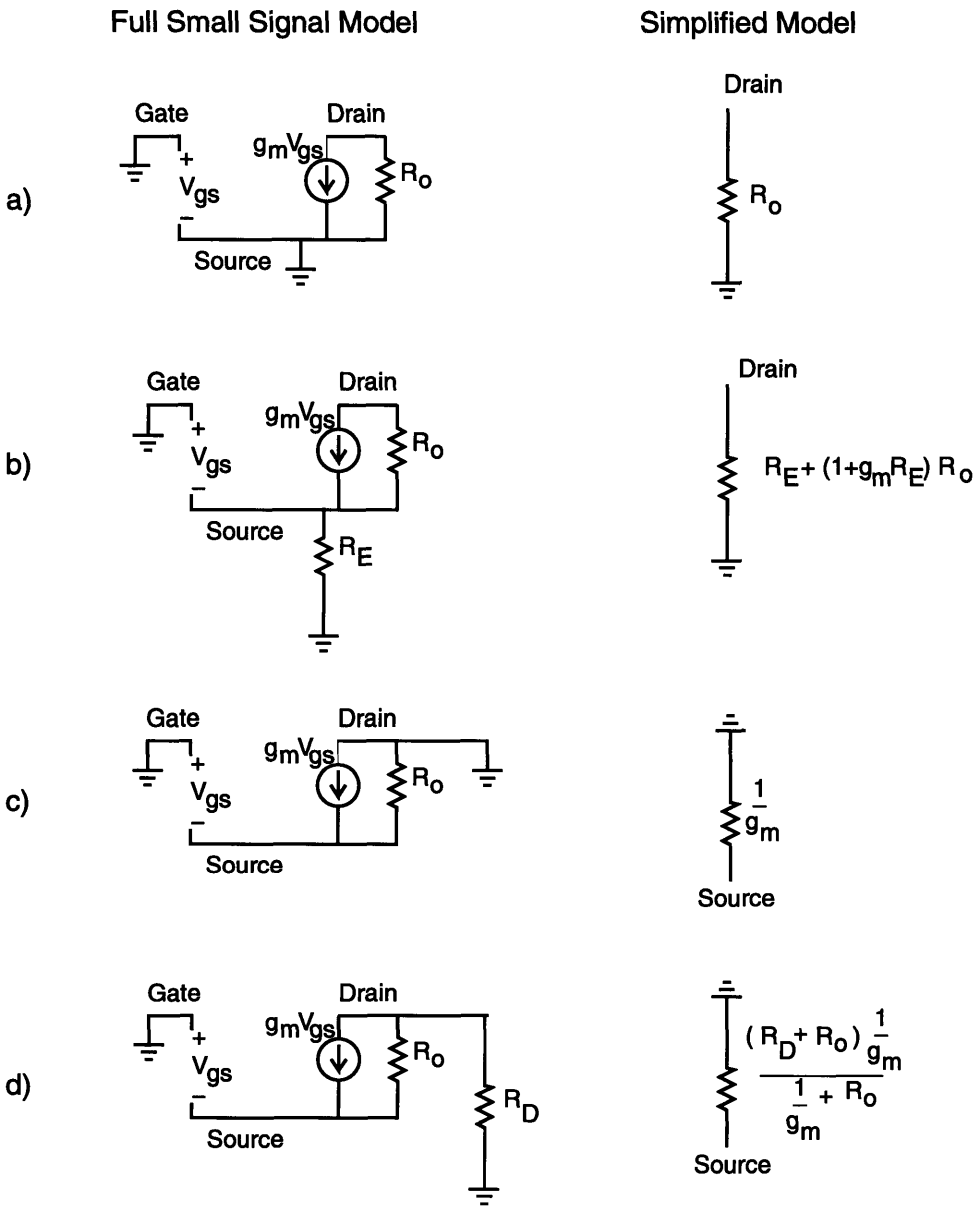

Figure 4-2: Simplified Small Signal Models

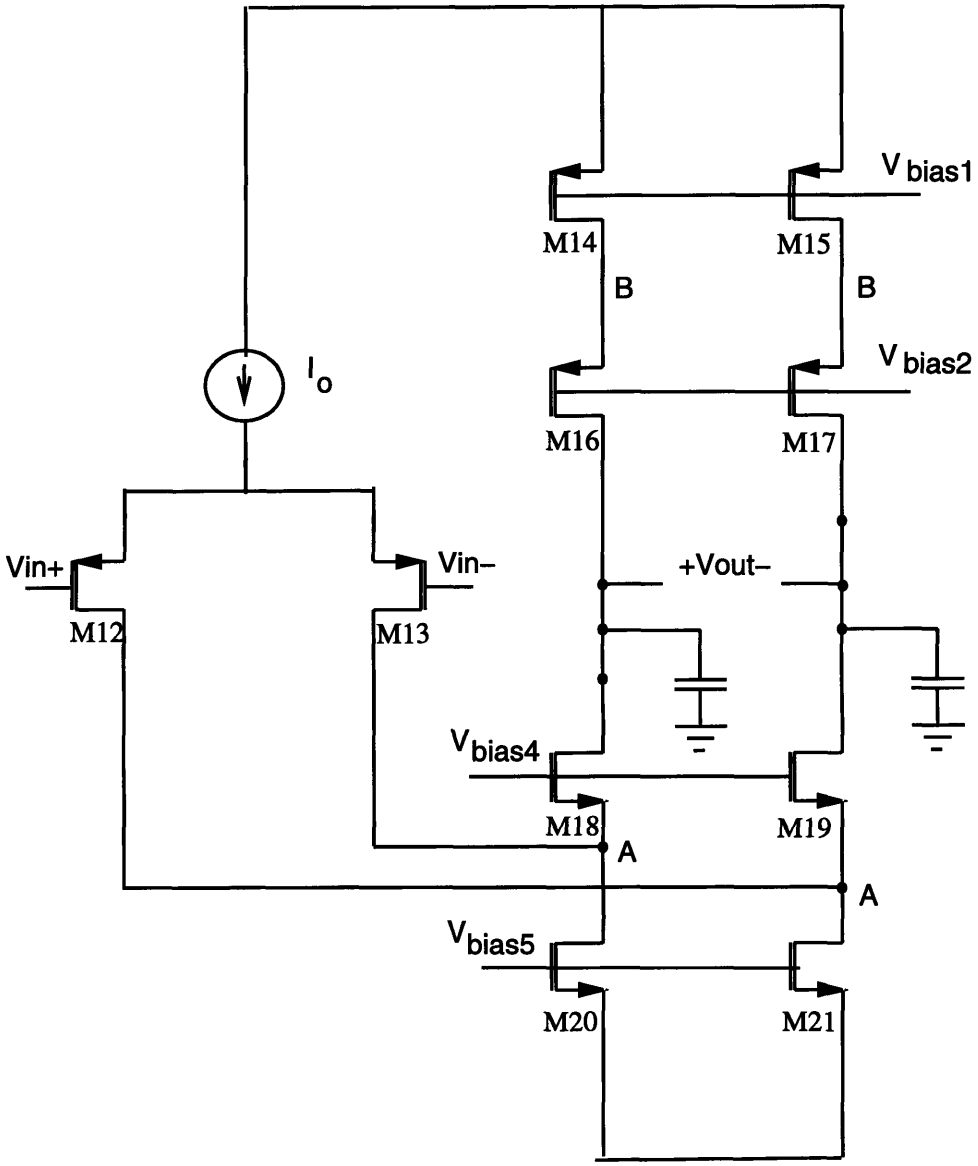

Figure 4-3: Folded Cascode Topology

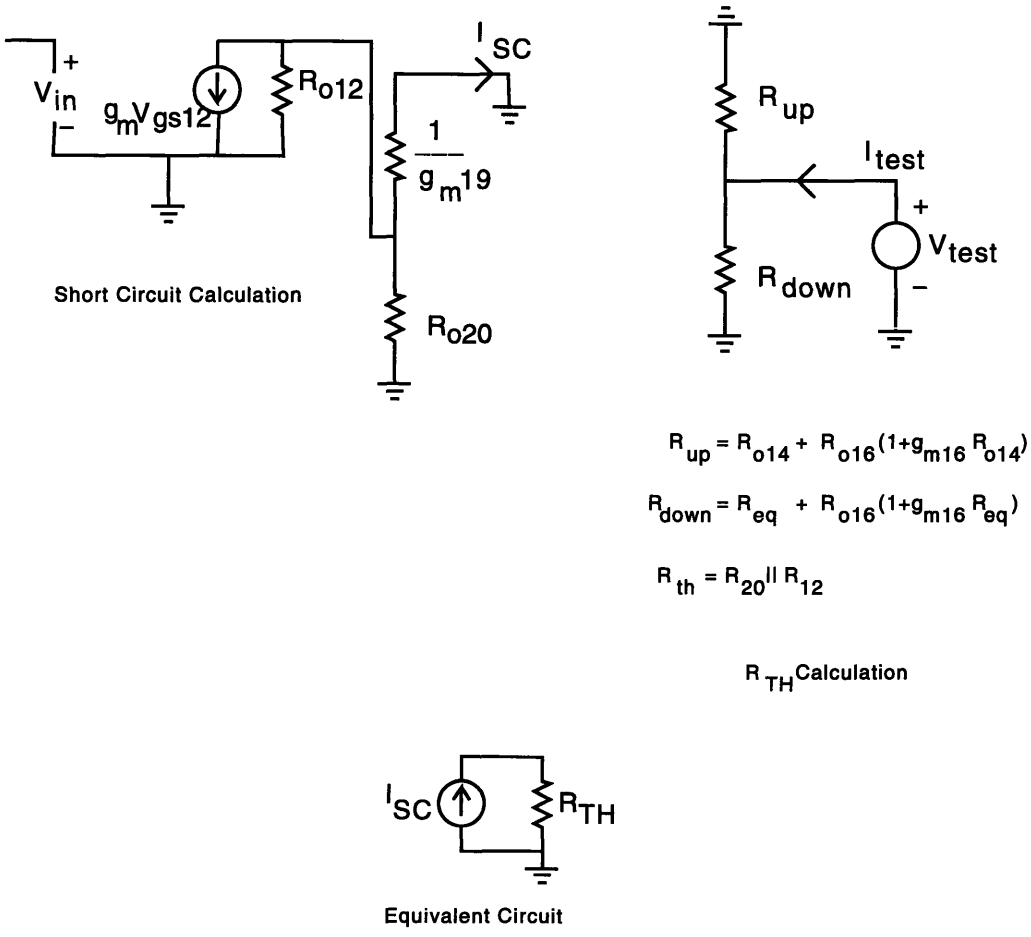

Figure 4-4: Small Signal Equivalent of Folded Cascode

When the device is in strong inversion, as is shown below, this product is related to $\frac{1}{\sqrt{I}}$, and is therefore larger at lower currents. When the device enters subthreshold, this product is constant, so lowering current will not help the intrinsic gain and will lower bandwidth by unnecessarily increasing device size. Although there are other issues that affect current (such as slew rate, bandwidth, and noise), a lower current will raise the intrinsic gain. In addition, for a given current, W/L should be increased until the device is biased at at moderate inversion. This is advantageous to a low power design.

Above Threshold:

$$g_m = \sqrt{2\mu C_{ox}(\frac{W}{L})I_d} \tag{4.3}$$

$$R_o = \frac{1}{\lambda I_d} \tag{4.4}$$

$$A_{oc} = g_m R_o = \sqrt{\frac{2\mu C_{ox}(\frac{W}{L})}{\lambda^2 I_d}} \tag{4.5}$$

Below Threshold:

$$g_m = \frac{I_d}{V_{th}} \tag{4.6}$$

$$A_{oc} = \frac{1}{\lambda V_{th}} \tag{4.7}$$

4.3.2 Bandwidth

Open circuit time constants can be used to find the frequency response of the amplifier. By a large degree, the dominate pole is at the output:

$$f = \frac{1}{2\pi C_L R_{TH}} \tag{4.8}$$

where C_L is the load capacitance and R_{TH} is the same as found above in the gain calculation. The gain-bandwidth product, and therefore the unity gain frequency, is therefore:

$$G * BW = \frac{g_{m12}R_{TH}}{2\pi C_L R_{TH}} = \frac{g_{m12}}{2\pi C_L} \tag{4.9}$$

The other major pole is at the source of M18 (M19). The time constant is approximately:

$$\tau_2 = \frac{C_{18}}{g_{18}} \tag{4.10}$$

where C_{18} corresponds to the capacitance at the source of $M_{18,19}$. This is the pole that determines the bandwidth of the system since it determines the phase margin at unity gain.

Figure 4-5 and Figure 4-6 are bode plots of the forward transfer function. This represents a gain of 100,000, a unity gain bandwidth of 16.4MHz and a phase margin of 69 degrees.

4.3.3 Noise Performance

Chopping circuitry, or in the case of the preamplifier, correlated double sampling, is used to eliminate 1/f noise from the amplifier. The major noise source of consideration is therefore the broadband thermal noise.

The thermal noise of a MOSFET in saturation can be modeled as with equivalent input noise:

$$v_{eqMOS}^2 = 4kT\frac{2}{3g_m}\Delta f \tag{4.11}$$

The equivalent input noise of the operational amplifier can be found by adding the effect of the input noise power of each of the devices, referred back to the input. The dominant transistors are the input transistors M12 and M13 and the current source loads M20 and M21. Noise from the other transistors in the signal path is divided by

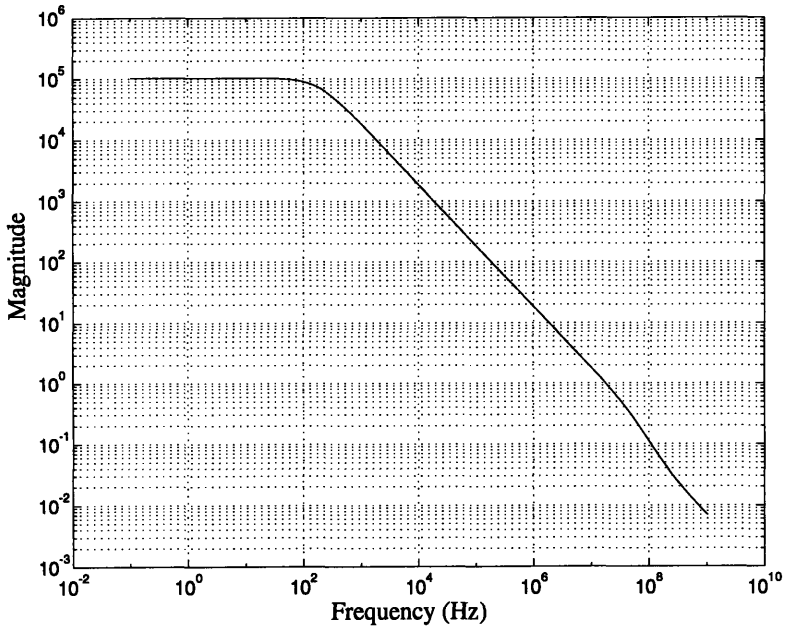

Figure 4-5: Forward Transfer Function Gain

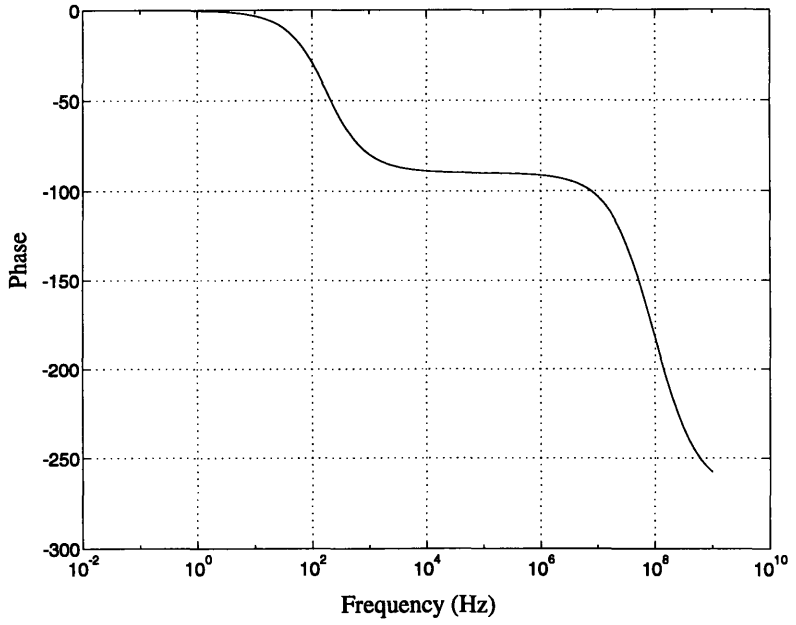

Figure 4-6: Forward Transfer Function Phase

the first stage gain.

$$v_{eq}^2 = 2(4kT\frac{2}{3g_{m12}} + (\frac{g_{m20}}{g_{m12}})^2 4kT\frac{2}{3g_{m20}}) \tag{4.12}$$

$$v_{eq}^2 = 2(4kT\frac{2}{3g_{m12}} + (\frac{g_{m20}}{g_{m12}^2})4kT\frac{2}{3}) \tag{4.13}$$

The larger the g_m of the input devices M12 and M13, the lower the noise power. Decreasing the equivalent input noise requires burning power in the input leg.

From a noise perspective, the current load devices, M20 and M21, should be biased with a low g_m, and therefore a low W/L for a given current. This is in opposition to the biasing requirement the other transistors (M12, M13, M18, M19, M16, M17), which should be biased at the threshold to maximize the intrinsic voltage gain. R_{out}, but not g_m, of devices M20 and M21 are important for the gain of the amplifier, so these two biasing requirements are not in opposition.

Therefore, to minimize noise and thus power usage, M20 and M21 should be biased in strong inversion. The W/L can not be made infinitely small because there is a pole in the current mirror[22]. In addition biasing these devices in inversion will lower the output swing of the operational amplifier, which is important for the sigma-delta modulator.

4.3.4 Dynamic Range

For a high gain, the transistors in the output leg must remain in their saturated region. When the output is too high or low, transistors M18, M19, M17, and M16 will be forced into their ohmic region and the gain is reduced. The differential output swing of the circuit with a 3 Volts supply ranges from -1.5 to 1.5 Volts, or a 3 Volt differential output swing. Biasing devices in weak inversion increases the output swing.

4.4 Common-mode feedback

Common mode feedback is necessary to keep the common mode at the output at the desired bias level. Without such feedback, the gain of the amplifier is so high that the inevitable small discrepancies between the design and actual circuit will cause the output to saturate.

There are several ways to implement common mode feedback. One is through capacitive refreshing [23]. This, however, requires 4 capacitors on the order of a picofarad, which consumes area. Szajda used a different technique, as demonstrated in his thesis.[4] In this technique, two differential transistor pairs are used to compare the output nodes to a common mode. The current from the differential pairs join at their source. If the common mode at the output does not equal the desired common mode, the mismatch in current is mirrored back to the output leg. This technique of common mode feedback takes 40% of the current for the total operational amplifier. If the current were reduced, the differential mode range of the feedback would be reduced.

Figure 4-7 shows another method of common mode feedback. In this scheme, two transistors, M9 and M10, biased in their ohmic region, are placed above the biasing transistor of the input stage. It is also possible to have the pair of transistors in the ohmic region are placed in the output leg, either above as PMOS or below as NMOS. [16] Placing the ohmic transistors in the input leg has the advantage of trading output swing for input common mode swing. This was chosen since the input common mode range is not required to be large.

M9 and M10 act as negative feedback for the common mode. The two outputs of amplifier are fed back into the gates of these two transistors. These two transistors are in their ohmic region of operation. The relevant parameters for this mode of

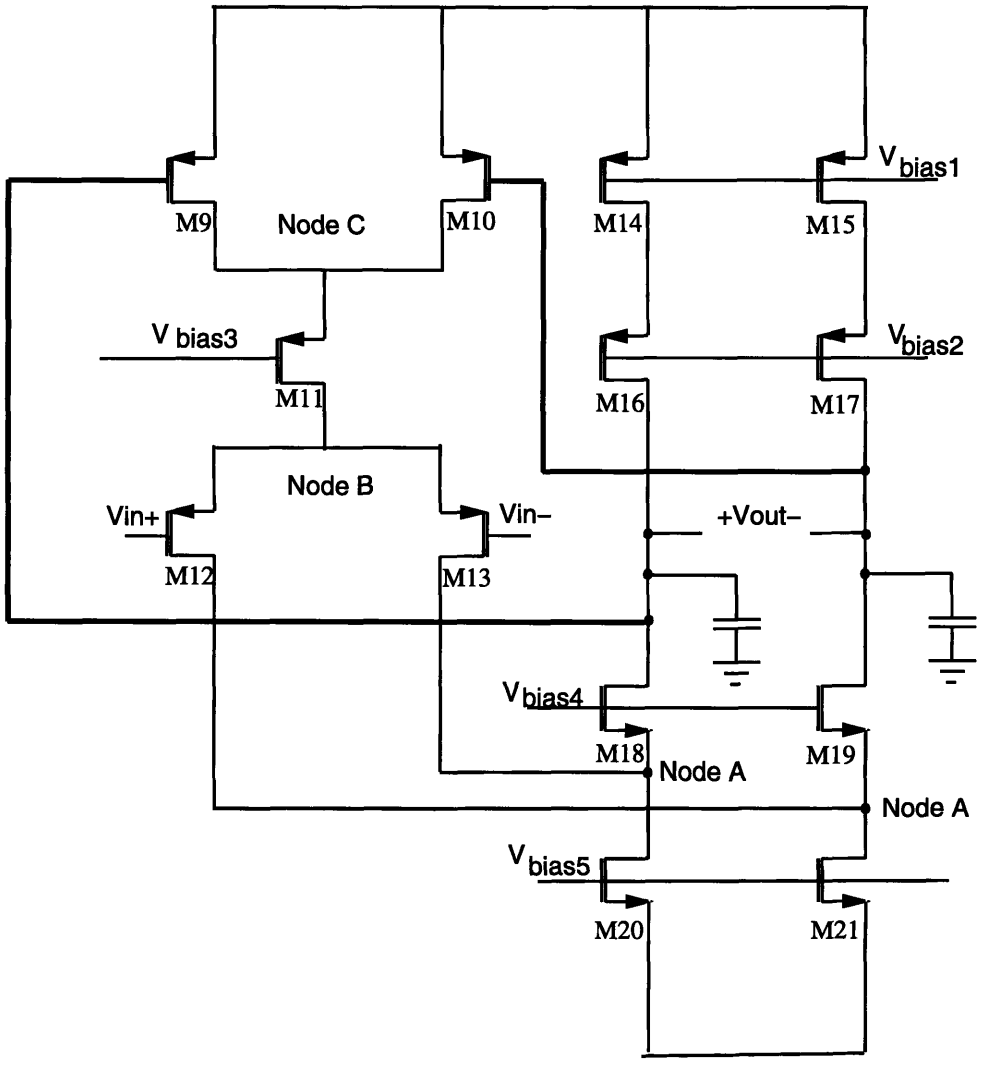

Figure 4-7: Common Mode Feedback

operation are:

$$I = \frac{W}{L}\mu C_{ox}(V_{gs} - V_{th})V_{DS} - \frac{V_{DS}^2}{2} \tag{4.14}$$

$$g_m = \frac{W}{L}\mu C_{ox}V_{DS} \tag{4.15}$$

$$R_o \approx \frac{1}{\frac{W}{L}\mu C_{ox}(V_{GS} - V_{TH})} \tag{4.16}$$

To look at the gain of this feedback loop, we open the loop. The loop is opened between the outputs of the amplifier and the gates of M9 and M10. We then find the common mode gain from the gates of transistors M9 and M10 to the output. First, assume that the differential output is 0 Volts, so M9 and M10 look identical. I_{SC} is found by grounding the output applying a common mode voltage at the inputs. Figure 4-8 diagrams the small signal model used to find I_{SC}. In this diagram, the simplified small signal models from Figure 4-2 are used.

Three steps are used to simplify the model. In 4-8a is the small signal representation from Node A to the output. Since $R_{o20} >> \frac{1}{g_{m18}}$, then:

$$R_a \approx \frac{1}{g_{m18}} \tag{4.17}$$

If 4-8b, the small signal model is from Node B to ground. Since $R_a << R_{o13} and R_{o13} >> \frac{1}{g_{m13}}$:

$$R_b \approx \frac{1}{g_{m13}} \tag{4.18}$$

Finally, 4-8c represents the full small signal path. Since $R_b << R_{o11} and R_{o11} >> \frac{1}{g_{m11}}$.[5]

$$R_c \approx \frac{1}{g_{m11}} \tag{4.19}$$

[5]Another way of viewing this derivation is that M18, M19, M12 and M13 are common source amplifiers with a current gain of approximately 1.

From this circuit, I_{SC} is:

$$I_{SC} = V_{cm} g_{m9} \frac{R_{o9}}{R_{09} + \frac{2}{g_{m11}}} \tag{4.20}$$

R_{th} is the same R_{th} found for the forward transfer function of the operational amplifier. I_{SC} of the common mode feedback is smaller that the I_{SC} of the forward transfer function for two reasons. First, the g_m of the transistors in their ohmic region is about an order of magnitude smaller (4x10-5 compared to 4x10-4). Second, because R_o of the ohmic resister is relatively small (10kΩ) compared to 3kΩ (1/gm). Thus, all the current generated in M9 and M10 does not pass through M11.

The major poles of the feedback are the same as the dominant pole of the forward transfer function. The gain of the feedback loop is about 7.5% of the overall gain of the amplifier. Since the low frequency gain of the feedback loop is lower, the crossover frequency will be lower as well, which guarantees stability.

For a small signal, the differential gain for the common-mode feedback is zero because the two transistors, M9 and M10, will have a $g_m v_{gs}$ of equal and opposite magnitude. More important is the large signal characteristics, because the common mode should not change drastically with the varying differential output. The derivative of the transistor current shows that the current is linearly related to V_{GS} when the transistor is in its ohmic region. Thus for a large signal differential output voltage, the current gain of one will be balance by a current decrease of the another.

$$\frac{\partial I}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} V_{DS} \tag{4.21}$$

Thus, the feedback action is limited to when M9 and M10 remain in their ohmic region. In saturation, the change in current through the device is no longer independent of V_{GS}:

$$\frac{\partial I}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - Vth) \tag{4.22}$$

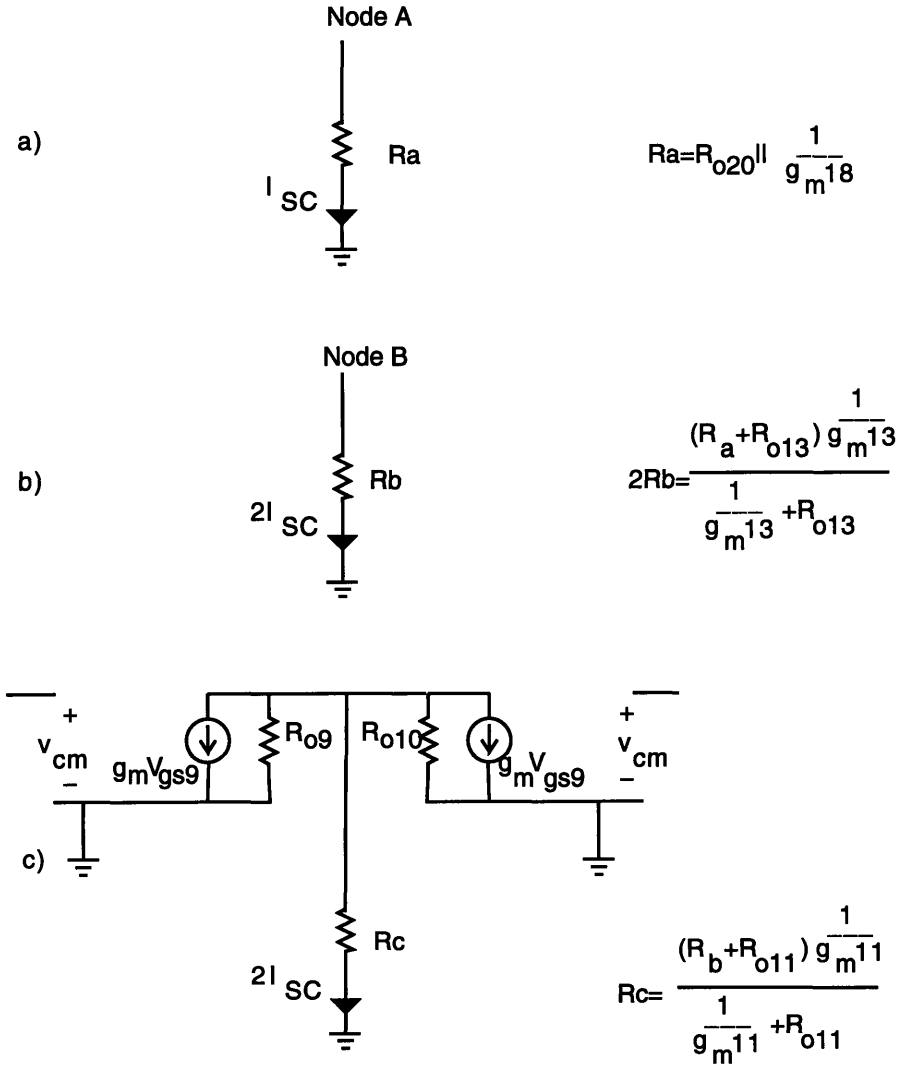

Figure 4-8: Common Mode Feedback Small Signal

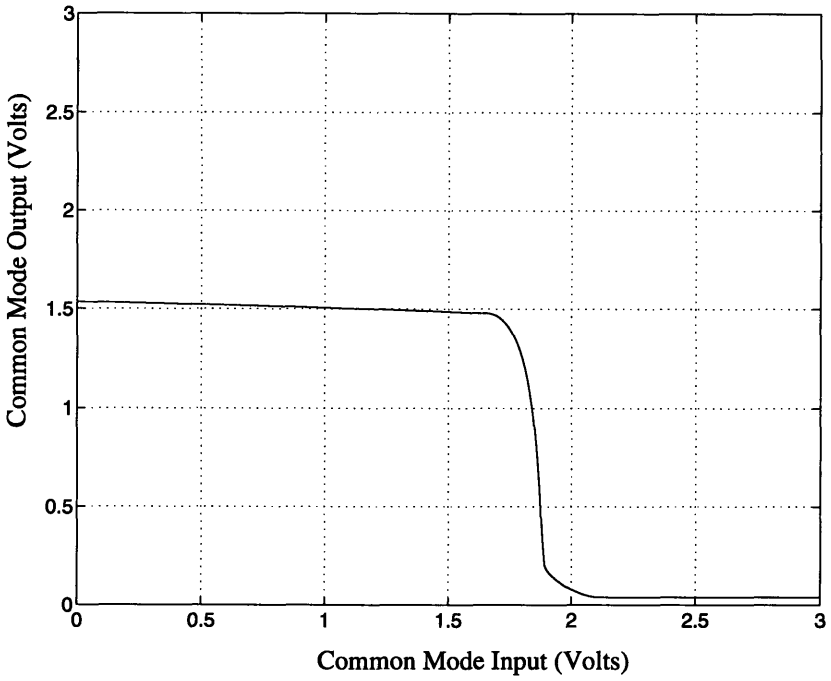

Figure 4-9: Common Mode Output Versus Common Mode Input

Once the output swing puts one of these transistors in saturation, its current no longer linearly varies with V_{GS}. Current changes in M9 and M10 induced by a larger differential voltage will not be balanced, and the common mode output voltage will vary with differential output voltage to compensate. For this reason, V_{DS} of M9 and M10 is kept low (.2 Volts) so that the transistors remain in their ohmic region as long as possible. SPICE simulations have verified that the common-mode output voltage varies by only a small amount (20μV) throughout the differential output range of interest.

The value of the common mode relies on M11 remaining in saturation. If the input common mode is too high, the voltage at the source of M11 will begin to increase. M9 and M10 respond to their decreased V_{DS} voltages by lowering the common mode. Figure 4-9 shows the relation of common mode output to common mode input.

4.5 Biasing

If V_{bias3} is a constant voltage, the common mode biasing in Figure 4-7 is very sensitive to both absolute device parameters and current values of M9, M10, and M11. For example, if the current through M11 is more than designed, the common mode voltage will more than designed for two reasons. First, the voltage at the drain of M9 and M10 will be increased because there is more current through M11. Second, more current flows through M9 and M10. The result of both of these is a rise in the common mode voltage beyond the designed value.

The operational amplifiers are self-biased on the sensor chip. Typically self biasing current sources are nominally accurate to only 20%. In addition, the current value varies with temperature. Figure 4-10 shows the value of the common mode when V_{bias3} is constrained to a constant value and the current in the first stage of the operational amplifier changes from 18.5μA to 20μA. This change in bias current, about 10%, is typical for a temperature range of 30 to 50 °C. In this case, the change in the common mode is 50 mV. When using a small voltage supply (3 V), it is necessary to construct a biasing scheme insensitive to absolute parameters of the circuit to preserve output swing.

4.6 Complementary Biasing

A new self-biasing circuit was designed to "mirror" the structure of the common mode feedback, while establishing a biasing current (See Figure 4-1, the main circuit diagram). Because the ratio of $\frac{W_9+W_{10}}{L_{9,10}}$ to $\frac{W_2}{L_2}$ is the same as the ratio of $\frac{W_{11}}{L_{11}}$ to $\frac{W_4}{L_4}$ (N_3 in both cases), the voltage at the gate of M9 and M10, when everything is matched, will be the same as the voltage at the gate of M2. Therefore the common mode at the output will track the value of VCMREF. Figure 4-11 shows the result of

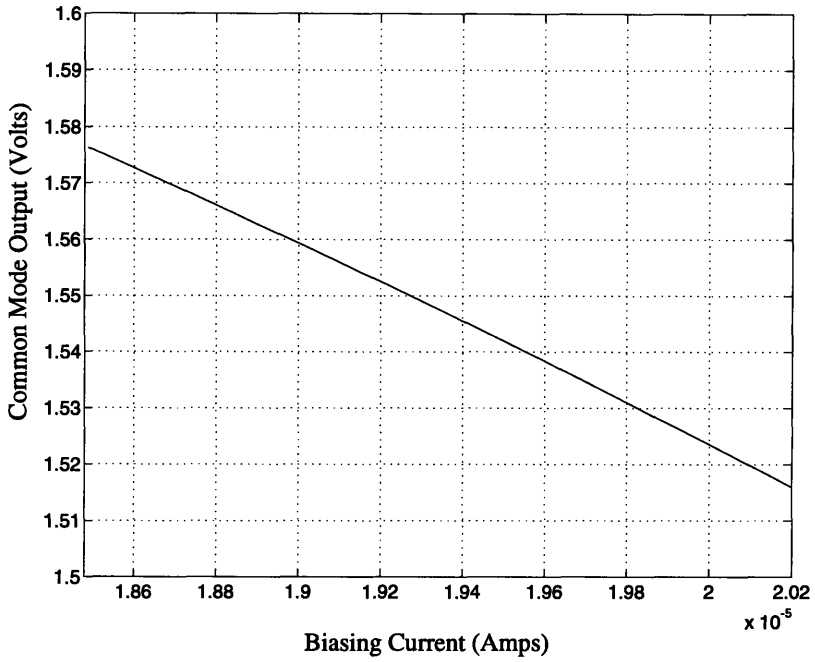

Figure 4-10: Common Mode Output Versus Input Current

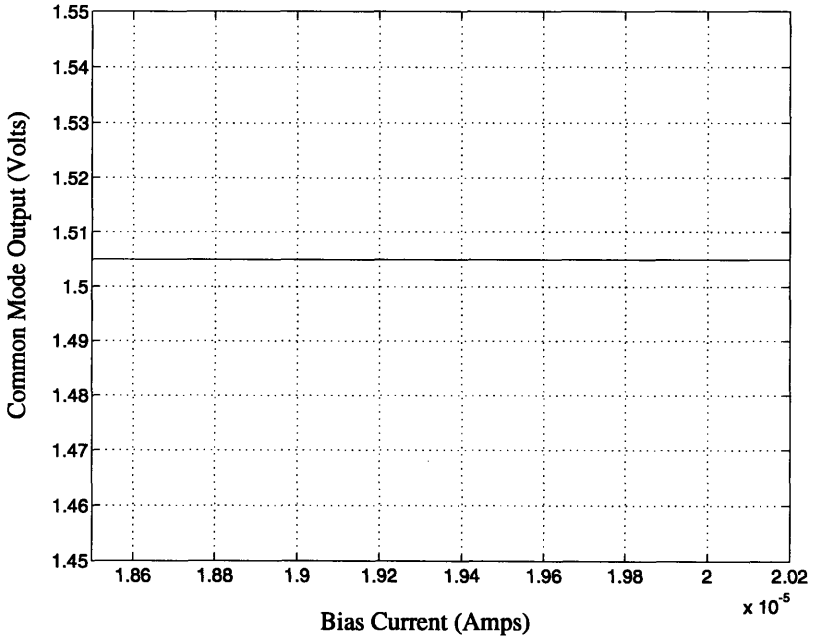

Figure 4-11: Common Mode Output Versus Temperature with Complementary Biasing

improvement. Here, a temperature variation of 30 to 50 °C will still cause a current variation through M9 and M10 of 18.5 to 20 uA. However, because V_{bias3} adjusts to this change, the common mode output voltage remains essentially constant.

The transistors determining biasing the current are shown in Figure 4-12. As in most voltage independent biasing circuit, a loop is formed in which the size ratios of the transistors determine unique solutions. Transistors M7 and M8 are a current mirror, which forces the current through both legs to be equal. M1 is ratioed to M2. Because these transistors are in their ohmic region, they can be treated as resistors of value R and N_2R. The voltages from the power supply to the gate of M3 and M4 must be equal:

$$IRN_1 + V_{gs3} = IR + V_{gs4} \tag{4.23}$$

$$IRN_1 + \sqrt{\frac{IL}{KWN_2}} + V_T = IR + \sqrt{\frac{IL}{KW}} + V_T \tag{4.24}$$

$$IR(N_1 - 1) + \sqrt{I}(\sqrt{\frac{L}{KWN_2}} - \sqrt{\frac{L}{KW}}) = 0 \tag{4.25}$$

Solving for I:

$$I = 0 \tag{4.26}$$

$$I = (\frac{\sqrt{\frac{L}{KWN_2}} - \sqrt{\frac{L}{KW}}}{R(N_1 - 1)})^2 \tag{4.27}$$

The first possibility, I=0, is prevented by the circuitry in the left of Figure 4-12. If the current is zero, the drain of M3 will be at the positive rail, thus forward biasing the diode and conducting current. When I is set by the second solution, this diode is reverse biased and conducts no current.

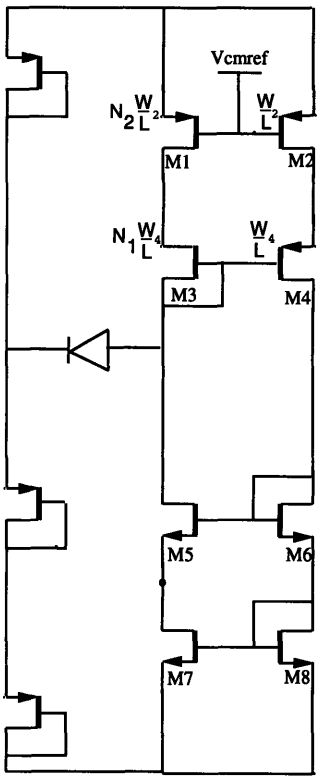

Figure 4-12: Operational Amplifier Biasing

4.7 Design Implications for Power

Since common mode feedback uses only the current available in the input leg of the transistor, the power considerations remain to choose the currents in the two output legs.

The current in the output leg is chosen to limit the slewing time to less than 10% of the clock cycle. This will allow 90% of the clock cycle for linear settling . The maximum rate of voltage change required at the output of an amplifier is in the preamplifier, where a signal must move from the initial common mode voltage to its maximum final value of 1 Volt during one half a clock cycle.(7.6μs) An upper bound on slewing time is determined by assuming that the capacitor reaches its final value solely by slewing. If slewing were limited to .76 μs, or the first 10% of the half cycle, this would require a slew rate of at least 1.31 V/μs. With a 10 pF load, the output current in each leg must be at least 6.6μA.[6]

Low current in the input stage favors a high gain. However, lower currents lead to a low g_m in the input devices, and therefore a higher equivalent input noise. Current through the input stage must be high enough to meet the noise requirement.

These design requirements determine the lowest power necessary to meet the design specification. The rest of the design involves meeting a gain/bandwidth tradeoff. The areas of the transistors can be increased, increases device lengths and R_{out}, thereby increasing the gain. However, larger device sizes will decrease the value of the bandwidth determining time constant at the source of M16 by adding extra capacitance to this node. G_{m16} may by increased by biasing M16 at a higher threshold voltage. This will increase the bandwidth, but will lowerthe gain.

The following table summarizes important parameters in the operational amplifier.

[6]The actual current in the output legs is 8uA, which is an overdesign for the system requirements reported in this thesis. This was based on a sigma-delta design for adequate noise shaping at 50Hz.

	Old Implementation	New Implementation
DC Gain	110000	100000
Unity Gain Bandwidth	16.4 MHz	16.4MHz
Phase Margin	69°	69°
Power Supply	6V	3V
Differential Output Swing	8V	3V
Power Dissipation (excl. ref. current)	560 uW	175uW
Power Dissipation (incl. ref. current)	1.56mW	425 uW

Table 4.1: Operational Amplifier Characteristics

Chapter 5

Layout

The major constraint on the layout is that the chip must fit inside a 22 gauge needle. Allowing room for inaccuracies due to sawing, the allowable width for the chip itself, including bus wiring is 580 microns. A strategy was developed to reduce the length of the design.

SubCircuit	Number	Width (microns)
Pads	2	280
Sensor (without Op Amp)	1	450
OpAmp	5	240
Pre Amplifier Capacitors	1	280
Modulator Capacitors	3	570

Table 5.1: Summary of Layout Components

The whole chip is divided into subblocks. Each subblock has a vertical axis of symmetry, with matched devices next to each other along this axis. The minimum length is achieved when the devices have the same length and the width of the chip is fully utilized. Therefore, no area is wasted.[1] This layout strategy for a single subblock

[1] A similar scheme could be used with a horizontal axis of symmetry. The transistors would be

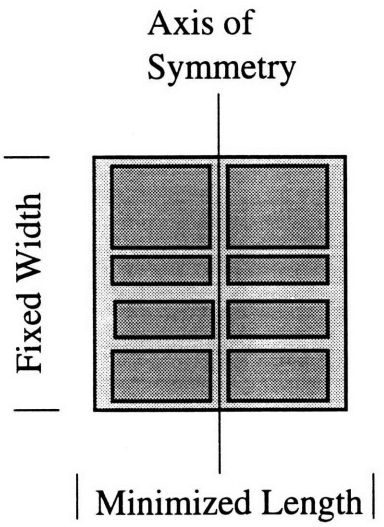

Figure 5-1: Layout Strategy

is demonstrated in 5-1.

In addition to using this scheme, reductions in area resulted from removing two of the seven operational amplifiers, reducing bus lines, combining some clock generation circuitry, and removing excess capacities of the digital circuitry (i.e., the enables). A schematic of the overall layout appears in 5-2.

The size of each subunit is reported in Table 5.1. Overall, the previous designed measured 8300 microns. The new pass measures 3930 microns, an improvement of about 50%.

sized to reach the maximum width, minimizing the length. However, the fixed chip width of 580 microns is much larger than the maximum dimension of most of the transistors.

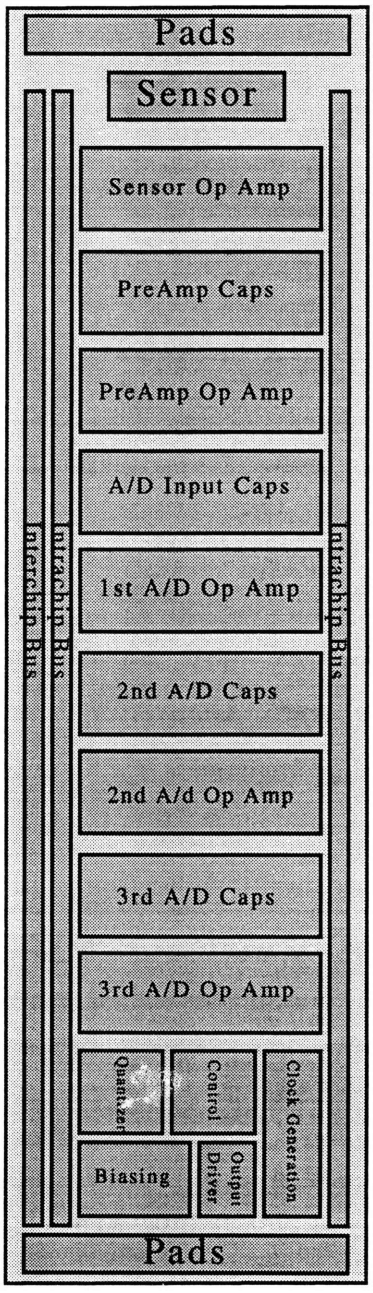

Figure 5-2: Layout

Chapter 6

Peripheral Circuits

6.1 Sensor Selection

Since each needle contains several sensor chips, a control mechanism is needed to select the proper sensor to operate. Control of the needle is handled with a shift register (Figure 6-3). The shift register is split between the sensors, so that each has a bit, or D-latch on each chip.[24] Each D-latch will pass the input signal, S, to the output, Q, when the clock inputs shifts from high to low.[1] Two pins are used: the clock input to the register is controlled with Vref, making dual use of this pin as a reference voltage for the modulator and a control bit. The control signal is sent through a separate pin, AD0. The scheme has the capability of controlling an unlimited number of sensors with only one extra pin, AD0, needed for addressing. Fewer pads simplifies bonding, greatly easing the manufacture of needle.

To control the system, a signal is put on AD0. Lowering Vref triggers the shift register. The input signal on AD0 moves to the output of the first edge triggered flip flop. Since the output of the first chip is the input to the second, the second chip

[1] For a review of these building blocks, refer to [25].

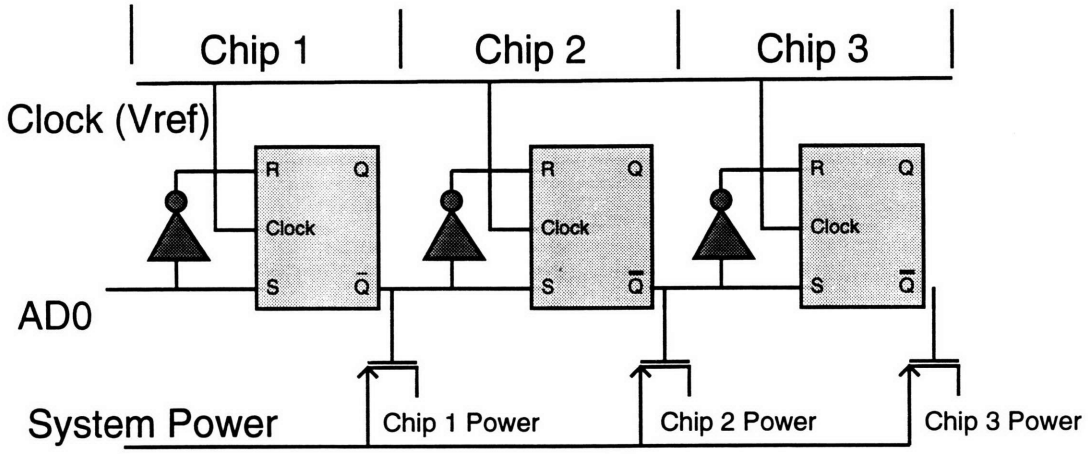

Figure 6-1: Shift Register

now stores the previous value of the first chip. The other bits are similarly shifted. Proper on/off codes for all the chips can be communicated by the following scheme: send the signal for the last chip to AD0, lower Vref, raise Vref, send the signal for the second to last chip to AD0, lower Vref, raise Vref, and so forth until the bits have all moved into position.

On each chip, the output of the edge triggered flip flop,Q, controls the power connection of that sensor by controlling the state of a PMOS transistor. When the output is low, the chip power is connected to the power pin and the sensor is active.

6.2 Output Driver

The output of the comparator in the A/D converter is driven off the sensor chip through a series of inverters. Because the output pins of all the sensors are connected together, inactive sensors must not load down the active sensor. In addition, the comparator output is guaranteed to be a valid logic high or low only when phi is low. To prevent excess static power dissipation, the output must be isolated from the inverter during half cycle when phi is high.

Figure 6-2 is the output driver. M1 and M3 form an inverter from the quantizer output to the chip output, while M2, M4 and M5 are switches. When the sensor is on, the chip power is high and the control bit (the same bit that controls the sensor power,) is low. M4 will be on (Figure 6-2a).

When the chip is active and phi is low (Figure 6-2b), M2 is on and M5 is off, so the driver performs as an inverter. When phi is high (Figure 6-2c), M2 is off and M5 is on, connecting the output to ground. The driver does not burn power regardless of the quantizer output.

When the sensor is off (Figure 6-2d), the clock output is grounded and chip power is isolated. The driver is therefore isolated from the power supplies (Figure 6-2e). Therefore, the inactive sensor chips do not load the output of the active chip on the needle.

6.3 Control Chip

The needle has to have the capability to drive high capacitance lines. Instead of a large driver on each sensor, a control chip is used for this purpose.[2]

[2]This chip may also be used to control the on/off state of the sensors, as it was in the first generation design. [4] In this design, the control chips pass the control bits directly to the first sensor chip.

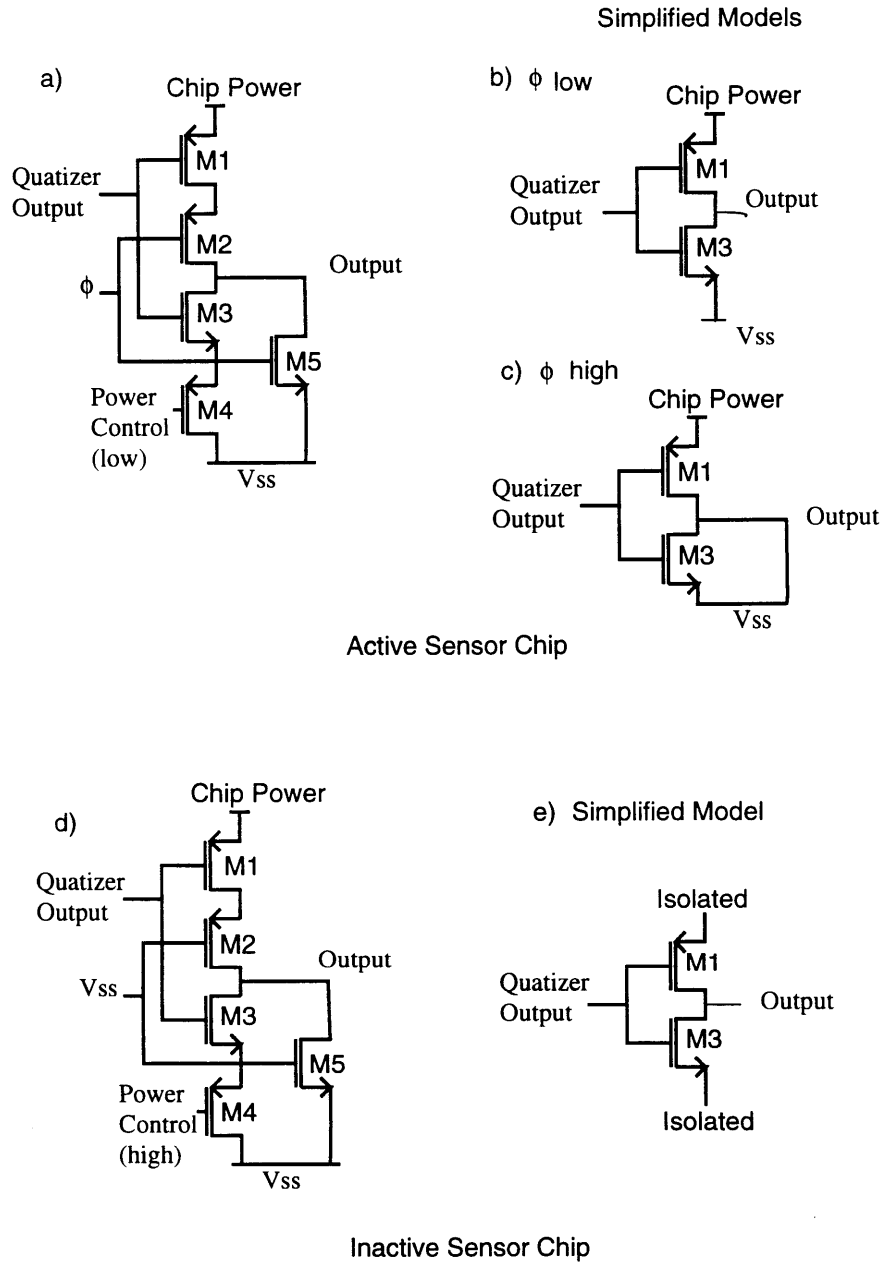

Figure 6-2: Sensor Output Buffer

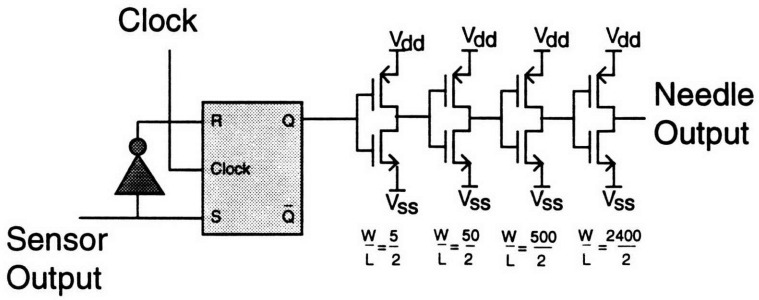

Figure 6-3: Controller Chip

The output from the sensor chip is fed into the control chip. This output is buffered with an D-Latch. The signal is driven off-chip through a series of upwardly scaled transistors. Each inverter provides the driving power for the next, larger inverter. The last inverter, is very large to drive the capacitance of the output line.

6.4 ESD Protection

The gates of MOS devices are extremely susceptible to ESD, or electrostatic discharge damage. The peak value of ESD pulses can be several kilovolts, well over the 15-20 Volts that would damage the gates. To protect against accidental damage, simple ESD protection is provided.(Figure 6-4)[26] If the voltage on a pin is forced more than a

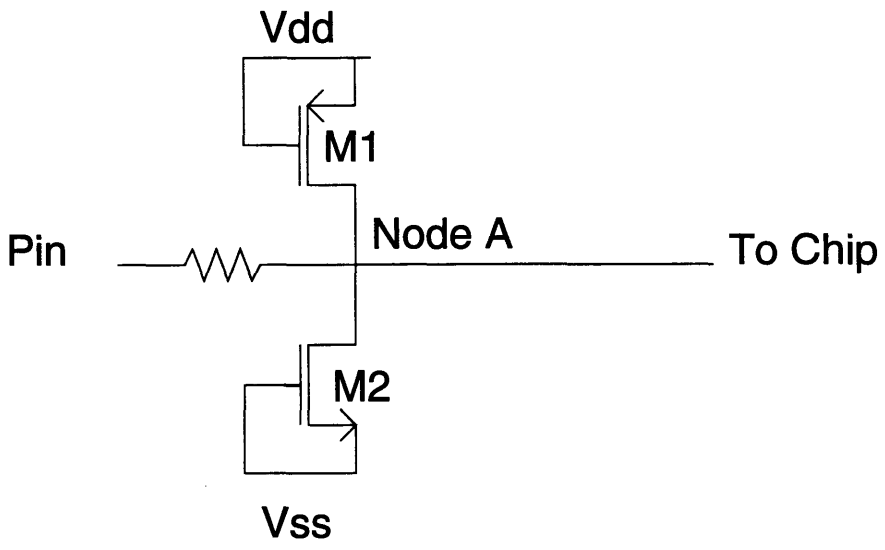

Figure 6-4: Chip Protection

threshold voltage above Vdd, M1 will turn on and drive node A to V_{dd}. Similarly, if the pin voltage is more than a threshold voltage below Vss, M2 will turn on and drive node A to ground. The resistor also provides high current protection through a drop in voltage.

Chapter 7

Decimation

Since the A/D converter is incorporated on the needle, the information received from the instrument will be a digital bitstream. As explained in Chapter 4, these bits contain information at individual frequencies. High frequencies contain quantization noise as a result of the noise shaping in the A/D converter. The lower frequencies have the information of interest. With proper filter design, this bit stream can be low-pass filtered to extract signal information much higher than 1 bit.

The signal out of the modulator and is sent through a serial port to a DSP board. The DSP board (TMSC31) inside the PC will process the bits, and send the information to the PC for display. The filter coefficients used by the DSP board is quite flexible, as they can be loaded from a text file at the time of measurement, so different processing can be used for different sampling speeds.

Since only the lower frequencies contain important information, the sampling rate may be reduced after the filtering is done. Therefore, with a clock speed of 65 kHz, reduction the sampling rate by 1000 would retain information at 1 Hz. If an FIR filter is used, filtering and down-sampling may be done in the same step. For example, if you are downsampling by a factor of 1000, the filter output only has to be calculated

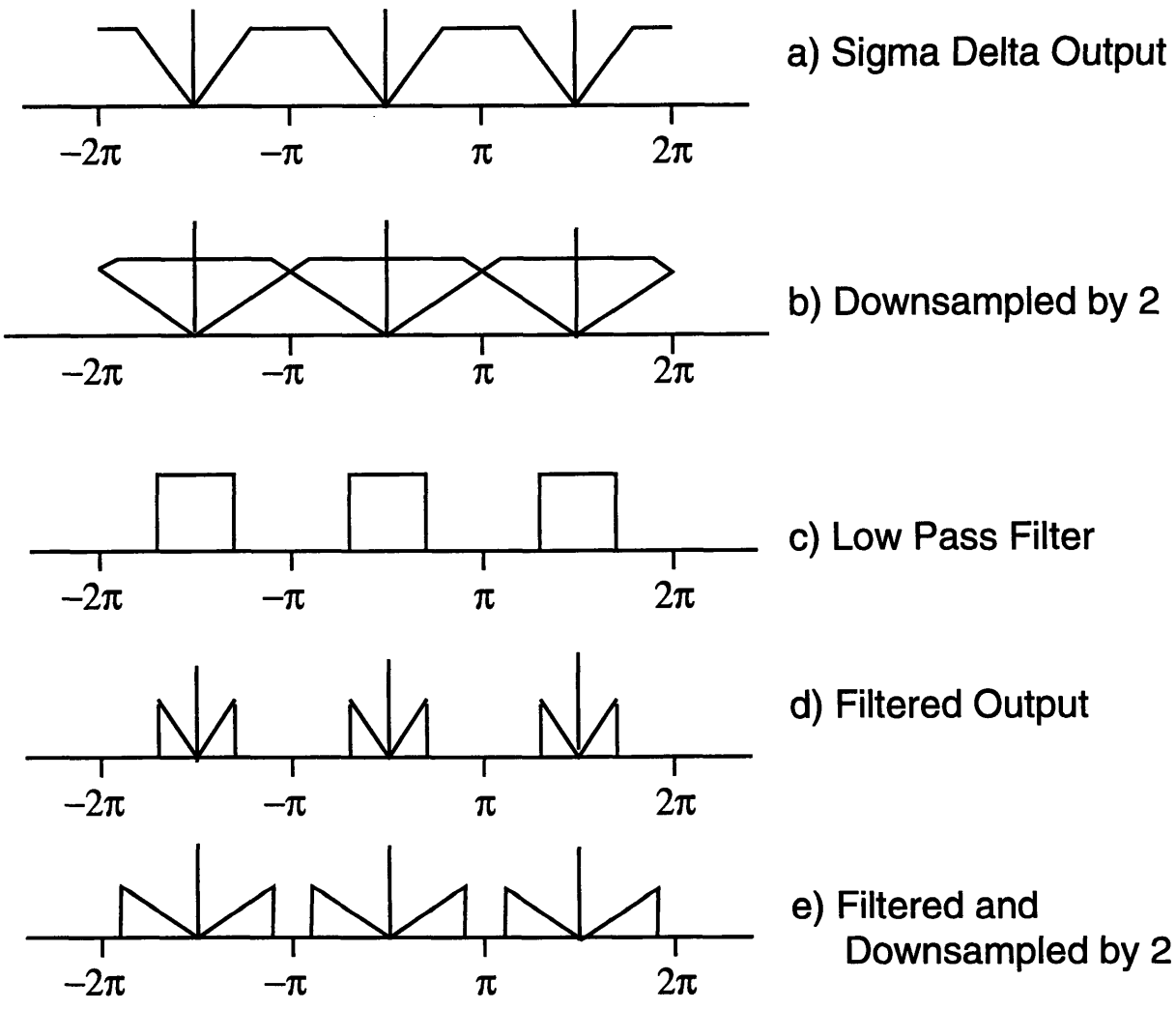

Figure 7-1: Filtering and Downsampling

every 1000th step. This is a considerable reduction in the speed requirement of the signal processing.[27]

The major caution in using downsampling is aliasing. Figure 7-1 demonstrates this point. Figure 7-1a is a typical spectrum of signals at the output of the needle. There is a signal near DC, with considerable noise at high frequency. Because this is a discrete-time system, the spectrum repeats every 2π.

Figure 7-1b shows the effect of downsampling by a factor of 2. Because only frequencies up to half the sampling rate can be represented uniquely, the spectrum must overlap when this sampling rate is decreased. The once accurate spectrum at DC now contains a large amount of noise. If the system had been downsampled by 1000, DC would contain 1000 overlapped spectrums.

Figure 7-1c shows a low pass filter that can solve this problem. When the high frequencies are first filtered before downsampling 7-1d, aliasing will be prevented Figure 7-1e. The fully aliased signal must below 118 dB to maintain an accuracy of 18.3 bits. When the output is downsampled, approximately 1000 more copies from the original signal at this frequency will be at DC. Since the signal aliased approximately 1000 times, this requires 60 dB more of prefiltering. In this case, any frequency above 32.5 Hz must be filtered at least 178 dB before downsampling.

Chapter 8

Conclusion

This thesis has described design changes made to a temperature sensor that will facilitate the measurement of perfusion. The major goals were to lower the area and power dissipation in the system.

8.1 Summary of Accomplishments

Overall the size of the chip was reduced in length from 8300 to 3930 microns, or about 50%. Size was reduced by:

- Adoption of a layout strategy for a fixed width layout
- Combining some of the clock generation
- Eliminating duplicated bias lines
- Removing excess capacities of the digital circuitry
- Reduction from 7 Operational Amplifiers to 5 due to reduction of Sigma Delta A/D converter from 4th order to 3rd and a change in architecture

The power in the circuit was reduced from 4.92 mW to .94 mW, about an 80% reduction. Major methods of reduction are:

- 40% Reduction in Operational Amplifier current due to common-mode feedback change
- Reduction from 7 Operational Amplifiers to 5 due to reduction of Sigma Delta A/D converter from 4th order to 3rd and a change in architecture
- Further reduction in input current of 2 of the 3 operational amplifiers in the A/D converter due to relaxed noise constraints
- 50% Reduction in biasing current to compensate for load of the biasing
- Reduction of the power supplies from 6 to 3 Volts.

In addition, other accomplishments are as follows:

- Control of the chips was simplified and now has the capacity of controlling an unlimited number of chips without changing the circuitry
- Elimination of three input pads from the needle, which will allow the pad size to be enlarged and which will ease bonding
- Modification of the output driver on the sensor to prevent inactive sensors from loading the output line
- Addition of a very large output driver to the controller to drive high capacitances off chip
- Increase in the driving capacities of the clock circuits
- Addition of electrostatic discharge circuitry to protect device gates

- Construction and programming of a decimation scheme to facilitate real-time decimation of the signal

8.2 Future Work

These circuits are currently being fabricated using the BioCMOS process developed at MIT. This flow is a derivative of the CCD/CMOS process developed by Dr. Craig Keast [28] and modified by Dr. Kenneth Szajda.[4] Upon completion, the system will be tested, incorporating real-time decimation.

Future work on this project will focus on perfusion sensing. To quantify perfusion, the power needed to apply at temperature step to the sensor will be measured. Heating and power sensing circuitry will be added to the sensor. Control of this measurement system will require a feedback between the measured temperature and power application to the chip. Figure 8-1 diagrams a proposed system combining the needle sensors, a DSP processing board, and a personal computer. The personal computer is the center for control. The personal computer selects a sensor and controls the amount of power applied to the heaters. Sensors on the needle measure temperature and total power consumption on the chip. The sensor output is fed directly to a DSP processor, which perform necessary signal processing. The processed data is then sent to the personal computer for presentation and appropriate control decisions.

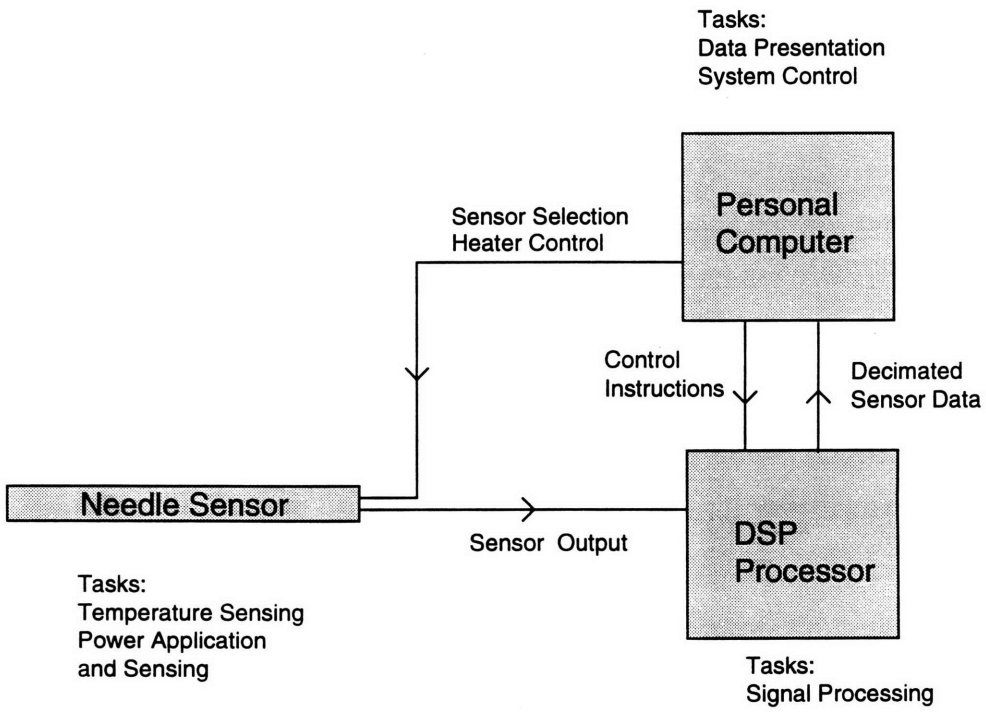

Figure 8-1: Proposed Perfusion Measurement Sytem

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