A Comparator-Based Switched-Capacitor Pipelined Analog-to-Digital Converter

by

John K. Fiorenza

B.S., University of Notre Dame (1999)
S.M., Massachusetts Institute of Technology (2002)

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Signature of Author .....
Department of Electrical Engineering and Computer Science
March 14, 2007

Certified by .....
Hae-Seung Lee
Professor of Electrical Engineering
Thesis Supervisor

Certified by .....
Charles G. Sodini
Professor of Electrical Engineering
Thesis Supervisor

Accepted by .....
Arthur C. Smith
Chairman, Department Committee on Graduate Students
Department of Electrical Engineering and Computer Science

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Abstract

A new comparator-based switched-capacitor(CBSC) technique is proposed that eliminates the need for high gain op-amps in switched-capacitor circuits. The CBSC technique replaces the op-amp in switched-capacitor circuits with a comparator and a current source. Compared to op-amps, comparators suffer less from the negative effects of scaled CMOS. The technique is applicable to a broad class of sampled-data circuits including analog-to-digital converters, digital-to-analog converters, sample-and-holds, integrators and filters. As a proof of concept the technique is demonstrated in the design of a pipelined analog-to-digital converter. The prototype CBSC 1.5 b/stage pipelined ADC implemented in a 0.18 µm CMOS process operates at 7.9 MHz, achieves 8.6 effective bits of accuracy, and consumes 2.5 mW of power.

Sources of offset and nonlinearity are identified and analyzed. The analysis reveals the potential of the CBSC technique for lower power dissipation and provides design guidelines for energy efficient comparator-based switched-capacitor circuit design.

Thesis Supervisor: Hae-Seung Lee
Title: Professor of Electrical Engineering

Thesis Supervisor: Charles G. Sodini
Title: Professor of Electrical Engineering

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Looking back at my time at MIT what I will remember most vividly, more than the time I spent working on research or the time spent studying for classes will be the time I spent with the people I met at MIT. Given that my time here has been large portion of my adult life, this is not surprising. This is also not surprising, given that a vast majority of what I learned here technical or otherwise was taught to me by someone I met along the way. All of these people deserve the credit for whatever I achieved here and for all that I take from this place.

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Chapter 1

Introduction

The needs of large digital systems have driven the development of modern scaled CMOS processes. Process advances such as lower power supplies and shorter gate lengths which lead to lower power consuming, faster digital circuits can also lead to higher power consuming, lower performance analog circuits. Although the higher f_Ts of scaled devices can be used to increase analog performance, other process characteristics such as reduced transistor output resistance and lower supply voltage make the design of op-amps, a fundamental analog building block, more challenging. Traditional analog design techniques require op-amps with very high gain to achieve accurate results. The objective of this work is to develop a comparator-based switched-capacitor technique that removes the need for op-amps in switched-capacitor circuits.

1.1 Motivation

The persistent advance of CMOS process technology which has enabled unprecedented performance advancement of digital integrated circuits has also created many new challenges in the design of analog integrated circuits. Analog designers have been able to overcome the challenges of modern CMOS technology in order to take advantage of its inherent advancement. As CMOS continues to scale this will become more and

more difficult.

One of the most important design challenges posed by CMOS scaling is the design of high gain operation amplifiers (op-amps). Op-amps are essential analog building blocks. They often limit the performance integrated systems. Often the gain of the op-amp will limit the accuracy of the analog system and the bandwidth of the op-amp will limit the speed of the system. One specific example is the pipelined analog-to-digital converter. The gain of op-amps contained in the input sample-and-hold as well as the pipeline stages will directly limit its accuracy.

Two aspects of CMOS scaling are increasing the difficulty of designing high gain op-amps: smaller gate length and reduced supply voltage.

The ever shrinking gate length of modern CMOS devices is the heart of CMOS scaling. Smaller transistors enable faster smaller digital circuits, but also provide lower output resistance (r_o). Since the $g_m \times r_o$ product of a transistor fundamentally limits the gain of any amplifier, scaled devices produce lower gain op-amps. This effect could traditionally be negated by using longer than minimum length devices in a design. Intrinsic speed (f_T) would be sacrificed for higher intrinsic gain. The output resistance of of a modern digital devices [1] does not increase significantly with increasing length. This effect is due to the pocket implants that are used to maintain gate control of deeply scaled devices. Unfortunately, the output resistance of such devices is primarily determined by the modulation of the energy barrier created by the pocket implant [2–4] rather than by channel length modulation. Increasing the gate length does not significantly effect this mechanism, therefore increasing gate length does not significantly improve output resistance.

Reduced supply voltages are both a feature and requirement of scaling. Using a lower supply voltage enables lower power consumption in digital circuits, but it is also a requirement of using scaled devices. In order to maintain gate control over very small devices it is required that one uses a very thin gate oxide. A low supply voltage must be used in order not to damage this oxide or cause break down in the very short channel. Unfortunately in analog circuits a lower supply voltage usually

leads to higher power dissipation for a similarly performing circuit. A lower supply voltage limits the output swing and consequently causes the signal to noise ratio to decrease. In order to maintain the same signal to noise ratio capacitor sizes must be increased to reduce $\frac{kT}{C}$ noise. The power consumption of the circuit must be increased to drive the larger capacitors at the same speed as the original circuit.

In order to achieve reasonable gain in an amplifier designed in a scaled technology it is often necessary to cascode transistors. The cascoded topology further reduces the already limited output swing.

To address the challenges of scaled CMOS analog circuit design, a new class of comparator-based switched-capacitor circuit topologies is proposed [5, 6], that does not require op-amps in the signal path. The combination of a comparator and a current source replaces the op-amp. Most techniques and architectures used in traditional op-amp based switched-capacitor circuits [7] can also be used in comparator-based switched-capacitor circuits.

1.2 Prior Work

Many different approaches have been taken to address the challenge of designing high gain op-amps in scaled CMOS technology. One alternative to a cascoded op-amp is to cascade several lower gain stages to create an overall high gain op-amp. Stabilizing such an amplifier in feedback becomes problematic. Techniques used to stabilize the amplifier, such as nested Miller compensation [8], require an increased power consumption to maintain the same speed of operation.

Different techniques have been developed to avoid or to compensate for the effects of low op-amp gain. One approach [9] uses a charge coupled device process to avoid the limitation of scaled CMOS. Dynamic amplifiers [10, 11] have been used to avoid explicit operational amplifiers, however, as dynamic amplifiers turn off, their input transistors enter weak inversion causing their outputs to settle very slowly. For low precision applications, parametric amplifiers [12] are another alternative. More

recently, digital calibration has been used to compensate for the poor performance of both low-gain op-amps [13] and open loop amplifiers [14]. Also finite gain compensation techniques have been developed [15, 16] which alter the traditional switch capacitor switching scheme to boost the effective gain of an op-amp.

Analog circuits have been designed in the past using comparators and current sources or voltage ramps. Examples include the dual slope ADC, a time based ADC [17] and a RipSaw ADC [18]. These techniques differ from the proposed technique in that they are specific methods for quantizing signals and are therefore only applicable to ADCs. Comparators have been used in a similar manner to the way they are used in the proposed technique for a low noise reset in imagers [19] and to produce sample-and-hold circuits using discrete components [20, 21].

1.3 Thesis Organization

Chapter 2 provides an introduction to the comparator-based switched-capacitor technique. This chapter explains the basic principle of operation and compares the technique to the standard op-amp based switched-capacitor technique.

Chapter 3 reviews the operation of the pipeline ADC architecture. This describes the 1 b/stage and 1.5 b/stage ADC's and discusses the effect of non-idealities on pipeline ADC performance.

Chapter 4 presents the details of the CBSC prototype 1.5 b/stage pipeline ADC. It outlines the overall design of the ADC as well as discussing the design of selected circuit blocks.

Chapter 5 examines the sources of offset and nonlinearity in CBSC designs and analyzes their effect on circuit performance.

Chapter 6 describes the overall test system including the PCB test board and presents the simulated and measured results of the prototype.

Finally, Chapter 7 summarizes the contributions of this thesis and suggests areas for future work.

Chapter 2

Comparator Based Switched Capacitor Circuits

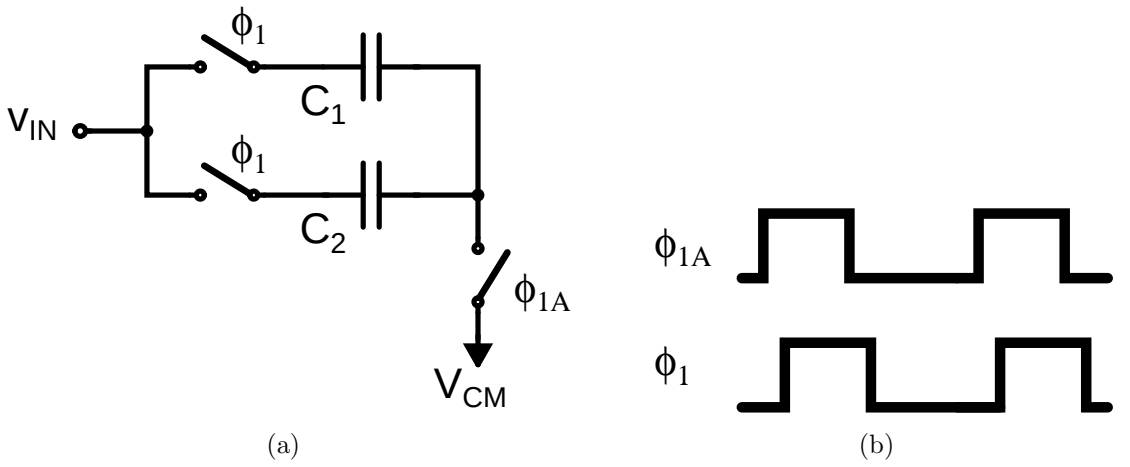
2.1 Comparator-Based Switched-Capacitor Circuits

The operation of op-amp based and comparator-based switched-capacitor gain stages are very similar. The fundamental difference is that while the op-amp *forces* the virtual ground condition for the entire charge transfer phase, the comparator *detects* the virtual ground condition and triggers sampling.

Traditional Op-amp Based Switched-Capacitor Gain Stage

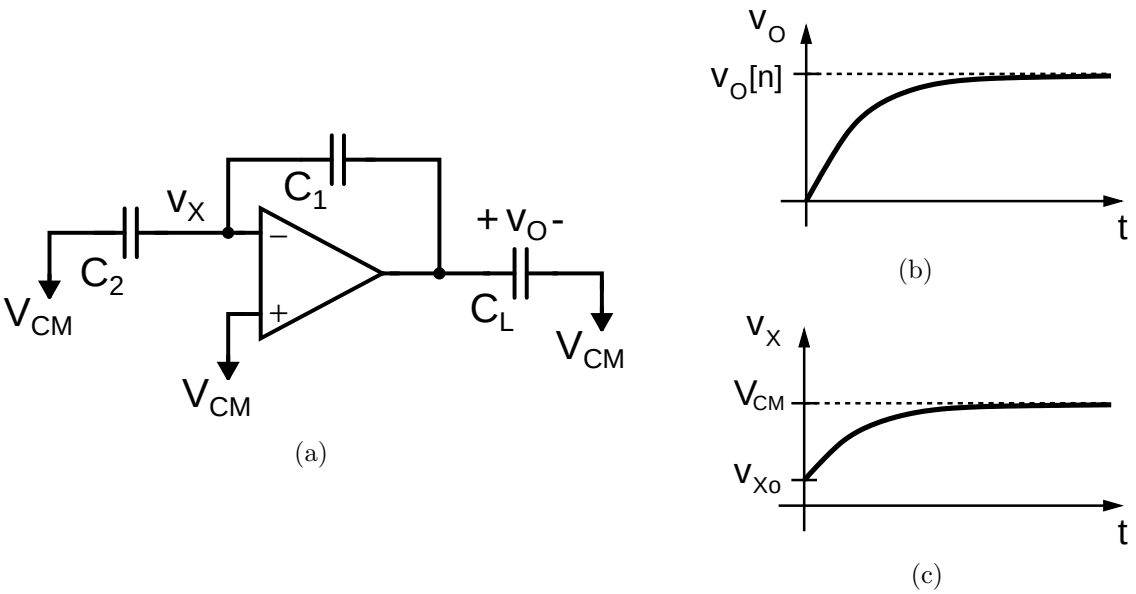
An op-amp based switched-capacitor gain stage operates on a two phase cycle: a sampling phase and a charge transfer phase. During the sampling phase ϕ_1, the input voltage is sampled onto both C_1 and C_2 using the open-loop sampling circuit shown in Fig. 2-1. The falling edge of the clock ϕ_{1A} defines the sampling instant in order to minimize signal dependent charge injection [22, 23].

For the charge transfer phase, the capacitors are reconfigured as shown in Fig. 2-2. The op-amp forces a virtual ground condition at the summing node, which transfers all the charge that was originally sampled on C_2 onto C_1. During the charge transfer, both the output voltage v_O and the summing node voltage v_X settle exponentially



(a) (b)

Figure 2-1: Bottom plate open-loop sampling (a) Sampling circuit. (b) Sampling clocks. ϕ_{1A} defines sampling instant to minimize input dependent charge injection.



(a) (b) (c)

Figure 2-2: Op-amp based switched-capacitor gain stage charge transfer phase. (a) Switched-capacitor circuit (b) The output voltage exponentially settles to the final value. (c) The summing node voltage exponentially settles to the virtual ground condition.

to their steady-state values as shown in Fig. 2-2. The time-constant of the closed loop system determines the settling speed. In the simplified one-pole system shown in Fig. 2-2 a single time constant determines the settling speed. In a more realistic multi-pole system the time constant of the decay of the output voltage envelope determines the settling speed. In either case, after a number of time constants the output voltage settles sufficiently and it is sampled onto the load capacitance C_L. The relationship between the input and the output samples is given by:

$$v_O[n] = \left(\frac{C_1 + C_2}{C_1}\right) v_{IN}[n - \tfrac{1}{2}]. \tag{2.1}$$

During the charge transfer phase, the accuracy of the output voltage is directly related to the accuracy of the virtual ground condition. The op-amp tries to force the virtual ground in a continuous-time manner. However, the only time an accurate virtual ground is necessary in switched-capacitor circuits is at the sampling instant. Therefore, it should be possible to detect the virtual ground condition with a comparator rather than force it with an op-amp. Also, the former should be more energy efficient than the latter.

Comparator-Based Switched-Capacitor Gain Stage

A comparator-based switched-capacitor gain stage operates on a similar two phase cycle as an op-amp based switched-capacitor gain stage. The sampling phase ϕ_1 of a comparator-based circuit is identical to the sampling phase of the op-amp based circuit (Fig. 2-1).

The charge transfer phase of a comparator-based switched-capacitor gain stage is shown in Fig. 2-3. The op-amp has been replaced with a threshold-detection comparator and a current source I_X. During a short preset phase, not shown in Fig. 2-3, v_O is shorted to ground thereby presetting v_X below V_{CM}. Then, the current source I_X turns on, charges up the capacitor network consisting of C_1, C_2, and C_L, and creates the ramp waveforms v_O and v_X shown in Fig. 2-3. The voltages continue

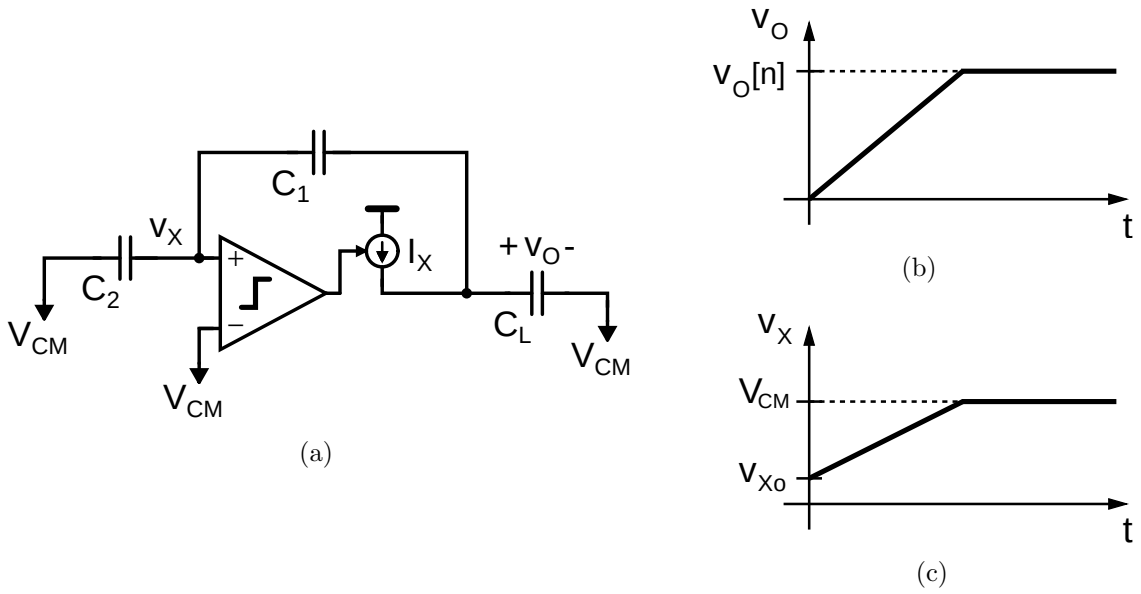


Figure 2-3: Comparator-based switched-capacitor gain stage charge transfer phase. (a) Switched-capacitor circuit with an idealized zero delay comparator. (b) The output voltage ramps to the final value. (c) The summing node voltage ramps to the virtual ground condition.

to ramp until the comparator detects the virtual ground condition (v_X=V_{CM}), and turns off the current source. In this way, the comparator determines the sampling instant. At the sampling instant, the same virtual ground condition has been obtained as in the op-amp based circuit. All the charge from C_2 has transfered to C_1, and the same output voltage is sampled on C_L.

2.2 Comparator-Based Switched-Capacitor Charge Transfer

This section describes the comparator-based switched-capacitor charge transfer in greater detail. To achieve high accuracy and linearity the charge transfer phase is divided into three sub-phases: a preset phase (P), a coarse charge transfer phase (E_1), and a fine charge transfer phase (E_2). The timing for a complete clock cycle is as shown in Fig. 2-4. A large portion of the total clock cycle is reserved for phase

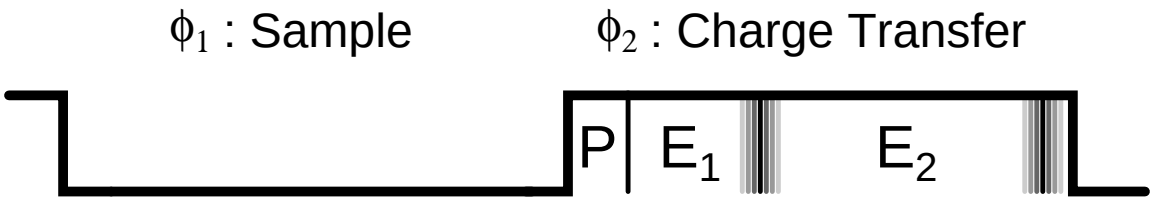
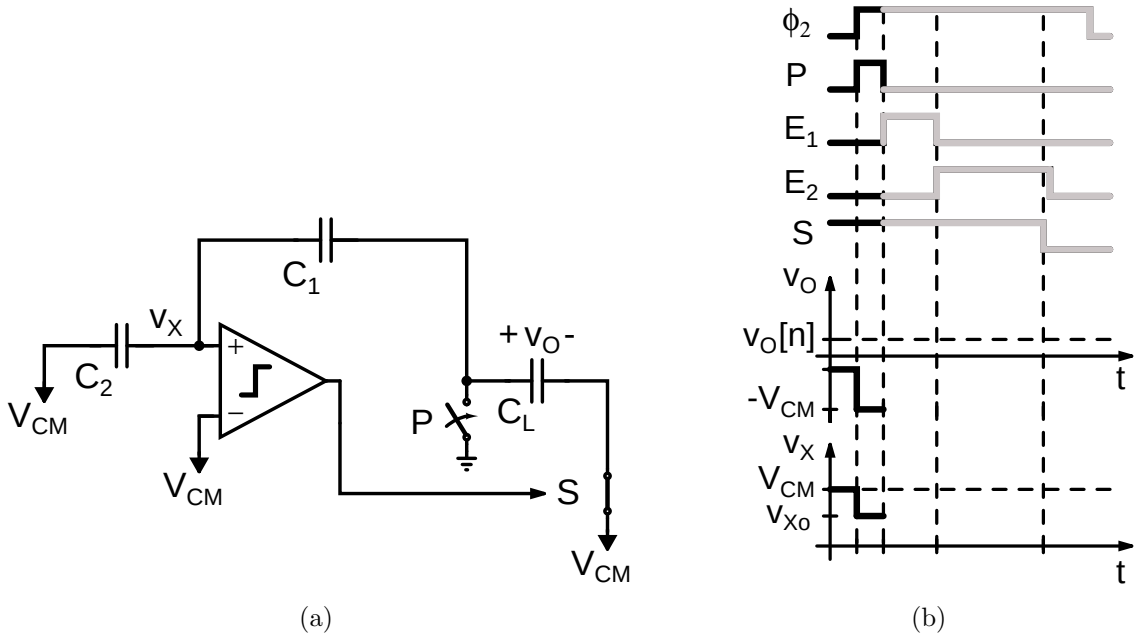


Figure 2-4: CBSC Clock Cycle: Preset (P), Coarse Charge Transfer Phase (E_1); it has a variable duration depending on the input, Fine Charge Transfer Phase (E_2); it has a variable end point depending on the input

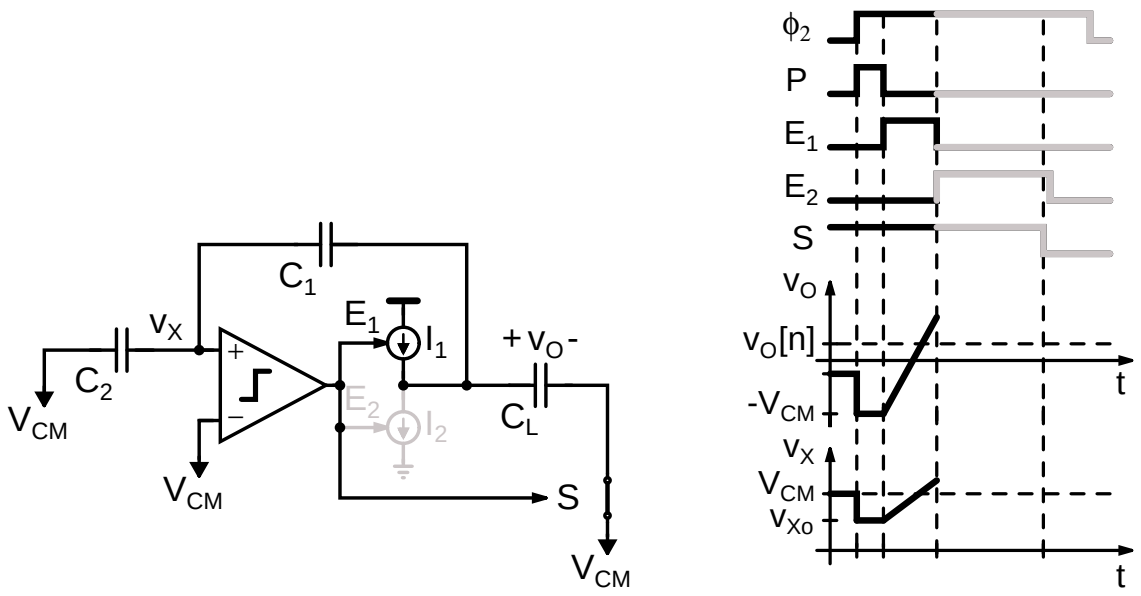


(a) (b)

Figure 2-5: Preset phase (P). (a) Switch P closes. (b) v_O grounded and v_X brought below V_{CM}

E_2 in order to minimize the sensitivity of the circuit to nonlinearity and to maximize the accuracy of the circuit. The comparator decision time is allowed to take up most of E_2 so that the noise bandwidth of the comparator can be minimized.

A short preset phase (P), shown in Fig. 2-5, is used to ensure that v_X starts below the virtual ground condition. After sampling completes at the end of phase ϕ_1, the voltage v_X is equal to V_{CM}. During the preset, V_{CM} is connected to C_2, and the output of the stage is connected to the lowest system voltage. This causes v_X to step low and results in V_{Xo} being less than V_{CM} over the range of input voltages. The sampling switch S is also closed during the preset phase to preset the load capacitance.



(a) (b)

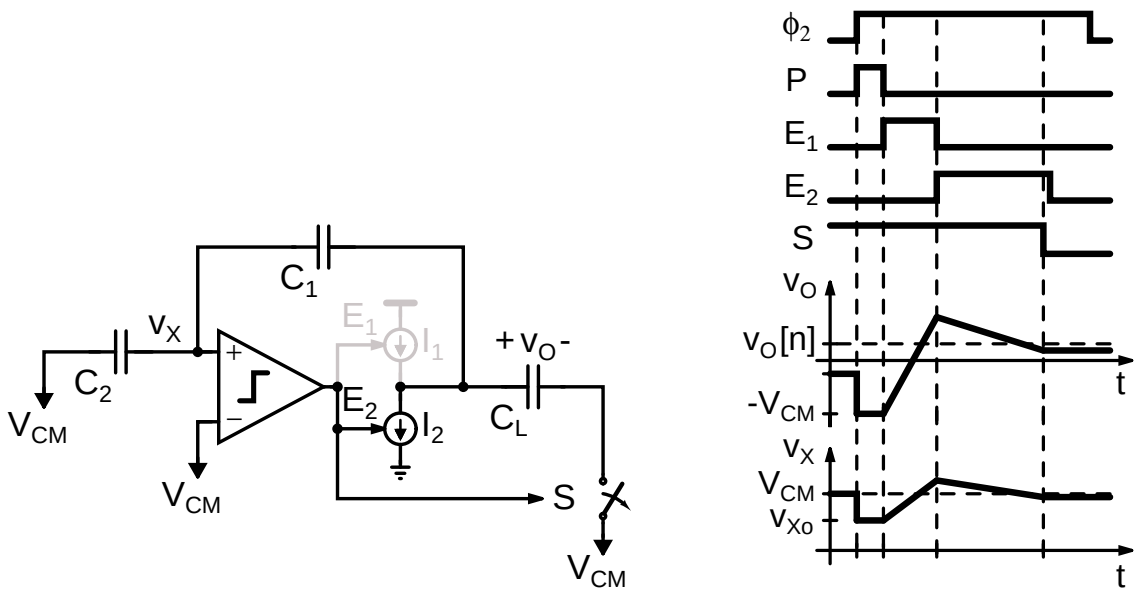
Figure 2-6: Coarse charge transfer phase (E_1). (a) Current source I_1 charges output. (b) v_O and v_X ramp and overshoot their ideal values.

The coarse charge transfer phase (E_1), shown in Fig. 2-6, is used to get a fast, rough estimate of the output voltage and virtual ground condition. The finite delay of the comparator and the high output ramp rate results in an overshoot of the correct value. When the comparator makes its decision, the current source I_1 is turned off.

The fine transfer phase (E_2), shown in Fig. 2-7, is used to get a more accurate measurement of the virtual ground condition and consequently a more accurate value for the output voltage. The fine phase current I_2 is much less than the coarse phase current I_1 and of opposite sign. This allows the comparator to have a long delay without causing a large final overshoot.

When the comparator detects the second threshold crossing, the sampling switch S is opened. This defines the sampling instant and locks the sample charge on the load capacitance C_L. The I_2 current source is turned off slightly after the sampling switch opens, but the extra current it sinks does not disturb the sampled charge because it only discharges the parasitic capacitance at the output node.

The time required to complete the charge transfer is signal dependent. The du-

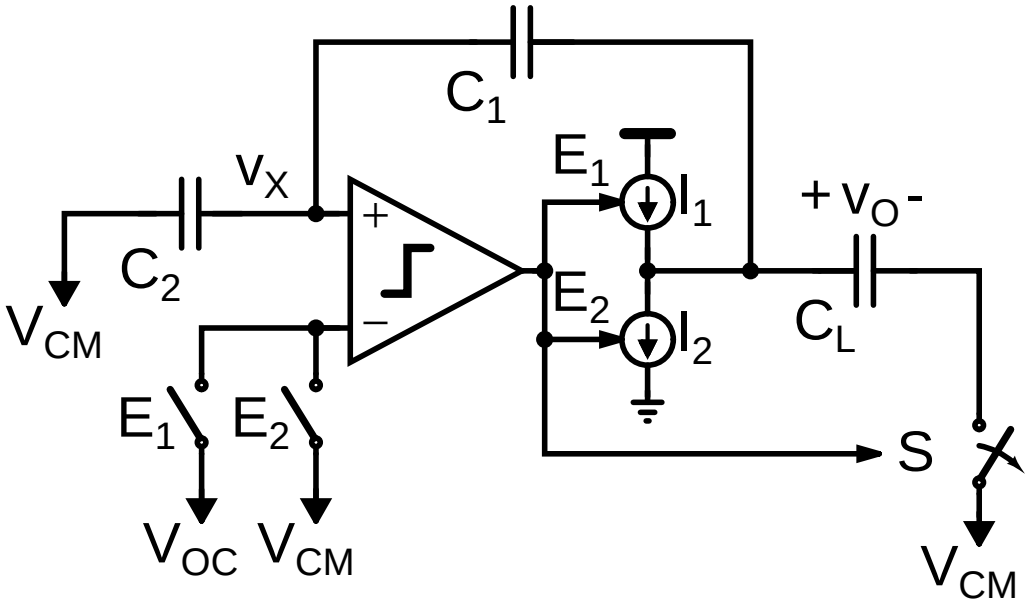


(a) (b)

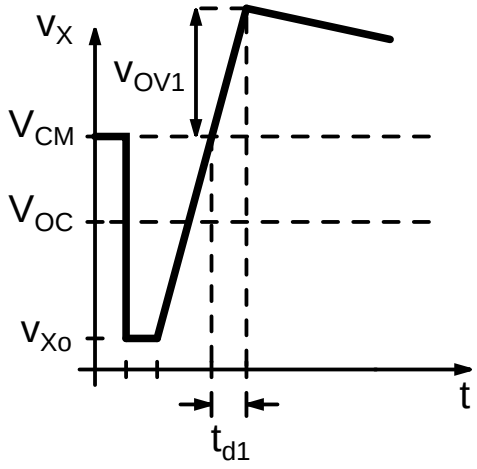
Figure 2-7: Fine charge transfer phase (E_2). (a) Current source I_2 discharges output. (b) v_O and v_X ramp to their final values.

ration of the coarse charge transfer phase E_1 depends on the preset value v_{Xo}, which depends on the input signal. The charge transfer is self-timed, but for correct operation, the total charge transfer must be complete before the end of the time allocated for charge transfer. As shown in Fig. 2-7, the falling edge of ϕ_2 represents the end of the allocated charge transfer time.

During the coarse charge transfer phase, a large current is used to charge the output capacitance thereby creating a potentially large offset and nonlinearity. The large overshoot slows the operation of the circuit because the fine phase current requires a long time to discharge the output and recover from the coarse phase overshoot. In order to minimize this recovery time, a portion of the overshoot is canceled. One way to do this is to change the reference voltage of the level detection comparator from V_{CM} to a lower voltage V_{OC}. This operation is shown in Fig. 2-8, and is also discussed in detail in Section 5.2.2. V_{OC} is a reference voltage that is the same for all possible output voltages. It is set to cancel as much of the overshoot as possible while still allowing the output to overshoot for all output voltages. If the overshoot is canceled



(a)



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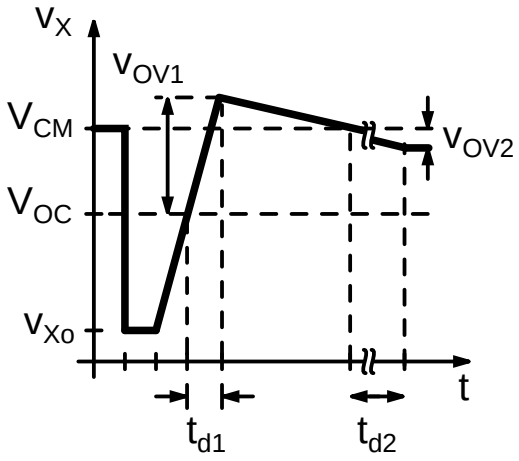


(c)

Figure 2-8: Overshoot cancellation. (a) CBSC stage with overshoot cancellation. (b) v_X node voltage during the charge transfer phase without overshoot correction. The large overshoot during the coarse phase prevents the charge transfer operation from finishing in allowed time. (c) CBSC stage with overshoot cancellation.

too aggressively the output voltage will not overshoot for an output value and the circuit will not operate correctly.

2.3 Conclusion

The CBSC technique shares many similarities with traditional op-amp based switched capacitor circuits. The two techniques share the same two phase clock cycle and the same sampling phase. The charge transfer phase represents the difference between the two. During the charge transfer phase op-amp based circuits use the op-amp to continuously force a virtual ground while CBSC circuits use a comparator to sense a virtual ground condition.

Chapter 3

Traditional Pipelined ADC

Pipeline ADCs are high performing and versatile modern data converters. They are used in many applications including wireless systems, wireline systems, medical electronics, still and video cameras and electronic test equipment. Commercial pipelined ADCs provide resolutions between 8 b and 16 b and have sampling rates between 1 MS/s and 250 MS/s [24–26]. This chapter provides a brief overview of pipelined ADCs and describes the traditional op-amp based pipelined ADC [27].

3.1 Operation and Architecture

Figure 3-1 shows the ADC architecture. The ADC consists of a number of stages (M). Each stage resolves n bits and produces a residue to pass on to the next stage. The ADC operates in a pipelined manner so that each stage is always either resolving bits and producing a residue or sampling the residue of the previous stage. The bits of all of the stages enter the shift register to be time aligned. The shift register outputs the total number of time aligned bits, nM.

Figure 3-2 shows the composition of a single stage. It consists of an n-bit ADC, an n-bit DAC and a amplifier and subtraction circuit. The ADC resolves the bits. The DAC and subtraction circuit subtract the analog representation of the resolved bits from the input signal. This value is then multiplied by 2^n to produce the residue

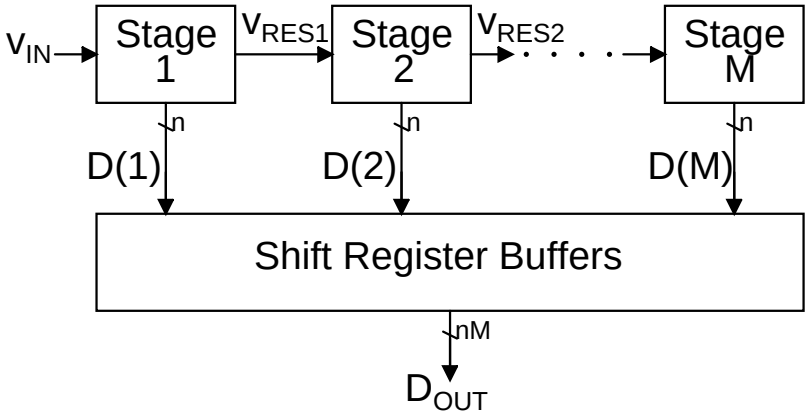


Figure 3-1: Pipeline ADC

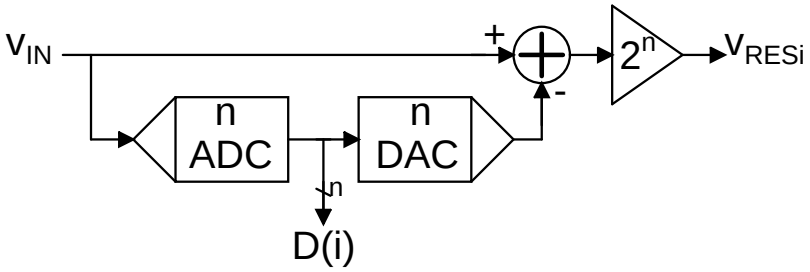


Figure 3-2: Pipeline ADC stage

voltage.

For the case of a 1 b/stage Pipelined ADC each stage first determines whether an input is above or below the mid value of the input range (V_{CM}) and then takes the portion of the input range that the input is in and amplifies it and shifts it so that this residue takes up the entire input range of the next stage.

3.2 Op-Amp Based Circuit Implementation

Traditional Pipelined ADCs employ op-amps to provide the amplification and subtraction needed in a stage. The schematic of a stage of a 1 b/stage Pipelined ADC is shown in Figure 3-3.

This schematic is very similar to the op amp based gain-of-two stage discussed in chapter 2. A comparator has been added to resolve a bit and reference voltages are

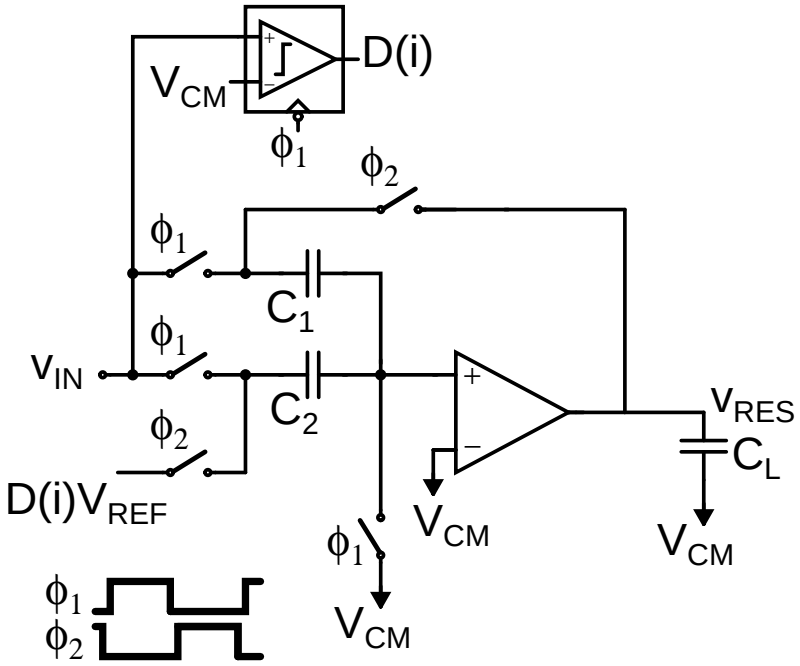


Figure 3-3: Traditional op-amp based 1 b/stage Pipelined ADC stage

connected to C_2. The stage produces the residue voltage,

$$v_{RES} = \frac{C_2 + C_1}{C_1} \bullet v_{IN} - D(i) \bullet \frac{C_2}{C_1} \bullet V_{REF}. \tag{3.1}$$

Ideally $C_1 = C_2$ and the residue is

$$v_{RES} = 2 \bullet v_{IN} - D(i) \bullet V_{REF}. \tag{3.2}$$

where

$$D(i) \bullet V_{REF} = V_{MIN} \qquad v_{IN} < V_{CM} \tag{3.3}$$

$$D(i) \bullet V_{REF} = V_{MAX} \qquad v_{IN} > V_{CM} \tag{3.4}$$

and the digital output bit is 1 for $v_{IN} > V_{CM}$ and 0 for $v_{IN} < V_{CM}$.

The plot of this residue is the solid line in Figure 3-4. Notice that in a 1 b/stage ADC any offset in the comparator will cause the residue voltage to exceed the maxi-

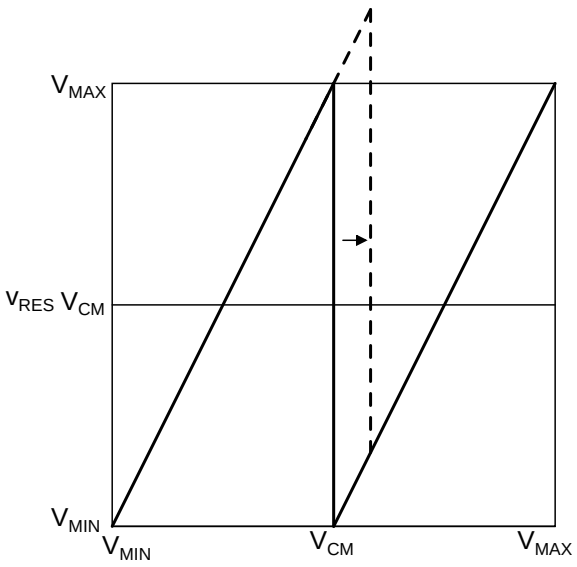


Figure 3-4: Residue plot of a single stage of a 1 b/stage Pipelined ADC.

mum voltage of the ADC, V_{MAX}. This effect is shown by the dashed line. The offset causes the residue voltage to exceed the input range of the succeeding stage. The portion of the residue that exceeds the input range is not processed by the rest of the pipeline. This effect causes gross nonlinearity in the ADC transfer characteristic and missing decision levels.

In order to avoid errors due to comparator offset, digital error correction [27] is usually used in the ADC design. One version of digital error correction is the 1.5 b/stage scheme [28–30]. An op-amp based implementation of the 1.5 b/stage ADC is shown in Figure 3-5. A second comparator is added to the 1 b/stage ADC as well as a third reference level. The reference levels are now

$$D(i) \bullet V_{REF} = V_{MIN} \qquad v_{IN} < V_{RN} \tag{3.5}$$

$$D(i) \bullet V_{REF} = V_{CM} \qquad v_{IN} > V_{RN} \,\&\, v_{IN} < V_{RP} \tag{3.6}$$

$$D(i) \bullet V_{REF} = V_{MAX} \qquad v_{IN} > V_{RP}. \tag{3.7}$$

The bit decision is resolved to be 1 if $v_{IN} > V_{RP}$, 0 if $v_{IN} < V_{RP}$, and if v_{IN} is between V_{RN} and V_{RP} the bit decision is passed further down the pipeline to be made by a

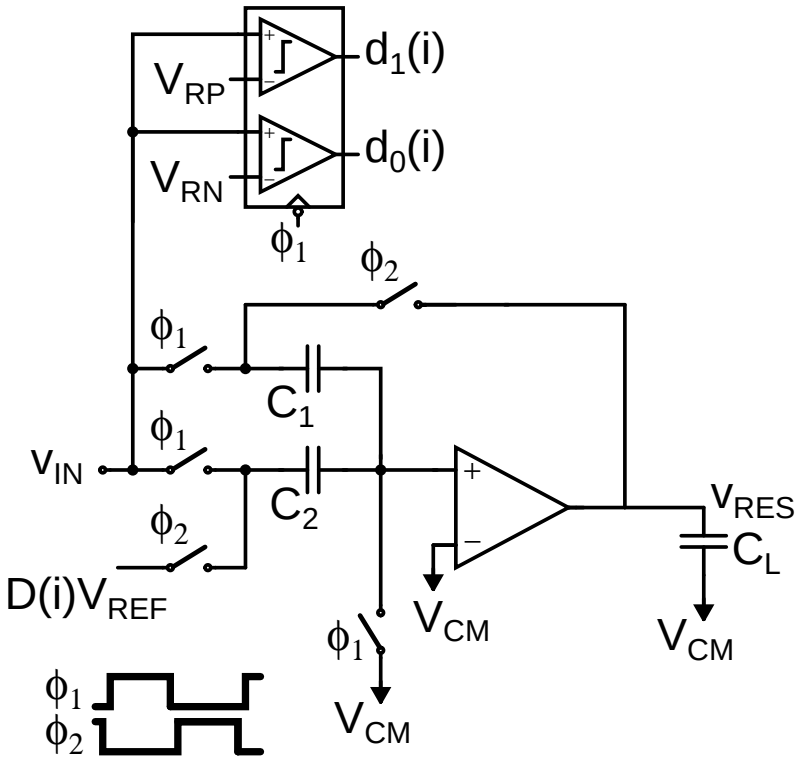


Figure 3-5: Traditional op-amp based 1.5 b/stage Pipelined ADC stage

later stage. The 1.5 b/stage residue plot in figure 3-6 shows that a small comparator offset will not cause the residue voltage to exceed the input range of the succeeding stage. To allow the maximum correction range for comparator offset V_{RN} is set to $\frac{3}{8}V_{FS} + V_{MIN}$ and V_{RP} is set to $\frac{5}{8}V_{FS} + V_{MIN}$ where $V_{FS} = V_{MAX} - V_{MIN}$. These comparator reference levels allow each comparator to have offsets of $\pm\frac{1}{8}V_{FS}$.

The low intrinsic transistor gain in scaled technologies, described in Chapter 1, causes INL in Pipelined ADCs. Low gain transistors produce low gain op-amps which in turn produce stage gain error. Linear gain errors can be removed using well known calibration techniques [31]. Nonlinear gain errors can only be removed through statistical calibration using a large number of input samples [14]. Chapter 4 describes the application of the CBSC technique to a 1.5 b/stage ADC to address the effects of low op-amp gain on the performance of switched capacitor circuits.

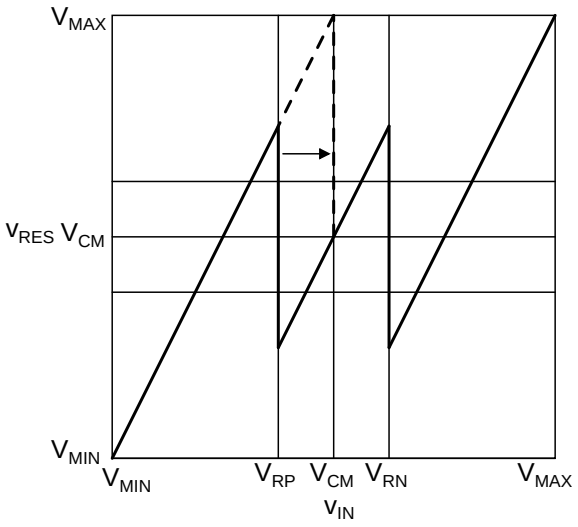


Figure 3-6: Residue plot of a single stage of a 1.5 b/stage Pipelined ADC.

Chapter 4

CBSC Pipelined Design

4.1 CBSC Applications

The CBSC design method applies not only to the gain stage used in the description of the technique but to switched-capacitor circuits in general. The technique applies to a broad range of switched-capacitor circuits including, filters, integrators in sigma-delta converters, switched capacitor DACs, and switched-capacitor ADCs.

4.2 1.5 b/stage CBSC Pipelined ADC

As a proof of concept the CBSC method was applied to a 1.5 b/stage Pipelined ADC. A simplified schematic of the first two stages of the pipeline is shown in Figure 4-1. For the prototype, a single-ended circuit design was used as is shown in the schematic. The prototype consists of 13 identical stages. The first 12 stages resolved bits. The 13th stage is only present to provide a load for the 12th stage. The bit decisions of the 13th stage are not recorded. The later stages were left unscaled in order to simplify the design. They could be scaled to reduce the ADCs power consumption. Unlike a traditional 1.5 b/stage ADC the final stage does not produce a whole number of bits such as 1 or 2 bits, but rather ouputs three decisions. This could easily be changed by wiring the comparator references for the 12th stage to V_{CM} rather than V_{RN} and

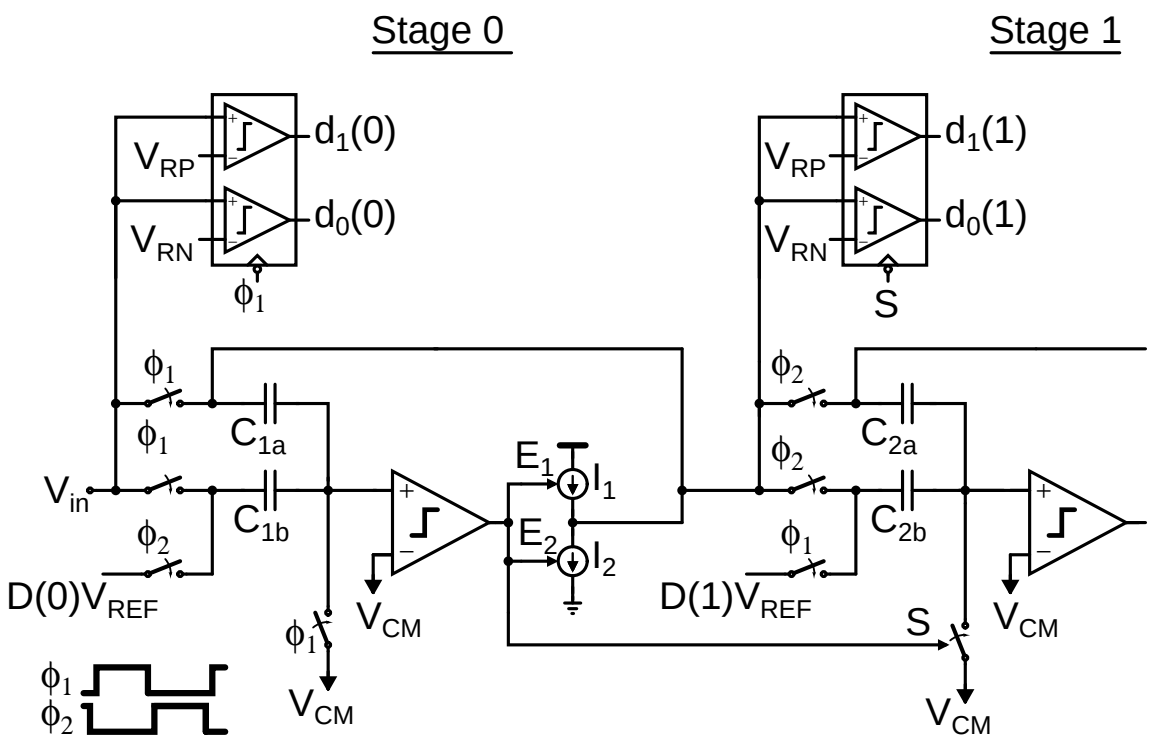


Figure 4-1: First two stages of the prototype Pipelined ADC.

V_{RP} and eliminating the 13th stage.

4.2.1 Threshold Detection Comparator

A critical circuit in the CBSC method is the virtual ground detection comparator. Unlike a traditional clocked comparator that compares voltages at a specific point in time the virtual ground detection comparator must detect the time a voltage ramp crosses the virtual ground condition and must then open the output sampling switch.

Comparators can achieve high gain by cascading several gain stages. Because the comparator is only used in an open-loop configuration, there are no associated stability issues with this approach. A high level schematic of the comparator used in the prototype is shown in Figure 4-2. The first stage of the comparator determines the noise accuracy of the virtual ground detection. This band-limiting stage is followed by a series of 3 wide-band amplifying stages that drive a level converter to create the complementary logic signals used to control the current source and sampling switch

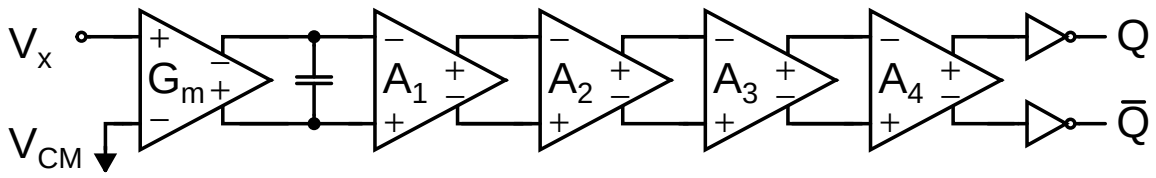


Figure 4-2: Diagram of the Threshold Detection Comparator

logic circuits.

A more detailed schematic of the comparator is shown in Figure 4-3. The first stage is the actively loaded band-limiting stage. The stage's common-mode feedback circuit is not shown in the figure. The output is clamped by two back-to-back MOS diodes for faster recovery of the comparator. Also, it is the total parasitic capacitance at the output of this first stage analog with its transconductance that sets the bandwidth. The band-limiting amplifier is followed by 2 low-swing, wide-bandwidth gain stages which drive the final gain stage. The final stage drives a pair of level converters whose outputs are buffered with standard CMOS inverters. For greater detail about the threshold detection comparator see [32].

4.2.2 Bit Decision Comparator

The bit decision comparators are dynamic clocked comparators. A schematic of the comparator is shown in Figure 4-4. At the falling edge of ϕ_1 the input series switches are opened. This samples the input and reference voltages on to the inputs of the cross coupled inverters. Just after the falling edge of ϕ_1, ϕ_L rises and connects the header switches, M_{PA} and M_{PB}, and footer switches, M_N. This triggers the positive feedback and causes the comparator to resolve a bit.

The inputs to the comparator are not high impedance nodes. This allows for the possibility that the comparator can draw extra current through its inputs during some portion of its input range. It has two independent header switches, M_{PA} and M_{PB}, rather than a single switch seen in a traditional comparator in order to prevent input current draw. Sepke [32] provides a more detailed explanation of this effect.

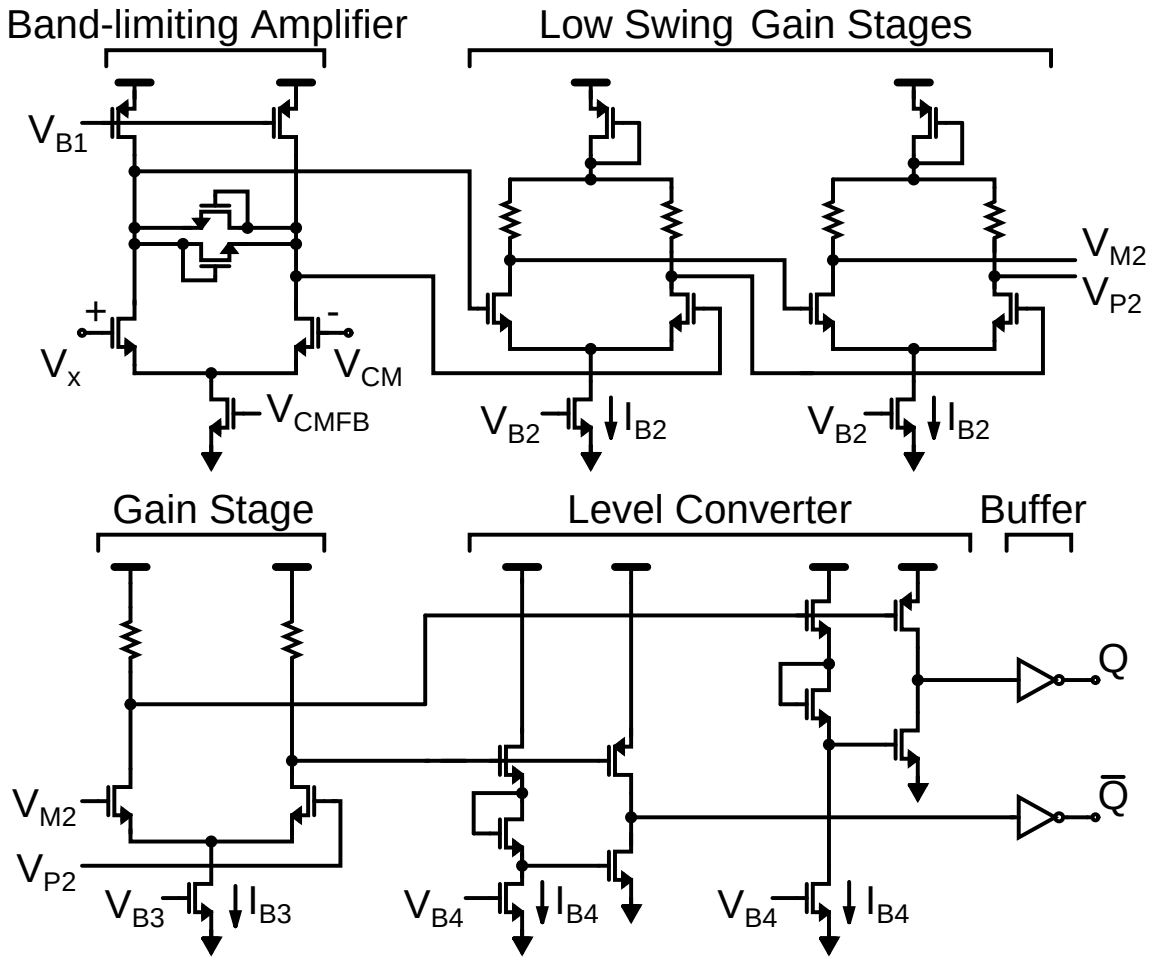


Figure 4-3: The Threshold Detection Comparator Schematic

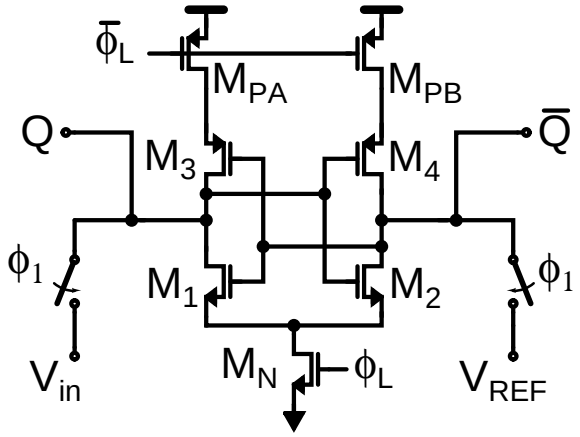


Figure 4-4: Bit Decision Comparator Schematic

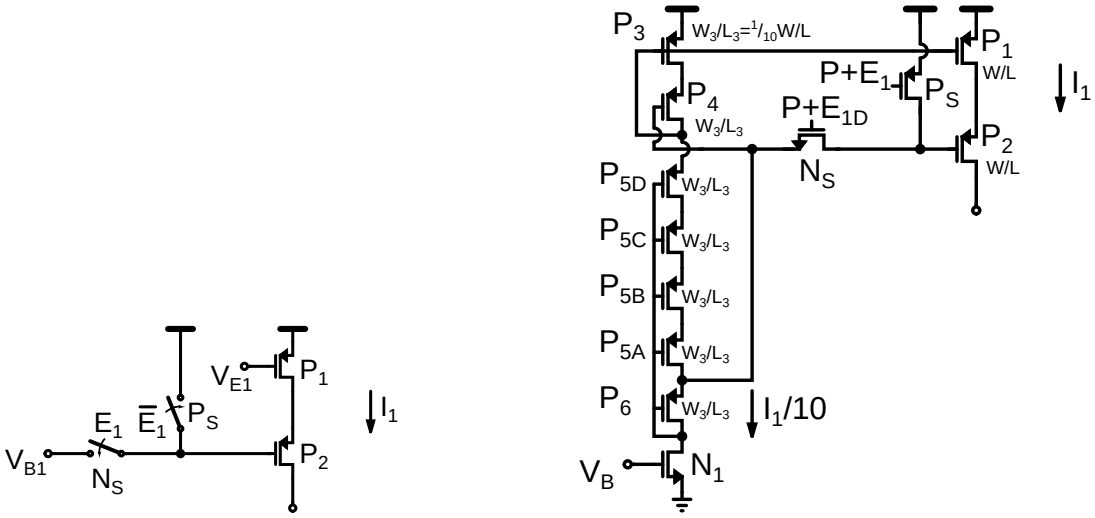


Figure 4-5: Coarse Current Source.

4.2.3 Ramp Generation

Another important part of the implementation is the ramp generation. The prototype uses two switched current sources to produce the output voltage ramps.

The coarse charge transfer phase current source I_1 was implemented with a cascode current source, and is switched on and off by controlling the gate voltage of the cascode device P_2 as shown in Figure 4-5(a). During the coarse charge transfer phase E_1 the gate of the cascode transistor P_2 is connected to the bias voltage V_{B1}. After this phase the gate of the cascode transistor P_2 is disconnected from V_{B1} and connected to the power supply. This action shuts the current source off.

The coarse current source for each stage has its own cascode bias circuit. This was done so the noise created by turning the current source off in one stage would not disrupt the bias voltage line and couple to the current sources in the other stages. A detailed view of the current source and bias circuit appears in Figure 4-5(b). The bias circuit is based on the Sooch mirror [33, 34]. Using this mirror reduces power consumption because it requires only one leg for biasing rather than the two legs required by the standard wide swing cascode bias [35–37]. Also the bias leg is scaled down by 10× to further reduce the power consumption of the circuit. Transistors P_3

P_1	24.8 µm/0.5 µm
P_2	24.8 µm/0.5 µm
P_3	2.48 µm/0.5 µm
P_4	2.48 µm/0.5 µm
P_{5A}-P_{5D}	2.48 µm/0.5 µm
P_6	2.48 µm/0.5 µm
P_S	1 µm/0.18 µm
N_1	6 µm/1.5 µm
N_S	1 µm/0.18 µm
I_1	70 µA

Table 4.1: Coarse Current Source Transistor sizes

and P_4 operate as they do in the wide swing cascode mirror. The gate of P_3 is set at $V_T + \Delta V$ below V_{DD} because P_3 is diode connected. Transistor P_4 ensures that P_3 has ΔV drop across it just as P_1 does. The gate of P_4 must be set to $V_T + 2\Delta V$ below V_{DD} to ensure that the current source has the same wide swing as the wide swing cascode mirror. Transistors P_{5A}-P_{5D} and transistor P_6 serve to set the gate of transistor P_4 at the appropriate value. The transistors P_{5A}-P_{5D} operate in triode and have the same function as a single transistor of $\frac{1}{4}$ the W/L of transistor P_{5A}. Replacing the Transistors P_{5A}-P_{5D} with a transistor of $\frac{1}{3}\,W_3/L_3$ would cause ΔV to be dropped across this transistor. This voltage drop sets the gate of P_4 at the required voltage. Further explanation of this circuit is found in Appendix B. The effective $\frac{1}{4}\,W_3/L_3$ transistor (P_{5A}-P_{5D}) used in the prototype has a larger V_{ds} than a transistor of $\frac{1}{3}\,W_3/L_3$ would have. Transistors P_{5A}-P_{5D} therefore set the gate of P_4 is at a voltage further from V_{DD}. The lower gate bias voltage of P_4 provides some margin for P_3 and P_1 and ensures that they stay saturated despite process variation.

A disadvantage of the biasing circuit used in the prototype is that it requires a substantial amount of headroom.

$$V_{DDMIN} = 2\,V_{TP} + 3\Delta V \tag{4.1}$$

The process in which the prototype was manufactured has lower threshold voltages than the standard 0.18 µm CMOS process, with V_{TP} of 300 mV. Assuming that the overdrive voltage ΔV is set at 200 mV the minimum V_{DD} is 1.2 V. Therefore, for this technology, the bias leg can be easily fit in the 1.8 V supply. The details of the coarse current source are shown in table 4.1.

The coarse current source used in the prototype suffers from a slow turn on time. A certain amount of time is needed for the gate of the cascode device to settle to the correct voltage. In order to give the coarse current source more time to settle to the correct current it is turned on during the preset time. Turning on the current source during the preset time also prevents charge sharing between the output and the drain of P_1. In the prototype, the current source continues to settle during the beginning of the coarse transfer phase. This leads to increased output voltage ramp variation during the coarse transfer phase. This ramp rate variation in the coarse phase does not degrade the linearity of the final result because the fine phase sets the accuracy of the final result. In order improve the turn on time the bias leg can be scaled less aggressively. More current in the bias leg would allow it to charge the gate of the cascode transistor more quickly. Alternatively a large decoupling capacitor could be added between the gate of P_4 and V_{DD}. This capacitor would provide the charge to the gate of P_2 needed to turn the cascode on.

A second disadvantage with the bias circuit used in the prototype is that I_1 depends on the matching of transistor N_1 between stages for each stage to have the same coarse current. Routing a current to each stage is preferred to routing the voltage V_B to each stage because the matching of currents depends only on local transistor matching rather than matching across the chip. This change can be achieved by placing the N_1 transistors for each stage close to each other on one end of the chip. They will not suffer from cross chip mismatch due to their proximity to each other. Placing the N_1 transistors close to their matching diode that accepts the off chip current will also make them less sensitive to supply noise from the ground voltage. The transistors proximity to the low impedance diode lessens the supply noise that

couples on to V_B.

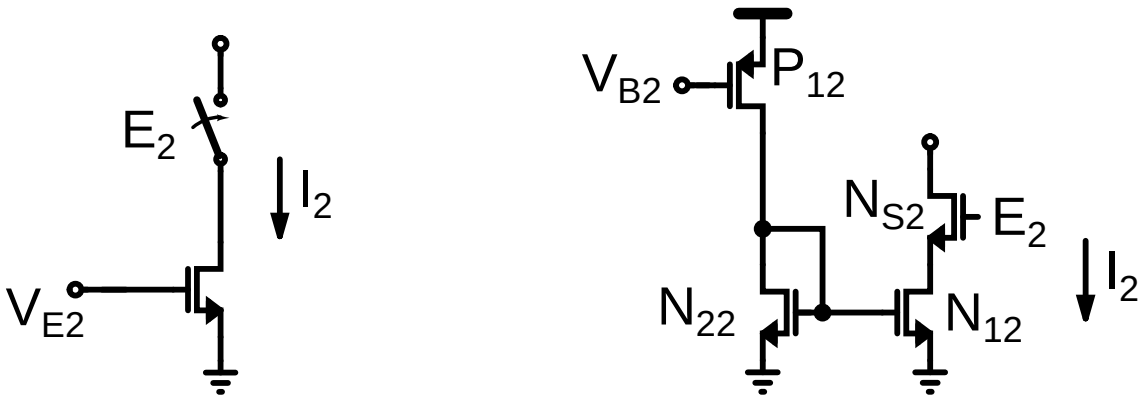
In order to reduce power dissipation, it is possible to make a single bias leg for the entire pipeline. This structure could lead to coupling between stages as mentioned above and would also be more sensitive to power supply noise than the structure used in the prototype. Power supply noise coupling into the bias leg at one end of the chip would not match noise coupling in at each stage. This could allow local power supply variation to disturb the current sources.

The fine charge transfer phase current source I_2 must produce much less current than current source I_1, which means a single device will have a much larger output resistance than a device suppling I_1. The current source I_2 is implemented as a simple current source controlled with a series switch as shown in Figure 4-6(a). It is shown in Chapter 6 that the output resistance of the single transistor current source was ultimately not large enough to achieve 10 bit linearity.

A detailed view of the fine current source and bias circuit appears in Figure 4-6(b). Transistor N_{S2} is a series switch controlled by E_2. When E_2 goes high N_{S2} turns on and current I_2 flows from the output node through the current source N_{12}. N_{S2} is in triode for all output voltages except for output voltages above 1.2 V. At output voltages above 1.2 V N_{S2} becomes saturated and forms a cascode with N_{12}. The N_{S2}-N_{12} cascode provides a much higher output resistance than the N_{S2} transistor alone. Consequently, for output voltages above 1.2 V the current source has a very large output resistance while for lower output voltages it produces a more moderate output resistance. Similar to the coarse current source, a separate bias circuit is used for the fine current source in each stage. The details of the fine current source are shown in table 4.2.

4.2.4 Clock Generation and Control

The system clock controls the sampling and bit decision clocking for the first stage only. For all subsequent stages, the level detection comparators control the sampling and the bit decision clocking through signal S. This is shown in Figure 4-1. Fig-



(a) (b)

Figure 4-6: Fine Current Source.

P_{12}	7.56 µm/1.5 µm
N_{12}	2.48 µm/1.34 µm
N_{22}	2.48 µm/1.34 µm
N_{S2}	0.44 µm/0.18 µm
I_2	3 µA

Table 4.2: Fine Current Source Transistor sizes

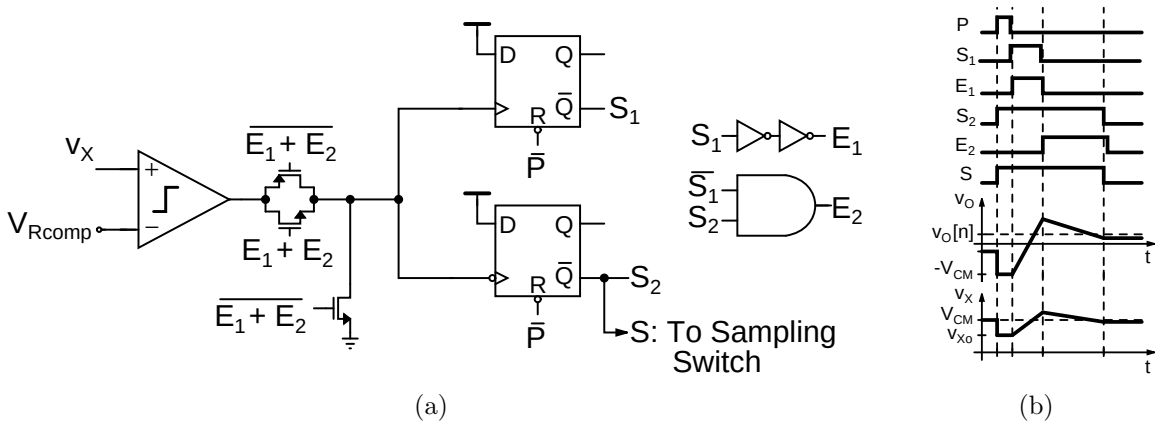


Figure 4-7: (a) CBSC state machine. (b) CBSC control signals.

ure 4-7(a) shows how the sampling signal S, the coarse current source control signal E_1, and fine current source control signal E_2 are generated. Figure 4-7(b) shows the signals for a single charge transfer operation. The flip-flops connected to the output of the comparator generate the control signals. The two flip-flops are reset during the preset phase so their $\overline{Q}$ outputs go high. The output of the comparator starts the charge transfer phase low. When v_X crosses V_{REF} the output of the comparator goes high. This edge causes the top flip-flop to flip and causes S_1 to go low. E_1, the buffered value of S_1, goes low turning off the coarse current source. Signal S_1 going low also causes E_2 to go high which causes the fine current source to turn on. Voltage v_X now reverses direction and is slowly discharged by the fine current source. When v_X crosses V_{REF} again the output of the comparator goes low. The bottom flip-flop senses this negative edge and causes S_2 to go low. Signal S_2 turns off the sampling switch and forces E_2 low shutting off the fine current source. The control signals are created using flip-flops so that they will only go high once during each cycle. Noise in the circuit cannot cause them to flip back and forth between states.

In order to perform the output overshoot cancellation discussed in Section 2.2 and shown in Fig. 2-8, the reference of the threshold detection comparator is changed as the ADC passes through the conversion cycle. The scheme to do this is shown in Figure 4-8. During the time the comparator is not in use, the reference voltage is held

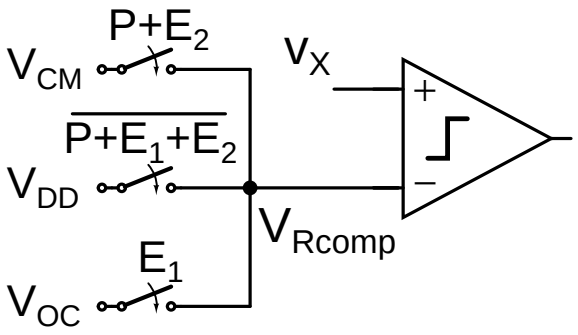


Figure 4-8: Level detection comparator reference switching.

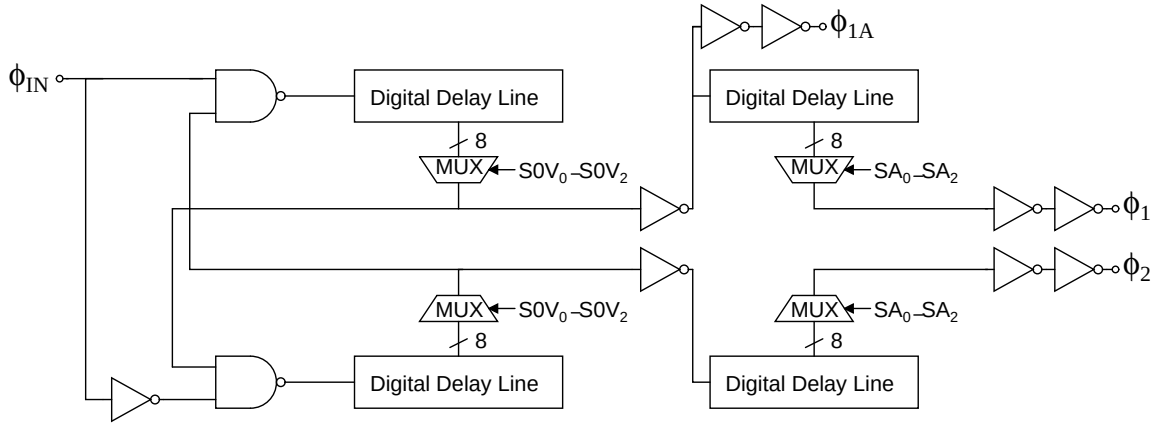


Figure 4-9: Nonoverlaped Clock Generation Circuit.

at V_{DD} to ensure that its internal nodes are all reset to their starting position. During the preset, the reference is set to V_{CM}. The reference is not lowered to V_{OC} so that there is less of a chance that a noise event will cause v_X to cross the reference value and start to flip the comparator. The reference is set to V_{OC} during the coarse charge transfer phase and is set back to V_{CM} during the fine charge transfer phase. V_{OC} is chosen to cancel a portion of the output overshoot. The choice of V_{OC} is covered in more detail in section 5.2.2.

The nonoverlaping clocks are generated using the standard circuit shown in Figure 4-9. A digital delay line and a MUX are used to vary the nonoverlaping period. The rest of the system clocks are generated from the nonoverlaping clock phases using digital delay lines and flip-flops. The clock generation circuit is shown in Figure 4-10. Phase ϕ_{1A} is the advanced clock used in the first stage sampling. Phase ϕ_{1S} signals

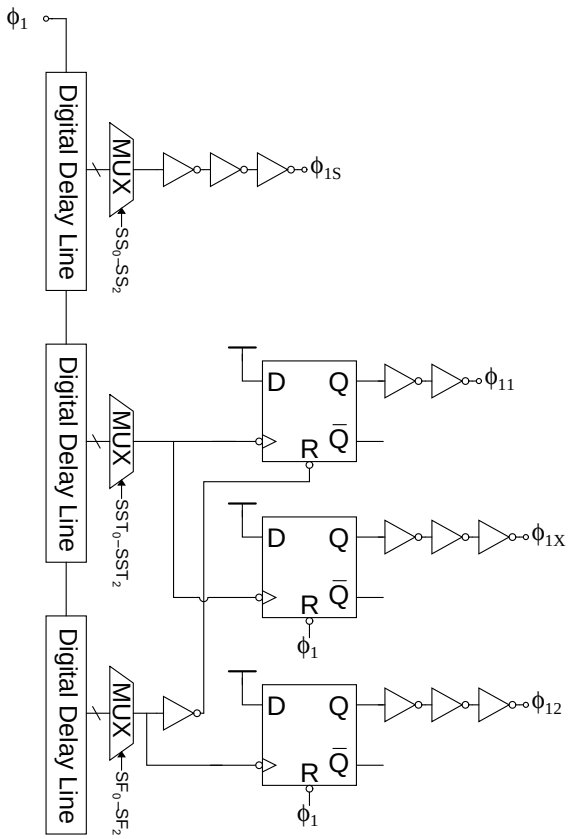


Figure 4-10: Clock Generation Circuit.

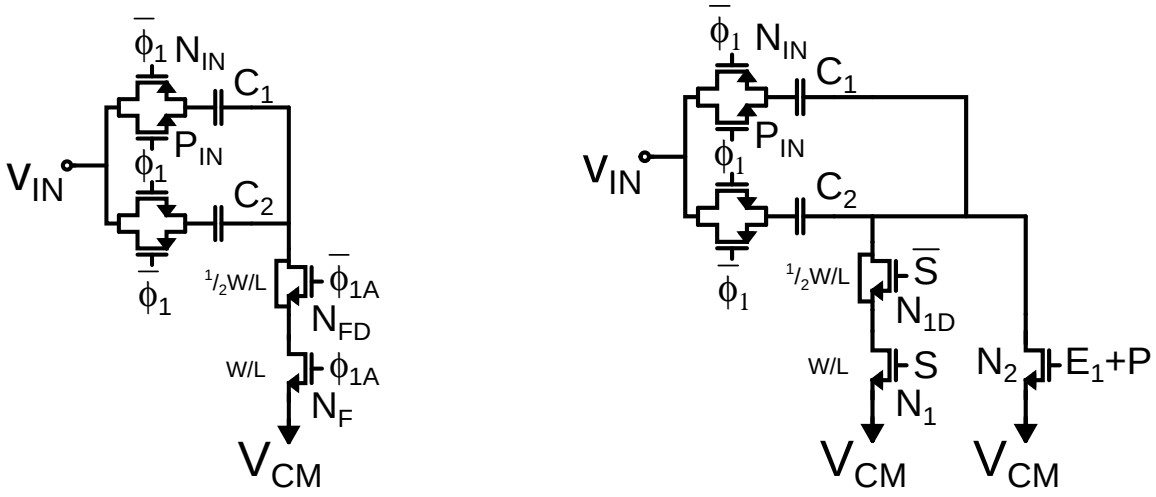


Figure 4-11: Input sampling circuits. (a) Input sampling circuit of the first stage. (b) Input sampling circuit of the second through twelfth stages.

N_F	3.04 µm/0.18 µm
N_{FD}	1.52 µm/0.18 µm
N_1	1.52 µm/0.18 µm
N_{1D}	0.76 µm/0.18 µm
N_2	3.0 µm/0.18 µm
N_{IN}	1.04 µm/0.18 µm
P_{IN}	3.2 µm/0.18 µm

Table 4.3: Sampling circuit transistor sizes

the bit decision comparators to store their results in latches. Phase ϕ_{1X} passes the bit decisions to the reference voltages. Phase ϕ_{11} controls the length of the preset time P. Phase ϕ_{21} sets the duration of the charge transfer time $E_1 + E_2$.

4.2.5 Input Sampling

The input sampling performed in the first stage differs from the input sampling performed in all of the succeeding stages. The input sampling circuit of the first stage is shown in Figure 4-11(a). The first stage input sampling circuit uses the standard bottom plate sampling technique [22, 23] to minimize input dependent charge injec-

tion. When input sampling switches consisting of N_{IN} and P_{IN} turn off the amount of charge they inject on to the sampling capacitors, C_1 and C_2, depends on the input voltage v_{IN}. This input dependent charge corrupts the voltage sampled on to C_1 and C_2 and creates overall circuit nonlinearity. Turning off transistor N_F before turning off the sampling switches locks the charge on the sampling capacitors and prevents the charge injected from the sampling switches from disrupting the sampled voltage. Transistor N_F also injects charge as it turns off. Some amount of this injected charge can also be input dependent. When N_F turns off, the charge in its inversion layer splits between its source and its drain. The proportion of charge that exits from its source and drain depends on the impedances seen from these two nodes. The impedance seen from its drain depends on the input voltage, therefore the charge injected from the drain of N_F on to the bottom plate of C_1 and C_2 also depends on the input voltage. The amount of input dependent charge injected from N_F is much less than the input dependent charge that would be injected by N_{IN} and P_{IN}. Adding a dummy device N_{FD} to the bottom plate of the sampling capacitors reduces the total charge injected from the sampling switch N_F on to the sampling capacitors [37]. As N_F turns off N_{FD} turns on and absorbs the charge injected by N_F. The details of the transistors sizes is shown in Table 4.3. The sampling switch N_F is sized to minimize charge injection while still enabling adequate settling time.

The input sampling circuit used in all of the stages succeeding the first stage is shown in Figure 4-11(b). This circuit differs from the circuit in the first stage in two ways: the sampling switch N_1 is controlled by the comparator output of the previous stage S and a switch N_2 is placed in parallel with the sampling switch. Transistor N_2 is only on during the coarse charge transfer phase. During this phase a large current passes through the switch potentially creating a large voltage drop across it. The parallel device N_2 lowers the overall switch impedance and consequently lowers the voltage drop across the switch. The charge injected by N_2 is sunk by N_1 to V_{CM} during the fine charge transfer phase and consequently has no effect on the final sampled value. During the fine charge transfer phase a much smaller current passes

through the sampling switch N_1 creating a smaller voltage drop. The sampling switch N_1 can consequently be narrower and have a larger resistance. The charge it injects can potentially disrupt the sampled charge as mentioned above. The sampling switch N_1 is sized small so that it injects a minimum amount of charge.

4.2.6 Layout

The die photo in Figure 4-12 shows the overall layout of the chip. The pipeline consists of 13 identical stages. The last stage does not resolve any bits. It just provides the correct load to the 12th stage. The outputs of only the first 10 stages were used in testing. The 11th and 12th stages were included in case the ADC had linearity and noise performance exceeding 10 bits. The chip also contains a configuration register, a clock generator and a test bit decision comparator. The area of the pipeline is $1.2\,\mathrm{mm}^2$ while the area of the overall chip is $10.9\,\mathrm{mm}^2$. The total chip area is much larger than the pipeline because the design required a large number of pads for testing flexibility and because the pipeline was not folded. Most of the pads were used by bit outputs. All of the raw bit outputs were taken off chip and reduced from 24 to 12 using MATLAB. In order to avoid design complexity the pipeline was laid out in a line rather than being folded into two lines. This was done so that each stage would see the same capacitance and therefore could use the same currents. If the pipeline was folded the stage directly before the fold would see more output capacitance than all of the rest. It would therefore have required a unique design or unique bias voltages.

The layout of a single stage of the ADC is shown in Figure 4-13 and a stage floor plan is shown in Figure 4-14. Since the ADC is a single ended design, the stage is not laid out in a symmetric fashion. Only the bit decision and threshold detection comparators are laid out symmetrically because they are differential circuits. The two sampling capacitors are each divided in two and laid out in a cross-quad with dummy capacitors surrounding them. This layout technique minimizes the potential for capacitor mismatch. The clock lines and bit lines are located at the top of the stages far away from the sensitive analog nodes to prevent coupling from the digital

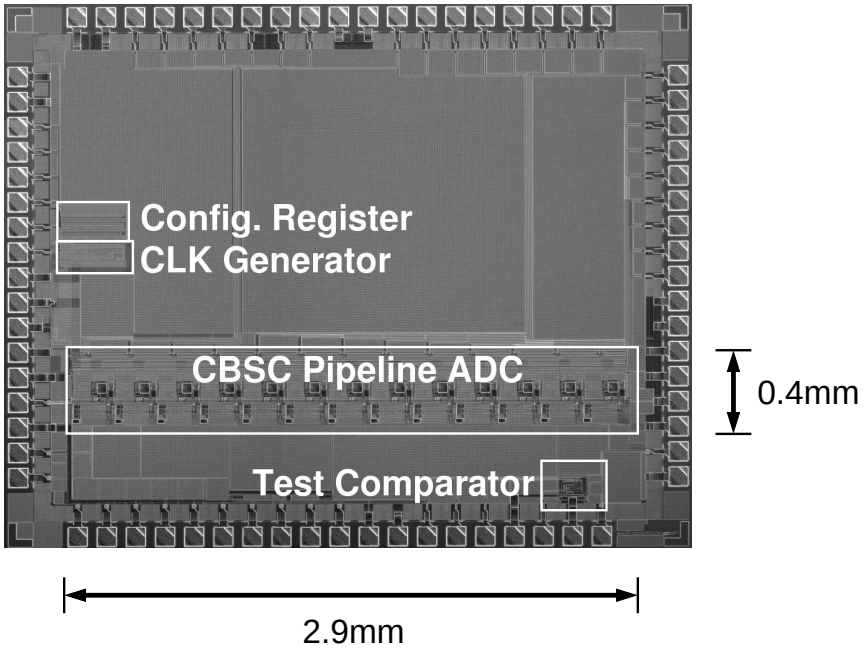


Figure 4-12: Die photograph. 0.18 µm CMOS process. Pipeline Area: 1.2 mm^2.

to the analog circuits. All of the sensitive analog circuits are ringed with n-wells and substrate connections to minimize substrate noise coupling. The most sensitive nodes such as the input to the continuous time comparator are shielded on all sides by metal to prevent stray signals from coupling on to them.

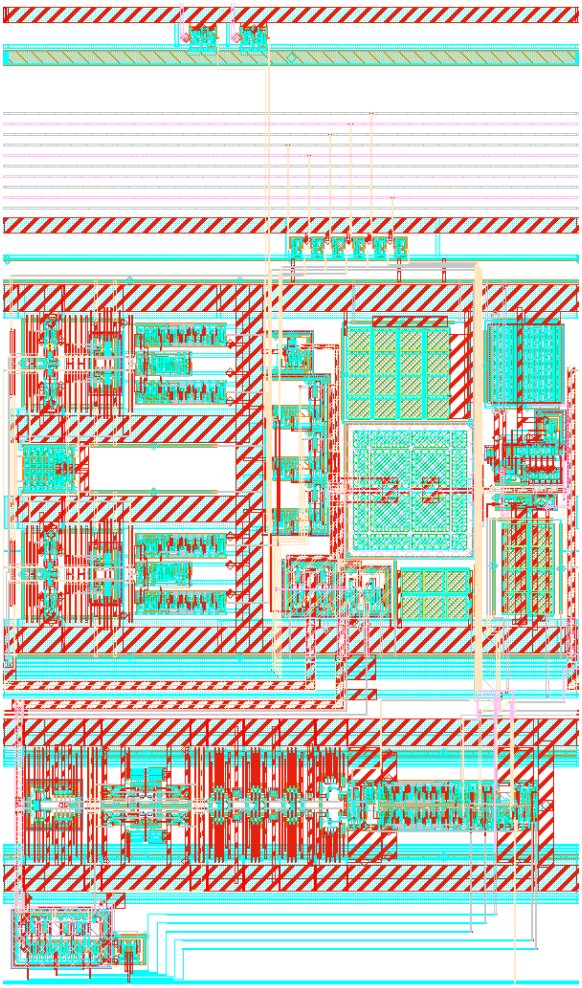


Figure 4-13: Layout of one stage of the prototype Pipelined ADC

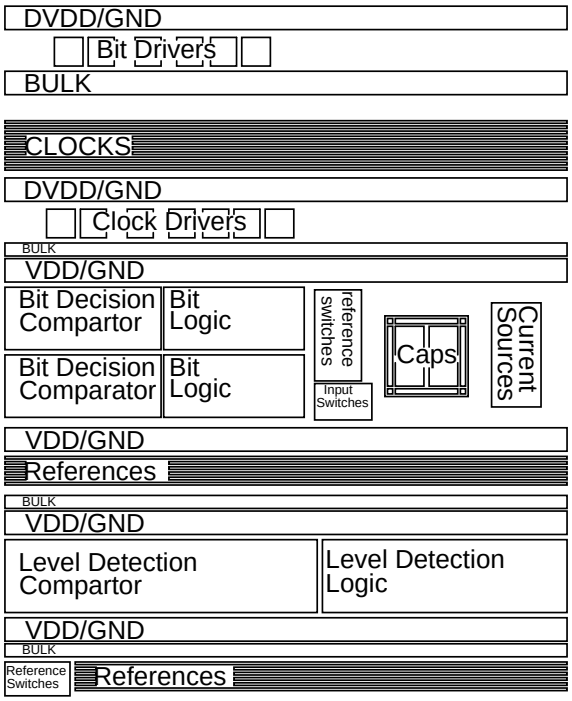


Figure 4-14: Floor plan of one stage of the prototype Pipelined ADC

Chapter 5

Offset and Nonlinearity in CBSC Circuits

A number of sources of offset and nonlinearity constrain the performance of CBSC circuits. In this chapter these sources and their effects on circuit performance are studied and techniques to manage their effects at a minimum power consumption are discussed.

5.1 Sources of Offset and Nonlinearity in CBSC Circuits

Two mechanisms create nonlinearity and offset in CBSC circuits: fine phase output overshoot due to finite threshold-detection comparator delay and voltage drops across switches with finite on-resistance. The two mechanisms produce errors in the output of a CBSC circuit. The average of these errors over the input voltage range results in offset and the change in these error over the input voltage range results in nonlinearity. For most applications, an offset in a circuit can be removed by a variety of known methods while nonlinearity in a circuit produces overall system nonlinearity. Nonlinearity is therefore a much larger concern than offset and consequently most of

the analysis will focus on nonlinearity.

5.1.1 CBSC Error Sources

Output voltage overshoot during the fine charge transfer phase and switch resistance voltage drop during the fine charge transfer phase create error is CBSC circuits.

The output voltage of a CBSC circuit overshoots its ideal value because the threshold detection comparator has a finite delay. The overshoot voltage depends on circuit parameters in the following manner

$$v_{OV} = \frac{i_X}{C_x + C_p + C_l} t_d \tag{5.1}$$

where C_x is the series combination of C_1 and C_2, C_l is the load capacitance of the circuit, C_p is the parasitic capacitance at the output of the current sources, i_X is charging current and t_d is the delay of the threshold detection comparator. The current i_X could be the coarse or fine phase current depending on whether v_{OV} is the coarse or fine phase overshoot. All of these values are functions of the output voltage v_O. The values change as the output voltage changes. The charging current changes with output voltage due to finite current source output resistance. The capacitances change as parasitic junction and gate capacitances change with output voltage. The comparator delay changes as the comparator input ramp rate changes with output voltage. The overshoot voltage can also be viewed as the product of the output voltage slope and the comparator delay,

$$v_{OV} = m\, t_d \tag{5.2}$$

where

$$m = \frac{dv_O}{dt} \tag{5.3}$$

is the output voltage slope.

The constant charging current passing through the finite resistance switches cre-

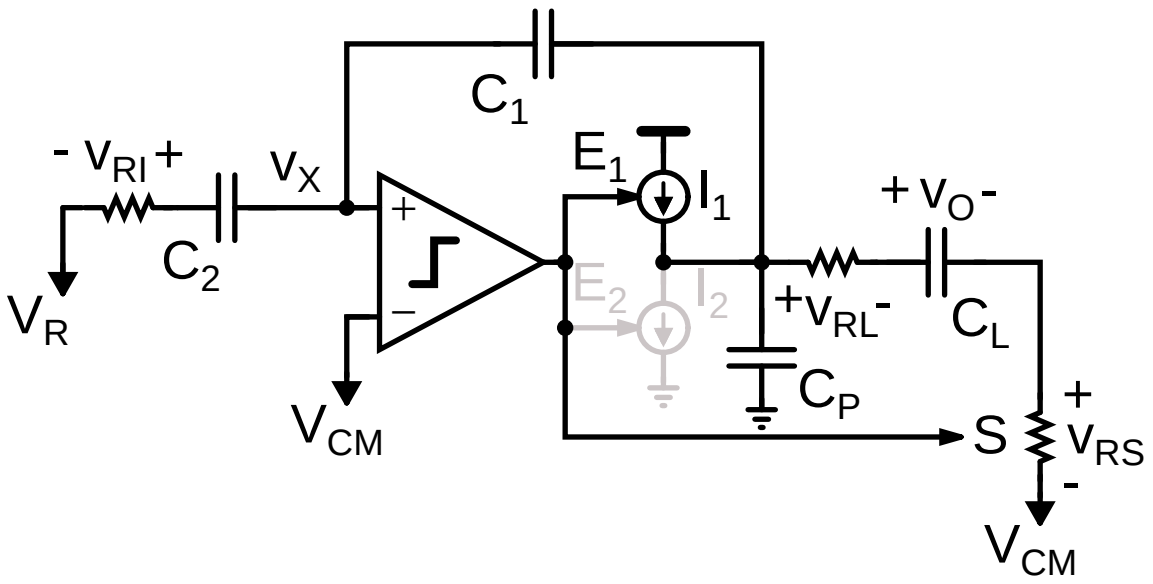


Figure 5-1: Switch resistance errors: v_{RS} and v_{RI} create offset, v_{RL} causes nonlinearity

ates a voltage drop across each switch. Fig. 5-1 shows the effect of the switch resistances on CBSC gain stage during the fine charge transfer phase. The output voltage error due to the voltage drop across the switches is:

$$v_{O\epsilon r} = \frac{C_2}{C_1} v_{RI} + v_{RL} + v_{RS} \tag{5.4}$$

The switch voltage drop $v_{O\epsilon r}$ combines with the output overshoot v_{OV} to produce an output voltage error. The instantaneous output voltage is

$$v_O = \frac{C_1 + C_2}{C_1} v_{IN} - \frac{C_2}{C_1} V_R - V_{CM} + v_{OV} - v_{O\epsilon r}. \tag{5.5}$$

Assuming that $C_1 = C_2$,

$$v_O = 2\, v_{IN} - V_R - V_{CM} + v_{OV} - v_{O\epsilon r}. \tag{5.6}$$

The desired output is

$$v_{Oi} = 2\, v_{IN} - V_R - V_{CM}. \tag{5.7}$$

This leaves an error in the output voltage of

$$v_{O\epsilon} = v_{OV} - v_{O\epsilon r}. \tag{5.8}$$

This error voltage varies as the output voltage varies. Assuming that the input range and output range of the CBSC stage are the same, the average of the error over the input range is

$$V_{O\epsilon} = V_{OV} - V_{O\epsilon r}. \tag{5.9}$$

Where V_{OV} and $V_{O\epsilon r}$ are the average values of the overshoot v_{OV}, and the switch voltage drop $v_{O\epsilon r}$. $V_{O\epsilon}$ is the output referred offset of a single CBSC stage. The offset is input referred by dividing the output referred offset by the gain of the stage. In a pipelined ADC employing digital error correction the output referred offsets of all of the stages can be referred to the input of the ADC and can be removed as a single global offset.

5.1.2 CBSC Nonlinearity

The nonlinearity of a single stage is the amount that the output error voltage changes for a given change in the output voltage. The INL contribution of a single stage is the maximum change in output error $\Delta\, v_{O\epsilon}$ across the output voltage range.

$$\Delta\, v_{O\epsilon} = \Delta\, v_{OV} - \Delta\, v_{O\epsilon r}. \tag{5.10}$$

The INL of an ADC is the sum of the INL contributions of each stage referred to the input of the ADC.

Output Overshoot Variation

The change in overshoot voltage across the output voltage range is the change in the product of the output slope m and the comparator delay t_d

$$\Delta\, v_{OV} = \Delta(m \times\, t_d). \tag{5.11}$$

The average value of the output voltage slope m is

$$M = \frac{I_X}{C_X + C_P + C_L} = \frac{I_X}{C_T}. \tag{5.12}$$

Where C_X, C_P and C_L are the average values of C_x, C_p and C_l, C_T is the average value of the total capacitive load at the output C_t, and I_X is the average value of the charging current i_X. The value of 5.11 depends on the relationship between output ramp rate m and the delay of the comparator. If the comparator delay is independent of the slope of the voltage ramp at its input it is also independent of the output voltage. The change in the overshoot voltage is simply the product of the change in the ramp rate and the comparator delay,

$$\Delta\, v_{OV} = \Delta\, m \times\, T_d. \tag{5.13}$$

Where ramp rate variation ($\Delta\, m$) is produced by variation in the total output capacitance C_t and variation in the charging current i_X. At different output voltages the output slope is different. As shown in fig. 5-2, the different slopes cause the output to overshoot different amounts during the delay time (t_d).

Load capacitance varies with output because the nonlinear junction and gate capacitances connected to the output vary as the output voltage changes. The charging current varies because the current sources have finite output resistance. These two

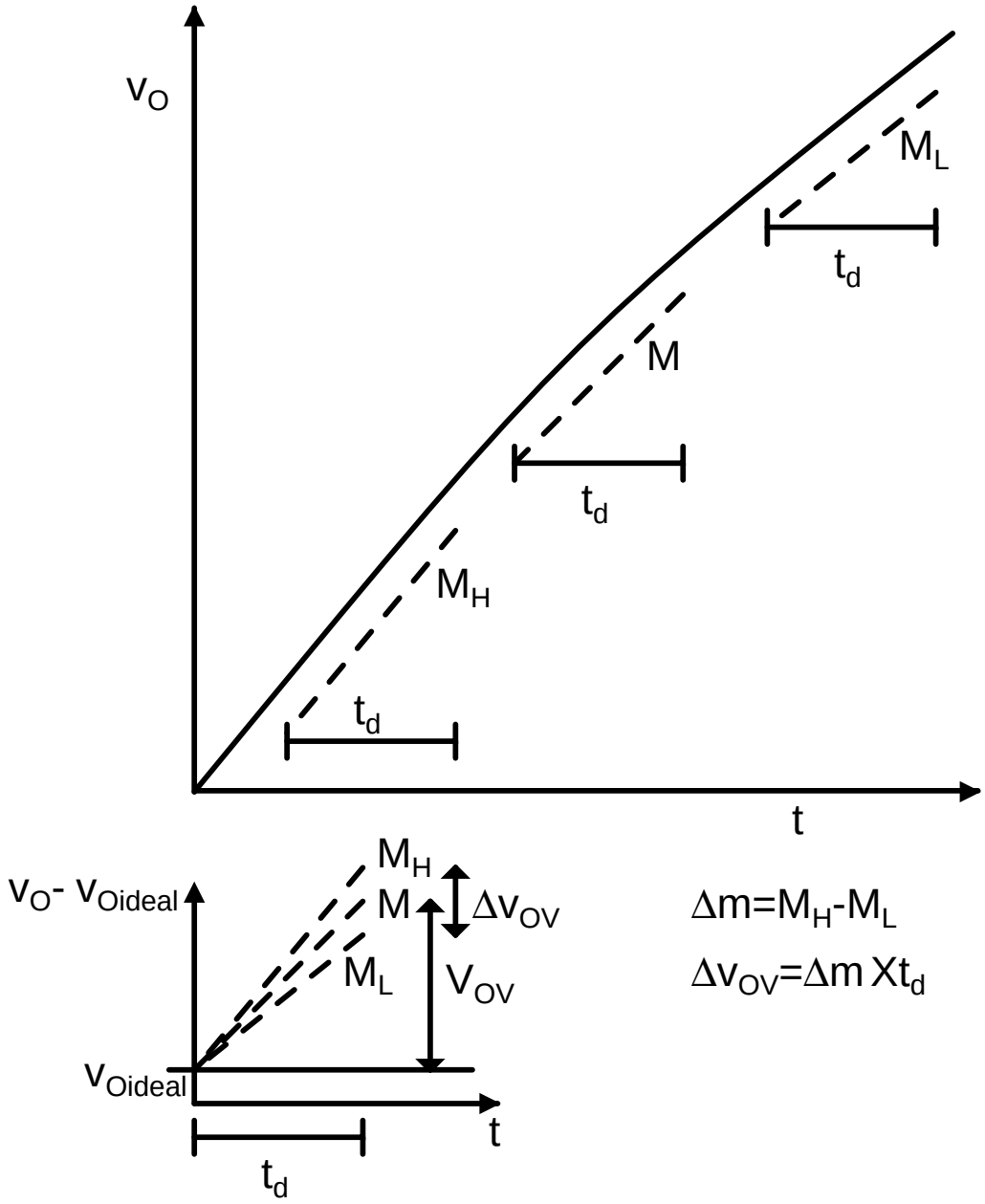


Figure 5-2: Output voltage slope variation : Depending on the output voltage the slope will be different. The difference in the slopes causes the output to overshoot different amounts during the delay time. The output variation is shown for a comparator with a fixed delay.

variations combine to produce slope variation in the following way:

$$\Delta m = \frac{\partial m}{\partial i_X}\Delta I_X + \frac{\partial m}{\partial C_t}\Delta C_T$$
$$\Delta m = \frac{\Delta i_X}{C_T} - \frac{\Delta C_t I_X}{C_T}$$
$$\frac{\Delta m}{M} = (\frac{\Delta i_X}{I_X} - \frac{\Delta c_T}{C_T}) \tag{5.14}$$

The comparator used in the prototype consists of a band-limited integrating preamp that feeds a wide band level detection circuit. The comparator does not have a fixed delay, but rather has a delay that was inversely proportional to the voltage ramp rate at its input. The voltage ramp input becomes a quadratic function at the output of the preamplifier [32]. The delay time of this comparator is the time needed for the output to reach the level detection trip voltage, V_M.

$$t_d = \sqrt{\frac{2 V_M C_i}{m_X G_M}} \tag{5.15}$$

Where G_M is the transconductance of the preamplifier input pair, C_i is the capacitance at the output of the preamplifier and m_X is the slope of the ramp at the input of the comparator. For the prototype m_X is half of the output slope m because a capacitive divider of

$$H = \frac{C_1}{C_1 + C_2} = \frac{1}{2} \tag{5.16}$$

exists between the output of the stage and the input of the comparator. The ramp rate at the input of the comparator is the output ramp rate multiplied by this divider. The divider is similar to the feedback factor in an op-amp system. The output overshoot

is

$$
\begin{aligned}
v_{OV} &= m \times t_d \\
v_{OV} &= \sqrt{\frac{4\, m\, V_M\, C_i}{G_M}} \\
v_{OV} &= \sqrt{\frac{4\, i_X\, V_M\, C_i}{G_M\, C_t}}
\end{aligned} \tag{5.17}
$$

Finding the change in 5.17 for changing ramp rate and substituting 5.14 gives

$$
\begin{aligned}
\Delta\, v_{OV} &= \frac{\partial\, v_{OV}}{\partial\, i_X}\Delta\, i_X + \frac{\partial\, v_{OV}}{\partial\, C_t}\Delta\, C_t \\
\Delta\, v_{OV} &= \frac{1}{2}\sqrt{\frac{4\, V_M\, C_i}{G_M\, C_t}}\frac{1}{\sqrt{i_X}}\Delta\, i_X - \frac{1}{2}\sqrt{\frac{4\, i_X\, V_M\, C_i}{G_M}}\frac{1}{C_t^{\frac{3}{2}}}\Delta\, C_t \\
\Delta\, v_{OV} &= \frac{1}{2}\, M\, T_d\frac{\Delta\, i_X}{I_X} - \frac{1}{2}\, M\, T_d\frac{\Delta\, C_t}{C_T} \\
\Delta\, v_{OV} &= \frac{1}{2}\Delta\, m \times T_d
\end{aligned} \tag{5.18}
$$

An increase in the ramp rate decreases the comparator delay time. This effect partially cancels the effect of ramp rate variation on the overshoot voltage.

A wide band amplifier can also be used as a comparator. The delay of such a circuit is

$$t_d = \frac{V_M\, C_i}{m_X\, A}. \tag{5.19}$$

Where A is the gain of the amplifier. The delay of amplifier is inversely proportional to the voltage ramp rate. As the ramp rate increases the delay decreases proportionally.

The overall effect is that the overshoot voltage does not change.

$$
\begin{aligned}
v_{OV} &= m \times \frac{V_M\, C_i}{m\, A} \\
\Delta\, v_{OV} &= \frac{\partial\, v_{OV}}{\partial\, i_X} \times \Delta\, i_X + \frac{\partial\, v_{OV}}{\partial\, C_t} \times \Delta\, c_T \\
\Delta\, v_{OV} &= 0 \times \Delta\, i_X + 0 \times \Delta\, C_t \\
\Delta\, v_{OV} &= 0
\end{aligned} \tag{5.20}
$$

The effect of the output slope variation on the overshoot voltage is completely canceled by the varying comparator delay.

For the comparator used in the prototype the delay consists of the response time of the first integrating stage t_i and the delay of the level translation stages t_{do}. The delay of the level translation stages is independent of the voltage ramp. The delay of the overall comparator effects the sensitivity of the overshoot voltage to ramp rate changes.

$$\Delta\, v_{OV} = \frac{1}{2}\Delta\, m \times\, T_i + \Delta\, m \times\, T_{do}. \tag{5.21}$$

For simplicity the effect of the level translation stages is neglected in the following analysis. The total delay is assumed to only consist of the integrator response time ($t_d = t_i$).

Switch Resistance Voltage Drop Variation

The change in switch voltage drop across the output voltage range is sum of the change in the voltage drop across each switch.

$$\Delta\, v_{O\epsilon r} = \frac{C_2}{C_1}\Delta\, v_{RI} + \Delta\, v_{RL} + \Delta\, v_{RS}. \tag{5.22}$$

The voltage drop across a each switch is

$$\begin{aligned} v_{RI} &= r_I\, i_X \frac{C_x}{C_t} = r_I\, i_X \frac{C_x}{C_x + C_p + C_l} \\ v_{RL} &= r_L\, i_X \frac{C_l}{C_t} = r_L\, i_X \frac{C_l}{C_x + C_p + C_l} \\ v_{RS} &= r_S\, i_X \frac{C_l}{C_t} = r_S\, i_X \frac{C_l}{C_x + C_p + C_l} \end{aligned} \tag{5.23}$$

For v_{RI} the change in voltage drop across output voltage is

$$\Delta\, v_{RI} = \frac{\partial\, v_{RI}}{\partial\, i_X}\Delta\, i_X + \frac{\partial\, v_{RI}}{\partial\, r_I}\Delta\, r_I + \frac{\partial\, v_{RI}}{\partial\, C_x}\Delta\, C_x + \frac{\partial\, v_{RI}}{\partial\, C_p}\Delta\, C_p + \frac{\partial\, v_{RI}}{\partial\, C_l}\Delta\, C_l. \tag{5.24}$$

$$\Delta\, v_{RI} = R_I \frac{C_X}{C_T}\Delta\, i_X + I_X \frac{C_X}{C_T}\Delta\, r_I + R_I\, I_X \frac{C_P + C_L}{C_T^2}\Delta\, C_x - \frac{R_I\, I_X}{C_T^2}\Delta\, C_p - \frac{R_I\, I_X}{C_T^2}\Delta\, C_l. \tag{5.25}$$

The change in v_{RL} and v_{RS} can be found in the same way. The changes in C_x and C_l can be ignored. Capacitance variation is due to nonlinear junction and gate capacitances. The nonlinear capacitances are from the switches, the current sources and the inputs to the threshold-detection and bit-decision comparators. The output node has much more nonlinear capacitance connected to it than any of the other nodes. The large sampling switches, the bit-decision comparators and the current sources all connect to this node. Therefore only changes in C_p are considered. The switch resistance r_S does not connect to the output node so it does not vary with v_O. The switch resistance r_I only varies as V_R varies. V_R changes between a few discrete values depending on the bit decisions. In the 1.5 b/stage prototype ADC V_R is either the bottom of the input voltage range V_{MIN}, the top of the input voltage V_{MAX} or the middle of the input voltage range V_{CM}. Each of these reference voltages can be adjusted to produce the correct voltage after taking into account the resistance of r_I at that voltage. Using this technique the variation of r_I can be compensated for. Its variation is therefore not a fundamental contribution to nonlinearity and can be ignored. Only the variation is r_L must be considered.

Using the simplifying assumptions above and assuming $C_1 = C_2$ the change in total switch resistance drop at the output is

$$\begin{aligned}\Delta v_{O\epsilon r} &= R_I \frac{C_X}{C_T}\Delta i_X - R_I I_2 \frac{C_X}{C_T^2}\Delta C_p + R_L \frac{C_L}{C_T}\Delta i_X - R_L I_X \frac{C_L}{C_T^2}\Delta C_p + I_X R_L \frac{C_L}{C_T}\Delta r_L \\ &\quad + R_S \frac{C_L}{C_T}\Delta i_X - R_S I_X \frac{C_L}{C_T^2}\Delta C_p. \end{aligned} \tag{5.26}$$

Equation 5.26 is changed to

$$\begin{aligned}\Delta v_{O\epsilon r} &= R_I I_X \frac{C_X}{C_T}\frac{\Delta i_X}{I_X} - R_I I_X \frac{C_X}{C_T}\frac{\Delta C_t}{C_T} + R_L I_X \frac{C_L}{C_T}\frac{\Delta i_X}{I_X} - R_L I_X \frac{C_L}{C_T}\frac{\Delta C_t}{C_T} \\ &\quad + I_X R_L \frac{C_L}{C_T}\frac{\Delta r_L}{R_L} + R_S I_X \frac{C_L}{C_T}\frac{\Delta i_X}{I_X} - R_S I_X \frac{C_L}{C_T}\frac{\Delta C_t}{C_T}. \end{aligned} \tag{5.27}$$

Substituting the average values of the switch resistance voltage drops V_{RI} V_{RL} and V_{RS} leaves

$$\Delta v_{O\epsilon r} = V_{RI}\frac{\Delta i_X}{I_X} - V_{RI}\frac{\Delta C_t}{C_T} + V_{RL}\frac{\Delta i_X}{I_X} - V_{RL}\frac{\Delta C_t}{C_T} + IV_{RL}\frac{\Delta r_L}{R_L} + V_{RS}\frac{\Delta i_X}{I_X} - V_{RS}\frac{\Delta C_t}{C_T}. \tag{5.28}$$

Substituting the average total switch resistance error simplifies 5.28 to

$$\Delta v_{O\epsilon r} = \frac{\Delta i_X}{I_X} V_{O\epsilon r} - \frac{\Delta C_t}{C_T} V_{O\epsilon r} + \frac{\Delta r_L}{R_L} V_{RL}. \tag{5.29}$$

Substituting 5.14 into 5.28 leaves

$$\Delta v_{O\epsilon r} = \frac{\Delta m}{M} V_{O\epsilon r} + \frac{\Delta r_L}{R_L} V_{RL}. \tag{5.30}$$

Finally, combining equations 5.17 and 5.30 leaves

$$\Delta v_{O\epsilon} = \frac{\Delta m}{M}(\frac{1}{2}V_{OV} - V_{O\epsilon r}) - \frac{\Delta r_L}{R_L} V_{RL}. \tag{5.31}$$

Equation 5.31 is the maximum deviation of the output voltage from the average output voltage across the input voltage range. It shows that the nonlinearity of CBSC

circuits is proportional to the overshoot voltage, the voltage drop across switches, the voltage ramp variation and to the switch resistance variation. For the rest of the analysis it is assumed that the ramp rate variation is a much larger source of nonlinearity than the switch resistance variation. It is also assumed that the overshoot voltage is much larger than the switch resistance voltage drop. These assumptions hold true for the prototype. The second assumption simplifies the analysis and makes the results more conservative than they otherwise would be because including the effect of the switch resistance voltage $V_{O\epsilon r}$ reduces the effect of varying ramp rate on the circuit nonlinearity as indicated in equation 5.31. The resulting simplified equation is

$$\Delta\, v_{O\epsilon} \approx \frac{1}{2}\frac{\Delta\, M}{M} V_{OV}. \tag{5.32}$$

For an example, a circuit with a 5 mV final overshoot and a 10% ramp rate variation across the input range, a stage produces a 250 µV nonlinear voltage variation across the output range. For an ADC, this nonliearity can be converted into INL by referring the maximum output voltage variation $\Delta\, v_{O\epsilon}$ to the input of the ADC and comparing it to a LSB voltage. Equations 5.31 and 5.32 apply for a circuit with an integrating comparator. For a circuit with a fixed delay comparator the factor of $\frac{1}{2}$ is replaced by a factor of 1.

5.1.3 Other Sources of Nonlinearity and Offset

Since CBSC circuits contain an initial sampling circuit that is identical to traditional switched capacitor circuits they suffer from the sources of distortion that are associated with the sampling circuit. Both charge injection and switch resistance in the input sampling circuit can create nonlinearity and offset. The traditional bottom plate [22, 23] sampling technique can be used to minimize the susceptibility of the circuit to the effects of input dependent charge injection. Sampling switch bootstrapping [38, 39] or related techniques can be used to minimize the effect of input sampling switch resistance variation on the circuits linearity performance across input

frequency.

5.2 Techniques to Increase Accuracy in CBSC Circuits

The design of highly accurate CBSC based systems requires the use of circuit techniques that reduce circuit offset and nonlinearity. In this section, the operation of these techniques is explained.

5.2.1 Multiple Ramps

The offset and nonlinearity of a CBSC stage are proportional to the charging current. A large charging current produces a large overshoot and consequently a large offset. Additionally, the output voltage nonlinearity is the product of the percentage change in the ramp rate and the overshoot voltage. For a given percentage change in the ramp rate the nonlinearity is reduced by reducing the overshoot. In order to produce a small overshoot and to achieve a low level of nonlinearity at a high speed, two or more charge transfer phases can be used. The charging current can be reduced from one charge transfer phase to the next to reduce the overshoot and nonlinearity.

5.2.2 Overshoot Correction

Overshoot Correction Techniques

During the coarse charge transfer phase a large charging current is used to achieve a rough estimate of the output voltage. A the end of this phase the output voltage result has a relatively large offset and correspondingly large nonlinearity. The switches can be made to have a small enough resistance so that the voltage overshoot dominates the offset and nonlinearity. Since the offset is the same for all inputs it can be canceled. One way to do this is to change the voltage that the level detection comparator compares to v_X. This operation is shown in Figure 5-3.

Limits to Overshoot Correction

Two factors limit the amount of overshoot cancellation. The first limitation is that for all inputs the input to the threshold-detection comparator v_X must exceed the comparator threshold at the end of the coarse phase for the circuit to operate correctly. This means that the output voltage will exceed the ideal output voltage for all inputs. The nonlinearity of the overshoot and switch voltage drop determines the minimum overshoot that needs to be allowed. The output that produces the smallest overshoot must at least reach the ideal output value. If the smallest overshoot is completely canceled the largest residual overshoot will be

$$V_{OVr} = \Delta m\, t_d, \tag{5.33}$$

assuming that the comparator delay is fixed. If an integrating type comparator is used the residual overshoot will be half of 5.33 because as is shown in equation 5.18 the integrating comparator cancels half of the overshoot variation caused by a varying ramp rate. The maximum overshoot correction and resulting residual overshoot is shown in Figure 5-4. Equation 5.33 can be rewritten as

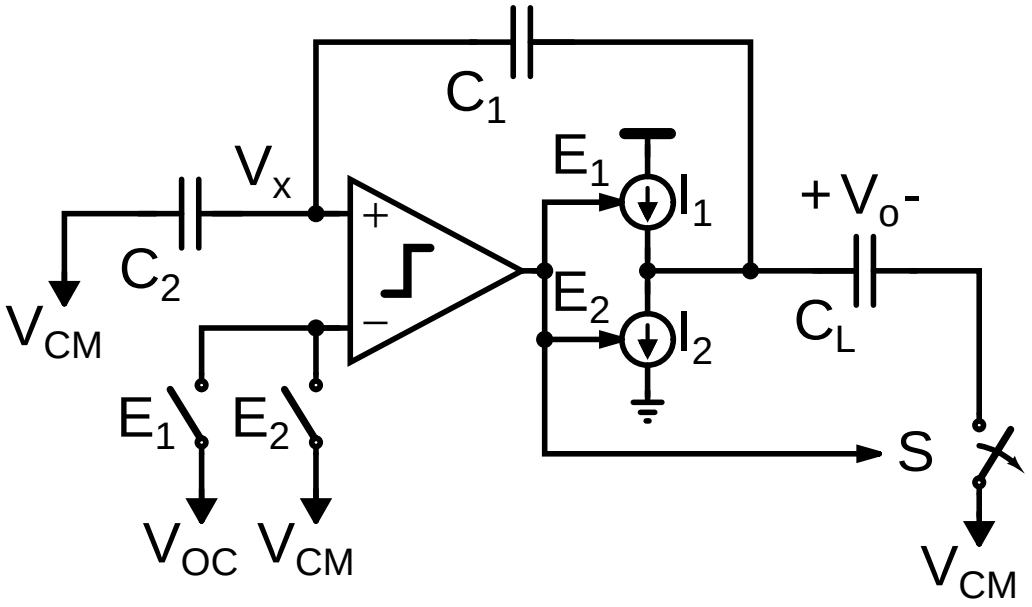
$$V_{OVr} = \frac{\Delta m}{M} V_{OV}. \tag{5.34}$$

Where V_{OV} is the original average uncorrected overshoot voltage. The maximum overshoot correction at the input to the comparator is then the minimum uncorrected output overshoot divided by the closed loop gain of the stage.

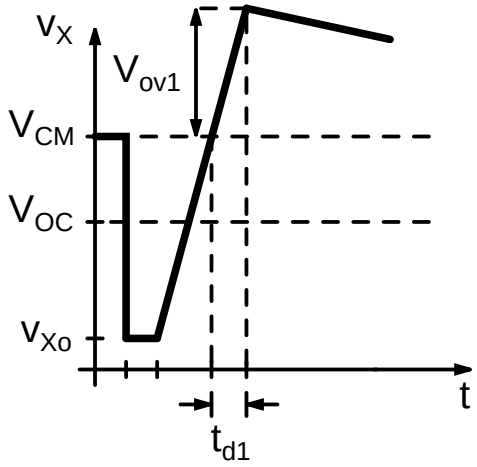
$$V_{COR} = \frac{C_1}{C_1 + C_2} V_{OVMIN}. \tag{5.35}$$

Where

$$V_{OVMIN} = V_{OV} - \frac{\Delta m}{2} t_d. \tag{5.36}$$



(a)



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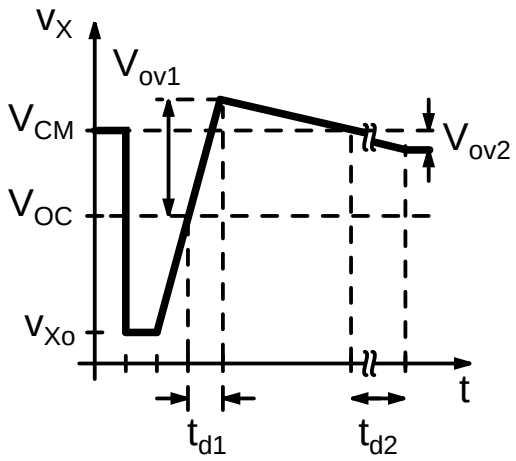


(c)

Figure 5-3: Overshoot cancellation. (a) CBSC stage with overshoot cancellation. (b) v_X node voltage during the charge transfer phase without overshoot correction. The large overshoot during the coarse phase prevents the charge transfer operation from finishing in allowed time. (c) CBSC stage with overshoot cancellation.

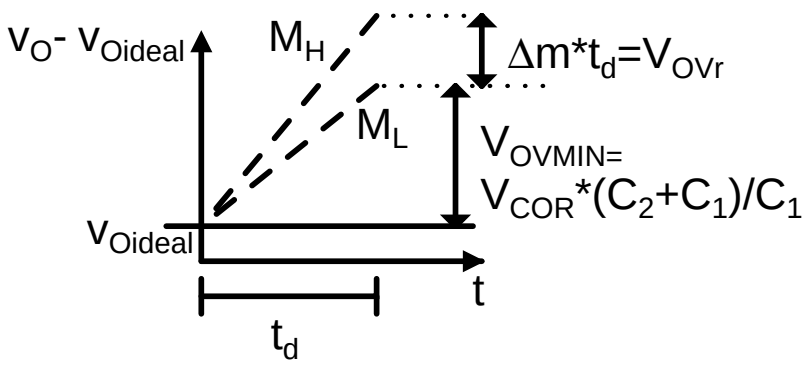


Figure 5-4: The maximum overshoot correction is determined by the ramp linearity. The output must overshoot for all input voltages. The smallest overshoot is completely canceled and the largest residual overshoot depends on the ramp nonlinearity and the value of the original uncorrected overshoot, V_{OV}.

assuming that average ramp rate M is half way between the maximum and minimum ramp rates. Equation 5.35 simplifies to

$$V_{COR} = \frac{C_1}{C_1 + C_2} V_{OV} (1 - \frac{1}{2} \frac{\Delta m}{M}) \tag{5.37}$$

V_{OC} is set at a voltage V_{COR} below V_{CM}

$$V_{OC} = V_{CM} - \frac{C_1}{C_1 + C_2} V_{OV} (1 - \frac{1}{2} \frac{\Delta m}{M}) \tag{5.38}$$

A trade off exists between output signal range and overshoot correction. The minimum possible output voltage V_{MIN} must be greater than the amount of overshoot that is corrected at the output. Referring this limitation to the input of the comparator requires dividing by the stage gain $\frac{C_1+C_2}{C_1}$;

$$V_{CORMAX} = \frac{C_1}{C_1 + C_2} V_{MIN}. \tag{5.39}$$

If the overshoot is corrected by more than V_{CORMAX}, v_X will start above V_{OC} and the circuit will not work. Using an overshoot correction greater than V_{CORMAX} would require the comparator to trip when the output is less than 0V. This overshoot correction limitation, shown in Figure 5-5, sets an absolute maximum on the amount of

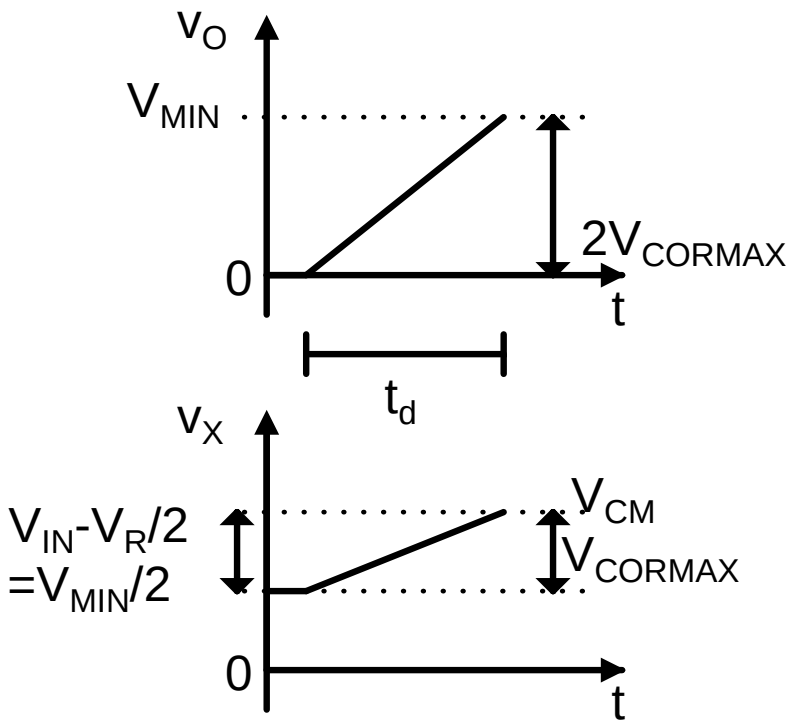


Figure 5-5: The maximum possible overshoot correction (V_{CORMAX}) is determined by the minimum output voltage.

overshoot correction of any CBSC circuit. Therefore the steepest ramp allowed in a CBSC circuit is the one that produces an uncorrected overshoot of V_{MIN} with the given comparator delay time.

5.3 Limitation of Linearity and Speed

As in op-amp based circuits, a trade off exists in CBSC circuits between accuracy, speed and power consumption. In order to achieve a certain accuracy a circuit must produce sufficiently low noise as well as being sufficiently linear. Sepke [32] examines the noise performance of CBSC circuits and determines the power consumption required to achieve specific noise performance. In a similar fashion, the additional power consumption required to achieve a specific linearity can also be determined. This analysis involves a number of steps. First, the maximum allowed final overshoot is determined from the linearity requirement. Then, the number of comparator de-

lays required to achieve the desired linearity or alternatively the largest fraction of the charge transfer phase that can be occupied by the comparator delay and still achieve the desired linearity is determined. Finally these two results are used along with the results from Sepke's analysis to determine the transconductance required to achieve a certain linearity and noise performance. The required circuit power consumption is then determined from the required transconductance.

5.3.1 Linearity and Overshoot

For a specific nonlinearity requirement a maximum allowed final overshoot can be determined. For a 1.5 b/stage pipelined ADC, if a $\frac{1}{2}$ LSB INL contribution from the first stage is acceptable a 1 LSB voltage variation can be allowed at the output of this stage. The LSB voltage equals

$$V_{LSB} = V_{FS}\, 2^{-B}. \tag{5.40}$$

Since the prototype used a integrating type comparator, Equation 5.32 is combined with 5.40 to produce

$$\frac{1}{2}\frac{\Delta m}{M}\, V_{OV} = V_{FS}\, 2^{-B}. \tag{5.41}$$

The maximum allowed output voltage overshoot for the first stage is then

$$V_{OVMAX} = \frac{V_{FS}\, 2^{-B}}{\frac{1}{2}\frac{\Delta m}{M}}. \tag{5.42}$$

For a comparator with a fixed delay the maximum allowed output voltage overshoot for the first stage is

$$V_{OVMAX} = \frac{V_{FS}\, 2^{-B}}{\frac{\Delta m}{M}}. \tag{5.43}$$

This overshoot value determines the maximum final ramp rate for stage assuming a given comparator delay. For the previously described gain stage, assuming that the capacitor sizes were determined from $\frac{kT}{C}$ noise considerations, the maximum final

phase current can be determined. Sepke [32] shows that the final voltage overshoot can be used, along with other factors, to determine the threshold detection comparator performance needed to achieve a circuit noise specification.

5.3.2 Linearity-Speed Trade Off

A trade off between linearity and speed exists in both op-amp based circuits and CBSC circuits. An op-amp based circuit must settle for a certain number of time constants to reach a sufficiently accurate result. CBSC circuits require short enough comparator delay to reach the same result.

The comparison between a time constant and a comparator delay time is appropriate because both are proportional to the overall power consumption of the circuit. For a single-stage op-amp frequency compensated by the load capacitance, the settling time constant (τ_o) equals

$$\tau_o = \frac{1}{\omega_{3dB}}. \tag{5.44}$$

Where the 3dB frequency is

$$\omega_{3dB} = \frac{G_m}{C_L} F. \tag{5.45}$$

F is the feedback factor and G_m is the transconductance of the op-amp input pair. In a gain of two stage the feedback factor is $\frac{1}{2}$. Figure 5-6(a) demonstrates the relationship between the time constant and the speed of the circuit. The circuit requires n time constants to settle. For example for to settle to 13 bits or .01% the circuit must settle for 9 time constants. The the half clock cycle equals

$$\frac{T}{2} = n\tau_o. \tag{5.46}$$

Given that the sampling frequency equals

$$f_s = \frac{1}{T}, \tag{5.47}$$

5.44 5.45 5.46 and 5.47 are combined to show

$$G_m = 4C_L\, f_s\, n. \tag{5.48}$$

For a specific speed the required transconductance is proportional to the required number of time constants, n. Transconductance translates into a power consumption through the relationship between G_m and I_D for the input transistors of the comparator. For sub-threshold operating points,

$$G_m \propto I_D \tag{5.49}$$

and for devices operating in strong inversion,

$$G_m \propto \sqrt{I_D}. \tag{5.50}$$

The same relationship between transconductance, linearity and speed that exists for op-amp based circuits also exists for CBSC circuits [32]. An integrating type comparator produces an output current

$$i_{Ocomp} = G_m\, v_{Icomp}, \tag{5.51}$$

proportional to the input voltage,

$$v_{Icomp} = m_x\, t. \tag{5.52}$$

Where G_m is the transconductance of the integrator and m_X is the voltage slope at the input of the comparator. The output current i_{Ocomp} is integrated on the comparator load capacitance C_i to produce a quadratic output voltage,

$$v_{Ocomp} = \frac{G_m}{C_i}\, m_X\, t^2. \tag{5.53}$$

Assuming that the comparator delay time equals the time the required for the output of the integrator to reach the level detection stage threshold voltage, V_M ($t_i = t_d$)(See Section 5.1.2). The integrating comparator flips when its output reaches a voltage threshold (V_M). Solving for the comparator delay t_d leaves

$$t_d = \sqrt{\frac{2\,V_M\,C_i}{m_X\,G_M}}. \tag{5.54}$$

Solving 5.54 for G_M produces

$$G_M = \frac{2\,V_M\,C_i}{m_X\,t_d^2}. \tag{5.55}$$

The output overshoot voltage can be shown to be

$$V_{OV} = t_d\,2\,m_x. \tag{5.56}$$

Figure 5-6(b) demonstrates the relationship between the comparator delay time and the speed of the circuit. Assuming, the comparator delay time takes up a fraction (α) of the half clock cycle,

$$\frac{T}{2} = \frac{1}{\alpha}\,t_d. \tag{5.57}$$

Equations 5.55 5.56 and 5.57 are combined to show

$$G_M = 8\,C_L\,f_s\frac{1}{\alpha}\frac{V_M}{V_{OV}}. \tag{5.58}$$

Similarly to the op-amp circuit, for a specific speed the required transconductance is proportional $\frac{1}{\alpha}$, the number of comparator delays that fit in a half clock period. The time constant of the op-amp circuit or alternatively the delay time of the comparator must be small enough to meet a specific speed and accuracy requirement. An analysis is made to determine the minimum power consumption needed to achieve a certain linearity assuming two different types of comparators: a comparator with a fixed delay and an integrating type comparator with a delay that is inversely proportional to the square root of the voltage ramp rate at its input.

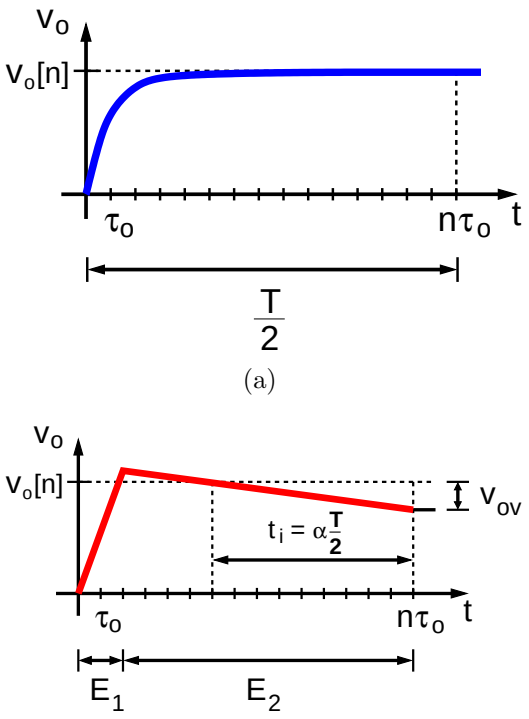


Figure 5-6: Noise bandwidth comparison. (a) Op-amp time constant (τ_o). (b) Comparator delay ($t_d \approx t_i$).

Comparator with a Fixed Delay

In order to simplify the analysis, first a CBSC circuit with a fixed delay is considered. The optimal number of voltage ramps and the slope of each ramp must be determined to determine the minimum power consumption needed to achieve a certain linearity. Depending on the required bit resolution a different number of charge transfer phases are used, each with a different output voltage ramp. In the prototype two ramps were used, for lower bit resolutions a single ramp is used and for higher bit resolutions three ramps are used.

The slope of the final ramp is derived from equation 5.42. Assuming a fixed delay the final ramp rate is

$$M_{MAX} = \frac{V_{OVMAX}}{t_d} \tag{5.59}$$

For the example gain stage the final phase output current will be the maximum ramp rate (M_{MAX}) divided by the total load capacitance. This capacitance includes the sampling capacitors of the stage ($\frac{1}{C_X} = \frac{1}{C_{1,i}} + \frac{1}{C_{2,i}}$), the sampling capacitors of the next stage ($C_L = C_{1,i+1} + C_{2,i+1}$) and the total parasitic capacitance at the output (C_P). The size of the sampling capacitors for each stage is determined by the $\frac{kT}{C}$ noise sampled by these capacitors. As in op-amp circuits the noise generated during the sampling operation is proportional to $\sqrt{\frac{kT}{C}}$, where the C is the total sampling capacitance. The sampling capacitors of the first stage suffer from $\frac{kT}{C}$ noise in the traditional way. Sepke [32] shows that for CBSC stages other than the first stage, the $\frac{kT}{C}$ sampled noise is less than the sampling noise of op-amp based circuits.

For a single ramp circuit, the time required to transfer all of the sampled charge and to achieve a specific linearity is the output voltage divided by the voltage ramp rate, M_{MAX}. The circuit must be fast enough to complete the charge transfer for all outputs during the half clock cycle. The circuit requires the longest amount of time to transfer charge for highest possible output voltage V_{MAX}. This voltage therefore

is used in the analysis and the minimum time need for charge transfer is

$$t_1 = \frac{V_{MAX}}{M_{MAX}}. \tag{5.60}$$

The required number of comparator delays is therefore

$$m_1 = \frac{V_{MAX}}{V_{OVMAX}}. \tag{5.61}$$

Substituting the result from equation 5.43 for a comparator with a fixed delay gives

$$m_1 = \frac{V_{MAX}}{V_{FS}} 2^B \frac{\Delta m}{M}. \tag{5.62}$$

As the required bit resolution becomes smaller the allowable overshoot becomes larger and the number of required comparator delay times becomes smaller. When the overshoot reaches V_{MIN}, the minimum input voltage, it can no longer be canceled. This places an upper limit on the overshoot voltage and a lower limit on the required number of delay times of

$$m_{1min} = \frac{V_{MAX}}{V_{MIN}}. \tag{5.63}$$

In order to determine the required number of delay times needed in a circuit with two charge transfer phases the ramp rates of the coarse and fine voltage ramps must be determined. The ramp rate of the fine ramp is determined from the linearity requirement to be M_{MAX} from equation 5.59. The ramp rate for the coarse ramp is chosen so that the overall charge transfer time is minimized. The output voltage of the two ramp circuit for the maximum output voltage is shown in figure 5-7. The maximum possible output voltage is analyzed because this is the case that requires the longest time to complete the coarse charge transfer phase and thus requires the longest time to complete the total charge transfer.

The minimum charge transfer time occurs when the time needed to reach the output voltage during the coarse phase, t_1, equals the overshoot recovery time, t_2. A greater coarse ramp rate shortens the initial charging time, but creates a larger

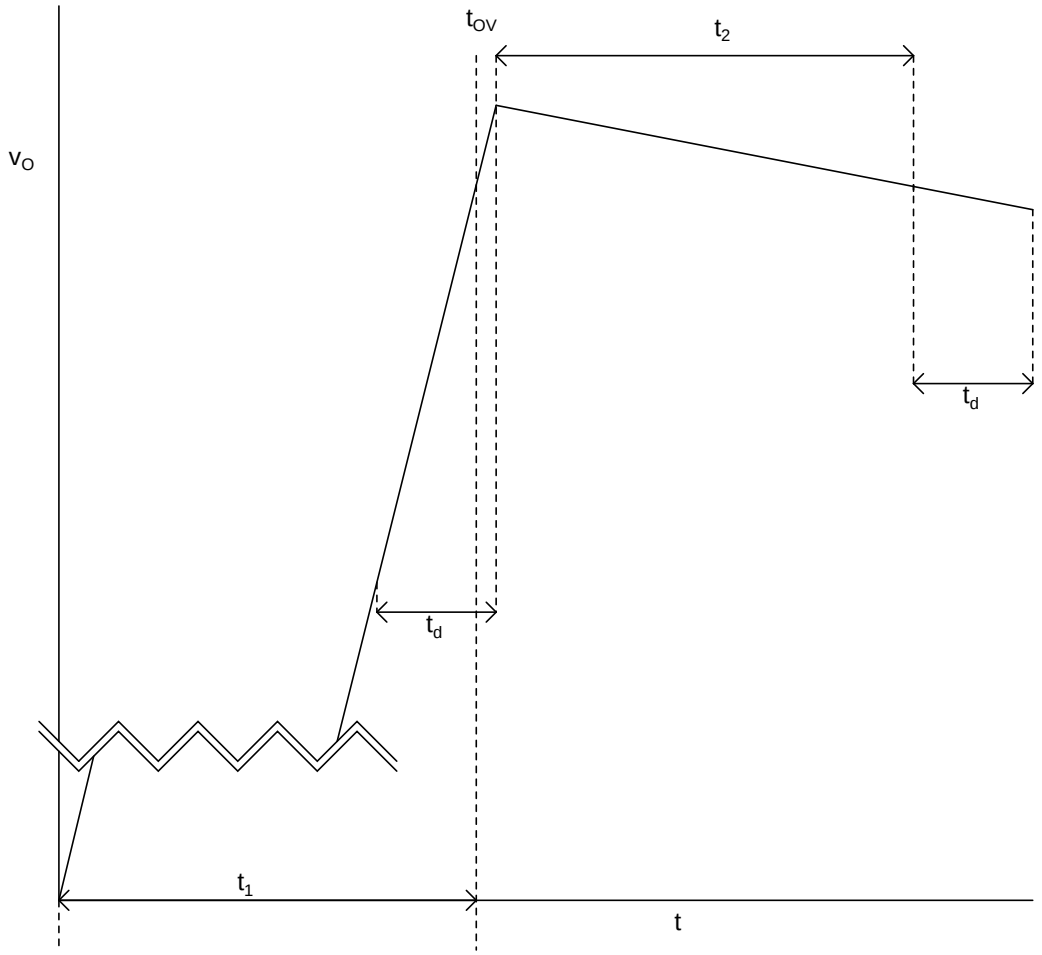


Figure 5-7: Two-phase circuit output voltage: The minimum charge transfer time is achieved when t_1=t_2.

overshoot and therefore lengthens the overshoot recovery time, while a lessor coarse ramp rate lengthens the initial charging time, but creates a smaller overshoot and therefore shortens the overshoot recovery time. The total charge transfer time is derived in Appendix A. It equals

$$m_2 = \frac{V_{MAX}}{V_{OV1}} + \frac{\Delta m}{M} + \frac{\Delta m}{M}\frac{V_{OV1}}{V_{OV2}} + 1. \tag{5.64}$$

comparator delays. Substituting 5.42 for V_{OV2} and using the value of V_{OV1} that causes $t_1 = t_2$ derived in Appendix A simplifies 5.64 to

$$m_2 = \frac{\Delta m}{M}\sqrt{\frac{V_{MAX}}{V_{FS}}}\,2^{\frac{B}{2}+1} + \frac{\Delta m}{M} + \frac{\Delta m}{M} + 1. \tag{5.65}$$

This equation is not valid for low bit resolutions. At a lower number of bits the values of V_{OV1} and V_{OV2} exceed the maximum allowable value. Constraining the overshoot voltages produces an m_2 value that is larger than that predicted by equation 5.65 for low bit resolutions.

To produce a very highly accurate CBSC circuit the use of three voltage ramps may be required. To achieve $\frac{1}{2}\ LSB$ INL at the input of a circuit requires

$$m_3 = \frac{V_{MAX}}{V_{OV1}} + \frac{\Delta m}{M} + \frac{\Delta m}{M}\frac{V_{OV1}}{V_{OV2}} + 1 + \frac{\Delta m}{M}\frac{V_{OV2}}{V_{OV3}} + 1 \tag{5.66}$$

comparator delays. The derivation of 5.66 is found in Appendix A.2. Further simplification is made using equation 5.42 and the values of V_{OV1} and V_{OV2} found in Appendix A.2,

$$m_3 = 3\,\frac{\Delta m}{M}\sqrt[3]{\frac{V_{MAX}}{V_{FS}}}\,2^{\frac{B}{3}+\frac{1}{3}} + \frac{\Delta m}{M} + 2. \tag{5.67}$$

This minimum value for this equation is constrained by the maximum ramp rate limitation.

Figure 5-9 shows a plot of the number of comparator delay verses bits for a one, two and three ramp CBSC system and the number of time constants verses linearity in terms of bits for an op-amp system. For an op-amp the required minimum number

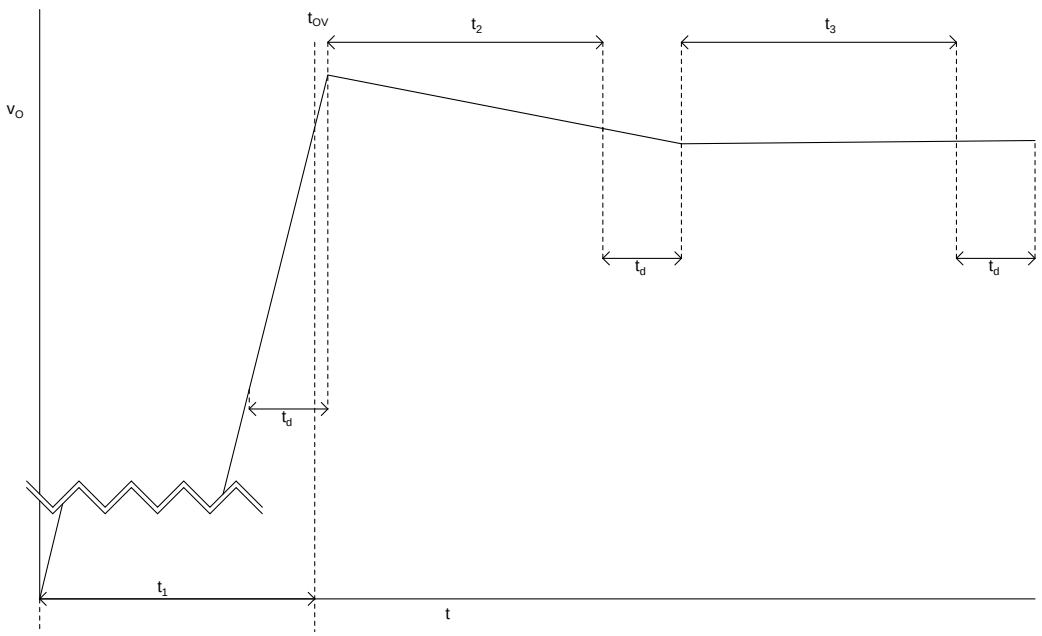


Figure 5-8: Three-phase circuit output voltage

of time constants is linearly proportional to the number of bits.

$$n = B\,ln(2) \tag{5.68}$$

The number of comparator delays for a CBSC circuit is proportional to the ramp linearity and two raised to the number of bits divided by the number of ramps.

$$m_{\#R} \propto \frac{\Delta\, m}{M} \sqrt[\#R]{\frac{V_{MAX}}{V_{FS}}}\, 2^{\frac{B}{\#R}} \tag{5.69}$$

For lower bits only one ramp needs to be used. For higher bit levels using two ramps produces a faster or lower power consuming circuit and at the highest bit levels ($B > 14$) three ramps are preferred. The plot shows the curves for a 1% ramp nonlinearity. Figure 5-10 shows how the output voltage changes as the required bit resolution declines. This plot traces the two ramp system line from higher to lower bit resolution. As the required bit resolutions declines, V_{OV2} and V_{OV1} can increase and the required number of delays (m) can decrease. Figure 5-11 shows how the required number of delays increases as the ramp becomes less linear.

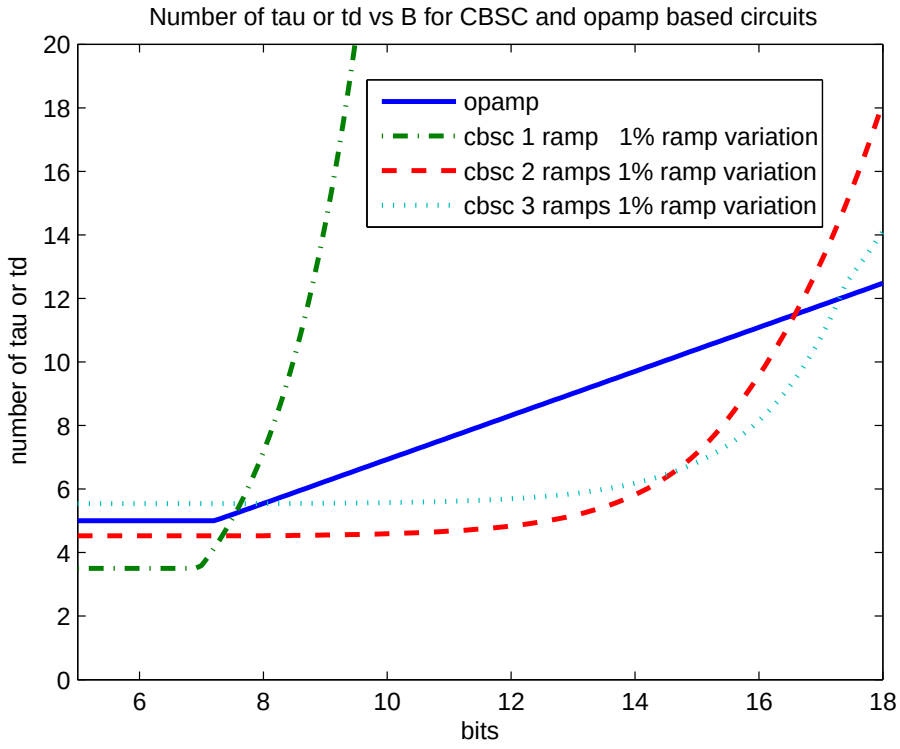


Figure 5-9: Number of comparator delays or time constants vs linearity in terms of Bits. The values used were the same as those used in the prototype. The full scale voltage V_{FS} is 1.0 V. The minimum input voltage V_{MIN} is 0.4 V. The maximum input voltage V_{MAX} is 1.4 V.

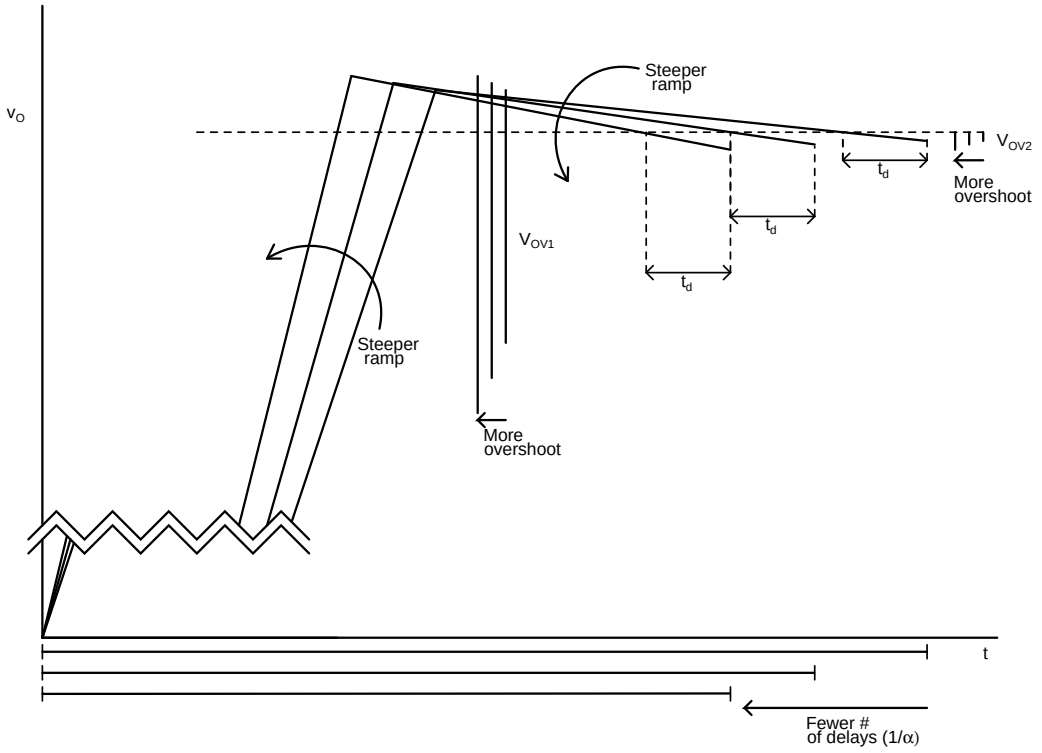


Figure 5-10: V_{OUT} for a two ramp system. As the required bit resolutions declines, V_{OV2} and V_{OV1} can increase and the required number of delays ($\frac{1}{\alpha}$) can decrease.

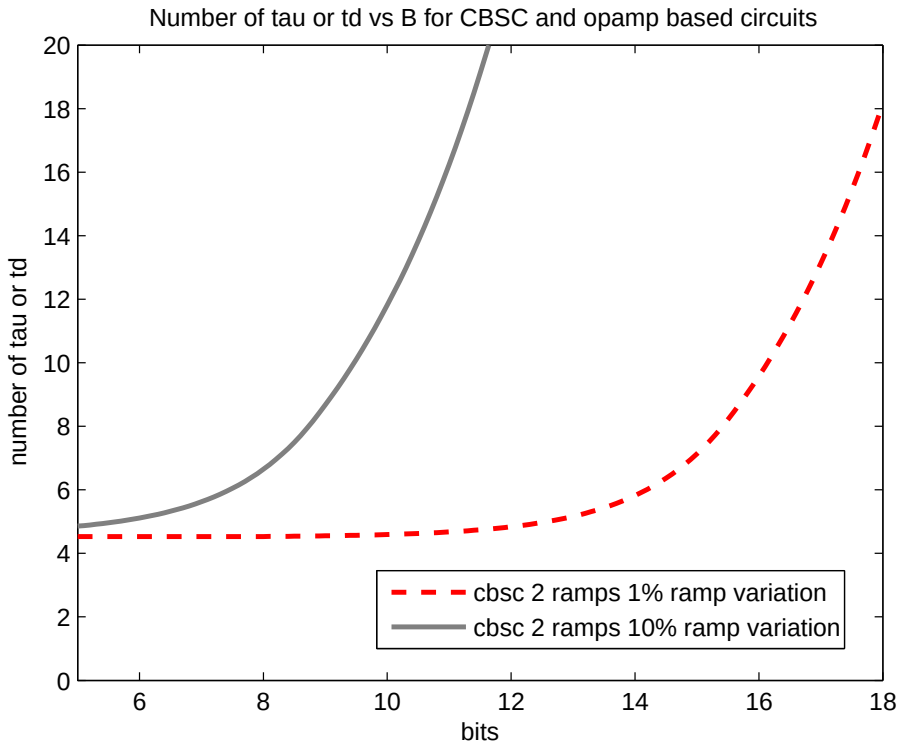


Figure 5-11: Two-phase number of comparator delay vs Bits

Integrating Type Comparator

The linearity analysis for a CBSC circuit with an integrating comparator is similar to the above analysis with a fixed delay comparator. The primary difference is that, for CBSC circuits with more than one ramp, the number of comparator delays needed to achieve a certain linearity is not independent of the speed of the circuit. The comparator delay during each phase is not equal. Except for the final phase a fast fixed delay comparator can used because a large amount of noise can be tolerated. For the final phase, a low noise integrating type comparator can be used. It is therefore not possible to divide the total charge transfer time by a single comparator delay to produce a number of required comparator delays, m. Therefore instead of determining the number of comparator delays needed to achieve a certain linearity, the maximum portion (α) of the half clock cycle that can taken up by the final comparator delay for a specific operating speed is determined. From the fraction α the transconductance needed to achieve a certain linearity at a specific operating speed is determined.

A number of assumptions are made to simplify the analysis. Different comparators are assumed to be used for each phase. The comparators used in the initial charge transfer phase or phases are assumed to use very little power. The input pair of the comparator used in the final phase is assumed to consume the majority of the power supplied to the circuit. The power consumption of the comparator used in the final charge transfer phase depends on its required transconductance. As is shown in section 5.3.2 for op-amps, the operating region of the input transistors determine the power consumption of the comparator.

For a single slope system the required number of comparator delays is the same whether an integrating comparator or a fixed delay comparator is used.

$$m_1 = \frac{V_{MAX}}{V_{OVMAX}}. \tag{5.70}$$

or

$$m_1 = \frac{V_{MAX}}{V_{FS}}\, 2^{B+1}\, \frac{\Delta\, m}{M}. \tag{5.71}$$

Sepke [32] shows that the required transconductance of the preamplifier input pair is

$$G_M = \frac{2}{t_i} \frac{V_M}{V_{OVX}} C_i. \tag{5.72}$$

Where t_i is the portion of the comparator delay that occurs while the preamplifier is integrating. For simplicity, it is again assumed for this analysis that the delay time t_d only consists of this integration time. V_{OVX} is the final overshoot voltage at the input to the comparator. For the 1.5 b/stage ADC V_{OVX} is half of the output overshoot, V_{OV}. It is calculated using equation 5.42. C_i is determined from a mean-squared noise specification $\bar{v_n^2}$,

$$C_i = \frac{G_N}{G_M} \frac{V_{OVX}}{V_M} \frac{k\,T}{\bar{v_n^2}}. \tag{5.73}$$

Where G_N is the noise conductance of the input pair. $\frac{G_N}{G_M}$ is equal to $\frac{2}{3}$ the effective number of devices of noise at the input to the comparator. For a single slope system equation 5.72 can be further simplified by substituting 5.73 for C_i and by substituting $t_i = \frac{\frac{2}{T}}{m_1} = \frac{1}{2\,f_s\,m_1}$ for t_i,

$$G_M = 4\,f_s\,m_1 \frac{G_N}{G_M} \frac{k\,T}{\bar{v_n^2}}. \tag{5.74}$$

Substituting 5.71 into 5.74 produces

$$G_{M1} = 4\,f_s \frac{G_N}{G_M} \frac{k\,T}{\bar{v_n^2}} \frac{V_{MAX}}{V_{FS}} 2^{B+1} \frac{\Delta\,m}{M}. \tag{5.75}$$

For two and three slope CBSC circuits G_M and t_i are solved together using 5.72 and a linearity constraint. It is assumed that only the final slope uses an integrating comparator. The other slope or slopes use a fixed delay comparator. The time required for a two ramp CBSC circuit to complete charge transfer is

$$t_{t2} = \frac{V_{MAX}}{M_1} + \frac{\Delta\,m}{M}\,t_{d1} + \frac{\Delta\,m}{M}\frac{M_1}{M_2}\,t_{d1} + t_{d2}. \tag{5.76}$$

Equation 5.76 is derived in Appendix A.1. As in the analysis of CBSC using a fixed delay comparator the optimal coarse ramp M_1 is found which produces the minimum

charge transfer time t_{t2}. The minimum charge transfer time is then set equal to a half period $\frac{T}{2}$ and the result is solved for the maximum allowable delay time for a two phase CBSC circuit operating at a frequency of $\frac{1}{T}$. The maximum allowable delay time is shown in Appendix A.1 to be

$$t_{d2} = \frac{T}{2} - \frac{\Delta m}{M} t_{d1} + 2\frac{V_{MAX}}{V_{OV2}} \frac{\Delta m}{M} t_{d1} \left(1 - \sqrt{1 - \frac{V_{OV2}}{V_{MAX}} + \frac{1}{2} \frac{V_{OV2}}{V_{MAX}} \frac{t_{d1}}{T} \frac{1}{\frac{\Delta m}{M}}} \right). \quad (5.77)$$

The time required for a three slope CBSC circuit to complete charge transfer is shown in Appendix A.2 to be

$$t_{t3} = \frac{V_{MAX}}{M_1} + \frac{\Delta m}{M} t_{d1} + \frac{\Delta m}{M} \frac{M_1}{M_2} t_{d1} + t_{d2} + \frac{\Delta m}{M} \frac{M_2}{M_3} t_{d1} + t_{d3}. \quad (5.78)$$

Solving equation 5.78 for t_{d3} at a specific sampling frequency requires solving a cubic equation that produces a very complicated result which is omitted here.

Figure 5-12 shows the relationship between linearity and the fraction of the clock cycle α that can be taken up by the final phase comparator delay.

$$\alpha = \frac{t_{d2}}{\frac{T}{2}} \; or \; \frac{t_{d3}}{\frac{T}{2}} \quad (5.79)$$

The fraction of the clock cycle taken up by the comparator delay for two and three slope CBSC circuits is compared to the fraction of of the clock cycle taken up by the time constant of an op-amp based circuit. The circuits are required to have less than $\frac{1}{2}$ LSB INL referred to their inputs. The comparator for the last phase is assumed to be an integrating type comparator. For the other phases a comparator with a fixed delay is assumed. The power consumption of the fixed delay comparators are neglected. For this plot a operating frequency of 10 MHz, a ramp linearity of 1%, and a fixed delay of 500 ps are assumed. The fixed delay is 1% of the half clock cycle. The plot of α will not change for different sampling frequencies as long the ratio of the fixed delay length to the length of the half clock cycle stays the same. The maximum length of the comparator delays are constrained by the maximum overshoot condition

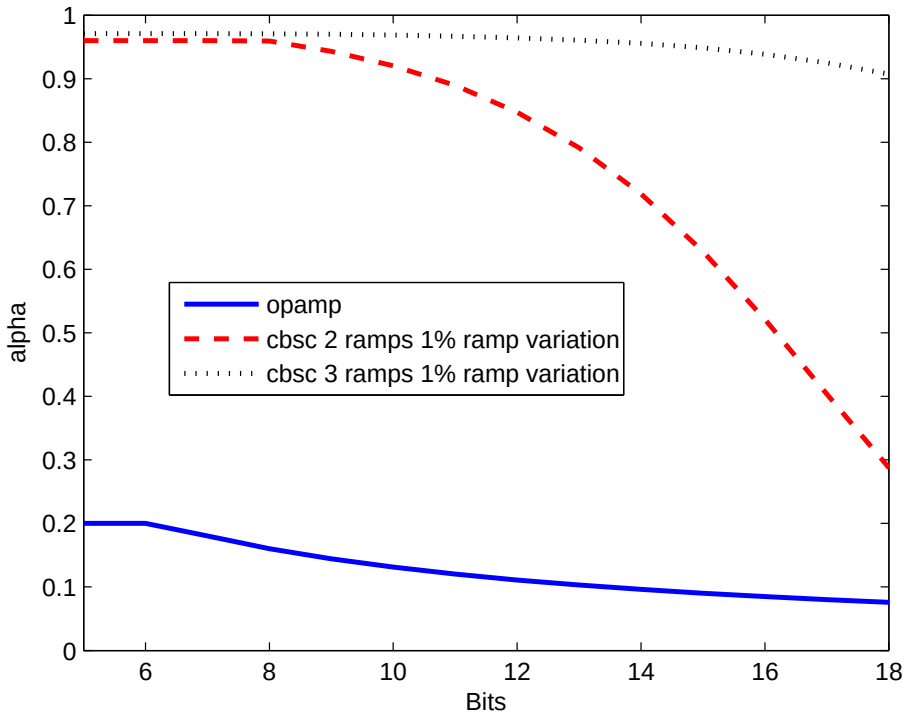


Figure 5-12: Fraction (α) of the half clock cycle, $\frac{T}{2}$ occupied by the final phase comparator delay t_{d2} vs. Linearity with an integrating final comparator. The linearity of each circuit is required to be $\frac{1}{2}$ LSB referred to the input. The sampling frequency is 10 MHz and first and second fixed ramp delays are each 1% of the half clock cycle ($t_{d1} = 500\,\text{ps}$).

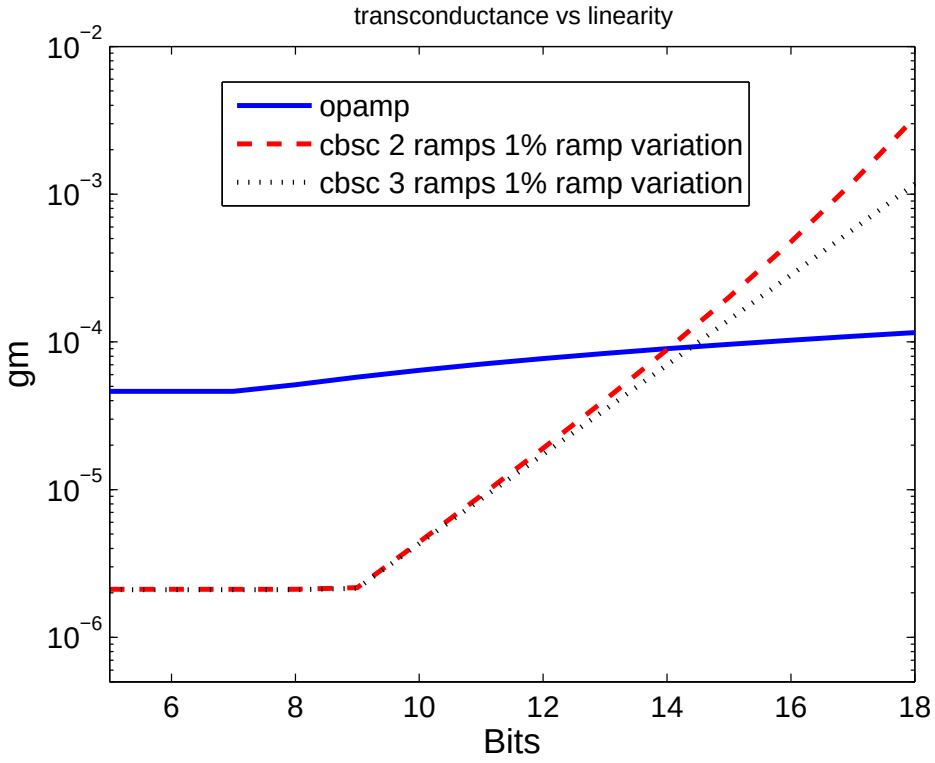


Figure 5-13: Transconductance vs. Linearity with an integrating final comparator: The linearity of each circuit is required to be $\frac{1}{2}$ LSB at the input. The sampling frequency is 10 MHz and first and second fixed ramp delays are each 500 ps.

in the same way that the minimum number of comparator delay were constrained in the previous section.

Figure 5-13 shows the relationship between linearity and comparator transconductance for two and three slope CBSC circuits verses that of op-amp based circuits for $\frac{1}{2}$ LSB INL referred to their inputs. The Figure is made under the same conditions as Figure 5-12. The minimum transconductances are constrained by the maximum overshoot condition in the same way that the minimum number of comparator delays were constrained in the previous section. Comparing Figures 5-12 and 5-13 reveals that lower transconductance is required for a comparator as its delay time is allowed to increase. The op-amp line does not take into account the effects of finite op-amp gain. Considering the effects of finte op-amp gain would increase the required transconductance of an op-amp at high bit resolutions.

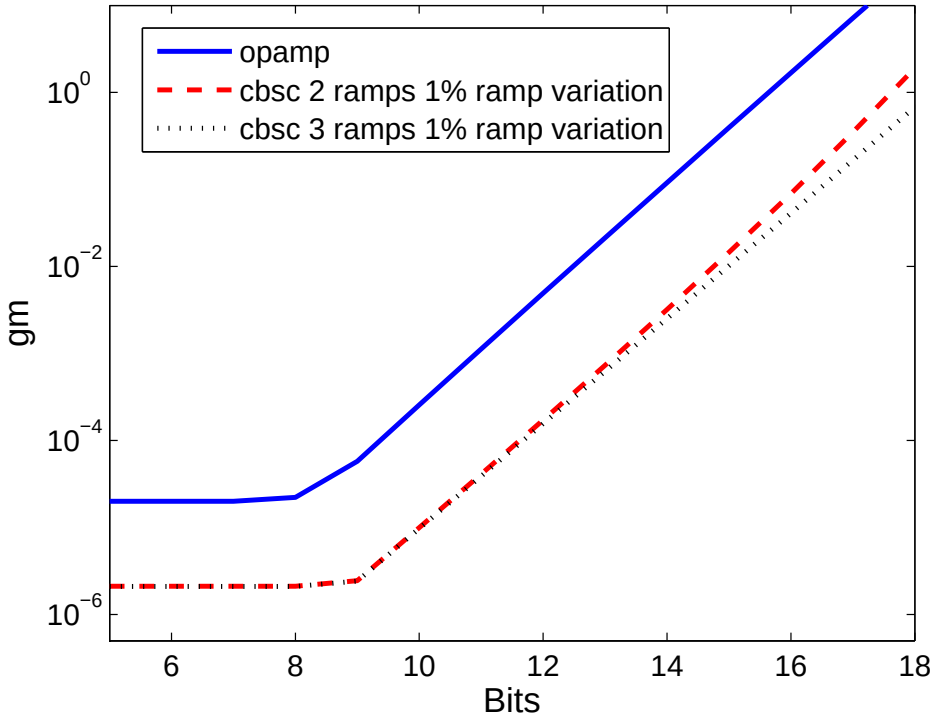
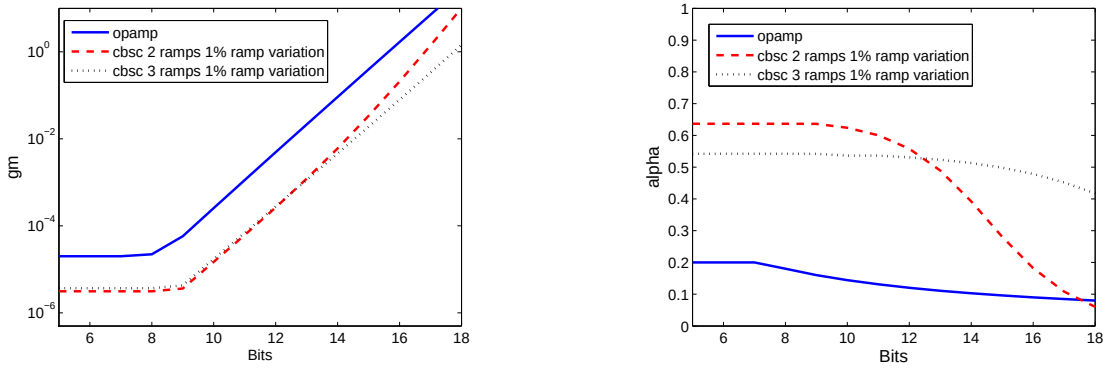


Figure 5-14: Transconductance vs. Linearity and Noise with an integrating final comparator: The linearity and mean squared noise of each circuit is required to be $\frac{1}{2}$ LSB at the input. The sampling frequency is 10 MHz and first and second fixed ramp delays are each 500 ps.

A single slope CBSC circuit is not included in this plot because such a circuit would not use a comparator that draws static current. Therefore there would not be the same relationship between power consumption and linearity for such a circuit. The power consumption for a single phase CBSC circuit would have to be compared to the power consumption of the fixed delay comparators. For simplicity the power consumption of these fixed delay comparators is ignored in this analysis. The number of comparator delays required by a single slope system is the same as in the fixed delay case described by Equation 5.71.

Figure 5-14 shows the relationship between linearity and noise performance, and required comparator transconductance for two and three slope CBSC circuits verses that of op-amp based circuits. The circuits achieve $\frac{1}{2}$ LSB INL and $\frac{1}{2}$ LSB peak-to-



(a) (b)

Figure 5-15: A CBSC stage with an integrating final comparator: The linearity and mean squared noise of each circuit is required to be $\frac{1}{2}$ LSB at the input. The sampling frequency is 10 MHz. The first and second fixed ramp delays are each 5 ns. (a) Transconductance vs. Linearity and Noise (b) Fraction (α) of the half clock cycle occupied by the final phase comparator delay vs. Linearity.

peak noise at their inputs. The same assumptions made in Figure 5-12 are made in this figure. Additionally the scaling of capacitor sizes for both the op-amp and comparator based circuits is assumed to be limited. As the noise requirement decreases, the comparator integration capacitor and the op-amp sampling capacitors are allowed to decrease. The scaling is limited to the minimum practical values of 10fF for the integration capacitor and 100fF for the sampling capacitor. This causes the curves to flatten out at low bit resolutions.

The linearity vs transconductance relationship for a CBSC circuit with an integrating comparator leads to similar observations as a CBSC circuit with fixed delay comparators. Given a low enough ramp nonlinearity the power consumption of a CBSC circuit will be lower than an op-amp based circuit. Also, using more than two ramps in a CBSC circuit only becomes especially advantageous at high bit resolutions (B$>$ 14 bits). Figure 5-15(a) shows that for lower bit resolutions two ramps is more power efficient that three ramps. This is more evident in Figure 5-15(a) than in Figure 5-14 because the length of the fixed delays ($t_{d1} = t_{d2} = 5$ns) in Figure 5-15(a) are larger relative to the length of the half clock cycle than in Figure 5-14. The fixed

delays equal 10% rather than 1% of the half clock cycle. Figure 5-15(b) shows the advantage of three ramps at high bit resolution in terms of the portion of the half clock cycle α taken up by the final comparator delay.

5.4 Implementation Details

A number of implementation details extend the time needed to transfer charge in CBSC circuits thereby increasing the power consumption required to achieve a linearity specification.

5.4.1 Preset Time

In the preceding analysis the preset time t_p is ignored. During the first portion of the charge transfer the output node is shorted to ground to ensure that v_X starts below V_{CM} for all input voltages. Adding the preset time to the rest of the charge transfer time increases the required number of comparator delays or decreases the maximum comparator delay. The shorter comparator delay requires an increased power consumption in the comparator. The preset time must be long enough for the reference voltage and input to the comparator to settle. If the charge transfer starts before these nodes settle an error will be created in the output. This error is smaller for larger outputs than for smaller outputs because the reference has more time to settle during the longer charge transfer time of larger outputs. In a two phase system the reference does not have to be completely settled until the end of the second phase as long as the first phase overshoot is large enough to compensate for the contribution to ramp nonlinearity created by the varying reference.

During the preset time the output voltage should also settle to its grounded preset value. If the output does not completely settle an error will not occur, but the maximum amount of overshoot correction will be limited. The overshoot correction is limited by the voltage that the output starts at.

Another implementation detail related to the preset time is the turn on time of

the coarse current source. The cascode bias node of the current source must settle for the current source to produce an accurate current. The coarse current source was enabled during the preset time to provide time for the current source bias to settle. If it is not settled by the time the charge transfer starts it will cause ramp nonlinearity. This effect places another constraint on the preset time.

5.4.2 Excess Overshoot Requirement

In the analysis in this chapter, the ramp nonlinearity determines the minimum required voltage overshoot. For CBSC circuit with more than one ramp, the switch voltage drops and the finite gain of the comparator add to the overshoot requirement. Up to this point it has been assumed that the output of the integrating comparator begins to change once its inputs become equal. In reality, it starts to change before the inputs are equal because it is not a true integrator [32]. The comparator has a finite gain. It turns on when its differential input voltage equals its clamped output voltage divided by its gain.

$$v_{Icomp} = \frac{-V_D}{g_m R_L}. \tag{5.80}$$

Where v_{Icomp} is the input to the comparator, V_D is the clamped voltage, g_m of the comparator and R_L is the output resistance of the comparator. Figure 5-16 shows how this effect can create nonlinearity. Figure 5-16(b) shows the desired operation of the integrating type comparator. The output reaches the clamped voltage V_D during the coarse phase overshoot and switches back to the opposite clamped voltage $-V_D$ during the fine charge transfer. All memory of the coarse phase is erased in this procedure. The size of the coarse phase overshoot does not effect the fine phase overshoot. Figure 5-16(b) shows what happens when the comparator turns on early and the coarse phase overshoot is not enough: the integrating comparator output does not reach the clamp voltage V_D. Changing the comparator reference V_{Rcomp} from V_{OC} during the coarse phase to V_{CM} during the fine phase causes the comparator to start

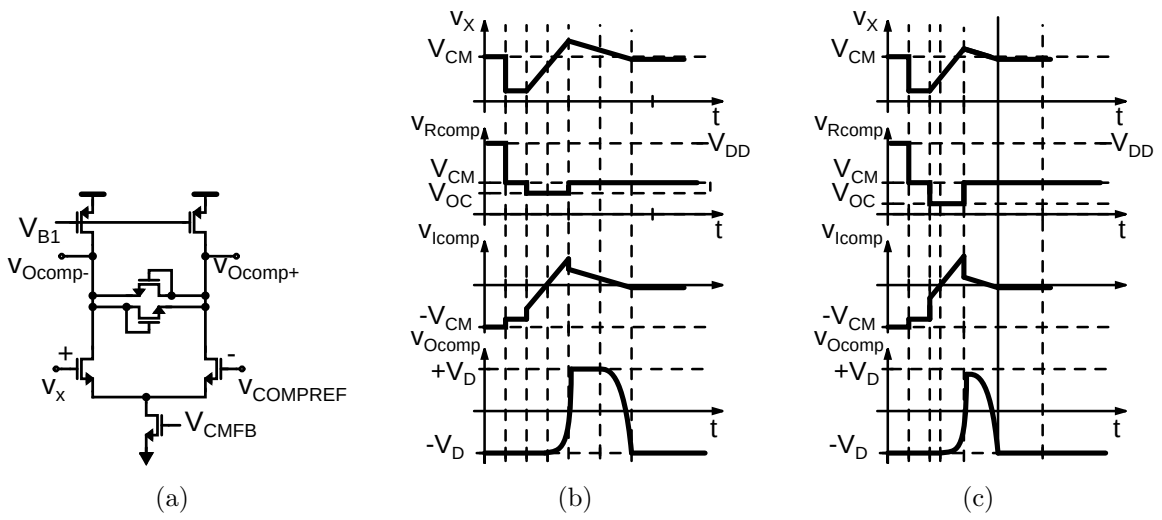
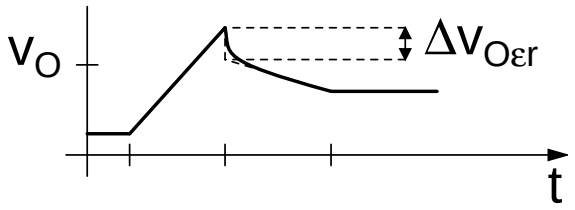


Figure 5-16: (a) Comparator integrating preamplifier schematic (b) Comparator integrating preamplifier output. The output reaches and stays at the clamped state before flipping. Memory of the coarse phase is erased. (c) Comparator integrating preamplifier output that does not reach the clamped state

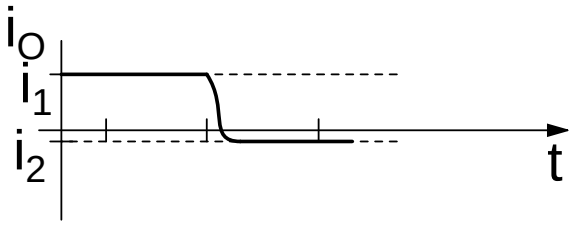
to trip before to reaches the clamp voltage V_D. The comparator retains memory of the coarse phase overshoot when it does not reach the clamp. The delay of the comparator during the fine phase depends on the overshoot in the first phase. The output of the comparator can fail to reach the top clamp even when stage output overshoots the desired value.

This potential source of nonlinearity can be managed by canceling less of the coarse phase overshoot or by lowering the comparator reference voltage during the fine phase. Allowing a greater coarse phase overshoot lengthens the coarse and fine phases. Lowering the comparator reference during the fine phase lengthens the fine phase and increases the output offset.

The voltage drop across the circuits switches add to the required overshoot requirement and lengthen the minimum charge transfer time. At the end of the coarse charge transfer phase the coarse current turns off and the fine current turns on. At this moment the voltage drop across the switches disappears and a voltage drop in the opposite direction appears. A voltage step occurs at both the output of the circuit and at the input to the comparator. The coarse phase overshoot voltage must be



(a)



(b)

Figure 5-17: Switch voltage drop transient. (a) The switch voltage drop $\Delta\, v_{O\epsilon r}$appears at the output during the transition from the coarse phase to the fine phase. A transient occurs as v_O settles to a constant ramp. (b) The output current switches direction during the transition from the coarse phase to the fine phase. The coarse current source turns off and the fine current turns off during the transition.

large enough that this step does not trigger the comparator for any input voltage. This additional overshoot voltage requires a slight extension of the coarse phase but does not require an extension of the fine phase. The additional overshoot voltage disappears at the time of the two charge transfer phases and therefore does not need to be overcome during the fine phase. This effect is shown by the dashed line in Figure 5-17(a).

One effect that does require a longer fine charge is the settling transient that occurs at the beginning of the fine charge transfer phase. The switch voltages do not disappear instantaneously due to the resistance and parasitic capacitances in the circuit. Also, as shown in Figure 5-17(b), the coarse current source needs time to turn off and the fine current source needs time to turn on. All of these effects cause the output voltage to settle to a constant ramp rate, as shown by the solid line in in Figure 5-17(a). Time must be allowed for the transient to settle before the comparator triggers. If the comparator triggered during the settling transient it

would have a shorter delay because of the steeper voltage ramp at its input. This would create input dependent comparator delay variation and would contribute to nonlinearity.

5.5 Design Procedure

The analysis contained in this chapter suggests an approach for the design of CBSC circuits. Starting with a linearity constraint a maximum final overshoot and output slope are determined. The slopes of coarse phases are then chosen to produce the fastest possible charge transfer. This occurs when the initial charging time equals the the length of the phases required to overcome the residual output overshoot of the initial phase. Given the constraint on the maximum overshoot correction and the linearity of the voltage ramps, the number of phases needed to achieve a minimum charge transfer time can be determined. The procedure produces a design with the maximum possible performance. Practical circuit details neglected in the analysis will reduce the achievable performance. Practical details may require the values obtained from calculations to be altered and may require an iteration of the procedure. The result of the procedure will be a circuit which meets linearity, noise and speed requirements at a minimum power consumption.

5.6 Conclusion

CBSC circuits contain a number of different sources of offset and nonlinearity. Some of these are common to op-amp based circuits and some are unique to CBSC circuits. Circuit techniques such as using multiple slopes and overshoot cancellation allow for the design of highly accurate CBSC circuits. The minimum number of comparator delays needed to achieve a minimum circuit linearity is determined. Consequently the minimum required power consumption of a CBSC circuit is also determined. These result compare favorably with the op-amp based circuit as long as the CBSC

ramp nonlinearity can be made small enough. The linearity analysis shows that the choice of CBSC topology depends on the desired resolution. CBSC circuits with more ramps become more power efficient than those with fewer ramps as the required circuit linearity increases.

Chapter 6

Test System and Results

6.1 Introduction

This chapter describes the test system that was used to characterize the prototype CBSC ADC and presents the results of the characterization. The design of the printed circuit board is explained. The test equipment needed for testing is cataloged. The tests used to characterize the ADC are described and the results of these tests are presented and compared to the simulated results.

6.2 Test System

The test system used to characterize the prototype is show in Figure 6-1. The test setup was configured differently for static and dynamic testing. For static testing a 9kHz input signal was produced by the Audio Precision System I. A simple RC filter on the board filtered the input signal. . For the dynamic testing a 3.8MHz sine wave produced by the HP8662B signal generator passed through a low pass filter and then on to the board where it passed through a transformer before reaching the test chip. The low pass filter reduced the harmonics of the input signal. For both testing regimes an Agilent 8644B signal generator was used to clock the prototype chip. Its output was low pass filtered before it reached to reduce high frequency noise. The test

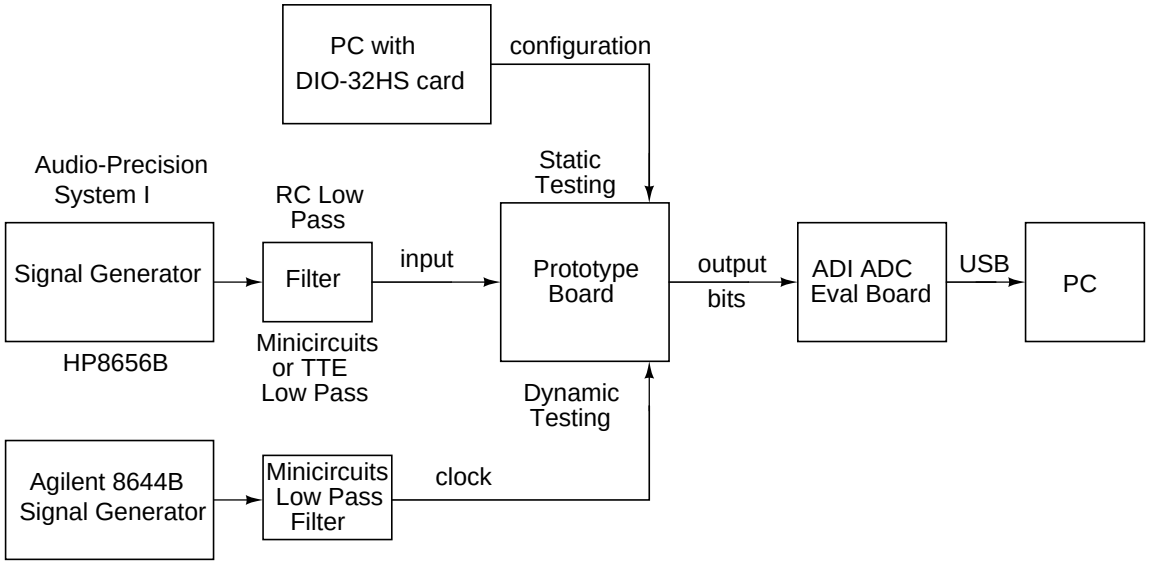


Figure 6-1: Test setup. The component descriptions above the blocks correspond to static testing while the component descriptions below the blocks correspond to dynamic testing.

chip was configured using a National instrument's DIO-32HS data acquisition card. The output data was passed from the test board to an ADI HSC-ADC-EVAL-DC ADC evaluation board where is was buffered and sent over a USB link to a PC.

6.2.1 Printed Circuit Board Layout

The PCB test board has 4 layers. The top of the board is used for routing and component placement. The second layer is made of up various voltage supply planes. They are

VDD5: The 5 V supply for the reference circuits and for the data National Instruments card interface circuits.

VSS5: The -5 V supply for the reference circuits.

VDD33: The 3.3 V supply for the interface circuits for the ADI evaluation board and the National Instruments card.

IOVDD18: The 1.8 V supply for the input/output circuits on the test chip.

The third layer contains the ground. The entire layer is composed of a large ground plane. The plane is divided into portions for the input signal, for the reference and

for the clock. This was done to isolate the noisy portions of the board from the quiet ones. The three ground planes are connected close to the chip. The bottom side of the board contains components and routing as well as supply voltage planes. The supply voltage planes are

AVDD18: The 1.8 V supply for the analog circuits on the test chip.

DVDD18: The 1.8 V supply for the non-input/output digital circuits on the test chip

6.2.2 Printed Circuit Board Circuits

The circuits on the PCB test board consisted of interface circuits and reference circuits.

Interface Circuits

The input signal, clock, configuration register and output lines all require on board interface circuits. During dynamic measurements the input passes through a Mini Circuits transformer and directly goes to the chip. The transformer isolates the chip from the input source and allows for the input common mode to the chip to be different than the common mode of the signal generator. The transformer was replaced by a DC blocking capacitor for the static measurements because the input signal was at a lower frequency than the passband of the transformer. The clock is converted to a differential signal by a transformer and passed into a differential line receiver(DS90LV048A). The output of the receiver is translated from 3.3 V to 1.8 V by a bus transceiver(SN74AVCA164245). Solder jumpers are placed on the board so that the transformer, line receiver and bus transceiver can by bypassed and the sine wave clock sent directly into the chip. The digital lines of the configuration register enter the board from the data acquisition card as 5 V signals. The inputs from the data acquisition card are terminated by an array of Schottky diodes (SN74S1053). They are then translated from 5 V to 1.8 V using two bus transceivers (SN74ALVC164245 and SN74AVCA164245). The output data bits are translated from 1.8 V to 3.3 V and passed to the ADI ADC evaluation board.

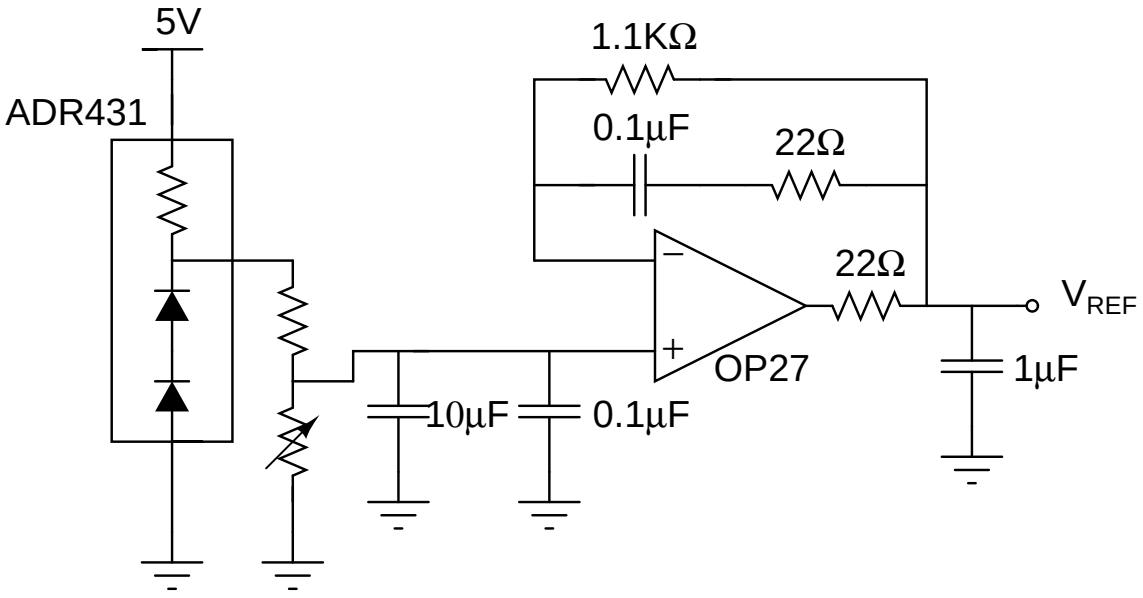


Figure 6-2: Voltage bias circuit.

Reference and Bias Circuits

The circuit [40,41] used to set the bias voltages for the test chip is seen in Figure 6-2. The reference [40] is generated from a low noise band gap reference (ADR431) and is buffered with a low noise op-amp (OP27). The resistors and capacitor in the feedback loop are not required for the circuit to operate successfully. Buffers with similar feedback networks have been previously published [42]. The circuits [40, 41] that set the test chip bias currents are shown in Figures 6-3 and 6-4. The current is produced using an op-amp and a bipolar transistor. The circuit in Figure 6-3 provides current to on-chip PMOS current mirrors and the circuit in Figure 6-4 provides current to on chip NMOS current mirrors. The current values are determined by measuring the voltage across the emitter resistor. The circuit in Figure 6-4 is potentially sensitive to supply noise. Variation in the 5 V supply will change the current through the emitter resistor. The same supply noise will not couple to the input node of the opamp. The capacitor in parallel with the on chip diode should filter out most of this noise. Also the 5 V supply is heavily bypassed on the board to reduce supply variation.

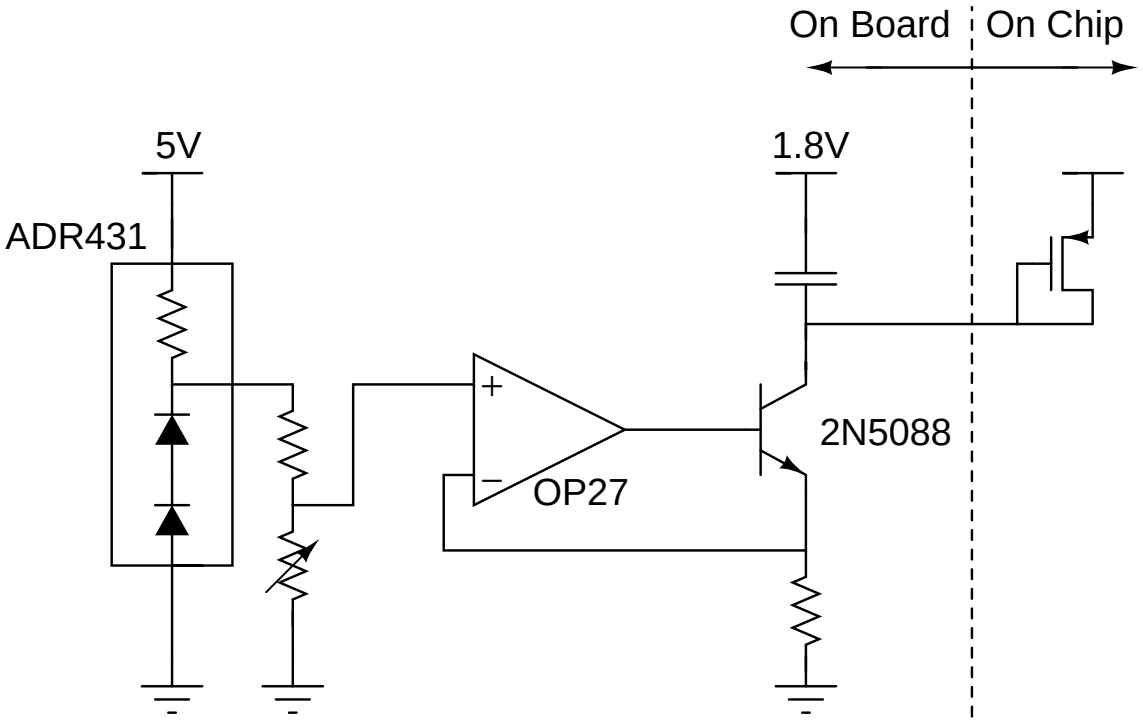


Figure 6-3: Current bias circuit for on chip PMOS current mirrors.

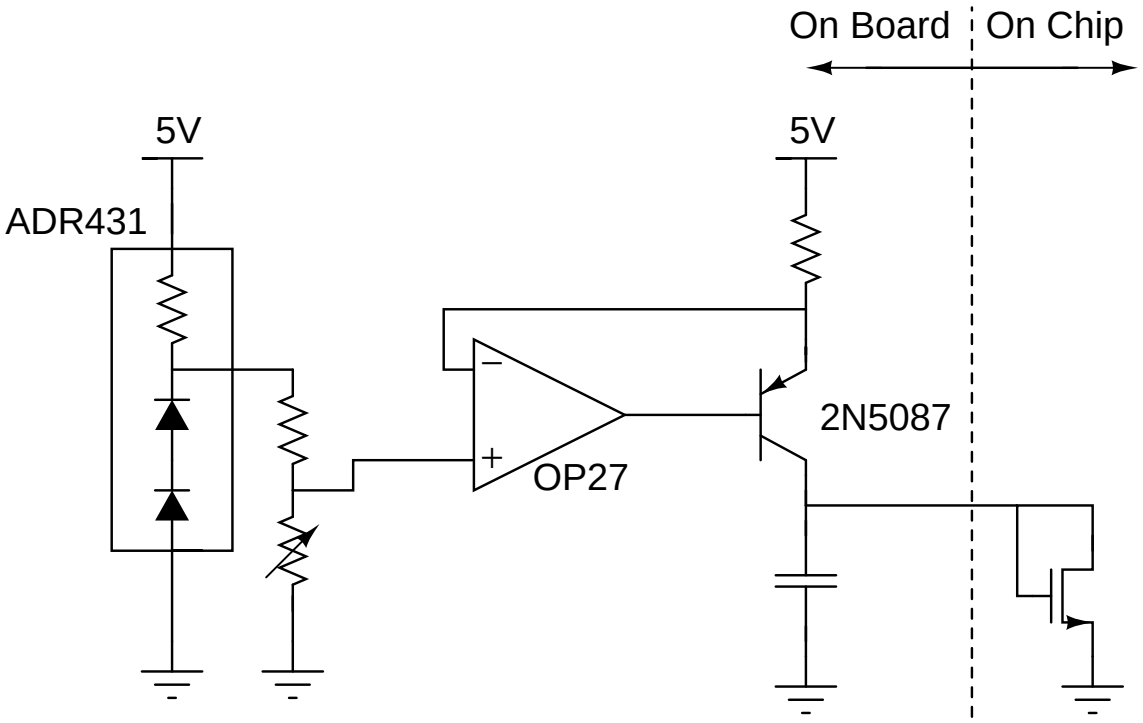


Figure 6-4: Current bias circuit for on chip NMOS current mirrors.

6.3 Results

6.3.1 Measured Results

The CBSC pipelined ADC achieved 10 bit resolution with a 0.8 pJ/step figure of merit [43]. The standard figure of merit of

$$FOM = \frac{P}{2\, f_{in}\, 2^{ENOB}} \tag{6.1}$$

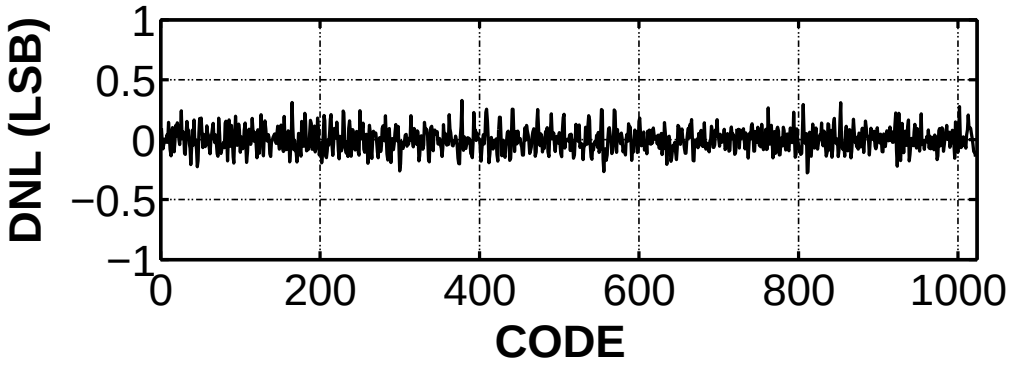
is used. Where P is the power dissipated by the ADC core, f_{in} is the maximum input frequency, and $ENOB$ is the effective number of bits calculated from the signal to noise and distortion ratio ($SINAD$) for a full scaled input with the maximum input frequency. The figure of merit value is competitive with traditional op-amp based ADCs.

6.3.2 Static Performance

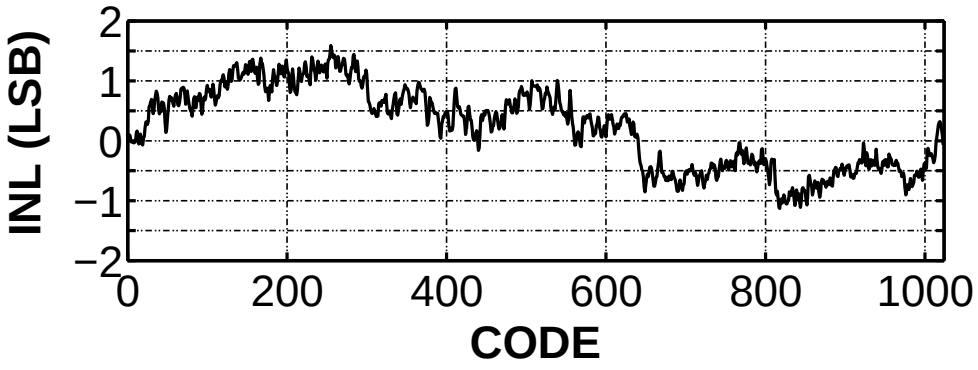
The measured 10 b static performance of the pipelined ADC with a 7.9 MHz sampling clock is shown in Fig. 6-5. The DNL is +0.33 LSB and −0.28 LSB, and the INL is +1.59 LSB and −1.13 LSB. Linearity of the overshoot in the fine charge transfer is the mechanism limiting the ADC's INL. The finite output resistance of the fine current source is the primary cause of the nonlinear overshoot variation. As is shown in Chapter 5, the linearity of the fine phase voltage ramp determines the linearity of the entire circuit. The fine phase current source in the prototype suffers from low output resistance, and consequently produces a fine phase voltage ramp with large ramp rate variation. This variation combines with the fine phase overshoot to produce INL. This effect is further explained in Section 6.3.5

6.3.3 Dynamic Performance

Fig. 6-6 shows the frequency response of the ADC from an FFT test with an input frequency of 3.8 MHz and input amplitude 1dB below full scale. Fig. 6-7 displays



(a)



(b)

Figure 6-5: ADC INL and DNL for 7.9 MHz sampling frequency. (a) DNL. (b) INL.

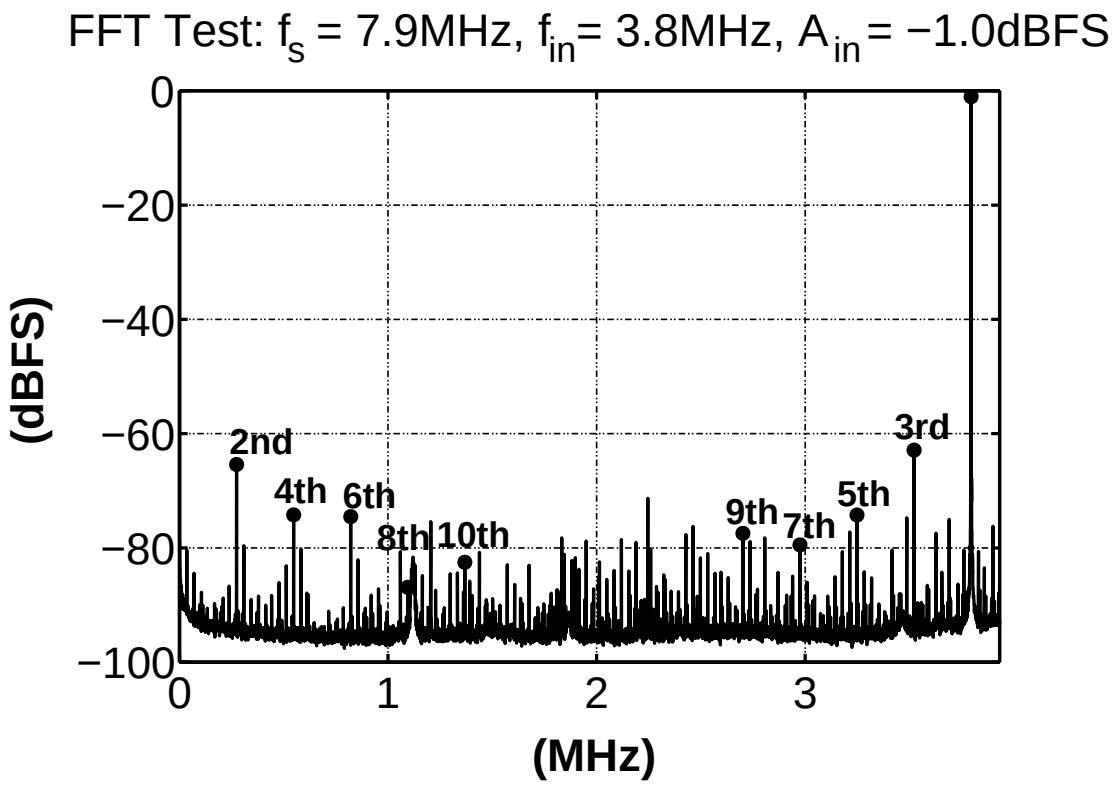


Figure 6-6: Output FFT for 7.86MHz clock and 3.8MHz input.

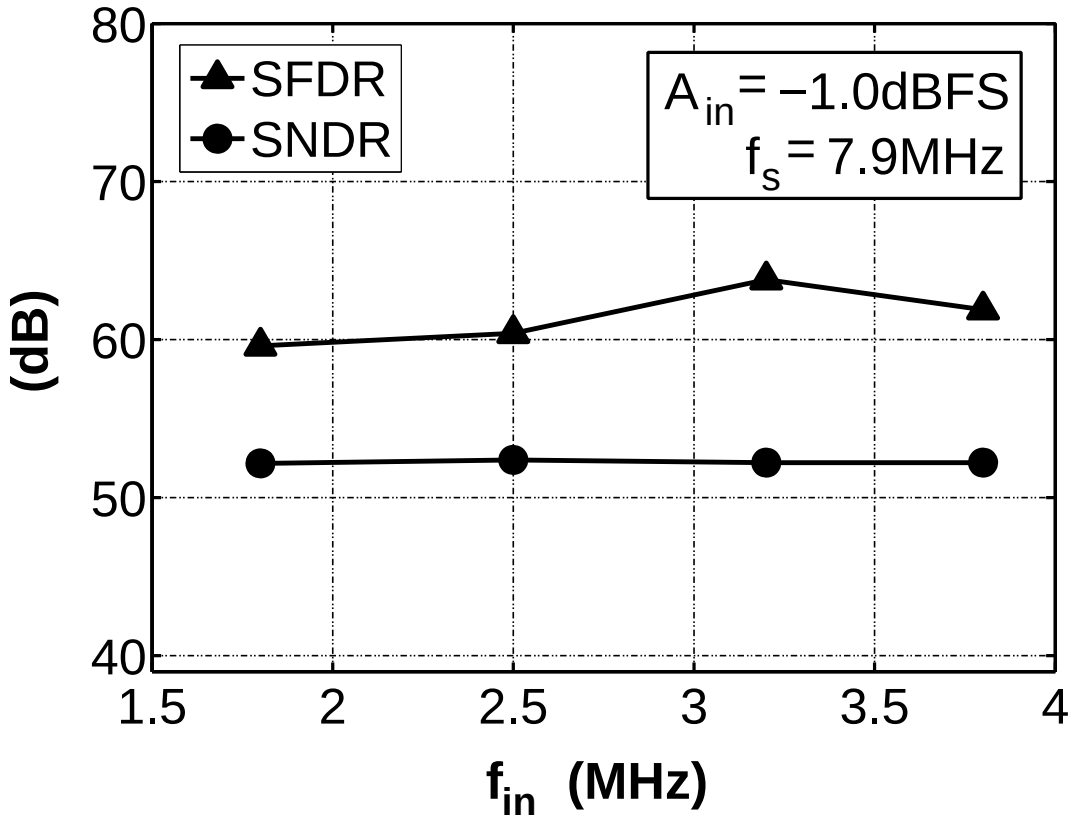


Figure 6-7: SNDR and SFDR versus input frequency.

the performance of the ADC versus input frequency with an input amplitude of 1dB below full scale. The SNDR and SFDR are essentially constant across input frequency up to the Nyquist rate.

6.3.4 Figure of Merit

Table 6.1 summarizes the performance of the prototype ADC. Operating at 7.9 MHz, with a single-ended 1V full-scale range, the converter has 8.6 effective bits of accuracy, and consumes 2.5 mW of power. The figure of merit [43] based on the ADC dynamic performance is 0.8 pJ/step.

Table 6.1: ADC Performance Summary

f_s	7.9 MHz
V_{FS}	1 V (single-ended)
DNL	+0.33/-0.28 LSB_{10}
INL	+1.59/-1.13 LSB_{10}
SFDR	62 dB
SNDR	52 dB
SNR	53 dB
ENOB	8.6 b
Power	2.5 mW
$\text{FOM} = \frac{P}{2 f_{\text{in}}\, 2^{\text{ENOB}}}$	0.8 pJ/step

6.3.5 Measured vs. Simulated results

Simulation of the ADC shows better linearity performance than the measured prototype linearity performance. The simulated INL is shown in figure 6-8. The INL is less than +0.2/-0.4 LSB_{10}. The measured inl shown in figure 6-5(b) falls within +1.59/-1.13 LSB_{10}.

The simulation predicted a lower INL than was measured partially due to a limitation in the transistor models used in simulation. The BSIM3 models originally used in simulation do not accurately model the effect of pocket implants on the output resistance of transistors [1, 3, 4]. Pocket implants are highly doped portions of the substrate adjacent to the source and drain. They counteract the threshold voltage roll off that occurs in scaled devices due to short channel effects. A minimum length device has a larger portion of its area taken up by the pocket implants than a long device so it has a higher average substrate doping and consequently a higher threshold voltage than the long device. Unfortunately pocket implants reduce the output resistance of a transistor. The pocket implanted region at the drain end of the channel appears as a very short transistor with a high threshold voltage in series with a

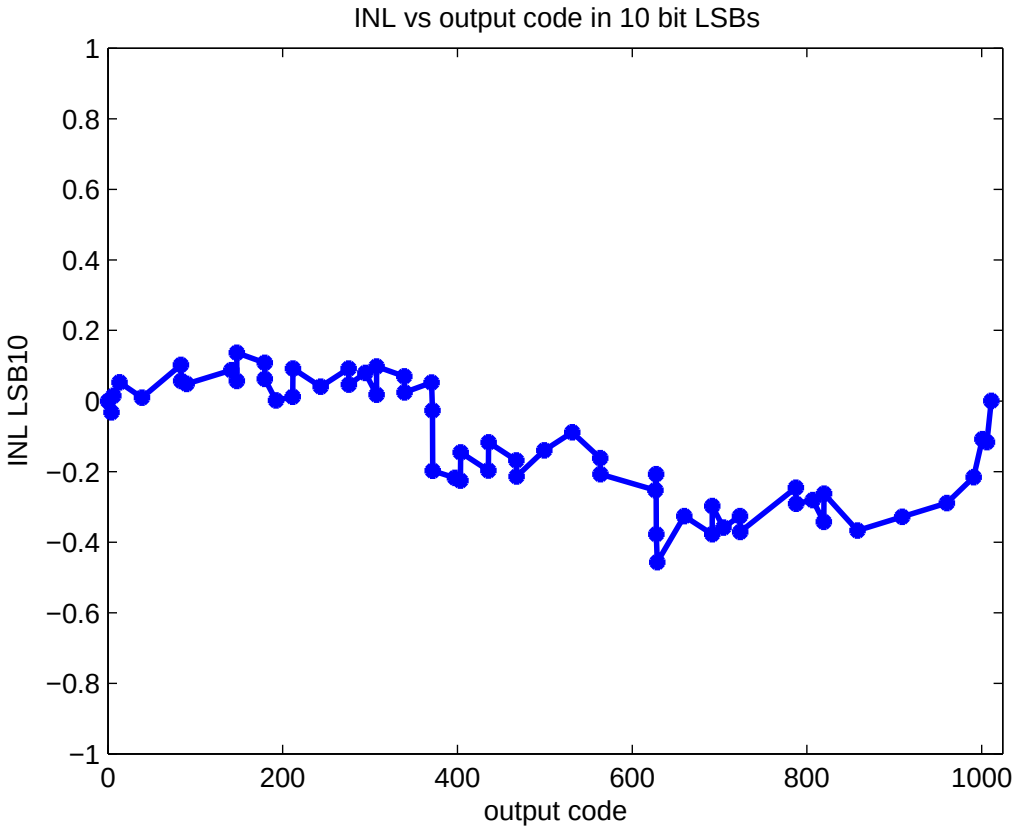


Figure 6-8: Simulated ADC INL: the INL is less than +0.2/-0.4 LSB_{10}

transistor that represents the rest of the channel. This transistor at drain determines the output resistance of the entire device. Modulation of the energy barrier created by the drain pocket implant by the drain voltage sets the output resistance for the transistor. The output resistance is much lower than it would be if the implant was not included in the device. Lengthening the transistor does not significantly effect the output resistance because the drain side pocket implant remains unchanged. The original models used in simulation ignored the effect of the pocket implants on the output resistance and predicted an output resistance that was larger than what was achieved. A long 1.34 µm NMOS transistor was used as the fine phase current source. This device had a much lower resistance than predicted by simulation. The ADC linearity performance depends heavily on the output resistance of this device.

Simulations were rerun using improved models which accounted for the effects of

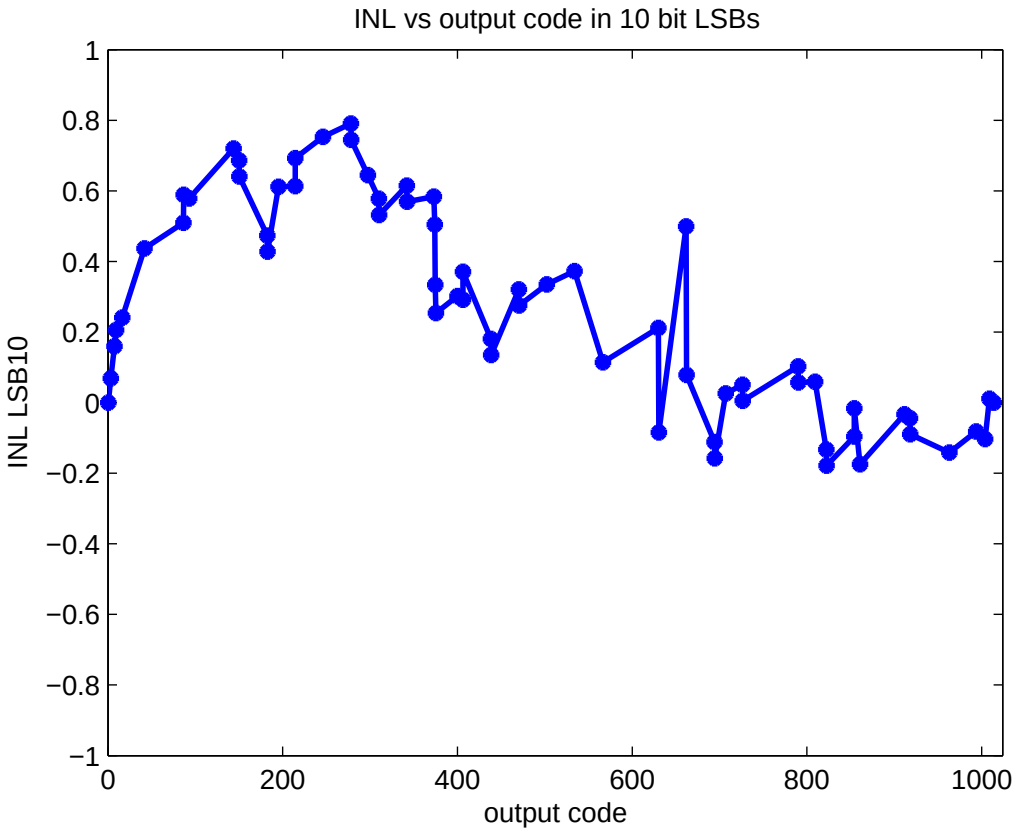


Figure 6-9: Simulated ADC INL using updated NMOS models: the INL is +0.8/-0.2 LSB_{10}

the pocket implants. The result of these simulations is shown in Figure 6-9. The simulated INL using the updated models is +0.8/-0.2 LSB_{10}. It is significantly higher than in the original simulation. Figure 6-9 also shows a similar characteristic to the measured data in Figure 6-5(b) where the INL is higher for the lower portion of the output range. This occurs because the fine ramp overshoots more for high output voltages than low output voltages. This occurs because, as in shown in section 4.2.3, the fine phase current source becomes a cascode and has a higher output resistance for larger output voltages. The results obtained from the simulation using the revised models suggests that low output resistance of the fine phase current is a major, but not sole contributor to the INL of the prototype ADC. The ADC linearity can be improved by using a fine phase current source with a larger output resistance. A larger output resistance can be achieved by using a cascode for the fine phase current source.

Chapter 7

Conclusions

7.1 Conclusions

A new comparator-based switched-capacitor design methodology has been presented. The technique has been demonstrated with the design of a 10 b, 7.9 MS/s pipelined ADC with a 0.8 pJ/step figure of merit. The CBSC method has a number of important advantages when compared to traditional op-amp based switched capacitor circuits.

Comparator-based switched-capacitor circuits have a number of advantages that make them a compelling alternative to traditional op-amp based switched-capacitor circuits. The analysis in chapter 5 demonstrates that comparator-based designs have the potential for significant power consumption reduction compared to traditional op-amp based designs. Also, because the different design constraints on the comparator and current sources, CBSC designs are more amenable to design in scaled technologies than their op-amp counterparts. A related advantage is that feedback and stability concerns are removed from CBSC systems because they detect the virtual ground condition in an open-loop manner. Finally, the CBSC design methodology is applicable to a wide range of switched-capacitor circuits and is compatible with most known architectures.

One important issue with the CBSC technique is that, unlike the op-amp based circuits, only switched-capacitor loads can be driven. A CBSC stage does not act

as a voltage source capable of driving arbitrary loads because it does not contain an output amplifier. A second issue is that circuits designed using the CBSC technique cannot simultaneously drive both sides of the sampling capacitor. This means that the method is incompatible with the conventional closed-loop offset cancellation technique that samples with reference to a driven virtual ground. Thirdly, output voltage ramp linearity causes nonlinearity in a manner similar to finite gain in an op-amp. However, it is easier to create a constant ramp than to design a high-gain op-amp. The input signal does not pass through the current source creating the ramp as it would in an op-amp. The current source also carries much less current than the bias current of an op-amp. Finally, CBSC is a new technique, and therefore not all of the issues and limitations have been discovered.

7.2 Thesis Contributions

The comparator-based switched-capacitor technique [5, 6] was developed and implemented in a prototype ADC. The overall technique was developed and the details of the circuit implementation were explored. A top level design was completed which enabled the competitive performance and power dissipation of the prototype. Individual components of the prototype were developed including switches and current sources. An overshoot cancellation scheme was developed to enable acceptable circuit performance and a switching scheme was developed to enable proper operation and to minimize the effects of circuit non-idealities.

Sources of offset and nonlinearity were identified and analyzed. Their effects on system linearity, speed, and power consumption were quantified. The analysis shows that comparator-based circuits have a potential power consumption advantage when compared to op-amp based circuits. A design approach to minimizing power consumption at a specific speed, noise and linearity specification is described. The identification of sources of nonlinearity and the design approach can be used as a starting point for future comparator-based switched-capacitor circuit designs.

7.3 Future Work

Some suggestions for future work:

- Implement a fully differential CBSC design. A high resolution fully differential design would require a common mode feedback circuit to balance charging and discharging currents. The common mode feedback circuit would prevent common mode errors from compromising circuit performance.
- Design a power efficient high speed current source with output resistance greater than that of a cascode.
- Develop methods for constant ramp generation at lower supply voltages where a cascode current source can no longer be used.
- Develop a design methodology to optimize the power consumption linearity trade off by balancing the contributions of the different sources of nonlinearity.
- Explore robust circuit techniques that enable different sources of nonlinearity to cancel one another.
- Investigate hybrid op-amp based and comparator-based topologies.
- Determine the limits of power reduction for CBSC designs. Maximize the portion of the half clock cycle taken by the the preamplifier integration time t_i.
- Experiment with the CBSC approach in other ADC design spaces (eg. high speed or high accuracy).
- Design other switched-capacitor circuits using the CBSC technique including DACs, filters and Delta-Sigma ADCs
- Create multi-bit-per-stage designs and compare the power efficiency of such designs to single-bit-per-stage designs and multi-bit-per-stage op-amp based designs.

References

[1] D. Buss, "Device issues in the integration of analog/RF functions in deep submicron digital CMOS," in *IEEE IEDM Technical Digest*, December 1999, pp. 423–426.

[2] S. Ogura, C. F. Codella, N. Rovedo, J. F. Shepard, and J. Riseman, "A half micron MOSFET using double implanted LDD," in *Intl. Electron Devices Meeting (IEDM) Technical Digest*, 1982, pp. 718–721.

[3] A. Chatterjee, K. Vasanth, D. T. Grider, M. Nandakumar, G. Pollack, R. Aggarwal, M. Rodder, and H. Shichijo, "Transistor design issues in integrating analog functions with high performance digital CMOS," in *VLSI Technology, 1999. Digest of Technical Papers. 1999 Symposium on*, 1999, pp. 147–148.

[4] K. M. Cao, W. Liu, X. Jin, K. Vasanth, K. Green, J. Krick, T. Vrotsos, and C. Hu, "Modeling of pocket implanted MOSFETs for anomalous analog behavior," in *Electron Devices Meeting, 1999. IEDM Technical Digest. International*, 1999, pp. 171–174.

[5] T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway, and H.-S. Lee, "Comparator based switched capacitor circuits for scaled CMOS technologies," in *IEEE ISSCC Dig. Tech. Papers*, February 2006, pp. 220–221.

[6] J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, and H.-S. Lee, "Comparator based switched capacitor circuits for scaled CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, December 2006.

[7] R. Brodersen, P. Gray, and D. Hodges, "MOS switched-capacitor filters," *Proc. IEEE*, vol. 67, no. 1, pp. 61–75, January 1979.

[8] J. H. Huijsing and D. Linebarger, "Low-voltage operational amplifier with rail-to-rail input and output ranges," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1144–1150, December 1985.

[9] S. Paul, H.-S. Lee, J. Goodrich, T. Alailima, and D. Santiago, "A Nyquist-rate pipelined oversampling A/D converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1777–1787, December 1999.

[10] M. A. Copeland and J. M. Rabaey, "Dynamic amplifier for M. O. S. technology," *Electronics Letters*, vol. 15, no. 10, pp. 301–302, May 1979.

[11] B. Hosticka, "Dynamic CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 15, no. 5, pp. 881–886, October 1980.

[12] S. Ranganathan and Y. Tsividis, "Discrete-time parametric amplification based on a three-terminal mos varactor: analysis and experimental results," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2087–2093, December 2003.

[13] E. Siragusa and I. Galton, "A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, December 2004.

[14] B. Murmann and B. Boser, "A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, December 2003.

[15] J. Fiorenza, "Gain compensated sample and hold," Master's thesis, Massachusetts Institute of Technology, 2002.

[16] J. Li and U.-K. Moon, "A 1.8-v 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1468–1476, 2004.

[17] H. Yang and R. Sarpeshkar, "A time-based energy-efficient analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1590–1601, August 2005.

[18] P. Holloway and G. O'Donoghue, "An 8-channel 16 b charge-to-digital converter for imaging applications," in *IEEE ISSCC Dig. Tech. Papers*, February 1992, pp. 176–177.

[19] K.-H. Lee and E. Yoon, "A CMOS image sensor with reset level control using dynamic reset current source for noise suppression," in *IEEE ISSCC Dig. Tech. Papers*, February 2004, pp. 114–516.

[20] *Special Sample and Hold Techniques (AN294)*, National Semiconductor, April 1982.

[21] J. Williams, *High Speed Comparator Techniques (AN13-1)*, Linear Technology, April 1985.

[22] D. G. Haigh and B. Singh, "A switching scheme for switched capacitor filters which reduces the effect of parasitic capacitances associated with switch control terminals," in *Proceedings of IEEE International Symposium on Circuits and SysteMS*, April 1983, pp. 586–589.

[23] K.-L. Lee and R. G. Meyer, "Low-distortion switched-capacitor filter design techniques," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1103–1113, December 1985.

[24] *LTC2208 Data Sheet*, Linear Technology. [Online]. Available: http://www.linear.com/pc/productDetail.do?navId=H0,C1,C1155,C1001,C1150,P13693

[25] *AD9230 Data Sheet*, Analog Devices, March 2006. [Online]. Available: http://www.analog.com/UploadedFiles/Data_Sheets/86636523AD9230_pre.pdf

[26] *MAX1205 Data Sheet*, Maxim Integrated Products. [Online]. Available: http://datasheets.maxim-ic.com/en/ds/MAX1205.pdf

[27] S. Lewis and P. Gray, "A pipelined 5-MSample/s 9-bit analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 22, no. 6, pp. 954–961, 1987.

[28] G. Jusuf, P. Gray, and A. Sangiovanni-Vincentelli, "CADICS-cyclic analog-to-digital converter synthesis," in *Computer-Aided Design, 1990. ICCAD-90. Digest of Technical Papers., 1990 IEEE International Conference on*, 11-15 Nov. 1990, pp. 286–289.

[29] B. Ginetti, P. G. A. Jespers, and A. Vandemeulebroecke, "A CMOS 13-b cyclic RSD A/D converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 7, pp. 957–965, July 1992.

[30] H.-S. Lee, "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC," *IEEE J. Solid-State Circuits*, vol. 29, no. 4, pp. 509–515, April 1994.

[31] A. Karanicolas, H.-S. Lee, and K. Barcrania, "A 15-b 1-MSample/s digitally self-calibrated pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1207–1215, Dec. 1993.

[32] T. Sepke, "Comparator design and analysis for comparator-based switched-capacitor circuits," Ph.D. dissertation, Massachusetts Institute of Technology, 2006.

[33] N. Sooch, "MOS cascode current mirror," U.S. Patent No. 4550284, October 1985.

[34] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. John Wiley and Sons, Inc., 2001.

[35] T. Choi, R. Kaneshiro, R. Brodersen, P. Gray, W. Jett, and M. Wilcox, "High-frequency cmos switched-capacitor filters for communications application," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 652–664, 1983.

[36] J. Babanezhad and R. Gregorian, "A programmable gain/loss circuit," *IEEE J. Solid-State Circuits*, vol. 22, no. 6, pp. 1082–1090, 1987.

[37] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley and Sons, Inc., 1997.

[38] T. Cho and P. Gray, "A 10 b, 20 MSample/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, 1995.

[39] A. Abo and P. Gray, "A 1.5-V, 10-bit, 14.3-MS/s cmos pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599–606, 1999.

[40] P. Yu, "Low-power design techniques for pipelined analog-to-digital converters," Ph.D. dissertation, Massachusetts Institute of Technology, 1996.

[41] A. N. Karanicolas, "Digital self-calibration techniques for high-accuracy, high-speed analog-to-digital converters," Ph.D. dissertation, Massachusetts Institute of Technology, 1994.

[42] *Voltage References of the CS5012A / CS5014 / CS5016 / CS5101A/ CS5102A / CS5126 Series of A/D Converters*, Crystal Semiconductor, July 1994.

[43] R. Walden, "Analog-to-digital converter technology comparison," in *IEEE GaAs IC Symp. Tech. Digest*, October 1994, pp. 217–219.

[44] K. Gulati, "A low-power reconfigurable analog-to-digital converter," Ph.D. dissertation, Massachusetts Institute of Technology, 2001.

Appendix A

Linearity Analysis Derivation

This Appendix shows the derivation of minimum charge transfer time for two and three phase CBSC circuits. The optimal output ramp rates needed to achieve a linearity constraint and a minimum charge transfer time are determined.

A.1 Two Phase CBSC Circuit

The two phase CBSC charge transfer is shown in Figure A-1. The total charge transfer time, t_{t2}, consists of four intervals: the initial charging time t_1, the coarse overshoot time t_{ov}, the overshoot recovery time t_2, and the fine phase comparator delay t_{d2}.

$$t_{t2} = t_1 + t_{ov} + t_2 + t_{d2} \tag{A.1}$$

The initial charging time t_1 equals the maximum possible output voltage V_{MAX} divided by the coarse phase ramp rate M_1,

$$t_1 = \frac{V_{MAX}}{M_1}. \tag{A.2}$$

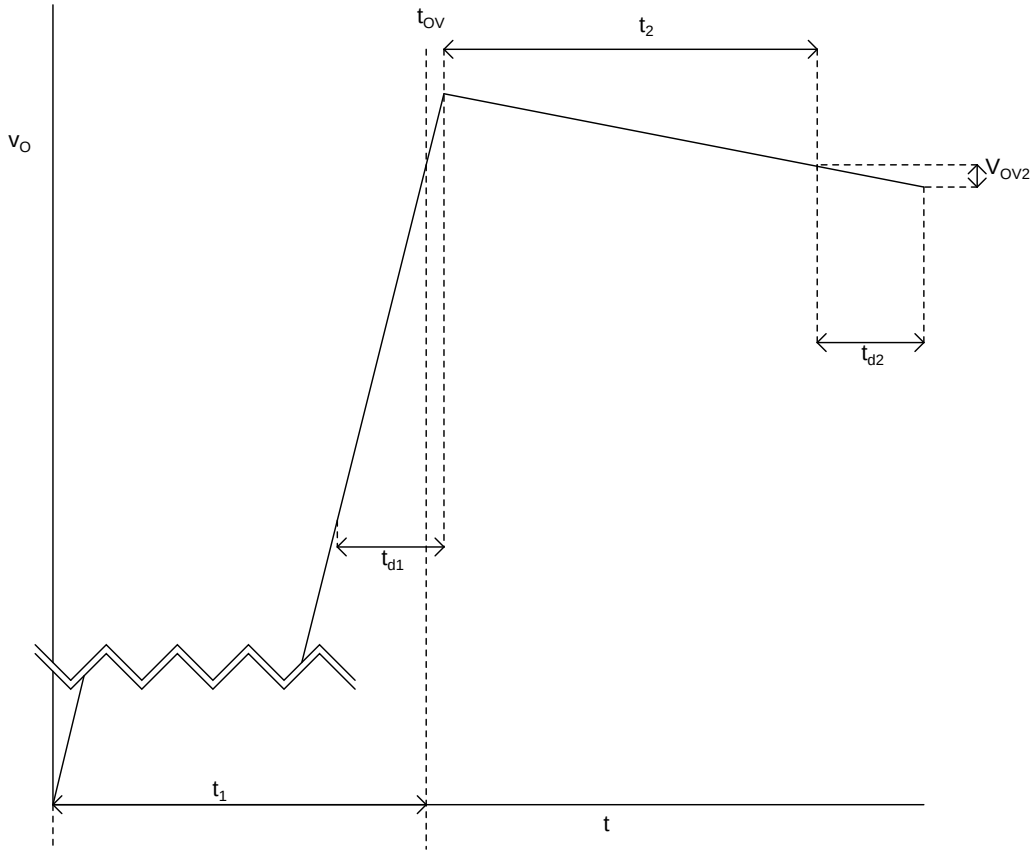


Figure A-1: Two-phase circuit output voltage: The minimum charge transfer time is achieved when t_1=t_2.

The coarse overshoot time t_{ov} equals the residual coarse phase overshoot V_{OV1r} divided by the coarse phase ramp rate M_1,

$$t_{ov} = \frac{V_{OV1r}}{M_1}. \tag{A.3}$$

From equation 5.34

$$V_{OV1r} = \frac{\Delta M}{M} V_{OV1}. \tag{A.4}$$

Substituting equation A.4 into equation A.3 leaves

$$t_{ov} = \frac{\Delta M}{M} t_{d1}. \tag{A.5}$$

The overshoot recovery time t_2 equals the residual coarse phase overshoot V_{OV1r} divided by the fine phase ramp rate M_2,

$$t_2 = \frac{V_{OV1r}}{M_2}. \tag{A.6}$$

Substituting equation A.4 into equation A.6 leaves

$$t_2 = \frac{\Delta M}{M} \frac{M_1}{M_2} t_{d1}. \tag{A.7}$$

The total charge transfer time equals

$$t_{t2} = \frac{V_{MAX}}{M_1} + \frac{\Delta M}{M} t_{d1} + \frac{\Delta M}{M} \frac{M_1}{M_2} t_{d1} + t_{d2}. \tag{A.8}$$

In order to determine the minimum charge transfer time the coarse M_1 and fine M_2 ramp rates must be determined. The fine phase ramp rate M_2 is determined from equation 5.43 and a linearity constraint,

$$M_2 = \frac{V_{OV2}}{t_{d2}}. \tag{A.9}$$

The fine phase overshoot is chosen to be as large as possible while meeting the linearity constraint,

$$V_{OV2} = \frac{V_{FS}\, 2^{-B}}{\frac{\Delta M}{M}}. \tag{A.10}$$

The coarse phase ramp rate M_1 is chosen to produce the shortest charge transfer time. In order to determine this value of M_1 the charge transfer time is differentiated with respect to M_1 and set equal to zero.

$$\frac{dt_{t2}}{dM_1} = 0 \tag{A.11}$$

$$\frac{dt_{t2}}{dM_1} = -\frac{V_{MAX}}{M_1^2} + \frac{\Delta M}{M}\,\frac{t_{d1}}{M_2} \tag{A.12}$$

To ensure that value of M_1 produces the minimum charge transfer time and not the maximum charge transfer time the second derivative of the charge transfer time is taken. The result is shown to be greater than zero.

$$\frac{d^2t_{t2}}{dM_1^2} > 0 \tag{A.13}$$

$$\frac{d^2t_{t2}}{dM_1^2} = \frac{2\,V_{MAX}}{M_1^3} > 0 \tag{A.14}$$

This second derivative is greater than zero, therefore the minimum charge transfer time has been found. Rearranging equation A.12 shows that the minimum charge transfer time occurs when the initial charging time t_1 equals the overshoot recovery time t_2. A larger coarse ramp rate shortens the initial charging time, but creates a larger overshoot and therefore lengthens the overshoot recovery time. The optimal coarse ramp rate causes the two intervals to equal one another and produces the shortest charge transfer time.

$$-\frac{V_{MAX}}{M_1^2} + \frac{\Delta M}{M}\,\frac{t_{d1}}{M_2} = 0 \tag{A.15}$$

$$\frac{V_{MAX}}{M_1^2} = \frac{\Delta M}{M}\,\frac{t_{d1}}{M_2} \tag{A.16}$$

$$\frac{V_{MAX}}{M_1} = \frac{\Delta M}{M}\,\frac{M_1}{M_2}\,t_{d1} \tag{A.17}$$

$$t_1 = t_2 \tag{A.18}$$

Equation A.12 is solved for the optimal coarse ramp rate.

$$M_1 = \sqrt{\frac{V_{MAX}\,M_2}{\frac{\Delta M}{M}\,t_{d1}}} \tag{A.19}$$

Substituting equation A.19 into equation A.8 leaves the total charge transfer time in terms of the comparator delays, t_{d1} and t_{d2}, the ramp nonlinearity ,$\frac{\Delta M}{M}$ and the fine phase ramp rate, M_2.

$$t_{t2} = 2\sqrt{\frac{\frac{\Delta M}{M}\,t_{d1}\,V_{MAX}}{M_2}} + \frac{\Delta M}{M}\,t_{d1} + t_{d2} \tag{A.20}$$

Substituting equation A.9 into equation A.20 replaces the fine phase ramp rate with the known final overshoot.

$$t_{t2} = 2\sqrt{\frac{\frac{\Delta M}{M}\,t_{d1}\,t_{d2}\,V_{MAX}}{V_{OV2}}} + \frac{\Delta M}{M}\,t_{d1} + t_{d2} \tag{A.21}$$

If the comparator delays in the coarse and fine charge transfers are fixed and equal $t_{d1} = t_{d2} = t_d$, equation A.21 simplifies to

$$t_{t2} = 2\sqrt{\frac{\frac{\Delta M}{M}\,V_{MAX}}{V_{OV2}}}\,t_d + \frac{\Delta M}{M}\,t_d + t_d. \tag{A.22}$$

Dividing the total charge transfer time t_{t2} by the delay time t_d produces the number of comparator delays $m_2 = \frac{t_{t2}}{t_d}$ needed to achieve the linearity constraint.

$$m_2 = 2\sqrt{\frac{\frac{\Delta M}{M}\,V_{MAX}}{V_{OV2}}} + \frac{\Delta M}{M} + 1 \tag{A.23}$$

Substituting equation A.10 into equation A.23 leaves the required number of delays

$$m_2 = \frac{\Delta M}{M}\sqrt{\frac{V_{MAX}}{V_{FS}}}2^{\frac{B}{2}+1} + \frac{\Delta M}{M} + 1, \tag{A.24}$$

in known terms: the ramp nonlinearity $\frac{\Delta M}{M}$, the maximum output voltage V_{MAX}, the full scale voltage V_{FS} and the required number of bits B.

If the comparator delays in the coarse and fine charge transfers are not equal $t_{d1} \neq t_{d2}$, a required number of comparator delay cannot be determined. If the coarse phase comparator delay is fixed and known the maximum value of the fine phase comparator delay can be determined for a circuit operating at a specific sampling frequency f_s. The total charge transfer time must be less than half of of the sampling clock period, therefore

$$t_{t2} = \frac{T}{2} = \frac{1}{2\,f_s}. \tag{A.25}$$

Substituting equation A.25 into with equation A.21 leaves

$$\frac{1}{2\,f_s} = 2\sqrt{\frac{\frac{\Delta M}{M}\,t_{d1}\,t_{d2}\,V_{MAX}}{V_{OV2}}} + \frac{\Delta M}{M}\,t_{d1} + t_{d2} \tag{A.26}$$

Rearranging equation A.26 leaves

$$t_{d2} + 2\sqrt{\frac{\frac{\Delta M}{M}\,t_{d1}\,V_{MAX}}{V_{OV2}}}\sqrt{t_{d2}} + \frac{\Delta M}{M}\,t_{d1} - \frac{1}{2\,f_s} = 0. \tag{A.27}$$

Solving equation A.27 produces the maximum value for the fine phase comparator delay

$$t_{d2} = 2\frac{V_{MAX}}{V_{OV2}}\frac{\Delta M}{M}\,t_{d1}\left(1 - \sqrt{1 - \frac{V_{OV2}}{V_{MAX}} + \frac{1}{2}\frac{V_{OV2}}{V_{MAX}}\frac{t_{d1}}{T}\frac{1}{\frac{\Delta M}{M}}}\right) - \frac{\Delta M}{M}\,t_{d1} + \frac{T}{2}. \tag{A.28}$$

The maximum fraction of the half clock cycle taken up by the comparator delay will be the same for any sampling frequency as long as the fixed delay scales with clock frequency. If the fine phase comparator is an integrating type comparator 5.42 is

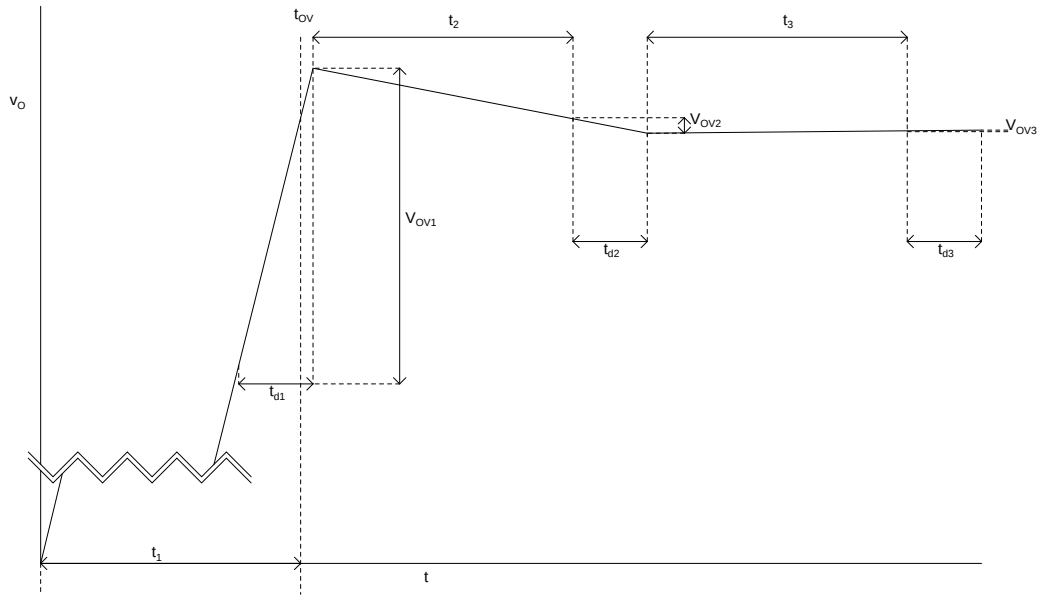


Figure A-2: Three-phase circuit output voltage

substituted into A.28 and the delay time can be related to the transconductance of the comparator using the following equation,

$$g_m = \frac{4\,V_M\,C}{V_{OV2}\,t_{d2}}. \tag{A.29}$$

The required transconductance of the comparator is related to the minimum power consumption of the circuit through the drain current and transconductance relationship of the input pair transistors of the comparator.

A.2 Three Phase CBSC Circuit

The three phase CBSC charge transfer is shown in Figure A-2. The total charge transfer time, t_{t3}, consists of the following intervals: the initial charging time t_1, the first phase overshoot time t_{ov}, the first overshoot recovery time t_2, the second phase comparator delay t_{d2}, the second overshoot recovery time t_3, and the third phase comparator delay t_{d3}

$$t_{t3} = t_1 + t_{ov} + t_2 + t_{d2} + t_3 + t_{d3} \tag{A.30}$$

The initial charging time t_1 equals the maximum possible output voltage V_{MAX} divided by the first phase ramp rate M_1,

$$t_1 = \frac{V_{MAX}}{M_1}. \tag{A.31}$$

The coarse overshoot time t_{ov} equals the residual first phase overshoot V_{OV1r} divided by the first phase ramp rate M_1,

$$t_{ov} = \frac{V_{OV1r}}{M_1}. \tag{A.32}$$

From equation 5.34

$$V_{OV1r} = \frac{\Delta M}{M} V_{OV1}. \tag{A.33}$$

Substituting equation A.33 into equation A.32 leaves

$$t_{ov} = \frac{\Delta M}{M} t_{d1}. \tag{A.34}$$

The first overshoot recovery time t_2 equals the residual first phase overshoot V_{OV1r} divided by the second phase ramp rate M_2,

$$t_2 = \frac{V_{OV1r}}{M_2}. \tag{A.35}$$

From equation 5.34, the second phase residual overshoot is

$$V_{OV2r} = \frac{\Delta M}{M} V_{OV2}. \tag{A.36}$$

The first overshoot recovery time t_2 equals

$$t_2 = \frac{\Delta M}{M} \frac{M_1}{M_2} t_{d1}. \tag{A.37}$$

The second overshoot recovery time t_3 equals the residual second phase overshoot V_{OV2r} divided by the third phase ramp rate M_3,

$$t_3 = \frac{V_{OV2r}}{M_3} = \frac{\Delta M}{M}\,\frac{M_2}{M_3}\,t_{d2} \tag{A.38}$$

The total charge transfer time equals

$$t_{t3} = \frac{V_{MAX}}{M_1} + \frac{\Delta M}{M}\,t_{d1} + \frac{\Delta M}{M}\,\frac{M_1}{M_2}\,t_{d1} + t_{d2} + \frac{\Delta M}{M}\,\frac{M_2}{M_3}\,t_{d2} + t_{d3}. \tag{A.39}$$

In order to determine the minimum charge transfer time the first M_1, second M_2, and third M_3 ramp rates must be determined. The third phase ramp rate M_3 is determined from equation 5.42 and a linearity constraint

$$M_3 = \frac{V_{OV3}}{t_{d3}} \tag{A.40}$$

The final phase overshoot is chosen to be as large as possible while meeting the linearity constraint,

$$V_{OV3} = \frac{V_{FS}\,2^{-B}}{\frac{\Delta M}{M}} \tag{A.41}$$

The first phase M_1 and second phase M_2 ramp rates are chosen to produce the shortest charge transfer time. In order to determine these values of M_1 and M_2 the charge transfer time is differentiated with respect to M_1 and the results set equal to zero and then is differentiated with respect to M_2 and the result is set equal to zero.

$$\frac{dt_{t3}}{dM_1} = 0 \tag{A.42}$$

$$\frac{dt_{t3}}{dM_1} = -\frac{V_{MAX}}{M_1^2} + \frac{\Delta M}{M}\,\frac{t_{d1}}{M_2} \tag{A.43}$$

The value of M_1 is shown to produce the minimum charge transfer time by demonstrating that the second derivative of the charge transfer time is greater than zero.

$$\frac{d^2 t_{t3}}{dM_1^2} = \frac{2\,V_{MAX}}{M_1^3} > 0 \tag{A.44}$$

$$-\frac{V_{MAX}}{M_1^2} + \frac{\Delta\,M}{M}\,\frac{t_{d1}}{M_2} = 0 \tag{A.45}$$

$$\frac{V_{MAX}}{M_1^2} = \frac{\Delta\,M}{M}\,\frac{t_{d1}}{M_2} \tag{A.46}$$

$$\frac{V_{MAX}}{M_1} = \frac{\Delta\,M}{M}\,\frac{M_1}{M_2}\,t_{d1} \tag{A.47}$$

As in the two phase circuit the minimum charge transfer occurs when the initial charging time equals the first overshoot recovery time,

$$t_1 = t_2. \tag{A.48}$$

Equation A.45 is solved for the optimal first ramp rate in terms of known factors and the second phase ramp rate M_2,

$$M_1 = \sqrt{\frac{V_{MAX}\,M_2}{\frac{\Delta\,M}{M}\,t_{d1}}}. \tag{A.49}$$

The second phase ramp rate M_2 is determined by differentiating the total charge transfer time with respect to M_2 and setting the result equal to zero.

$$\frac{dt_{t3}}{dM_2} = 0 \tag{A.50}$$

$$\frac{dt_{t3}}{dM_2} = -\frac{\Delta\,M}{M}\,\frac{M_1}{M_2^2}\,t_{d1} + \frac{\Delta\,M}{M}\,\frac{1}{M_3}\,t_{d2} \tag{A.51}$$

The value of M_2 is shown to produce the minimum charge transfer time by demonstrating that the second derivative of the charge transfer time is greater than zero.

$$\frac{d^2 t_{t3}}{dM_2^2} = 2\,\frac{\Delta M}{M}\,\frac{M_1}{M_2^3}\,t_{d1} > 0 \tag{A.52}$$

$$-\frac{\Delta M}{M}\,\frac{M_1}{M_2^2}\,t_{d1} + \frac{\Delta M}{M}\,\frac{1}{M_3}\,t_{d2} = 0 \tag{A.53}$$

$$\frac{\Delta M}{M}\,\frac{M_1}{M_2^2}\,t_{d1} = \frac{\Delta M}{M}\,\frac{1}{M_3}\,t_{d2} \tag{A.54}$$

$$\frac{\Delta M}{M}\,\frac{M_1}{M_2}\,t_{d1} = \frac{\Delta M}{M}\,\frac{M_2}{M_3}\,t_{d2} \tag{A.55}$$

The minimum charge transfer occurs when the first overshoot recovery time t_2 equals the second overshoot recovery time t_3,

$$t_2 = t_3. \tag{A.56}$$

Substituting equation A.48 into equation A.56 shows that the minimum charge transfer time occurs when initial charging time t_1 equals the first overshoot recovery time t_2 and the second overshoot recovery time t_3,

$$t_1 = t_2 = t_3. \tag{A.57}$$

Solving equation A.53 for M_2 produces

$$M_2 = \sqrt{M_1\,M_3\frac{t_{d1}}{t_{d2}}}. \tag{A.58}$$

Substituting equation A.49 into equation A.58 leaves

$$M_2 = \sqrt{\sqrt{\frac{V_{MAX}\,M_2}{\frac{\Delta M}{M}\,t_{d1}}}\,M_3\frac{t_{d1}}{t_{d2}}}. \tag{A.59}$$

Rearranging equation A.59 produces the equation,

$$M_2^{\frac{3}{4}} = V_{MAX}^{\frac{1}{4}} \left(\frac{\Delta M}{M}\right)^{\frac{-1}{4}} t_{d1}^{\frac{-1}{4}} M_3^{\frac{1}{2}} t_{d1}^{\frac{1}{2}} t_{d2}^{\frac{-1}{2}}. \tag{A.60}$$

Simplfying A.60 leaves an equation of known values,

$$M_2 = V_{MAX}^{\frac{1}{3}} \left(\frac{\Delta M}{M}\right)^{\frac{-1}{3}} M_3^{\frac{2}{3}} t_{d1}^{\frac{1}{3}} t_{d2}^{\frac{-2}{3}}. \tag{A.61}$$

Substituting equation A.61 into equation A.49 leaves an expression for M_1,

$$M_1 = V_{MAX}^{\frac{1}{2}} V_{MAX}^{\frac{1}{6}} \left(\frac{\Delta M}{M}\right)^{\frac{-1}{6}} M_3^{\frac{1}{3}} t_{d1}^{\frac{1}{6}} t_{d2}^{\frac{-1}{3}} \frac{\Delta M}{M}^{\frac{-1}{2}} t_{d1}^{\frac{-1}{2}} \tag{A.62}$$

Simplifying equation A.62 leaves an equation of known values,

$$M_1 = V_{MAX}^{\frac{2}{3}}, M_3^{\frac{1}{3}} t_{d2}^{\frac{-1}{3}} \left(\frac{\Delta M}{M}\right)^{\frac{-2}{3}} t_{d1}^{\frac{-1}{3}}. \tag{A.63}$$

Substituting the expressions for M_1 and M_2 shown equation A.62 and equation A.61 into equation A.39 leaves the total charge transfer time in terms of the comparator delays, t_{d1}, t_{d2} and t_{d3} the ramp nonlinearity ,$\frac{\Delta M}{M}$ and the third phase ramp rate, M_3.

$$t_{t3} = 3\sqrt[3]{\frac{(\frac{\Delta M}{M})^2 t_{d1} t_{d2} V_{MAX}}{M_3}} + \frac{\Delta M}{M} t_{d1} + t_{d2} + t_{d3} \tag{A.64}$$

Substituting equation A.40 into equation A.20 replaces the third phase ramp rate with the known final overshoot.

$$t_{t3} = 3\sqrt[3]{\frac{(\frac{\Delta M}{M})^2 t_{d1} t_{d2} t_{d3} V_{MAX}}{V_{OV3}}} + \frac{\Delta M}{M} t_{d1} + t_{d2} + t_{d3} \tag{A.65}$$

If the comparator delays in the three charge transfer phases are fixed and equal

$t_{d1} = t_{d2} = t_{d3} = t_d$, equation A.65 simplifies to

$$t_{t3} = 3\sqrt[3]{\frac{(\frac{\Delta M}{M})^2 V_{MAX}}{V_{OV3}}}\, t_d + \frac{\Delta M}{M}\, t_d + t_d + t_d \tag{A.66}$$

Dividing the total charge transfer time t_{t3} by the delay time t_d produces the number of comparator delays $m_3 = \frac{t_{t3}}{t_d}$ needed to achieve the linearity constraint,

$$m_3 = 3\sqrt[3]{\frac{(\frac{\Delta M}{M})^2 V_{MAX}}{V_{OV3}}} + \frac{\Delta M}{M} + 2. \tag{A.67}$$

Substituting equation A.41 into equation A.67 leaves the required number of delays,

$$m_3 = 3\frac{\Delta M}{M}\sqrt[3]{\frac{V_{MAX}}{V_{FS}}}2^{\frac{B}{3}} + \frac{\Delta M}{M} + 2 \tag{A.68}$$

in known terms: the ramp nonlinearity $\frac{\Delta M}{M}$, the maximum output voltage V_{MAX}, the full scale voltage V_{FS}, and the required number of bits, B.

If the comparator delays in the three charge transfer phases are not equal $t_{d1} \neq t_{d2} \neq t_{d3}$, a required number of comparator delay cannot be determined. If comparator delays of the first two phases are fixed and known the maximum value of the coarse phase comparator delay can be determined for a circuit operating at a specific sampling frequency f_s. The total charge transfer time must be less than half of of the sampling clock period, therefore

$$t_{t3} = \frac{T}{2} = \frac{1}{2\, f_s} \tag{A.69}$$

Substituting equation A.69 into equation A.65 leaves

$$\frac{1}{2\, f_s} = 3\sqrt[3]{\frac{(\frac{\Delta M}{M})^2\, t_{d1}\, t_{d2}\, t_{d3}\, V_{MAX}}{V_{OV3}}} + \frac{\Delta M}{M}\, t_{d1} + t_{d2} + t_{d3} \tag{A.70}$$

Rearranging equation A.70 leaves a cubic equation,

$$t_{d3} + 3\sqrt[3]{\frac{(\frac{\Delta M}{M})^2\, t_{d1}\, t_{d2}\, V_{MAX}}{V_{OV3}}}\sqrt[3]{t_{d3}} + \frac{\Delta M}{M}\, t_{d1} + t_{d2} - \frac{1}{2\, f_s} = 0. \tag{A.71}$$

Solving equation A.71 produces an complicated expression for t_{d3} which is omitted here. The expression is in terms of know values. If the comparator used in the final phase is an integrating type comparator 5.42 is substituted into the equation for t_{d3} and the transconductance of the comparator input pair required to meet speed and linearity requirements is

$$g_m = \frac{4\, V_M\, C}{V_{OV3}\, t_{d3}}. \tag{A.72}$$

The power consumption of the circuit is determined from the required transconductance and the operating region of the input pair.

Appendix B

Cascode Bias analysis

This Appendix explains the operation of the Sooch cascode bias circuit [33, 34].

B.1 Sooch Cascode Bias Circuit

The Sooch Cascode Bias is shown in B.1. The circuit serves to set the voltage at the gate of P_1 at $|V_T + \Delta V|$ below V_{DD} and the gate of P_2 at $|V_T + 2\Delta V|$. In order to do this $|\Delta V|$ must be dropped across P_5. Making the width of P_5 $\frac{1}{3}$ the width of the other transistors causes its V_{DS} to be the required ΔV. To see why P_5 drops the correct value we first determine the drain currents of P_5 and P_6. P_6 is a diode connected device so it must be in saturation. P_5 cannot be saturated because $V_{SG6} = V_{DG5}$ and V_{SG6} is large enough to invert the in channel of P_6. Therefore the drain of P_5 cannot be pitched off and consequently P_5 cannot be saturated. Since P_6 is saturated and P_5 is in triode their drain currents are

$$I_{D6} = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}(|V_{GS6}| - |V_T|)^2, \tag{B.1}$$

and

$$I_{D5} = \frac{1}{2}\frac{W_5}{L_5}\mu_p C_{OX}((2\,|V_{GS5}| - |V_T|)\,|V_{DS5}| - |V_{DS5}|^2). \tag{B.2}$$

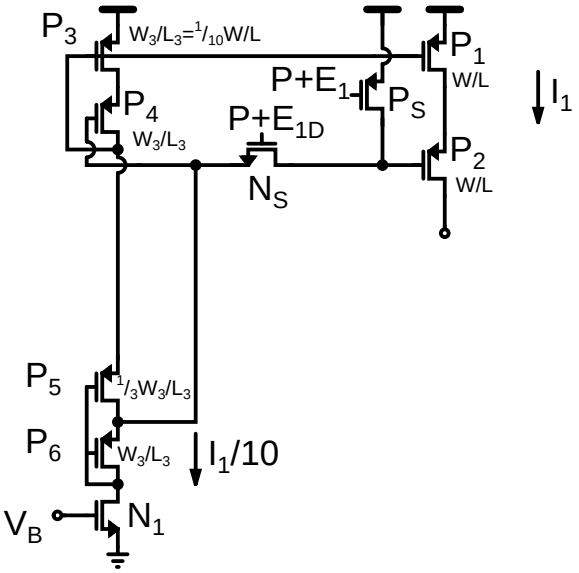


Figure B-1: Coarse current source with Sooch Bias.

Substituting $\frac{W_5}{L_5} = \frac{1}{3}\frac{W_6}{L_6}$ into I_{D5} produces

$$I_{D5} = \frac{1}{2}\frac{1}{3}\frac{W_6}{L_6}\mu_p C_{OX}((2\,|V_{GS5}| - |V_T|)\,|V_{DS5}| - |V_{DS5}|^2). \tag{B.3}$$

Setting $I_{D6} = I_{D5}$ leaves

$$\frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}(|V_{GS6}| - |V_T|)^2 = \frac{1}{2}\frac{1}{3}\frac{W_6}{L_6}\mu_p C_{OX}((2\,|V_{GS5}| - |V_T|)\,|V_{DS5}| - |V_{DS5}|^2). \tag{B.4}$$

Equation B.4 simplifies to

$$(|V_{GS6}| - |V_T|)^2 = \frac{1}{3}((2\,|V_{GS5}| - |V_T|)\,|V_{DS5}| - |V_{DS5}|^2). \tag{B.5}$$

Since P_6 is diode connected,

$$|V_{GS6}| = |V_T| + |\Delta\, V|. \tag{B.6}$$

Knowing that

$$|V_{GS6}| = |V_{GS5}| - |V_{DS5}|, \tag{B.7}$$

the V_{GS} of P_5 is

$$|V_{GS5}| = |V_{GS6}| + |V_{DS5}|. \tag{B.8}$$

Substituting equation B.8 into equation B.5 leaves

$$(|V_{GS6}| - |V_T|)^2 = \frac{1}{3}((2\,|V_{GS6}| + |V_{DS5}| - |V_T|)\,|V_{DS5}| - |V_{DS5}|^2). \tag{B.9}$$

Substituting equation B.6 into equation B.9 leaves

$$(|\Delta\, V|)^2 = \frac{1}{3}((2\,|\Delta\, V| + |V_{DS5}|)\,|V_{DS5}| - |V_{DS5}|^2). \tag{B.10}$$

Equation B.10 simplifies to

$$(|\Delta\, V|)^2 = \frac{2}{3}|\Delta\, V||V_{DS5}| + \frac{2}{3}|V_{DS5}|^2 - |V_{DS5}|^2, \tag{B.11}$$

and

$$|\Delta\, V|^2 = \frac{2}{3}|\Delta\, V||V_{DS5}| - \frac{1}{3}|V_{DS5}|^2, \tag{B.12}$$

and

$$-\frac{1}{3}|V_{DS5}|^2 + \frac{2}{3}|\Delta\, V||V_{DS5}| + |\Delta\, V|^2 = 0, \tag{B.13}$$

and finally

$$|V_{DS5}|^2 - 2|\Delta\, V||V_{DS5}| + |\Delta\, V|^2 = 0. \tag{B.14}$$

Solving for V_{DS5} leaves

$$V_{DS5} = |\Delta\, V|. \tag{B.15}$$

Therefore setting the width of P_5 at $\frac{1}{3}$ the width of the other transistors causes the required voltage to drop across P_5. The Sooch mirror produces allows for a wide swing and requires only one leg for biasing.

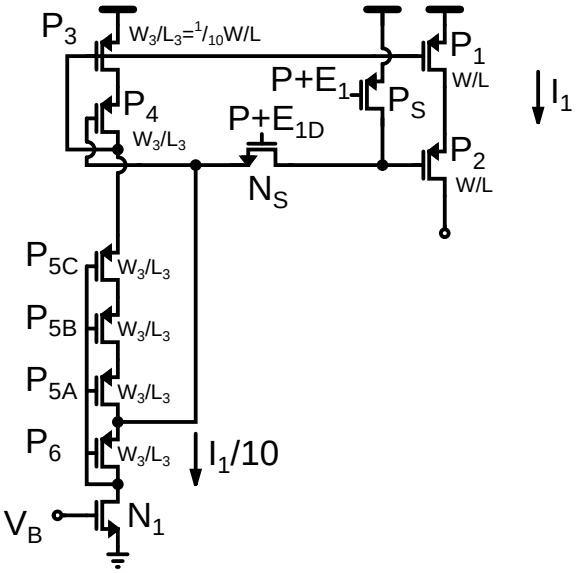


Figure B-2: Coarse current source with Sooch Bias using series triode devices.

B.2 Sooch Cascode Bias Circuit Using Series Triode Devices

The prototype uses the mirror shown in figure B.2 rather than the mirror shown in figure B.2, because the series transistors in the former circuit are easier to layout and match the rest of the mirror better than the narrow device in the former circuit. The three series devices biased in triode [44], P_{5A}, P_{5B} and P_{5C}, perform the same purpose as the single narrow device, P_5. In order for the three devices to perform the same purpose $|V_{DS5A}| + |V_{DS5B}| + |V_{DS5C}|$ must equal $|\Delta V|$. The following analysis shows that this is true. First V_{DS5A} is determined. The drain currents of P_6 and P_{5A} are

$$I_{D6} = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}(|V_{GS6}| - |V_T|)^2, \tag{B.16}$$

and

$$I_{D5A} = \frac{1}{2}\frac{W_5 A}{L_5 A}\mu_p C_{OX}((2\,|V_{GS5A}| - |V_T|)\,|V_{DS5A}| - |V_{DS5A}|^2). \tag{B.17}$$

Simplifying I_{D5A} leaves

$$I_{D5A} = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}((2\,|V_{GS5A}| - |V_T|)\,|V_{DS5A}| - |V_{DS5A}|^2). \tag{B.18}$$

Setting $I_{D6} = I_{D5A}$ leaves

$$\frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}(|V_{GS6}| - |V_T|)^2 = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}((2\,|V_{GS5A}| - |V_T|)\,|V_{DS5A}| - |V_{DS5A}|^2). \tag{B.19}$$

Simplifying B.19 leaves

$$(|V_{GS6}| - |V_T|)^2 = ((2\,|V_{GS5A}| - |V_T|)\,|V_{DS5A}| - |V_{DS5A}|^2). \tag{B.20}$$

Since P_6 is diode connected,

$$|V_{GS6}| = |V_T| + |\Delta\, V|. \tag{B.21}$$

Knowing that

$$|V_{GS6}| = |V_{GS5A}| - |V_{DS5A}| \tag{B.22}$$

the V_{GS} of P_{5A} is

$$|V_{GS5A}| = |V_{GS6}| + |V_{DS5A}|. \tag{B.23}$$

Substituting equation B.23 into equation B.20 leaves

$$(|V_{GS6}| - |V_T|)^2 = ((2\,|V_{GS6}| + |V_{DS5A}| - |V_T|)\,|V_{DS5A}| - |V_{DS5A}|^2). \tag{B.24}$$

Equation B.24 simplifies to

$$(|\Delta\, V|)^2 = ((2\,|\Delta\, V| + |V_{DS5A}|)\,|V_{DS5A}| - |V_{DS5A}|^2), \tag{B.25}$$

and

$$(|\Delta\, V|)^2 = 2|\Delta\, V||V_{DS5A}| + 2|V_{DS5A}|^2 - |V_{DS5A}|^2, \tag{B.26}$$

and

$$|\Delta V|^2 = 2|\Delta V||V_{DS5A}| + |V_{DS5A}|^2, \tag{B.27}$$

and finally

$$|V_{DS5A}|^2 + 2|\Delta V||V_{DS5A}| - |\Delta V|^2 = 0. \tag{B.28}$$

Solving for V_{DS5A} leaves

$$V_{DS5A} = (\sqrt{2} - 1)|\Delta V|. \tag{B.29}$$

The procedure above is repeated to determine V_{DS5B}.

$$I_{D6} = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}(|V_{GS6}| - |V_T|)^2 \tag{B.30}$$

$$I_{D5B} = \frac{1}{2}\frac{W_5 B}{L_5 B}\mu_p C_{OX}((2\,|V_{GS5B}| - |V_T|)\,|V_{DS5B}| - |V_{DS5B}|^2) \tag{B.31}$$

$$I_{D5B} = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}((2\,|V_{GS5B}| - |V_T|)\,|V_{DS5B}| - |V_{DS5B}|^2) \tag{B.32}$$

$$I_{D6} = I_{D5B} \tag{B.33}$$

$$\frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}(|V_{GS6}| - |V_T|)^2 = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}((2\,|V_{GS5B}| - |V_T|)\,|V_{DS5B}| - |V_{DS5B}|^2) \tag{B.34}$$

$$(|V_{GS6}| - |V_T|)^2 = ((2\,|V_{GS5B}| - |V_T|)\,|V_{DS5B}| - |V_{DS5B}|^2) \tag{B.35}$$

$$|V_{GS5B}| = |V_{GS5A}| + |V_{DS5B}| \tag{B.36}$$

$$|V_{GS5B}| = |V_{GS6}| + |V_{DS5A}| + |V_{DS5B}| \tag{B.37}$$

$$(|V_{GS6}| - |V_T|)^2 = ((2\,|V_{GS6}| + |V_{DS5A}| + |V_{DS5B}| - |V_T|)\,|V_{DS5B}| - |V_{DS5B}|^2) \tag{B.38}$$

$$(|\Delta V|)^2 = ((2\,|\Delta V| + 2(\sqrt{2} - 1)|\Delta V| + |V_{DS5B}|)\,|V_{DS5B}| - |V_{DS5B}|^2) \tag{B.39}$$

$$(|\Delta V|)^2 = 2\sqrt{2}|\Delta V||V_{DS5B}| + 2|V_{DS5B}|^2 - |V_{DS5B}|^2 \tag{B.40}$$

$$|V_{DS5B}|^2 + 2\sqrt{2}|\Delta V||V_{DS5B}| - |\Delta V|^2 = 0 \tag{B.41}$$

$$V_{DS5B} = (\sqrt{3} - \sqrt{2})|\Delta V| \tag{B.42}$$

The procedure is repeated again to determine V_{DS5C}.

$$I_{D6} = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}(|V_{GS6}| - |V_T|)^2 \tag{B.43}$$

$$I_{D5C} = \frac{1}{2}\frac{W_5 C}{L_5 C}\mu_p C_{OX}((2\,|V_{GS5C}| - |V_T|)\,|V_{DS5C}| - |V_{DS5C}|^2) \tag{B.44}$$

$$I_{D5C} = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}((2\,|V_{GS5C}| - |V_T|)\,|V_{DS5C}| - |V_{DS5C}|^2) \tag{B.45}$$

$$I_{D6} = I_{D5C} \tag{B.46}$$

$$\frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}(|V_{GS6}| - |V_T|)^2 = \frac{1}{2}\frac{W_6}{L_6}\mu_p C_{OX}((2\,|V_{GS5C}| - |V_T|)\,|V_{DS5C}| - |V_{DS5C}|^2) \tag{B.47}$$

$$(|V_{GS6}| - |V_T|)^2 = ((2\,|V_{GS5C}| - |V_T|)\,|V_{DS5C}| - |V_{DS5C}|^2) \tag{B.48}$$

$$|V_{GS5C}| = |V_{GS5B}| + |V_{DS5C}| \tag{B.49}$$

$$|V_{GS5C}| = |V_{GS6}| + |V_{DS5A}| + |V_{DS5B}| + |V_{DS5C}| \tag{B.50}$$

$$(|V_{GS6}| - |V_T|)^2 = ((2\,|V_{GS6}| + |V_{DS5B}| + |V_{DS5A}| + |V_{DS5C}| - |V_T|)\,|V_{DS5C}| - |V_{DS5C}|^2) \tag{B.51}$$

$$(|\Delta V|)^2 = ((2\,|\Delta V| + 2(\sqrt{2}-1)|\Delta V| + 2(\sqrt{3}-\sqrt{2})|\Delta V| + |V_{DS5C}|)\,|V_{DS5C}| - |V_{DS5C}|^2) \tag{B.52}$$

$$(|\Delta V|)^2 = 2\sqrt{3}|\Delta V||V_{DS5C}| + 2|V_{DS5C}|^2 - |V_{DS5C}|^2 \tag{B.53}$$

$$|V_{DS5C}|^2 + 2\sqrt{3}|\Delta V||V_{DS5C}| - |\Delta V|^2 = 0 \tag{B.54}$$

$$V_{DS5C} = (\sqrt{4} - \sqrt{3})|\Delta V| \tag{B.55}$$

$$V_{DS5C} = (2 - \sqrt{3})|\Delta V| \tag{B.56}$$

Adding up the three drain-to-source voltages leaves

$$V_{DS5T} = V_{DS5A} + V_{DS5B} + V_{DS5C} = (\sqrt{2}-1)|\Delta V| + (\sqrt{3}-\sqrt{2})|\Delta V| + (\sqrt{4}-\sqrt{3})|\Delta V|. \tag{B.57}$$

This simplifies to

$$V_{DS5T} = |\Delta V|. \tag{B.58}$$

Therefore the three series transistors provide the same effect as the one narrow transistor in the original circuit. Both circuits bias the cascode current source for a wide swing with a single bias leg.