Construction and Operation of a Mirror Langmuir Probe Diagnostic for the Alcator C-Mod Tokamak

by

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ABSTRACT

Langmuir probe diagnostic systems presently employed on Alcator C-Mod and elsewhere generally suffer from a severe limitation: unless multiple electrode or high-frequency bias techniques are employed, these systems can not resolve the rapid changes in plasma electron temperature, floating potential and ion saturation current that are associated with plasma turbulence. Moreover, no existing system can provide real-time output of these three parameters using a single electrode. To remedy this limitation, an advanced, high-bandwidth Langmuir probe system has been constructed for Alcator C-Mod using state-of-the-art design tools and components. The system produces a fast-switched, three-state probe bias waveform and employs a new method for outputting plasma conditions in real-time, a 'Mirror Langmuir Probe' (MLP), which utilizes high-bandwidth bipolar transistors to electrically simulate a Langmuir probe's response. Detailed information on the design, construction and performance of this new diagnostic is described in this thesis, representing the first proof-of-principle demonstration of the MLP technique. The MLP system was found to meet all the performance goals set forth at the beginning of the project: real-time output of electron temperature, floating potential and ion saturation current, ability to track changes in plasma parameters within a ~1 μs timescale, while utilizing only a single Langmuir electrode. The system was tested using an 'electronic Langmuir probe' and also using an actual Langmuir probe in Alcator C-Mod. In both cases, the system accurately locked onto changing plasma conditions (< ~5% error in outputted parameters), with the exception of some severe transient events found in C-Mod plasmas (ELMs), which challenged the system's accuracy. Further refinements to the system have been identified to handle such cases. The MLP clearly demonstrated superior performance to existing Langmuir probe systems on Alcator C-Mod and should enable researchers to study edge plasma turbulence in much greater detail in the future.

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Chapter 1 – Introduction

1.1 – Background and Motivation

Langmuir probes are one of the oldest and most fundamental plasma diagnostics. Their usefulness is demonstrated by the wide range of plasmas in which they can be used to infer plasma parameters [1-3]. From low temperature plasmas (~0.05 to ~5eV) to those of moderate temperature (~5eV to ~100eV) and high electron density (~10^{20} m^{-3}), a Langmuir probe can be used to measure local electron temperature, densities and electric potentials. Each of these parameters is obtained by applying a voltage (V) to a Langmuir probe and measuring the resultant current (I). From this I-V characteristic, parameters such as electron temperature, ion saturation current and floating potential can be deduced by fitting the data points with model parameters.

The most straightforward use of a Langmuir Probe involves only one electrode, which is inserted into the plasma region of interest and biased with respect to the metallic chamber that contains the plasma. The bias voltage is typically swept at a given frequency over a range that is comparable to the electron temperature. Transient analog-to-digital (A/D) recorders are typically used to record the Langmuir probe's I-V characteristic for a given plasma discharge. Plasma parameters of interest are later extracted during a post-processing step, where customized software is used to fit the I-V characteristic.

At the MIT Plasma Science and Fusion center, the tokamak plasma confinement experiment Alcator C-Mod makes use of several Langmuir Probes (single electrode type) at various locations to make plasma edge measurements using the method described above. Although this system works well in an ideal world, two principle issues have limited the effectiveness of the measurements made with these probes. First, owing to bandwidth limitations of the bias and I-V sensing electronics, the voltage applied to the probe is swept at a frequency of 2 kHz or less. This is an issue because plasma turbulence can change the local values of electron temperature, ion saturation current and floating potential over a much shorter time scale, on the order of a microsecond [4]. On the current Alcator systems, the turbulent fluctuations show up as 'noise' on

the I-V characteristic. The fitted data is therefore useful to track long time-scale trends only. Moreover, parameters derived from a least-squares fit to such a 'noisy' I-V characteristic may be in error since the I-V response is actually a nonlinear function of plasma potential and electron temperature fluctuations.

The second limitation deals with the post-processing needed to extract the plasma parameters from the I-V data points. Since the data processing step is computationally intensive, it can not provide researchers with valuable real-time information. For example, if real time values for the parameters were available, they could be used in a feedback system to alter the voltage waveform being applied. This is advantageous because the voltage bias to a Langmuir probe has an optimal range for a given set of plasma parameters. On the current Alcator system, a best guess is made before hand on what the average plasma parameters will be and the bias is set accordingly.

The limitations of the current Langmuir probe system on Alcator C-Mod are significant enough to necessitate an upgrade. What kind of upgrade to apply is where this thesis project begins. Alternative schemes already exist that have advantages over the current C-Mod system. These include the triple probe method [5], which can directly output all three plasma parameters of interest and the double probe method [6] that can output electron temperature directly. One clear drawback of these systems is that they involve more than one probe which means the current mechanical systems on C-Mod would have to be changed to accept additional probes. The second problem with these systems is the assumption that plasma parameters are the same at each probe for a given measurement, which because of turbulence [7] would almost never be the case.

Recently, a new idea for a Langmuir probe bias scheme was proposed based on the concept of a 'Mirror Langmuir Probe' (MLP) [8, 9]. The MLP utilizes only one electrode and involves a new concept of linking the I-V characteristics found in the edge of a magnetically confined plasma with the I-V characteristic found in bipolar RF transistors. By constructing a system of active feedback around the transistors, one can imagine a system that forces the rf transistors to mimic the Langmuir probe's I-V response in a scaled down manner. Once the I-V responses are

matched, the circuitry can output the plasma parameters in real-time. Furthermore, the entire system could utilize state-of-the-art components to ensure that the system will be fast enough to track the rapid (on the order of a microsecond) changes caused by the plasma turbulence.

The theoretical basis for the MLP has already been developed by Dr. Brian LaBombard of the MIT PSFC and was not the focus of this work. Instead, this thesis was concerned with the construction and operation of an actual MLP system. The scope of this thesis involved everything from initial proof-of-principle computer modeling through proto-board development of each subsystem to a final working version of the circuit boards that make up the MLP system.

1.2 – Goals and Outline of Thesis

The goal of this thesis was to build a working Mirror Langmuir Probe system for probes on Alcator C-Mod based on the concepts outlined by Dr. LaBombard. Chapter 2 covers the basics of Langmuir probes and demonstrates how the current systems in use today are not capable of resolving the effects of turbulence in magnetically confined fusion devices. An in-depth overview of Dr. LaBombard's theory is covered in Chapter 3, which subsequently sets the framework for the majority of the work performed on this project. Chapter 4 shows the fruit of this labor and details the circuit boards that achieved the design parameters specified by the MLP theory. A custom-designed electronics package was assembled using state-of-the art components and designed with the help of the latest circuit construction, simulation and fabrication tools. The OrCAD suite [10] of electronic design and simulation software was used for this purpose. In particular, this effort focused on the design and fabrication of the key components: a master-clock timing module (TTL Waveform Board), a fast-switching probe voltage drive board using high-voltage RF MOSFETs (FET Driver Board), and an analog computer board, implementing the Mirror-Probe method to deduce plasma parameters in real-time (MLP Data Board). While the performance of these circuits is also covered in Chapter 4, the bench testing of the system as a whole is reserved for Chapter 5. Finally, Chapter 6 presents results from initial tests of the MLP system using Langmuir probes on Alcator C-Mod. A summary of this thesis project with suggestion for future work is contained in Chapter 7.

Chapter 2 – Langmuir Probes

(Note: If the reader already possesses a basic knowledge of plasma physics and Langmuir probe theory, please skip to section 2.3 for a review of current probe techniques before moving onto Chapter 3)

Before an in-depth description of the Mirror Langmuir Probe (MLP) concept can be covered, a basic understanding of plasma physics is required. In particular, the interaction of the charged particles in a fully ionized plasma with a solid object is crucial to understanding what a Langmuir probe is used for and how it works. Please note that the analysis provided below is highly simplified, but accurate enough to explain the basic forces at work. In certain situations, such as with a magnetized plasma, the true complexity of this interaction reaches depths that are still not fully understood or correctly modeled to this day [11, 12].

2.1 – Plasma Basics

Plasma, quite simply, is the fourth state of matter. Unlike the other three states which involve the chemical bonding between atoms or molecules, a plasma is created when electrons are able to overcome the electric forces binding them to their orbits. When this binding energy is overcome by an electron, it becomes disassociated with the nucleus and is able to move on its own. The remaining atom is left with a net positive charge, becoming an ion. So long as the electron remains energetic enough to overcome the electric force attracting it to the ion, these two particles will not recombine. When sufficient numbers of these free electrons and ions exist in a region of space, they are collectively called the plasma state of matter.

The two most common methods to create a plasma are by either heating a gas to a high temperature where the atomic collisions are so strong that electrons are "knocked loose" or by exposing a gas to a strong enough electric field that the electrons are pulled from the atoms they occupy. Initially, only one electron is removed from an atom when it is ionized as the positive charge created on the atom by the departure of the first electron causes the energy needed to

remove a second one to be much higher. Furthermore, more stable atoms such as those with filled valance bands (i.e. helium atoms) require more energy to ionize than atoms with unfilled bands (i.e. hydrogen atoms).

When a large number of particles are ionized, they form a sea of positive and negative charges that must coexist together. Although these particles are energetic enough to keep from recombining, the negative and positive charges still affect each other and can create electric fields if too much of one charge builds up in a certain area. Because of these interactions, the plasma cloud quickly reaches a steady state where the net charge of any section of the cloud is always near zero. Although the ions and electrons are moving around this cloud, a net charge will never develop as long as an external force or perturbation is not introduced. Furthermore, through collisions, the populations of electrons and ions tend towards having the same temperature. As a result, the electrons have a much high velocity than the comparably massive ions [3].

2.2 – An Electric Probe in a Plasma

One of the first methods developed to study plasma was to simply insert an object into it (usually a conductor) and study its effect on the plasma. Although any object will do, a metallic probe will be used for this example. When an electrically isolated probe is instantaneously introduced to the plasma, it is exposed to the free flowing electrons and ions. Due to the electron's higher velocity, more electrons will initially strike the probe than ions, which causes a negative voltage to build on the probe in relation to the otherwise ambient potential of the plasma, Φ_P [13]. Eventually, the probe will start to repel a certain percentage of electrons as it becomes biased further negative. Meanwhile, the heavier, slow-moving ions become attracted by the probe, but can only approach the probe at the maximum "plasma-fluid" velocity, i.e., the sound speed [3]. Thus, even though the probe is building up negative charge, the ion particle flux on the probe tends to remain the same[1]. For this reason, the rate of ion collection by the probe is called the

[1] NOTE: For cylindrical or spherical probe geometries in a plasma without a magnetic field, the "ion saturation current" is more generally a function of V_b as the Debye shielding distance varies with bias. However, when a magnetic field is present, the motion of the ions is constrained to follow the field lines. In this case, the ion collection rate becomes independent of bias as long as the probe size is larger than the ion Larmor radius and the Debye length. The latter case is highlighted here.

"ion saturation current" (I_{sat}). Finally, the bias on the probe (V_b) will reach a level, called the floating potential (V_f), where the particle flux or current from the electrons (I_{elec}) has been reduced enough by the negative bias to be equal to the current coming from the ions. Thus, in this "floating state" the following equations are satisfied:

$$V_b = V_f \tag{2.1}$$

$$-I_{sat} = I_{electron} \tag{2.2}$$

$$I_{probe} = I_{electron} + I_{sat} = 0 \tag{2.3}$$

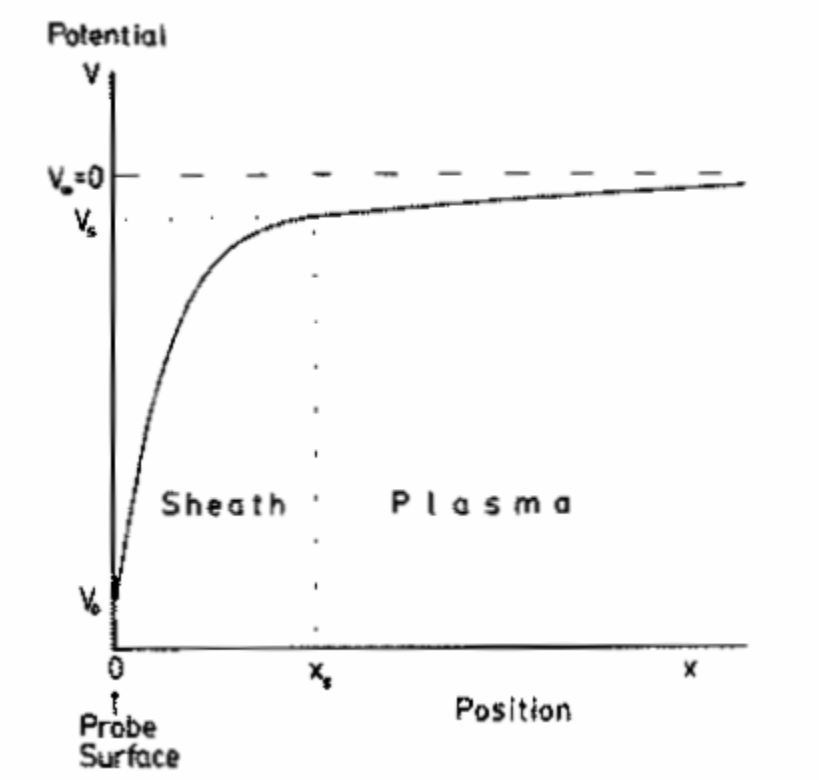


Figure 2.1 - Example of the Electric Potential Variation near the Surface of Probe [3]

Since this probe is now at a different potential level than the surrounding plasma, the previous unperturbed state of quasi-neutrality has been lost. The floating potential V_f is significantly more negative than the plasma potential with a difference that is typically on the order of three times the electron temperature (T_e) [14]. In order to maintain this state, the plasma creates a buffer zone around the probe called the sheath. This sheath region is very thin (on the order of the Debye length or roughly 3 - 30 μm in the edge region of a typical tokamak) and has a net

positive charge per unit volume that approximately equals the negative charge density on the probe. Thus, the charge of the sheath region cancels out the charge on the probe and the quasi-neutrality is restored for the rest of the plasma. This effective shielding of the plasma from the probe via the sheath is an important event because it localizes the plasma disturbance to a small region near the probe, keeping other regions unperturbed. Besides facilitating the region where the potential drop between the plasma and probe occurs, the effects of the sheath region can be largely ignored provided that the probe is much larger than the thickness of the region.

Although a probe placed into a plasma was used in the above example, the resultant effect applies for any plasma interaction with a floating solid object. Thus, if the plasma cloud is moved from free space into a container such as a vacuum vessel, the walls surrounding the plasma will undergo the same process and will be at the floating potential. The importance of this fact will be demonstrated by a more complex example. Using the plasma cloud inside of a vacuum vessel, a probe is inserted into the edge of the plasma and isolated separately from the vessel. A negative bias (Vp.) is now applied to the probe with respect to the vessel. At this bias level, the balance of electrons and ion current to the probe is disturbed as the energy required for an electron to reach the probe has now been increased. As the applied bias is decreased, a point is reached where effectively no electrons are able to reach the probe. Meanwhile the ion current, which is relatively unaffected by the bias level on the probe, is the only component remaining. Thus, by applying a negative bias to the probe relative to the floating potential and measuring the resultant current level, a measurement of the ion saturation current can be made. In this negative bias situation, the following equations are satisfied:

$$V_b = V_f + V_{p-} \tag{2.4}$$

$$I_{electron} \cong 0 \tag{2.5}$$

$$I_{probe} \cong I_{sat} \tag{2.6}$$

If a positive bias is applied to the probe (V_{p+}), a much different behavior is observed. Please note that $|V_{p+}|$ is not necessarily the same as $|V_{p-}|$. Ion saturation current remains the same as always, but the electron current component increases exponentially with increasing bias levels. Eventually, the electron component will dominate the total current on the probe. At sufficiently positive bias the electron current no longer increases, being limited by the "electron saturation"

level, but these levels of positive bias are outside of the realm of interest in this study. The exponential behavior of the electron current with bias arises from the Maxwellian distribution of electron velocities. As small changes in bias are applied to the probe, the energy required for an electron to reach the probe is decreased by small amounts. However, small changes in this energy level causes large increases in the electron flux and thus current to the probe. At this positive bias situation, one must account for both electron and ion collections. The following equations are satisfied:

$$V_b = V_f + V_{p+} \tag{2.7}$$

$$I_{probe} = I_{electron+} I_{sat} \tag{2.8}$$

The process described above of applying different bias levels to a probe immersed in plasma is known as a Langmuir probe, which is named after the plasma science pioneer and Nobel laureate who invented the technique, Dr. Irving Langmuir. The three distinct areas of plasma-probe interaction described above fuse together to yield a distinct probe current vs. probe voltage relationship when V_b is swept continuously from V_{p-} to V_{p+}. This typical response (shown in Figure 2.2) is commonly known as the Langmuir probe I-V characteristic and it contains a significant amount of information about the properties of the plasma being investigated. To extract this information, the mathematical description of Langmuir probe current as a function of applied bias voltage is presented as[2]:

$$I_p = I_{sat}\left(e^{(V_p - V_f)/T_e} - 1\right) \tag{2.9}$$

The exponential component represents the electron current and the constant component is only dependant on the ion saturation. It can be seen that plugging in the three levels of Vp into this equation satisfies the corresponding conditions specified above. This model has been generated using a much more detailed and quantitative approach to the plasmas' interaction with the probe, which can be found in most introductory plasma science texts and review articles [1-3, 14].

[2] Again, only the case of a probe immersed in a strong magnetic field is considered.

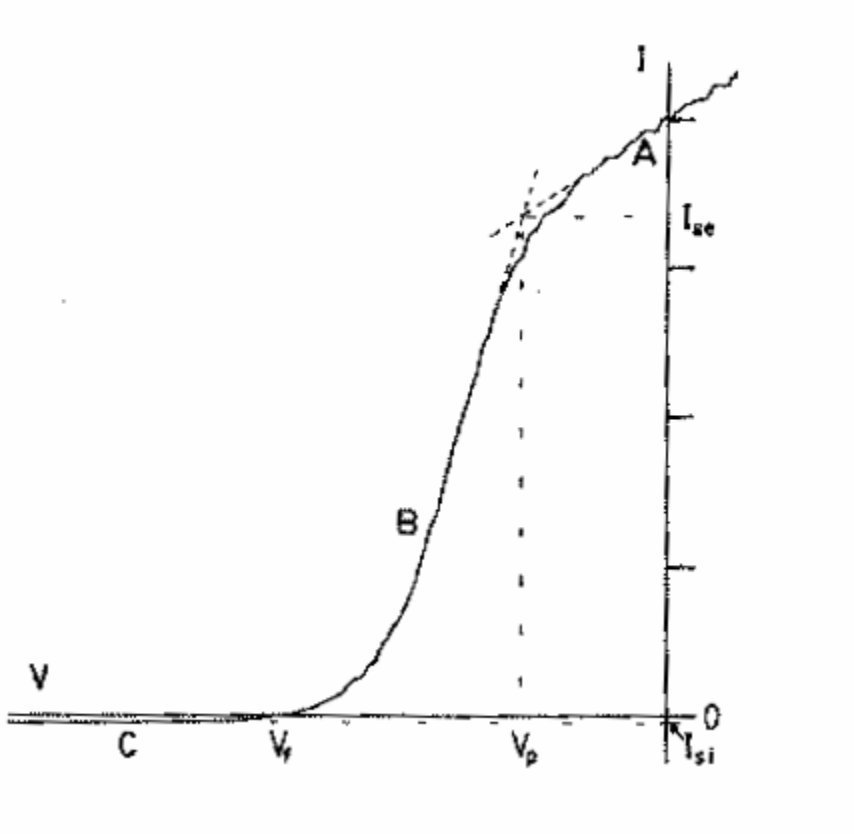


Figure 2.2 – Example of a Langmuir Probe I-V Characteristic [3]

In the ideal sense, this model provides a direct relationship between three plasma parameters of principle investigation (Isat, Vf and Te) and a current signal (Ip) which is easily controlled using a variable voltage source. All that is needed is for the voltage signal to be swept with a certain frequency (f) and predetermined amplitude (Vp) and to have the voltage and current signal recorded simultaneously in time. Software can then be used to post-possess the current and voltage data and fit the three parameters to the signals using a basic iterative algorithm. However, due to fluctuations in density, temperature and potential that exist in most hot plasmas, the practical implementation of this process proves to have difficulties. Thus, many variations of Langmuir probe bias techniques have been attempted, each of which has certain advantages and disadvantages with respect to each other. To date, no Langmuir probe technique has stood out as clearly superior to the basic method implemented by Dr. Langmuir nearly a century ago [9]. A brief overview of the current Langmuir probe methods is presented in the following section,

where the need for a new approach, such as the "Mirror Langmuir Probe" technique is highlighted.

2.3 – Langmuir Probe Methods

All Langmuir probe methods are interested in obtaining the current measurements in each of the three bias regions discussed in section 2.2. The techniques differ only in the two variables under control, which are how the bias is applied and how the current is measured.

The most common approach is to use the "single probe technique." This technique is used extensively on C-Mod. A periodic bias (usually a sinusoid) is applied to a single electrode and analog-to-digital converters are used to record both the voltage being applied and the resultant current as a function of time. When this data is finished being recorded, computer algorithms are then used to post-process the data and numerically fit Isat, Vf and Te. Achieving these measurements using a single probe is advantageous because all measurements are made at a single location in space. Using more than one probe to map an I-V characteristic demands that plasma conditions be identical at multiple locations, which can introduce significant error.

While this technique seems to obtain the desired measurements, a closer inspection reveals several flaws. First, the bias waveforms applied to most single probe set-ups, including the probes on C-Mod, are usually too slow to properly sample the changing conditions in the edge region of a tokamak plasma. While bias signals are typically swept at frequencies below 2 KHz, conditions in the plasma can change on the order of a microsecond. Thus, many of the parameter fluctuations happen too fast for the method to follow and important details are lost. Instead of obtaining a clear picture as to how these parameters behave in time under various circumstances, only the general, longer time scale trends can be followed. One may argue that only a faster bias signal and current measurement is needed to improve this resolution, which is true to some degree. However, implementing such a solution exacerbates the second drawback of this technique, which is the need to digitize, store and post-process the raw data. This data acquisition requires extensive additional hardware and makes the probe a rather inefficient diagnostic. It would be highly advantageous to obtain each of the three plasma parameters

directly, as the data storage and processing requirements could be significantly reduced. Also, measuring the parameter values in real-time would allow the possibility to use feedback to control the bias waveform based on the plasma conditions being experienced by the probe.

An alternative to the single-probe method is the use of multiple probes. By using additional probes, static voltages can be applied to each, which then directly outputs one plasma parameter. For example, a probe with no bias applied becomes a "floating" probe that only reports Vf. However, for this multiple probe set-up to be useful, the probes must all be interacting with a plasma that is the same at each probe interface. If the Vf experienced at the "floating" probe is not the same as the Vf experienced by the other probes measuring Isat or Te, then all three direct measurements are useless because they all do not represent readings from the same plasma. Unfortunately, every multiple Langmuir probe alternative developed to date makes this concession.

The following list shows the most common techniques in use today. The basic implementation, advantages and disadvantages of each are outlined.

(a) Triple probe technique [5]

- Three probes are operated simultaneously: a double probe with fixed differential bias and a single floating probe.
- Electron temperature is directly outputted, deduced from difference in floating probe and double probe potentials; ion saturation current and floating potential are also directly outputted.
- Advantage: direct readout of three plasma parameters.
- Disadvantage: plasma conditions must be identical at all three electrodes, even during turbulent fluctuations - a condition rarely satisfied.

(b) Admittance probe [15]

- A single frequency voltage drive is applied to a Langmuir electrode and a "dummy" electrode through a capacitor bridge.

- Change in probe admittance induced by the plasma is deduced, which is proportional to ion saturation current divided by electron temperature.
- Advantage: direct readout of ion saturation current divided by electron temperature.
- Disadvantage: need additional probe to measure ion saturation current; again, plasma conditions must be identical at both electrodes.

(c) Time-domain triple probe [16]

- A double probe is operated with voltage bias switched between positive, negative and floating states.
- Resultant *I*-*V* characteristics are digitized at high sampling rate and stored.
- Electron temperature, ion saturation current and floating potential are unfolded in way similar to the "triple probe technique" from the different bias states, assuming that electron temperature is unchanged during the "floating" state.
- Advantage: requires two electrodes - an improvement over triple the probe method.
- Disadvantage: need to digitize, store, and post process large data stream; again, plasma fluctuations must be identical at both electrodes.

(d) Fast-swept single Langmuir probe [16]

- A fast voltage sweep is applied to a single Langmuir electrode, using a "dummy" electrode to null a balanced current-sensing bridge in the absence of plasma.
- Resultant *I*-*V* characteristics are digitized at high sampling rate and store results.
- *I*-*V* characteristics are fit numerically with a model function, yielding electron temperature, ion saturation current, and floating potential.
- Advantage: requires only one electrode.
- Disadvantage: need to digitize, store, and post-process a large data stream.

(e) Harmonic probe current detection technique [17]

- A pure frequency voltage drive is applied to a single Langmuir probe, using a "dummy" Langmuir probe to null a balanced current-sensing bridge in absence of plasma.
- Ratio of first and second harmonic current signal is monitored with analog circuitry.

- An analog signal proportional to plasma electron temperature is outputted directly.
- Advantage: direct readout of plasma electron temperature using only one probe.
- Disadvantage: Additional probes needed for ion saturation current and floating potential measurements; again, plasma fluctuations must be identical at all electrodes.

This list illustrates that there is no one technique that is superior in all aspects. In constructing a new probe system for Alcator C-Mod, it would be most beneficial to target a method that has the following attributes:

- This new system must be able to directly output measurements for Isat, Vf and Te.
- It must utilize one probe to ensure all measurements are made under the same plasma conditions.
- All measurements must be generated and recorded in under a microsecond to ensure all significant fluctuations are properly resolved.

Once these primary objectives are reached, several secondary goals can also be established.

- To have the system use the real-time measurements to control and optimize its bias signal, which would generate better measurements.
- To build the system with expandability in mind, making the addition of more independent probes a relatively easy task.
- To utilize readily available components in the construction of the system and for ease of maintenance and to use state-of-the-art design methods to facilitate rapid fabrication.

As discussed in the introduction of this thesis, a new technique for the measurement of plasma parameters using a single electrode has been recently proposed, the "Mirror Langmuir Probe" [8, 9]. This method has the potential to satisfy all of the above goals and forms the basis of the new probe system developed in this thesis for Alcator C-Mod.

Chapter 3 – Mirror Langmuir Probe Theory

3.1 – Goals of New Langmuir Probe System

As a brief summary of Chapter 2, the primary and secondary goals of this next generation Langmuir probe system are as follows:

- Primary Goals
    - Output real-time signals of ion saturation current, electron temperature and floating potential
    - Operate at a high enough bandwidth to resolve plasma turbulence ($\geq$ 1 MHz)
    - Require only one Langmuir probe electrode
- Secondary Goals
    - Use real-time signals to control Langmuir probe bias and set to optimal level
    - Be expandable to handle at least 4 Langmuir electrodes to study plasma flows
    - Make use of off-the-shelf components and industry standard design tools to facilitate rapid reproduction and potential implementation of system at other fusion facilities

With these goals in mind, the background is set to introduce a new technique that can potentially meet all these criteria. This concept has been dubbed the 'Mirror Langmuir Probe' (MLP) by its creator, Dr. LaBombard of the MIT PSFC, and will be investigated in the sections below (much of this chapter's material is referenced from Dr. LaBombard's MLP concept paper [9]).

3.2 – Fundamental Theory of Mirror Langmuir Probe

The heart of the MLP theory lies with a key observation: With properly scaled voltages and currents, the non-linear I-V response of a pair of NPN and PNP transistors can be made to mimic the I-V characteristic of a Langmuir Probe [9]. This notion is demonstrated by comparing the fundamental equations that govern Langmuir probes and bipolar transistors. As discussed in Chapter 2, the current collected by a Langmuir probe consists of two components; the constant ion saturation current and the current due to the electrons, which is a function of the applied bias.

The interaction of these currents based on the bias of the probe yields equation 2.9, which is restated below:

$$I_p = I_{sat}\left(e^{(V_p - V_f)/T_e} - 1\right) \tag{2.9}$$

The current through the collector, I_C, of a bipolar transistor follows the Ebers-Moll equation, which is presented below [18]:

$$I_c = I_s\left(e^{(\alpha V_{BE})} - 1\right) \tag{3.1}$$

Here, I_S is the transistor saturation current, $\alpha = 1/T_{RT,}$ where T_{RT} is the temperature of the electrons in the transistor ($T_{RT} \approx 1/40$ volts at room temperature) and V_{BE} is the base-emitter voltage, which is the controlling variable [9, 18]. After a quick comparison, one might think that these equations are essentially equal and that a single transistor can be made to mimic a Langmuir probe I-V characteristic. A closer inspection, however, shows that unlike equation 2.9, the exponential term in the Ebers-Moll equation is always much larger than 1 in this application, so the -1 term in equation 3.1 is dropped. Thus, the Ebers-Moll model is left in a form where only the exponential term remains. From this result, the model illustrates that a single transistor lacks the constant current component needed to mimic the entire response of a Langmuir probe.

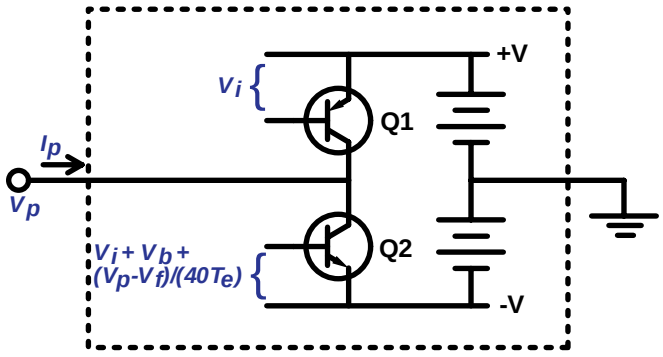


Figure 3.1 – Bipolar Transistor Pair Biased to Mimic Langmuir Probe Response [9]

Although a single bipolar transistor can not mimic the response of a Langmuir probe, the simplified circuit shown in Figure 3.1 illustrates how using a pair of transistors can achieve the

desired response. Here a PNP transistor is used to source current to the input line while an NPN transistor is used to sink current. The values of V_i, V_f and $1/40T_e$ are constant and are set by an external circuit. Furthermore, V_b is a constant voltage used to negate inherent differences between the transistors (such as different Is values) and V_p represents the variable drive voltage being applied to this simulated Langmuir probe. Incorporating these bias levels indicated into the Ebers-Moll equation results in the following net current to the input line:

$$I_p = I_s^{npn}\, e^{(\alpha^{npn}\{V_i + V_b + (V_p - V_f)/(40T_e)\})} - I_s^{pnp}\, e^{(\alpha^{pnp} V_i)}, \tag{3.2}$$

Here, the NPN and PNP superscripts call out the potential different temperatures and saturation currents of the two transistors. This equation reduces to a form very similar to equation 2.9,

$$I_p = I_{sat0}\left(I_{sat}/I_{sat0}\right)^{(\alpha^{npn}/\alpha^{pnp})} e^{(\alpha^{npn}\{(V_p - V_f)/(40T_e)\})} - I_{sat}, \tag{3.3}$$

when

$$V_i = \ln[I_{sat}/I_s^{pnp}]/\alpha^{pnp}, \tag{3.4}$$

and

$$V_b = (1/\alpha^{npn} - 1/\alpha^{pnp})\ln[I_{sat0}] + \ln[I_s^{pnp}]/\alpha^{pnp} - \ln[I_s^{npn}]/\alpha^{npn} \tag{3.5}$$[3]

Notice that when the temperatures of the NPN and PNP transistors are both at room temperature (i.e. $\alpha^{npn} = \alpha^{pnp} = 40$ volts^{-1}), equation 3.3 reduces to equation 2.9 and this transistor pair is set up to mimic the magnetized Langmuir probe response. Because of the temperature assumption being made here, the transistors should be placed in close proximity to each other to minimize any differences. Although such layout considerations will be made, the current error created by a temperature mismatch is at worse case approximately 1.6% of Isat per 1°C difference [9] and thus will be ignored during later calculations.

A close inspection of equations 3.3 – 3.5 indicates the roles that the three principle constants (V_i, V_f and $1/40T_e$) have in mimicking a Langmuir probe response. V_i controls the ion saturation

[3] Equations 3.1 – 3.5 are all obtained from Dr. LaBombard's MLP concept paper. A more detailed analysis of the theory referenced here is also available in said paper [9].

level, which dominates at low bias levels, Vf corresponds to the floating potential and $1/40T_e$ to the shape of the exponential response at positive bias levels. The final constant, V_b, is set to ensure that the output current is zero when the bias is at Vf, which may not otherwise be the case due to intrinsic temperature or saturation current differences between the transistors.

3.3 –Mirror Langmuir Probe System Concept

Since the transistor pair and bias arrangement of Figure 3.1 is set-up to yield an I-V characteristic that looks like a Langmuir probe, it can be used as a "Mirror Langmuir Probe" (MLP). When exposed to the same bias signal being applied to a real Langmuir probe, the MLP will generate the same current response as the real probe when its input parameters (V_i, V_f and $1/40T_e$) directly correspond to the parameters of the plasma. Thus, when the MLP is precisely "mirroring" the real probe, the three parameters being sent to the transistors to generate the correct response can also be directly outputted, which provides a real-time measurement of the plasma parameters. These parameters are rapidly changing in the plasma, however, thus the circuitry that sets these values must be able to update on time scales comparable to that of the fluctuations. In order to track these fluctuations, a highly optimized feedback system is built around the MLP transistors, which is shown as a block diagram in Figure 3.2.

The system begins with a high frequency bias waveform that takes a different form than previous Langmuir probe systems. Instead of a constantly oscillating probe bias, this waveform is generated in three steps, each of which corresponds to one of the three regions on the I-V characteristic. The bias rapidly moves from the positive state (electron collection) to the floating state and then to the negative state (ion saturation) and then repeats. However, once it reaches a certain state it remains a constant level for a designated period. The need for such a waveform will be clear when the method for updating each parameter is discussed. It should be noted that the waveform needs to complete a cycle in under a microsecond to ensure that all plasma fluctuations can be properly observed. Furthermore, the bias level between the positive and negative stages are optimally set to +.64W and -2.4W respectively, where W is a function of T_e. This ratio is needed to cover the optimal bias range for a given plasma ($\sim 3T_e$) while making the

electron current collected during the positive bias phase approximately equal to the ion current collected during the negative bias phase [9].

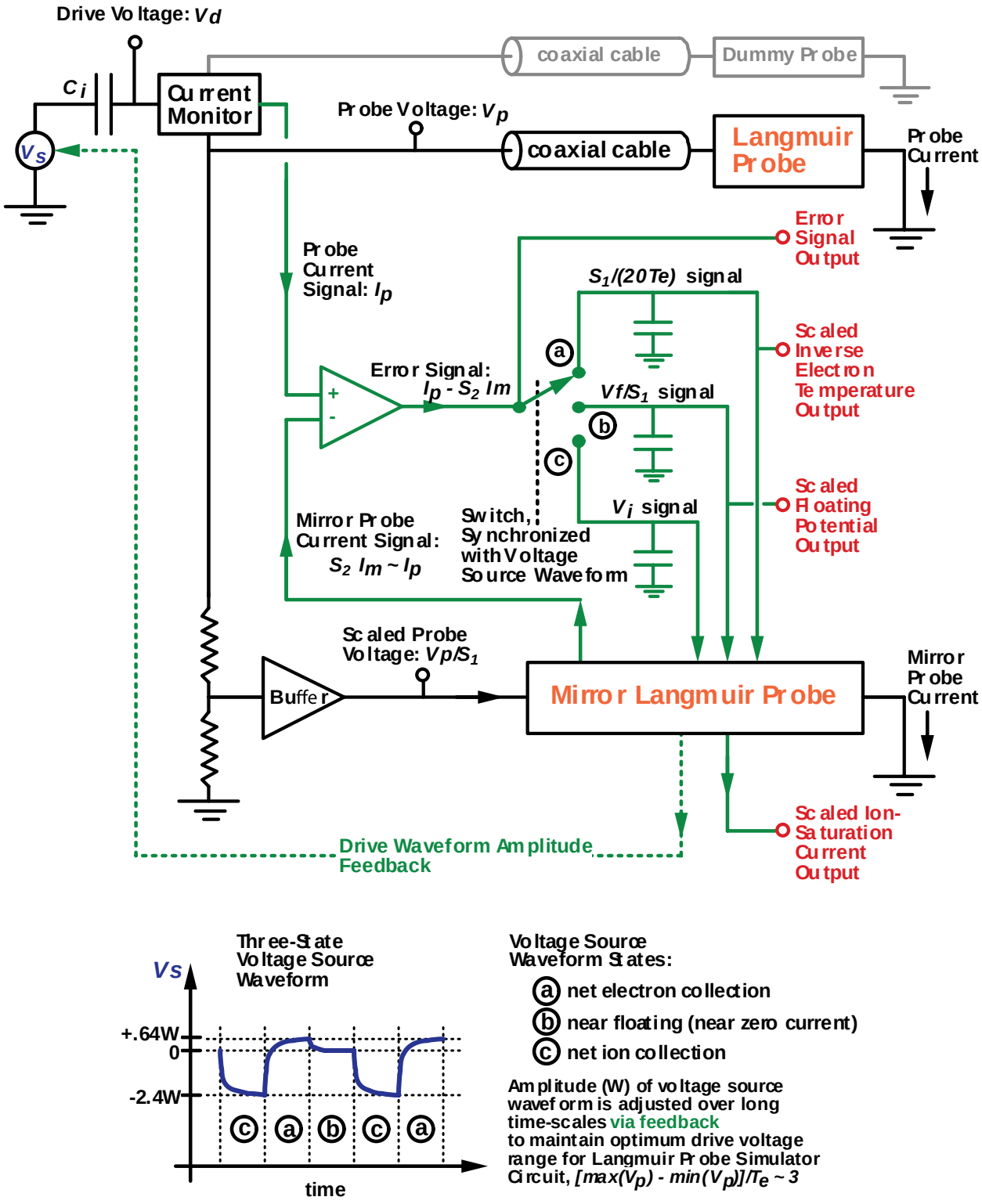


Figure 3.2 – MLP System Concept [9]

This bias waveform is then applied to the Langmuir probe and both the bias and corresponding current signals from the probe are recorded by the MLP system. To properly measure the current from the Langmuir probe, a "dummy probe" is utilized to nullify the transmission line effects of coax cable on the current signal. The RF transistors that form the MLP system can not handle the bias or current levels typical of a real Langmuir probe. Therefore, the system works with scaled down versions of these quantities. The scaled down bias signal (V_p) is then combined with the most current stored values for V_i, V_f and $1/40T_e$ and is applied to the transistors in a way that corresponds to Equation 3.3. The output or "mirror" current signal is scaled back to an appropriate level where it is compared to the current reading from the real Langmuir probe. If the two signals are different, an error signal is generated to indicate that one of the parameters has to be adjusted. Which parameter is adjusted, however, depends on what stage the bias signal is currently in. If it is in the negative bias state, then the error signal corresponds to the V_i parameter and it is adjusted accordingly. This adjustment is accomplished through the use of integrators which try and reduce the error signal to zero. The V_i parameter is only allowed to update during the positive bias state and simply holds its value during the other bias waveform states. The same process is used for the other parameters during their respective bias waveform states. By choosing the integrator switches to be on only during the flat portions of the bias waveform, current measurement errors associated with finite pulse propagation time in the coaxial cables, unbalanced probe capacitance, as well as finite settling times of the electronics are avoided. The speed of this entire process is set by the bias waveform and thus is of the order of 1 MHz.

The above description outlines a system that is capable of outputting the plasma parameters of interest in real-time while operating at the 1 MHz level and utilizing a single Langmuir probe. Thus, the primary goals of the next generation Langmuir probe system are within reach according to the MLP system theory. Designing the actual circuit components that will turn this theory into reality was the main purpose of this thesis. The steps involved and results achieved in constructing the first MLP system are covered in Chapter 4.

Chapter 4 – Mirror Langmuir Probe System Design

4.1. - System Overview

The following four modules make up the principle components of what has become the first fully functional MLP system. An additional circuit, the Electronic Langmuir Probe, used for testing purposes is mentioned here, but is not a part of the main system and is discussed in Chapter 5. A block diagram that shows how these components connect with each other and the external world is shown in Figure 4.1.[4]

1. 'TTL Waveform Generator' – This unit functions as the 'master clock' of the MLP system and provides timing signals to both the FET and Data boards. The TTL signals generated here not only control the state switching of the bias waveform, but also dictate the timing of the integrator circuits on the Data board. Details of this board's design and construction are contained in section 4.2.
2. 'FET Drive Board' – This circuit utilizes high-frequency switching MOSFETs to generate a three-state voltage bias waveform with a maximum range of -240 to +120V and output current of ~2A. The amplitude of the bias waveform is adjustable in real-time and utilizes two signals from the Data board (Isat and normalized bias) to set the ideal bias level for the current plasma conditions. This circuit applies the bias signal to the probe in a capacitively coupled manner to ensure that the output floats at V_f when no bias is applied. The output coupling capacitance is also changed dynamically in response to the Isat signal. Details of this board's design and construction are contained in section 4.3.
3. 'MLP Data Board' – This circuit monitors the voltage and current on the real Langmuir probe and dynamically adjusts the three input parameters to its MLP transistors to attain a match between the two. This board outputs the real-time plasma parameters of ion saturation, floating potential and inverse electron temperature, while also generating the bias control signals utilized by the FET board. Details of this board's design and construction are contained in section 4.4.

[4] Although the system has been designed to accommodate several pairs of FET and Data boards, discussion from this point on will assume that only one pair is present unless specified otherwise.

4. Compact PCI Data System and Associated Linux Server – These systems record the signals from the Data board. The analog signals can be digitized at either 50 MHz (maximum of 8 channels) or 10 MHz (maximum of 32 channels).
5. 'Electronic Langmuir Probe' – This circuit is used to simulate a Langmuir probe immersed in a magnetically confined plasma. It is used to test the MLP system in place of a real Langmuir probe. This circuit utilizes TTL signals to rapidly switch between preset values for each of the three plasma parameters, which allows for dynamic response testing of the MLP system in a controlled environment. Details of this board's design, implementation and test results are contained in Chapter 5.

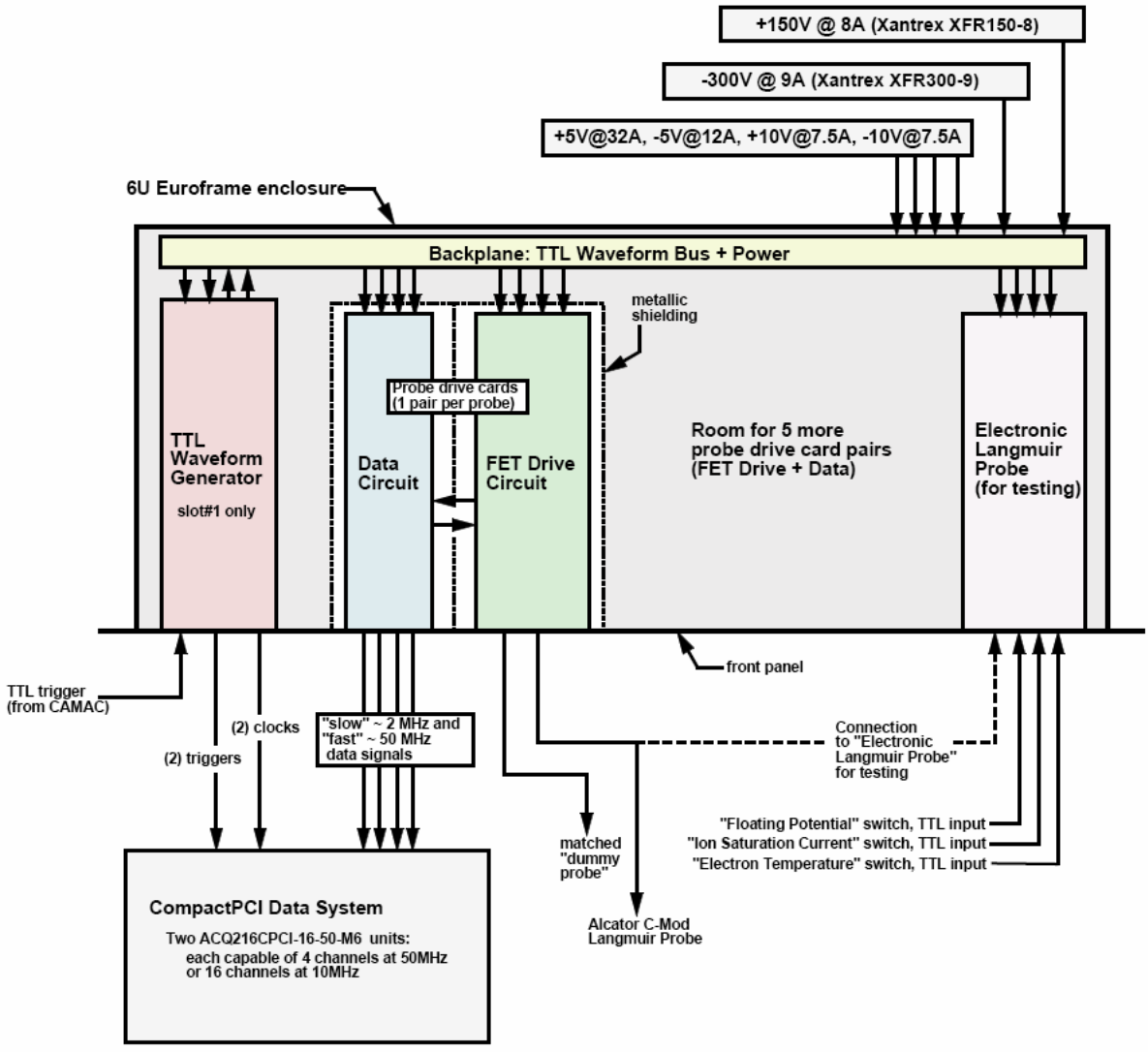


Figure 4.1 – MLP System Block Diagram

The overall MLP system is housed in a steel chassis and is made up of five sections. The top section is a custom built Eurorack with backplane connectors for the various MLP circuit boards. Next are the low voltage, DC power supplies from Acopian [19] that provide +10V at 7.5A, -10V at 7.5A, +5V at 32A and -5V at 12A (all supplies have less than 0.25mV RMS ripple) to the boards. The third section consists of two ACQ216CPCI 16 channel 50 MSPS Simultaneous Digitizers from D-TACQ Solutions, Ltd [20]. Below the digitizers is the Linux server which manages the digitizers and allows for remote use. The final section is made up of high voltage, DC power supplies from Xantrex [21] which provide +150V at 8A (Model # XFR150-8) and -300V at 9A (Model # XFR300-9) to the FET Driver Board.

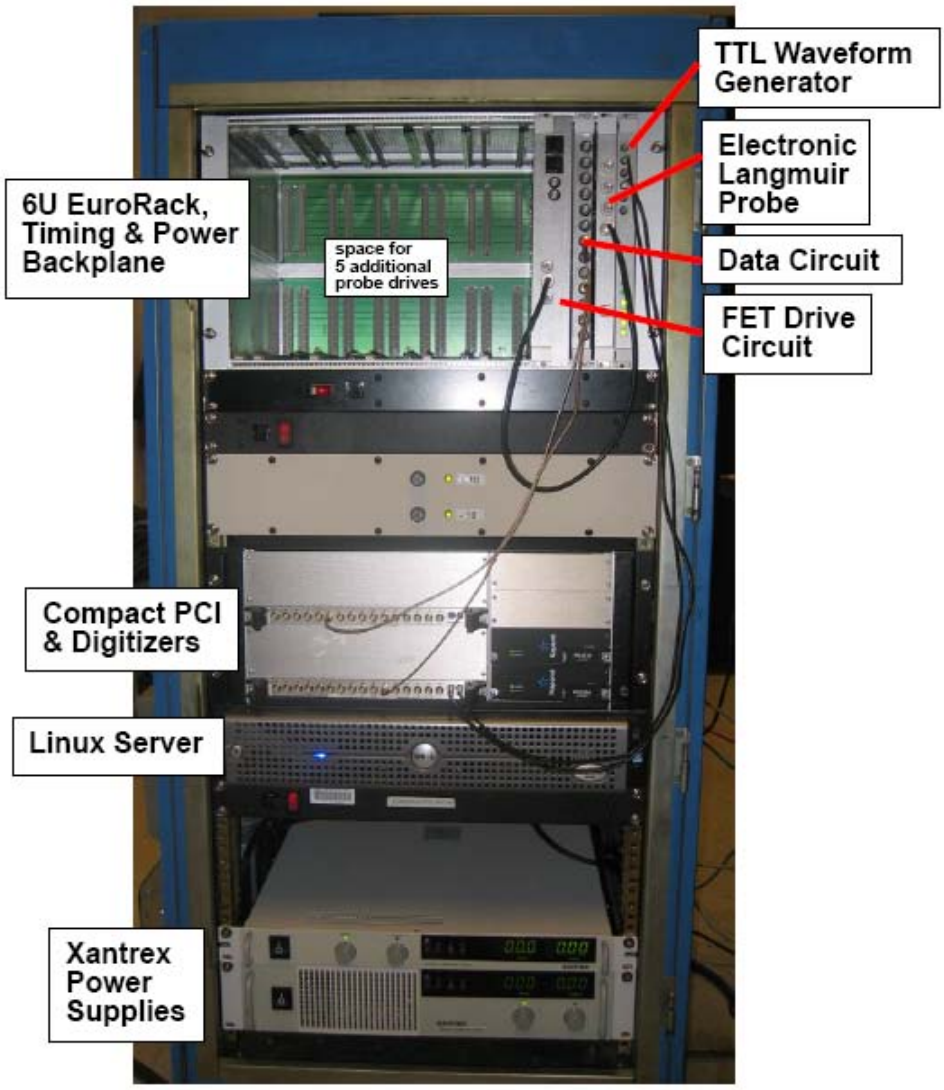


Figure 4.2 – MLP Rack Assembly

Connections among these five sections can be broken down into two areas: power and data. The power connections between the high and low voltage supplies and the Eurorack are done through the back of the Eurorack. #14 AWG wires are used connect to the backplane, where it is distributed to each of circuit boards in the rack. Furthermore, power supply sense leads are also attached to the backplane to compensate for voltage drop along the power supply wires.

Data signals move between the circuit board rack and the digitizers through 50Ω SMA wires on the front of the chassis. The primary data signals are outputs from the MLP Data board and contain measurements of the ion saturation, floating potential and electron temperature as well as the corresponding error signals that indicate the validity of the calculated parameters. The other data signals of importance involve the sharing of trigger and clock information from the TTL Waveform board to the digitizers, which is done with LEMO connectors and 50 Ω coax. Also, the connection of the FET Driver board to the Langmuir Probe is made via a BNC connector and 50Ω coax cable on the front of the FET board. Finally, data from the digitizers is transferred to the Linux server via a gigabit Ethernet router and the Linux server is likewise connected to the local network via gigabit Ethernet.

4.1.1 – Circuit Board Design and Fabrication

The bulk of the effort in this thesis project was centered on designing, constructing and testing the set of high-performance, custom-made boards described above. This effort followed the same procedure for each circuit and development of each was done in parallel. The initial work done on this project was in the form of computer simulation using the OrCAD Capture and PSpice PCB design package from Cadence [22]. Once initial simulations demonstrated that the MLP concept was feasible, the requirements for each circuit were set and the design effort changed from testing general concepts to optimizing specific functions. Ideal PSpice parameters were replaced with specific device models in an effort to study the actual behavior of as many components as possible. If PSpice parameters did not exist for certain components, prototypes were bread-boarded to ensure that no device was only investigated using its ideal model.

When the final form of each circuit had been completed in Capture, another program in the OrCAD suite called Layout was used to generate the manufacturing files that are used to build

the physical board [22]. In the following sections, special Layout considerations for each board are highlighted, but some general items will be mentioned here. The TTL and FET Drive boards consist of four layers and contain a mix of through-hole and surface mount-components. Both of these boards were built by PCB Express [23] and are the same height, width and thickness. The MLP Data board, however, consists of 6 layers and almost exclusively contains surface-mount components. This board is the same height and width as the others, but is thicker to accommodate the additional layers. Due to the special manufacturing requirements of this board, the more advanced capabilities of Circuit Board Express, Inc [24] were used. An inventory of all the components used in these circuits was created at the PSFC and the boards were loaded with components using in-house capabilities.

4.1.2 - Board Interconnects

The most important data signal connections are made inside the Eurorack. The first group of these signals is the TTL signals that go to the MLP Data and FET Driver boards from the TTL waveform generator. These signals are generated from the TTL Waveform Generator and put on the backplane of the Eurorack. Thus, every pair of FET and MLP Data boards that are plugged into the Eurorack receives these signals when they are generated.

The second group of these signals deals with the data the must travel between a given pair of FET Driver and MLP Data boards. The voltage and current signals from the Langmuir Probe are transferred from the FET board to the Data Board so that the MLP transistors obtain the proper bias and current signals. The Data board in turn reports the level of Isat and normalized bias amplitude back to the FET board so that the bias can be adjusted accordingly. These connections are all made with short 50 Ω coax cables connected through SMB connectors.

4.1.3 - Board Overview

As mentioned above, the heart of the MLP circuitry consists of three primary components; the TTL Waveform Generator, the FET Drive and MLP Data circuit boards. An optional fourth component is made up of the Electronic Langmuir Probe circuit board which is used for testing and diagnosis purposes. This three-component system accommodates a single Langmuir probe, but it can be expanded to work with up to 6 probes in a one rack system. For each additional probe added to the system, an additional FET Drive and MLP Data board must be inserted into

the rack (and paired together). The limitation on expandability comes from the rack being unable to accommodate more FET/Data board pairs. The single TTL Waveform Generator board provides the same switching signals to each FET/MLP Data board pair and thus does not need to be expanded as more pairs are added to a given rack.

4.2 - TTL Waveform Generator

The TTL Waveform Generator has three primary functions. The first primary function is to provide visual confirmation that power is being supplied to the backplane of the Eurorack. The second function is to generate the TTL switching signals that control the FET and MLP Data boards. The final function is to provide a clock and trigger signal(s) to the digitizer. The actual implementation of these functions is covered in the section below.[5]

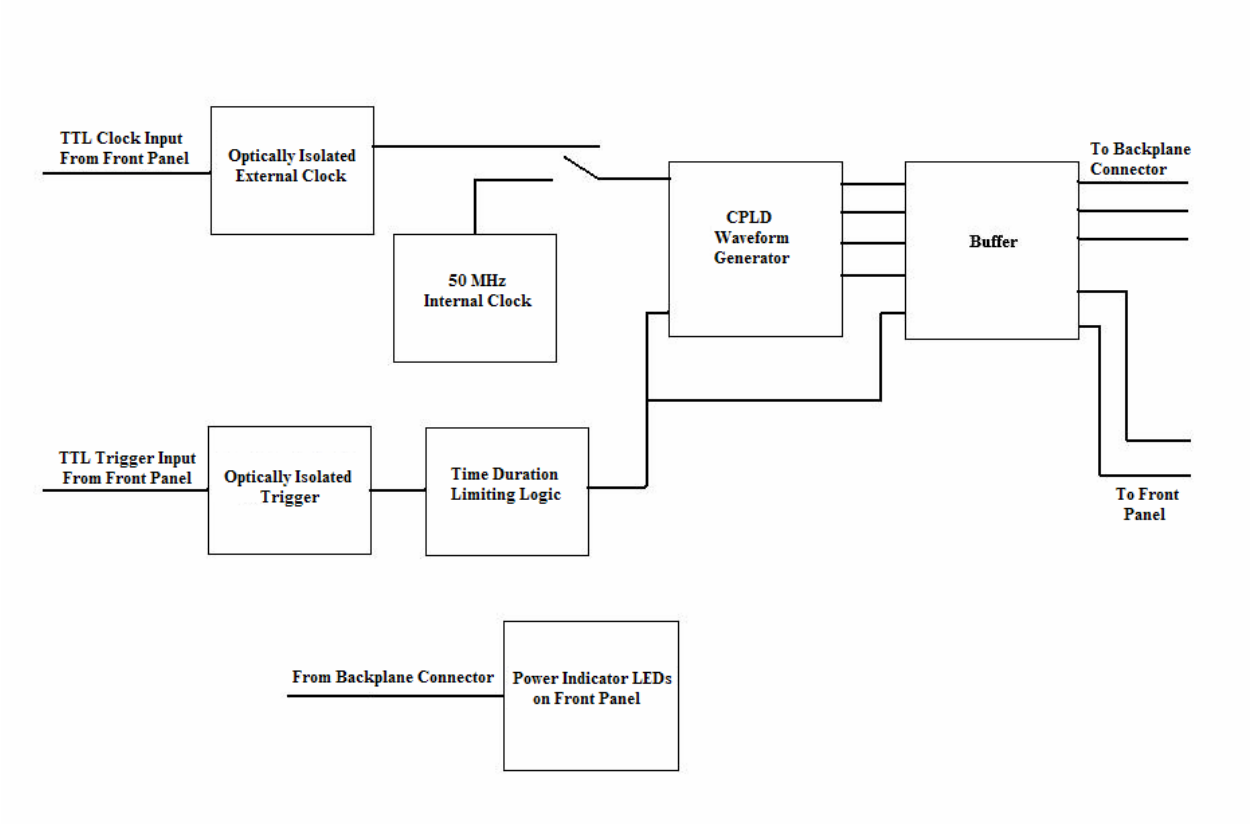


Figure 4.3 – TTL Waveform Generator Functional Block Diagram

[5] A complete schematic of the TTL Waveform Generator circuit can be found in Appendix A.

4.2.1 – TTL Waveform Generator Subsection Detail

The heart of the TTL generation comes from the high-speed programmable logic device used in this design; the ATF750C chip (U5) [25]. The TTL signals generated by this chip are fully customizable and can be reconfigured using a PC programming module and associated software. After the desired waveform has been programmed into the chip, it only requires two inputs to generate the voltage waveforms; a trigger signal to turn the chip on and a clock signal to set the pace. The trigger comes from the C-Mod data system and indicates that a plasma is about to be generated and that the MLP system should begin to record data. Since this signal is coming from an outside source, it can be subject to errors beyond our control. Thus, several fail-safes have been built into this circuit board. The first feature is a HCPL-2430 optical isolator, which is shown as U15 in Figure 4.4 [26]. This chip provides a clean signal to our digital logic circuitry in the event that the input signal is noisy. The second and more important feature is to isolate the ground on the shield of the LEMO connector, which eliminates a ground loop.

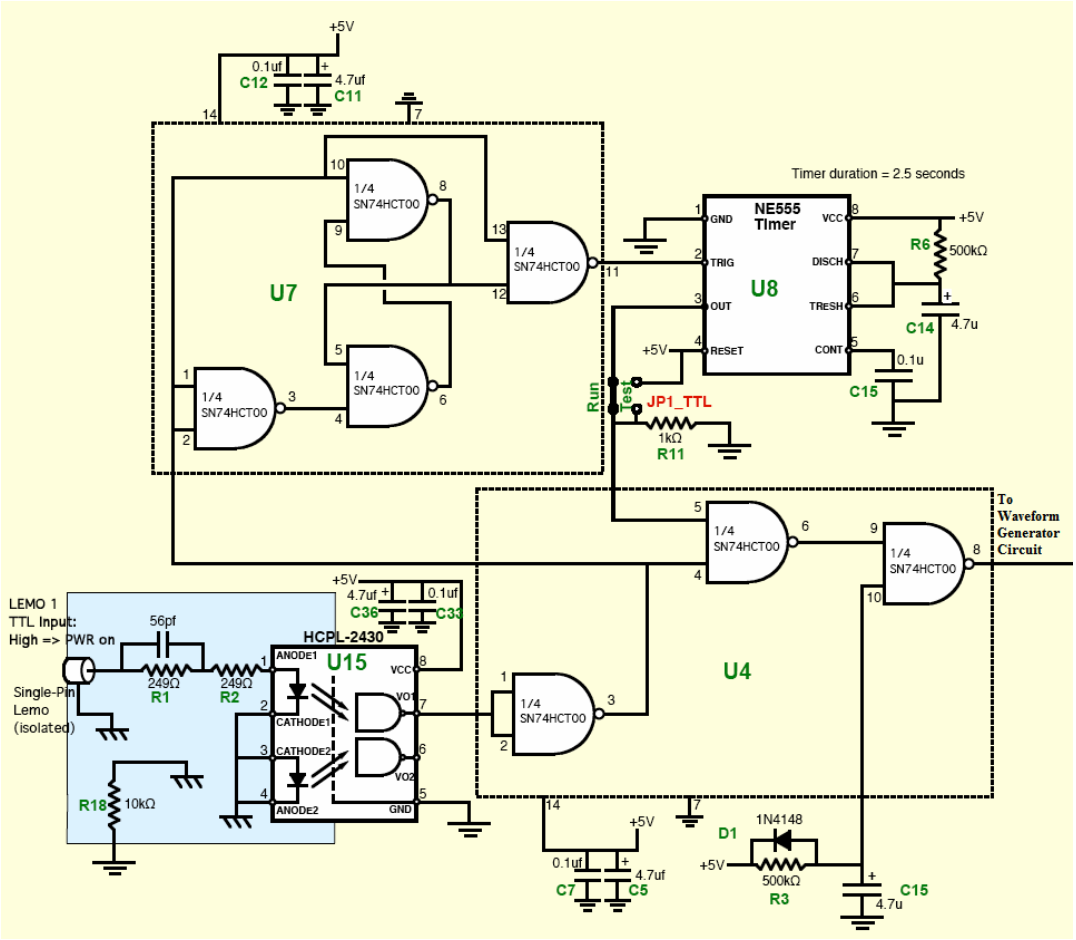


Figure 4.4 – Trigger and Time Duration Limit Circuit

The second fail-safe deals with the length of time that the trigger is applied to our system. The MLP system has been optimized to run for periods of time that are comparable with the duration of a plasma inside of C-Mod, which is usually less than 2 seconds. The high-power switching of the FET Driver board causes components to heat rapidly and could result in component failure if the system was allowed to run for an extended period of time. Since the entire MLP system is active while this trigger is high, a trigger that remains high for a longer period of time than desired could be a problem. Thus, the digital flip-flop composed from U4 combined with U7 and U8 ensures that no matter how long the external trigger remains high, the signal that actually reaches the TTL generator chip (U5 in Figure 4.6) only lasts for a maximum of 2.5 seconds. For testing purposes, this system can be bypassed by moving the JP1_TTL jumper into the "Test" position, which results in the system running for as long as the trigger is high.

Once the trigger signal is outputted from our time-limiting digital logic, it proceeds to the input pin of the high-speed programmable logic device. This signal is also sent through jumper JP2_TTL, to a buffer chip (U6 in Figure 4.6) and is put on the backplane. This signal is needed by the FET and MLP Data boards to know whether the system is active or not, which will be described later. This signal is also sent to a resistor-LED combination (R4 & D2 in Figure 4.4) similar to the low voltage power supplies at the front panel to provide visual confirmation of an active trigger signal.

The other input of U5 is the clock signal that dictates how rapidly the chip will generate its programmed waveforms. Primarily, this signal comes from U1, which is a 50 MHz oscillator and enables U5 to complete an iteration of its waveform in under a microsecond. The jumper JP3_TTL, however, provides the option of having direct control of the speed of U5 through an optically isolated external clock. This signal is isolated for the same reasons as the trigger signal. The HCPL-9000 [26] chip used to isolate the signal, however, requires an isolated +5V power supply, which is provided by a NME0515S DC-DC converter (U11) [27] and a LM78M05CT voltage regulator (U14) [28] (see Figure 4.5). This external clock is used primarily for testing purposes so that the entire MLP system can be slowed down for troubleshooting and analysis.

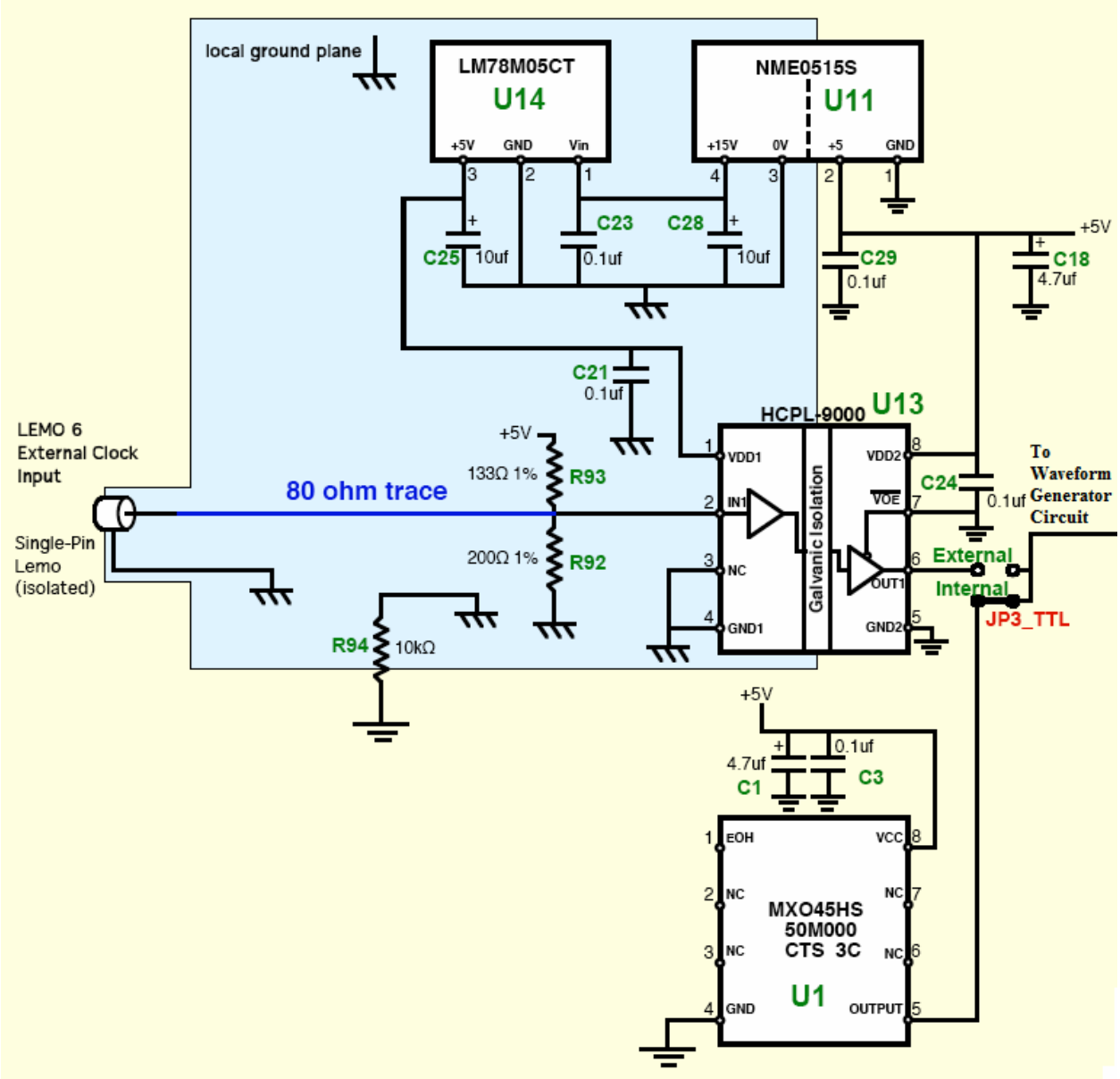


Figure 4.5 – Internal and External Clock Circuit

The ATF750C has been programmed to output 10 signals, which can be grouped into three categories; FET switching signals, MLP Data switching signals and clock/trigger outputs. There are three FET switching signals (pins 21-23) each of which controls one of the three bias states (ion saturation, floating potential and electron temperature) described earlier. There are likewise three MLP Data switching signals, which control the integrators that correspond to each bias state. There is a delay of several clock signals between the FET and MLP Data signal for a given

bias state. This is done to allow time for the voltage and current signals from the Langmuir Probe to settle after undergoing one of the rapid bias changes. The final four signals are reserved for generating two clock and two trigger signals that can be sent to the two digitizers. All signals from U5 are sent to fast-switching NAND gates (U2, U6, U9 in Figure 4.6), which act as buffers that can drive the signals across the backplane or through a LEMO connector in the case of the clock/trigger signals. It should also be mentioned that 133Ω pull up and 200Ω pull down bus termination resistors have been built into the backplane for each of the FET and MLP Data signal lines. These resistors match the impedance of the backplane circuit board traces (80Ω) and reduce the TTL voltage to the range of 0-3V, resulting in a fast, clean TTL pulse on the backplane.

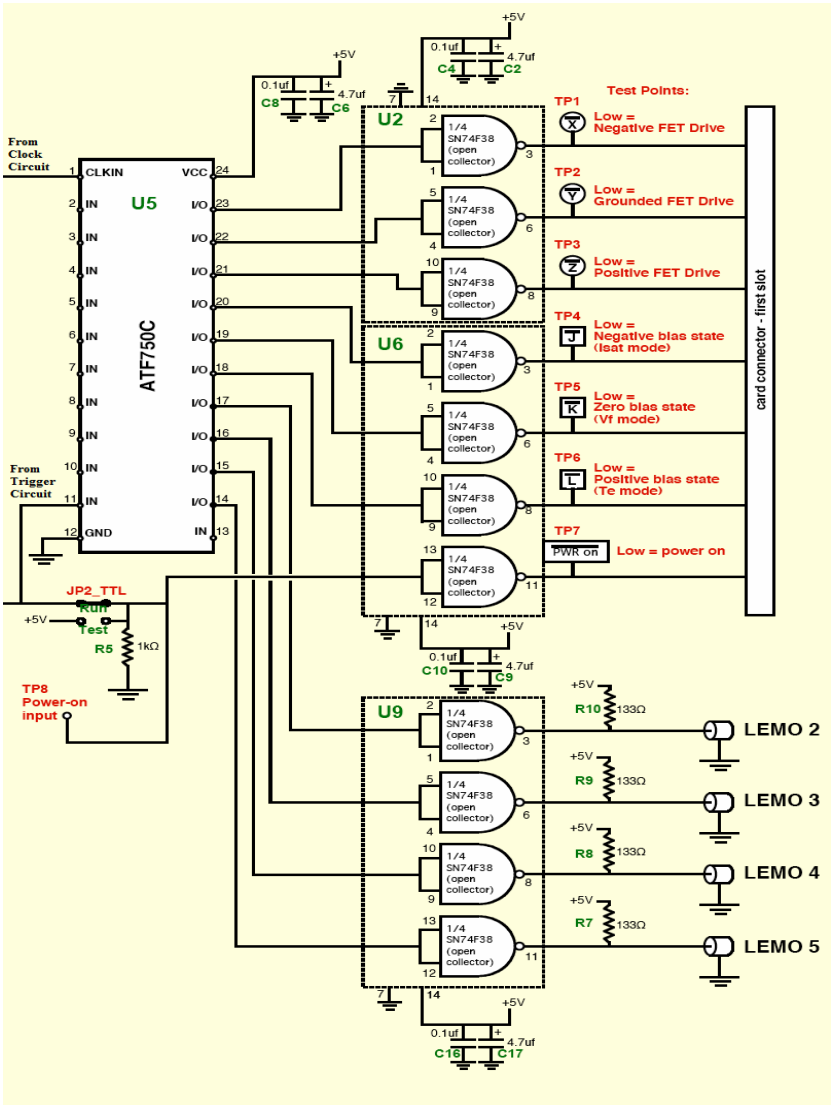


Figure 4.6 – Waveform Generator Circuit

Visual evidence of power on the backplane is provided by six red LEDs on the front panel of the circuit board, each of which corresponds to one of the six power supplies. For the +10V, -10V, +5V and -5V power indicators, a specific resistor is placed in series with each LED so that when the voltage reaches the correct level, the LED will conduct. For the higher voltage supplies, op-amps are used as comparators to indicate the status of the supplies. These comparators are set to turn on the LEDs when the power supplies reach +50V and -50V respectively.

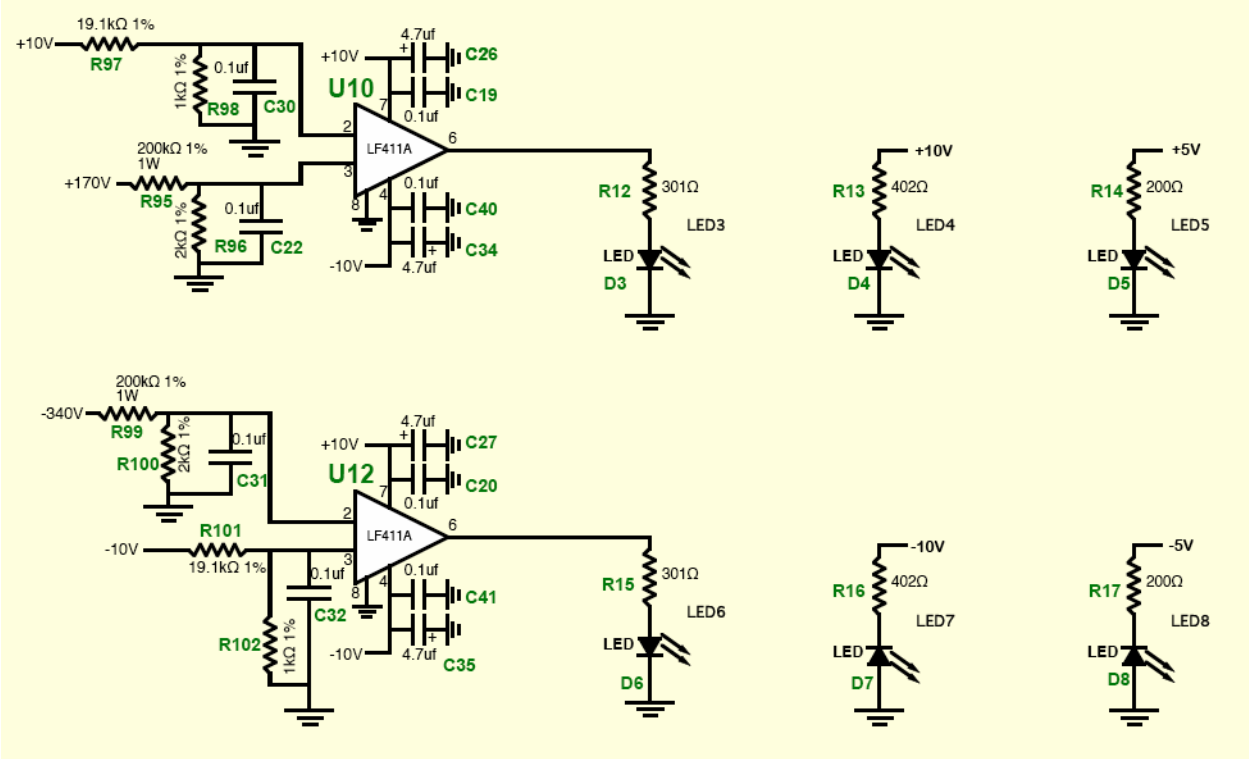


Figure 4.7 – Power Indicator Circuit

4.2.2 - TTL Layout & Optimization

The only area of consideration for layout on this board was with minimizing the lengths of traces that carry high frequency signals and the isolation of the external clock and trigger signals. Since the important high frequency signals were the ones being sent to the backplane, the signal generating components were all placed close to the backplane connector. The power indicator components, however, were placed near the front panel more for convenience than for performance. The board itself is made up of four layers where the signal traces were on the top

and bottom layer, a solid ground plane was on the second layer (or first inner layer) and power traces were on the third layer (second inner layer). The trace thicknesses were sized to yield an 80Ω characteristic impedance (.012" width, .020" layer spacing) for the external clock and trigger inputs.

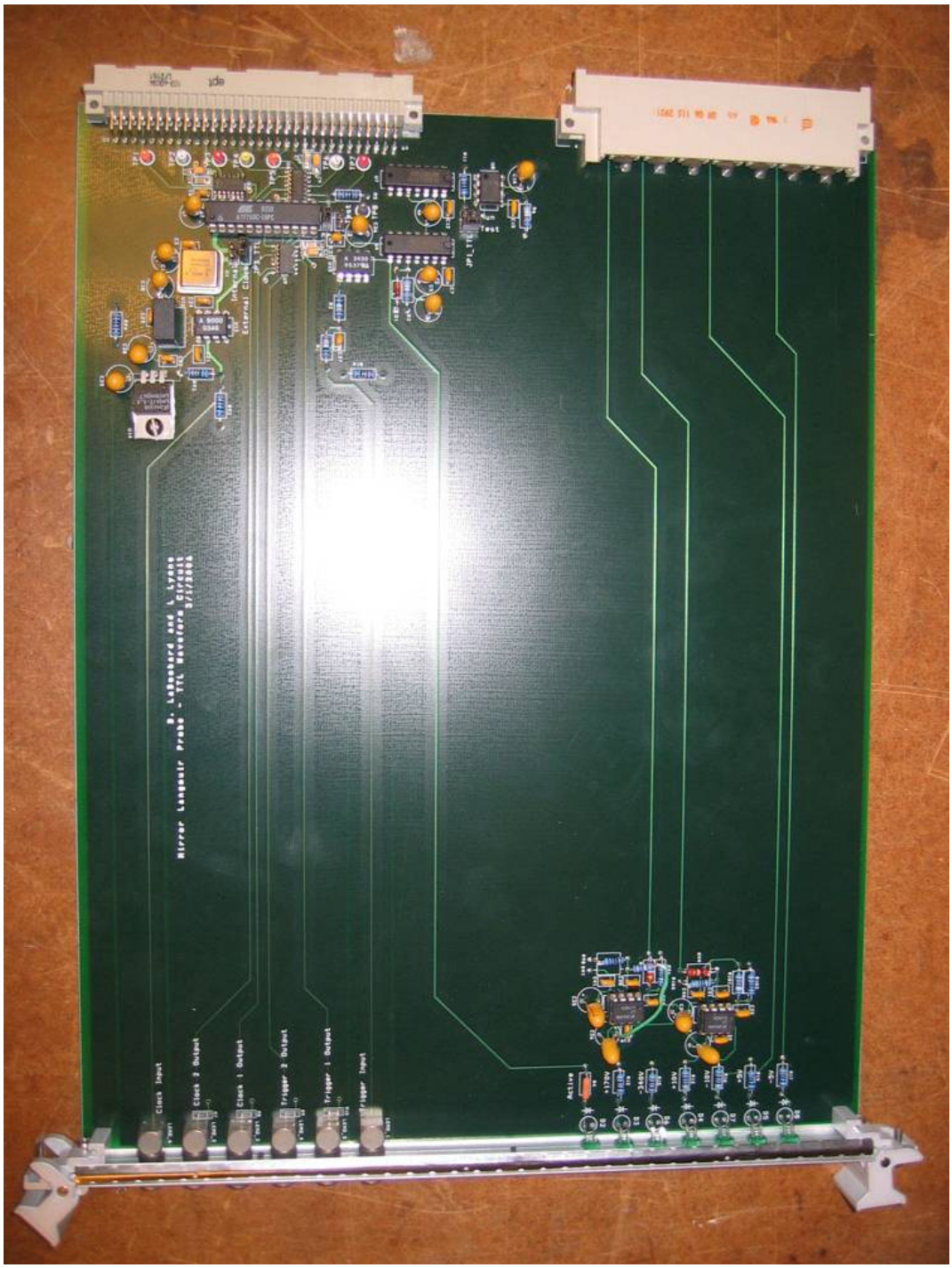


Figure 4.8 – TTL Waveform Generator Layout

4.2.3 - TTL Performance

The only testing necessary on this board was to visually confirm the power indicator LEDs and to evaluate the waveforms being generated on the backplane. As discussed above the primary signals consist of the three FET switching signals and the corresponding MLP Data board switching signals. Figure 4.9 shows that the overall period of all waveforms is 900 ns, which is generated using a 50 MHz clock. This period means that all three MLP Data parameters are updated once every 900 ns, which is below the targeted update time of 1 µs. All TTL pulses are clean, exhibiting rise and fall times under 20 ns.

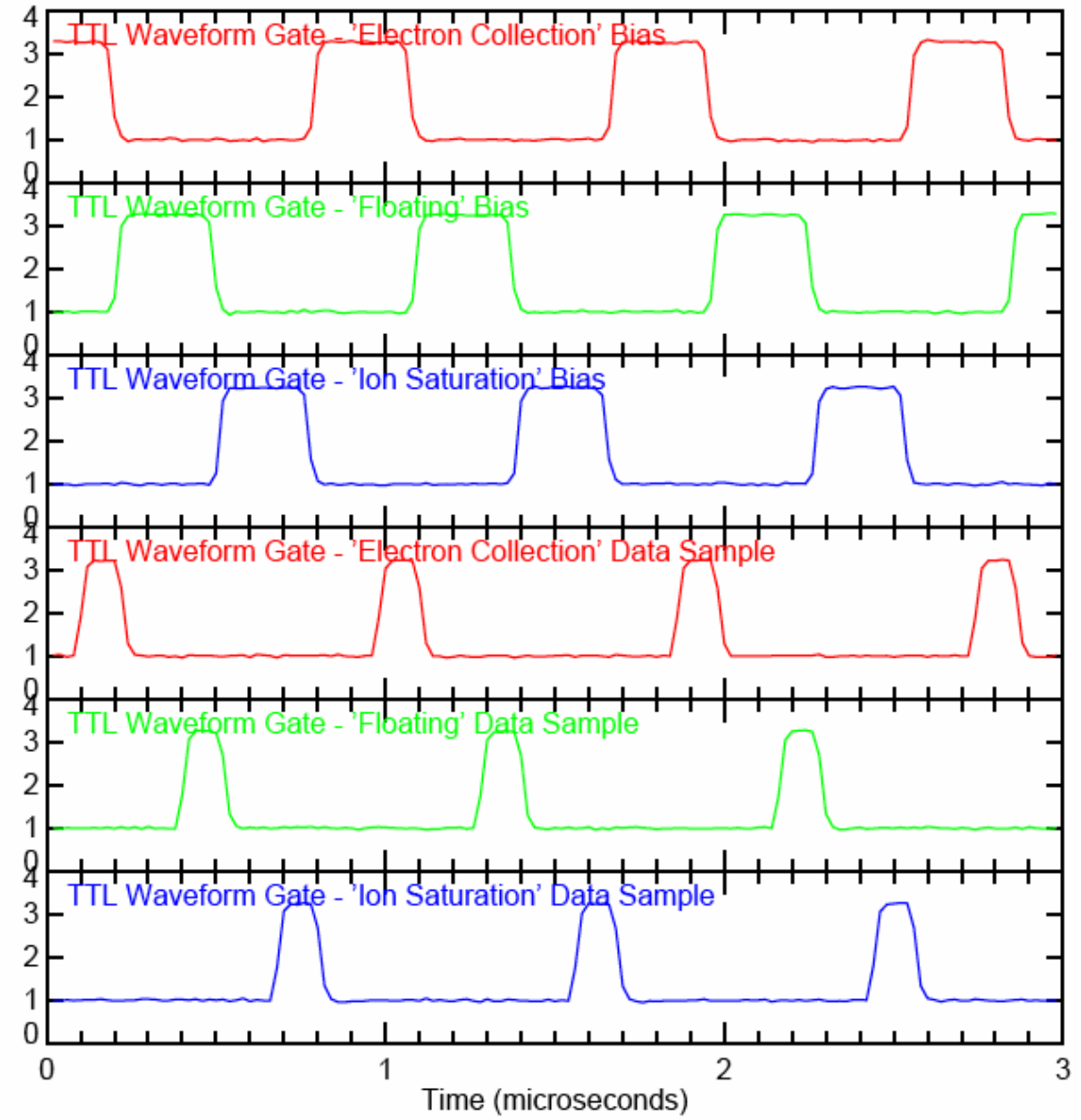


Figure 4.9 – TTL Waveform Generator Signal Output

As mentioned above, each MLP Data board switching signal should occur some time during its corresponding FET signal. A glance at this figure shows that the MLP Data signals are adjusted to be much shorter than their FET counterparts and occur during the end of the FET signal. This is an important feature which is used to avoid noise that is generated during the switching and settling time periods of the FET voltage waveforms. When the FET TTL signal goes high, there is a 150 ns delay associated with the FET fully closing and the waveform changing states. Additionally, when the waveform is changing states, a substantial spike in current persists after the waveform has reached its value. Thus, additional delay in the activation of the MLP Data integrators must be added to allow the current to settle out to its true value. Under closer examination, it can be observed that the MLP signals actually remain high after the FET signals have gone low. This was done in response to bench testing that showed the voltage waveform was delayed by 40 ns between when the TTL signal went low and when it actually started to change its voltage level. This delay meant that there was more time available during which voltage and current levels are stable enough for the MLP Data circuit to operate. Through additional bench testing of the system, the near optimal waveform timing, shown in Figure 4.9, was obtained.

4.3 - FET Drive Board

The primary function of the FET Driver board is to create a three-state waveform that is capable of operating with a frequency of at least 1 MHz and over a voltage range of +120V and -250V (as discussed in section 3.3). Secondary (but still critical) functions of this board include the ability to self-adjust the bias and to add or subtract output coupling capacitance in response to signals from the MLP Data board. These three functions will allow the FET Driver board to optimize its waveform to the plasma conditions being applied to the Langmuir probe at that point in time. The actual implementation of how these functions are obtained is covered in the section below.[6]

[6] A complete schematic of the FET Drive circuit can be found in Appendix A.

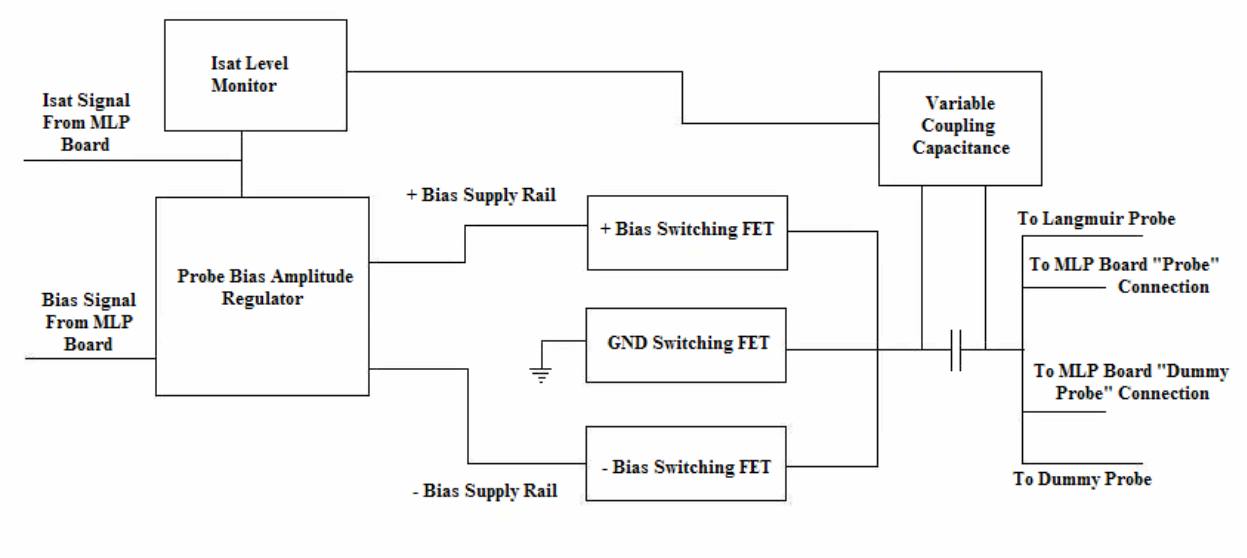


Figure 4.10 – FET Drive Functional Block Diagram

4.3.1 – FET Drive Subsection Detail

The three-state waveform is created by using three high-power, megahertz switching IXFH12N50F MOSFETs (Q3, Q5 & Q4 in Figure 4.11) [29]. Each of these FETs connects the output line to the positive voltage rail, negative voltage rail and ground respectively. As a FET has voltage applied to its gate, it allows current to pass through its drain and source. Thus, depending on which FET is conducting, the output line is connected to one of the three voltage states above. Due to this set up, it is important that only one FET be in conduction at any one time because if two or more were in conduction then the power supply rails will be shorted to ground or each other. Therefore, it is imperative that the three TTL signals (X, Y & Z) that control the gates of each FET are never high at the same time. Also, a UG8JT fast reverse-recovery diode [30] is used to keep the "grounding FET" from conducting current during negative output voltages. Thus, the "grounding FET" must be programmed to fire after the "positive bias FET".

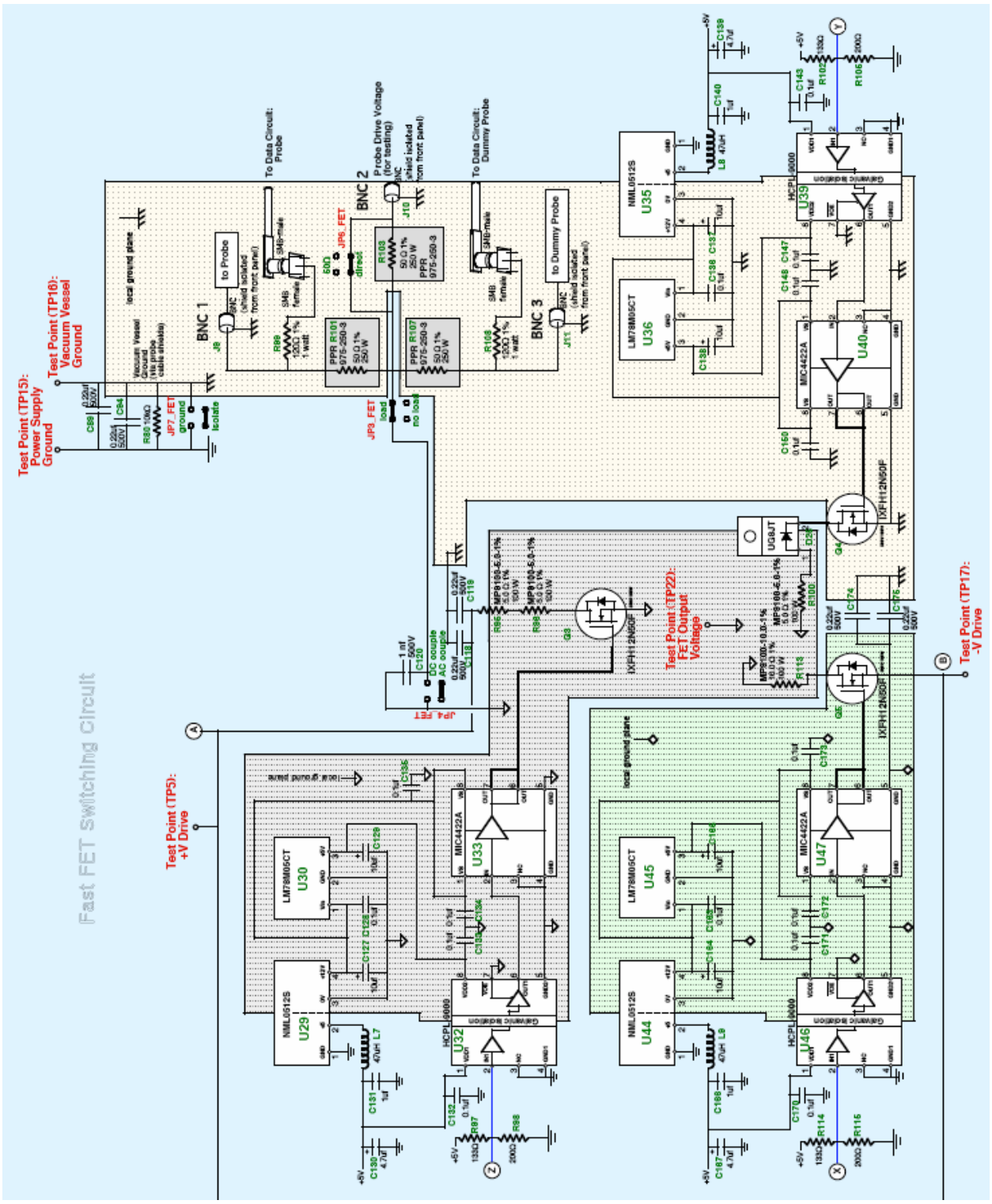


Figure 4.11 – FET Switching Output Circuit

An important aspect to each FET is the manner in which the TTL signal is applied to its gate. Since the gate signal must be with respect to the source of each FET, the TTL signals coming from the backplane can not be directly applied to their respective gates. To solve this issue, a circuit similar to the one used to isolate the external clock on the TTL board is implemented here. The TTL signals are optically isolated using the same HCPL-9000 chips and an isolated ground plane is created for each FET. The source of each FET is then connected to the isolated ground plane of its respective TTL signal. This set up allows the TTL signals to be isolated from the high voltages associated with the FETs while still being able to control their gates. Note that the optically isolated TTL signals do not directly control the FET gates, but rather control the MIC4422A MOSFET drivers [31] which are connected to the gates. Bench tests showed that there is a ~25 ns time delay between a rising TTL edge and the trigger of the MOSFET. A longer delay of ~40 ns was observed between the falling TTL edge and MOSFET turnoff.

Special consideration was paid to the output interface from the FET board. Simply connecting the output line directly to a coax cable that runs to the Langmuir probe would cause reflections from an unmatched transmission line and in turn adversely affect the generated voltage waveform. To eliminate these reflections, a high wattage, thin film PPR-975-250-3 50Ω resistor [32] is put in series with the output line. Thus, any reflections that emanate from impedance mismatches at the Langmuir probe are absorbed by the 50Ω resistor. In addition, a coax cable is attached to the dummy probe side of the output (which also has a 50Ω resistor) that has the same length that runs to the real Langmuir probe. Remaining reflections and loading effects of each coax cable will tend to be similar. Since the MLP Data board deduces the current by comparing the voltage on the "probe" and "dummy probe" taps, this method can be used to null-out the current under no-plasma conditions.

If controlling the bias amplitude of this three stage waveform was not a goal of this project, connecting the high voltage power supplies to the power rails of the above stage and would complete this circuit. However, since the MLP system must dynamically adjust the bias voltage in response to plasma parameters, the power rails must be able to change in real-time. Controlling the power rails is achieved primarily through the use of STP5NB40 [33] and FQP4P40 [28] high voltage MOSFETS (M1-M6) and PA-93 [34] high voltage op amps (U10

and U17 in Figure 4.12) that control them. These op amps set the bias of the output waveform using two input signals from the MLP Data board; the Bias signal and the Isat signal. Here, the Isat signal is used as a measurement of the current level flowing through the FET switches. At high current levels (~1A) there will be a voltage drop across the 50Ω matching resistor and 10Ω or 5Ω snubber resistors on the FET outputs (~60V). Therefore, the output voltage is scaled up in the proportion of 60V (for both the + and – power rail) per amp of Isat. This function is achieved by U7 and U16, inputting to the non-inverting inputs of U10 and U17.

The MLP Data board outputs a "bias signal", which corresponds to the peak-to-peak bias voltage amplitude normalized to the electron temperature. Ideally, this quantity should be maintained at a value near ~3. The FET Drive board achieves this by a feedback loop: U4, U3 and U12 form an error-integrator, comparing the bias signal to 3 volts. If the bias signal is under 3 volts the integrator capacitor charges, increasing the amplitude of the ± power rails until the 3 volt level is achieved. Resistor values and gain of U11 is set so that the increase in the negative power rail is 3.75 times that of the positive power rail – the ideal bias proportion discussed in Chapter 3. A reading of the voltage level of each power rail (÷100 for negative and ÷50 for positive power rails) is outputted on the front panel so that changes in bias can be monitored.

It should also be noted that the bias control system operates at a much slower speed than the MLP Data circuit. While the MLP Data circuit will update all three parameters and likewise the output signals to the FET circuit in under a microsecond, the FET Driver board was designed to respond to changes on the order of 100 microseconds or longer. This enables the bias to respond more to the trends of its changing inputs rather than track every fluctuation. This system allows the MLP Data circuit to have multiple iterations to precisely lock onto a given parameter set before the bias is changed. This protects against the bias being set to an incorrect level while the system is still trying to lock.

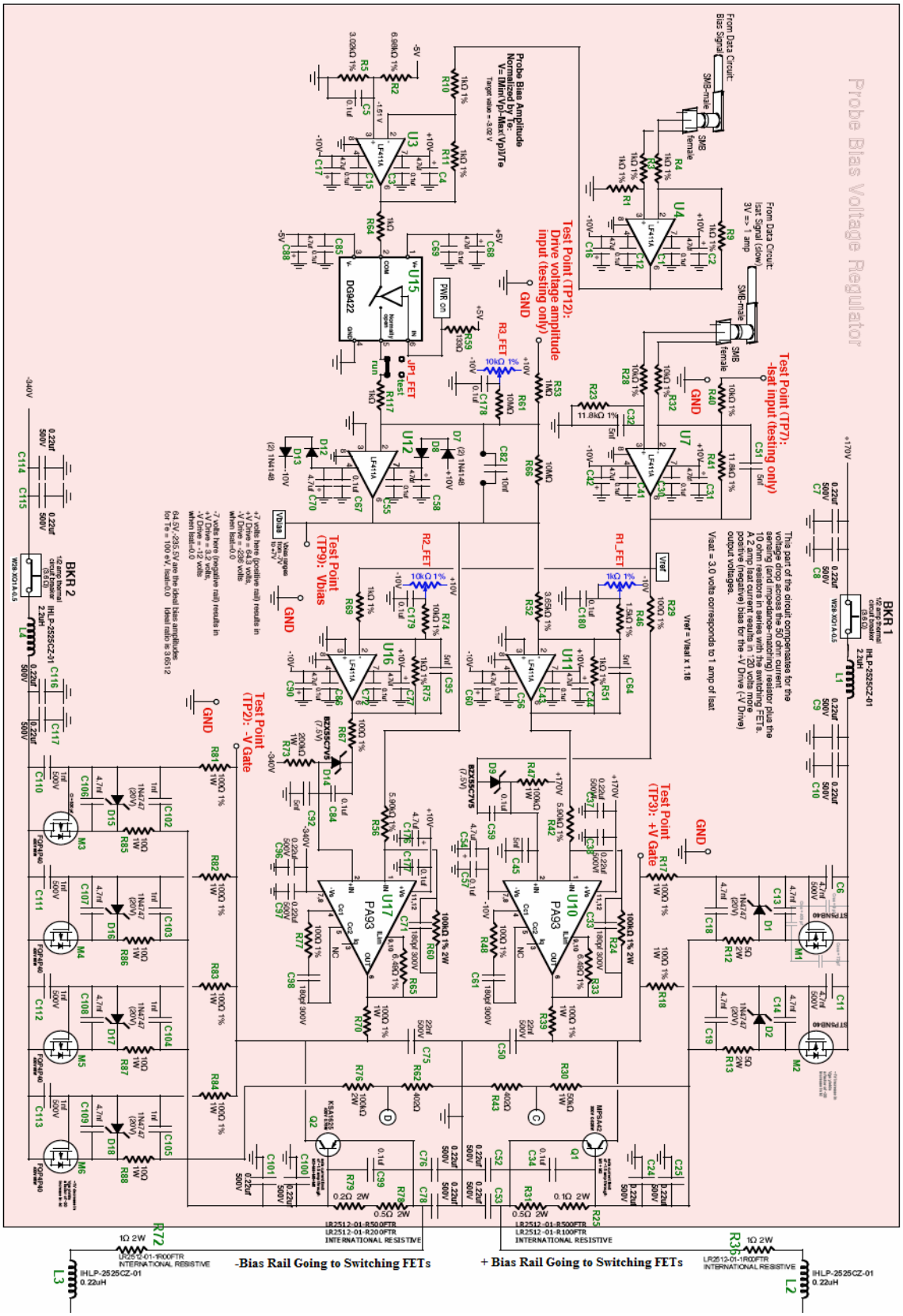


Figure 4.12 – Probe Bias Regulator Circuit

Within the bias control subsection, two important features should be highlighted. These include a current-limiting circuit and a digital switch that is inline with the bias control integrator. The system has two primary current level requirements in the form of quiescent and plasma load. The quiescent load arises from the charging and discharging of output capacitance on each of the switching FETs. Thus, even though there is no load from a plasma, the system still draws time-averaged current levels of roughly 0.5 A for the positive rail and 0.4 A for the negative rail. When a maximum plasma load is put on the system, an additional 0.7 A of current is required from each rail. Thus, when at full operating capacity, the system should draw less than 1.5 A time averaged current from each rail. A current-limiting circuit, which is made up by Q1, R25 and R31 for the positive supply rail and Q2, R76 and R79 for the negative rail, was implemented to limit the time-averaged current for each power rail at this level. This circuit protects against failure modes where the positive or negative rails are connected to ground, limiting the current through the FETs to 1.5 A during such an event. After 3 – 15 seconds at this current level, the high voltage circuit breakers will trip and protect the remaining functional components from thermal destruction.

The digital switch (U15 in Figure 4.12) is used to isolate the FET board from the bias signal during periods when the system is not running. The "PWR on" signal that controls the switch comes from the TTL Waveform Generator board through the backplane and is low when the trigger signal on the TTL board is low. When the trigger is high, this signal is also high. This allows the FET board to return to its quiescent output voltage levels while waiting for the next waveform to be generated. The quiescent levels of this section (and on most of the other boards) are set with fixed resistors with additional potentiometers to fine tune certain levels. The quiescent output waveform amplitude is +6V and -24V, a condition that correspond to the ideal bias voltage for a plasma with Te = 10eV. This procedure of using digital switches to isolate signals while the system is not running is also used extensively in the MLP Data board.

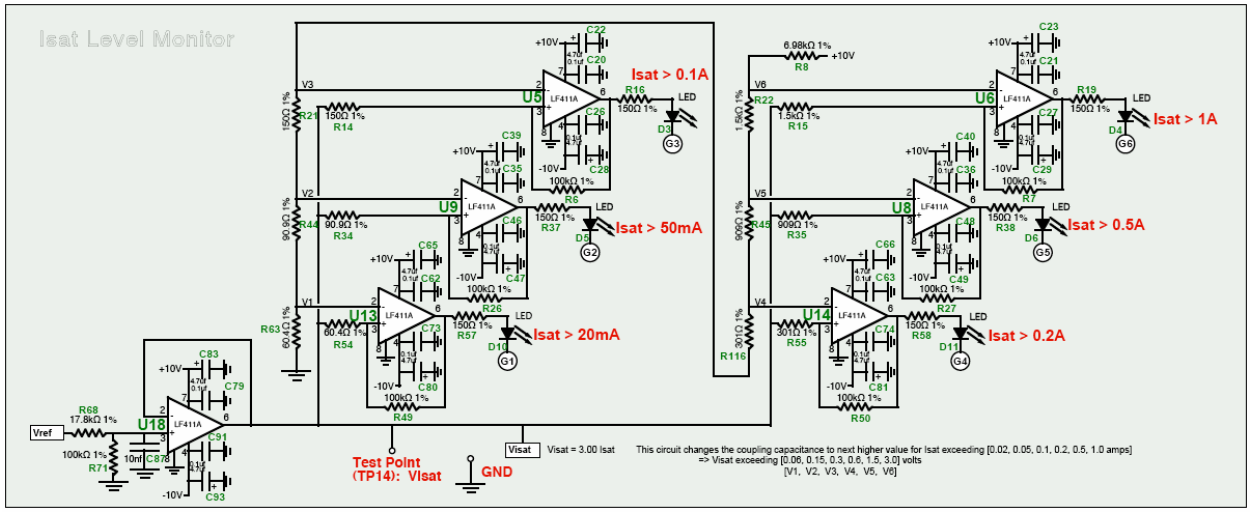


Figure 4.13 – Isat Level Monitor Circuit

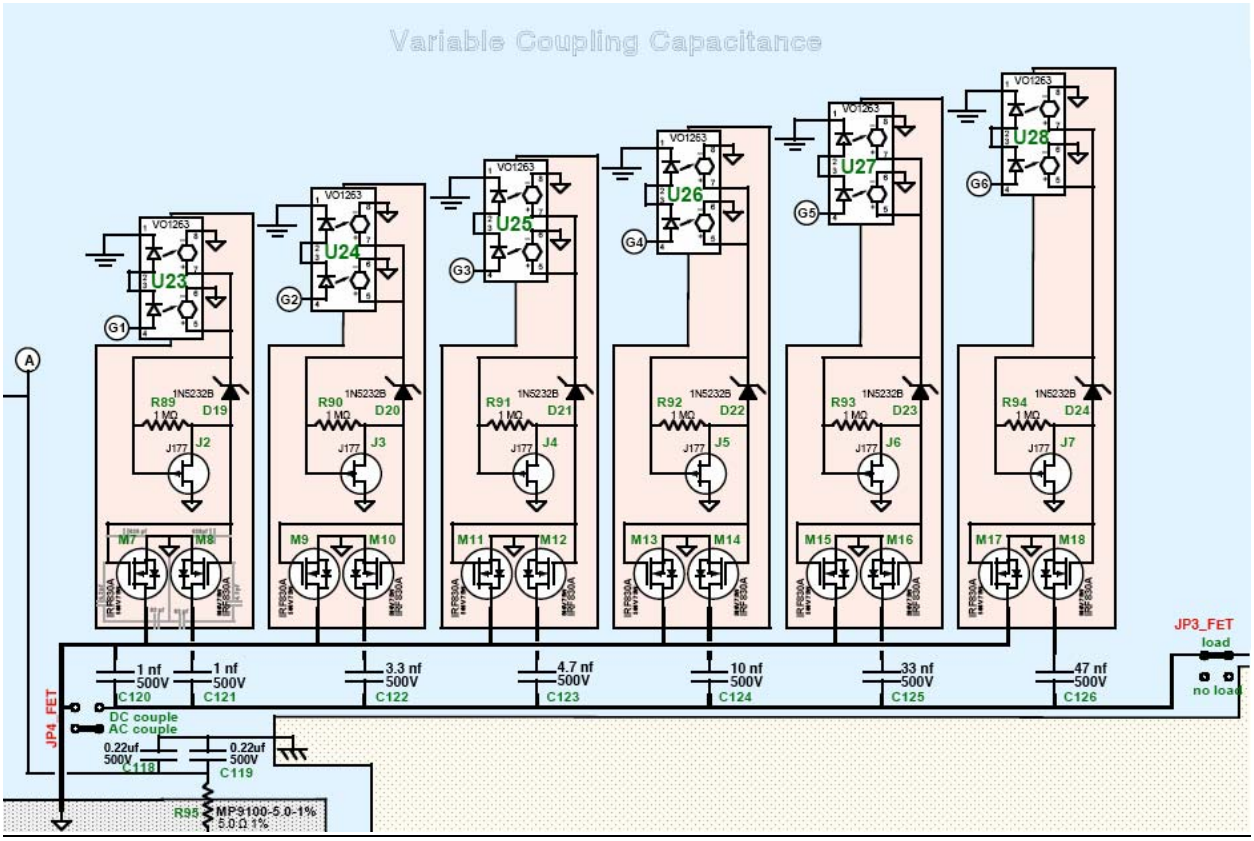


Figure 4.14 – Variable Coupling Capacitances Circuit

The final subsection of the FET Driver board deals with the capacitive coupling of the output line for different levels of ion saturation current. Under normal operation, the output line will be

AC coupled to the FET board to ensure that the time-averaged net current through the Langmuir probe is zero. However, the ideal level of capacitance changes for different levels of ion saturation current. If the capacitance is too small, the output voltage will droop during a given bias state at a rate of $dv/dt \approx Isat/C$. On the other hand if the capacitor is too large then many bias state cycles would be required for the output voltage (during the Vf state) to approach the floating potential value. Thus, this circuit monitors the ion saturation level being reported by the MLP Data board and compares the value to six preset threshold levels. When the ion saturation current increases beyond a threshold, the circuit adds a corresponding capacitor to the output line. Similarly, when the signal falls below a threshold, the capacitor is removed from the output line. Figure 4.13 shows the arrangement of six Schmitt-trigger circuits for this purpose.

The capacitance is altered by either adding or subtracting C121 - C126 from the output line, which is done by the six circuits in Figure 4.14, each of which corresponds to one of the Schmitt-triggers. These circuits utilize back-to-back IRF830A [30] power MOSFETS to act as switches. Similar to the switching FETs, these FETs also require optically isolate gate signals because of the high voltage that exists on the drain. Since response time is not as important here as with the switching FETs, new specialized VO1263 Photovoltaic MOSFET Drivers [30] can be used. These chips isolate the gate signal and drive the FETs in one step while also operating without an isolated power supply. These chips, therefore, greatly simplify the isolation circuit and reduce the number of components needed.

Similar to the bias control circuit, the capacitance on the output line is changed on a time scale much greater than that of the MLP Data board (~1 ms). Again, this is done to track the relatively slower time scale trends in ion saturation current.

4.3.2 – FET Drive Layout & Optimization

The most crucial section of the FET Driver board is the section that generates the waveform. Since these high frequency, high voltage waveforms involve moving a lot of charge around very rapidly (switching transients of ~20A), much effort was put into optimizing the physical layout of the board. First, the entire waveform-generating section was placed near the front of the board because the output signal leaves the board through a BNC connector on the front panel. Second, lab ground, which elsewhere fills the free space of the top, bottom and first inner layer of this 4

layer board, was removed from this section to minimize capacitance to ground. Each of the three isolated grounds was put on the first inner layer of the board and all the components that share a given isolated ground were put as close together as possible. These three ground planes were then put as close to each other as possible (without overlapping) to form an interlocking center where the three switching FETs meet. The output line trace was made extra thick and all ground planes were removed from below it to minimize parasitic capacitances. Resistors R95, R96, R113 and R100 (in Figure 4.11) act as "snubbers" to eliminate high-frequency ringing that would arise from the intrinsic capacitance and inductance of components and traces. These values were chosen empirically. They do not substantially degrade the switching rise/fall times of the output waveforms. The final output stage from the FET section was made as symmetric as possible to ensure that the signal traveling to the real probe connector would be the same as the signal traveling to the dummy probe connector. Finally, a shield was placed over this entire section to minimize the broadcasting of RF waves.

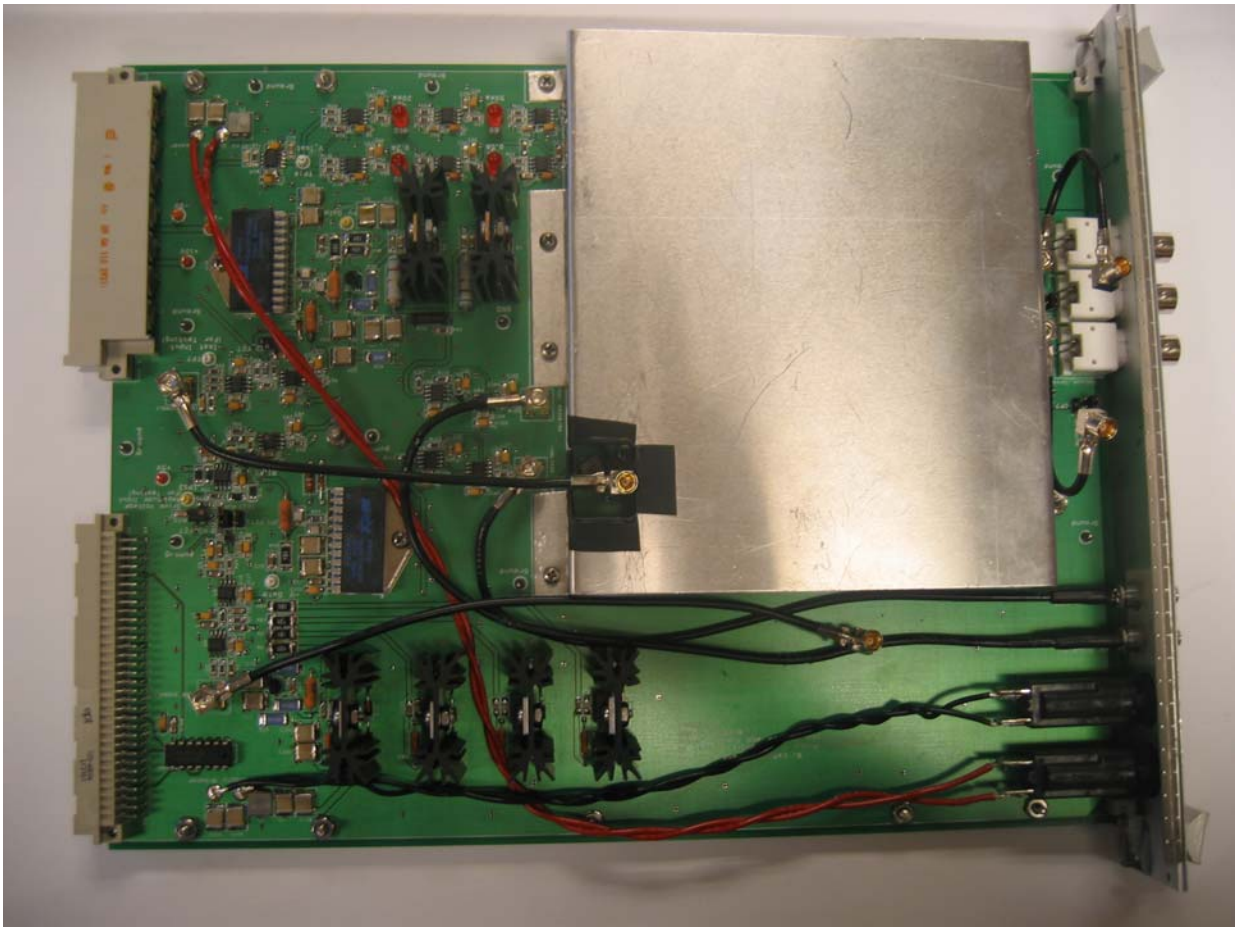


Figure 4.15 – FET Board with Shield and MLP Data Board Interconnections

The other sections involve signals that are either much lower in power, frequency or both and do not require any particular special layout considerations. Attention was paid, however, to heating concerns of the various high power devices on the FET Board. All of the switching FETs (including their respective high wattage resistors) and power rail regulating FETs were attached to heat sinks before being loaded on to the board. These heat sinks help take some of the thermal load during waveform generation and increase the rate of cooling from the fans that are constantly circulating air through the rack. The only other components capable of producing significant heat are the PA-93 high voltage op amps (~3W). These op amps were laid flat on the board so that the ground plane on the top layer of the board would act as a heat sink for these devices. A shield was attached to the back of the board that spans its entire area to minimize interference with the MLP Data board from the additional FET/MLP Data Board pair that will be installed behind it in the near future.

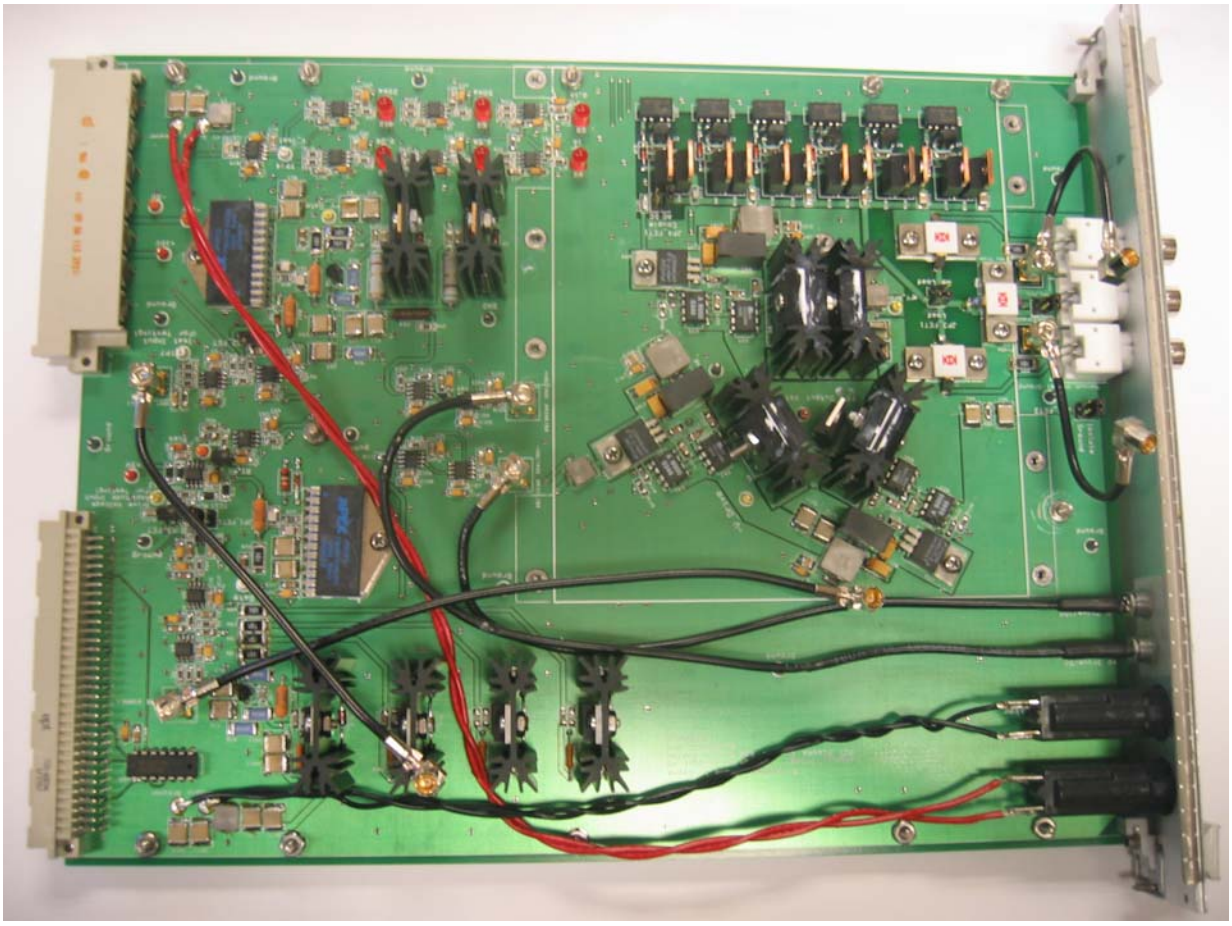


Figure 4.16 – FET Board without Shield

4.3.3 – FET Drive Performance

There are 4 primary bench tests needed on the FET Drive board; an output showing the waveform generation, the bias control, the Isat control and the variable coupling capacitance. The most basic test is to view the output waveform and compare it to the controlling FET TTL signals as well as the MLP Data TTL signals to make sure the timing is correct. Of course, to record the voltage waveform, the current and voltage sense circuit from the MLP Data board is needed, so this can also be viewed as a test of this circuit as well. Figure 4.17 shows the TTL signals, voltage waveform and current readings for the waveform with maximum value of Vbias[7] (Isat =0) and with no coax cables connected to the output line. The delay between the TTL signals and the actual changing of the waveform is evident. Also, the MLP Data TTL signals are lined up to properly sample during the time periods when voltage and current are both settled. During these sampling periods, the current hovers around ±2mA, a level that is below the sensitivity of the MLP Data board. During the waveform transitions, however, the current can spike to ~90mA, which is a significant signal and illustrates the need for precise delay in the MLP Data board TTL signals. The amplitude of the output waveform is -230V to +60V. This corresponds to the ideal bias for a plasma with Te = 100eV. The 1/e rise and fall times for these waveforms are roughly 75 ns.

[7] Note: Vbias is the output of the probe bias error integrator (U12 in Figure 4.12)

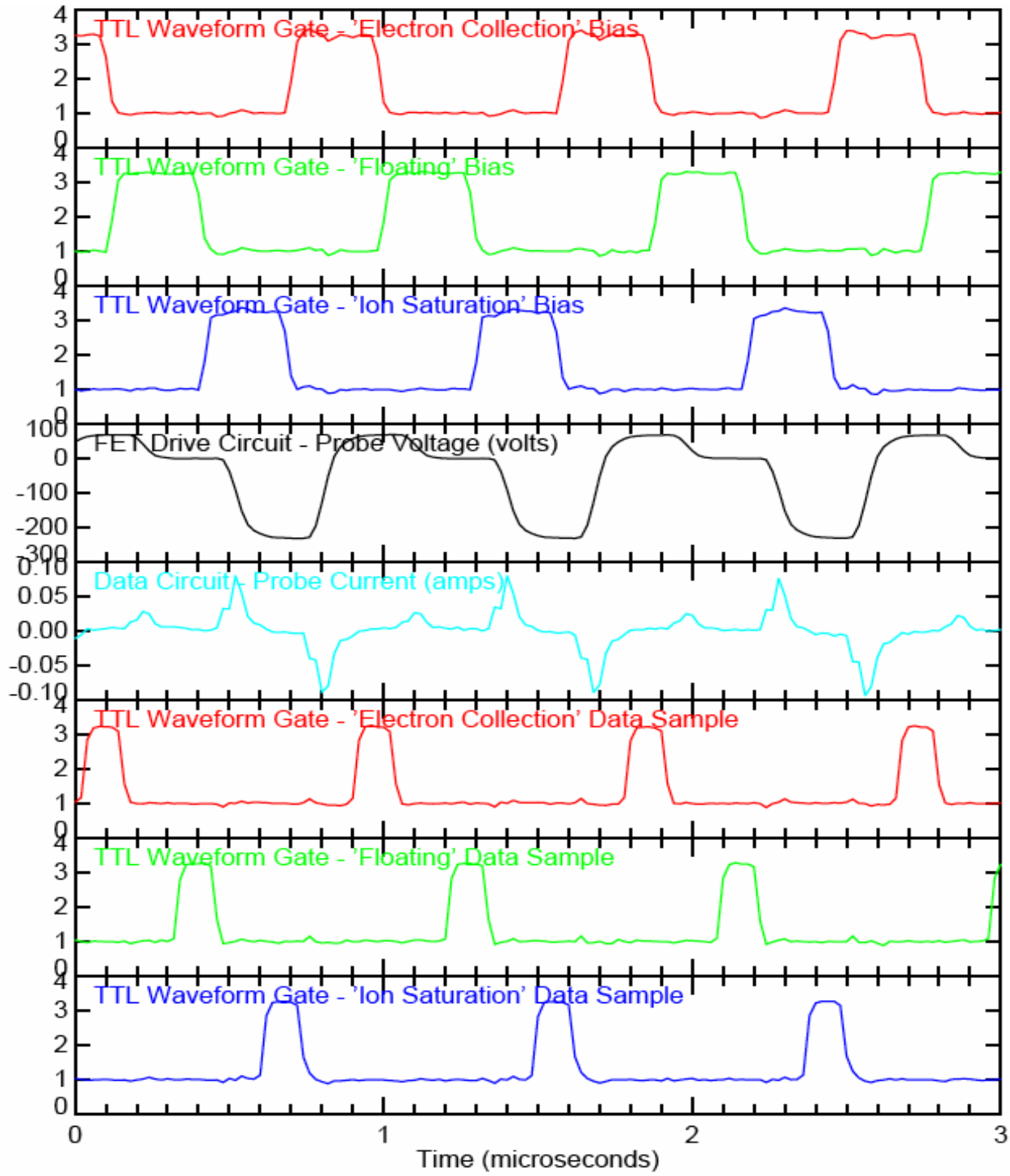


Figure 4.17 – FET Board Output (Max Bias) with TTL Signals

Figure 4.18 is the same as 4.17, but is generated with the quiescent level of bias (-24V, +6V for Te=10eV). Under this test, the spurious current levels are observed to be proportionally lower

than that of the maximum bias test, evidence that they involve balanced capacitances in the current sensing circuit. The timing of the TTL signals in relation to the voltage and current signals, however, remains the same.

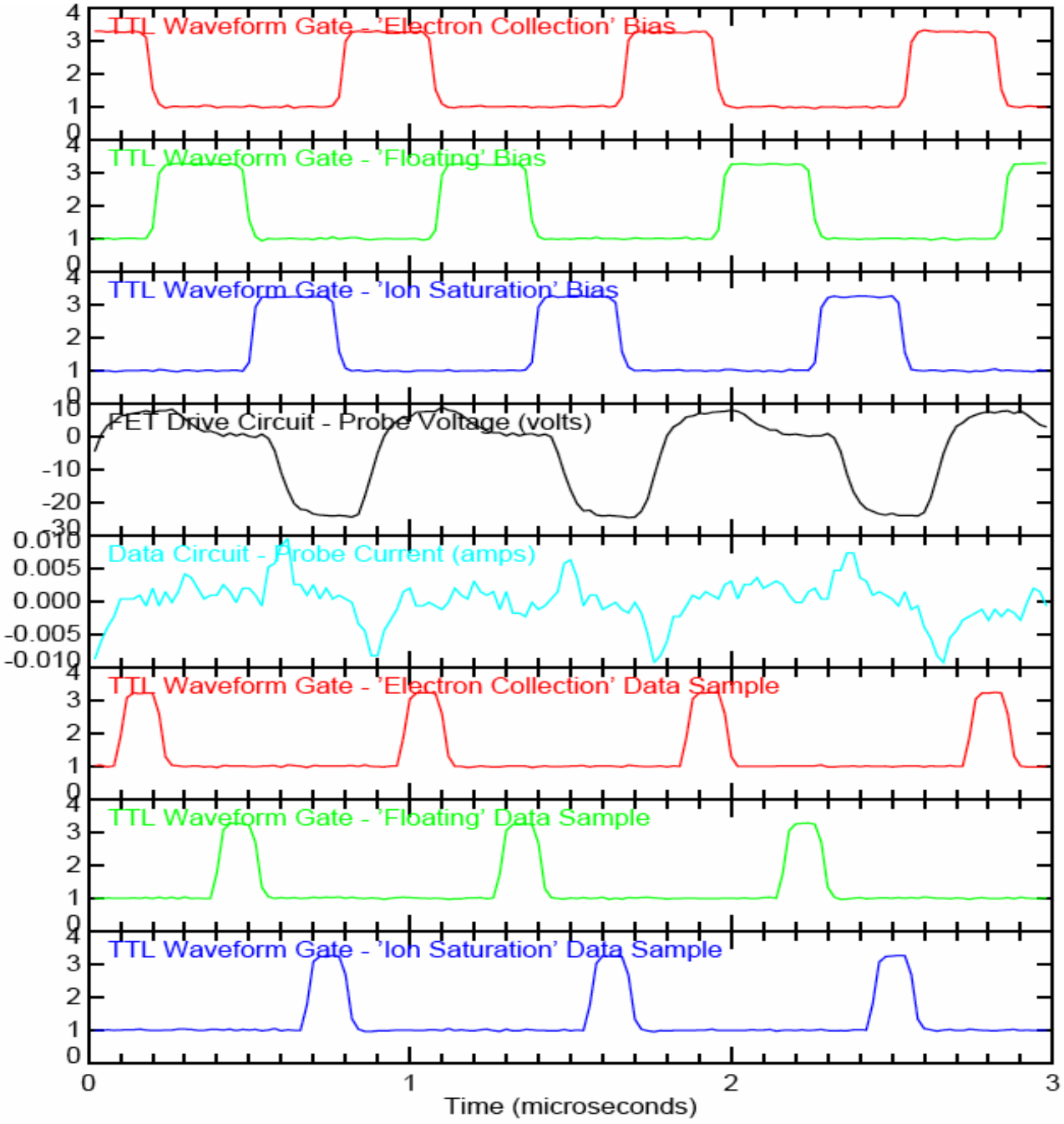


Figure 4.18 – FET Board Output (Min Bias) with TTL Signals

Although these two figures show the two extremes of Vbias on the FET board, they do not show the circuit's response to this signal. As described above, the bias control is meant to respond over long time scales, thus Figure 4.19 takes a long-time view of this signal's affect on the waveform. For these tests, Vbias was controlled directly; the error integrator (U12) was disabled by opening JP1_FET. The functionality of this aspect of the FET circuit is self-evident.

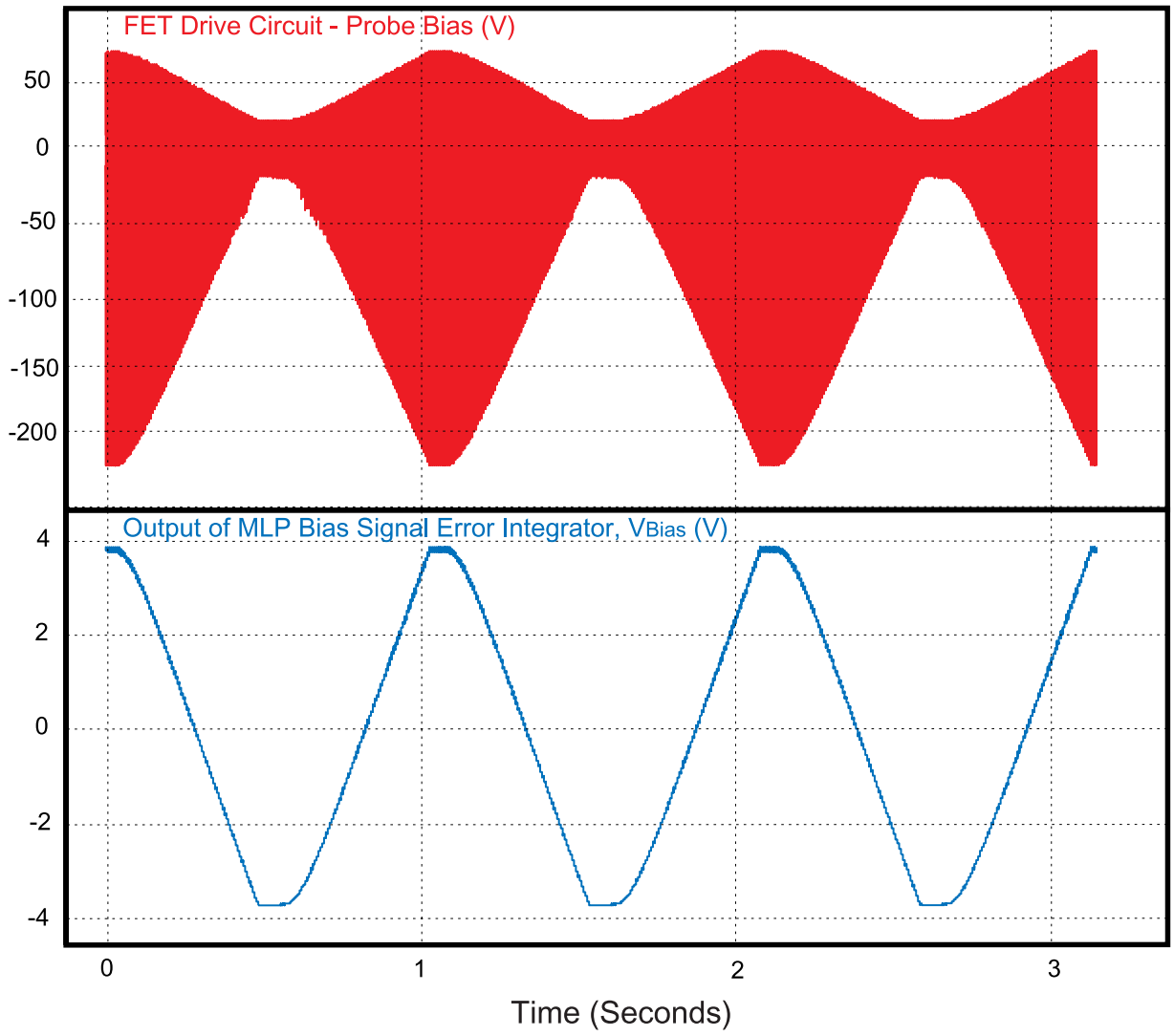
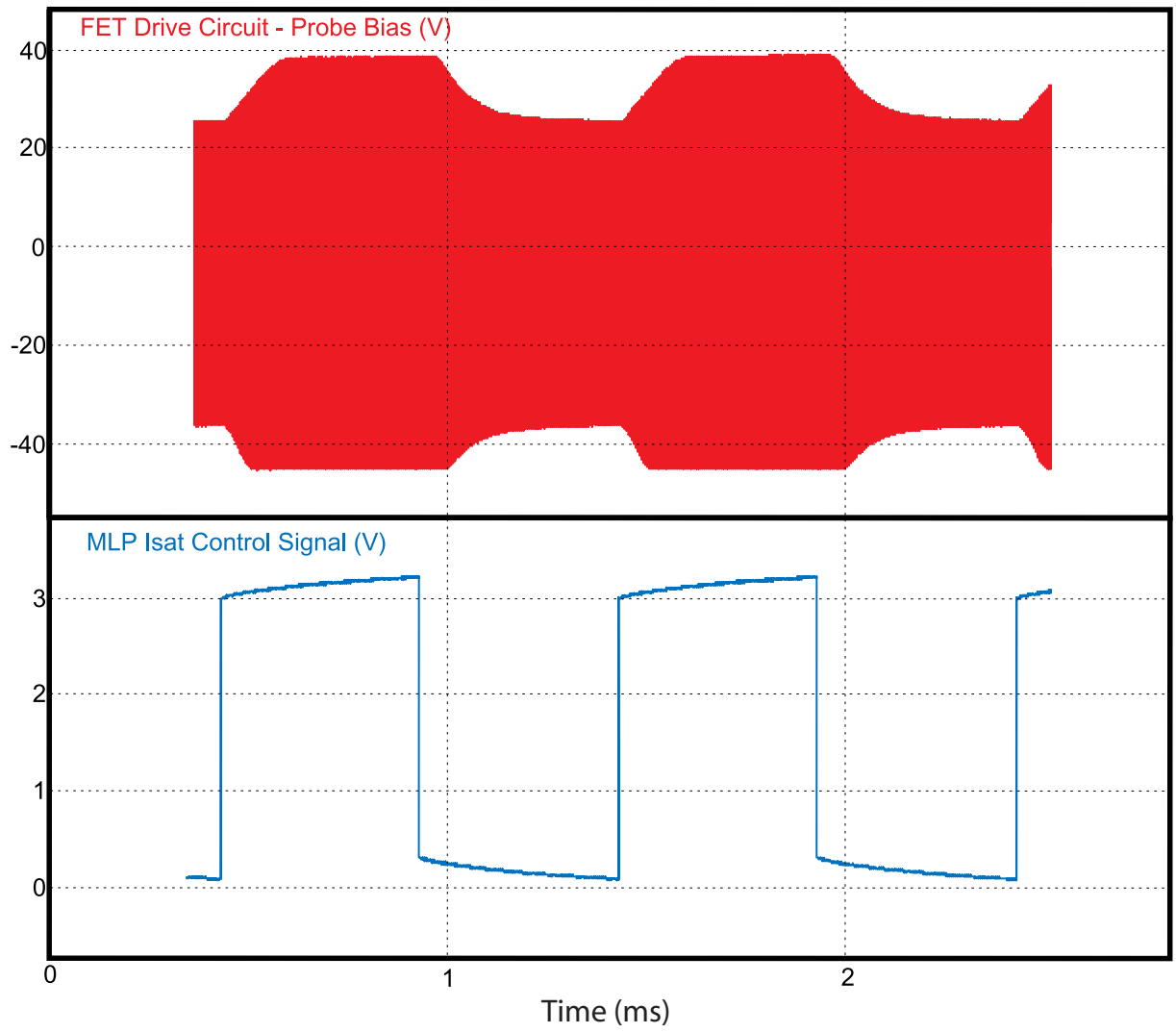


Figure 4.19 – FET Board Output with Variable Bias

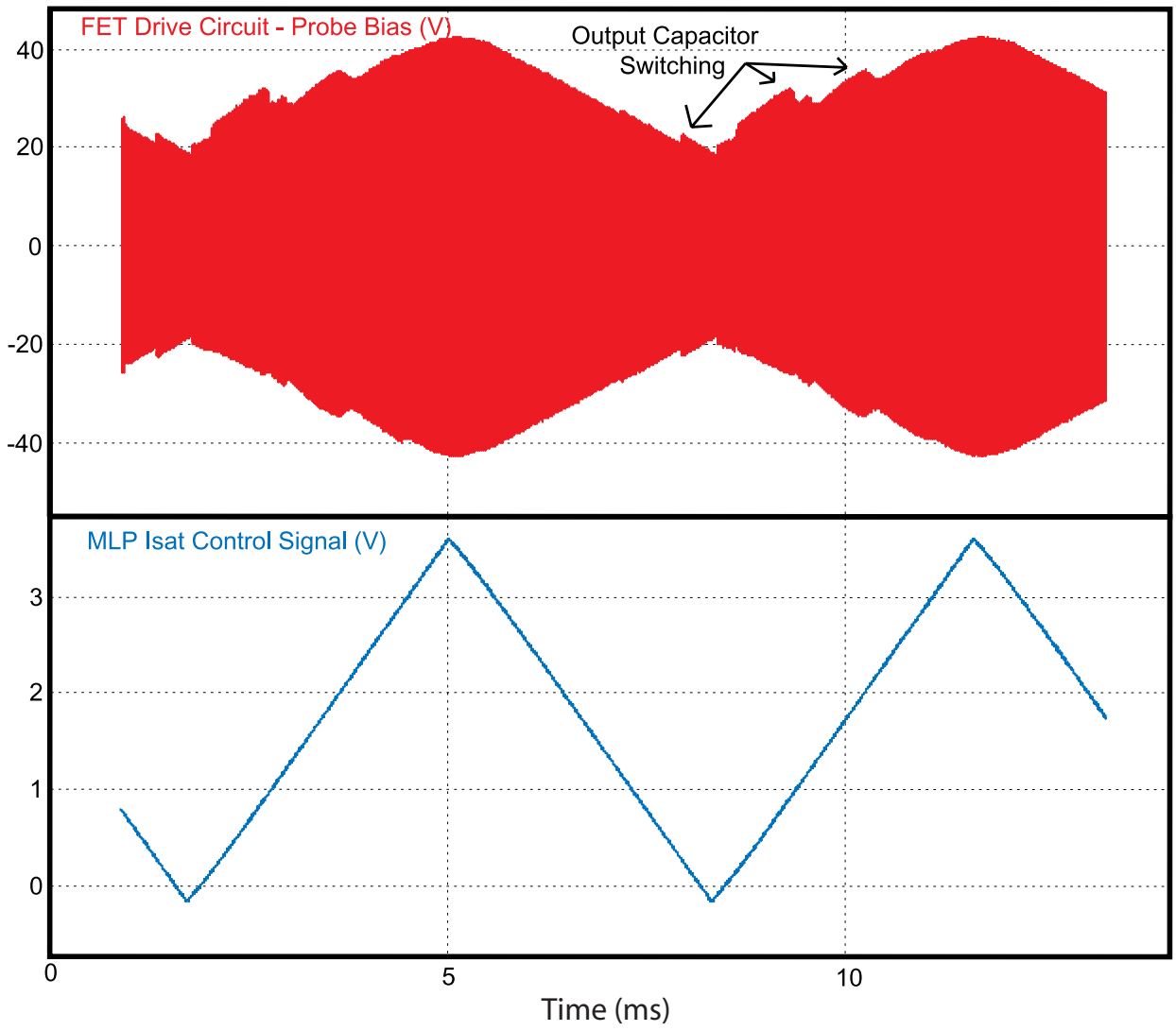
Finally, the FET board's response to the Isat signal was investigated. In Figure 4.20, a rapid change in Isat is shown, which illustrates the designed slow response. In Figure 4.21, a ramped change in Isat is applied to show the response of changing capacitances on the output line.

Evidence of additions and subtractions in capacitance can be seen as sharp changes in the envelope of the voltage waveform.



Note: 3 Volts on the control signal corresponds to 1 A of Ion Saturation Current.

Figure 4.20 – FET Board Output with Rapidly Changing Isat



Note: 3 Volts on the control signal corresponds to 1 A of Ion Saturation Current.

Figure 4.21 – Slow Changing Isat with Capacitance Effects on Waveform

4.4 – MLP Data Board

The brain of this project lies with the MLP Data board. While the other boards are important, they merely create the necessary environment and support signals that the MLP Data circuit needs to perform its measurements and analyses. The MLP Data board is in charge of measuring the voltage and current from the Langmuir probe, calculating electron temperature, floating potential and ion saturation in real-time, generating the bias amplitude control signals for the

FET board and outputting all this information to the outside world. Needless to say, accomplishing all of these functions leads to the MLP Data board being very complicated and also the product of most of the time invested in this project.[8]

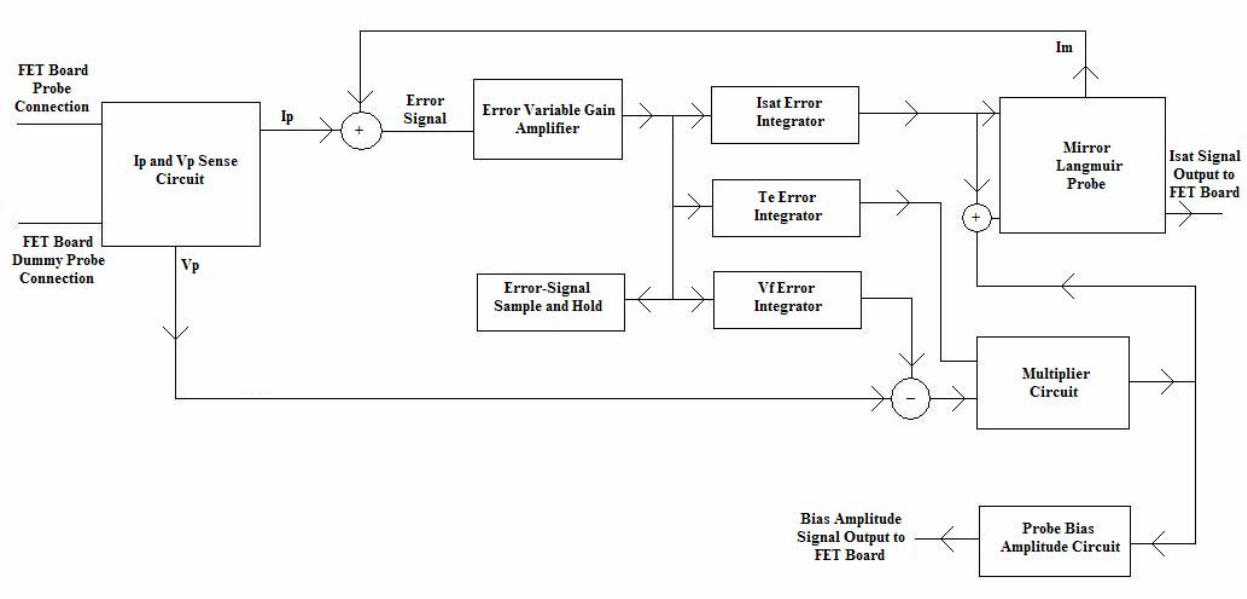


Figure 4.22 – MLP Data Circuit Functional Block Diagram

4.4.1 – MLP Data Subsection Detail

The entire theory of the MLP system is based on being able to rapidly and accurately measure the voltage and current from the Langmuir probe and this is where the MLP Data circuit starts. This section is critical because voltage and current must be measured correctly or the MLP system will never have a chance of outputting the correct plasma parameter values. The current and voltage sensing sub-circuit must not only be fast and accurate but also able to handle a wide range of values (-250 to +120V and 10mA to 2A). To accomplish all of these design specifications, the MLP Data board uses two mechanisms; a precision-tuned voltage divider for voltage measurements and a broadband RF transformer to sense the current level.

[8] A complete schematic of the MLP Data circuit can be found in Appendix A.

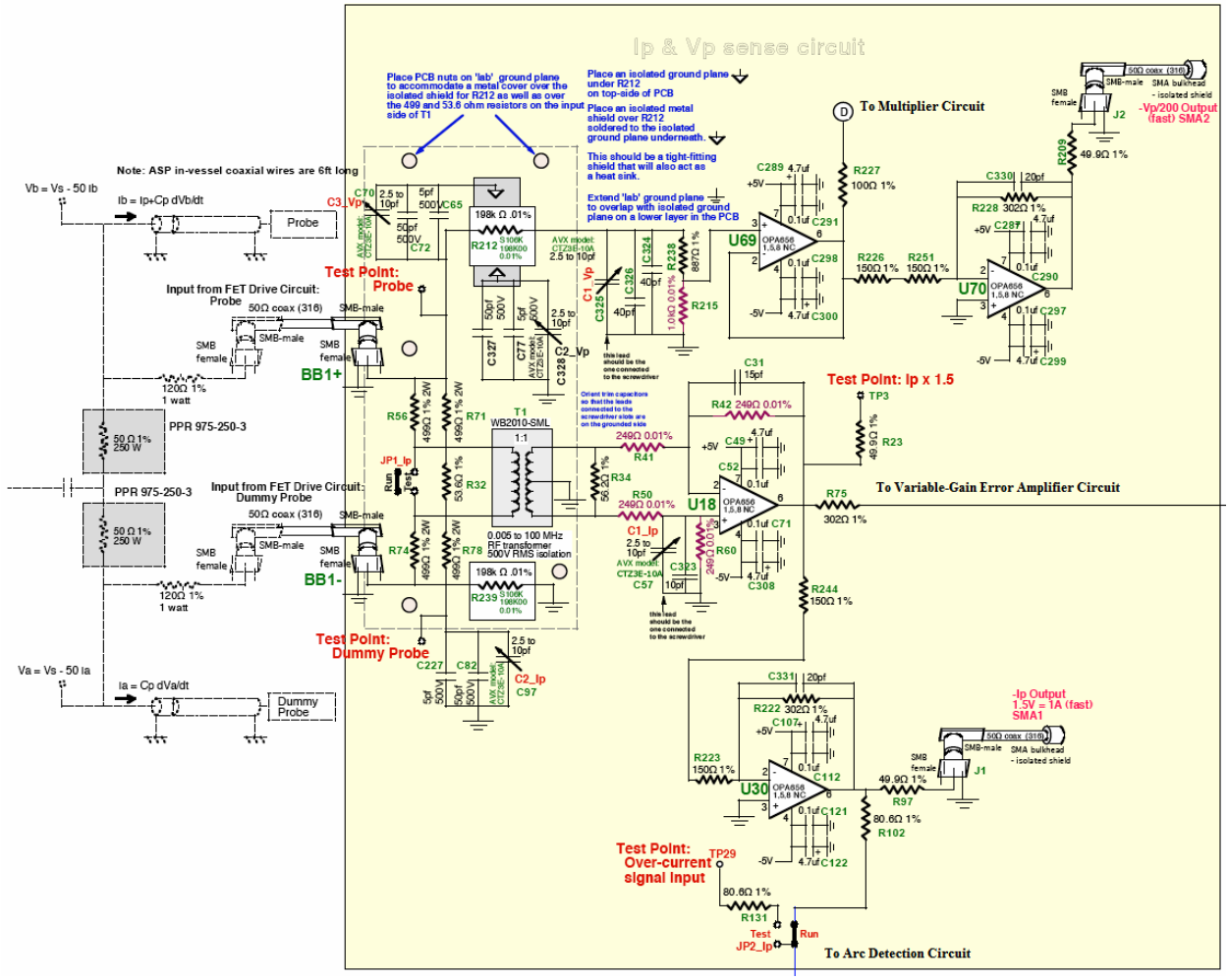


Figure 4.23 – Current and Voltage Sense Circuit

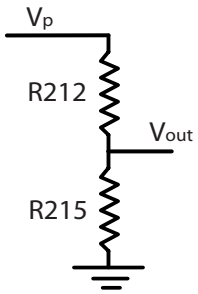
The current measurement is performed with the help of a WB2010-SML [35] wideband RF(0.005 – 100 MHz) transformer operating with a 1:1 turns ratio. However, setting up this device in the proper manner is critical to ensure an accurate current reading. When a voltage is applied to the Langmuir probe, it responds with a current (Ip), which is the signal of interest. However, the 50Ω coax transmission line used to connect the FET Driver board to the Langmuir probe introduces capacitance and signal reflections. Thus, the current signal returning from the Langmuir probe includes these spurious currents and a significant error in our measurement could be introduced. (However, by choosing the "Data sample" TTL waveforms to occur at the right time, much of these spurious effects can be avoided. See Figure 4.17 and associated discussion). To null out these effects, an identical coax cable is attached to FET Output line in

the exact same manner as the real probe connector. This other cable is called a "dummy" probe. The difference in currents flowing through the 50Ω resistors that terminate the "probe" and "dummy probe" coaxes is measured by shunting a portion of this difference current though the RF transformer (T1). The combination of shunt resistors is chosen so as to produce an output voltage on U18 that corresponds to 1.5V per ampere of probe current. R32 in conjunction with the shunt resistors provide a 50Ω source impedance for T1. R34 combined with the input resistors for U18 to provide a 50Ω load for T1.

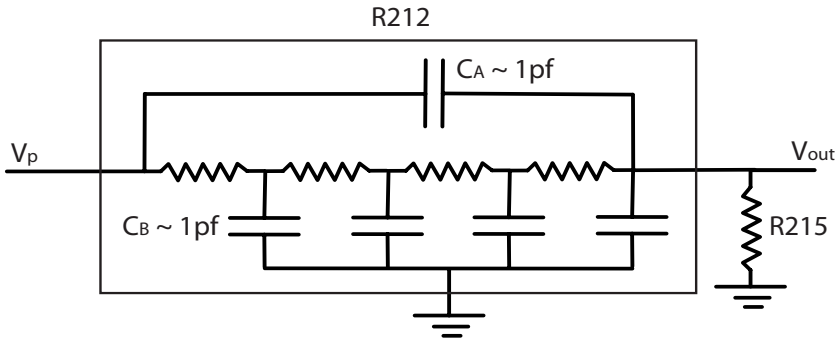
In theory, measuring the voltage on the probe is much easier. There are no concerns about the coax cables or other parasitic capacitance affecting the signal since the voltage is being driven by the robust FET Driver circuit. The voltage signal arriving from the FET Drive probe connector is the true signal of interest, so a simple voltage divider can be used to step down the range from +120 to -250V to +0.3 to -0.625V in order for the RF op amps and transistors to utilize the signal. The only requirement is that the divider be made up of resistors with the following characteristics; high resistance value so as to not load down the FET output, high precision to ensure an accurate measurement is made, a power rating that will handle the maximum current level and no capacitance or inductance in the device. There are no resistors in existence that meet all these criteria and only a few that meet the first three. These select few resistors have relatively small intrinsic parallel capacitance (C_A) and distributed capacitance to their outside case (C_B) but when they are combined with the high resistor values of interest (198kΩ), the voltage experiences an RC roll off time of roughly 200 ns, which makes our voltage measurement much too slow (See Figure 4.24).

The parallel capacitance can be easily compensated by adding a suitable capacitor to the other divider resistor (C_1). Two fixed capacitors plus a variable one is employed for this task on the MLP board. However, the compensation for the case capacitance is more complicated. Since it is impossible to isolate the resistor from the board while being connected to the circuit, the next best option is to surround the case of the resistor with a conductor that is at a similar voltage level as the input. With this set up, the signal in the resistor only experiences capacitance to a voltage level very similar to itself which minimizes the dV/dt and the resultant RC roll off.

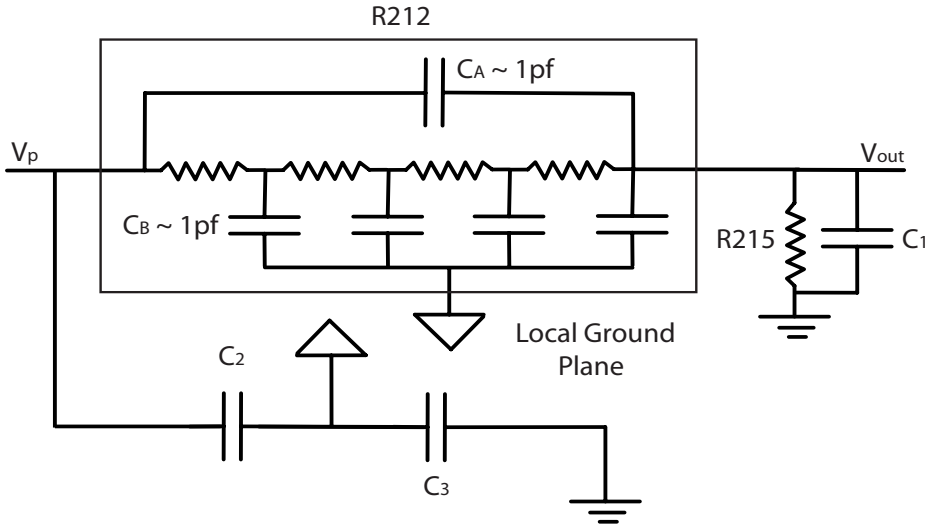
A) Ideal Model:



B) Real Model:



C) Compensation Scheme:



- C_1 compensates for parallel parasitic capacitance (C_A) forming an AC voltage divider

-C_2 and C_3 form another AC voltage divider to place the local ground plane and foil shield of R212 at a voltage of approximately 1/2 of V_p. This nulls out the influence of the distributed capacitance to the resistor case (C_B).

Figure 4.24 – Method to Compensate for Parasitic Capacitance R212

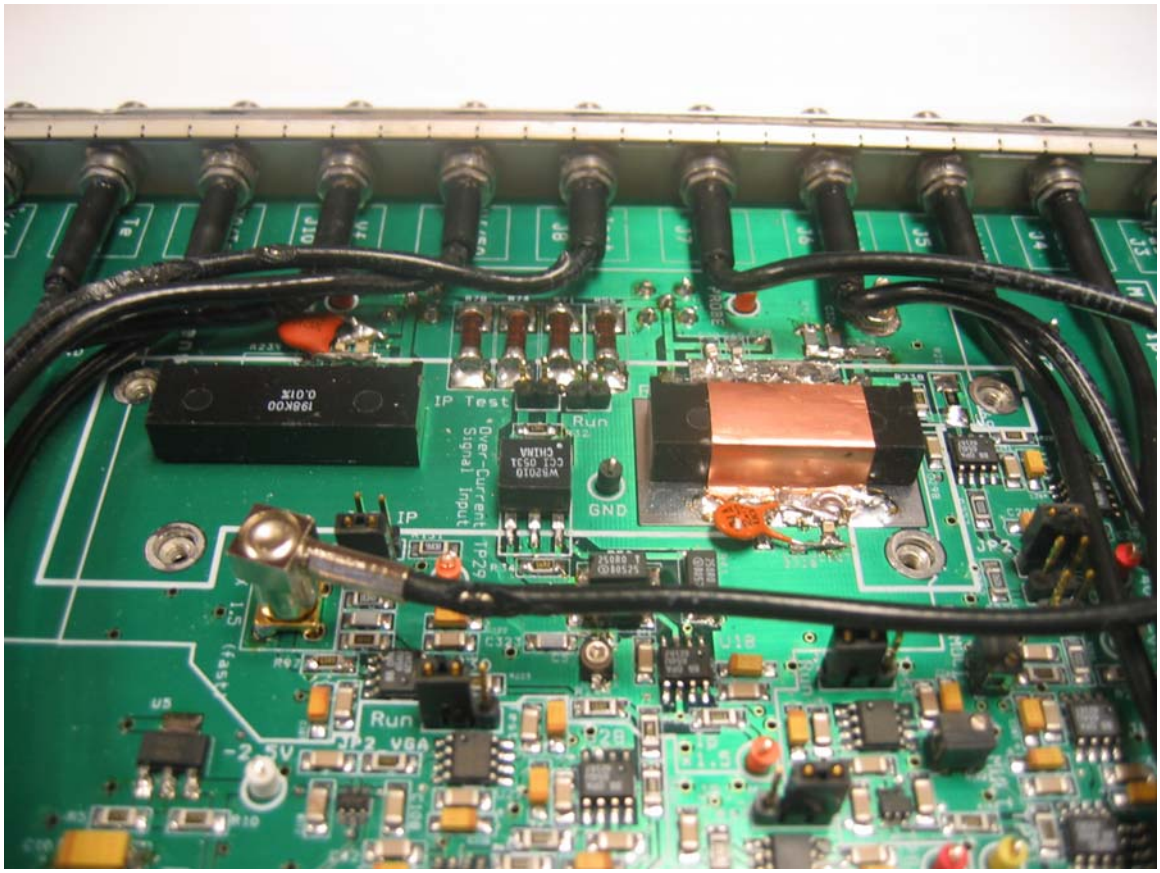


Figure 4.25 – Current and Voltage Sense Circuit Photo

In order to account for this RC effect, a capacitive voltage divider (C2, C3) was utilized in parallel with the resistive one. Since C_B is a distributed capacitance that couples voltages all along the resistor to its case, the ideal voltage to surround the resistor is one that is halfway between the resistor's input and output terminals. High frequency signals were of primary concern here, thus using a capacitor voltage divider is ideal. As seen in Figure 4.25, the 198kΩ S106K [30] resistor was laid flat on an exposed, tined copper plane and its leads were soldered into their respective pins. Copper tape was then wrapped around the case of the resistor and it was soldered to the exposed plane. Capacitors were then placed from the input line to the plane, from the plane to ground and from the output line to ground. Using static and adjustable capacitors, the capacitance in these three areas was tweaked until the RC roll off was no longer noticeable. Once the capacitance was set, the variable capacitors were replaced with static devices of the same value due to concerns of the variable capacitors changing their value with

time. After the optimization was finished, a grounded shield was installed over the current and voltage sensing circuit to protect this highly sensitive area from external interference.

Entering the next stage of the MLP circuit, a fast, accurate and scaled-down reading of the current and voltage on the Langmuir probe is available for the high bandwidth electronics to analyze. The next step is to apply the voltage to the PNP/NPN transistors and generate the Mirror Langmuir Probe current signal. But before this voltage signal can be applied to the transistors, it must be appropriately scaled to the form discussed in Chapter 3. To achieve this, the voltage measured from the Langmuir probe must have the scaled version of the most recent floating potential (Vf) calculation subtracted from it before being multiplied by a scaled and inverted version of the most recent electron temperature (Te) calculation. These two calculations are carried out by a summing junction for the Vf adjustment and by an AD835 250MHz bandwidth multiplier chip (U61) [36] for the Te adjustment (see Figure 4.26).

Implementation of both functions is relatively straightforward, but a few extras are added to ensure maximum accuracy in these calculations. First, two potentiometers (R1_MULT and R2_MULT) are used to remove DC offsets at the input to the multiplier chip. This adjustment allows for the multiplier chip to be accurate on the sub-millivolt scale, ensuring that a zero on either input will yield zero output. The second accuracy enhancing feature is achieved using a digital switch and integrator (U63 and U66). The integrator is used remove any DC offset in the output stage of U61. R3_MULT is used to enhance the gain accuracy of the multiplier, ensuring that 1 x 1 = 1. The "PWR on" signal that controls the digital switch is obtained from the TTL Waveform circuit via the backplane and is high whenever the system is active. In this case, a high PWR signal causes the switch to open and the integrator will hold its value and not respond to changes in the output of the multiplier. This is obviously done to keep the integrator from affecting the output of U61 while the system is running. When the system goes inactive and PWR goes low, the switch closes and the integrator once again acts to ensure that the output of U61 is zero during this time when the Vp and Vf inputs are zero. This offset-zeroing sub-circuit is repeated many times throughout the MLP Data board in areas where DC offsets on important signals need to be zeroed to prepare the circuit for the next active session. This also ensures that the MLP Data circuit always returns to the same quiescent state between active sessions.

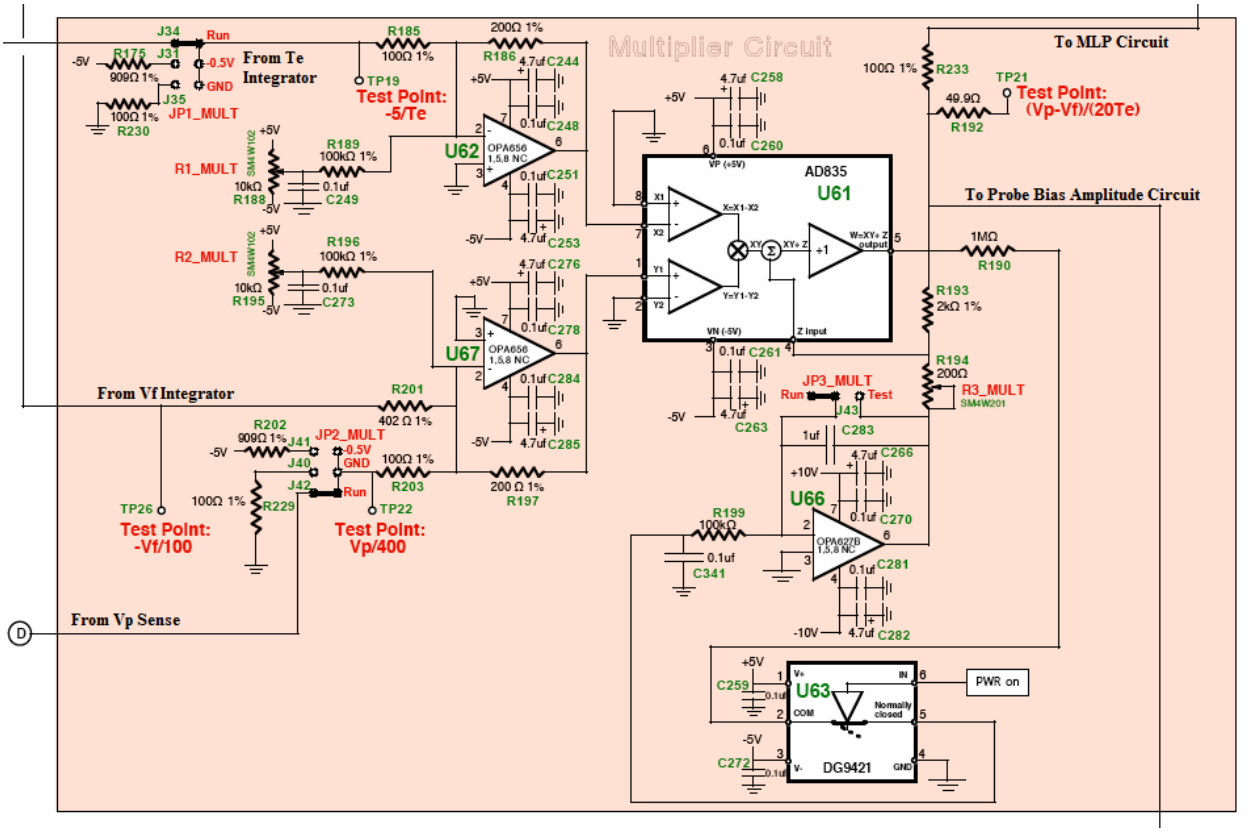


Figure 4.26 – Multiplier Circuit

The voltage that leaves the multiplier circuit represents the quantity (Vp-Vf)/20Te and is applied to the emitter of the NPN MLP transistor (Q3) via U33 (Figure 4.27), which divides it by two. It should be noted that the MLP circuit drives the transistors through their emitters, keeping a fixed bias on their bases. This configuration avoids the 'Miller Effect', which would limit their bandwidth [18]. U33 also receives the ion saturation signal from the integrator and applies it to the emitter of Q3, which satisfies half of the MLP theory. As covered in Chapter 3, the function of the PNP MLP transistors is to just source a scaled representation of the ion saturation current. Thus, the signal from the ion saturation integrators is also applied to their emitters via U17 and the input stage to the "brain" of the MLP system is complete.

The MLP transistors now have the input voltages necessary to generate the most important signal of the system, which is the Mirror Current (Im). Much time was spent running PSpice simulations of different transistor pairs in order to find the combination that most closely resembled the ideal current response calculated from theory. The BFT92 PNP and BFR505 NPN transistors [37] were found to achieve the best performance but only as long as their output

current was kept low (less than 2mA). As a result, an extensive reduction of the current flowing through these transistors was needed. Likewise, a substantial scaling up of Im is required to restore the proper relationship with the Ip measurement from the current sense circuit. This scaling factor is set by the resistor through which the MLP transistors drive Im to ground and the subsequent voltage amplification of this signal. The 2kΩ resistor (R58) in combination with the gain of U34 and U28 (Figure 4.28) sets a scale factor of 8000. The buffer U34 sends this voltage to the next stage of the MLP Data circuit where it is compared to the Ip measurement.

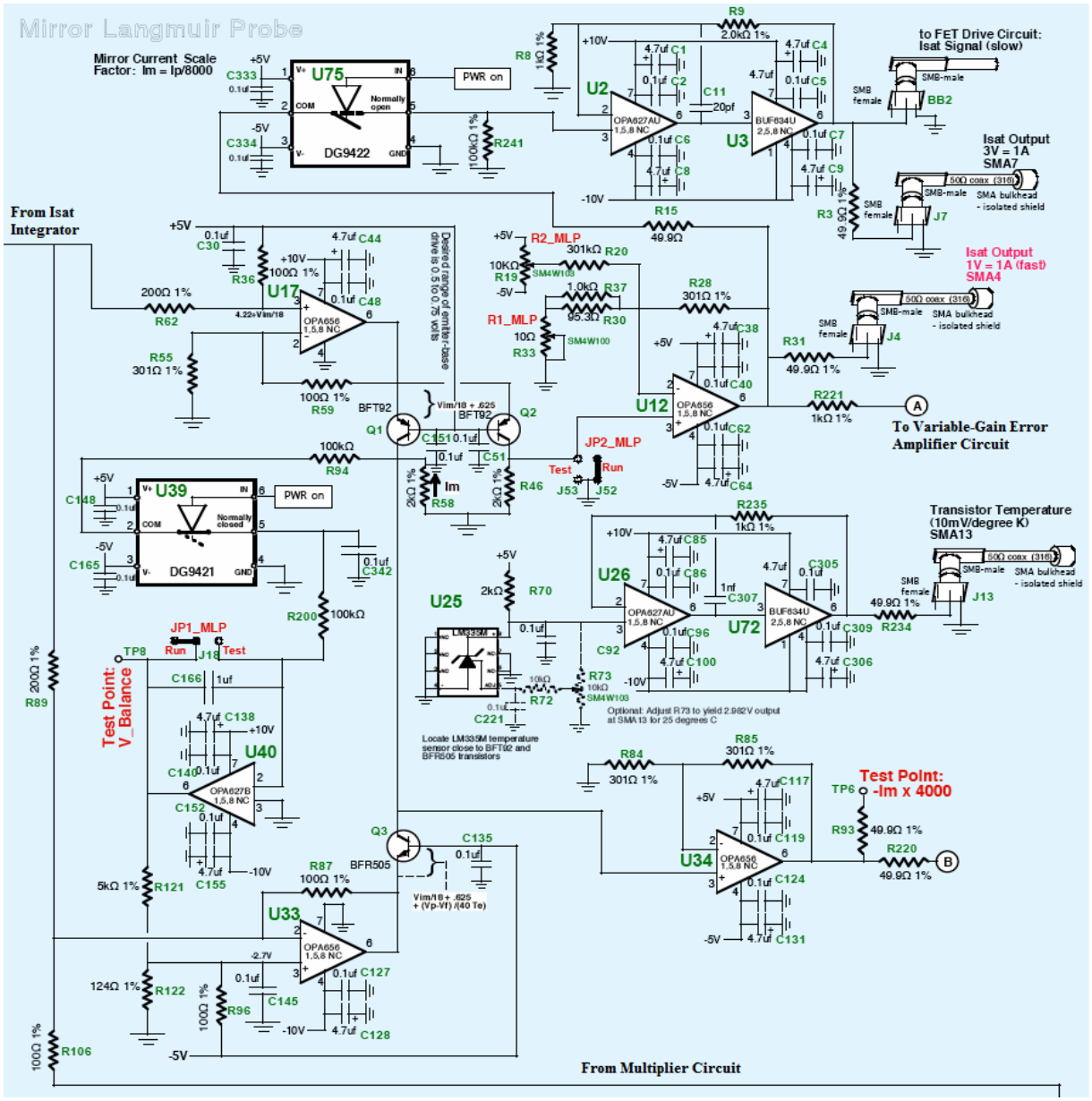


Figure 4.27 – Mirror Langmuir Probe Circuit

While transistors Q1 and Q3 are operating as a pair to generate Im, transistor Q2 produces the second important output of the MLP sub-circuit, the ion saturation current signal. The MLP theory states that obtaining a complete mirror current requires the use of an NPN and PNP transistor, which is the implementation discussed above. However, the theory also shows that if ion saturation current alone is desired, a mirror output can be obtained through the use of an additional PNP transistor. Q2 acts as a "mirror" of Q1; the current being driven to ground across the separate 2kΩ resistor (R46) by Q2 creates a voltage which corresponds to the ion saturation current that the MLP circuited has calculated. For this measurement to truly be useful (and accurate), Q1 and Q2 must respond in the same manner when experiencing the same input signal. Therefore, they are located close together on the board to ensure that they operate at the same temperature.

A high precision op amp (U12) monitors the voltage on R46 and scales it to obtain a 1V:1A output ratio. R1_MLP provides a fine adjustment of the gain to compensate for mismatches in Q1 and Q2. This signal is then outputted to four other areas. Since a measurement of ion saturation is one of the three plasma parameters desired from this system, this signal is sent to the front panel where it will be connected to the 50 MHz digitizer and recorded. Similarly, this signal is buffered through U2 and U3 and sent to the front panel again as a slower version that can be captured using a 10MHz digitizer. This buffered signal is also sent to the FET board to provide the Isat signal for bias control purposes. Finally, an un-buffered Im signal is sent to another stage of the MLP circuit, the Variable-Gain Error Amplifier.

Rounding out the MLP circuit are three additional, non-primary features consisting of two auto-zeroing functions and a board temperature monitor. The sub-circuit involving U40 and U39 operates as a PWR signal controlled, auto zeroing function in the same manner used in the multiplier circuit. This subsystem insures that the mirror current is zero when the probe bias is at the floating potential (Vp=Vf). The other digital switch (U75) is also controlled by the PWR signal and zeroes the two buffered output signals while in the non-active state. This is done to ensure the Isat signal being sent to the FET board is zeroed, which is needed for the FET board to return to its quiescent state. Finally, a temperature monitoring chip is used (U25) to record the

temperature of the board near the transistors so adjustments can be made to measurements during analysis to account for the effect of transistor temperature on Im.

The next stage of the MLP Data circuit is in charge of comparing the measured Langmuir probe current (Ip) with the calculated MLP current (Im) and calculating an error signal for any differences between the two. This calculation starts at a summing junction where Ip and Im combine. When these signals meet, Im is scaled to the same level as Ip but is inverted. Thus, they should cancel each other out if Im has been correctly calculated by the MLP circuit. If not, then an error exists and the MLP circuit must adjust Im until it cancels out Ip at this summing junction.

Any non-zero voltage at this summing junction represents the error between Im and Ip and reducing this error is the primary goal of the entire MLP system. This error reduction is performed by three integrator circuits in the next section of the MLP circuit, but the large variations in probe currents ($0.01A < Ip < 2A$) require the error signal to be amplified by a variable gain. The need for variable gain error signal amplification is best demonstrated in the following scenario. First, Ip is measured at a level of 50 mV (remember currents are measured as voltages throughout this circuit) but the MLP system has not fully locked onto the correct signal and returns a scaled Im of 30 mV. In this case, the system has a significant error of 40% and the integrators would be set-up in a fashion to respond rapidly to a 20 mV error signal. However, the plasma soon changes and Ip is measured at 2 V while Im is calculated at 1.98 V. Now, a 1% error in mirror current corresponds to the same 20 mV error signal, which means only a slight adjustment in Im is actually needed. But since the integrators were previously optimized to be highly sensitive to a 20 mV signal, their rapid response at this high level of current would cause the system to go unstable. Similarly, if the integrators were instead optimized at the higher current levels they would not respond fast enough at the lower current levels.

For the error reducing integrators to truly be optimized, they must always be given the same signal level for a given error percentage. A solution to the scenario above would be to optimize the integrators to the large current levels and directly pass the error signal at these levels while

amplifying the error signal that occurs at the lower current levels in a way that is proportional to the measured ion saturation current. Thus, even though the low current error is 20 mV, it represents a 40% error so it would be amplified to 800 mV to reflect a 40% error at the high current level. The high current error, however, would be passed directly to the integrators as 20 mV since it is only a 1% error at that level. This setup is ideal because the integrators are optimized to one set level of current and all of the error signals generated throughout the range of currents are properly scaled to this level. All that is needed is for an amplification to be applied to the error signal that is proportional to the measured Isat level. It must be kept in mind, however, that the current level is not static as in the simple example above, but rapidly fluctuating with changes in the plasma being probed. Thus, it is imperative that the gain on the error amplification be dynamic enough to cover the entire range of currents in the system while also possessing the high bandwidth necessary to track the changes in current. These performance goals are met on the MLP Data board by the Variable-Gain Error Amplifier circuit.

The raw error signal is calculated at the summing junction where Im and Ip combine, which monitored by U28. The complex amplification outlined above is achieved primarily by two TI THS7530 300 MHz bandwidth, fully differential and continuously variable gain amplifiers [38]. These devices have a gain range of 4 to 200, which is controlled by an external voltage, Vg. The first of these chips (U16) takes in a differential version of the error signal and amplifies it based on the voltage on its gain level input (Vg). The error signal is then converted back to a ground referenced signal and is sent to the integrator circuits and the front panel so it can be digitized and recorded. The second THS7530 chip does not look at the error signal, but rather takes the Isat calculation from the MLP circuit as its input. The Isat signal is then amplified based on the same Vg signal that controls the error amplification. The gain for both chips is then set by U38, which compares the amplified Isat signal with a voltage set by R117 and R118 and adjusts Vg by negative feedback until both voltages are equal. Thus, the combination of U35-U38 is constantly monitoring Isat and altering the gain of itself in addition to the error signal amplification. The other minor features of this circuit include a copy of the auto zeroing circuit, which eliminates DC offsets in the error signal while the system is inactive. Also, two potentiometers (R1_VGA and R2_VGA) are used to fine tune the range and sensitivity of the gain calculation.

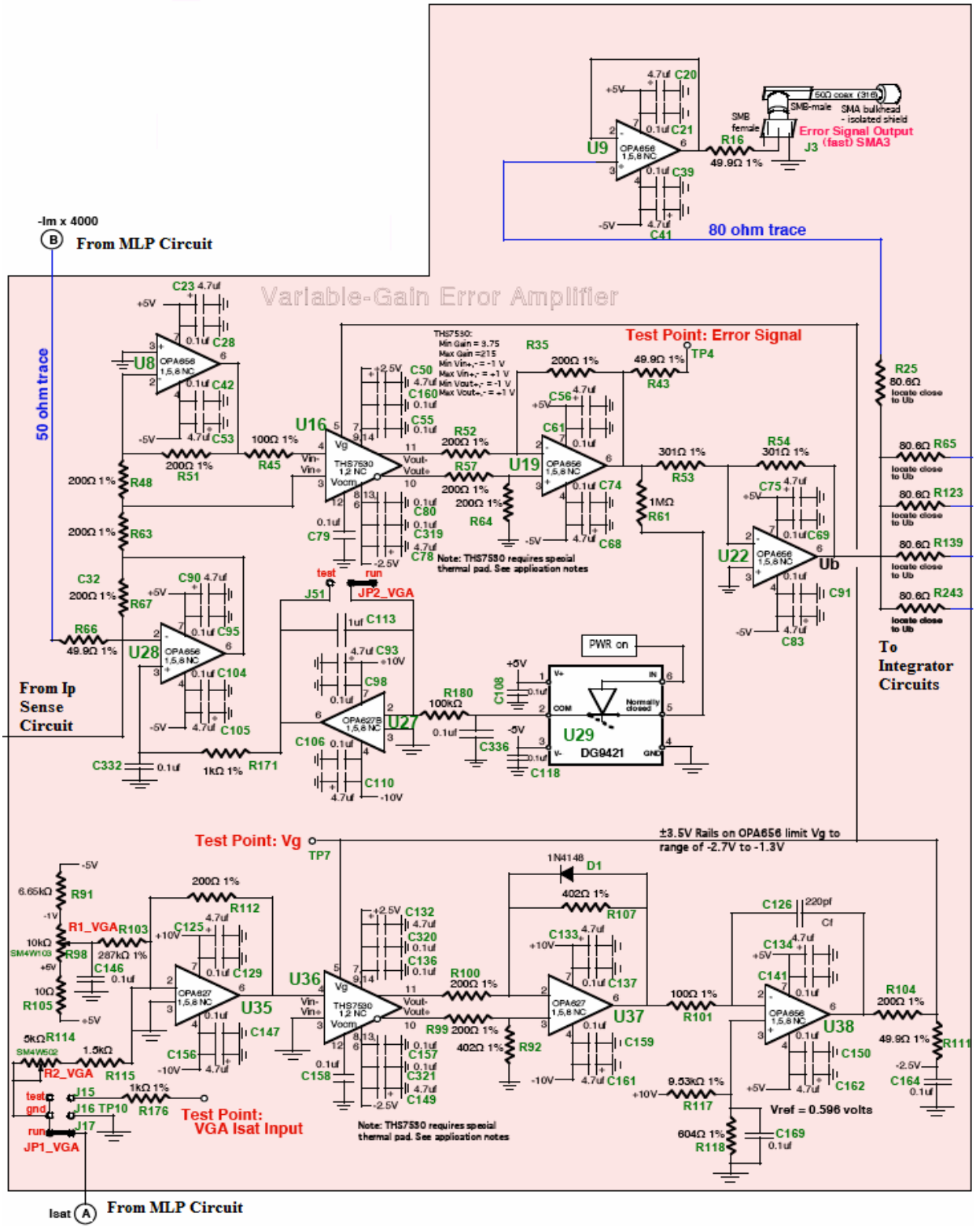


Figure 4.28 – Variable-Gain Error Amplifier Circuit

The processed error signal heads out to one of three different integrators depending on which state the voltage waveform is in. Although each integrator is slightly different, their overall operation and functionality are the same. Each integrator is connected to the error signal through a separate DG612 high-speed, low-glitch digital switch [30]. Each digital switch is controlled by one of the three Data Board TTL signals described in section 4.2.3. As discussed before, each Data Board TTL signal corresponds to one of the FET Bias TTL signals. Thus, when the waveform is in its negative bias state (TTL signal X), the error signal that is generated corresponds to the Isat calculation. During this time, the switch (U24) on the Isat integrator receives the signal to close (TTL signal J) and the circuit attempts to reduce the error signal to zero. As the Isat bias time period ends, the switch opens and the integrator is isolated from the error signal. The Isat integrator then holds the last value calculated across its capacitor (C12_TH) until the switch closes during the next Isat bias state. Meanwhile, the voltage waveform switches to the positive bias state, which corresponds to the Te calculation. The Te integrator then goes through the same process as Isat after its switch is closed by a high TTL signal 'L'. Similarly, when Te's integration period is over it is isolated while the Vf integrator works through the same procedure. The entire processed is repeated while the MLP system is active.

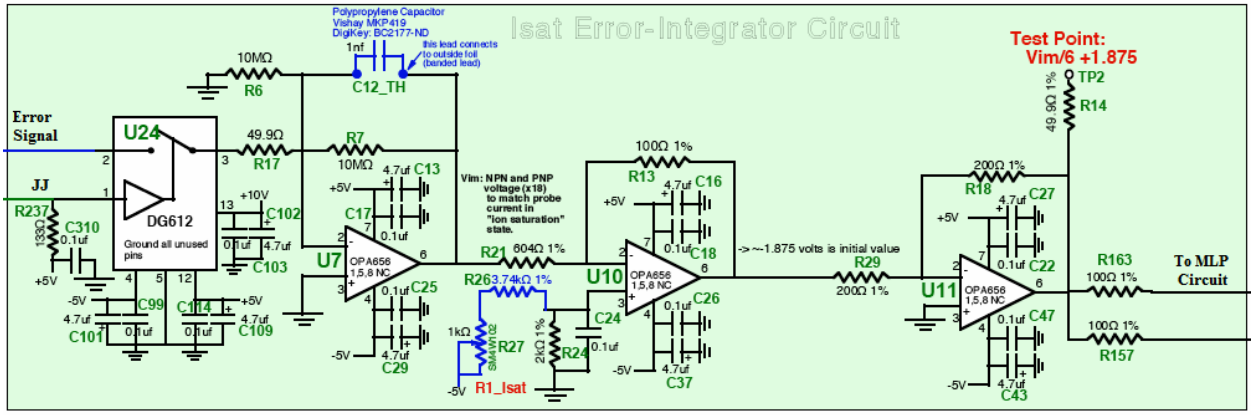


Figure 4.29 – Isat Error-Integrator Circuit

When a particular switch is closed, it creates a feedback loop through the corresponding integrator circuit. In the Isat case, a feedback loop is created from the summing junction, through the error amplifier, Isat integrator and MLP circuit at which point Im is altered and sent

back to the summing junction. The primary adjustment parameter for this feedback loop is the value of the capacitor in the Isat integrator (C12_TH). The sensitivity of the Isat integrator to the error signal is set by the value of this capacitor. Thus, this capacitor was designed to be one of the few through-hole devices on the board in order to make changing values easier during bench testing (this was done in the other integrator circuits as well). Furthermore, the voltage across this capacitor contains the raw information on Isat and can be viewed as the Isat memory module. To ensure that dielectric soakage would not affect the voltage on the capacitor, MKP-419 high precision poly-propylene capacitors were used [30]. Finally, the potentiometer (R1_Isat) is used to set the quiescent (power off), initial level of 0.030mA for Isat in the MLP system.

The other two integrators are different from Isat in two areas. First, the voltage stored on their capacitors represent output data (-Vf/100 and -10/Te). Thus, their values are buffered and sent to the front panel. The second difference has to do with the need to further scale the error signal according to the value of Te. As discussed in Chapter 3, the MLP system measures three data points along the I-V characteristic. The value of Isat is calculated directly from one the measured data points due to the ion saturation period occurring at the flattest part of the I-V curve. The other two measurements, which are the voltage at which probe current is near zero for Vf and where the slope of the I-V characteristic is steep for Te, must take into account the most recent Te calculation (i.e. the curvature of the I-V characteristic) in order to respond properly to the newest error signal. To account for this, the error signal is scaled once more before reaching the integrating capacitor of both circuits. Both circuits use the most recent Te calculation to set the resistance level across a 2N4392 JFET (Q4 for Vf and Q5 for Te) [30], which have a pinch-off gate threshold voltage of ~ -4V. In this set up, the JFET acts as an adjustable resistor which has its resistance increase for high values of Te and decrease for low values [18].

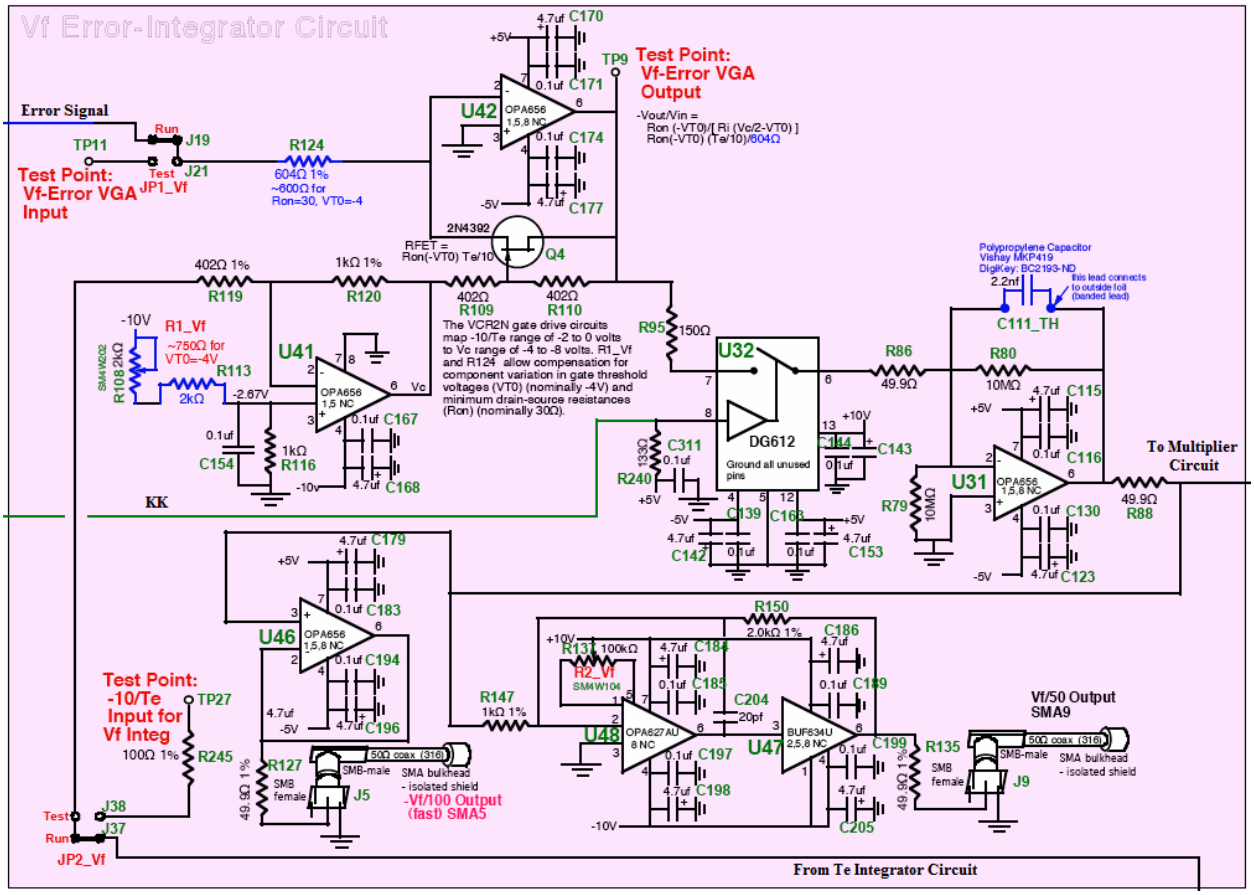


Figure 4.30 – Vf Error-Integrator Circuit

The JFET adjustable resistors are used differently in the Vf and Te integrator sub-circuits. Although both JFETs are setup to respond to Te in the same manner, the Vf integrator becomes more sensitive to the error signal with a high Te, while the Te integrator becomes less sensitive. This is accomplished by the different placement of the JFETs. In the Vf circuit, the JFET is placed in the feedback of and op amp (U42). Thus, as the resistance of the JFET is increased, so is the gain on the error signal in a manner proportional to Te. In the Te circuit, the JFET is placed in series with the error signal. In this case, an increase in resistance causes less of the error signal to reach the integrating capacitor, which in effect reduces its sensitivity to the error signal in a manner proportional to 1/Te.

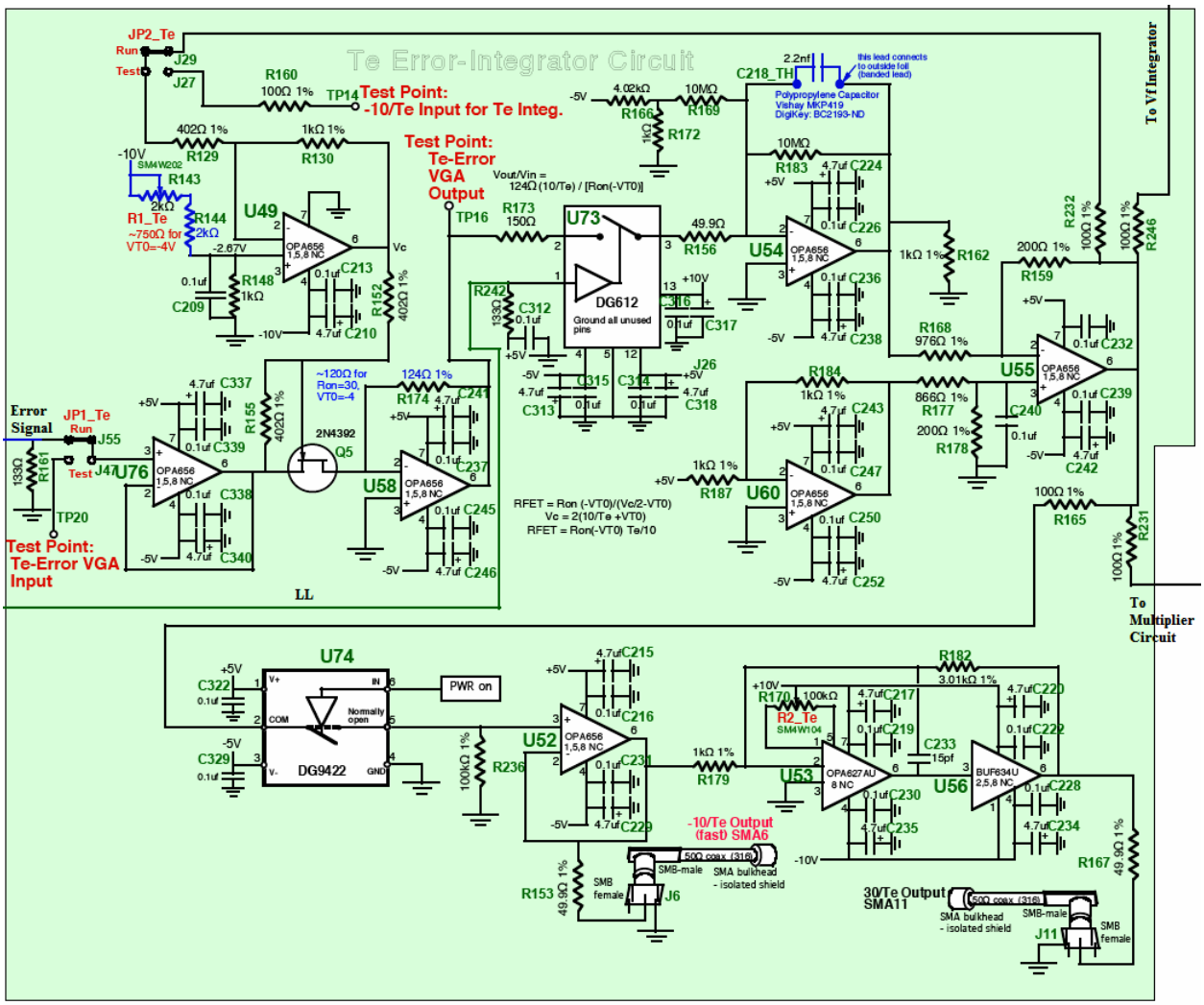


Figure 4.31 – Te Error-Integrator Circuit

Some final points worth mentioning include the resisters and potentiometers that are used to fine tune the circuit based on the threshold voltage of the JFETs. The threshold voltage of each JFET is measured on the bench. Only those with threshold voltages near -4 volts are used. Resistors R124 and R174 are set to correspond to the resistance of the JFET when Te = 10eV. R1_Vf and R1_Te are used to fine tune the control signals to the JFETs relative to their threshold voltages. Jumpers JP1_Vf, JP2_Vf, JP1_Te and JP2_Te allow adjustments to be made so that the proper gain proportionalities are achieved (proportional to Te for Vf error, proportional to 1/Te for Te error). Additionally, each circuit has its initial value set differently. In the Vf circuit, the initial value is set to zero by R79, which removes the charge on the capacitor over long time scales. In the Te circuit, op amp U60 is set to its negative rail by tying its input to the +5 V supply.

Resistors R168, R177 and R178 were then chosen to set the maximum value for Te at 120eV, which occurs when U54 also hits its negative rail. The minimum value of Te of 7eV occurs when U54 hits its positive rail. Resistor R183 force the Te integrator capacitor voltage to zero during quiescent periods, yielding an "initial value" of Te = 10eV. The outputs of both integrator circuits go to the multiplier circuit and combine with the probe voltage (Vp) in the manner described before. These represent the final two feedback signals of the MLP circuit.

The final section of the MLP Data circuit concerning the error signal is the sample and hold circuits. This section is made up of three standard sample and hold circuits that are all connected to the error signal through separate digital switches. Each switch is connected to one of the three Data TTL signals that control the integrators. Thus, when one of the TTL signals goes high, the switch closes and the error signal for the corresponding integrator is outputted to the front panel and recorded. When the switch opens, the capacitor holds the last recorded value until the switch closes again. With the error signal of all three integration time periods being recorded, an accuracy measurement can be obtained for the plasma parameter values being calculated by the circuit. During times when the error signal is high, the corresponding parameter value can be ignored. High precision poly-propylene capacitors are used in all sample-and-hold circuits.

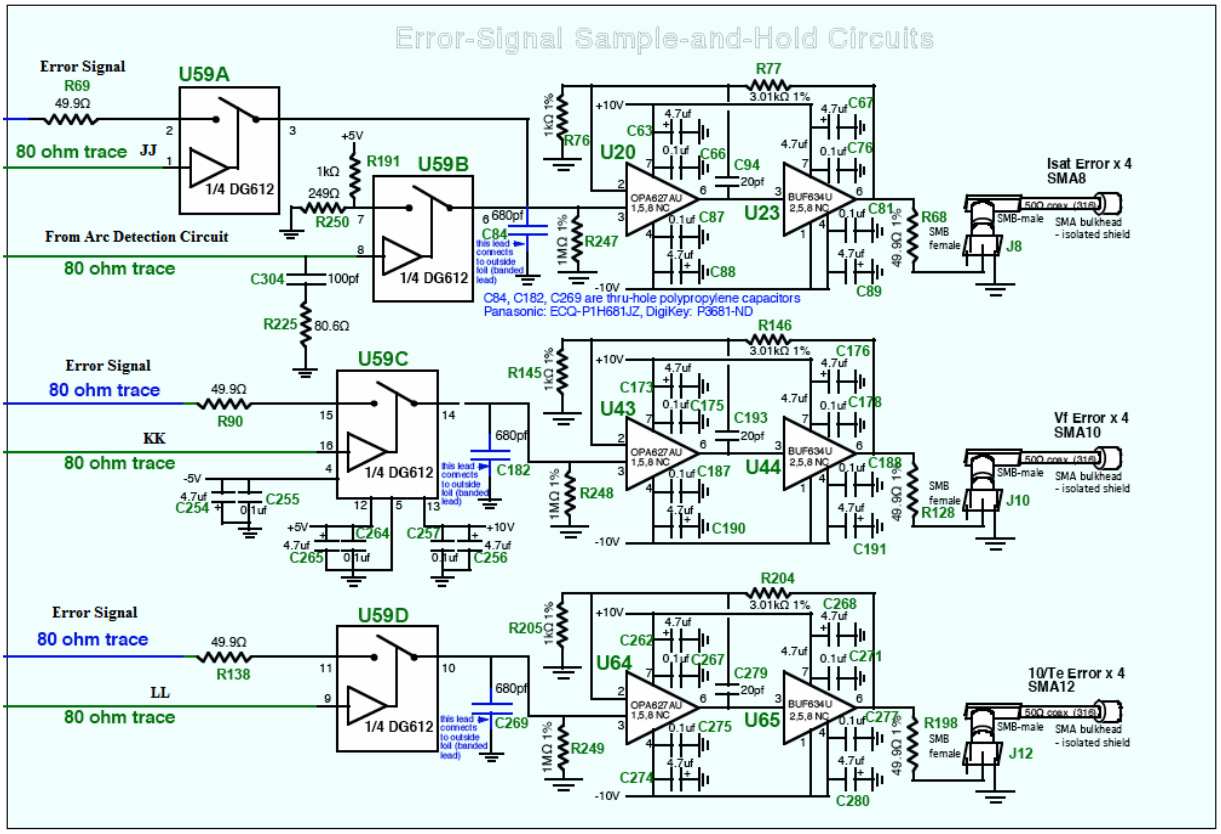


Figure 4.32 – Error-Signal Sample-and-Hold Circuits

One may argue that these circuits are redundant since the error signal is already being sent to the front panel. It must kept in mind, however, that the final (planned) implementation of this board will only output the buffered readouts of the three parameters and well as the corresponding sample and holds. Most of the other signals being sent to the front panel, including the direct error signal, either require a 50 MHz digitizer to be usefully recorded or are meant for diagnosis or testing purposes only. Also, the error signal is only of interest during integration time periods and recording the entire signal is a waste of digitizer storage.

The final features of the MLP Data circuit include the FET Switch Drive and the Probe Bias Amplitude circuit. The principal function FET Switch Drive circuit is to invert the TLL signals received from the backplane. These driver chips also help clean up the TTL signals as they can pick up noise when traveling through the backplane and connectors from the TTL Generator. Also, a simple arc detection system was implemented here using an AD8564 high-speed analog comparator (U45) [36]. This chip monitors the Ip measurement and disables all of the TTL

signals when a current greater than 2.0A is detected. It also rails the Isat error-signal sample and hold output to indicate that an arc was detected.

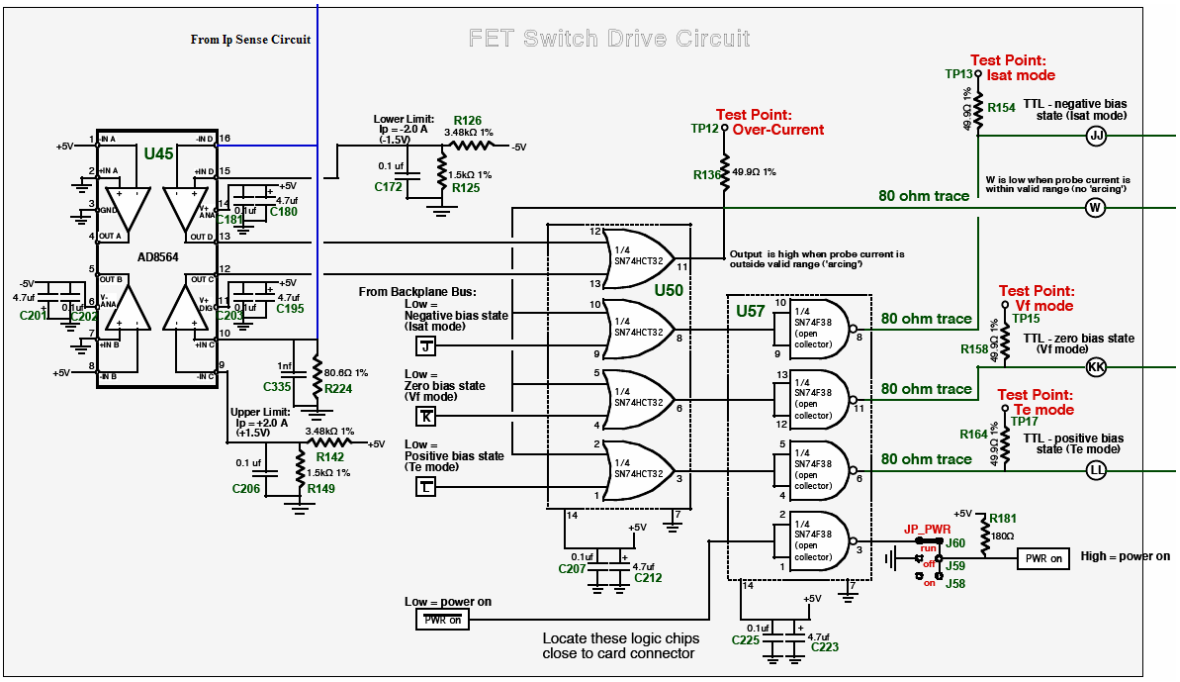


Figure 4.33 – FET Switch Drive Circuit

The final circuit is the Probe Bias Amplitude circuit. This circuit connects to the output of the Multiplier circuit and generates the bias signal that is sent to the FET board. Some important features here include the RC on the front end and the unique diodes. The high-pass RC on the front end removes low-frequency components since this circuit is only interested in determining the peak-to-peak signal amplitude. The 1PS70SB85 (D3) and 1PS70SB86 (D2) planar Schottky barrier diodes [37] are combined with an op amp to separate the multiplier signal into a maximum and minimum voltage signal, which is then sent to the FET board. These are fast, "hot carrier" diodes with low forward voltage drop. The arrangement shown below eliminates this forward voltage drop on the output signals of U68. The output of the circuit is {(max(Vp) – min(Vp))/Te}, which is feedback controlled to have a time-averaged value of ~ 3V by the FET drive board.

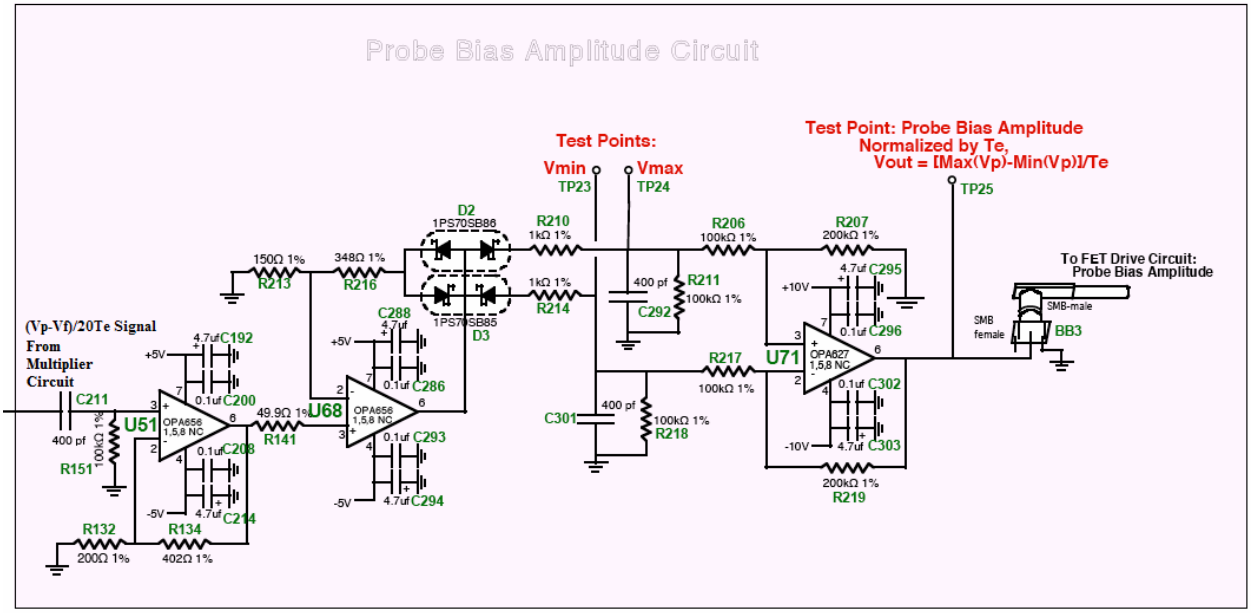


Figure 4.34 – Probe Bias Amplitude Circuit

4.4.2 – MLP Data Circuit Layout & Optimization

The use of so many high frequency signals and components on this board made a proper layout crucial to performance. A six layer board with all surface mount components (except where specified) had to be utilized here to ensure that a proper layout/performance was achieved. This careful layout started with the Ip & Vp sense circuit whose fine tuning was already discussed above. The Ip and Vp signals make their way to the error signal amplifier circuit either directly (in the case of Ip) or indirectly through multiplier, MLP and Im calculating circuit (in the case of Vp). Thus, these signal paths are the most important in the circuit and are the most highly optimized. All traces and components associated with these paths have all ground and power planes removed around them and no other signals are allowed to cross their paths on other layers. Trace lengths between components in these signal paths are minimized and in most cases the components are placed as close together as possible.

After the layout of the above signals was complete, the second most important signals were addressed, which are made up of the error signal and the signals that go through the three integrators. The ground and power planes were also removed from the traces and components in these sections. However, since the signals described above were a higher priority in terms of

layout, this left the error amplifier circuit relatively far away from the integrator circuits. To accommodate this distance, the error signal traces were made to match 80 Ω and were properly terminated at both ends of the trace with a resistor.

The remaining sections were not in need of special placement or layout and were placed in the remaining free space areas of the board. The only exception to this was the FET Switch Drive Circuit which was placed adjacent to the data signal backplane connector. The TTL signals from this circuit were also made into 80 Ω traces to ensure that no reflections on these lines would trigger the digital switches that connect to these lines. Rounding out the layout of this board was a shield placed over the Ip and Vp sense circuit to minimize outside interference and another shield coving the entire back of the board to better insulate the sensitive Data board from the noisy FET board.

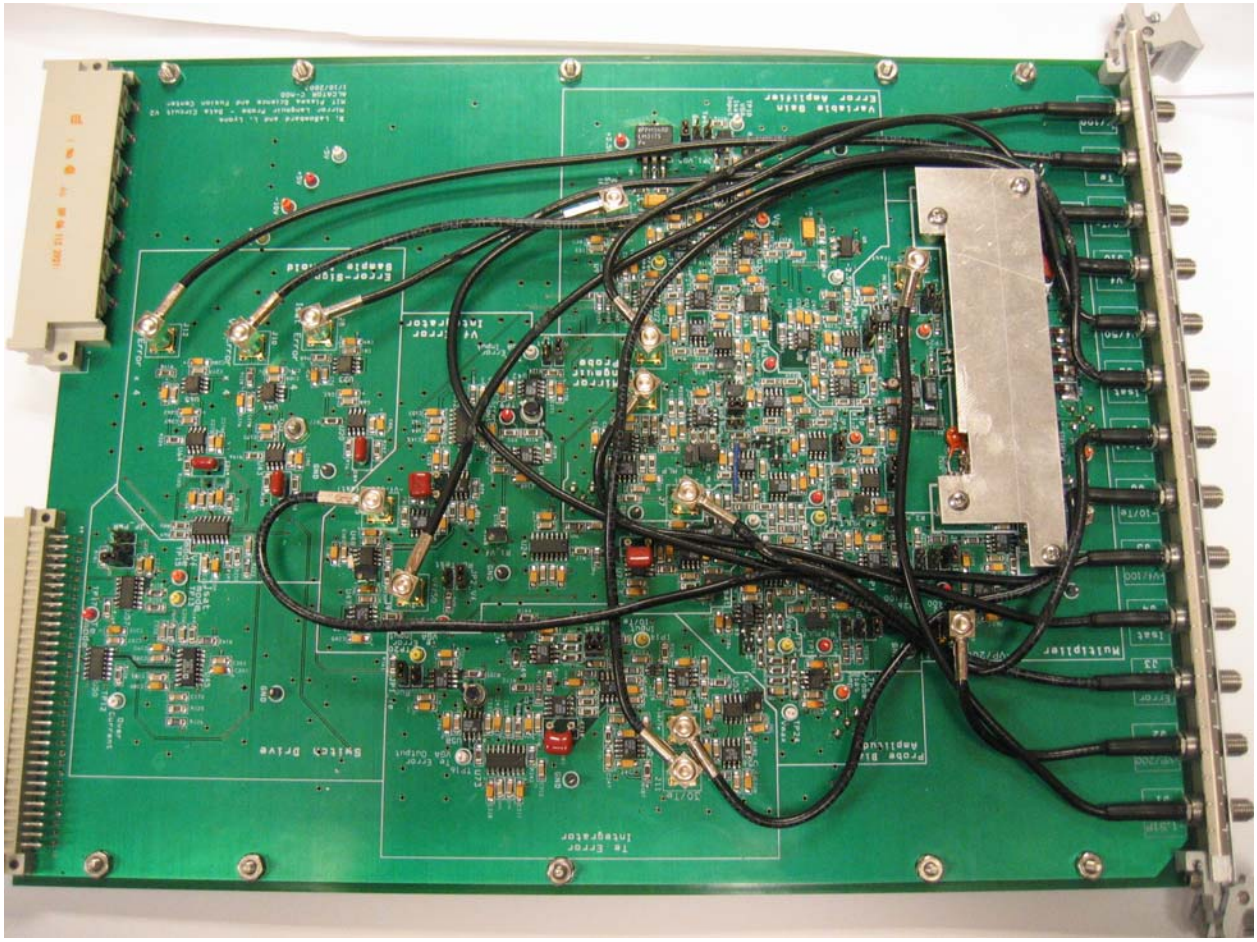


Figure 4.35 – MLP Data Board with Shield

4.3.3 – MLP Data Performance

Unlike the other two boards, the MLP Data board has no crucial tests that could be performed individually. The MLP Data board represents the brain of the entire MLP system and the only way to properly test it is to use it as an entire system with the FET drive board and TTL waveform generator. The bench testing and subsequent real plasma testing of the system is covered in the following chapters.

Chapter 5 – MLP System Bench Performance Tests

Before presenting the data obtained from the MLP system, the term "bench testing" must be properly explained. As mentioned several times in this paper, the MLP system was designed to operate in the conditions typically found in the edge of plasma-fusion confinement devices. To properly test the MLP system, a set-up is required that provides these conditions in a controlled environment. The ideal arrangement would be to have unlimited access to the Langmuir probes on Alcator C-Mod where the system can be optimized in its designed environment. Although promising in theory, this arrangement is severely constraining for many reasons including a limited run schedule (C-Mod only runs 15 weeks a year), limited plasma availability during active runs (C-Mod produces a maximum of 30 plasmas, 2 second duration, during a run day) and extensive periods of downtime (~10 minutes) between plasmas while C-Mod's magnets re-cool. Furthermore the MLP system would have to be installed in the C-Mod experimental cell which is locked down during run days, meaning changes can only be made to the system once a day.

While using C-Mod is possible, it would most likely take an entire run campaign to properly test and optimize the MLP system. Another option may be to utilize another plasma creating device and install a Langmuir probe onto it. This too proves to be a dead-end since the temperatures and ion saturation levels required are simply not found outside of fusion level plasmas. Thus with no real plasma solution to this testing problem, the only option left is to create a device that mimics the I-V characteristic behavior of a Langmuir probe in a magnetically confined plasma. This was accomplished on the MLP system through the use of a fourth circuit board called the Electronic Langmuir Probe (ELP).

5.1 – Electronic Langmuir Probe Overview

Although the ELP served an important function in the testing phase, it is not technically a part of the MLP system and thus was not described in the previous chapter. Likewise, it will not be covered in great detail here since the data obtained through the use of the ELP is much more

relevant to this thesis than the precise functionality of this circuit. With that said, the ELP is based on the same theory as the MLP Data circuit in that it uses RF transistors to mimic the response of a Langmuir probe. The key difference with the ELP, however, is that the voltage signals applied to the transistors are manually controlled to generate a predictable current response. The ELP uses specific resistor values, which can be selected through the use of a jumper, to change the Langmuir probe behavior that is trying to be emulated (i.e. double the ion saturation current or change the floating potential). Furthermore, once a particular resistor is chosen it can be tied to +5V, -5V or ground through another jumper, which introduces additional changes in the I-V characteristic. Finally, three digital switches are used on the ELP to rapidly change the I-V characteristic via a TTL signal.

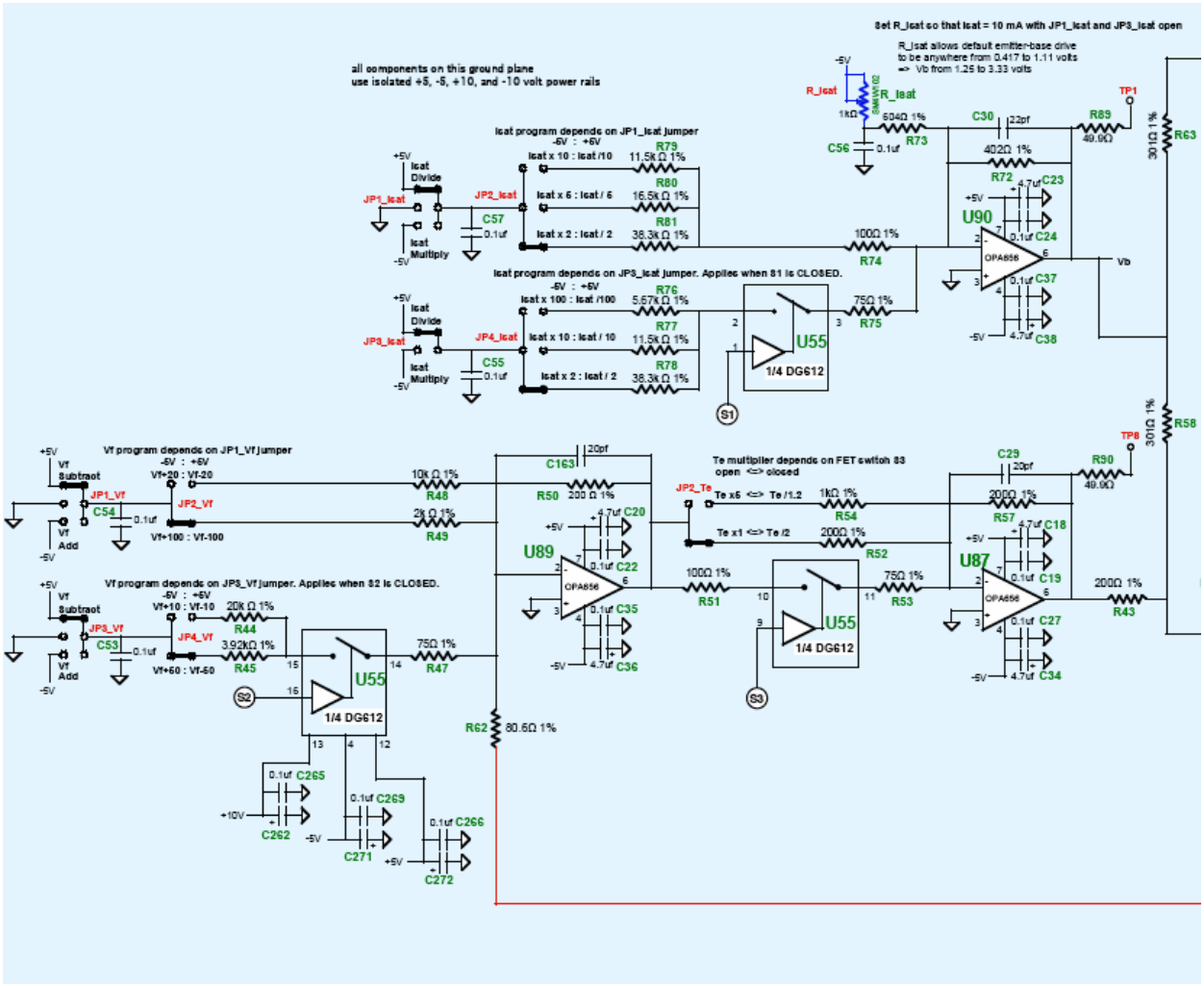


Figure 5.1 – Various Adjustable Parameters on Electronic Langmuir Probe Circuit

Once a particular parameter set is targeted, the jumpers are set accordingly and the voltage is applied to the transistor stage of the ELP. The key point to grasp here is that this voltage signal has static, predetermined values for ion saturation, floating potential and electron temperature factored into to it whereas the voltage signal on the MLP Data board uses its internal, calculated values for the three parameters to set the voltage. Thus, when the MLP Data circuit has locked on to the ELP, its plasma parameter outputs should be the same as the preset values on the ELP.

The last crucial point to mention on the ELP is how it obtains its drive voltage. As mentioned in the MLP theory, the voltage applied to the transistors is a function of probe voltage (Vp on the MLP Data board). To provide this signal, the FET Drive board has an additional output called Probe Drive Voltage, which is only used during ELP testing. This drive voltage raises an additional problem since the ELP components must be able to operate over the full bias range of the FET output. While this signal is needed to generate the three stage response current, the range would be too great if it were referenced to ground. Thus, a solution was obtained by creating an isolated ground which all components reference. This isolated ground is then driven by the FET Probe Drive. Thus, the components "ride" along at the various bias levels as they generate the proper current signal. The output of this circuit is then connected to the Langmuir probe connector on the FET Drive board much like a real probe. Finally, please note that many pairs of NPN and PNP transistors operate in parallel in the ELP so that the high levels of current can be generated when necessary.

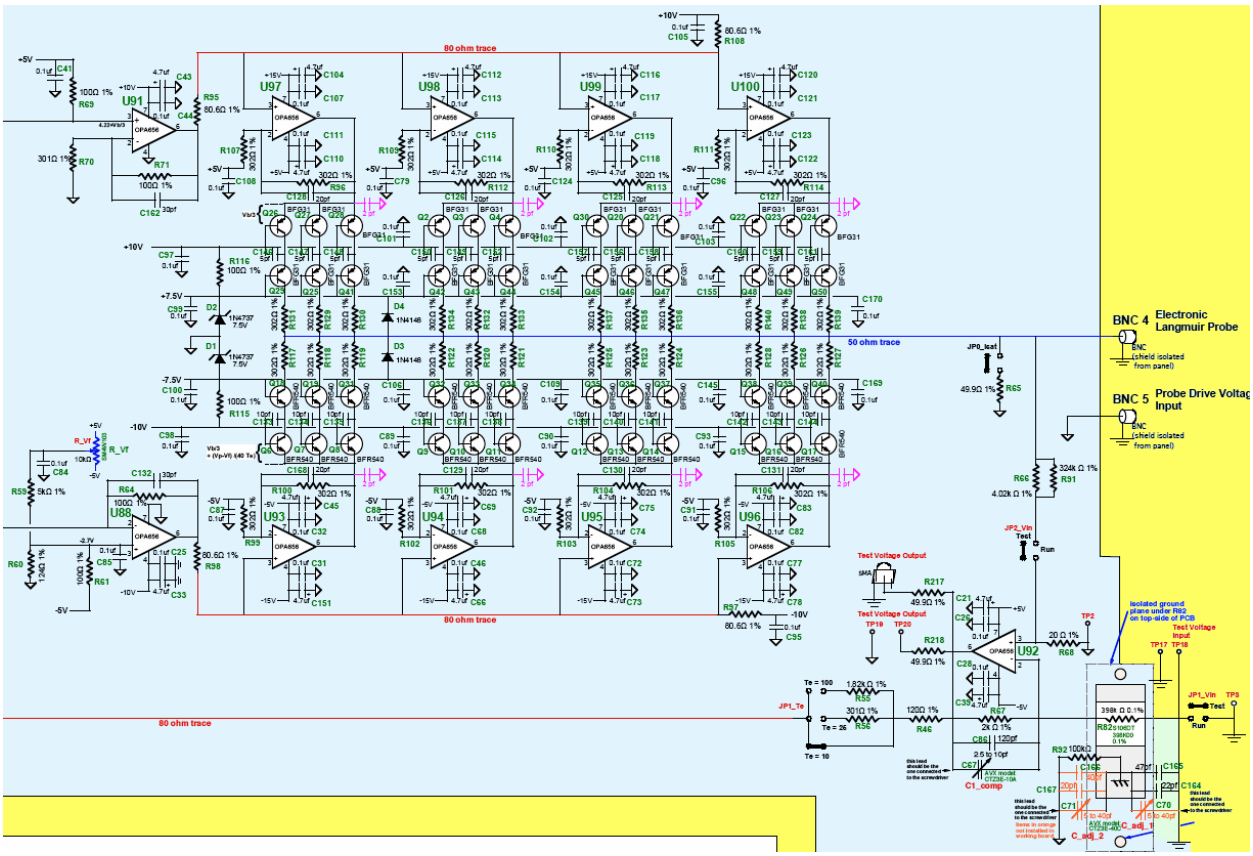


Figure 5.2 – Transistor Core of Electronic Langmuir Probe Circuit

5.1.1 – Electronic Langmuir Probe Drawbacks

Although the theory behind the operation of the ELP is sound and was proven so in PSpice simulations, the actual implementation was met with difficultly. The principle problem came from the fact that all PSpice testing was done using parallel transistors that are all exactly the same in the software. In reality, the transistors have minor differences in threshold voltages or intrinsic capacitance that cause the circuit to be unstable. The intended direct control of the plasma parameters using the jumpers proved to be inaccurate and the circuit was only stable for only a limited set of jumper settings. Also, in this limited parameter space, a FET bias greater than +/- 50V would cause instability in the circuit, which limited its usefulness further. Finally, the 900 ns period waveform proved to be too fast for the ELP to handle, so the waveform was generated at 1/5 speed to ensure proper operation. Some of this instability proved to be useful as the ELP would rapidly (and randomly) change its parameter set, which the MLP system would then track. In most instances, however, the lack of control on the ELP did not allow the MLP

system to be tested over all the designed ranges of operation. Despite all of these drawbacks, the ELP was found to be adequate for the basic testing of the MLP system and, as will be discussed in Chapter 6, running the system on an actual plasma provides challenges that a fully functional ELP would not have provided anyways.

5.2 – MLP Performance Test – Static Parameters on ELP

Once a proper testing environment was made available with the ELP, the MLP system was optimized and benchmarked. To start off, the ELP was set with its most stable parameters (Te = 10eV, Isat = 20mA, Vf = 0V) and a test shot was taken. The outputs of interest from the MLP system were selected as Probe Voltage, Probe Current, Error Signal, Ion Saturation, Floating Potential and Electron Temperature. One important point worth noting is the process by which the system was benchmarked. Since the ELP was neither accurate nor reliable enough to use its own parameter values for comparison to the MLP outputs, two software based benchmarks were developed. These algorithms post-process the voltage and current signals and calculate the resultant values of Isat, Vf and Te using two different methods. The first algorithm (referred to as M1) uses equation 2.9 at the three different bias levels to solve for the three unknowns with three equations. In principle, this algorithm can follow fast changes in Isat, Vf and Te and can be compared to the iterative process of "finding the solution" that is implied by the real circuits. The second method (M2) operates in the same manner as the real circuits by iteratively changing one parameter at a time. Thus, the outputs from the circuit should perfectly overlay with the M2 outputs under ideal conditions. For more information on the post-processing algorithms, please refer to Appendix B. The outputs of the MLP system are overlaid with the computed values from M2 in Figure 5.3.

The inherent instability of the ELP circuit is shown over the duration of this performance test. However, having these random changes in parameter values is actually an added bonus since a real plasma will never be static for any extended period. It is clear from this shot that the MLP system is outputting values that precisely overlay with the M2 computed values. This long time scale view is too broad to show the individual iterations of the integrator circuit updating the values. Thus, Figure 5.4 highlights a narrower time window where the individual updates of the various integrators can be observed.

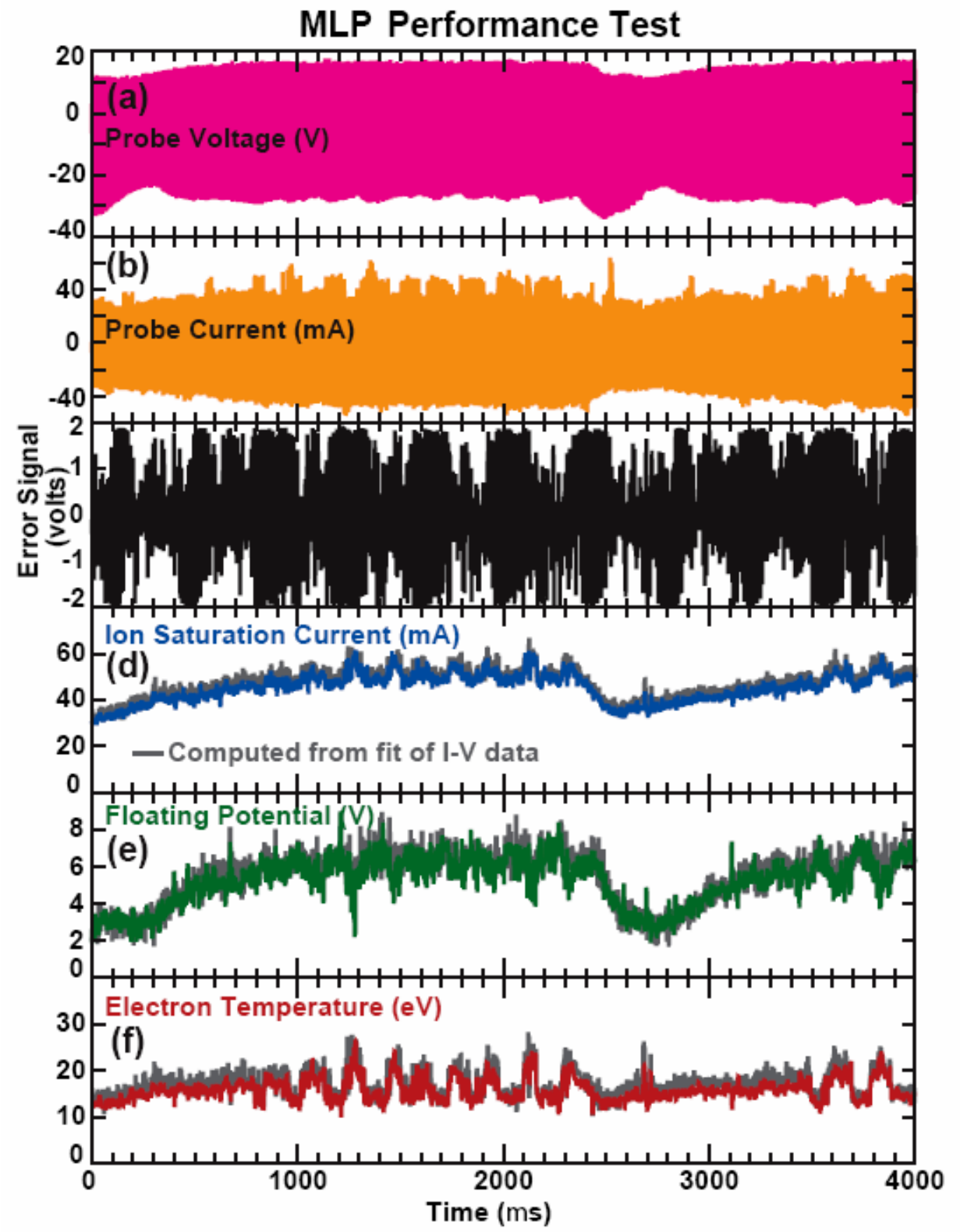


Figure 5.3 – Static ELP Test – Long Time Scale

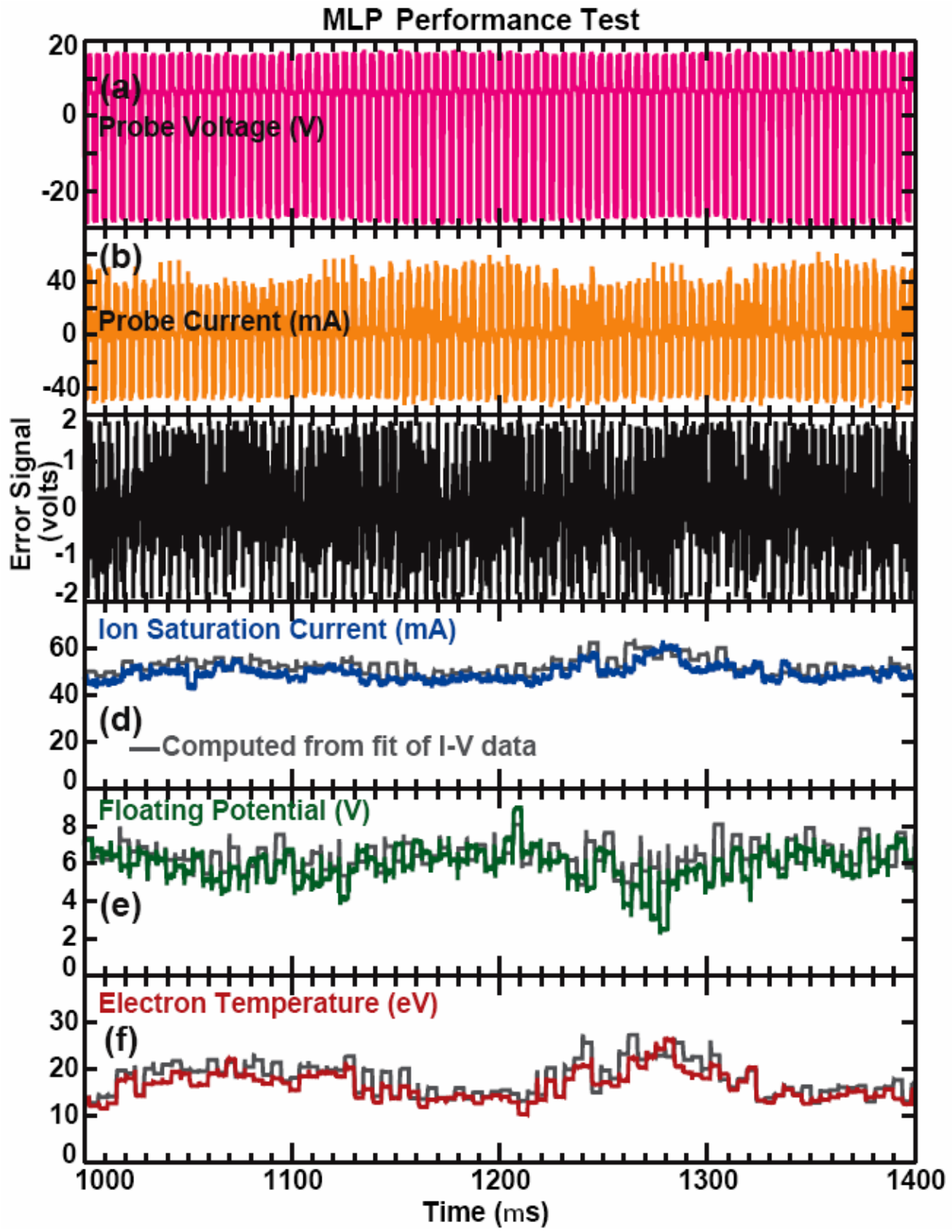


Figure 5.4 – Static ELP Test – Medium Time Scale

At this level of detail, it can be observed that the M2 computed values of the three parameters are noisier than the values outputted by the MLP. This illustrates one of the key advantageous of the real-time measurement compared to a post-processed calculation. This discrepancy arises from the fact that the voltage and current signals that are used to compute the parameter values are subject to additional noise as they make their way from the MLP Data board to the digitizers. The MLP Data board also uses these signals but obtains them directly on the board, which is the cleanest possible signal. Regardless of this discrepancy, the MLP and computed values continue to overlay with excellent agreement.

As a further investigation of this "static" test, the output data is viewed on a time-scale of a few iterations to see if the MLP Data board is updating its parameters during the appropriate stage of the voltage waveform. At the time period selected in Figure 5.5, the adjustments made by the integrators can be seen as small "bumps" on the signal level. These changes indicate that the circuit is locked onto the correct set of parameters and is only making negligible adjustments. Further evidence of a good lock is shown by a near-zero error signal during the periods of time when one of the integrators is engaged. While the error signal as a whole looks large and noisy, it is important to remember that the error signal is only relevant during periods when the voltage waveform and probe current signals have settled to a constant value and one of the integrator switches has been closed. During these time periods, a near-zero error signal is evident.

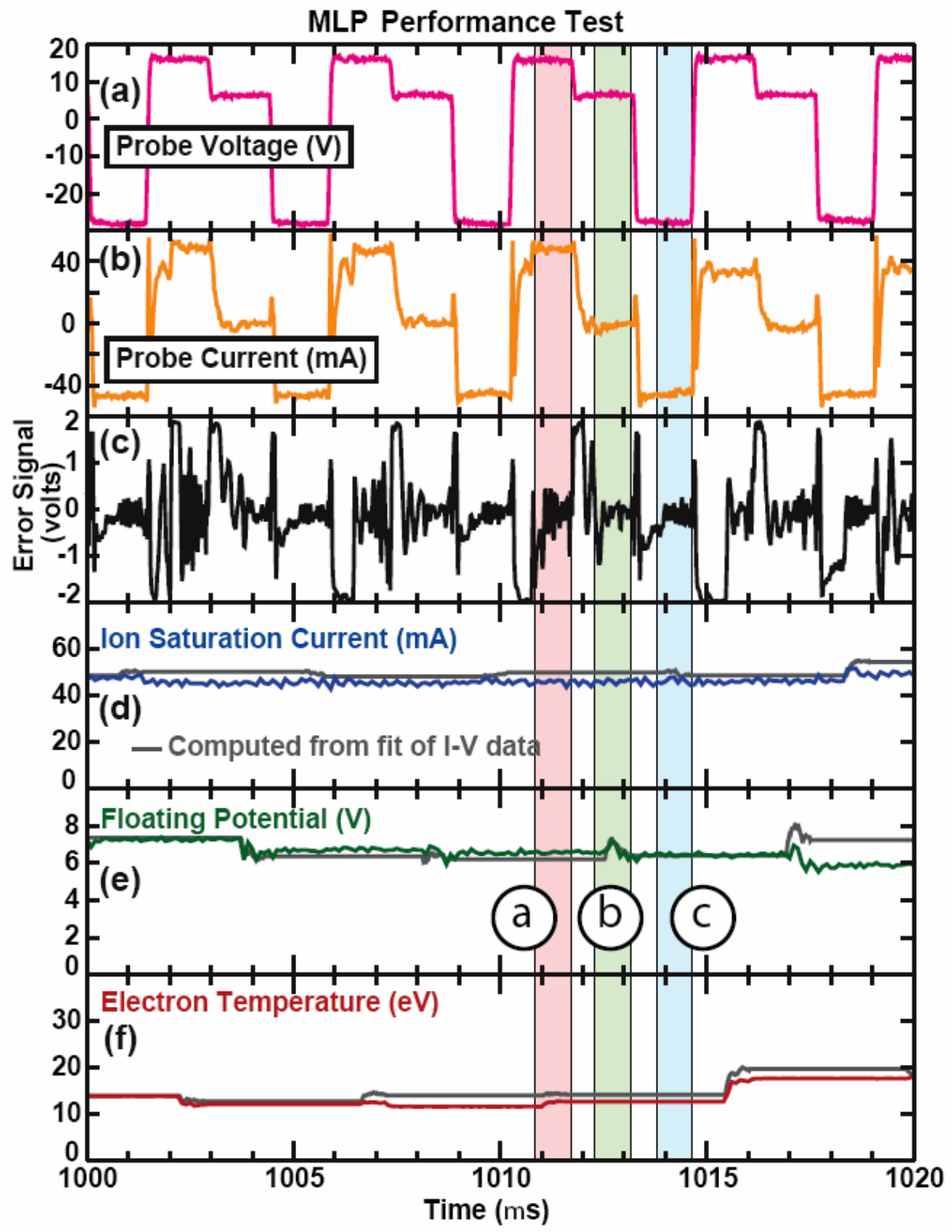


Figure 5.5 – Static ELP Test – Small Time Scale

5.3 – MLP Performance Test – Variable Parameters on ELP

With a fully functional ELP, the entire parameter space could be investigated to observe the locking ability at different levels. Unfortunately, moving outside of the parameters used in the test above causes the ELP to no longer emulate a plasma-immersed Langmuir probe. The only other test that proved to be useful on the ELP was to use the TTL switching of the Te parameter. In theory, this signal would only toggle Te between two values, but actual operation found that the other two parameters (Isat and Vf) were also affected. Again, while the ELP was not designed in this manner, the end result was useful because it created a worse case scenario where all parameter levels undergo a substantial change at the same time. Even with these extreme changes, however, the MLP system appears to be able to track all values and to obtain results similar to the M2 calculations seen in Figure 5.6.

To investigate the variable parameter performance in more depth, the output waveforms were studied during the short time-scale periods of rapid change. In Figures 5.7 and 5.8, an upward and downward going change is observed along with the output for the M2 algorithm. It is evident that the system is returning excellent results and is able to track these changes in real-time while doing so. In figures 5.9 and 5.10, the M1 post-processed data is overlaid. In these figures, the difference between the two algorithms can be seen. The M1 algorithm does not follow the same path as the circuit output, but rather is able to change all three parameters at the same time. However, within 4 iterations (20 μs) on the circuit, the real-time and post-processed outputs are in agreement. It must be kept in mind that the circuit is operating at 1/5 speed in these tests and in under normal operating conditions there would be five times as many iterations over a set period. Thus, it is believed that the circuit will be able to track the M1 algorithm better at full speed and will require less time for the two parameter outputs to overlay after similar step changes occur in a real plasma.

A final point to mention is in regards to the error signal, which is large during the periods of change. This signal, once again, acts as a primary indicator as to whether the system has locked on to the correct parameter values or not. Furthermore, it is only valid during the second half of each bias state when the MLP integrator switches are closed. All of these Figures illustrate how the current and voltage signals must be stabilized for a given bias state before the integrator

switches can close. If this timing is incorrect, the error signal will contain noise and the parameter values will not be calculated correctly.

With the ELP incapable of functioning at high levels of Isat or higher levels of bias, the performance testing of the MLP system was severely limited. While these limitations may suggest that the ELP was a failure, it must be emphasized that ELP proved its worth during a crucial time – the initial diagnosis and optimization period. During these periods of development, the exact parameters of the ELP were not important so long as its I-V characteristic behaved as a Langmuir probe. It was here when a quick source of data was needed that the ELP really benefited this project.

With the limits of the ELP pushed as far as possible, the only remaining option was to install the MLP system inside of the C-Mod experimental cell and prepare to obtain real plasma data. The initial data obtained from C-Mod using the MLP system is presented and discussed in the following chapter.

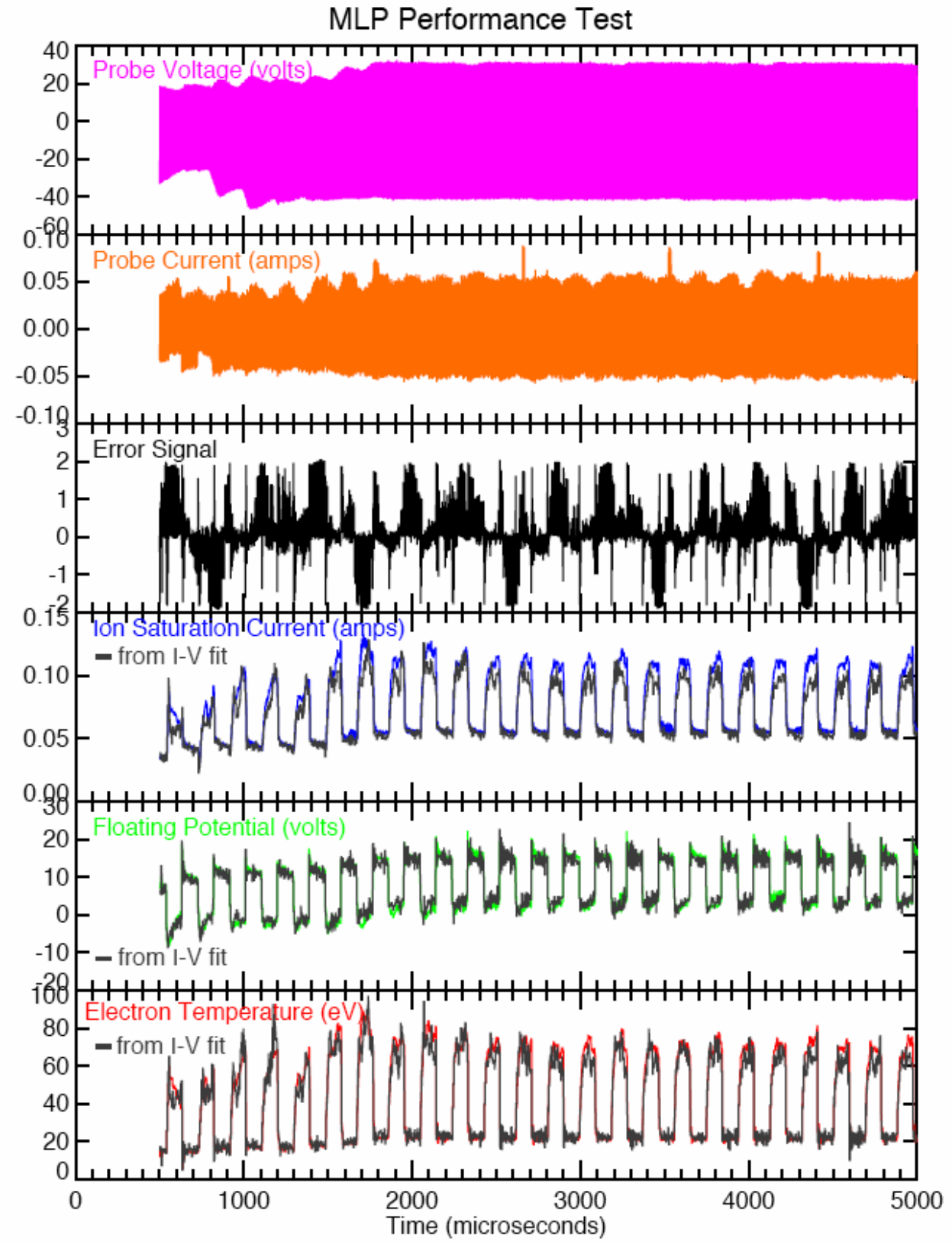


Figure 5.6 – Variable ELP Test

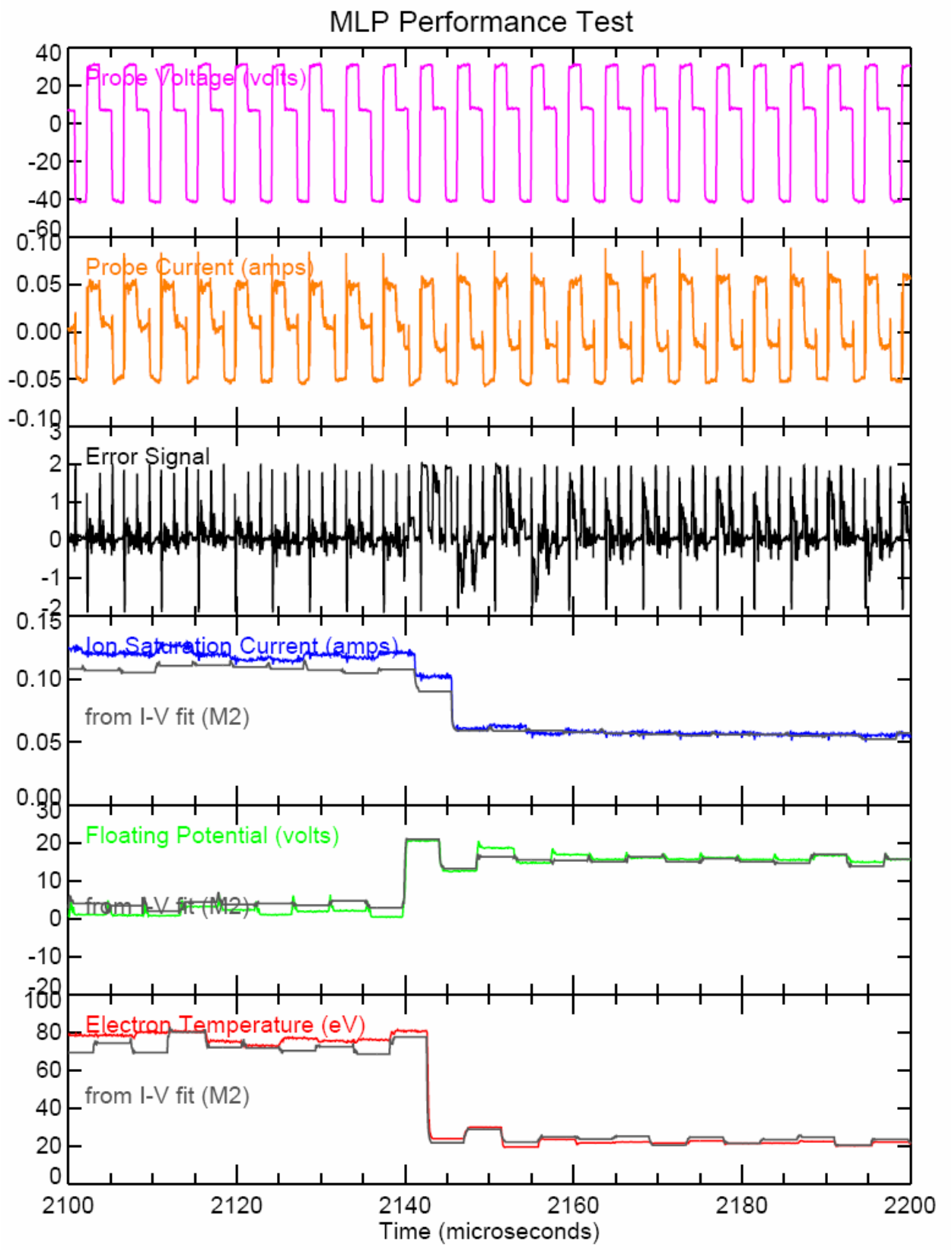


Figure 5.7 – Variable ELP Test – Small Time Scale with M2 Output

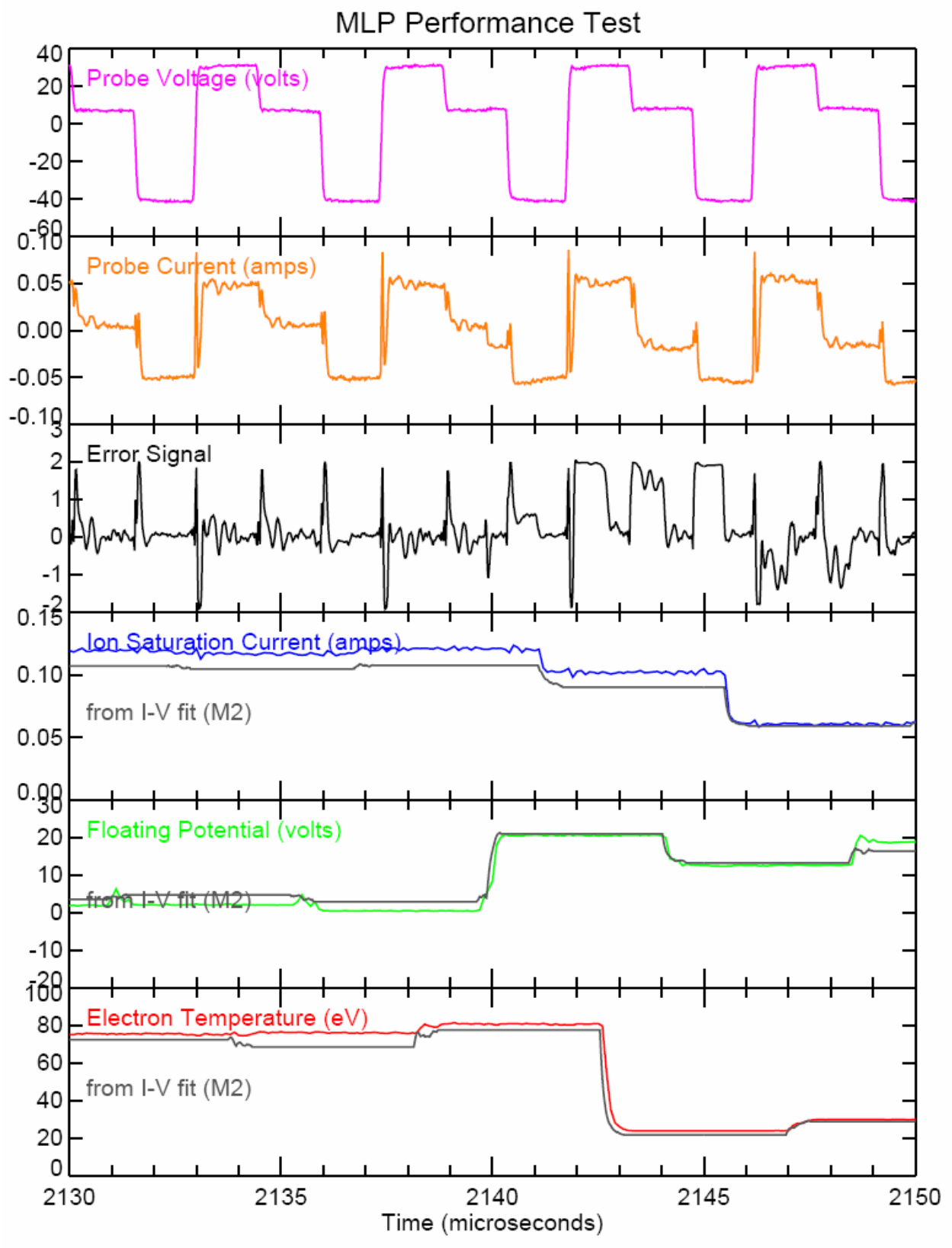


Figure 5.8 – Variable ELP Test – Smaller Time Scale with M2 Output

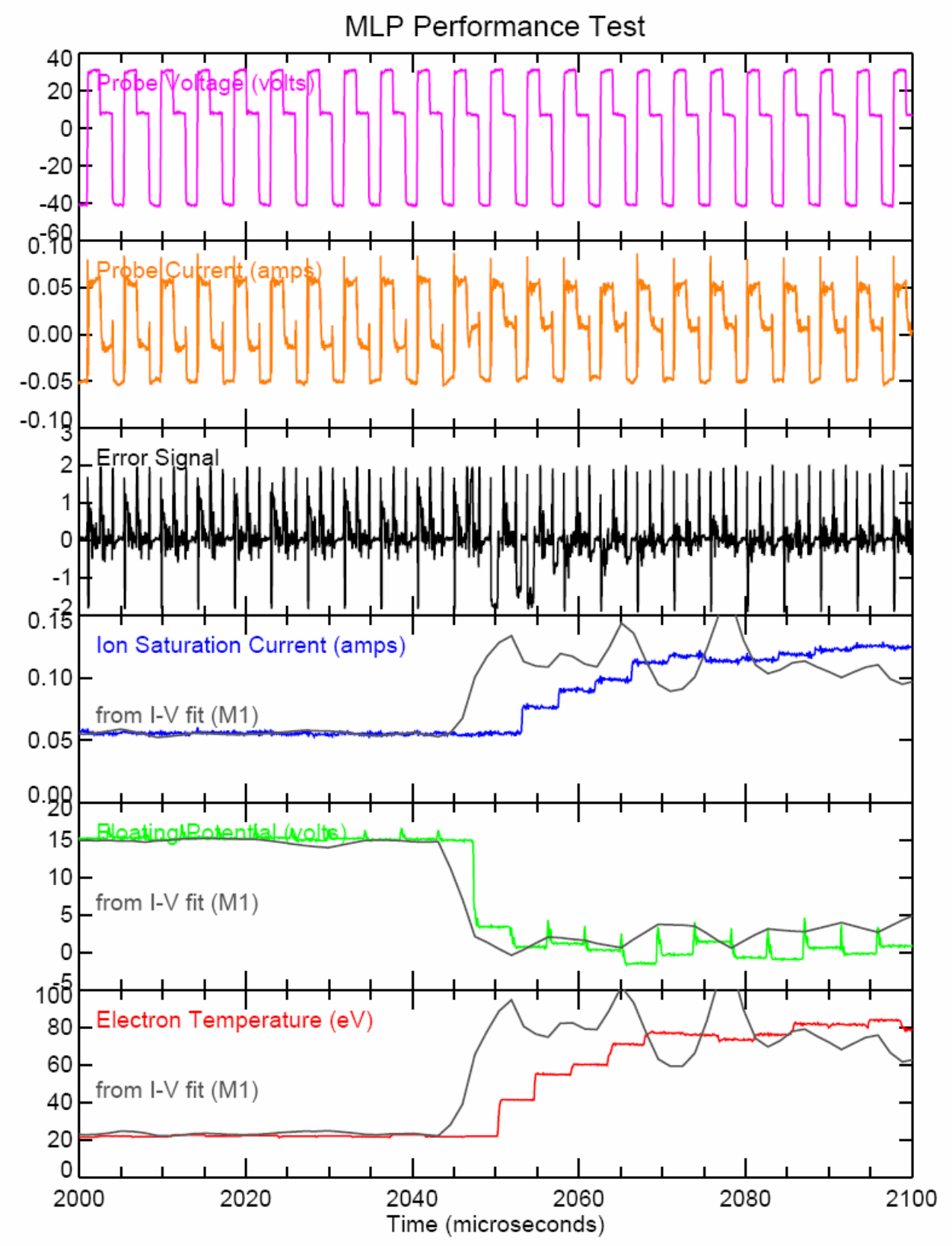


Figure 5.9 – Variable ELP Test – Small Time Scale with M1 Output

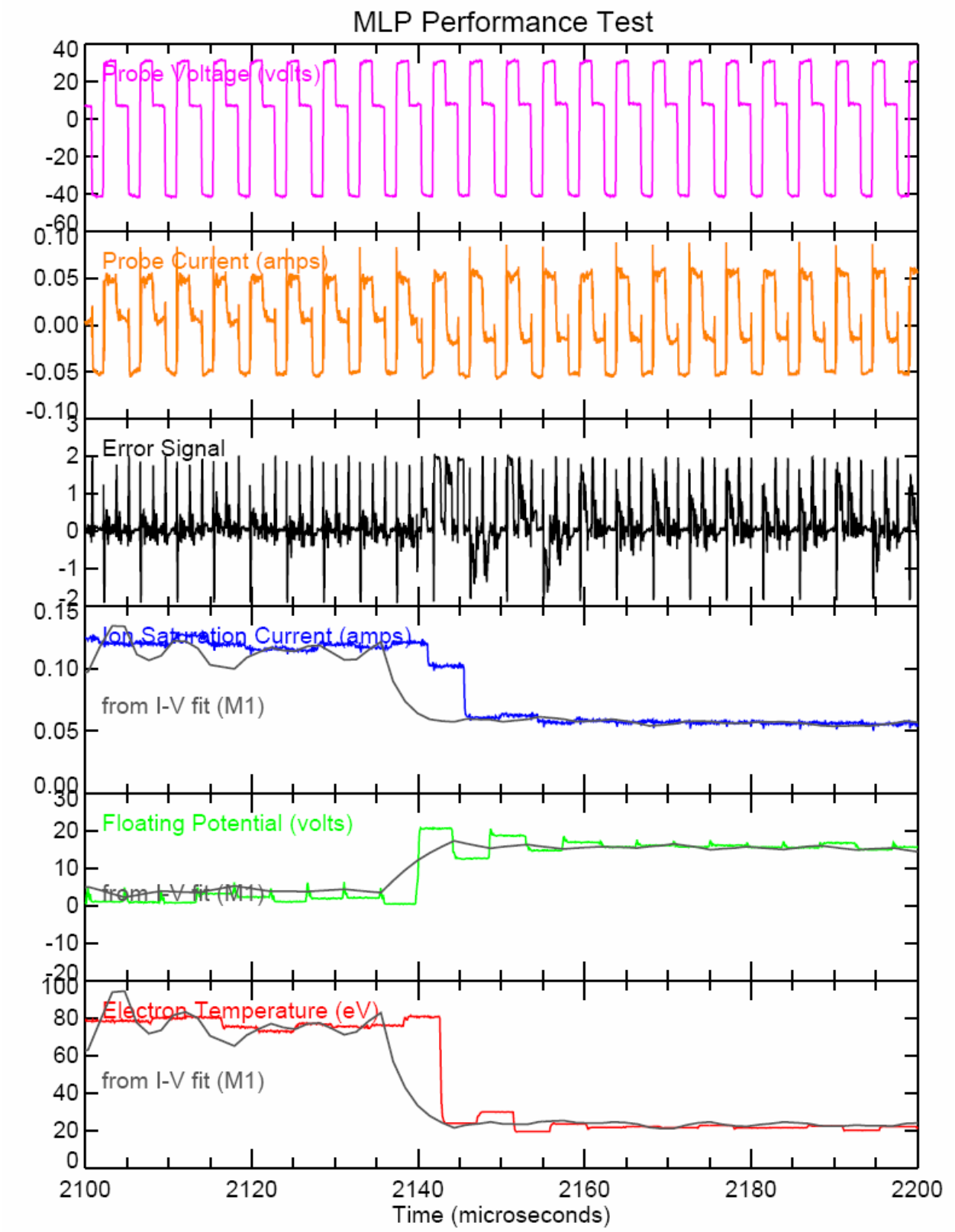


Figure 5.10 – Variable ELP Test – Small Time Scale with M1 Output

Chapter 6 – MLP System Tests – Real Plasma

Initial testing of the MLP was performed on the Alcator C-Mod tokamak, collecting data from a few plasma discharges. The objective was not to study the plasma conditions in C-Mod but to obtain some initial Langmuir Probe data from real plasmas, develop benchmarks to validate the system's output and get a first look at what is currently possible as far as performance goals. Identifying any areas of possible improvement would be useful at this juncture as well.

6.1 – Experimental Set-up

The MLP system was connected to the "north-east" electrode (NE) on Alcator C-Mod's horizontal scanning probe drive (see Figure 6.1). At the same time, the floating potential on the other three electrodes (SE, SW, NW) were monitored (1 MHz sampling rate) using the existing data acquisition systems. All four electrodes have a plasma-collection area of 1 mm^2 and are located close together (spacing ~ 2 mm).

Data from several plasma shots were obtained with the system, but the results from only one is presented here since it is representative of typical results. These data were obtained during the 29^{th} shot on Friday, April 6^{th} 2007, which was during the start-up phase of the latest campaign on Alcator C-Mod. The run on this day (and likewise shot 29) was not dedicated to the operation of the MLP system, but the targeted plasma conditions were stable enough to allow for testing of the MLP. Some of the basic information for the plasma created during shot 29 is shown in Figure 6.2.

The top four time traces contain information about the conditions inside the discharge: Plasma current, toroidal magnetic field strength, central plasma density and central electron temperature. The last trace shows the position of the horizontal scanning probe. It is "plunged" into the cold, edge region of the discharge, with peak insertion at around 0.8 seconds. Approximately 15 ms before this peak insertion occurs, the MLP system (including D-TACQ digitizers) is triggered to begin operation for a duration of ~30 ms. The depth of the probe insertion was adjusted so as to collect peak current on the order of 0.1 amps.

6.2 – Initial MLP Data from Real Plasma

Figure 6.2 contains the primary outputs from the MLP system recorded over the full duration of the MLP operation. In addition, the floating potential recorded independently on the SE electrode is shown. At these time scales, it is difficult to follow the fast responses, but there are several points worth noting. First, there is an obvious trend in all the data plots that is directly correlated with the probe position in the plasma. At the apex of the probe's plunge into the plasma, all of the data traces show a significant amount of fluctuation when compared to periods when the probe is moving in or out of the plasma. This seems like a logical result due to the fact that as the probe moves into hotter, more turbulent plasma, the plasma parameters are going to have more fluctuations and larger values. Near peak insertion, a series of quasi-periodic "spikes" are seen on the ion saturation current, floating potential (both MLP and SE electrodes), and electron temperature traces. These "events" are thought to be a plasma fluctuation phenomena associated with "edge localized modes" (ELMs) in the plasma boundary [39]. Some other information available in this plot is the operation of the bias control system. The plus and minus drive voltages change with both short-term spikes and longer term trends. The values are seen to be approximately correct; -50V and +20V correspond to a time-averaged temperature of ~20eV. Although the bias control system attempts to respond to the spikes in Te, these events are too fast. Thus, the high-temperature events, if they are real, are computed by the MLP system using a bias range that is far from optimum (~3Te). This point is addressed again in discussions below. This plot also illustrates that during periods when there is no plasma exposed to the probe (i.e. times less than 0.0065s and greater than 0.025s in Figure 6.3), the MLP system wanders around to random values of the parameters as it struggles to match an I-V characteristic that is nonexistent. This is shown in the blue floating potential curve, which wanders away from the red floating potential curve during these periods.

Figure 6.4 shows an expanded timescale when the probe is furthest into the plasma to explore the "ELM" events in more detail. As the probe reaches this point, all three of the plasma parameters begin to show a behavior of spikes that occur roughly every 0.5 ms. These events are very significant with certain parameters changing values by an order of magnitude. While it is beyond the scope of this paper to explore these events, they show how the system responds to such rapid fluctuations; these are perhaps the most violent fluctuations that a Langmuir Probe

could experience in C-Mod. The floating potential agreement between the red and blue curves in Figures 6.4 and 6.5 offers the only indication to this point that the MLP system is calculating the correct parameter values. In fact, as the time scale is reduced further in Figures 6.6 and 6.7, the floating potential outputs from the MLP system and the floating probe system continue to agree with excellent precision, which establishes an early level of trust in these measurements.

As the spikes are investigated in more detail in Figures 6.6 and 6.7, it becomes clear that the spikes in all parameter values are occurring during the same periods. This leads one to believe that the MLP system is observing a real plasma phenomenon where the Langmuir probe is surrounded by a relatively stable plasma most of the time, but is periodically bombarded by a much hotter plasma that causes the observed spikes. These spikes are observed to last roughly 40-60 μs, which is well within the bandwidth of the MLP system. However, these spikes are much too short lived for the previous C-Mod Langmuir probe bias system to notice (it operates at 2 KHz), so this data can not be compared with previous measurements. Again, the reason or nature of these spikes is not of primary concern here; discovering the accuracy of the MLP measurements is the main goal.

6.3 – Capacitive Coupling and Bias Range Checks

As outlined in section 4.3.1, an important feature of the FET Drive circuit output is the variable coupling capacitance. The drive voltage is capacitively coupled to the Langmuir Probe so that the positive and negative bias voltage will "ride" on top of the changes in the floating potential over a time-scale of a few bias cycles. Thus, the coupling capacitance must be small enough to allow these adjustments over short time-scales but not too small to cause droop in the voltage during a given bias state. Under ideal conditions, the system should yield a voltage output in the "floating potential" bias state that closely corresponds to the floating potential output of the Langmuir Probe (which is reported by the MLP system)

Figure 6.8 provides a test of this function. The floating potential output signal is overlaid with the probe bias voltage in the first panel. Despite the rapid ramp-up in floating potential associated with the apparent "ELM" event, the floating potential value is always within the min-

max range of the driven probe voltage. While it does not precisely track the voltage during the floating potential state, it is apparently close enough to allow the system to lock-on to the true floating potential, as indicated by the comparison with "SE Floating Potential" in the fourth panel. Since there is little evidence of voltage droop on any given state of the bias waveform, it is concluded that the output capacitance values are set at appropriate values.

In the second panel of Figure 6.8, another instructive check is made. Here the ion saturation current output is overlaid with the probe current waveform (with change in sign). In the ideal situation, the amplitude of the voltage in the "ion saturation" bias state is sufficiently negative to collect ~90% of the ion saturation value. However, it can be seen that the probe often collects a net negative current that is only a fraction of the reported Isat value, particularly during times when Te is reported to be high. This behavior is readily understood because the voltage bias range is set by the external slow feedback loop to accommodate the time-averaged Te value of ~20eV. Thus, the MLP circuit has insufficient bias to sample probe currents close to the Isat level during the rapid, high Te excursions; it must derive the Isat values by extrapolating the I-V characteristic to large negative voltage levels. As a result, the Isat values reported by the MLP may be subject to error during the Te spikes. A possible solution for this problem is to operate the MLP system with a larger drive voltage range, say 5 times the time-averaged Te value instead of 3 times, in anticipation of such high Te "spike events."

6.4 – Comparison of Real-Time Output with Post-Processing Analysis

Figures 6.9 and 6.10 show the MLP outputs along with the computed values from the M2 algorithm. With the exception of during a short period of time (labeled "slew-rate limiting Vf ramp-down"), the MLP ion saturation current and floating potential signals are seen to be well-matching to the post-processed values. Te values from the M2 algorithm tend to overlay with the MLP derived values but appear to be "noisier" with spikes lasting only one bias state duration. These sub-spikes may be caused by noise in the current and voltage traces as they are separately recorded by the CPCI digitizers. In addition, unlike the MLP circuit, the M2 algorithm does not have the burden of charging a capacitor to change its reported Te values. Thus, the MLP integrator time-constraints may be filtering some of the Te fluctuations.

There is a notable difference between the MLP and M2 parameters in the time range before 14.95 ms in Figure 6.10. The Vf ramp-down looks like it lags the (perhaps) true ramp-down computed by M2. Figure 6.11 explores this feature in more detail and also displays some additional traces. The bottom panel shows the error signals reported by the sample-and-hold circuits for the Isat, Vf and Te outputs. During the "ramp-down", the Vf error signal is near its saturated value. Thus, it does appear that the Vf output is indeed ramping down at its maximum rate. The cause of this relatively slow ramp-down is the fast-drop in the reported Te value. Recall from Chapter 4 that the error signal sensitivity in the floating potential state is proportional to Te. Therefore, situations that lead to a simultaneous fast drop in Vf and Te values will be the most difficult for the MLP system to track.

Figures 6.11 and 6.12 also show an instructive overlay of a "model current" signal with the actual probe current signal. The model current signal is generated by taking the MLP outputted Isat, Vf and Te values and the voltage signal for any given point in time and calculating a "model" current level using Equation 2.9. If the three output parameters were being properly deduced by the MLP system, then the measured currents and computed currents should overlay. Some significant differences are evident, particularly during "slew-rate limited Vf ramp-down" in figure 6.11. It should be noted that the error signals provide a rough measure of the differences in the current between the actual and mirror Langmuir probes. The sample-and-hold error signal voltage divided by 32 corresponds to the difference in currents normalized to the ion saturation current, hence these labels on the plots. Figure 6.12 shows that the ion saturation current error hovers within the ±5% level during the time when no "ELM" events occur. Vf and Te errors are generally larger, in the ±10% range. The up and down jog on the Te output and error signal in Figure 6.12 suggests that there may be unresolvable high frequency components to the plasma's electron temperature fluctuations and that the system might benefit by using a larger Te-integrator capacitor to reduce the resultant step-to-step variation.

Throughout all of the tests performed, at no time did the MLP system lock onto a nonsensical state. As long as there was sufficient current signal, the MLP system was found to faithfully track the Langmuir probe and report reasonably accurate results, even during some of the extreme variations found during the "ELM" events. Further improvements to the MLP system

could be made, including an increased bias range (~5Te) and perhaps an increased switching frequency to help follow the plasma fluctuations in the sub-microsecond time range.

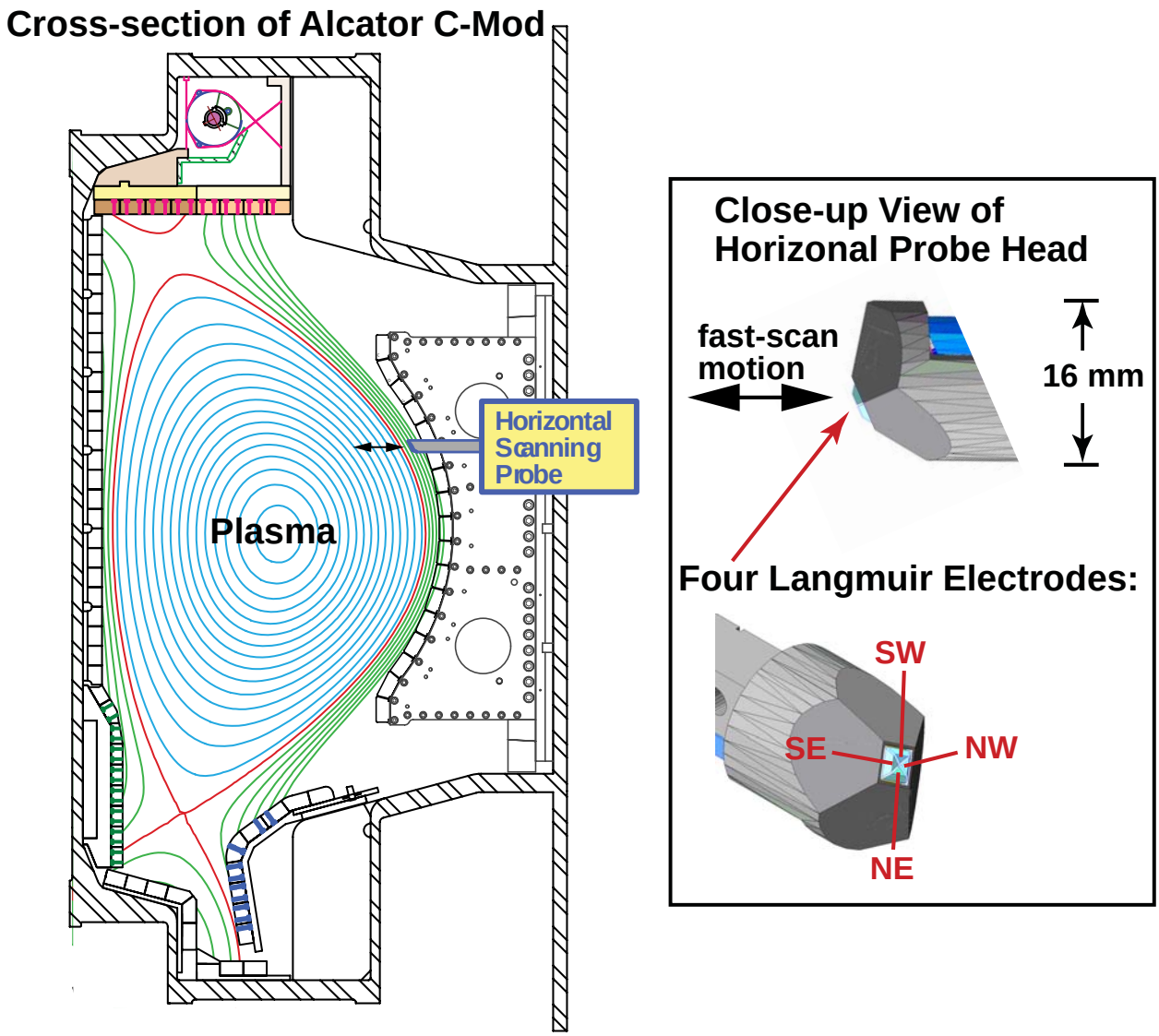


Figure 6.1 – Cross-section of Alcator C-Mod and Horizontal Probe Head Detail

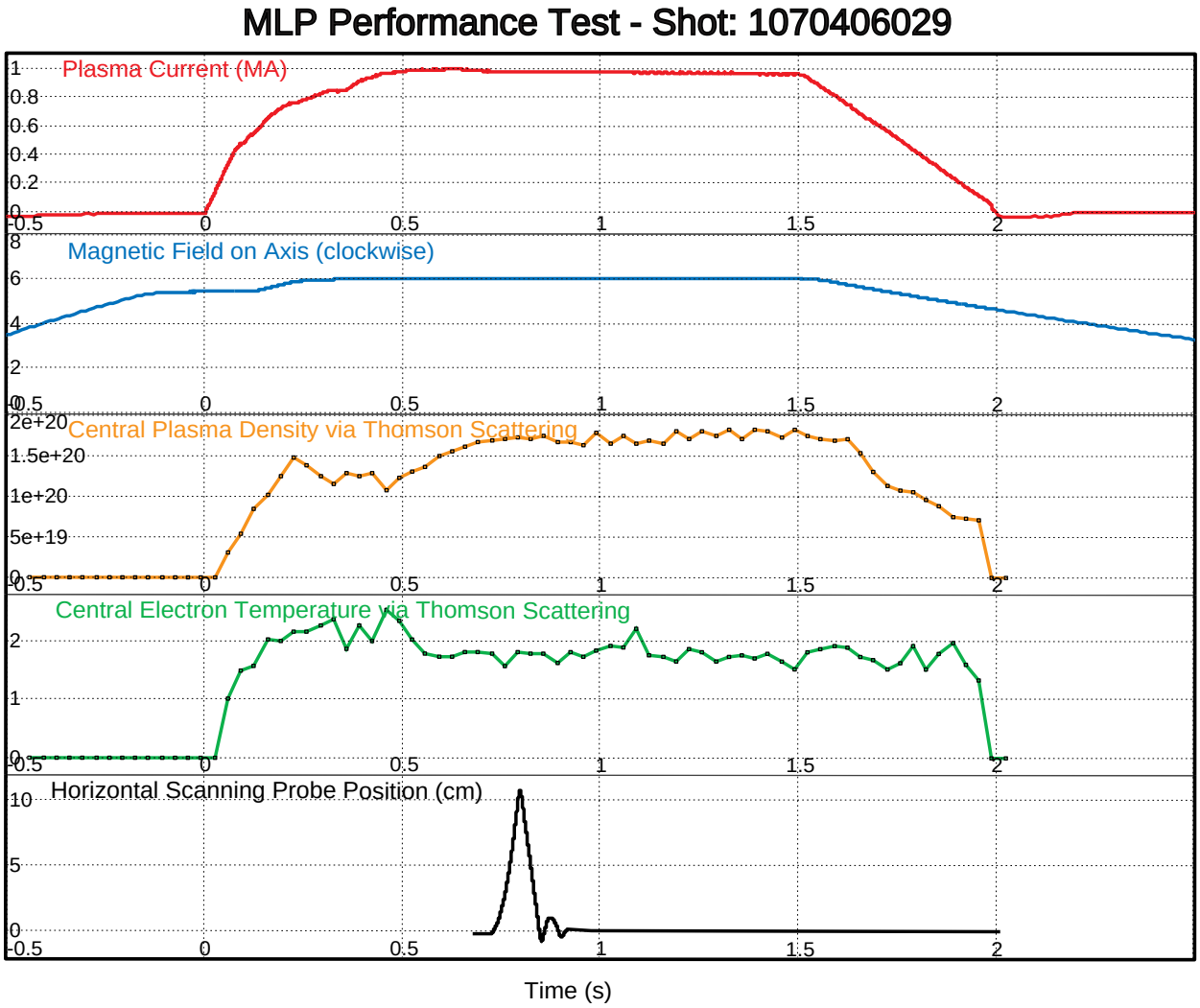


Figure 6.2 – Plasma Parameters for Alcator C-Mod Shot 1070406029

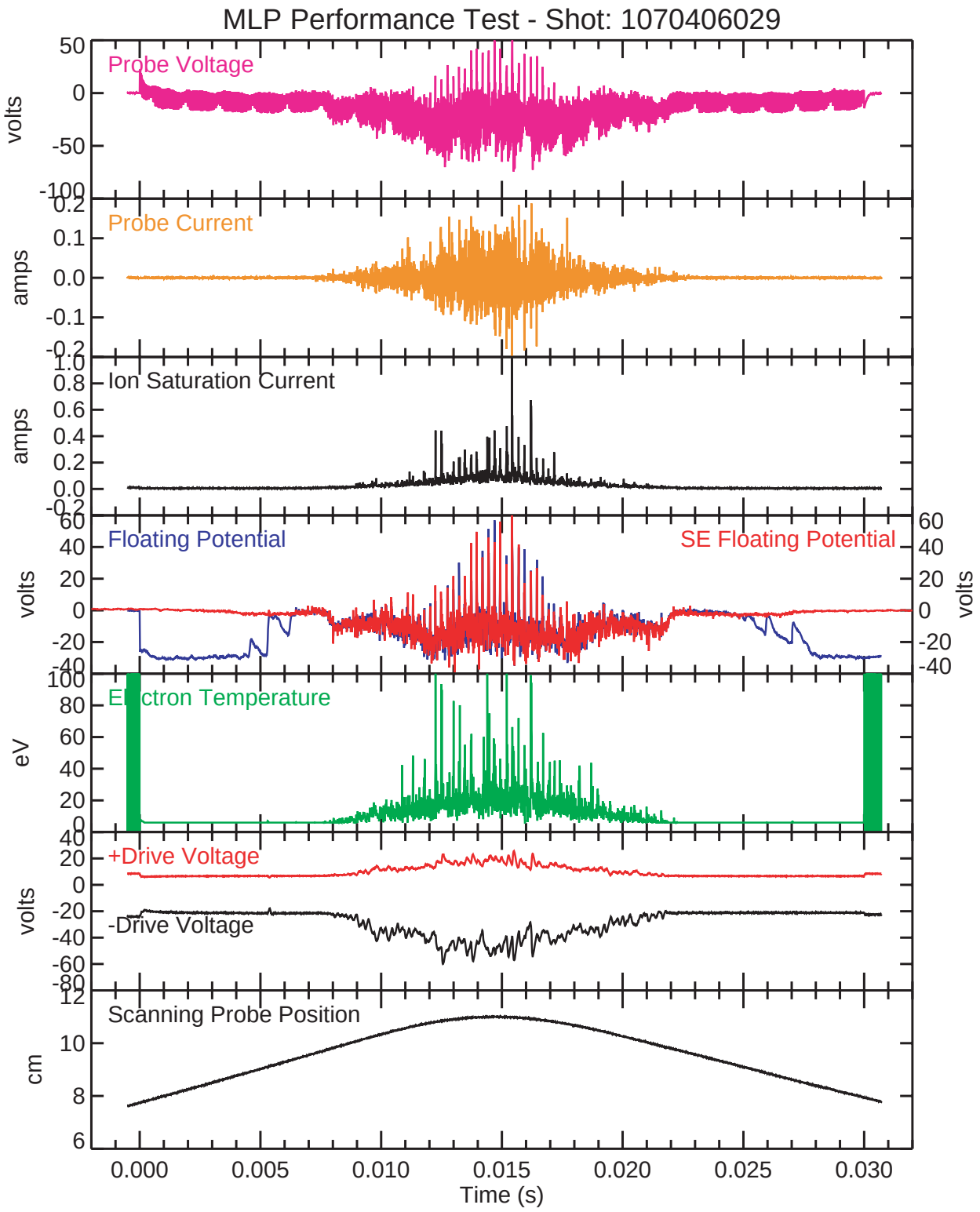


Figure 6.3 – MLP Data from Alcator C-Mod with Floating Probe Overlay

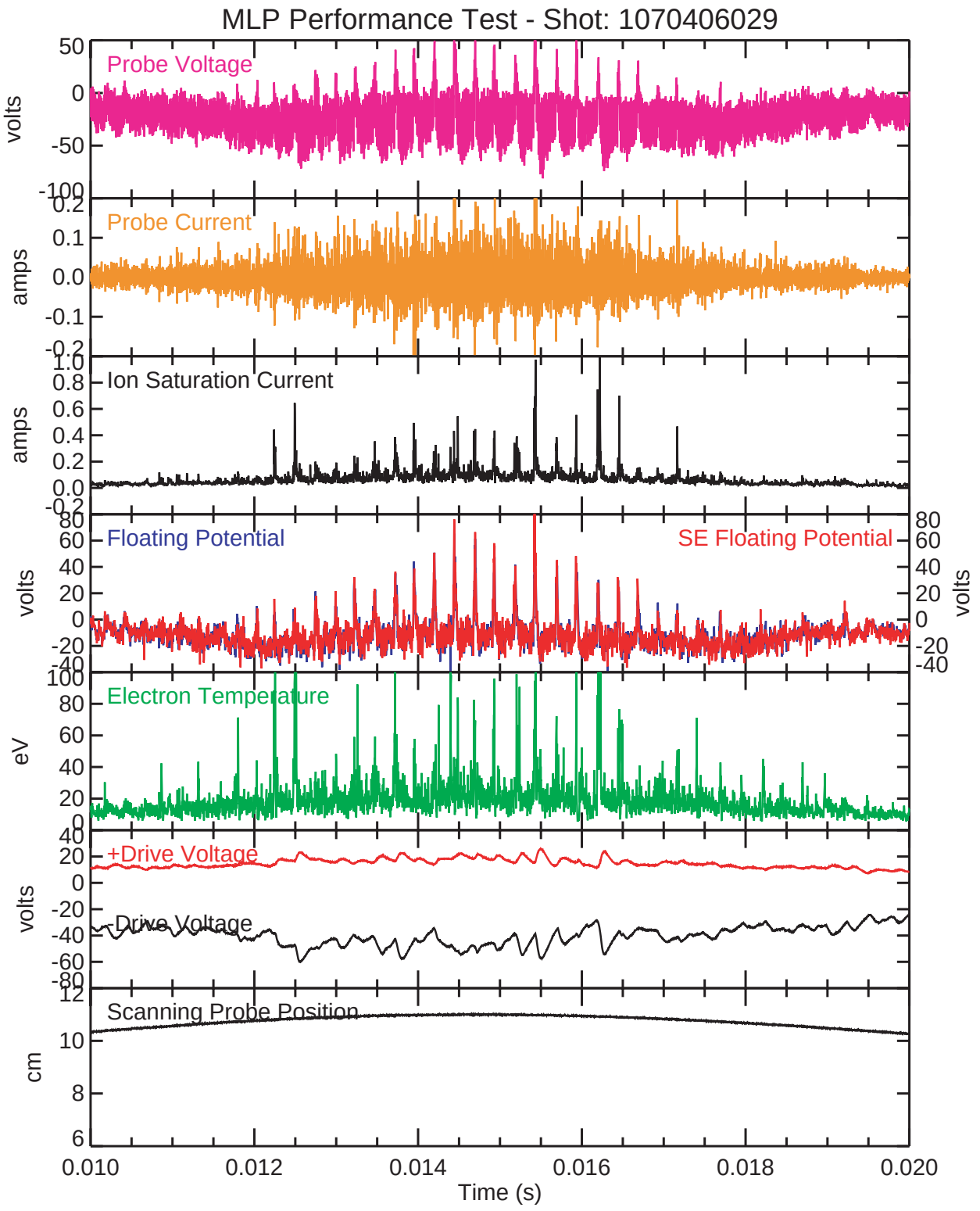


Figure 6.4 – MLP Data from Alcator C-Mod with Floating Probe Overlay

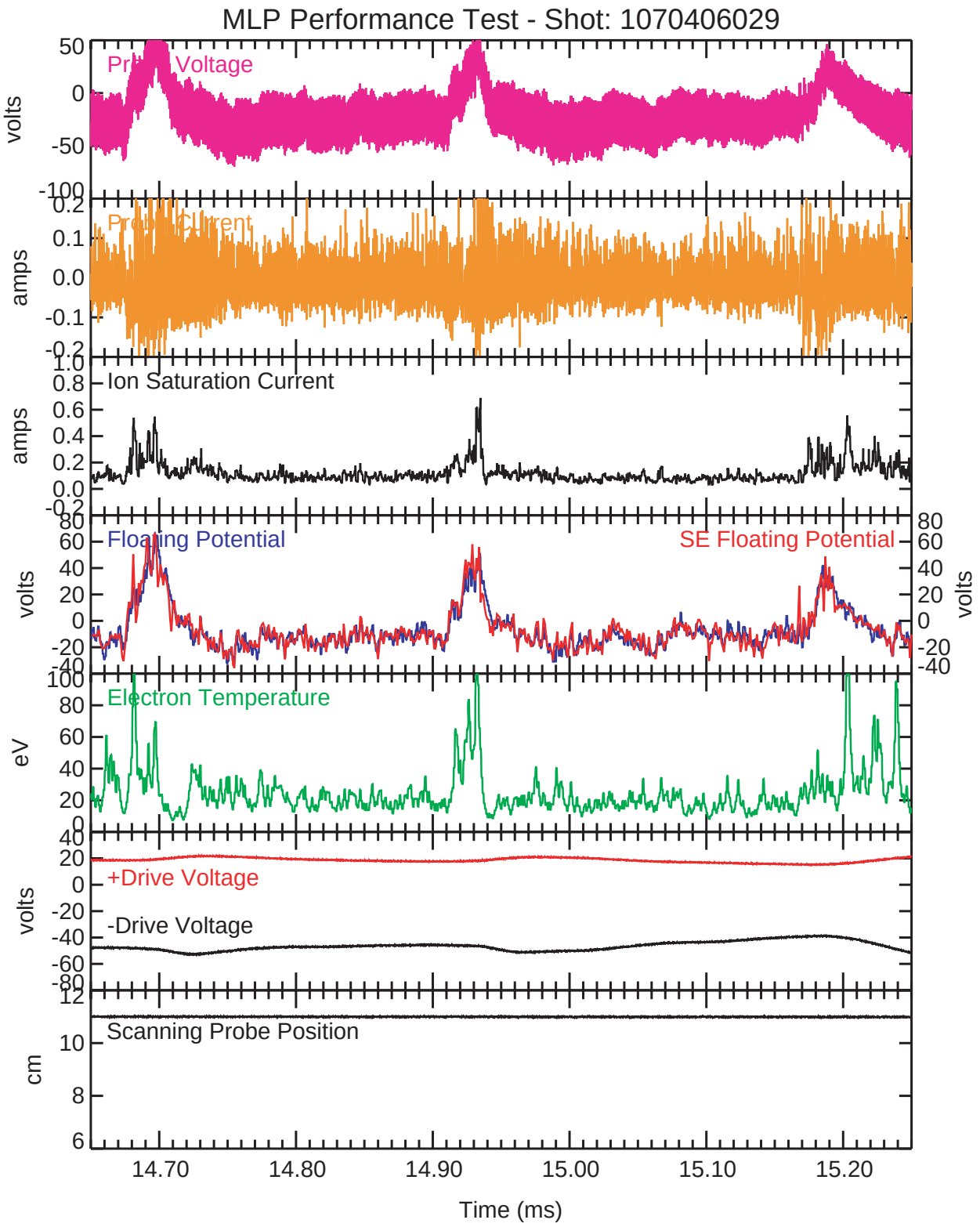


Figure 6.5 – MLP Data from Alcator C-Mod with Floating Probe Overlay

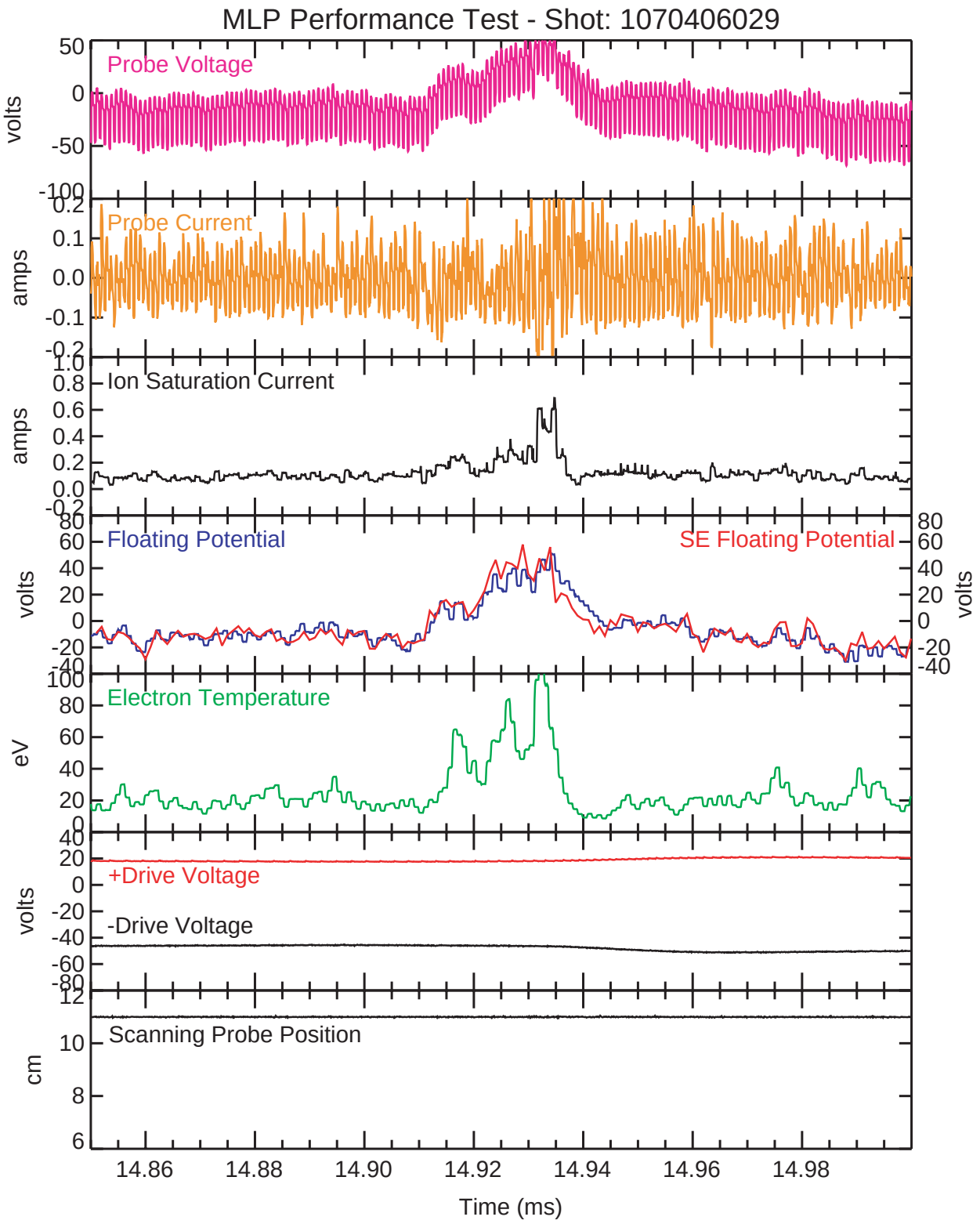


Figure 6.6 – MLP Data from Alcator C-Mod with Floating Probe Overlay

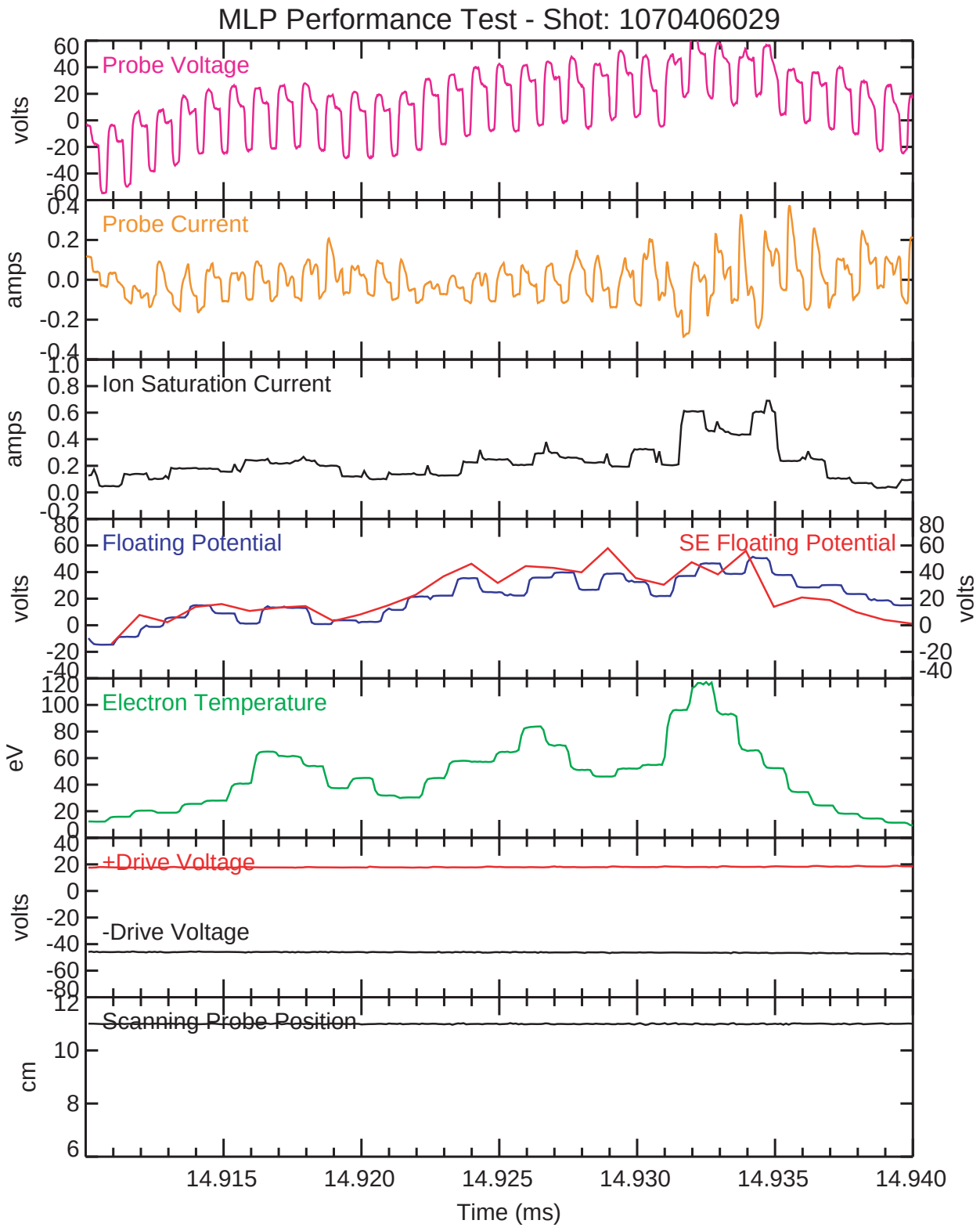


Figure 6.7 – MLP Data from Alcator C-Mod with Floating Probe Overlay

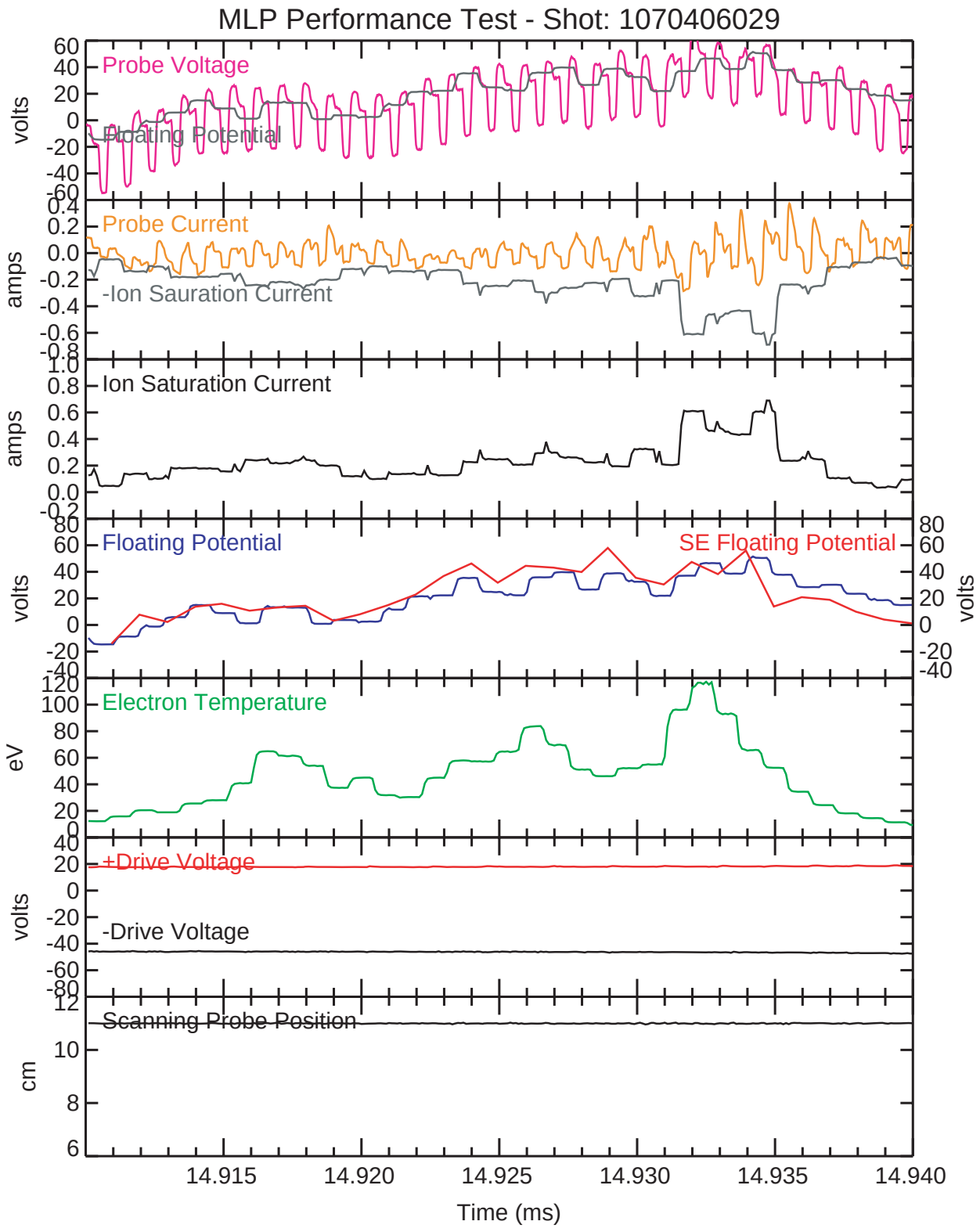


Figure 6.8 – MLP Data from Alcator C-Mod with Floating Probe, Vf and Isat Overlay

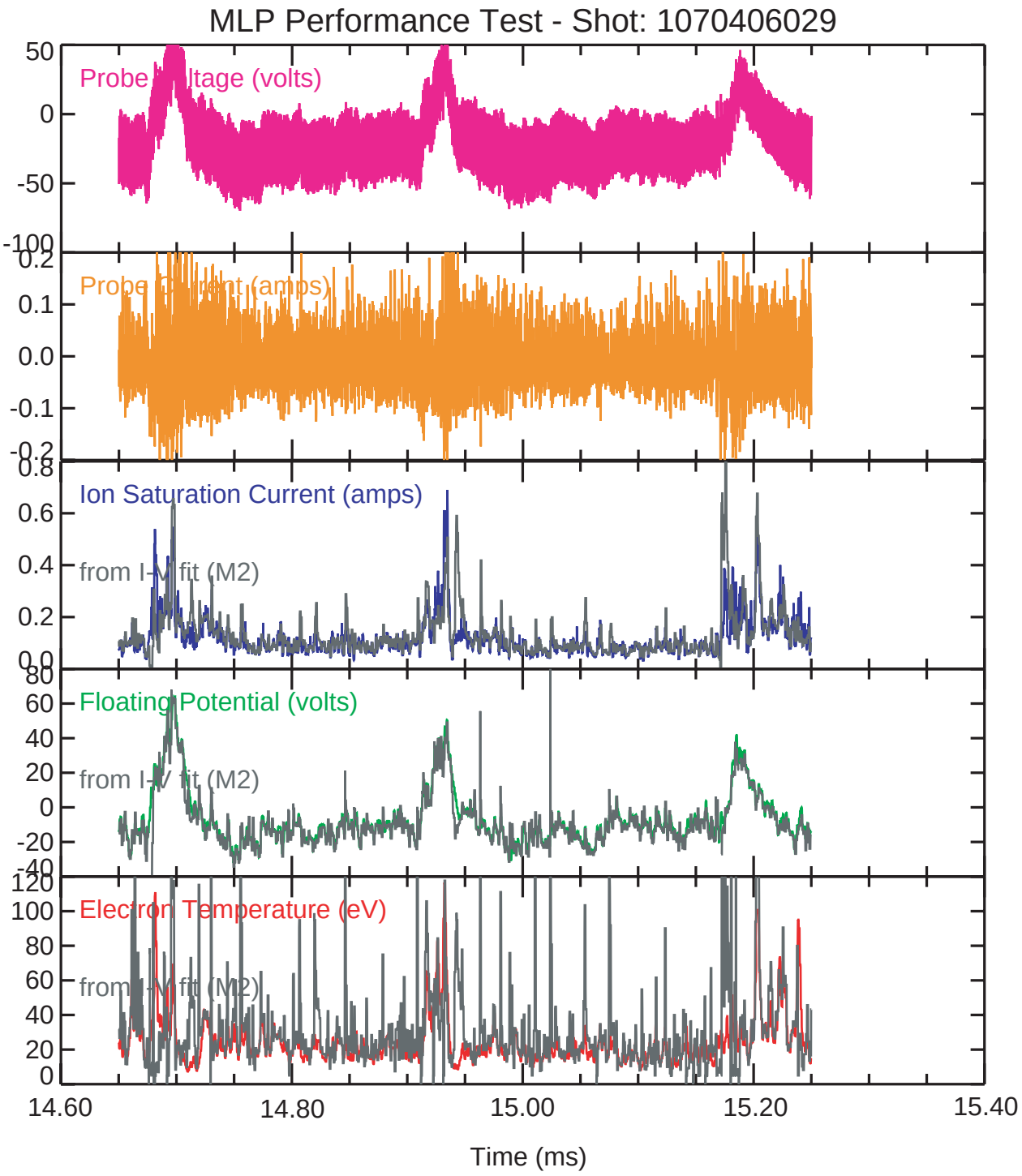


Figure 6.9 – MLP Data from Alcator C-Mod with M2 Output Overlaid

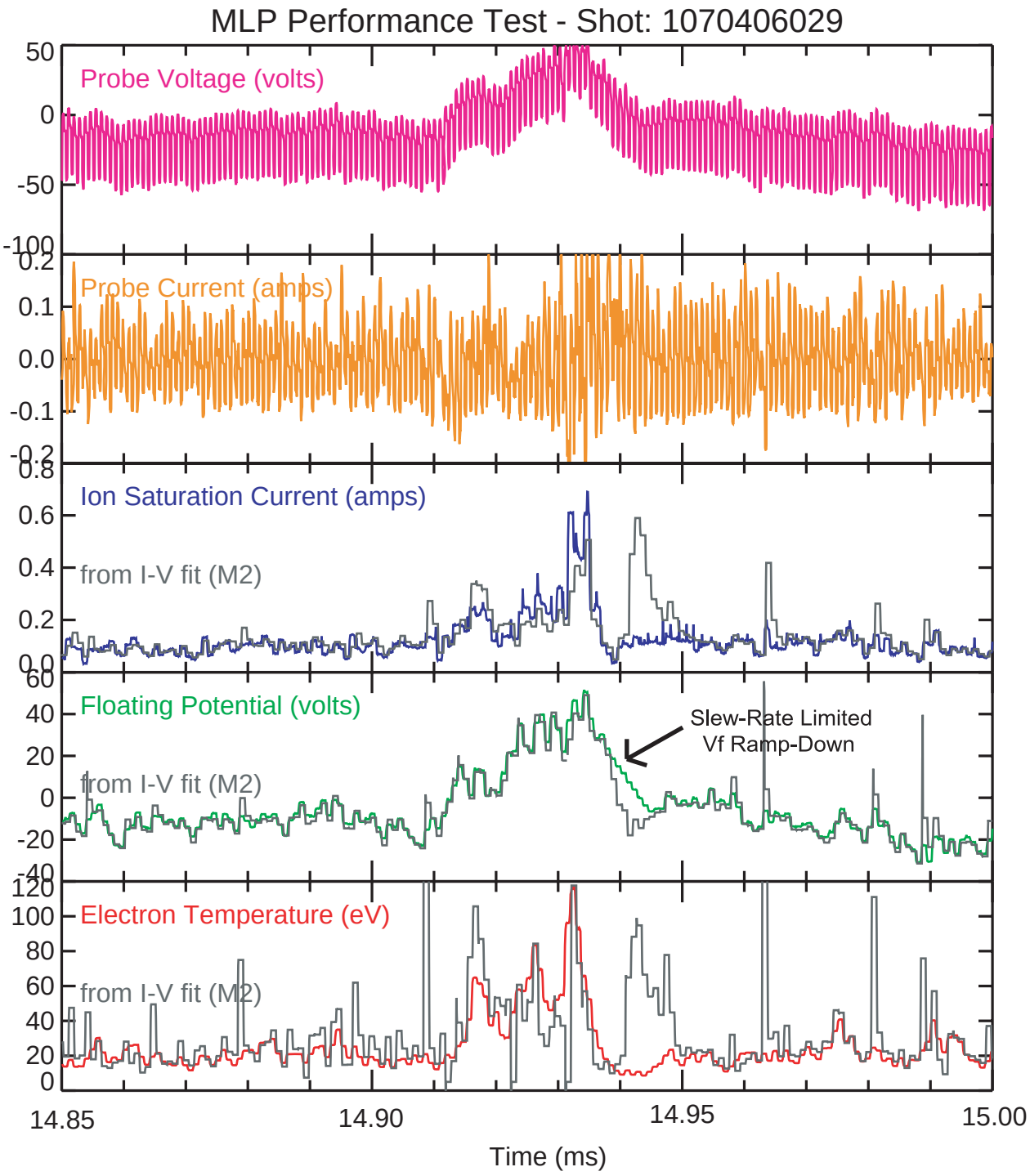


Figure 6.10 – MLP Data from Alcator C-Mod with M2 Output Overlaid

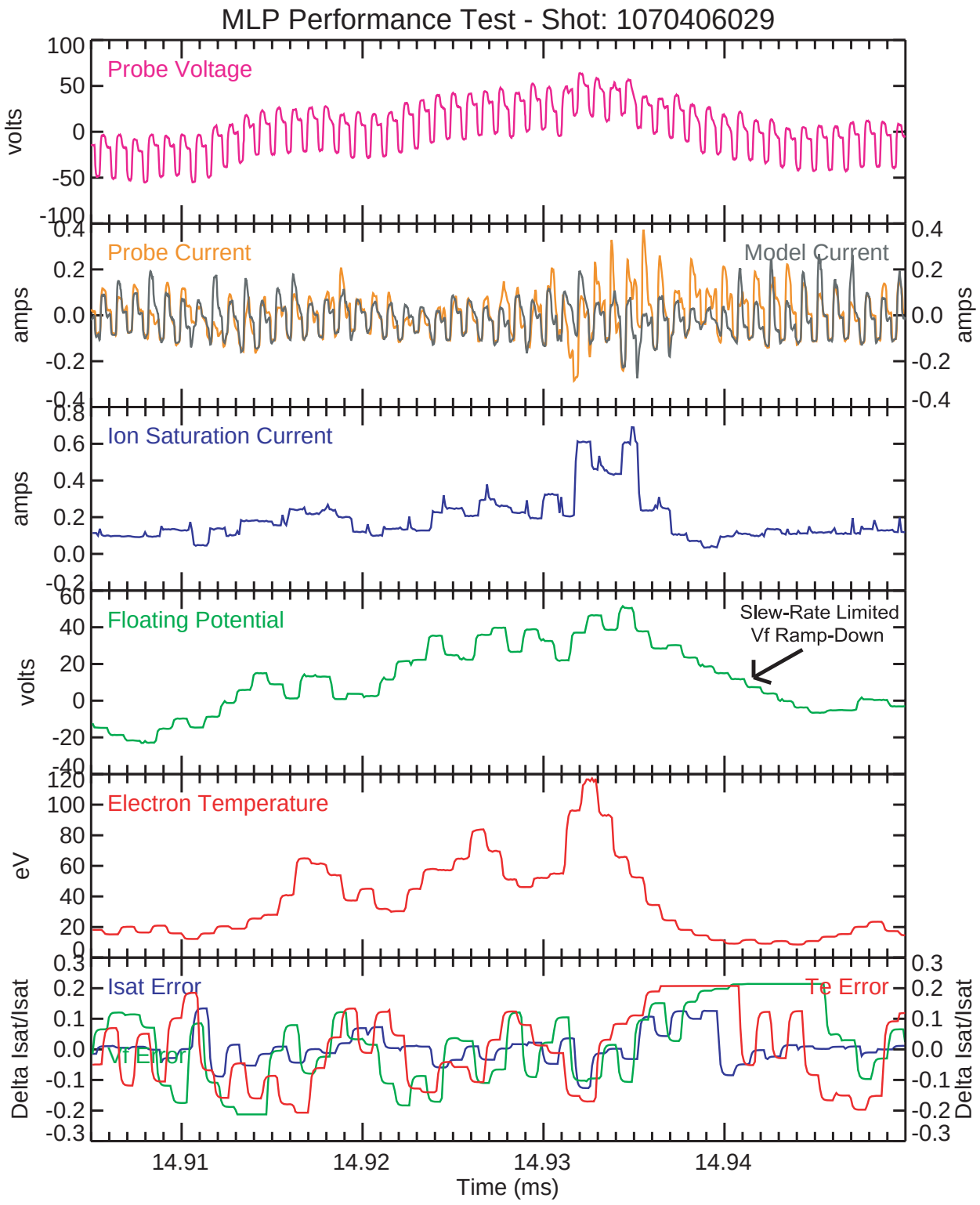


Figure 6.11 – MLP Data from Alcator C-Mod with Computed Current and Error Signals

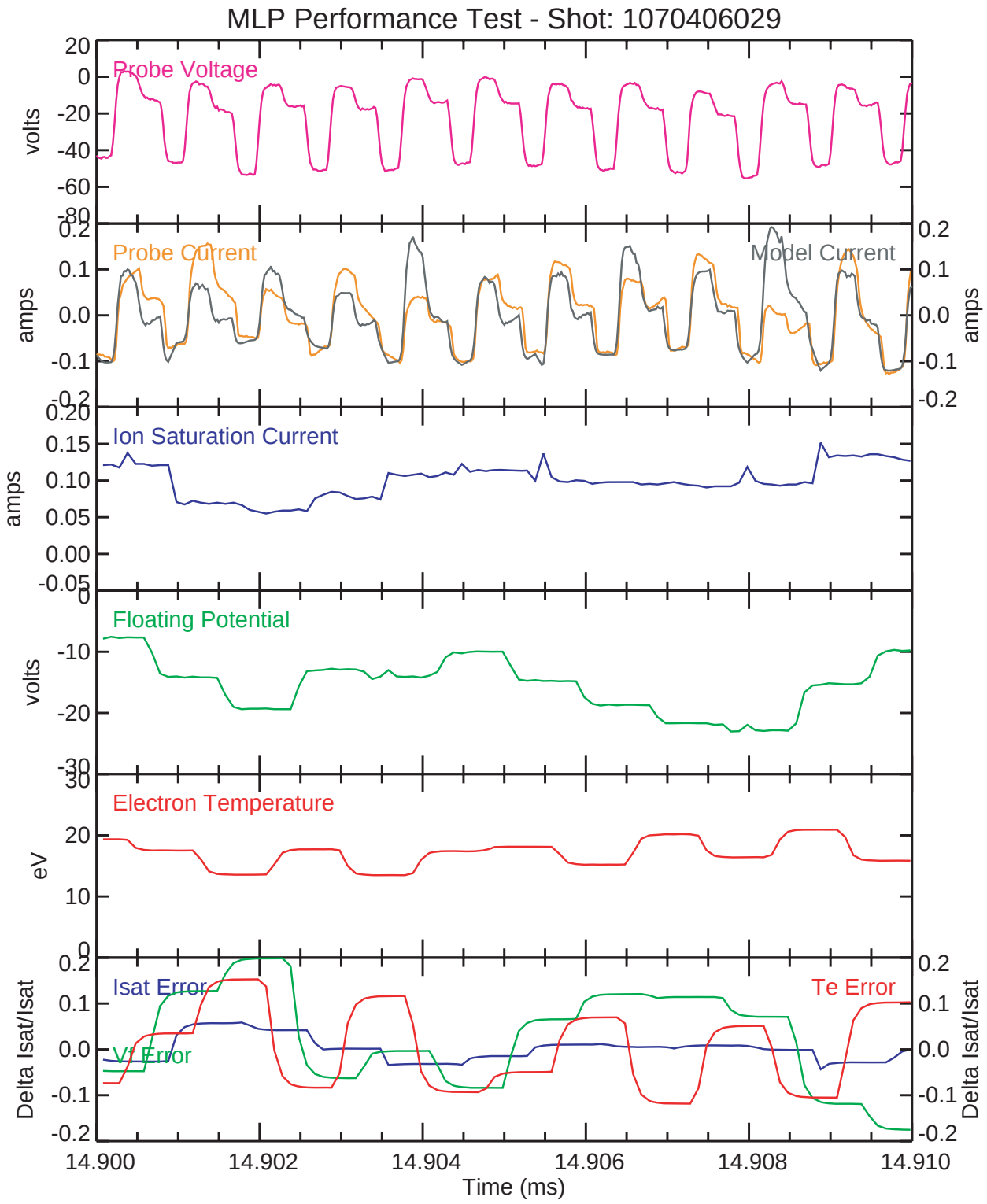


Figure 6.12 – MLP Data from Alcator C-Mod with Computed Current and Error Signals

Chapter 7 - Summary and Conclusion

An advanced high-bandwidth Langmuir probe diagnostic system for Alcator C-Mod has been designed, constructed, tested and operated. The system is based on the concept of a "Mirror Langmuir Probe" (MLP) and represents a proof-of-principle demonstration of this novel technique. Through the use of a fast switching bias waveform and RF transistors, the MLP system has been demonstrated to track changes in ion saturation, floating potential and electron temperature in real-time using a single Langmuir Probe electrode. The system has been shown to resolve fast changes in these three parameters on the 1 μs time scale while maintaining an accuracy that corresponds to an error of less than ~5% in each parameter under most conditions.

This project started with the initial mirror Langmuir probe concept, proved that it was indeed viable (through PSpice simulation) and set the necessary specifications for a physical system. The MLP system consists of three primary circuits housed in a modular Euroframe rack that is capable of operating 6 Langmuir probes simultaneously. Key features and performance values that were attained are:

- 'TTL Waveform Generator' – This unit functions as the 'master clock' of the MLP system and provides TTL timing signals (<20 ns rise times) to control the state switching of the FET Drive board and the timing of the integrator circuits on the Data board.
- 'FET Drive Board' – This circuit utilizes high-frequency switching MOSFETs to generate a three-state voltage bias waveform with an output range of -240 to +120V and current of ~2A. The amplitude of the bias waveform (with voltage rise times of <70 ns) is adjusted in real-time to the optimum value utilizing two signals from the Data board. The output is capacitively coupled with capacitance values that are changed dynamically in response to the Langmuir probe current.
- 'MLP Data Board' – This circuit monitors the voltage and current on the real Langmuir probe and dynamically adjusts the three input parameters to its "mirror" transistors to attain a match between the two. This board outputs the real-time plasma parameters of ion saturation, floating potential, inverse electron temperature and error signals for each.

The MLP system was tested on the "bench" using an electronically simulated Langmuir probe and on Alcator C-Mod using a fast-scanning Langmuir probe electrode. The three-state bias waveform and MLP Data circuit was demonstrated to complete update cycles with a period of less than 1 μs. Bench tests showed that the system was able to accurately report ion saturation, floating potential and electron temperature values with less than 5% error when compared to post-processed data analysis. The system was additionally tested on a limited number of plasma shots on Alcator C-Mod and initial results proved promising, with tracking behavior and accuracy similar to bench tests. However, the plasma tests also subjected the system to several time-periods of extreme change in the three plasma parameters (thought to be caused by ELMs), where values would change by 2x – 5x over a period of ~40 μs. These periods proved to be a challenge for the MLP system and inaccuracies were evident.

While the MLP system has already proved its utility and is currently operating on Alcator C-Mod, a number of areas for improvement have been identified including:

- A larger bias range (~5Te) could be used to improve the response to rapid fluctuations (ELMs seen in Chapter 6)
- A faster update cycle (< 0.5 μs update time) may also be possible, which also would help with ELMs.
- Error signals for Vf and Te sometimes show an under-damped behavior during certain periods. This behavior appears to be caused by plasma fluctuations with timescales shorter than 1 μs. Increased integrator capacitors or decreased amplifier gains could be used to improve the outputted signals, but with some potential degradation of frequency response.
- In addition to a nearby "floating" electrode (Chapter 6), another electrode biased into "ion saturation" could be used to benchmark the MLP during C-Mod plasma tests. This would allow the accuracy of the Isat parameter to be independently assessed, particularly during ELM events

The implementation of the MLP system on Alcator C-Mod was by all accounts a successful project. It clearly has the capability of providing a wealth of data on plasma fluctuations and will enable researchers to explore new areas of plasma physics in the future.

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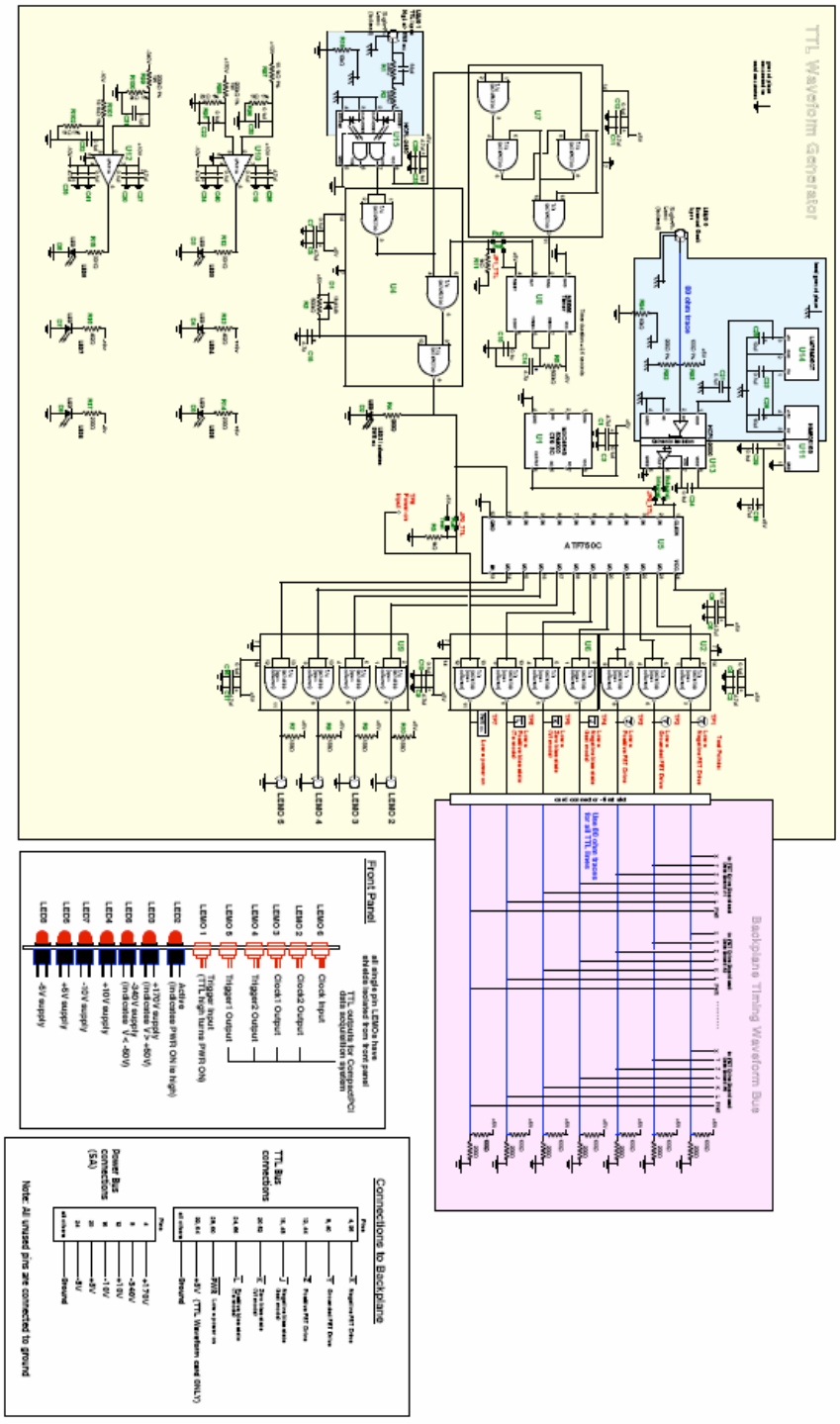
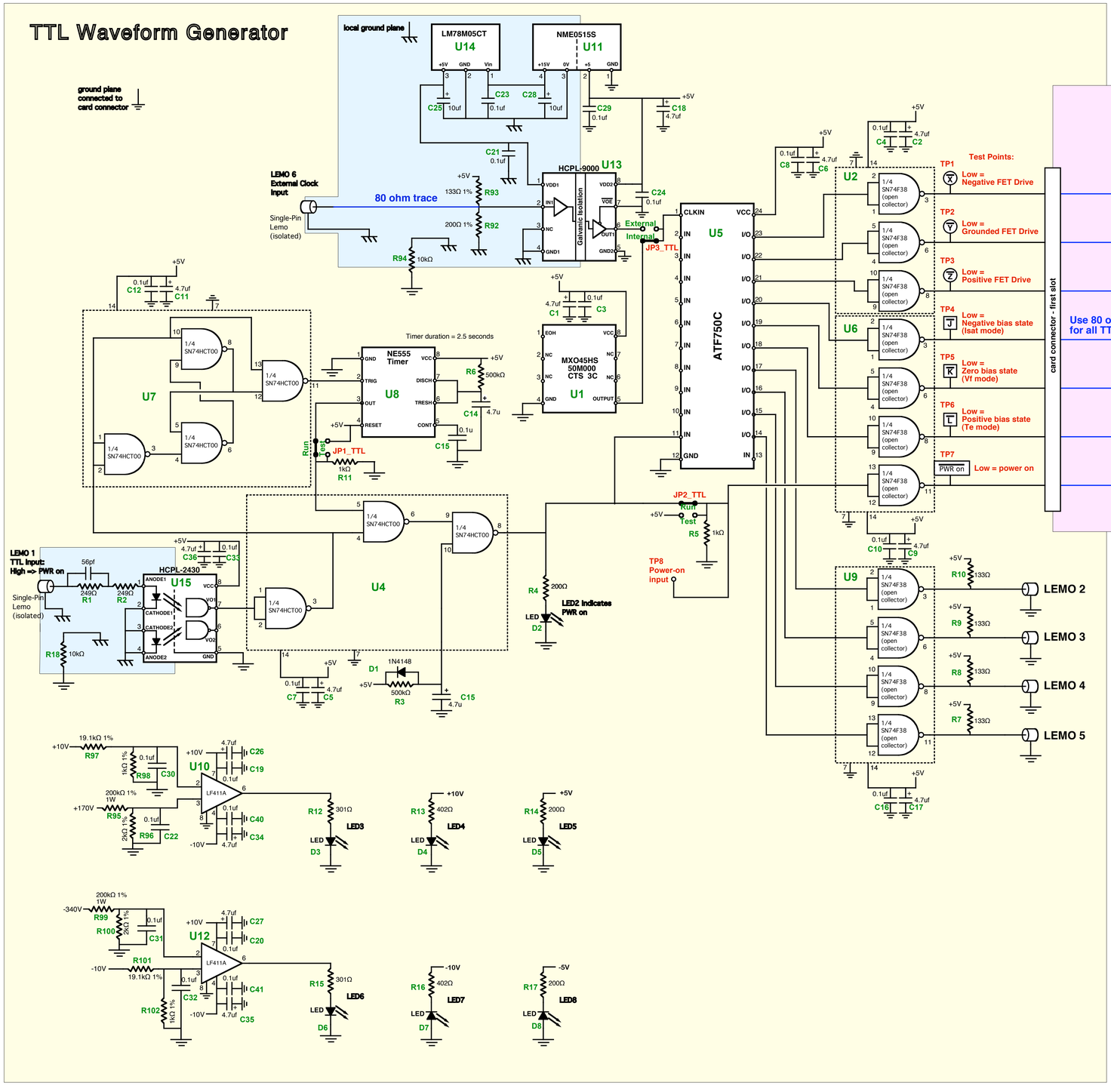
Appendix A – Mirror Langmuir Probe Circuit Schematics[9]

TTL Waveform Generator Circuit

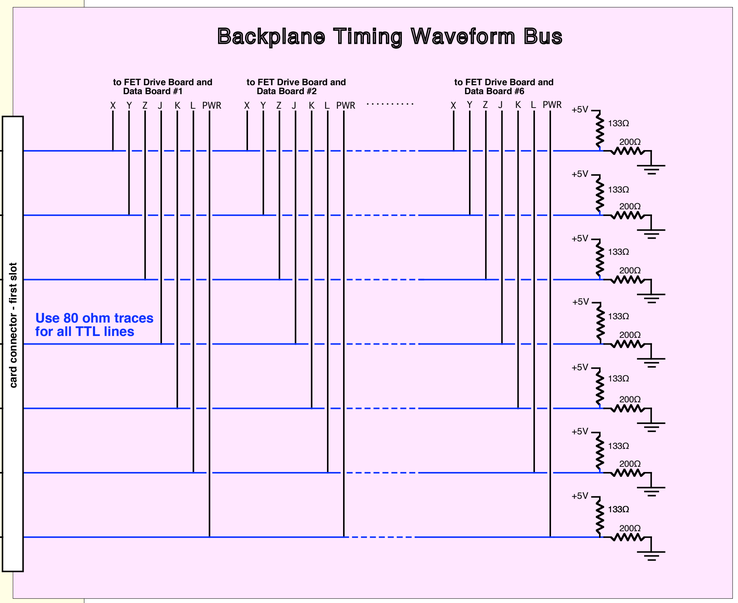


[9] High resolution versions of each circuit diagram are available in the electronic version of this paper.

TTL Waveform Generator



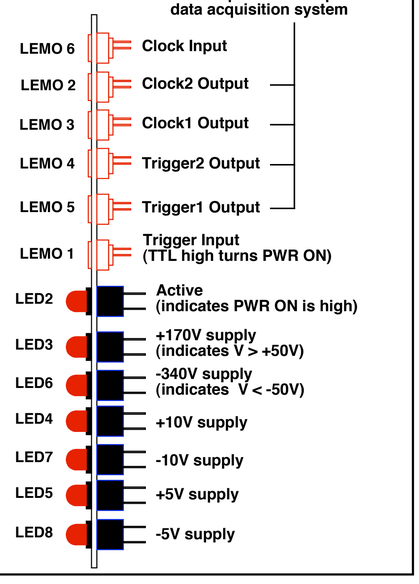
Backplane Timing Waveform Bus



Front Panel

all single pin LEMOs have shields isolated from front panel

TTL outputs for CompactPCI data acquisition system



Connections to Backplane

TTL Bus connections

Pins	
4, 36	$\overline{X}$ Negative FET Drive
8, 40	$\overline{Y}$ Grounded FET Drive
12, 44	$\overline{Z}$ Positive FET Drive
16, 48	$\overline{J}$ Negative bias state (Isat mode)
20 52	$\overline{K}$ Zero bias state (Vf mode)
24, 56	$\overline{L}$ Positive bias state (Te mode)
28, 60	$\overline{PWR}$ Low = power on
32, 64	+5V (TTL Waveform card ONLY)
all others	Ground

Power Bus connections (5A)

Pins	
4	+170V
8	-340V
12	+10V
16	-10V
20	+5V
24	-5V
all others	Ground

Note: All unused pins are connected to ground

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Mirror Langmuir Probe ~ TTL Waveform Circuit and Backplane Waveform Bus

B. LaBombard and L. Lyons

Modified- 6/21/2006

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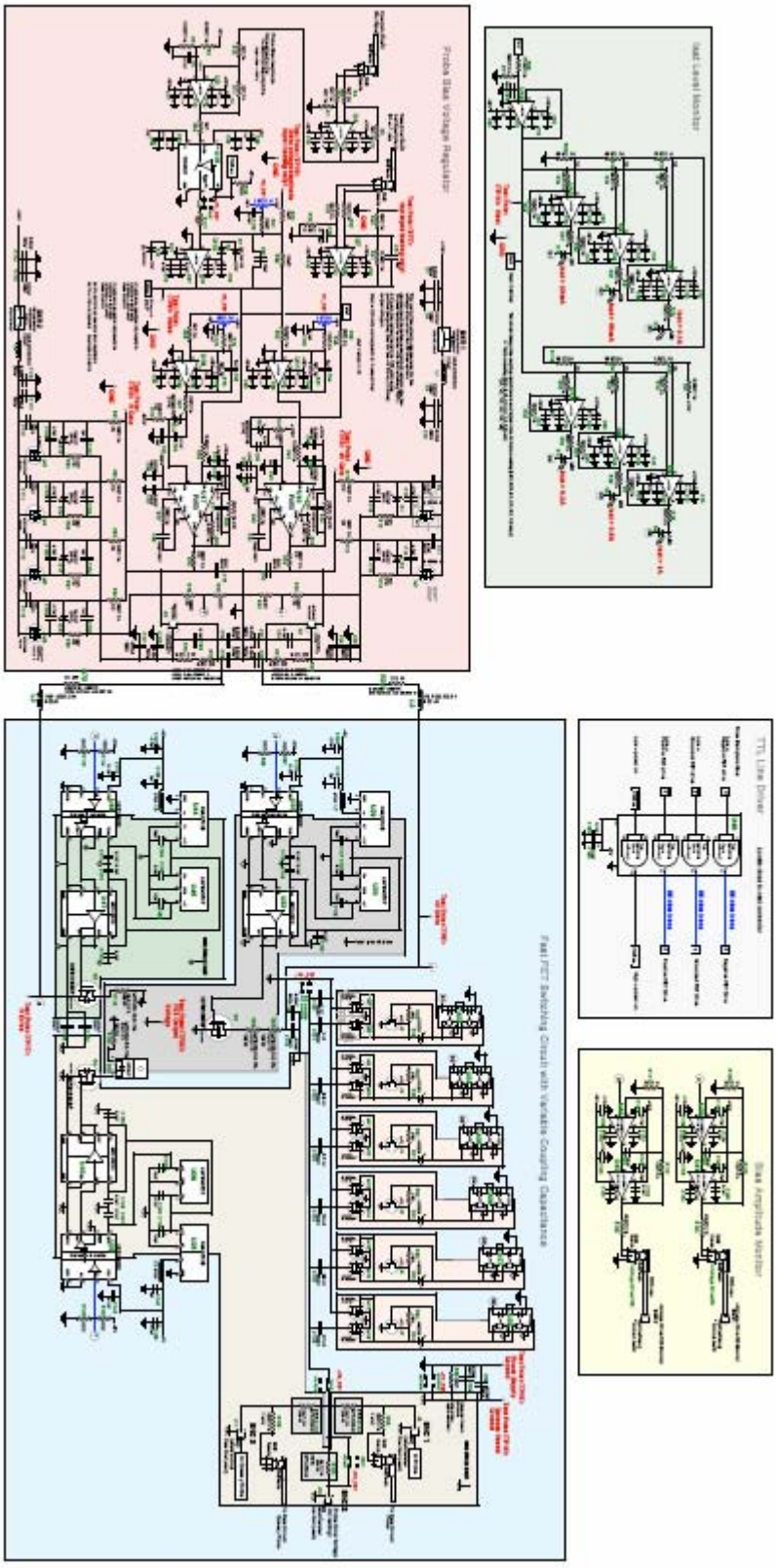
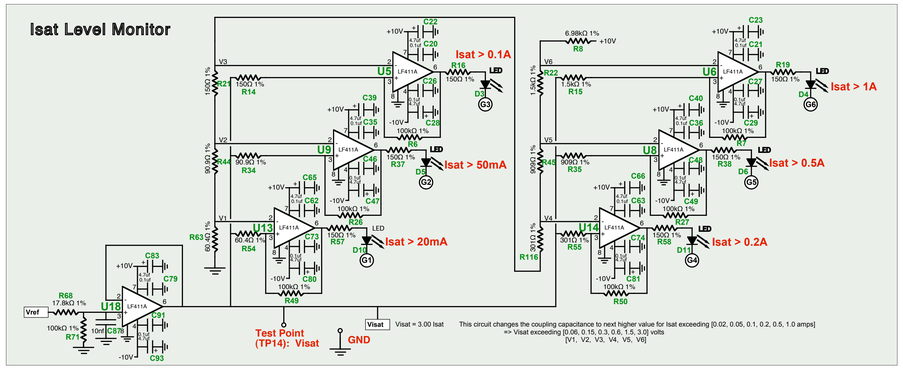
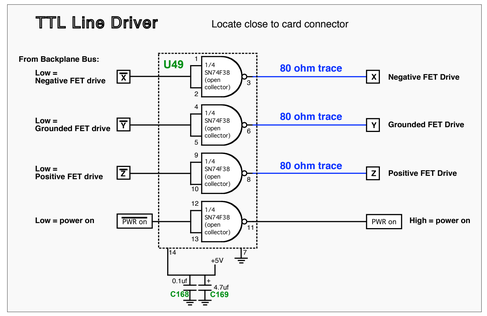
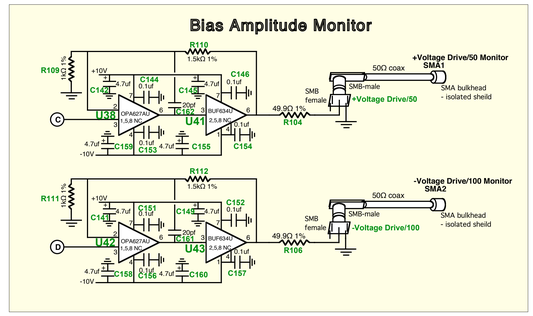
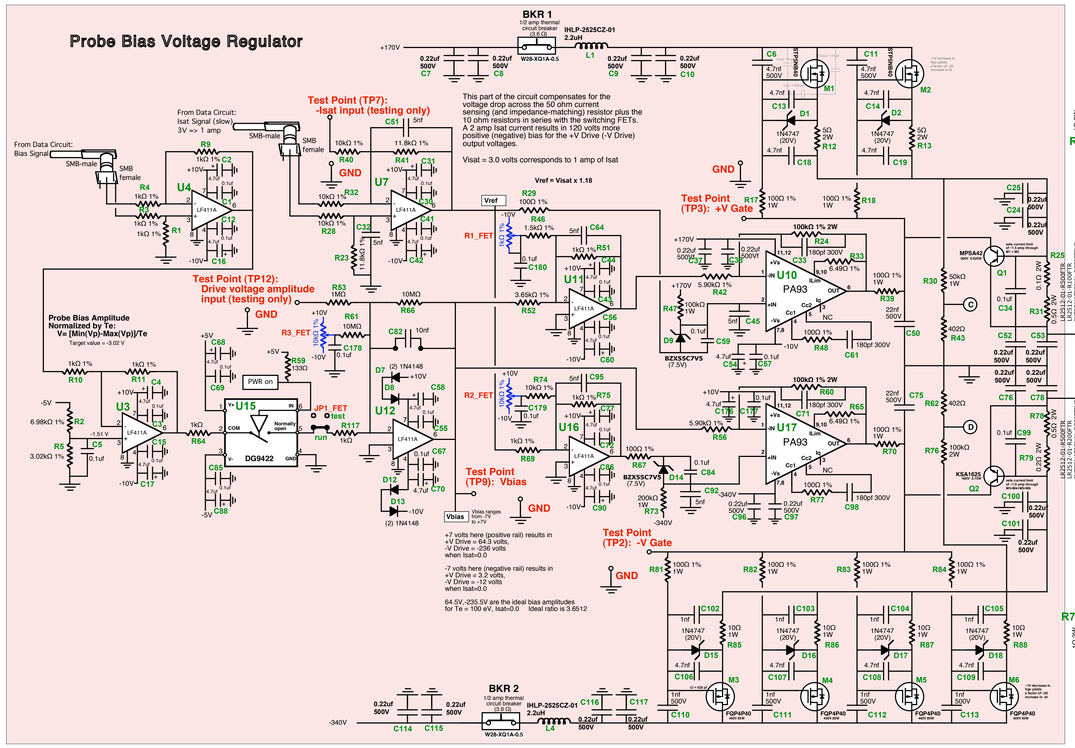
FET Drive Circuit

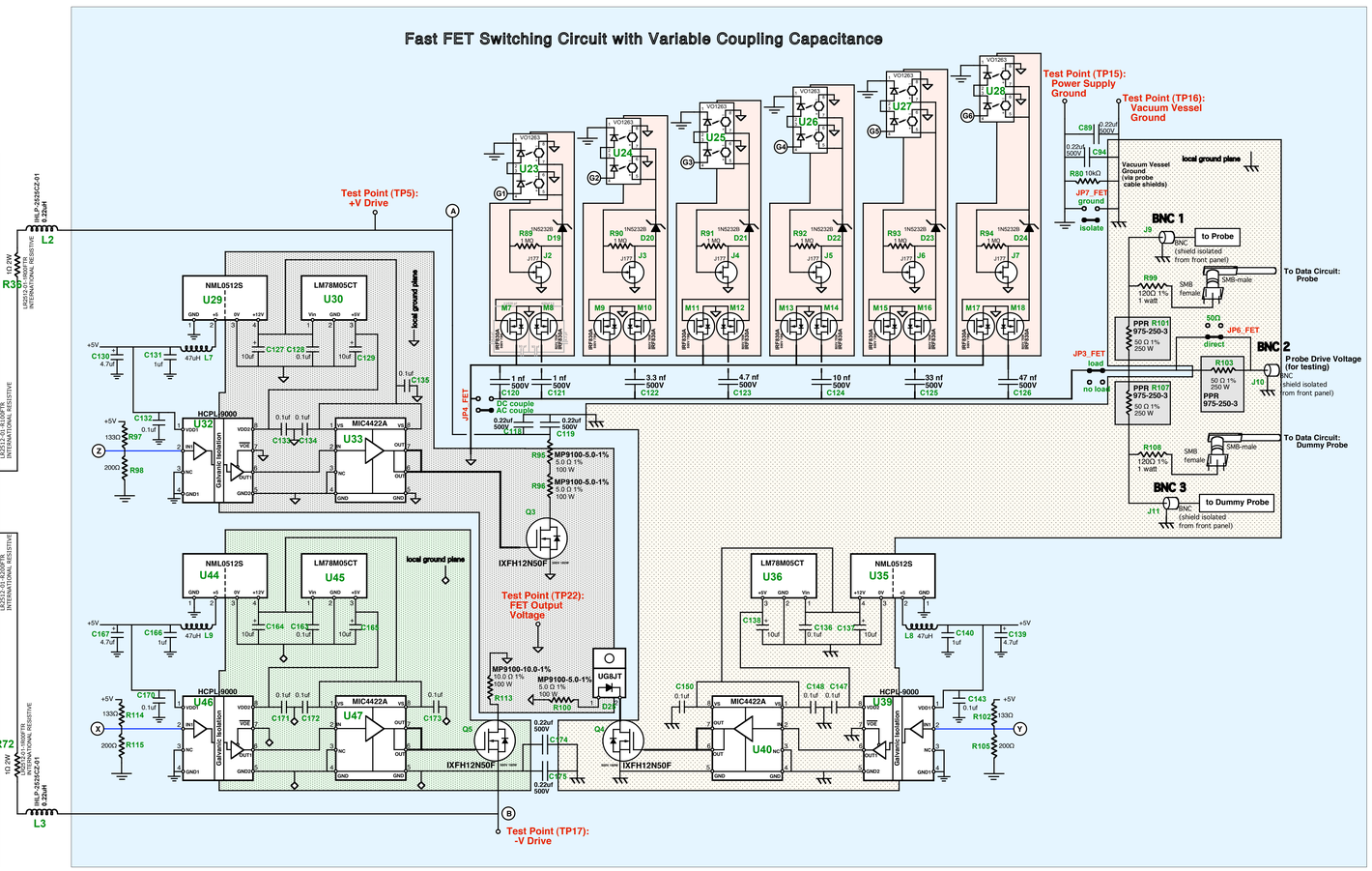


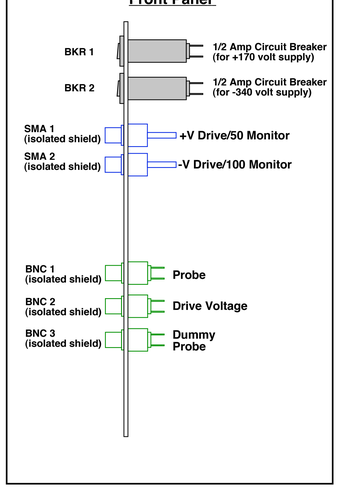


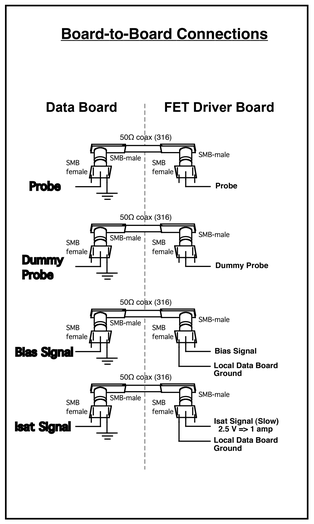


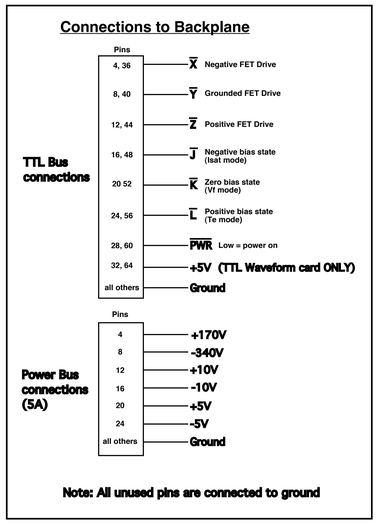












Calibration and Adjustment Procedures

Probe Bias Voltage Regulator:

Positive and Negative Drive Amplitude

- Set JP1_FET = test. Disconnect "Isat Signal" cable from Data Circuit. Monitor "Test Point: Vbias".
- Adjust R3_FET until Vbias is on the negative power supply rail of U12.
- Trigger TTL waveform circuit to generate FET switching waveform.
- Monitor probe drive voltage output at BNC2.
- Adjust R1_FET until peak positive output is at 3.22 volts.
- Adjust R2_FET until peak negative output is at -11.78 volts.
- Increase amplitude of output waveform by adjusting R3_FET. Check that negative and positive amplitudes track in the ratio of -3.65 to 1.
- Adjust R1_FET and R2_FET to optimize this ratio at high voltages, yet keeping output to near -12 to +3 volts when Vbias is on negative rail.

Quiescent Voltage Amplitude

- With same setup as above, adjust R3_FET until output voltage amplitude is -23.6 to +6.4 volts.

Notes on quiescent power requirements (when switching is on but without plasma load):

Each IXRH12N50F FET has 290 pf of output capacitance (Coss).
290pf x 3 x 510 V = 4.4x10^-7coulombs of charge must be supplied by the +V Drive in order for the output to go from -340V to +170 V.
290pf x 3 x 170 V = 1.5x10^-7coulombs of charge must be sinked to ground for the output to go from +170V to 0V.
290pf x 3 x 340 V = 3.0x10^-7coulombs of charge must be supplied by the -V Drive for the output to go from 0V to -340V.
The quiescent currents during a 1 MHz switching waveform are therefore: +V Drive =0.44 amps, -V Drive = 0.3 amps
The quiescent power dissipation is: +V Drive =0.44 A x 0.5 x 510 V = 112 watts, Ground =0.15 A x 0.5 x 170 = 13 watts, -V Drive = 0.3 A x 0.5 x 340 = 51 watts

Notes on plasma load:

The largest magnitude of current to be drawn by the Langmuir Probe is nominally ±2 amps.
The probe will draw up to +2 amps during 1/3 of the bias cycle (supplied by +V drive) and up to -2 amps during another 1/3 (supplied by -V drive).
Therefore the maximum time-averaged load currents are: +V Drive =0.67 amps -V Drive = 0.67 amps

Notes on power dissipation in STP5NB40 and FQP4P40 FETs:

Normal Case - 0.875 amp continuous operation (1/2 amp thermal breakers may trip in 1 hour):
Maximum power dissipation occurs when +V Drive and -V Drive are 1/2 the source voltages, +85 and -170 volts.
Therefore the maximum steady-state power dissipation is: STP5NB40s => 85V x 0.875A = 74 watts (2 STP5NB40s can handle 160W SS)
FQP4P40s => 170V x 0.875A = 149 watts (4 FQP4P40s can handle 340W SS)

Off- Normal or Pulse Operation Case with 1.5 amp over-current limit activated:
With a 1 MHz switching waveform, the +V Drive current available to the probe will be 1.5 - 0.44 = 1.06 amps time-averaged or 3.2 amps peak.
In this operation, the 1/2 amp thermal breakers will trip in 3 to 15 seconds.
In the worst-case scenario, +V Drive and -V Drive will be shorted to ground with resultant currents limited to 1.5 amps.
The power dissipation is: STP5NB40s => 170V x 1.5A = 255 watts (2 STP5NB40s can handle 160W SS)
FQP4P40s => 340V x 1.5A = 510 watts (4 FQP4P40s can handle 340W SS)

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Mirror Langmuir Probe ~ FET Drive Circuit - Rev 2

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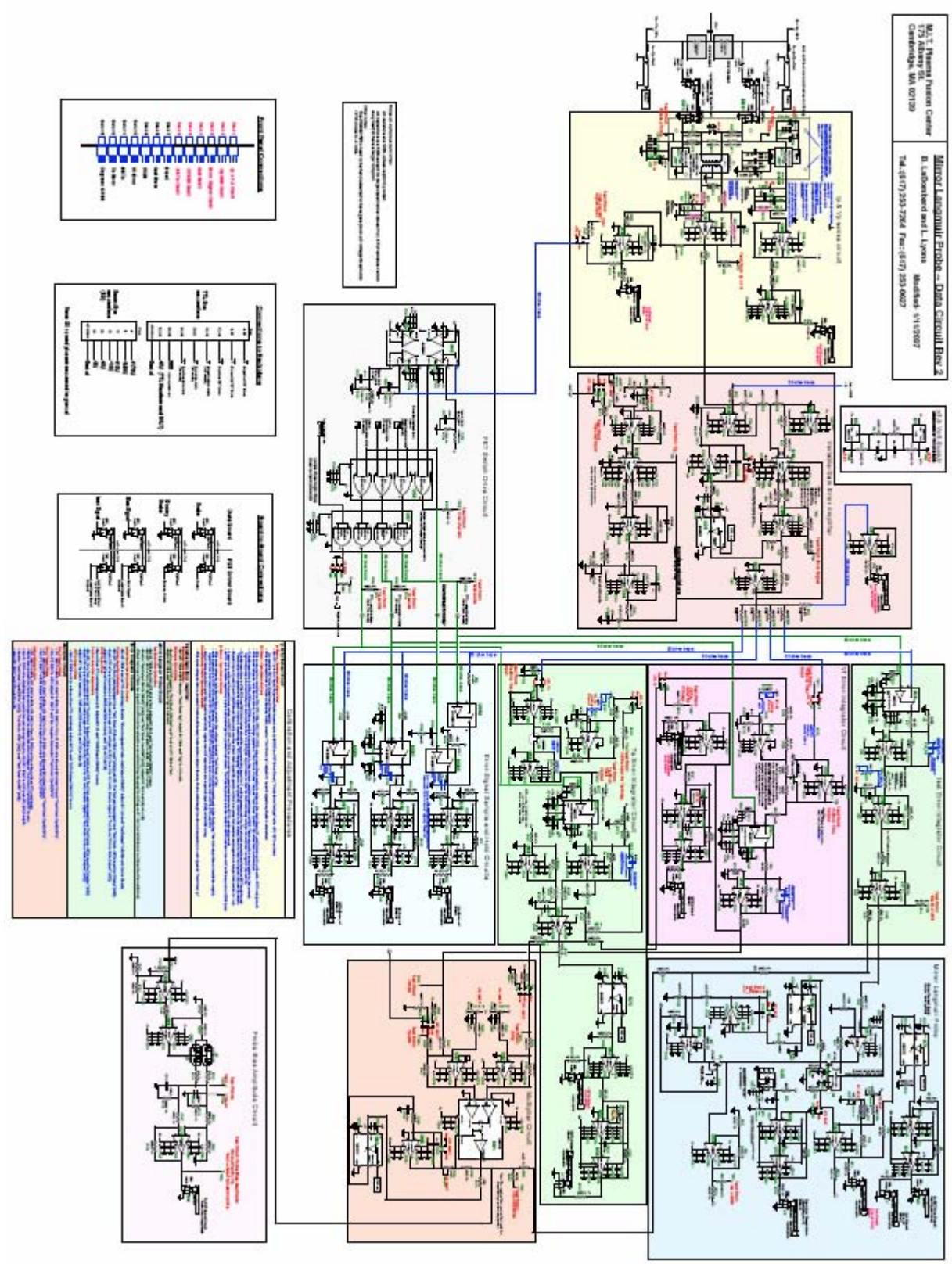
MLP Data Circuit



Mirror Langmuir Probe ~ Data Circuit Rev 2

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Modified- 1/11/2007

±2.5 Volt Supply

Locate close to THS7530 chips

Ip & Vp sense circuit

Note: ASP in-vessel coaxial wires are 6ft long

Test Point: Probe

Test Point: Dummy Probe

Test Point: Ip x 1.5

Test Point: Over-current signal input

-Ip Output 1.5V = 1A (fast) SMA1

Variable-Gain Error Amplifier

Test Point: Error Signal

Test Point: Vg

Test Point: VGA Isat Input

-Im x 4000

Isat Error-Integrator Circuit

Test Point: Vim/6 +1.875

Vf Error-Integrator Circuit

Test Point: Vf-Error VGA Output

Test Point: Vf-Error VGA Input

Test Point: -10/Te Input for Vf Integ

Te Error-Integrator Circuit

Test Point: -10/Te Input for Te Integ.

Test Point: Te-Error VGA Output

Test Point: Te-Error VGA Input

Mirror Langmuir Probe

Mirror Current Scale Factor: Im = Ip/8000

Isat Output 3V = 1A SMA7

Isat Output 1V = 1A (fast) SMA4

Transistor Temperature (10mV/degree K) SMA13

Test Points: Vf Bias Amplitude

FET Switch Drive Circuit

Test Point: Isat mode

Test Point: Over-Current

Test Point: Vf mode

Test Point: Te mode

Locate these logic chips close to card connector

Error-Signal Sample-and-Hold Circuits

Isat Error x 4 SMA8

Vf Error x 4 SMA10

10/Te Error x 4 SMA12

Multiplier Circuit

Test Point: -5/Te

Test Point: Vp/400

Test Point: -Vf/100

Test Point: (Vp-Vf)/(20Te)

Note: The length of this trace to C211 and U51 should be kept as short as possible

Notes on surface-mount sizes:

All resistors are 1206, unless explicitly noted.

All capacitors are 1206 except for large capacitance values (1uf, 4.7uf tantalum) which may need to have a larger footprint.

Other notes:

The 2N4392 FETs need to be hand-selected to have gate pinch-off voltage thresholds (VT0) close to -4 volts

Front Panel Connections

SMA 1	-Ip x 1.5 (fast)
SMA 2	-Vp/200 (fast)
SMA 3	Error Signal (fast)
SMA 4	Isat (fast)
SMA 5	-Vf/100 (fast)
SMA 6	-10/Te (fast)
SMA 7	3 Isat
SMA 8	Isat Error
SMA 9	Vf/50
SMA 10	Vf Error
SMA 11	30/Te
SMA 12	Te Error
SMA 13	Degrees K/100

Connections to Backplane

TTL Bus connections

Pins	
4, 36	X Negative FET Drive
8, 40	Y Grounded FET Drive
12, 44	Z Positive FET Drive
16, 48	J Negative bias state (Isat mode)
20 52	K Zero bias state (Vf mode)
24, 56	L Positive bias state (Te mode)
28, 60	PWR Low = power on
32, 64	+5V (TTL Waveform card ONLY)
all others	Ground

Power Bus connections (5A)

Pins	
4	+170V
8	-340V
12	+10V
16	-10V
20	+5V
24	-5V
all others	Ground

Note: All unused pins are connected to ground

Board-to-Board Connections

Data Board	FET Driver Board
Probe	Probe
Dummy Probe	Dummy Probe
Bias Signal	Bias Signal, Local Data Board Ground
Isat Signal	Isat Signal (Slow) 2.5 V => 1 amp, Local Data Board Ground

50Ω coax (316)

Calibration and Adjustment Procedures

Ip & Vp Sense Circuit:

Ip Sense - Common Mode Signal Null
- Set JP1_Ip = test. Apply large-amplitude square wave to BNC#2 on FET Drive Circuit, "Probe Drive Voltage" with JP3_FET = no load. (or operate FET Drive Circuit in off-line mode)
- With no connections to Probe or Dummy Probe, monitor "Test Point: Ip". Adjust C1_Ip until signal amplitude is minimized.

Vp Sense - Capacitance Balance
- With no capacitors installed in C70, C72, C65, C327, C77, C328, use a capacitance meter to measure the capacitance (C_pad) between the pad under R212 and ground.
- With same setup as in Ip Sense above, monitor voltage signals at "Test Point: Probe" (A) and "Test Point: Vp/400" (B) with a fast oscilloscope.
- (1) Add capacitors to C328, C325 and C326 as needed to compensate for the intrinsic parallel capacitance in R212. These capacitors compensate for the prompt, high-frequency overshoot behavior associated with a fast d(Vp)/dt. Adjust these so that the fast-switching voltage rise matches in signals (A) and (B).
- (2) Add capacitors to C70, C72 and C65 (total value should be approximately equal to C_pad) to compensate for the intrinsic capacitance between R212 and its pad. These capacitors quicken the signal response, removing an "RC charging" behavior in signal (B) relative to (A). Adjust these so that the signals (A) and (B) match.
- Repeat steps (1) and (2) until (A)/400 and (B) exactly overlay. Check that signal (B) quickly settles to a value that remains unchanged over longer time scales (> 1 us).
- If necessary, add small capacitance values to C327, C77 or C328 to increase the capacitance between R212's pad and ground.
- NOTE: use variable capacitors to aid in determining the optimal fixed values. The final capacitors must be rated for 500V and have low drift with temperature (C0G type).

Ip Sense - Capacitance Balance
- With same setup as in Ip Sense above, monitor the voltage signal at "Test Point: Ip" (A).
- Add capacitors to C327, C82 and C97 (Dummy Probe leg) as needed to balance the total capacitance in the Probe leg. The total capacitance should be roughly equal to the total capacitance of R212's pad plus C327, C77 and C328 in series with the total of C70, C72 and C65.
- Adjust these capacitors until the signal is null at (A). Again, low drift capacitors are required (type C0G) with 500V rating.

Probe/Dummy Probe Capacitance Match
- With same setup as above, connect Probe and Dummy Probe cables. Adjust Dummy Probe cable length (or discrete capacitor) to null signal at "Test Point: Ip"

Variable Gain Error Amplifier:

Maximum Gain Setting
- Set JP1_VGA = GND. Monitor "Test Point: Vg". Adjust R1_VGA until "Vg" is -1.5 volts.

Minimum Gain Setting
- Apply a +2 volt DC signal to "Test Point: VGA Isat Input" and set JP1_VGA = Test.
- Adjust R2_VGA until "Test Point: Vg" is -2.5 volts.

Mirror Langmuir Probe Circuit:

Ion Saturation Calibration
- Set JP_PWR = On. Set JP2_MLP = Test. Adjust R2_MLP until "Isat Output (SMA7)" is zero.
- Set JP1_MLP = Test, JP2_MLP = Run, JP_PWR = On, JP2_MULT = -0.5V, JP3_MULT = Test
- Monitor "Isat Output 3V=1A (SMA7)" [=(A)] and "Test Point: -Im/4000" [=(B)]. Adjust R1_MLP until (A) = 6 x (B).
- Check tracking of these two signals for different ion saturation current levels by changing the setting on R1_Isat (see Initial-Guess ion Saturation Current below).

Error Integrator Circuits:

Initial-Guess Ion Saturation Current
- Set JP_PWR = on (no TTL switching). Monitor "Mirror Langmuir Probe - Isat Output (SMA7)". Adjust R1_Isat until "Isat Output" is 0.030 volts (Isat = 10 mA).

Vf-Error Amplifier Adjustments
- Set JP1_Vf = Test, passing signal from "Test Point: Vf-Error VGA Input" [=(A)] and JP2_Vf = Test, passing signal from "Test Point: -10/Te Input for Vf Integ" [=(B)].
- Apply 250 mV p-p squarewave to (A) and a range of DC voltages to (B), from -2 to -0.1 volts. Monitor signal at "Test Point: Vf-Error VGA Output" [=(C)].
- Adjust R1_Vf (and if necessary 604Ω and 2KΩ resistors) until (C) = 0.2 (A)/(B).

Vf/40 Output Zero
- Run with no TTL switching (power-off). Adjust R2_Vf until "Vf/40 Ouput (SMA9)" is zero.

Te-Error Amplifier Adjustments
- Set JP1_Te = Test, passing signal to "Test Point: Te-Error VGA Input" [=(A)] and JP2_Te= Test, passing signal from "Test Point: -10/Te Input for Te Integ." [=(B)].
- Apply 250 mV p-p squarewave to (A) and a range of DC voltages to (B), from -2 to -0.1 volts. Monitor signal at "Test Point: Te-Error VGA Output" [=(C)].
- Adjust R1_Te (and if necessary 124Ω and 2KΩ resistors) until (C) = (A) x (B).

25/Te Output Offset
- Set JP_PWR = off (or = Run with no TTL switching). Adjust R2_Te until "25/Te Output (SMA11)" is zero.

Multiplier Circuit:

Zero X Input Offset
- JP1_MULT = GND, JP2_MULT = RUN, JP3_MULT = Test, JP_PWR = On. Record DC offset (Vox) at "Test Point: (Vp-Vf)/20Te".
- Set JP2_MULT= -0.5V. Adjust R1_MULT until Vox is again observed at "Test Point: (Vp-Vf)/20Te".

Zero Y Input Offset
- JP1_MULT = GND, JP2_MULT = RUN, JP3_MULT = Test. JP_PWR = On. Record DC offset (Voy) at "Test Point: (Vp-Vf)/20Te".
- Set JP1_MULT = -0.5V. Adjust R2_MULT until Voy is again observed at "Test Point: (Vp-Vf)/20Te".

Adjust Multiplier Gain
- JP1_MULT = GND, JP2_MULT = RUN, JP3_MULT = Run, JP_PWR = off (or = Run with no TTL switching).
- Wait a few seconds for the auto-zeroing circuit to reduce the offset voltage at "Test Point: (Vp-Vf)/20Te" to zero.
- Set JP_PWR = On, disabling the input to the auto-zeroing integrator. Set JP1_MULT = -0.5V and JP2_MULT =-0.5V.
- Monitor "Test Point: (Vp-Vf)/20Te" [=(C)], "Test Point: -5/Te" [=(A)] and "Test Point: Vp/400" [=(B)].
- Adust R3_MULT until (C) = -4 (A) x (B)

Probe Bias Amplitude Circuit

Test Points: Vmin, Vmax

Test Point: Probe Bias Amplitude Normalized by Te, Vout = [Max(Vp)-Min(Vp)]/Te

To FET Drive Circuit: Probe Bias Amplitude

Appendix B – Post Processing Methods to Compute Te, Vf, and Isat from Langmuir Probe Current and Voltage Data

Method 1

The pseudo-code for the M1 algorithm is as follows:

1) Record I & V values during the Isat states (averaging the I & V data over the times when the JTTL is high). Call them I_Isat, V_Isat.

2) Similarly record I & V values during Te and Vf states (call them I_Te, V_Te, I_Vf, V_Vf)

3) Using these, interpolate for I_* & V_* values for all state times (i.e., when J, K, or L are on)

4) Then for each state time, solve for Isat, Te and Vf in the expression: I_* = Isat*(EXP[(V_*-Vf)/Te]-1), where I_* and V_* agree with the measured/interpolated values at each state time. This non-linear equation is solved by iteration using a packaged IDL routine.

Method 2

The pseudo-code for the M2 algorithm is as follows:

1) Set initial values for Isat, Te and Vf. Update each parameter using equation 2.9 to solve for one parameter while holding the other two constant.

2) If J TTL signal is high, update Isat signal, else hold at last recorded value.

3) If K TTL signal is high, update Vf signal, else hold at last recorded value.

4) If L TTL signal is high, update Te signal, else hold at last recorded value.