CMOS Circuits for VCSEL-Based Optical IO

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Abstract

Electrical IO is becoming limited by copper interconnect channel losses that depend on frequency and distance. Package-to-package optical interconnects see negligible frequency-dependent channel losses, but data rates are limited by the intrinsic optical dynamics and electrical parasitics of the optical devices. This thesis presents 90nm CMOS front-end circuits which apply techniques to operate optical components beyond the intrinsic data rates imposed by these bandwidth limits.

The differential TIA is based on a proposed core amplifier which uses cross-coupled NMOS cascodes to increase gain and bandwidth. A symmetric feedback method provides constant gain from DC to 9GHz. The TIA operates at 12.5Gb/s with 260fF input capacitance and 18Gb/s with 90fF input capacitance for an input current of 200uA.

The presented VCSEL driver operates a standard commercial GaAs VCSEL at 18Gb/s by using pre-emphasis to compensate for the large capacitance and intrinsic optical dynamics of the VCSEL. The driver derives timing information directly from the full-rate input data and generates pre-emphasis pulses with width resolution less than one bit period in a manner that is compatible with full-rate IO architectures.

Because commercial GaAs VCSELS have limited bandwidth but short optical links often have excess link budget, multilevel signaling can be used to increase data rate by increasing the number of bits per symbol instead of increasing the symbol rate. A four-level (PAM-4) VCSEL driver architecture is therefore proposed to transmit at 20Gb/s with lower power consumption than the pre-emphasis driver due to reduced bandwidth requirements. Electrical and optical simulations of the transmitter circuits and behavioral simulations of a PAM-4 receiver and CDR are presented.

Thesis Supervisor: Anantha P. Chandrakasan
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Chapter 1

Introduction

1.1 Motivation for Optical Interconnect

As processing power scales exponentially with Moore's law, the total aggregate data bandwidth for communication between the components of high-performance computer systems must increase proportionally to prevent a communication bottleneck from limiting system performance. While electrical links have traditionally been employed for interconnects within computer systems, high-frequency loss and interference will eventually limit the performance of these links at high data rates. Optical links have already replaced electrical links for all long-haul data networks and high-performance local networks, and will become advantageous for ever shorter link lengths as data rates increase.

Package-to-package optical interconnects are characterized by many of the same design criteria as long-haul optical links. Ideally, both links are high-speed, low-power, compact, inexpensive, and easy to integrate. However, the relative importance of each of these metrics varies dramatically between the two applications. A long-haul link design may be optimized for speed at the expense of power and cost, but the balance for a package-to-package link is much more complex. The link still requires high speed, but the power consumption, cost, and size must simultaneously be limited to levels that allow the integration of highly parallel optical interconnects. Cleaved semiconductor lasers did not provide the performance required to make this type of
link technically and economically feasible, but vertical-cavity, surface-emitting lasers, (VCSELs) [1], have significantly lower threshold current and higher bandwidth and are therefore an attractive solution in this new design space constrained by power, area, and cost.

Figure 1-1 illustrates several package-to-package applications requiring increasing bandwidth in future technology generations, including links between processors, bridges, memory, and peripheral IO bridges. While it is clear that higher bandwidth and lower power are required, determining whether electrical or optical links provide better performance for a particular application requires a more complicated analysis based on knowledge of many optical and electrical system parameters. In the past decade, much research has been devoted to predicting when optical links will achieve superior performance as compared to electrical links. While predicting the answer to this question for future generations requires speculative assumptions about component performance, a framework for analyzing the effect of each parameter has recently been developed [3]. The work defines the metric of critical length, the link length at which an optical link consumes lower power than an electrical link for a specific set of performance criteria. The model demonstrates that the critical length is reduced for higher bit rates, improved optical devices, reduced optical insertion loss, and lower bit error rates. As scaling to higher bit rates is inevitable, this result indicates that improvements in optical devices have a direct impact on the performance improvement that can be achieved with optical interconnect. Because there are many variables in the performance analysis, the appropriate metrics for a specific interconnect cannot
be chosen without prioritizing and constraining the system parameters. For example, if a lower bound on bit rate is set a priori, then minimizing the mW/Gb/s subject to the bit rate constraint is appropriate. If an upper bound on power consumption is set instead, then the Gb/s can be maximized subject to this constraint. The relative importance of power consumption and data rate must be determined at the system level in order to arrive at the optimal link design.

Several recent works have made specific predictions regarding the time frame and application space in which optical IO will replace electrical IO. High-performance symmetric multiprocessor (SMP) server systems, in which two or more individual processors share common memory, require ever increasing data bandwidth in processor-processor and processor-memory links in order to maintain memory and cache coherency [4]. Recent research suggests that multiprocessor systems and network routers may benefit from intra-card package-to-package optical links as early as 2010 [4]. Even in single-processor systems, processor performance scaling drives an increased demand for bandwidth to memory. In memory applications, some have argued that the dominance of memory latency in commodity DRAM in determining memory access time will limit the potential impact of optics for this application [5]. However, while optics may have little impact on the physical latency to memory, system level research suggests that that architectural and software techniques applied in high performance systems to mitigate the impact of memory latency will drive increased demand for memory bandwidth [6]. The potential benefits of optical interconnect extend beyond sheer bandwidth performance. Total power consumption promises to become a limiting factor in parallel interconnects, and recent work suggests that optical links have a theoretical power advantage over electrical links in the 90nm node at 6Gb/s for critical lengths as short as 43cm [3], and decreasing length for higher data rates. The physical density of interconnect to the chip may also limit the maximum aggregate bandwidth in larger server systems. With the development of dense waveguide packages, optics will have the potential to provide higher linear bandwidth density by eliminating the need for low-loss controlled impedance electrical traces [7].

It is important to note that increases in the published data rates for short electrical
links have been partially facilitated by decreasing the distance between the transmitter and the receiver. For example, one recently published serial link achieved 20Gb/s but could operate at this maximum published rate over only 2 inches of copper [8]. Another electrical architecture with different equalization operates at the full 20Gb/s over 7 inch copper traces [9]. In contrast, optical signals are relatively insensitive to distance and could potentially be used to build flexible IO links to operate over distances between a few inches and a few meters. Such physical flexibility could allow new architectural innovations for high-performance systems.

For both optical and electrical links, maximizing the per-pin data rate is essential because the number of data pins will remain nearly constant across future technology generations [10]. Instead of channel limitations, optical links must overcome the bandwidth limitations of the optical components in order to achieve maximum performance. This requires the application of circuit techniques to compensate for the intrinsic and parasitic bandwidth limitations associated with the VCSEL and photodiode. CMOS front-end circuitry is the only practical choice for short-distance optical IO as it provides the maximum possible level of integration at the minimum cost.

1.2 Contributions

The three main contributions of this thesis are front-end building blocks designed in 90nm CMOS [11] to maximize the data rates achievable with commercially available optical components. They include a cross-coupled NMOS cascode TIA with 9GHz bandwidth, a digitally tunable pre-emphasis VCSEL driver for 18Gb/s operation, and a PAM-4 VCSEL driver operating at 10GSym/s (20Gb/s).

The feedback TIA is based on a proposed cross-coupled cascode voltage amplifier, which increases the gain and bandwidth of a standard cascode amplifier. The technique not only doubles the voltage gain, but also allows gain peaking to optimize the bandwidth by compensating for large load capacitance. A common-mode feedback biasing technique is introduced to eliminate the low-frequency gain reduction associated with standard symmetric feedback and extend the TIA bandwidth down...
to DC. This reduces the link overhead by allowing the transmission of data which is
not coded to eliminate low-frequency content. The TIA has a simulated bandwidth
of DC to 8.9GHz and measured results demonstrate operation at 12.5Gb/s for 260fF
of input capacitance and 18Gb/s for 90fF of input capacitance.

The presented 18Gb/s pre-emphasis VCSEL driver is among the fastest reported
CMOS drivers for a commercial GaAs VCSEL. Commercial GaAs VCSELs have sig-
nificant capacitance, typically 700fF, and are therefore limited by electrical parasitics
as well as intrinsic optical dynamics. In [12], falling edge pre-emphasis reduces the op-
tical fall time of experimental 990nm InGaAs VCSELs. These InGaAs devices have
smaller capacitance, typically 160fF, and are not significantly limited by electrical
parasitics [13]. Dual edge pre-emphasis compensates for both optical and electrical
limitations in GaAs VCSELs [14], but the reported architecture has a minimum pre-
emphasis pulse width of one bit period and requires phase tuning of the interleaved
clocks to minimize systematic jitter. The presented driver derives timing information
directly from the full-rate input data and generates pre-emphasis pulses with width
resolution less than one bit period in a manner that is compatible with full-rate IO
architectures.

A 20Gb/s multilevel (PAM-4) VCSEL driver architecture is proposed as an al-
ternative method to achieve higher data rates using standard 10Gb/s class devices.
Because short optical links are not typically limited by noise, the optical signal power
may be divided into several levels while maintaining an acceptable received bit error
rate (BER). When two bits are encoded in each four-level symbol, the symbol rate
for an equivalent data rate is reduced by a factor of two, which allows transmission of
20Gb/s PAM-4 data with frequency content comparable to 10Gb/s PAM-2 data. The
power consumption of the transmitter is reduced significantly, as this lower symbol
rate reduces power consumption in on-chip data paths and eliminates the need for
pre-emphasis of the VCSEL current. Extracted circuit simulations and optical rate-
equation simulations are presented for the PAM-4 driver. Behavioral simulations of
a PAM-4 receiver are presented and receiver complexity is compared for PAM-2 and
PAM-4 links.
Chapter 2

Background

Optical links are proposed as an alternative to electrical links, so this chapter begins with a short overview of basic link architectures and the current electrical state-of-the-art in Section 2.1 in order to place this work in context. Since the clock and data recovery (CDR) circuit architectures are similar for optical and electrical links, this overview also provides background for the discussion of PAM-4 CDR architectures in Chapter 5. In Section 2.2, the basic architecture of an optical link and the concept of the link budget are reviewed in order to provide an understanding of how the critical parameters of each component are combined to determine the overall link performance. Section 2.3 discusses recent research on manufacturable packaging methods for optical package-to-package interconnect. Finally, Section 2.4 describes the methods used to model the optical dynamics of VCSELs. Discussion of prior work on VCSEL drivers and transimpedance amplifiers is reserved for discussion within the respectively relevant chapters.

2.1 Link Architectures: Serial and Parallel

Traditional electrical links are typically divided into two categories: serial links and parallel links. Serial links are generally found in applications where a single channel is used to transmit the data, in which case using an additional channel to transmit a clock alongside the data would introduce unacceptable overhead. Therefore, as
illustrated in the basic serial link architecture of Figure 2-1, the data is transmitted without a forwarded clock and a clock and data recovery (CDR) architecture is used to recover both phase and frequency information from the incoming data and generate an appropriate receiver clock. Perhaps the most common method of clock recovery from random data is sampling the received data twice per bit period, where the data sample (D) nominally occurs in the center of the bit and the edge sample (E) nominally occurs at the transition. A bang-bang phase detector [15] compares each edge sample to the two adjacent data samples in order to decide if the data was sampled early or late. A charge pump then adjusts the VCO control voltage in the direction which moves the clock into alignment with the received optical data.

Serial links with full clock recovery require significant receiver complexity and therefore parallel links, which forward a clock in parallel with several data links, are often used in shorter distance applications when the clock path overhead may be amortized over many data channels. In older technologies, where data symbol periods were long compared to the propagation time in the channel, variations in propagation time were insignificant and the transmit clock could be used directly to retiming the receive data. However, as illustrated in the basic parallel link architecture of Figure 2-2, phase adjustment of the data on a per-pin basis is typically required in multigigabit links as channel delay variations are significant with respect to data rate [16], [17]. This requirement has increased the complexity of parallel links and has blurred the previously clear distinction between serial and parallel links. Perhaps modern links are more appropriately categorized by whether the transmitter and receiver share...
a common frequency reference. When no common reference is shared, the receiver must recover frequency and phase information directly from the incoming data. For short links with many channels, expanding the CDR to include this functionality may be more cumbersome than sharing a frequency reference. When a reference is shared, either directly or by a forwarded clock, the receiver must only recover the phase information and the CDR architecture is dramatically simplified.

Two 20Gb/s electrical links in 90nm CMOS demonstrating both embedded-clock and forwarded-clock architectures were presented at ISSCC 2006 [8], [9]. In addition to demonstrating different TX/RX architectures, the works illustrate the increased complexity of electrical links at high data rates, as both employ equalization in order to operate at 20Gb/s over only 2-7 inches of copper traces on FR4. In the embedded clock architecture [8], 3-tap equalization with 6b resolution is employed for pre-equalization at the transmitter and a linear equalizer is used at the receiver. Data is serialized and transmitted at 20Gb/s and the receiver uses eight comparators, 4× interleaving on both edges of a 5GHz clock, to recover the total of 40GSamples/second required for clock and data recovery. These data and edge samples are processed through a bang-bang detector and majority voter to adjust the phase of a local 10GHz LC-VCO. In the forwarded-clock architecture [9], the transmitter uses 4-tap equalization with 6b resolution for transmit pre-emphasis and a continuous-time
Figure 2-3: One possible hybrid architecture with shared reference clock

source-degenerated equalizer at the receiver. The receiver uses per-pin deskew in the form of an eight-stage DLL and phase interpolator to generate a four-phase clock to drive the 4× interleaved sampling comparators.

The simultaneous publication of both forwarded-clock and embedded-clock systems indicates that the choice between these two architectures is not yet obvious for short-distance links. Unlike long-haul links, where the overhead of sharing a frequency reference is clearly prohibitive, in shorter links with many data pins this overhead may be less onerous than the additional complexity of recovering both frequency and phase at each pin. Furthermore, in an architecture with TX/RX parallel links transmitting in both directions, use of a shared reference frequency could further simplify the architecture. Assuming PLLs are used at both ends of the link to generate low-jitter and high-frequency transmit clocks, simply locking both PLLs to a shared reference would guarantee identical frequency of the local clocks at both ends of the link. Then, local per-pin phase recovery could be used to align each receive clock to the incoming data as illustrated in Figure 2-3.

While clock and data recovery is not the focus of this thesis, behavioral modeling of a PAM-4 receiver to demonstrate the benefits of using edge selection to eliminate PAM-4 edges with bad timing information is a significant component of Chapter 5 and certain assumptions must be made about the CDR architecture in order to implement
such a system. The PAM-4 receiver architecture will assume that a full-rate clock is available, either from a directly forwarded clock or from a shared reference clock architecture such as the one illustrated in Figure 2-3. Timing recovery at the receiver is then implemented with a DLL and digital phase selection and interpolation, which may now occur at a lower loop bandwidth to minimize the jitter contributed by the bang-bang phase detector. Because DLLs are more stable than PLLs and can tolerate more latency in the feedback loop, this architecture also allows for CDR logic to be performed after deserialization in order to reduce power consumption. This will be particularly advantageous for PAM-4 clock recovery which requires more complex logic and is discussed in more detail in Chapter 5.

2.2 Optical Links: Components and Link Budget

At the most basic level, an optical link consists of a transmitter, channel, and receiver. The transmitter converts electrical data to a modulated optical signal, which then propagates through the channel and is converted back into the electrical domain at the receiver. Design constraints for links with different target applications place significantly different requirements on these three sub-systems. The design space for short-reach optical links prioritizes high data rate, low power, low cost, and compact form factor. This encourages the use of low-cost, highly integrated CMOS transmitter and receiver circuits and low-threshold current VCSEL devices. While longer links can compromise on cost, power, and form factor to achieve higher data rate, package-to-package links will not be practical without meeting challenging targets for each of these specifications. However, due to shorter link length and channel loss, transmit power and receiver sensitivity requirements are relaxed.

The link budget provides a mechanism for analyzing the system performance implications of each component. The signal and noise power at each stage in the transmission process are analyzed in order to guarantee that the signal power incident to the receiver allows acceptable system performance. A basic analysis of link budgeting is presented here for the specific case of a short optical link and further details
and theory may be found in most introductory texts on optical communications [18]. First, the power budget considerations for the transmitter, channel, and receiver are discussed and representative values are determined. Finally, an example link budget analysis using the determined values is presented.

2.2.1 VCSEL and Transmit Power

The vertical-cavity, surface-emitting laser (VCSEL) is a small laser device fabricated in the plane of the substrate. A light-emitting diode structure with a quantum well gain medium is fabricated inside an optical cavity consisting of two distributed Bragg reflectors (DBRs). The basic structure of a modern VCSEL is shown in Figure 2-4, which is reproduced from an invited paper presented in 2000 by the inventor of the VCSEL, K. Iga [1]. The VCSEL is ideal for short optical interconnects due to its small size, low threshold current, and suitability for array integration.

When a VCSEL is biased above threshold, the output power of the device is approximately a linear function of the junction current. The current through the device is modulated between two current levels (‘0’ and ‘1’) to transmit a binary signal. The
small-signal bandwidth of a VCSEL increases with the current and the lower bound on the ‘0’ current is therefore determined by the minimum bias over threshold that results in sufficient bandwidth. The upper bound on the ‘1’ current is imposed by power consumption, reduced laser efficiency due to device heating, and reliability concerns. Most commercially available high-speed 850nm VCSELs have a threshold current of 1mA to 2mA, a usable current range of about 2mA to 10mA, and a slope efficiency of between 0.3mW/mA and 0.5mW/mA [19, 20, 21]. In a typical transmitter design, the VCSEL might be modulated from 2mA to 8mA. If we assume a device with a threshold of 1mA and slope efficiency of 0.4mW/mA, this results in a ‘0’ power of 0.4mW and a ‘1’ power of 2.8mW. The average power is then 1.6mW (2.0dBm) and the optical modulation amplitude (OMA) is then 2.4mW (3.8dBm). This calculation is an example of the maximum power that can be transmitted with existing high-speed GaAs VCSELs. If lower power is required by the system constraints, the ‘1’ current may be reduced accordingly. However, if high-speed performance is of utmost importance and power consumption is secondary, the VCSEL might be biased with a larger average current and smaller OMA. In further discussions throughout this thesis, references to the transmitted optical power of the VCSEL refer to the modulation power or OMA, since this quantity is most significant for analyzing receiver performance. While only the modulation power aspect of VCSEL performance is considered here, further details on the high-speed performance and optical dynamics are found in Section 2.4. Once generated, this modulated optical signal is launched into the optical channel.

2.2.2 Optical Channel

Unlike the copper traces used for high-speed electrical interconnect, optical channels exhibit negligible frequency-dependent losses. From this perspective, the primary challenge for obtaining high-speed operation of an optical link lies in the electrical-optical and optical-electrical conversion. However, optical packages for short links play a critical role in providing a high quality optical channel and thereby maximizing system performance. For example, although coupling loss in the channel is
independent of frequency, it has a direct and often significant impact on the link budget through the relationship $P_{TX} - P_{LOSS} = P_{RX}$. A channel with significant coupling loss will impact the system by requiring increased transmit power or receiver sensitivity, both of which come at the expense of power consumption, area, and circuit complexity. Therefore, loss reduction as a result of ongoing research on optical integration [22],[23] will relax the design constraints on remaining system components and improve overall link performance. For this work, the worst case expected channel loss through the optical package is 12dB [22].

2.2.3 Receiver Sensitivity

Optical receivers typically consist of a photodiode and transimpedance amplifier and their important performance metrics are bandwidth and sensitivity. Receiver sensitivity is defined as the minimum received power that allows the receiver to resolve the signal with a specified bit error rate (BER) and is therefore a function of the total noise at the receiver due to both the photodiode and receiver circuits. Analysis of receiver sensitivity is generally quite complex, but may be simplified in most P-I-N diode receivers since the dominant causes of receiver degradation are limited to shot noise in the diode and input-referred noise from the receiver circuits. The interested reader may refer to [24], [25], [26], and [27] for a more detailed analysis.

In beginning an analysis of receiver sensitivity, it is helpful to first quantify the total equivalent input current noise, $I_{eq}^2$, since input current noise may be directly related to the signal photocurrent to determine the signal-to-noise ratio and therefore the sensitivity for a given BER [18]. It is important to note that $I_{eq}^2$ does not describe a real physical quantity, but is simply defined as the square of the total output voltage noise divided by the peak magnitude squared of the receiver transfer function, $R_t^2$, as in (2.1). The definition and calculation of $I_{eq}^2$ effectively refers the total output noise to the peak magnitude frequency of the receiver transfer function and allows direct comparison of this quantity to the received signal current if we assume that the signal power occurs within the band where $|Z_t(f)| \approx R_t$. (Here, the receiver transfer function is represented as $Z_t(f) = R_t H_t(f)$, where $Z_t(f)$ is the total receiver
transfer function, \( R_t \) is the peak magnitude, and \( H_t(f) \) is the amplitude-normalized, frequency-dependent component.)

\[
I_{neq}^2 \equiv \frac{V_{no}^2}{R_t^2} 
\]

To find \( I_{neq}^2 \), \( V_{no}^2 \) is first determined by integrating the output noise spectral density, \( v_{no}^2 \), over all frequencies as in (2.2). Next, (2.3) relates \( v_{no}^2 \) to the input-referred noise spectral density, \( i_{neq}^2 \), through the transfer function, \( Z_t(f) \). Finally, the \( R_t \) term is separated from the transfer function to reach a solution for \( I_{neq}^2 \) (2.4). Several methods exist for analytical calculation of the integrals when simplifying assumptions are made about the amplifier transfer function [28],[18],[27]. In this work, when considering the TIA design of Chapter 3, we will use simulation to determine the input-referred noise spectral density and then assume a noise equivalent bandwidth (NEB) to approximate the total equivalent input noise current.

\[
V_{no}^2 = \int_0^\infty v_{no}^2(f)df 
\]

\[
V_{no}^2 = \int_0^\infty i_{neq}^2 (f)|Z_t(f)|^2df 
\]

\[
I_{neq}^2 \equiv \frac{V_{no}^2}{R_t^2} = \int_0^\infty i_{neq}^2 (f)|H_t(f)|^2df 
\]

Once the total output voltage noise and total equivalent input current noise are calculated and a maximum allowable BER is specified, it is possible to calculate the minimum allowable received power. This sensitivity analysis is relatively simple for the particular case of optical receivers based on P-I-N diodes, as it has been previously shown that the noise is dominated by electronic receiver noise and that representing the noise as a signal-independent Gaussian distribution typically yields results accurate to within 1 dB [28]. Furthermore, because high-speed operation of VCSEL transceivers requires a relatively significant bias above threshold, the analysis
keeps the general case of a non-zero received power for the ‘0’ bit but assumes that
dark current in the diode is negligible.

To derive the probability of error, following the analysis of [18], we begin with the
assumption that the probability density function of the output voltage noise of the
transimpedance receiver is described by (2.5) and (2.6), where $V_n$ is taken from the
result of (2.3) and $v_0$ and $v_1$ are the nominal expected values of the output for either
a received ‘1’ or ‘0’.

$$P_0(v) = \frac{1}{\sqrt{2\pi}V_n} \exp\left(-\frac{(v - v_0)^2}{2V_n^2}\right)$$

$$P_1(v) = \frac{1}{\sqrt{2\pi}V_n} \exp\left(-\frac{(v - v_1)^2}{2V_n^2}\right)$$

If we define the voltage threshold of the decision circuit following the TIA to be
$v_t$ and assume that ‘1’ and ‘0’ are received with equal probability, then the total
probability of error is the average of the integral of $P_0(v)$ for $v > v_t$ and the integral
of $P_1(v)$ for $v < v_t$ as shown in (2.7). It is clear that the choice of threshold is
critical and it can be shown that the optimal threshold is exactly centered between
the two expected values if the noise present in the system is signal-independent and
the symbols occur with equal probability.

$$P_E = \frac{1}{2} \int_{v_t}^{\infty} \left[\frac{1}{\sqrt{2\pi}V_n} \exp\left(-\frac{(v - v_0)^2}{2V_n^2}\right)\right]$$

$$+ \frac{1}{2} \int_{-\infty}^{v_t} \left[\frac{1}{\sqrt{2\pi}V_n} \exp\left(-\frac{(v - v_1)^2}{2V_n^2}\right)\right]$$

These functions are not analytically integrable, so the function $Q(z)$ is defined to
simplify analysis (2.8).
By completing separate substitution of variables on (2.7), \( x=(v - v_0)/V_n \) for the first term and \( x=(v_1 - v)/V_n \) for the second term, (2.7) is expressed in terms of the \( Q \) function as in (2.9). Applying the further assumption that \( v_t \) is optimally centered at the average of \( v_0 \) and \( v_1 \), then \( v_1 - v_t = v_t - v_0 = \frac{v_1 - v_0}{2} \) and this expression is further simplified to (2.10).

\[
P_E = \frac{1}{2} Q\left(\frac{v_1 - v_t}{V_n}\right) + \frac{1}{2} Q\left(\frac{v_t - v_0}{V_n}\right) \tag{2.9}
\]

\[
P_E = Q\left(\frac{v_1 - v_0}{2V_n}\right) \tag{2.10}
\]

The function describes the total probability of error and may be referred back to the receiver input and parameterized with respect to the input power and the total equivalent input noise current \( I_{neq} \) (2.11), where \( R \) is the receiver sensitivity and \( P_0 \) and \( P_1 \) are the power levels received for ‘1’ and ‘0’.

\[
P_E = Q\left(\frac{R \cdot (P_1 - P_0)}{2 \cdot I_{neq}}\right) \tag{2.11}
\]

The required value of \( P_E \) is specified at the system level by the BER. In order to determine the minimum received modulated power, \( P_1 - P_0 \), a table of numerically computed values of \( Q(z) \) may be used to determine the required value of the \( Q \)-function argument, \( Q_F \), for the specified BER. Figure 2-5 plots this calculation and illustrates the required \( Q_F \) values for common BER specifications. It is useful to remember that we require approximately \( Q_F=6 \) for a BER of \( 10^{-9} \), \( Q_F=7 \) for a BER of \( 10^{-12} \), and \( Q_F=8 \) for a BER of \( 10^{-15} \). Once the BER is chosen and the total equivalent input current noise is determined, the required input power may be
Figure 2-5: Q-function calculation for BER=[10^{-9}, 10^{-12}, 10^{-15}]

calculated as in (2.12) and the associated receiver sensitivity is calculated as in (2.13).

\[ P_1 - P_0 = \frac{2 \cdot Q_F \cdot I_{neq}}{R} \]  \hspace{1cm} (2.12)

Sensitivity = 10\log\left(\frac{P_1 - P_0}{1\text{mW}}\right) \hspace{1cm} (2.13)

Details on the analysis of \( I_{neq} \) and determination of the sensitivity for the designed receiver are provided in Chapter 3. The worst case result is -10dBm at a BER of \(10^{-12}\), which is comparable to other reported CMOS receivers designed for 10Gb/s operation.

2.2.4 Example Link Budget Analysis

The link margin is defined as the difference between the received power and the receiver sensitivity, and must be positive to ensure that the link meets the target specifications. For the example case, assume that the VCSEL transmits 0dBm optical
power. Subtracting a typical link loss of 8dB leaves a received power of -8dBm, which is 2dB greater than the worst-case expected receiver sensitivity of -10dBm and will therefore result in correct link operation. In practice, many additional factors and noise sources may be included in the link budget analysis. Details may be found in [18], but this basic example provides a starting point for a simple link budget analysis.

2.3 Integration and Packaging Methods

Demonstration of compact, cost-effective, manufacturable packaging and integration techniques is necessary in order for optical package-to-package interconnects to become a practical alternative to electrical links in short-reach systems. As a result, a significant amount of recent industry research has focused on the implementation of such techniques. Many variations with different advantages and challenges have been proposed and are summarized in this section.

2.3.1 Single Wavelength

Parallel single-wavelength links were the first proposed alternative and remain the best candidates for practical integration in the near term. Alternate package architectures have been proposed by Intel in [22] and [23] and by the Terabus project in [29]. The two packages are illustrated for comparison in Figure 2-6.

The Intel package of Figure 2-6(a) provides dual 1x12 optical channels to the same CMOS chip to allow simultaneous transmit and receive. This is accomplished by flip-chip bonding the CMOS chip and the 1x12 optical component arrays to a small organic substrate and making an electrical connection between them with short copper traces. This approach is attractive as the manufacturing techniques are more mature than those proposed by the Terabus project and because the thermal coupling between the CMOS and optical components is dramatically reduced, which will improve VCSEL performance and reliability. However, the traces connecting the CMOS and optical components are several millimeters long and must therefore be treated as transmission lines at higher data rates. For example, the 10GHz funda-
mental of 20Gb/s data has a wavelength of 1.4cm assuming a substrate with a relative permittivity of 4.4. These short traces are near the boundary where traces must be treated as transmission lines, which occurs when their length exceeds one-tenth of the shortest wavelength [30], which in this case occurs at 1.4mm. A terminated driver was therefore designed for use with this package architecture.

The Terabus package of Figure 2-6(b) provides a 4×12 single-direction optical channel from a CMOS transmitter chip to a CMOS receiver chip. The front of the CMOS chip is first bonded to a silicon carrier with through-silicon vias and surface wiring to provide power and electrical signals to the transmitter or receiver. A 4×12 VCSEL or photodiode array is then flip-chip bonded to the sub-assembly consisting of the CMOS chip and silicon carrier - the optical devices are bonded front-to-front with the CMOS chips but etched lenses allow optical coupling through the back side. This entire assembly is bonded to an optical card and waveguide, so the optical signals are then turned at a right angle with gold plated mirrors into a polymer waveguide mounted on the board. While the package does not integrate transmit and receive functionality onto a single chip, it provides higher aggregate data capacity for a one-way link, and future dual-direction link implementation is not precluded. The integration process, which is more complex than that of the Intel package, allows direct integration of the VCSEL and photodiode onto the CMOS chip. This allows the use of high-impedance VCSEL drivers, which provide power savings as compared with terminated drivers. However, VCSEL reliability and performance issues resulting from the close thermal coupling of the VCSEL and CMOS in this design require careful thermal management.
2.3.2 Multiple Wavelength

In addition to the described single-wavelength links, multi-wavelength coarse wavelength-division multiplexing (CWDM) has been proposed to increase the total aggregated data rate for an interconnect limited system [31]. This proposed package, which provides a one-direction 1×12×4λ optical channel, is illustrated in Figure 2-7. The CMOS chip is used as a base for the assembly and includes a 4×12 array of sites for flip-chip bonding optical components and an additional set of pads around the perimeter for wire bonding the CMOS to the package substrate. Four 1×12 arrays of optical components are flip-chip bonded front-to-front with each CMOS chip to provide the four wavelengths of 990nm, 1020nm, 1050nm, and 1080nm. The devices are bottom-emitting and the optical signals are therefore coupled out through lenses etched in the back surface of the optical components. A silicon seal ring is bonded to the CMOS to provide a hermetic seal and set the spacing between the CMOS base and the optical MUX/DEMUX. Optical MUX/DEMUX devices are then bonded to the seal ring. These components allow the transmission of 48 optical signals through 12 fibers by combining one signal of each wavelength into each physical channel. Finally, an alignment structure is bonded to the top of the stack to allow physical alignment with standard optical MT connectors. Development of manufacturable integration methods for wavelength division multiplexing will facilitate higher data density, but as optical multiplexing occurs after the electrical to optical conversion, it will not influence the design of the interface circuits unless different methods for the CMOS interface to the optical components are required.
2.4 Modeling Methodologies

While accurate compact models for transistors already exist and photodiodes may be simply modeled as capacitors, VCSEL modeling for circuit design applications is a relatively new area of research and selection/implementation of an appropriate model is an important part of any driver design endeavor. This section discusses model requirements and reviews prior work. The selected model is fit to data published in the literature for a commercial GaAs VCSEL [21]. This device was selected since the paper presented the most complete set of electrical and optical data for fitting the model.

2.4.1 Model Requirements and Prior Work

VCSELs may be simulated at many levels of detail. Full finite-element simulations may be required to model the most complex effects, but these types of simulations are computationally intensive and incompatible with standard circuit simulation environments. However, simple rate equations with no consideration of spatial dependence do not model effects such as carrier diffusion and spatial hole burning and may be inappropriate for simulations requiring high levels of accuracy.

In order to select an appropriate level of model complexity, it is necessary to consider both the availability of suitable characterization data and the intended use of the model. Since the model parameters must be fit to the actual VCSEL device, the model complexity should not exceed the available level of device characterization data. For the case of the VCSEL driver design, it is important for the VCSEL model to capture the AC and DC characteristics of the VCSEL output power and the electrical parasitics of the VCSEL. Furthermore, given the limited interaction between VCSEL suppliers and circuit designers, the model should contain only parameters that may be approximated from the literature or fit to the VCSEL using relatively simple measurements such as S-parameter data. Model accuracy near threshold is not essential because bandwidth limits at lower bias currents prevent high-speed drivers from operating VCSELs in this range. Given these constraints, models based on rate
equations are the most appropriate choice.

Much of the relatively recent work on rate equation models has investigated methods of transforming the spatiotemporal rate equations into systems of ordinary differential equations [32], [33], [34], [35], [36], [37]. This approach assumes an arbitrary number of optical mode profiles a priori, represents the electrical carrier density as a finite set of terms in a Bessel series expansion, and leaves weighting coefficients for the carrier densities in each optical mode and series expansion term as the only unknowns during simulation. This method is flexible and may be used to retain either radial or radial and azimuthal dependence and for an arbitrary number of optical modes. However, the fitting of these models requires knowledge of the mode profiles of the VCSEL and since this kind of data is rarely reported in literature or data sheets, a spatially-independent rate equation model is much more practical. Recent work [38] has demonstrated that such models may be used in conjunction with simplified linear electrical VCSEL models to provide sufficient accuracy for opto-electronic co-simulation of VCSEL drivers using 10Gb/s GaAs VCSELs.

2.4.2 Electrical Model

An electrical VCSEL model must be developed in order to simulate the electrical interaction of the VCSEL with the driver circuits. A diode junction model and appropriate parasitic capacitances and resistances may be used in conjunction with the intrinsic rate equation model to provide a complete description of the laser. However, this requires co-simulation of Verilog-A and may result in convergence issues in some simulators. If the VCSEL will only be operated above threshold, the diode model is nearly linear and may be modeled as a resistor and voltage source in series for ease of simulation. Parasitics associated with the package, the bond pad, and the DBR are reported to be constant across bias and may therefore be included as linear elements from the standard circuit simulator. The complete electrical model is shown in Figure 2-8, where \( R_P = 90\Omega \), \( C_P = 50\text{fF} \), \( R_{DBR} = 19\Omega \), \( C_J = 700\text{fF} \), and a 1.5V source and 45Ω resistor were substituted in series for the intrinsic diode [21]. The current flowing through the VCSEL junction was exported from Cadence and optical
2.4.3 Optical Model

The following analysis of optical rate equation dynamics, expanded from a recent paper on rate equation modeling of VCSEL devices [38], is described in sufficient detail to allow its implementation and use by other circuit designers. The equations of (2.14) and (2.15) describe the interaction of photons and electrons when the effect of the separate confinement heterostructure (SCH) is neglected. The carrier densities experience relaxation oscillations in response to sudden changes in the injected current which result in overshoot of the VCSEL output power. Attempts to fit this model to the measured VCSEL data yielded small-signal AC results with excess gain peaking which would cause any transient simulations to predict pessimistic levels of overshoot. This suggests that an addition real source of damping may be neglected by this model.

\[
\frac{dP}{dt} = -\left[\frac{1}{\tau_p}\right] P + \left[\frac{\Gamma\beta}{\tau_N}\right] N + \Gamma g_0 v_g \left[\frac{N - N_{tr}}{1 + \epsilon P}\right] P \tag{2.14}
\]

\[
\frac{dN}{dt} = \left[\frac{\eta_n}{qV}\right] I - \left[\frac{1}{\tau_N}\right] N - g_0 v_g \left[\frac{N - N_{tr}}{1 + \epsilon P}\right] P \tag{2.15}
\]

Adding a third equation to model the interaction between the electrons in the quantum wells and the electrons in the SCH yields a better-matched result since
this effect increases the damping of the photon-electron interaction and reduces over-
shoot. The variables P, N, and M represent, respectively, the photons, electrons in
the quantum well, and electrons in the SCH.

\[
\frac{dP}{dt} = -\left[\frac{1}{\tau_p}\right] P + \left[\frac{\Gamma \beta}{\tau_N}\right] N + \Gamma g_0 v_g \left[\frac{N - N_{tr}}{1 + \epsilon P}\right] P \tag{2.16}
\]

\[
\frac{dN}{dt} = \left[\frac{1}{\Gamma_q \tau_{cap}}\right] M - \left[\frac{1}{\tau_N} + \frac{1}{\tau_{esc}}\right] N - g_0 v_g \left[\frac{N - N_{tr}}{1 + \epsilon P}\right] P \tag{2.17}
\]

\[
\frac{dM}{dt} = \left[\frac{\Gamma_q \eta_t}{q V}\right] I - \left[\frac{1}{\tau_{cap}}\right] M + \left[\frac{\Gamma_q}{\tau_{esc}}\right] N \tag{2.18}
\]

By setting the time derivatives equal to zero and solving the equations of (2.16)-(2.18) the DC solution given in (2.19)-(2.24) is obtained. (The results for \(N_0\) and \(P_0\) are also valid for the solution of the rate equations of (2.14)-(2.15).)

\[
P_0 = -b + \sqrt{b^2 - 4ac} \frac{I_0}{2a} \tag{2.19}
\]

\[
N_0 = \frac{\tau_n}{(1 - \beta)} \left(\frac{1}{\Gamma_{\tau_p}} S_0 + \frac{\eta_t}{q V} I_0\right) \tag{2.20}
\]

\[
M_0 = \tau_{cap} \left[\frac{\Gamma_q \eta_t}{q V} I_0 + \frac{\Gamma_q}{\tau_{esc}} N_0\right] \tag{2.21}
\]

\[
a = \frac{\tau_n g_0 v_g + \epsilon}{\Gamma_{\tau_p}(1 - \beta)} \tag{2.22}
\]

\[
b = g_0 v_g N_{tr} + \left[\frac{1}{\Gamma_{\tau_p}(1 - \beta)}\right] - \left[\frac{\eta_t}{q V}\right] \left[\frac{\tau_n g_0 v_g + \beta \epsilon}{(1 - \beta)}\right] I_0 \tag{2.23}
\]

\[
c = -\left[\frac{\eta_t \beta}{q V(1 - \beta)}\right] I_0 \tag{2.24}
\]

The AC solution to the rate equations may be found by expanding the non-linear
term using the linearization term given in (2.25).
\[
\begin{align*}
\left[ N - N_{\text{tr}} \right] P & \approx \left[ \frac{NP_0}{1 + \epsilon P_0} + \frac{P(N_0 - N_{\text{tr}})}{(1 + \epsilon P_0)^2} \right] \\
(2.25)
\end{align*}
\]

The linearized versions of the rate equations giving the AC solution \((P,N,M)\) around any given DC operating point \((P_0,N_0,M_0)\) are given in (2.26)-(2.28).

\[
\begin{align*}
\frac{dP}{dt} & = -\left[ \frac{1}{\tau_p} \right] P + \left[ \frac{\Gamma \beta}{\tau_N} \right] N + \Gamma g_o v_g \left[ \frac{NP_0}{1 + \epsilon P_0} + \frac{P(N_0 - N_{\text{tr}})}{(1 + \epsilon P_0)^2} \right] \\
(2.26) \\
\frac{dN}{dt} & = \left[ \frac{1}{\Gamma q \tau_{\text{cap}}} \right] M - \left[ \frac{1}{\tau_N} + \frac{1}{\tau_{\text{esc}}} \right] N - g_o v_g \left[ \frac{NP_0}{1 + \epsilon P_0} + \frac{P(N_0 - N_{\text{tr}})}{(1 + \epsilon P_0)^2} \right] \\
(2.27) \\
\frac{dM}{dt} & = \left[ \frac{\Gamma q \eta_i}{qV} \right] I - \left[ \frac{1}{\tau_{\text{cap}}} \right] M + \left[ \frac{\Gamma q}{\tau_{\text{esc}}} \right] N \\
(2.28)
\end{align*}
\]

After taking the Laplace transform, (2.28) may be solved for \(M\) as a function of \(I\) and \(N\) as in (2.29). This result is then substituted into the Laplace transform of (2.27) and the similar terms collected to give (2.30) and the terms of the Laplace transform of (2.26) are collected to give (2.31), with the constants (2.32)-(2.35) defined for readability.

\[
M = \frac{\tau_{\text{cap}} \Gamma q}{(1 + s \tau_{\text{cap}})} \left[ \frac{\eta_i}{qV} I + \frac{1}{\tau_{\text{esc}}} N \right] \quad (2.29)
\]

\[
N \left[ s + k_3 + \frac{1}{\tau_{\text{esc}}} \right] - \frac{1}{\tau_{\text{esc}}(1 + s \tau_{\text{cap}})} = \left[ \frac{\eta_i}{qV(1 + s \tau_{\text{cap}})} \right] I - k_4 P \quad (2.30)
\]

\[
P \left[ s + k_2 \right] = k_1 N \quad (2.31)
\]

40
\begin{align*}
  k_1 &= \frac{\Gamma \beta}{\tau_n} + \frac{\Gamma g_0 v_g P_0}{1 + \epsilon P_0} \quad (2.32) \\
  k_2 &= \frac{1}{\tau_p} - \frac{\Gamma g_0 v_g (N_0 - N_{tr})}{(1 + \epsilon P)^2} \quad (2.33) \\
  k_3 &= \frac{1}{\tau_n} + \frac{g_0 v_g P_0}{1 + \epsilon P_0} \quad (2.34) \\
  k_4 &= \frac{g_0 v_g (N_0 - N_{tr})}{(1 + \epsilon P_0)^2} \quad (2.35)
\end{align*}

Finally, (2.30) and (2.31) are combined to the result of (2.36) which gives the AC solution for the photon density as a function of only the AC input current.

\[ P \left[ (s + k_2) \left( s + k_3 + \frac{1}{\tau_{esc}} - \frac{1}{\tau_{esc}(1 + s\tau_{cap})} \right) + k_1 k_4 \right] = \left[ \frac{\eta k_1}{qV(1 + s\tau_{cap})} \right] I \quad (2.36) \]

Note that if at this point we let \( \tau_{cap} = 0 \) and \( \tau_{esc} = \infty \) then this result simplifies to the AC solution of the rate equations with no SCH. In that case we would find the modulation transfer function (MTF) of (2.37).

\[ P = \left[ \frac{A}{s^2 + \gamma s + \omega_0^2} \right] I \quad (2.37) \]

\[ A = \frac{\eta k_1}{qV} \quad (2.38) \]

\[ \gamma = k_2 + k_3 \quad (2.39) \]

\[ \omega_0^2 = k_2 k_3 + k_1 k_4 \quad (2.40) \]

If, instead, we keep the extra terms we can use the definition of (2.41) to simplify the solution and the MTF of (2.37) is modified to include the sub-terms of (2.42)-(2.44).
Figure 2-9: AC comparison of measurements and model

\[ \chi = 1 + \frac{\tau_{cap}/\tau_{esc}}{1 + s\tau_{cap}} \]  \hspace{1cm} (2.41)

\[ A = \frac{\eta_1 k_1}{(qV)(1 + s\tau_{cap})(\chi)} \]  \hspace{1cm} (2.42)

\[ \gamma = k_2 + \frac{k_3}{\chi} \]  \hspace{1cm} (2.43)

\[ \omega_0^2 = \frac{k_2 k_3 + k_1 k_4}{\chi} \]  \hspace{1cm} (2.44)

### 2.4.4 Model Fitting

The existence of analytical DC and AC solutions allow efficient model fitting. A detailed analysis of the sensitivity of the VCSEL parameters is presented in [38], which concludes that a majority of the VCSEL parameters may be set based on their design values or taken from the literature but that the performance is strongly dependent on the accuracy of a select set of parameters which must therefore be
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
<th>Equation</th>
<th>Description</th>
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<tr>
<td>$r$</td>
<td>$4E^{-4}$</td>
<td>cm</td>
<td>-</td>
<td>VCSEL Radius</td>
</tr>
<tr>
<td>$dQW$</td>
<td>$10E^{-7}$</td>
<td>cm</td>
<td>-</td>
<td>Quantum Well Thickness</td>
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<td>-</td>
<td>Number of Quantum Wells</td>
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<td>$L$</td>
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<td>$\frac{2 \pi nQW \cdot dQW}{L}$</td>
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</tr>
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<td>-</td>
<td>-</td>
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<td>-</td>
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<td>W$\cdot$Photon$^{-1}$</td>
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<td>Output Power: POW=$kP$</td>
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</tbody>
</table>

Table 2.1: Estimated and extracted VCSEL parameters used in simulations
extracted from measured results. It was therefore determined that $g_0$, $\epsilon$, $\eta_i$ and $\tau_{cap}$ should be fit to the measurement data.

The measurement data for the VCSEL was provided in the form of a model fit to the MTF at several bias currents between 1mA and 9mA [21]. It was assumed that this measurement was obtained by measuring the VCSEL through a 50$\Omega$ transmission line and that the incoming wave therefore saw 50$\Omega$ in parallel with the VCSEL parasitics to mitigate the bandwidth limitations. Therefore, in order to fit the AC results to the measurement, the AC junction current applied to the rate equation model of (2.37) was first shaped by an electrical low-pass filter describing this measurement condition.

A gradient descent optimization method was used to minimize the mean-square-error (MSE) between the measured and modeled results across several bias currents. The final set of parameters chosen are given in Table 2.1. The comparison of the measured data and the AC solution of the model with the fitted parameters is shown in Figure 2-9. At biases below 2mA the model begins to predict excessive peaking, but since the VCSEL will not be operated in this range, the close fit at and above 2mA is sufficient.

### 2.5 Summary

This chapter reviewed the basics of link architectures and discussed the present performance and limitations of electrical serial links in order to motivate the future need for optical package-to-package interconnect. Optical links and the concept of link budget were introduced, along with a summary of the performance of commercial optical components and the techniques necessary to perform the receiver sensitivity analysis of Chapter 3. A brief review of the different types of optical-electrical packaging provided context for the VCSEL driver design decisions of Chapter 4. Finally, the VCSEL models used to simulate the PAM-4 transmitter in Chapter 5 were derived and compared to measured VCSEL data.
Chapter 3

Cross-Coupled Cascode TIA

The transimpedance amplifier performs the optical to electrical conversion at the receiver. It must overcome large input capacitance to achieve high bandwidth while simultaneously providing high gain in order to reduce the total input-referred noise of the receiver. If the following circuits are differential, the TIA must also perform a single-ended to differential conversion on a received optical signal which contains a DC offset proportional to the average VCSEL power. This chapter reviews basic TIA theory, defines the TIA specifications for this link, describes the core voltage amplifier and feedback TIA, and presents alternatives for TIA biasing.

3.1 TIA Theory and Specifications

To optimize the trade-off between noise integration and ISI, a TIA should have a closed-loop bandwidth of seven-tenths of the bit rate for standard NRZ data transmission in order to achieve a sufficiently open eye without integrating unnecessary noise due to excess bandwidth [15]. Assuming that a standard feedback topology is used, the overall TIA bandwidth and gain characteristics are determined by the input capacitance, internal voltage amplifier gain, and feedback resistance. When input and output specifications are defined a priori, the required values of these circuit metrics are well constrained.

In order to achieve a data rate of 12.5Gb/s, the TIA design targets a bandwidth of
10GHz. If we temporarily assume that the core voltage amplifier has sufficient bandwidth that its poles do not interact with the dominant pole defined by the photodiode capacitance and input resistance, the simplified figure of Figure 3-1 then allows the definition of the remaining block-level specifications. The photodiode capacitance is 250fF and will dominate the input capacitance since the amplifier gate capacitance may be chosen to be as low as 20% of the photodiode capacitance without significantly degrading noise performance [39]. Therefore, assuming a total input capacitance of $C_{PD}=250\text{fF}$, the input resistance, $R_{IN}$, must be $64\Omega$ in order to place the dominant pole at 10GHz. The transmitted power and optical coupling losses in the channel predict a received current of 200µA peak-to-peak and the following LIA stage requires a differential input voltage of $2\times50\text{mV}$, so the closed-loop transimpedance gain, $V_O/I_S$, must be $2\times250\Omega$. Given these constraints, the required voltage amplifier gain may be determined from the relationship $V_O/I_I = (-A)(R_{IN})$ and is found to be $A=7.8$. This is equivalent to a gain of ±3.9 from the single-ended input to each differential output. Finally, the required value of the feedback resistor ($R_F$) is determined by $R_F = (R_{IN})(1 + \frac{A}{2})$, yielding a value of 314Ω.

In practice, the analysis becomes more complex as TIAs for high data rate applications employ realistic core voltage amplifiers with finite bandwidth and non-zero input capacitance. Nevertheless, the foregoing first-order analysis provides insight into the interaction of the various system-level parameters. Simulations of bandwidth and phase margin may be used for optimization and validation.
3.2 High-Speed Receivers: Prior Work

TIA circuits have been a research topic of interest for several decades, initially due to their many applications in high-speed, long-haul optical links and more recently for shorter distance applications. There is a large body of work in the field covering a wide range of target applications, but in the interest of brevity only the most recent and relevant results are summarized in this section. The interested reader may find a more detailed summary and analysis of traditional TIA topologies in [15]. These common topologies include the open-loop common-gate TIA and the feedback TIA consisting of a common-source input stage, source-follower buffer, and resistor feedback network. The latter may be implemented in either single-ended or pseudo-differential form. In this section, a summary of recent performance of linear TIA circuits is presented and then a few recent papers on alternatives to the traditional linear TIA are considered.

3.2.1 Linear TIA Receivers

TIA designs are categorized by several distinguishing characteristics including whether they are differential or single-ended, whether they require inductors, and whether they are open-loop or feedback. Their performance may be characterized by several metrics, including power consumption, bandwidth or data rate, sensitivity, and gain. Differential TIA topologies are more tolerant of supply and substrate noise and interface more easily with following stages which are commonly differential. Therefore, a differential topology is proposed in this thesis, but both single-ended and differential circuits are reviewed here for completeness.

Recent work on single-ended TIA topologies is summarized in Table 3.1. One work, [40] proposes adding a floating current mirror to the common-gate topology, for the purpose of making the output bias independent of input current. While this TIA achieves low-power and high bandwidth in an older CMOS process, the gain falls significantly short of other reported topologies. Another, [41] proposes adding a resonant network including several inductors to optimize the bandwidth of a cascoded common-source/source-follower feedback topology. While the bandwidth
<table>
<thead>
<tr>
<th>Process</th>
<th>$C_{PD}$</th>
<th>Power</th>
<th>Sensitivity $\text{BER} = 10^{-12}$</th>
<th>BW/ Rate</th>
<th>L?</th>
<th>Gain</th>
<th>Cit.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25$\mu$m</td>
<td>-</td>
<td>1.6mW</td>
<td>-10.6dBm</td>
<td>12.5Gb/s</td>
<td>No</td>
<td>42.2dBΩ</td>
<td>[40]</td>
</tr>
<tr>
<td>0.18$\mu$m</td>
<td>500fF</td>
<td>137mW</td>
<td>-18dBm</td>
<td>9.2GHz</td>
<td>Yes</td>
<td>54dBΩ</td>
<td>[41]</td>
</tr>
<tr>
<td>90nm</td>
<td>320fF</td>
<td>2.2mW</td>
<td>-8dBm</td>
<td>13.4GHz</td>
<td>Yes</td>
<td>52dBΩ</td>
<td>[43]</td>
</tr>
</tbody>
</table>

Table 3.1: Prior work: single-ended transimpedance amplifiers

and sensitivity performance is impressive, it comes at a cost of large area and high power consumption. A TIA based on a regulated cascode is proposed in [42], and a version modified for lower voltage operation is proposed in [43] and provides low power consumption and relatively high bandwidth, though the 20GHz performance claimed in the paper title is reduced to 13.4GHz in the presence of diode capacitance. The topology requires two inductors and has somewhat lower sensitivity than other reported work.

Differential TIA topology performance is summarized in Table 3.2. In [44], which reports an implementation of the multistage Cherry-Hooper topology of [45] in an updated technology, few circuit details are provided in the paper and the TIA has high gain but consumes significant power. An interesting differential Cherry-Hooper amplifier with inductive peaking is reported in [46]. In [47], a differential amplifier with regulated cascode input stages and transformer inductive peaking achieves good bandwidth, gain, and sensitivity but the input capacitance is relatively small and the power consumption is not reported separately for the TIA stage. An AC coupled and differential version of the TIA described in [40] is fabricated in a newer CMOS technology [48] and is competitive in all performance metrics, but requires inductors. A TIA based on three-stage CMOS inverter amplifiers with resistive feedback is reported in [49]. Two such amplifiers, one with the real photodiode input and one with a dummy input, are connected with symmetric resistive feedback around the second stage which claims to reduce the effect of power supply noise. The gain is relatively high, which is expected as a result of the three stage gain topology. Finally, while most of the differential TIA circuits summarized here actually rely on a single-ended input and a reference voltage or current to generate a differential output, the TIA
Table 3.2: Prior work: differential transimpedance amplifiers

<table>
<thead>
<tr>
<th>Process</th>
<th>$C_{PD}$</th>
<th>Power</th>
<th>Sensitivity</th>
<th>BW/Rate</th>
<th>L?</th>
<th>Gain</th>
<th>Cit.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.18μm</td>
<td>150fF</td>
<td>108mW</td>
<td>-</td>
<td>9GHz</td>
<td>No</td>
<td>62dBΩ</td>
<td>[44]</td>
</tr>
<tr>
<td>0.18μm</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>6GHz</td>
<td>Yes</td>
<td>-</td>
<td>[46]</td>
</tr>
<tr>
<td>0.18μm</td>
<td>150fF</td>
<td>-</td>
<td>-12dBm</td>
<td>8GHz</td>
<td>Yes</td>
<td>53dBΩ</td>
<td>[47]</td>
</tr>
<tr>
<td>0.13μm</td>
<td>-</td>
<td>3mW</td>
<td>-13.1dBm</td>
<td>10Gb/s</td>
<td>Yes</td>
<td>50dBΩ</td>
<td>[48]</td>
</tr>
<tr>
<td>90nm</td>
<td>200fF</td>
<td>15mW</td>
<td>-</td>
<td>10GHz</td>
<td>No</td>
<td>60dBΩ</td>
<td>[49]</td>
</tr>
<tr>
<td>90nm</td>
<td>400fF</td>
<td>6.5mW</td>
<td>-</td>
<td>19GHz</td>
<td>Yes</td>
<td>45dBΩ</td>
<td>[50]</td>
</tr>
</tbody>
</table>

reported in [50] proposes using two matched photodiodes to generate a differential optical input. Here, two common-gate input stages are followed by a cascoded differential amplifier with inductive peaking. The circuit achieves exceptional bandwidth in the presence of a large input capacitance, but the gain is much lower than other published topologies.

A wide variety of TIA topologies are proposed, likely because each specific TIA application will place different relative importance on the gain, bandwidth, area, power consumption, and sensitivity of the TIA circuit. For the TIA described in this thesis, the design objective was to achieve at least 54dBΩ (2x250Ω) gain in a circuit with a single-ended input having 250fF parasitic diode capacitance, a differential output, and no inductors while co-optimizing the power and bandwidth performance. No obvious solution exists among the reviewed literature, and later sections of this chapter will demonstrate that the proposed cross-coupled NMOS cascode TIA provides the necessary performance.

### 3.2.2 Non-Traditional Receiver Architectures

Several recent publications have proposed receiver architectures that entirely bypass the use of the traditional TIA circuits at the optoelectronic interface. One proposed method [51], [52] involves using short optical pulses, generated by a mode-locked laser, to deliver precise clocking information across a chip. This is achieved by stacking two matched photodiodes with a CMOS gate at the shared node. Illuminating the top
diode with a short pulse generates a rising edge, while illuminating the bottom diode generates a falling edge. Therefore, the two diodes must be driven with separate pulse trains at the desired clock frequency with a half-period phase shift between them. The group also proposes using the same architecture for transmitting and receiving data [53], [54]. Although the receiver is unchanged, additional complexity is required at the transmitter since short-pulses cannot be generated with small integrated sources. Therefore, an external mode-locked laser source is used to illuminate reflective modulators at the transmitter. While this technique may have long-term potential, particularly for clock distribution, the complexity of the free-space optics required for data transmission applications will likely make this solution less practical than other alternatives in the near term.

Another proposed receiver design eliminates the TIA and operates by integrating the received photocurrent directly onto a sampling capacitor [55], [56], [57], [58]. A low-pass filter is used to subtract a DC current from the input node such that the net currents for received ‘1’ and ‘0’ symbols have equal magnitude and opposite sign. Pass-gates are used to sample the capacitor voltage onto the two inputs of a differential comparator at one bit period spacing. If the voltage increases between samples then a ‘1’ was transmitted in the previous bit and if the voltage decreases then a ‘0’ was transmitted. Timing information is recovered by observing that, if two consecutive bits are not equal, then samples before the first bit and after the second bit should have an equal voltage when the clock phase is correct. Deviations from this ideal timing will result in unequal voltages, and the sign of the difference may be combined with the data sample values to determine if the clock is early or late and adjust the phase accordingly. Analysis of bandwidth and sensitivity for this receiver differs from the analysis for a traditional TIA. Here, the sampling comparators have a defined voltage sensitivity and the input current must be sufficient to displace the capacitor voltage beyond this sensitivity within a single bit period. There is no architectural constraint precluding a full-rate implementation of this receiver, but the published implementation cited power constraints and comparator resolution time of the small voltage differences as justification for using a 5× interleaved clocking
3.3 Core Voltage Amplifier Design

According to the analysis in Section 3.1, the core voltage amplifier in this design requires a differential gain of 7.8. The presented core voltage amplifier topology, shown in Figure 3-2, meets this requirement by using feedback from cross-coupled NMOS cascode devices to boost the gain at the output node.

A small-signal analysis explains the mechanism by which the TIA design provides increased gain as compared with a standard differential-pair amplifier. Applying basic feedback principles to construct the small-signal analysis both increases the clarity
and simplifies the algebra. The half-circuit model, feedback system representation, and small-signal model for the half-circuit model of the core voltage amplifier are shown in Figure 3-3.

The transfer functions $F$ and $G$ represent, respectively, the currents that would be injected into node $V_{x+}$ due to modulation of $V_i$ and $V_y$ if $V_x$ were at small-signal ground. (Because the circuit is symmetric, each pair of nodes $V_+/V_-$ are assumed to have respective voltages of $+V$ and $-V$.) $H_1$ is the impedance from $V_{x+}$ to ground, assuming that each element connected to $V_{x+}$ has the opposite node connected to small-signal ground. The voltage at $V_{x+}$, $V_x$, is then easily calculated as a function of $V_x=(F \cdot V_i+G \cdot V_y)(H_1)$. This sequential grounding is a convenient analysis shortcut and its validity may be understood through the following logic. By superposition, the current through any branch is equal to the sum of the currents induced by the voltage at each end of the branch when the opposing end is grounded. So, for example, instead of explicitly solving for the current flowing from $V_{i+}$ to $V_{x+}$ as a function of $V_i$ and $V_x$ and then ignoring any branches connecting the two nodes in the determination of the impedance at $V_{x+}$, we can instead ignore $V_x$ in the determination of the injected current and account for it separately by including an additional term in the impedance at $V_{x+}$. Finally, $H_2$ is the transfer function from $V_{x+}$ to $V_{y+}$, which is found by assuming $V_{y-}=-V_{y+}$.

### 3.3.1 DC Small-Signal Analysis

If, at first, we consider only the DC components and ignore the capacitors then the solution provides insight into the way that the feedback increases the DC gain. With this simplifying assumption, the block transfer functions are given in (3.1)-(3.4). Since $M_3$ and $M_4$ are matched devices, instances of $M_4$ parameters are replaced with the equivalent parameters for $M_3$. 

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Applying Black’s formula to the feedback loop, the closed loop transfer may be obtained as given in (3.5), and evaluating the result with simulation-obtained values for the conductances yields a calculated gain of 9.1. By comparison, a simple differential pair amplifier has a gain described in (3.6), which evaluates to 4.2 at a similar bias point. A cascode amplifier with the cascode voltages at a steady-state bias at the common-mode value of $V_y$ has a gain given by (3.7) which evaluates to 4.8.
\[
\frac{V_{y^+}}{V_{i^+}} = \frac{g_{m1}(g_{ds3} + g_{m3})}{G_L(g_{m3} + g_{ds1} + g_{ds3}) - g_{ds1}(g_{m3} - g_{ds3})} \quad (3.5)
\]

\[
\frac{V_{y^+}}{V_{i^+}} = \frac{g_{m1}}{G_L + g_{ds1}} \quad (3.6)
\]

\[
\frac{V_{y^+}}{V_{i^+}} = \frac{g_{m1}(g_{ds3} + g_{m3})}{G_L(g_{m3} + g_{ds1} + g_{ds3}) + g_{ds1}g_{ds3}} \quad (3.7)
\]

Equation (3.5) indicates that, for certain values of the small-signal parameters, the denominator of the transfer function goes to zero. This would result in a gain singularity and sign change, which would cause instability, so understanding of the mechanism through which this could occur is critical. An alternative approach to the circuit analysis provides additional insight for this particular case. The transfer function can be formulated as (3.8), where \( g^* \) (3.9) is the conductance looking into the source of M3.

\[
\frac{V_{y^-}}{V_{i^+}} = -g_{m1} \cdot \frac{g^*}{g^* + g_{ds1}} \cdot R_L \quad (3.8)
\]

\[
g^* = \frac{-G_L(g_{ds3} + g_{m3})}{g_{m3} - G_L - g_{ds3}} \quad (3.9)
\]

Nominal device sizes are chosen such that \( g^* \) is negative and \( g^* + g_{ds1} < 0 \). This means that the impedance at \( V_{x^+} \), the gain from \( V_{x^+} \) to \( V_{y^-} \), and the gain from \( V_{i^+} \) to \( V_{y^-} \) are all negative. If, however, parameter variation causes \( g^* + g_{ds1} \) to approach zero, then the impedance at \( V_{x^+} \) becomes singular. Intuitively, this occurs when the negative conductance component due to the cross-coupled cascode feedback is exactly equal to the positive conductance components. Therefore, as with any feedback circuit, simulation over process corners is required to verify performance.
3.3.2 AC Small-Signal Analysis

Inclusion of capacitors in the analysis provides a more complete model of the feedback system and allows a full analysis of the mechanism through which the circuit provides gain peaking and improved bandwidth. Adding the capacitors and recalculating the transfer functions yields the results of (3.10)-(3.13). (The drain-bulk and source-bulk parasitics are included in the small-signal equations but omitted from the small-signal model of Figure 3-3 for clarity. However, it is clear by inspection that $C_{db1}$ and $C_{sb3}$ are in parallel with $C_X$ and that $C_{db3}$ is in parallel with $C_L$.)

\[
F = sC_{gd1} - g_m1 \quad (3.10)
\]

\[
H1 = \frac{1}{s(C_{gd1} + C_{db1} + C_{gs3} + C_{sb3} + C_X) + (g_{ds1} + g_{ds3} + g_m3)} \quad (3.11)
\]

\[
H2 = \frac{sC_{gs3} - (g_{ds3} + g_m3)}{s(C_L + C_{gs3} + 4C_{gd3} + C_{db3}) - (g_m3 - g_{ds3} - G_L)} \quad (3.12)
\]

\[
G = sC_{gs2} + (g_m3 - g_{ds3}) \quad (3.13)
\]

By applying Black’s formula again with the above transfer functions, we find that the input-output voltage transfer function has two poles and two zeros. Figure 3-4 shows the matching of the analytical small-signal model of Figure 3-3 to a transistor-level simulation with load capacitance ($C_L$) swept from 0fF to 30fF and no additional capacitance ($C_X$) to increase peaking. The results show that the load capacitance limits the amplifier bandwidth.

In order to improve the amplifier performance for a given load capacitance, additional capacitance may be introduced at $C_X$ to split the poles, thereby optimizing bandwidth. In this two-pole/two-zero system, the zeros occur well beyond the unity-gain frequency and have a minor effect on the amplifier dynamics in the frequency range of interest. The remainder of the analysis will therefore focus on the placement of the two poles.
Applying simulated conductance and capacitance values in the closed-loop equation shows that the amplifier has two poles on the real axis of the complex plane when little or no additional capacitance is added at $C_X$. In this case, the pole with the lower frequency limits the overall amplifier performance. Increasing $C_X$ moves the poles toward each other until they split from the real axis and form a complex pair. Gain peaking may be introduced by further increasing $C_X$ to move these poles further from the real axis and reduce the damping. The pole locations in the complex plane are shown in Figure 3-5 for $C_L=25\text{fF}$ and $C_X$ swept from 0fF to 50fF. The system will be well-damped when the poles lie to the left of the dashed 45 degree line. To the right of this point, the resonance of the complex pole pair will become prominent.

Re-positioning the poles has a direct effect on the bandwidth of the amplifier and its damping near the pole frequency. Figure 3-6 shows the amplifier gain for a load capacitance of 25fF and a peaking capacitance swept from 0fF to 50fF. Choosing a peaking capacitor in the center of this range will provide the best trade-off between bandwidth and damping.

However, if the amplifier itself is to be used in feedback, as is the case with the TIA configuration, then careful attention must also be paid to maintain sufficient phase

Figure 3-4: Voltage amplifier bandwidth for various $C_L$
Figure 3-5: Pole locations as a function of $C_X$

Figure 3-6: Bandwidth and damping impact of sweeping $C_X$
margin or instability may result. In the case of the TIA design, a relatively small 15fF load capacitance, consisting primarily of the gate capacitance of the source-follower stages, is present at $V_y$. Figure 3-4 shows that the bandwidth limit is not dominated by the load capacitance in this case and additional peaking with $C_X$ is not required. However, as demonstrated by Figure 3-4, additional capacitance at $C_X$ can be advantageous for stand-alone voltage amplifier applications with larger load capacitance.

3.4 TIA Biasing Configurations

The current generated at the photodiode by the received optical signal is single-ended and has a non-zero switching threshold current since the VCSEL modulates the transmitted power between two positive values. Therefore, the receiver must first implement offset cancellation and then bias the negative input of the voltage amplifier at the midpoint of the positive input voltage in order to complete the single-ended to differential conversion. This section first presents and analyzes several methods for biasing the negative amplifier input and then discusses a method of DC offset cancellation that could be applied in conjunction with any of the biasing methods.

3.4.1 Symmetric Feedback

In order for the differential output signals to have equal common-mode voltages, the negative input of the core voltage amplifier must be set to the correct reference level. Figure 3-7 shows the circuit configuration that forms the basis for many published single-ended to differential TIAs. The RC feedback from the positive and negative outputs of the TIA is symmetric. In some designs, the capacitor at the reference node is matched to the parasitic capacitance of the photodiode in order to minimize the single-ended supply and/or coupling noise of the photodiode. While this technique may be advantageous for long-haul receiver designs with relatively low levels of integration, package-to-package links are constrained by stringent pin limits and an extra pin cannot be allocated an additional
Figure 3-7: Traditional symmetric feedback TIA biasing

pin to bring the reference node off chip for matched biasing. Therefore, since the reference node capacitor cannot be connected to the photodiode supply, the common-mode noise advantages of matched capacitance are lost. In this case, there are stability advantages to increasing the value of this capacitance to set the reference node to AC ground.

This analysis considers the circuit of Figure 3-7 where the feedback capacitance $C_F$ is neglected and the core amplifier modeled as a single-pole low-pass system with lossless differential to single-ended conversion, no output resistance, and infinite input impedance. The general case of the analysis for arbitrary $C_{DC}$ is too cumbersome to provide insight, but the comparison of two special cases demonstrates the advantage of increasing the capacitance at the bias node. In the first case, we assume that the two input capacitances are matched such that $C_{PD}$. In the second case, we assume that the bias node capacitance is large enough that the node may be considered AC ground over the frequency range relevant to overall TIA dynamics.

First, the stability for matched capacitances is analyzed. We begin the analysis by writing equations for the input current in terms of input and output voltages (3.14), the reference voltage in terms of the positive output (3.15), and the differential transfer function of the amplifier (3.16).
The closed-loop $dV_o/dI$ transfer function is found by solving (3.14) to find $dV_i$, subtracting (3.15) from this result to obtain $dV_i - dV_r$, substituting this result into (3.16) to eliminate $dV_i - dV_r$, and solving to obtain $dV_o/dI$ as shown in (3.17).

$$\frac{dV_o}{dI} = \frac{\frac{A_0\omega_0}{2C_{PD}}}{s^2 + s\frac{1+\omega_0 C_{PD} R_F}{C_{PD} R_F} + \frac{(1+A_0)\omega_0}{C_{PD} R_F}}$$

(3.17)

The dynamics of a second-order system may be analyzed by placing the denominator in the form $s^2 + 2\zeta\omega_n + \omega_n^2$. In the case of (3.17), the resonant frequency may then be given by (3.18). Then, $\zeta$ may be found by substituting this result for $\omega_n$ into the $s$ term of the denominator and solving $2\zeta\omega_n$ to obtain $\zeta$ as in (3.19).

$$\omega_n = \sqrt{\frac{(1 + A_0)\omega_0}{C_{PD} R_F}}$$

(3.18)

$$\zeta = \frac{1 + \omega_0 R_F C_{PD}}{2\sqrt{R_F C_{PD}(1 + A_0)\omega_0}}$$

(3.19)

Observing that acceptable damping is obtained when $\zeta = \sqrt{2}/2$, setting the result of (3.19) equal to this value, and using the quadratic formula to solve for the required core amplifier bandwidth, $\omega_0$, yields the result in (3.20) and its approximation valid for relatively large $A_0$. This result defines the minimum acceptable bandwidth for the core amplifier with the small input capacitance configuration.
Figure 3-8: AC response of symmetric feedback TIA for small/large bias capacitance

\[ \omega_0 = \frac{A_0 \pm \sqrt{A_0^2 - 1}}{R_F C_{PD}} \approx \frac{2A_0}{R_F C_{PD}} \] (3.20)

Alternatively, the analysis can be completed assuming that the voltage reference node of the core amplifier input is AC ground at frequencies affecting amplifier dynamics. An identical procedure is followed for deriving the solution, except that at the beginning of the analysis we let \( dV_r = 0 \) instead of the result in (3.15).

\[ \omega_0 = \frac{A_0 \pm \sqrt{A_0^2 - 4}}{2R_F C_{PD}} \approx \frac{A_0}{R_F C_{PD}} \] (3.21)

The final result, given in (3.21), shows that the necessary bandwidth of the core amplifier is reduced by a factor of two from the PD-matched capacitance case. When a large capacitor is used, the amplifier bandwidth is equivalent to that required in a single-ended TIA with equivalent input resistance. The results in Figure 3-8 show the response of the actual symmetric-feedback TIA to an AC input current with both photodiode-matched bias capacitance and large (10pF) bias capacitance. The simula-
tion supports the analysis that the high-speed dynamics are improved by introducing a large capacitor at the bias node.

### 3.4.2 Common-Mode Feedback

While the capacitance at the bias node can easily be made large enough to separate the poles and improve the amplifier dynamics, the specifications for this TIA also require it to handle arbitrarily long runs of data. The low-frequency gain reduction problem associated with symmetric feedback TIAs may be understood from the following simplified system analysis. Amplifier frequency response and the effect of feedback capacitance \( C_F \) are neglected in this analysis since we are concerned about lower frequency performance.

The limitations of the system shown in Figure 3-7 may be understood most intuitively by analyzing the zero-current DC condition, the response to a high-frequency input signal, and the response to non-zero DC input current. First, since the inputs to the amplifier are purely capacitive, it should be clear that all four input and output voltages will settle to a shared common-mode, \( V_C \), when the input current is zero. The response to DC and high-frequency input signals may then be analyzed with respect to this common mode.

Assume the TIA receives a net input current of magnitude \( dI \) and the node voltages are named as in Figure 3-7. After simplification and cancellation of the \( V_C \) terms, equations (3.22) and (3.23) describe the voltage-current relationships within the TIA, feedback, and biasing network.

\[
\begin{align*}
dV_i + dV_o &= dI \cdot R_F \quad (3.22) \\
A_o[dV_i - dV_r] &= 2 \cdot dV_o \quad (3.23)
\end{align*}
\]

We have two equations with four variables and wish to write an equation for \( dV_o \) in terms of only \( dI \). Therefore, \( dV_i \) can be eliminated by using the extra equation
and \( dV_r \) can be eliminated by making assumptions about the frequency of the input signal.

Suppose the input current begins at zero and then rises suddenly to \( dI \). The low-pass filter on the voltage reference node holds the voltage at \( VC \), so for high-frequency input \( dV_r = 0 \). Eliminating \( dVi \) and solving gives the result in (3.24). The substitution of \( 2 + A \) in the denominator in place of the traditionally expected \( 1 + A \) reduction in input resistance is a result of the differential to single-ended conversion.

\[
\frac{dV_o}{dI} = \frac{A_0 \cdot R_F}{2 + A_0} \tag{3.24}
\]

However, immediately after the transition, the reference voltage will begin increasing with the time constant of the low-pass filter. Once the system reaches a new DC steady-state, \( dV_r = dV_o \). Imposing this new condition on (3.22) and (3.23) leads to the new solution shown in (3.25). By inspection, it is clear that the DC gain is half the high frequency gain in the limit as \( A_0 \to \infty \). For the more realistic case of \( A_0 = 8 \), a 45 percent reduction in gain results.

\[
\frac{dV_o}{dI} = \frac{A_0 \cdot R_F}{2(1 + A_0)} \tag{3.25}
\]

Although the LIA does have excess gain sufficient for resolving the reduced signal to logic levels given expected current input levels, allowing this gain reduction effectively introduces a 3dB sensitivity penalty at low frequency and could limit the potential for reducing input optical power. Therefore, it is either necessary to guarantee that the filter has a sufficiently low cutoff frequency to limit the droop of any potential input signal or to introduce a biasing scheme that does not rely on filtering.

The common-mode feedback biasing (CMFB) configuration shown in Figure 3-9 instead uses two matched resistors to extract the common mode of the output signal. The system response is again given by the equations of (3.22) and (3.23), since the voltage-current relationships they describe are consistent between the two circuits.
In fact, even the high-frequency response is identical to the previous analysis. The difference arises when determining the steady-state value of $dV_r$, which now settles to 0 instead of $dV_o$, since the resistive divider finds the common-mode of the two output voltages which remains nominally at $VC$ for any input current. Therefore, the gain is not reduced at low frequencies and the broadband gain of the new circuit is equal to the high frequency gain of the original circuit given in (3.24).

In practice, a number of factors suggest that large-value resistors should be used in the CMFB circuit, despite the theoretical resistance-independence of the circuit described above. First, the core voltage amplifier has finite output drive current and using small resistors would reduce gain by partially shorting the two outputs. Second, the combination of single-ended input and finite output resistance of the current source in the TIA differential pair causes small differences in the magnitude of the positive and negative amplifier output signals. This means that the common-mode actually shifts slightly depending on the sign of the input current. While the gain reduction is minor even when these non-idealities are comprehended, placing a low-pass filter in the feedback can eliminate this effect for most frequencies of interest. This low-pass operation can also provide high-frequency compensation for potential mismatch of the CMFB resistors.

Figure 3-10 shows a comparative simulation of the symmetric and common-mode biasing schemes. To allow for fair comparison, both circuits used $8k\Omega$ feedback resistors and $2pF$ bias capacitors. For the symmetric case, the gain degrades to the
expected DC value after the filter cutoff. For the CMFB case, a minor gain reduction is observed after the filter cutoff due to inefficiencies and mismatches in the differential to single-ended conversion. However, the DC gain is improved by approximately 5dB compared to the low-pass filtering configuration.

3.5 Bandwidth and Power Consumption

Figure 3-11 shows extracted simulations of both configurations of the TIA using realistic capacitance and resistance values and a 250fF input capacitance. For the symmetric case, $C_{DC}=10pF$ and the feedback resistors are matched and symmetric with a value of 314Ω. Reducing $C_{DC}$ to more reasonable on-chip values would result in even narrower bandwidth performance. For the common-mode feedback case, $C_{DC}=2pF$ and the common-mode feedback resistors are 8kΩ. The 3dB bandwidths, referenced from the respective amplifier gains at 1GHz, are also plotted. For the symmetric feedback TIA, the bandwidth is 76MHz to 9.1GHz. The common-mode feedback configuration increases the bandwidth range to DC to 8.9GHz. The slight discrepancies in gain and upper bandwidth limit are due to differences in output
Because the TIA was integrated with a LIA on the test chip, direct measurement of bandwidth and power consumption were not possible. Bandwidth performance can be inferred from the achievable data rate and power consumption is determined from simulations. The TIA operates from a 1.8V supply and draws 4.8mA through the core amplifier and 1.5mA for each source follower, which results in a total power consumption of 14mW. This is 1.1mW/Gb/s at 12.5Gb/s and 0.78mW/Gb/s at 18Gb/s.

### 3.5.1 Offset Cancellation

To implement offset cancellation, a DC current is subtracted from the input node so that the one and zero levels of the TIA input current are symmetric around zero. The traditional method of DC offset cancellation employs an operational amplifier and a low pass filter to set the offset cancellation current such that the output common-mode voltages are equal. However, this technique is only appropriate if the data transmitted over the channel is coded to be DC-balanced and limited to a defined bandpass frequency content. For package-to-package links, such encoding schemes are avoided due to the latency and bandwidth penalties. The TIA design is then required
to be operational for arbitrary run lengths and offset cancellation methods based on low-pass filtering are unacceptable as the offset cancellation would eventually cancel the entire input signal during long runs.

To solve this problem, this design uses a DAC to set the value of the DC current at the input. This offset cancellation circuitry simultaneously provides the ability to cancel any input-referred offsets generated by device variations in the amplifier stages by shifting the DC level of the net input current. In differential amplifier design, an inherent trade-off exists between choosing large devices for low offset or small devices for high bandwidth. As devices shrink and bandwidth requirements increase, the required speed can only be achieved with minimum length devices and the resulting offsets must be tolerated. Once the expected offset is characterized, however, digital offset cancellation techniques may be implemented to minimize the impact.

The input-referred current offset is characterized for a receiver consisting of the TIA with the CMFB biasing proposed in Section 3.4.2 and a LIA which limits the TIA output to a full-swing CML signal. Figure 3-12 shows the configuration of the offset simulation. The photodiode input is set at a DC value of 75µA, the current through the mirror is swept from 0µA to 150µA, and the value of the mirror current is recorded when the LIA outputs are equal.

A Quasi-Montecarlo simulation was used to characterize the statistical variation of the input-referred offset current. A total of 800 full transistor-level simulations were chosen by the simulator to characterize the variation space and the results were used to complete a 10,000 point Montecarlo simulation. As expected, the offset is large due to the use of minimum-sized devices. Therefore, a DAC was implemented to adjust the offset cancellation current. Assuming that the DAC compensates for the input-referred offset to within half an LSB, this method provides a $24 \times$ reduction in the input-referred offset current from the $3\sigma$ statistical value.
Figure 3-12: Test circuit for receiver offset simulation

3.6 Measured Results

Both symmetric feedback and common-mode feedback versions of the TIA were designed and layout was completed for both versions. The common-mode feedback version of the TIA is still in fabrication, and the symmetric-feedback version has been fabricated and measured. These measurements verify both the functionality of the core amplifier, the high-speed performance of the TIA for a range of input capacitances, and the sensitivity of the TIA.

3.6.1 Measurement Setup

The TIA was measured using an RF probe station and the complete measurement setup is illustrated in Figure 3-13. A bias-T was used to provide a DC current to the 50Ω termination, $R_T$, and set the TIA DC input current to zero. The calibration of the DC input was achieved by disabling the AC input and tuning the DC input until the two LIA outputs achieved an equal DC voltage.

A 314Ω resistor, $R_M$, was included between the input pad and the TIA input in order to provide a current-mode input for realistic testing of the TIA. However, this addition slightly complicates the problem of determining the relationship between the AC input signal level and the TIA input current. Therefore, the complete test circuit, including $R_T$ and $R_M$, was simulated to determine that the TIA input current would
be 100μA for each 40mV of voltage swing at the input pad. Measurements of the pattern generator output determined that 30dB, 36dB, and 42dB attenuation result in 80mV, 40mV, and 20mV signal swing when measured on the 50Ω oscilloscope, and these attenuated signals were used to drive the test circuit in order to generate 200μA, 100μA, and 50μA TIA input signals. A binary capacitor array was included directly at the TIA input to allow TIA testing for a range of input capacitance. Different capacitor combinations were cut using FIB to obtain TIA test circuits with five input capacitance values: 440fF, 260fF, 145fF, 205fF, and 90fF. Probing of the bias node with a DC probe introduces a large external capacitance at the negative TIA input. This increases the bandwidth where the TIA maintains constant gain by moving the feedback zero to lower frequency, but cannot be avoided due to the DC probe configuration. The performance of the proposed common-mode feedback configuration is expected to be similar to the measured system. The outputs were probed and measured with an Agilent sampling oscilloscope. Because the LIA output is connected directly to the output pads without a 50Ω driver, the output swing measured at the oscilloscope is only 40mV, which is consistent with complete current switching at the final LIA stage.
3.6.2 Data Rate Testing

The TIA was measured across a range of data rates and input capacitance and representative results are included in Figure 3-14. These results show that the TIA operates at 12.5Gb/s with 260fF of input capacitance, which is a realistic value for commercial photodiodes. Furthermore, the TIA operates at 18Gb/s if the input capacitance is reduced to 90fF. This indicates that, as photodiode technology improves and parasitic capacitance is reduced, new photodiodes could be combined with the TIA to attain higher data rates.

3.6.3 Sensitivity Testing and Analysis

The TIA was designed to operate with a relatively large input current of 200μA, so bandwidth, gain, power consumption were prioritized over noise performance during the design process. Simulations indicated that the total input-referred noise integrated to 10GHz is 2μA, but measured eye diagrams suggest that more noise may be present in the fabricated TIA. Because a LIA follows the TIA, observation of the SNR at the output is not meaningful, as any noise at the input will be limited and appear only as timing jitter at the output. However, the output jitter is observed to vary as a function of input signal current and input capacitance. Measurements of
this variation may be used to estimate the transimpedance amplifier noise.

To gain an intuitive understanding of the relationship between amplitude and timing noise, consider a perfect single-stage limiting amplifier with an output that switches rail-to-rail when the input crosses the switching threshold. If the input noise is set at a fixed level and the signal transition time is increased, the jitter at the output will increase as the combined input signal spends more time in the uncertain area around threshold due to the reduced slew rate. This relationship has been quantified for ring oscillators in [59]. The result was extended to LIA and AGC circuits in [60], which observes that the standard deviation of the jitter may be directly related to the standard deviation of the input amplitude by (3.26). Here, $\sigma_{\Delta T}$ is the jitter standard deviation, $\sigma_n$ is the TIA output voltage noise standard deviation, and $S$ is the slew rate of the TIA output voltage in the vicinity of the threshold. This assumes that both the current noise and jitter have white Gaussian distributions, that both TIA signal and noise are referred to the TIA output, and that the TIA is followed by an ideal noiseless LIA.

\[
\sigma_{\Delta T} = \frac{\sigma_n}{S} \tag{3.26}
\]

If we make the simplifying assumption that the TIA bandwidth is described by a first order low-pass filter with a time constant $\tau$, then the output voltage during a downward transition from the peak current to zero is described by (3.27), where $V_o(t)$ is the TIA output voltage, $I_{pk}$ is the peak-to-peak input current, and $A$ is the peak transimpedance gain. The slew rate at threshold is determined by taking the derivative of the current and evaluating the magnitude at the transition midpoint $t = 0.69\tau$, which yields the slew rate result of (3.28).
\[ V_o(t) = A \cdot I_{pk} \cdot e^{-\frac{t}{\tau}} \quad (3.27) \]

\[ S = \left| \frac{d}{dt} [V_o(t)] \right|_{t=0.69\tau} = \frac{A \cdot I_{pk}}{2\tau} \quad (3.28) \]

This result makes intuitive sense, since increasing either the bandwidth or the signal amplitude results in a faster transition through the threshold region. In order to begin evaluating these results, we must make certain assumptions about the noise and bandwidth performance of the receiver as a function of capacitance. For simplicity, we assume that the TIA has a fixed input resistance \( R = 65\Omega \) and a total input capacitance equal to the sum of the added test capacitance, \( C \), and the fixed gate and parasitic capacitance, \( C_p \), which we assume to be 80fF. We also know that, for a first order low-pass system, the noise equivalent bandwidth (NEB) is \( 1.5 \times \) the filter bandwidth and we assume the input-referred noise has a white spectral density given by \( i_n \). Here, \( i_n \) is the unknown variable and will be determined by fitting the model to the measured jitter data. The TIA time constant and output voltage noise standard deviation may then be defined, respectively, in (3.29) and (3.30). Finally, (3.26), (3.28), (3.29), and (3.30) are combined to yield the expression for the jitter as a function of input noise current density given in (3.31).

\[ \tau = R \cdot (C + C_p) \quad (3.29) \]

\[ \sigma_n = \sqrt{\left( \frac{1}{2\pi\tau} \right) \cdot \left( \frac{3}{2} \right) \cdot (A \cdot i_n)^2} \quad (3.30) \]

\[ \sigma_{\Delta T} = \sqrt{\frac{3 \cdot i_n^2 \cdot R \cdot (C + C_p)}{\pi \cdot I_{pk}^2}} \quad (3.31) \]

We have now developed a method to estimate the input noise from a series of output jitter measurements. Figure 3.15 shows edge jitter measurements when TIA
circuits with 440fF and 205fF input capacitance are driven with 1GHz clock signals with amplitudes of 200µA, 100µA, and 50µA. A fourth measurement was performed with 700µA input current, but is omitted from the figure. The RMS jitter from each of these measurements was recorded and fit to the jitter model by sweeping the input-referred noise current spectral density, $i_n$. Because the clock source has an RMS jitter of $\sigma_{\Delta T_{\text{CK}}}=1.1\text{ps}$, this variance was added to the TIA jitter model variance to obtain the final modeled result: $\sigma_{\Delta T_{\text{TOT}}} = \sqrt{\sigma_{\Delta T_{\text{CK}}}^2 + \sigma_{\Delta T}^2}$.

Circuit simulations predicted at average noise of $i_n=20\text{pA}/\sqrt{\text{Hz}}$ up to 10GHz with increasing noise at frequencies beyond 10GHz, so the value was swept in this range to determine the best fit. Figure 3-16 shows the matching of the measured and predicted output jitter assuming a noise current of $i_n=38\text{pA}/\sqrt{\text{Hz}}$. When integrated over the assumed noise bandwidth, this results in a total equivalent input noise current of $I_{\text{neq}}=3.2\mu\text{A}$ for the 440fF case and $I_{\text{neq}}=4.3\mu\text{A}$ for the 205fF.

While this estimate of the noise is somewhat higher than expected, there are several factors in addition to the TIA noise that may contribute. Additional termination resistors in the test setup, noise from the DC bias source, and small reflections on the RF cables may contribute to the amplitude of the input noise. Furthermore, the LIA may contribute additional noise which would be particularly significant at lower current levels. Nevertheless, even the worst case estimate of $I_{\text{neq}}=4.3\mu\text{A}$ is still within the range that will allow low error rate operation with the expected input current of 200µA. The required current level for the TIA receiver is derived in (2.12), and if we require $Q_F=7$ for a BER of $10^{-12}$, then the signal level must be at least $I_{pk} = 2 \cdot Q_F \cdot I_{\text{neq}}$. For $I_{\text{neq}}=4.3\mu\text{A}$, the receiver should meet the error rate target for input currents down to 60µA, assuming that the resulting timing noise is not prohibitive at the desired bit rate of operation. Figure 3-17 demonstrates proper TIA functionality at 10Gb/s for input capacitance of 260fF and 440fF, measured with a $2^7-1$ pattern at 200µA and 100µA input current and with a $2^{31}-1$ pattern at 200µA input current.
Figure 3-15: Jitter as a function of capacitance and input current
3.7 Summary

A TIA employing a core amplifier with cross-coupled NMOS cascodes to improve gain and bandwidth was designed in 90nm CMOS. Symmetric and common-mode feedback methods to bias the negative amplifier input are proposed and analyzed. The common-mode feedback method provides a differential TIA with near-constant gain from DC to 9GHz when used in conjunction with a DAC to perform DC offset cancellation and input-referred offset cancellation. Simulations and measurement demonstrate that the TIA has the required gain and bandwidth to operate at 12.5Gb/s with 260fF input capacitance and 18Gb/s with 90fF input capacitance for an input current of 200µA. Worst case noise performance is estimated at $I_{n_{eq}}=4.3\mu A$ for an input capacitance of 205fF, based on measurements of the output jitter distribution.
Figure 3-17: 10Gb/s TIA eyes for varying signal strength, capacitance, and pattern
A VCSEL is a current-mode device which generates output power proportional to the input current once the current exceeds the device threshold. The VCSEL driver provides an interface between on-chip voltage signals and the required output modulation current. In many cases, the overall link performance is limited by intrinsic and parasitic effects associated with the VCSEL device itself. Several parasitic and intrinsic effects contribute to the bandwidth limitation of the typical VCSEL. Parasitic elements in the VCSEL include pad capacitance and resistance, resistance associated with the distributed Bragg reflector (DBR) mirrors, and capacitance and resistance associated with the diode junction. While the values of the pad and DBR parasitics are relatively constant over the operating range, the parasitics associated with the junction vary significantly with bias [21]. The intrinsic bandwidth and relaxation oscillation frequency of the VCSEL are controlled by the time constant of the interaction between electrons and photons within the active volume. Optical output power increases linearly with bias current above threshold and, as a result, bandwidth also increases with bias current since the carriers injected by a modulation are consumed faster in a strongly lasing cavity. The slow turn-off time constant and large turn-on oscillations that occur when the VCSEL bias current is modulated across the threshold may be explained by the same logic. The turn-off transition occurs with a slow time constant since the remaining carriers are consumed increasingly slowly as the VCSEL approaches a final state with minimal stimulated emission. The turn-on
transition exhibits a delay and oscillations. The delay is present because the device is not initially lasing and the injected current gradually accumulates in the active area until the threshold carrier density is attained. When the device finally crosses threshold and lasing begins, the optical field intensity increases rapidly and the carrier population is suddenly reduced by the stimulated emission. The rate of stimulated emission is, in turn, reduced by falling carrier density and decaying oscillations ensue.

Application of pre-emphasis circuit techniques has been proposed as a method to compensate for the bandwidth limitations of VCSEL devices and thereby maximize the achievable data rate. This chapter first summarizes the prior work in the area and then describes the design, fabrication, and measurement of the presented VCSEL driver, which is a full-rate architecture in 90nm CMOS operating at 18Gb/s without the use of inductors.

4.1 Prior Work

Circuit techniques may be used to implement pre-emphasis in the driver to partially equalize VCSEL dynamics and thereby extend the overall system bandwidth, and various levels of driver complexity have been proposed in the literature. A few theoretical papers have suggested complex equalization techniques to cancel the relaxation oscillation dynamics of the VCSEL exactly [61], [62], [63]. However, this work was based on an extremely simplified second-order description of the dynamics and neglected important spatial effects. Addition of these effects would make the calculation of the exact pre-emphasis waveform mathematically intractable. Furthermore, the required precise analog current-shaping is far too complex to implement at the required speeds and this type of approach therefore remains impractical from a circuit perspective in current technology.

However, simplified approaches featuring pre-emphasis of reduced complexity can be implemented in current CMOS processes and have the potential to significantly enhance the system bandwidth. Several authors have proposed and implemented current-peaking VCSEL drivers. While earlier results demonstrated lower data rates,
Table 4.1: Prior work: high-speed VCSEL drivers

<table>
<thead>
<tr>
<th>CMOS Process</th>
<th>VCSEL Material</th>
<th>$C_{VXL}$</th>
<th>Data Rate</th>
<th>Power mW/Gb/s</th>
<th>L?</th>
<th>Full Rate?</th>
<th>Cit.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.13μm</td>
<td>InGaAs</td>
<td>160fF</td>
<td>20Gb/s</td>
<td>3.5</td>
<td>Yes</td>
<td>Yes</td>
<td>[12]</td>
</tr>
<tr>
<td>90nm</td>
<td>GaAs</td>
<td>740fF</td>
<td>10Gb/s</td>
<td>2.1</td>
<td>Yes</td>
<td>Yes</td>
<td>[66]</td>
</tr>
<tr>
<td>90nm</td>
<td>GaAs</td>
<td>700fF</td>
<td>16Gb/s</td>
<td>3.0</td>
<td>No</td>
<td>No</td>
<td>[14]</td>
</tr>
</tbody>
</table>

Table 4.1 summarizes the most relevant reported characteristics of the three recently reported VCSEL driver results. In [12], an experimental 990nm InGaAs VCSEL with improved bandwidth is employed. The VCSEL used in this work has only 160fF of parasitic capacitance, which is approximately four times smaller than the typical capacitance of commercial GaAs VCSELs and the optical dynamics are improved such that the device is limited by optical bandwidth only beyond 14GHz [13]. This relaxes the design requirements for the pre-emphasis VCSEL driver, which does not have to compensate for electrical bandwidth limitations and instead employs pre-emphasis exclusively on the downward transition in order to reduce the fall time, which is asymmetrically limited by intrinsic optical dynamics. However, such InGaAs devices are still experimental and designing circuits to operate standard GaAs VCSELs at high data rates is a more practical near term solution. The most advanced commercially available GaAs VCSELs are designed for a nominal data rate of 10Gb/s, and a 10Gb/s CMOS driver is presented in [66]. A pre-driver with inductive peaking is used to introduce asymmetric pre-emphasis in order to reduce the timing jitter and the architecture achieves the lowest published power per data rate, but since the target data rate is only 10Gb/s, the application does not require substantial pre-emphasis. Finally, [14] reports an 16Gb/s digital pre-emphasis architecture employing a 4-tap equalizer to generate symmetric pre-emphasis to compensate for parasitic and intrinsic bandwidth limitations. The architecture uses 5× interleaved data paths which are multiplexed at the output stage, which allows low power consumption compared to
full-rate transmitters at similar data rates, but requires multiphase clocks and clock phase tuning to minimize systematic jitter. It is therefore incompatible with full-rate CDR architectures. This chapter presents a full-rate pre-emphasis VCSEL driver operating at 18Gb/s and incorporating digital control of pulse height and width.

4.2 VCSEL Driver Architecture

The presented VCSEL driver operates at 18Gb/s, which is the highest reported measured data rate for a link consisting of a full-rate CMOS driver and an 850nm GaAs VCSEL. The VCSEL driver in this work achieves an optical data rate of 18Gb/s with a standard commercial 850nm GaAs VCSEL by applying dual-edge pre-emphasis to compensate for the lower device bandwidth. The architecture is highly manufacturable, as full-rate pre-emphasis is generated directly from the data, the output stage is compatible with standard packages, and the design does not use inductors.

While prior designs have flip-chip bonded the VCSEL to the silicon, this method is incompatible with standard microprocessor and chip set packages in which the top surface of the microprocessor is inaccessible once it is flip-chip bonded onto the package substrate. This driver is output terminated to allow combination with a microprocessor-compatible package [22] in which the CMOS chip and VCSEL are both flip-chip bonded to the substrate and connected with short controlled-impedance copper traces. Termination is required because the traces are sufficiently long compared to the data rate that reflections could impact performance. The transmitter generates the pre-emphasis timing directly from the input data and is therefore easily incorporated into existing full-rate IO architectures with minimal system-level modifications. Since the time constant of the VCSEL response is expected to be at or near the bit period, the sub-bit-period timing resolution of 10ps allows the characterization of the effect of varying the pre-emphasis pulse width.

The architecture and basic operation of the pre-emphasis block are shown in Figure 4-1. The input is divided into two paths with a digitally programmable delay difference \( \Delta T_{DEL} \) to generate primary (D) and delayed (D*) versions of the data.
These signals drive two current-mode drivers to generate switched currents $I_D$ and $I_{D^*}$. $I_{D^*}$ is inverted and scaled with respect to $I_D$, and the total drive current ($I$) resulting from the summation of the two currents at the output node contains pre-emphasis pulses of duration $T_{DEL}$ during the period following each data transition where $D \neq D^*$. The current levels of $I_D$ and $I_{D^*}$ are set by modulation and pre-emphasis bias currents, $I_{B1}$ and $I_{B2}$, which are generated by two 5-bit DACs.

Figure 4-2 shows combined simulations of the electrical VCSEL model described in Chapter 2 and the terminated output driver demonstrating the benefit of pre-emphasis on the rise time of the junction current, $I_{JCT}$. Pre-emphasis reduces the electrical rise time to 30ps, which is a 50 percent improvement from the 60ps rise time simulated without pre-emphasis. These values are consistent with the RC bandwidth limit predicted for typical GaAs VCSEL characteristics of $C_{JCT}=700\text{fF}$ and $R_{DBR}+R_{JCT}=65\Omega$ in the model of Figure 2-8.

The output stage, shown in Figure 4-3, consists of two current switches with differential input and single-ended output. The cascode devices improve the symmetry of the current switching by isolating the drains of the input differential pairs from the mismatched output swing. The primary driver is sized $3\times$ larger than the pre-
emphasis driver to accommodate the expected nominal current ratio and the drivers have independent biasing to adjust the currents around their nominal values. The current mirror ratios are 1:36 in the primary driver and 1:12 in the pre-emphasis driver, such that \( I_M = 36 \cdot I_{B1} \) and \( I_P = 12 \cdot I_{B2} \). The modulation and pre-emphasis current are controlled by two 5-bit DACs, and after the 36x and 12x mirror ratios, \( I_D \) and \( I_{D\prime} \) have respective ranges/resolutions of 48mA/1.5mA and 16mA/0.5mA.

The driver includes digital control of the pre-emphasis pulse duration, modulation current and pre-emphasis current. This improves robustness to VCSEL variation and allows characterization of the effect of pre-emphasis pulse height and width on the optical transient response. The pre-emphasis pulse width is controlled by a 4-tap digital delay line, shown in Figure 4-4, consisting of a buffer chain to generate four data phases and a two-level MUX tree to select a tap. Extracted simulation results shown in Figure 4-5 predict a range of 35ps to 65ps with 10ps steps, which allows fine optimization of the pre-emphasis width around the expected optimal range of one bit period. The final delay stage has shorter delay since the final buffer is loaded only with a MUX.

Figure 4-6 shows the simulated improvement of the electrical eye diagram that
Figure 4-3: VCSEL driver output stage schematic

Figure 4-4: Digital delay line architecture

Figure 4-5: Delay line input data and four output phases
is achieved when the extracted VCSEL driver is simulated in conjunction with the electrical VCSEL model for the cases of no pre-emphasis and the nominal 3:1 design ratio of pre-emphasis. Although the eye is nearly 50 percent closed without pre-emphasis, application of appropriate pre-emphasis results in an open electrical eye.

### 4.3 Experimental Results

#### 4.3.1 Fabrication

Layout was completed and the driver was fabricated in 90nm CMOS [11]. The output stage, pre-emphasis block, and DACs occupy active areas of 0.009μm², 0.014μm², and 0.01μm². This driver design was included in a fabricated test chip containing a full transmitter designed to operate at 20Gb/s. This channel includes an on-chip pseudo-random bit pattern generator (PRG), designed by Jason Liao of Intel Corporation, which multiplexes two taps from a 10Gb/s PRG to provide a 20Gb/s pattern. In this design, the bias currents for the VCSEL driver are controlled by the two 5-bit DACs as described in the previous section, and the DAC and digitally-controlled delay line inputs are set using the scan chain. This chip was packaged as reported in [22] and
preliminary measurement results have been obtained.

Because optical packaging is also an area of ongoing research, measurements included in this chapter are based on a test circuit designed to allow independent RF measurement of the VCSEL driver in order to decouple driver performance from the package and other transmitter circuits. To facilitate this testing, a test circuit containing the core VCSEL driver with external biasing instead of DACs was fabricated to allow independent wafer-level characterization of the driver performance and the layout is shown in Figure 4-7. This circuit was fabricated on a pad row with two RF signal pads for RF input and output, of which one was used for differential input to the VCSEL driver and one was used for single-ended output. The pad also has 12 DC signals, of which four supply $V_{SS}$ and two supply $V_{CC}$. The remaining six are used for the two bias currents ($I_{B1}$, $I_{B2}$), the bias for CML gates ($V_{CS}$), the select bits ($S_0$, $S_1$), and the tunable supply voltage for the termination resistor ($V_H$).

4.3.2 Measurement Setup

The test circuit was measured on the wafer-level probe setup illustrated in Figure 4-8. The inputs are driven by a differential bit pattern generator (BPG) with a $2^7-1$ pattern. The AC-coupled BPG outputs are connected through matched RF bias-T circuits and 50Ω cables in order to set the input common mode at the same 0.9V that would be provided by the preceding CML gates. At the output, a 50Ω cable
was used to connect the VCSEL driver to an external 8μm aperture GaAs VCSEL. An outside-only DC block was used to break the DC ground path in the RF cable shielding and allow independent biasing of the VCSEL supply. The VCSEL output was free-space coupled to a multi-mode fiber using micropositioners and detected with a 12GHz optical receiver manufactured by NewFocus. Because determination of fiber coupling loss and exact value of the receiver responsivity could not be measured, power is reported at the receiver based on the nominal responsivity.

In order to calibrate the supply voltages and bias currents to provide the desired on and off current in the VCSEL, a series of DC measurements were completed before each measurement. First, supplies were adjusted to set $V_{CC}=1.2V$, $V_{CS}=0.5V$, and $V_B=3.0V$. Second, a voltage value of diode connected $I_{B2}$ reference was selected to set the relative amount of pre-emphasis; when $I_{B2}=0V$ there is no pre-emphasis and with $I_{B2}=I_{B1}$ the pre-emphasis current is one third of the modulation current. The differential inputs were then set to the DC ‘0’ state so that $I_M$ was switched to $V_{CC}$ and $I_P$ was switched to the output node. $V_H$ was then adjusted until the current drawn through the VCSEL from $V_B$ was equal to the desired ‘0’ current, generally around 2mA to 3mA. Next, the inputs were set to the ‘1’ state and $I_{B1}$ was adjusted until the current through the VCSEL was equal to the desired ‘1’ current, usually 8mA to 10mA. With this procedure complete, the BPG was connected to the RF inputs and high-frequency measurements were completed.

Figure 4-8: VCSEL driver test setup on RF probe station
### Table 4.2: Measured eye improvement data from Figure 4-9

<table>
<thead>
<tr>
<th>Fig</th>
<th>Description</th>
<th>Eye Height</th>
<th>Eye Width</th>
<th>Height Increase</th>
<th>Width Increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-9(a)</td>
<td>2-8 Y</td>
<td>49</td>
<td>32.3</td>
<td>104%</td>
<td>48%</td>
</tr>
<tr>
<td>4-9(b)</td>
<td>2-8 N</td>
<td>24</td>
<td>21.8</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4-9(c)</td>
<td>2-10 Y</td>
<td>71</td>
<td>34.9</td>
<td>122%</td>
<td>76%</td>
</tr>
<tr>
<td>4-9(d)</td>
<td>2-10 N</td>
<td>32</td>
<td>19.8</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

#### 4.3.3 Measurement Results

The measurement results obtained using the procedure described above are presented in this section. First, the significant effect of pre-emphasis on eye opening and rise/fall time is demonstrated at 18Gb/s and 10Gb/s. Second, the transmitter power consumption is analyzed and broken down by functional block, which provides a framework for understanding the power cost of pre-emphasis and allows preliminary analysis of the power allocation might change for implementation of pre-emphasis in future CMOS technologies.

**Eye Diagrams**

The VCSEL driver performance was measured for a range of data rates. For each measurement, the pre-emphasis width and height were manually adjusted to optimized the eye quality. Representative results at 18Gb/s demonstrating the benefit of pre-emphasis are presented in Figure 4-9 for modulation from 2mA to 8mA and 2mA to 10mA. In both cases, $V_{cc}$ is 1.2V, $V_B$ is 3.0V, and $D^*$ is selected from the second tap. $I_{B1}$, $I_{B2}$, and $V_H$ are adjusted as described in the previous section to set the bias, modulation, and pre-emphasis currents. Reported optical power corresponds to the power received at the detector after fiber coupling and is calculated using the 120mV/mW nominal detector efficiency of the 12GHz NewFocus detector. Electrical power is reported for the complete transmitter and includes drive-strength buffering from a low-strength input, full-rate pre-emphasis generation, termination, and VCSEL power.

For 2mA to 8mA modulation, which requires a total modulation current of 15mA
Figure 4-9: Effect of pre-emphasis at 18Gb/s
Figure 4-10: Effect of pre-emphasis at 10Gb/s and 18Gb/s
due to the resistive divider formed by the VCSEL and the termination, the optical modulation amplitude (OMA) is 1dBm and pre-emphasis improves the vertical eye opening by 104% and the horizontal eye opening by 48%. With pre-emphasis, the drive and pre-emphasis currents are 21mA and 6mA, $V_{DDH}$ is 1.5V, and the power is 119mW (6.6mW/Gb/s). Without pre-emphasis, the drive current is 15mA, $V_H$ is 1.2V, and the power is 103mW (5.7mW/Gb/s). For 2mA to 10mA modulation, which requires a total modulation current of 19mA, the OMA is 2.1dBm and pre-emphasis improves the vertical eye opening by 122% and the horizontal eye opening by 76%. With pre-emphasis, the drive and pre-emphasis currents are 27mA and 8mA, $V_H$ is 1.6V, and the power is 131mW (7.3mW/Gb/s). Without pre-emphasis, the drive current is 19mA, $V_H$ is 1.2V, and the power is 109mW (6.1mW/Gb/s). The performance improvement is summarized in Table 4.3.3, along with details of the measured eye height and eye width for the four cases.

An additional set of measurements comparing 10Gb/s and 18Gb/s performance with and without pre-emphasis is included in Figure 4-10. The VCSEL is nominally designed for 10Gb/s, so the eye is open at this rate even without pre-emphasis, but the pre-emphasis noticeably improves the rise and fall time in the pre-emphasized eye of Figure 4-10(a) over the un-emphasized eye of Figure 4-10(b). At 18Gb/s, this reduction in rise and fall time results in an improved vertical eye opening in Figure 4-10(c) over Figure 4-10(d). Furthermore, these figures illustrate that the pre-emphasis compensates for the electrical parasitic limitations sufficiently to allow observation of the relaxation oscillation overshoot due to the intrinsic optical dynamics. Without pre-emphasis, electrical bandwidth limiting apparently prevents the junction current transitions from occurring fast enough to cause relaxation oscillations.

**Power Consumption**

While high data rate is the most obvious performance metric for short distance optical links, power consumption is also of critical importance as future systems will have a limited power budget to operate many parallel optical links. In order to achieve full-rate operation and 50Ω package compatibility, this architecture consumes somewhat
Table 4.3: Measured power consumption during PRBS measurement

<table>
<thead>
<tr>
<th>Fig</th>
<th>Description</th>
<th>VCC (mA)</th>
<th>IVCC (mA)</th>
<th>VH (mA)</th>
<th>IVH (mA)</th>
<th>VB (mA)</th>
<th>IVB (mA)</th>
<th>Power (mW)</th>
<th>Power (mW/Gb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#</td>
<td>IMOD PE V</td>
<td></td>
<td>V</td>
<td>mV</td>
<td>V</td>
<td>mV</td>
<td>V</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>4-9(a)</td>
<td>2-8 Y</td>
<td>1.2</td>
<td>77.0</td>
<td>1.5</td>
<td>8.1</td>
<td>3.0</td>
<td>4.9</td>
<td>119</td>
<td>6.6</td>
</tr>
<tr>
<td>4-9(b)</td>
<td>2-8 N</td>
<td>1.2</td>
<td>71.2</td>
<td>1.2</td>
<td>2.2</td>
<td>3.0</td>
<td>4.9</td>
<td>103</td>
<td>5.7</td>
</tr>
<tr>
<td>4-9(c)</td>
<td>2-10 Y</td>
<td>1.2</td>
<td>80.8</td>
<td>1.6</td>
<td>11.0</td>
<td>3.0</td>
<td>5.5</td>
<td>131</td>
<td>7.3</td>
</tr>
<tr>
<td>4-9(d)</td>
<td>2-10 N</td>
<td>1.2</td>
<td>73.5</td>
<td>1.2</td>
<td>3.3</td>
<td>3.0</td>
<td>5.7</td>
<td>109</td>
<td>6.1</td>
</tr>
</tbody>
</table>

Table 4.4: Measured power consumption for DC on/off states

<table>
<thead>
<tr>
<th>Fig</th>
<th>Description</th>
<th>IVCC (mA)</th>
<th>IVH (mA)</th>
<th>IVB (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#</td>
<td>IMOD PE</td>
<td>ON OFF</td>
<td>ON OFF</td>
<td>ON OFF</td>
</tr>
<tr>
<td>4-9(a)</td>
<td>2-8 Y</td>
<td>69.8 84.9</td>
<td>12.8 3.9</td>
<td>8.5 2.1</td>
</tr>
<tr>
<td>4-9(b)</td>
<td>2-8 N</td>
<td>64.2 78.9</td>
<td>6.6 -2.1</td>
<td>8.3 2.1</td>
</tr>
<tr>
<td>4-9(c)</td>
<td>2-10 Y</td>
<td>71.5 90.3</td>
<td>16.7 5.8</td>
<td>10.2 2.1</td>
</tr>
<tr>
<td>4-9(d)</td>
<td>2-10 N</td>
<td>64.2 83.1</td>
<td>8.8 -2.1</td>
<td>10.3 2.1</td>
</tr>
</tbody>
</table>

more power than previously published works at similar data rates, but an analysis
of the power breakdown by functional block shows that a significant portion of the
power is consumed by low fan out drive strength buffering which is required because
the performance limits of the CMOS CML are close to the target data rate. Because
power supplies are shared across many functional blocks and the output stage draws
power from several supplies, block power cannot be measured directly during testing.
Therefore, power consumption is instead measured at each supply for active PRBS
transmission, continuous ‘1’ transmission, and continuous ‘0’ transmission and this
data is used to calculate the block power consumption under the assumption that ‘1’
and ‘0’ occur with equal frequency in the transmitted data.

Table 4.3.3 summarizes the power consumption from each supply during normal
PRBS operation. The sum of the power consumed from the three supplies is the
actual measured power consumption, and will be used as a reference to determine the
validity of the per-block power calculated from DC measurements.

Table 4.4 shows the DC power consumption from each of the three supplies for
the ‘1’ and ‘0’ DC states of each measurement of Figure 4-9 and Table 4.5 shows how
the block power may be calculated from this information. First, we observe that in
the ‘1’ state, $I_D$ is switched to the output node and $I_{D*}$ is switched to $V_{CC}$. In the ‘0’
state, the currents are reversed so that $I_{D*}$ is switched to the output node and $I_D$ is switched to $V_{CC}$. Since all output node current flows either through the VCSEL or the termination, this allows direct calculation of $I_D$ and $I_{D*}$ from information about $I_{VH}$ and $I_{VB}$. With the branch currents for each DC state known, the assumption that '1' and '0' are equally likely to occur allows calculation of average block power by summing average powers drawn from each supply by each block, as summarized by the equations of Table 4.5.

Finally, Table 4.6 summarizes the resulting power consumed by each block during normal operation. The reader will note that the values for total power consumption are in close agreement with the directly measured results of Table 4.3.3. Because the signal-strength buffering and pre-emphasis generation power cannot be individually measured, we must rely on calculations to determine the relative power consumption of these blocks. Counting the CML gates of each size that are used in the schematic for the purposes of buffering and pre-emphasis generation results in the conclusion that 60% of the CML power is used for signal-strength buffering in the primary path. Because 20Gb/s operation stretches the technology limits, low fan-out was required in this path which results in relatively high power consumption. Therefore, this

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Table 4.5: Equations for calculating block power from data in Table 4.4

<table>
<thead>
<tr>
<th>Result</th>
<th>Symbol</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary Current</td>
<td>$I_D$</td>
<td>$I_{VH_ON}+I_{VB_ON}$</td>
</tr>
<tr>
<td>Pre-Emphasis Current</td>
<td>$I_{D*}$</td>
<td>$I_{VH_OFF}+I_{VB_OFF}$</td>
</tr>
<tr>
<td>Buffer/Pre-Emphasis Power</td>
<td>$PBPE$</td>
<td>$V_{CC}\cdot(I_{VCC_ON}\cdot I_{D*})$</td>
</tr>
<tr>
<td>Output Stage Power</td>
<td>$POUT$</td>
<td>$V_{CC_AVG}[I_D, I_{D*}]+V_{DDH_AVG}[I_{DDH_ON}, I_{DDH_OFF}]$</td>
</tr>
<tr>
<td>VCSEL Power</td>
<td>$PVXL$</td>
<td>$V_{BIAS_AVG}[I_{BIAS_ON}, I_{BIAS_OFF}]$</td>
</tr>
<tr>
<td>Total Power</td>
<td>$PTOT$</td>
<td>$PBPE+POUT+PVXL$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fig</th>
<th>Description</th>
<th>ID</th>
<th>ID*</th>
<th>PBPE</th>
<th>POUT</th>
<th>PVXL</th>
<th>PTOT</th>
</tr>
</thead>
<tbody>
<tr>
<td>#</td>
<td>IMOD</td>
<td>PE</td>
<td>mA</td>
<td>mA</td>
<td>mW</td>
<td>mW</td>
<td>mW</td>
</tr>
<tr>
<td>4-9(a)</td>
<td>2-8</td>
<td>Y</td>
<td>21.4</td>
<td>6.0</td>
<td>76.5</td>
<td>29.0</td>
<td>16.0</td>
</tr>
<tr>
<td>4-9(c)</td>
<td>2-8</td>
<td>N</td>
<td>14.9</td>
<td>0.0</td>
<td>77.0</td>
<td>11.6</td>
<td>15.7</td>
</tr>
<tr>
<td>4-9(c)</td>
<td>2-10</td>
<td>Y</td>
<td>26.9</td>
<td>7.9</td>
<td>76.3</td>
<td>39.0</td>
<td>18.4</td>
</tr>
<tr>
<td>4-9(d)</td>
<td>2-10</td>
<td>N</td>
<td>19.2</td>
<td>0.0</td>
<td>77.0</td>
<td>15.5</td>
<td>18.7</td>
</tr>
</tbody>
</table>

Table 4.6: Calculated block power from equations in Table 4.5

---

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component of power has the potential to be reduced significantly with CMOS scaling. Other possible avenues to reducing power in future designs include using inductors to allow more efficient, higher fan out buffering without introducing ISI and replacing the passive termination with a more power-efficient method.

4.4 Summary

This chapter describes a full-rate pre-emphasis VCSEL driver with digital pulse shape control. Two 5-bit DACs control the modulation and pre-emphasis current and a four-tap digital delay line allows selection of the pulse with in the range of 30ps to 60ps. Pre-emphasis is therefore achieved completely with digital techniques, without requiring inductors, and both aspects of pre-emphasis are tunable in real-time. The architecture does not require clocking, as all pre-emphasis timing information is generated directly from the full-rate input data, which makes it particularly compatible with existing full-rate link architectures. Measured optical results demonstrate operation at 18Gb/s, where the pre-emphasis improves the horizontal and vertical eye opening, respectively, by 122% and 76%.
Chapter 5

20Gb/s Optical PAM-4 Transceiver Architecture

The previous chapter demonstrates that using pre-emphasis to compensate for VCSEL bandwidth limits allows 18Gb/s operation of 10Gb/s class VCSELs. The pre-emphasis approach increases the data rate through the bandwidth-limited channel and requires minimal changes to existing full-rate CDR architectures. However, full-rate 18Gb/s data paths and circuit techniques to compensate for VCSEL bandwidth limitations are achieved at the expense of increased power consumption. In future generations of package-to-package optical IO, it will be critical to simultaneously minimize power consumption and maximize per-pin data rate. Alternative link architectures may offer superior power consumption for a fixed per-pin data rate and must therefore be considered in order to achieve the best overall link performance. This chapter considers the application of four-level signaling to package-to-package optical links. Figure 5-1 compares a conventional binary (PAM-2) signal and a four-level (PAM-4) signal and illustrates the trade-off between symbol rate and signal levels. For a fixed total transmit power and bit rate, using a four-level transmit signal to encode two consecutive bits into a single symbol allows a doubling of the bit period at the expense of a three-fold reduction in difference between two adjacent power levels. This tradeoff is attractive because short-distance optical links are constrained by data rate and power consumption, but typically have large enough received optical power that
they are not noise limited. Therefore, reducing the received optical power per symbol level is acceptable if the resulting architecture allows a significant reduction in link power consumption. The transmitter for 20Gb/s PAM-4 signaling has a maximum on-chip data path speed of 10Gb/s and allows the optical components to operate at their nominal bandwidth, which results in a significant power savings over the 18Gb/s pre-emphasis transmitter.

While the front-end circuit designs differ significantly, many aspects of the PAM-4 receiver and CDR are common for electrical and optical links. The prior work section of this chapter therefore begins by reviewing several relevant papers on electrical PAM-4 transceivers, before moving on to discuss the conclusions of a recent board level demonstration of PAM-4 VCSEL modulation. Next, the receiver sensitivity for PAM-4 is reviewed. The third section describes the proposed transmitter architecture, which was designed in 90nm CMOS and is being fabricated at the time of writing. The final section compares the complexity and power consumption for PAM-2 and PAM-4 receivers and presents behavioral simulations for one possible PAM-4 receiver architecture.

5.1 Prior Work

Electrical PAM-4 links have been proposed as alternative to PAM-2 links in bandwidth limited high-speed serial applications. Due to the severity of the frequency
dependent losses in these backplane and cable applications, PAM-4 is often combined with equalization to achieve data rates in the range of 10Gb/s. A backplane link with decision feedback equalization and both PAM-2/PAM-4 capabilities at 2.5Gb/s to 10Gb/s is presented in [67]. An 8Gb/s PAM-4 transceiver, described in [2], employs both transmit and receive equalization and a novel linear edge detection scheme. A 20Gb/s PAM-4 receiver presented in [68] uses 2× interleaving with I and Q clock phases generated from a 10GHz reference clock to recover the received data. Because a reference clock and DLL are employed in the CDR, the loop dynamics allow implementation of the CDR logic after data demultiplexing which saves power and layout area. In each of the three designs, the CDR accounts for the fact that the PAM-4 eye is asymmetric and not all data transitions occur at the nominal optimal sampling point for all thresholds [69]. This requires selecting a subset of the data transitions, including the major and minor transitions, to consider during clock recovery in order to reduce the deterministic jitter potentially introduced by the asymmetric transitions.

One recent publication considers the application of PAM-4 signaling to optical links [70]. In this work, a standard transceiver chip set with built-in equalization and eye optimization in 0.13µm CMOS was used to modulate the VCSEL. The optical test platform uses a high-speed commercial photo-receiver and RF balun to convert the optical signal back to a differential signal for the receiver chip. The results demonstrate 8Gb/s (4GSym/s) operation and the paper concludes that bandwidth limitations and the increased reliability obtained by operating at lower bias (and therefore lower VCSEL bandwidth) are likely to overcome the PAM-4 power penalty and give PAM-4 an advantage over PAM-2 at data rates at and beyond 20Gb/s. This chapter describes the design and implementation of an integrated 20Gb/s PAM-4 driver for a 10Gb/s class VCSEL and a CppSim [71] behavioral model for an integrated PAM-4 receiver. Circuit simulations of the transmitter demonstrate a significant power savings over the pre-emphasis alternative and the fabricated chip will provide the first platform for testing a PAM-4 VCSEL link at 20Gb/s and verifying the conclusions of this prior work.
Table 5.1: Gray coding of two bits \((B0,B1)\) to \((\text{MSB},\text{LSB})\)

<table>
<thead>
<tr>
<th>B0</th>
<th>B1</th>
<th>Level</th>
<th>MSB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>3X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>2X</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1X</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0X</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

### 5.2 Receiver Sensitivity for PAM-4

Systems employing a PAM-4 architecture can tolerate lower bandwidth, but also require a higher receiver sensitivity since the available optical signal power is divided into four levels and the receiver must be able to differentiate between these reduced levels with low BER. While extra link margin is often available in short distance optical links, it is nevertheless necessary to understand the sensitivity implications of PAM-4 in order to determine whether it is appropriate for a particular application. While part of required increase in receiver sensitivity is a fundamental consequence of dividing the transmit power into four levels, other components may be avoided through good design practices including the use of the Gray code, summarized in Table 5.2, which guarantees that adjacent symbols differ by only one bit and therefore reduces the bit error rate. The following sensitivity analysis will assume that the architecture uses Gray coding.

Recalling the analysis of probability of error for a simple PAM-2 receiver presented in Chapter 2, we can extend this analysis to cover the case of a PAM-4 receiver. Figure 5-2 illustrates the probability density function for PAM-4, assuming again that the noise is independent of the signal level. In a PAM-2 receiver, only one tail of each distribution crosses a decision threshold - the one and zero signals may have arbitrarily large positive and negative noise, respectively, without triggering an error and the probability of error may be calculated as in (2.9). For PAM-4, the analysis is somewhat more complicated so we begin by making the simplifying assumption that errors due to signals crossing non-adjacent thresholds are negligible compared to errors due to signals crossing adjacent thresholds.
With this assumption, the problem is then reduced to a set of simpler problems similar to the PAM-2 analysis. We observe that only one distribution tail for the ‘00’ and ‘10’ levels crosses a threshold, while both tails for the ‘01’ and ‘11’ levels cross thresholds and result in bit errors. Since we have used coding to guarantee that adjacent level errors result in only one bit error each and we assume that the four levels are transmitted with equal probability and that the signal power is equally divided between levels, the probability of error may then be expressed as (5.1). Finally, if we relate the total optical power modulation of the PAM-2 and PAM-4 systems, such that $P_{00}=P_0$ and $P_{10}=P_1$, the results now allow a direct comparison of the relative sensitivities of each system.

$$P_E = \frac{3}{2} \left[ Q\left(\frac{v-vt}{V_{no}}\right) \right]$$  \hspace{1cm} (5.1)

The expression for the PAM-2 BER is repeated in (5.2) for comparison and the simplified expression for the PAM-4 BER is given in (5.3). Assuming that we require a BER of $10^{-12}$ in both cases, then numerical methods may be applied to determine
that the Q-function argument must equal 7.035 in (5.2) and 7.091 in (5.3), where the small difference results from the leading factor of 1.5 in the PAM-4 equation.

\[ P_E = Q \left( \frac{R \cdot (P_1 - P_0)}{2 \cdot I_{\text{eq}}} \right) \quad (5.2) \]

\[ P_E = \frac{3}{2} \left[ Q \left( \frac{R \cdot (P_1 - P_0)}{6 \cdot I_{\text{eq}}} \right) \right] \quad (5.3) \]

Simulations of the TIA indicated that the total equivalent input current noise is \( I_{\text{eq}} = 2 \mu A \), though measurements suggest that a higher noise value of \( I_{\text{eq}} = 4.3 \mu A \) is present in the fabricated TIA. Therefore, the PAM-4 link budget will be considered for both cases. From (5.3), with \( I_{\text{eq}} = 2 \mu A \) the required signal current is 85 \( \mu A \) and with \( I_{\text{eq}} = 4.3 \mu A \) the required current is 183 \( \mu A \). Assuming a photodiode sensitivity of \( R = 0.6 \) in both cases, then the respective received optical modulation powers must be 0.14mW (-8.5dBm) and 0.30mW (-5.2dBm) for the PAM-4 system. This represents a 3\( \times \) (4.8dB) penalty over the required received optical power of 0.05mW (-13.3dBm) and 0.10mW (-10dBm) for the PAM-2 case. If we assume a transmitted VCSEL power of 0dBm, the PAM-4 architecture link budget can be met for \( 10^{-12} \) BER if the total optical link loss can be reduced to between 5dB-8dB. Results near this range have already been reported in [22] and loss may be further reduced as optical packaging technology improves. Furthermore, the TIA noise estimates considered here are based on a TIA optimized for bandwidth and power consumption, so redesigning to improve noise performance could add margin to the link budget. Therefore, PAM-4 architectures for short distance optical links are feasible from the perspective of sensitivity and BER.

### 5.3 Transmitter Architecture

Once it is determined that PAM-4 signaling is the best alternative given the system specifications and channel loss, the next step is designing a transmitter to modulate
a VCSEL between four power levels. This must be accomplished with minimized timing jitter, minimized electrical power consumption, and maximized linearity and symmetry between the optical power levels. Figure 5-3 illustrates the relationship between drive current, output power, and threshold levels for an idealized VCSEL current-power curve. The VCSEL is modulated between four current levels above threshold to generate four optical power levels. The resulting optical signal must be converted back into the electrical domain at the receiver and then sampled at three thresholds to determine the transmitted level.

In order to improve the current matching between the MSB and LSB current levels and to minimize any skew between the two paths due to differential loading, the complete output stage is assembled from an output stage unit cell as shown in Figure 5-4. The MSB has two unit cells and the LSB has one unit cell, which results in the desired binary weighting between the two bits. In the fabricated test chip, the two inputs are driven by separate taps from an on-chip PRBS. In order to minimize skew, a dummy buffer is used to match the delay of the MSB and LSB paths.

The circuit implementation of the output stage is shown in Figure 5-5. The unit cell applies the cascode circuit described in Chapter 4 to isolate the differential pair devices from the VCSEL voltage swing in order to improve current matching. The LSB cell is physically located between the two MSB cells in order to minimize any MSB/LSB mismatch due to process gradients across the output stage. A common bias current, $I_B$, is shared by all three output cells and generated by a 5b DAC (not shown).
on the test chip. A 50Ω output termination resistor is included for compatibility with the package and is biased to an independent supply, \( V_H \), for maximum flexibility in testing. However, due to the more predictable biasing conditions in the PAM-4 driver, it is expected that this supply will be set to the same 1.2V as the nominal on-chip \( V_{CC} \).

The circuit layout of the PAM-4 VCSEL driver including the buffers, output stage, and termination is shown in Figure 5-6. Because chip measurements are not available at the time of writing, electrical and optical simulations of the output driver are presented. Electrical simulations are based on capacitive parasitic extracted layout netlists and optical simulations are performed using the method described in Chapter 2. The transmitter was simulated for various VCSEL biases and modulation depths, but a single representative simulation from 3mA to 10mA is included and described in this section.

The junction current is determined by simulating the extracted driver circuit and the result is exported to Matlab, where the ODE45 differential equation solver is used to determine the optical output power as a function of input current and time according to the derived differential rate equation model. The eye diagrams of Figure 5-7 show the extracted electrical simulation of the junction current and the optical power eye diagram, which is obtained by using the junction current waveform.
Figure 5-5: Multilevel VCSEL driver output stage schematic

Figure 5-6: Layout of PAM-4 VCSEL driver with buffers and output stage
Junction Current and TX Power – PAM-4

Figure 5-7: Circuit simulations of junction current and optical power simulation

as the input to the ODE solver for the fitted VCSEL rate equations. These transient results show the expected dynamics including slight overshoot on the rising edge and longer tails on the falling edge. Additionally, the slope efficiency is well matched to the actual VCSEL. An optical modulation amplitude (OMA) of 3mW is simulated for an input current of 3mA to 10mA, which corresponds to a slope efficiency of 0.43 and the data sheet specifies slope efficiency at 0.4. However, due to a lack of acceptable data for fitting, the model does neglect thermal rollover which may introduce nonlinearity for larger VCSEL currents. The optical dynamics introduce relaxation oscillations in the transient response and significantly reduce the optical rise time.

The power consumption for the PAM-4 driver is significantly reduced in comparison to the pre-emphasis driver. This is possible because pre-emphasis generation is not required and CML fan-out is reduced since each path is operated at 10Gb/s instead of 18Gb/s. Three CML buffers placed before the output stage consume a constant total current of 9.6mA from a 1.2V supply for a power consumption of 11.5mW. For the output stage, we assume that each data bit is equally likely to occur when calculating power consumption. The VCSEL supply of 3.04V provides the 3mA for the lowest power level and 10mA at the highest power level, for an average power

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of 19.76mW. The termination supply of 1.2V sinks the VCSEL bias current of 3mA for the lowest power level and sources 6mA at the highest power level, for an average power of 1.8mW. Finally, the core supply of 1.2V provides the total modulation current of 16mA to the output stage during transmission of the lowest power level when no modulation current is switched to the dummy load cascodes and supplies no current when the total modulation current is switched to the VCSEL. This results in an average power consumption of 9.6mW. When all four of these power components are summed, the transmitter consumes a total of 42.7mW, which is equivalent to 2.1mW/Gb/s at 20Gb/s.

5.4 Receiver Architecture

While PAM-4 offers clear advantages in power consumption and timing at the transmitter, the receiver design is necessarily more complex than a PAM-2 architecture. Prior work on circuits and architectures for electrical PAM-4 links may be directly applied to the design of an optical PAM-4 receiver, since only a few key aspects differentiate the optical and electrical designs. In particular, the optical receiver must convert a small input photocurrent with a DC offset into a larger voltage signal which can be sampled at the three thresholds. Aside from these differences in the front-end of the receiver, the same clock and data recovery architectures can be used for both optical and electrical PAM-4. The received data is amplified in a linear manner and sampled at three thresholds to determine the transmitted symbol, in contrast to the simpler nonlinear amplification and single threshold sampling required for PAM-2. Furthermore, as described in [69], PAM-4 transitions do not all occur at the optimal edge center point and additional CDR logic is therefore required to select the edge transitions with nominally correct timing information for use in the clock recovery process.

Because minimization of total optical link power consumption is desired, it is important to verify that the additional receiver complexity for PAM-4 will not negate the power reduction achieved at the transmitter. Accurate modeling of the power
consumption requires technology-specific knowledge of noise and power performance for TIA and amplifier circuits at different bandwidths, but simple approximations are possible by comparing the number of high-speed CML latches required in each receiver. Several electrical receivers in 90nm CMOS using PAM-2 [8], [9] and PAM-4 [68] have employed interleaved sampling at 5GHz, which indicates that this frequency provides a good balance between latch speed and receiver complexity. To achieve 2× oversampling, a PAM-2 receiver at 20Gb/s then requires four phases sampling at both edges on a single voltage threshold. In comparison, 20Gb/s PAM-4 requires two phases sampling at both edges on three separate voltage thresholds. As five latches are required to achieve dual-edge sampling for each phase, this results in a total front-end CML latch count of 20 for PAM-2 and 30 for PAM-4, which can be used to make a first order power comparison based on the per-latch power consumption. In practice, more accurate analysis must account for technology-dependent differences in power consumption of the TIA, linear voltage-shifting amplifier, and clock generation and distribution. This analysis should be undertaken in order to determine the power consumption implications of PAM-4 for each particular technology and system specifications.

While circuit implementation of a PAM-4 receiver is beyond the scope of this thesis, a combination of behavioral simulations and circuit simulations are presented to demonstrate the feasibility of a PAM-4 optical receiver and CDR. Behavioral simulations are presented for a PAM-4 CDR architecture based on a delay-locked loop with phase interpolation and using 8:1 demultiplexing and 1.25Gb/s logic for correct edge selection and timing recovery, which shares several architectural features with previous electrical PAM-4 work [68]. As the transimpedance amplifier and front-end sampling latches comprise the critical timing path for the receiver, circuit simulations are completed for these blocks using manual adjustment of TIA offset cancellation and clock phase. Behavioral simulations are performed using CppSim, a tool designed specifically for the behavioral simulation of PLL/DLL circuits [71], [72]. By representing the two binary data states as ±1 and encoding the exact transition timing in continuous value of the transition sample on $-1 < x < 1$, the tool allows accurate
A block diagram of the proposed receiver architecture is shown in Figure 5-8. The optical input signal reaches the photodiode and TIA, where offset cancellation occurs and the data is converted from a single ended optical power signal to a differential voltage signal. Optionally, additional linear amplification or an AGC amplifier may be added after the TIA to relax the timing constraints on the sampling latches. Following the TIA and gain stages, a level-shifting amplifier stage with a shared input and three distinct outputs shifts the input data by minus one LSB to test T23, zero to test T12, and plus one LSB to test T01. Shifting the differential signal level as described essentially adjusts the data level such that the decision threshold occurs at the point where the positive and negative differential data signals are equal. This allows simple differential CML latches to sample the three shifted signals and resolve the transmitted data bits. The level shifting amplifier of Figure 5-9 [2] is included in the receiver circuit simulations in this chapter, but alternative topologies featuring digital word control of level shift have also been proposed in the literature [68].

After the level shifter, the three linear signals are sampled with regenerative latching comparators to choose binary values for the received data. This is the first synchronous block within the receiver and therefore requires a discussion of the clocking
Figure 5-9: Level shifting pre-amplifier [2]

and CDR design. In order to increase the time allowed for the front end latches to resolve metastability in the edge transitions, $2\times$ interleaving and dual-edge sampling are employed to obtain the $2\times$ oversampling required for the implementation of a bang-bang CDR. The two required clock phases may be generated from a 10GHz reference clock by using a phase interpolator and an I/Q divider. As discussed in Chapter 2, in a bi-directional transceiver architecture where both TX and RX capability are implemented on both ends of the link, the use of a 10GHz clock introduces little overhead since transmit PLL blocks on both chips must already generate 10GHz clocks and could easily be locked to a shared reference due to their relatively short distance separation. Therefore, the data frequency is known a priori and the CDR is only required to recover the phase, which allows a DLL architecture to be used and eliminates any frequency acquisition range problems. This simulation used a simple behavioral model of a digital phase interpolator with 64 equal phase steps covering the complete $2\pi$ radians, but several circuit implementations of digital phase interpolators have been proposed in the literature [73], [74].

The proposed latch configuration and timing diagram for receiver operation is shown in Figure 5-10, where signals that would be differential in a circuit implementation are shown as single ended for schematic clarity. Each of two 5GHz quadrature clocks drives a bank of five latches and performs an immediate 2:1 demultiplexing by collecting data and edge samples on both the rising and falling edges of the clock. The
Figure 5-10: 2x oversampling front-end latch schematic and timing

Figure 5-11: Circuit simulation of receiver front end
circuit simulation of Figure 5-11 shows the TIA output and recovered data samples obtained when the TIA, level shifter, and data latches are simulated with manually adjusted offset and clock phase. (In the figure, the MSB and LSB are remultiplexed and phase shifted into alignment with the TIA output to allow easy visual verification that the correct data is recovered.) This simulation verifies that 5GHz sampling is possible in 90nm CMOS for the small voltage swings present in the optical front end.

The logic for PAM-4 clock recovery is relatively complex compared to the logic in a PAM-2 CDR. Therefore, in order to reduce power consumption and design complexity, the data and edge samples can be demultiplexed and the CDR logic and digital loop filter can be implemented in standard CMOS logic. The demultiplexed data rate must be low enough to allow standard CMOS logic and, in most applications, this implies that the most practical choice will be to demultiplex to the on-chip logic clock frequency. Latency due to demultiplexing is inside the CDR feedback loop and the digital filter must limit the phase update rate accordingly to stabilize the loop. Since this limits the tracking rate of the CDR, demultiplexing beyond the level required for standard CMOS logic should be avoided. In the presented simulation, 2:8 demultiplexing reduces the bit rate to $8 \times 1.25$Gb/s on each of the three data and edge sample levels for a total of 48 ($8 \times 3 \times 2$) parallel paths. This set of data contains all the necessary information to recover the transmitted data bits and the clock phase.

In order to understand the need for special CDR logic in a PAM-4 receiver, it is useful to consider the simple RC limited PAM-4 eye diagram of Figure 5-12. The bottom, center, and top thresholds are indicated with dotted lines and threshold crossing times for each possible data transition are shown with the various symbols indicated in the legend. For a transition beginning at time $t=0$, the optimal halfway point will occur at $t=0.69\tau$. An inspection of this figure reveals that only transitions that are symmetric around a particular threshold cross the threshold with this optimal timing. Asymmetric transitions will occur as early as $0.18\tau$ and as late as $1.79\tau$, which would give the jitter distribution a bimodal component if all center threshold transitions were used in clock and data recovery as is the case for a PAM-2 receiver. Instead, a PAM-4 receiver should use only the transitions indicated with circles,
which include the center threshold crossing of the major transition from the lowest to highest level and each minor transition when only a single threshold is crossed. The squares indicate additional transitions that could potentially be incorporated if higher transition density were required for the CDR, but these transitions are generally ignored since including them would increase receiver complexity by requiring the introduction of an additional two thresholds not used for data sampling.

Logic for generating early and late signals is implemented in the behavioral model based on the previous work [69], [67]. The early and late signals from the eight parallel sets of PAM-4 transition logic are combined with a majority voter. This information is then input to a digital loop filter to determine whether the clock phase should be updated. This loop filter should maximize the tracking rate while providing sufficient delay to eliminate unnecessary limit cycles in the phase interpolator which occur when updates do not have sufficient time to propagate through the loop before additional updates occur. Optimal digital filter design will vary with application and is an interesting area for ongoing work, but a relatively simple filter was chosen for this work and is described here. The filter is programmed to wait a defined number of 1.25GHz clock cycles between phase interpolator updates, and the phase interpolator
is updated when an early/late is received only if sufficient time has passed since the last update. In addition, locked and unlocked states are defined, which allows a reduction in the wait time to improve slew rate when the loop is unlocked and an increase in the wait time to improve stability when the loop is locked. The loop declares itself to be unlocked after issuing a set number of consecutive up or down phase adjustments and to be locked again after issuing an adjustment in the opposite direction. In the presented simulations, the loop updates every sixth cycle when the loop is locked and every cycle when the loop is unlocked. Four consecutive adjustments in the same direction are required before the filter determines that the loop is unlocked. While further investigation of loop filter design will likely yield an improved trade-off between update latency and stability, the basic digital loop filter presented here attains reasonable tracking bandwidth without introducing limit cycles while the loop is locked. This design will therefore be used in behavioral simulations of the CDR loop to demonstrate the performance improvement that is achieved when edge transitions with bad timing information are ignored during clock recovery.

Instead of implementing circuit-like behavioral models of the TIA and linear level shifting amplifier in CppSim, a higher level behavioral block was designed to directly generate three signals with edges occurring according to the timing described in Figure 5-12. This approach takes advantage of the fundamentally behavioral nature of
the simulator and allows fast simulation of the complete CDR. At each step, two random bits are generated and compared to the previous bits to determine which thresholds will be crossed to reach the next data state and how each threshold crossing should be timed. This data is then input to the front end latch stages of the CDR architecture which, with the exception of the TIA and level shifting amplifier, is completely implemented in CppSim. Figure 5-13 compares the simulated performance of the PAM-4 receiver to a receiver applying a PAM-2 center transition clock recovery technique to PAM-4 data. During the first 1μs of the simulation, the CDR tracks a ±0.25UI 1MHz input phase variation and during second half the CDR is locked to data with constant phase. While both CDR architectures demonstrate good loop stability, the PAM-2 CDR exhibits excursions from the correct phase during steady-state as a result of updating based on bad timing information. PAM-4 logic improves tracking performance and eliminates these phase excursions.

The behavioral PAM-4 CDR implementation demonstrates several important aspects of the PAM-4 receiver. The results show that a DLL architecture based on demultiplexed data is feasible from a stability perspective, which allows the implementation of the more complex PAM-4 CDR logic with higher parallelism and that PAM-4 CDR logic significantly improves the jitter performance of the PAM-4 receiver.

5.5 Summary

This chapter describes the system-level advantages and concerns for optical PAM-4 IO and presents a PAM-4 VCSEL transmitter implemented in 90nm CMOS and a behavioral implementation of a PAM-4 CDR. System-level and sensitivity calculations indicate that the present TIA design can achieve a PAM-4 BER of 10^{-12} for a minimum input current of 183μA, which is within the expected range for existing transceiver packages. The total transmitter power is reduced to 42mW, which is a significant improvement over the power consumption of the full-rate pre-emphasis transmitter. Circuit simulations of the optical receiver front end and behavioral simulations of a PAM-4 CDR demonstrate an implementation of a PAM-4 receiver.
Chapter 6

Conclusions

6.1 Summary of Contributions

This thesis explores circuit techniques to maximize the performance of a short optical link using commercial GaAs VCSELs.

In the core voltage amplifier proposed for use in the TIA, the cross-coupled cascodes double the amplifier gain compared to a standard cascode amplifier and extend the bandwidth by introducing peaking. The proposed common-mode feedback configuration allows broadband TIA operation. The TIA achieves 9GHz bandwidth with 250fF input capacitance and TIA measurements demonstrate 18Gb/s operation with 90fF capacitance and 12.5Gb/s operation with 260fF of capacitance.

The pre-emphasis VCSEL driver is among the fastest reported CMOS drivers for a commercial GaAs VCSEL. It provides digital tuning of pulse width, pulse height, and modulation depth and generates timing information directly from the full-rate input data in a manner that is compatible with standard full-rate link architectures. Optical measurements demonstrate 18Gb/s operation.

The PAM-4 transmitter achieves a simulated data rate of 20Gb/s. Encoding two bits per symbol reduces the bandwidth requirements for both the VCSEL and the on-chip data paths, resulting in reduced power consumption of only 2.1mW/Gb/s.
6.2 Conclusions and Future Work

This dissertation demonstrates several circuit techniques to increase the data rate through a channel with bandwidth-limited optical components. In future technology generations, interconnects must continue to scale with both increased data rate and reduced power consumption. A strong correlation presently exists between data rate and power consumption, so techniques to reduce the coupling between these two performance metrics are critical. Ongoing opportunities exist to impact link performance through the optimization of front-end circuits and optical devices. While circuit techniques can be applied to increase the data rate through existing optical components, increasing the electrical and optical bandwidth of optical devices would have a direct impact on performance. According to the demands of the particular application, improved optical device performance would allow either reduced power consumption for a fixed data rate or increased data rate for a fixed power consumption. Improved optoelectronic CAD will be essential for future optimized circuit design.

Despite circuit optimization, however, relatively higher power consumption is inevitable if the link architecture constrains the circuits and optical components to operate near their bandwidth limits. Architectures that reduce the bandwidth requirements for individual circuits without compromising data rate could therefore have a significant impact on system performance. The presented PAM-4 driver, receiver, and CDR comprise one alternative architecture and the transmitter achieves significantly reduced power consumption at 20Gb/s compared to the full-rate alternative. One complicating aspect of PAM-4 is the increased receiver complexity - several reference levels are required and cancellation of systematic jitter and offset may be necessary as the received data is sampled with several different latch banks. Interleaved, multi-phase architectures have similar complexities which have presented a barrier to adoption beyond the research community. Both architectures would become much more practical for product-level integration if low-power, automatic digital techniques could be applied to cancel offsets, set reference levels, and adjust clock phases. By making more complex architectures practical from a manu-
facturing perspective, such digital techniques could have a direct impact on the power and bandwidth performance of optical interconnect. The following sections provide more detailed analysis of areas for future work with the potential to impact the power consumption and data rate of optical interconnect.

6.2.1 Device Scaling

Supply voltages for core CMOS logic are scaling to 1V and below in future technology generations. Scaling of VCSEL supply voltages is inherently limited by the 1.5V bandgap-defined threshold of GaAs VCSELs, but decreased VCSEL resistance would allow smaller voltage swing across the device for a fixed output power. This would facilitate the design of VCSEL drivers in the core CMOS voltage and reduce power consumption. VCSEL and photodiode devices must continue to achieve reduced capacitance and higher bandwidth, and new circuit designs will be required to take full advantage of the new optical device performance. Depending on the limiting metric for the particular interconnect, these techniques could target lower power for a fixed data rate or higher data rate for a fixed power consumption.

6.2.2 Optoelectronic CAD

While several research papers have proposed techniques for modeling VCSEL devices at various levels of complexity, there is no existing standard for large-signal modeling of VCSEL devices and manufacturers rarely provide modeling information beyond a few S-parameter measurements in VCSEL data sheets. This leaves the circuit designer of a driver for a commercial VCSEL with the task of developing a device model based on limited device measurements and estimates of physical parameter information. The accuracy of such a model is inherently limited and the circuit design must therefore include features to adjust the driver parameters for optimal performance. Such features come at the expense of area and power consumption, so improvement of VCSEL models would result in better circuit performance as well as reduced design time. Many circuit simulators have introduced support for flexible behavioral model-
ing tools such as Verilog-A. Development and distribution of an accurate behavioral VCSEL model including process corners, noise, and thermal effects would allow faster development cycles and further optimization of VCSEL driver performance.

6.2.3 Hybrid Analog-Digital Techniques

As CMOS technology scales, exponentially improving digital performance is bought at the expense of degraded analog performance. Mismatch and offset have an increasing impact on performance, while small blocks of digital logic may be integrated together with analog blocks at a negligible power and area cost. This trend suggests that high-performance analog and RF circuits in the future may benefit from the use of digital techniques to compensate for analog mismatches. Furthermore, digital circuits and state machines could be used to adapt transceivers based on varying parameters of the optical components of the channel. In the proposed front-end circuits of this dissertation, there are several opportunities for this type of hybrid approach. In the pre-emphasis VCSEL driver, digital control knobs for pulse width, pulse height, and modulation depth are included and adjusted manually for this design. Development of digital techniques to set these driver parameters would make this design self-sufficiently robust to VCSEL variation and even more attractive for manufacturing. At the receiver side, the CMFB TIA topology includes a DAC to set the DC offset cancellation current. Most techniques for DC offset rely on low-pass filter feedback which limits the bandwidth of the receiver. Implementation of digital techniques, possibly in conjunction with transmitter training sequences, could allow automatic calibration of the bias current and allow operation down to DC for links required to operate for uncoded data. In the PAM-4 receiver, digital logic and offset calibration algorithms could be applied to set levels for the level shifting amplifier. Offsets associated with the individual data and edge latches could be calibrated automatically to reduce systematic jitter. Such techniques offer significant performance enhancements for analog blocks at negligible cost, and therefore have significant potential to impact performance in future optical links.
6.2.4 System-Level Optimization

Implementation of digital techniques for cancellation of analog offset and mismatch will create new possibilities for the types of link architectures that can be integrated in high-volume products. While full-rate transmitter architectures are presently preferred as a result of their lower systematic jitter, low cost techniques for correcting the offset of interleaved architectures could allow link designers to capture the potential power consumption benefits of such techniques. Digital techniques for automatic threshold generation and offset cancellation would allow transmission of uncoded data and make receivers more robust and self-calibrating. Careful system-level design will allow the selection of the best architecture and signaling scheme for a given combination of data rate, power consumption, area, optical device performance, channel, and CMOS technology. Circuit optimization within the context of a well-chosen link architecture will result in the best overall performance as optical transceiver designs pursue high-speed and low-power performance in future technology generations.
Bibliography


