Carbon Nanotube Field Effect Transistors for Power Application

by

Tao Pan

Submitted to the Department of Electrical Engineering and Computer Science
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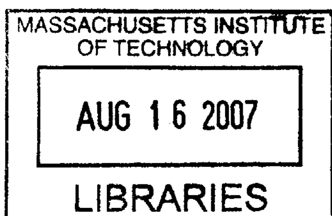
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Abstract

Carbon nanotubes (CNTs) are nanometer-diameter cylinders formed from rolled-up graphene sheets which have found widespread interests due to their many excellent electrical properties. In particular, most of them are direct bandgap semiconductors from which carbon nanotube field effect transistors (CNTFETs) can be made. The small feature size and high electron mobility of the CNT makes it attractive and a good candidate to replace modern MOSFETs.

So far, most fabricated CNTFETs conduct currents only on the order of microamps under low voltage bias which cannot be used to drive large output loads. In this work, we attempt to explore the ultimate performance benefits from utilizing multiple CNTs for CNTFETs. Two ways of making multi-tube CNTFETs are demonstrated in this thesis. Devices are fabricated, measured and analyzed. A simple model is used to evaluate the ideal ballistic behavior of CNTFETs. Parasitics that are measured from experiments and extracted from numerical tools are added to the model. As an application, we compare the performance of CNTFETs with MOSFETs, both used as power transistors in a Buck DC-DC converter circuit.

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Chapter 1

Introduction

1.1 Motivation for Utilizing Carbon Nanotube Devices in IC Design

Aggressive scaling of CMOS devices over different technology generations has led to higher integration density and better performance. However, shrinking the conventional MOSFETs beyond the 45nm-techology node faces severe barriers due to the fundamental physics that constrains the conventional MOSFETs, such as exponential increase in leakage current, large parameter variations caused by weak control of dopant atoms, quantum-mechanical tunneling of carriers through the thin gate oxide [11]. Hence, research has started in earnest to consider alternative devices and circuit architectures in the sub-50nm era. Among them, carbon nanotube field effect transistors are of particular interest.

Compared to MOSFETs, CNTFETs have several advantages. First, because of its one dimensional structure, near ballistic transport of carriers can be achieved which makes possible ultra fast and high efficient devices. Second, high-κ dielectric materials can be used as gate dielectric without degrading carrier transport in the channel due to the absence of dangling bonds in carbon nanotubes. This leads to efficient gate field coupling that results in low subthreshold slope.

CNTFETs have been previously reported and have achieved high performance

[7][5][9]. Simple logic gates (inverter, NOR, SRAM and ring oscillator) and analog circuit (mixer) using CNTFETs have been demonstrated [12][13][14]. Although these circuits show potential and some of them operate at frequency as high as 50GHz [13], a lot of challenges exist for nanotubes to fully replace CMOS technology. Thus, a hybrid system where CNTFETs are selectively integrated into a CMOS chip is a plausible approach to demonstrate the advantage of nanotube devices and to improve circuit performance.

1.2 Background on CNT Structure, Properties, and Synthesis

1.2.1 Carbon Nanotube Structure

Chirality

The structure of carbon nanotubes has been explored by high resolution TEM and STM techniques, yielding direct confirmation that the nanotubes are cylinders derived from the honeycomb lattice structure of the graphene sheet. Graphene sheet is shown in Figure 1-1(a). The structure of the nanotube is uniquely determined by its circumference vector $\vec{C}_h = n\hat{a}_1 + m\hat{a}_2$ which connects two crystallographically equivalent sites on a 2D graphene sheet. The cylinder connecting the two hemispherical caps of the carbon nanotube is formed by superimposing the two ends of the vector $\vec{C}_h$. In the (n, m) notation for $\vec{C}_h = n\hat{a}_1 + m\hat{a}_2$ the vectors (n,0) or (0,m) denote zigzag nanotubes and the vectors (n,n) denotes armchair nanotubes. All other vectors (n,m) correspond to chiral nanotubes. Figure 1-1(b) shows typical nanotube structures of different chiralities.

Single Wall and Multi Wall Carbon Nanotubes

When folding graphene layers into carbon cylinders, one can possibly get a single shell - single wall carbon nantubes (SWCNTs) or several shells - multi-wall carbon

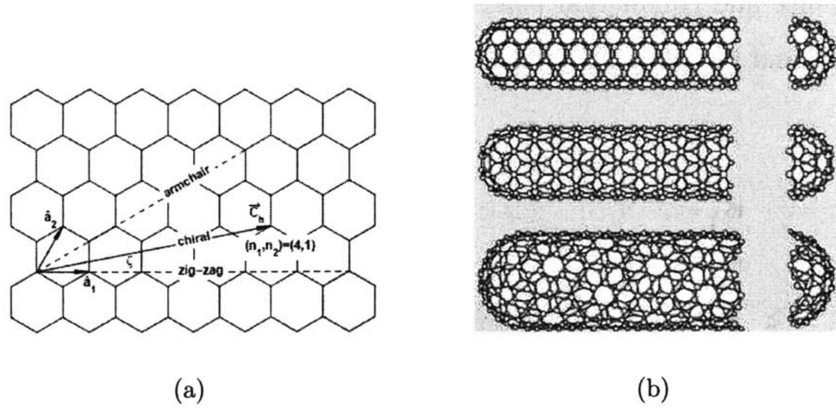


Figure 1-1: Schematic models for grahene sheet and single-wall carbon nanotubes. (a) The chiral vector $\vec{C}_h = n\hat{a}_1 + m\hat{a}_2$ is defined on the 2D graphene sheet lattice [1]; (b) Three types of nanotube structures. Shown here is a (5,5) armchair nanotube(top), a (9,0) zigzag nanotube(middle) and a (10,5) chiral nanotube(bottom) [2].

nanotubes (MWCNTs). MWCNTs consist of concentric CNT cylinders held within each other by van der Waals forces. The distance between shells is approximately 3.4 Å , which is close to the distance of two carbon layers in graphite.

The concentric shells of MWCNTs can differ in their chiralities and can consist of both semiconduting and metallic nanotubes. If a MWCNT consists of both semiconduting and metallic cylinders, the metallic shells can negate the possible semiconducting properties. As a consequence, MWCNTs have a limited use as field effect transistors. And thus for the rest of the work, we will be focusing on the SWCNTs.

1.2.2 Electrical Properties

Metallic and Semiconducting CNTs

Because carbon nanotubes are rolled up graphene sheet, in the circumferential direction periodic boundary conditions apply. The reciprocal space is obtained by doing Fourier Transforms to the real space structure of CNTs. A periodical lattice structure corresponds to a discrete energy dispersion relation, which can be viewed as sampling the graphene $E - \vec{k}$ relation along the directions of certain wave vectors $\vec{k}$. Figure 1-2 shows the energy dispersion relation of the graphene. The π curve and $\pi *$ curve

are the valence and conduction band respectively. At the K point, the valence and conduction band intersects, resulting in a zero bandgap in graphene.

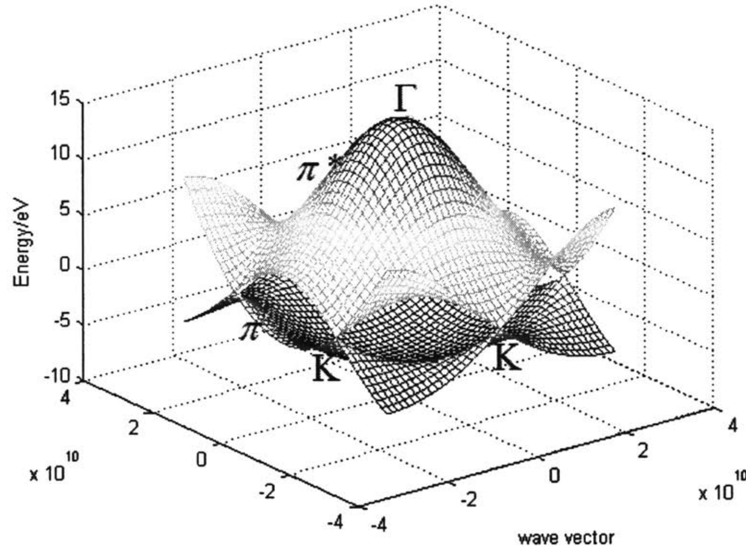


Figure 1-2: Energy dispersion relation of graphene

Figure 1-3 shows how carbon nanotube's energy dispersion relation is obtained from discretizing graphene's Brillouin zone.

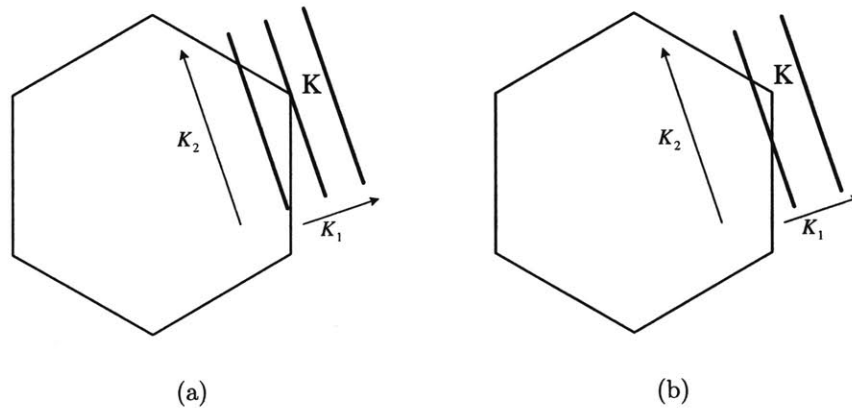


Figure 1-3: The wave vector k of CNT is shown in the Brillouin zone of graphene. (a) metallic tubes $n - m = 3q$; (b) semiconducting tubes $n - m \neq 3q$.

If the wave vector contains the K point (Figure 1-3(a)), there is no bandgap in the nanotube band diagram, so that the tube is metallic. On the other hand, if the wave

vector doesn't contain the K point (Figure 1-3(b)), the conduction and valence bands don't intersect creating a gap between them and the nanotube shows semiconducting behavior. Theoretical analysis further reveals how chirality vector numbers n and m determine the conductivity of CNTs:

$$n - m = 3q \quad \text{metallic} \tag{1.1}$$

$$n - m \neq 3q \quad \text{semiconducting} \tag{1.2}$$

where q is an integer [15]. Therefore, all armchair (n, n) nanotubes are metallic. Only 1/3 of the possible zigzag $(n, 0)$ nanotubes are metallic and 1/3 of the chiral nanotubes are metallic. Figure 1-4 plots the one dimensional energy dispersion relations for 3 different chiralities of nanotubes.

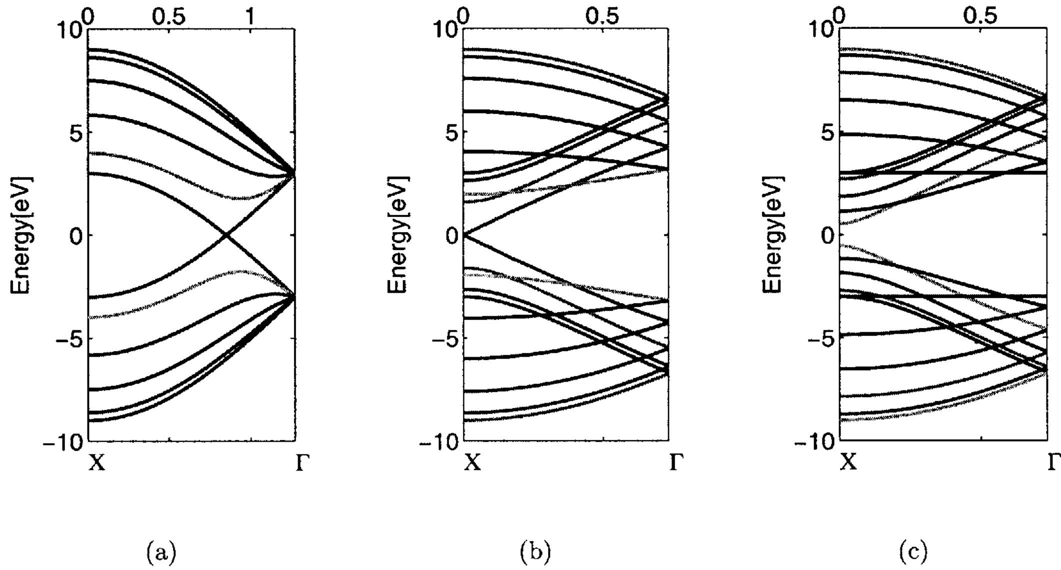


Figure 1-4: One-dimensional energy dispersion relations for (a) armchair(5,5) nanotubes; (b) zigzag(9,0) nanotubes; (c) zigzag(10,0) nanotubes.

For semiconducting tubes, the bandgap E_g is determined by

$$E_g = 0.8/d\, eV \tag{1.3}$$

where d is the diameter of the naotube and is again determined by the chirality vector,

$$d = \sqrt{3}a_{C_C}(m^2 + mn + n^2)^{1/2}/\pi = C_h/\pi \tag{1.4}$$

where a_{C_C} is the C_C bandlength in graphene. A typical single wall carbon nanotube with a diameter of 1.7nm thus has a bandgap of around 0.47eV.

Electron Mobility Characteristics

Owing to their molecular uniformity and quasi-one-dimensional nature, nanotubes is expected to exhibit near ballistic transport properties. [16] and [17] report electron mobility in the range of $10^3 \sim 10^4$cm^2/V·s with the value derived from conductance experiments in transistors. Theoretical prediction also yields a mobility of 10^4cm^2/V·s in semiconducting tubes of radii up to ~2nm [18].

The current carrying capacity of multi-wall nanotubes has been demonstrated to be more than 10^9A/cm^2, without degradation (such as that due to electromigration) after several weeks well above room-temperature [19].

For CNTFETs, there're theoretical predictions that the normalized current density of a 1nm-diameter single wall nanotube can reach the order of 10^8A/cm^2 [1].

1.2.3 Chemical Vapor Deposition (CVD) Synthesis

SWCNTs are difficult to grow. Currently, there are three methods to produce mass quantities of SWCNTs with a reasonably high yield, namely, arc discharge, laser ablation and CVD. Most of these processes take place at high temperatures. Large quantities of nanotubes can be synthesized by these methods. Advances in large scale and growth processes are making CNTs more commercially viable.

Among these methods, chemical vapor deposition shows most promise for industrial scale manufacturing in terms of low cost. It also has other advantages that it is capable of growing nanotubes directly on a desired substrate. The growth site is controllable by careful deposition of the catalyst. Also aligned nanotube growth has been made possible by controlling the direction of gas flow.

During a CVD, a substrate is prepared with a layer of metal (nickel, cobalt, iron) catalyst particles. This substrate is heated to approximately 900°C, with two gases - process gas (ammonia, nitrogen, hydrogen, etc) and carbon-containing gas (acetlylene, ethylene, ethanol, methane, etc) - to flow through the reactor to initiate the growth. the carbon-containing gas molecules decomposed at the surface of the catalyst particle, and the carbon dissolves. Once the solution becomes saturated, carbon will precipitate out in the form of CNTs. The detailed steps in this mechanism are still not well understood.

However, there're limitations with current CVD growth. For example, the chirality cannot be fully controlled by this process. Only a certain range and distribution of CNT diameters can be achieved by changing catalyst size and gas flow.

1.3 Thesis Contribution and Overview

In this work, we are focusing on making CNTFETs with large current carrying capacity that can be used in a hybrid CNT/CMOS system, in particular, a DC-DC converter circuit with the CNTFETs as power transistor switches. Chapter 2 focuses on the theoretical aspect of CNTFETs. First, we use a simple ballistic 1D transistor model to describe the ultimate performance of CNTFETs. Then, both analytical and numerical calculations are presented when considering the parasitics in CNTFETs. A few device design guidelines and predictions are brought up based on this theoretical model. Chapter 3 first compared and assessed the most state-of-the-art CNTFETs and two different approaches of growing nanotubes and making CNT devices are described. In Chapter 4 measurements of the fabricated devices are presented. A few conclusions are drawn by discussing the relation between device performance and the design. The CNTFETs are put into a DC-DC converter circuit and benchmarked in Chapter 5. Finally, conclusions are drawn in Chapter 6 and a few suggestions for future work are proposed.

Chapter 2

Theory and Modeling of CNTFETs

There have been significant interest in predicting the ballistic transport and ultimate performance of CNTFETs and systems [20][21][22]. In this work, we are going to model a top-gate CNTFET with its schematic drawn in Figure 2-1(a) as the small signal equivalent circuit model in Figure 2-1(b).

The main function of the nanotube is modeled as a voltage controlled current source I_{DS} that is determined by the gate-drain, gate-source voltages V_{GD} and V_{GS}. There are several capacitances to be considered. One is the intrinsic gate-to-drain and gate-to-source capacitance C_{GDi} and C_{GSi}. It consists of the quantum capacitance of the CNT and the capacitance between CNT and the gate electrode. C_{GDo} and C_{GSo} are parasitic capacitances between the electrodes. They strongly depend on fabrication process and lithography quality. So far, overlap and fringe capacitance is one of the limiting factors of CNTFET application. We have ignored the capacitances between G/D/S electrodes and the substrate because CNTFETs are three terminal devices (MOSFETs are four terminal devices). Since bulk SiO_2 doesn't play a role in fabrication we could make it very thick. We need to consider this capacitance again if CNTFETs are integrated with Si process that they are fabricated on the same substrate. The contact resistance R_D and R_S are large in CNTFETs due to the fact that electrons have to travel from three dimensional metal bulk to one dimensional nanotube and also that it is challenging in fabrication to make good metal-CNT contact. The resistance caused by dimension difference is 6.5kΩ [23].

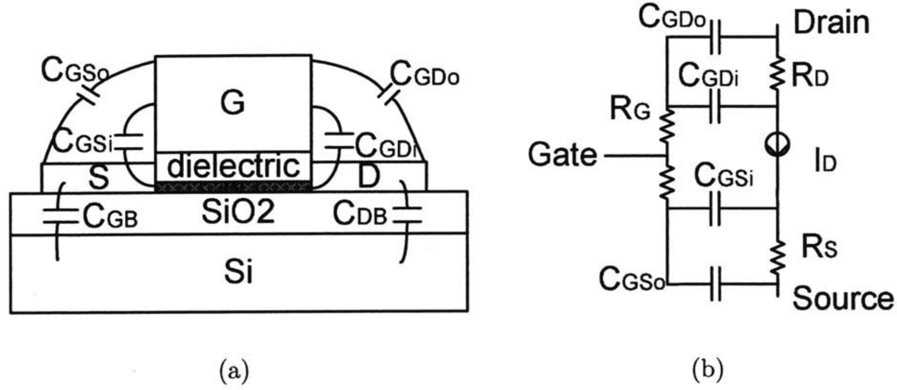


Figure 2-1: (a) Schematic of a top-gate CNTFET; (b) Equivalent small signal circuit model of the top-gate CNTFET.

2.1 CNT Electrostatics

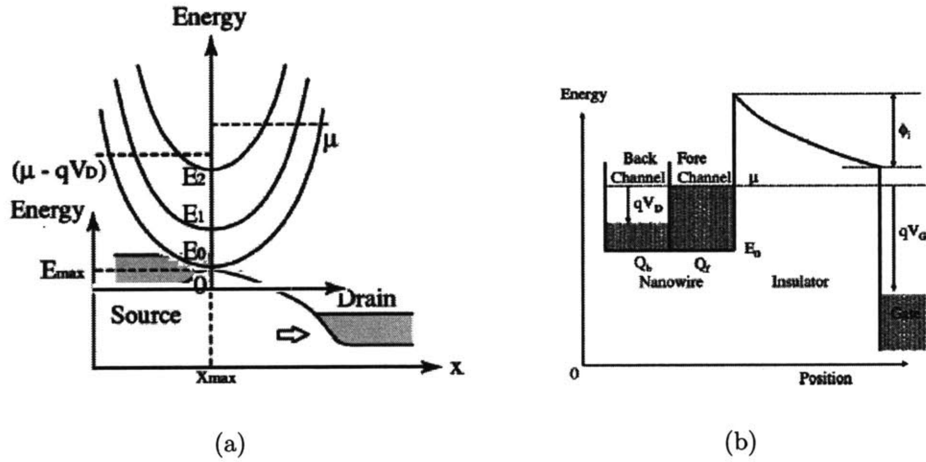


Figure 2-2: Electrostatics of nanotube [3]. (a) Schematic diagrams of the potential profile along the channel; (b) Schematic of potential profile across the device.

As illustrated in Figure 2-2(a), the gate voltage applied at the device induces the charges Q_{int} in the nanotube channel. As a result, it shifts the Fermi level of the nanotube μ due to the change of electron population in the subband. Thus

$$V_{GS} - V_{FB} = \frac{\mu - \mu_0}{q} + \frac{Q_{cnt}}{C_{G,ox}} \tag{2.1}$$

where V_{FB} is the flatband voltage and μ_0 the Fermi potential at the zero state(V_{GS}=0).

$C_{G,ox}$ is the gate capacitance between the gate electrode and the nanotube. Q_{cnt} can be calculated by neglecting charges due to holes and summing up electrons populated in the channel. It can be calculated as,

$$Q_{cnt} = q \sum_{i} \int_{E_{i,min}}^{E_{i,max}} D(E)(f_s(E,\mu) + f_d(E,\mu - qV_{DS}))dE \tag{2.2}$$

$D(E)$ is the 1D universal nanotube density of states which can be calculated by first principle [24]. For an ideal one dimensional device, carriers flow in both directions. Carriers propagating from source to drain are populated according to the source Fermi level while carriers going the opposite direction is populated according to the drain Fermi level. Figure 2-2(a) shows the Fermi level of the source and drain respectively.

2.2 Ballistic CNTFETs

To get a simple expression for drain current in CNTFET, we assume [3]:

- No Schottky barrier exists at contacts which means both source and drain electrodes can supply sufficient carriers to and sink carriers from the channel without reflection. *This is true for Ohmic contact transistors. And it can be realized by using metals with the right work function.*

- Backscattering or reflection due to the scatters or to the device structure in the course from source to drain is neglected. *Extensive studies show that under low bias, the mean free path(mfp) is observed to be ~1μm in CNTs and is thought to be nearly elastic and limited by acoustic phonon scattering. Under high bias, optical emission dominates, and short (~10nm) mfp results [25].*

- The bandgap is sufficiently large so that the charge due to holes in the valence band is neglected. *By choosing CNT with certain diameters, this can be achieved.*

Landauer-Büttiker equation [26] then gives,

$$I_D = \frac{q}{\hbar\pi} \sum_i \int_{E_i} [f(E,\mu) - f(E,\mu - qV_{DS})] dE_i \tag{2.3}$$

where E_i is the energy of the ith subband, μ the Fermi potential, V_{DS} the drain bias voltage and

$$f(E,\mu) = \frac{1}{1 + \exp(\frac{E-\mu}{k_B T})} \tag{2.4}$$

is the Fermi distribution function with Fermi level μ and k_B the Boltzmann constant.

Integrating Equation 2.3, we get,

$$I_D = \frac{qk_BT}{\pi\hbar} \sum_i \left(\ln \frac{1 + \exp[(\mu - E^+_{i,min})/k_BT]}{1 + \exp[(\mu - E^+_{i,min})/k_BT]} - \ln \frac{1 + \exp[(\mu - qV_{DS} - E^-_{i,min})/k_BT]}{1 + \exp[(\mu - qV_{DS} - E^-_{i,min})/k_BT]} \right) \tag{2.5}$$

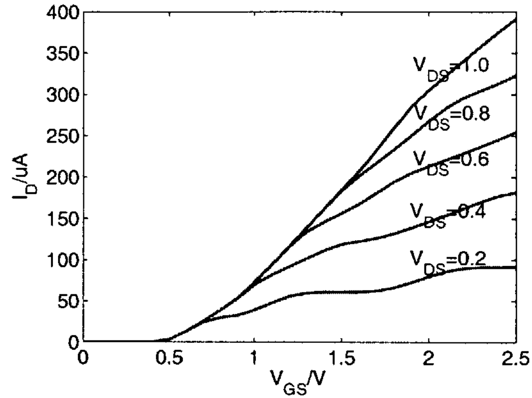
In order to calculate Equation 2.5, μ must be obtained by solving Equation 2.1 in the previous section and the E-k dispersion relation can be obtained from discussions in Chapter ??. Figure 2-3 evaluates the I-V characteristics of a (19,0) CNTFET with a diameter of 1.5nm. High-κ dielectric is assumed in this device structure.

It shows in the plot that one CNT can have a channel resistance of as low as 2.5kΩ plus 6.5kΩ intrinsic resistance with 1.13fF/μm gate capacitance when a 2.5V gate voltage is applied. This is much smaller than its CMOS counterpart. Although this model doesn't describe some of the phenomenon observed in experiments, it does provide insight into the ultimate performance limit of CNTFETs.

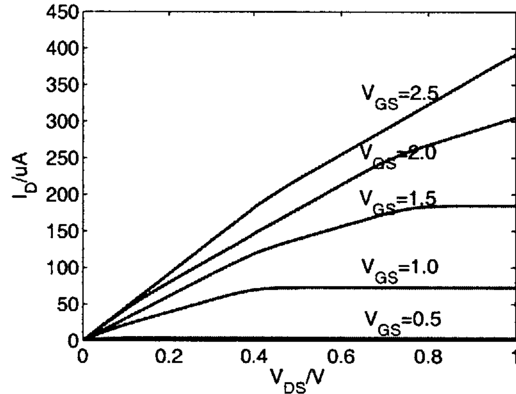
2.3 Schottky Barrier Behaviors

2.3.1 Ohmic versus Schottky Barrier CNTFETs

Experimental measurements suggest that most fabricated CNTFETs are not Ohmic contact but Schottky barrier CNTFETs. A Schottky barrier transistor is often caused by the formation of metal-semiconductor junctions. An illustration of different transistor band diagrams is shown in Figure 2-4. Take an n-type transistor for example,



(a)



(b)

Figure 2-3: I-V characteristics of an ideal Ohmic contact (19,0), D_{CNT}=1.5nm CNT-FET. We assume 2nm thick TiO_2 with its $\varepsilon = 40\varepsilon_o$ as gate dielectric. (a) I_D versus V_{GS}; (b) I_D versus V_{DS}.

for Ohmic contact CNTFET, the Fermi level of contact metal is above the conduction band of the CNT which means both contacts are capable of providing infinite number of electrons when the tube is conducting. When the two materials with different Fermi levels are connected, the Fermi potential automatically levels itself. Given a certain voltage applied at the gate, there is no barrier between the source and the channel so that electrons can pass through freely. On the other hand, electrons need to go through a barrier height of $(E_C - E_{MF})/q$ in a Schottky CNTFET. The current

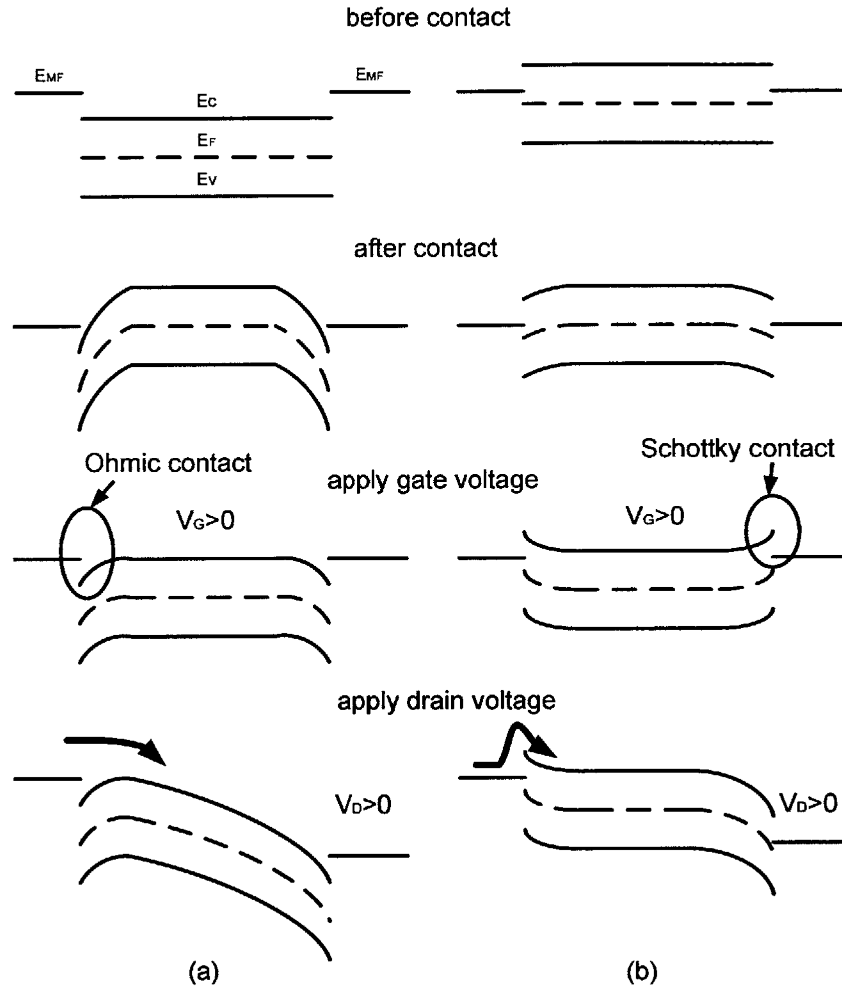


Figure 2-4: (a) Ohmic contact CNTFET formation; (b) Schottky barrier CNTFET formation.

is strongly dependent on the barrier height and width which are determined by the material characteristic and applied voltage.

2.3.2 Ambipolar Behavior

Fabricated CNTFETs shows ambipolar behavior, i.e., transistors conduct current even when turned "further" off, especially if a large voltage(normally 4mV) is applied at its source and drain. There are two causes for this. First the CNT bandbap is usually small and CNT Fermi level lies in the middle of the bandgap. This means both electrons and holes have large probability to travel through the channel. Second

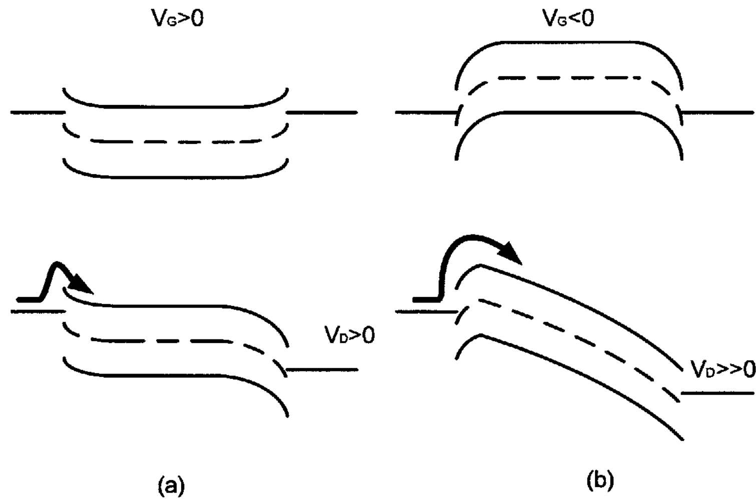


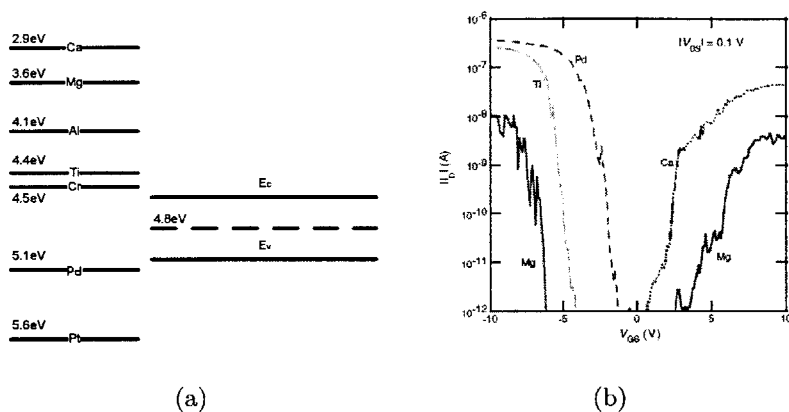
Figure 2-5: The illustration of ambipolar behavior of CNTFETs. (a) Device is biased on. Electrons pass through Schottky barrier; (b) Device is biased off. Large V_{DS} gives electrons enough energy and narrows the potential barrier. Electrons still inject into the channel.

the Fermi level of the metal contact isn't near enough to either one of the conduction or the valence band. This phenomenon can be explained by Figure 2-4 and Figure 2-5. When the gate voltage is reversely biased, it creates a big hurdle for electrons, yet it lowers the barrier for holes and causes a certain amount of holes to go through. Once a large V_{DS} is applied, it narrows the barrier and provides the holes with enough energy. The OFF current is thus comparable to the ON current. This effect due to large V_{DS} is more noticeable in short channel devices because voltage applied across the channel has stronger control over the electrostatics of the channel.

2.4 N-type and P-type CNTFETs

CNTs are assumed to have Fermi level lying in the middle of their bandgap so there is no distinction between n-type and p-type CNTs. The transistors show n-type and p-type behavior based on the different work functions of the contact metal. Theoretically, if the metal's Fermi level is near the CNT's conduction band, it is easier for electrons than holes to pass through and it is a n-CNTFET. Vice versa, if the metal Fermi level is near the valence band of the CNT, the FET is p-type. There is no real

measurement of the CNT work function. We use an estimation of 4.8eV [27] from that of the graphene's work function. A comparison of work functions of possible contacts metals is shown in Figure 2-6(a).



(a) (b)

Figure 2-6: (a) Work functions of different metals and CNT; (b) I_D-V_{GS} of fabricated devices with various contact metals [4].

The IV dependence on metal work function is demonstrated in experiments [4] where metals with large work function (Pd,Ti) form p-type devices and metal with small work function (Ca) forms n-type device. Devices with Mg contact (intermediate work function) shows strongest ambipolar behavior. However, in experiment also, Ti (ϕ_M=4.4eV) and Cr (ϕ_M=4.4eV) still form p-type CNTFET. The reason is that the presence of absorbed oxygen affects the height of Schottky barriers at the surface, such that the Fermi energy is pinned closer to the valence band maximum, allowing tunneling of holes, but not electrons. Modeling of the Schottky CNTFETs is complicated. [28] and [1] are some good references.

2.5 Gate Capacitance

2.5.1 Intrinsic Capacitance

Looking at the gate capacitance, a nanotube is grown on a thick silicon dioxide and then surrounded by a thin gate oxide. A metallic gate rests on the thin oxide, creating a coaxial capacitance structure with the nanotube at the center. To get an analytical

equation of the capacitance between the gate and CNT we simplify the gate electrode to be an infinite plane and the CNT to be a metal cylinder. The capacitance between the two can be expressed as,

$$C_{G,ox} = \frac{2\pi\varepsilon}{\ln\frac{\sqrt{d+t}+\sqrt{t}}{\sqrt{d+t}-\sqrt{t}}} \tag{2.6}$$

In reality, the gate is not infinite. We denote W_{ov} as the channel that is wider than the diameter of the CNT on both sides as illustrated in Fig.3-7(a). We use a multi-pole accelerated capacitance exaction software FASTCAP [29] developed at the Computational Prototyping Group at MIT to numerically calculate the capacitance between gate and the nanotube. Figure 3-7(b) shows the discretization scheme. Figure 3-7(c) plots capacitance versus W_{ov}. It shows that for the gate width that is exactly the same as the diameter of the nanotube (which is the most area-efficient case), the capacitance is only half of that calculated from Equation 2.6. The capacitance stays almost stable when W_{ov} reaches about 60nm (30 times the dielectric thickness). This happens to be around the minimum alignment error that could be achieved today. Thus we consider the analytical solution as an accurate value in later device evaluations. The plot also shows that further increasing in W_{ov} doesn't change the device performance except the fact the device size will increase. Using a coarse discretization (partition the cylinder in the circumferential direction into eight), we reach an error of 4%. This error goes down to 1.1% when we discretize twice as much in all three dimensions. But it will be time consuming in complex simulations that involve multiple tube devices.

Figure 2-8 shows the gate capacitance dependence on different geometry parameters of the FET structure. Here a channel length of 100nm is assumed. It can be seen that capacitance doesn't drop as drastically when dielectric thickness increases to above 100nm. This means an 100nm thick silicon dioxide basically has similar control of tube current as that of 250nm thick SiO_2. It also shows that tubes with larger diameter couple with gate more. Bigger tubes intrinsically has smaller Schottky barrier for carriers thus are capable of conducting larger current. Stronger coupling

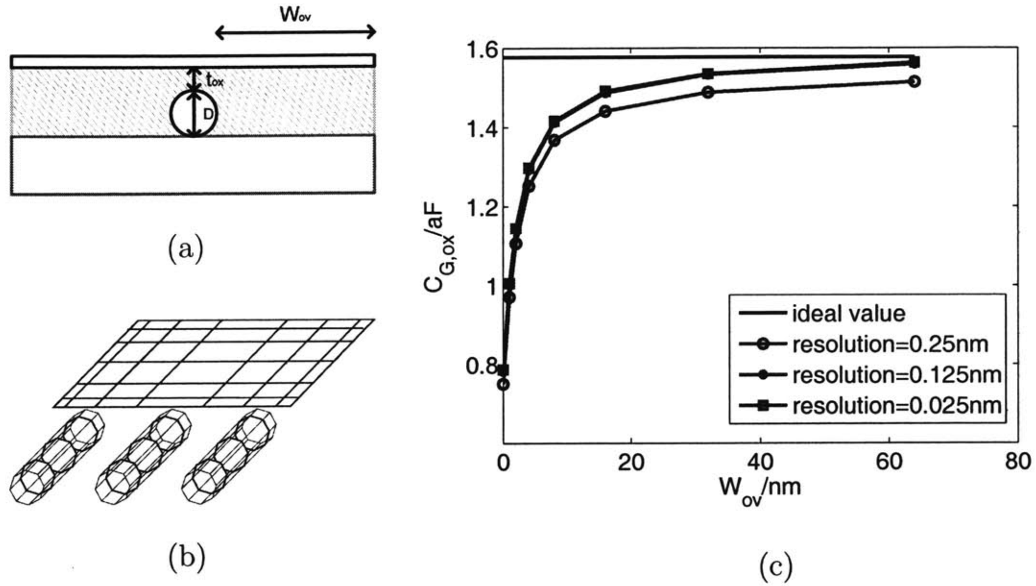


Figure 2-7: Numerical simulation of $C_{G,ox}$. (a) Cross section of top-gate CNTFET; (b) Discretizing metal electrode and CNT in 3D space; (c) Extracted capacitance values of different discretizing granulation as compared to analytical value.

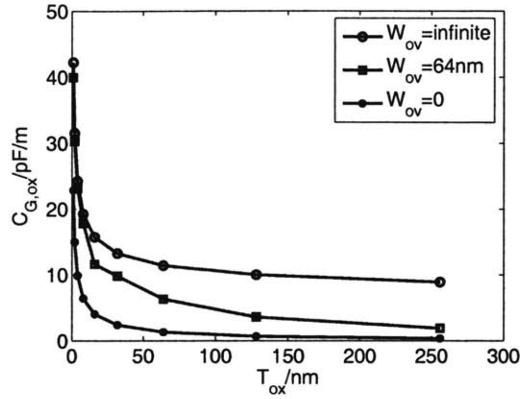
with gate electrode further increases their conductivity.

In a bottom-gate structure, the capacitance is simulated slightly different since the CNT is not surrounded by the same type of insulators anymore. Yet this turned out not to be a big difference.

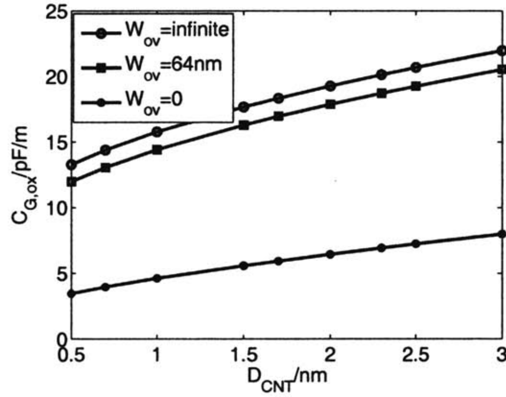
In a CNTFET, the gate capacitance is composed of two parts, $C_G^{-1} = C_{G,ox}^{-1} + C_{G,q}^{-1}$. $C_{G,ox}$ is the electrostatic gate capacitance that we have just calculated. $C_{G,q}$ is the quantum capacitance of the nanotube. For simple calculations, the unit length single tube $C_{G,q}/L$ can be treated as $4 \times 10^{-16}\mathrm{F}/\mu\mathrm{m}$ [30].

2.5.2 Parasitic Capacitance

Self-alignment is a revolutionary invention in the CMOS technology. It saves one step of photolithography and reduces overlap capacitances between gate and source/drain significantly. Self-alignment in CNTFET is possible [5], but challenging. Therefore most often there is overlap between gate and source/drain as illustrated in Figure 2-9(a), giving rise to parasitic capacitance. The state-of-the-art mis-alignment error using ebeam lithography is about 50nm. We will use this number for comparison



(a)



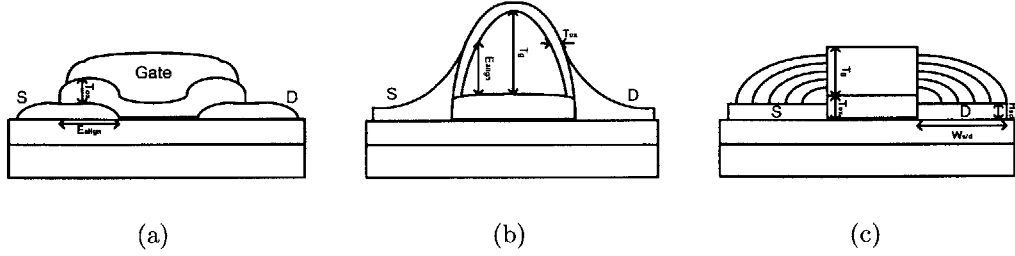
(b)

Figure 2-8: Gate capacitance dependence on device geometry. (a) $C_{G,ox}$ versus dielectric thickness; (b) $C_{G,ox}$ versus nanotube diameter.

later.

The authors of [5] demonstrate a way to self-align top-gate CNTFETs. In theory if materials can be deposited vertically, there won't be any overlap capacitance. In reality, however, because of the slope of the profile as illustrated in Figure 2-9(b), insulation of electrodes is realized by the natural oxidation layer of Al that is typically 4-8nm thick. Because this layer is thin and the dielectric constant of Al_2O_3 is higher than SiO_2, this capacitance is considerable.

Another issue related with parasitic capacitance of CNTFET is the fringing ca-



(a) (b) (c)

Figure 2-9: (a) Top-gate CNTFET with overlap capacitance; (b) Device cross section presented in [5]; (c) Fringing capacitance in perfectly aligned device.

pacitance between gate and source/drain. Unlike MOSFETs, the S/D electrodes of CNTFETs also serve as the source and drain contacts. This brings the distance between these metal by a considerable amount. [31] gives an analytical expression

$$C_{fr} = \frac{2\varepsilon W}{\pi} \ln \left[\frac{T_{g,s/d} + \eta T_g + \sqrt{L_{un}^2 + (\eta T_g)^2 + 2T_{g,s/d}\eta T_g}}{L_{un} + T_{g,s/d}} \right]$$

$$+ \frac{k\varepsilon W}{\pi} \ln \frac{\pi W}{\sqrt{L_{un}^2 + T_{g,s/d}^2}} e^{-\left|\frac{L_{un} - T_{g,s/d}}{L_{un} + T_{g,s/d}}\right|} \tag{2.7}$$

for fringing capacitance of structure shown in Figure 2-9(c). Where $\eta = \exp\left[\left(L_{sd} + L_{un} - \sqrt{L_{un}^2 + T_g^2 + 2T_{g,s/d}T_g}\right)/\tau L_{sd}\right]$ and $T_{g,s/d} = T_{ox} - H_{sd}$. k and τ are constants and [31] suggests values of 0.1 and 0.37 respectively. L_{un} in our case is 0.

Table 3.1 lists the parasitic capacitances of different device structures discussed above and compares them to the 32nm(L_{ch}) CMOS technology predicted by Berkeley predictive technology model [32].

For a device with 70nm channel, this parasitic capacitance is about 3 times the intrinsic gate capacitance. And the ratio will increase with further scaled devices.

Device	Parasitic	L_{ch}	T_{ox}	E_{align}	$W_{s/d}$	T_g	$C/width$
Fig2-9(a)	overlap	-	8nm	50nm	-	-	430μF/μm
Fig2-9(b)	overlap	-	6nm	25nm	-	50nm	660μF/μm
Fig2-9(c)	fringing	-	8nm	-	200nm	50nm	108μF/μm
CMOS	overlap	32nm	1.65nm	-	-	-	170μF/μm

Table 2.1: Comparison of parasitic capacitance of different device structures.

2.6 Multi-tube Devices

2.6.1 CNT Network Devices

The maximum current capacity of one single SCNT is 25μA [33]. In order to make a device that could conduct large amount of current, people have been trying to use multiple tubes. If hundreds of nanotubes could be put in parallel, they only occupy small areas and generate small capacitance.

However since making parallel aligned, dense CNT arrays is quite challenging, one alternative solution is to randomly put down nanotube network on substrate and deposit metal pads to obtain multi-tube devices. The schematic of this device is shown in Figure 2-10(a).

This method will reduce the current considerably. A MATLAB script is written to compare the random network device with the ideal case. We assume the nanotube lengths range between 1nm and 5nm which is observed from AFM image. We choose a typical 50kΩ as the resistance of one nanotube. The density of nantoube is determined by the concentration of catalyst particles. We assume there is one catalyst particle in every 0.1$\times$0.1μm^2 and 0.5$\times$0.5μm^2 square which is also based on AFM images. The channel length is varied from 100nm to 5μm in our comparison.

Figure 2-11(a) shows that only the curve of 100 tube/square, aligned nanotube has a conductance above 1S and is better than a W=100nm transistor in 65nm technology node. The fact that the nanotubes are randomly distributed decreases

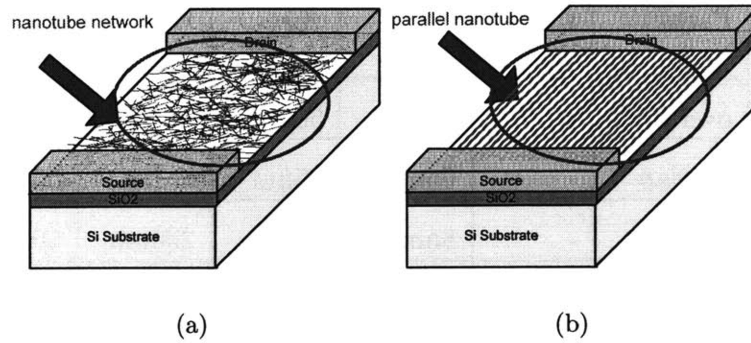


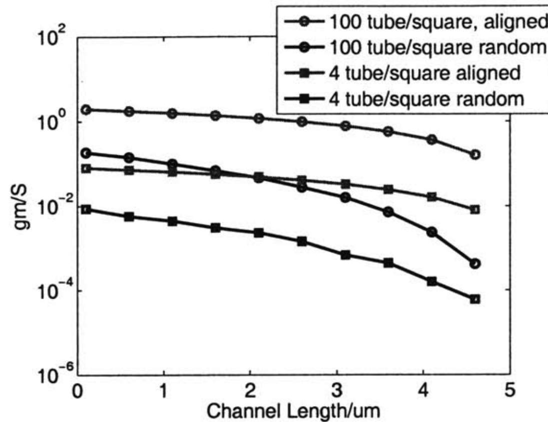
Figure 2-10: (a) Random network of nanotubes between source and drain; (b) Aligned nanotubes between source and drain.

the conductance for more than a factor of 10 even when the channel length is only 100nm. It goes down by another order of magnitude when the channel length reaches 5μm.

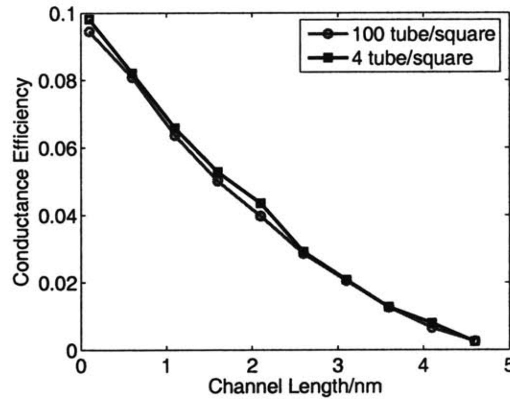
2.6.2 Devices with Parallel Aligned CNTs

Although carbon nanotubes in parallel with small pitches are still hard to fabricate, it is useful for circuit designers to get the intuition of how the electrostatic will change once multiple tubes are put together and screening effect begins to take place.

Again we use FASTCAP to perform the numerical calculation. We define "pitch" as the spacing between two nanotubes(edge to edge). We also assume a 64nm misalignment error in our structure as mentioned in Section 2.5 which is for fabrication concerns. Figure 2-12(a) shows how gate capacitance depends on the pitches. As the spacing between CNTs increases, the screening effect between them reduces and there's more arc coupling with the gate so the capacitance increases more slowly. It is interesting to note from Figure 2-12(b) that there is a maximum capacitance/width value occurring at around 10nm for CNTs with 2nm diameter. This is different from MOSFET for which the $C_{G,ox}/W$ is nearly constant regardless of W.



(a)



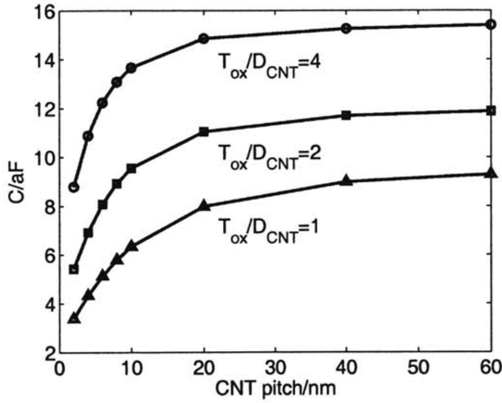
(b)

Figure 2-11: Current capacity degradation from CNT randomness. square: 1μm by 1μm area.(a) Conductance versus channel length; (b) Conductance efficiency versus channel length.

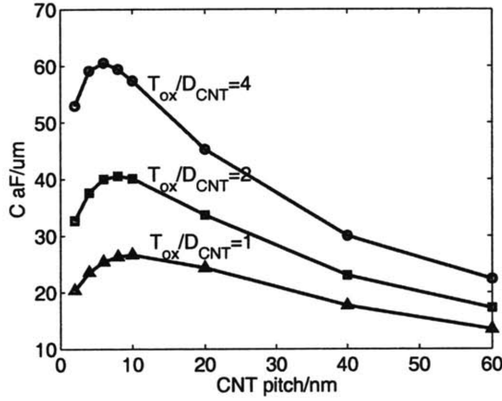
2.6.3 Devices with Vertically Stacked CNTs

Another question of interest is: Can we stack nanotubes on top of each other instead of putting them in parallel as illustrated in Figure 2-13.

To answer this question, we need to understand that the nanotube is a discrete material. For example, as we mentioned before, in order to increase current, we increase the number of nanotubes under a shared metallic gate instead of increasing the device width as is done for Si-based devices. In a CMOS device, when the gate



(a)



(b)

Figure 2-12: (a) The gate-to-nanotube capacitance versus pitch; (b) The unit width gate-to-nanotube capacitance versus pitch.

voltage increases, electrons from the substrate are attracted towards to the interface with the dielectric material, forming a thin layer known as the inversion layer, as shown in Figure 2-14(b). The number of electrons increases exponentially with the gate voltage and the thickness of the inversion layer reaches a maximum value. That may not happen in nanotubes. The electrical lines start from the gate and ends at the source and drain which provide the mobile carriers. The nanotubes only serve as channels being turned on and off between the source and drain. The difference of the

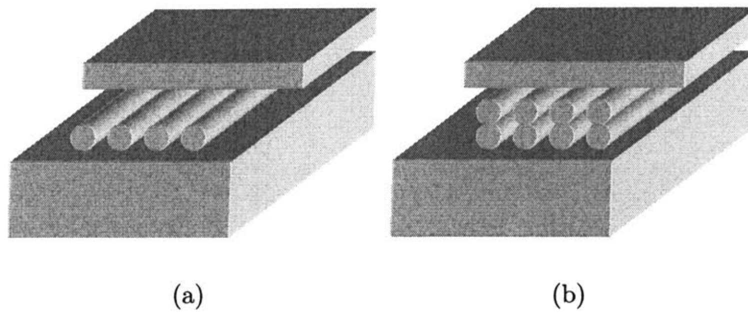

(a) (b)

Figure 2-13: CNTFETs of vertically stacked CNTs. (a) parallel nanotubes; (b) nanotubes stack on top of each other.

metal, silicon and stacked-nanotube device cross section is compared in Figure 2-14.

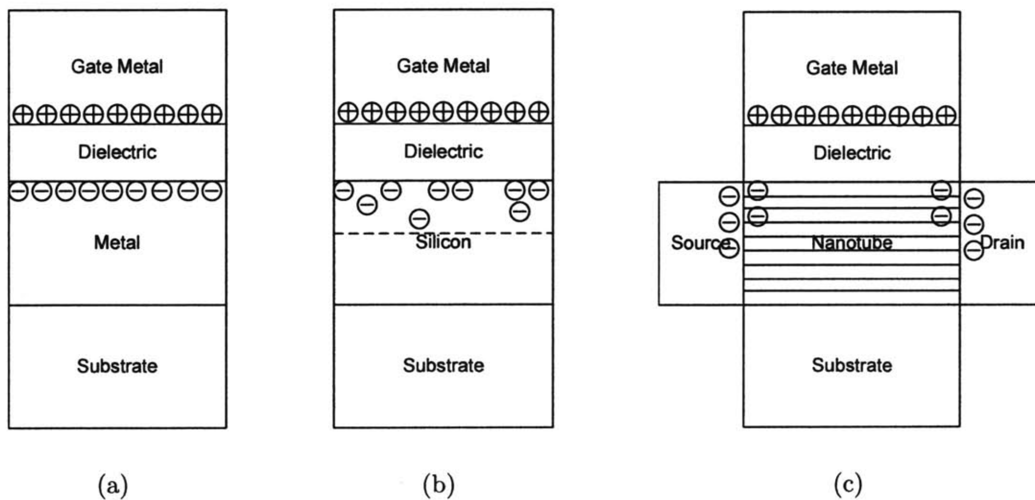


Figure 2-14: Electrostatics of different materials as channel. (a) metal; (b) silicon; (c) CNT.

When there is a high carrier concentration at one end of the device, and one CNT is incapable of transferring all of them to the other terminal, a second CNT will conduct even though it's not under the direct control of the gate. Therefore, stacking CNTs on top of each other might be an option to increase CNTFETs' current capacity without increasing the device size.

Chapter 3

CNTFET Device Structure and Fabrication Processes

The first carbon nanotube field effect transistor using semiconducting CNTs was reported in [34] and [35] as early as in 1998. Ever since then, remarkable progress has been made to improve the performance of CNTFETs by approaches such as: reducing the gate oxide thickness, adopting high-κ dielectrics for the gate oxide, using electrolyte as the gate, reducing contact resistance by choosing proper contact metals and doing post processing treatments. These techniques have significantly improved the performances of CNTFETs that compare favorably to the state-of-the-art MOSFETs. In the first section of this chapter, we will compare and assess the state-of-the-art CNTFETs in literature.

One disadvantage with the reported devices is that since there's only one tube conducting, the on current is small. For power applications which require delivering ~100mA current, CNTFETs with multiple tubes need to be fabricated.

We are trying two approaches to fabricate CNTFETs with large current capacity. One way requires growing densely distributed nanotubes on chip and the devices are defined when metal contacts are deposited as source and drain at relatively arbitrary locations. The number of tubes connecting source and drain obeys statistics and are roughly proportional to the width of the device when the device is large enough. The maximum current is proportional to the number of tubes between two metal

contacts. A metallic nanotube removal process is required for this type of device and is the major challenge.

The second method involves growing one long straight nanotube and depositing a cross-digitized structure as source and drain to make use of many different segments of the same long tube. This is equivalent to putting hundreds of nanotubes in parallel between source and drain. Although this method creates larger parasitic capacitances and resistances, this method overcomes the problem of low I_{ON}/I_{OFF} ratio that is caused by the presence of metallic tubes. This method requires "high quality" nanonube growth. By 'high quality' we mean single-wall, long, straight, semiconducting single nanotube with a reasonable diameter. Fabrication process also needs to be carefully designed to locate a good segment of nanotube.

3.1 Comparison of State-of-the-Art CNTFETs

Table 3.1 lists the key performance and fabrication parameters of the most state-of-the-art CNTFET devices.

Refs	[6]	[7]	[10]	[9]	[5]	[8]
Dielectric	SiO_2	SiO_2	ZrO_2	HfO_2	HfO_2	TiO_2
Contact Metal	Pd	-	-	Pd	Pd	Pd
Channel Length	600nm	18nm	3μm	2μm	50nm	1.2μm
Tube Diameter	1.8nm	1.1nm	-	2.3nm	1.7nm	1.3nm
Oxide Thickness	10nm	12nm	8nm	8nm	8nm	18nm
I_{ON}/I_{OFF}	10^5	10^6	10^3	10^3	10^3	10^4
R_{ON}/kΩ	60	30	200	65	30	200

Table 3.1: Comparison of key performances of state-of-the-art CNTFETs.

[6] and [7] are two most recent back-gate (as illustrated in Figure 3-1) CNTFETs. In [6], Pd contacts are used to minimize the Schottky barrier height for hole carriers at the metal/nanotube contacts. The nanotube is 1.8nm (calculated from distribution)

wide in diameter and the source and the drain are separated by 600nm. A very thin layer of silicon dioxide (10nm) is used as bottom gate dielectric. Thin dielectric is effective in controlling the current yet it is very prone to gate leakage because in bottom-gate structure the gate area is much larger than that in the top-gate structure. The fabricated device achieves I_{ON}/I_{OFF} ratio $\geq 10^5$ under 0.5V bias and 55kΩ turn-on resistance.

A common way to pattern source/drain contact is to use lithography (ebeam or photo), deposit metal and do lift-off. [7] uses a different type of resist hydrogensilsequioxane(HSQ) to achieve ultra short (18nm) channel length. This work also uses Pd as contact metal and grows nanotube of diameter as small as 1.1nm in order to increase the CNT bandgap and thus to increase I_{ON}/I_{OFF} ratio. The reported I_{ON}/I_{OFF} ratio is 5.5$\times 10^5$ at 0.4V bias and the ON resistance is 40kΩ. This work adopts very thin(12nm) back gate dielectric layer as well.

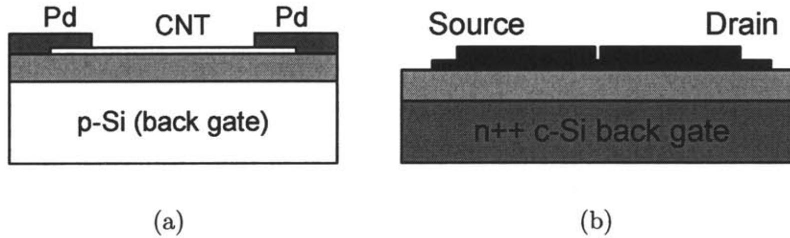


Figure 3-1: Bottom-gate CNTFET structure. (a) Ref [6]; (b) Ref [7].

Recent top-gate CNTFET structures are shown in Figure 3-2. In 2002, Javey et al. [10] for the first time used high-κ insulator zirconium oxide (κ $\sim$25) thin film ($\sim$8nm) as gate dielectrics by atomic-layer deposition (ALD). High-κ material afford high capacitance without relying on ultra-thin film thickness, thus allowing for efficient charge injection into transistor channels and meanwhile reducing direct tunneling leakage currents. With a $\sim$ 3μm spacing between source and drain, this device achieves more than 10^3 I_{ON}/I_{OFF} ratio even under 1V bias and 10^4 under 0.1V. The ON resistance is 200kΩ. Later in 2003, Javey et al. [9] improved the same type of device by changing the high-κ material into HfO_2 and the metal contact into Pd. Device channel length is reduced to 2μm. The device has an I_{ON}/I_{OFF} ratio of

10^3 under 0.3V bias voltage and an ON resistance of 65kΩ.

A novel self-aligning technique was proposed by Javey et al. [5] again in 2004. In this work, 8nm HfO_2 and 50nm Al gate electrodes were first deposited by ALD on top of SWCNT. This step takes advantage of native Al_2O_3 on the Al metal gate. Very thin Pd metal (~7nm) is then deposited in the region and is separated by the $HfO_2/Al/Al_2O_3$ stack, forming the S and D electrode. The device structure is shown in Figure 3-2(a). By this means, no high quality alignment is required. However, as we calculated in Chapter 2 the parasitic capacitance related to this structure is no smaller than a CNTFET without self-aligning. Also naturally formed oxide are not reliable to prevent leakage, which limits this method being used in mass production. The performance of this device, however, is the highest reported so far. It achieves I_{ON}/I_{OFF} ratio of 10^3 under 0.3V bias and an on resistance is 30kΩ.

The latest work is done by Yang et al. [8]. The device employs Pd as electrodes for Ohmic contact and high-κ material TiO_2 as gate dielectric. Device channel length is 1.2μm. The interesting feature of this device is that the gate structure doesn't cover the whole channel, as shown in Figure 3-2(b). This means gate control over exposed nanotube is relatively weak. This device offers I_{ON}/I_{OFF} ratio of 10^4 under 0.2V bias and the ON resistance of 200kΩ.

Since these devices are fabricated with different processes and conditions, it is hard to compare because a lot of uncertainties exist. Yet it can be concluded that in order to get good performance, metal with high work function is very preferred. All devices use Pd as contacts. It seems CNT with small diameter gives better trade-off between conductance and I_{ON}/I_{OFF} ratio, though theoretically, larger nanotube would be more conductive. This is probably because parasitic resistance overwhelms the influence of the tube diameter. For the same reason, device channel length does not make a big difference either. This leads us to try to use devices with longer channel to reduce the fabrication cost while maintaining the performance.

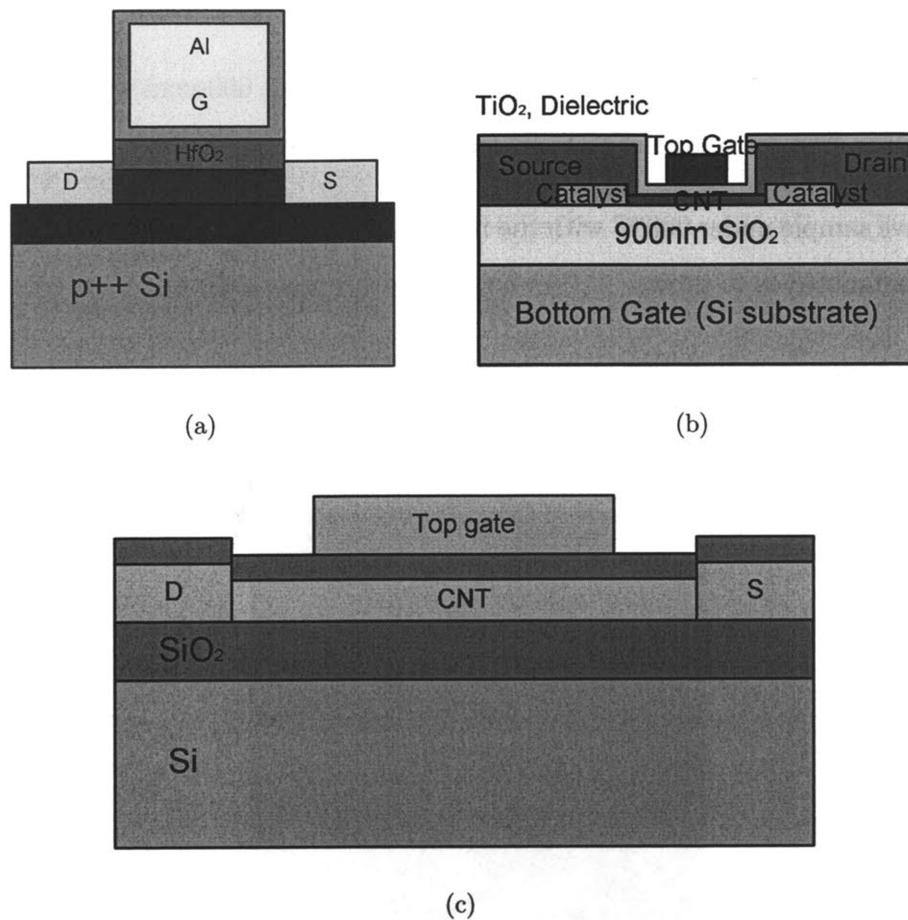


Figure 3-2: Top-gate CNTFET structure. (a) Ref[5]; (b) Ref[8]; (c) Ref[9], [10].

3.2 Nanotube Film Devices

3.2.1 Nanotube growth

The recipe to grow dense nanotube film is described as following:

(1) Put a drop of catalyst ferritin (Sigma Aldrich, type I from. 0.66vol. in H_2O) on the substrate. Wait for 5min to allow the particles to attach to the substrate and then rinse with water.

(2) Anneal the sample in air under 700°C for 5min to burn away protein covering the iron content.

(3) Heat the sample up to 900°C with the flow of 440sccm hydrogen and 600sccm

argon.

(4) Leave sample under 900°C in 440sccm hydrogen and 600sccm argon for 5min to reduce iron oxide to the metallic iron state.

(5) Leave sample under 900°C with the flow of 500sccm argon and 1000sccm methane for nanotubes to grow.

(6) Leave sample with 440sccm hydrogen and 600sccm argon to cool down.

Figure 3-3 is an AFM image of the grown nanotubes.

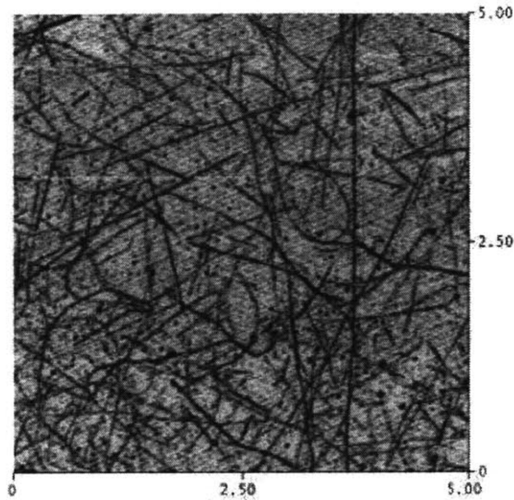


Figure 3-3: AFM image of densely grown nanotubes.

3.2.2 Device Fabrication

We use the following processes to fabricate CNTFETs.

(1) Thermally grow 250nm silicon dioxide on silicon substrate. Grow nanotubes based on method described in Section 3.2.1. Figure 3-4 is the cross section of the CNTs on the substrate.

(2) Photo lithography, deposition and lift-off are used to generate metal electrodes. Patterns are generally of 300μm width and 2μm channel length. 5nm Ti and

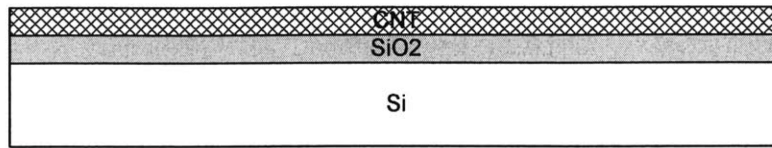


Figure 3-4: Fabrication step (1) - CNT growth.

5nm Au are used as contact materials. Ti is used for its large work function, good adherence to silicon dioxide and good welding property with CNT. Since Ti oxidizes easily in air which introduces large resistance, Au is needed as the protection layer. To avoid non-conformability when growing SiO_2 as top gate dielectrics, metals are deposited as thin as possible. This step is illustrated in Figure 3-5.

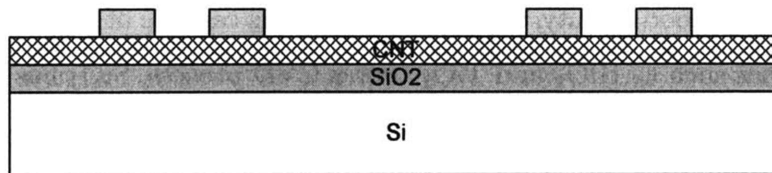


Figure 3-5: Fabrication step (2) - source/drain contact deposition.

(3) Use aligned photo lithography, deposit and lift-off for large metal pads. Since the metal thickness in the previous step is too thin for probing and wire bonding, this step is required. Pads size is 200μm$\times$200μm and Ti and Au are used again. For a simple bottom gate structure, step (2) and (3) could be combined into one. The device cross section is shown in Figure 3-6.

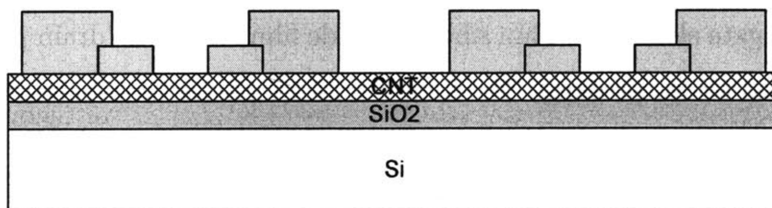


Figure 3-6: Fabrication step (3) - source/drain pads deposition.

(4) Photo lithography and O_2 plasma etching. Since the position of the grown CNTs is not controlled, network of CNTs shorts out pads to pads and hence devices to devices. Thus O_2 plasma etching is required to isolate each device and to prevent malfunction. This step is illustrated in Figure 3-7.

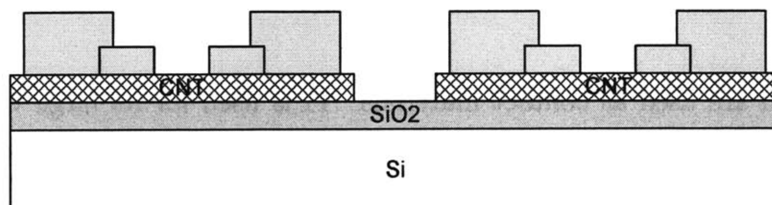


Figure 3-7: Fabrication step (4) - O_2 plasma etching of CNTs.

(5) SiO_2 CVD or atomic layer deposition (ALD) of high-κ material. To get gate dielectric of good quality, CVD is used. ALD is capable of growing dense highκ dielectrics such as HfO_2 and TiO_2. For a CVD process, SiO_2 has to be at least 10nm thick to guarantee insulation and conformability. The cross section of the device is shown in Figure 3-8.

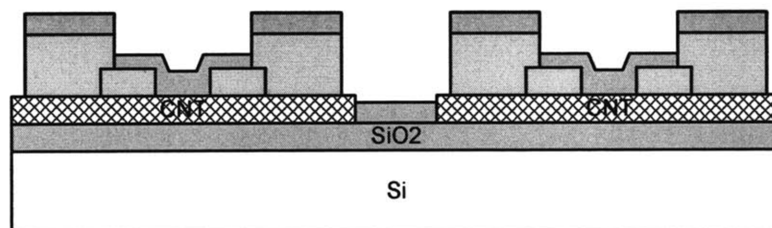


Figure 3-8: Fabrication step (5) - gate dielectric deposition.

(6) Photo lithography and gate electrode deposition. 5nm Ti and 45nm Au are again used as gate electrode. Thin silicon dioxide film on source/drain pads need to be scratched off for probing. The final CNTFET device cross section is illustrated in Figure 3-9.

Figure 3-10 shows the 1cm×1cm die photo mask for the process. Devices of difference lengths and widths and of difference pad sizes are designed for performance comparison.

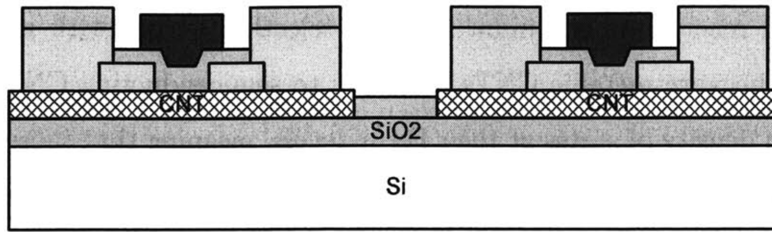


Figure 3-9: Fabrication step (6) - gate electrode and pad deposition.

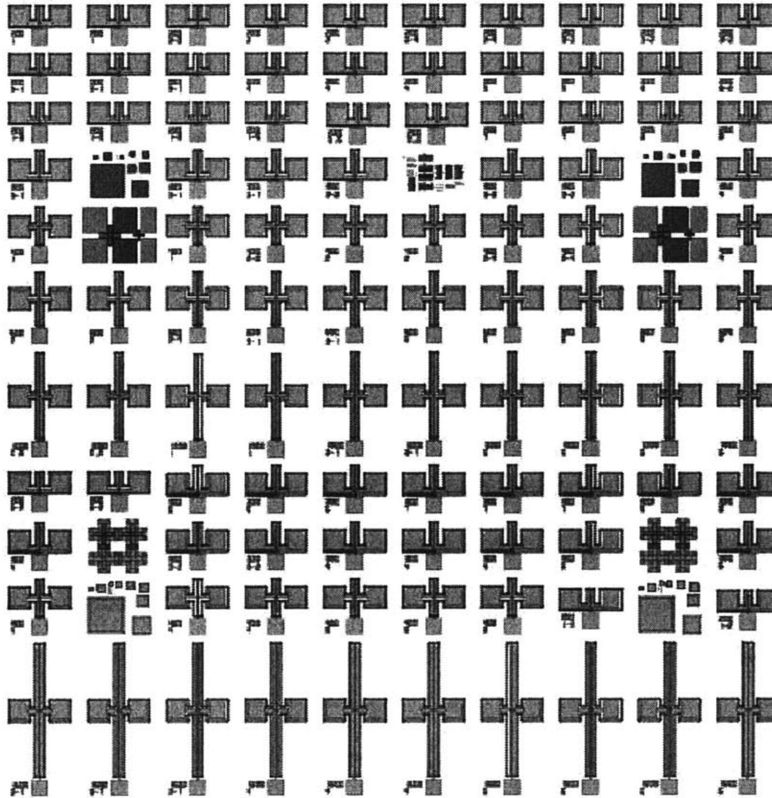


Figure 3-10: Photo mask of 1cm×1cm die.

3.2.3 Selective Removal of Metallic Nanotubes

Current literature provides three ways to eliminate metallic tubes from network nanotube film devices and are described as follows:

(1) Electrical burning. Applying a large voltage across source and drain while simultaneously gating the film to deplete the semiconductors of carriers results in the selective breakdown of the metallic CNTs [36].

(2) Chemical reaction. Diazonium reagents selectively react with metallic CNTs. This is because metallic CNTs, contrary to semiconducting CNTs, have finite electron density of states at their Fermi levels, meaning that there are electrons available to stabilize the charge-transfer complex presumably formed by the diazonium reagent at the nanotube surface, which is suggested to facilitate the reaction. On the other hand, the absence of the electrons near the Fermi level makes semiconducting nanotubes less likely to react with the diazonium reagent [37].

(3) Chemical etching. A gas-phase plasma hydrocarbonation reaction selectively etches and gasifies metallic nanotubes [38].

In our experiment, however, since the CNT film is thick, a noticeable number of semiconducting CNTs are possibly damaged in the process to remove the metallic CNTs. When a high voltage is applied at the two terminals of the device, large current generates enough heat so that CNTs burn with oxygen in the air. The heat may also cause nearby semiconducting CNTs to burn as well. However, if the amount of energy is controlled just that only turned on CNTs are burned, the number of semiconducting CNTs sacrificed will be reduced and thus it increases the I_{ON}/I_{OFF} ratio as desired.

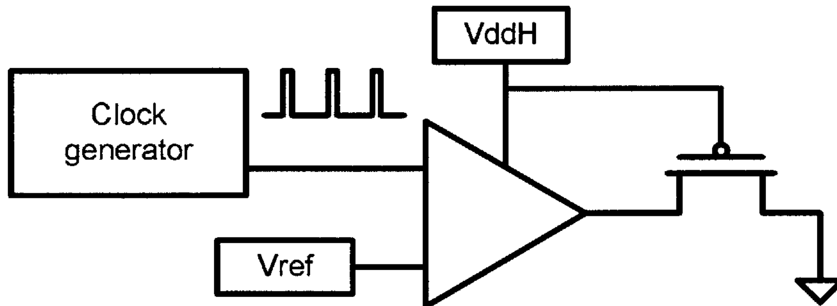


Figure 3-11: Electrical removal of metallic CNTs by applying high voltage pulses.

Figure 3-11 shows the schematic to burn away metallic nanotubes. It consists of a clock generator to generate narrow voltage pulses and a high voltage comparator to level shift the output to VddH that is applied across the CNTFET.

3.3 Electrically Parallel Nanotube Array Devices

3.3.1 Nanotube growth

The recipe we adopt for long nanotube growth is as follows:

(1) Make catalyst by dissolving 3mg of $FeCl_3$ into 1mL of water. Mix solution with hexane as 1:3. Add 30mg of HMDS into emulsion to help materials blend well.

(2) Place catalyst bottle on a magnetic plate for 20min to stir. Dip one edge of the chip into the catalyst bottle. Wait for a second and then blow dry the chip with nitrogen gun.

(3) Place the chip into a small quartz tube inside a quartz tube to make sure the gas flow is smooth. Start with 440sccm of hydrogen and 600sccm of argon. Heat up to 900^oC to burn away the organic residue, leaving behind the Fe compound nanoparticles as catalyst.

(4) Enter conditioning phase by leaving samples under 900^oC in argon(600sccm) and hydrogen(440sccm) environment for 12min.

(5) Turn on the reaction gas, 1000sccm methane with the presence of 440sccm hydrogen for CNT growth.

(6) Turn off reaction gas. Turn off inert gas after sample is cooled down.

Figure 3-12 is a SEM image of grown nanotubes.

Normally, single wall CNTs are difficult to grow. But this method is rather reliable and has almost a 100% yield. There're usually 10 straight long tubes on a 1cm$\times$1cm chip with their lengths ranging between 1mm and 5mm. There're two problems with this growing method though. One is that it is not guaranteed to grow one isolated CNT instead of CNT bundles. It is difficult to differentiate the two cases by SEM imaging. Raman analysis is complicated and yet not accurate. One way to study the distribution is by AFM imaging and measuring and curve fitting the diameter of the CNTs.

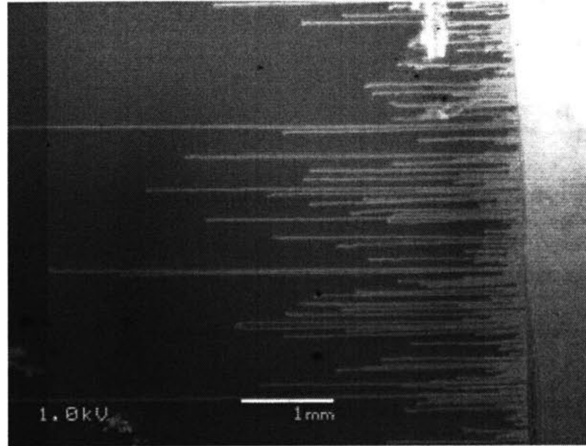


Figure 3-12: SEM image of long straight nanotubes.

Figure 3-13 shows the measured diameter distribution(dots) by AFM. Assuming a single CNT has a diameter of D, for a bundle of n CNTs the appeared diameter should be $h = D(1 + \frac{\sqrt{3}}{2}(n-1))$. Curves D1, D2, D3 and D4 represent bundles of 1, 2, 3 and 4 CNTs respectively. By summing up the number of CNTs(solid line) and comparing it with measured data(dots), we obtain that the fitted mean diameter of one nanotube is 1.45nm with a variation of ± 0.6nm. The ratio between the number of D1, D2, D3 and D4 can be read from the figure and is 12.4:4.6:2.4:1. One single tube is most desirable for our application and it has a portion slightly above half of the grown CNTs.

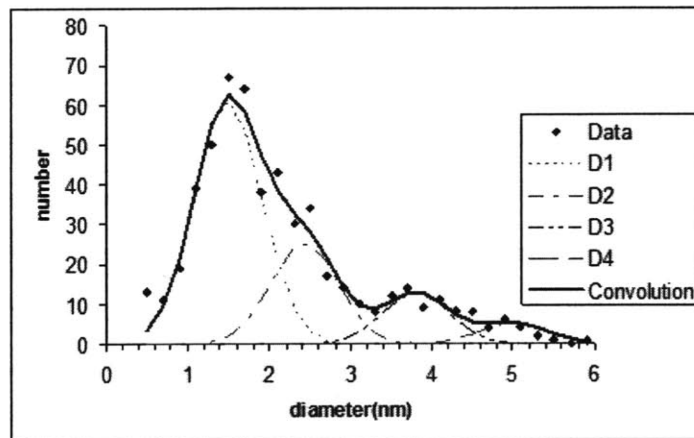


Figure 3-13: Measured diameter distribution by AFM. *In Courtesy to Mario Hofmann*

Another issue with this method is the observed non-consistency in behavior with even the same CNT. It is possible that during the process of CNT growth unstable condition or undesired particles cause defects in CNT and changes its chirality. It may even turn a semiconducting CNT into a metallic one. To avoid this happening, proper cleaning of the chip before and a careful control of gas flow during the process is required. In our experiment, we also try to put the devices as near to each other as possible to eliminate the possibility of changed CNT chirality.

3.3.2 Device Fabrication

(1) Photo lithography. Location of CNTs is one of the challenges. If the position of the CNT can be pinpointed, the width of the device can be made sufficiently small, which reduces the parasitic capacitance. Since we use SEM for alignment, at least 3 points are required. 5 is chosen and 2 of them are backup points. These location markers are located at the corner of the chip. During aligning, one only need to image at the edge of the chip so the patterns in the middle will not be accidentally exposed. Also, alignment markers that are far away from each other help to increase the accuracy of the location. In addition, alignment markers for photo lithography are needed for later steps of etching. Markers on the left side of the mask help to define catalyst region for nanotube growth. The whole photo mask is shown in Figure 3-14(a).

(2) CNT growth. The detailed description of growing recipe is in the previous subsection. It is important to make sure the direction of the nanotube growth is the same as the alignment markers since our SEM machine can only tolerate an error of ± 6 degree. To make the gas flow as smooth as possible so that the nanotubes can grow straight, not only a double quartz configuration is used, dummy devices are also placed in front of the sample to further confine the flow of the gas. The whole growth setup is shown in Figure 3-15. The grown nanotubes are illustrated in Figure 3-14(b)

(3) Locating CNT. Both alignment markers' and CNT segments' coordinates are

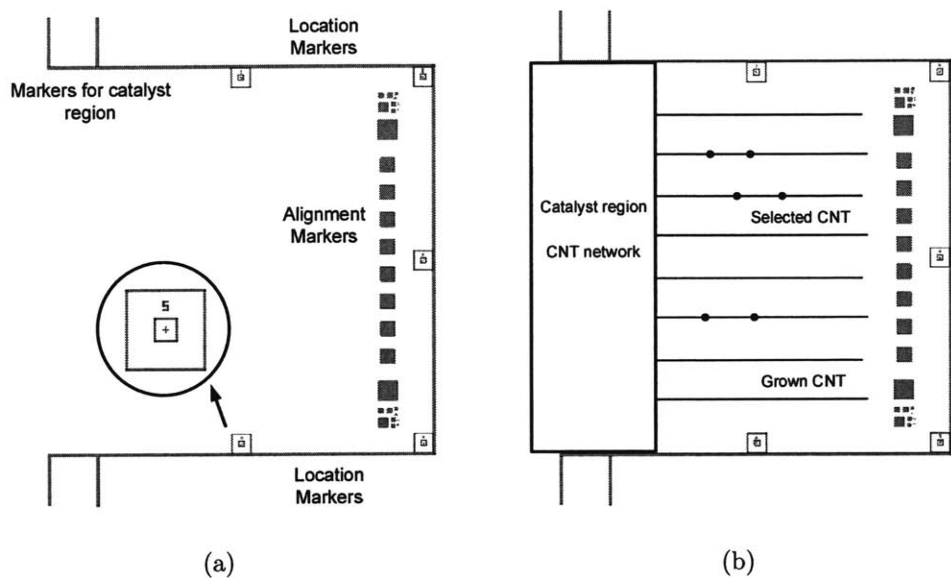


Figure 3-14: (a) Photo lithography step mask with various alignment markers; (b) Nanotube growth region and orientation.

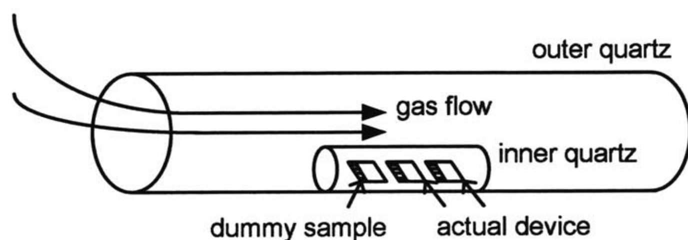


Figure 3-15: CNT growth environment setup.

recorded using an ebeam lithograhpy machine. CNT dimension is mostly below the resolution of current SEM machines. But since CNTs are conducting, they can be seen under low acceleration voltages when sitting on top of insulating materials (such as SiO_2) due to contrast. On the one hand, the voltage can't be too low so that error in focusing will cause misalignment. On the other hand, high accelerating voltage might damage the nanotube. We choose 3kV to meet both requires. Because of the error in the mis-orientation of CNTs and that the chip can be placed at different locations when put into the machine, a mapping algorithm is needed when designing the mask to compensate these errors. Here, we only need to deal with shifts and rotations so a two-points

mapping algorithm is enough.

(4) Patterning cross-digitized source/drain structure(shown in Figure 3-16(b)). Making Contacts to CNT is one of the most crucial steps in CNTFET fabrication. In general, Palladium has large work function and good welding property with CNTs and thus made ideal as Ohmic contact materials in CNTFETs. However, Pd as a noble metal does not stick to SiO_2 well and therefore its patterns are easily damaged on silicon dioxide. Pads made of Pd are delicate and not suitable for wirebonding or probing. In order to make the processes compatible, we use Pd only to form the small and thin patterns. A 300nm PMMA is used and only 10nm Pd is deposited. One advantage about thin metal layer is very fine features can be written (<100nm). Also it makes lift-off much easier. In order to compare device geometry(W, L)'s influence on device property, multiple patterns of different parameters are written on the same nanotube at the same time.

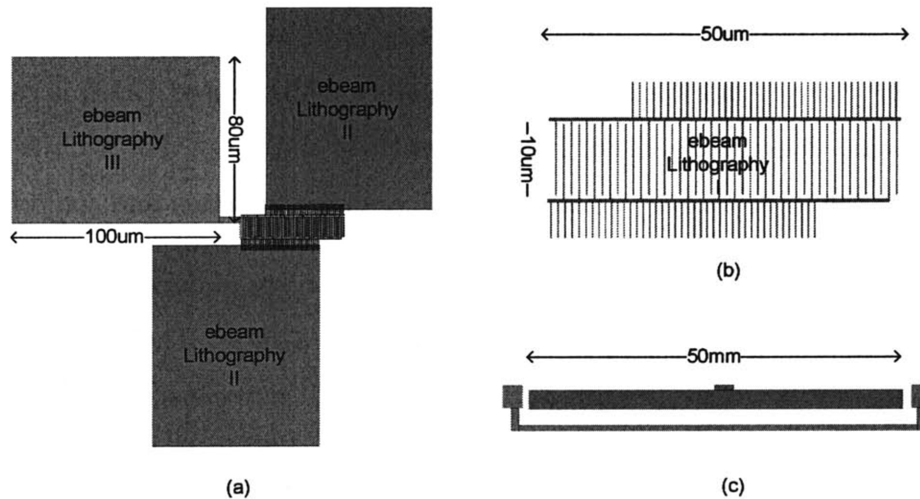


Figure 3-16: (a) A complete top gate CNTFET device pattern; (b) Zoom in of the source/drain cross digitized pattern with $1\mu m$ channel length, $10\mu m$ device width and 44 segments of CNTs in parallel; (c) Pattern to measure CNTFET gate capacitance.

(5). Source/Drain pads deposition. In order to wirebond the devices and solder them into a circuit board, big strong gold pads are required. Experiments show

these pads need to be at least $100\mu m \times 100\mu m$ big and 100nm thick to form firm wirebonds. Thick PMMA and large ebeam electron dose is used in order to lift off thick metal. Both Ti and Au are used to adhere to silicon substrate. The pattern for this second ebeam lithography is shown in Figure 3-16-(b). The pads are designed in a way that there's no thin strip between the two which often causes problems in lift off.

(6). O_2 plasma etching. As shown in Figure 3-14(b), there is a noticeable region of CNT network on the edge of the chip caused by the way we deposit catalyst. It is very likely these CNTs fall off the edge of chip and contact the Si substrate. Although the effect is weak, these CNTs may also cause the long CNTs we use to make devices to connect with each other. This is less a problem in top-gate configuration since devices are not connected to substrate anymore. yet it is safer to perform one step of photo lithography and O_2 plasma etching to get rid of these CNTs. The etched region is shown in Figure 3-17.

(7). Dielectric growth. SiO_2 CVD or atomic layer deposition (ALD) of high-κ material. To get gate dielectric of good quality, CVD is used. ALD is capable of growing dense highκ dielectrics such as HfO_2 and TiO_2. For a CVD process, SiO_2 has to be at least 10nm thick to guarantee insulation and conformability.

(8). Gate electrode deposition. After this step. two types of devices will be formed. One is the top gate CNTFET shown in Figure 3-16(a). The other is a capacitance test structure (Figure 3-16(c)). CNTFET gate capacitance is small and often overwhelmed by parasitics. Thus it is very difficult to perform direct measurements. Thanks to the growth of long nanotube, it is possible to deposit a long gate electrode ($\sim$0.5mm). The gate capacitance can be measured by a AC probe station.

A more detailed recipe for each processing step is described in Appendix C. Figure 3-17 is a mask with complete markers and possible device patterns.

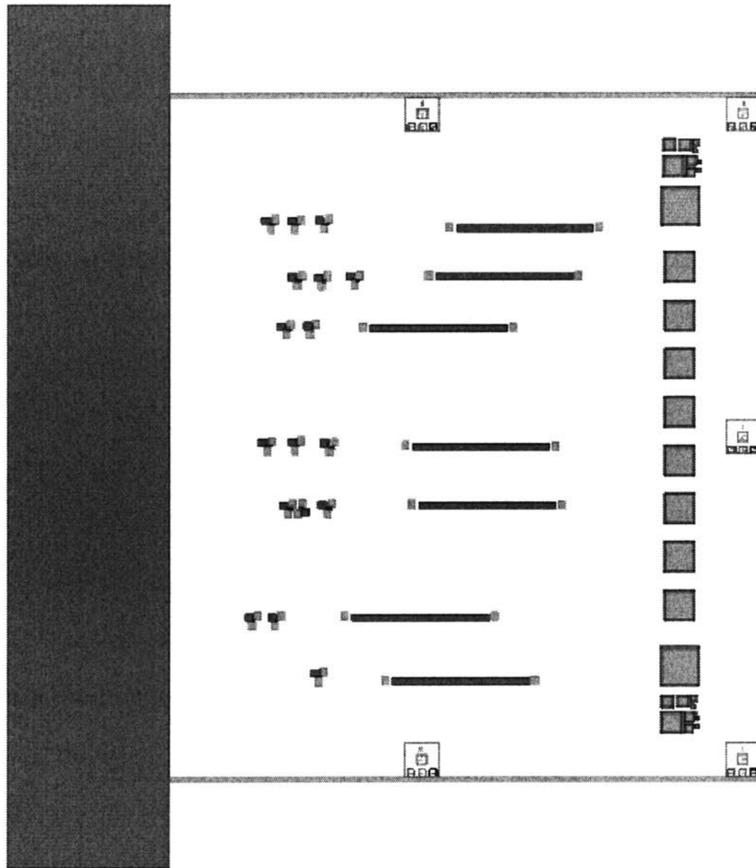


Figure 3-17: Photo mask and ebeam pattern of 1cm×1cm die.

Chapter 4

Measured Results

We have fabricated both types of devices at MTL clean room and NSL Laboratory at MIT. The film devices are capable of carrying large currents and they don't suffer from obvious ambipolar behavior, yet the I_{ON}/I_{OFF} ratio is low. We made the electrically parallel CNTFETs with a maximum of 44 segments from the same CNT. Devices with lower than 1kΩ ON resistance are demonstrated, showing their potential to carry large currents. These devices have relatively high I_{ON}/I_{OFF} ratios. The only problem is the I_{ON}/I_{OFF} degrades under high V_{DS} bias. We will show this problem might be solved by choosing CNTs with small diameter.

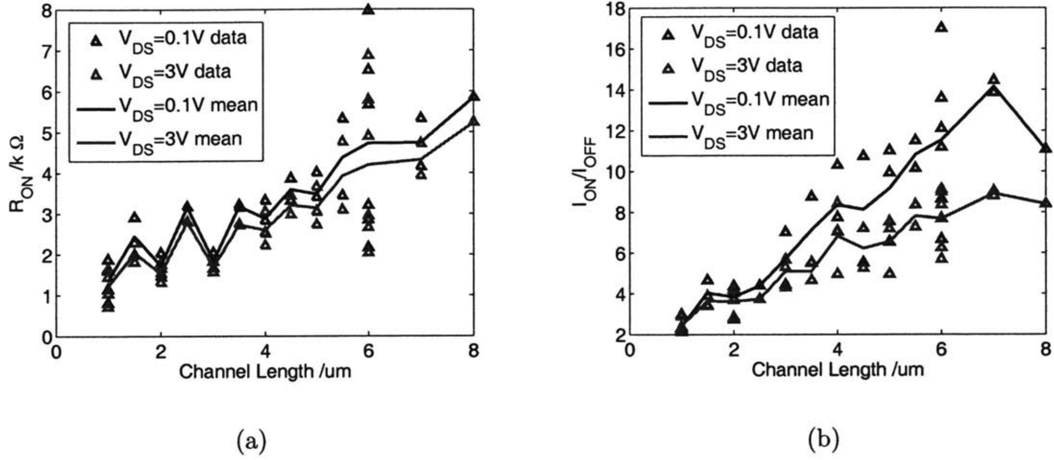
Because of facility limitations, we didn't implement top-gate devices. Top-gate device characteristic is predicted by scaling dielectric thickness from the measurement data of bottom-gate devices in the next chapter for evaluation.

4.1 Nanotube Film Devices

4.1.1 DC Characteristics

Figure 4-1 plots the on resistance and on-off current ratio of twenty-seven 200um wide CNT film devices with various channel lengths ranging from 1μm to 8μm.

As can be predicted, the device resistance goes up linearly as the channel length increases. But the I_{ON}/I_{OFF} ratio gets much improved with longer devices. The on



(a) (b)

Figure 4-1: (a) On resistance of 200μm wide devices with different channel lengths; (b) I_{ON}/I_{OFF} ratio of 200μm wide devices with different channel length.

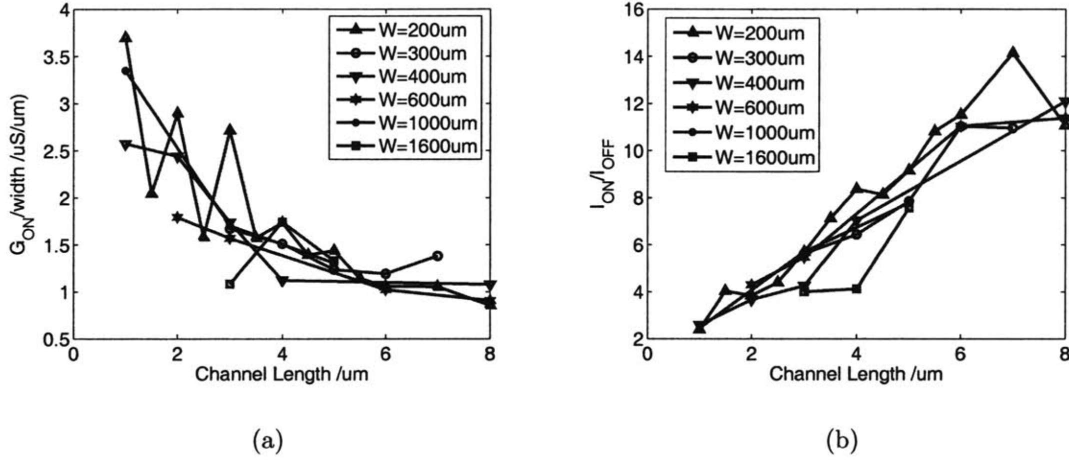
resistance is around the value of 4kΩ and recalling the calculation we did in Chapter 2 this is about 50 times degraded from a device with all paralleled CNTs. Thus, for a 200μm device, we would expect the on resistance to be brought down to around 100Ω, which is about the same value(93.8Ω) if we assume a CNT density of one per 0.5μm$\times$0.5μm square with each CNT having a resistance of 40Ω.

The device, as expected, suffers from variation because the number/chirality of the CNTs in the channel is not well controlled. The resistance normally varies by $\pm$25%. However, it is also interesting to note that the device's I_{ON}/I_{OFF} ratio doesn't degrade under high bias voltages as much as most single tube CNTFETs. This is possibly caused by the film feature of the material.

4.1.2 Device Performance versus Device Geometry

Devices of different geometry is compared in Figure 4-2 where the channel lengths changing from 1μm to 8μm and device width varying from 200μm to 1.6mm. The conductance is inversely proportional to channel length and proportional to channel width as can be seen from Figure 4-2(a). Again, a better switching property (high I_{ON}/I_{OFF}) is accompanied with longer channel lengths. And this improvement is

fairly uniform through devices of different width.



(a)

(b)

Figure 4-2: (a) Unit width conductance of devices with various W and L; (b) I_{ON}/I_{OFF} ratio of devices with various W and L.

4.1.3 Selection of Semiconducting CNTs

Electrical burning is performed using an HP4145B semiconductor parameter analyzer. Voltage as high as 40V is applied to the source and drain terminals of the device with its gate inversely biased. The I-V curve after each burning procedure is shown in Figure 4-3(a). The increase of I_{ON}/I_{OFF} versus time is plotted in Figure 4-3(b). A 10^4 increase can be achieved, however, with the sacrifice of large decrease in conductance.

4.2 Electrically Parallel Nanotube Array Devices

Figure 4-4 shows the SEM images of fabricated devices. 100nm channel length is achieved by ebeam lithography. The number can go down to as low as 40nm as long as it is still the cross-digitized structure due to its symmetry. Multiple devices are fabricated on the same nanotube and some top-gate devices are experimented.

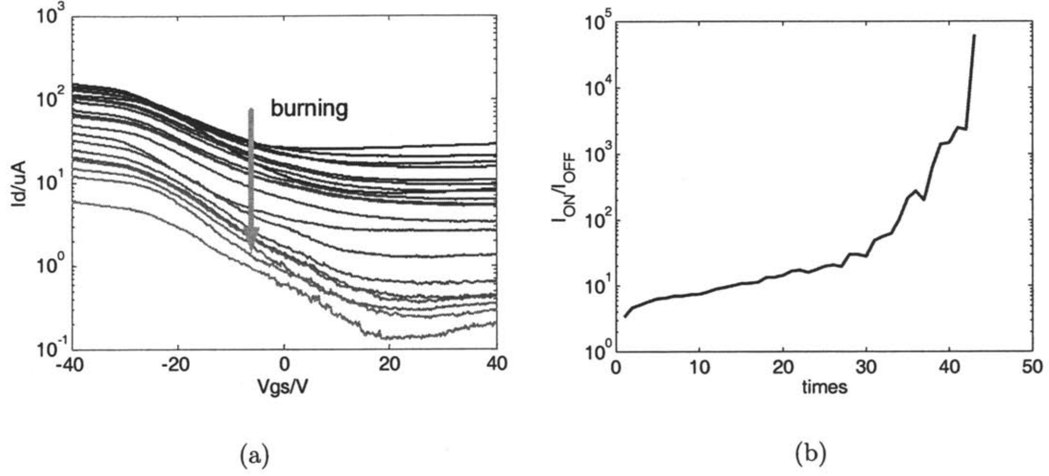


Figure 4-3: (a) I_D-V_{GS} curves before and after electrical burning; (b) I_{ON}/I_{OFF} increases with time

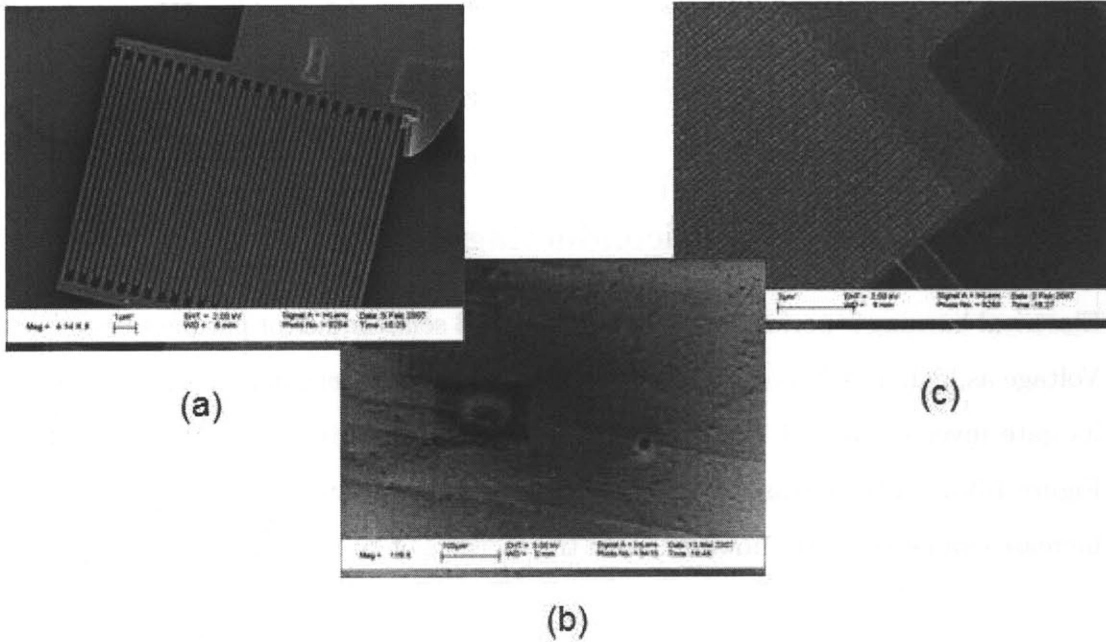


Figure 4-4: SEM images of fabricated CNTFETs. (a) Bottom-gate device with 100nm channel length and 200nm pitch; (b) A 1μm device and a 100nm device fabricated on the same CNT; (c) A top-gate device.

4.2.1 DC Characteristics

Figure 4-5 shows one typical I_D-V_{GS} curve of our fabricated devices. These two devices are of the same structure (1μm long channel, 44 paralleled segments, 1.45nm

in diameter) fabricated from the same CNT. The two devices display very similar characteristics demonstrating the robustness and uniformity of tube.

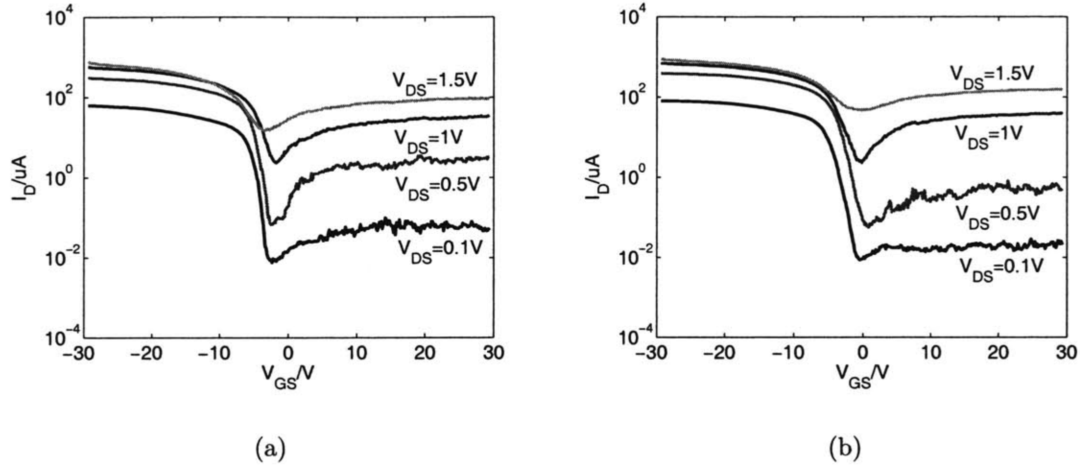


Figure 4-5: I_D-V_{GS} curves of two 44× W/L=10/1 CNTFETs fabricated on the same D_{CNT}=1.45nm CNT with V_{DS} ranges from 0.1V to 1.5V.

Our fabricated CNTFET is capable of delivering 117μA current under V_{DS}=0.1V bias which corresponds to 850Ω resistance. This is a very low value among reported devices based on our knowledge. The device achieves a decent I_{ON}/I_{OFF} ratio of almost 10^4 under 0.1V bias. However, this degrades to only 50 (100x smaller) when V_{DS} rises up to 1.5V. This is due to the relatively small bandgap (0.55eV) of the CNT and the fact that the metal's work function is not deep into the valence band of the nanotube. When V_{DS} is high, it becomes easier for minority carriers to tunnel through the barrier.

4.2.2 Role of CNT Diameter

Table 4.1 lists the measured DC performance of CNTFETs with various diameters. The devices are back-gate by -20V. We could see the transistor resistance is inversely proportional to the diameter of the nanotube. Meanwhile the current's on-off ratio follows roughly the same trend as that of the resistance. This result is in agreement with theory.

Diameter	1.2nm	1.45nm	1.6nm	2.3nm	2.4nm	3.1nm
$I_{ON}(V_{DS}$=0.1V)	105μA	117μA	124μA	142μA	142μA	146μA
R_{ON} per CNT	42.0kΩ	37.5kΩ	35.4kΩ	31.2kΩ	30.9kΩ	30.1kΩ
$I_{ON}/I_{OFF}(V_{DS}$=0.1V)	6.3e5	9.4e3	6.4e3	3.4e3	3.2e3	9.7e2
$I_{ON}/I_{OFF}(V_{DS}$=1.5V)	2.2e3	51	30	19	17	6

Table 4.1: Role of CNT diameter on I_{ON} and I_{OFF}.

4.2.3 Role of CNTFET Geometry

We've fabricated devices of L=1um and L=0.1um on the same nanotube. And their DC characteristics are compared in Table 4.2.

Diameter/nm	1.45	1.6	2.4	3.1
$R_{ON}(1\mu)$:$R_{ON}(0.1\mu)$	0.95	2	1.5	1.3
$I_{ON}/I_{OFF}(1\mu)$:I$_{ON}/I_{OFF}(0.1\mu)$,V_{DS}=0.1V	1.3	1.2	1.0	1.4
$I_{ON}/I_{OFF}(1\mu)$:$I_{ON}/I_{OFF}(0.1\mu)$,V_{DS}=0.8V	12	3.6	13	18

Table 4.2: Role of device channel length on I_{ON} and I_{OFF}

We could see that longer devices suffer from a slightly bigger resistance. The I_{ON}/I_{OFF} ratio, on the other hand, is slightly bigger as well under 0.1V bias. Under 0.8V bias this adtvantage is more manifest by an order of 10~20. This result is interesting that it shows CNTFETs, at least Schottky barrier CNTFETs may not scale the same way as MOSFETs. There might be a best channel length that optimizes the tradeoffs between different circuit specs. The devices of both channel length behave decently under low bias voltage which opens up the possibility of operating CNTFETs under ultro low power supplies.

Chapter 5

Power CNTFETs in DC-DC Converter Circuit

5.1 Buck DC-DC Converter Circuit

Motivated by emerging portable applications that demand ultra low power hardware to maximize battery run-time and System on a Chip(SoC) that requires different power domains for digital, analog and RF blocks, the design of high-efficiency DC-DC converters becomes a key issue in integrated circuits and systems design. A detailed discussion of different DC-DC converter topologies can be found in [39].

A Buck converter circuit which can produce any arbitrary output voltage $0 \leq V_{out} \leq V_{in}$ is shown in Figure 5-1(a). Two power transistors are turned on and off providing alternating high and low voltages at V_x. Low pass filter elements L_f and C_f smooth out the changes in V_x and produce a constant voltage at V_{out}.

The total efficiency of a DC-DC converter is defined as

$$\eta = \frac{E_{load}}{E_{drawn}} = \frac{E_{load}}{E_{load} + E_{cond} + E_{sw} + E_{leak} + E_{control}} \tag{5.1}$$

where E_{drawn} is the total energy drawn from the power supply. It consists of several terms: E_{load} is the energy delivered to the load; E_{cond} is the conduction loss due to the energy dissipated on power transistor ON resistance and is equal to $\int_0^{T_{on}} i(t)^2 R_{ON} dt$;

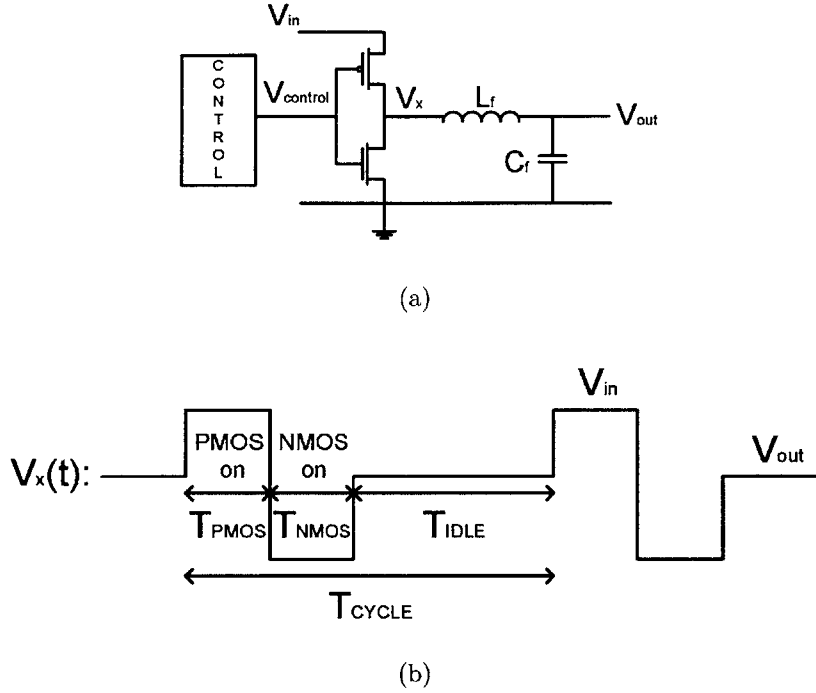


Figure 5-1: (a) A Buck DC-DC converter topology; (b) PFM mode operation of the converter.

E_{sw} is the switch loss due to charging/discharging gate/parasitic capacitances of power transistors and is equal to $\frac{1}{2}(C_{p,G}V_{control}^2 + C_{n,G}V_{control}^2)$; E_{leak} is the energy lost due to leakage and is equal to $\int_0^t I_{leak}V_{in}$; $E_{control}$ is the energy dissipated by the controlling circuitry.

According to [40], when the converter operates at high output voltage, $E_{control}$ is neglegible. When the output voltage is low, $E_{control}$ is still less than half of the energy consumed by the power transistors. Thus, the quality of the power transistors is essential for converter efficiency and we define the efficiency of the power transistors as the energy supplied to V_{out} devided by energy drawn from V_{in},

$$\eta_{device} = \frac{E_{load}}{E_{load} + E_{cond} + E_{sw} + E_{leak}} \tag{5.2}$$

Buck converter can be operated in the Pulse Frequency Modulation mode (PFM) as illustrated in Figure 5-1(b). PMOS and NMOS transistors are on for a time

period T_{PMOS} and T_{NMOS} respectively and are both off for time T_{IDLE} until the output voltage drops below the desired value. For this mode of operation, [40] gives a more detailed analysis and if considering only conduction and switching loss while neglecting other factors, the efficiency of the circuit versus output voltage can be expressed as,

$$\eta_{device} = \frac{\frac{T_{PMOS}^2 (V_{in} - Vout) V_{in}}{2L_f}}{\frac{T_{PMOS}^2 (V_{in} - Vout) V_{in}}{2L_f} + \frac{R_{ON} (V_{in} - Vout)^2 T_{PMOS}^3 V_{in}}{3L_f^2 V_{out}} + C_G V_{control}^2} \tag{5.3}$$

It can be seen the efficiency is determined by the ON resistance and gate capacitance of the device, which is usually a pair of trade-off for both MOSFETs and CNTFETs. Thus, careful sizing of the devices is required.

Replacing the CMOS power transistors with CNTFETs, we show a DC-DC converter block diagram concept depicted in Figure 5-2. A feedback control circuit determines the duty cycle of the clock generator which controls the ON-OFF status of power transistors. Level shifters will be needed if the CNTFET threshold voltage is not yet adjusted compatible with CMOS technology and thus needs a separate supply. The level shifter can be made out of low-to-high voltage comparator. Two p-type CNTFETs (or one p-type CNTFET with a diode) will be used as power transistors. Due to the low operating range of CNTFETs, the The input voltage should not exceed 1.2V.

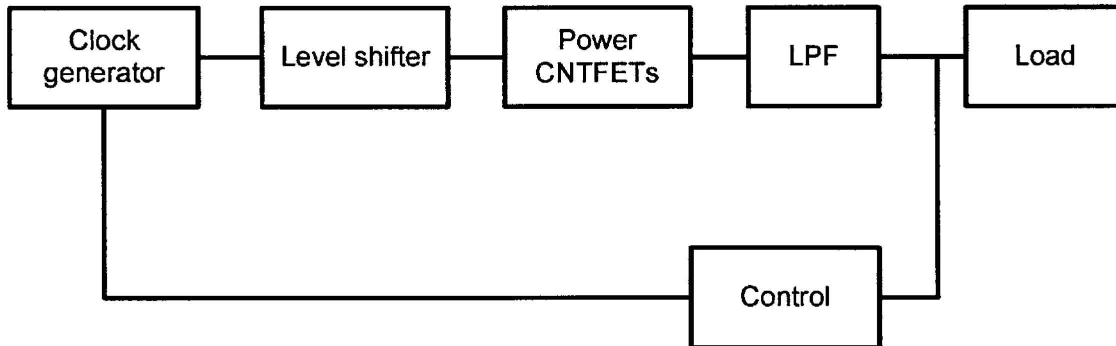


Figure 5-2: DC-DC converter block diagram concept with CNTFETs as power transistors.

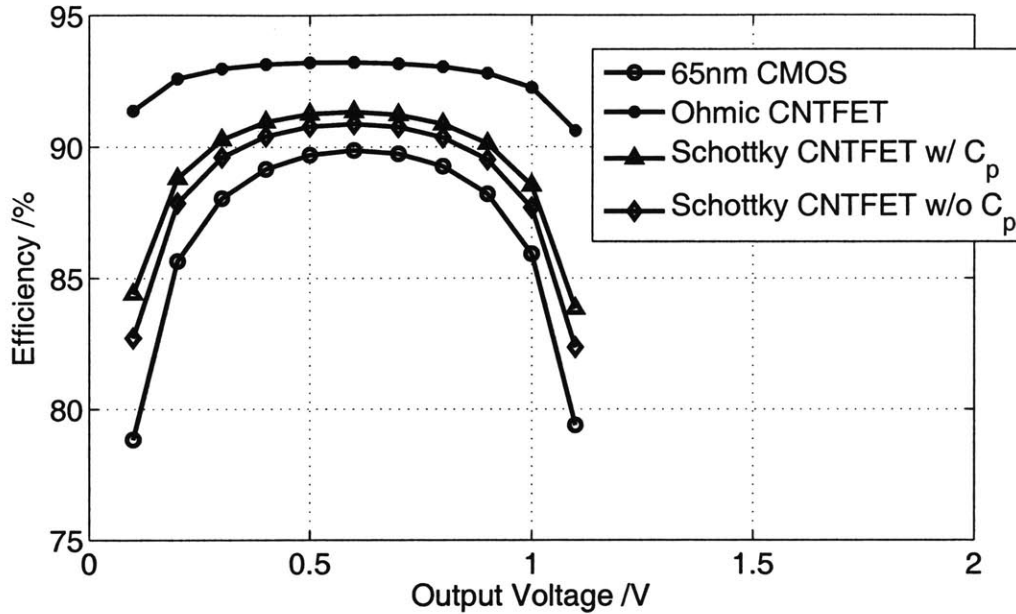
5.2 Performance Benchmarking

In this section, we will focus on the power losses due to power transistors and compare the efficiency between MOSFETs and CNTFETs. In order to make the comparison fair, attention needs to be paid to two issues. First, the two types of devices operate according to different device physics. Although the CNTFET has similar IV characteristics, it is not the scaled version of Si FET. Second, the fabrication of CNTFET is not yet mature and devices are not optimized. Variation exists from process to process and a general conclusion is hard to make.

To handle the first problem, we try to focus more on the small signal circuit model than the detailed device physics. From a circuit point of view, the most commonly used FET performance metric is the gate delay metric, namely $C_{gate}V_{DD}/I$. C_{gate} and I are two tradeoff factors. In order to get a high driving capacity, one wishes to increase C_{gate} to have a tight control of the device and thus increase I. However, that in turn increases the load to drive as well. In the power domain, specifically in the application of DC-DC converters as we have discussed in the previous section, on the one hand we prefer large devices with small R_{ON} for a low conduction loss. On the other hand large devices introduce large gate capacitance which causes large switching loss. Devices will be evaluated based on Equation 5.3.

To eliminate the limitation and variations introduced by fabrication, we are going to compare MOSFETs with CNTFETs of different non-idealities. Figure 5-3 shows the evaluation of these devices based on Equation 5.3. A 1.2V supply voltage, PFM mode of operation with the first device turning on for 16ns and a constant output current are assumed. The 1D ballistic model is used to evaluate the Ohmic contact CNTFET ON resistance. ON resistances of Schottky barrier devices are obtained from measurements. We use numerical simulation tools to calculate both gate capacitance and parasitic capacitance.

The modeled Ohmic contact CNTFETs without parasitic capacitance nor leakage current perform considerably better than MOSFETs. The device has only half the loss that of the MOSFETs. For the Schottky barrier devices, the performance is still



(a)

Figure 5-3: Conversion efficiency of MOSFETs and CNTFETs.

slightly better than MOSFETs. The parasitic capacitance consumes roughly 10% more energy loss. Equation 5.3 needs to be adjusted if considering the leakage of CNTFETs under high bias. The efficiency goes down to only 60% with the measured 10^3 I_{ON}/I_{OFF} ratio. Thus in order to improve the performance of CNTFET, the most important issue is to increase the low I_{ON}/I_{OFF} ratio under high bias. This may possibly be solved by playing with CNT/metal work functions by the means of doping, which is also what people do in CMOS technology.

5.3 Design Methodology

Using transistor built out of carbon nanotubes is an emerging technology. It is still early to propose CNT circuit design rules. However, because of the uniqueness of carbon nanotubes there is a lot of space for circuit designers. Here are some possible aspects for consideration.

5.3.1 Optimizing the Number of CNTs

The number of CNTs in parallel is an equivalent concept as the width of a MOSFET. Large number of CNTs will reduce ON resistance but will increase capacitance and leakage. The energy loss in a DC-DC converter is,

$$E_{\text{loss}} = E_{\text{switch}} + E_{\text{cond}} + E_{\text{leak}}$$

$$= C_G V_{control}^2 + \frac{R_{ON}(V_{in} - V_{out})^2 T_{PMOS}^3 V_{in}}{3L_f^2 V_{out}} + \frac{V_{in}^2}{V_{out}} T_{PMOS} I_{leak} \tag{5.4}$$

Here the parameters obey that $C_G = NC_{G0}$, $R_{ON} = R_{ON0}/N$ and $I_{leak} = I_{leak0}N$ where N is the number of CNTs and C_{G0}, R_{ON0} and I_{leak0} are gate capacitance, ON resistance and leakage current with a single tube. Inserting the relations into Equation 5.4, we can solve for the optimum number of CNTs to be

$$N = \sqrt{\frac{R_{ON0}(V_{in} - V_{out})^3 T_{PMOS}^3 V_{in}}{3L_f^2 V_{out} \left(C_{g0} V_g^2 + \frac{V_{in}^2}{V_{out}} I_{leak0} \right)}} \tag{5.5}$$

5.3.2 Optimizing CNT Diameter

As we have seen from the measurements, the transistor behavior heavily depends on the CNT diameter which in turn affects the performance (power, speed, etc.) of the circuit. Based on the measured data, we plot the conversion efficiency versus nanotube diameter in Figure 5-4. The four curves represent the four cases of V_{out}=0.3V, considering parasitic capacitances; V_{out}=0.9V, considering parasitic capacitance; V_{out}=0.3V, not considering parasitic capacitance and V_{out}=0.9V, not considering parasitic capacitance respectively.

It can be seen that when parasitic capacitance is taken into account, because switching loss is dominant and it affects CNTFETs of different diameters similarly, the curves are relatively flat. On the other hand, when there is no parasitic capacitance, since leakage plays a more important role than conduction loss, CNTs with smaller diameters show advantages. Also, the 0.9V curve is flatter than the 0.3V curve meaning leakage loss is more of a problem when converting to a low voltage.

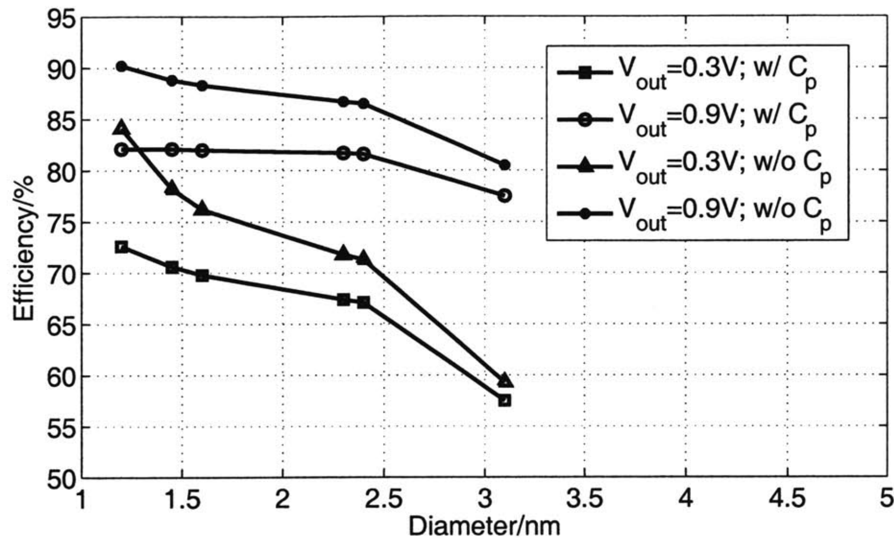


Figure 5-4: Conversion efficiency versus CNT diameter.

Thus based on the specs of the circuit and the specific fabrication process, we can choose CNTFET with different diameters for optimization. In general, considering the current fabrication conditions, CNTs with smaller diameters are preferable.

5.3.3 Optimizing Spacing between CNTs

The spacings between CNTs may also be a factor for optimization. Increasing spaces between parallel CNTs will increase the gate capacitance as discussed in Chapter 2 and at the same time decrease the ON resistance. This will also introduce more parasitic capacitance if there is any. Because there's no measured data on capacitance, we will not discuss this part in detail.

In short, because of the discrete nature of CNT, flexibility is added to circuit design which provides space to make trade-offs.

Chapter 6

Conclusions and Guidelines for Future Work

6.1 Conclusions

In this work, we tried to explore and leverage the advantages from using CNTFETs in circuit design, especially for power applications. A simple theoretical model based on Landauer-Büttiker equation is used to evaluate the ideal performance of ballistic CNTFETs with Ohmic contacts. Then non-idealities and parasitic effects are added from either numerical simulations or measured results. Process flows to fabricate CNTFETs capable of carrying large current are proposed and analyzed. Devices utilizing many segments of the same nanotube that is capable of conducting $\sim 100\mu$A current at V_{DS}=0.1V are demonstrated.

Several conclusions are drawn from measurements. The DC characteristics of CNTFETs heavily depend on its diameter size. A small diameter indicates large I_{ON}/I_{OFF} ratio, but its corresponding I_{ON} is smaller. CNTFETs don't scale in the same way as MOSFETs do in the sense that the conductance doesn't decrease much with increased channel lengths due to its ballistic transport within the channel. Yet under high bias voltages, an increased I_{ON}/I_{OFF} ratio benefits from long channel lengths because of the suppressed tunneling of electrons in a p-type device and that of holes in a n-type device.

Combining the measured results and theoretical calculations, we are able to benchmark the performance of CNTFETs and compare it with that of MOSFET devices in the setting of a Buck DC-DC converter circuit. We can see without fabrication limitations or the contact issue, the CNTFETs have full potential to pass the traditional MOSFETs. In order to make this happen, it is most critical to decrease leakage current by forming Ohmic metal-CNT contact. Parasitic capacitance caused by mis-alignment in fabrication is another issue that needs to be solved. Theoretically, by optimizing the number of nanotubes, nanotube diameter, spacing between nanotubes, device channel length and dielectric thickness, we can achieve the optimum performance of CNTFETs.

6.2 Future Work

A lot of further work can be done on the topic of power application of CNTFETs, and also CNTFETs at both the device and circuit level. It is critical to figure out the physics and working mechanism behind CNTs and CNTFETs, and verify it with experiments. Although CNTFETs work similarly to MOSFETs, they are not completely the same. Thus instead of applying the rules from MOSFET circuit design to CNTFETs, it is better to start from the uniqueness of CNTFETs to look for applications. For example, a lot of the fabricated devices show hysteresis behavior, the physics of which is not very well understood. If the hysteresis is intrinsic with CNT, they may not be suitable for high speed applications despite of their ballistic transport. Instead, they may be used as memory element [41]. Meanwhile, if the reason for hysteresis is known, people can seek for ways to reduce it effectively.

CNT synthesis, i.e., controlling the grown CNT position, orientation, density and even chirality has been a hot topic among chemists for a while. As we have analyzed in this work, it is something that must be done before CNTFETs to surpass MOSFETs in performance.

People have been improving and optimizing CMOS process during the past 50 years. And current CMOS technology requires more than 200 processing steps. Con-

sidering that, there must be enough room for research in the area of CNTFET fabrication. Methods to improve the CNTFET performance and increase the yield are anticipated.

There have been many published works on predicting improvements by replacing MOSFETs with CNTFETs in integrated circuits. However, designing a circuit involves trade-offs between different aspects. It would be more informative to compare these two types of devices thoroughly in all aspects. And a good model that can capture the characteristic of CNTFETs of various geometries is needed.

In particular, we suggest the following aspects as a continuation of this work:

(1) More experiments need to be done to guarantee the yield of CNT growth. Although we managed to reach a decent yield in this work, a lot of the condition parameters such as growth time, catalyst concentration, CVD tube length are yet to be optimized. An effective method to differentiate single SCNT from SCNT bundles is very desirable since it not only increases the yield but also saves cost to fabricate on CNT bundles.

(2) In this work, we showed how device IV characteristics depend on CNT diameter and device channel length. More fabricated devices are needed for a statistical analysis. And dependences on contact metal, dielectric thickness would be of interests. These measurements will help justify/disprove proposed theories on CNTFETs which will in turn serve as fabrication guidelines.

(3) Several fabrication steps may be improved. For example, SiO_2 is used as the substrate to grow nanotubes. Yet using other materials such as polymers won't change the fabrication flow but may help CNTs and metals stick better to the device. Using those materials might save one ebeam lighography step. It is also possible to transfer the whole fabrication process to clean rooms of higher rating. In ebeam deposition, a clean environment will improve the quality of device contact.

(4) Some of the proposed ideas are not fully implemented due to the lack of equipment. Top-gate devices and capacitance testing structures can be built once

ALD is available. These structures are very useful in evaluating the AC performance of CNTFETs.

(5) If a mature fabrication flow is available, future work can focus on device variation characterization, threshold voltage engineering and noise analysis.

Appendix A

Analytical Expression for Ohmic Contact CNTFET Current

Current is formed when charged particles flow in a direction with velocity v_i.

$$
\begin{aligned}
I &= \sum_i q v_i \\
&= \sum_i q \frac{1}{\hbar} \frac{\partial E(k_i)}{\partial k_i} \\
&= \sum_{k_i} q \frac{1}{\hbar} \frac{\partial E(k_i)}{\partial k_i} \cdot 2\partial N(k_i) \\
&= \sum_{k_i} 2 \frac{q}{\pi\hbar} dE(k_i) dE \frac{\partial N(k_i)}{\partial k_i} \\
&= \sum_E \frac{q}{\pi\hbar} f(E) dE \\
&= \int \frac{q}{\pi\hbar} f(E) dE
\end{aligned}
$$

Adding both fore channel and back channel current in CNT and summing up from all the energy bands i, we get

$$
I_D = \frac{q}{\hbar\pi} \sum_i \int_{E_i} [f(E,\mu) - f(E,\mu - qV_{DS})] dE_i \tag{A.1}
$$

Appendix B

Analytical Expression for CNTFET Gate Capacitance

The cross section view of a top-gate CNTFET device is shown in Fig.B-1(a). It can be modeled by an infinitely large conducting plane and a hollow metal cylinder(Fig.B-1(b)). Based on electrostatics all the electrical lines must be perpendicular to the metal plane. Using symmetry, the electrical field is the same as that by replacing the infinite plane with a mirrored cylinder with negative charge at the other side(Fig.B-1(c)). It can be shown that these two cases form the same capacitances between them.

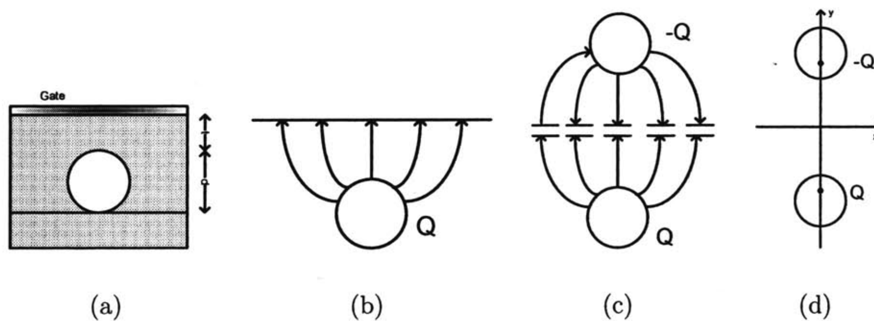


Figure B-1: (a) Cross section of CNTFET; (b) Infinite metal plate and hollow metal cylinder; (c) Mirrored metal cylinder; (d) Equivalent charged lines

In order to calculate the capacitance in B-1(c), we can further replace the two

cylinders with two charged lines of the same amount of charge Q. This step can be validated by computing the electrical potential contours of the charged lines. In fact, for two lines located at $(x = 0, y = \pm a)$, the U_0 contour is a cylinder centered at $(0, \frac{k^2+1}{k^2-1}a)$ with a radius of $r = \frac{2ka}{k^2-1}$, where $k = \exp(\frac{2\pi\varepsilon U_0}{Q})$.

In order for the charged lines' potential contours be exactly the cylinders, relations

$$\begin{cases} \frac{k^2+1}{k^2-1}a + \frac{2ka}{k^2-1} = d + t \\ \frac{k^2+1}{k^2-1} - a\frac{2ka}{k^2-1} = t \end{cases} \tag{B.1}$$

must be satisfied. Thus

$$\begin{cases} a = \sqrt{(d+t)t} \\ k = \frac{\sqrt{d+t}+\sqrt{t}}{\sqrt{d+t}-\sqrt{t}} \end{cases} \tag{B.2}$$

Since

$$k = \frac{\sqrt{d+t}+\sqrt{t}}{\sqrt{d+t}-\sqrt{t}} = \exp(\frac{2\pi\varepsilon U_0}{Q}) \tag{B.3}$$

we obtain

$$U_0 = \frac{Q \ln \frac{\sqrt{d+t}+\sqrt{t}}{\sqrt{d+t}-\sqrt{t}}}{2\pi\varepsilon} \tag{B.4}$$

The capacitance is calculated as

$$C = \frac{Q}{U_0} = \frac{2\pi\varepsilon}{\ln \frac{\sqrt{d+t}+\sqrt{t}}{\sqrt{d+t}-\sqrt{t}}} \tag{B.5}$$

Appendix C

CNTFET Fabrication Process Flow

Step	Description	Lab:Machine	Recipie
0	**Sample Pre-preparation**		
0.1	buy wafer from vendor	siliconquest	4" P<100>; 1-10$\Omega - cm$; 500-550μm; 250μm silicon dioxide
0.2	cut wafer	ICL:diesaw	1cm$\times$1cm chip
1	**Maker Patterning**		
1.1	prebake	EML:hotplate	150°C, 1min
1.2	spin coat	EML:coater	NR7-1000, r000rps, 30sec
1.3	bake	EML:hotplate	100°C, 1min
1.4	expose	EML:HiRes	12sec
1.5	develop	EML:hood	NR6, 1min; water, 30sec; water
1.6	metal deposition	EML:ebeam	Ti, 5nm; Pt, 50nm
1.7	lift off	EML: hood	RR-4; water
2	**CNT** Growth		
2.1	deposit catalyst	NMELAB:hood	$FeCl_3$ in water/hexane
2.2	growth	NMELAB:furnace	1000Sccm CH_4, 900°C, 20min

3	**CNT** Location		
3.1	SEM image	NSL:Raith	3kV
3.2	make mask		
4	**S/D Patterning**		
4.1	spin coat PMMA	EML:coater	4.5% PMMA, 3000rps, 45min
4.2	bake	EML:hotplate	100°C, 20min
4.3	ebeam lithography	NSL:Raith	30kV, 230 $C/\mu m^2$
4.4	develop	NMELAB:hood	PSK 2:1, 90sec; IPA, 1min
4.5	depostion	EML:ebeam	Pd, 10nm
4.6	lift off	NMELAB:hood	NMP, 12hr
5	**Pads Patterning**		
5.1	spin coat PMMA	EML:coater	6% PMMA, 2500rps, 45min
5.2	bake	EML:hotplate	100°C, 20min
5.3	ebeam	NSL:Raith	10kV, 200 $C/\mu m^2$
5.4	develop	NMELAB:hood	PSK 2:1, 90sec; IPA, 1min
5.5	depostion	EML:ebeam	Ti, 10nm; Au, 100nm
5.6	lift off	NMELAB:hood	NMP, 10min
6	**Destroy Extra CNT**		*Optional*
6.1	prebake	EML:hotplate	150°C, 1min
6.2	spin coat	EML:coater	3000rps, 30sec
6.3	bake	EML:hotplate	100°C, 1min
6.4	expose	EML:HiRes	12sec
6.5	develop	EML:hood	NR6, 1min; water 30sec
6.6	plasma etch	EML:RIE	O2, 500W, 3min
7	**Package**		
7.1	wire bonding	ICL:goldwire	150°C

Table C.1: Fabrication process for electrically parallel CNTFET.

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