Pulse-Based Ultra-Wideband Transmitters for Digital Communication

by

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B.S., University of Michigan (1999)
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Abstract

Ultra-wideband radio (UWB) is a rapidly developing wireless technology that promises unprecedented data rates for short-range commercial radios, combined with precise locationing and high energy efficiency. These benefits stem from the use of wide bandwidths and impulse signaling, implying high channel capacity and precise time resolution. UWB has been used for military radar and imaging since the 1950's; however, in 2002 the Federal Communications Commission approved the use of the 3.1-10.6GHz band for unlicensed UWB applications. The restriction on transmitted power spectral density in this band is equal to the noise emission limit of household digital electronics. This band is also shared with several existing services, therefore in-band interference is expected and presents a challenge to UWB system design.

This thesis covers the aspects of pulse generation and transmitter implementation for pulsed-UWB communication by exploring tradeoffs that can be made in the pulse shaping in order to reduce power consumption in the transmitter electronics. A transmitter has been developed that exploits the exponential properties of a BJT to approximate a Gaussian shape. It generates BPSK modulated pulses at 100Mb/s in one of 14 channels in the 3.1-10.6GHz band, targeting high data rate applications. The transmitter has been fabricated in a 0.18μm SiGe BiCMOS process, and experimental results are presented. A second transmitter has been developed that uses an all-digital architecture. This architecture is made practical by relaxing the RF frequency tolerance, suitable for communication with an energy detection receiver using pulse position modulation. By using an all-digital architecture, energy is consumed only in CV^2 switching losses and subthreshold leakage currents, and no RF oscillator or analog bias currents are required. This transmitter has been fabricated in a 90nm digital CMOS process, and demonstrated in a 16.7Mb/s wireless link.

Thesis Supervisor: Anantha P. Chandrakasan
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Chapter 1

Introduction

Pulsed ultra-wideband (UWB) signaling is an emerging field of research that has roots that can be traced back to the original Marconi spark gap radio. This field is only recently gaining momentum because of a change in FCC regulations that now allows unlicensed communication using UWB. UWB signaling has many attributes that make it attractive for a wide range of applications; from ultra-low-power RFID tags and wireless sensors to streaming wireless multimedia and wireless USB at greater than 1Gb/s. This chapter introduces UWB signaling and regulations, with more details on its wide application space, and outlines the contributions of this thesis presented in the following chapters.

1.1 Background

In February of 2002, the FCC approved the use of the 3.1-10.6GHz band for UWB communication [1, 2]. This was after six years of receiving the suggestions and concerns from a handful of determined UWB startups and several large companies and government agencies. Several concerns were raised by the Department of Defense, which has used UWB for years in military applications and didn't want the technology commercialized. Interference to GPS devices was also a major concern for the military. The Department of Transportation and Federal Aviation Administration (FAA) were concerned UWB would interfere with aircraft radar. Cellular and per-

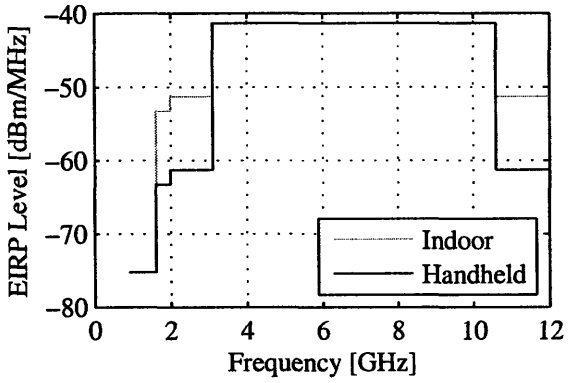

Figure 1-1: FCC emissions limit for indoor and outdoor UWB communication.

sonal communications service (PCS) companies such as Sprint and Cingular were concerned about interference to cell phones, and the threat of future competition [3]. The FCC reviewed nearly 1000 suggestions, and commissioned studies of its own through the National Telecommunications and Information Administration (NTIA) [4]. Ultimately, the FCC approved the commercial use of UWB, and a new technology for wireless communication was born.

The noise emissions limit for digital electronics above 960MHz is set by the FCC at a constant -41.3dBm/MHz [5]. For example, personal computers are allowed to radiate noise below this level at any frequency above 960MHz. The original intent of UWB communication was to transmit data within the emissions limits already placed on personal computers. However, due to interference concerns from UWB radiators to other existing wireless services the FCC placed "conservative" requirements on UWB emissions. These limits are shown in Figure 1-1 and tabulated in Table 1.1. Instead of a constant -41.3dBm/MHz above 960MHz, a deep notch is placed around GPS and PCS services because these receivers have higher sensitivities. GPS operates at 1.2 and 1.6GHz, and PCS at 1.9GHz. There are also stricter requirements on outdoor, or handheld UWB devices, than indoor UWB devices.

UWB signaling has been used in the military since the 1960's for both communication and radar. The UWB pulses used in radar applications were low-frequency, high-power, and generated with non-linear devices and transmission lines that can not

Table 1.1: FCC Mask Limits

Frequency Range $[MHz]$	Indoor Limit $[dBm/MHz]$	Outdoor Limit $[dBm/MHz]$
Below 960	FCC 15.209	
960-1610	-75.3	-75.3
1610-1990	-53.3	-63.3
1990-31000	-51.3	-61.3
31000-10600	-41.3	-41.3
Above 10600	-51.3	-61.3

be integrated in a high volume process. Pulses were generated using bulk avalanche semiconductors, high voltage breakover devices, high voltage Gallium Arsenide thyristors, plasma diodes, or stacked arrays of step recovery diodes (SRD). They required hundreds to thousands of volts for proper operation, and supported pulse repetition frequencies (PRF) in the 1-10's of kHz range. Relatively low-power pulses were generated from avalanche transistors, low voltage SRDs, and Zener diodes. Typically the devices needed to be hand selected for avalanche or breakdown characteristics [3]. Some of this technology for low-frequency pulse generation is still actively researched today [6].

1.2 UWB Signal Characteristics

UWB has several advantages over traditional narrowband architectures. From a channel perspective, the wide bandwidth can offer excellent robustness to multi-path fading. For example, a Gaussian monocycle transceiver experiences only a 1.5dB fading margin in dense multipath, which is very low when compared to deep fades experienced in narrowband systems [7]. Additionally, the narrow pulses in time offer the ability to perform precise locationing combined with communication. UWB has the potential for a spatial capacity that is orders of magnitude above other popular wireless standards like 802.11a, 802.11b, and Bluetooth [8]. The main limitation of UWB communication is the presence of strong, in-band interference that can easily saturate the UWB receiver front-end. The overlap between UWB and existing services is a

major concern in both the transmitter and receiver design, since UWB transmitters will also raise the noise floor seen by narrowband victim receivers.

The IEEE 802.15 working group has selected nine interferer models to be considered when evaluating the performance of a UWB communication standard: a microwave oven (2.4GHz), 802.15.1 (Bluetooth), 802.11b, 802.15.3, 802.11a, 802.15.4, generic in-band modulated interference, generic in-band tone interference, and out-of-band interference [9]. Of the interferers considered, 802.11a is the only one whose frequency band is overlapped by the UWB communication band. WiMAX was not included in this list, but will likely communicate in the 3.4-3.6GHz band. This range of frequencies for WiMAX directly interferes with all WiMedia compliant UWB chipsets available today [10].

The Unlicensed National Information Infrastructure (U-NII) band is divided into three subbands: 5.15-5.25, 5.25-5.35, and 5.725-5.825GHz. This is a problem for UWB systems because this range falls in the middle of the UWB band, and uses relatively large power levels. Each band has an EIRP limit of 4, 11, and 16dBm/MHz, respectively, five orders of magnitude higher than the UWB emissions limit. The subbands are further divided into five 20MHz channels. The 802.11a standard employs OFDM with 52 carriers in four of the five channels in each U-NII band, for a total of 12 channels.

By far the most popular solution for coexistence between UWB and 802.11a is for the UWB devices to avoid the 802.11a band entirely [10, 11]. Several UWB architecture proposals specify no signals will be transmitted in this band, and that the UWB receiver have a notch filter to combat the jamming effect of an 802.11a signal. Recent work has shown that notch filtering of the U-NII bands can be integrated into the antenna [12].

1.3 UWB Applications

UWB communication is being considered for a wide range of applications, as illustrated in Figure 1-2. UWB chipsets have already been demonstrated in short range,

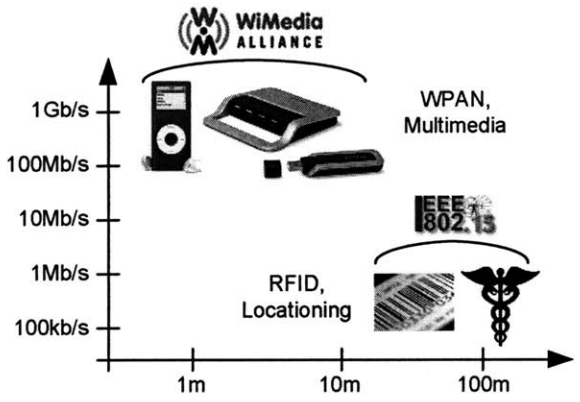

Figure 1-2: Ultra-wideband technology is being considered for a wide range of applications.

high data rate applications including streaming video from a DVD player to an in-home TV, or to headrest-mounted LCD displays in a vehicle. Wireless USB has also been demonstrated over UWB, and the first wireless USB product appeared in 2006. UWB offers the potential for precise locationing capabilities, therefore it is also being used for RFID tagging and low data rate, long range communication. One of the largest applications in this space has been for asset and patient tagging in hospitals.

1.3.1 High Data Rate Applications

The IEEE created the 802.15.3a task group in 2002 to investigate using UWB as a physical layer for high data rate, short range wireless personal area networks (WPAN). This task group solicited proposals for a new WPAN standard, requiring that all proposals submitted to the committee to meet certain specifications [13]. The minimum specifications were a data rate of 100Mb/s at 10m and 200Mb/s at 4m with a maximum power consumption of 100mW and 250mW, respectively, and a maximum uncoded bit error rate (BER) of 10^{-9}. Additionally, a data rate greater than 480Mb/s was desirable, even if at reduced ranges. Four piconets in close proximity were required to simultaneously operate at these data rates. These specifications are sufficient for most WPAN applications, some of which are listed in Table 1.2.

The 802.15.3a task group had narrowed the proposals for a WPAN standard down to two by 2005: one OFDM based, and one pulse based. The task group was dis-

Table 1.2: Data rate requirements for short range wireless applications.

Application	Data Rate [Mb/s]
High-definition video stream	19.2
Dolby Digital 5.1 or 10.2 channel audio	13.8 or 27.6
PC monitor or projector	63 to 1000
Video camera with MPEG2 resolution	75 to 150
Wireless hard drive	> 1000

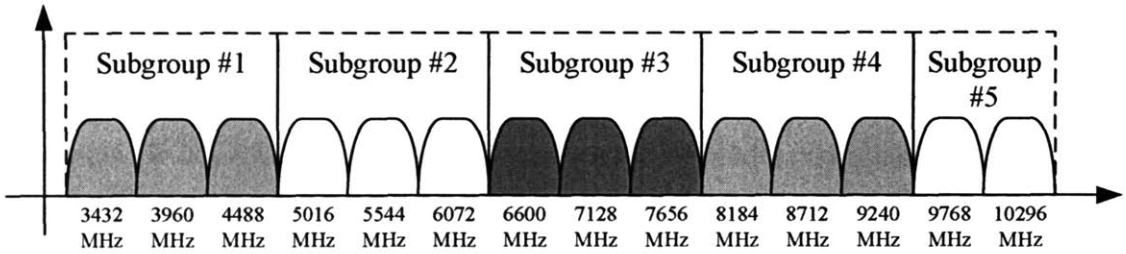

Figure 1-3: Band plan for the WiMedia Alliance OFDM based proposal for WPAN.

banded in 2006 when an agreement couldn't be reached on which proposal should become the standard.

1. *OFDM Proposal* - Proposed by the MultiBand OFDM Alliance (MBOA) [10], and later adopted by the WiMedia Alliance, this technical approach uses an OFDM standard that essentially expands on other current OFDM physical layers, such as 802.11g. The supported data rates range from 53.3Mb/s to 480Mb/s. The transmitted signal is synthesized with a high speed DAC, and can therefore be very spectrally efficient compared to pulse-based transmitters. OFDM modulation is inherently robust against channel multi-path, as well as gain, phase, or group delay variations in the transceiver. This proposal divides the UWB band into 14 channels, spaced 528 MHz apart, as shown in Figure 1-3. The channels are grouped into subgroups of two or three channels, and frequency hopping is implemented within each subgroup.

   As the OFDM transmitter hops among three bands in a band group, it transmits a power level that is three times the maximum FCC limit. Therefore, at any given time, the transmitter uses one third the bandwidth and three times

the power spectral density. As the transmitter rapidly hops among the three channels in the subgroup, the emissions average out to the FCC limit in any given channel. The higher transmit power can pose an increased risk to victim receivers, however a waiver was granted by the FCC specifically for this approach [14]. A drawback to this frequency hopping scheme is the rate at which hops are made must be less than 10ns with a maximum hop distance of 1056MHz. This is to be accomplished with a PLL, therefore multiple oscillators are required with a either a multiplexer to select the LO [15–17], or replicated hardware in the RF front-end for each channel [18].

2. *DS-UWB Proposal* - The alternate proposal submitted to the 802.15.3a task group is a direct sequence UWB (DS-UWB) architecture from the UWB Forum [11]. This architecture is pulse based, using BPSK modulation or an optional bi-orthogonal keying (BOK) mode. BOK modulation uses a set of orthogonal codes for direct sequence spreading, increasing the data rate by selecting a code based on the transmitted data. The signal is transmitted in two general bands, one from 3.1-4.85GHz and one from 6.2-9.7GHz as shown in Figure 1-4. The actual center frequency depends on the piconet channel being used, and the channels are offset by 39MHz. The piconets are therefore designed with significant overlap, using baseband signal processing to resolve the channels. The supported data rates range from 28Mb/s to 1320Mb/s.

   One advantage of this architecture is many components of the baseband processor may be made scalable, such as the number of fingers in the rake receiver, the time duration of the equalizer, or the datapath bit widths. This scaling is attractive for energy efficiency, because the power consumption can scale gracefully with performance, depending on the signal SNR and multipath. The ability to scale the hardware sets the DS-UWB approach apart from OFDM systems. OFDM architectures do not scale as well and have hard limits on the minimum processing required for arbitrarily high SNR.

A high data rate transmitter has been developed as a part of this thesis that inte-

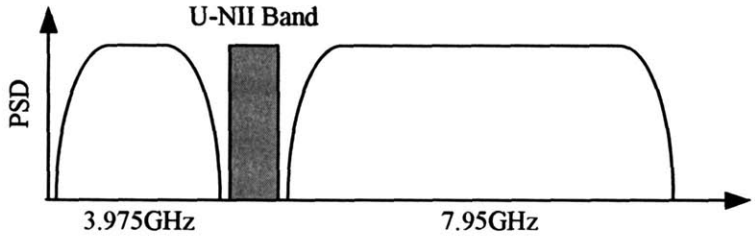

Figure 1-4: Band plan for the DS-UWB pulse based proposal for WPAN.

grates into a custom chipset as a team effort with other students [19]. This transceiver is targeting high data rate applications (Table 1.2) with a data rate of 100Mb/s at 10m. The architecture combines features from the two 802.15.3a proposals. From the OFDM proposal, the 14-channel frequency plan is adopted to better partition system complexity between the analog and digital domains. The signaling is BPSK pulses, with a digital back-end architecture similar to that for the DS-UWB proposal. The architecture leverages the graceful scaling of power consumption and performance of the DS-UWB architecture to build an adaptable transceiver.

1.3.2 Low Data Rate, Tagging Applications

Another application well suited for UWB is radio frequency identification (RFID) tags. In September 2004, Parco Wireless installed a network of RFID tags using UWB for communication and locationing to track patients, staff, and equipment in a Washington D.C. hospital. The tags relay battery status, tag tampering information, and status of the medical device to which they are attached using UWB technology [20]. The advantages of using UWB for this application are the startup time for the tag radios, and the positions of the tags can be tracked with sub-foot precision [21]. The required data rate in this application is less than 100b/s, but data rates for RFID tags in general could be much lower. In this regime when buffering data is not practical, radio startup time dominates the energy consumption in the network. UWB circuits have transient responses on the order of 100ps, and often do not require a local oscillator and phase-locked loop to startup and settle. Therefore, they may be started up in a very short amount of time, reducing the total energy consumed in

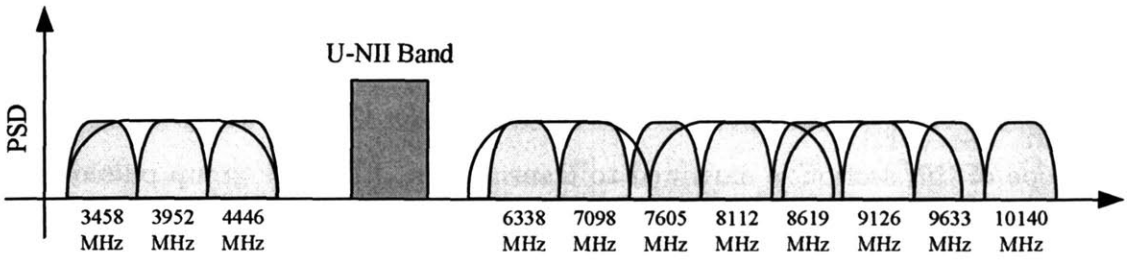

Figure 1-5: Band plan for the IEEE 802.15.4a WPAN standard.

the network.

Conventional RFID tags communicate with narrowband signals in the 125kHz, 13.56MHz, or 915MHz bands. The higher RF power allowed in these bands enables passive tags to harvest energy from the received narrowband RF signal. Harvesting energy from a pulse-based UWB signal is not practical due to the low transmitted power level. The total transmitted power allowed by the FCC from 3.1-10.6GHz is -2.5dBm, that is, if the entire band could be used with 100% efficiency. Therefore, UWB RFID tags must either be active (battery powered) or use some other form of energy harvesting. Transmitting via backscattering, commonly used in narrowband RFID applications [22], is also not practical at these power levels. UWB signaling does offer advantages such as precise locationing, virtually undetectable communication, and energy efficiency.

The IEEE has recently completed a standard, titled 802.15.4a, for short range, low data rate communication and ranging in a wireless personal area network (WPAN) [23]. The standard utilizes the 2.4GHz ISM band, sub-GHz UWB band, and 3.1-10.6GHz UWB band. The 3.1-10.6GHz band has been subbanded into the frequency plan shown in Figure 1-5. The data rates supported range from 100kb/s-27Mb/s, using pulse position modulation (PPM), or a combination of PPM and BPSK. This standard is extremely flexible, supporting several mandatory and optional modes to accommodate a range of radio architectures and applications.

1.4 Previous Work

This thesis focuses on the aspects of pulse generation for UWB transceivers; therefore, the scope of this section is narrowed to transmitters. I broadly group pulsed-UWB transmitter architectures into two categories defining how the pulse energy is generated in the 3.1-10.6GHz UWB band:

1. The first category includes transmitters that generate a pulse at baseband and up-convert it to a center frequency in the UWB band by mixing with a local oscillator (LO) [24, 25]. The transmitter may not have an explicit mixer that performs the up-conversion mixing. This architecture is easiest identified by having a LO at the center frequency of the pulse. The transmitters presented in Chapters 3 and 4 fall into this category.

2. The second category includes transmitters that generate a pulse that directly falls in the UWB band without requiring frequency translation. The pulse width for these types of transmitters is usually defined by delay elements that may be tunable or fixed, as opposed to oscillators. A baseband impulse may excite a filter that shapes the pulse [26, 27], or the pulse may be directly synthesized at RF with no additional filtering required [28, 29]. The transmitter presented in Chapter 5 falls into this category.

The up-conversion architecture generally offers more diversity and control over the frequency spectrum, but at the cost of higher power since an LO must operate at the pulse center frequency. This architecture is usually found in high-data rate direct sequence communication systems, where the pulse shape and center frequency must be well-defined [24, 25].

A summary of recently published pulsed-UWB transmitters is given in Table 1.3. It is interesting to note that the data rate of these transmitters varies from 1Mb/s to 2Gb/s. This goes to show the wide range of applications that UWB is being used for. Also note that for over three orders of magnitude in data rate, and various modulation techniques, the energy/pulse remains roughly in the 100pJ/pulse range.

Table 1.3: Performance summary of UWB chipsets

Specification	[30]	[20]	[11]	[24]	[31]	[32]	This work Chapter 4	This work Chapter 5
PRF	400MHz	1MHz	1.4GHz	1GHz	80MHz	499.2MHz	100MHz	16.7MHz
Bandwidth	2GHz	1.25GHz	1.6GHz	1.5GHz	3.5GHz	500MHz	528MHz	550MHz
Center frequency	4.1GHz	6.2GHz	4.1GHz	4GHz	3GHz	multi	multi	multi
Energy/pulse	190pJ	240pJ	56pJ	105pJ	125pJ	40pJ	313pJ	43pJ
Modulation	PPM	n/a	BPSK	QPSK	PPM+ BPSK	PPM+ BPSK	BPSK	PPM+ DB-BPSK

[32] does not include power consumption of the power amplifier.

This shows how UWB gracefully UWB transmitters can scale power consumption with data rate. This scaling is not seen in radios that require a LO and PLL, where energy/bit typically increases as data rate is reduced because the constant power electronics remain on for longer periods of time.

1.5 Thesis Contributions

This thesis covers several aspects of pulse generation and transmitter implementation for pulsed ultra-wideband communication. The broad theme of this thesis is to explore tradeoffs that can be made in the pulse shaping in order to reduce energy consumption. The task can be broken up into the following contributions.

1. *Analysis of Pulse Shapes* – In order to understand the tradeoffs of pulse generators, a rigorous analysis on several pulse shapes is performed. This analysis compares several performance metrics of pulse shapes, and how overall system performance is affected. This analysis also includes a summary of FCC regulations and their implications on transmitter specifications.

2. *Gaussian Pulse Approximation* – Spectral efficiency and pulse localization in the time and frequency domains is critical for high data rate pulsed-UWB transceivers. The Gaussian pulse shape offers the best combination of these metrics; however, the Gaussian shape is nontrivial to generate with low power and high bandwidths. A technique for generating pulses that accurately approximates a Gaussian shape is presented the does not compromise spectral

efficiency or matching between BPSK pulses. This is performed by exploiting the exponential properties of a BJT. The proposed pulse shaping technique has been demonstrated in a fabricated test chip that was designed for use in a 100Mb/s transceiver.

3. *All-Digital Pulse Generation* – The available bandwidth in the UWB band far exceeds what is required for low data rate applications. UWB transceivers may capitalize on this fact by relaxing the specifications on frequency precision in order to reduce the energy/bit of the system. This approach has been applied to develop an all-digital UWB transmitter architecture that supports programmable pulse widths and center frequencies, without requiring an RF local oscillator. The transmitter has been demonstrated in a fabricated test chip in 90nm CMOS. This transmitter is designed using only full-swing static CMOS circuits, and no analog biases are required. A digital calibration technique is also demonstrated to calibrate the pulse spectrum.

4. *Delay-Based BPSK Modulation* – For some forms of UWB modulation, the spectrum produced will contain tones even when modulated by purely random data. Spectrum scrambling is therefore required, and the most common technique used combines BPSK scrambling with other forms of UWB modulation to eliminate all tomes. BPSK is costly to implement in an all-digital architecture. A spectrum scrambling technique is proposed that is suitable for digital transmitter architectures, and produces the same scrambling effect as BPSK in the main lobe of the spectrum. This technique is also suitable for replacing BPSK as the sole pulse modulation in a coherent transceiver.

Chapter 2

Pulse Shaping

In allowing UWB communication in the 3.1-10.6GHz band, the FCC placed restrictions on measuring a UWB transmitter's output spectrum that make characterizing the transmitter nontrivial. This chapter presents an analysis of the FCC regulation hurdles, and details how the measurements were taken for the custom transmitters presented in the following chapters. This analysis is relevant because measurement results of pulsed signals may vary widely, even by as much as 11dB [4], depending on the measurement technique. This chapter also presents a comparison of several pulse shapes that are considered for UWB communication, and why the Gaussian and square pulse shapes are used in the custom transmitters.

2.1 Pulse Modulation Schemes

Several pulse-based modulation schemes are found in literature such as pulse amplitude modulation (PAM), on-off keying (OOK), pulse position or bit position modulation (PPM or BPM), binary phase shift keying (BPSK), and transmitted reference [33]. BPSK has an advantage over pulse amplitude and position modulation due to an inherent 3dB increase in separation between constellation points, as shown in Figure 2-1. In a study of UWB SISO and MIMO systems employing direct sequence (DS) BPSK, time hopping (TH) BPSK, and TH-PPM, the two BPSK systems always outperformed the TH-PPM system. In the single user case, TH-BPSK and DS-BPSK

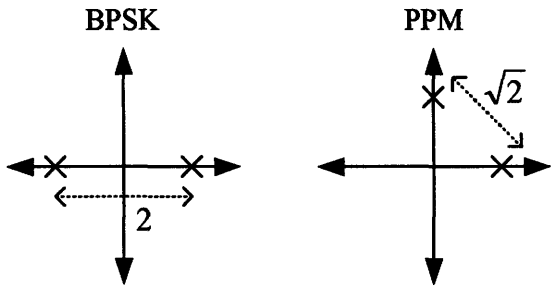

Figure 2-1: Constellations for BPSK and PPM modulation.

showed similar performance, while in the multi-user case, DS-BPSK outperformed both time hopping schemes [34].

The high data rate transmitters presented in Chapters 3 and 4 use BPSK modulation with a coherent receiver. BPSK was chosen in order to minimize losses in the link budget, to obtain the maximum distance at 100Mb/s. The low data rate transmitter presented in Chapter 5 uses PPM modulation with a non-coherent, energy detection receiver. PPM was chosen to achieve the lowest energy/bit transceiver because this form of modulation relaxes several transmitter and receiver specifications, reducing the total power consumption.

2.2 Pulse Shape Analysis

There are several pulse shapes found in literature for UWB communication, ranging from spectrally inefficient [7, 35–37], to precisely controlled frequency tolerance [24, 38]. The optimal choice of a pulse shape depends not just on the pulse time and frequency response, but also on the application. This section analyzes the pulse shapes commonly found in literature, and motivates the choice of pulses for the custom transmitters presented in later chapters.

2.2.1 Pulse Metrics

The performance in terms of BER has been analyzed for a range of pulse shapes and modulation techniques [34,39,40]. However, for linear receivers, the performance can

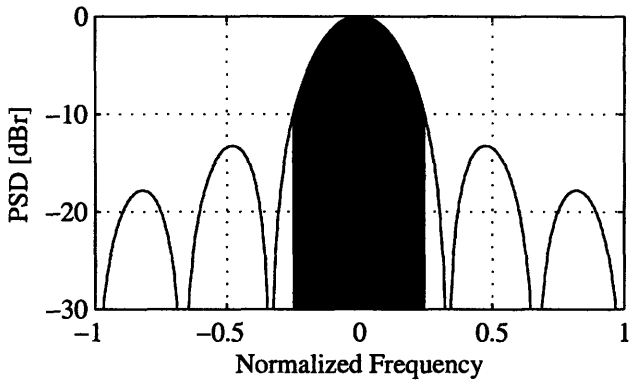

Figure 2-2: Spectral efficiency of a square pulse. The shaded area represents the pulse energy within the -10dB bandwidth (E_{ch}).

be completely characterized by signal to noise and interference ratios [41]. Therefore, the three metrics used in this thesis to quantify a pulse shape are: spectral efficiency, out-of-band emissions, and time-bandwidth product.

1. The spectral efficiency of a pulse quantifies how well the pulse spectrum utilizes the available bandwidth. The system performance in terms of BER depends only on the received pulse's energy [41], and not on its actual shape. Therefore, given an average power limit and a -10dB channel bandwidth in the receiver, the transmitter must fill the channel spectrum as tightly as possible. The spectral efficiency of a pulse is the loss incurred from incomplete filling of the -10dB channel bandwidth, calculated by

$$\eta_{ch} = \frac{E_{ch}}{P_{EIRP} BW_{-10dB}} \tag{2.1}$$

where E_{ch} is the pulse energy within the -10dB channel bandwidth, P_{EIRP} is the maximum average power spectral density in W/MHz, and BW_{-10dB} is the -10dB bandwidth in MHz.

2. The out-of-band emissions metric of a pulse is the ratio of energy outside the -10dB channel to the energy within the -10dB channel, shown in Figure 2-2. Note that this is not the ratio of out-of-band energy to total pulse energy. This

metric is used to analyze adjacent channel interference, and is calculated by

$$\eta_{out} = (E_{tot} - E_{ch})/E_{ch} \tag{2.2}$$

where E_{tot} is the total pulse energy given by

$$E_{tot} = \int_{-\infty}^{\infty} p(t)^2 dt. \tag{2.3}$$

3. The time-bandwidth product is a figure of merit of the localization of a pulse in both time and frequency. The lower this number, the more localized a pulse is in both time and frequency, which generally produces the best combination of performance in both the time and frequency domains. The time-bandwidth product is calculated by

$$B_{t\omega} = D \cdot d \tag{2.4}$$

where

$$D^2 = \frac{1}{2\pi E} \int_{-\infty}^{\infty} \omega^2 |F(\omega)|^2 d\omega \tag{2.5}$$

and

$$d^2 = \frac{1}{E} \int_{-\infty}^{\infty} t^2 |f(t)|^2 dt. \tag{2.6}$$

$F(\omega)$ is the Fourier transform of the pulse, and $f(t)$ is the pulse in the time domain [42, 43]. E is the pulse energy, calculated by

$$E = \int_{-\infty}^{\infty} |f(t)|^2 dt = \frac{1}{2\pi} \int_{-\infty}^{\infty} |F(\omega)|^2 d\omega. \tag{2.7}$$

The definitions of the Fourier transform used for these equations are

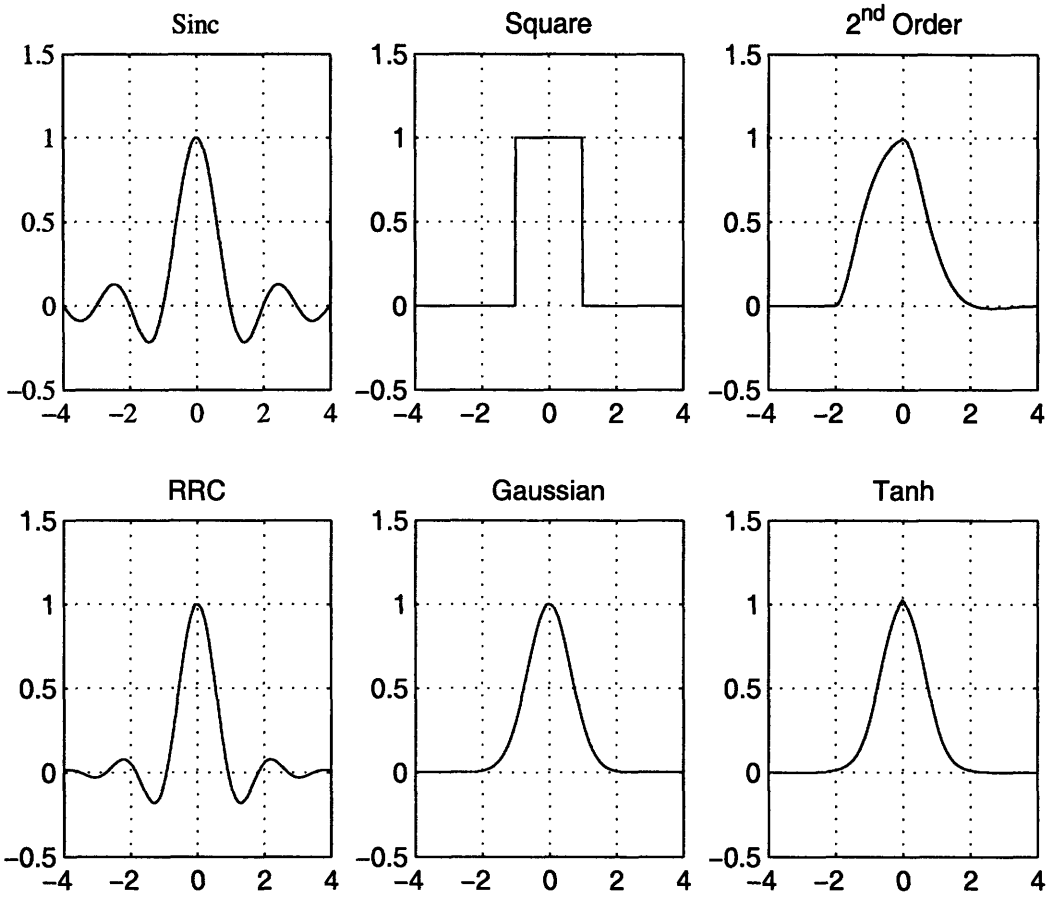

Figure 2-3: Normalized time domain plots of the six pulse shapes analyzed.

$$F(\omega) = \int_{-\infty}^{\infty} f(t)e^{-j\omega t}dt \tag{2.8}$$

and

$$f(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} F(\omega)e^{j\omega t}d\omega. \tag{2.9}$$

2.2.2 Pulse Shapes

The time domain pulse shapes considered are the *sinc*, *square*, 2^{nd} *order filtered*, *root-raised cosine* [44, 45], *Gaussian*, and *tanh*. Time domain plots of these pulses are shown in Figure 2-3. The *sinc* and *square* pulses represent the extremes in frequency and time limited pulses, respectively. The 2^{nd} *order filtered* pulse is a square pulse

filtered by a 2^{nd} order low-pass filter, represented by

$$H_{2nd}(s) = \frac{1}{(s/\omega_n)^2 + 2\zeta s/\omega_n + 1} \tag{2.10}$$

where $\zeta = 0.8$ and $\omega_n = 4/PW$ where PW is the width of the square pulse. These values were calculated to minimize the mean squared error (MSE) between the 2^{nd} *order filtered* pulse and a *Gaussian* pulse. *The root-raised cosine* pulse is represented by

$$p_{RRC}(t) = \begin{cases} 1 - \alpha + 4\frac{\alpha}{\pi}, & t = 0 \\ \frac{\alpha}{\sqrt{2}}[(1 + \frac{2}{\pi})sin(\frac{\pi}{4\alpha}) + (1 - \frac{2}{\pi}cos(\frac{\pi}{4\alpha}))], & t = \pm\frac{T}{4\alpha} \\ \frac{sin(\pi(1-\alpha)t) + 4\alpha t(cos(\pi(1+\alpha)t)}{\pi t(1-(4\alpha t)^2)}, & \text{for all other } t \end{cases} \tag{2.11}$$

where T is the symbol period, and α is the excess bandwidth parameter [44, 45]. For example, the DS-UWB proposal specifies that $\alpha = 0.3$ [11]. The *Gaussian* pulse is a standard Gaussian shape with no differentiation. The *tanh* pulse is the pulse shape specified for the custom pulse generator described in Chapter 4. The *tanh* pulse is designed to minimize the MSE between it and the Gaussian pulse.

This section considers only pulse shapes with spectral content at DC under the assumption that these baseband pulses will be up-converted to the UWB band. A separate class of pulse generators exists that generate higher-order pulses with a spectrum that directly falls in the UWB band [28, 29, 35, 46]. This approach offers no frequency diversity for avoiding in-band interference and therefore these pulse shapes are not considered in this analysis.

2.2.3 Results

The three performance metrics are summarized in Table 2.1 for the six pulse shapes. The *sinc* and *root-raised cosine* pulses have the highest spectral efficiencies, but require the most complex transmitter to generate. The *square* pulse is the simplest

Table 2.1: Comparison of pulse shapes.

	Spectral Efficiency	Ouf-of-Band Emissions	Time-BW Product
Sinc	100% (0dB)	0% (-∞dB)	∞
Square	60.0% (-2.2dB)	12.8% (-8.9dB)	∞
2^{nd} order filtered	59.2% (-2.3dB)	2.8% (-15.6dB)	0.55
Root-raised cosine	84.6% (-0.7dB)	0.4% (-23.8dB)	0.85
Gaussian	56.5% (-2.5dB)	3.3% (-14.9dB)	0.50
Tanh	58.4% (-2.3dB)	2.7% (-15.7dB)	0.53

to generate, however it results in the highest out-of-band emissions. The *Gaussian* pulse has the lowest time-bandwidth product, which is why it is typically preferred and the most common pulse shape found in the literature. With a moderate amount of filtering of a square pulse, the 2^{nd} *order filtered* pulse and the *tanh* pulse both perform similarly to the *Gaussian* pulse.

The Gaussian pulse shape is desired for the high data rate transmitter presented in Chapter 4 because this architecture uses a tightly-spaced, 14 channel frequency plan that calls for high spectral efficiency with low inter-symbol interference (i.e. low time-bandwidth product). Because the Gaussian is a relatively complex pulse shape to generate with circuits, the tanh pulse shape is introduced in Chapter 4 which has comparable performance to the Gaussian, but significantly simplifies the pulse generation.

With the amount of bandwidth available for UWB communication, it isn't necessary that a UWB transceiver always be spectrally efficient. By adding guard bands and increasing channel spacing, more out-of-band emissions may be tolerated at the expense of maximal utilization of the entire UWB band. This tradeoff is acceptable for low to moderate data rate applications where energy efficiency is the critical design objective. This tradeoff is exploited in the low data rate architecture presented in Chapter 5, in order to reduce the total energy/bit. The transmitter uses square pulses, having the highest out-of-band emissions, but requiring the least amount of energy/pulse in circuits to generate.

2.3 Pulsed-UWB Measurements

Of the FCC regulations for UWB transmitters, the rules affecting high data rate transmitters are a minimum -10dB bandwidth of 500MHz and a maximum average power spectral density of -41.3dBm/MHz [1]. The measurement of average power spectral density has several requirements on the measurement setup specified by the FCC that alter the results. These alterations always err on the conservative side. This penalizes the transmitter, and forces designers to back off from the -41.3dBm/MHz mask. This back-off isn't usually considered in a link budget, except for within the link margin.

There is an additional FCC regulation on peak power emissions for UWB transmitters of 0dBm when measured in a 50MHz bandwidth. The peak power limit is usually not approached by high data rate transmitters; however, low data rate transmitters (i.e. less than 1Mb/s) may be limited by peak power rather than average power. The peak power measurement can depend heavily on the impulse response of the spectrum analyzer's input filters [47]. This measurement is also complicated by the specified resolution bandwidth of 50MHz. Until very recently, no commercially available spectrum analyzer could measure peak power with a 50MHz resolution bandwidth (RBW). Therefore, the FCC allows this measurement to be taken at lower RBW by scaling the peak power limit to $20\log(RBW/50)$dBm where RBW is in MHz.

The measurement procedure for pulsed-UWB signals varies from that for narrowband signals. There are two distinct regions in which the measurement results, obtained with a spectrum analyzer (SA), follow different trends for peak and average measurements of modulated and repetitive (unmodulated) pulse trains. These two regions are defined by the ratio of the SA resolution bandwidth to the PRF. One must be conscious of this ratio in order to correctly interpret measured results. The next section presents calculations for approximating spectral measurements of pulsed signals with an SA [4,47]. The expressions given are for peak and average power levels measured at the center frequency of the pulse, assuming this is the maximum value.

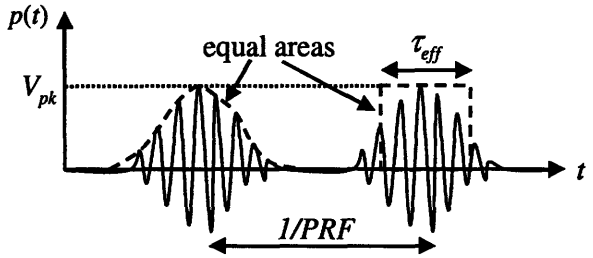

Figure 2-4: Definitions for pulse and equivalent rectangular pulse of width τ_{eff}.

These calculations are used to analyze measured results from the pulse generators in Sections 3.2.2, 4.3, and 5.6. The SA used for all measurements is an Agilent 8564EC.

2.3.1 Pulse Desensitization Correction Factor

For narrow pulses defined by a pulse width $PW < 0.1/RBW$, the intermediate frequency (IF) filter of the SA cannot completely respond to the pulse. In this case, the SA measures the pulsed response of its IF filter, rather than the pulse itself. Thus, a pulse desensitization correction factor (PDCF) is defined to relate the peak power measured by an SA to the actual peak power of the pulse [47]. There are several restrictions described in [47] on the setup of the SA to ensure accurate results when applying the PDCF.

The PDCF depends on the shape of the pulse. In order to accommodate arbitrary pulse shapes, the pulse can be approximated by a rectangular pulse with the same peak voltage and area as the arbitrary pulse shape. The effective width τ_{eff} of the rectangular pulse is calculated by

$$\tau_{eff} = \int_0^{\frac{1}{PRF}} \frac{p(t)}{V_{pk}} dt \tag{2.12}$$

where $p(t)$ is an arbitrary pulse shape, and V_{pk} is the peak voltage of the pulse as shown in Figure 2-4 [47]. The measured peak power of a pulse train without modulation is related to V_{pk} by

$$P_{pk}^{no\,mod} = 10\log\left(\frac{V_{pk}^2}{2Z_0}\right) + PDCF \tag{2.13}$$

The PDCF will be defined for the *low-* and *high*-PRF regions in Section 2.3.3, and Z_0 is the characteristic impedance.

2.3.2 Modulated Power Calculation

The average power of a pulse train modulated by a random sequence of data can also be calculated from the actual peak power of a pulse. The derivation can be readily found in communication textbooks; therefore, only the result is repeated here. The power spectral density for a 1Ω load in W/Hz is given by

$$G(f) = PRF \cdot |P(f)|^2 . \tag{2.14}$$

where $P(f)$ is the Fourier transform of the pulse voltage waveform. For the rectangular pulse with effective pulse width τ_{eff}, the average power spectral density of a modulated pulse train is calculated by

$$P_{avg}^{mod} = 10\log(\frac{V_{pk}^2}{2Z_0}) + 20\log(\tau_{eff}) + 10\log(PRF \cdot RBW). \tag{2.15}$$

In a study conducted on several UWB transmitters [4], it was reported that a measurement using an SA with an RMS average detector provides the most accurate average power reading. The RMS detector is more robust to the UWB signaling schemes than the logarithmic average typically used for narrowband average power measurements. In one case of pulsed measurements, the logarithmic average power is 10-15dB lower than the RMS average power.

2.3.3 Measurement Trends in Low/High-PRF Regions

The measurement of peak and average power for modulated and repetitive pulse trains can be divided into two regions. These are defined by the ratio of RBW to PRF being greater or less than 1. This section summarizes the measurements in these two regions. At the transition region around where $PRF = RBW$, the measured spectrum is highly dependent on the modulation and SA filter response,

and therefore more difficult to predict [4].

1. *Low-PRF Region* ($RBW/PRF > 1.7$): In this region pulses are spaced far enough apart in time to allow the output of the IF filter in the SA to return to zero between each pulse. Because of this, the peak and average measurements are independent of whether modulation by random data is applied or not, therefore $P_{pk}^{mod} = P_{pk}^{no\,mod}$ and $P_{avg}^{mod} = P_{avg}^{no\,mod}$. Average power is calculated from (2.15). The peak power in the *low*-PRF region (modulated or unmodulated) measured by the SA can be approximated by (2.13), where

$$PDCF = 20\log(\tau_{eff} \cdot RBW \cdot k_{pulse}) \tag{2.16}$$

and k_{pulse} relates the RBW frequency to an effective IF bandwidth for pulsed signals [47]. The value of k_{pulse} depends on the SA used and varies from 1.5-1.617. The peak power measurement is independent of PRF and has a 20log() dependence on RBW and τ_{eff}.

2. *High-PRF Region* ($RBW/PRF < 0.3$): In this region the RBW is narrow enough such that a "line spectrum" of impulses spaced at the PRF is visible on the SA for a repetitive pulse train of identical pulses. Peak and average power measurements are affected by modulation in this region. The average power of a repetitive pulse train is equal to the peak power, $P_{avg}^{no\,mod} = P_{pk}^{no\,mod}$. The unmodulated peak (and average) power measured by the SA can be approximated by (2.13), where

$$PDCF = 20\log(\tau_{eff} \cdot PRF). \tag{2.17}$$

$P_{pk}^{no\,mod}$ has a 20log() dependence on PRF and τ_{eff}, and is independent of RBW. For modulated signals that are similar to Gaussian noise, the measured average power is given by (2.15). The measured peak power will be $7 - 11\ dB$ above the average power level, statistically depending on the amount of time the peak

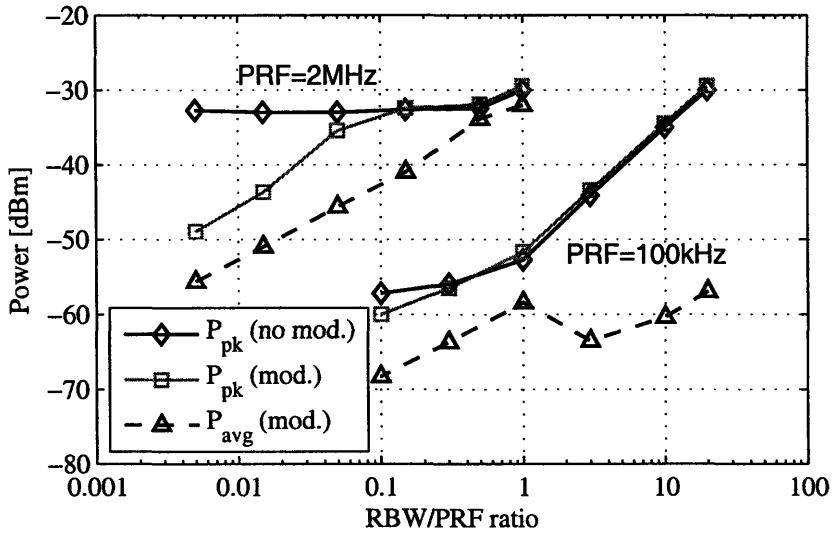

Figure 2-5: Measurements of a rectangular pulse up-converted to 5GHz with τ_{eff}=50ns and PRF=100kHz and 2MHz. For each measurement, RBW is swept from 10kHz to 2MHz.

measurement is taken over [4]. Both peak and average power of modulated signals follow a 10log() dependence on RBW and PRF in the *high*-PRF region.

2.3.4 Experimental Verification

To illustrate the measurement trends for each region, various measurements were performed on a rectangular pulse train. BPSK modulated pulses were generated with an arbitrary waveform generator and up-converted to a 5GHz center frequency, similar to the pulses shown in Figure 2-4. An instantaneous peak pulse amplitude of 50.8mV was measured with an oscilloscope. The pulse width was 50ns, which is equal to τ_{eff} since the pulse is rectangular. The RBW was varied from 10kHz to 2MHz, and the PRF varied from 100kHz to 2MHz. Plots of the measurements spanning the *low*- and *high*-PRF regions are shown in Figure 2-5.

Peak power was measured with the SA positive peak detector, a video bandwidth (VBW) of 3MHz, and a sweep time of 1s. The measurements for modulated and unmodulated peak power matched very well with the predicted values, and followed the predicted trends for varying PRF and RBW in their respective regions. Average

power was measured with the SA detector in sample mode, a VBW of 3MHz, and the sweep time set to auto. An RMS detector was not available for these measurements. The noise marker featured on the SA was used to measure the average power of the modulated signal, which is similar to Gaussian noise. This marker displays the logarithmic average of trace points around a selected frequency, and corrects for errors due to averaging, and a wider effective RBW [48]. The results matched with calculations except for the RBW/PRF > 1 region, where the power was lower than expected by up to 12dB. These results are similar to those found in [4] where the logarithmic average power was lower than the RMS average power by 10-15dB for low duty cycle, impulsive signals. Average power follows the expected 10log($PRF \cdot RBW$) trend in both regions.

2.4 Conclusions

The measurement results from a spectrum analyzer for peak and average power of modulated and unmodulated pulse trains depends on the ratio of RBW to PRF, and on the internal parameters of the spectrum analyzer. For typical high data rate transmitters, RBW/PRF $\ll 1$, and therefore peak and average power of a modulated pulse train have a 10log() dependence on PRF and RBW. Calculations of peak and average power can be made from the peak pulse voltage and an effective pulse width for an arbitrary pulse shape. The equations for calculating the powers are summarized in Table 2.2.

Three pulse metrics for qualifying a pulse shape have been presented and compared for six shapes typically found in literature. In selecting a pulse shape, these metrics should be considered, as well as the architecture of the transceiver and intended application. The available bandwidth in the UWB band is excessive for many low to medium data rate applications. The wide bandwidth can be exploited by relaxing the frequency specifications to simplify the transceiver architecture and optimize for a specification other than spectral efficiency. This is typically not true for narrowband radios where spectral efficiency is critical, and differentiates optimal UWB

Table 2.2: Summary of equations for peak and average power calculations in the low- and high-PRF regions.

Low-PRF Region ($RBW/PRF > 1.7$)	
Unmodulated	$P_{avg} = 10\log\left(\frac{V_{pk}^2}{2Z_0}\right) + 20\log(\tau_{eff}) + 10\log(PRF \cdot RBW)$ $P_{pk} = 10\log\left(\frac{V_{pk}^2}{2Z_0}\right) + 20\log(\tau_{eff} \cdot RBW \cdot k_{pulse})$
Modulated	$P_{avg} = 10\log\left(\frac{V_{pk}^2}{2Z_0}\right) + 20\log(\tau_{eff}) + 10\log(PRF \cdot RBW)$ $P_{pk} = 10\log\left(\frac{V_{pk}^2}{2Z_0}\right) + 20\log(\tau_{eff} \cdot RBW \cdot k_{pulse})$
High-PRF Region ($RBW/PRF < 0.3$)	
Unmodulated	$P_{avg} = 10\log\left(\frac{V_{pk}^2}{2Z_0}\right) + 20\log(\tau_{eff} \cdot RBW)$ $P_{pk} = 10\log\left(\frac{V_{pk}^2}{2Z_0}\right) + 20\log(\tau_{eff} \cdot RBW)$
Modulated	$P_{avg} = 10\log\left(\frac{V_{pk}^2}{2Z_0}\right) + 20\log(\tau_{eff}) + 10\log(PRF \cdot RBW)$ $P_{pk} = P_{avg} + 11dB$

$k_{pulse} = 1.5 - 1.617$

architectures from those of narrowband radios.

There is no single pulse shape or modulation that fits all applications. Pulse shapes may be compared by their spectral efficiency and out of band emissions to determine relative performances in terms of BER. For high data rate applications with multiple users, the specifications on the pulse spectrum may be strict in order to support the maximum bits/Hz in the available bandwidth. In this case, QPSK modulated Gaussian or root-raised cosine pulses may be optimal. For low data rate applications, the specifications on the pulse spectrum may be relaxed in order to reduce power consumption. In this case, a PPM square pulse may be ideal. Therefore, the choice of modulation and pulse shape should consider the target application and implications on the hardware power consumption, in addition to a typical link budget analysis.

Chapter 3

Prototyping Platform

A flexible platform for prototyping a UWB system provides several advantages over simulation alone, or iteration of a design in silicon. It offers the ability to program system specifications such as the pulse shape, ADC bit precision, or front-end non-linearities, and to measure system performance and to compare with simulations. System specifications may also be swept in the hardware using a discrete prototype for determining optimal settings for the realized transceiver. Additionally, as individual integrated circuits such as the baseband processor, ADC, or front-end are realized, the corresponding component in the discrete prototype may be substituted by the fabricated part. This enables testing each chip in a complete system, on top of verifying that the component meets its individual specifications. Therefore, the prototype is useful throughout the entire design cycle for specifying the system, verifying baseband algorithms, and testing the final integrated circuits.

This chapter describes the architecture of a highly flexible prototyping platform that was developed for the high data rate transceiver chipset in Chapter 4. The goal of this discrete prototype was to provide a modular platform primarily verification of the digital back-end algorithms and system specifications. Some experimental results are presented that demonstrate how the prototype was used for verification of the high data rate system.

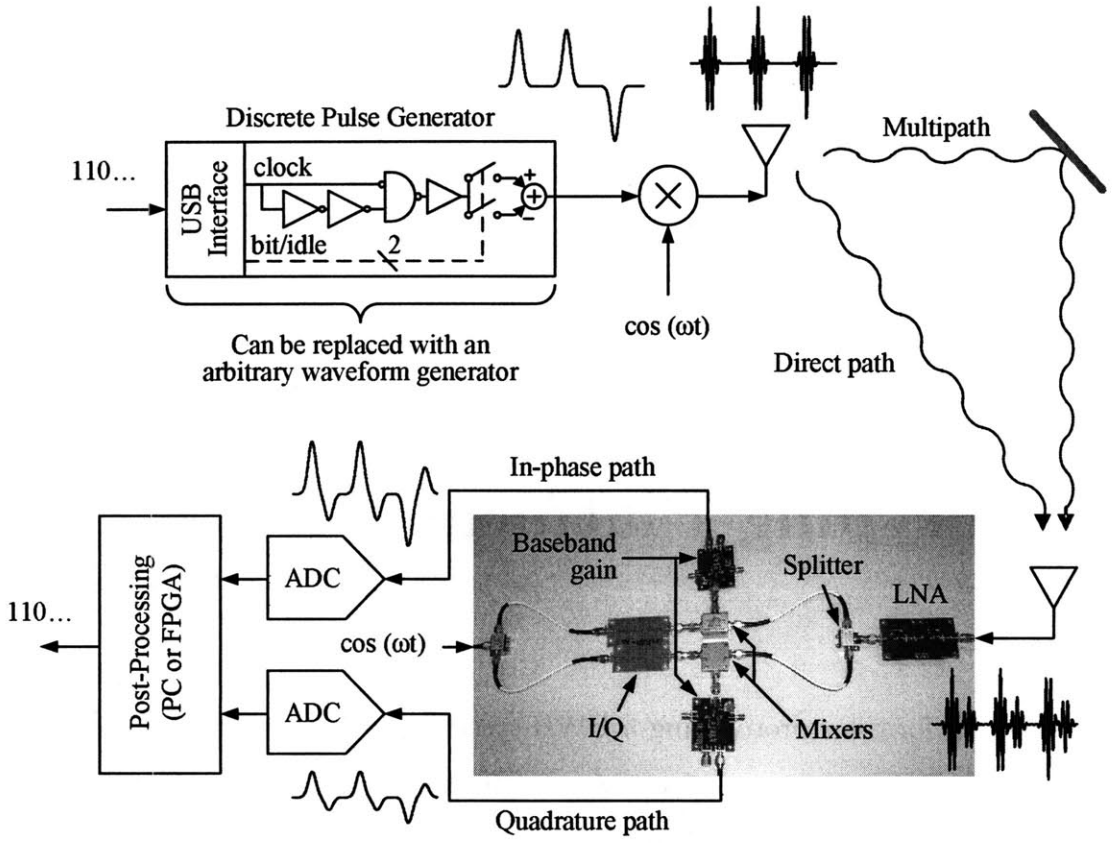

Figure 3-1: Block diagram of the discrete prototype.

3.1 Architecture

Prior to integrating the high data rate chipset in Chapter 4, a discrete prototype of the system was built using commercially available off-the-shelf components and test and measurement equipment. The prototype can be divided into three distinct sections: the transmitter, the receiver, and the ADC and baseband processing. The link between the transmitter and receiver can be made through wireless transmission using various antennas [12] and spatial configurations to emulate a wide range of channels. The transmitter and receiver may otherwise be directly connected through a cable with a variable attenuator to emulate an ideal channel with a fixed propagation loss.

A block diagram of the prototype is shown in Figure 3-1, which has an architecture that is identical to the custom chipset. Baseband pulses are generated with either an

arbitrary waveform generator (AWG) or a custom pulse generator, and up-converted to one of seven channels in the 3.1-7GHz portion of the UWB band. The channel center frequencies are $f_{center} = 2904 + 528 \cdot n_{ch}$MHz, where $n_{ch} = 1, 2, \ldots, 7$. The receiver uses an I/Q direct conversion architecture to down-convert the signals to baseband, where they are sampled by dual ADCs. Once the signal is digitized, it is post-processed either in Matlab, or in an FPGA implementing a subset of the digital back-end algorithms.

3.2 Transmitter

The transmitter has been implemented with two approaches in order to verify separate aspects of the system operation. The first implementation uses commercial test and measurement equipment for the greatest flexibility in signal generation. This setup is useful for implementing one-way communication with great flexibility and testing different pulse shapes with the system, but is limited in how fast new data can be downloaded to the instrument. In order to implement real-time communication, a dedicated pulse generator was implemented with a USB interface to a PC for streaming wireless data. This transmitter has less flexibility in the signals it could generate; however, it was useful for verifying the system works in a streaming data application.

3.2.1 Arbitrary Waveform Generator

For the most flexibility in the pulse generator, the transmitted UWB signal is synthesized using a programmable baseband arbitrary waveform generator (AWG), and a vector signal generator (VSG) as the up-conversion mixer and amplifier. The AWG has a 16MSample memory, enough to store 4 ms of data sampled at 4GS/s. The AWG enables a large amount of flexibility in the shape of the signals transmitted, the modulation scheme, and the duration of the transmission.

Matlab is used to generate the data packets, which can be modulated using either OFDM or BPSK Gaussian shaped pulses. The modulation scheme is certainly not

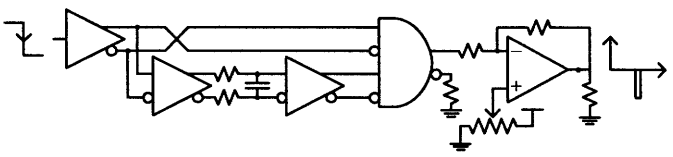

Figure 3-2: ECL pulse generator and level shifter for the discrete pulse generator. On every falling edge of the input clock, a negative pulse is generated with an effective width of $\tau_{eff} = 2.4ns$.

limited to these two. Virtually any modulation or pulse shape can be synthesized, limited only by the specifications of the AWG and VSG (500MHz analog bandwidth). Matlab may also be used to introduce non-idealities into the signal, such as gain mismatch, non-linearity, or timing jitter with 250ps resolution. In-band interferers such as 802.11a or random tones may also be added using Matlab.

3.2.2 Discrete Pulse Generator

A custom pulse generator has also been built using commercial off-the-shelf discrete components as part of the complete prototype transceiver [49]. It is designed for BPSK modulation of pulses at a variable PRF of up to 50MHz, therefore the maximum data rate supported is 50Mb/s. Pulses are up-converted to any of the channel center frequencies in the 3.1-7GHz range. Individual packets are downloaded from a PC to the transmitter's commercial FPGA board in real-time over a USB interface. Once a packet has been fully buffered in the FPGA, the bits are shifted out to the pulse generator and transmitted at 50 Mb/s.

Hardware Description

The architecture of the transmitter is similar to the custom high data rate transmitter described in Chapter 4. Baseband pulses are generated by the circuit shown in Figure 3-2, similar to [35]. A TTL-level clock operating at the PRF is converted to 3.3V ECL levels. The inverted clock and a delayed clock are inputs to an *AND* gate, the output of which is a pulse on every falling edge of the input clock. The pulse width is set by an RC filter between two ECL buffers. The output of the ECL *AND* gate is

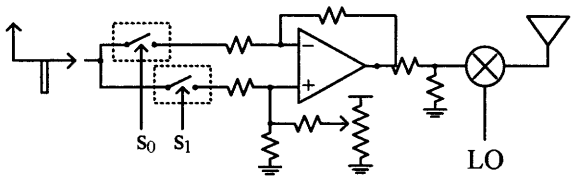

Figure 3-3: Schematic of the modulation and up-conversion circuit for the discrete pulse generator.

at 1.6-2.4V levels; therefore, a high-speed inverting level shifter is used to bring the pulse down to 0V. In later sections, the operation of the transmitter is described in more detail.

The baseband pulses are then modulated and up-converted to a center frequency of 5.355GHz using the circuit shown in Figure 3-3. Depending on the data bit, the pulse is switched to either the positive or negative input of a differentiating amplifier using high-frequency analog switches. When each switch is in the off position, it terminates the input of the amplifier to ground. Both switches are turned off to put the transmitter in an idle state outputting no pulses. This state can also be used to vary the PRF by inserting idle periods between pulses. The output of the amplifier is a BPSK modulated pulse train which is attenuated and up-converted to 5.355GHz by a passive mixer. An offset adjustment is provided at the positive input of the amplifier to correct for offsets at the input of the mixer. This adjustment is necessary to minimize LO feedthrough to the antenna.

Experimental Results

A screen capture of the discrete pulse generator in operation is shown in Figure 3-4. The top trace is the input clock of 50MHz, the two traces beneath the clock are the switch input signals S_0 and S_1. The bottom trace is the pulse train measured at the input to the mixer and after the attenuator. This pulse train is subsequently up-converted to the desired channel frequency.

The spectrum of the pulses has a -10dB bandwidth of 550MHz. The effective rectangular pulse width τ_{eff} is 2.4ns, calculated from the frequency of the first null

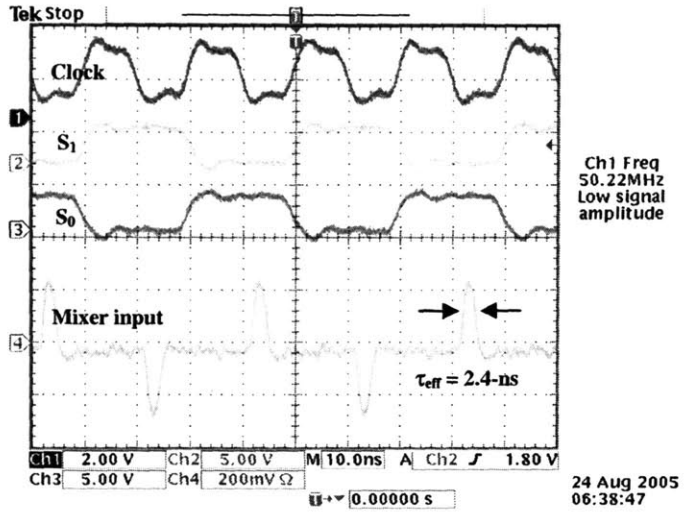

Figure 3-4: Plot of the input clock and switch signals for the discrete pulse generator at a PRF of 50MHz. The pulses are sampled at the input to the up-conversion mixer.

Table 3.1: Discrete Transmitter Measurement Results

		Measured	Calculated
High-PRF Region	Un-modulated P_{pk}	-25.9 dBm	-25.2 dBm
$PRF = 50\,MHz$	Modulated P_{avg}	-43.4 dBm	-42.2 dBm
$RBW/PRF = 0.02$	Modulated P_{pk}	-32.2 dBm	-31.2 dBm
Low-PRF Region	Un-modulated P_{pk}	-54.1 dBm	-55.0 dBm
$PRF = 50\,MHz$	Modulated P_{avg}	-73.8 dBm	-72.2 dBm
$RBW/PRF = 20$	Modulated P_{pk}	-53.5 dBm	-55.0 dBm

in the measured spectrum by $\tau_{eff} \approx 1/(f_{1st\,null} - f_{center})$. The peak voltage of the up-converted pulse is 104mV. These measured values were used in the equations from Section 2.3 to generate the calculated peak and average power levels, which are compared to the spectrum measurements in Table 3.1. The peak and average modulated measurements were taken with the transmitter outputting 250kb of pseudo-random data. Measurements were made at a 50MHz and 50kHz PRF to demonstrate the accuracy of the calculations in the *low-* and *high*-PRF regions.

3.3 Receiver

The RF front-end was designed by Fred Lee and built entirely using discrete components [50]. As shown in Figure 3-1, the received signal is amplified by two cascaded LNAs, then the signal is split and applied to two identical passive mixers performing I/Q direct conversion. The 90° phase shift in the local oscillator (LO) is implemented with a commercial phase splitter that operates over the 3-7GHz range. A fixed delay between I and Q LO paths has also been used to generate the 90° phase shift at a single frequency. The advantage of this approach is it also allows for tuning of the I/Q phase error simply by tuning the RF center frequency. Tunable phase error is desirable in the prototype for testing the robustness of the digital back-end algorithms to I/Q phase offset. After I/Q down-conversion, the baseband signals are filtered and amplified with digitally controlled gain before being digitized.

3.4 ADC and Baseband Processing

Baseband sampling and processing can be performed with one of two methods that both use commercially available equipment. In the first method, the baseband I and Q signals are sampled by an 8-bit, 1 GS/s ADC board that interfaces directly to a PC through a PCI slot. The samples are captured to a file, and the baseband processing is implemented in Matlab. The key specifications of an ADC are its sampling rate, number of bits, and full scale input voltage. The implemented flexible platform allows testing of all three of these parameters. This ADC and baseband implementation was used to verify acquisition and fine tracking loops, channel modeling and estimation, and demodulation in the digital back-end. This implementation, however, lacks a real-time implementation.

The second method for baseband sampling and processing uses a commercially available dual-ADC and FPGA board stack. The I and Q baseband signals coming from the RF front-end are sampled using two synchronized 500MS/s ADCs. These ADCs can provide 8-bits per channel, but for the demodulation process only the

4 most significant bits are used. These samples are parallelized as vectors of four consecutive complex samples synchronized with a 125 MHz clock, and routed to an FPGA with an effective number of gates of 1 million.

The FPGA included in the UWB development platform allows testing of different architectures for the reception of UWB wireless signals. Although the system is fully programmable, the maximum number of gates in the FPGA sets a bound on the functionality that can be implemented within it. It is usually only possible to use less than 70% of the gates in the FPGA in order to avoid serious routing problems. Implementing a debugging procedure requires on the order of a 30% of the FPGA gates in auxiliary circuitry. That leaves a 40% of the FPGA available for actual receiver circuits. The signal processing that may be implemented in this FPGA is reduced because of these constraints. The limited signal processing impacts the time to achieve coarse acquisition and the complexity of the compensation incorporated for multipath channels.

3.5 Range of Applicability

Several of the components of the discrete prototype are controlled remotely by a PC communicating over a GPIB bus. This enables automated control of many system specifications set by the hardware. In addition, the baseband processing is implemented in Matlab or in an FPGA and therefore is entirely flexible. The sections that follow highlight examples of how the discrete prototype can be programmed to emulate a range of UWB systems and specifications.

3.5.1 System Performance

Several of the concepts developed in the previous sections may be tested using the prototype. For example, the trade-off between quality of service and signal processing complexity may be evaluated, as well as how this trade-off depends on the channel quality. Figure 3-5 shows a plot in which the impact of the number of bits used to represent the channel impulse response is plotted for two different channels. On the

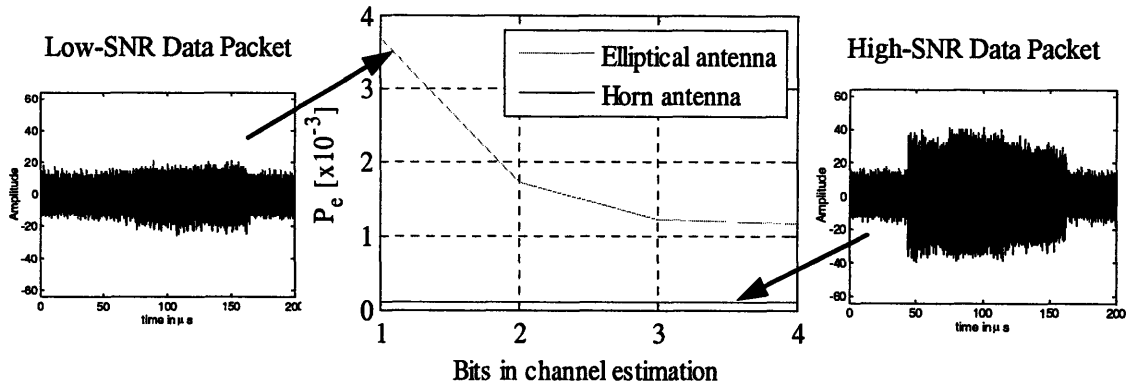

Figure 3-5: Effective probability of error for transmission with two different antennas measured using the discrete prototype.

top curve, an isotropic antenna [12] is used that allows multipath to be captured (similar to an antenna that a WPAN device would use). The duration of the impulse response measured with this antenna is 20ns, which includes echoes from reflectors in the channel. A decrease in the probability of error is obtained as the number of bits of the representation of the channel increases [51]. The low SNR of this channel emphasizes the effect. The lower curve represents the case in which both transmitter and receiver are using a directional horn antenna with 13dB of gain in the direct path, and no significant echoes. The higher SNR combined with the presence of only a clear direct path makes the performance for this kind of channel independent of the number of bits used to represent the channel impulse response. Both curves were obtained using measured data and a MLSE of four states. The presence of the MLSE improved the performance of the transceiver by reducing bit errors in the multipath channel.

These two experiments have shown that it is possible to trade off complexity of the signal processing with quality of service, but that this trade-off is only relevant if the channel quality is known. For some situations it is possible to reduce the complexity of the signal processing to the minimum.

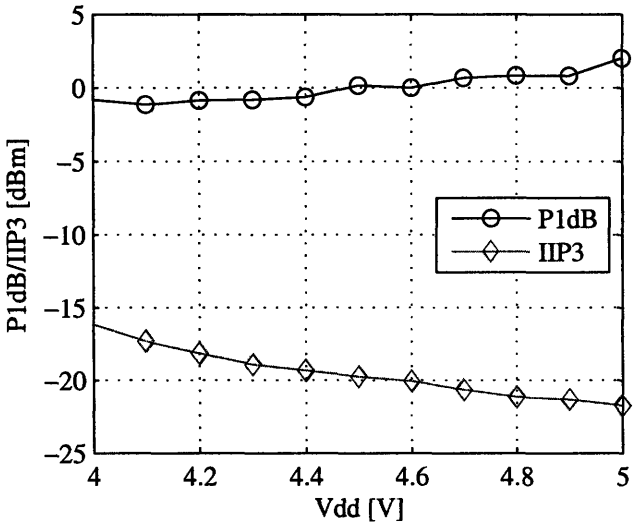

Figure 3-6: Measured programmable IIP3 and P1dB in the discrete LNA.

3.5.2 Receiver Non-Linearity

Figure 3-6 shows an example of how the IIP3 and P1dB performance metrics of the cascaded LNAs can be programmed by setting the power supply voltage accordingly. Some specifications, such as IIP3, P1dB, and LNA gain, are highly correlated with supply voltage and cannot be independently set. Consequently, other components are tuned to compensate. Adjusting the gain of the higher-linearity baseband stages allows for independent control of LNA non-linearity and overall receiver gain.

3.5.3 OFDM or Pulse-Based Platform

The architecture of this platform is very similar to the WiMedia OFDM architecture. Because a 4GS/s DAC is used to synthesize the baseband signal that is in turn up-converted to the UWB band, many forms of modulation can be used, limited only by the 500MHz analog bandwidth of the mixer input. In particular, OFDM and pulse-based modulation schemes are interesting because these are two competing technical approaches for short range, high data rate communication. The prototype platform is versatile enough to support both technical approaches, as shown in Figure 3-7.

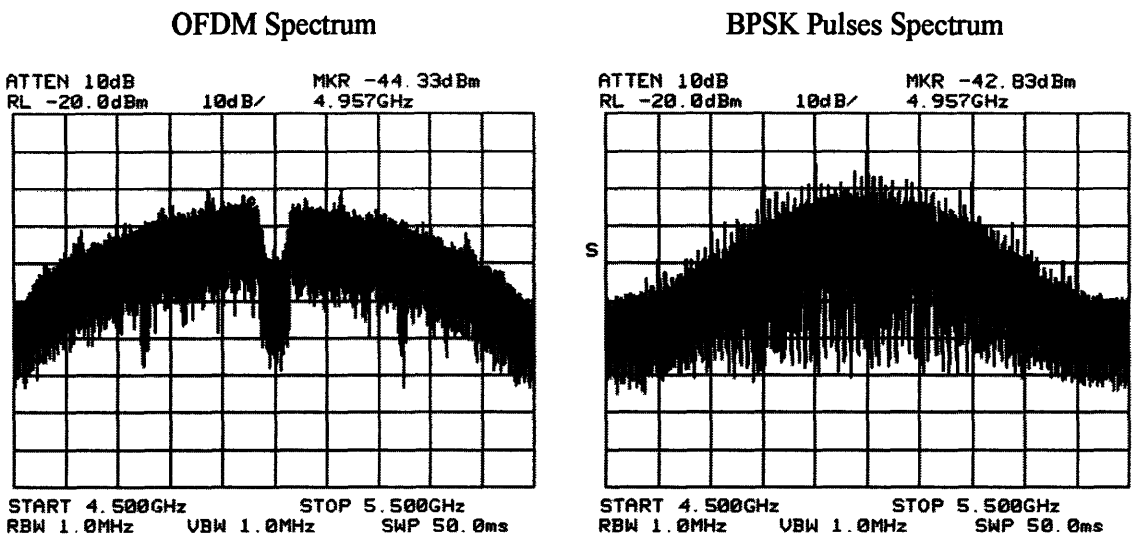

Figure 3-7: Measured OFDM and BPSK pulses spectra that were generated using the AWG.

Figure 3-7 (left) shows the measured spectrum of the discrete prototype transmitting a complete WiMedia Multiband OFDM Alliance (MBOA) [10] packet. Figure 3-7 (right) shows the transmitted spectrum of a Gaussian-shaped pulse, modulated by BPSK with a random sequence of bits.

3.5.4 Phase and Frequency Offsets

The discrete prototype may be used to evaluate the system's robustness to timing non-idealities such as jitter or offset in the pulse repetition frequency (PRF), offsets in the RF carrier frequency, or I/Q mismatch in the receiver. The latter is demonstrated in Figure 3-8. These two plots are a subset of received I and Q data for a pulse-based UWB packet, normalized to the ADC full-scale voltage. Plotting I and Q data against each other would ideally trace a perfect circle. The data on the left was taken from the discrete prototype with balanced I/Q. The data on the right was taken with a 11.7° phase imbalance between I and Q. This I/Q imbalance is programmable in the discrete prototype.

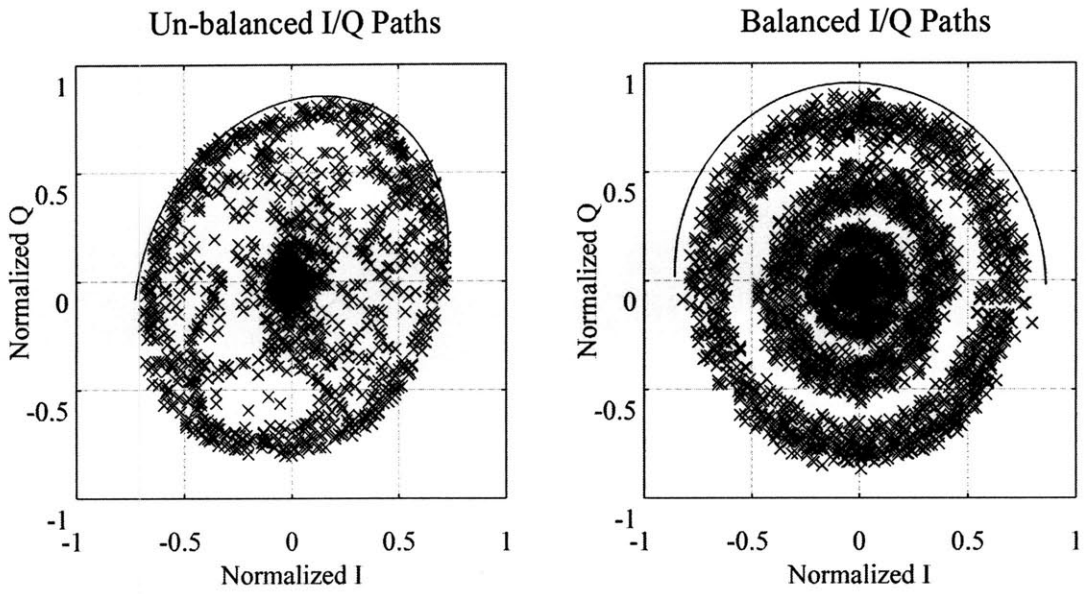

Figure 3-8: Example of I/Q path balancing measured using the discrete prototype.

3.5.5 Analog to Digital Converter

The implemented flexible platform allows testing of three performance specifications of the ADC. These are its sampling rate, number of bits, and full scale input voltage. The maximum sampling rate of the ADC board is 1 GHz for both channels, while the maximum input frequency of the I and Q channels is 250 MHz. This allows a direct comparison between Nyquist sampling and oversampling by 2 with a decimation filter for a constant sample rate output of the ADC. This comparison is particularly useful in determining anti-alias filtering requirements for the sampling operation. The anti-alias filter in this implementation is formed from the low-pass filtering inherent in the front-end plus an additional variable cutoff low-pass filter on the ADC board. Nyquist sampling was used in the final implementation.

The ADC output is always set at 8 bits, but post-processing is done to reduce this to any number of bits up to 8, and see its effect on the overall system performance (in particular, the BER). Specific non-linearities can be generated in the mapping of 8-bit to lower resolutions to test the effect of these non-linearities on overall system performance.

Finally, the input full scale voltage is variable on the ADC board from 100mV

to 5V. Changing the full scale input directly changes the requirements of the analog front-end; effectively, the full scale input determines the partition between ADC preamp gain and the gain of the amplifier chain in the receiver front-end.

3.6 Summary

A modular prototyping platform realized with discrete components and commercial test and measurement equipment assists in the design and verification of hardware, baseband processing algorithms, and models for UWB systems. The prototype uses an architecture identical to the high data rate UWB system presented in Chapter 4. This way, as the custom ICs become available, they can be individually demonstrated in a UWB system by substituting into the discrete prototype.

Chapter 4

High Data Rate Transmitter

One promising application for UWB communication that is being considered by the integrated circuits community is high data rate, last-meter wireless links such as wireless USB or streaming video. With this application space in mind, a 100Mb/s UWB transceiver has been developed as a joint project with other students [19]. This chapter begins by introducing the transceiver architecture, and then presents the transmitter designed for this transceiver as a contribution to this thesis.

A technique for generating pulses that accurately approximates a Gaussian shape is presented in this chapter. A near-Gaussian pulse is shaped from a triangle input signal by exploiting the exponential properties of a BJT. The proposed pulse shaping technique has been demonstrated in a fabricated test chip that was designed for use in the 100Mb/s transceiver. This chapter presents an analysis and optimization of the hyperbolic tangent pulse shaping technique, the architecture of the test chip, and measured results.

4.1 System Architecture

The UWB transceiver architecture uses a pulse-based, binary phase-shift keyed (BPSK) communication scheme where information is encoded as a pulse with either positive or negative polarity [52]. A baseband pulse train is up-converted to one of 14 channels with 528 MHz spacing in the 3.1-10.6 GHz UWB band. This frequency plan has been

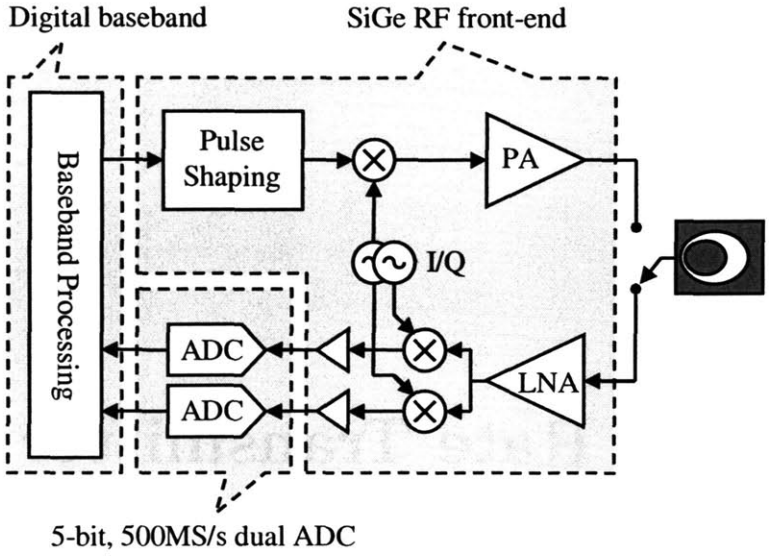

Figure 4-1: Block diagram of the high data rate, fourteen channel UWB system architecture.

adopted from the WiMedia MBOA specifications for wireless USB using UWB, with the exception that fast frequency hopping is not implemented [10]. The maximum pulse repetition frequency (PRF) supported is 100MHz. During the payload of each packet, data is represented by one pulse per bit. Therefore, a maximum data rate of 100Mb/s can be achieved. Each packet contains a preamble in which a 31-bit CDMA code is transmitted. This code is repeated to allow the receiver to synchronize to the packets and perform channel estimation.

A block diagram of the transceiver architecture is shown in Figure 4-1. The transmitter generates a baseband BPSK modulated train of Gaussian pulses, and up-converts it to one of the 14 channels in the UWB band. The receiver performs I/Q direct conversion to baseband, where the received signal is sampled by dual 5-bit, 500MS/s ADCs. Coarse acquisition, channel estimation, fine tracking, and demodulation are all performed in the digital back-end. A mostly-digital architecture was chosen for greater flexibility, however performing correlations in the analog domain can result in lower power [53].

During acquisition, the receiver averages 31 received pulses to perform channel estimation. This averaging of pulses produces a single template of the received pulses

to be used in the rake receiver. Under the assumption that positive and negative pulses are exactly equal and opposite, the receiver uses the template pulse and its inverse when correlating with a BPSK signal and demodulating data. For this reason, amplitude and timing matching between positive and negative pulses are critical to the quality of service. Any mismatch in shape or total energy between a positive pulse and negative pulse (for BPSK modulation) manifests itself as an offset in the receiver. The linearity requirement in the transmitter is relaxed since the pulse shape is learned before demodulation. However, non-linearities in the transmitter will cause spurious emissions, which can cause adjacent channel interference or exceed the FCC spectral regulations.

4.2 Related Work on UWB Transmitters

The Gaussian pulse cannot be generated with passive components alone, since it is an exponential shape, and digital filtering implies pulse synthesis which is power hungry at UWB bandwidths. Previous work shows that the Gaussian pulse shape can be approximated by direct synthesis, step recovery diodes [6], cascaded filters [26], or other approximations [25, 54].

The tanh pulse shaping technique proposed in this chapter relies on the exponential current-to-voltage relationship of a BJT differential pair. The exponential behavior of a differential pair has been used in waveform generation for decades. A popular triangle-sine wave converter achieving 0.2% THD using a single differential pair was first published in 1976 [55]. Trans-linear circuits also rely on this relationship [56]. Additionally, a need exists for simple, accurate Gaussian shaping circuits in neural networks, not for generating pulses, but as a radial basis function that maps a DC input voltage or current value onto a Gaussian curve [57–60]. The circuits used in neural networks to generate the Gaussian curve have been carried over to UWB pulse generation by increasing the operating bandwidth of the circuits and applying transient inputs [7, 36, 54, 61]. This approach has limitations in matching BPSK pulses, and suffers from spurious emissions that are generated during a resetting phase of the

pulse shaping circuits.

Other UWB pulse generators have been published that seek to approximate the Gaussian shape. Pulse generators have been proposed that approximate a 2^{nd} derivative Gaussian pulse using four NPN differential pairs [7], or by using a squaring circuit, weak-inversion CMOS device, and 2^{nd} order filter for differentiating [36]. These pulse generators rely on ramp input signals, and generate pulses on both the positive and negative slopes of the ramp input. Either a reset phase is required that may produce unwanted transient signals, or a pulse is intentionally generated on both slopes of the input signal. Due to mismatch in the ramp generation or in the pulse-shaping circuit, the positive and negative ramping pulses will not be symmetric. This form of mismatch is problematic in the digital back-end that is demodulating the signal, and manifests itself as an offset in the received signal.

The pulse generator in [54] uses vertical PNPs in a 0.18μm CMOS process to generate a 2^{nd} derivative Gaussian approximation. This transmitter approximates a Gaussian with the $sech^2$ function, generated from a tanh input signal and trans-linear squaring circuit using the identity $sech^2 = 1 - tanh^2$. The Gaussian pulse is differentiated twice by a 2^{nd} order filter, and the output is an approximate 2^{nd} derivative Gaussian pulse. This transmitter requires a reset phase, otherwise pulses are generated on the rising and falling edges of the input. This technique for shaping pulses is affected by temperature variations; therefore, a temperature-compensated version of this is pulse generator has also been presented [61].

4.3 Integrated Tanh Pulse Generator

A transmitter has been fabricated in a 0.18μm SiGe BiCMOS process as part of the custom chipset for a 100Mb/s pulse-based UWB transceiver discussed in Section 4.1 [52, 62]. The goal of this work was to design a low-power UWB transmitter that emits Gaussian shaped pulses due to their desirable time and frequency response. By exploiting the exponential behavior of a BJT, the Gaussian pulse can be accurately approximated with an elegant analog circuit that simultaneously performs

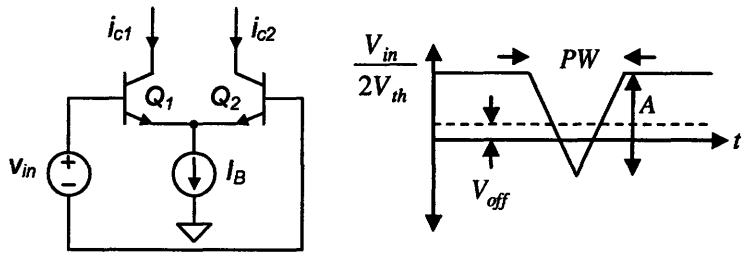

Figure 4-2: BJT differential pair and input voltage waveform for generating a tanh pulse.

up-conversion mixing to the 3.1-10.6GHz band. Pulses are up-converted to one of 14 channel center frequencies. The center frequencies are set by

$$f_{center} = 2904 + 528 \cdot n_{ch}\ [MHz] \tag{4.1}$$

where $n_{ch} = 1, 2, \ldots, 14$.

4.3.1 Tanh Pulse Shaping

The transmitter uses a differential pair of BJTs with a triangle signal input to generate and shape a pulse of one polarity, shown conceptually in Figure 4-2. For the proper choice of A, PW, and V_{off}, the current i_{C2} will have a shape that approximates that of a Gaussian.

For a fixed bias current I_B, the collector currents in the differential pair are approximately related by $I_B = i_{C1} + i_{C2}$. By substituting terms into the exponential equations for the collector current of a BJT, it can be shown using hyperbolic identities that the collector current i_{C2} is described by

$$i_{C2} = \frac{1}{2} I_B [1 - tanh(V_{in}/2V_{th})] \tag{4.2}$$

where V_{th} is the thermal voltage, equal to kT/q.

The output current i_{C2} of the differential pair will be a pulse with tanh-shaped rising and falling edges for the triangle input signal shown in Figure 4-2. Note that the y-axis is normalized to V_{in}/V_{th}, the argument of the tanh function in (4.2). Current i_{C1}

is not used, and can be terminated to the power supply. The pulse is simultaneously up-converted to the UWB band by additionally modulating the tail current I_B with an LO. Furthermore, BPSK pulses are generated by inverting the LO signal in the tail current.

This architecture has several benefits: 1) The input signal begins and ends at the same level; thus, there is no "reset" phase required as in differentiating pulse generators, eliminating transients. 2) Positive and negative pulses can be generated with the same triangle input signal and inverted LO to improve matching between BPSK pulses, which is difficult to achieve with complementary circuits. 3) Up-conversion is performed by adding an LO signal to the tail current I_B; thus, no additional mixer is required. 4) The triangle signal can be generated with well-known techniques, and the accuracy of the Gaussian approximation is not sensitive to small deviations in the values of A and PW.

4.3.2 Optimization

The optimal values for A, PW, and V_{off} were found by sweeping each variable and searching for the minimum mean squared error (MSE) between the resulting tanh-shaped pulse and the Gaussian pulse given by

$$V_{Gauss} = V_p e^{-t^2/2\sigma^2}. \tag{4.3}$$

The energies of the two pulses are equalized before calculating the MSE. A contour plot of the MSE is shown in Figure 4-3 for $V_{off} = 1.0$ and $\sigma = 1.0$. The diamond indicates the values of A and PW resulting in the minimum MSE. A plot of the corresponding tanh-shaped pulse for the minimum MSE point is compared with a Gaussian reference pulse in Figure 4-4. The time and frequency domain responses are shown. The side lobes of the tanh-shaped pulse are 45dBr from the main lobe. The results of the parameter optimization are as follows.

1. *Normalized Amplitude A*: The amplitude normalized to $2V_{th}$ does not vary with σ, and varies linearly with V_{off} for $V_{off} > 1.0$. The equation for setting A is

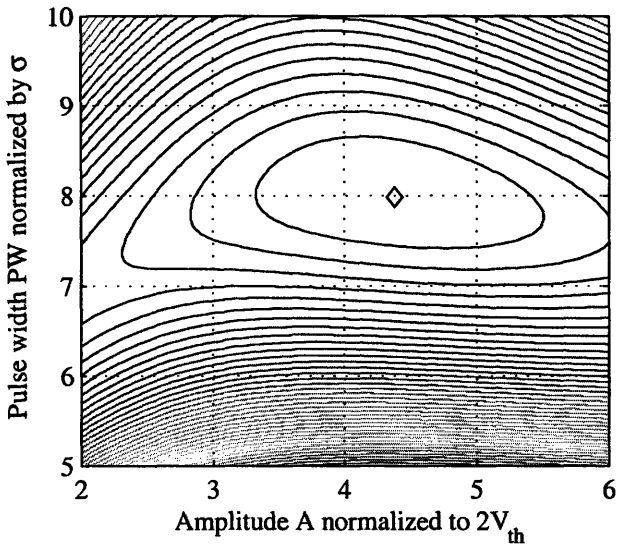

Figure 4-3: Mean squared error contours and minimum error point for $\sigma = 1.0$, $V_{off} = 1.0$.

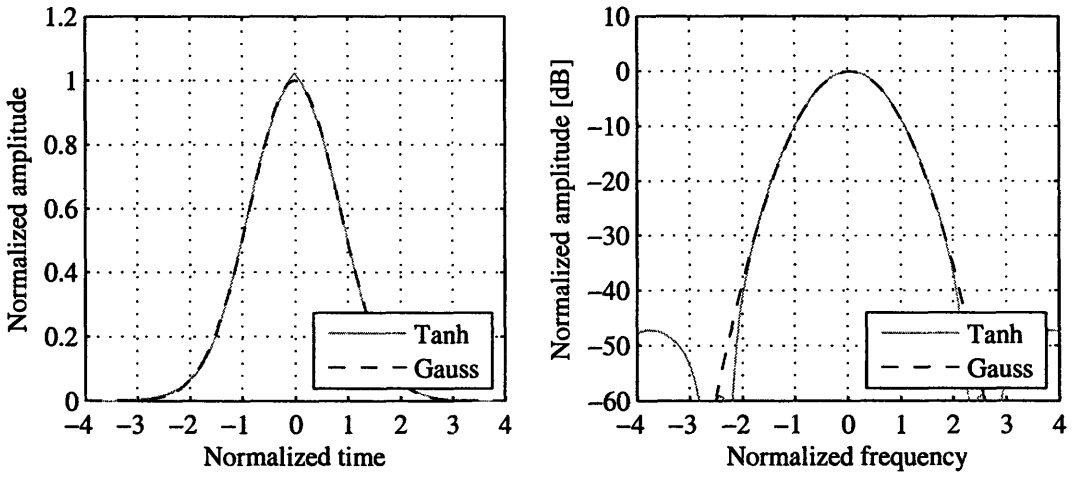

Figure 4-4: Time and frequency response of the optimized tanh pulse for $\sigma = 1.0$, $V_{off} = 1.0$.

$$A = 2.4 + 2.0 \cdot V_{off}. \tag{4.4}$$

2. *Pulse Width PW*: The pulse width is proportional to σ, and varies linearly with V_{off} for $V_{off} > 1.0$. The equation for setting PW is

$$PW = \sigma(4.37 + 3.61 \cdot V_{off}). \tag{4.5}$$

3. *Normalized Offset V_{off}*: The offset normalized to $2V_{th}$ does not vary with σ of the Gaussian function, and should be greater than 1.0 for best results. This ensures the differential pair steers enough current away from the output node in the off state. Increasing V_{off} beyond this value affects the circuit after all current has been steered from the output. Therefore, making it arbitrarily large does not improve the response, and it should remain within the biasing constraints of the circuit.

$$V_{off} \geq 1.0 \tag{4.6}$$

As shown in Figure 4-3, the minimum MSE between the tanh and Gaussian pulses is broad. This relaxes the requirements on the circuitry used to generate the triangle signal. It also relaxes the dependency of the pulse shape on temperature through V_{th}. Varying temperature over a range of 28% (of Kelvin) results in an 11% variation in bandwidth and 0.2dB in peak power for the pulse shown in Figure 4-4.

4.3.3 Transmitter Architecture

A block diagram of the transmitter is shown in Figure 4-5. The triangle signal is implemented off-chip, but is suitable for integration. To generate BPSK pulses, the triangle signal is switched to either the positive or negative input of the mixer. The inactive mixer input is simultaneously switched to a constant voltage. The same triangle signal is used to generate both polarity pulses to improve matching between

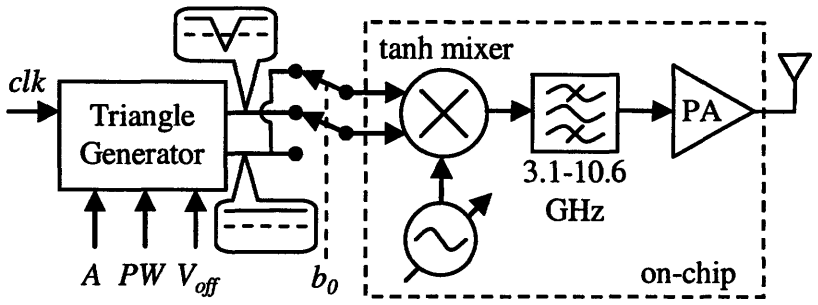

Figure 4-5: BPSK UWB transmitter block diagram.

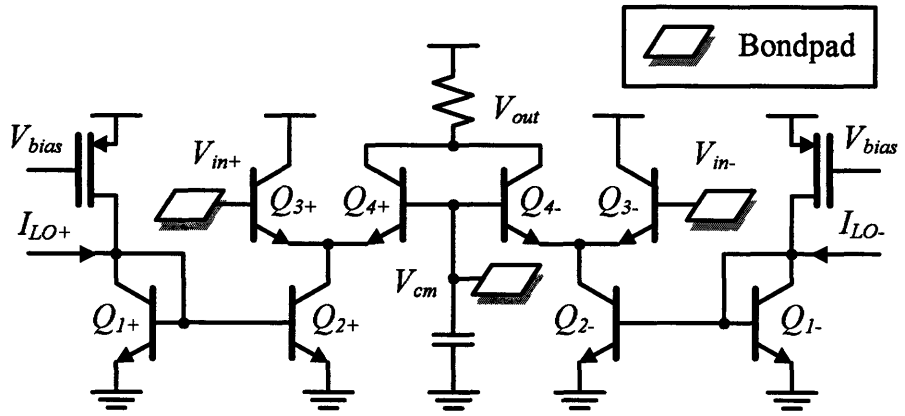

Figure 4-6: Schematic of the tanh pulse shaping UWB mixer.

pulses. The triangle signal switch also has an off state to implement variable PRF or a standby mode. The up-converted pulse is filtered and amplified on-chip before being DC-coupled to the off-chip UWB antenna.

4.3.4 Circuit Description

A schematic of the tanh pulse-shaping mixer is shown in Figure 4-6. At the core are two tanh shaping pulse generators made by transistors $Q_{3+/-}$ and $Q_{4+/-}$. The tail currents of the pulse generators are modulated by LO signals. This enables simultaneous pulse shaping and up-conversion mixing. The LO signals to the two pulse generators are 180° out of phase, giving the inversion for BPSK pulse generation.

The LO signal is generated on-chip, or can be switched to an external source, and can be tuned from 3.1-10.6GHz. The LO signal path is balanced to ensure equal amplitudes and 180° phase difference between the differential signals. The differential

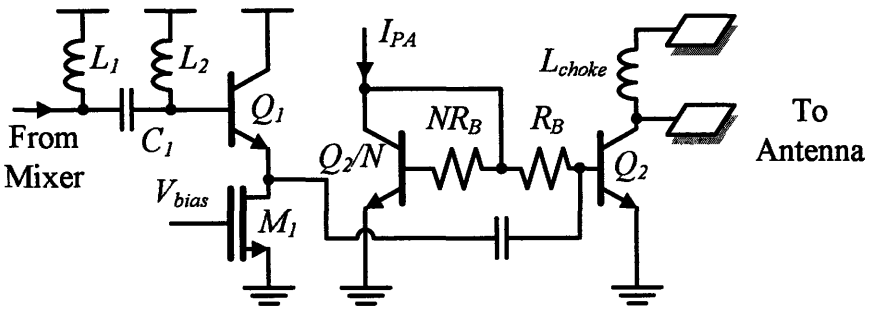

Figure 4-7: Schematic 3.1-10.6-GHz filter and power amplifier.

LO signals are converted to a current and mirrored, along with a bias current, into the tails of the two differential pairs.

Up-converted positive or negative pulses are generated by applying the triangle input signal to V_{in+} or V_{in-}, respectively. The triangle signal voltage is relative to V_{cm}, which is at a fixed potential. Applying the triangle signal to $Q_{3+/-}$ with the bases of $Q_{4+/-}$ fixed reduces unwanted signals from coupling to the output. The output currents of the differential pairs are summed at node V_{out}. This provides first-order cancellation of LO feedthrough, similar to a double-balanced Gilbert cell mixer.

A schematic of the UWB band select filter and power amplifier (PA) is shown in Figure 4-7. The mixer output is fed into the filter made by L_1, L_2, and C_1, providing a 2^{nd}-order roll-off below 3GHz to reduce out-of-band emissions. The simulated frequency response of the mixer and filter is plotted in Figure 4-8. The signal is then buffered and AC coupled to the PA. The PA is class A, with an RF choke at the output, and can be DC coupled to the antenna. The PA output impedance is sized to meet the output power requirement, and as a result is not matched to the 50Ohm antenna impedance. This does not cause degradation of the pulse because reflections off the antenna are minimal.

4.3.5 Experimental Results

The transmitter was fabricated in a 0.18μm SiGe BiCMOS process, and packaged in a 48 lead MLF/QFN package, which is a wirebonded package. Due to a resonance with the bondwires at the input of the mixer, the pulses generated in channels 6-10

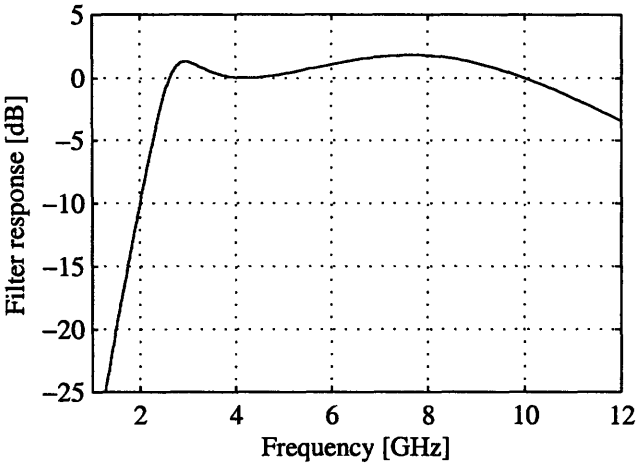

Figure 4-8: Simulated AC response of the LO path through the mixer and filter.

were distorted and did not have a Gaussian shape. An external LO was used as the center frequency of the pulses for all measurement results.

The matching between positive and negative pulses was evaluated at each of the center frequencies by measuring the peak power and bandwidth of a train of all positive or all negative pulses. An external LO was used to set the center frequency of the pulses, with an on-chip, single to differential converter to generate the differential LO used for inverting pulses. This converter has inherent mismatch in its differential outputs that varies with frequency, which can directly lead to mismatch between positive and negative pulse amplitudes. The spectral measurements fall into the *high*-PRF region for a PRF of 100MHz and RBW of 1MHz; therefore, a line spectrum is observed for a repetitive pulse train and peak power levels are independent of RBW. The measurements of peak pulse power in each channel are shown in Figure 4-9. The undistorted pulse responses demonstrated matching better than 2.5dB.

The peak voltage V_p of the pulse was measured at each center frequency with a high-speed sampling oscilloscope. The effective pulse width was approximated from the spectrum measurement by $\tau_{eff} \approx 1/(f_{1st\,null} - f_{center})$. This was used in (2.13) and (2.17) to predict the measured peak power level. The calculated and measured results can be compared in Figure 4-10. Each peak power data point is the RMS average of the negative and positive pulse powers at that center frequency. There is

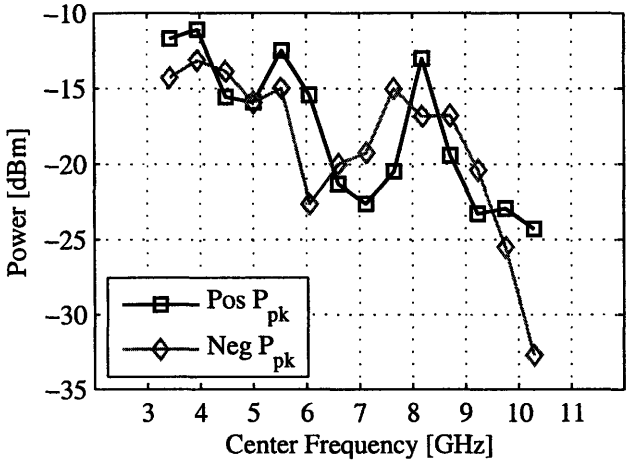

Figure 4-9: Unmodulated peak power matching between positive and negative pulses.

very good agreement between the calculated and measured peak powers. This peak power is of an unmodulated pulse train.

The FCC restrictions for the UWB band that affect most high data rate communication systems are the average emissions mask with a maximum of -41.3dBm/MHz between 3.1-10.6GHz, and the minimum signal bandwidth requirement of 500MHz within this band. The average power of a pulse train modulated with random data is calculated using (2.15) with measured data and plotted in Figure 4-10. This data is based on an RMS average of the positive and negative pulse peak power levels. The -41.3dBm/MHz FCC limit is exceeded in some channels using nominal biasing; however, this can be corrected by reducing the gain adjustment in the power amplifier. The modulated peak power is expected to be 11dB above the average power and follows a $10log(RBW)$ trend in the *high*-PRF region [4]. For a 2MHz RBW, the calculated peak power does not exceed the FCC limit of -28dBm when the -41.3dBm/MHz average power limit is not exceeded.

A measured pulse with a center frequency of 4GHz is shown in Figure 4-11 as an example of an up-converted tanh-shaped pulse. Table 4.1 provides a summary of the pulse generator specifications. The architecture and frequency plan of this pulse-based transmitter is closest to the architecture of WiMedia compliant OFDM transmitters [10]. Therefore, this work is compared to OFDM transmitters in Table

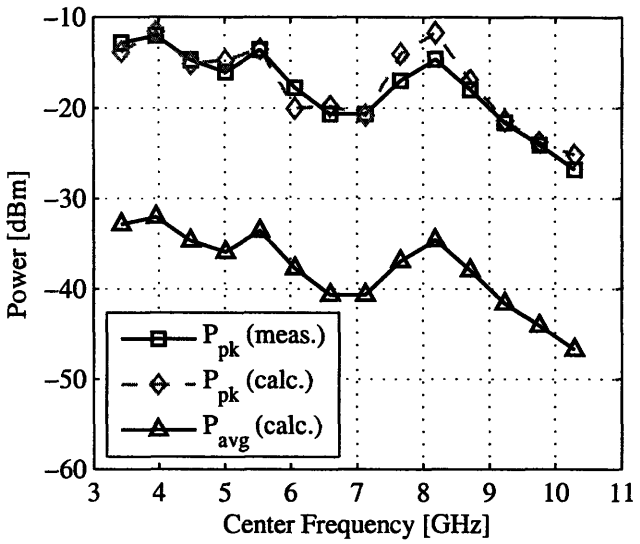

Figure 4-10: Plot of the pulse power levels in the 14 UWB channels. Peak power reported is with no modulation. Modulated peak power is expected to be 11dB above modulated average power [4].

4.2. A die photo of the transmitter is shown in Figure 4-12.

4.4 Conclusion

A technique for generating pulses that accurately approximates a Gaussian shape has been proposed as a contribution to this thesis. By exploiting the exponential properties of a BJT, a near-Gaussian pulse is shaped from a triangle input signal. This

Table 4.1: Transmitter Specifications Summary

Specification	Value
Mixer and LO buffering power	25.2 mW
PA power	6.1 mW
Total power	31.3 mW
Pulse repetition frequency	100 MHz
Effective pulse width τ_{eff} (ch. 1-5, 11-14)*	1.7-3.3 ns
-10dB bandwidth** (ch. 1-5, 11-14)*	426-558 MHz

*Pulses in channels 6-10 distorted by resonance at mixer input
**Weighted average BW of positive and negative pulses in each channel

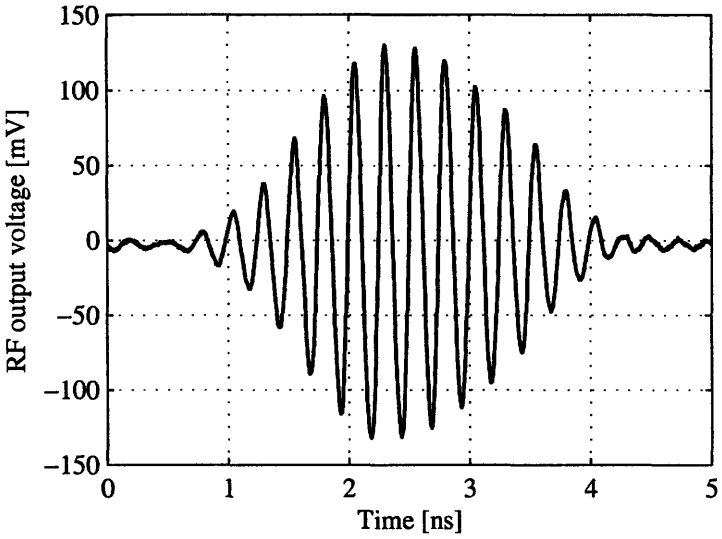

Figure 4-11: Measured pulse modulated by a 4.0-GHz external LO.

Table 4.2: Performance Comparison of this work to OFDM transmitter front-ends with similar frequency specifications.

	[63]	[64]	This Work
Supply	2.7V	1.2V	1.8 V
Total power	116mW	36mW	31.3 mW
Process	0.25μm BiCMOS	90nm CMOS	0.18μm BiCMOS
Active die area	n/a	0.1mm^2	0.8mm^2
Modulation	OFDM	OFDM	BPSK
-10dB bandwidth	528MHz	1GHz	426-558 MHz

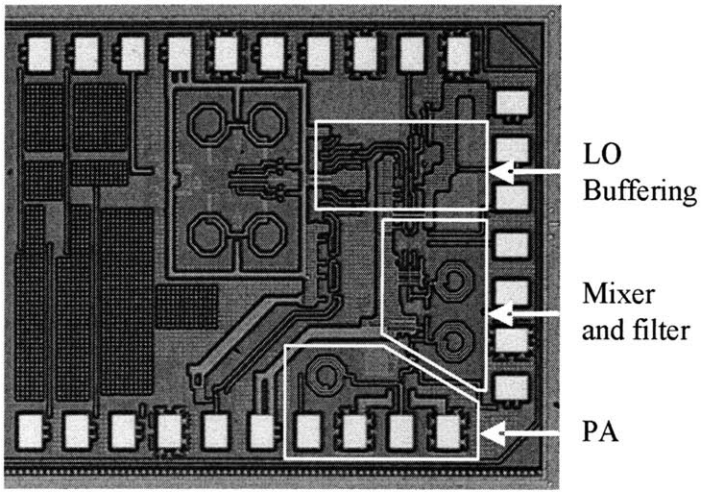

Figure 4-12: Die photo of the transmitter with a tanh shaping pulse generator. The dimensions are 1.7mm by 1.4mm.

technique provides several advantages, such as improved matching between BPSK pulses, no requirement for a reset phase in the pulse generation, a simplified up-conversion technique, and the potential of extending the approach to higher-order modulation such as QPSK.

Parameters specifying the input triangle signal have been empirically optimized in order to minimize the MSE between the resulting tanh pulse and a true Gaussian. The result is a maximum error of 2.4% within the -10dB bandwidth of the tanh spectrum and a true Gaussian spectrum. The tanh pulse shaping technique has been demonstrated in a 0.18μm SiGe BiCMOS chip. The pulse shaping and up-conversion to the UWB band is implemented in one circuit, with the inversion performed in the LO to improve matching between BPSK pulses. Pulse shaping in the chip is limited in channels 6-10 due to parasitics on the mixer input. Matched BPSK pulses, and near-Gaussian pulse generation has been demonstrated at a PRF of 100MHz in all other channels.

Chapter 5

All-Digital Transmitter

The amount of available bandwidth in the UWB band far exceeds the bandwidth required for low data rate transceivers. UWB radios are uniquely positioned to exploit the available bandwidth by trading off spectral efficiency for other system specifications such as energy/bit. This is in contrast to the design of the transceiver presented in Chapter 4, with restrictions on spectral efficiency to maximize the aggregate data rate in a multi-user environment.

The pulse generation technique and transmitter presented in this chapter capitalizes on the available bandwidth by using an all-digital architecture that consumes energy only in CV^2 losses and subthreshold leakage. The key contributions of this work are a delay-line-based pulse generation technique with a programmable pulse center frequency and bandwidth, a digital calibration technique, and a pulse spectrum scrambling technique suitable for digital transmitter architectures. This chapter begins with a description of the overall transceiver architecture in which the transmitter is designed to operate. Then following sections present the design, implementation, and results from the all-digital transmitter.

5.1 Motivation

CMOS radios are encountering challenges associated with shrinking power supplies and gate leakage as CMOS processes scale into the ultra-deep-submicron regime [65].

The reduction in voltage headroom requires either an increase in power consumption to maintain fixed performance, or a new circuit topology with limits on stacking devices. Linearity also suffers as the drain voltage reduces for similar gate overdrive voltages. This is a result of the device operating at the transition between the linear and saturation regions. Increasing gate leakage affects drooping of stored voltages on MOS capacitors, commonly used in analog-to-digital converters and phase-locked loops. This ultimately results in replacing MOS capacitors with lower-density capacitors, increasing die area. Gate leakage mismatch is a significant source of mismatch in 65nm and below.

In the face of these adversities, analog and RF circuits are migrating into the digital domain in order to take advantage of CMOS scaling [32,66,67]. Digital complexity is being added to correct for poorer performance of the analog transistors, or new architectures are being developed to accommodate the limitations of deep-submicron CMOS processes.

What deep-submicron CMOS processes lack in analog precision and linearity, they make up for in speed. The fast switching makes them ideal for processing pulsed UWB signals. The performance weighting towards speed is desirable for UWB circuits, where pulses are very short and precise in time and the amplitude and linearity performance are secondary. Non-coherent UWB architectures alleviate some of the receiver specifications such as linearity and frequency resolution, with moderate noise performance and gain requirements [68]. Pulsed-UWB transmitters, however, are ideally suited for integration in a CMOS process. When considering a non-coherent receiver architecture with relaxed frequency tolerances, an all-digital transmitter implementation is feasible with no need for analog gain blocks or pulse generators, only precision timing circuits.

5.2 System Architecture

The transmitter presented in this chapter is designed to operate in transceiver architecture with three main objectives; 1) frequency diversity for robustness to interferers,

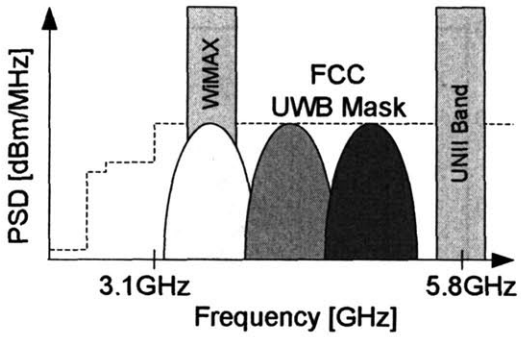

Figure 5-1: Three-channel frequency plan for the all-digital transmitter with known in-band interferers.

2) a variable low-data rate with power consumption that scales with data rate, and 3) minimized energy consumption per bit. This section describes the architecture of the transceiver.

Most pulsed-UWB transceivers use only a single band for communication, offering no frequency diversity and leaving them vulnerable to interference [24, 31, 69, 70]. Single-band pulse generator architectures can be extremely simple, and often operate open-loop (i.e. no closed-loop regulation of the pulse width or amplitude). Having a fixed band also simplifies the receiver architecture. Susceptibility to interference is possibly the single most criticized aspect of UWB architectures and it must be addressed.

This transceiver uses a three-channel frequency plan shown in Figure 5-1 with the channel center frequencies of 3.45GHz, 4.05GHz, and 4.65GHz. This plan avoids the UNII band in the 5-6GHz range, and provides two channels that will not overlap the future WiMAX band of 3.4-3.5GHz. Thus, the transceiver can use the optimal channel for communication in the presence of multipath and known in-band interferers.

Pulsed-UWB signals are inherently duty-cycled; that is, UWB signals are pulses in time that are separated by periods of time when no signal is present. This is compared to continuous waves used for narrowband communication, in which signals are on continuously. Pulsed signaling is advantageous because the active circuits only need to be powered when transmitting or receiving the short pulse. During the interval between pulses, the circuits can be gated off. This effectively decouples the

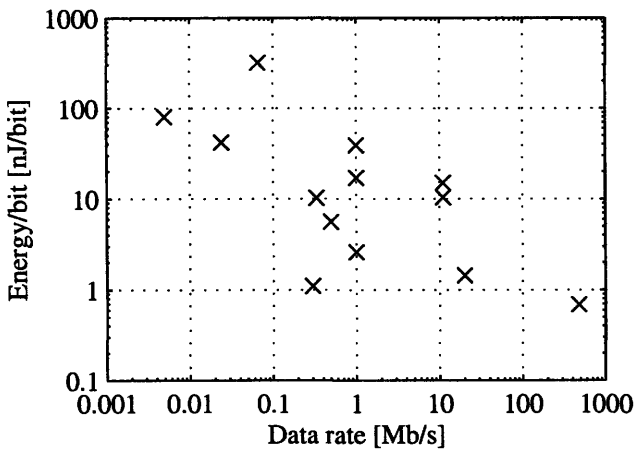

Figure 5-2: Trend of energy/bit versus data rate for various radios [73–85].

energy/bit from the data rate, because the data rate is varied by changing the time between pulses. No additional energy is consumed during the interval between pulses other than by subthreshold leakage currents. This results in an energy/bit that is fixed over a wide range of data rates. This is typically not the case for radios that include an LO and PLL, which show a trend of increasing energy/bit as the data rate is reduced, as shown in Figure 5-2. Duty cycling can be applied at a higher level to radios requiring an LO and PLL to reduce their net data rate while maintaining a fixed energy/bit; however, with limitation. For data rates typically below 1Mb/s, the energy/bit becomes dominated by the fixed startup cost of the PLL and the upward trend in energy/bit is observed [71, 72].

In order to decouple the data rate from energy/bit and minimize energy consumption per pulse, some aspects of the transceiver must be traded-off. First, pulse position modulation (PPM) is used so that a non-coherent, energy-detection receiver may be implemented. This type of receiver squares the incoming signal, therefore no local oscillator (LO) is required for down-conversion. Eliminating the LO means there is no PLL settling time or LO start-up time, which dominate the startup time of receivers. Therefore, the receiver can turn on in 2ns. The use of a non-coherent receiver also relaxes the specifications on the pulse generator; in particular, the accuracy of the center frequency and bandwidth of the pulse may be 6000ppm, where <100ppm

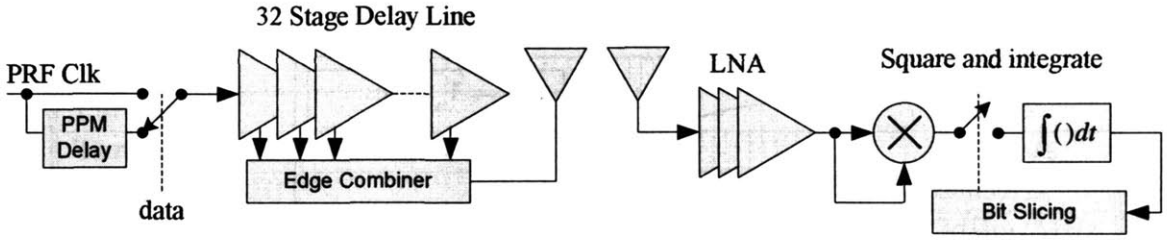

Figure 5-3: Block diagram of the all-digital transmitter and square-and-integrate PPM receiver.

is typical for narrowband radios. This enables the use of an all-digital architecture for the transmitter with the equivalent of no turn-on time. SNR suffers an immediate 3dB loss by using PPM instead of BPSK signaling, and the non-coherent architecture adds further losses to SNR when compared to a coherent one [41].

A block diagram of the transceiver is shown in Figure 5-3. The transmitter uses a delay line to synthesize pulses at the desired channel center frequency, and will be described in detail in the following sections. The non-coherent receiver uses tunable channel-select filters in the LNA gain stages to amplify pulses only in the desired channel. The pulses are then self-mixed to down-convert them to baseband, and the received power is integrated to determine which time slot the PPM pulse occurred in.

The probability of error for this receiver when $\frac{E_b}{N_0} < \frac{T_w B}{2}$ is given by

$$P_e = Q\left(\frac{E_b/N_0}{\sqrt{2T_wB + 2E_b/N_0}}\right) \tag{5.1}$$

where T_w is the integration window in seconds for 1 pulse, and B is the bandwidth in Hertz [41, 86]. For a discrete time system with sample rate f_s, $B = \frac{f_s}{2}$, therefore oversampling must be considered when analyzing a continuous time system in discrete time. The BER curve for a 30ns integration window (and no oversampling) is shown in Figure 5-4, along with the BER curve for a coherent PPM receiver for comparison ($P_e = Q\left(\sqrt{\frac{E_b}{N_0}}\right)$). An $\frac{E_b}{N_0}$ of 14.7dB is required for a BER of 10^{-3}, which is an SNR of -0.5dB from $SNR = \frac{E_b}{N_0}\frac{R}{B}$ where R is the data rate and B is the signal bandwidth.

A link budget is shown in Table 5.1 for a BER of 10^{-3} at 16.7Mb/s and a range of 10m. The table is generated using the guidelines from the IEEE 802.15 working

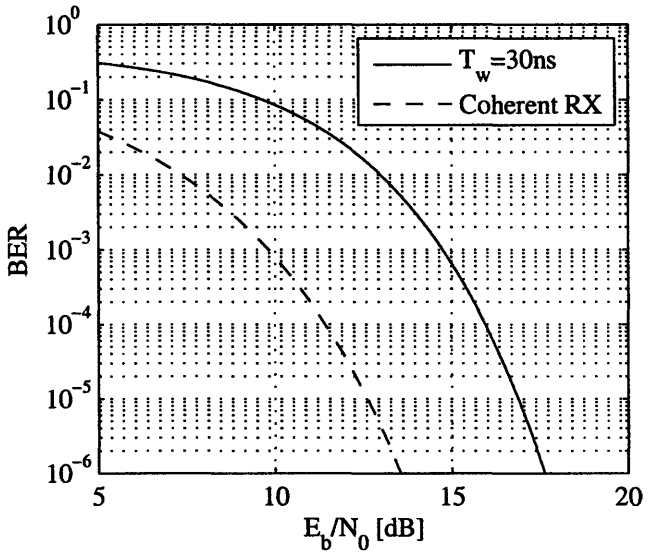

Figure 5-4: BER curve for the square-and-integrate PPM receiver with a 30ns integration window. Performance of a coherent PPM receiver is also plotted for comparison.

group [87]. The performance of the receiver is characterized by (5.1). The system has an expected link margin of 2.4dB.

5.3 Transmitter Signaling

5.3.1 Modulation

BPSK is the most common modulation found in literature for high and low data rate pulsed-UWB systems. It offers an inherent 3dB advantage in SNR over 2-PPM, a modulation which is also commonly found in literature for pulsed-UWB systems. In addition, the spectrum of BPSK modulated pulses with random data does not contain any spectral lines, which can be advantageous when maximizing transmit power while limited by the FCC mask. PPM is chosen in this transmitter in order to use a non-coherent, energy-detection receiver. This receiver architecture has several advantages over coherent receivers that allow it to operate at a relatively low energy/bit. The specific receiver architecture used allows for a relaxed accuracy on the center frequency of the transmitted pulse spectrum. In this case, the required accuracy is 6000ppm,

Table 5.1: Square-and-integrate receiver link budget.

Parameter	*Value*
Throughput (R_b)	16.7Mb/s
Bandwidth (B)	550MHz
FCC Limit (P_{FCC})	-41.3dBm/MHz
Maximum TX Power ($P_{max} = P_{FCC} + 10\log(B/1MHz)$)	-13.9dBm
Square pulse spectral efficiency (E)	-2.2dB
Average TX Power ($P_T = P_{max} + E$)	-16.1dBm
Path Loss @ 1m ($L_1 = 20\log(4\pi \cdot 4.05GHz/c)$)	44.6dB
Path Loss @ 100m ($L_2 = 20\log(d)$)	40dB
RX power ($P_R = P_T - L_1 - L_2$)	-71.7dBm
Avg. noise power per bit ($N = -174 + 10\log(R_b)$)	-101.8dBm
RX noise figure (N_f)	4dB
Total noise power per bit ($P_N = N + N_f$)	-97.8dBm
Minimum E_b/N_0 for 10^{-3} BER (S)	14.7dB
Link Margin ($M = P_R - R_N - S$)	2.4dB

compared to 100ppm for coherent receivers such as the one presented in Chapter 4. It is this relaxed specification that makes an all-digital transmitter practical. 6000ppm is chosen based on the constraints of the FCC mask, and the channel select filter bandwidth in the receiver [68].

The timing diagram for the PPM signaling used in this transceiver is shown in Figure 5-5. Data is encoded by placing the pulse in one of two consecutive time windows. This is demonstrated in the figure by encoding 0 (left) and 1 (right). The PPM separation time is 30ns, equal to the receiver integration window T_w. 30ns is chosen such that the worst case multipath channel and frequency offsets can be tolerated [50]. The PRF, and therefore the data rate, can be adjusted by varying T_{frame} from a minimum of $2T_w$ to an arbitrarily low PRF.

As shown in Figure 5-6, the spectrum of 2-PPM pulses will contain tones that are $10\log(\frac{PRF}{1MHz})$ dB above the spectrum of BPSK pulses when keeping all other factors, in particular the transmitted energy/pulse, equal [88]. The result of having tones in the output spectrum is a PPM transmitter will have to significantly lower its average power relative to a BPSK transmitter in order meet the FCC mask. For a PRF of

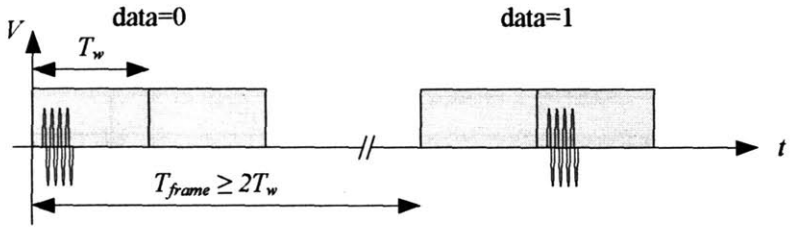

Figure 5-5: PPM modulated pulse timing diagram.

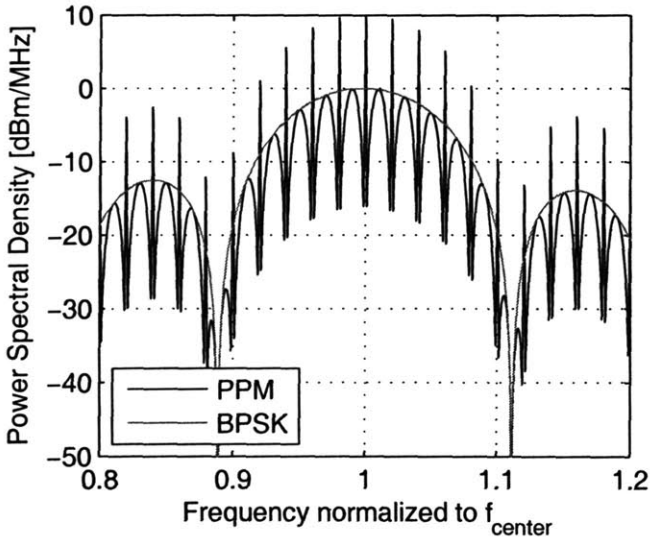

Figure 5-6: Ideal spectra for randomly modulated PPM and BPSK pulse streams. For both curves, pulse energy is fixed, $PRF = 10MHz$, and an *up-converted* square pulse is used with a width of 9 periods of the RF center frequency.

10MHz, the PPM transmitter power must be lowered by 10dB below the BPSK transmitter power. To avoid this penalty, BPSK scrambling is typically used in addition to 2-PPM, eliminating all PPM tones, and removing the need for reducing the average power [89]. These tones can also be scrambled by increasing the order of the PPM modulation; however, this increases the synchronization and power consumption in the receiver. BPSK scrambling decouples the scrambling problem from the modulation, and is transparent to an energy-detection receiver. Therefore, BPSK scrambling is more commonly implemented. For example, the 802.15.4a standard for low rate UWB communication specifies that PPM is applied to the start time of a burst of pulses, and BPSK modulation of the pulses is applied within each burst [23].

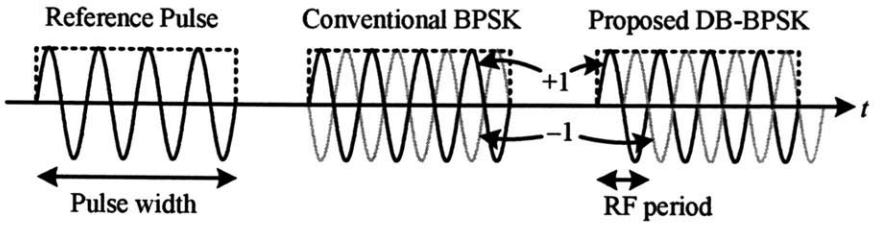

Figure 5-7: BPSK inversion and delay-based inversion. The reference 4-cycle pulse is overlaid with the inverted BPSK and DB-BPSK pulses for comparison.

BPSK modulation typically comes with a certain amount of added complexity and power consumption in the transmitter. This complexity often leads to the use of RF amplifiers and mixers dissipating static power, or passive components that consume a relatively large die area. Power and area are two key constraints for which circuit designers go to great lengths to minimize, often at the expense of performance. PPM transmitters and receivers, however, offer an advantage in system complexity over BPSK. Pulse generation circuits become much simpler, and a relatively low power and precision, non-coherent receiver can be used for demodulation.

It would therefore be advantageous from a spectrum scrambling and cost perspective to combine the spectral properties of BPSK signals with the implementation simplicity of a PPM transmitter. This can be achieved with the proposed *delay-based* BPSK (DB-BPSK) modulation.

5.3.2 Delay-Based BPSK for Phase Scrambling

Figure 5-7 demonstrates the subtle difference between BPSK inversion and delay-based BPSK inversion. The plots show a reference pulse in black that is a baseband square pulse multiplied by an RF carrier frequency, producing a 4-cycle pulse. An *inverted* pulse is overlaid in gray for BPSK and DB-BPSK. The BPSK inversion is obtained by multiplying the reference pulse by -1. The DB-BPSK "inversion" is instead a delay by half of the RF cycle period. I have termed this delay-based BPSK because of how the inversion is generated. Conceptually this appears to have the same effect as the BPSK inversion in the middle of the pulse, with only the ends of

Table 5.2: Table of equations for modulated pulse trains

Eq.	Modulation	Spectrum [W/Hz]
(1)	BPSK	0 $+\frac{1}{T_s}\left\|S(f)\right\|^2$
(2)	PPM	$\frac{1}{4T_s^2}\cdot\sum_{n=-\infty}^{\infty}\left\|S(\frac{n}{T_s})(1+e^{-j2\pi\frac{nT_{ppm}}{T_s}})\right\|^2\delta(f-\frac{n}{T_s})$ $+\frac{1}{T_s}\left\|S(f)\right\|^2-\frac{1}{4T_s}\left\|S(f)(1+e^{-j2\pi fT_{ppm}})\right\|^2$
(3)	PPM+ BPSK	0 $+\frac{1}{T_s}\left\|S(f)\right\|^2$
(4)	DB-BPSK	$\frac{1}{4T_s^2}\cdot\sum_{n=-\infty}^{\infty}\left\|S(\frac{n}{T_s})(1+e^{-j\frac{n\pi}{f_{RF}T_s}})\right\|^2\delta(f-\frac{n}{T_s})$ $+\frac{1}{T_s}\left\|S(f)\right\|^2-\frac{1}{4T_s}\left\|S(f)(1+e^{-j\frac{\pi f}{f_{RF}}})\right\|^2$
(5)	PPM+ DB-BPSK	$\frac{1}{4T_s^2}\cdot\sum_{n=-\infty}^{\infty}\left\|S(\frac{n}{T_s})(1+e^{-j2\pi\frac{nT_{ppm}}{T_s}})(1+e^{-j\frac{n\pi}{f_{RF}T_s}})\right\|^2\delta(f-\frac{n}{T_s})$ $+\frac{1}{T_s}\left\|S(f)\right\|^2-\frac{1}{4T_s}\left\|S(f)(1+e^{-j2\pi fT_{ppm}})(1+e^{-j\frac{\pi f}{f_{RF}}})\right\|^2$

the pulses differing from conventional BPSK. As the number of RF cycles per pulse increases, these differences become a smaller portion of the total pulse energy and one would expect DB-BPSK to approach BPSK.

A summary of equations describing the spectrum of PPM, BPSK, and DB-BPSK signals is shown in Table 5.2, modified from the analysis provided in [88]. This assumes the signal is modulated by purely random data. $S(f)$ is the Fourier transform of the reference pulse, T_s is the pulse repetition interval equal to $1/PRF$, f_{RF} is the center frequency of the pulse, equal to the cycle frequency for the pulses shown in Figure 5-7, and T_{ppm} is the PPM delay, assuming a fixed time-hopping sequence. For each modulation scheme, the spectrum is divided into two components: a discrete and continuous part. The discrete part describes the magnitude of any spectral lines, as indicated by the delta functions in these equations. The continuous part is a smooth spectrum, which is the desirable component when considering the FCC mask. The total spectrum is the sum of these two parts. The BPSK (Table 5.2.(1)) signal does not contain a discrete part, while the PPM (Table 5.2.(2)) spectrum contains discrete tones spaced at twice the PRF. When BPSK scrambling is added to a PPM signal (Table 5.2.(3)), the PPM tones are scrambled and the signal has only a continuous

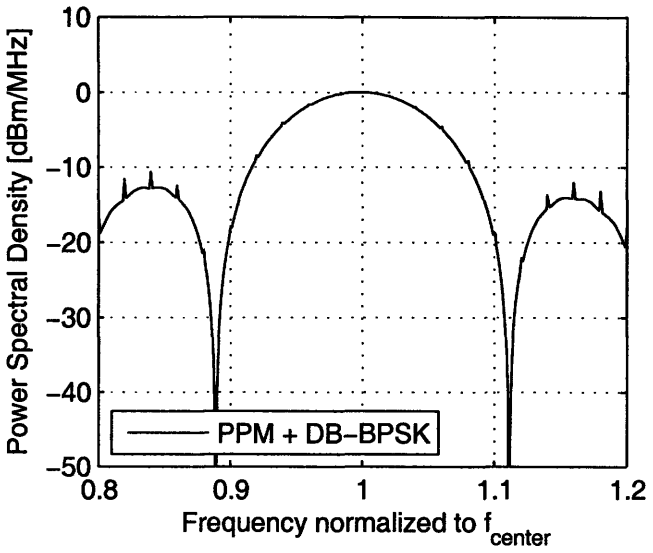

Figure 5-8: Spectrum for randomly modulated PPM pulses with DB-BPSK scrambling.

part, explaining why BPSK is often used for smoothing the spectrum of a PPM signal.

Just as BPSK can be applied to a PPM signal to scramble the spectrum, so can DB-BPSK. The spectrum for PPM + DB-BPSK (Table 5.2.(5)) has a discrete and continuous part similar to a PPM spectrum, with the addition of a $(1 + e^{j\pi f/f_{RF}})$ term. This term acts as a bandstop filter centered around f_{RF}, the center frequency of the pulse. At f_{RF}, the magnitude of this term is zero and the PPM + DB-BPSK equations collapse to those of a BPSK signal. At frequencies around f_{RF}, the filter term attenuates the unwanted lines of the spectrum.

The equations for the DB-BPSK scrambled PPM signal are plotted in Figure 5-8. The pulses have a center frequency of 1GHz, a PRF of 10MHz, and a PPM delay of 50ns. The pulse width is 10ns. In this example, the PPM tones are reduced by 10dB ($10\log(PRF/1MHz)$) by using DB-BPSK scrambling. Note that there are some spectral lines beginning to appear on the sidelobes of the PPM + DB-BPSK pulse. This is due to the reduced filtering effect of the $(1 + e^{j\pi f/f_{RF}})$ term, which has been overlaid in the plot. These tones are sufficiently below the main lobe of the pulse and don't affect FCC compliance.

Nine RF cycles per pulse is sufficient for scrambling all PPM tones in the main lobe

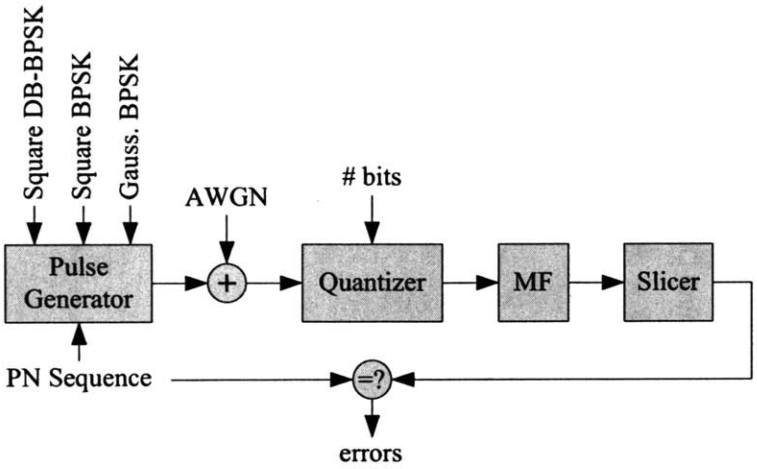

Figure 5-9: Block diagram of the matched filter receiver used in DB-BPSK simulations.

of the spectrum. This is demonstrated in Figure 5-8, where DB-BPSK scrambling has been added to the PPM pulses plotted in Figure 5-6.

5.3.3 Delay-Based BPSK for Communication

A further motivation for this form of "inversion" is the opportunity to implement a BPSK transmitter using this technique. The same principle is applied as for phase scrambling, however now data is modulating the pulse delay as opposed to a PN sequence.

The BER performance of DB-BPSK modulated square pulses in the presence of AWGN has been simulated, and the results compared to the performance of BPSK square pulses simulated with the same receiver. A PPM receiver alone is not usually capable of detecting BPSK signals, therefore a standard matched filter receiver is assumed for these simulations. A block diagram of the receiver is shown in Figure 5-9. The pulse waveforms are modulated by a PN sequence, and then added with AWGN. The output is quantized by a limiting quantizer with a variable number of bits. The quantized signal is convolved with the original signal in a matched filter, and the peak output is sliced to determine the bit.

1-bit and infinite-bit (no quantization) receivers were simulated to determine the

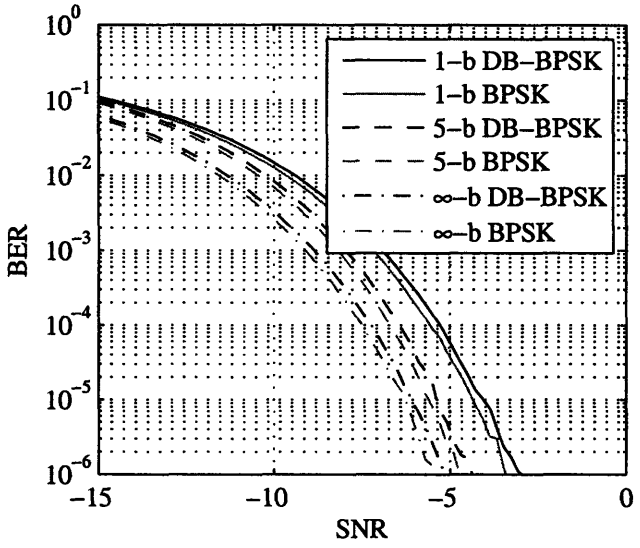

Figure 5-10: Waterfall curves comparing the performance of DB-BPSK modulation to BPSK for square pulses.

bounds on performance. A 5-bit simulation was also run to compare how DB-BPSK would perform in the high-data rate transceiver discussed in Chapter 4. Both square pulses and Gaussian pulses were analyzed, and the results are similar. The waterfall curves are plotted in Figure 5-10, which show the DB-BPSK curves are within 0.2 dB of the BPSK curves. This is a very promising result, implying DB-BPSK modulation could be used with a matched filter receiver, such as the one presented in Chapter 4, with only a 0.2dB impact in overall link budget.

5.4 Transmitter Architecture

5.4.1 Pulse Generation Principle

The basic pulse generation principle is to combine a series of equally-delayed edges to form a single RF pulse, as shown in Figure 5-11. A tapped delay line is used to generate the series of edges from each rising edge of the pulse repetition frequency signal. The edge combination is similar in operation to a frequency multiplier, where the output of the combiner is toggled when an edge is received on any of its inputs.

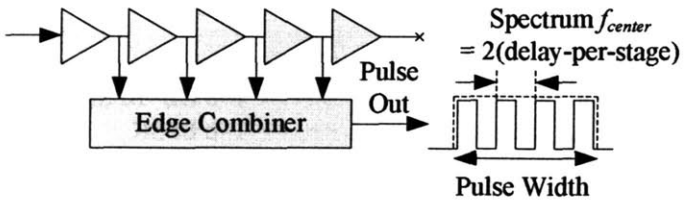

Figure 5-11: Basic pulse generation principle.

The generated pulse is mathematically equivalent to a baseband square pulse that has been multiplied by a square LO operating at the channel center frequency. The center frequency of the pulse spectrum is varied by controlling the delay-per-stage of the delay line. The width of the pulse is varied by making the number of edges combined programmable. By making both the delay-per-stage and number of edges programmable, the pulse spectrum may be precisely controlled without requiring an RF local oscillator.

5.4.2 Implementation

A block diagram of the transmitter (bottom) and the external FPGA controller (top) is shown in Figure 5-12. All blocks, including the RF pad driver, use full-swing, static CMOS digital circuits, and no analog bias currents are required. The transmitter is clocked by the FPGA with the PRF input, which triggers a single RF pulse on each rising edge of this signal. Each edge of the PRF input propagates through a 32-stage delay line with an 8-bit digitally controlled delay. During normal pulsed operation, the last stage of the delay line is disabled.

Recall that pulses are synthesized by combining a programmable number of edges. Twenty-five edges are required to synthesize DB-BPSK pulses in the highest channel, therefore a 32-stage delay line is used, from which thirty edges are made available for combination. Individual edges are selected by ANDing them with a 30-bit mask register. The $DB-BPSKPhase$ input selects between two mask values, used for scrambling the output spectrum. The 30 edges are combined using two time-interleaved 15-edge combiners, the outputs of which are XORed to complete the pulse synthesis.

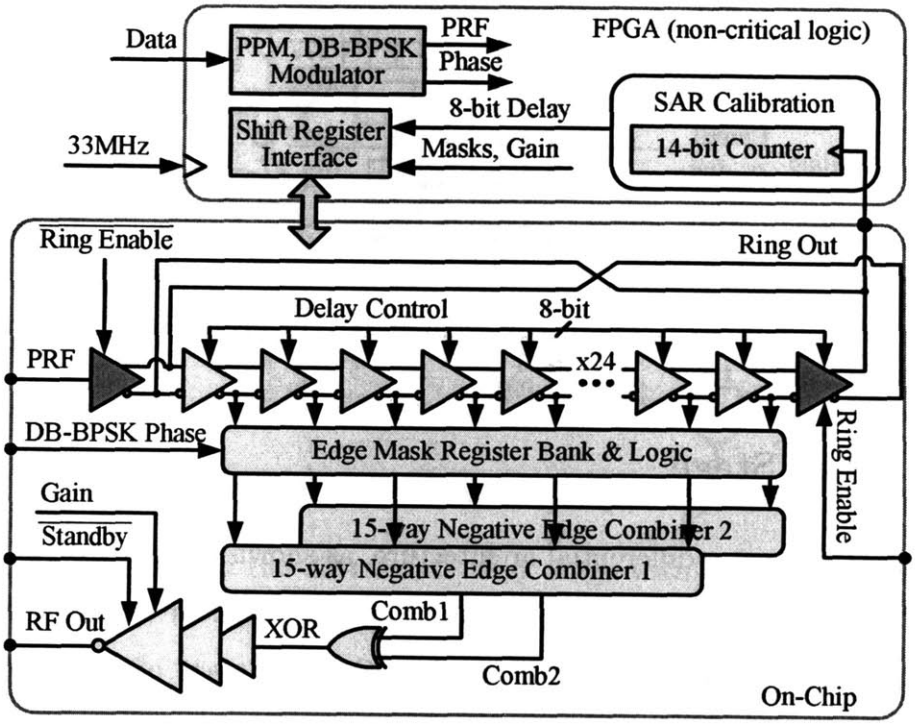

Figure 5-12: Block diagram of the transmitter IC and external FPGA controller.

The pulse is buffered by a digital pad driver, and the output is filtered by a UWB band-select filter that directly drives a 50Ω antenna. The FPGA performs the PPM modulation of the PRF signal, and the PN sequence generation for the scrambling of the output spectrum. It is also used to implement the digital algorithm for calibrating the delay-per-stage of the delay line. The entire transmitter is clocked at 33MHz.

A timing diagram of the edge combination is shown in Figure 5-13. The output edges $\overline{out[1:30]}$ are masked, and only the selected edges are combined by the interleaved combiners 1 and 2. The *Comb*1 and *Comb*2 signals are XORed, synthesizing the up-converted pulse with a spectrum centered in the desired channel.

5.5 Circuit Description

This section describes the circuit design for the transmitter. All of the blocks are be implemented as full-swing, static CMOS digital circuits.

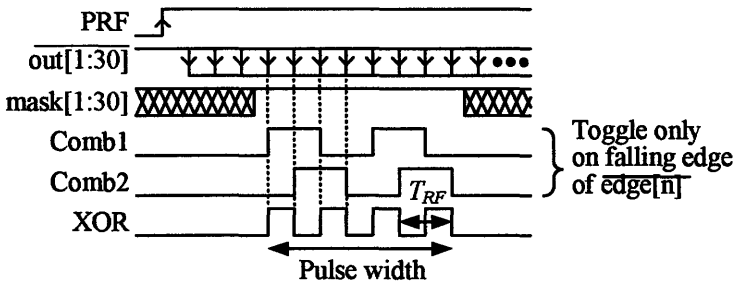

Figure 5-13: Timing diagram of the edge combination.

5.5.1 Delay Stage

Each delay stage uses a differential architecture, as shown in Figure 5-14. The delay is digitally controlled with a combination of binary-weighted current starving and a capacitor bank. An enable is used to place the final stage of the delay line in a high-impedance output state, which is the default configuration for pulsed operation. Enabling the last stage configures the delay line as a free-running oscillator, used only for calibration of the delay-per-stage.

Cross-coupled inverters are used for regeneration of the edges, serving two purposes: 1) to reduce the mismatch between rise and fall times of the differential signals, and 2) to suppress common mode latching in the ring, which has an even number of stages. The current source for the regeneration is kept separate from the current-starving network supplying the delaying inverters. This is to eliminate a shoot-through path that would exist in the last stage when it is disabled and both its inputs and outputs are driven at opposite polarities.

There are three constraints that motivated the use of a combination of current-starving and a capacitor bank to vary the delay: 1) mismatch between stages, 2) power consumption, and 3) parasitic capacitances on the internal nodes. The extracted parasitic capacitance on the internal nodes between delay stages ($in[n]$ and $out[n]$ in Figure 5-14) is 12fF, and dominates the parasitic gate capacitance on these nodes. MIM capacitors are added to these nodes to reduce the dependence of the delay/stage on parasitic routing capacitance, which has an unspecified variance. However, for every 1fF of load capacitance added, the transmitter energy/pulse increases by 64fJ.

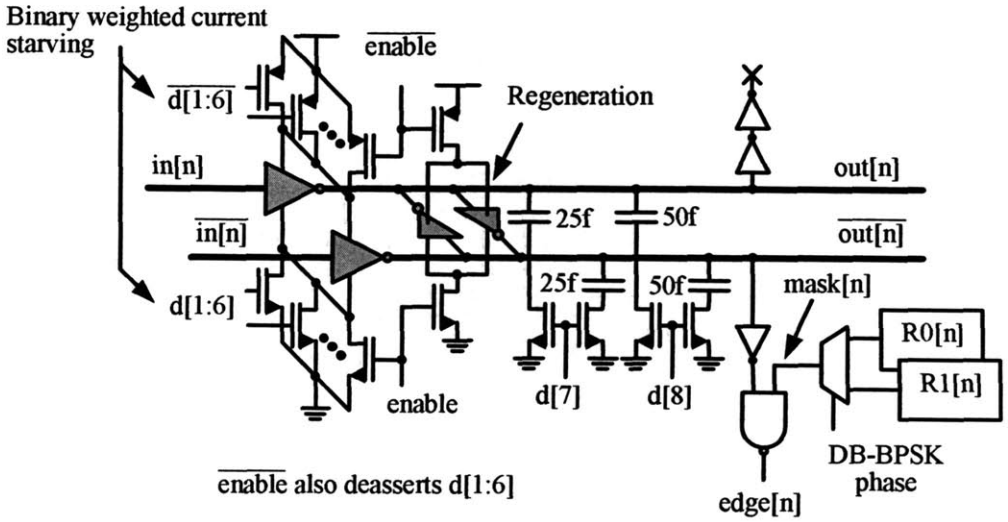

Figure 5-14: Schematic of the differential delay stage with binary weighted current starving and capacitor bank networks.

Therefore, a maximum of 75fF/node is used to dominate the 12fF parasitic wiring capacitance with a total 4.8pJ/pulse penalty in energy consumption. This accounts for 2 bits of the digital delay code. The remaining 6 bits of control can be obtained with binary weighted current starving transistors, as shown in Figure 5-14. These devices are sized so that there will be overlap in delay/stage between the 4 capacitor bank settings. The lengths of the current-starving transistors are 20% over minimum length to reduce leakage in the delay line.

5.5.2 Edge Combiner

There are two general categories in which combiners can be grouped: straight combinational logic [90–92] and combiners that preserve state [93]. Combinational logic edge combiners are typically used with a smaller number of edges, such as 4 to 8, due to the increasing logic depth with edges. Simulations in a 90nm CMOS process showed that even a 16-edge combination logic combiner using static CMOS could not operate at the required 5GHz speed. State-preserving edge combiners offer graceful scaling with an increasing number of edges.

The 30-edge combiner used to synthesize the UWB pulse is divided into two

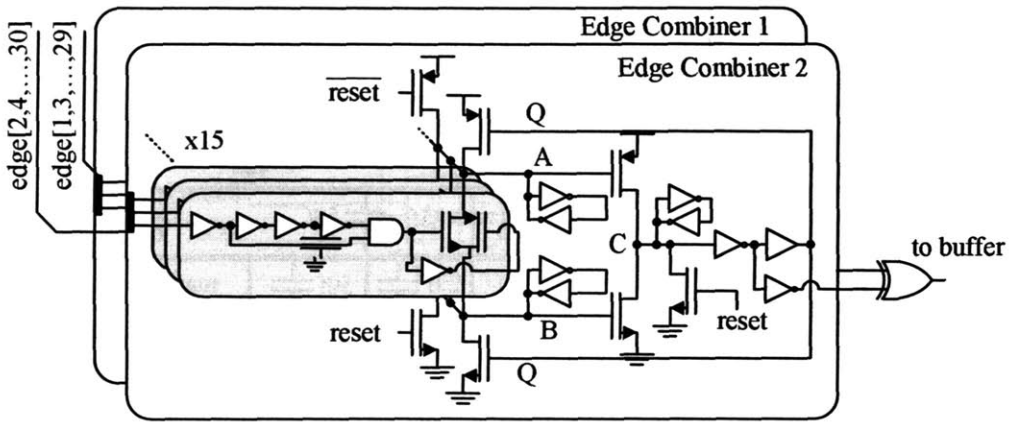

Figure 5-15: Time-interleaved, negative-edge combiner.

interleaved 15-edge combiners. A schematic of the 30-edge combiner is shown in Figure 5-15. The architecture is based on a clock generator that combines edges from a 4-stage DLL to generate a clock [93]. This architecture combines edges by generating a momentary short between nodes A and B when a negative edge is received on any of the 15 inputs. This momentary short then toggles the state of the latch at node C. A simulation of the edge combiner is shown in Figure 5-16. The top signal is a single edge from the delay line. The middle signal is the signal that controls the momentary short between nodes A and B, resulting in a single transition of the output. The combined signal is shown on the bottom.

5.5.3 Pass-Gate XOR

The outputs of the two interleaved edge combiners are XORed in order to synthesize the final pulse. This XOR was implemented using a pass-gate topology, which offers the best combination of speed and matched delay paths for a single-ended circuit. A schematic of the XOR is shown in Figure 5-17.

5.5.4 Pad Driver

The final stage of the RF pad driver is essentially a digital inverter with added functionality for varying the gain and reducing leakage. The transistors were sized in

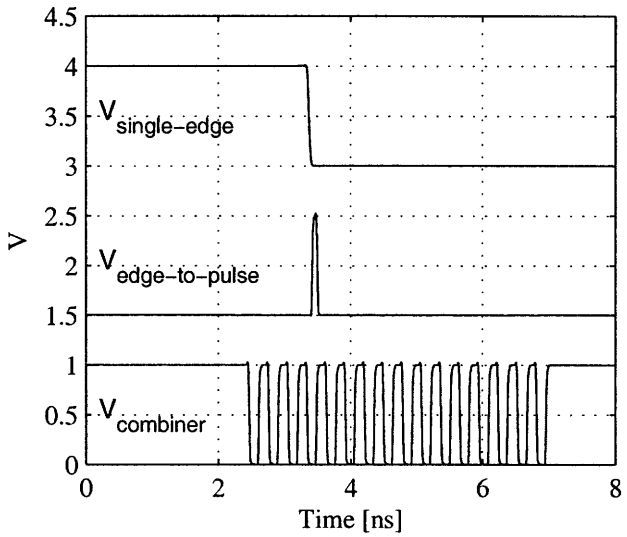

Figure 5-16: Simulation of the edge combiner showing a single edge tapped from the delay line, the edge-to-pulse signal, and the edge combiner output.

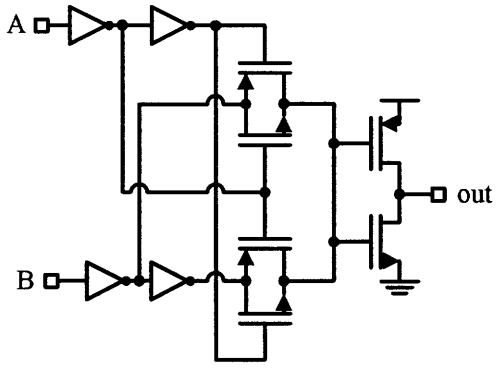

Figure 5-17: Schematic of the pass-gate XOR.

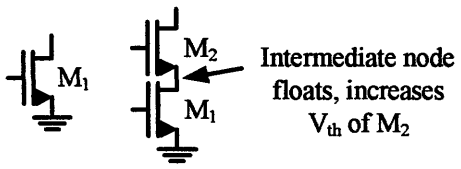

Figure 5-18: Stacked NMOS transistors to subthreshold reduce leakage current.

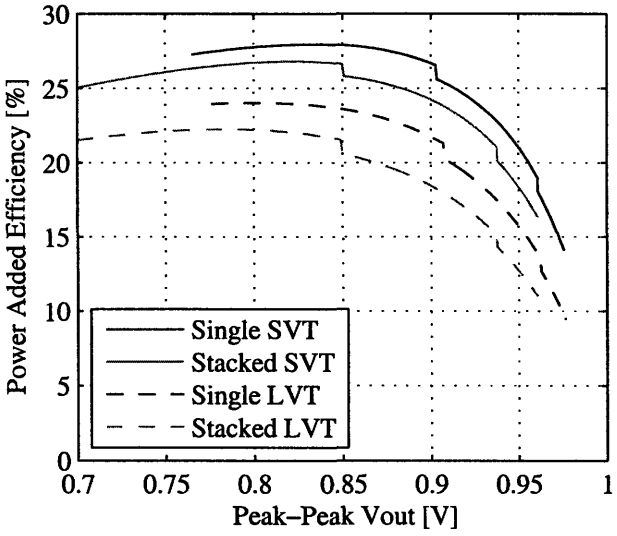

Figure 5-19: Pad driver efficiency as a function of the maximum pulse peak-to-peak voltage for low and standard V_t devices.

order to maximize the efficiency of the driver when driving a 50Ω antenna. Because the transistors are large, leakage is a concern in the final stage. A well-known technique of stacking NMOS devices was used in order to reduce leakage, as shown in Figure 5-18. In this case, the stacked NMOS transistors resulted in a leakage current 5 times lower than a single NMOS device for equal pull-down strengths. This is due to the intermediate node between transistors floating higher, increasing the threshold voltage of the top transistor due to the body effect.

The performance was simulated for a range of topologies and transistor sizes in order to model the efficiency of the driver. The two main contributions to loss are subthreshold leakage current and CV^2 switching losses. The efficiency can be modeled

as

$$\eta_{PA} = \frac{E_{pulse} f_{PRF}}{E_{pulse} f_{PRF} + E_{cond} f_{PRF} + V_{DD} I_{leak} + C_{eff} V_{DD}^2 N_{cycles} f_{PRF}}, \tag{5.2}$$

where E_{pulse} is the energy delivered to the antenna for a single pulse, f_{PRF} is the pulse repetition frequency, E_{cond} is the conduction losses per pulse, I_{leak} is the leakage current, and N_{cycles} is the number of RF cycles in a pulse. The efficiency is plotted for the driver using standard- and low-V_t devices in the final stage in Figure 5-19. Also compared are single NMOS devices and stacked NMOS devices to reduce the leakage component of the power consumption. The discontinuities in the curves are a result of adding extra buffer stages before the final output stage to account for the increasing width of the devices. Other topologies than the ones plotted were also explored, such as combinations of standard- and low-V_t devices, as well as stacked PMOS devices; however, the results yielded significantly lower efficiencies and aren't shown here.

The single NMOS standard-V_t driver resulted in the highest efficiency driver when actively generating pulses. Notice in (5.2) that the leakage component of the energy is the only term that is not scaled by f_{PRF}. Therefore, as f_{PRF} is reduced, or when the driver is placed in a standby mode ($f_{PRF} = 0$), the dominant contribution to losses is subthreshold leakage currents. This is not highlighted by the plots in Figure 5-19, which represent pulsed operation when leakage has much less of an impact. The stacked NMOS standard-V_t driver shows comparable efficiency results when transmitting pulses, while also reducing the subthreshold leakage by a factor of 5 due to the stacked effect. Additionally, a single NMOS driver offers no means for implementing a gain control, while this functionality comes at no additional cost with a stacked NMOS topology. The performance for both low-V_t topologies were lower than the standard-V_t. Therefore, the stacked NMOS standard-V_t topology was implemented in the final driver.

A schematic of the driver is shown in Figure 5-20. During pulse operation, the final stage is essentially a digital inverter formed by a strong PMOS pull-up ($MP1$) and the stacked NMOS pull-down network. The power of the output pulse is varied by

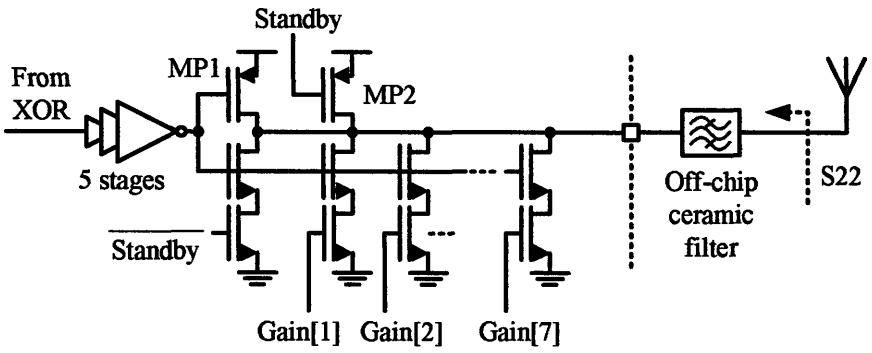

Figure 5-20: Schematic of the digital pad driver with linear-in-dB gain setting and standby mode.

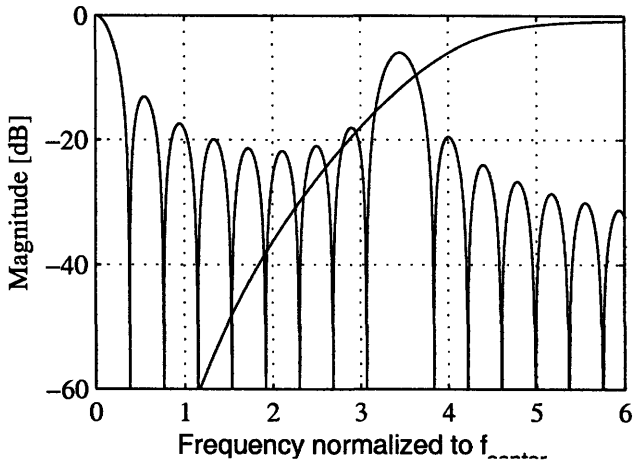

Figure 5-21: Simulated spectral content of the transmitter output before filtering and frequency response of the 5^{th}-order Butterworth filter.

increasing the drive strength of the pull-down network through the digital $Gain[1:7]$ controls. The widths of the NMOS devices in each of the branches of the pull-down network are weighted in order to produce a linear-in-dB power adjustment. During the idle period between pulses, the output node of the transmitter is strongly pulled to V_{DD} through $MP1$. The driver incorporates a high-impedance standby mode, where the output is pulled to V_{DD} through $MP2$, which is a weak device. The output is weakly held high in order to eliminate transients that would otherwise occur when coming out of standby mode.

The pulse generated by this transmitter will have spectral content centered around

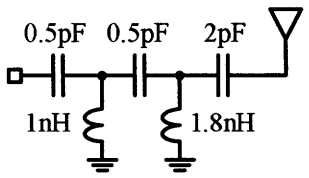

Figure 5-22: Schematic of the 5^{th}-order Butterworth filter implemented off-chip using discrete components.

the desired channel center frequency, as well as spectral content at DC, as shown in Figure 5-21 for a pulse center frequency of 3.45GHz. An off-chip band-select filter is required in order to eliminate the DC content. Two filter implementations were demonstrated with the transmitter. The first was a 5^{th}-order Butterworth high-pass filter built using discrete components on a PCB [94]. A schematic of this filter is shown in Figure 5-22, with the component values shown. The frequency response of the filter is shown in Figure 5-21, with a cutoff frequency of 4.5GHz. This cutoff is designed to be above the 3.1GHz edge of the UWB FCC mask to allow for parasitic capacitance on the PCB to shift the cutoff frequency lower, and to provide sufficient attenuation for the frequency range (960MHz-1.61GHz) that is deeply notched in the FCC mask.

Alternatively, a single-chip ceramic filter was used to filter the output spectrum [95]. This off-chip filter has a form factor of $3 \times 1.5 \times 1$mm with the equivalent frequency response of a 7^{th} order high-pass Butterworth filter. Because of the higher-order filter response than the discrete components filter, the cutoff frequency is placed at 2.8GHz and the same attenuation is achieved in the deeply notched portion of the FCC band. This filter can also be shared with the receiver, serving as the band-select filter, made possible by the high-impedance output mode of the driver stage.

5.6 Experimental Results

The transmitter was fabricated in a standard digital 90nm CMOS process with a MIM capacitor option. The design uses a combination of digital components from a standard cell library, as well as full-custom layout. The foundry was allowed to

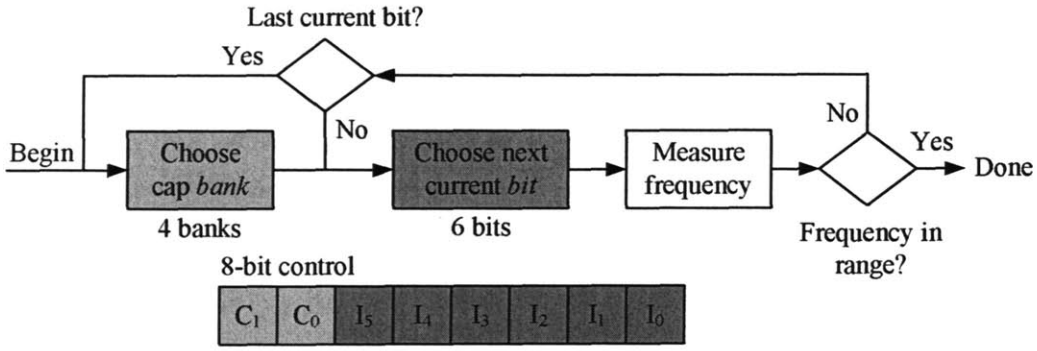

Figure 5-23: Flowchart of the successive approximation algorithm for calibrating the delay/stage.

automatically generate and place metal fill over the design to meet density rules. Automated metal fill is standard for digital design flows, but often metal fill is hand placed in RF circuit designs. Automated metal fill was allowed in this case to mimic a standard digital flow. The chips were packaged in a 24-lead, wirebonded QFN package. All measurement results presented in this section are of the packaged chips.

5.6.1 Delay Line and Calibration

The delay line is calibrated off-line by configuring the 32-stage delay line as a free-running oscillator and measuring the frequency of ocsillation. This is performed by disabling the driving stage, and enabling the last stage in the delay line which feeds back to the input, as shown in Figure 5-12. Ideally, the ring would oscillate at the pulse spectrum center frequency divided by 32 because it is a 32-stage ring oscillator. The pulse center frequency is predicted by measuring the frequency of the ring oscillator for a given digital delay control value. The delay control is adjusted in a successive approximation algorithm in order to center the pulse spectrum in the desired channel, and the ring oscillation frequency is measured by counting the ring cycles for a fixed period of time [96]. A flowchart of the calibration algorithm is shown in Figure 5-23. The calibration algorithm is implemented entirely in an FPGA, which automatically centers the pulse spectrum in the desired channel. The successive approximation search algorithm completes in a maximum $62\mu s$, stopping

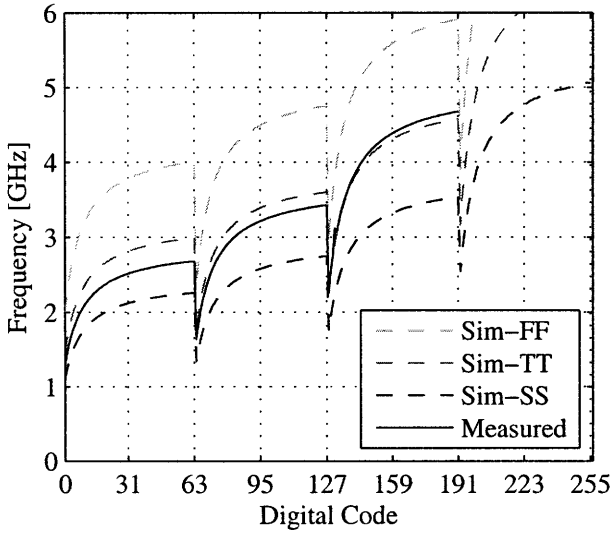

Figure 5-24: Simulated and measured center frequency of the pulse spectrum for all values of the delay code. The simulations are shown over process corners.

early as soon as a frequency in range is found. This time includes a 32-bit shift register interface between the FPGA and the IC. The delay line must be recalibrated periodically with fluctuations in temperature and power supply. During recalibration the transmitter only needs to search values around the last control setting and a full calibration is not required.

The transmitter was simulated, and the center frequency of the simulated pulse is shown in Figure 5-24 for the SS, TT, and FF corners, for each value of the 8-bit delay control value. Four regions are apparent in the graph, distinguished by discontinuities between the regions. These regions are the four capacitor bank settings, while the fine-tuning within each region is done with the 6-bit current starving control. These simulation results show the expected range in frequency of $\pm 30\%$ across process corners. Also plotted in Figure 5-24 is the center frequency of the measured pulse spectrum, plotted up to a delay value of 191. Results for delay control values above 191 are not shown because for these settings the IC is operating above the specification and does not properly combine edges from the delay line.

Pulses are generated by combining edges when the delay line is open-circuited

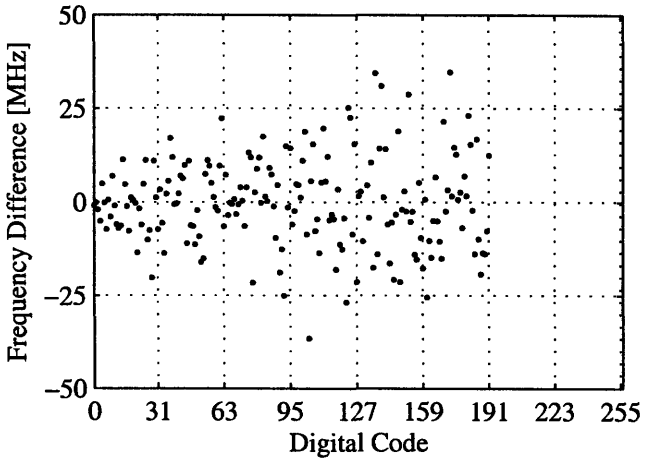

Figure 5-25: Difference between the pulse spectrum center frequency measured at the RF port, and the oscillation frequency when the delay line is configured as a ring oscillator when multiplied by 32.

at the end, whereas the delay/stage is calibrated by configuring the delay line as a ring oscillator and measuring the ring frequency. This relies on a measure of the ring frequency being an accurate prediction of the pulse center frequency after edge combining. The accuracy of the calibration is affected by unequal parasitic capacitance in the delay line as well as matching between stages. This accuracy was measured by configuring the delay line as a ring oscillator and simultaneously measuring the frequency of the ring and the center frequency of the combined pulse for each value of the delay control. The difference between the center frequency of the pulse spectrum and the ring frequency multiplied by 32 is shown in Figure 5-25. This plot shows that the accuracy of this method of calibration is $\pm 40MHz$, which is sufficient for the energy-detection receiver.

5.6.2 Pad Driver

During the time interval between pulses, the output driver stage idles in a high state with the output node strongly pulled high through a large PMOS device. The S_{22} shown in Figure 5-26 is measured during this idle state from the port indicated in Figure 5-20 which includes the off-chip filter. The deep notch in S_{22} at 2.8GHz

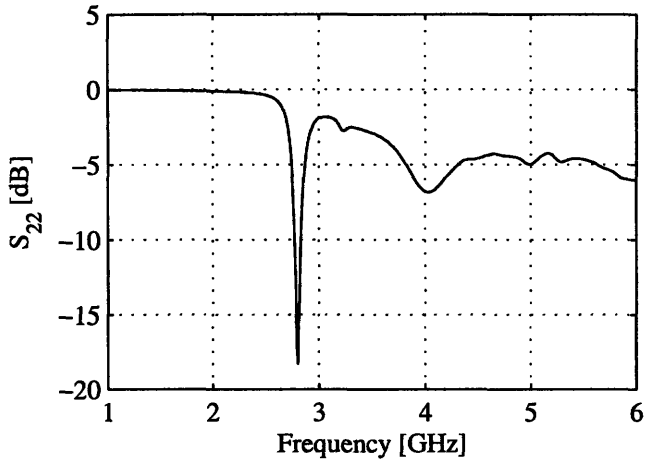

Figure 5-26: Measured S_{22} of the output driver.

is due to the frequency response of the off-chip filter. The driving impedance of the transmitter is less than 50Ω, typically between 7−12Ω, resulting in an S_{22} greater than -10dB. The transmitter therefore delivers *higher* power to the antenna than a matched driver with the same voltage headroom. This is significant, as the maximum available power from the transmitter is *the* limiting factor on link distance, as opposed to the FCC mask, for a low data rate system. Reflections off the transmitter should also be addressed. Consider an ideal source driving a transmission line that is terminated with it's characteristic impedance at the load end. In this case, there will be no reflections off the load end, and the source impedance should be 0Ω to deliver maximum power to the load. For a typical S_{11} of -10dB for a UWB antenna, this results in 10% of the power being reflected back to the transmitter. A transmitter S_{22} of -3dB results in 50% of the reflected wave returning to the antenna for a worst-case net pulse degradation of ±0.2dB. This is an acceptable loss, considering the reduced driving impedance of the transmitter increases the output pulse power by 0.7dB over a matched source.

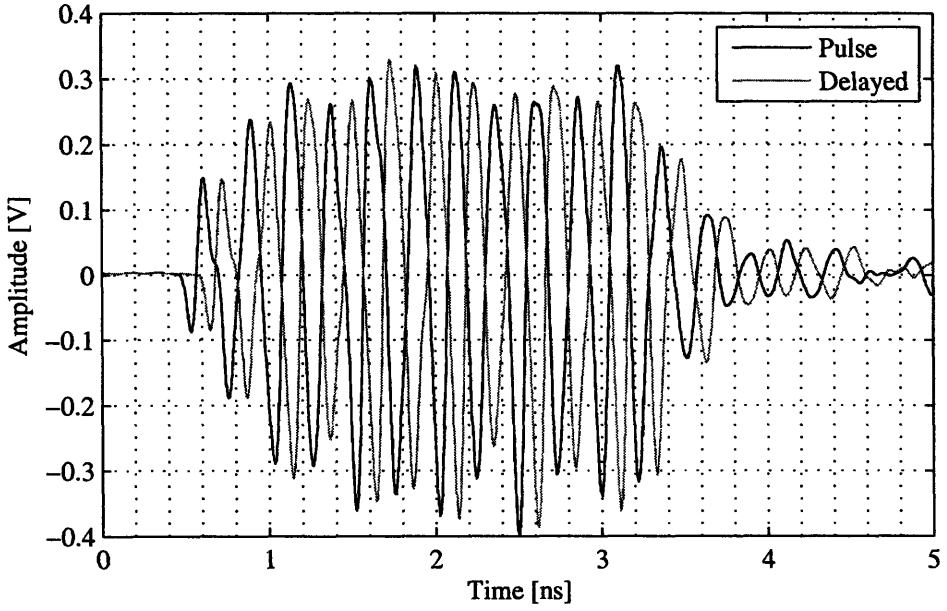

Figure 5-27: Measured DB-BPSK pulses with a center frequency of 4.05GHz. The two phases of the DB-BPSK pulses are superimposed, highlighting the $\frac{1}{2}f_{RF}$-cycle delay.

5.6.3 DB-BPSK Scrambling

Recall that DB-BPSK scrambles the output spectrum of PPM modulated pulses by randomly delaying the pulses by a half-period of the pulse center frequency. The delay/stage of the delay line is by definition equal to the required half-period shift between pulses. DB-BPSK is implemented in hardware by using two edge selection mask values that each select the same *number* of edges to be combined, but the edges used for combination are offset by one stage. The current mask is selected between these two mask values with a PN sequence at the pulse repetition frequency. The two phases of the measured DB-BPSK pulses are shown in Figure 5-27 with a pulse center frequency of 4.05GHz. The pulses are superimposed for easy comparison. These pulses appear to be inversions of each other, however by focusing on the beginning of the pulses, it is apparent that they are actually delayed by half of the RF cycle period.

The measured spectrum for PPM alone, and PPM with DB-BPSK scrambling

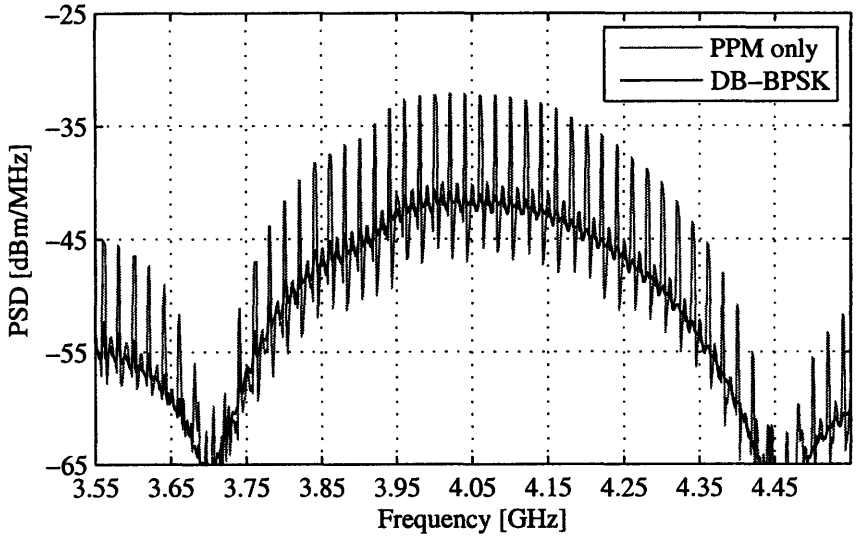

Figure 5-28: Measured spectrum for PPM pulses modulated by random data, and the same PPM pulses with DB-BPSK scrambling enabled.

enabled is shown in Figure 5-28. The PPM signal is modulated by random data; however, a line spectrum is still produced as predicted by the equations in Table 5.2. By applying random DB-BPSK scrambling to the same PPM modulated signal without making any other changes in the transmitter, the lines are eliminated in the main lobe. Notice that if scrambling is not used, the PPM spectrum exceeds the FCC mask and the transmitted energy/pulse would have to be reduced by 10dB in order to be FCC compliant. It is worth reiterating that DB-BPSK is implemented purely with digital hardware, and no analog inversion is required in the signal as for BPSK signaling. Additionally, scrambling of the PPM signal is transparent to the energy-detection receiver which is squaring the received signal; therefore, no additional decoding is required at the receiver end. Finally, DB-BPSK scrambling results in minimal losses in system performance.

5.6.4 Three-Channel Spectrum

The pulse spectrum was measured for each channel, and the results are superimposed in Figure 5-29 along with the FCC mask. DB-BPSK scrambling was enabled for these

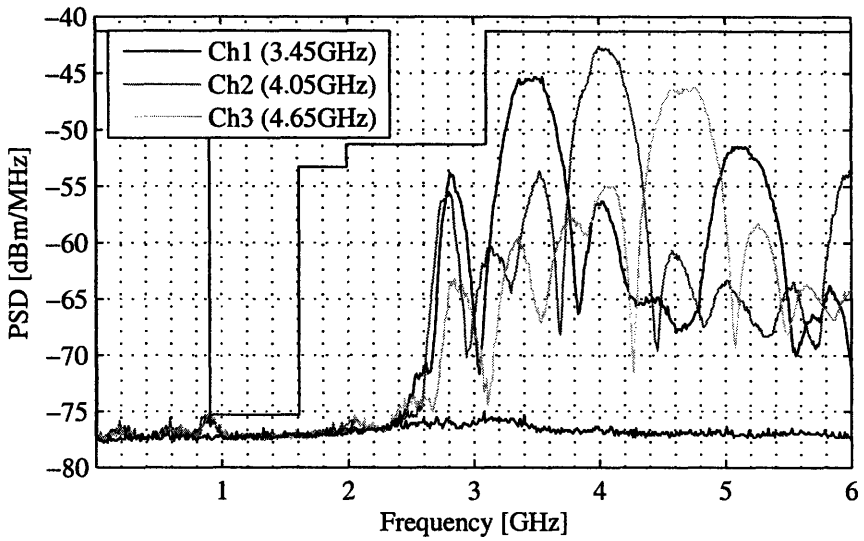

Figure 5-29: Measured spectra for the three channels.

three measurements. Due to a sub-harmonic of the pulse center frequency introduced by the interleaved edge combiners, the most difficult specification of the FCC mask to meet was the deep notch between 960MHz and 1.6GHz. The sub-harmonic of the lowest channel lies at 1.7GHz, and spectral content is produced there with a −10dB bandwidth of 550MHz. The off-chip band-select filter sufficiently attenuates the sub-harmonic to meet the mask.

The eight, linear-in-dB gain settings for channel 2 are shown in Figure 5-30. The gain is adjusted by scaling the strength of the NMOS pull-down network in the pad driver, while maintaining the same PMOS pull-up strength. This produces the desired output power adjustment, however the power saturates for the higher gain settings as shown in the plots.

5.6.5 Wireless Testing

A die photo of the transmitter is shown in Figure 5-31. The $0.8 \times 0.8\text{mm}^2$ chip is pad limited, and the active area is $0.2 \times 0.4\text{mm}^2$. Most of the active area is consumed by the delay line and control logic that configures the chip. A mix of digital components from a standard cell library and full-custom layout was used to implement the transmitter.

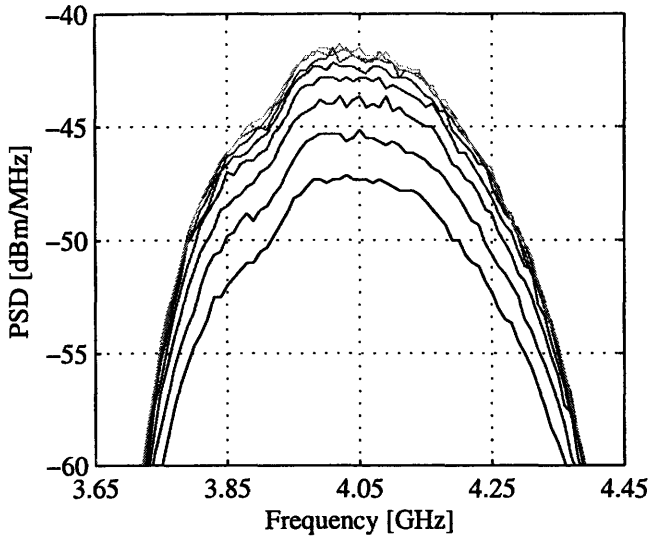

Figure 5-30: Measured spectra for each gain setting in channel 2 (4.05GHz).

Extensive metal fill was required across the chip, and was allowed over most of the active circuits. While custom layout and routing was require for this implementation, it is only one step away from a fully synthesizable UWB transmitter in a completely automated digital design flow.

Several transmitter nodes were built in order to test the all-digital transmitter with the energy-detection receiver in a complete wireless system. A photograph of the transmitter and FPGA board stack is shown in Figure 5-32. The FPGA implements the automatic calibration algorithm that centers the pulse spectrum in the desired channel. The FPGA board also supplies power to the transmitter IC from the USB bus for a portable solution. The antenna used for the wireless demonstration was a commercially available 3.1-5GHz UWB antenna. A receiver node was built using a similar board stack, with the FPGA implementing the packet acquisition and demodulation algorithms, and the custom receiver IC on a second board that directly interfaces to the FPGA. Both the transmitter and receiver interface to a PC using a USB bus. This interface is used to remotely control the nodes with a PC, and to upload and download packets to the nodes for wireless communication. With these nodes, a real-time wireless link was demonstrated at a data rate of 16.7Mb/s.

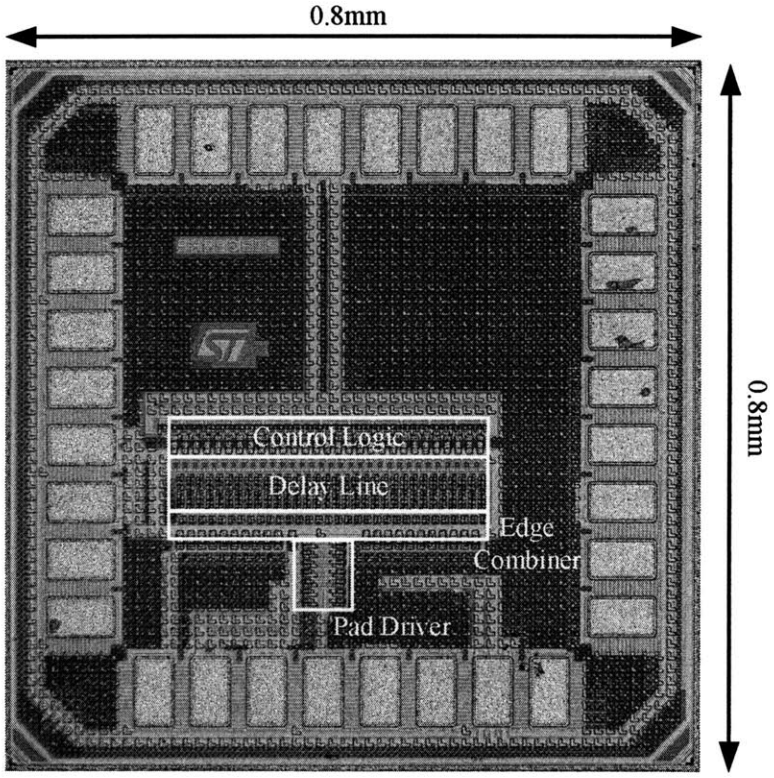

Figure 5-31: Die photo of the all-digital transmitter.

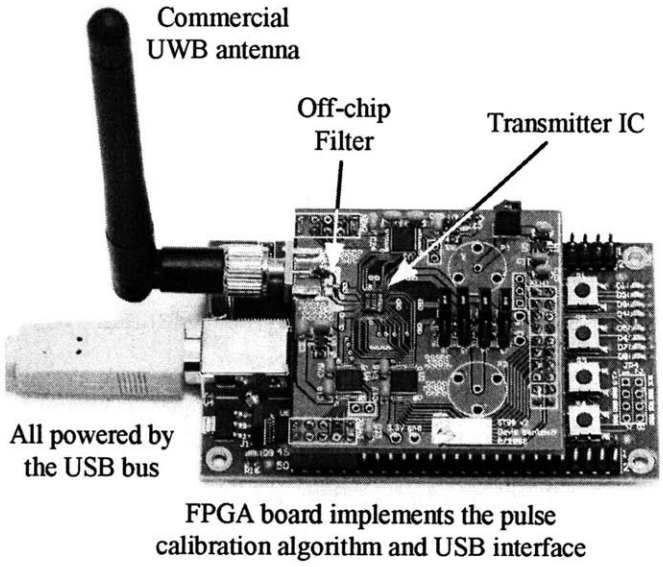

Figure 5-32: Photograph of the transmitter test board with FPGA for implementing calibration.

5.7 Conclusion

This transmitter demonstrated several concepts for generating UWB pulses with a spectrum tunable to three channels in the lower portion of the UWB band. Concepts such as DB-BPSK scrambling and the delay calibration algorithm rely on a delay-line-based transmitter architecture, and are amenable to an all-digital implementation. The digital architecture is desirable from an energy/bit perspective because for digital circuits, neglecting leakage, energy is *only* consumed by switching events which occur when a pulse is actually being synthesized. Otherwise, the circuits are idle and consume no static power during this time. Additionally, no analog bias voltages or currents are required. This can ultimately lead to a completely synthesizable transmitter using components purely from standard cell libraries with no custom layout required.

A summary of the transmitter performance is shown in Table 5.3. The PRF range quoted in this table of 10kHz to 16.7MHz is set by the operating range of the energy-detection receiver. The transmitter is capable of generating pulses at an arbitrarily low PRF, and theoretically up to 108MHz. The leakage power is $96\mu W$, and limits the energy/bit in the lower PRF range. Just the switching component (CV^2 losses) of the energy/pulse is 37pJ, regardless of the PRF. Summing the subthreshold leakage power and switching losses over the PRF range results in the an energy/bit of 9.6nJ to 43pJ.

Table 5.3: Performance Summary

Specification	Value	
Process	90nm CMOS	
Active Die Area	0.2x0.4mm^2	
Modulation	PPM+DB-BPSK	
PRF Range	10kHz to 16.7MHz	
Supply	1V	
	Standby Power	Active E/pulse
Buffer: Standby (Idle)	2.8μW (6.2μW)	13pJ
Delay Line and Edge Combiner	76.4μW	14pJ
Control	13.7μW	-
I/O and ESD	3.0μW	10pJ
Total	95.9μW	37pJ
Transmit Power per Channel		
Channel 1 (3.45GHz)	-18.4dBm	
Channel 2 (4.05GHz)	-17.1dBm	
Channel 3 (4.65GHz)	-19.3dBm	
Pulse repetition frequency (PRF)	10kHz	16.7MHz
Energy/pulse at PRF	9.6nJ	43pJ
Total power at PRF	96μW	713μW

Chapter 6

Conclusions

6.1 Thesis Summary

Ultra-wideband radio is suitable for a wide range of applications. UWB is uniquely positioned for using non-conventional radio architectures because of the amount of available bandwidth. Architectures for both high and low data rate transceivers have been presented in this thesis that focus on energy efficiency as the critical design constraint.

This thesis has investigated ways to shape and generate pulses optimally within the UWB band. For high data rate applications, pulse locality in the time and frequency domains is critical for minimizing inter symbol interference and adjacent channel interference, respectively. A Gaussian pulse shape is optimal for minimizing the pulse time-bandwidth product, however the shape is costly to generate with circuits and has several limitations that make it undesirable for implementing in UWB transceivers. A tanh pulse shaping technique has been demonstrated for accurately approximating a Gaussian pulse shape. The shaping technique exploits the exponential properties of a BJT differential pair. The core pulse shaping circuit can be combined with up-conversion mixing to the USB band. It also demonstrates how BPSK pulses may be inverted in RF, as opposed to baseband.

The power consumption in most short-range wireless systems is dominated by the electronics and not the transmitted power. This is particularly true for UWB

radios with a maximum transmit power allowed over the 3.1-10.6GHz band of only -2.5dBm. When the UWB band is divided in 500MHz channels, this transmit power reduces to -14.3dBm, or 37μW. Because power is dominated by the electronics, and with the amount of available bandwidth in the UWB band, it isn't necessary to be spectrally efficient for low data rate applications. In fact, if the spectral efficiency may be sacrificed for reduced power consumption in the electronics, this can drastically reduce the overall system power consumption.

A low data rate transmitter architecture has been presented that exploits the available bandwidth to reduce power consumption. An all-digital architecture is made practical by relaxing the frequency tolerance and spectral efficiency requirements, suitable for use with an energy detection receiver [68]. Power is only consumed in subthreshold leakage currents and CV^2 switching losses, and no analog bias currents are required. The pulse spectrum is programmable in center frequency and pulse width, supporting a three-channel frequency plan from 3.1-5GHz. In order to center the pulse spectrum in the desired channel, a digital calibration technique using a successive approximation algorithm is used. No RF oscillator is required by the transmitter; therefore, there is no startup time for generating pulses.

The low data rate transmitter communicates with an energy detection receiver using pulse position modulation (PPM) [68]. The form of PPM used is known to produce a spectrum with line, even when modulated by purely random data. Therefore, some form of spectrum scrambling is required. BPSK scrambling is typically used in addition to PPM to eliminate the tones; however, BPSK is costly to implement in an all-digital architecture. In this thesis, a spectrum scrambling technique termed delay-based BPSK (DB-BPSK) is presented that can be implemented in the all-digital transmitter with minimal overhead. DB-BPSK has been shown to produce the same scrambling effect as BPSK, and has been demonstrated in the low data rate transmitter.

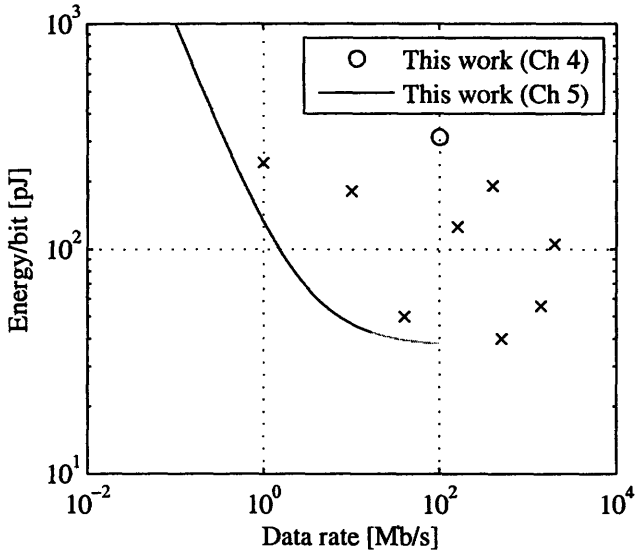

Figure 6-1: Comparison of this work to previously published UWB transmitters [11, 20, 24, 30–32, 97, 98].

6.2 Conclusions

In conclusion, the hardware required to generate UWB pulses must be considered when defining system specifications. The power consumption in pulsed-UWB transmitters in particular can be drastically reduced by relaxing the RF specifications. For many UWB applications, relaxed RF specifications are acceptable due to the large amount of available bandwidth. This has been demonstrated with the techniques presented in this thesis, such as the tanh approximation, synthesis from a delay line and edge combiner, and DB-BPSK scrambling.

The energy/bit of the UWB transmitters presented in this thesis are compared to previously published transmitters in Figure 6-1. The all-digital transmitter has the lowest energy/bit for the data rates compared. This curve is shown in black up to 16.7Mb/s, and extended in gray to 100Mb/s. The 16.7Mb/s limit is imposed by the energy detection receiver, but the transmitter supports a PRF up to 100MHz. In pulsed-UWB systems, the energy/bit in the receiver is on the order of 1-10nJ/bit [50]. The energy/bit of pulsed-UWB transmitters is therefore typically 2 orders of magnitude lower than in the receivers, making pulsed-UWB advantageous for transmit-

dominated applications.

6.3 Future Work

UWB radios for low data rate applications such as wireless sensor networks and implantable devices remain and active area of research. Low power, and low data rate radios are required to interface remote sensors with low bandwidth to centralized data analysis locations. In biomedical applications, devices are mostly interested in relaying information out of the body, and resources for reception of the transmitter signals are for all practical purposes, unlimited. UWB is a viable solution for transmit dominated applications, because transmit power levels are typically 2-3 orders of magnitude lower than receiver power levels in pulsed-UWB chipsets.

The low data rate transmitter presented in this work uses and all-digital architecture with full-custom layout. Custom layout requires a redesign whenever a change in specifications is made, which consumes resources and is prone to errors. An all-digital transmitter, by definition, should be able to be described using a hardware description language such as verilog. This would enable the transmitter to be completely synthesized, with layout performed using existing place and route algorithms. This would introduce mismatch in delay paths; therefore, additional calibration in the form of a built-in self test would be required. While this is certainly possible in deep-submicron processes, current synthesis tools do not support the ability to describe "analog" blocks. What is needed is a tool to add the functionality to describe a digitally controlled VCO or delay line to existing synthesis tools. This would allow an all-digital transmitter to be completely synthesized, and potentially implemented on an FPGA for maximum reconfigurability.

DB-BPSK modulation has been implemented in this thesis solely for scrambling a PPM signal for use with an energy detection receiver. DB-BPSK may also be used as the primary modulation for communicating data with a coherent receiver as a substitute for BPSK. The performance of a DB-BPSK transmitter in a coherent system has been analyzed and compared to a BPSK transmitter in this thesis. The

loss in terms of SNR was shown to be less than 0.2dB, which is well within the link margin of most UWB systems. In order for this to be practical, the frequency specifications of the transmitter must be tightened to operate with a coherent receiver. This would require more than simply increasing the resolution of the digital delay control in the low data rate transmitter. However, several of the techniques presented in this thesis apply to the design of a coherent UWB system using DB-BPSK as the only form of modulation.

Finally, for data rates below roughly 5Mb/s, the transmit power for the all-digital transmitter becomes limited by the 1V power supply and no longer by the FCC mask. A higher power pad driver is required in order to maximize transmit power at these rates. This can be achieved using techniques such as higher voltage I/O devices, or by an impedance transform of the load impedance.

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