# Electrical Degradation Mechanisms of RF Power GaAs PHEMTs

by

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## Abstract

GaAs Pseudomorphic High-Electron Mobility Transistors (PHEMTs) are widely used in RF power applications. Since these devices typically operate at high power levels and under high voltage biasing, their electrical reliability is of serious concern. Previous studies have identified several distinct degradation phenomena in these devices, but a complete picture has yet to be formed.

In this study, we have carried out a comprehensive study of the mechanisms of electrical degradation on a set of experimental RF power GaAs PHEMTs (non-commercial devices provided by our sponsor, Mitsubishi Electric). A wide variety of electrical stressing experiments employing different conditions (varying temperature, bias, environment) were performed on these devices in order to monitor their degradation with stressing.

Our general observations showed several forms of degradation, the most concerning being an increase in the drain resistance $R_D$ and a reduction in maximum drain current $I_{max}$. Contrary to what is often claimed in the literature, our experiments indicated that these forms of degradation were *not* driven by impact-ionization or hot-electron effects. Instead, we found the degradation to be strongly correlated with temperature, stressing environment, and drain-gate bias, which were all consistent with a corrosion mechanism. Via materials analysis we were able to confirm that the degradation of both $R_D$ and $I_{max}$ were due to surface corrosion on the drain side of the device, albeit at different specific locations. The increase in $R_D$ was attributed to oxidation on the n+GaAs ledge, while the reduction in $I_{max}$ was due to oxidation on the AlGaAs surface, closer to the gate.

A recoverable negative shift in the threshold voltage $V_T$ and a permanent decrease in $R_S$ were also observed during electrical stressing. The shift in $V_T$ was attributed to field-assisted tunneling of electrons out of traps under the gate, while the decrease in $R_S$ was found to be consistent with recombination-induced annealing of defects on the source side of the device.

Measurements were also performed to observe light emitted from the device during electrical stressing. The observed light-emission indicated that device degradation was proceeding in a highly non-uniform manner across the width of the device, due to a non-uniform electric field distribution. We attributed this to a non-uniform recess geometry across the device width. This suggested that it is important to ensure uniform geometry across the device width, in order to minimize non-uniformities in electric field distribution and enhance device reliability.

The physical understanding developed in this work should be instrumental to identifying and addressing future reliability issues in RF power GaAs PHEMTs.

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I see the atoms, free and fine,
That bubble like a sparkling wine;
I hear the songs electrons sing,
Jumping from ring to outer ring
–Lister *The Physicist*

*para mi familia*

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# Chapter 1

# Introduction

## 1.1 Background

GaAs Pseudomorphic High-Electron Mobility Transistors (PHEMTs) have been gaining popularity for use in RF power applications for wireless systems. Due to their high frequency response, GaAs PHEMTs are important devices for power amplification in cell phones, base stations, and satellite communication systems. However, significant reliability issues in these devices need to be addressed before they can realize their full potential in such applications.

The devices studied in this research are pseudomorphic HEMTs, as the layers forming the active structure of the device have slightly different equilibrium lattice constants (introducing strain in the channel layer). In PHEMTs, InGaAs (rather than GaAs) is used for the channel material, as the addition of indium decreases the bandgap and thus increases the channel mobility [1]. Fig. 1-1 shows a sketch of a typical PHEMT structure. In this schematic, the undoped channel layer lies between two very thin highly-doped layers which are separated by an undoped spacer layer. The thin"supply" layers provide the carriers that form a two-dimensional electron gas (2DEG) in the channel, and the spacer regions ensure that the 2DEG is separated from ionized donors in the supply layers.

The energy-band diagram of this type of device is shown in Fig. 1-2. Due to the large bandgap difference between AlGaAs and InGaAs, narrow triangular quantum wells are formed in the InGaAs

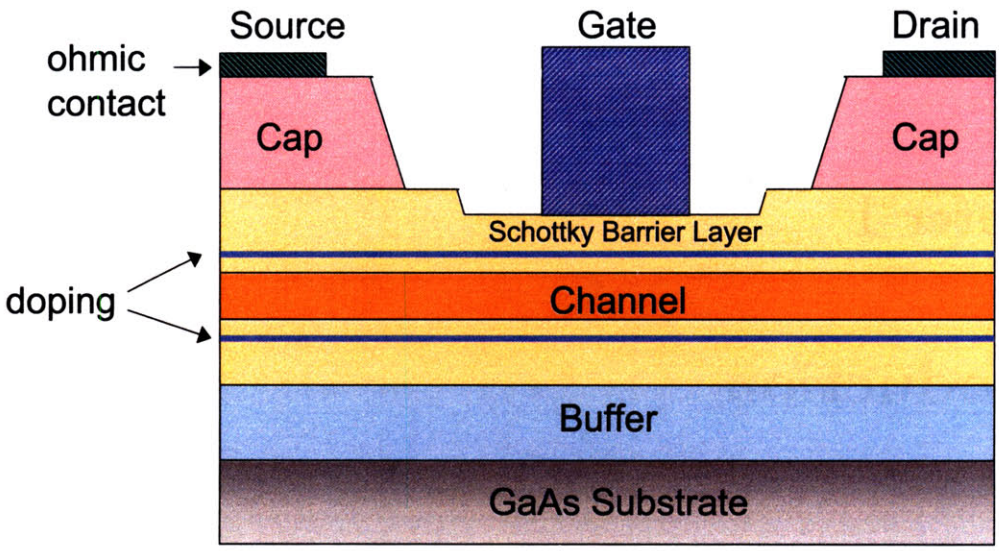



Figure 1-1: Sketch of double-recessed, double-heterojunction pseudomorphic HEMT structure on GaAs substrate.

channel near the AlGaAs/InGaAs interfaces, thus confining the electrons there to very thin sheets of charge (the 2DEGs). Since they are separated from their parent donor ions, the electrons in the 2DEG do not experience ionized-impurity scattering and thus exhibit enhanced mobilities [2]. The undoped AlGaAs spacer layers help to further isolate the 2DEG from the doped supply layers, resulting in even higher electron mobilities (with a compromise of decreased electron density in the 2DEG). Typical HEMTs have 2DEG sheet carrier densities on the order of $10^{12}$ $cm^{-2}$ [2]. Depending on the spacer thicknesses, indium content and other factors, GaAs PHEMTs with InGaAs channels have been typically found to have room-temperature mobilities from around 4,000 to 8,000 $cm^2/Vs$ [3,4]. Such high mobilities gives these devices their high frequency response, allowing their use in various high-speed applications.

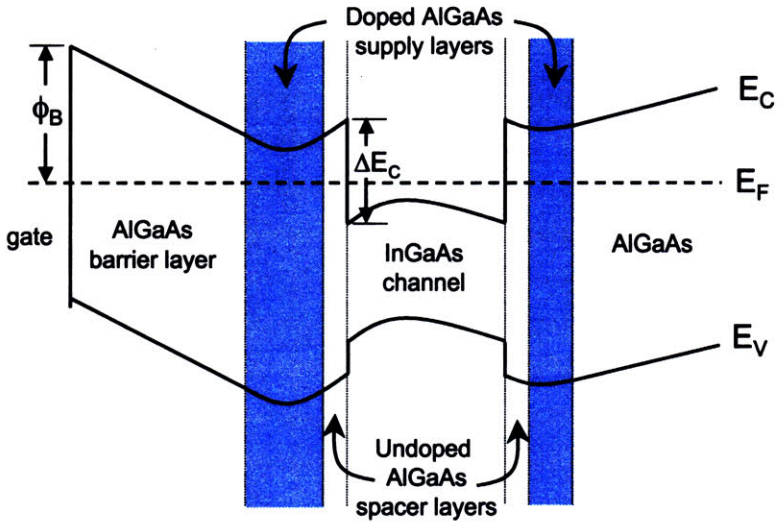
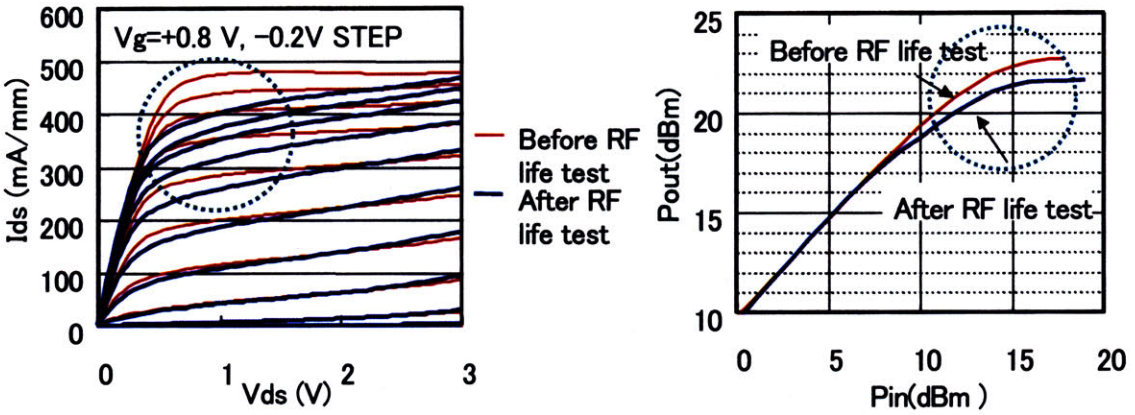



Figure 1-2: Energy band diagram of a double-heterojunction pseudomorphic HEMT.

## 1.2 Motivation

The high-power device applications of GaAs PHEMTs (as mentioned in the previous section) require severe and prolonged biasing conditions, which cause the devices to gradually degrade over time. Therefore the electrical degradation of RF power GaAs PHEMTs is of serious concern. The degradation is usually observed via an increase in the drain resistance $R_D$ and a decrease in the maximum drain current, $I_{max}$. This poses a problem because it results in a decrease in overall output power [5–7], as illustrated in Fig. 1-3.

Previous research on GaAs PHEMTs has attributed this degradation to various mechanisms, such as impact-ionization, electron-trapping, and surface corrosion [5–8]. However, complete details of the underlying physical mechanisms have not been totally spelled out. The overall picture of electrical degradation is somewhat confused by the simultaneous presence of other side effects of stressing (such as thermal effects, like self-heating, or environmental effects, such as hydrogen poisoning [9,10]). Furthermore, there are still reliability issues that are missing a thorough analysis. To date, there have been no studies examining the degradation across the width of the device (reliability studies have always assumed that degradation occurs uniformly across the device width).




(a) (b)

Figure 1-3: (a) DC characteristics of an AlGaAs/InGaAs PHEMT, before and after RF life test ($T_{channel}$ = 150°C, $V_{DS}$ = 5 V, $f$ = 18 GHz, 2000 hrs). (b) RF characteristics of same device, before and after RF life test. From [7].

This is also important to investigate because it is unclear how non-uniformities in degradation across the width of the device can impact device reliability.

## 1.3 GaAs PHEMT Reliability

In GaAs PHEMTs, several different mechanisms have been identified to be responsible for various types of device degradation. This section will discuss the main mechanisms that have been observed and discussed in the literature so far. Here the mechanisms are organized by the primary physical location of the degradation: the drain, gate, and source.

### 1.3.1 Drain

The region between the drain and the gate is of utmost concern in PHEMT reliability, largely due to the high electric field present under typical operating conditions. Hot electron degradation is the most widely reported failure mechanism of PHEMTs [11], so it is crucial to monitor the presence of hot electrons and other effects of the high electric field in the drain region. An important figure

of merit here is the drain resistance $R_D$, which gives an indication of the resistivity of the drain ohmic contact and the gate-drain access region. Since GaAs PHEMTs are widely used in RF power applications, the related RF figure of merit $I_{max}$ (measured as maximum drain current near the knee drain voltage) has become of greater significance. Thus degradation on the drain side of usually observed via an increase in $R_D$ and a decrease in $I_{max}$.

There have been numerous studies on the drain degradation of GaAs PHEMTs. Probably the most common explanations involve some kind of electron trapping in the region between the gate and drain. Many have proposed that impact ionization on the drain side of the device (due to the high electric field) generates hot electrons which create traps in the drain access region [6,12]. This is schematically illustrated in Fig. 1-4. The trapped negative charge thus reduces the sheet carrier concentration ($n_s$) in the extrinsic drain, thus causing the increase in $R_D$ and a decrease in $I_{max}$. And since the negative charge effectively widens the depletion region and decreases the peak electric field, this form of degradation is usually accompanied by an increase in the device breakdown voltage (commonly referred to as *breakdown walkout* [13]). As for the specific location of the traps, one such theory found evidence of the trapping to occur at an interface [8]. Another theory claimed that electrons are injected and trapped in the *passivation layer* above the drain access region [5,14]. In [14], it was found that in the early stages, the charge trapping in the passivation layer was reversible via thermally-activated emission of the trapped charge. This reversible degradation is referred to as *power drift*. In more advanced stages, the charge trapping becomes irreversible (this is referred to as *power slump*). In any case the symptoms of the resulting degradation were very similar: an increase in $R_D$ and $BV_{DG}$ and a decrease in $I_{max}$ and $P_{out}$. Also, this type of degradation has been found to *decrease* with higher stressing temperatures [12], indicating a close correlation with impact-ionization and/or hot electron temperature, which have negative temperature dependence in these devices.

In contrast to these trap-related theories, another explanation for the $R_D$ and $I_{max}$ degradation involves the *corrosion* of the semiconductor surface between the gate and drain [7]. This is illustrated schematically in Fig. 1-5. This degradation is found to be more closely correlated to the stressing drain current and temperature than to impact-ionization, and is found to be accelerated

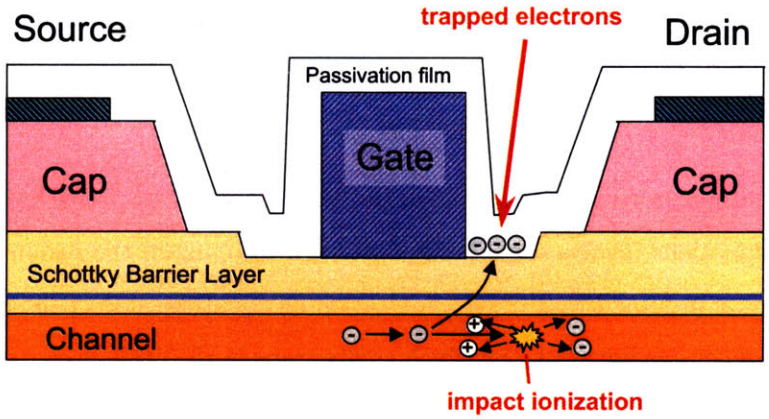



Figure 1-4: Schematic illustration of PHEMT with trapped electrons in drain access region, caused by hot electrons generated by impact-ionization on drain end of channel (discussed in [5,6,12–14]).

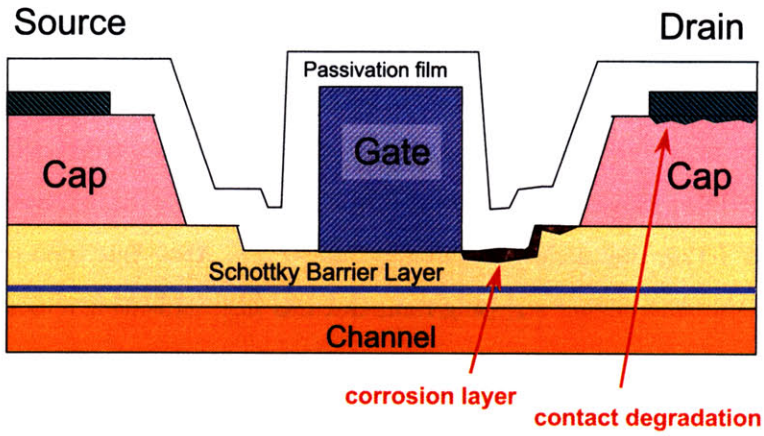



Figure 1-5: Schematic illustration of PHEMT with corrosion degradation (discussed in [7]) and ohmic contact degradation (described in [15,16]) affecting drain side of device.

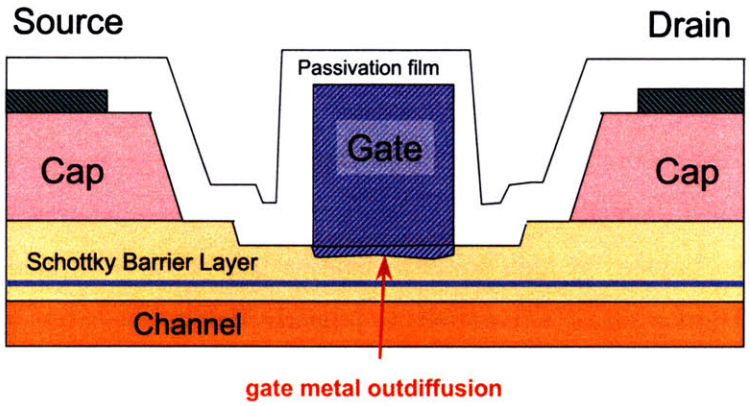



Figure 1-6: Schematic illustration of PHEMT with gate metal outdiffusion into barrier layer (discussed in [18]).

in an air environment [7, 17]. A special treatment to the semiconductor surface before passivation has been found to be effective in suppressing this type of degradation.

Increases in $R_D$ have also been attributed to ohmic contact degradation (also illustrated in Fig. 1-5.). Evidence of this has been observed under unbiased high-temperature storage tests [15] and under DC bias life tests with high channel temperatures [16]. The contact degradation mechanism is basically due to metal-semiconductor interdiffusion, and is mainly thermally activated [15]. Since temperature is the main accelerating factor for this mechanism, contact degradation typically affects the source as well as the drain (resulting in increases in both $R_S$ and $R_D$) [15, 16].

### 1.3.2 Gate

Aside from trapped charge modulation (see last paragraph in this section), the majority of degradation mechanisms affecting the gate appear to be due to either thermal or environmental effects. However, since such effects can be present under typical electrical stressing conditions, it is important to be aware of them and their effects on device characteristics.

Probably of greatest concern is gate sinking, a thermally-activated mechanism which refers to the gradual interdiffusion of the Ti gate metal into the semiconductor. This is schematically illustrated in Fig. 1-6. The effect is a positive shift in the threshold voltage $V_T$, which thus causes a

decrease in $I_D$ (and therefore a decrease in output power). Due to the smaller distance between the gate metal and the channel, an increase in the peak transconductance $g_{mpeak}$ is sometimes also observed [18]. Since the interdiffusion mechanism typically has an activation energy around 1.4-1.6 eV, its presence usually requires relatively high temperatures [11]. But even under room-temperature electrical stressing, such thermal effects can be present, due to high channel temperatures (possibly as high as 100°C) induced by high power dissipation [19]. Thus while analyzing degradation behavior under electrical stress, it is important to properly identify the effects of gate sinking and isolate them from mechanism directly relating to the electric field.

Other degradation mechanisms involving the gate metal in GaAs PHEMTs have been attributed to environmental effects, such as hydrogen poisoning. Hydrogen is typically out-gassed from hermetic packaging materials, or it can be left over from PECVD dielectric deposition [20]. The main effect of hydrogen is its reaction with the Ti metal to form TiH [9]. This is a reliability concern because the formation of TiH creates tensile stress in the semiconductor heterostructure that shifts $V_T$. Since this involves a piezoelectric effect, the sign of the $V_T$ shift depends on the length and the orientation of the gate [10]. The conditions in which hydrogen degradation is readily observed involve relatively high temperatures, and so its effects must also be tested for and isolated from thermal and/or environmental effects in analyzing effects of electrical stress.

Another set of mechanisms pertaining to the gate region involves the neutralization of trapped charge under the gate. The mechanism can be either thermal (trapped electrons gaining enough energy to escape) or electrical (holes generated from impact ionization recombining with the trapped electrons) [21]. In both cases, this has the effect of creating a negative shift in $V_T$ (and thus increasing $I_D$). Since these mechanisms involve the filling and emptying of traps, their effects tend to saturate with stressing and are mostly recoverable with room-temperature storage [12,21]. This effect has been observed in electrical stressing at room temperature, as well as under high-temperature storage [21].

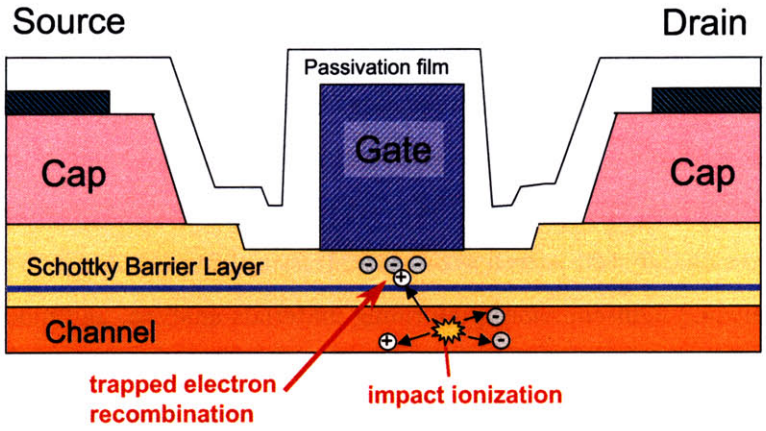



Figure 1-7: Schematic illustration of PHEMT with trapped electrons under gate recombining with hot holes generated by impact-ionization on drain end of channel (discussed in [12,21]).

### 1.3.3 Source

In terms of electrical reliability, the source region is of relatively minor concern, since the electric field in the source-gate region is much smaller than in the drain-gate region under normal biasing conditions. The main figure of merit here is the source resistance $R_S$, which gives an indication of the resistivity of the source ohmic contact and of the source-gate access region. In the early days of HEMT reliability studies, $R_S$ (along with $R_D$) was reported to increase significantly under stress, which was eventually attributed to ohmic contact degradation, as a result of temperature-induced metal-metal or metal-semiconductor diffusion [15]. However, since then commercial HEMTs have employed effective barrier layers to prevent this from happening [11]. Thus, in more recent studies, $R_S$ has been reported to either remain unchanged [22] or decrease slightly [12,21] under prolonged electrical stress. The slight decrease in $R_S$, when observed, has been attributed to thermally-activated detrapping of electrons in the source-gate access region [21], and has been generally found to be recoverable. However, significant *permanent* changes in $R_S$ (reductions of almost 10%) have also been observed [17], and despite its association with an increase in sheet carrier concentration on the source side of the device, the details of the underlying mechanism are unclear.

## 1.4 Thesis goals and outline

The goal of this thesis is to deepen the understanding of fundamental degradation mechanisms in RF power GaAs PHEMTs. We seek to accomplish this via a systematic investigation of the degradation of experimental RF power PHEMTs under prolonged electrical stress. By examining various types of stressing (off-state as well as on-state stressing, nitrogen and hydrogen environments as well as air), analyzing light-emission, performing materials analysis, and modeling degradation in these devices, we hope to identify the physical mechanisms responsible for degradation in GaAs PHEMTs. Once this is done we can then make suggestions for device design that will mitigate electrical degradation and thus improve reliability.

This thesis will be organized in the following manner. Chapter 2 describes the experimental stress and measurement setup used to perform electrical stressing experiments on the PHEMTs. This chapter describes our device characterization suite used to monitor the various device figures of merit while the device is under stress. The bias stressing scheme used to stress the devices is also explained. This chapter summarizes the findings previously discovered using this setup (in S.M. thesis) and concludes with the various issues that need further investigation.

In Chapter 3, we first present the overall results of the bias-stressing experiments, which illustrates the main forms of degradation and the unresolved issues in each case. This chapter focuses on the degradation associated with the drain side of the device, namely the increase of $R_D$ and decrease of $I_{max}$. The results of various electrical stressing experiments investigating the effects on degradation due to environment, bias voltage, bias current, and temperature are discussed. The time evolution of degradation is also examined and the electrical degradation is correlated with damage observed via materials analysis (STEM, EDX) of degraded devices. This chapter is concluded with a summary of the findings from these experiments and proposed mechanisms for the degradation.

Chapter 4 discusses the mechanisms behind two independent forms of degradation associated with the gate and source side of the device, namely the negative shift in $V_T$ and the decrease in $R_S$. For each case, the time evolution of the degradation and its dependences on environment,

electric field, impact-ionization, and temperature are all investigated, and a proposed mechanism is presented.

Chapter 5 contains a description of our light-emission experiments performed on the PHEMTs, done in order to obtain a spatial picture of carrier recombination and electric field under stressing. The experimental setup and the overall results from these light-emission experiments are described. This chapter also contains materials analyses of devices that explain the origin of the light-emission pattern observed. This chapter concludes with a summary of the findings from the light emission experiments and corresponding analyses, which makes a correlation between device geometry and light-emission behavior and the mentions the possible consequences for device reliability.

Finally, in Chapter 6, the conclusions of this work are presented with all the degradation mechanisms identified in this study. The results of our findings are compared and contrasted with observations reported in the literature. This section also contains some suggestions for the suppression of these degradation mechanisms.

# Chapter 2

# Experimental

## 2.1 Device Technology

We will start by describing the devices that are studied in this research. A schematic cross-section of the PHEMTs under study is shown in Fig. 2-1. These PHEMTs are non-commercial, experimental devices that were designed and fabricated by Mitsubishi Electric. The active channel is made of InGaAs, which is sandwiched between two thick layers of undoped AlGaAs. Within each intrinsic AlGaAs layer, there is a thin heavily-doped AlGaAs electron supply layer, which provides the carriers in the channel. The device has a double-recessed T-gate structure of length $L_g = 0.25$ $\mu$m. $L_{rs}$ and $L_{rd}$ both range from 0.2 $\mu$m to 0.9 $\mu$m. However, the main type of device studied (referred to as a "standard-parameter" device) has $L_{rs} = 0.4$ $\mu$m and $L_{rd} = 0.5$ $\mu$m. The various gate widths of the devices studied are $W_g = 40$ $\mu$m (2 fingers of 20 $\mu$m each), $W_g = 100$ $\mu$m (2 fingers of 50 $\mu$m each), and $W_g = 160$ $\mu$m (4 fingers of 40 $\mu$m each). Single-gate-finger devices of $W_g = 50$ $\mu$m were also available.

A typical virgin device has a current-gain cutoff frequency $f_T$ around 40-50 GHz. For a standard-parameter device, a typical value for the drain resistance $R_D$ is 0.7 $\Omega$-mm, while a typical source resistance $R_S$ is around 0.6 $\Omega$-mm. The threshold voltage $V_T$ typically ranges from -0.6 to -0.7 V, and the drain current at $V_{GS} = 0$ V and $V_{DS} = 1.2$ V is $I_{Dss}$ =200 mA/mm. The drain current near the knee voltage (usually known as $I_{max}$ in PHEMT power applications) is measured at $V_{GS} = 0.8$ V

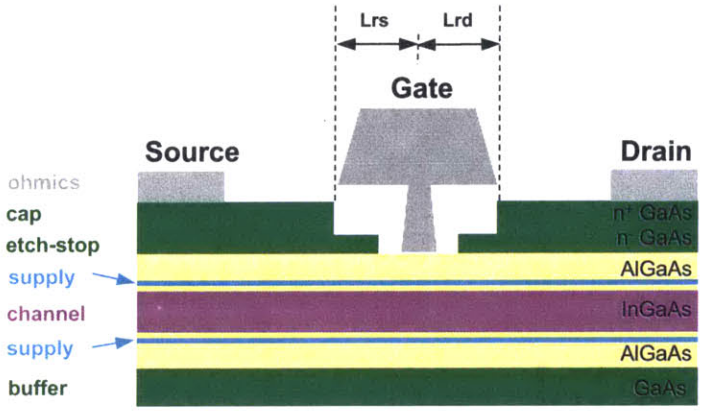



Figure 2-1: Schematic cross-section of GaAs PHEMT under study. $L_{rs}$ and $L_{rd}$ are the distances between the center of the gate to the edge of the n+ GaAs cap on the source side and on the drain side, respectively.

and $V_{DS} = 1.0$ V and is typically $I_{max} = 470$ mA/mm. The off-state breakdown voltage $BV_{DGoff}$ ranges from 12 to 16 V.

## 2.2 Stress and Measurement Setup

To investigate the degradation of these PHEMTs we employed a specially-designed stress and measurement setup, which had been developed in [23]. This setup employed an automated bias-stressing program (written in HP VEE) which allowed us to stress a device under a variety of conditions, while monitoring its key figures of merit. By this means we were able to evaluate device performance during electrical stress degradation.

### 2.2.1 Experimental Setup

The device under test is probed on a Cascade Microtech probe station, using Picoprobe GSG 150 $\mu$m microwave probes. A chamber encloses the chuck and test area containing the probes and the sample, which provides shielding from light and allows gases (such as nitrogen and forming gas) to be pumped into the chamber. The 8-inch chuck is connected to a Temptronix TP03000A temperature-

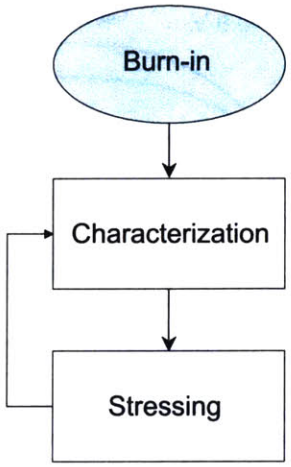



Figure 2-2: Flowchart illustrating the in-situ characterization of the device in a bias-stressing experiment.

controller, which allows us to set the ambient temperature of the stressing environment. A Windows PC running HP VEE controls an HP4155A Semiconductor Parameter Analyzer, which is used to electrically stress the device as well as characterize it.

Once this entire setup is in place, the stressing program is first calibrated to factor out external series resistance of the system in its measurements. After the probes are placed on the device, the device undergoes a one-time burn-in measurement (described in Section 2.3.3 of [23]) in order to quickly exhaust any initial fast transients that typically occur with repeated measurements on a new device. Once the burn-in is completed, the bias-stressing program is executed, which stresses the device for extended periods of time, while characterizing the device at frequent intervals. This flow of events is shown schematically in Fig. 2-2.

### 2.2.2 Device Characterization

The device under test is characterized by means of a comprehensive device characterization suite. The measurements in this suite are careful to implement relatively low voltages and currents, so that the characterization suite itself does not introduce any degradation to the device [23]. The

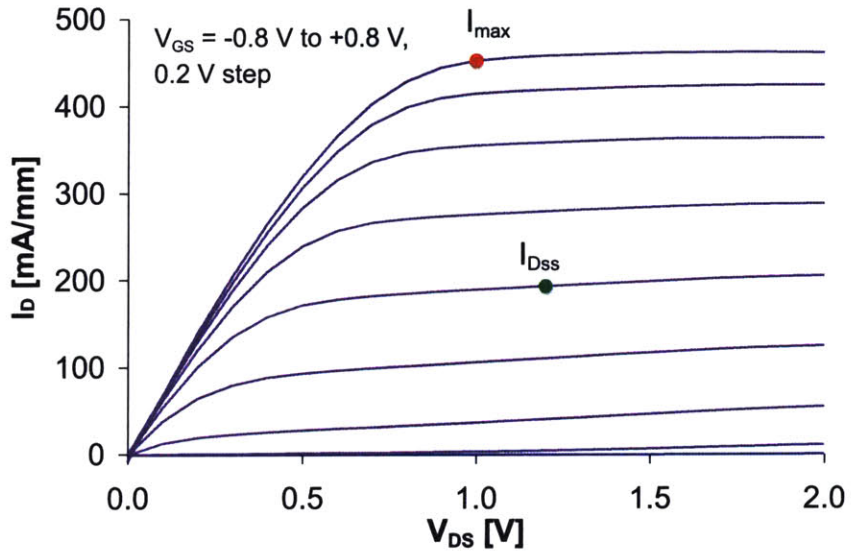



Figure 2-3: Output characteristics of a standard-parameter, virgin PHEMT. $W_g = 160\mu$m. Measurements taken at room temperature. Red point indicates where $I_{max}$ is measured ($V_{GS} = 0.8$ V, $V_{DS} = 1.0$ V), green point indicates where $I_{Dss}$ is measured ($V_{GS} = 1.0$ V, $V_{DS} = 1.2$ V).

characterization suite obtains the output, transfer, and subthreshold characteristics of the device under test, in addition to extracting several key parameters (including source and drain resistances, maximum drain current, threshold voltage, and off-state breakdown voltage). The specifics of all the individual measurements performed in the suite are detailed in [23]. Fig. 2-3 shows a typical set of output characteristics for a virgin PHEMT, taken at room temperature, with the measurements for $I_{Dss}$ and $I_{max}$ indicated on the plot. Fig. 2-4 shows a set of transfer characteristics taken on the same device. The subthreshold characteristics are shown in Fig. 2-5. For the measurement of off-state breakdown voltage, $BV_{DG,off}$, the drain-current injection technique, as described in [24], was used. A small positive current is injected into the drain, while $V_{GS}$ is swept from zero to negative bias. $BV_{DG,off}$ is then measured as the drain-to-gate voltage corresponding to the maximum $V_{DS}$ (see Fig. 2-6).

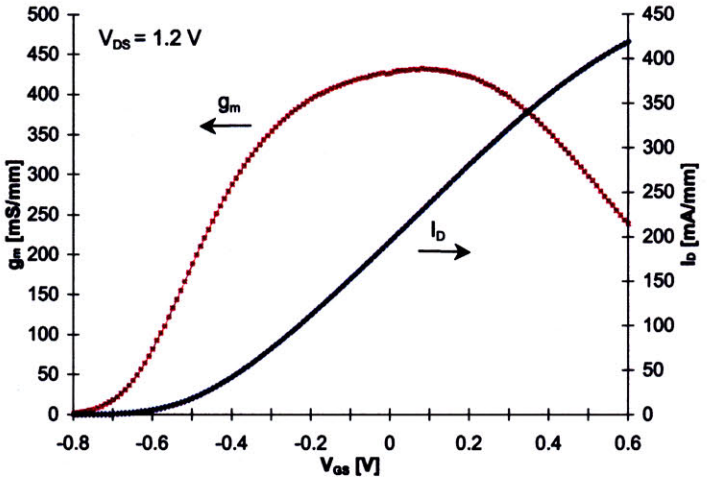



Figure 2-4: Transfer characteristics of a standard-parameter, virgin PHEMT. $W_g = 160\mu$m. Measurements taken at room temperature.

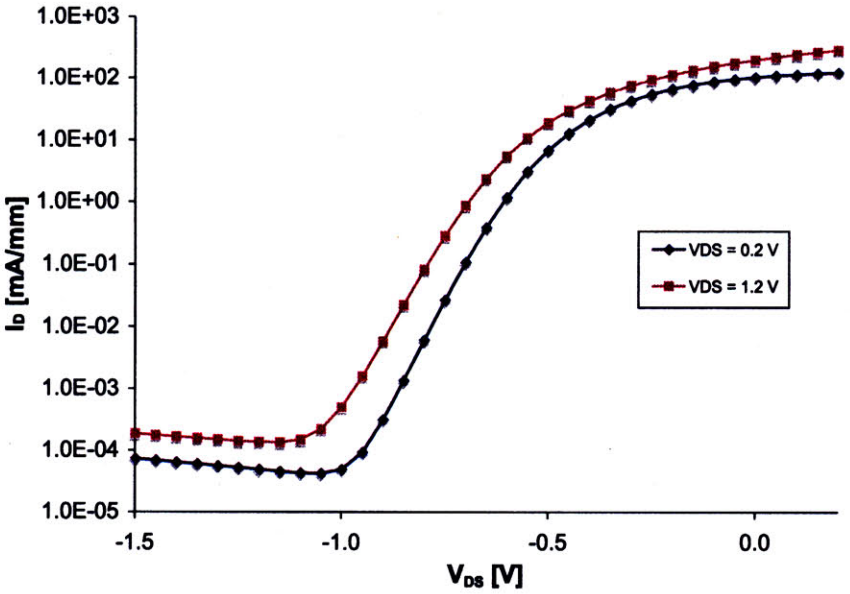



Figure 2-5: Semi-log plot of subthreshold characteristics of a standard-parameter, virgin PHEMT. $W_g = 160\mu$m. Measurements taken at room temperature.

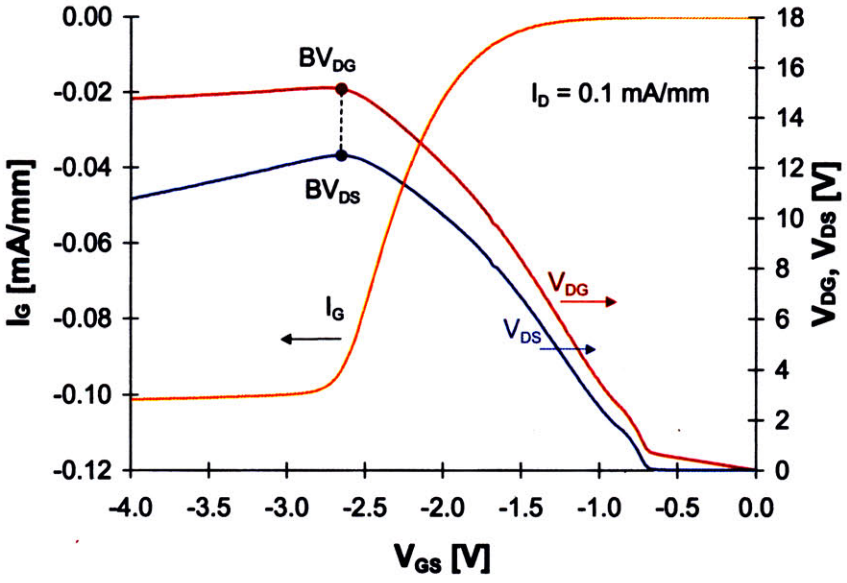



Figure 2-6: Measurement of the off-state breakdown voltage of a standard-parameter, virgin PHEMT, using the drain-current injection technique [24]. $BV_{DG,off}$ is measured as the $V_{DG}$ corresponding to maximum $V_{DS}$. $W_g = 160\mu$m. Measurements taken at room temperature.

### 2.2.3 Electrical Stressing Methodology

Since previous research [5, 6, 12, 25] has linked impact ionization with electrical degradation in HEMTs, we wanted to choose a bias stressing scheme that, to the first order, should keep the impact-ionization rate constant. As described in [26], the impact-ionization current in a HEMT has been found to exhibit the following dependence on the biasing conditions:

$$I_{ii} = AI_D \exp \frac{-B}{V_{DGo} + V_T} \tag{2.1}$$

where $A$ and $B$ are constants depending on the extent of high-field region and device design, and $V_{DGo}$ is the intrinsic drain-to-gate voltage drop (excludes external resistance such as $R_D$). Thus keeping impact-ionization constant would require keeping the stressing drain current $I_D$ constant and $V_{DGo} + V_T$ constant. This type of stressing scheme is optimal also because it keeps the intrinsic stressing conditions imposed on a device relatively immune to variations in $V_T$ and $R_D$. If instead the applied bias voltages were kept constant during stressing (i.e. a stressing scheme of constant $V_{GS}$ and constant $V_{DS}$) then the resulting stressing current $I_D$ and intrinsic gate-drain stressing voltage ($V_{DGo}$) would change significantly upon any changes in $V_T$ and $R_D$ during the experiment. A stressing scheme of constant $I_D$ and constant $V_{DGo} + V_T$ would thus result in more uniform intrinsic stressing conditions throughout an experiment, as shown in [27].

In many experiments, in order to enhance the experimental productivity and/or to observe the effects of various bias levels, $V_{DGo} + V_T$ is stepped up in regular time intervals. A graph of such a step-stressing experiment is shown in Fig. 2-7. This figure shows the behavior of the source and drain resistances, $R_S$ and $R_D$, during a typical step-stressing experiment. The left vertical axis shows the normalized values of $R_S$ and $R_D$, while the right vertical axis shows the bias stressing voltage $V_{DGo} + V_T$. As one can see, such a stressing experiment lets us observe the dynamic effects of bias on each key device parameter. Note that the stressing conditions here (and in most of our stressing experiments) are quite aggressive; usually, bias currents close to $I_{max}$ (nearly triple the typical operating $I_D$) and high bias voltages were implemented in our experiments. Such conditions were chosen in order to be able to observe device degradation in a reasonable time frame.

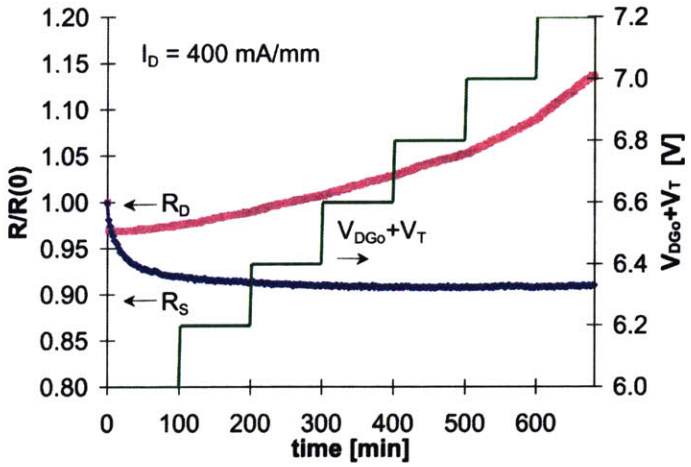



Figure 2-7: Time evolution of $R_D$ and $R_S$ for a typical a step-stressing experiment. Performed on a $W_g = 100$ $\mu$m standard-parameter device in an air environment.

## 2.3 Previous Findings

In [23], we conducted an initial set of electrical stressing experiments on these PHEMTs and also on special test structures (Transmission-Line Model structures, or TLMs). A TLM has essentially the same structure as a PHEMT, but without a gate. Being less complicated than the PHEMTs, but having similar structure, the TLMs were useful devices in studying degradation. From our experiments on both TLMs and PHEMTs, we identified three main forms of degradation associated with the three regions of the PHEMT: the source, the gate, and the drain (see Fig. 2-8). We observed a decrease in $R_S$, a negative shift in $V_T$, and an increase in $R_D$ (and a correlated decrease in $I_{max}$). The decrease in $R_S$ was found to be associated with a permanent increase in sheet carrier concentration on the source side. The negative shift in $V_T$ was attributed to charge modulation occurring under the gate (likely electron de-trapping). The increase in $R_D$ and drop in $I_{max}$ was attributed to a decrease in sheet carrier concentration on the drain side, and also to drain contact degradation.

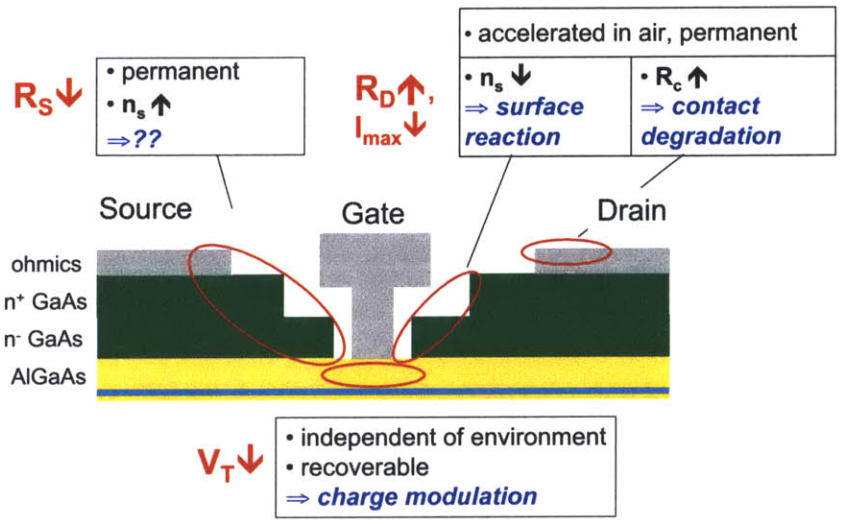



Figure 2-8: A schematic of the top layers of a GaAs PHEMT, illustrated the three main modes of degradation that were identified in S.M. thesis [23].

## 2.4 Summary

In this chapter we have described the GaAs PHEMT devices under study as well as the stress and measurement setup implemented to monitor their degradation. This setup is effective for *in situ* observation of device degradation during electrical stressing. From our initial experiments utilizing this setup, we were able to obtain a general idea of the main forms of degradation present in these devices. However, the specifics of the underlying mechanisms still remained unclear. In order to pinpoint the specific mechanisms behind the observed degradation, we have performed a more thorough investigation of each form of degradation. The results of these experiments and analyses are discussed next.

# Chapter 3

# $R_D$ and $I_{max}$ Degradation of PHEMTs

This chapter describes the degradation of $R_D$ and $I_{max}$ observed in our electrical stressing experiments on experimental RF power GaAs PHEMTs. The general results are first presented, followed by more specific results pertaining to various additional experiments performed in order to uncover the mechanism(s) behind this degradation.

## 3.1 Overall Results of Stressing Experiments

### 3.1.1 General Observations

Fig. 3-1 and Fig. 3-2 show the overall results of a typical on-state degradation experiment performed on a $W_g = 100\mu$m standard-parameter device ($L_{rd} = 0.5\mu$m, $L_{rs} = 0.4\mu$m). Fig. 3-1 shows how during the stressing, $R_D$ increases while $R_S$ decreases and saturates. Fig. 3-2(a) shows how the stressing also causes a negative shift in $V_T$. This shift thus causes an increase in $I_{Dss}$ and $I_{max}$. However, under prolonged stressing eventually $I_{max}$ begins to decrease (see Fig. 3-2(b)). This and other experiments discussed in [23] indicated that $R_D$ and $I_{max}$ were both correlated with degradation on the drain region. Eventually catastrophic breakdown (burnout) occurs in the device after several hours of stressing, when the bias voltages become very high (corresponding to a $V_{DS}$ of 8-9 V). Typically, the only sign of impending burnout is a dramatic drop in the off-state breakdown voltage immediately before (shown in Fig. 3-3).

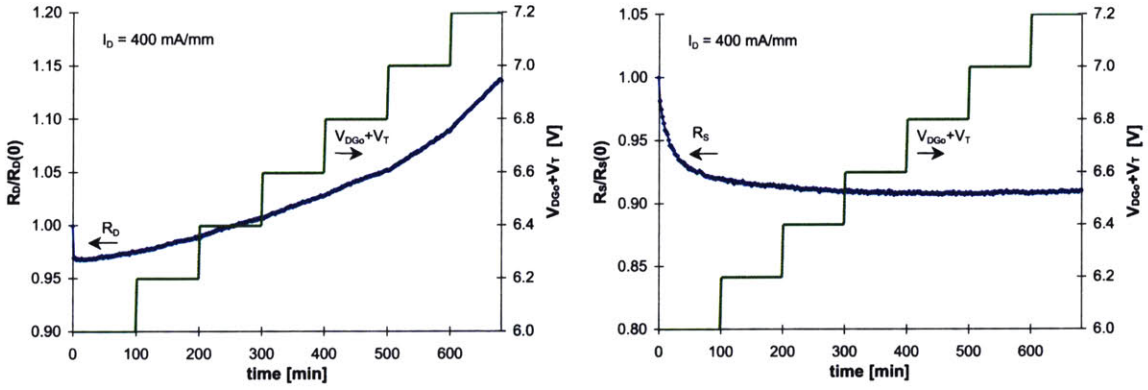



Figure 3-1: (a) Time evolution of normalized $R_D$ (a) and $R_S$ (b), for voltage step-stress experiment performed on standard-parameter PHEMT in air environment, at room temperature. $W_g = 100\mu$m.

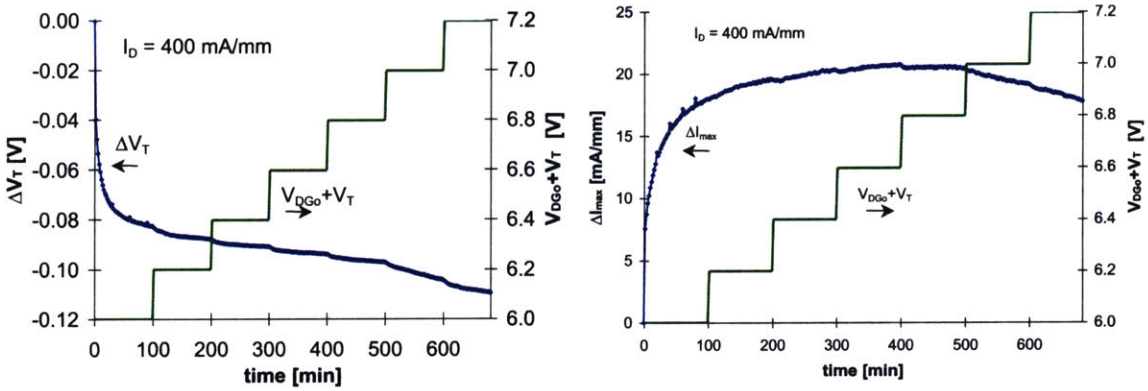



Figure 3-2: (a) Time evolution of normalized $V_T$ (a) and $I_{max}$ (b), for voltage step-stress experiment performed on standard-parameter PHEMT in air environment, at room temperature. $W_g = 100\mu$m.

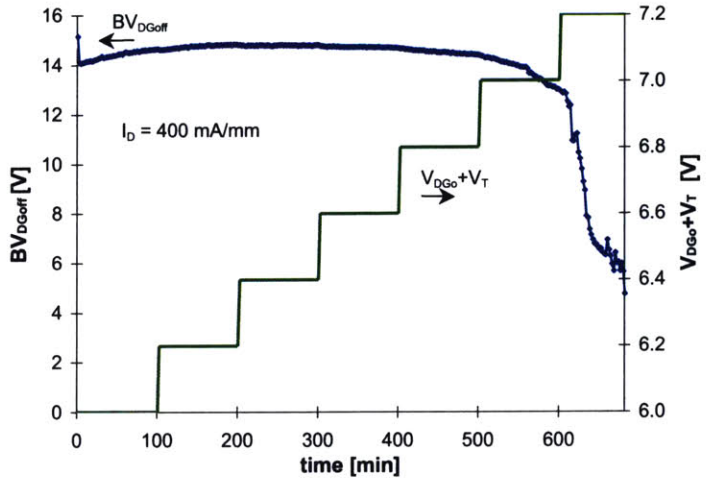



Figure 3-3: Time evolution of normalized $BV_{DGoff}$ for voltage step-stress experiment performed on standard-parameter PHEMT in air environment, at room temperature. $W_g = 100\mu$m.

### 3.1.2 Observation of Impact Ionization

As mentioned in Section 2.2, it is suspected that impact ionization and hot-electron effects play some role in the drain degradation of PHEMTs [5, 6, 12, 25]. So in addition to the usual device characterization, separate measurements were also performed to try to observe impact ionization in the devices studied. Under high biases, the PHEMTs indeed showed various indications of impact ionization. Previous measurements of gate current $I_G$ vs. $V_{GS}$ at high values of $V_{DS}$ exhibit a bell-shaped curve [23], which is a classic signature of impact ionization [28]. To confirm that this observed behavior indicated impact-ionization (and not another high-field process, such as thermionic field emission) we also investigated the temperature dependence of this phenomenon. Fig. 3-4 shows the $I_G$ vs. $V_{GS}$ curves at $V_{DS}$ of 6.0 V, measured at 25°C, 50°C, and 75°C. Although all temperatures exhibit a bell-shaped curve, the magnitude of the gate current decreases for higher temperatures, which is consistent with impact ionization (and not with thermionic field emission, which has a positive temperature dependence).

In addition to these measurements, output characteristics at certain values of $V_{GS}$ were also measured at various temperatures. By measuring both the drain and gate current vs. $V_{DS}$ at

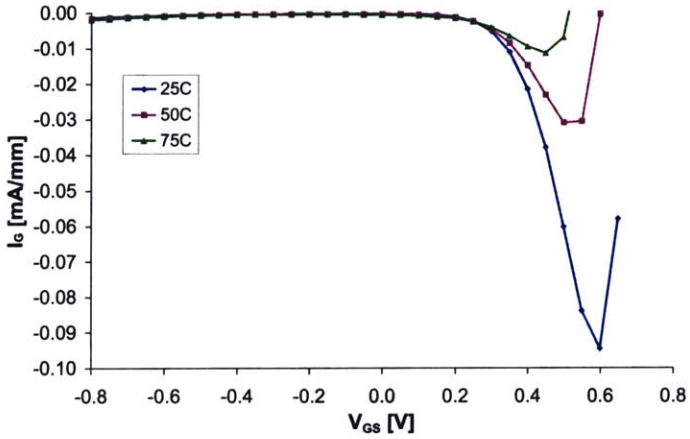
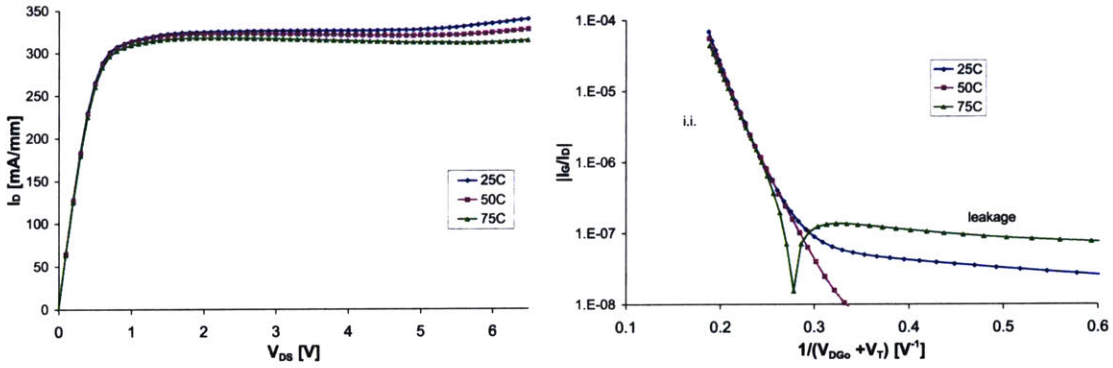



Figure 3-4: $I_G$ vs. $V_{GS}$ for an unstressed standard-parameter PHEMT, taken at 25, 50 and 75°C in $N_2$, for $V_{DS}$ = 6.0 V. $W_g = 100\mu$m.

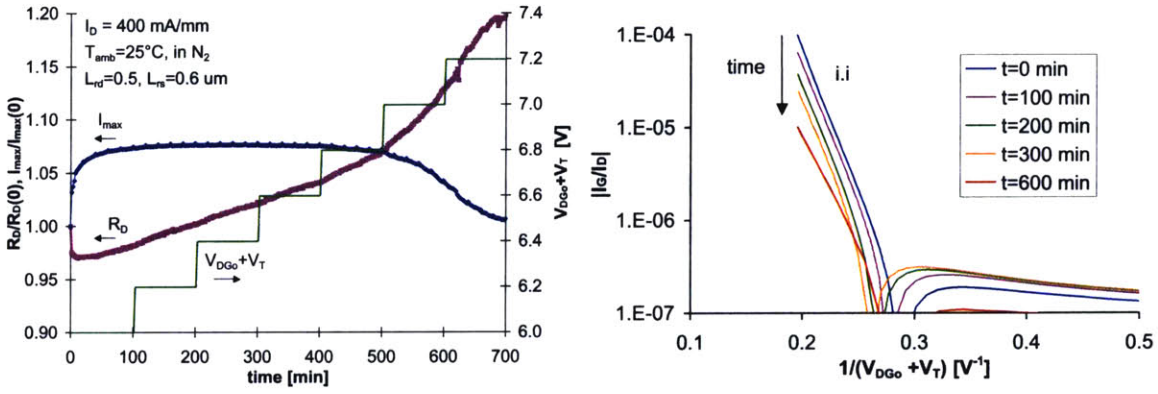



(a) (b)

Figure 3-5: Plot of $I_D$ vs. $V_{DS}$ (a) and semi-log plot of $|I_G/I_D|$ vs. $1/(V_{DGo} + V_T)$ (b), for a set of measurements taken at $V_{GS}$= 0.3 V, at 25, 50, and 75°C in $N_2$, on standard-parameter PHEMT. $W_g = 100\mu$m.

constant $V_{GS}$, a plot of the normalized gate current $|I_G/I_D|$ versus $1/(V_{DGo}+V_T)$ could be created. This is shown in Fig. 3-5. As one can see from the right graph, the behavior at high $V_{DGo}+V_T$ ($V_{DGo}+V_T > 4$ V) clearly indicates impact ionization (refer to Eq. 2.1 for dependence of impact ionization on $V_{DGo}+V_T$). For low $V_{DGo}+V_T$, the level of impact-ionization is so small that $I_G$ is dominated by the reverse leakage current of the gate-drain Schottky junction [29].

From these graphs one can see that in order to observe reasonable levels of impact ionization, it is necessary to perform measurements at high voltages ($V_{DS} > 5$ V). Because of this, we could not incorporate such measurements in our regular characterization suite, since doing so could potentially introduce significant degradation in the device. However, this degradation could be minimized if the high-voltage measurements were performed at only a few instances during a stressing experiment. Thus, during select experiments, these high-voltage measurements were performed at occasional time points throughout electrical stressing. Fig. 3-6 shows $R_D$ and $I_{max}$ degradation during such a step-stressing experiment, along with a plot of $|I_G/I_D|$ vs. $1/(V_{DGo}+V_T)$ for a few time points during this experiment. As one can see, here impact ionization decreases consistently as time goes on and the device degrades. This could be due to the reduction of the maximum electric field between the gate and drain, as a result of the increase in $R_D$ [12, 30]. It can also be due to the decrease in $I_{max}$, which suggests lower sheet carrier concentration $n_s$ on the extrinsic drain, which would tend to increase $BV_{DGoff}$ [31]. But then this seems to be inconsistent with the *decrease* in $BV_{DGoff}$ that is observed with electrical stressing. This brought forth an issue that required some further investigation, and will be discussed later on in this chapter.




(a) (b)

Figure 3-6: (a)Time evolution of $R_D$ and $I_{max}$ for a voltage step-stressing experiment at constant $I_D$ = 400mA/mm, at 25°C in $N_2$. (b) Semi-log plot of $|I_G/I_D|$ vs. $1/(V_{DGo} + V_T)$ for a set of measurements taken at $V_{GS}$ = 0.4V at various timepoints during same voltage step-stressing experiment. $W_g = 100\mu$m.

| Observations in TLMs | Correlation with PHEMTs |
|---|---|
| Regime 1: $n_s \uparrow$ on source, insensitive to $H_2O/O_2$ | Initially $R_S \downarrow$, insensitive to $H_2O/O_2$ |
| Regime 2: $R_C \uparrow$ on drain, accelerated in air | $R_D \uparrow$, accelerated in air |
| Regime 3: $n_s \downarrow$ on drain, accelerated in air | $R_D \uparrow, I_{max} \downarrow$, accelerated in air |
| all degradation accelerated with temperature | all degradation accelerated with temperature |

Table 3.1: General forms of degradation observed in TLMs, and their correlation with observed behavior in PHEMTs.

### 3.1.3 Mechanisms behind $\Delta R_D$ and $\Delta I_{max}$

As discussed in [17,23], in order to obtain a simple, clearer picture of the various degradation mechanisms in the PHEMTs, electrical stressing experiments were also performed on TLM structures. The observations from these experiments helped us clarify what was happening on the drain side in the PHEMTs. The general forms of degradation observed in the TLMs and their correlation to PHEMTs are summarized in Table 3.1. These findings suggested that the increase $R_D$ was due to degradation of the drain ohmic contact, followed by a decrease in sheet carrier concentration $n_s$ on the drain side. The decrease $I_{max}$ is correlated with the decrease in $n_s$ on the drain side. As these forms of drain degradation were both accelerated with temperature and in air, all these findings were consistent with some kind of chemical reaction on the drain side (possibly corrosion happening on the surface of the drain-gate region, as described in [7]).

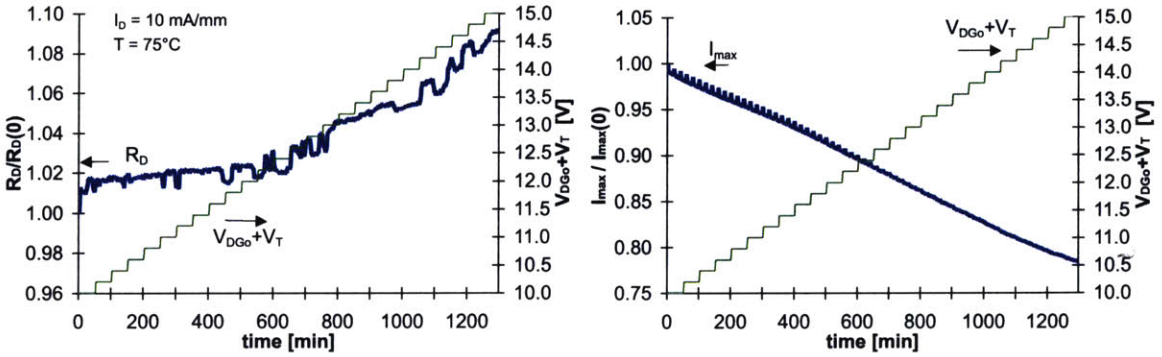
However, there were still some unanswered questions surrounding this theory of degradation. Did the corrosion reaction require a significant drain current, or just a high-electric field? In order to determine if the degradation could be induced by just an electric field itself (without any significant drain current), it was necessary to perform *off-state* stressing experiments as well. Also, if oxygen or moisture was required for the corrosion reaction, it was unclear why some $R_D$ and $I_{max}$ degradation could still be observed while stressing in nitrogen environment, as seen in [23]. Thus we needed to take a closer look at the drain degradation in air vs. nitrogen, in both off-state

and on-state stressing experiments. Also, we needed to obtain a quantitative measurement of the temperature dependence of the degradation. And of course, we wanted to obtain direct evidence of the suspected corrosion layer in degraded devices (by means of materials analysis).

## 3.2 Off-State Stressing

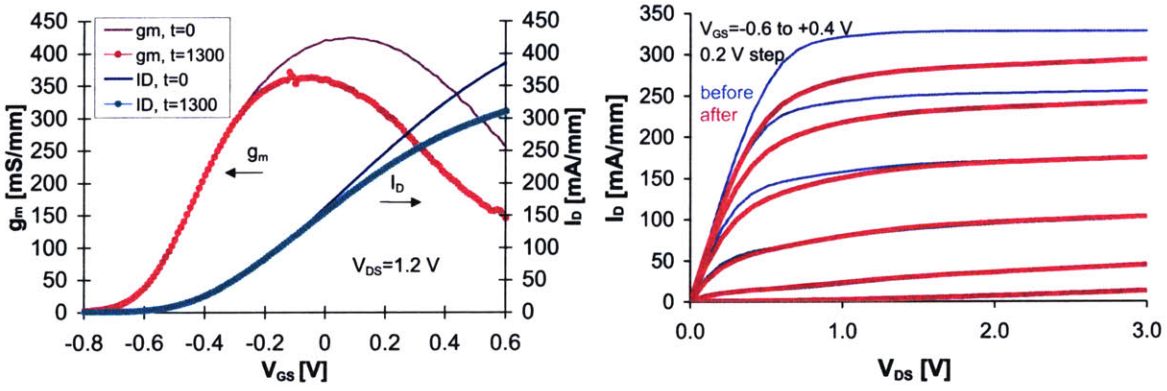
Initially, all of our previous stressing experiments were done in the on-state, where the drain current was quite high ($I_D > 400$ mA/mm). This was done in order to accelerate device degradation, so that changes in parameters could be observed in a reasonable time frame. However, the main issue with this type of stressing is the fact that the channel temperature is dependent on the biasing conditions. Thus it is difficult to isolate the effects of higher voltage or current biases from the effects of increasing channel temperature. One way around this is to perform stressing experiments in the off-state condition, in which the drain-gate bias is very high, but $V_{GS} \sim V_T$ such that the drain current is very small. In this case, the dissipated power causes a negligible increase in channel temperature, and thus the channel temperature will remain more or less at the ambient temperature, regardless of any increase in bias voltage.

Our typical off-state experiments employed a stressing current of $I_D = 10$ mA/mm and $V_{DGo} + V_T$ starting from 10 V and stepping up 0.2 V every 50 minutes, up to 15 V. Fig. 3-7 illustrates the time evolution of $R_D$ and $I_{max}$ during such an experiment, which was done at $T_{amb} = 75°C$ in air. From the left graph, one can observe a small but significant increase in $R_D$. From the right graph, one can observe a very significant decrease in $I_{max}$. Fig. 3-8(a) illustrates the transfer characteristics and before and after stressing, showing a significant reduction in $g_{mpeak}$ while no major shift in $V_T$. Fig. 3-8(b) shows the output characteristics before and after stressing, clearly illustrating the dramatic effect of the degradation on drain current. From these experiments it is quite clear than the mechanism behind $R_D$ and $I_{max}$ degradation does *not* need significant drain current to occur, as long as there is a large enough electric field between the gate and the drain.




(a) (b)

Figure 3-7: Time evolution of normalized $R_D$ (a) and $I_{max}$ (b), for off-state experiment performed on standard-parameter PHEMT at $T_{amb} = 75°C$ in air. $W_g = 100\mu m$.




(a) (b)

Figure 3-8: Transfer characteristics (a) and output characteristics (b) before and after 1300 minutes of stressing for off-state experiment performed on standard-parameter PHEMT at $T_{amb} = 75°C$ in air. $W_g = 100\mu m$.

## 3.3 Effect of Environment

### 3.3.1 Off-State Stressing

In order to study the effects of the environment, we also performed off-state stressing experiments in nitrogen. Fig. 3-9 shows the time evolution of $R_D$ and $I_{max}$ for identical off-state stressing experiments done in air and in nitrogen at ambient temperature of 75°C. As one can see, the stressing environment does not make a difference here; the device stressed in nitrogen exhibits essentially the same amount of $R_D$ and $I_{max}$ degradation as in air. This suggests that if the degradation observed here is due to corrosion, then the oxygen or moisture for the reaction must be being obtained from a source other than the environment (possibly from the silicon dioxide passivation layer).

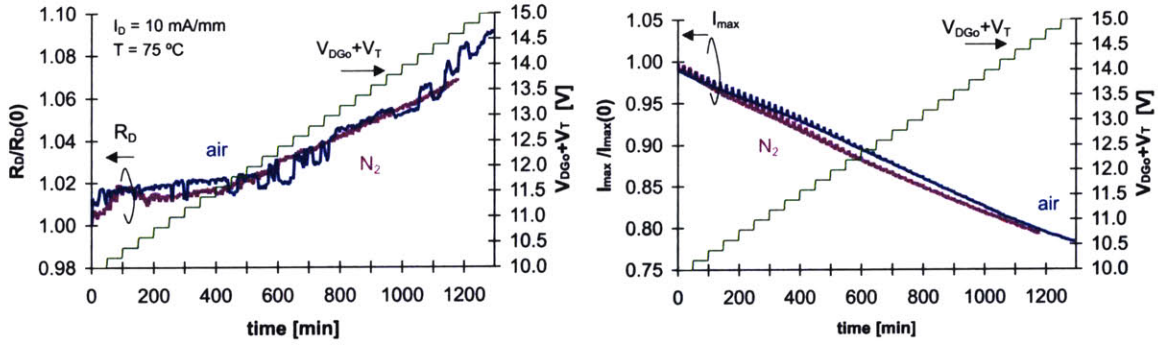
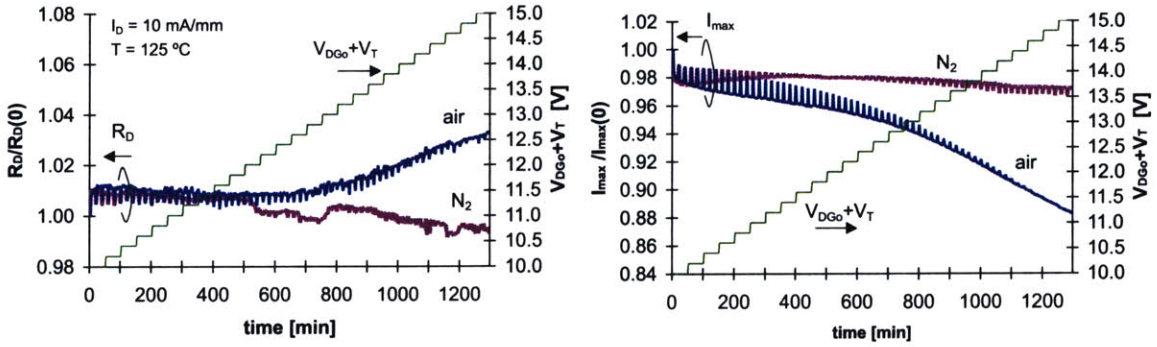



Figure 3-9: Time evolution of normalized $R_D$ (a) and $I_{max}$ (b), for off-state step-stress experiments performed on standard-parameter PHEMTs in air & nitrogen environments at $T_{amb} = 75$°C. $I_D = 10$ mA/mm. $W_g = 100\mu$m.

However, when the same experiments were performed at higher temperature, the degradation under nitrogen was quite different from that in air. Fig. 3-10 shows the time evolution of $R_D$ and $I_{max}$ for identical off-state stressing experiments done in air and in nitrogen, at an ambient temperature of 125°C. As one can see, the stressing environment makes a considerable difference here; the device stressed in nitrogen exhibits only negligible degradation of $R_D$ and $I_{max}$.




(a) (b)

Figure 3-10: Time evolution of normalized $R_D$ (a) and $I_{max}$ (b), for off-state step-stress experiments performed on standard-parameter PHEMTs in air & nitrogen environments at $T_{amb}$ = 125°C. $W_g = 100\mu$m.

This behavior was initially quite puzzling, since at ambient temperatures just 50°C lower, the environment had no noticeable impact whatsoever on the degradation. It was soon discovered, however, that in our experiments where high ambient temperatures are employed (125°C or higher), the mere heating of the device introduces a significant effect on device degradation. Namely, heating tends to impede subsequent degradation. Heating in nitrogen was more effective in preventing degradation than heating in air. This explains the difference in degradation observed in Fig. 3-10. This effect will be discussed in further detail in Sec. 3.4.

### 3.3.2 On-State Stressing

In our on-state stressing experiments, despite significant degradation on the drain (as evidenced by an increase in $R_D$) it is sometimes difficult to observe a significant decrease in $I_{max}$, partially because $I_{max}$ is also affected by the negative shift in $V_T$, which tends to *increase* $I_{max}$ (refer to Fig. 3-2(b)). Thus, in order to adequately compare the degradation of $R_D$ and $I_{max}$ in different environments, a set of on-state experiments employing a very high level of stressing current ($I_D$= 450 mA/mm) was performed, so that a clear decrease in $I_{max}$ as well as an increase in $R_D$ could be observed in both cases. Fig. 3-11 shows the results of these experiments. As one can see, the relative increase

of $R_D$ and decrease of $I_{max}$ are both reduced by about 1/3 by stressing in nitrogen instead of air. This suggests that oxygen and moisture in the air play a significant role in the drain degradation here, and thus supports the presence of an oxidation mechanism. However, the fact that here the degradation is not *completely* suppressed by stressing in nitrogen suggests that either (1) the corrosion reaction is somehow able to proceed without oxygen and/or moisture from the air, or (2) there is a separate, environment-independent mechanism occurring that is contributing to the degradation of $R_D$ and $I_{max}$. In the first case, it could be that the oxygen is being somehow obtained from the silicon dioxide passivation layer. Additional experiments discussed later in this chapter will shed some light on this issue.

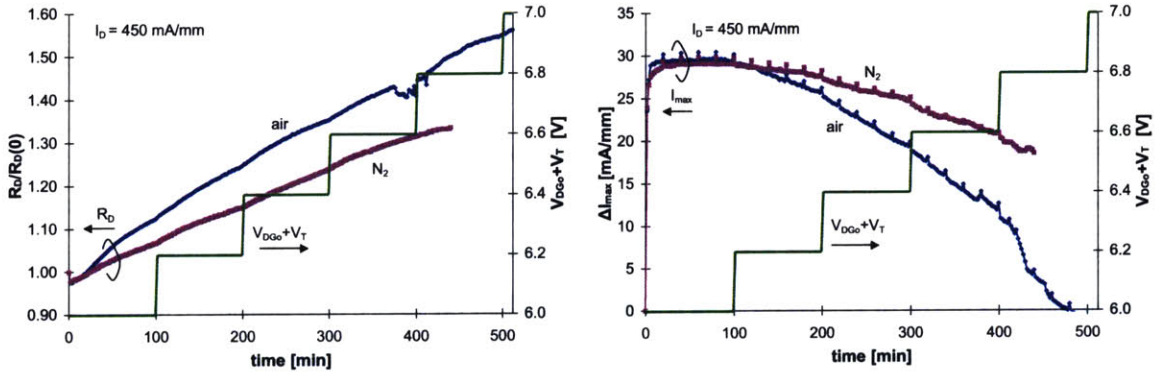



Figure 3-11: Time evolution of normalized $R_D$ (a) and $I_{max}$ (b), for voltage step-stress experiments performed on standard-parameter PHEMTs in air & nitrogen environments, at $T_{amb} = 25°$. $W_g = 100\mu$m.

## 3.4 Annealing Effect

During the course of performing various off-stressing experiments, it was discovered that simply heating the devices at high temperatures had significant effects on their subsequent degradation. After unbiased high-temperature storage for a period of time, devices would exhibit less degradation of $R_D$ and $I_{max}$ upon electrical stressing. An example of this is illustrated in Fig. 3-12, which

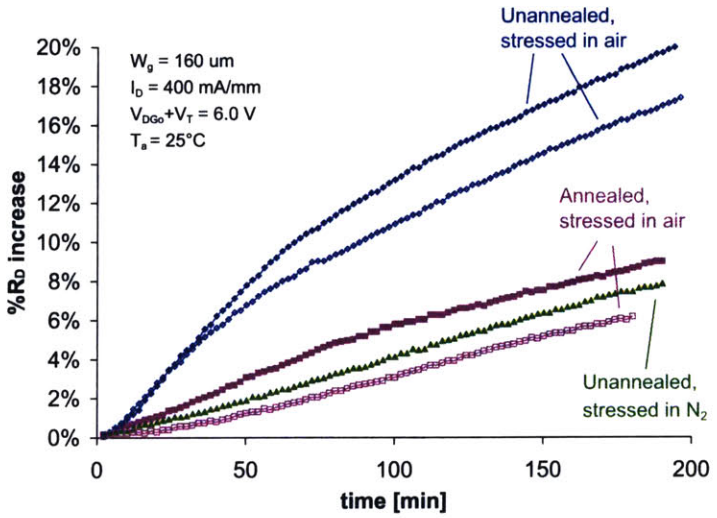
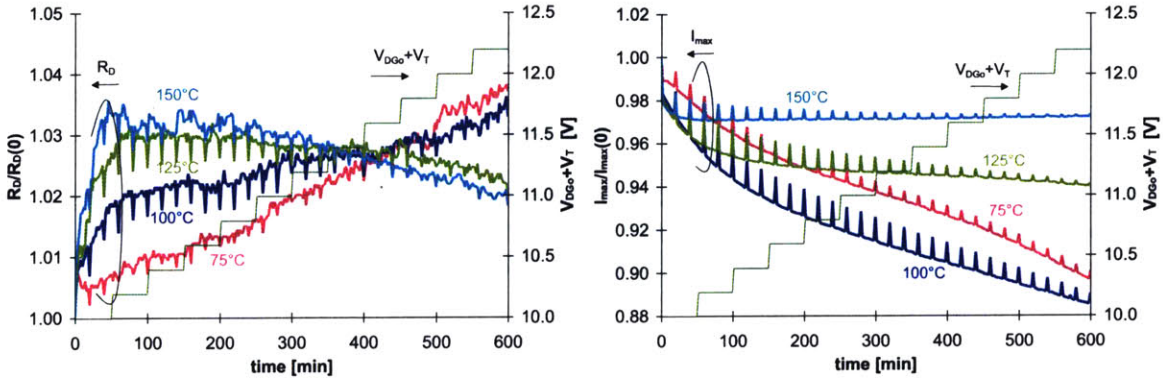



Figure 3-12: Time evolution of normalized $R_D$ during on-state stressing experiments performed with $I_D = 400$ mA/mm, $V_{DGo} + V_T = 6$ V at $T_{amb} = 25$°C. Devices shown in magenta were heated prior to stressing. Heating was done for 48 hours at 175°C in air.

shows the time evolution of $R_D$ for a number of devices stressed in the on-state condition at $I_D = 400$ mA/mm, $V_{DGo} + V_T = 6$ V at room temperature. Devices stressed in air without any prior heating are shown in dark blue, where the devices stressed in air but which were heated in air (at $T_{amb} = 175$°C for 48 hours) prior to stressing are shown in magenta. Although there is some variation among the devices tested, it is clear that the heating prior to stressing had the effect of inhibiting the degradation. It is interesting to note that heated devices stressed in air have about the same level of degradation as an unheated device stressed in nitrogen. This suggests that the heating prior to stressing somehow prevents oxygen/moisture from the environment from reaching the semiconductor surface and reacting to form the corrosion layer. The heating could be somehow making the silicon dioxide passivation layer more impermeable to oxygen and water from the air, either by annealing out defects in the passivation (hindering impurity diffusion?) or densifying the passivation.

This effect of heating can also be seen *during* our electrical stressing experiments, in which high ambient temperatures are employed. Fig. 3-13 shows the time evolution of $R_D$ and $I_{max}$ for a

series of off-state step-stressing experiments performed at ambient temperatures from 75 to 150°C in nitrogen. In Fig. 3-13(a), we can see that for the first 50 minutes of stressing, there is an increase in $R_D$ for all temperatures. However, for the devices stressed at 125 and 150°C, there is *no further degradation* upon further stressing. A similar phenomenon is happening with the $I_{max}$ degradation shown in Fig. 3-13(b). Initially, a reduction in $I_{max}$ is observed for all temperatures; however, after about an hour of stressing, for the devices stressed at 125 and 150°C, the decrease in $I_{max}$ "saturates" and no further degradation is observed, despite the increasing bias.




(a) (b)

Figure 3-13: Time evolution of normalized $R_D$ (a) and $I_{max}$ (b), for off-state step-stress experiments performed on standard-parameter PHEMTs in nitrogen environment at $T_{amb} = 75, 100, 125, 150$°C. $W_g = 100\mu$m.

These observations thus suggest that for ambient temperatures above 125°C, heating begins to have a significant effect on the devices under test by making them less susceptible to degradation. This effect seems more pronounced if the heating is done in a nitrogen environment, as the degradation of $R_D$ and $I_{max}$ become completely suppressed in this case. This can thus explain the discrepancy seen in the effects of the environment in the off-state experiments discussed in Sec. 3.3.1. Recall that in Fig. 3-10, where devices were stressed in the off-state at $T_{amb} = 125$°C, the degradation of $R_D$ and $I_{max}$ seemed to be completely suppressed when stressed in nitrogen. However, the degradation observed in identical experiments stressed at 75°C yielded no difference between stressing in air and nitrogen. Now we can see that this is because at 125°C, the high

temperature over time was making the devices less susceptible to degradation. Although both devices were getting heated, the one heated in nitrogen became more impervious to degradation. This makes sense, as heating a device in nitrogen could not potentially introduce any additional oxygen or moisture to the device. This suggests that the effect of heating is to drive out residual oxygen/moisture from the surface, thus preventing corrosion from taking place.

## 3.5 Effect of Temperature

In [23] we observed that in the stressing experiments on the TLMs, all main forms of degradation were accelerated with increasing ambient temperature. Since then, analogous stressing experiments have been performed on the PHEMTs and similar tendencies have been observed ($R_D$ and $I_{max}$ degradation accelerated with temperature).

### 3.5.1 Estimating Channel Temperature

In order to accurately analyze the temperature dependence of the degradation, the actual *channel temperature* of the device under stress must be known. Due to the high currents and voltages employed in typical electrical stressing experiments, a significant amount of heat is dissipated by the device, thus causing the channel temperature to be significantly higher than the ambient temperature. Thus it is important to consider this channel temperature (rather than the ambient temperature) in the analysis of the temperature dependence of any type of degradation.

To determine the actual channel temperature of a device ($T_{ch}$) while it is being it stressed at a specific biasing condition and ambient temperature ($T_{amb}$), we use the following equations:

$$T_{ch} = T_{amb} + P_{diss}\theta_{jc} \tag{3.1}$$

where

$$P_{diss} = V_{GS}I_G + V_{DS}I_D \tag{3.2}$$

The thermal resistance of the device $\theta_{jc}$ (in °C/W) is estimated by comparing DC I-V charac-

teristics with pulsed characteristics, as described in the Appendix. At room temperature, for a standard-parameter device of $W_g = 160\mu$m, $\theta_{jc}$ was extracted to be 241°C/W. This agrees well with calculations done using the Cooke method (also described in Appendix), which give 254°C/W for a $W_g = 160\mu$m device. However one must note that since the thermal conductivity decreases with temperature, $\theta_{jc}$ will increase with temperature [32]. So to obtain the most accurate estimate for $\theta_{jc}$, one must take into account the ambient temperature and the power dissipation during each particular stressing experiment. Also, it should be noted that $\theta_{jc}$ depends on the device width (narrower devices will have a larger thermal resistance). This is further discussed in the Appendix.

Using the thermal resistance, we can now estimate how much the temperature increases during a typical on-state stressing experiment. For a standard $W_g = 160$ $\mu$m device at room temperature under $I_D = 400$ mA/mm and $V_{DGo} + V_T = 6.0$ V, $V_{DS}$ is about 7.4 V, and the actual drain current $I_D$ is 64 mA. Both $I_G$ and $V_{GS}$ are much smaller than $I_D$ and $V_{DS}$, so we can ignore the second term and just say that $P_{diss} = I_D V_{DS}$, which gives a power dissipation of about 0.47 W. This results in a channel temperature increase of 150°C above the ambient temperature. The thermal resistance here is about 310°C/W, which is a significant increase from the value at room temperature.

From this analysis we can easily see that any increase in bias will lead to an increase in channel temperature. Consequently, during an on-state step-stressing experiment, the channel temperature is not constant, making it difficult to separate the effects of bias and temperature on degradation. Thus, we decided to perform additional stressing experiments at various temperatures, in which the channel temperature is held more or less constant throughout each experiment. These consist of off-state step-stressing experiments (where $T_{amb} = T_{ch}$ regardless of bias voltage, since there is little power dissipation), or on-state stressing experiments at constant bias voltages (no stepping).

### 3.5.2 Off-State Stressing

We will first examine the temperature dependence of the degradation in the off-state condition. We performed a series of off-state step-stressing experiments done over a wide range of temperatures (25°-175°C) in air. Fig. 3-14 and Fig. 3-15 show the degradation of $R_D$ and $I_{max}$, respectively, for these experiments. Since different behaviors were observed for low and high temperatures, the

results are split up into two groups: data from 25-75°C, and 100-175°C.

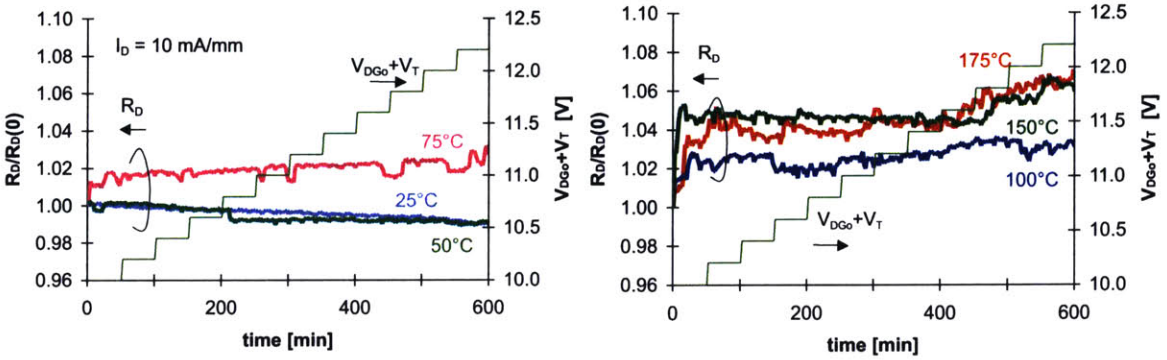



Figure 3-14: Time evolution of normalized $R_D$ for off-state step-stressing experiments performed on standard-parameter PHEMTs in air environments, for $T_{amb}$ = 25, 50, 75°C (a) and $T_{amb}$ = 100, 150, 175°C (b). $I_D$ = 10 mA/mm. $W_g$ = 100$\mu$m.

First, looking at the behavior of $R_D$, one can note that the degradation is relatively non-existent below 50°C. Overall, the $R_D$ degradation appears to increase slightly with temperature, for the entire range of temperatures. However, the behavior of $I_{max}$ is somewhat different. In these experiments, the reduction of $I_{max}$ has a different dependence on temperature for low temperatures and high temperatures. For 25-75°C, the $I_{max}$ degradation increases with increasing temperature, thus exhibiting a positive temperature dependence. In contrast, for 100-175°C, the degradation has a *negative* temperature dependence.

First of all, from the discussion in Sec. 3.4, we know that with storage at high ambient temperatures the devices tend to become less prone to degradation. So this explains the negative temperature dependence of the $I_{max}$ degradation observed above 100°C; as the devices are heated more, the stronger the "annealing effect" and the more impervious they become to degradation. Because of the presence of this effect in experiments done at high temperatures, we should focus on the behavior at lower temperatures in studying the temperature dependence of the degradation. In this case, the $I_{max}$ degradation exhibits a positive temperature dependence, which indicates that the degradation could be limited by the oxidation reaction rate.

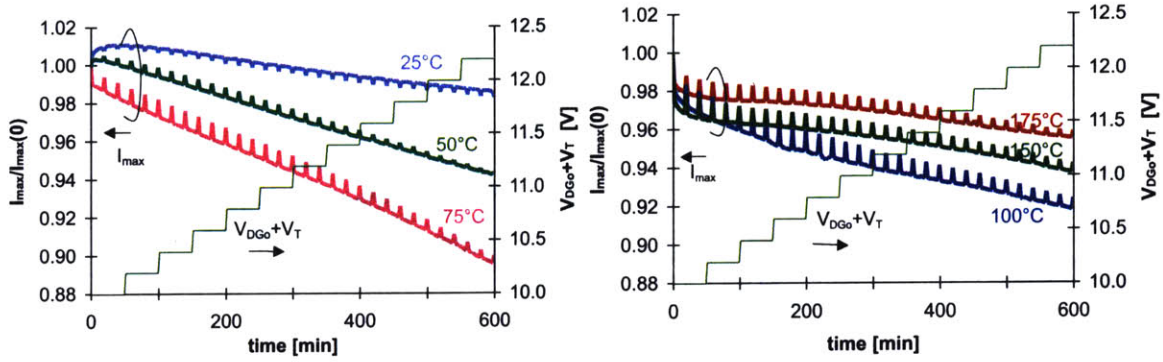



Figure 3-15: Time evolution of normalized $I_{max}$ for off-state step-stressing experiments performed on standard-parameter PHEMTs in air environments, for $T_{amb}$ = 25, 50, 75°C (a) and $T_{amb}$ = 100, 150, 175°C (b). $I_D$ = 10 mA/mm. $W_g$ = 100$\mu$m.

Fig. 3-16 shows an Arrhenius plot of the change in $I_{max}$ in these experiments. Here one can see that the best fit to the data points corresponds to an activation energy of $E_a$ = 0.32 eV. This activation energy likely represents that of the corrosion reaction rate under these conditions.

To assess the accuracy of this extracted activation energy, we examined the possible variation of $E_a$ due to uncertainties in the experimental data. The main contributor to changes in $E_a$ was the variation in the relative amount of degradation observed. Although all devices tested are nominally identical, due to process variations the amount of degradation observed for a given stressing condition will vary slightly from device to device, thus introducing some uncertainty. In the off-state experiments we determined that the uncertainty in $\%I_{max}$ degradation was about 10%. This was used to construct the error bars shown along with the data in Fig. 3-16. From this it was determined that the extracted value of 0.32 eV is accurate to $\pm$0.04 eV.

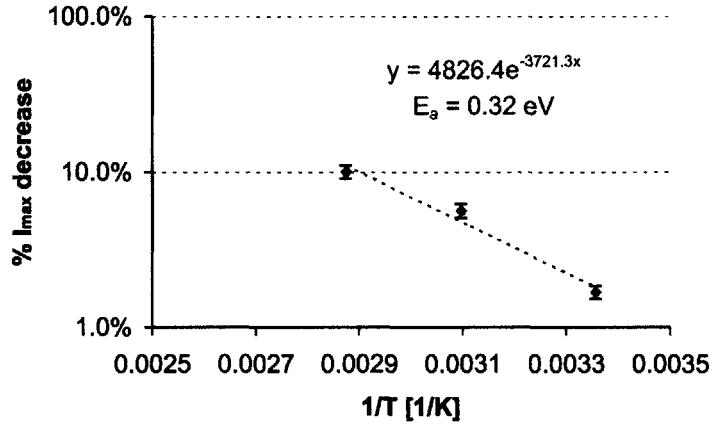
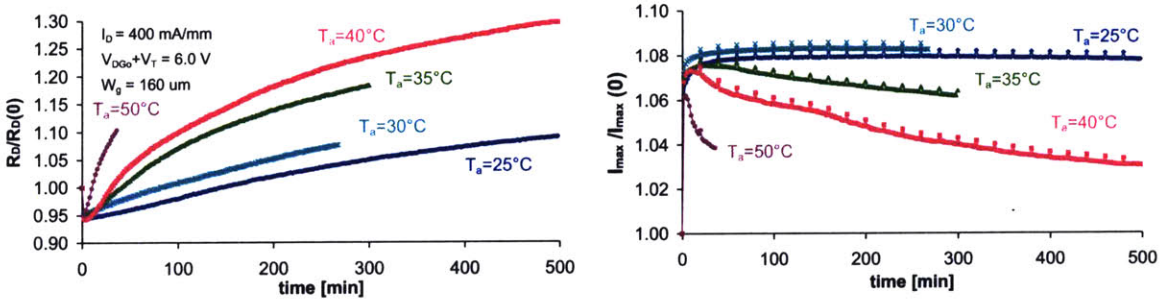



Figure 3-16: Arrhenius plot of percent decrease in $I_{max}$ after 600 minutes of stressing for off-state step-stressing experiments performed on standard-parameter PHEMTs in air environments, for $T_{amb}$ = 25, 50, 75°C . $I_D$ = 10 mA/mm, $W_g$ = 100$\mu$m.

### 3.5.3 On-State Stressing

We performed on-state stressing experiments with constant bias voltage, at various ambient temperatures. Fig. 3-17 shows the time evolution of $R_D$ and $I_{max}$ for devices stressed at $V_{DGo}+V_T = 6.0$ V under various temperatures, in a nitrogen environment. From this one can clearly see that even small increases in temperature have a drastic effect on the degradation of both $R_D$ and $I_{max}$.

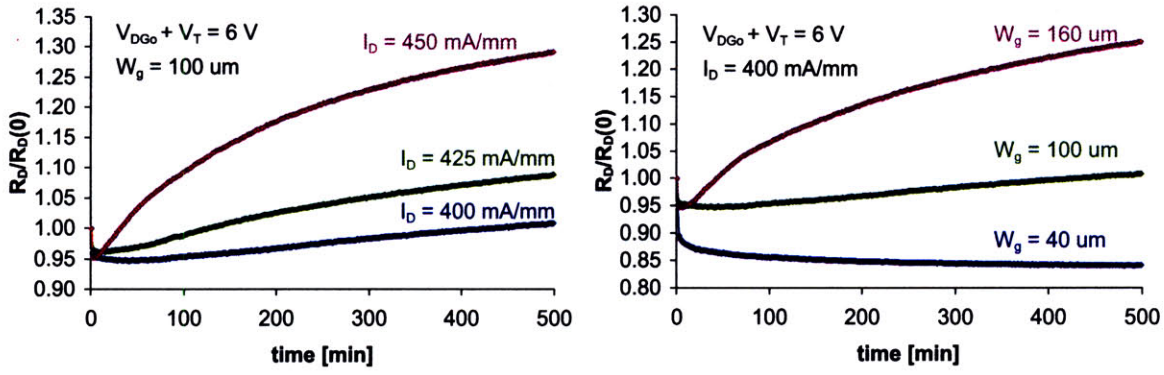



(a) (b)

Figure 3-17: Time evolution of normalized $R_D$ (a) and change in $I_{max}$ (b), for constant $V_{DGo}+V_T$ and constant $I_D$ experiments performed on standard-parameter PHEMTs in nitrogen environments, at $T_a$ = 25, 30, 35, 40, and 50°C. $W_g = 160\mu$m.

It is clear from these graphs that in the on-state condition, the degradation of $R_D$ and $I_{max}$ have a very strong positive temperature dependence. But to analyze this dependence accurately, it is important to consider the actual *channel temperature* in each case. As discussed in Sec. 3.5.1, the channel temperature is determined by device power dissipation as well as the ambient temperature. Thus we must acknowledge that other factors that affect power dissipation (such as stressing current, device width) can affect the channel temperature. Fig. 3-18(a) illustrates the effect of stressing current on $R_D$ degradation. Fig. 3-18(b) illustrates the effect of device width on $R_D$ degradation. These graphs illustrate that as $I_D$ or $W_g$ increase, the $R_D$ degradation increases. This makes sense, as either increasing $I_D$ or $W_g$ will cause the device to heat up more.

Acknowledging the effect on $I_D$ on $T_{ch}$ then raises the possibility that the effect of increasing stressing current on degradation is *only* because of the resulting increase in channel temperature. To look further into this, we then investigated a set of similar stressing experiments where $V_{DGo}+V_T$

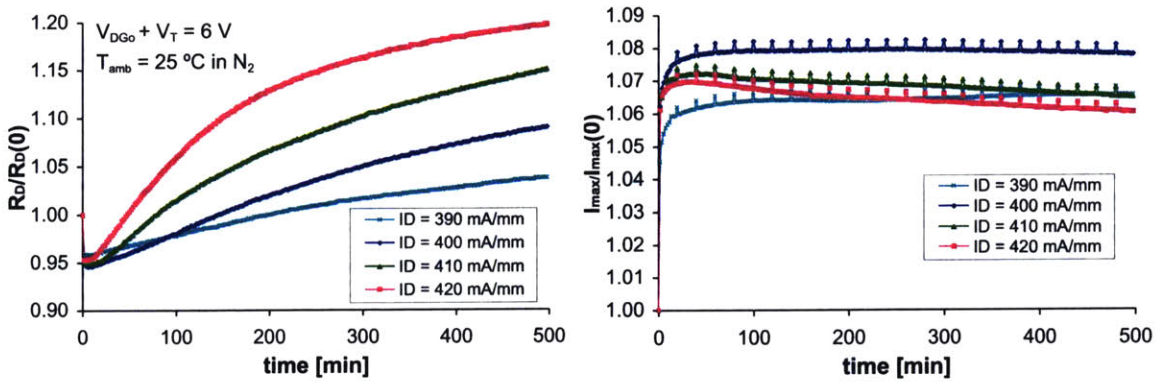



(a) (b)

Figure 3-18: Time evolution of normalized $R_D$ for constant $V_{DGo}+V_T$ and constant $I_D$ experiments performed on standard-parameter PHEMTs in air environment at $T_a = 25°C$, for varying stressing currents (a) and varying widths (b).

and $I_D$ where held constant, but instead of varying $T_{amb}$ as in Fig. 3-17, the stressing $I_D$ was varied slightly, from 390 mA/mm to 420 mA/mm. Fig. 3-19 shows the time evolution $R_D$ and $I_{max}$ for these experiments. First of all, one can see that changing the stressing current also has a very strong effect on the $R_D$ degradation; for example, just a 5% increase in $I_D$ (400 mA/mm to 420 mA/mm) essentially *doubles* the increase in $R_D$. The effect on $I_{max}$ appears to be much less, and is difficult to observe due to the relatively small amount of degradation and the simultaneous presence of the negative $V_T$ shift. As for the strong effect on $R_D$ degradation, instead of simply assigning this effect to the increased current itself, we first calculate the channel temperatures in each of these experiments and those in Fig. 3-17 and compare them. Specifically, we will examine devices stressed under different $I_D$ and different $T_a$, but with similar $T_{ch}$. If the level of degradation observed in these devices is the same, then we can conclude that the effects of varying the stressing $I_D$ (at least, over a moderate range) is indeed only due to the change in $T_{ch}$.

Table 3.2 shows the values of $T_{ch}$ calculated for all of the experiments in Fig. 3-17 and Fig. 3-19. The two experiments shown in bold (one stressed at $I_D = 420$ mA/mm and $T_{amb} = 25°C$, the other with $I_D = 400$ mA/mm and $T_{amb} = 35°C$) have very similar channel temperatures ($T_{ch} \approx 190°C$), so we will examine the degradation in those cases. Fig. 3-20 shows the $R_D$ and $I_{max}$ degradation




(a) (b)

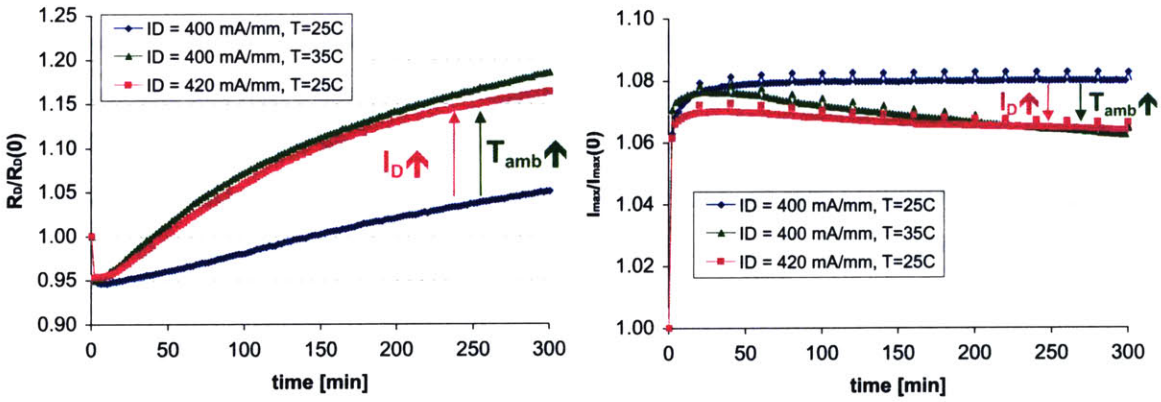
Figure 3-19: Time evolution of normalized $R_D$ (a) and $I_{max}$ (b), for constant $V_{DGo} + V_T$ and constant $I_D$ experiments performed on standard-parameter PHEMTs in nitrogen environments at $T_a = 25°C$, with $I_D = 390, 400, 410, 420$ mA/mm. $W_g = 160\mu$m.

of these two experiments, along with a third "nominal" experiment with a much lower channel temperature, where $I_D = 400$mA/mm and $T_{amb} = 25°C$. As one can see, the behavior of $R_D$ and $I_{max}$ is virtually the same in the two cases with similar $T_{ch}$. So whether $I_D$ was increased by 20 mA/mm or $T_{amb}$ by 10°C from the nominal conditions, both result in increasing $T_{ch}$ by about the same amount from the nominal case, thus inducing more or less the same amount of degradation. This hence suggests that, in these devices, $T_{ch}$ is what is really critical for degradation, and not actually $I_D$ itself.

Now to obtain a quantitative sense of the temperature dependence of the degradation, we sought to create an Arrhenius plot of the degradation rates and extract the activation energies. We first examine the increase of $R_D$, which was more readily observed that the decrease of $I_{max}$. To represent the degradation rate, $1/\tau$ was used, where $\tau$ was the time required for a 10% increase of $R_D$. Fig. 3-21 shows the Arrhenius plot containing data points from the eight experiments summarized in Table 3.2. As one can see, the data points from these experiments fit nicely to an activation energy of $E_a = 1.21$ eV. This activation energy represents the strong temperature dependence of the $R_D$ degradation, for this type of device under constant $V_{DGo} + V_T = 6.0$V, in a nitrogen environment.

| $I_D$ [mA/mm] | $T_{amb}$ [°C] | $P_{diss}[W]$ | $\Delta T$ | $T_{ch}$ [°C] |
|---|---|---|---|---|
| 390 | 25 | 0.465 | 144.3 | 169.3 |
| 400 | 25 | 0.480 | 150.3 | 175.3 |
| 410 | 25 | 0.495 | 156.4 | 181.4 |
| 400 | 30 | 0.483 | 154.9 | 184.9 |
| **420** | **25** | **0.511** | **163.0** | **188.0** |
| **400** | **35** | **0.482** | **157.5** | **192.5** |
| 400 | 40 | 0.483 | 161.5 | 201.5 |
| 400 | 50 | 0.486 | 169.8 | 219.8 |

Table 3.2: Table showing estimated changes in temperature $\Delta T$ and resulting $T_{ch}$ for constant $V_{DGo} + V_T$ and constant $I_D$ experiments shown in Fig. 3-17 and Fig. 3-19. $W_g = 160\mu$m, nitrogen environment. $T_{ch}$ values calculated taking into account temperature dependence of thermal resistance.




(a) (b)

Figure 3-20: Time evolution of normalized $R_D$ (a) and $I_{max}$ (b) for three different experiments of constant $V_{DGo} + V_T$ and constant $I_D$ performed on identical standard-parameter PHEMTs in nitrogen environment. $W_g = 160\mu$m.

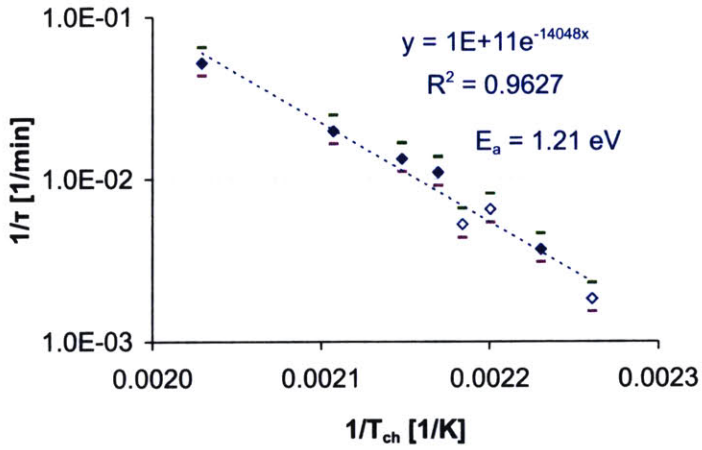



Figure 3-21: Arrhenius plot of $R_D$ degradation rate for series of constant $V_{DGo} + V_T$ and constant $I_D$ experiments performed on standard-parameter PHEMTs in nitrogen environment under various $T_{amb}$ and stressing $I_D$ (same experiments summarized in Table 3.2). Error bars (assuming 20% uncertainty in measurement of $\tau$) indicated by magenta and green lines.

As was done in Sec. 3.5.2 we examined the possible variation of $E_a$ due to uncertainties in the experimental data. The biggest contributor to changes in $E_a$ was the uncertainty in the values of $\tau$. As mentioned previously, the amount of degradation under given stressing conditions varies slightly, thus causing variations on $\tau$. For our on-state experiments we determined that the uncertainty in $\tau$ was about 20%. This was used to construct the error bars shown along with the data in Fig. 3-21. From this it was determined that the minimum and maximum values of $E_a$ for this set of data were 1.10 and 1.40 eV, respectively. Thus we can say that the extracted value of 1.21 eV is accurate to $\pm 0.2$ eV.

An activation energy was also extracted for the decrease in $I_{max}$. To represent the degradation rate, $1/\tau$ was used, where $\tau$ was the time required for a 1.5% decrease of $I_{max}$. Since in these experiments, relatively little $I_{max}$ degradation was observed, only the three hottest devices (with the most reduction in $I_{max}$) were used in this analysis. Fig. 3-22 shows the Arrhenius plot containing these data points. Here one can see that the temperature dependence can be fitted to an activation energy of $E_a = 2.18 \pm 0.3$ eV. The fact that this activation is much higher than that for $R_D$ can explain why the $I_{max}$ degradation is not as readily observed under these conditions.

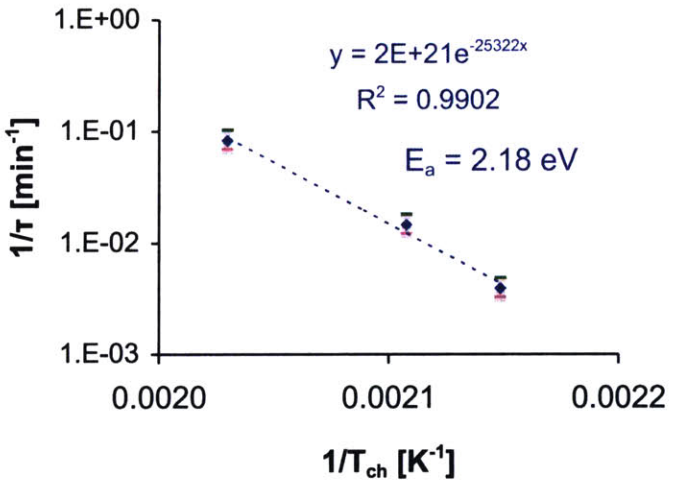



Figure 3-22: Arrhenius plot of $I_{max}$ degradation rate for series of constant $V_{DGo} + V_T$ and constant $I_D$ experiments performed on standard-parameter PHEMTs in nitrogen environment under various $T_{amb}$ (includes experiments summarized in Table 3.2). Error bars (assuming 20% uncertainty in measurement of $\tau$) indicated by magenta and green lines.

## 3.6 Time Evolution of Degradation

In order to obtain better physical understanding of the mechanisms behind the degradation, we closely examined the time evolution of $R_D$ during stressing. We focused on the $R_D$ degradation in the on-state experiments, since in that case $R_D$ degradation was more readily observed than $I_{max}$ degradation.

We looked at the time evolution of $R_D$ in various on-state experiments, and attempted to fit the data to various mathematical models. For this analysis, the percentage increase from the minimum value of $R_D$ (not the inital value) was examined. This allowed us to factor out the transient decreases in $R_D$ observed in the initial data points and thus make better comparisons between the relative amount of degradation in the experiments.

Fig. 3-23 shows a log-log plot of the percent increase of $R_D$, for the same set of stressing experiments observed in Fig. 3-17. From this graph one can see that although the devices have varying levels of degradation (due the differences in temperature), they all seem to follow the same general pattern; there seems to be two "regimes" of degradation. For initial stages of degradation (less than 10% increase in $R_D$), the degradation seems to be more or less linear in time. But then the degradation slows down, becoming closer to a logarithmic dependence in time. The logarithmic behavior is better seen in Fig. 3-24, which shows a semi-log plot of the same data with both the linear and log fits superimposed. As one can see, in each case these fits are very close to the actual data. Other fits (including power fits, with $n \approx 0.6$) could also be fitted to the 2nd regime data reasonably well, but did not seem to fit as well as logarithmic fits, which seemed to better capture the slowing down of the degradation with longer times.

This dual-regime behavior of the degradation of $R_D$ now gives us some insight into the underlying mechanism. In fact, this time dependence observed in the increase in $R_D$ (initial linear behavior, followed by logarithmic) is the same as the dependence observed for oxide growth on GaAs [33]. Initially, as a GaAs surface is oxidized, the oxide layer is thin so the oxide growth at the GaAs/oxide interface is simply limited by the reaction rate, thus giving a linear dependence in time. However, as the oxide layer thickens, the oxide formation then becomes limited by the

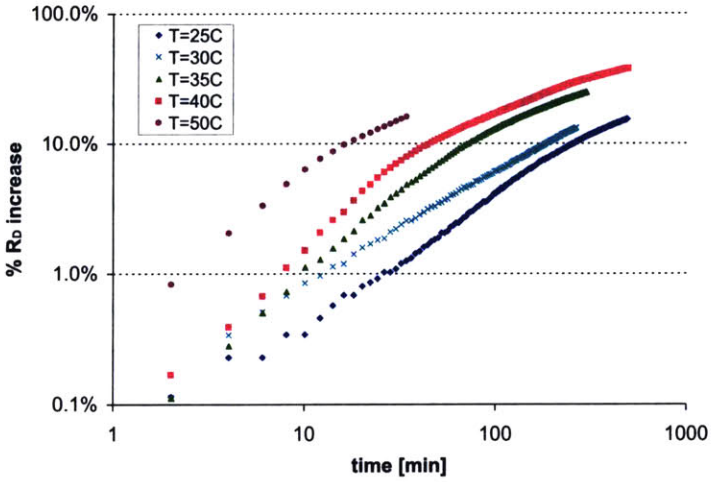



Figure 3-23: Log-log plot of percent increase of $R_D$ versus stressing time for series of constant $V_{DGo} + V_T = 6.0$ V and constant $I_D = 400$ mA/mm experiments performed on standard-parameter PHEMTs in nitrogen environment at $T_{amb} = 25$, 30, 35, 40, and 50°C. (same experiments shown in Fig. 3-17).

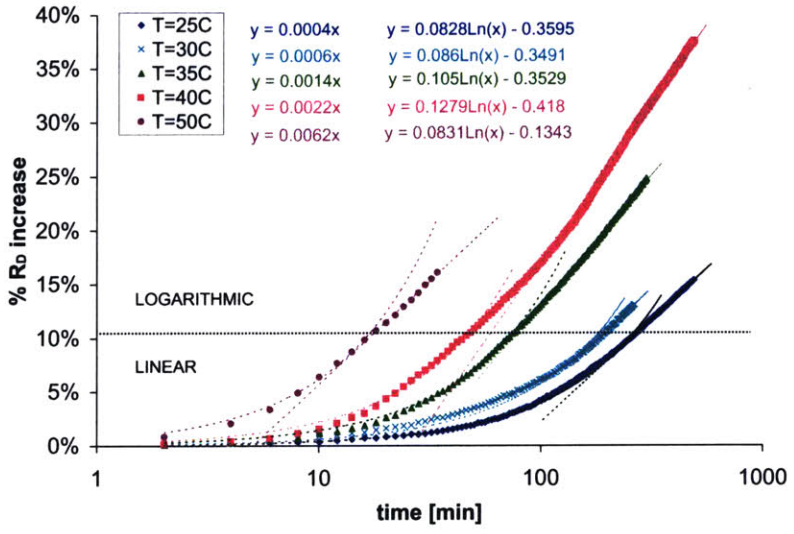



Figure 3-24: Semi-log plot of percent increase of $R_D$ versus stressing time for series of constant $V_{DGo} + V_T$ and constant $I_D$ experiments performed on standard-parameter PHEMTs in nitrogen environment at $T_{amb} = 25$, 30, 35, 40, and 50°C. (same experiments shown in Fig. 3-17) Linear and logarithmic fits are shown for each set.

*transport* of the oxidizing agent (e.g. oxygen or water) to the GaAs/oxide interface [33]. This transport process has been observed to have a logarithmic dependence by several [33–35].

Physically, a logarithmic growth law is caused by some physical mechanism involving an exponentially decreasing particle current that is limiting the oxide growth [36]. This has been attributed to several different physical phenomena; one theory is that it is due to constraints on ion diffusion imposed either by void formation or space charge in the oxide, caused by a large interfacial barrier which prevents the injection of electrons into the oxide [34]. A growth rate limited by ion diffusion alone would give a square-root dependence in time, so another limiting transport process as mentioned must be involved to result in a logarithmic growth rate.

So this suggests that the observed increase in $R_D$ could be directly related to the growth of an oxide layer on the semiconductor surface, on the drain side of the device. A possible theory is that in the initial stages of stressing, an oxide begins to form on the surface, as a result of a reaction with oxygen/water from the atmosphere and electrons at the surface. At first, the oxide layer is very thin so the oxide growth rate is linear in time, hence resulting in a linear degradation of $R_D$. However, eventually the oxide layer becomes thick enough so that further oxide growth is limited by the arrival of electrons to the GaAs/oxide interface, resulting in a logarithmic growth rate. Thus, the increase of $R_D$ eventually slows down to follow a logarithmic dependence on time.

## 3.7 Materials Analysis

The previous section suggested a correlation between the degradation of $R_D$ and oxide growth. In [7], a correlation was found between $I_{max}$ degradation and the formation of corrosion layer. However, in order to confirm our theory that corrosion was ultimately responsible for the observed degradation of $R_D$ and $I_{max}$ , we had STEM and EDX analyses performed on select devices that were degraded in our stressing experiments. We had these analyses performed on devices degraded in both air and nitrogen environments, and under off-state and on-state environments, in order to examine any differences in the form of degradation.

### 3.7.1 Off-State Stressing

For the materials analysis of off-state degradation, we chose a standard-parameter $W_g = 100\mu$m PHEMT that had been stressed at $T_{amb}$=75°C in air (same device stressed in Fig. 3-7). $I_D$ was kept constant at 10 mA/mm, and $V_{DGo} + V_T$ was stepped from 10 to 15 V in regular intervals. Since under these conditions, devices stressed in nitrogen exhibited the same degradation as in air, only one sample (the device stressed in air) was sent in for analysis. The time evolution of the degradation of $R_D$ and $I_{max}$ for this device can be seen in Fig. 3-7 in Sec. 3.2. Note that although there is less than a 10% increase in $R_D$, $I_{max}$ is reduced by more than 20%.

Fig. 3-25 shows the STEM device cross-section of the degraded PHEMT. One can clearly see that there is damage on the AlGaAs surface, as indicated by the red circle. There is also some damage on the n-GaAs and n+GaAs ledges, on both the source and drain sides, but it appears to be relatively minor compared to that on the AlGaAs. The damage on the AlGaAs can be seen more clearly in Fig. 3-26, which zeroes in on the gate and the surrounding inner recess. As one can see, the damage on the AlGaAs is only on the drain side.

To confirm that the damage observed on the AlGaAs is due to corrosion, EDX analysis was performed to determine the composition of the damaged region. Fig. 3-27 shows the EDX data of a selected area of the damaged region (indicated by inset image). This shows that there is a significant amount of oxygen present, among Ga, As, and Al. Thus this indicates that the damaged

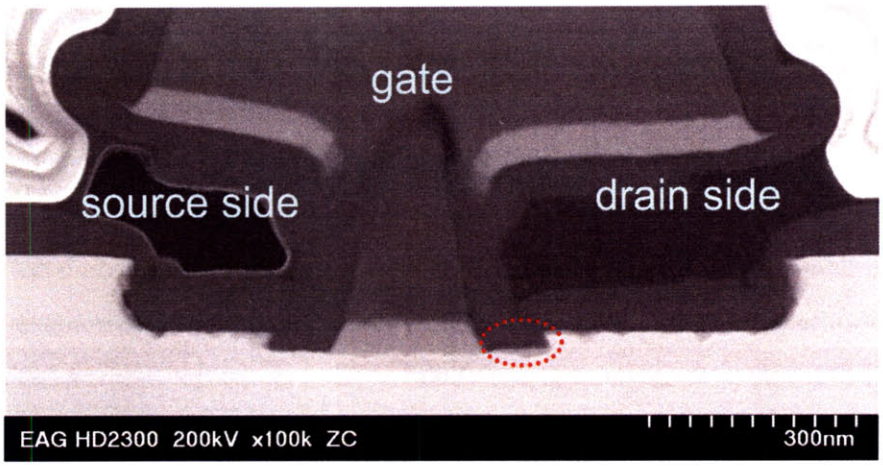



Figure 3-25: STEM image of device cross-section of standard-parameter PHEMT after 1300 min of off-state stressing in air. Stressing conditions: $V_{DGo}+V_T$ = 10-15 V, $I_D$ = 10 mA/mm, $T_{amb}$ = 75°C. $W_g$ = 100$\mu$m.

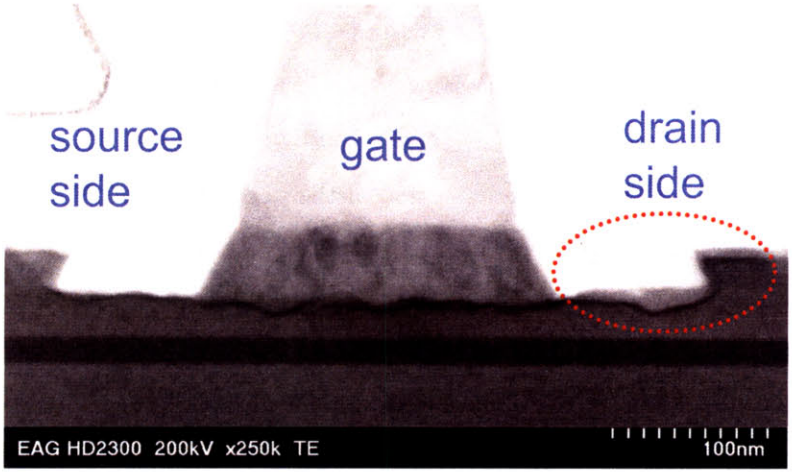



Figure 3-26: STEM cross-section image of intrinsic region of standard-parameter PHEMT after 1300 min of off-state stressing in air. Stressing conditions: $V_{DGo}+V_T$ = 10-15 V, $I_D$ = 10 mA/mm, $T_{amb}$ = 75°C. $W_g$ = 100$\mu$m.

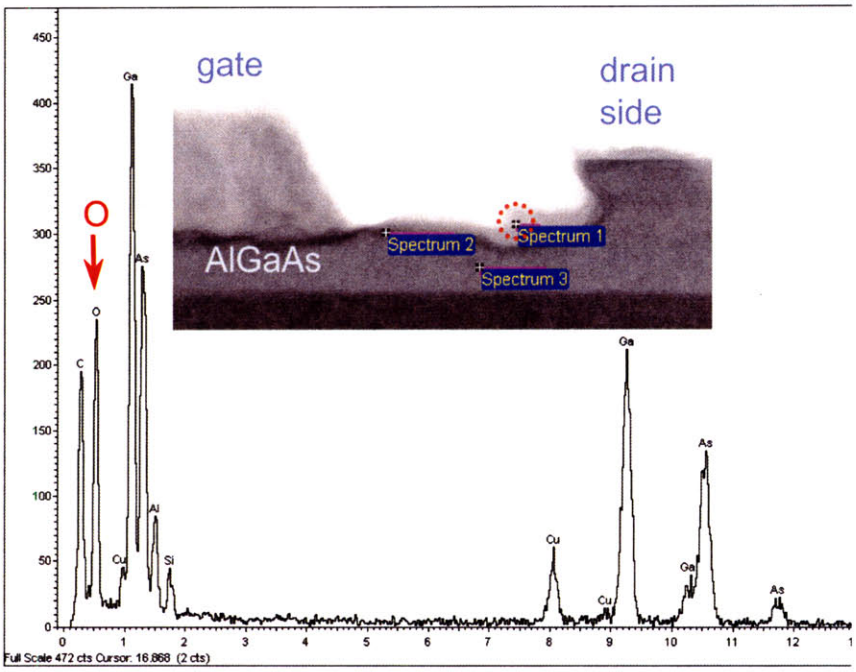
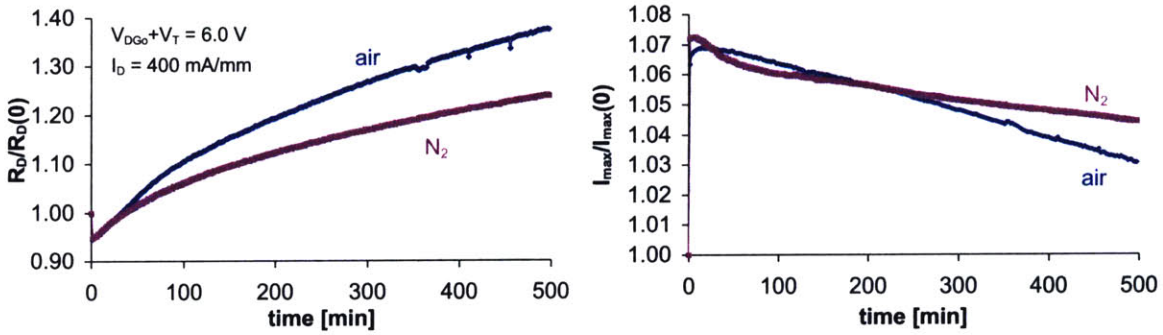



Figure 3-27: EDX analysis on select area of damaged region (indicated by red circle) on standard-parameter PHEMT after of-state stressing in air. Peaks indicate the various elements present.

region is indeed an oxide layer, formed by corrosion of the AlGaAs surface.

### 3.7.2 On-State Stressing

For the materials analysis of on-state degradation, we chose two standard-parameter $W_g = 160\mu$m PHEMTs that had been stressed at constant $V_{DGo} + V_T$ and constant $I_D$ at $T_{amb}$=35°C. One was stressed in air, the other in nitrogen. Fig. 3-28 below shows the degradation of $R_D$ and $I_{max}$ for both of these experiments. As expected, the device stressed in air showed significantly more degradation. And in both cases, $I_{max}$ does not decrease much (less than 5%), but $R_D$ increases by more than 20%. Fig. 3-29 shows the time evolution of the off-state breakdown voltage for these devices. Although both exhibited a decrease in $BV_{DGoff}$, the device stressed in air shows a much larger reduction in $BV_{DGoff}$, indicating some major gate-drain leakage current was induced by the degradation.




(a) (b)

Figure 3-28: Time evolution of normalized $R_D$ (a) and $I_{max}$ (b) for constant $V_{DGo}+V_T$ and constant $I_D$ experiments performed on standard-parameter PHEMTs in air and nitrogen environments at $T_{amb} = 35$°C. $W_g = 160\mu$m.

Fig. 3-30 shows the STEM device cross-sections of the two PHEMTs. One can see that both devices exhibit significant damage on the drain side, as indicated by the red circles. There is some slight damage on the source side as well, but it is not as much as on the drain. Fig. 3-31 shows STEM cross-section images of the drain side in each case. Although both show heavily damaged regions on the n-GaAs ledge (yellow circles) and n+GaAs ledge (red circles), the device stressed in air shows more extensive degradation on the surface. This can be seen more clearly in Fig. 3-32,

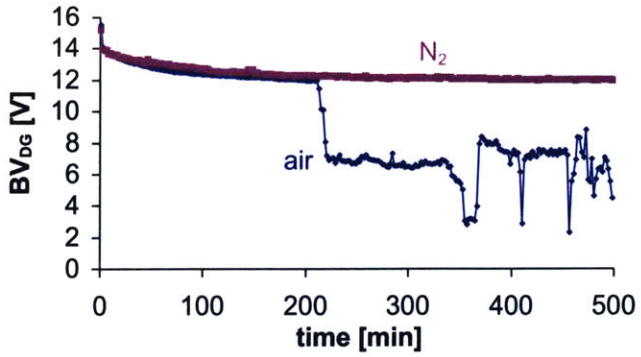
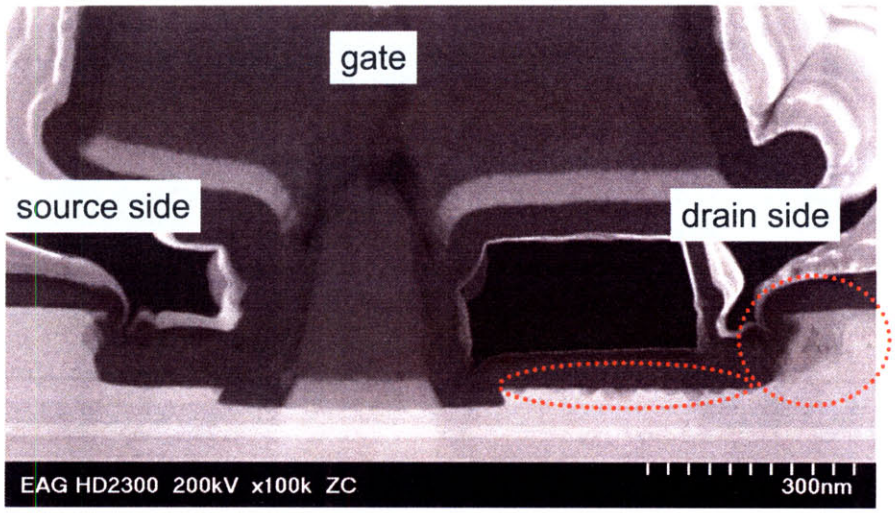


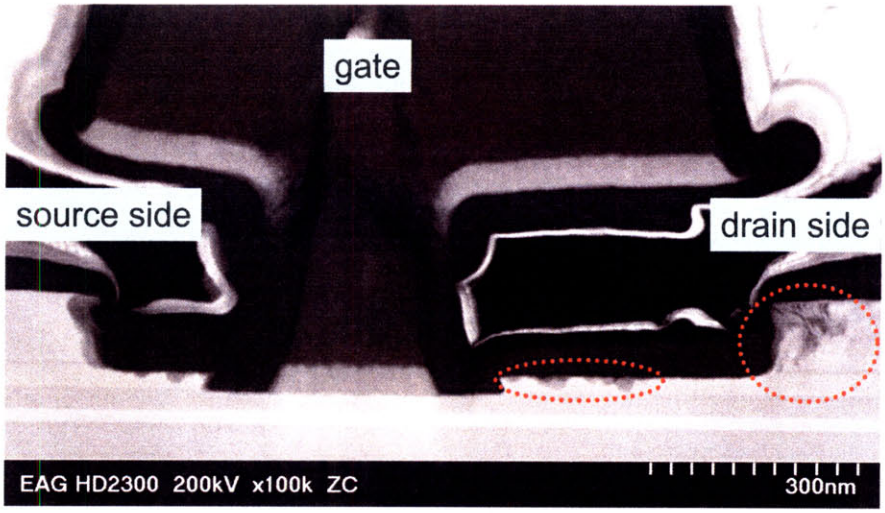

Figure 3-29: Time evolution of normalized $BV_{DGoff}$ for constant $V_{DGo} + V_T$ and constant $I_D$ experiments performed on standard-parameter PHEMTs in air and nitrogen environments at $T_{amb} = 35°C$. $W_g = 160\mu m$.

which are STEM images focusing on the damaged n+GaAs region in each device. As highlighted by the dashed lines, the device stressed in air clearly has more degradation along the semiconductor surface. In both cases, there appears to be some crystallographic defects underneath the degraded layer. This type of damage is not observed on the source side.

In order to confirm that the damage on the drain side observed in these images is due to corrosion, we had EDX analysis performed to determine the composition of the damaged regions. Fig. 3-33 shows the EDX data of a selected area of the damaged region near the surface (indicated by inset image), for both devices. One can see that in both cases, the main elements present are Ga, As, and O, thus indicating that the damaged region indeed consists of oxides of Ga and As. Note that the device stressed in air appears to have a relatively higher amount of oxygen present, indicating a higher level of oxidation.

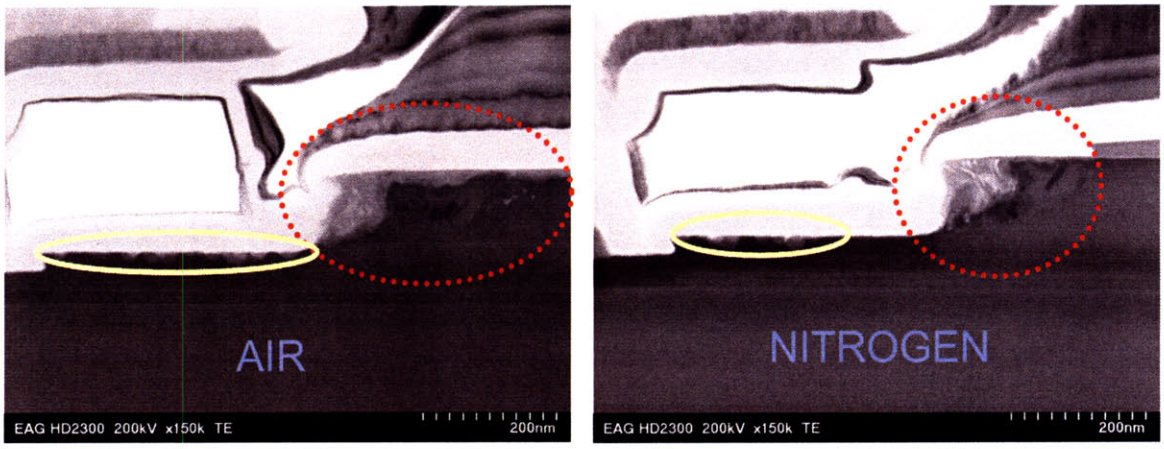



(a)



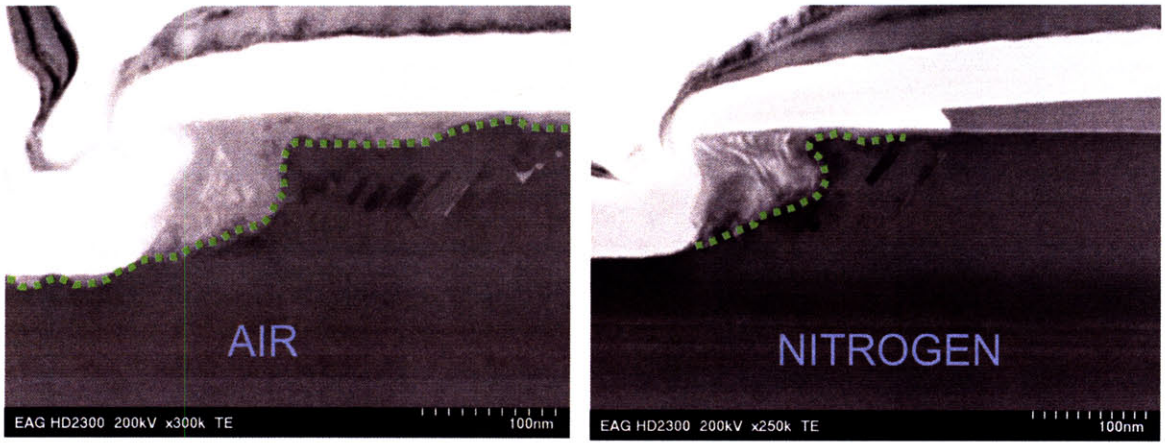

(b)

Figure 3-30: STEM image of device cross-section of standard-parameter PHEMT after 500 min of on-state stressing in air (a) and nitrogen (b). Stressing conditions: $V_{DGo} + V_T = 6.0$ V, $I_D = 400$ mA/mm, $T_{amb} = 35°C$.



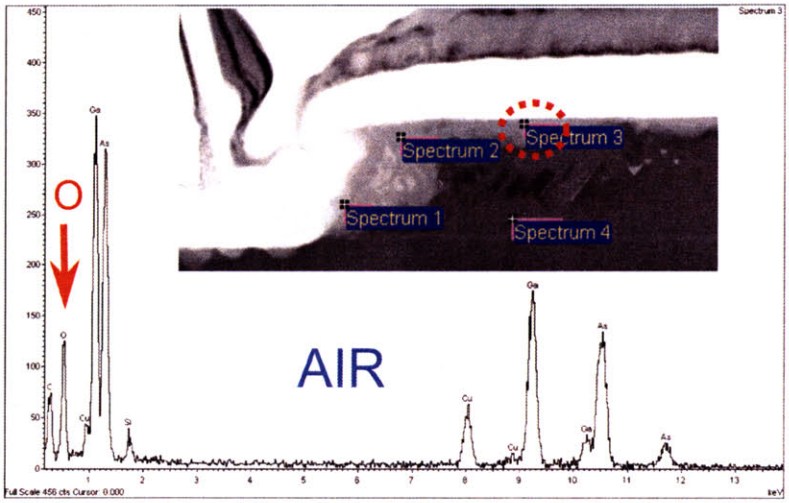

(a) (b)

Figure 3-31: STEM cross-section image of drain side of standard-parameter PHEMT after on-state stressing in air (a) and nitrogen (b). Yellow circles indicate damage on n-GaAs layer, and red circles indicate damage on n+GaAs layer.

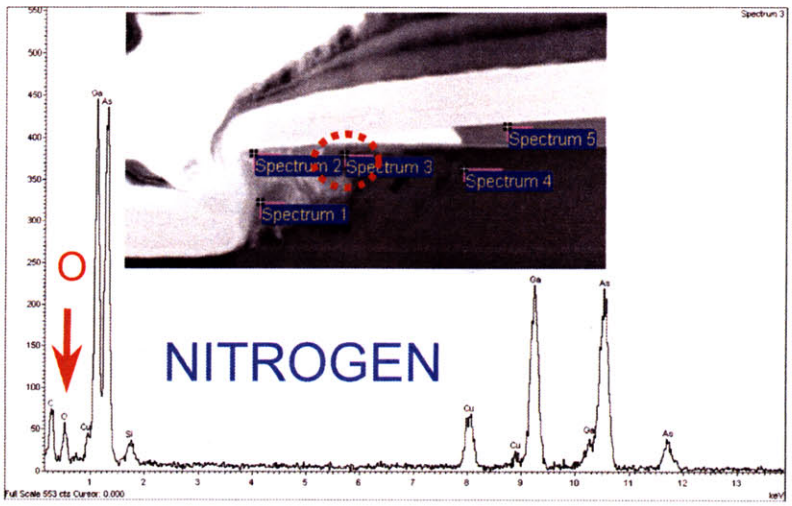



(a) (b)

Figure 3-32: STEM cross-section image focusing on damaged region on drain side of standard-parameter PHEMT after on-state stressing in air (a) and nitrogen (b). Dashed lines outline corroded regions.




(a)




(b)

Figure 3-33: EDX analysis on select area of damaged region (indicated by red circle) on standard-parameter PHEMT after on-state stressing in air (a) and nitrogen (b). Peaks indicate the various elements present.

## 3.8 Discussion

Now that we have examined the degradation of $R_D$ and $I_{max}$ under a variety of stressing conditions and have observed physical evidence of the damage occurring, we can make some general comments and then propose hypotheses regarding the mechanisms.

A summary of the various observations for the $R_D$ and $I_{max}$ degradation discussed in this thesis is given in Table 3.3. An important thing to note is the difference in $R_D$ and $I_{max}$ degradation observed in off-state and on-state conditions. As illustrated in Fig. 3-1 and Fig. 3-2, in the on-state the increase of $R_D$ is much more readily observed than the reduction of $I_{max}$. And as evidenced in Fig. 3-7, in the off-state experiments, $I_{max}$ degrades much more than $R_D$.

This is more clearly seen in Table 3.4, which compares the total degradation observed in $R_D$ and $I_{max}$ in two standard-parameter PHEMTs, one degraded under off-state stress and the other under on-state stress. From this it is clear that the degradation of $R_D$ is more prevalent under on-state stress, whereas $I_{max}$ degradation is more prevalent under off-state stressing.

The devices described in Table 3.4 were among the devices analyzed with STEM/EDX in the previous section. As discussed in Sec. 3.7.1, the device stressed in the off-state condition (which had 22% reduction in $I_{max}$) exhibited a corrosion layer on the AlGaAs surface, on the drain side of the inner recess. This damage was not observed in the device stressed in the off-state condition, which only had a 4% reduction in $I_{max}$. Therefore, we can correlate the reduction of $I_{max}$ with corrosion on the AlGaAs surface in the inner recess.

In an analogous manner, we can correlate the increase of $R_D$ with corrosion on the n+GaAs ledge, on the drain side. As described in Sec. 3.7.2, the device stressed in the on-state condition (which had a 38% increase in $R_D$) exhibited major corrosion on the corner of the n+GaAs cap on the drain side. In contrast, the damage to the n+GaAs cap on the device stressed in the off-state condition (which had only a 9% increase in $R_D$) was very minor.

In each case, the corrosion results from chemical reactions with oxygen and/or moisture at the semiconductor surface. The oxygen or moisture can come from the air environment, but also must be coming from residual $O_2/H_2O$ on the surface or from the $SiO_2$ passivation, as there is

| Effect of... | $\mathbf{R_D}$ **increase** | | $\mathbf{I_{max}}$ **decrease** | |
|---|---|---|---|---|
| | *On-state* | *Off-state* | *On-state* | *Off-state* |
| Electric Field | accelerated with $V_{DGo}+V_T$ | accelerated with $V_{DGo}+V_T$ | Accelerated with $V_{DGo}+V_T$ | Accelerated with $V_{DGo}+V_T$ |
| Environment | Reduced in $N_2$ | $T_a$ < 100°C: independent of environment, $T_a$ > 100°C: suppressed in $N_2$ | Reduced in $N_2$ | $T_a$ < 100°C: independent of environment, $T_a$ > 100°C: suppressed in $N_2$ |
| Temperature | Strong positive dependence ($E_a \sim 1.2$eV) | Weak positive dependence ($E_a \sim 0.3$eV) | Strong positive dependence ($E_a \sim 2.2$eV) | Weak positive dependence ($E_a \sim 0.3$eV) |
| Drain Current | Positive dependence, due to $T_{ch}$ increase | no major effect up to 20 mA/mm | Positive dependence, due to $T_{ch}$ increase | no major effect up to 20 mA/mm |
| Level of Degradation | $R_D$ increase <~50% | $R_D$ increase <~10% | $I_{max}$ decrease <~7% | $I_{max}$ decrease <~22% |
| Time Evolution | initially linear, then logarithmic | | | |
| Location of Degradation | on drain side, corner of n+GaAs cap, n-GaAs surface | slight damage on n-GaAs surface | | AlGaAs surface (inner recess) on drain side, slight damage on n-GaAs surface |

Table 3.3: Summary of the various observations on the degradation of $R_D$ and $I_{max}$ under various stressing experiments.

| Type of Stressing | Bias Conditions | Temperature | $\Delta R_D$ | $\Delta I_{max}$ |
|---|---|---|---|---|
| Off-state | $I_D$ = 10mA/mm, $V_{DGo}+V_T = 10-15$V, 1300 min | $T_a$ = 75°C, $T_{ch} \approx 80$°C | +9% | **−22%** |
| On-state | $I_D$ = 400mA/mm, $V_{DGo} + V_T$ = 6.0V, 500 min | $T_a$ = 35°C, $T_{ch} \approx 190$°C | **+38%** | −4% |

Table 3.4: Stressing conditions and resulting degradation for on-state and off-state experiments performed on standard-parameter PHEMTs in air. For on-state experiment, $W_g = 160\mu$m, and for off-state experiment, $W_g = 100\mu$m.

degradation observed even in nitrogen environments. Our hypothesis is that the semiconductor surface that is being oxidized (either the AlGaAs or the n+GaAs cap) acts as the anode, and the gate metal acts as the cathode. Since it is generally believed that holes accumulated at the surface are what induce corrosion in GaAs [37], the following oxidation reaction is proposed to proceed at the anode:

$$\mathrm{GaAs} + 6h^+ \rightarrow \mathrm{Ga^{3+}} + \mathrm{As^{3+}} \tag{3.3}$$

At the gate electrode, the following reduction reaction will occur:

$$\frac{1}{2}\mathrm{O_2} + \mathrm{H_2O} + 2\mathrm{e^-} \rightarrow 2\mathrm{OH^-} \tag{3.4}$$

The resulting $OH^-$ ions diffuse through the passivation layer to the oxidized semiconductor surface and cause further reactions to with the Ga and As ions, which result in the formation of oxides and/or hydroxides of Ga and As [38]:

$$\mathrm{Ga^{3+}} + 3\mathrm{OH^-} \rightarrow \mathrm{Ga(OH)_3} \tag{3.5}$$

$$2\mathrm{Ga^{3+}} + 6\mathrm{OH^-} \rightarrow \mathrm{Ga_2O_3} + 3\mathrm{H_2O} \tag{3.6}$$

$$\mathrm{As^{3+}} + 3\mathrm{OH^-} \rightarrow \mathrm{As(OH)_3} \tag{3.7}$$

$$2\mathrm{As^{3+}} + 6\mathrm{OH^-} \rightarrow \mathrm{As_2O_3} + 3\mathrm{H_2O} \tag{3.8}$$

Schematics illustrating this corrosion mechanism for the degradation of $R_D$ and $I_{max}$ are shown in Fig. 3-34. This general corrosion mechanism can explain how the damaged regions observed in our STEM/EDX analysis are formed. Although we do not know the exact chemical makeup of the damaged regions, from the EDX analysis we do know that they consist of some kind of oxides of Ga and As.

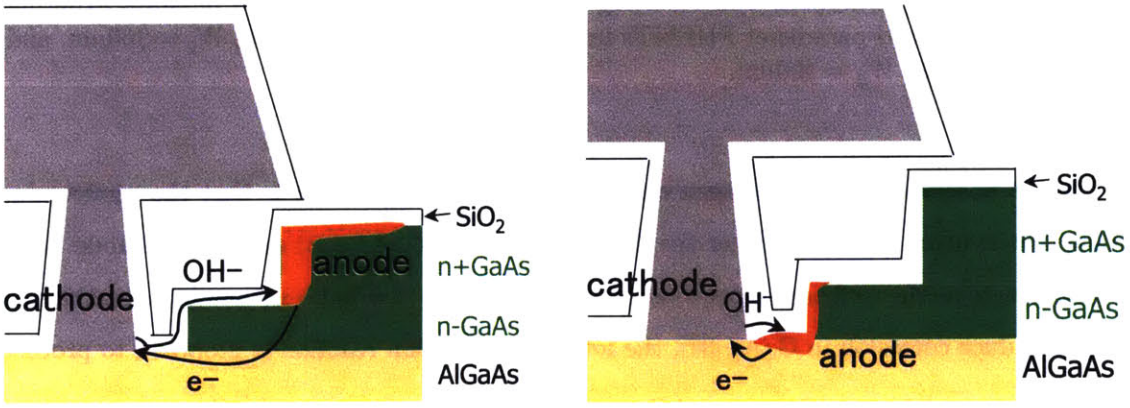



Figure 3-34: Schematics illustrating corrosion mechanism behind degradation of $R_D$(a) and $I_{max}$(b). The semiconductor surface (either n+GaAs or AlGaAs) acts as the anode whereas the gate metal acts as the cathode. Ionic species diffuse through the $SiO_2$ passivation layer.

Since it is unclear which of Eq. 3.5- 3.8 proceed and what type of oxides are eventually formed, it is difficult to define an overall chemical reaction for the corrosion and thus determine the reaction rate. However, we can still obtain the general form of the rate for the corrosion, which can help to understand the mechanism behind the observed degradation. We know that the corrosion rate depends on the reaction rate constant ($k_{corr}$), and the concentration of the reactants [39]:

$$rate = k_{corr}[\text{reactants}] = Ae^{-E_a/kT}[\text{reactants}] \tag{3.9}$$

Here $A$ is a constant and $E_a$ is the activation energy for the reaction (in eV), and $k$ is the Boltzmann constant ($8.63 \times 10^{-5}$ eV/K). Note that the rate constant $k_{corr}$ has an Arrhenius de-

pendence on temperature, which is consistent with the temperature dependences observed for the degradation of both $R_D$ and $I_{max}$. Also, note how the corrosion rate depends on the concentration of reactants, which will include $O_2$ and $H_2O$. This can explain the accelerated degradation in air environments.

Although both the degradation of $R_D$ and $I_{max}$ involve corrosion of GaAs, they occur in different locations. Whether the corrosion happens on the n+GaAs or the AlGaAs seems strongly connected to the particular stressing conditions. Thus we need to compare the physics of what is going on in the on-state and off-state conditions. In the on-state, the electric fields are moderately high (typically $V_{DGo} + V_T = 6 - 7$ V) and the current is extremely high (typically $I_D = 400$mA/mm) so there is a large amount of power dissipation, causing high channel temperatures ($T_{ch} > 170°$C). Now in the off-state conditions, there is very little current (typically $I_D = 10$mA/mm) so there is very little impact ionization, but the *electric field* is much higher ($V_{DGo} + V_T = 10 - 15$V). And since there is negligible self-heating, $T_{ch} = T_{amb}$ so the temperatures are usually much lower than in the on-state. Thus it seems like under high channel temperatures, the corrosion is more likely to happen on the n+GaAs, and under high-electric fields, the corrosion is more likely to occur on the AlGaAs. This can be seen by looking the activation energies for each type of degradation, over a range of biasing conditions. Fig. 3-35 shows the activation energies for $\Delta R_D$ and $\Delta I_{max}$ extracted from various stressing experiments, as a function of $V_{DGo} + V_T$. First of all, one can see that for $V_{DGo} + V_T = 6.0$ V (on-state condition), the activation energy for $\Delta I_{max}$ ($E_a \sim 2.2$ eV) is much higher than that for $\Delta R_D$ ($E_a \sim 1.2$ eV). The higher activation energy can explain why $I_{max}$ is less readily observed in the on-state condition.

The reason why the activation energy is higher for $I_{max}$ degradation could be related to the availability of holes in both types of degradation. First, one should recall that the oxidation of GaAs as shown in Eq.3.3 requires holes. Since holes are generated by the transfer of electrons from the valence band to the conduction band, then one would expect that the availability of holes to be related to the bandgap of the semiconductor. For GaAs, the band gap is $E_g = 1.42$ eV, whereas for AlGaAs (in our devices, Al fraction is 0.24), $E_g = 1.7$ eV [40]. The higher bandgap for AlGaAs can thus explain the higher activation energies for the $I_{max}$ degradation, which is associated with

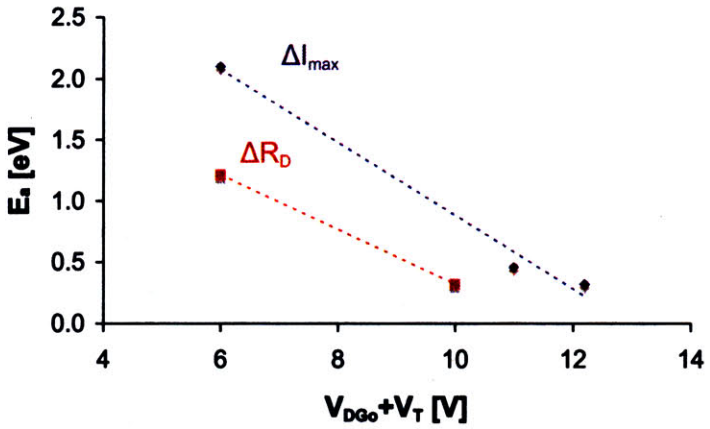



Figure 3-35: Extracted activation energies for degradation of $R_D$ and $I_{max}$ as a function of $V_{DGo} + V_T$.

corrosion on the AlGaAs.

And although both activation energies are small at high bias, recall that the $R_D$ degradation is not as readily observed in the off-state as it is in the on-state. An explanation for this could be that in general, AlGaAs is more readily oxidized than GaAs. This hypothesis is supported by various reports in the literature demonstrating that the oxidation of AlGaAs is significantly accelerated with increasing Al content [41, 42], since the oxidation of AlAs compared to GaAs is more thermodynamically favorable [43]. This is attributed to the extreme reactivity of Al and its tendency to form various oxygen-rich compounds [44]. Although most of these reports are for thermally-grown oxides on AlGaAs with high Al-content (Al fraction $> 0.8$), one can still use these findings to hypothesize that for the same conditions, the corrosion rate for the AlGaAs in our devices (Al fraction $= 0.24$) is likely higher than that of the n+GaAs, due to the increased reactivity of aluminum. Thus this could explain why the n+GaAs does not corrode much in the off-state condition, in spite of similar activation energy ($E_a \sim 0.3$ eV).

The main thing to note from Fig. 3-35, however is how the activation energies decrease with increasing $V_{DGo}+V_T$. This phenomenon can be explained by an electrochemical phenomenon called *anodic activation polarization*. By introducing a bias on the anode, the energy of the atoms on the anode surface are increased, making it more favorable for the atoms to form ions [45]. This is

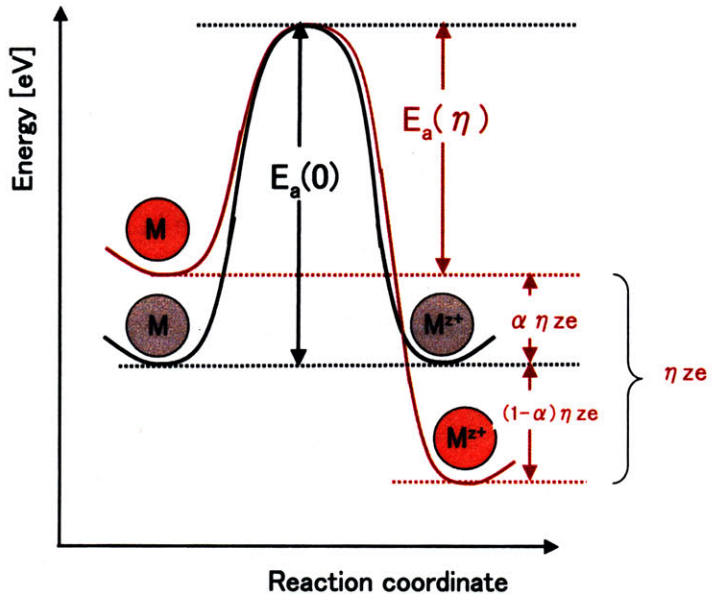



Figure 3-36: An energy profile for an anode at equilibrium (black) and a similar profile for anodic activation polarization, for generic anode reaction $M \rightleftharpoons M^{z+} + ze^-$. Adapted from [39].

illustrated in Fig. 3-36, which shows the energy profile for a generic anode at equilibrium and the profile under anodic activation polzarization (adapted from [39]). The overpotential (in volts) is denoted by $\eta$, and the amount of anodic polarization is denoted as $\alpha\eta$. To convert to an energy scale (in eV), the amount of polarization is scaled by $ze$, where $z$ is the valence, or number of electrons in the anodic reaction (e.g. for oxidation Ga or As, would be 3), and $e$ is the charge of one electron. As illustrated in this graph, the anodic polarization causes the atoms at the surface to be at higher energy, which effectively reduces the energy barrier required for them to become ionized. Quantitatively, the activation energy is reduced by $\alpha\eta ze$, resulting in the new activation energy $E_a(\eta) = E_a(0) - \alpha\eta ze$. From this one can easily see that as $\eta$ is increased, the resulting activation energy will be decreased further. This phenomenon can thus explain the dependence on activation energy with bias that is observed for the degradation of both $R_D$ and $I_{max}$. This can also explain why the drain-gate bias is so critical for degradation, and why temperature alone is not the only accelerating factor.

In addition to $R_D$ and $I_{max}$, the corrosion on the surface also seems to affect the off-state

breakdown voltage, $BV_{DGoff}$. Because the degradation of $R_D$ and $I_{max}$ reduce the peak electric-field and $n_s$ on the drain side, one would expect an improvement in $BV_{DGoff}$ during stressing. However, in our experiments a decrease in $BV_{DGoff}$ is typically observed, especially under on-state stressing in air. This decrease is accompanied by an increase in the magnitude of $I_G$. As shown in Sec. 3.7.2, the device stressed in air (which had major decrease in $BV_{DGoff}$) had more extensive corrosion on the surface of the n+GaAs than the device stressed in nitrogen (which did not show a significant decrease in $BV_{DGoff}$). This seems to suggest that the surface corrosion on the n+GaAs layer is somehow causing increased leakage between the gate and the drain.

## 3.9 Summary

Our various experiments and analyses have shown that increase of $R_D$ and the decrease of $I_{max}$ are indeed due to corrosion on the drain side of the device. However, they are associated with damage on different areas of the extrinsic drain. The increase of $R_D$ is mostly due to corrosion on the corner of the n+GaAs cap, whereas the reduction of $I_{max}$ is mostly due to corrosion on the AlGaAs. The general mechanism in both cases involves the oxidation of GaAs by holes at the anode (n+GaAs or AlGaAs surface), and the reduction of oxygen and water at the cathode (gate). The corrosion layer is formed by the reaction with the resulting hydroxide ions (which diffuse to the semiconductor surface from the gate) with Ga and As ions.

The location of the corrosion (n+GaAs or AlGaAs) depends on the specific stressing conditions, as the activation energies for each type of corrosion are different. The activation energy for the corrosion on AlGaAs is nominally higher than that for the n+GaAs, likely due to the higher bandgap of AlGaAs. Thus, under moderate electric fields and high channel temperatures the corrosion mostly happens on the n+GaAs cap. However, under very high electric fields, the activation energies are reduced and the corrosion mostly occurs on the AlGaAs. The reduction in activation energy with increasing drain-gate bias was attributed to anodic polarization of the semiconductor surface on the drain side, which makes it easier for Ga and As to become ionized. This phenomenon could explain why the drain-gate bias as well as temperature is important to the degradation of $R_D$ and

$I_{max}$.

Since the degradation of $R_D$ and $I_{max}$ involve corrosion reactions at a semiconductor surface, the device temperature, electric field and stressing environment play a much stronger role than impact-ionization. In order to suppress this degradation during stressing, the semiconductor surface must be prevented from becoming corroded. We found that this could be accomplished by unbiased high-temperature storage of the device for several hours. It is suggested that this heating somehow prevents oxygen and moisture in the air from reaching the semiconductor surface, or drives out residual oxygen/moisture already present.

# Chapter 4

# Change of $V_T$ and $R_S$ in PHEMTs

This chapter describes the negative shift in $V_T$ and decrease in $R_S$ observed in our electrical stressing experiments. In each case, the overall results are first presented, followed by more specific results pertaining to various additional experiments and analyses performed in order to uncover the underlying mechanisms.

## 4.1 Negative $V_T$ Shift

As shown in Sec. 3.1.1, a significant negative shift in $V_T$ is observed in our electrical stressing experiments, which has a major effect on $I_{Dss}$, $I_{max}$, and other parameters. This change was found to be mostly recoverable with unbiased storage at room temperature [23] and was independent of the stressing environment (the shift was the same, whether in air or in nitrogen). Negative shifts in $V_T$ have been previously observed in GaAs HEMTs under stress, though a wide variety of very different mechanisms have been proposed [5, 10, 12, 21, 46]. Although a hypothesis for the $V_T$ shift seen in our devices was proposed in [23], it was later discovered that some assumptions made about the relative levels of impact ionization in the devices studied were incorrect. In addition, we had yet to examine the effect of temperature on the $V_T$ shift, or the possibility of non-electrical mechanisms (such as hydrogen degradation) from possibly causing a shift in $V_T$. Thus it was necessary to revisit some of our experiments and perform a more thorough analysis, in order to determine the specific

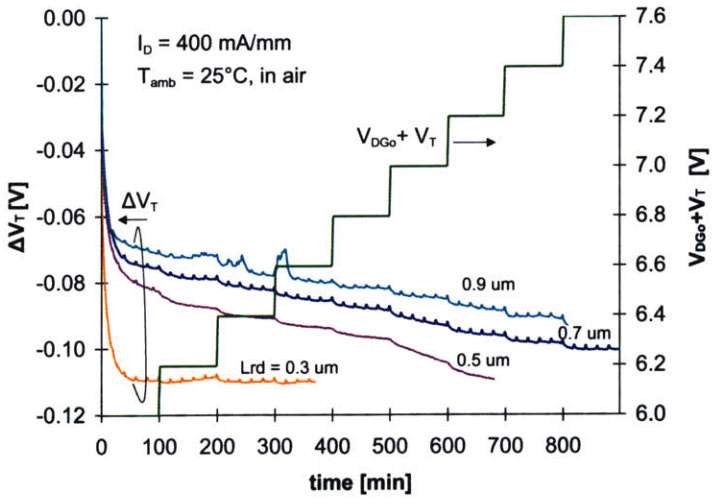



Figure 4-1: Time evolution of $\Delta V_T$, for step-stressing experiments performed on four different devices with different values of $L_{rd}$. $W_g = 100\mu$m.

mechanism responsible in this case.

### 4.1.1 Effect of $L_{rd}$

To examine the impact of impact ionization on $V_T$ shift, we examined the effect of $L_{rd}$ (the n+GaAs recess length on the drain side, as illustrated in Fig. 2-1). Initially, we assumed that devices with larger $L_{rd}$ would have less impact ionization for a given bias, since the peak electric field would be smaller. Step-stressing experiments on devices with different $L_{rd}$ were performed, and the relative shifts in $V_T$ were compared. Fig. 4-1 shows the time evolution for the change in $V_T$ for these experiments. Looking at this graph, it is clear that the shift in $V_T$ is indeed decelerated as $L_{rd}$ gets larger. This behavior thus prompted us to initially conclude that impact ionization (which was assumed to decrease with $L_{rd}$) was the driving force behind the shift in $V_T$. This consequently led us to attribute the shift to a mechanism where holes generated by impact ionization neutralize electrons trapped underneath the gate, as proposed in [21].

However, separate experiments performed later on revealed that the assumption of less impact ionization with larger $L_{rd}$ was actually not necessarily true (at least, in the devices we studied).

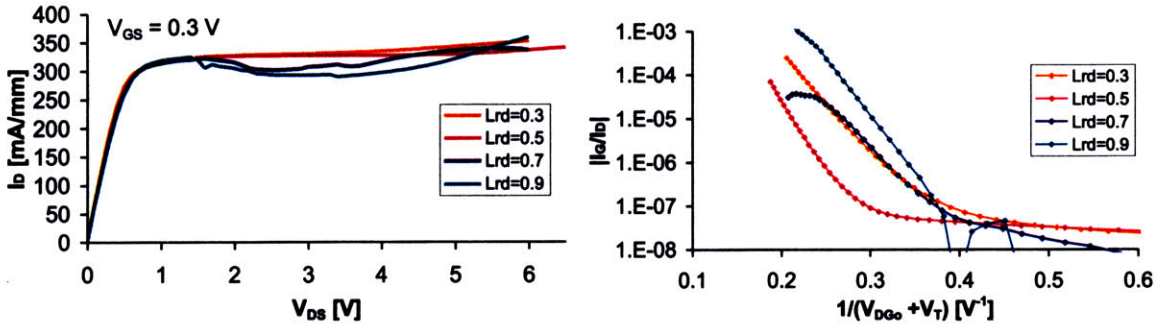
| $L_{rs}$ [$\mu$m] | $L_{rd}$ [$\mu$m] | $BV_{DGoff}$ [V] | $R_D$ [$\Omega$-mm] | $R_S$ [$\Omega$-mm] | $V_T$ [V] |
|---|---|---|---|---|---|
| 0.4 | 0.3 | 11.70 | 0.661 | 0.571 | -0.605 |
| 0.4 | 0.5 | 15.56 | 0.723 | 0.577 | -0.621 |
| 0.4 | 0.7 | 17.88 | 0.787 | 0.560 | -0.616 |
| 0.4 | 0.9 | 20.06 | 0.841 | 0.545 | -0.629 |

Table 4.1: Device Parameters and Measured Data of unstressed PHEMTs of varying $L_{rd}$. Measurements taken at 25°C in nitrogen.

This was discovered via measurements of impact-ionization on another set of devices of varying $L_{rd}$. Table 4.1 shows the device parameters and key figures of merit for this set of four devices, all identical except for the parameter $L_{rd}$. One can note that the off-state breakdown voltage $BV_{DGoff}$ increases with larger $L_{rd}$, which indicates that devices with longer $L_{rd}$ do have smaller electric fields. Despite this however, subsequent electrical measurements show that for some of these devices, electric field does not necessarily correlate with impact ionization. This is illustrated in Fig. 4-2, which shows a plot of $I_D$ vs. $V_{DS}$ and a semi-log plot of $|I_G/I_D|$ vs $1/(V_{DGo}+V_T)$ from measurements taken at $V_{GS} = 0.3$ V for each device. As one can see, although the 0.3$\mu$m and 0.5$\mu$m device seem to behave as expected (smaller $L_{rd}$ results in more impact ionization), the devices with long $L_{rd}$ ($L_{rd} = 0.7\mu$m and 0.9$\mu$m) exhibit odd output characteristics and non-linear behavior in the high $V_{DGo}+V_T$ regime. This strange behavior is attributed to oscillations on these particular devices, as discussed in [47].

Thus upon realizing that devices with very long $L_{rd}$ actually have *more* impact ionization, we had to rethink our proposed mechanism causing the $V_T$ shift during stressing. It cannot be due to a mechanism driven by impact ionization, as it cannot explain why some devices that actually have more impact ionization still end up a *slower* rate of $V_T$ degradation, as shown in Fig. 4-1. To uncover the underlying mechanism, we must examine the dependences of the $V_T$ shift on various factors. We first look at the the dependence of the $V_T$ shift on $I_G$, which will allow us to see what kind of dependence the $V_T$ shift actually has on impact ionization (if any).

A separate set of devices of varying $L_{rd}$ were electrically stressed under similar conditions, at $I_D = 400$ mA/mm, $V_{DGo}+V_T = 5.0$ V, at 25°C in nitrogen. A lower bias voltage was chosen here




(a) (b)

Figure 4-2: Plot of $I_D$ vs. $V_{DS}$ (a) and semi-log plot of $|I_G/I_D|$ vs. $1/(V_{DGo}+V_T)$ (b), for a set of measurements taken at $V_{GS}$= 0.3 V, at 25°C in $N_2$, for devices with different values of $L_{rd}$. $W_g = 100\mu$m.

in order to be able to observe the change in $V_T$ more easily. Fig. 4-3 illustrates the time evolution of $\Delta V_T$ for these experiments. Similar to what was seen in Fig. 4-1, the $V_T$ shift is slower with longer $L_{rd}$, despite higher impact-ionization. Fig. 4-4(a) shows the absolute value of the $V_T$ shift at various time points during these experiments, versus the average value of $|I_G|$ during the initial stages of stressing. As one can see, the $V_T$ shift at various points during stressing are not correlated with $|I_G|$ at all. This suggests that $\Delta V_T$ is not correlated with impact-ionization, since in that case we would expect some positive correlation with $|I_G|$. Fig. 4-4(b) shows the change in $V_T$ for those same points, but plotted versus the inverse of $L_{rd}$. Since $L_{rd}$ is expected to be completely depleted, the peak electric field should be inversely related to $L_{rd}$ (the bigger the $L_{rd}$, smaller peak electric field). Here there clearly seems to be a correlation between $\Delta V_T$ and $1/L_{rd}$, suggesting that the $V_T$ shift is actually correlated with the peak electric field. This thus suggests a field-aided de-trapping mechanism, in which trapped electrons tunnel out of traps, as suggested in [46].

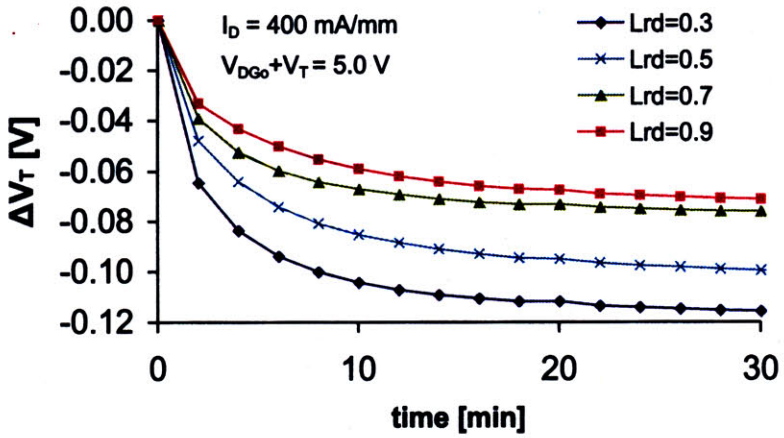



Figure 4-3: Time evolution of $\Delta V_T$, for set of stressing experiments employing constant $I_D$ = 400 mA/mm and constant $V_{DGo} + V_T = 5.0$ V, at $T_{amb} = 25°$ in air. $W_g = 160\mu$m.

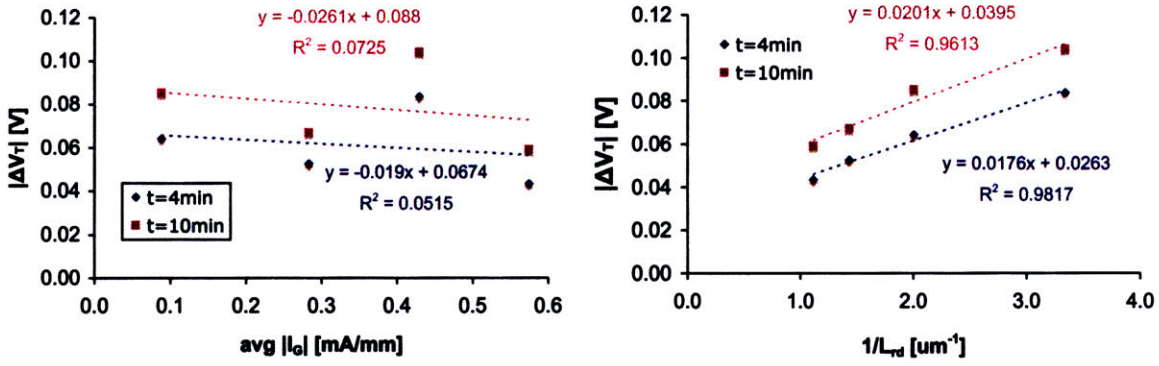



Figure 4-4: Absolute value of change in $V_T$ after $t = 4, 10$ minutes of stressing versus average gate current (a) and versus $1/L_{rd}$ (b) for stressing experiments employing constant $I_D = 400$ mA/mm and constant $V_{DGo}+V_T = 5.0$ V, at 25°C in air, on devices with different values of $L_{rd}$. $W_g = 160\mu$m.

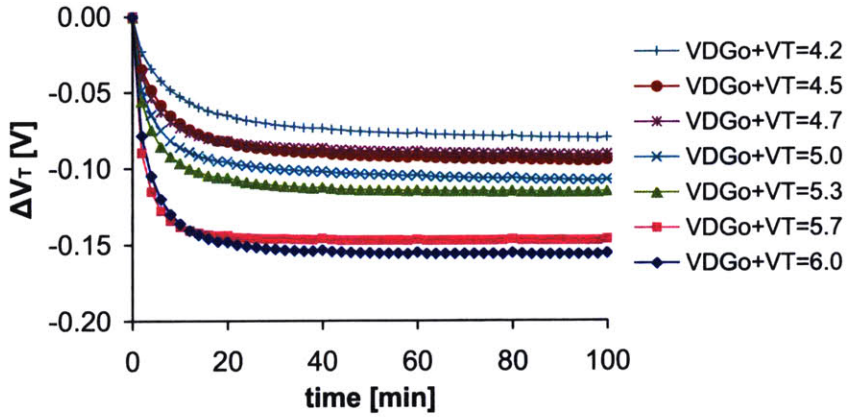



Figure 4-5: Time evolution of $\Delta V_T$, for set of stressing experiments employing constant $I_D$ = 400 mA/mm and constant $V_{DGo} + V_T$, at $T_{amb} = 25°$ in air. $W_g = 160\mu$m.

### 4.1.2 Effect of Electric Field

To further examine the dependence of $\Delta V_T$ on electric field, a set of stressing experiments employing constant $I_D$ but varying $V_{DGo} + V_T$ were performed on a set of identical devices. Fig. 4-5 shows the time evolution of the change in $V_T$ for these experiments. One can clearly see that increasing $V_{DGo} + V_T$ accelerates and increases the $V_T$ shift. If one examines the change in $V_T$ after a given amount of time, one can see that it obeys a linear dependence on $V_{DGo} + V_T$, as shown in Fig. 4-6. This further supports the correlation between the $V_T$ shift and the drain-gate electric-field. This dependence is very similar to what was observed in [46], thus confirming that a field-aided de-trapping mechanism is responsible for the change in $V_T$.

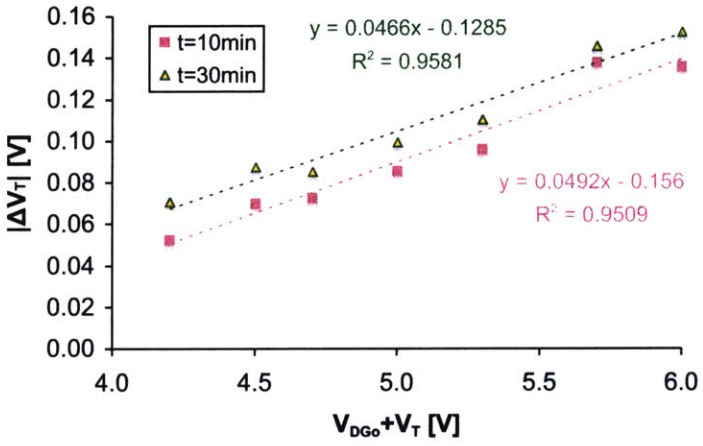



Figure 4-6: Absolute value of change in $V_T$ after $t = 10, 30$ minutes of stressing versus $V_{DGo} + V_T$, for set of stressing experiments employing constant $I_D = 400$ mA/mm and constant $V_{DGo} + V_T$, performed at $T_{amb} = 25°$ in air. $W_g = 160\mu$m.

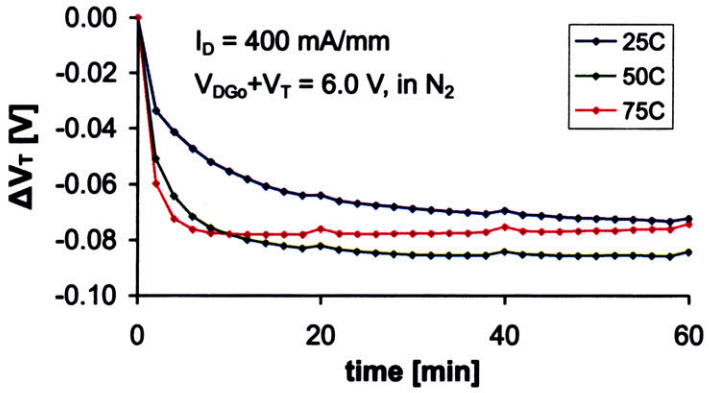



Figure 4-7: Time evolution of $\Delta V_T$, for constant $I_D$ and constant $V_{DGo}+V_T$ experiments performed on standard-parameter PHEMTs at 25, 50, 75°C in nitrogen. $W_g = 100\mu$m.

### 4.1.3 Effect of Temperature

To explore the temperature dependence of $\Delta V_T$, on-state stressing experiments performed at various ambient temperatures were performed. Fig. 4-7 shows the time evolution of $\Delta V_T$ for a set of constant $I_D$ and constant $V_{DGo} + V_T$ experiments, performed at 25, 50, 75°C in nitrogen. This shows that the shift in $V_T$ is accelerated with increasing temperature. This positive temperature dependence suggests that the de-trapping of electrons is thermally assisted to some extent.

And as discussed in Sec. 3.5.3, the channel temperature is also affected by $I_D$ and $W_g$, so consequently $\Delta V_T$ will depend on stressing current and gate width. Fig. 4-8(a) shows the time evolution of $\Delta V_T$ for a different set of stressing experiments, of varying $I_D$. Fig. 4-8(b) shows the time evolution of $\Delta V_T$ for a set of stressing experiments where $W_g$ was varied. One can see from these graphs that the change in $V_T$ is increased with either increasing $I_D$ or $W_g$.

A mathematical expression for the temperature dependence of $\Delta V_T$ will be presented in the next section, where models for the behavior of $\Delta V_T$ with time are fitted to the data and an activation energy for the degradation is extracted.

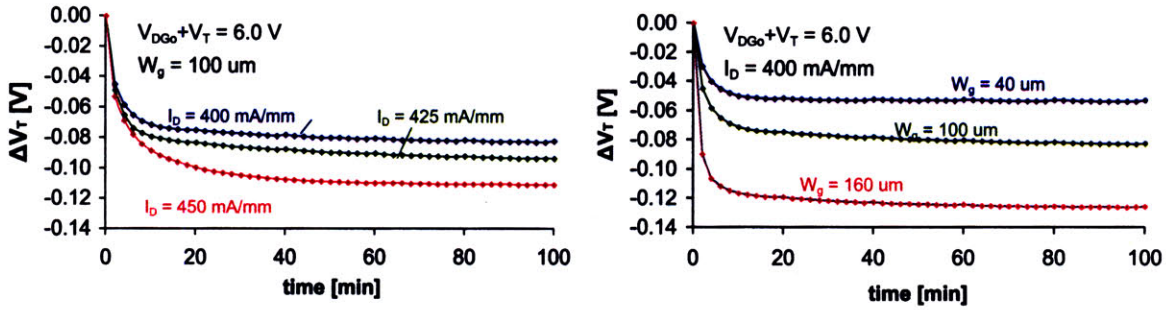



Figure 4-8: Time evolution of $\Delta V_T$ for constant $I_D$ and constant $V_{DGo} + V_T$ stressing experiments performed on standard-parameter PHEMTs in air environment at $T_{amb} = 25°C$, for varying stressing currents (a) and varying device widths (b).

### 4.1.4 Time Evolution of $\Delta V_T$

The time evolution of the change in $V_T$ under various conditions was examined. For this analysis, we focused on the first hour of stressing (where most of the changes occurred, before beginning to saturate). We also ignored the first data point, as the changes between $t = 0$ and $t = 2$ min usually involve what appears to be fast transient behavior of a different nature. We looked at data from the experiments performed in Fig. 4-7. Several models were attempted to fit the data, but a model containing an exponential of the form $e^{-t/\tau}$ fit the data best for all temperatures. These fits are shown in Fig. 4-9.

From each of these fits, a rate constant $\tau$ is extracted, which gives an indication of the rate of change of $V_T$. These value are summarized in Table 4.2, which shows the rate constant $\tau$ for each case, in addition to the estimated value of $T_{ch}$. These values are then used to create an plot of $1/\tau$ (degradation rate) vs. $1/T_{ch}$, as shown in Fig. 4-10. As one can see, the change in $V_T$ has an Arrhenius dependence with temperature, with an activation energy of $E_a = 0.42 \pm 0.09$ eV. This represents the energy required to de-trap the trapped electrons under the particular stressing conditions ($V_{DGo} + V_T = 6.0$ eV). This value is a bit different from activation energies found elsewhere (in [12], an activation energy for 0.21 eV for $\Delta V_T$ is reported). However, it is difficult to make a comparison with [12] as in that case $\Delta V_T$ was purely thermally activated and thus likely

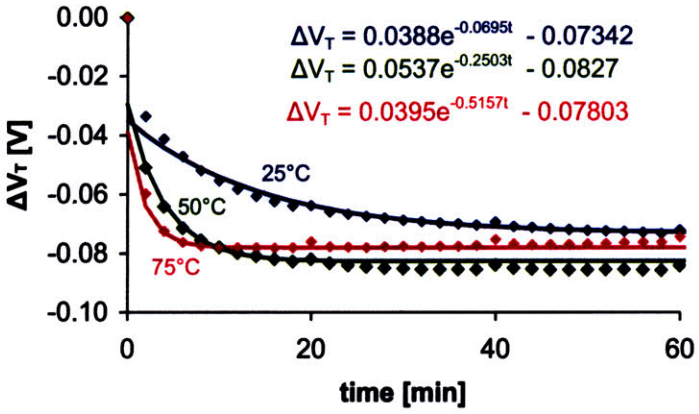



Figure 4-9: Time evolution of $\Delta V_T$, for constant $I_D$ and constant $V_{DGo}+V_T$ experiments performed on standard-parameter PHEMTs at $T_{amb}$ = 25, 50, and 75°C in nitrogen. Data is shown along with exponential fits. $W_g = 100\mu$m.

due a slightly different mechanism. Also, it is expected that the activation energy we extracted for $\Delta V_T$ will decrease with increasing electric field, due to increased tunneling.

Also, it is important to mention that since $\Delta V_T$ involves the de-trapping of electrons, the change in $V_T$ during stressing will eventually saturate once all the traps under the gate have been completely emptied out. This is typically observed under high drain-gate electric fields after long enough periods of time. This is illustrated in Fig. 4-1 for the $L_{rd} = 0.3\mu$m device. As one can see, after about 100 minutes of stressing, this device exhibits no further decrease in $V_T$, despite increases in bias. This indicates that there are no electrons under the gate left to be de-trapped. On the other hand, the other three devices (which have longer $L_{rd}$ and thus lower peak electric-fields) continue to experience a decrease in $V_T$ with increasing bias, since not all the electrons have been de-trapped yet.

| $T_{amb}$ [°C] | $P_{diss}$ [W] | $\Delta T$ [°C] | $T_{ch}$ [°C] | $\tau$ [min] | $1/\tau$ [sec$^{-1}$] |
|---|---|---|---|---|---|
| 25 | 0.294 | 99.2 | 124.2 | 13.79 | 1.23E-03 |
| 50 | 0.298 | 111.9 | 161.9 | 4.00 | 4.17E-03 |
| 75 | 0.301 | 124.8 | 199.8 | 1.94 | 8.60E-03 |

Table 4.2: Time constants obtained for $V_T$ change in stressing experiments done at $T_{amb}$= 25, 50, 75°C in nitrogen. $W_g = 100\mu$m.

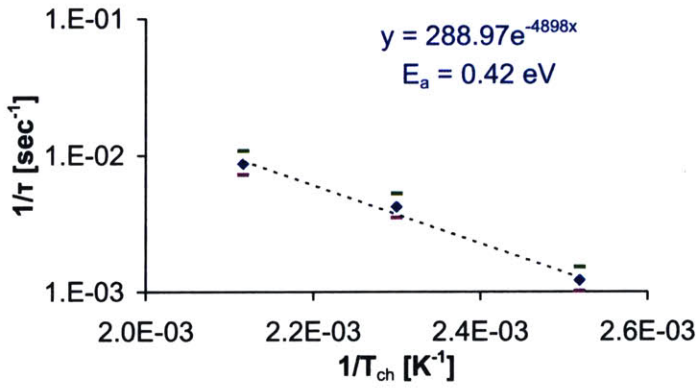



Figure 4-10: Semi-log plot of $1/\tau$ versus $1/T_{ch}$, using time constant ($\tau$) values for $V_T$ change during constant $I_D$ and constant $V_{DGo} + V_T$ stressing experiments performed at $T_{amb}$ = 25, 50, and 75°C. Shown with exponential fit to data and extracted activation energy. Error bars (assuming 20% uncertainty in $\tau$) indicated by magenta and green lines. $W_g = 100\mu$m.

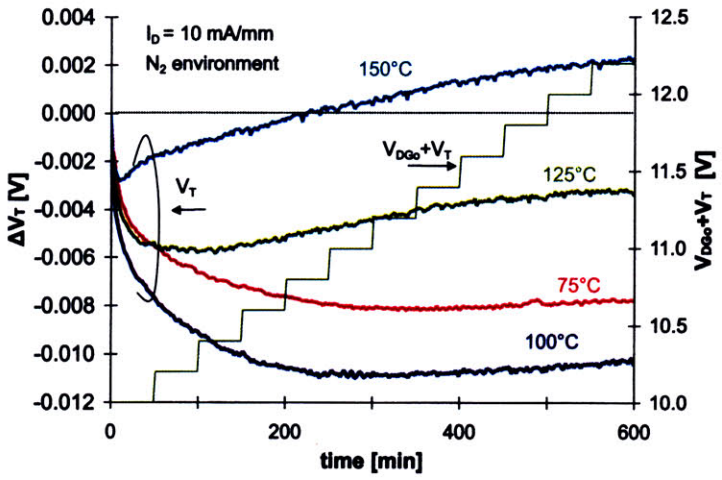



Figure 4-11: Time evolution of $\Delta V_T$ off-state step-stressing experiments performed at 75, 100, 125, and 150°C in nitrogen. $W_g = 100\mu$m.

### 4.1.5 Off-state Stressing

So far, the experiments and analyses investigating $\Delta V_T$ have involved the behavior of $V_T$ during on-state stressing. However, changes in $V_T$ were also observed in our off-state stressing experiments. Fig. 4-11 illustrates the time evolution of $\Delta V_T$ for a series of off-state stressing experiments performed at various ambient temperatures, in a nitrogen environment. As one can see, negative shifts in $V_T$ are observed here as well, indicating that the electron de-trapping can occur without significant drain current, as long as the electric field is high enough.

From this data, one can note that for low temperatures (below 100°C), the negative shift in $V_T$ increases with increasing temperature. This is the same as what is observed in on-state stressing and is consistent with thermally-activated de-trapping, as discussed in Sec. 4.1.3. However, one can see that for temperatures above 100°C, increasing the temperature actually reduces the negative $V_T$ shift, eventually causing the change in $V_T$ to become positive ($T = 150$°C). This suggests that at high ambient temperatures, a separate mechanism causing a *positive* shift in $V_T$ dominates over the electron de-trapping mechanism causing the negative $V_T$ shift. The nature of this separate mechanism will be discussed further in Sec. 4.1.7.

### 4.1.6 Hydrogen Experiments

As mentioned in Sec. 1.3.2, other HEMT reliability studies have demonstrated shifts in threshold voltages due to hydrogen degradation [10,20,48] . We needed to know if such effects were present in our devices, so that we could separate any such effects from those due to electrical stressing alone. Thus we performed hydrogen exposure experiments, similar those done in [10,48].

Our basic hydrogen experiments consist of three steps. The first step is to pre-bake the device in nitrogen, in order to exhaust any changes in device parameters due to thermal effects. Then the second step is a "thermal stability check," in which the device is stored at 200°C in nitrogen for 2.5 hours. Here device parameters are measured in-situ, and before proceeding to the next step it is confirmed that there are no significant changes due to thermal drift. The third and final step is the actual hydrogen exposure, in which the device is again stored at 200°C for 2.5 hours, but with forming gas ($95\%N_2, 5\%H_2$) now flowing in the probe station chamber. During this step the device continues to be monitored, thus allowing a comparison of device behavior of "before" and "during" exposure to hydrogen.

Although our experiments here consist of only three steps, in general, hydrogen experiments employ a fourth step of similar conditions to the first or second step (high-temperature storage in $N_2$) to see if any changes incurred during the hydrogen exposure can be recovered by annealing. However, as will be discussed below, we ended up not observing any changes during the hydrogen exposure, so there was no reason to do an additional step to check for recovery.

From our initial testing, we found that a pre-baking temperature of 230°C was adequate to saturate changes from thermal effects in a reasonable time frame (~30 hours). Although at this temperature we could not do in-situ characterization (the maximum chuck temperature for our probe station was 200°C), the device was removed from the oven at various intervals in order to be characterized. From this we found that $V_T$ was the main parameter that showed significant changes due to thermal storage. Fig. 4-12 shows the time evolution of $V_T$ of one device during this prebake step. The characterizations were all done at 200°C.

As one can see, with storage at 230°C, initally $V_T$ increases rapidly, but after ~30 hours, the change in $V_T$ has significantly slowed down. As for the mechanism behind this change in

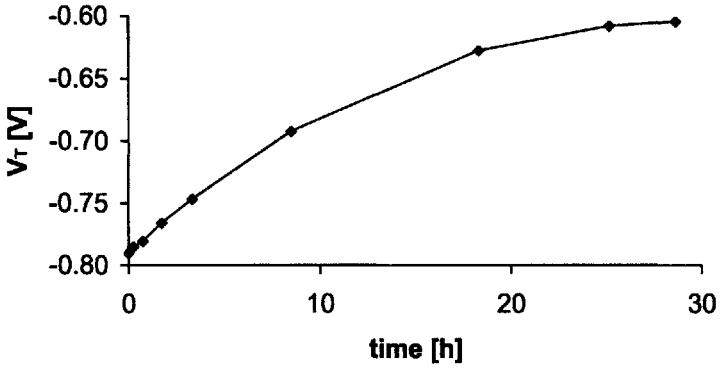



Figure 4-12: Time evolution of $V_T$ during 230°C storage in $N_2$ (measurements taken at 200°C). $W_g = 100\mu$m.

$V_T$, previous studies have attributed the positive $V_T$ shift observed under high temperatures to gate-sinking [18]. Since this mechanisms is driven by diffusion, this mechanisms has a $t^{1/2}$ dependence [15]. Fig. 4-13 shows a log-lot plot of the change in $V_T$ versus time, along with a best power fit (of the form $t^n$), and a square root fit (a power fit where $n = 0.5$). Looking at the data along with the best power fit (dashed blue line), it appears that the change in $V_T$ tends to follow a power law, where $n$ is about 0.8. A square root fit (magenta line) can also be attempted to fit the data, but does not fit so well to the early data points ($t < 5$ hours). Despite this discrepancy, however, it is still highly likely that the $V_T$ shift here is due to gate sinking; even though the extent of gate metal interdiffusion may be strictly following a $t^{1/2}$ dependence, the change in $V_T$ can have a slightly more complex dependence.

From this data we then assumed that $N_2$ storage for 230°C for 30 hours was enough to minimize further thermal changes on these devices at lower temperatures. These same conditions were then used for the pre-bake step in our subsequent hydrogen degradation experiments. A complete summary of the conditions from our hydrogen experiments is shown in Table 4.3.

We performed a full experiment of this type on a new device of the same type. The prebake steps was performed (causing $V_T$ to shift by +0.15 V) and then in the prober, steps 2 and 3 of the experiments were carried out. Fig. 4-14 shows the time evolution of $V_T$ during these steps.

As one can see, $V_T$ remains virtually unchanged during the thermal stability check step, thus

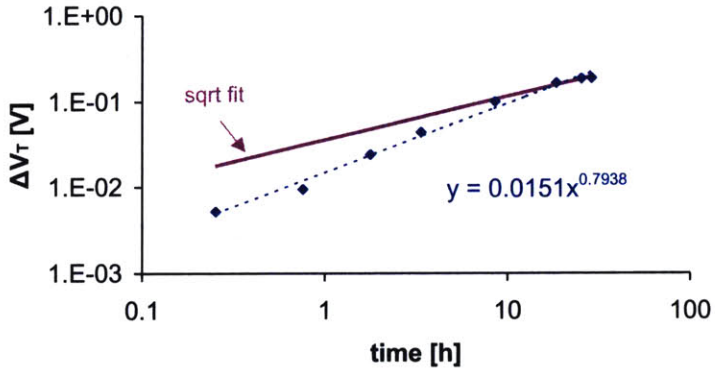



Figure 4-13: Log-log plot of time evolution of $\Delta V_T$ during 230°C storage in $N_2$ (measurements taken at 200°C), with best power fit (dashed dark blue line) and $(\text{time})^{1/2}$ fit (magenta). $W_g = 100\mu$m.

| Step | Description | Temp [°C] | Env | Location | Time [hr] |
|---|---|---|---|---|---|
| 1 | Prebake | 230 | $N_2$ | oven | 30 |
| 2 | Thermal Stability Check | 200 | $N_2$ | prober | 2.5 |
| 3 | Hydrogen Exposure | 200 | $5\%H_2$ | prober | 2.5 |

Table 4.3: Outline of Steps for Hydrogen Degradation Experiments.

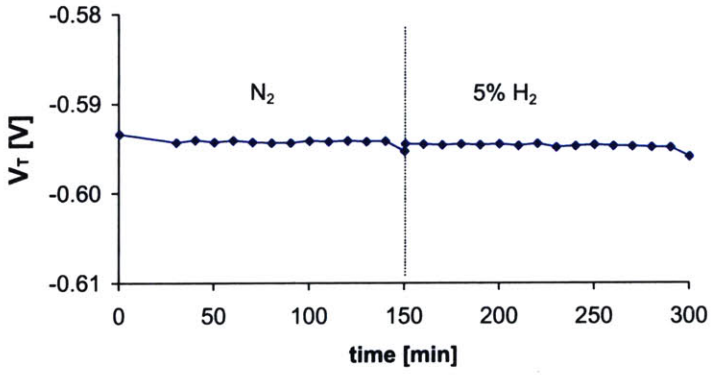



Figure 4-14: Time evolution of $V_T$ during steps (2) and (3) of hydrogen degradation experiment. $T = 200$°C. $W_g = 100\mu$m.

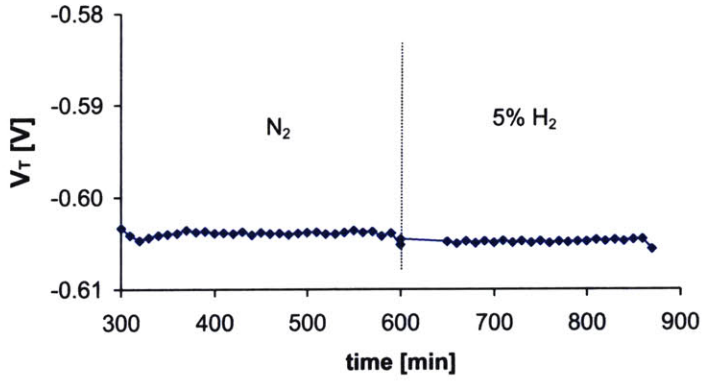



Figure 4-15: Time evolution of $V_T$ during additional steps of hydrogen degradation experiment. $T = 200°C$.

confirming that thermal effects have largely saturated. Upon subsequent $H_2$ exposure, $V_T$ still does not change appreciably. But before assuming that hydrogen has no effect on these devices, we first decided to prolong hydrogen exposure. So on the same device, we repeated steps (2) and (3), for an extended period of time. At 200°C, we stored the device in $N_2$ for 5 hours, and then in forming gas for another 4.5 hours. Fig. 4-15 shows the time evolution of $V_T$ during these additional steps to the experiment. One can notice that the initial $V_T$ of the additional degradation steps is not exactly the same as the final $V_T$ of the first degradation steps (as shown in Fig. 4-14). However, this difference is very small (~7 mV), and is likely because the additional degradation steps were not started immediately after the first degradation steps (the device was first brought down to room temperature and stored for a few hours before resuming degradation).

At this point, since the device has undergone a total of 7 hours of hydrogen exposure at 200°C without any observable changes, we assume that hydrogen degradation is not of serious concern for these particular devices, at least under the conditions we employ in our stressing experiments. However, as previous studies have shown that hydrogen effects tend to vary with gate orientation [48], it could be possible that devices like these but with different gate orientation would experience some effects due to hydrogen exposure. Also, it is possible that at higher temperatures (> 200°C) the devices would begin to experience some effects from the hydrogen, but due to limitations with

our setup, such experiments were not possible.

### 4.1.7 Discussion

In the previous section, although no hydrogen-induced $V_T$ shifts were observed, a positive shift in $V_T$ is observed under high-temperature storage, which we attributed to gate sinking, a previously identified mechanism [18]. This mechanism could explain the behavior of $V_T$ in our off-state stressing experiments performed at high temperatures. Since gate sinking is a thermally-activated mechanism [11], at high enough temperatures, the gate sinking mechanism dominates over the de-trapping mechanism, eventually making the shift in $V_T$ more positive with increasing temperature.

That being said, in the majority of our electrical stressing experiments, lower ambient temperatures are employed, resulting in a negative shift in $V_T$. Since this effect is more prominent and the underlying mechanism was less clear, we focused on investigating the negative shift in $V_T$ and uncovering the mechanism responsible.

From our initial studies, we observed the negative shift in $V_T$ to be largely recoverable with unbiased storage at room temperature. This points to charge modulation underneath the gate, namely electron de-trapping, as described in [21]. Though some have attributed this phenomena to hot holes generated from impact-ionization neutralizing trapped electrons under the gate [21], from our experiments discussed in Sec. 4.1.1, it appears that $\Delta V_T$ is actually not correlated with impact ionization. Instead, $\Delta V_T$ seems to have a significant correlation with the peak electric field in the drain-gate region. This suggests that the de-trapping mechanism involves field-assisted tunneling of the electrons out of the traps, as mentioned in [46]. The de-trapping can be thermally activated [21], which explains how $\Delta V_T$ is accelerated with increasing temperature. This mechanism is illustrated in Fig. 4-16.

The fact that $\Delta V_T$ is driven by the electric field instead of impact ionization has profound implications on the behavior of $V_T$ during various stressing conditions. For instance, this means that negative shifts in $V_T$ can still occur under conditions with relatively low levels of impact-ionization but with high electric fields (e.g. off-state stressing). This was demonstrated in our off-state stressing experiments, where significant negative shifts in $V_T$ were observed during stressing. Typically in

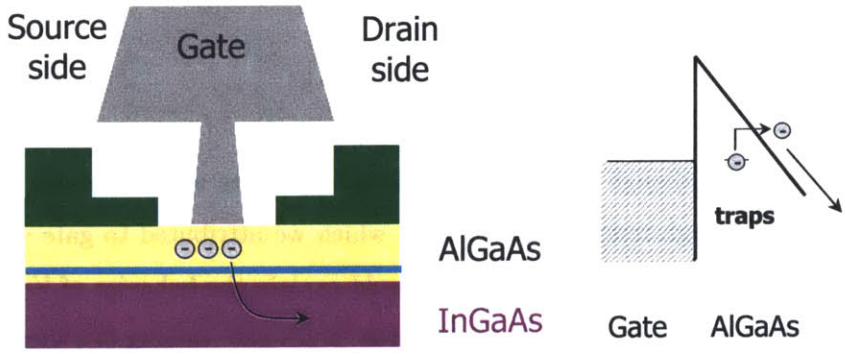



Figure 4-16: Spatial diagram (a) and energy band diagram (b) illustrating electron de-trapping mechanism causing negative shift in $V_T$.

off-state experiments $V_T$ shifts by ~10-20 mV, compared to the ~100 mV changes observed under on-state stressing. This discrepancy may be due to differences in channel temperature (typically on-state temperatures are must hotter). However, these changes are still large enough to have significant effects on $I_{Dss}$ and $I_{max}$.

## 4.2 Decrease in $R_S$

As shown in Sec. 3.1.1, a permanent decrease in $R_S$ is typically observed in our devices upon electrical stressing. While a recoverable decrease in $R_S$ has been reported [21], a *permanent* decrease in $R_S$ has not. The fact that this change is not recoverable with room-temperature unbiased storage seems to rule out a trapping effects, which is the suggested mechanism behind the temporary change in $R_S$ [21].

Our previous stressing experiments on various types of TLMs allowed us to clearly identify a permanent increase in sheet carrier concentration, $n_s$, present in the first stages of stressing [23]. Since this increase was found to occur mostly on the source side, this correlated very will with the decrease in $R_S$ observed in the PHEMTs. However, aside from this, there was not much else that could be said about the actual physical mechanism behind the decrease of $R_S$. Some

of the aspects of the $R_S$ degradation seemed to contradict each other, or were otherwise quite puzzling. The experiments investigating the effect of $L_{rs}$ (source-gate gap) suggested a surface-related mechanism, but then separate experiments showed that the $R_S$ was the same in both air and in nitrogen, ruling out any surface oxidation effects. The experiments investigating the effect of $L_{rd}$ (drain-gate gap) on $\Delta R_S$ seemed to show a negative dependence on impact-ionization, but then separate experiments showed that the degradation was accelerated with higher bias currents. So in order to clarify this picture and determine the nature of the mechanism behind the $R_S$ change, additional experiments and further analyses were necessary.

### 4.2.1 Effect of $L_{rd}$

First we will re-examine the effect of $L_{rd}$ on device degradation. Fig. 4-17 shows the change in $R_S$ for four different devices of varying $L_{rd}$ during a set of a identical stressing experiments at constant $I_D$ and constant $V_{DGo} + V_T$. From this graph one can clearly see that the two devices with longer $L_{rd}$ ($L_{rd} = 0.7$ and $0.9\mu$m) exhibit a faster decrease in $R_S$. Initially this behavior was puzzling, as it was assumed that devices with longer $L_{rd}$ should have less degradation, as the peak electric field was smaller for a given bias. But as discussed in Sec. 4.1.1, it was later found that the devices with longer $L_{rd}$ actually exhibited oscillation problems that caused them to have higher levels of impact-ionization than those with shorter $L_{rd}$. Therefore, the decrease of $R_S$ could actually be correlated with impact ionization after all. To look further into this, the magnitude of the gate current during these experiments was examined.

Fig. 4-18(a) plots the $R_S$ decrease at various time points, versus the average value of $|I_G|$ during the initial stages of stressing. As one can see, the decrease in $R_S$ does seem to have a roughly linear correlation with $|I_G|$, suggesting that $\Delta R_S$ is indeed correlated with impact-ionization. Fig. 4-18(b) shows the decrease in $R_S$ for those same points, but plotted versus the inverse of $L_{rd}$. Here there is clearly not a positive correlation between $\Delta R_S$ and $1/L_{rd}$. This thus suggests that change in $R_S$ is driven by impact-ionization more than the electric field.

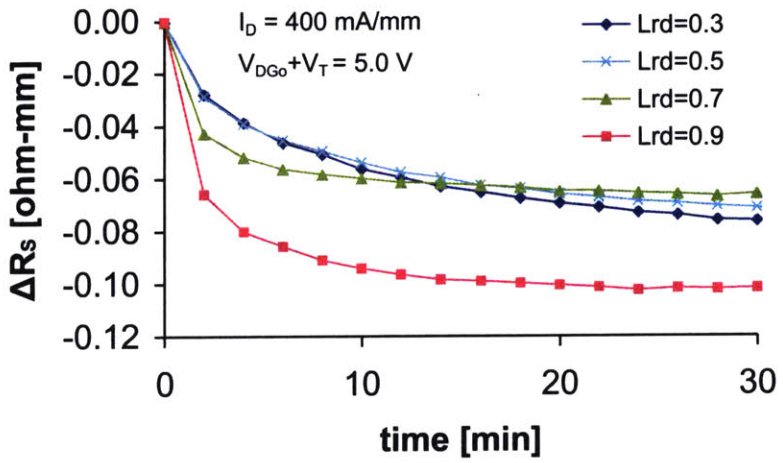



Figure 4-17: Time evolution of $\Delta R_S$, for set of stressing experiments employing constant $I_D$ = 400 mA/mm and constant $V_{DGo} + V_T = 5.0$ V, at $T_{amb} = 25°$ in air. $W_g = 160\mu$m.

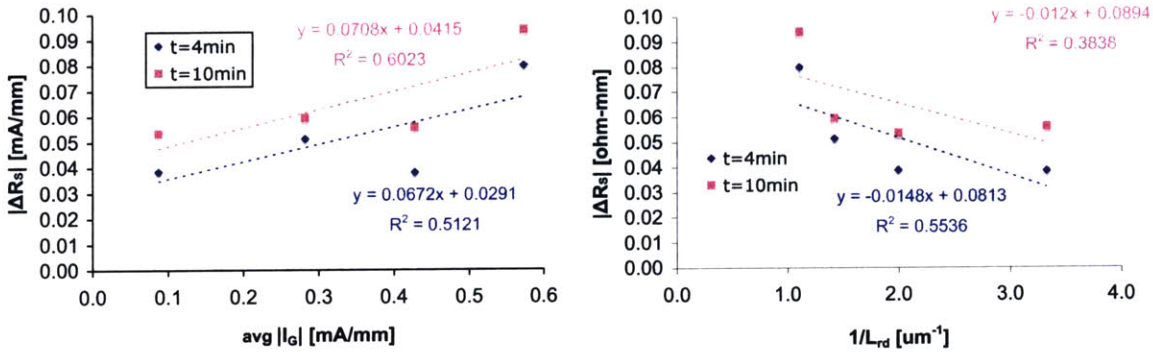



Figure 4-18: Absolute value of change in $R_S$ after $t = 4, 10$ minutes of stressing versus average gate current (a) and versus $1/L_{rd}$ (b) for stressing experiments employing constant $I_D = 400$ mA/mm and constant $V_{DGo}+V_T = 5.0$ V, at 25°C in air, on devices with different values of $L_{rd}$. $W_g = 160\mu$m.

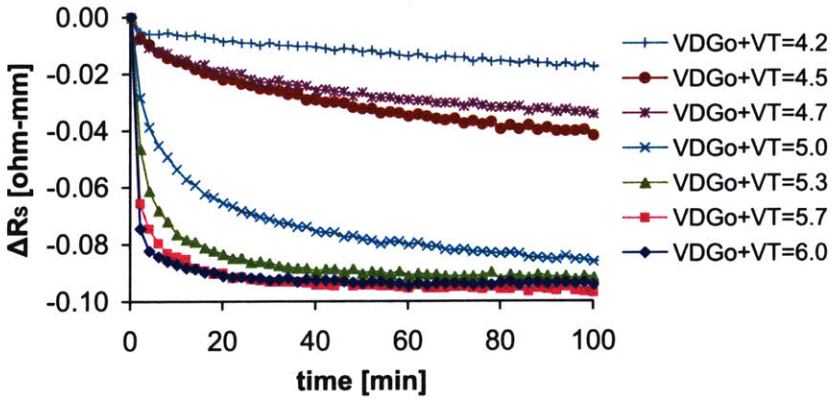



Figure 4-19: Time evolution of $\Delta R_S$, for set of stressing experiments employing constant $I_D$ = 400 mA/mm and constant $V_{DGo} + V_T$, at $T_{amb} = 25°$ in air. $W_g = 160\mu$m.

### 4.2.2 Effect of Electric Field

The set of stressing experiments employing different $V_{DGo}+V_T$ (described in Sec. 4.1.2) was also used to examine the decrease in $R_S$ as a function of electric field. If $\Delta R_S$ is driven by impact-ionization, we expect that it should have an exponential dependence on $V_{DGo} + V_T$. We first look at the time evolution of $\Delta R_S$ for these different experiments. This is shown in Fig. 4-19. One can clearly see that increasing $V_{DGo}+V_T$ accelerates the decrease in $R_S$. However, unlike with $\Delta V_T$, the dependence of $\Delta R_S$ on $V_{DGo} + V_T$ seems highly non-linear. Starting at $V_{DGo} + V_T = 4.2$ V, the degradation increases dramatically with small increments of $V_{DGo} + V_T$, but then around $V_{DGo} + V_T = 5.3$ V the change quickly saturates, despite increasing the bias up to 6.0 V.

To get a better picture of this non-linear dependence on bias, the change in $R_S$ at given time points (after 10 and 30 minutes of stressing) is plotted versus $V_{DGo}+V_T$. This is shown in Fig. 4-20. This clearly shows the "saturation" of $\Delta R_S$ at higher biases (especially after 30 minutes). But even if one just looks at the data points at lower biases, the behavior still doesn't seem quite linear. Since the previous section suggested $\Delta R_S$ was related to impact-ionization, then that should result in an exponential relationship with $1/(V_{DGo} + V_T)$. Fig. 4-21 shows the change in $R_S$ at selected time points versus the *inverse* of $V_{DGo} + V_T$. For this plot, the two highest bias points are omitted, as to remove the effect of the "saturation" of the degradation. From this graph, one can see that

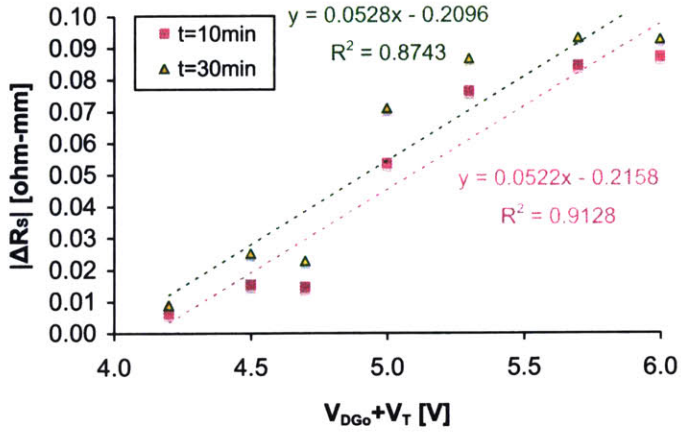



Figure 4-20: Absolute value of change in $R_S$ after $t = 10, 30$ minutes of stressing versus $V_{DGo} + V_T$, for set of stressing experiments employing constant $I_D = 400$ mA/mm and constant $V_{DGo} + V_T$, performed at $T_{amb} = 25°$ in air. $W_g = 160\mu$m.

the data fit reasonably well to the exponential fits, thus further supporting the idea that impact ionization is what is driving $\Delta R_S$, and not so much electric field.

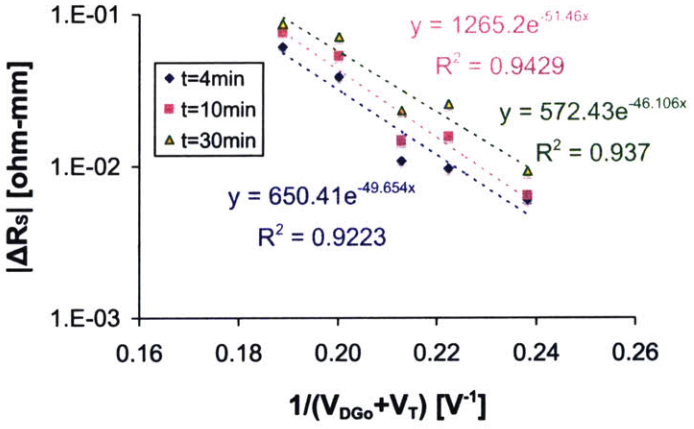



Figure 4-21: Absolute value of change in $R_S$ after $t = 4, 10, 30$ minutes of stressing versus $1/(V_{DGo}+V_T)$, for set of stressing experiments employing constant $I_D = 400$ mA/mm and constant $V_{DGo}+V_T$, performed at $T_{amb} = 25°$ in air. $W_g = 160\mu$m.

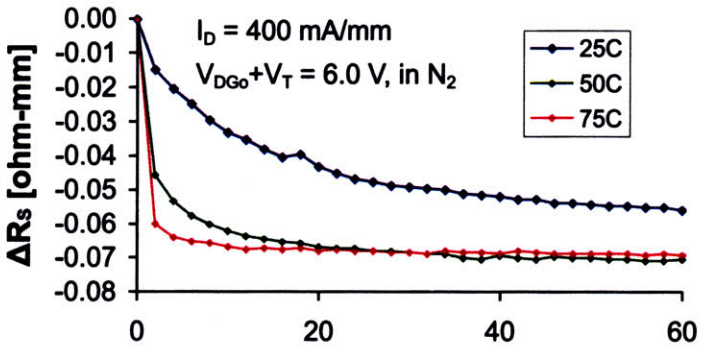



Figure 4-22: Time evolution of $\Delta R_S$, for constant $I_D$ and constant $V_{DGo}+V_T$ experiments performed on standard-parameter PHEMTs at 25, 50, 75°C in nitrogen. $W_g = 100\mu$m.

### 4.2.3 Effect of Temperature

To explore the temperature dependence of $\Delta R_S$, the time evolution of$R_S$ in the stressing experiments performed at various ambient temperatures (described in Sec. 4.1.3) were examined. Fig. 4-22 shows the time evolution of $\Delta R_S$ for these experiments. This clearly shows that the decrease in $R_S$ is accelerated with increasing temperature.

So although the decrease in $R_S$ seems to be driven by impact-ionization, it has an overall positive temperature dependence. This suggests that mechanism behind $\Delta R_S$ must also involve another physical process that has a positive dependence on temperature. The temperature dependence will be further examined in the next section, where an activation energy for the change in $R_S$ is extracted.

### 4.2.4 Time Evolution of $\Delta R_S$

The time evolution of the change in $R_S$ under various conditions was further examined, in order to obtain a mathematical model for the behavior. As done in the analysis of $\Delta V_T$ in Sec. 4.1.4, we focused on the first hour of stressing, where most of the changes occurred, and ignored the first data point. We looked at data from the experiments performed in Fig. 4-22. Like with $\Delta V_T$, a model containing an exponential of the form $e^{-t/\tau}$ fit the data best for all temperatures. These fits are shown in Fig. 4-23.

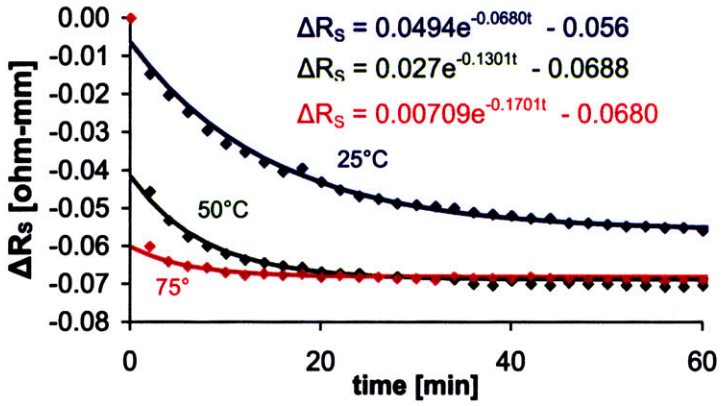



Figure 4-23: Time evolution of $\Delta R_S$, for constant $I_D$ and constant $V_{DGo}+V_T$ experiments performed on standard-parameter PHEMTs at 25, 50, 75°C in nitrogen. Data is shown along with exponential fits. $W_g = 100\mu$m.

| $T_{amb}$ [°C] | $P_{diss}$ [W] | $\Delta T$ [°C] | $T_{ch}$ [°C] | $\tau$ [min] | $1/\tau$ [sec$^{-1}$] |
|---|---|---|---|---|---|
| 25 | 0.294 | 99.2 | 124.2 | 14.71 | 1.13E-03 |
| 50 | 0.298 | 111.9 | 161.9 | 7.69 | 2.16E-03 |
| 75 | 0.301 | 124.8 | 199.8 | 5.88 | 2.84E-03 |

Table 4.4: Time constants obtained for $R_S$ change in stressing experiments done at $T_{amb}$= 25, 50, 75°C in nitrogen. $W_g = 100\mu$m.

From each of these fits, a rate constant $\tau$ is extracted, which gives an indication of the rate of change of $V_T$. These value are summarized in Table 4.4, which shows the rate constant $\tau$ for each case, in addition to the estimated value of $T_{ch}$. These values are then used to create an plot of $1/\tau$ (degradation rate) vs. $1/T_{ch}$, as shown in Fig. 4-24. As one can see, the change in $R_S$ has an Arrhenius dependence with temperature, with an activation energy of $E_a = 0.19 \pm 0.09$ eV.

### 4.2.5 Discussion

From all of our various experiments and analyses, we have been able to make a number of observations about the decrease in $R_S$. Our early experiments showed that it was independent of the environment and that it was not recoverable with unbiased storage at room temperature. Experiments investigating the effect of $L_{rd}$ suggested that $\Delta R_S$ is closely related to impact-ionization

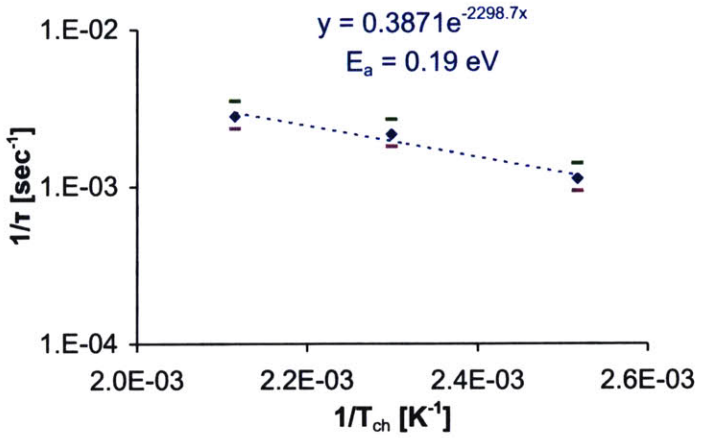



Figure 4-24: Semi-log plot of $1/\tau$ versus $1/T_{ch}$, using time constant ($\tau$) values for $R_S$ change during constant $I_D$ and constant $V_{DGo} + V_T$ stressing experiments performed at $T_{amb}$ = 25, 50, and 75°C. Shown with exponential fit to data and extracted activation energy. Error bars (assuming 20% uncertainty in measurement of $\tau$) indicated by magenta and green lines. $W_g = 100\mu$m.

more than with the drain-gate electric field. This is consistent with the fact the decrease in $R_S$ was not observed at all under off-state stressing conditions; even under very high electric field, if there is no impact-ionization, there is no decrease in $R_S$.

However, there seems to be another physical process involved, since $\Delta R_S$ is accelerated with temperature ($E_a$ = 0.19 eV), and we know that impact-ionization has a *negative* temperature dependence. Also, what's unique about the $R_S$ degradation is that it saturates, both with voltage and with time. These observations are consistent with the mechanism of recombination-enhanced defect annealing, as described in [49]. In this process, electron-hole recombination gives off energy to defects, which enables them to get annealed out. The annealing rate of this process in GaAs diodes was found to be $E_a$ = 0.34 eV [49], which is not very different from the activation energy we found for the decrease of $R_S$, especially considering the error of ±0.09 eV. The difference can be also possibly accounted for by the fact that impact-ionization has a negative temperature dependence which would reduce the $E_a$ that is extracted. So this defect-annealing process could be what is happening on the source side, where recombination is occurring as a result of impact-ionization on the drain side. As the defects get annealed out, the sheet carrier concentration $n_s$ on the source

increases, thus decreasing $R_S$. Once all the defects are annealed, $n_s$ stops increasing, thus causing $\Delta R_S$ to eventually saturate. Since carrier recombination is required for this annealing, this can explain the strong correlation of $\Delta R_S$ with impact-ionization; the decrease in $R_S$ will only be observed if there is impact-ionzation present to cause electron-hole recombination.

## 4.3 Summary

In this chapter, we have presented the results of systematic electrical stressing experiments performed in order to uncover the mechanisms behind the negative shift in $V_T$ and the decrease in $R_S$ observed during electrical stressing. Although these forms of "degradation" seem to improve device characteristics and are thus less worrying than the degradation of $R_D$ and $I_{max}$, since they do induce some significant changes during electrical stressing it is important to acknowledge their effects and understand the underlying mechanisms.

From our early experiments, it was known that the negative shift in $V_T$ is recoverable with room-temperature unbiased storage, which suggested a mechanism involving some de-trapping of electron under the gate. Initially, this was attributed to hot holes generated from impact-ionization neutralizing the trapped electrons. However, later experiments investigating the effect of $L_{rd}$ and $V_{DGo} + V_T$ allowed us to determine that the negative shift in $V_T$ is actually correlated with the drain-gate electric field, and not impact ionization as previously thought. This allowed us to identify the de-trapping mechanism as field-assisted tunneling of the electrons out of the traps. Under bias stress, this de-trapping can be thermally activated, with an activation energy of $E_a = 0.42$ eV.

In contrast to the shift in $V_T$, the decrease in $R_S$ was not recoverable, which ruled out a similar de-trapping mechanism on the source side. From experiments investigating $L_{rd}$ and $V_{DGo} + V_T$, it was found that the change in $R_S$ was more correlated with impact-ionization that electric field. Also, it was noted the $\Delta R_S$ tend to "saturate" with high bias. Analysis of the temperature dependence gave an activation energy of $E_a = 0.19$ eV. All these findings are consistent with a mechanism of recombination-enhanced defect annealing on the source side. Under electrical stressing, the recombination on the source side produced by impact-ionization gives energy to local

defects, causing them to be annealed out. This in turn results in a higher carrier concentration $n_s$ on the source side, thereby reducing $R_S$.

The following chapter will discuss our experiments performed to observe light-emission from the PHEMTs during stressing. In this study it will be shown that there is significant recombination occurring on the source side of the device, strengthening the theory of recombination-induced defect annealing behind $\Delta R_S$.

# Chapter 5

# Non-Uniformities in Degradation

In [23], light-emission experiments were performed on TLM structures, which allowed us to obtain spatial pictures of the light emitted from the TLM as it was being stressed. These experiments showed that the distribution of light emission along the width was very non-uniform: initially, it was very heavily concentrated in the center, but with stressing it spread out and eventually concentrated towards the edges. So we decided to perform analogous light-emission experiments on the PHEMTs to see if they exhibited similar behavior.

## 5.1 Introduction

As mentioned in the previous section, the degradation of $R_D$ and $I_{max}$ was mainly attributed to moisture-induced corrosion of the surface on the drain side, which is accelerated by high electric fields. We know that under these high-electric fields, impact ionization tends to occur (as shown in previous chapter). The presence of impact ionization leads to the recombination of electrons and holes, which then results in emission of photons. This is illustrated in Fig. 5-1, containing a schematic of the PHEMT cross-section. Under high bias stressing, due to the high electric field in the drain-gate region, impact ionization occurs on the drain side, resulting in the creation of both electrons (shown as blue circles) and holes (white circles). The carriers recombine on both the source and the drain side, thus giving off light. So, if we can somehow capture a picture of the

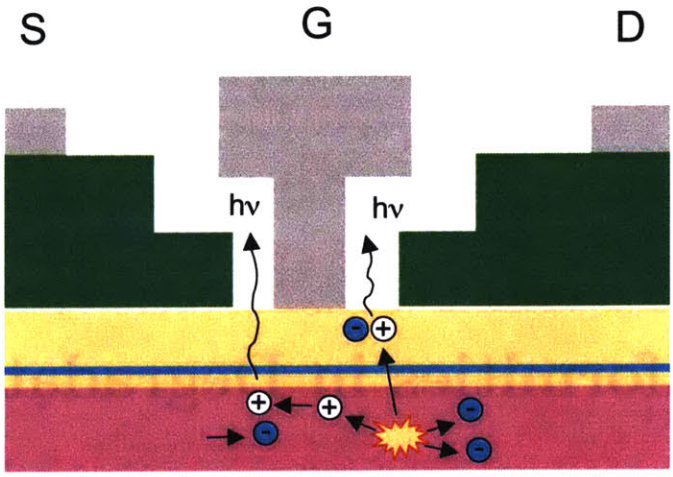



Figure 5-1: Cartoon illustration of impact ionization and consequent light-emission occurring in a PHEMT under high bias.

light emission of the device, we can thus get a picture of the distribution of impact ionization and of the electric field.

## 5.2 Experimental

In this study we took pictures of light emitted from the PHEMTs using a special setup created by Professor Mark Somerville at Olin College. This setup, which is pictured in Fig. 5-2 consists of a Cascade probe station equipped with an astronomical-grade CCD sensor. This setup allowed us to take light-emission photographs of a device while it was being electrically stressed. Due to limitations in this particular setup, for these stressing experiments we could not keep $V_{DGo} + V_T$ constant. So instead, we implemented a stressing scheme that kept $V_{GS}$ and $V_{DS}$ constant. And, to speed up degradation, we stepped $V_{DS}$ in regular intervals. This is illustrated in Fig. 5-3, which shows the bias stressing $V_{DS}$ as a function of time, for a typical experiment on a standard-parameter PHEMT. Here, $V_{GS}$ was kept constant at 0.3 V, and $V_{DS}$ was initially set at 6.6 V and increased by 0.2 V every 100 minutes. Photographs were taken at frequent intervals throughout the stressing

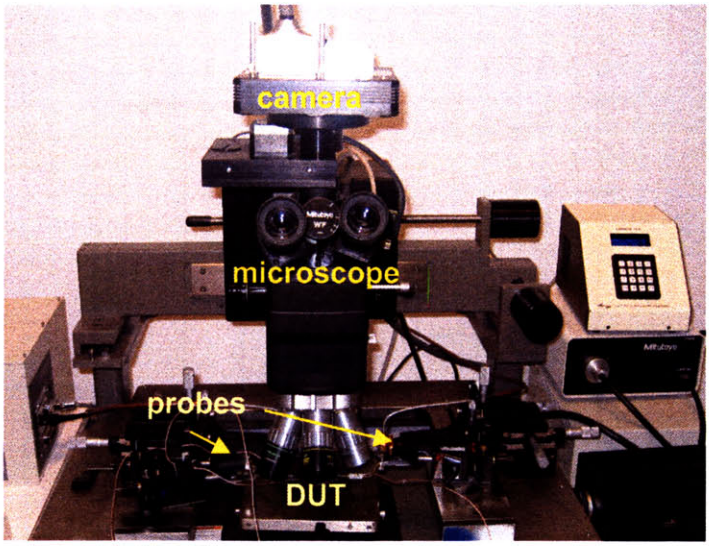



Figure 5-2: Photograph of light-emission setup in Professor Mark Somerville's laboratory at Olin College, used to measure light-emission of PHEMTs during stressing.

experiment (at least every 10 minutes) and also after each bias-stepping, where the bias $V_{DS}$ was momentarily returned to the initial biasing condition ($V_{DS} = 6.6$ V).

## 5.3 Light Emission During Step-Stressing

From every picture taken, we obtained the total light emission intensity (sum of all pixel values in the image, normalized to the exposure time). To account for the change in the drain current with stressing (from the downward shift in $V_T$), we normalized the total light intensity to the drain current. The blue data of Fig. 5-4 shows the total light emission (normalized to $I_D$) as a function of stressing time (each data point corresponds to data from one picture).

From this graph, one can see that in the initial stages of stressing, the intensity of the emitted light remains more or less constant for a given $V_{DS}$. However, with prolonged stressing (t > 500 min), the intensity tends to decrease with constant-VDS stressing. The light intensity also increases as $V_{DS}$ is increased (as expected, since there is more impact ionization). Fig. 5-5 shows the time evolution of the drain current $I_D$. As one can see, in the first half of the experiment,

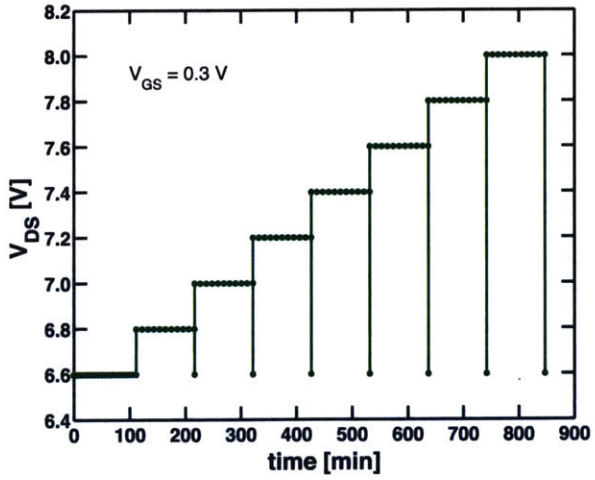



Figure 5-3: Applied stressing voltage $V_{DS}$ vs. stressing time for a typical light-emission experiment on a PHEMT. Each dot represents a point in time when a light-emission picture was taken. Throughout the experiment, $V_{GS}$ is held constant at 0.3 V.

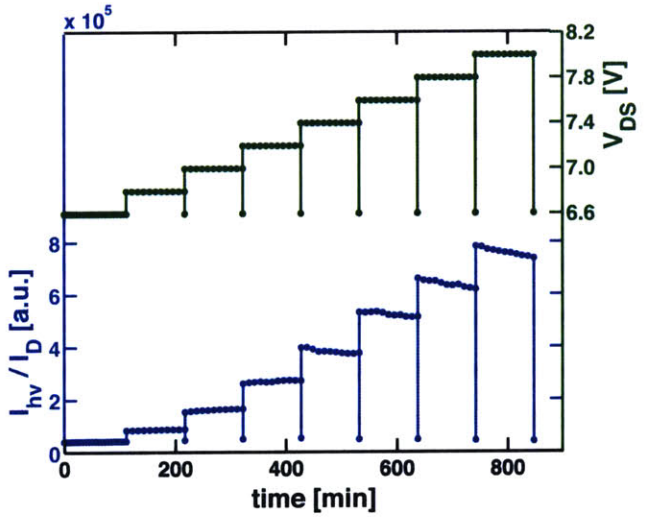



Figure 5-4: Applied stressing voltage (green) and total light emission intensity normalized to drain current (blue) vs. stressing time for light-emission experiment on a standard-parameter single-gate finger PHEMT ($W_g = 50\mu$m). $V_{GS} = 0.3$ V.

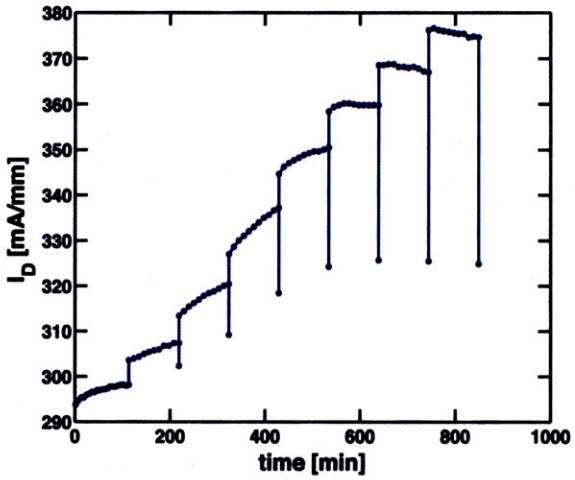



Figure 5-5: Drain current $I_D$ vs. stressing time for light emission experiment on a standard-parameter PHEMT.

$I_D$ increases even for a constant $V_{DS}$. As mentioned earlier, we can attribute this to the negative shift in $V_T$ that is typically observed during the initial stages of high-$V_{DS}$ stressing.

Over 100 photographs are typically taken during a light-emission experiment; a few of them will be shown next. For each of these pictures, the light-emission picture was superimposed with the device picture (which showed the source and drain contacts). Here, the source side is on the left, and the drain side on the right. The pictures taken at a fixed bias of $V_{DS} = 6.6$ V are examined first. Fig. 5-6 shows the light-emission coming from the source and drain, for different points during the experiment. One can see that the light emitted from the source side is much stronger than that emitted from the drain, suggesting the strong presence of cold-carrier recombination on the source side [28]. The main thing to note, however, is that initially, the light emission is mainly concentrated in the center of the width of the device (the center 30 $\mu$m). As the stressing proceeds, the light gradually spreads out to eventually cover the entire device width.

The light emission distribution of these pictures can be better analyzed by plotting the integrated light intensity along the width of the device for these various points. Since light was emitted from both the source and the drain, these two were separated and graphed separately. Fig. 5-7 shows the profile for the light distribution along the width (normalized to $I_D$) emitted from the

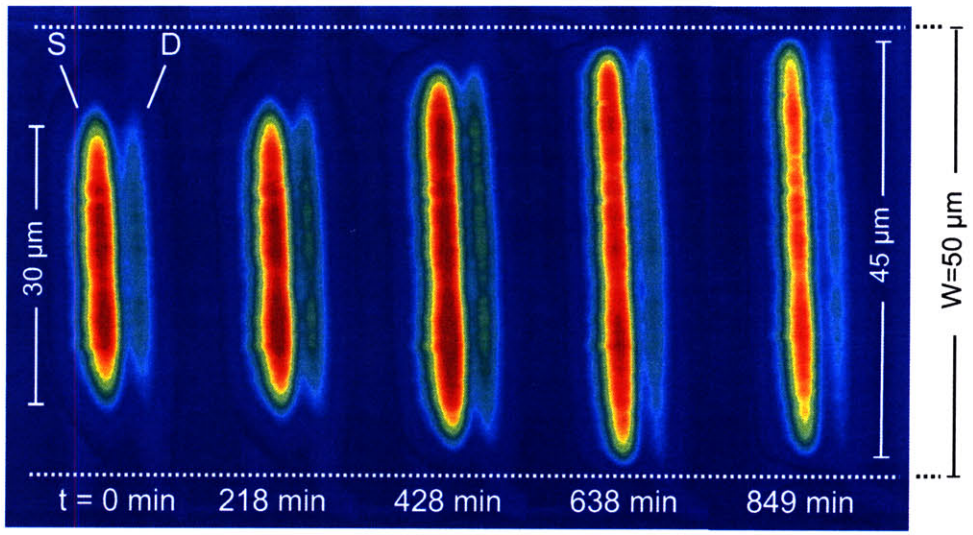
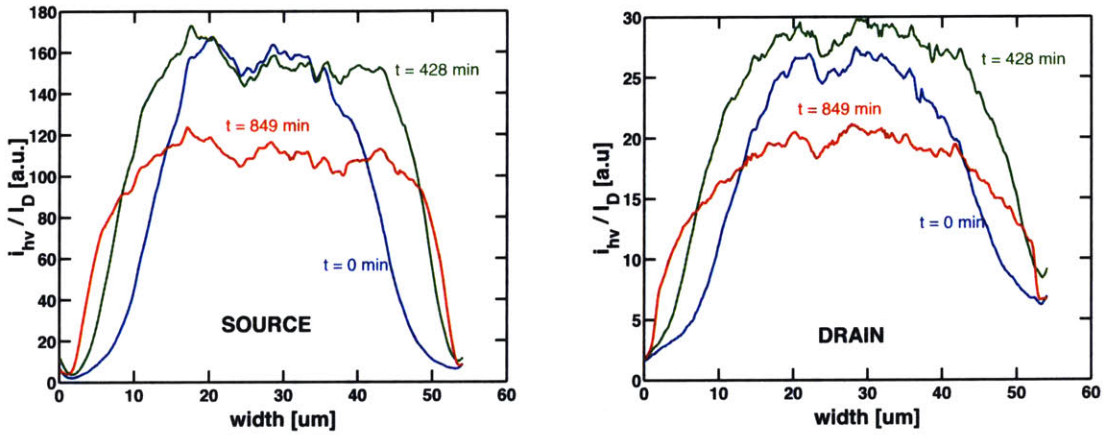



Figure 5-6: Photos of light emission from source and drain of standard-parameter PHEMT, at various points during the light emission experiment. Taken at $V_{GS} = 0.3$ V, $V_{DS} = 6.6$ V.

source (a) and drain (b) before, during, and after the experiment. From this one can see that in the first half of the experiment, the light emission just spreads out; in the second half, the main effect is an overall decrease in light intensity. This has an effect of an initial increase in the total light intensity (relative to $I_D$), followed by a steady decrease (as shown in Fig. 5-8 ). This suggests that, with stressing, the total impact-ionization initially increases (due to the width spreading) but then eventually decreases (due to the drain degradation). This is consistent with the $R_D$ degradation previously observed in Fig. 3-1(a): with stressing, $R_D$ initially decreases, but then steadily increases (which reduces the drain-gate electric field, and thus reduces impact-ionization, as shown in Fig. 3-6).

So far we have examined the light emission during the experiment at a fixed value of $V_{DS}$, which has basically allowed us to see the effects of stressing on the light emission distribution. We now turn to examine the light emission behavior during the stressing, at the actual stressing bias. This will hence give an indication of the distribution of the device degradation as it is actually happening. If we examine the light intensity at higher biases at later stages of stressing, we can




(a) (b)

Figure 5-7: Integrated light intensity (normalized to $I_D$) across width of standard-parameter PHEMT, at $V_{DS}$ = 6.6 V, for t = 0 (blue), t = 428 min (green), and t = 849 min (red).

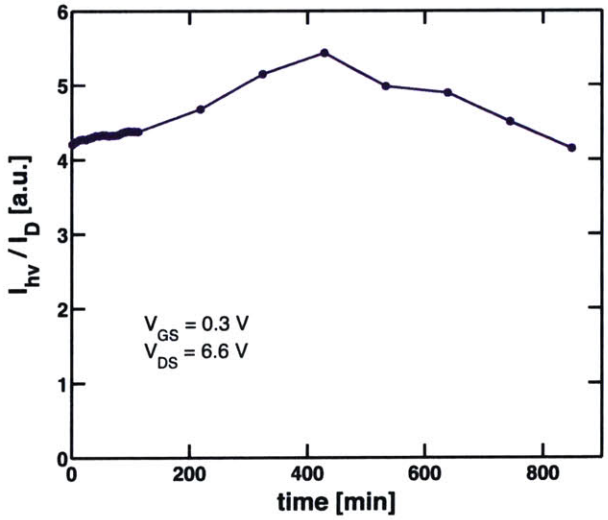



Figure 5-8: Total light intensity (normalized to $I_D$) vs. time (taken at $V_{DS}$) during light emission experiment on standard-parameter PHEMT.

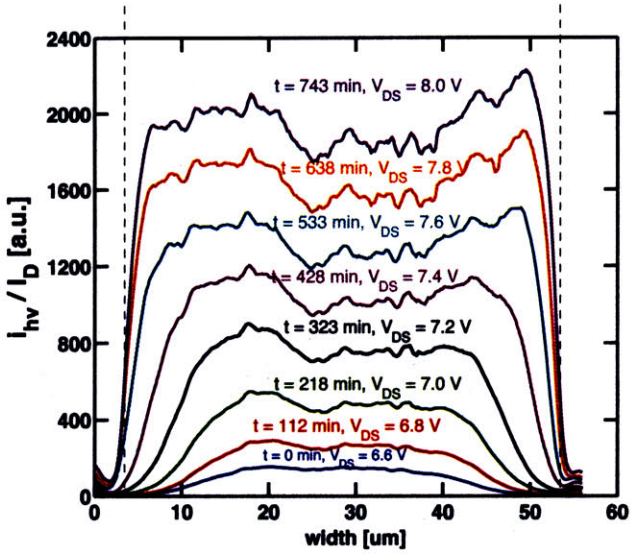



Figure 5-9: Light intensity (normalized to $I_D$) vs. device width, for light emitted from source side of device at various times during light-emission experiment, on a standard-parameter PHEMT. $W_g = 50\mu$m. Dotted black lines mark physical edges of device.

also that the light-intensity starts decreasing more in the center, thus concentrating towards the edges. Fig. 5-9 shows the light-emission profile along the width of the device, for the source side. The two dotted lines mark the location of the device edges. From this graph it is clear that as $V_{DS}$ is stepped up, the light intensity emitted from the source side increases and spreads out to cover the entire device width. One can also see here that for advanced stages of stressing (after $V_{DS} > 7.4$V), the light intensity in the center of the device has decreased so much that the profile becomes "peaked" at the edges of the device.

Fig. 5-10 shows the light-emission profile along the width for the drain side. Again, one can see here that as $V_{DS}$ is stepped up, the emitted light intensity increases and spreads out over the width. However the light emission from the drain is more uniform than that of the source (no major "peaks" form).

All these data suggests that under stressing, device degradation is proceeding in a non-uniform manner. The initial distribution of light-emission suggests that the impact-ionization rate on the drain side of the device is initially higher in the center of the device. As the device is stressed,

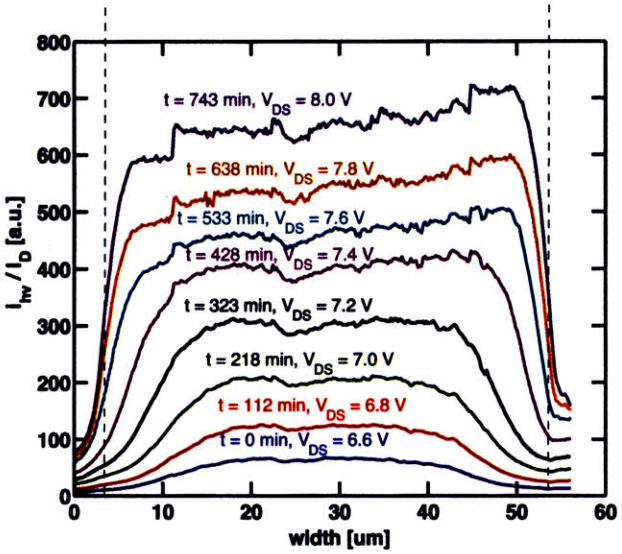



Figure 5-10: Light intensity (normalized to $I_D$) vs. device width, for light emitted from drain side of device at various times during light-emission experiment, on a standard-parameter PHEMT. $W_g = 50\mu$m. Dotted black lines mark physical edges of device.

the center degrades degrades faster than the edges, thus causing a reduction of impact-ionization (and light-emission) in the center. The non-uniformity in impact ionization rate can arise from three possible non-uniformities: drain current, electric field on the drain side of the device, or local temperature. Since there is a linear dependence between impact ionization and drain current, we can rule out non-uniformity in drain current as this would require the edges of the device to be virtually shut off. This would have a profound effect in the I-V characteristics of the device which is not observed. Similarly, since impact ionization in these devices has a negative temperature coefficient, impact ionization should be more prevalent on the *edges* of the device (which are expected to be cooler). This is inconsistent with our observations. Hence, we expect that the non-uniform pattern of impact ionization arises from a non-uniform electric field distribution on the drain side. This could easily occur as a result of a non-uniform recess geometry. In order to confirm this, materials analyses on the devices were performed. This is described in the next section.

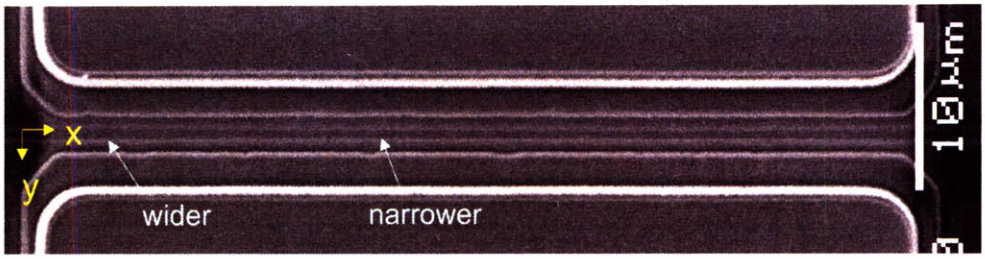



Figure 5-11: SEM micrograph of TLM ($L = 2.4\mu$m, $W = 60\mu$m) illustrating recess length variation across the device width.

## 5.4 Materials Analysis

In order to confirm the presence of a non-uniform recess geometry, we examined in detail the geometry of the n+ recess of TLMs ($L = 2.4\mu$m, $W = 60\mu$m) through AFM and SEM. An SEM micrograph of a typical TLM is shown in Fig. 5-11. Using the data from SEM and AFM, we can make fairly accurate measurements of the recess length across the width of the TLM. A typical result is graphed in Fig. 5-12, which clearly shows that the recess is longer at the edges and shorter in the center of the device. This non-uniformity produces a larger electric field at the center than at the edges, thus concentrating impact ionization towards the center of the device width. Since the PHEMTs are fabricated using the same process as the TLMs, and we observe analogous light-emission behavior in the TLMs, then it is likely that this same recess non-uniformity is present in the PHEMTs.

## 5.5 Summary

In our study of light-emission of PHEMTs during stressing, we observe a general pattern: initially, the light concentrates in the center of the device width, but then spreads out when undergoing high-bias stressing. After enough stressing, the light tends to decrease in intensity, and eventually becomes "peaked" at the edges. This behavior is remarkably similar to the light-emission behavior of the TLMs (refer to [17,23]), thus strongly suggesting that the same phenomenon is responsible in both cases.

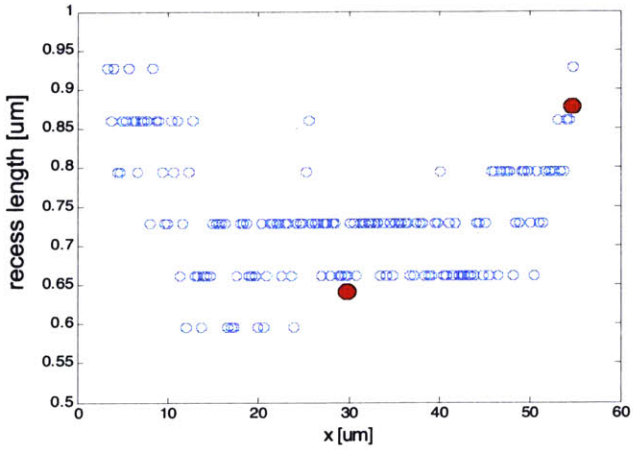



Figure 5-12: Length of n+ recess across width of TLM (from MATLAB analysis of SEM photograph). Marks in red show corresponding values from AFM measurements. $L = 2.4\mu$m, $W = 60\mu$m.

The origin of this non-uniformity in light-emission is attributed to a variation in the electric field along the width of the device. From our materials analyses on the TLMs, we observed that the recess width is actually narrower in the center than at the edges, thus causing the electric field to be higher in the center. This explains why initially, light-emission concentrates in the center, and why under stressing, the center tends to degrade faster, thus causing the intensity to decrease there and eventually peak at the edges.

These findings reveal a new and important dimension in the electrical reliability of PHEMTs - the uniformity of impact-ionization across the width of the device. Since excessive impact ionization can potentially have deleterious effects on device reliability, it is important to minimize any non-uniformities in the recess geometry that can give rise to non-uniformities in the electric field. This discovery should help develop fabrication processes that minimize impact-ionization-related electrical degradation in PHEMTs.

# Chapter 6

# Conclusions and Suggestions

## 6.1 Conclusions

In this work we have performed a comprehensive study of the electrical degradation mechanisms of GaAs RF power PHEMTs. Utilizing our stress and measurement setup we were able to effectively perform *in situ* monitoring of device degradation under electrical stressing. The general observations for our experiments indicated several different forms of degradation associated with the three regions of the device: the source, gate and drain. Further experiments and analyses investigating each form of degradation allowed us to formulate hypotheses for the underlying mechanisms. A cartoon summarizing all of the main forms of degradation identified in this thesis is shown in Fig. 6-1.

Concerning the drain side of the device, we observed an increase in $R_D$ and a decrease in $I_{max}$ under electrical stressing. These forms of degradation were of greatest concern as they potentially have deleterious effects on output power, as shown in [7]. In Chapter 3, the results of various experiments investigating the effects of stressing environment, bias voltage, bias current, and temperature on the degradation of $R_D$ and $I_{max}$ were discussed. Contrary to what is often claimed in the literature, our experiments indicated that these forms of degradation were *not* driven by impact-ionization or hot-electron effects. Instead, device temperature, the drain-gate electric field, and the stressing environment played strong roles in degradation, which suggested a corrosion

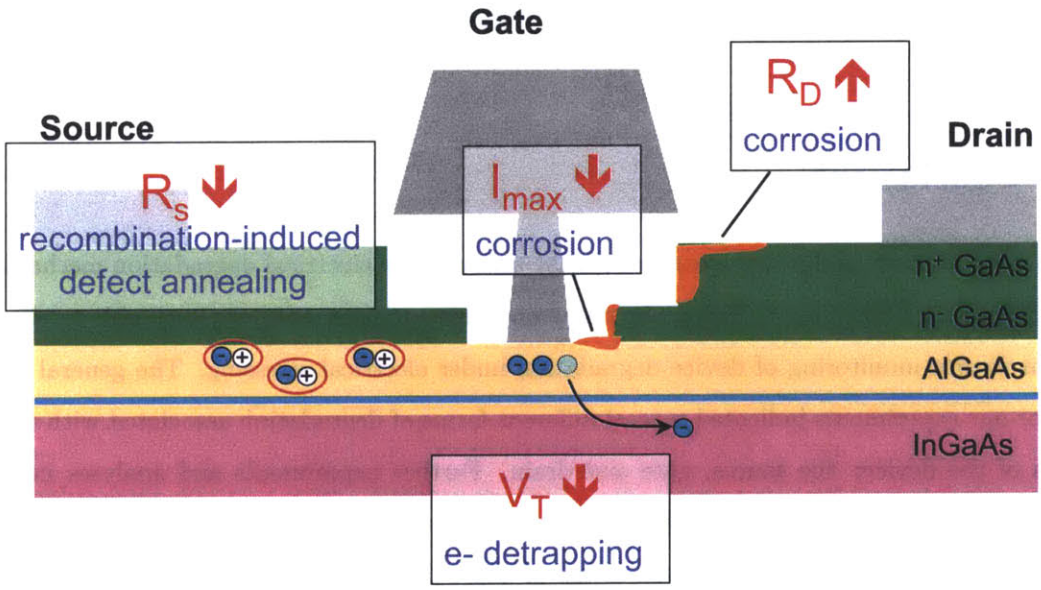



Figure 6-1: Schematic of top layers of a GaAs PHEMT, illustrating all the main forms of degradation that have been identified in this research.

mechanism on the drain side of the device. From STEM and EDX analysis, we were able to confirm that both the degradation of $R_D$ and $I_{max}$ were due corrosion on the drain side of the device, albeit at different locations. The increase of $R_D$ was correlated to corrosion on the corner of the n+GaAs cap, whereas the reduction of $I_{max}$ was correlated with corrosion on the exposed AlGaAs, closer to the gate. Whether the damage happened on the AlGaAs or the n+GaAs seemed closely related to the particular stressing conditions. Under high electric fields, the oxidation was more likely to occur on the AlGaAs; under high channel temperatures, the oxidation tends to happen mostly on the n+GaAs cap.

The proposed mechanism behind the corrosion involves the oxidation of Ga and As at the n+GaAs or AlGaAs surface (anode) and the reduction of oxygen at the gate metal (cathode). The rate of corrosion depends on the concentration of reactants (including oxygen and water) and the rate constant, which has an Arrhenius dependence. It was shown that the activation energy for the corrosion reaction is reduced with increasing drain-gate bias, via anodic polarization, which makes it easier for Ga and As to become oxidized. This mechanism of corrosion explains the dependences of of the degradation of $R_D$ and $I_{max}$ on stressing environment, temperature, and electric field.

In addition to the degradation of $R_D$ and $I_{max}$, in our experiments, other forms of degradation relating to the gate and source side of the device were observed: a negative shift in $V_T$ and a decrease in $R_S$. Although these forms of "degradation" seem to improve device characteristics and are thus of less concern than the degradation of $R_D$ and $I_{max}$, they do introduce changes in device characteristics to the extent that could potentially result in circuit malfunction. Thus, it was important to acknowledge their effects and understand the underlying mechanisms. In Chapter 4, the changes in $V_T$ and $R_S$ were discussed and mechanisms were proposed for each.

The negative shift in $V_T$ was found to be mostly recoverable with unbiased storage at room temperature, which suggested a mechanism involving some de-trapping of electrons under the gate. Initially, this was attributed to hot holes generated from impact-ionization neutralizing the trapped electrons, as described in [21]. However, later experiments investigating the effect of $L_{rd}$ and $V_{DGo} + V_T$ demonstrated that the negative shift in $V_T$ is actually correlated with the drain-gate electric field, and not impact ionization as previously thought. This allowed us to identify the

de-trapping mechanism as field-assisted tunneling of the electrons out of the traps, as discussed in [46]. Under bias stress, this de-trapping can be thermally activated, with an activation energy of $E_a = 0.42$ eV.

In contrast to the shift in $V_T$, the decrease in $R_S$ was *not* recoverable, which ruled out a similar de-trapping mechanism on the source side. With the exception of our previous work [17, 23], a permanent decrease in $R_S$ during electrical stressing was never previously reported for GaAs PHEMTs. From experiments investigating $L_{rd}$ and $V_{DGo} + V_T$, it was found that the change in $R_S$ was more correlated with impact-ionization that electric field. Also, it was noted the change in $R_S$ tended to "saturate" with time and high bias. Analysis of the temperature dependence gave an activation energy of $E_a = 0.19$ eV. All these findings were consistent with a mechanism of recombination-enhanced defect annealing on the source side, as described in [49]. Under electrical stressing, the recombination on the source side produced by impact-ionization gives energy to local defects, causing them to be annealed out. This in turn results in a higher carrier concentration $n_s$ on the source side, thereby reducing $R_S$. The change in $R_S$ saturates once all the defects are annealed out.

As suggested by Fig. 6-1, all of our stressing experiments described thus far have examined degradation in terms of the device cross-section (i.e. across the *length* of the device). This is how most HEMT reliability studies in the literature are conducted; device degradation is typically associated with specific regions pertaining to the device cross-section (e.g. ohmic contact, drain-gate access regions, etc). However, we recognized that it was also necessary to examine device degradation across the *width* of the device. In Chapter 5, we described our light-emission experiments performed on the PHEMTs, done in order to obtain a spatial picture of carrier recombination and electric field during stressing, and thus obtain a picture of degradation across the device width.

In our study of light-emission of PHEMTs during stressing, we observed a general pattern: initially, the light emitted from the device concentrates in the center of the device width, but then spreads out while undergoing high-bias stressing. Eventually the intensity of light in the center decreases, causing the light distribution to concentrate at the edges. This behavior was remarkably similar to the light-emission behavior of the TLMs (refer to [17, 23]), thus strongly suggesting that

the same phenomenon is responsible in both cases. The origin of this non-uniformity in light-emission was attributed to a variation in the electric field along the width of the device. From our materials analyses on the TLMs, we observed that the recess width is actually narrower in the center than at the edges, thus causing the electric field to be higher in the center. This explains why initially, light-emission concentrates in the center, and why under stressing, the center tends to degrade faster, thus causing the intensity to decrease there and eventually peak at the edges.

These findings revealed a new and important dimension in the electrical reliability of PHEMTs - the uniformity of electric field and impact-ionization across the *width* of the device. Since excessive impact ionization and high electric fields can potentially have deleterious effects on device reliability, it is important to identify and minimize any factors that can cause non-uniform electric fields across the device width.

## 6.2 Suggestions

After uncovering the various mechanisms behind the degradation, we are now in a position to suggest some possible remedies to alleviate them. First, we will discuss possible methods to prevent the degradation behind the increase in $R_D$ and decrease in $I_{max}$. Since corrosion is involved in both cases, the key to suppressing the degradation is to remove oxygen and water from the semiconductor surface, thus preventing any reactions from occurring. This could involve surface treatments prior to passivation that remove residual oxygen and water from the semiconductor surface. Also, the passivation layer itself could be somehow improved so that it provides better protection from the environment. For $SiO_x$ films, it has been reported that thicker and more compressive stress films and the incorporation of nitrogen and Si-H bonds in the film improve moisture resistance [50]. One could also consider using passivation materials other than $SiO_2$ (such as $SiN_x$) that may offer better barriers against ion diffusion, which would prevent corrosion. In [51], it was reported that $SiN_x$ passivation offers better resistance to moisture than $SiO_x$ films. However, if $SiN_x$ films are used, the PECVD deposition parameters (e.g. gas flux ratio, discharge frequency) must be carefully tailored in order to ensure a stable, moisture-resistant barrier [52]. Or, instead of PECVD, alternative

nitride deposition techniques (such as that described in [53]) may be implemented in order to deposit high-density nitride passivation layers, which should provide better hermeticity.

But even if such treatments or process modifications cannot be implemented, we have found another way to alleviate the corrosion degradation. As discussed in Sec. 3.4, it was discovered that unbiased storage at moderately high temperatures ($\sim 150 - 175°C$) prior to stressing tended to reduce the increase in $R_D$ and decrease in $I_{max}$ observed during stressing. This suggested that the heating tends to drive out residual oxygen and/or moisture away from the semiconductor surface (possibly due to increased diffusion at higher temperatures). Therefore, heating could possibly be employed in this manner to prevent future degradation. However, in implementing this treatment, caution must be taken as to not employ temperatures so high that other thermally-activated forms of degradation are introduced (e.g. gate sinking, ohmic contact degradation).

Because the negative shift in $V_T$ involves the de-trapping of electrons that is driven by electric field, the only way to mitigate this change under electrical stressing is to eliminate the formation of traps in the first place. However, since the change in $V_T$ is mostly recoverable with unbiased storage at room temperature, and does not have as deleterious effects on $P_{out}$, there is not too much concern in addressing this effect. The decrease in $R_S$ is also not of major concern, but as it is a permanent effect it may be more easily addressed. A more thorough "burn-in" which exhausts this decrease could be implemented, such that $R_S$ will remain more or less stabilized upon further stressing. This could possibly be done by biasing the device at high drain current ($\sim$ 450 mA/mm) for a short period of time ($\sim$ 5 minutes). However, caution must be taken since during this period of stressing, $R_D$ will begin to increase. Thus the conditions for this source burn-in must be carefully chosen as to exhaust the decrease in $R_S$ as much as possible but minimize any degradation introduced to $R_D$.

Regarding non-uniformities in degradation across the width of the device, it is important to minimize any non-uniformities in the recess geometry which will introduce non-uniformities in electric field distribution. During device fabrication, process steps must be modified to ensure uniform etching across the entire width of the device. This should result in more uniform distribution of electric field, which should help improve device reliability.

## 6.3 Future Work

Although in this work we have identified a number of physical mechanisms behind degradation in GaAs PHEMTs, there are still a few issues that could use further investigation. As mentioned in the previous section, improvements to device passivation should help in preventing corrosion of the semiconductor surface. Thus, a thorough investigation into improved deposition methods and/or alternate dielectric materials for higher-density, more impermeable passivation layers would be a good topic for future research.

Also, the work in this thesis focused on the gradual (non-catastrophic) degradation of PHEMTs under electrical stress. However, as the issue of catastrophic burnout is also of serious concern in PHEMT reliability, it is important to understand the mechanisms involved there as well. Studies investigating the underlying causes of device burnout in GaAs PHEMTs should help to further improve overall electrical reliability.

# Appendix A

# Extraction of Thermal Resistance

As mentioned in Sec. 3.5.1, in order to estimate the channel temperature of a PHEMT under specific biasing conditions, an estimate of the thermal resistance of the device is required. Thus the thermal resistances of the PHEMTs studied were extracted by comparing pulsed I-V characteristics to static (DC) I-V characteristics. Theoretical values for the thermal resistance using analytical formulas were also calculated.

## A.1 Experimental Measurements

As discussed in [54], measurements performed on a very short time scale (pulsed measurements) eliminate the effect of self-heating. As a result, for pulsed I-V curves, the channel temperature is approximately constant (independent of bias point), as it is only determined by the power dissipation at the quiescent bias point [55]. In the case of where pulsed I-V measurements are taken from a quiescent bias point of zero power dissipation (as in all of our measurements described here), the channel temperature is simply equal to the ambient temperature [56]:

$$T_{ch} = T_{amb} \tag{A.1}$$

This is in contrast to regular DC I-V measurements, where the channel temperature varies

according to the power dissipation of the specific bias point, as per Eq. 3.1 (repeated here for convenience):

$$T_{ch} = T_{amb} + P_{diss}\theta_{jc} \tag{A.2}$$

One can usually assume that at points of same $V_{GS}$ and $V_{DS}$ where two I-V curves share the same current value, the device has roughly the same channel temperature [57]. Thus, one can use the point of intersection of a pulsed I-V curve to the DC curve to determine $T_{ch}$ for that given bias point. This allows the thermal resistance to be extracted via Eq. A.2.

In order to perform pulsed I-V measurements, a setup different from the one described in Sec. 2.2 was necessary. We implemented two different types of pulsed-measurement setups: one setup to pulse the gate, and another to pulse the drain. The former setup and the measured data will be discussed first. This setup is similar to that described in [58]. Fig. A-1 shows a diagram of this setup. The device is probed on a Cascade Microtech probe station, using Picoprobe GSG 150 microwave probes. A Windows PC controls the oscilloscope (Tektronix TDS 640A), the pulse generator (Agilent 33250A) and the power supply (Agilent E3631A) via GPIB commands in MATLAB. The chuck temperature was controlled via a Temptronix temperature controller.

Using this setup, pulsed measurements were performed by applying a pulse to the gate of the device and measuring the response at the drain with the oscilloscope. The gate was pulsed from $V_{GS} = -0.6$V (near the pinch-off region) to a moderate positive voltage (e.g. $V_{GS} = 0.4$ V). A pulse width of 2 $\mu$s with a period of 1 ms was typically used (duty cycle = 0.2 %). As a result, during measurements the device was normally off (with zero power dissipation), except for during the short pulses.

A typical output (drain) pulse in response to the input (gate) pulse is shown in Fig. A-2. Here, $V_{DD}$ is held at 3 V and $V_{GS}$ is pulsed from $-0.6$ V to 0.4 V (not shown). From this graph one can see that initially the drain voltage is at $V_{DS} = V_{DD} = 3$ V, since the device is initially off and therefore there is no voltage drop across the load resistor. However, once the gate is turned on, $V_{DS}$ drops to about 0.6 V and stays there for the duration of the pulse ($2\mu$s). This is a result of the voltage drop induced by the drain current drawn through the load resistor. Using reverse load-line

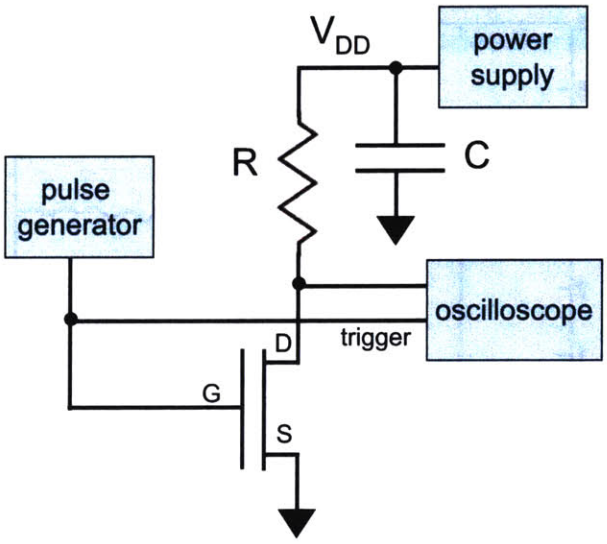



Figure A-1: Diagram of measurement setup for applying pulse to gate of transistor. $R = 47\Omega$, $C = 0.1\mu F$

analysis, one can then calculate the drain current for this value of $V_{DS}$. For this particular output pulse, the change in $V_{DS}$ was 2.428 V, which gives $I_D = 51.7$ mA.

In this manner, one can implement different values of $V_{DD}$ and obtain the corresponding $I_D$ for different values of $V_{DS}$. Thus by sweeping over a range of $V_{DD}$, one can generate a pulsed I-V curve for a given value of $V_{GS}$. Using this method, pulsed I-V curves as well as DC I-V curves could be measured. For the DC measurements, a very long pulse width (700$\mu$s) and period (1 ms) were used, such that the self-heating had enough time to take effect.

Fig. A-3 shows the DC I-V curves measured at 25°C, along with pulsed I-V curves taken at various ambient temperatures, for $V_{GS} = 0.4$ V. As one can see, the pulsed I-V curves intersect with the DC curves at different points, depending on ambient temperature. As the ambient temperature increases, the pulsed curves tend to intersect with the DC curve at points corresponding to higher power dissipation levels.

In comparing pulsed curves with DC curves, one would expect that, for a given temperature, the pulsed data to give *higher* current levels than the DC data. However, one should note that

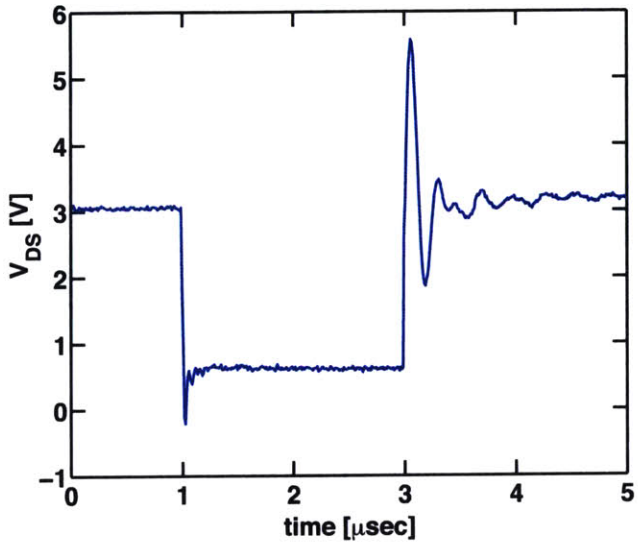



Figure A-2: Trace of drain voltage as measured by oscilloscope, as pulse was applied to gate. $V_{DD} = 3.0$ V, $V_{GS}$ pulsed from $-0.6$ V to 0.4 V. $W_g = 160\mu$m.

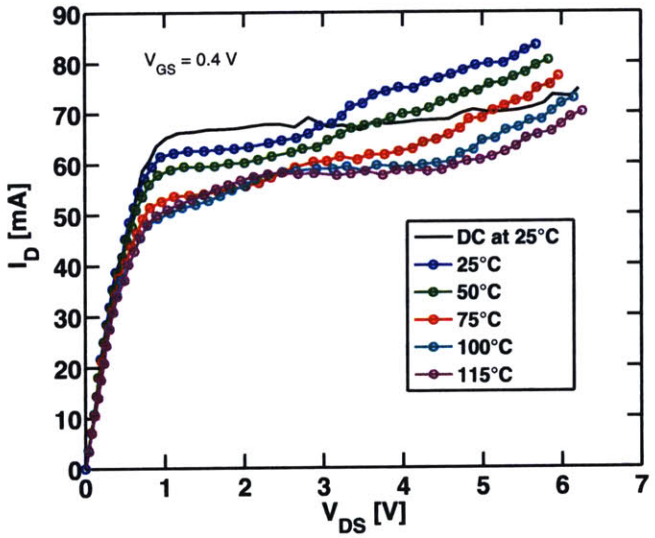



Figure A-3: DC I-V curve (at 25°C) and pulsed I-V curves taken at 25, 50, 75, 100, 115°C for $V_{GS} = 0.4$V ($V_{GS}$ pulsed from $-0.6$ V to 0.4 V). $W_g = 160\mu$m.

for the pulsed measurements shown in Fig. A-3, the drain currents for the pulsed measurements are actually lower, at least for lower $V_{DS}$ values (compare pulsed data with DC data at 25°C). The problem here seems to be the effect of current collapse for the pulsed measurements, as seen previously in [47]. This is likely due to delays caused by trapping at surface-states on the gate-drain access region, which tend to form a negatively-charged parasitic gate, as described in [59]. Unfortunately, due to the presence of these effects on the drain current, one cannot extract accurate value of the thermal resistance.

So in an attempt to work around this problem, a different setup was created, where a pulse was applied to the drain instead of the gate. This setup is shown schematically in Fig. A-4. Here, the bias on the gate was maintained by the power supply, whereas the bias on the drain was controlled via the pulse generator ($V_{DS} = V_{pulse} - I_D R$). The pulse generator was pulsed from zero ($V_{pulse} = V_{DS} = 0$) to a positive voltage, while the gate bias was kept constant. A trace of $V_{pulse}$ and corresponding $V_{DS}$ are shown in Fig. A-5. Here, $V_{GS}$ is kept constant at 0.3 V, while $V_{pulse}$ is pulsed from 0 V to 2.37 V. This causes the drain bias to go from 0 V to 1.1 V. Using reverse load-line analysis, one can calculate the drain current as $I_D = 27.27$ mA.

Similar to what was done previously with the pulsed-gate measurements, a pulsed I-V curve can be obtained by varying the high-level value of $V_{pulse}$. Fig. A-6 shows the DC I-V curves measured at 25°C, along with pulsed I-V curves taken at various ambient temperatures, for $V_{GS} = 0.3$ V, on a device of $W_g = 160\mu$m. As one can see, the effect of current collapse is not present here; for 25°C, the current for the pulsed data is higher than the DC data, which is what we would expect. And as the ambient temperature increases, the current for the pulsed data steadily decreases, which makes sense. Unfortunately, the data is more noisy in this case, likely due to inaccuracies caused by ringing and oscillations, in both the DC and pulsed measurements. However, one can still use this data to approximate the channel temperature, as the pulsed data give an indication of the channel temperature of the DC data. By focusing on the data at higher $V_{DS}$ ($V_{DS} > 3$ V), one can gather that the channel temperature of the DC curve at high $V_{DS}$ is close to 80°C. Since the last five data points of the DC and pulsed data tend to overlap with one another the most, the point of intersection is chosen at $V_{DS} = 4.32$ V (shown as circled in figure), which corresponds to

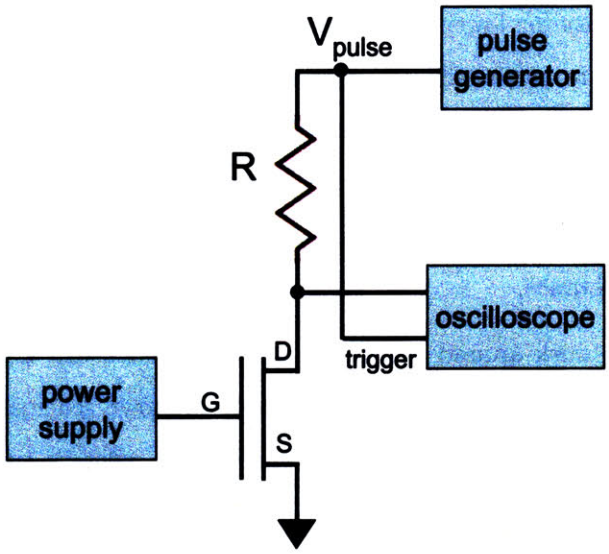



Figure A-4: Diagram of measurement setup for applying pulse to drain of transistor. $R = 47\Omega$.

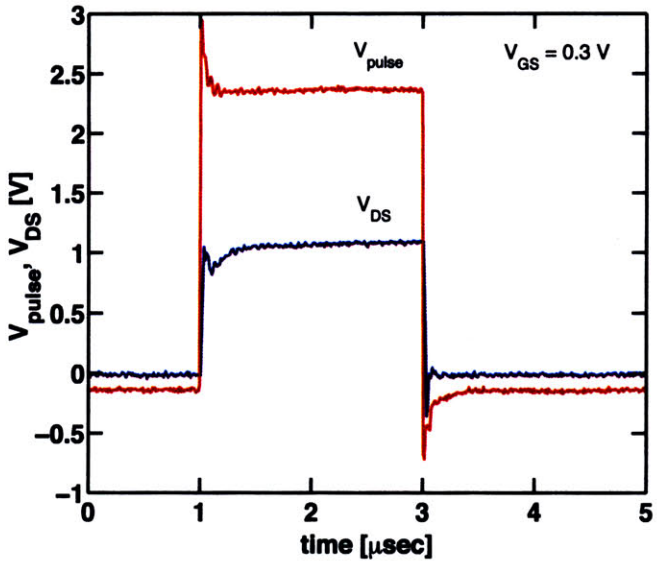



Figure A-5: Trace of pulsed voltage ($V_{pulse}$) and corresponding drain voltage ($V_{DS}$) as measured by oscilloscope, for pulsed-drain measurement. $V_{GS}$= 0.3 V, $V_{pulse}$ pulsed from 0 V to 2.37 V. $W_g = 160\mu$m.

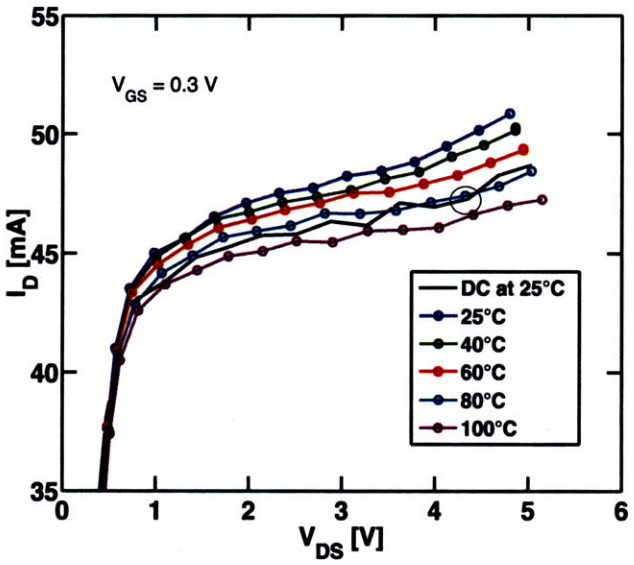



Figure A-6: DC I-V curve (at 25°C) and pulsed I-V curves taken at 25, 40, 60, 80, 100°C for $V_{GS} = 0.3$ V ($V_{DS}$ pulsed from 0 to about 5 V). $W_g = 160\mu$m.

a power dissipation of 0.205 W. So if we assume this point has 80°C, then by Eq. A.2 this gives $\theta_{jc} = 269$°C/W.

However, rather than just assuming this value of $\theta_{jc}$ for all of our experiments, we need to take into account for its dependence on temperature. First of all, one must note that for GaAs, the thermal conductivity $\kappa$ decreases with temperature as per the following equation [32]:

$$\kappa(T) = \kappa_{ref} \left( \frac{T}{T_{ref}} \right)^{-\alpha} \tag{A.3}$$

Note that all temperatures are in Kelvins. For GaAs, $\alpha = 1.25$ [32]. Since the thermal resistance is inversely proportional to the thermal conductivity, then the thermal resistance will increase with temperature. This dependence can thus be written as [32]:

$$\theta_{jc}(T_{amb}) = \theta_{jc,ref} \left( \frac{T_{amb}}{T_{amb,ref}} \right)^{\alpha} \tag{A.4}$$

However, this just covers the dependence of $\theta_{jc}$ on the *ambient* temperature. One must also

| $T_{amb}$ [°C] | $\theta_{jc,0}(T_{amb})$ [°C/W] |
|---|---|
| 25 | 241 |
| 30 | 246 |
| 35 | 251 |
| 40 | 256 |
| 50 | 266 |

Table A.1: Calculated values of $\theta_{jc}$ at zero power dissipation, for various ambient temperatures. For devices of $W_g = 160\mu$m.

consider that, due to self-heating, a device under test will have an even higher temperature than the ambient temperature, which will increase $\theta_{jc}$ even more [32]. Thus $\theta_{jc}$ is not only a function of ambient temperature, but of the dissipated power as well. These dependences are somewhat complicated, but after linearizing some dependences as described in [32,60] one can approximate the channel temperature as a function of ambient temperature and power dissipation by the following equation:

$$T_{ch} = T_{amb}\left(1 + \frac{(1-\alpha)P_{diss}\theta_{jc,0}(T_{amb})}{T_{amb}}\right)^{\frac{1}{1-\alpha}} \tag{A.5}$$

Here $\theta_{jc,0}$ is the thermal resistance at zero power dissipation. With this equation, one can then calculate the thermal resistance at the channel temperature as $\theta_{jc}(P_{diss}, T_{amb}) = (T_{ch} - T_{amb})/P_{diss}$. So mentioned previously, from our calculations we had obtained $\theta_{jc} = 269$°C/W, for $T_{ch} = 80$°C and $P_{diss} = 0.205$ W. Inverting Eq. A.5, we can solve for $\theta_{jc,0}$ at $T_{amb} = 25$°C, which gives 241°C/W. One can now use this value in Eq. A.5 for future calculations of $T_{ch}$ for experiments done at ambient temperatures of 25°C. For conditions employing different ambient temperatures, Eq. A.4 is first used to calculate $\theta_{jc,0}$ for that specific ambient temperature. Table A.1 illustrates the values of $\theta_{jc,0}$ extracted for a variety of ambient temperatures. These values and the average power dissipation during stressing are used in Eq. A.5 to calculate $T_{ch}$ for specific stressing experiments.

Also, it should be mentioned that $\theta_{jc}$ depends on device width, so all the values shown so far are only valid for experiments on $W_g = 160\mu$m devices. Separate pulsed measurements need to be performed for devices of different widths. To obtain the thermal resistance of devices of

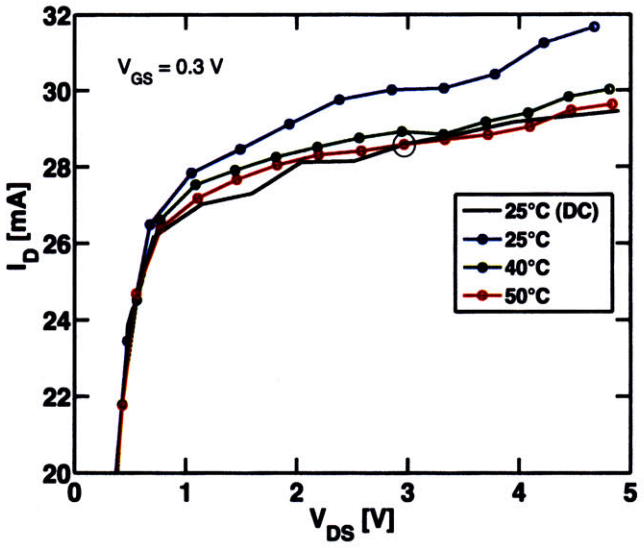



Figure A-7: DC I-V curve (at 25°C) and pulsed I-V curves taken at 25, 40, 50°C for $V_{GS} = 0.3$ V ($V_{DS}$ pulsed from 0 to about 5 V). $W_g = 100\mu$m.

width $W_g = 100\mu$m, pulsed measurements were performed on these devices as well. Fig. A-7 shows the DC and pulsed I-V curves measured for a $W_g = 100\mu$m device, where a pulse was applied to the drain and the gate was held constant $V_{GS} = 0.3$ V. From this graph, one can note that due to the narrower width, the currents were significantly smaller, thus making the data a bit harder to analyze for these devices. However, from the clear overlap of the DC data with the pulsed data taken at 50°C, it does appear that that channel temperature for the DC curve in the saturation regime must be around 50°C. The intersection point was selected at moderate $V_{DS}$ ($V_{DS} = 3.0$ V), corresponding to a power dissipation of $P_{diss} = 0.0846$ W. The extracted thermal resistance at this point is 295°C/W, which gives $\theta_{jc,0} = 281$°C/W, for zero power dissipation (at $T_{amb} = 25$°C). And as mentioned previously, $\theta_{jc,0}$ varies with ambient temperature so for different ambient temperatures, $\theta_{jc,0}$ must be calculated per Eq. A.4. Table A.2 shows the values of $\theta_{jc,0}$ extracted for a few ambient temperatures.

| $T_{amb}$ [°C] | $\theta_{jc,0}(T_{amb})$ [°C/W] |
|---|---|
| 25 | 281 |
| 50 | 311 |
| 75 | 341 |

Table A.2: Calculated values of $\theta_{jc}$ at zero power dissipation, for various ambient temperatures. For devices of $W_g = 100\mu$m.

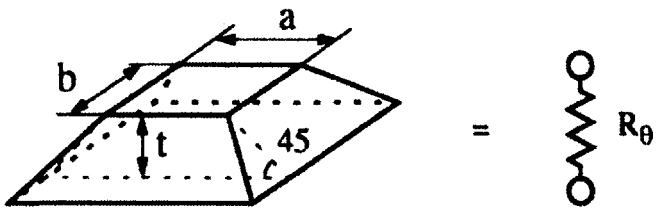



Figure A-8: Basic model for theoretical calculation of thermal resistance. Heat source is upper rectangle of dimensions $a \times b$, and $t$ is the thickness. From [61].

## A.2 Theoretical Calculations

The thermal resistance of devices can also be calculated based on analytical equations for heat flow from a device. Fig. A-8 shows the model used to calculate thermal resistance in this manner. The rectangle at the top is the heat source with dimensions of $a \times b$, and the thickness is $t$. The thermal resistance $R_\theta$ of that region can be thus calculated from the following equation [61]:

$$R_\theta = \frac{1}{\kappa}\int_0^t \frac{1}{(a+2x)(b+2x)}dx \tag{A.6}$$

$$= \frac{1}{\kappa}\frac{1}{2(a-b)}\ln\left\{\frac{a(b+2t)}{b(a+2t)}\right\} \tag{A.7}$$

Here, $\kappa$ is the thermal conductivity of GaAs at room temperature (0.46 W/cm°C). Fig. A-9 shows the model for calculating the thermal resistance of a multi-fingered device. As one can see, in this model there are two regions, one thin one near the device surface (Region 1) and a thicker one extending up to the backside of the chip (Region 2). One can then think of the total thermal resistance as the total thermal resistance for Region 1 (thermal resistance of each finger in parallel

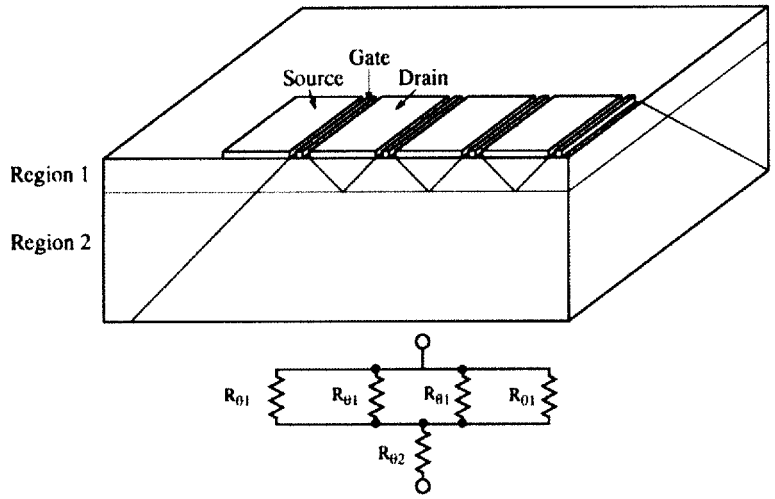



Figure A-9: Model for theoretical calculation of thermal resistance, illustrating multi-fingered device and regions for calculating individual thermal resistance values. From [61].

with on another) plus the thermal resistance of Region 2. Putting in all the device dimensions (e.g. unit finger width, number of fingers, substrate thickness, etc), one can thus calculate the overall $\theta_{jc}$ for the device.

Based on these calculations, the thermal resistance for a $W_g = 160\mu$m device (4 fingers of $40\mu$m each) is estimated to be $\theta_{jc} = 254°$C/W (at room temperature). This is in good agreement with the value extracted from experiments (as described in previous section) of $\theta_{jc,0} = 241°$C/W (for zero power dissipation, at room temperature). For devices of $W_g = 100\mu$m (2 fingers of $50\mu$m each), the thermal resistance calculations yield a value of 365°C/W, which is somewhat higher than the experimental value of 281°C/W. However, from [62], we know that the accuracy of the theoretical calculations tends to increase for smaller devices. Thus for our calculations of $T_{ch}$ in this thesis, we have used the thermal resistance values extracted from the experimental measurements (values in Table A.1 and Table A.2), along with Eq. A.5.

## A.3 Summary

For the purposes of extracting the thermal resistance of our PHEMTs, we have performed both experimental measurements and theoretical calculations. For the experimental measurements, we have implemented two different pulse-measurement setups to obtain pulsed I-V characteristics. The first consisted of applying a pulse to the gate and measuring the response on the drain. However, the measurements obtained from this setup exhibited the problem of current collapse, and thus could not really be used to extract the thermal resistance. So a second setup was created where the gate bias was kept constant, and a pulse was applied to the drain through a load resistor. The pulsed and DC I-V curves obtained from measurements using this setup were compared and thermal resistances were extracted. Although both the pulsed and DC data are somewhat noisy, the data was able to nonetheless give a reasonable estimate for the thermal resistance in our devices. The values of thermal resistance obtained experimentally are in reasonable agreement with calculated theoretical values. In this thesis, for calculations of channel temperature, the thermal resistances extracted from experimental measurements were used, while taking into account the dependences on ambient temperature and power dissipation.

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## Biographical note

Anita Villanueva was born in Lima, Peru on May 17, 1978. In August of 1981, at the age of three, she and her parents moved to the United States and settled in Cleveland, Ohio. In the summer of 1987 she and her family then moved to Santa Rosa, California, where she lived until the fall of 1996, when she began attending University of California, Berkeley. There she double-majored in Electrical Engineering & Computer Science and Materials Science & Engineering, and graduated with a B.S. in December of 2000. In September of 2001 she began graduate school at the Massachusetts Institute of Technology in the Department of Electrical Engineering & Computer Science, in Jesus del Alamo's research group. She obtained her S.M. degree in May 2003 on GaAs PHEMT reliability.

During her six years in graduate school, Anita participated in many extra-curricular activities. From July 2002 to May 2004 she was very active in the student government of her current dorm (Sidney-Pacific Graduate Community), where she was in charge of various publicity and communications efforts.

Anita is also an avid fan of long-distance running, and managed to complete 3 half-marathons (among other road races) during her tenure at MIT. In November 2004, she began marathon training with the Leukemia & Lymphoma Society, in an effort to raise funds for blood cancer research. In April 2005 she ran the Boston Marathon and succeeded in raising over $4,000 for this cause.

During graduate school Anita also took the opportunity to learn the Japanese language, taking six semesters of study at MIT. She participated in the MIT Japan Program and spent the summer of 2005 in Itami, Japan as an intern for Mitsubishi Electric. After completing the language classes she continued self-study in Japanese and participated in the MIT Japanese Lunch Table meetings.

And probably of most importance, in March 2005 Anita met the love of her life, Joe Pacheco, Jr (PhD '04). They became engaged in March 2006, and are to be wed in October 2007 in San Antonio, Texas.